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MICRO-OPTICAL TOMOGRAPHY

A DISSERTATION

SUBMITTED TO THE GRADUATE FACULTY

in partial fulfillment of the requirements for the

degree of

DOCTOR OF PHILOSOPHY

BY

ALBERT DURR EDGAR

1978

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MICRO-OPTICAL TOMOGRAPHY

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"Our Father which art in heaven, Hallowed be Thy name." To Jesus Christ, the highest honors. Also in the place of special honor I name my parents Albert C. and Clarine E.M. Edgar, and my bride Shirley.

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ABSTRACT

The quest for deeper vision has inspired a colorful chapter in man's development. From the time Leeuwenhock first opened the microworld to man's wondering, ever deeper vision has brought valuable treasures to light. This thesis defines micro-optical tomography, a new concept in microscopy allowing a deeper vision than is possible with an optical microscope, giving much of the depth clarity of an electron microscope without requiring the vacuum, dehydrated, lifeless environment of electron microscopy. Thus living cells can be viewed and life dynamics visualized. This is accomplished by digitizing an image from an optical microscope while focus and viewing angle are scanned to form a multi-dimensional image matrix. Where the power of optical transforms end, sequential scanning and the computer are used to reconstruct the wealth of detail born by light emanating from the subject. Reconstruction can take the form of optical dissection, or of imaging a dimensional object with elemental detail to 1/4 the wavelength of light in all planes of focus on one image.

Micro-optical tomography, with its principles and techniques, forms the major new technology claimed for this thesis. An available parts budget of about $1,500 definitely precluded purchase of required equipment at current prices, therefore the research portion of the thesis advances the state of the art to make a future system at the

university practical. This research includes the FOCUS number system and design of a low cost photographic quality digital image scanner.

The FOCUS microcomputer number system software provides in a 16-bit word the nature and accuracy of an 18-bit floating-point representation. In less time than would be required to write operands to a hypothetical infinitely fast arithmetic unit and read the result, the FOCUS software alone in an 8-bit 8080 microprocessor performs 16-bit arithmetic, including addition, subtraction, multiplication, and division, with overflow trapping and optimal roundoff, and without special hardware. FOCUS software permits a bare microcomputer to replace a more costly computer in many speed critical signal processing applications such as digital audio processing and micro-optical tomography. A package of 15 arithmetic, decisional, and decimal IO routines in 3 FOCUS versions, plus an inexpensive analog/FOCUS conversion circuit, together with in-depth mathematical analysis, are presented as a completed, tested system.

The digital image scanner is designed to be a general purpose research tool capable of inputting and outputting very high quality images in black and white or color. A special feature is a powerfully general yet simple command set permitting special techniques such as derastorization, hexagonal sampling, typesetting, phosphor correction, etc., to be implemented in software. To support the command set, many novel ideas are incorporated. For example there is a method of integrating an analog signal arbitrarily varying over many orders of magnitude for a time interval independently also varying over many orders of magnitude, with alternate applications to RMS measuring and voltage-variable low-pass filtering. There is a method of phosphor granularity correction for laser-scan gray-scale quality, mathematical analysis of the effect of differential nonlinearity on image noise, a unique approach to tricolor sensing, and other concepts whose usefulness transcends the present system. The primary contribution of this section is the design of a high-quality digital image processor that is affordable by a small business or an individual.

CHAPTER I

MICRO-OPTICAL TOMOGRAPHY

Quest for Deeper Vision

From Leewenhoeks's microscope and Lippershey's telescope through television and the electron microscope, advances in man's ability to see have illuminated exciting new vistas in science. The life sciences especially are intimately coupled to the ability to see the very small, and new technology of the latter opens new concepts in the former. The current state of the art of microvision is divided between two technologies. The optical microscope is the workhorse of biology, providing full color viewing of almost any material that can be mounted on a slide. However extreme narrowness of depth clarity has limited the optical microscope primarily to viewing thin slices of a specimen rather than viewing microscopic objects in full perspective as we might imagine a mythical ameoba might see his world. The scanning electron microscope has given us dimensional views of the micro-world with extreme clarity, often producing images of haunting beauty and profound significance. However the vacuum requirement and the corollary dehydration seriously limit what we can observe. We can not look into the workings of a cell, but rather must separate the parts and let them dry first. Most tissues can not be viewed as they are in life. The light of the electron will never let us see the micro-world in its natural color.

If it were possible to combine the desirable traits of both technologies, biology would have an extremely powerful new tool. Light waves emanating from a specimen bear information about all optically accessible detail down to a spatial wavelength equal to half the wavelength of light in the medium surrounding the specimen. It is frustrating that present technology has no means of simultaneously reconstructing this wealth of optical information to form the whole specimen image with a clarity even approaching the theoretical limit. It should be emphasized that light bears much richer information than is now used, providing information about all planes of focus simultaneously, with linear separability between elements, and with elemental clarity several times greater than allowed by present technology.

The objective of this research is to apply microcomputer image reconstruction techniques analogous to those used in tomography, operating on data derived from a dynamically changing optical system under computer control, to utilize more fully the richness of optical information, thus providing with light, in full color, in natural atmospheric or aqueous environment:

1. Useable magnifications to 3000 X in visible light, combined with
2. Unlimited depth of focus for viewing dimensional objects in living perspective, and
3. Ability to optically dissect a transparent specimen like a cell to view parts without disturbing larger interrelations.

Current Technology

Depth of focus has been extended beyond conventional limits in microscopy and also in a commercial 8mm movie camera by "integrated focusing" in which the focus is changed, with a special objective that prevents image size change during focus, during exposure. The result is a very soft image with, however, some fine detail from several planes. An important modification of this technique projects the illuminating light in a plane which is moved with the plane of focus, however this is primarily limited to opaque, convex objects with no concave pockets, and is also limited to very low N.A. objectives, or a very narrow viewing field, as it is theoretically impossible to obtain a beam of light one wavelength thick over a distance much wider than one wavelength. By working with extremely short De Broglie waves, the scanning electron microscope allows a N.A. of typically .005, equivalent in depth to a photograph of a plant or animal 2 feet from a 35mm camera with a normal 50mm focal length lens at f8, explaining the depth clarity obtainable with this instrument. However because most biological specimens are composed of large percentages of water, the requirement of a vacuum introduces seriously limiting considerations. Also an electron microscope will never "see" in natural color.

Flying spot scanning optical microscopes have been built, and are used primarily for counting and size classification of objects such as dust or blood cells. No mention has been found of computer controlled dynamic focusing. The field of microscopy is fast changing. At a time when the scanning electron microscope is only a little over a decade old, a newer invention - the microcomputer - places us within range of a new revolution of the optical microscope in viewing dimensional biological specimens.

Micro-optical tomography's namesake, x-ray tomography, shares the same goals of mathematically dissecting a subject. However beyond similar goals and etymology from the Greek root "tomos" = "a cutting", the means are dissimilar. Classical tomography uses a moving source and film to introduce a limited depth of field to the normally infinite depth x-ray system, the reverse of micro-optical tomography. Computer-aided-tomography (CAT) mathematically dissects a subject from a set of views at different angles. Because opaque reflection imaging and the critically limiting optical features of diffraction and focus do not exist in macro x-ray work, fundamentally different reconstruction algorithms are needed.

Principles of Micro-Optical Tomography

The wave front at the microscope objective is a transform of the specimen, containing all detail down to half the wavelength of light in spatial wavelength and a quarter of the wavelength of light in pixel size from all points of the subject. The functional transform performed by an objective lens is capable only of recreating detail in a narrow plane, and even then with serious attenuation of high spatial frequencies. However if images from many incremental focus displacements are arranged in a three-dimensional image matrix, it is mathematically possible to inverse-transform the matrix by convolving with the inverse transform of the three-dimensional "blurring function" of the lens subject to certain constraints, for example, for a spatial wavelength $< \lambda_0/N.A.$ in planes parallel to the lens and a more complex relation in other planes. Such a three-dimensional blurring function is

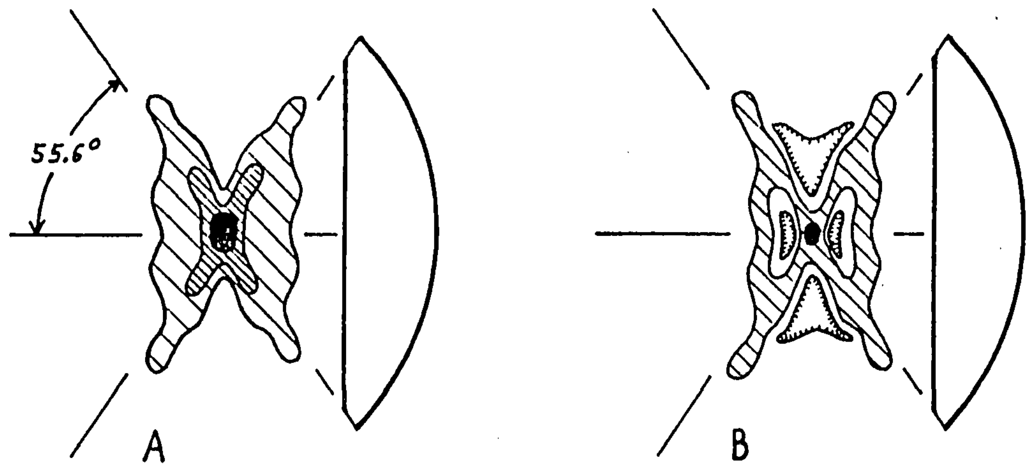


Figure 1.1 Three Dimensional Blurring Function and Reconstruction

represented in figure 1.1A, with the angle of acceptance that of a 1.25 N.A. objective in oil. This figure portrays:

1. The small core of best focus confining the highest spatial frequencies,
2. Bright rings circling the disk of a defocused point, transforming a slightly defocused point of light into an apparant ring with a dark center, and
3. Double cone shape of the region of sensitivity distant from the plane of focus, preventing a unique reconstruction of the third dimension without scanning the viewing angle as well as focus.

An impulse response of the corrected image is represented in figure 1.1B.

An exact reconstruction of the image within diffraction limits is not possible in the third dimenstion (perpendicular to the lens) with the dynamic-focus-generated data only, which resembles classical tomography. For example, consider an infinite sheet of transparent colored material near the image plane. An observer can not detect its position, as its effect is independent of the focus setting of the objective. However when extending depth of focus, a unique reconstruction of the third dimension is not needed, and dynamic focus alone is mathematically sufficient. When optical dissection of a specimen element is desired, the third dimensional frequency elements near the diffraction limit are fortunately reconstructable from dynamic focus data. To visualize this, note that a very small piece of the colored sheet could be reconstructed from dynamic focus data by using boundary conditions. The lower spatial frequency elements are reconstructable from an angular scan performed on the principle of single objective stereo microscopy, which provides data resembling that of computer aided x-ray tomography. This is visualized by noting that the infinite colored sheet would appear denser when viewed from an angle closer to the plane of the sheet, and thus could be located.

A three-dimensional image matrix is horrendous to contemplate; fortunately many simplifications are possible, such as used in the closed-form single-pass ART algorithm which reduces the computation time and relieves memory of mass storage in computer x-ray tomography.

For most work, only several image planes need be stored, and will be used in a block manner adaptable to sequential storage devices such as a disk drive. Other dynamically changing corrector images need only be stored with low resolution so as to fit in active memory.

Depth of field extension, as opposed to image dissection, is easily performed. A basic procedure could use a pattern recognition type program to detect correct focus, much as would a human observer, by noting a peaking of the ratio of high to low spatial frequency components. The detected area of focus can then be added to the image being formed. Omnipresent noise in all other non-focus planes would not be added.

Several complications arise. An effect well known to microscopists is the ability to view "through" small opaque objects. Actually the large N.A. of the microscope objectives allow the microscopist to view around the object on all sides. This transparency is not desirable when all objects can be focused simultaneously. It can be obviated by scanning from the back of the specimen to the front, allowing each detected area of focus to overwrite a posterior image. As a further complication, a bright defocused object will spill visually sharp rings considerably beyond its boundaries which could interfere with detection of focus. Fortunately the rings have distinguishing features that can be used to detect their presence instead of a true image. First, their visual position changes as a function of focus, while that of a focused image does not. Second, although they may appear visually "sharp", i.e. "contrasty" at middle spatial frequencies, they lack the highest spatial frequencies. The difference between "sharp" and "high resolution" is well known among photographers, and is easily detected mathematically. An object behind another can not cast these rings over an opaque object in front when the plane of focus intersects the front object. The converse effect can be cancelled as each object is brought into focus by use of a retained low-resolution depth-of-find matrix. A new area affects adjacent previously found areas as a function of lateral distance and relative depth between areas of focus.

A stereo microscope using micro-optical tomography is easily formed in software. Two separate image matrices are allocated. As focus scans from back to front, the position of each new image plane is biased linearly to the left for one matrix and to the right for the other. The transparency effect and overwrite procedure presented above would form two separate views of the specimen at apparently different angles. Conventional stereo microscopy uses two objectives or one objective optically divided into two. Diffraction is thus at least doubled. Requiring reasonable stereo difference angles and depth of field limits present-art stereo microscopy to very low magnifications. Conversely, the stereo micro-optical tomographic algorithm outlined above can use a maximum, full objective field for each image, for a dramatic advance in the state of the art.

Image Quality

Next let us consider what effective image clarity is possible from micro-optical tomography. Consider a typical situation in which an observation is normally made with a .65 numerical aperture objective. The spatial response of the lens transform at optimum focus is plotted in figure 1.2A which, for a full field illumination, may be derived from the overlap of the aperture disk at various displacements, corresponding to the ability of the lens to encompass both the direct and diffracted rays of a given spatial frequency. Note that a grating with spatial wavelength half that of light would diffract light 180^{o}, resulting in the fringe limit for a lens covering a 180^{o} cone of light, and also the fringe limit of light as a transform, because nothing can

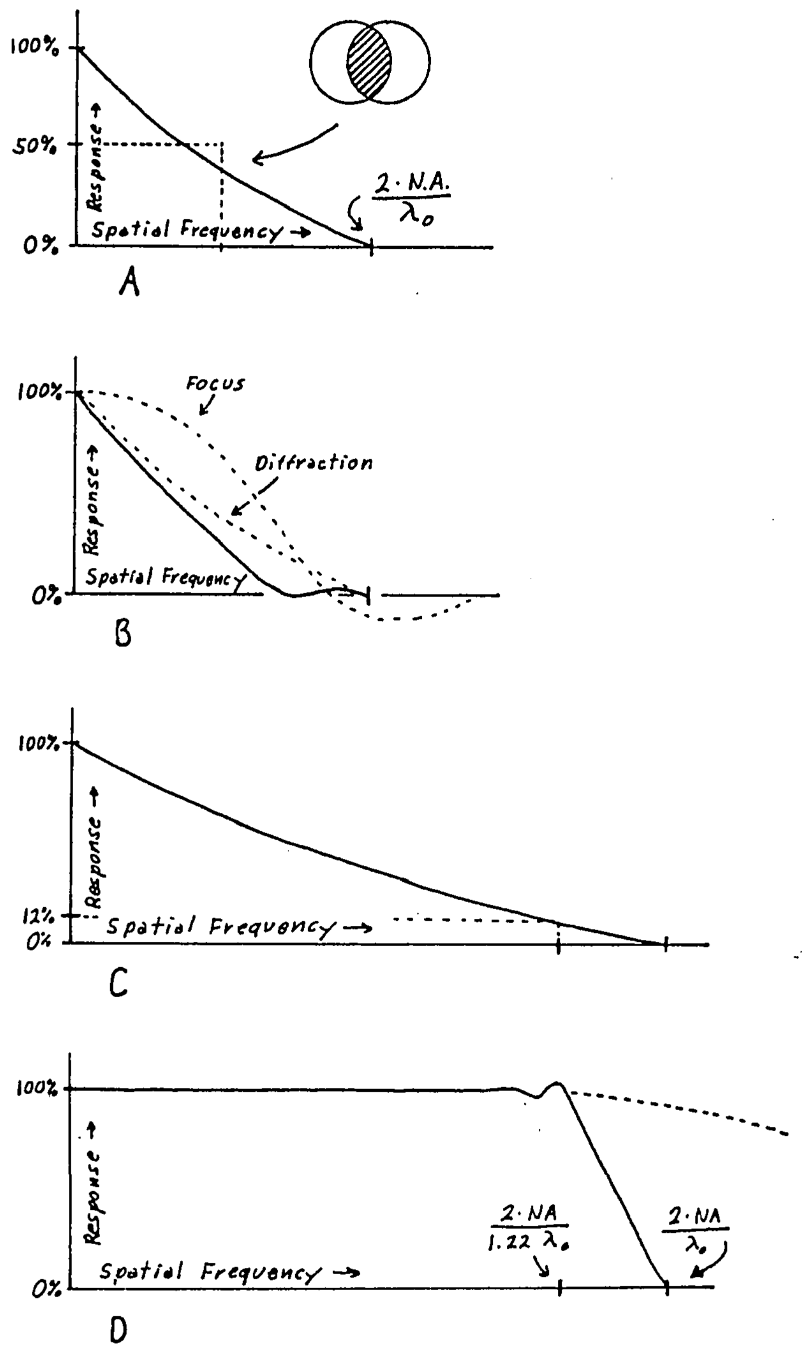


Figure 1.2 Modulation Transfer Functions

be redirected by more than 180°, modulo 360°. The modulation transfer function of a small N.A., focused, optically perfect lens in monochromatic, omnidirectional light, was calculated from disk overlap. Let s = spatial frequency normalized so $s = 1 = \lambda_c$. $0 \leq s \leq 1$. Then:

$$\text{M.T.F.} = 1 - \frac{2}{\pi}\cdot\left[s\cdot\sqrt{1 - s^2} + \sin^{-1}(s)\right]$$

Assume the microscopist chose the common .65 N.A. lens for maximum detail, indicating that a smaller aperture would reduce resolution by diffraction, and a larger one by depth of focus considerations. Thus a typical point on the object is blurred by an optimum balance of these two factors, represented in figure 1.2B. The M.T.F. near cutoff is higher than would be expected from convolving the diffraction and focus aberrations. Near cutoff, only the edges of the objective are able to encompass both the direct and diffracted rays. By forming the image with only the periphery of the lens, the defocus effects, arising from phase differences at different radial distances from the lens axis, are lessened.

When using micro-optical tomography there will be no depth of focus blurring effects, allowing direct use of a 1.25 N.A. (or higher) immersion objective, with response shown in figure 1.2C.

Assuming the data has a good signal to noise ratio, the high spatial frequences may be boosted, as shown in figure 1.2D. In this figure the dotted response assumes nonlinear harmonic estimation for the sole purpose of filtering image fringes. This is advisable because the normal Fraunhofer diffraction transforming an impulse into an Airy disk produces fringing that is substantially accentuated to form distracting effects approaching a two-dimensional sinc function, such as that obtained with point source lighting, and similar to but more severe than "Mackie lines" in some early photographs. One of several criterion for generating nonlinear estimation of frequencies beyond the diffraction limit is presented. Let:

REAL = real world image we attempt to recover

HAVE = image we have recorded = REAL + blurring and/or noise

TEST = a reconstructed image which is to be tested for quality

P(TEST) = probability TEST can be a real world image

P(TEST | HAVE) = probability TEST is the real world image given HAVE

P(HAVE | TEST) = probability blurring and/or noise would transform TEST into HAVE

We wish to find a TEST such that

P(TEST | HAVE)

is maximized, i.e. find a TEST with the highest probability of representing REAL. An alternative integrates each TEST times its probability. Using Bayes' theorem the above becomes:

$$P(\text{TEST} \mid \text{HAVE}) = \frac{P(\text{HAVE} \mid \text{TEST}) \cdot P(\text{TEST})}{P(\text{HAVE})} \propto P(\text{HAVE} \mid \text{TEST}) \cdot P(\text{TEST})$$

which, given a set of assumptions of the real world, blurring, and noise characteristics, can be directly calculated for any given TEST reconstruction. Finding a TEST that maximizes this function in the presence of noise has been the subject of research by others in the field. Linear frequency reconstruction maximizes the Bayes' formula for the false assumption that the real world image is gaussian, like "snow" on an empty television channel. This false assumption permits distracting fringe effects that an observer, with a priori knowledge of the real world, knows are not present at all specimen boundaries. Proposed future research would give the system "knowledge" that a true image is composed of edges with step size PDF logarithmically distributed. Unlike other fringe-suppressing algorithms proposed in the literature, the Bayes' approach would have no effect on known spatial frequencies in the absence of noise, rather would only estimate those beyond the diffraction limit. This could not claim to extend the diffraction limit, however it would make spatial frequencies near the limit more visually useful, and produce images with optimum RMS correlation to the true image. The dotted response in figure 1.2D is not included in subsequent calculations.

Various methods of quantifying image clarity based on M.T.F. (modulation transfer functions such as in figure 1.2) agree that in the absence of noise, and with magnification sufficient to avoid visual limitations, the area under the transfer function is a good specification of image clarity. Comparing figures 1.2B and 1.2D, the clarity improvement with micro-optical tomography is found as:

$$\frac{\text{Area of 1.2D}}{\text{Area of 1.2B}} = \text{effects from (N.A.} \cdot \text{Depth} \cdot \text{Enhancement)}$$

$$= \frac{1.25}{.65} \cdot \sqrt{2} \cdot \frac{.85}{.45} = 5.13$$

Thus for a typical subject we expect a five-fold increase in image clarity over present art microscopy. For comparison, imagine a 3 inch mask over a 15 inch TV to represent present technology, and the entire TV image to represent the image that is possible.

It is interesting to note that the Rayleigh resolution limit is

$$\frac{1.22 \cdot \lambda_o}{2 \cdot N.A.}$$

even though the ultimate limit is a spatial wavelength of

$$\frac{\lambda_o}{2 \cdot N.A.}$$

allowing independent sampling points as close as

$$\frac{\lambda_o}{4 \cdot N.A.}$$

With the low noise system presented, a maximum amplitude boost of ten fold is reasonable at a spatial frequency of F_{cutoff} / 1.22, allowing two dots at the Rayleigh separation to be observed completely separate with no overlap of "bridge" between the dots. Also of interest, it has been shown that for a small bounded object, such as a chromosome in a neutral field, it is theoretically possible to reconstruct detail arbitrarily far beyond the classical diffraction limit. This can be investigated, however even with the very low noise system, substantial gains beyond the classical limit are not anticipated because of extreme demands on data noise, linearity, and fidelity.

A typical 133 dot lithographic half-tone screen used for publication can resolve to 133/2 line pairs per inch or 133/(2·25.4) = 2.62 line pairs per millimeter before aliasing. Next, assuming a 1.25 N.A. objective used with 550 nm (yellowish green) light, the spatial cutoff frequency is

$$\frac{2 \cdot 1.25}{\lambda_o} = 4.55 \cdot 10^3 \ \frac{\text{line pairs}}{\text{millimeter}}$$

We plan to hold 100% transfer to

$$\frac{\text{maximum frequency}}{1.22} = 3.73 \cdot 10^3 \ \frac{\text{line pairs}}{\text{millimeter}}$$

thus suggesting a magnification of $\frac{3.73 \cdot 10^3}{2.62} = 1{,}424$ X. At this magnification, as far as the lithographic process is concerned, the resolution could have been infinite with no improvement in the finished plate. Conversely, the lithographic process will materially reduce the quality of the micrographic image. When screening an image, diffraction limitations are intentionally introduced to avoid aliasing. A magnification of 3000 X will still give the clarity of a typical "sharp" non-micrograph published picture.

CHAPTER II

THEORETICAL ASPECTS OF THE FOCUS MICROCOMPUTER NUMBER SYSTEM

Introduction

FOCUS is a number system and supporting software especially useful for microcomputer control and other signal processing applications. FOCUS has the wide ranging character of floating-point numbers with a uniformity of state distributions that give FOCUS approximately a four-fold accuracy advantage over an equal word length floating-point system. FOCUS computations are typically five times faster than equal word length single precision fixed-point or integer arithmetic for a mixture of operations, comparable with hardware arithmetic in speed for many applications. Algorithms for 8-bit and two versions of 16-bit FOCUS are included.

Sophistication of requirements in systems design has pressed digital systems into real-time signal processing. In addition to the usual software techniques, many hardware techniques are actively pursued. Besides, methods of representing a quantity and critical peripheral information, such as significant arithmetic, unnormalized arithmetic, error estimation in computer calculation, etc., are of vital concern in this field. This thesis presents a digital number system providing speed and accuracy for digital signal processing using a microcomputer.

Many digital control systems should respond qualitatively strong to gross errors between the output and control signal, but should respond quantitatively delicate as equilibrium is approached. The latter requirement often demands a minimum of 12 to 16-bit fixed-point systems to avoid chatter caused by quantum jumping near quiescence even though most of the resulting thousands of states are wasted in providing fractional parts-per-thousand control of the corrective force when there is a large error in the system being controlled. A much more efficient number system would focus available states near zero in analogy to the "virtual ground" of an operational amplifier or in analogy to the human eye which concentrates available resolution near a "center of focus" while retaining cognizance of distance states. The number system presented does allocate available states in this fashion, thus suggesting its name.

If there is time, a computer has an inherent ability to respond to the environment with an heuristic and complex nature that cannot be matched in analog form. The number system presented provides the speed required for a clearer focus of the complexities of the system environment and its control, thus again suggesting its name.

As an introduction to the FOCUS system, its abilities are now specified using numbers and statements that will be supported as the concept is developed.

An 8-bit FOCUS word provides the range and resolution in a fairly large area around and including zero of a 15 7/8 -bit fixed-point word. Compared to the logarithmically uniform FOCUS, a floating-point representation seems "out of focus" with typically one bit less efficiency based on RMS fractional error, two bits less based on peak fractional error, and further accuracy losses in computation. With the FOCUS coding a single 8-bit byte is in serious contention for non-trivial applications, providing bipolar operation with a 2½ % RMS fractional error over a range of 60,000 to 1 either side of zero. For comparison, 8-bit FOCUS gives less audible distortion of a signal than would transcription on a cassette tape recorder. 16-bit FOCUS 10.10 fulfills the requirements of most precision signal processing applications, providing 0.06 % RMS fractional error over a range of 32 orders of magnitude for positive and negative numbers, equivalent to an 18-bit floating point system.

Unlike floating-point software that gives accuracy at the expense of speed, the special feature of FOCUS is accuracy with speed. Compared with a uniform mixture of add, subtract, multiply, and divide, and with 8-bit fixed-point computations performed on a popular microprocessor, 16-bit FOCUS programs execute 3 times faster. This is not a fair number however because the fixed-point algorithms used for comparison do not fix up overflow, and the fixed-point software multiply and divide are only for positive numbers. When overflow fix-up and 4 quadrant ability are removed also from the FOCUS program, the 8-bit FOCUS executes 10 times faster than the 8-bit fixed-point.

Binary Representation

FOCUS programs use a logarithmic number coding in which, like floating-point, an exponent is stored, but unlike floating-point, no mantissa is given. Rather the exponent is a fixed-point number with a fractional part. Both the number and the exponent have signs which could be represented in sign-magnitude, offset binary, or one's or two's complement for 16 possible combinations. The combination of sign-magnitude for the number and offset binary for the exponent sign is found to be optimum from a computational viewpoint, and so is used for FOCUS programs. The same choice was used in the 26th reference to produce very fast ROM based hardware, limited to 12-bit or smaller words.

Two Bytes → FEDCBA98 76543210

FOCUS.16 Format → F EDCBA9.876543210

Corresponding Equation → $F \cdot 10^{EDCBA9.876543210}$

Sign Bit
"0" = positive
"1" = negative

Remaining 15 bits hold the base-10 logarithm of the absoluted value of the number plus an offset:
0 100000.000000000
with the binary point fixed as shown

Figure 2.1 FOCUS.16 Format

The formatting used in FOCUS.16 programs is given above. Sample words using this format are translated below:

$0\ 100000.000000000 = +10^{0} = 1$

$1\ 100001.000000000 = -10^{1} = -10$

$0\ 011111.000000000 = +10^{-1} = 0.1$

$0\ 100000.100000000 = +10^{.5} \simeq 3.16$

$0\ 111111.111111111 \simeq +10^{+32}$

$1\ 000000.000000000 = -10^{-32}$

Formats used in other FOCUS programs are shown below:

Program	Representation of Unity	Bits	Fraction bits	Log Base
FOCUS 10.10	0 10000.0000000000	16	10	10
FOCUS.16	0 100000.000000000	16	9	10
FOCUS.8	0 1000.000	8	3	2

Table 2.1 FOCUS Formats

Analog to FOCUS Conversion

General Considerations

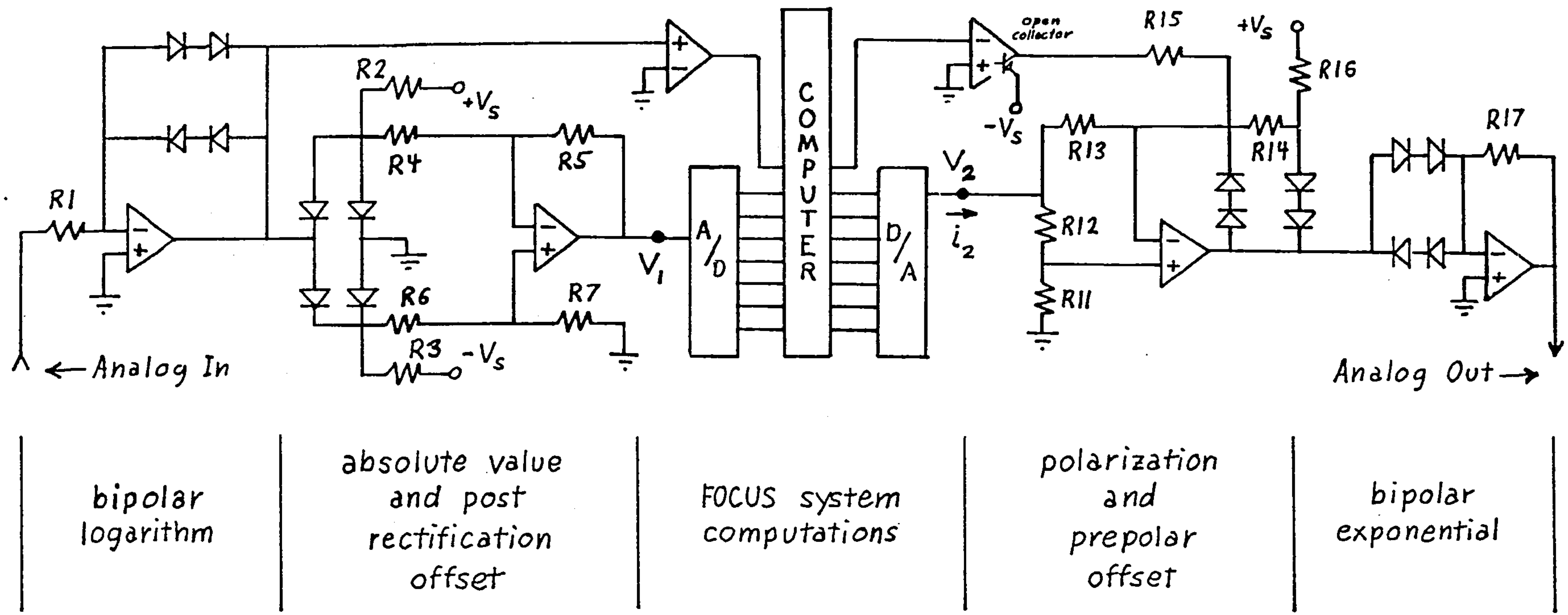
This section discusses the interface of an analog signal with FOCUS binary formatting. Translation of the signal while in analog form allows the characteristic resolution and range of FOCUS to be retained with fixed-point digital converters of reasonable bit size. Thus, although FOCUS.8 spans nearly five orders of magnitude, only 7-bit fixed-point converters are needed with the proposed circuit. 12-bit fixed-point converters service the 16-bit FOCUS format over a continuous bipolar range of eight orders of magnitude from 1 microvolt to $\pm$ 100 volts.

There are several methods of translating an analog signal into logarithmic form. It is possible to selectively multiply, rather than add, a constant associated with each bit, or construct a converter using several linear segment approximations of a logarithmic curve, or derive the logarithm and exponential functions in analog circuitry using diode or transistor characteristics, then use conventional linear converters. The last approach is chosen as combining accuracy, economy, and availability.

The circuit shown in Fig. 2.2 provides bipolar FOCUS conversion and reconversion. It features an arrangement permitting few, inexpensive parts without compromising accuracy. In the converting circuit, the logarithm is obtained initially in bipolar form to avoid the unpredictable gains or dead-bands for small signals associated with absolute-value-first circuitry. A novel single amplifier arrangement then derives the absolute value without operational-amplifier flopping over a dead-band at zero transition. The temperature dependence and voltage offset of the absolute-value section balances that of the bi-polar logarithm section. In the reconversion circuit a diode switch is used to eliminate FET switches, thus allowing low impedance, stable circuitry with inexpensive operational amplifiers. The temperature drift and voltage offset of the diode switch compensates that of the exponentiating circuit. The sign is reinserted with a circuit requiring only a single operational amplifier and a single-pole, single-throw diode switch, while at the same time compensating for the voltage offset of the exponentiator with either polarity. A set of typical component values for the circuit is indicated. This circuit has been built and its operation verified with parts costing under $4, excluding the digital section.

Because FOCUS has special accuracy near virtual ground with special capacity for wide dynamic excursions with lesser accuracy, it is often desirable to perform subtraction of differential input signals in analog form and to perform output integration in analog form, both in analogy to the functioning of a differential input internally stabilized operational amplifier.

In audio processing frequency pre-emphasis can be used with a minimum of concern for overranging. A dynamic expander-contractor is not needed as this feature is inherent in the logarithmic FOCUS coding. For image processing the desirable logarithmic response is automatic, an extra converter is not needed. The software difficulties of a logarithmic imaging system will be obviated.



TYPICAL VALUES

R1 = R17 = 2.0K	R4 = 6.2K	R7 = 30K	R13 = R14 = 6.8K
R2 = 33K	R5 = 33K	R11 = 910 Ω	R15 = 22K
R3 = 56K	R6 = 5.6K	R12 = 1.8K	R16 = 43K

Figure 2.2 Analog / FOCUS Conversion Circuit

Design Equations

Unexpected complications in analyzing the circuit of Figure 2.2 are condensed into design equations to aid the reader attempting to use the circuit. Let:

V_M = maximum input or output voltage (10V typical)

I_M = logarithmic diode current at V_M (5 ma typical)

V_R = reference input or output voltage corresponding to FOCUS number 1

I_R = logarithmic diode current of V_R (1/3 ma typical)

V_D = diode voltage at I_R (.5V typical)

V_S = source voltage. Must be constant, possibly zener stabilized, because V_S multiplies effective input (15V or 12V typical)

The input section is designed:

$R1 = V_M/I_M$

R5/R4 = gain from two diodes to A/D converter. example: for two series .1V/decade diodes, $\pm$2.5V A/D and FOCUS.8 with $10^{4.78}$ range, required gain = 5.23.

$R2/K = R3 \cdot K = V_S/I_R$

where $K \geq 1$. Unity gives average I_R in both diodes.

$$\frac{R6 + R7}{R3 + R6 + R7} > \frac{V_D}{V_S} \text{ and } \frac{R4}{R2} > \frac{1.8\ V_D}{V_S}$$

inequality should be by more than a factor of 2 for uniform I_R with sign transition.

$R4 \geq R6$ and $R5 \geq R7$.

equality gives equal biasing.

$R4/R5 = R6/R7$

The output section is designed:

$R17 = R1$

$R12 = 2 \cdot R11$

$R13 = R14$

Other combinations of R12/R11 and R13/R14 are possible. Those presented optimally compromise distortion and noise.

$R12 \approx R13$ for bi-polared averaged bias null

$$(R11 + R12) \,||\, (R13 \cdot \frac{R11 + R12}{R12}) = Z_{in}$$

$$Z_{in} = \frac{3}{4} R12 \text{ if } R12 = R13 = R14 = 2 \cdot R11$$

$\frac{R11}{R11 + R12}$ = gain of section from V_2 to dual diodes, $= \frac{1}{3}$ with given ratios. Choose Z_{in} for proper gain. For current output D/A one may add a resistor to reduce Z_{in} between V_2 and ground or decrease R11 and R12 while keeping their ratio constant. With a voltage output D/A one may wish to add a series resistor.

$$R16 = \frac{V_S - 2\,V_D}{I_R}$$

$$R15 = R16 \,||\, \frac{V_S - 2\,V_D}{4\,V_D} \cdot R14$$

$$\frac{R16}{R14} < \frac{V_S - 2\,V_D}{4\,V_D} \text{ for reference uniformity.}$$

Matched log-conformance transistors in a diode arrangement can replace the diodes, and thermistor networks can replace key resistors.

Trimming

Make adjustments in the order given to minimize readjustment. The input section is trimmed:

1. Null input op-amp at zero signal.

2. Input $+V_R \cdot 10$ and $+V_R/10$, adjust R5 so FOCUS number varies over 100:1.

3. Input $-V_R \cdot 10$ and $-V_R/10$, adjust R7 so FOCUS number varies over 100:1.

4. Input $+V_R$, adjust R1 for a FOCUS number of 1 (V_1 = 0V) R2 and R3 have reciprocal effects.

5. Input $-V_R$. If FOCUS number is not -1 (V_1 = 0) connect a high resistance from sign output (or buffered output) to appropriate + or - input terminal of second op-amp. If buffered through inverting gate, substitute $-V_R$ in step 4, $+V_R$ in step 5.

The output section is trimmed:

11. Output FOCUS number +1 ($V_2 = i_2 = 0$), adjust R16 for V_R volts out.

12. Output FOCUS number -1 ($V_2 = i_2 = 0$), adjust R15 for $-V_R$ volts out.

13. Output FOCUS numbers +10, +1/10, -10, and -1/10. Average ratio should be between 30:1 to 300:1. Else adjust series or parallel input resistor if included, or if not, R11 and R12 together.

14. Output FOCUS numbers -10 and -1/10, adjust R11 for output ratio of 100:1.

15. Output FOCUS numbers +10 and +1/10, adjust R14 for output voltage ratio of 100:1.

Arithmetic

Addition and Subtraction

The vital feature of the FOCUS programs is the ability to perform general calculations and to perform them rapidly. This hinges on the ability to perform addition directly in the logarithmic domain.

A theoretically possible but impractical method of addition would be to use a two dimensional lookup table. 16-bit addition using this method would require over four billion words of memory. Another theoretical possibility would be to use two 64K word arrays to translate back and forth between the linear and logarithmic domains. However such a system would execute slowly and increase computational error with two stages of roundoff.

The FOCUS addition/subtraction algorithm does use a lookup table, but requires only 2305 8-bit half word bytes for FOCUS.16, and 256 bytes for FOCUS.8. Execution is extremely fast, requiring only a single memory reference, sign test, and two binary additions when adding two positive FOCUS numbers. All answers materialize rounded to the nearest available state for the minimum possible computation error.

The basic addition algorithm for two positive numbers is now presented. Let X, Y, and Z be the FOCUS coded numbers representing the real world values X', Y', and Z', i.e.:

$$X = \log_2(X') + \text{offset}$$

$$Y = \log_2(Y') + \text{offset}$$

and the sum

$$Z = \log_2(X' + Y') + \text{offset}$$

We wish to find the FOCUS coded sum Z from X and Y with no reference to the real world values X' and Y'. To do this, the following operation is performed:

$$Z = X + F(X - Y)$$

The addition and subtraction are standard binary operations. F(N) is a one dimensional lookup table which is precalculated according to the formula derived below:

$$Z = \log_2(X' + Y') = X + F(X - Y)$$

$$X' + Y' = 2^{X + F(X - Y)}$$

$$2^X + 2^Y = 2^X \cdot 2^{F(X - Y)}$$

$$1 + \frac{2^Y}{2^X} = 2^{F(X - Y)}$$

$$\log_2(1 + 2^{Y-X}) = F(X - Y)$$

$$\log_2(1 + 2^{-N}) = F(N)$$

The offsets in X and Y cancel in the subtraction, leaving N as simple fixed-point, which may be arranged to always be positive. However, when referring to a table entry, the subscript N will be the integer value derived by ignoring the binary point. The value in storage, F(N), is always positive, and considered fixed-point. Subtraction, as with 4 quadrant addition, uses a complementary table $G(N) = \log_2(1 - 2^{-N})$. Kingsbury and Rayner in reference 28 first proposed the function F(N), concentrating on an interesting non-memory hardware method for approximating the function.

In logarithmic coding, addition usually results in an irrational coded number, however it is now shown that the algorithm used in FOCUS programs can always yield an answer rounded to the nearest available state. In the calculation of Z, the binary subtraction, lookup, and binary addition are all exact. The only source of error is the single roundoff necessary to fit the true F(N) as precalculated into the fixed point array storage when FOCUS is being programmed. Thus the type of roundoff is totally under the programmer's control. For the programs given logarithmic rounding was chosen, that is, in a system with states of ... ½,1,2,4... $\sqrt{2}$ is the rounding point between 1 and 2 so 1.49 is rounded to 2.0. The distinction with closer states is very subtle, but it is illustrated that the type of roundoff is optional.

In the FOCUS number system, although addition introduces roundoff error, multiplication is exact. This is the inverse of the situation using fixed-point arithmetic, and superior to floating-point where normally neither operation is exact.

An example is given to add 4 and 2 with FOCUS.8 arithmetic:

$X' = 4 = 2^2$	$X = 0\ 1010.000$	→ $0\ 1010.000$
$Y' = 2 = 2^1$	$Y = 0\ 1001.000$	
+	−	
	$0\ 0001.000$ — F(8) →	$0\ 0000.101$
		+
$Z' = 6 \simeq 2^{2\frac{5}{8}}$	$Z =$ →	$0\ 1010.101$

X' = 4 is stored in the FOCUS system coded as X and Y' = 2 is stored as Y. To find Z, the FOCUS coding equivalent of the sum 4 + 2 = 6, the formula $Z = X + F(X - Y)$ is used.

A specific algorithm for four quadrant FOCUS addition is given in figure 2.3. Because this algorithm considers all four quadrants, levels 1 and 2 are used to branch between addition and subtraction algorithms. Level 4 is used to insure that F(N) is always added to the largest magnitude of X or Y, thus limiting required storage for F(N) to positive values of N. All branches are based on the single sign bit; a number is ≥ 0 if the sign bit is clear. The identifying branch number is given in binary form suggestive of the relationship of each branch to the sign bits of X, Y, and K.

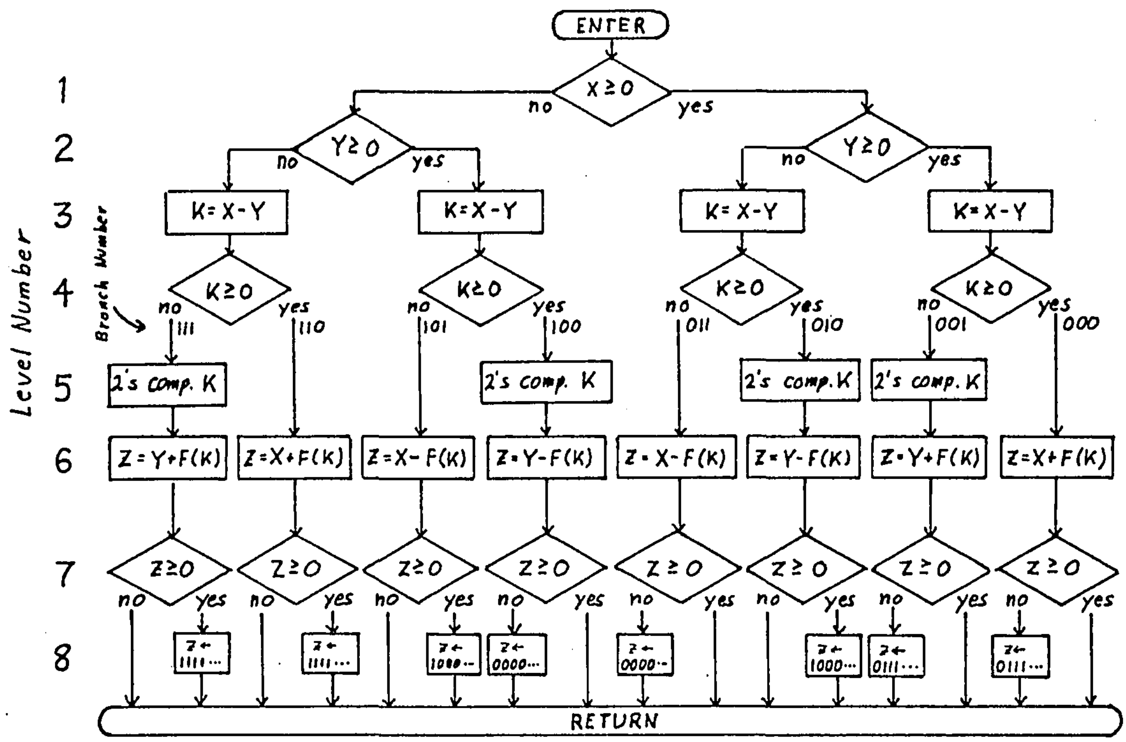


Figure 2.3 An Algorithm for Four Quadrant FOCUS Addition

On entering level 6, the sign bit of K distinguishes between an actual addition or subtraction. It will be set in the four middle branches for which X and Y have different signs. In FOCUS.8, the sign bit becomes part of the address, offsetting the lookup between the addition table F(N) and the subtraction table G(N), in effect combining these two into a single 256-byte table F(K).

In the case of FOCUS.8, F(K) for K $\geq$ 128 could be stored as a negative number, allowing all level 6 operations to be additions to facilitate hardware design. However storage economization features are more readily visualized with the subtractions included explicitly. Levels 7 and 8 test and correct for overflow and underflow.

Other Operations

Multiplication and division are very simple operations in the logarithmic FOCUS number system. Multiplication is performed by a binary addition followed by a subtraction of the offset. The correct sign bit materializes automatically. Division is complementary. Additional steps could test for overflow and underflow.

For example, to find $2 \cdot (-1/8) = -\frac{1}{4}$ in FOCUS.8 type coding:

$X' = 2 = 2^{1}$	$\rightarrow$	X = 0 1001.000
$Y' = -1/8 = -2^{-3}$	$\rightarrow$	Y = 1 0101.000
x		+
		1 1110.000
		- 1000.000 (offset)
$Z' = \frac{1}{4} = -2^{-2}$	$\rightarrow$	Z = 1 0110.000

Particularly trivial is the common multiplication by a constant.

The offset is subtracted from the constant at compilation time, reducing multiplication to a single "add immediate" instruction.

FOCUS is well suited to many other operations. For example, ignoring overflow and underflow:

$\lvert X \rvert$	Clear sign bit
$1/X$	Two's complement, complement sign
X^y	Similar to fixed-point multiplication when "y" is a fixed-point number
X^2	Shift left one bit, subtract offset
$\sqrt{X}$	Add offset, shift right one bit

Mathematical Derivation of Specifications

In this section the features of FOCUS will be expressed mathematically. Consider the parameters of a general FOCUS word to be expressed according to the following format:

```
        |<----- E bits ----->|  |<------ F bits ------>|
         1  0  0  0  0  0  0  .  0  0  0  0  0  0  0  0

 + · 2
|<------------------------- N bits ------------------------->|
```

Number of bits in fraction	= F	(= 8 above)
Bits an integer part of exponent	= E	(= 7 above)
Total number of bits	= N	(= 16 above)

Figure 2.4 Definition of Terms

F does not need to be an integer, in which case an exponent is visualized as operating on a base other than 2. In particular 9 fractional bits operating on base 10 is equivalent to $9 - \log_2(\text{Log}_2(10)) = 7.268$

fractional bits operating on base 2. One logarithm arises from the exponential relation of the binary number to the base, the other arises from the units which are in binary bits.

Accuracy

Because there are F number of bits following the binary point and the FOCUS number raises 2 to the fixed-point power, a transition of 2^F states will double or halve the FOCUS number and a single state incrementation will cause a fractional rise of $(2^{2^{-F}}-1) \cdot 100\%$ or a fractional drop of $(1 - 2^{-2^{-F}}) \cdot 100\%$. The logarithmic average of these two is:

$$\text{step size} = \frac{\ln(2^{2^{-F}}) - \ln(2^{-2^{-F}})}{2} = \ln(2) \cdot \frac{2^{-F} - (-2^{-F})}{2}$$

$$\text{step size} = \frac{\ln(2)}{2^F} \cdot 100\%$$

Note that if F = 0 and the step size is therefore ...½, 1, 2, ..., the value found by the above formula will not be 100% (1 to 2 up step = 100%, definition #1) or 50% (1 to ½ down step = 50%, definition #2) but will be $\ln(2) \cdot 100\% \simeq 69\%$ (log average, definition #3), which is considered an optimum compromise. The distinction between step size definitions is academic because for practical values of F the three different definitions coverage rapidly to equality.

Because of the optimum roundoff nature of FOCUS,

$$\text{maximum error} = \frac{\text{step size}}{2}$$

Let S be the step size as derived above. Then in a logarithmic sense the quantization error has a uniform distribution between $-\frac{1}{2}$ S and $+\frac{1}{2}$ S and the

$$\text{RMS error} = \frac{\int_{-\frac{1}{2}S}^{+\frac{1}{2}S} X^2 \, dX}{S} \qquad (\cdot 100\%)$$

$$\text{RMS error} = \frac{\text{step size}}{2\sqrt{3}} \qquad (\cdot 100\%)$$

Range

The largest and smallest magnitudes representable in FOCUS can be scaled to fit individual applications, however the overall range is set by the format chosen. Without scaling:

$$\text{Largest magnitude} = 2^{(2^{E-1} - 2^{-F})} \approx 2^{2^{E-1}} \approx 10^{\frac{2^{E-1}}{3.22}}$$

where $2^{E-1} - 2^{-F}$ is the largest number representable in the offset binary exponent, and the rest follows from this. Similarly:

$$\text{Smallest magnitude} = 2^{-2^{E-1}} \approx 10^{-\frac{2^{E-1}}{3.32}}$$

$$\text{Range} = \frac{\text{largest}}{\text{smallest}} = 2^{(2^{E} - 2^{-F})} \approx 2^{2^{E}} \approx 10^{\frac{2^{E}}{3.32}}$$

Noise and "Grain"

The absolute signal/noise ratio is computed using the maximum undistorted sinusoidal signal over the level of noise in the abscense of a signal. This leads to unreasonably good values for the logarithmic FOCUS coding, limited only by the step size between the smallest positive and largest negative number (over 1,000 db for 16-bit FOCUS coding.

$$\text{Absolute signal/noise} = 20 \cdot \log_{10}\left(\frac{\text{Range}}{\sqrt{2}}\right)$$

The instantaneous signal/noise is found by dividing the RMS value of the signal by the simultaneous additive RMS noise level. Because of the logarithmic nature of FOCUS, instantaneous signal/noise is a constant for any arbitrary interval, independent of signal magnitude, distribution, or frequency spectrum, with only the normally trivial requirement that the signal magnitude be within the range of FOCUS.

Instantaneous signal/noise = $-20 \cdot \log_{10}$(RMS error)

Magnetic recording tape becomes noisier when a signal is present than during quiescence, a factor that must be considered when comparing numerical specifications of tapes to FOCUS. In audio applications the noise level of even FOCUS.8 compares favorably to the highest quality cassette recordings as a means of signal handling.

In image processing, a particular kind of noise called "grain" or "snow" limits frequency enhancement and subjective quality. As a base for comparison, the RMS "grain" for a popular, nearly grainless, film is calculated. Kodachrome-64 exposed for a density of 1.0 ($10^{-1.0}$= 0.1 transmission) has an RMS density variation of 10×10^{-3} scanned with a 48 um diameter circular apperature, with density expressed in $\log_{10}$ units. Assuming white noise, a reasonable assumption at this spatial frequency range, this calculates to a density variation of 9×10^{-3} with 512 square pixels covering a linear dimension of 24mm, corresponding to commercial TV scanning a 35mm transparency. This density variation, in $\log_{10}$ units, corresponds to an RMS light variation of 2.1%. This is comparable with FOCUS.8 . FOCUS 10.10 has <u>35 times less</u> grain, which would be equal to that of a 33 by 50 inch transparency assuming white noise, however at such low spacial frequencies the noise of film becomes "pink", and probably no film would ever reach the grainlessness of FOCUS 10.10. Especially with modern negative films, the logarithmic state allocation of FOCUS allows a film-to-system noise ratio that is relatively independent of density, far superior to fixed point in which this ratio can vary up to several orders of magnitude as a function of density.

Accuracy Transecting Zero

Like the human eye in very low light levels, FOCUS has a blind spot at the center. A state is defined as "wasted" if its inclusion results in a step size smaller than the jump at zero. To find an expression for waste, call a state fractionally wasted in inverse proportion to neighboring step size relative to the jump at zero, resulting in a decaying exponential on a logarithmic plot for efficiency between the magnitude at which the step size equals the jump at zero (called M_1) to the minimum magnitude (called M_0). Call the maximum magnitude M_2. Note that the states are uniformly distributed logarithmically between M_0 and M_2, and in a mirror fashion from $-M_0$ to $-M_2$. The fraction of wasted states will therefore be the fractional "area" over the decaying exponential curve on a logarithmic graph between M_0 and M_1 divided by all states between M_0 and M_2. The reasonable approximation is made of ignoring the tail of the exponential decay, i.e. that

$$\int_{\log_2 M_0}^{\log_2 M_1} 2^{X-M_1}\, dX \approx \int_{-\infty}^{\log_2 M_1} 2^{X-M_1}\, dX = \frac{1}{\ln(2)} \approx 1.443$$

and therefore the fractional waste is equivalent to the ratio of the number of states between M_0 and $M_1/2^{1.443} = M_1/2.72$

$$M_0 = 2^{-2^{(E-1)}}$$

$$M_2 \approx 2^{2^{(E-1)}}$$

$$M_1 = \frac{\text{Jump at zero}}{\text{Fractional step size}}$$

$$\frac{M_1}{2.72} = \frac{2^{-2^{(E-1)}}}{\ln(2)/2^F} \cdot \frac{2}{2.72}$$

$$\text{Fraction wasted} \approx \frac{\log_2(\frac{M_1}{2.72}) - \log_2(M_0)}{\log_2(M_2) - \log_2(M_0)} = \frac{\log_2\left(\frac{2^F}{\ln(2)} \cdot \frac{2}{2.72}\right)}{\log_2(2^{2^E})}$$

$$\text{Fraction wasted} < \frac{F + .09}{2^E} \cdot 100\% \text{ of states}$$

or expressed in number of bits:

$$\text{Waste} < \log_2\left(\frac{2^E}{2^E - F - .09}\right) \text{ bits}$$

Bits spaced closer than the jump at zero are not entirely "wasted", so the estimate of efficiency based on this definition is excessively pessimistic in an RMS sense. Hence the inequality sign.

Note that waste falls rapidly with an increase in E, and rises slowly with an increase in F. For the three version presented:

Program	Waste
FOCUS.8	< 0.31 bits
FOCUS.16	< 0.05 bits
FOCUS 10.10	< 0.12 bits

A floating-point representation does not suffer from this blind spot, but does suffer from the worse malady of oscillations of fractional precision. It can be shown that the common hexadecimal-base floating-point system has an RMS error over a log range of $2^{1.29}$ times that of the purely logarithmic FOCUS coding. Therefore we may calculate the gain of FOCUS over hexadecimal-base floating-point representation by subtracting the bits wasted in FOCUS as found above from 1.29 bits. In practice the bit gain of FOCUS is larger than this number because of greater net precision of FOCUS calculations as mentioned before. In cases where the maximum relative error rather than the RMS relative error is the limiting factor, floating-point falls yet farther behind FOCUS as can be visualized by referring to figure 2.6.

The lack of zero in FOCUS seems philosophically bothersome, however, there is virtually no practical degredation of a control system because, except in a counting sense, zero does not exist in the physical world. For example, a one-foot long shorting wire of 18 guage copper at room temperature has a thermally induced "DC" noise voltage (averaged over ½ hour) across its terminals of about 10^{-13} volts, 10^{19} times larger than the smallest number in FOCUS.16. Similarly, by the Heisenberg Uncertainty Principle, zero position, velocity, and momentum are merely theoretical concepts. For image processing, the smallest FOCUS.16 number, 10^{-32}, corresponds to the current, in amps, from an ideal phototube (not photomultiplier) viewing two photons every million years. The difference between this and total darkness is academic.

Two other valid reasons for not being too concerned with the lack of a representation for zero are:

1. Floating-point computations usually don't result in an exact zero but we still use them.

2. The use of the FOCUS number system does not preclude the use of integer arithmetic where appropriate.

Array Area

A single program branching magnitude test of the subscript K at level 6 of figure 2.3 could eliminate storage requirements for the majority of states for which the lookup number if zero. A second magnitude test could eliminate more bytes of array area for which F(N) is similarly known to be 1. More magnitude tests could be arranged in sequential or tree form. Let M be the number of such program magnitude tests, where $M \geq 1$, then the required storage is:

Words in addition array F(N)

$$= \mathrm{INT}\,[-2^F \cdot \log_2(2^{\frac{M-.5}{2^F}} -1) + 1]$$

Words in subtraction array G(N)

$$= \mathrm{INT}[-2^F \cdot \log_2(1 - 2^{-\frac{M-.5}{2^F}}) + 1]$$

In these formulas INT(2.7) = 2. If L bits are in a single byte, then all FOCUS addition array numbers will fit in a single byte if $F < L$ (by barely more than an infinitesimal), and the number of FOCUS subtraction array words requiring a second byte of storage is the relatively small value

$$\mathrm{INT}[-2^F \cdot \log_2(1 - 2^{-2^{L-F}}) - 1]$$

Adding these three functions yields the minimum number of single bytes required for a two-byte FOCUS system in which $F < L$. These functions are derived through the F(N) table generation formulas presented in the second section by algebraically asking at what value of N the function F(N) will be below a value dependent on M and L above.

Figure 2.5 graphically compares the number of array words with accuracy. As described before, if some elements are stored as half words, the number of half words will be slightly higher.

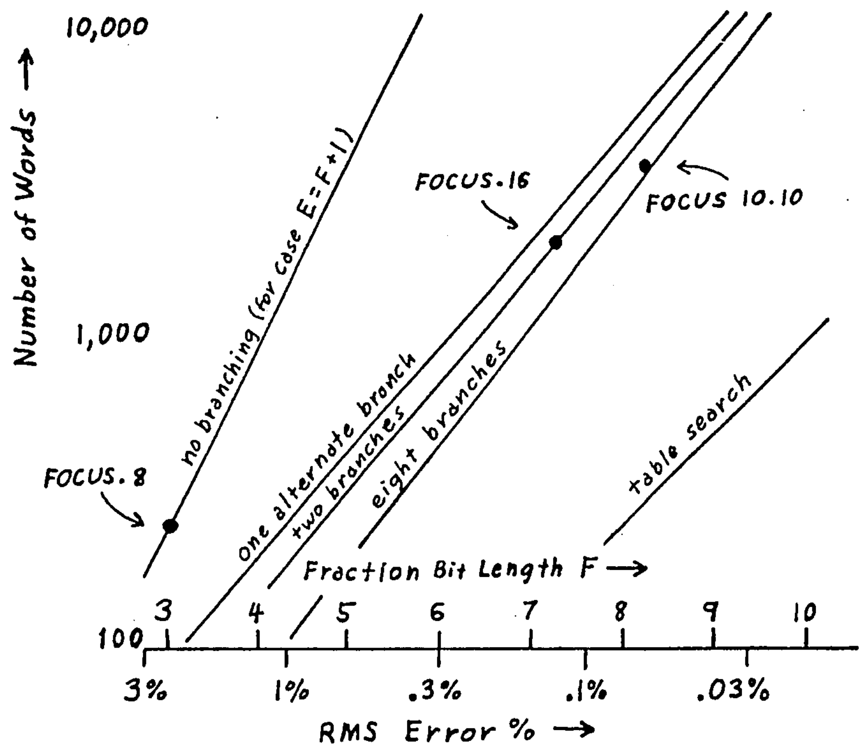


Figure 2.5 Required Memory Allocation vs Accuracy

Comparison of FOCUS, Fixed-Point, and Floating-Point

FOCUS is now compared with other number systems. The formulas of the previous section let us find the maximum fractional error for FOCUS.8 formatting to be 4.3%, which is uniform over the full range of 4.8 orders of magnitude, as represented in figure 2.6. 8-bit bipolar fixed-point will have a step size just at overflow of $100\%/2^7 \approx 0.8\%$ and a maximum relative error of half this assuming optimum roundoff. This error will vary inversly with the number represented. At 1/10 of overflow therefore the maximum relative error is $.8\%/.1 \cdot 2 = 4\%$, as represented in figure 2.6. Floating-point error is base-dependent. For comparison a base of 10 was chosen. 2 bits were allocated for the exponent, leaving 5 bits for the mantissa after the sign bit. A single mantissa cycle would thus have 4 times the error of normalized fixed-point, but there would be 4 cycles, as represented in figure 2.6. More points were computed and plotted to produce the quantitative comparison graph of figure 2.6. Note that the <u>uniformity</u> of distribution of available states give FOCUS a decided advantage over the inefficient state allocation system of floating-point. Had a base of 2 been chosen for the floating-point comparison, there would have been less oscillation of accuracy, but the median would have been elevated because base-2 floating-point has a 50% state <u>redundancy</u>.

It is interesting to quantitatively compare FOCUS to fixed-point, although such a comparison must be carefully qualified because in a way fixed-point also has an efficiently uniform state distribution. For certain applications, such as differential control, a system is limited primarily on the low end by the step size near quiescence (zero)

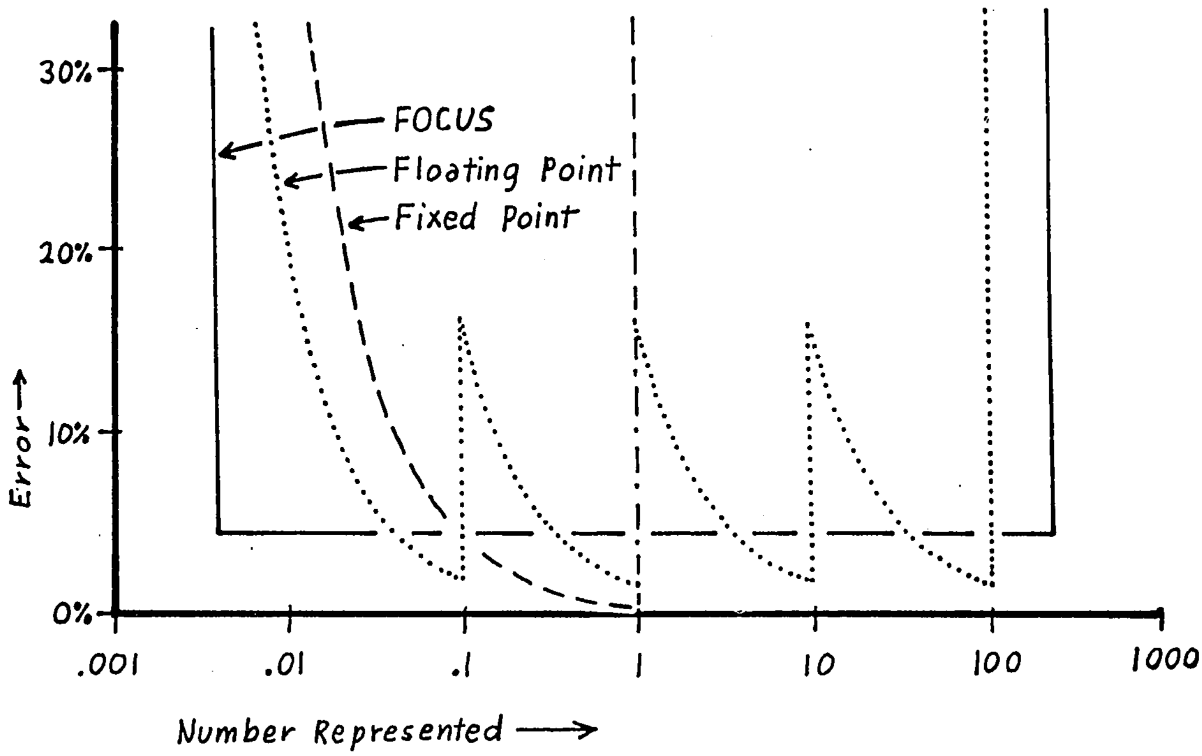


Figure 2.6 Comparison of FOCUS, Fixed-Point, and Floating-Point

and on the high end by the maximum possible amplitude without overflow, given reasonably fractional accuracy at other number levels. In FOCUS the step size at zero is twice the minimum positive number, which has been derived in the last section. Note that by the nature of FOCUS this jump at zero is the worst case error for a fairly large region around zero on both sides, and so we can validly call this step at zero the upper bound on absolute representational error of a number in a fairly large region around zero. We write for FOCUS.8:

$$\frac{\text{Linear range}}{\text{Step size at zero}} = \frac{2\cdot\max}{2\cdot\min} = \frac{2^{2^{E-1}-2^{-F}}}{2^{-2^{E-1}}} = 2^{2^{E}-2^{-F}}$$

$$= 2^{15\ 7/8}$$

Therefore under these conditions, FOCUS.8 coding provides the capability of a $15\frac{7}{8}$-bit fixed-point system.

Error Propagation

Compared to fixed-point or floating-point, programming with FOCUS is quite different, requiring new considerations to maximize benefits. These considerations are now discussed. Analysis of error propagation during calculation is of much concern. Both FOCUS and fixed-point exhibit state uniformities that allow a precision analysis of error propagation that is much more illusive in floating-point.

First we look at addition. Although FOCUS has sufficient accuracy for most applications, there is little room in 16 or 8 bits for unnecessary loss of resolution. In the prior art a programmer usually worked either with fixed-point addition which has no roundoff error, or with 32 or 64-bit floating-point addition where 16 bits of accuracy could be lost and never missed. Error propagation with addition and subtraction is the limiting factor in many applications of FOCUS.

Let σ be the fractional representational error and σ_N be the absolute representational error for the number N. (For FOCUS 10.10 σ is a constant = 0.0006 for which a formula has been developed in an earlier section and σ_{2000} for the representational error of the number 2000 is therefore $2000 \cdot \sigma = 1.2$) Let σ' and σ'_N be defined as the overall fractional and absolute errors including representational and propagated error. In computing the sum A = B + C, there will be error propagated from B and C, and error added in rerepresenting the sum as A. The total error:

$$\sigma'_A = \sqrt{\sigma_A^2 + \sigma_B'^2 + \sigma_C'^2}$$

Let B and C be equal and their fractional errors be the minimum value of σ. Thus $\sigma'_B = \sigma_B = \sigma'_C = \sigma_C$. If B and C are equal, A will have twice the value of either and thus $\sigma_A = 2 \cdot \sigma_B = 2 \cdot \sigma_C$, and therefore:

$$\sigma'_A = \sqrt{\sigma_A^2 + (\sigma_A/2)^2 + (\sigma_A/2)^2}$$

$$\sigma'_A/\sigma_A = \sqrt{1.5} \simeq 1.23$$

There has therefore been a minimum of increased fractional error in the sum compared to a pure roundoff performed on a "perfect" sum of "perfect" B and C.

Consider next an infinite sequence of sums of (nearly) equal values. First let the computation order be:

$$A = B + C + D + E + F + G + H + I + \ldots$$

It is easily shown that the fractional error of A approaches infinity. For a simplistic proof one merely extends the sum to where a new entry is less than the step size. This relies on the terminal string of systematic errors rather than RMS error propagation, but this is what happens in practice. Next consider a sum computed in the order of a binary tree:

$$A = \{[(B + C) + (D + E)] + [(F + G) + (H + I)]\} + \{\ldots$$

At each node the fractional error will increase, however the increase converges to zero and the fractional error at the root converges to $\sqrt{2} \cdot \sigma$. This can be shown by noting that when this error is reached (after an infinite number of additions) then there will be no change in error at higher nodes, i.e.:

$$\sqrt{2} \cdot \sigma = \sqrt{\sigma^2 + \left(\frac{\sqrt{2}}{2} \cdot \sigma\right)^2 + \left(\frac{\sqrt{2}}{2} \cdot \sigma\right)^2}$$

Note this is the fractional error, not the absolute error, that converges. Thus an (infinite) series of (equal) numbers of the same sign can be added in tree form with only (exactly) half a bit RMS accuracy loss compared to a paralled exact sequence added with infinite accuracy, and the sum rounded at the conclusion. Because of this the programmer should arrange additions to add numbers of roughly equal magnitudes.

As an example, suppose:

$B \simeq 2$

$C \simeq 2$

$D \simeq 2$

$E \simeq 1$

$F \simeq \frac{1}{2}$

$G \simeq \frac{1}{2}$

Then the sum:

$$A = (((B + C) + D) + F) + G$$

gives $\sigma_A = \sigma \cdot 1.92$ resulting in almost a whole bit of lost precision, but the sum:

$$A = (((G + F) + E) + D) + (B + C)$$

gives $\sigma_A = \sigma \cdot 1.34$, less than half a bit loss. Although not the preferred operation, FOCUS addition does not introduce excessive propagation error if handled correctly.

It is of interest how far a number system can count. FOCUS.8 can count accurately from 0 to 10. FOCUS.16 can count from 0 to 23 with perfectly rounded accuracy at each count, i.e., within the limits of representation (exceptions being the 6th, 8th, and 16th counts, within .002, .004, and .001 units respectively of being rounded to the nearest available states but the error disappears on the succeeding counts). The system can continue to count to 54 units within $\pm \frac{1}{2}$ unit accuracy, and to 390 units with strict monotonicity. FOCUS 10.10 has higher accuracy. Unlike integer arithmetic, FOCUS is equally suited to count by any unit, such as .00357. If the programmer desires an integer counter, the integer system is advised. If a counter must be built in FOCUS, a "product counter" should be investigated, i.e., "$\prod_{i=0}^{N} 1.0045$ until X" may serve as well as "$\sum_{i=0}^{N} 1.00$ until X". The former has been avoided in the prior art, but is fast and accurate in FOCUS.

Consider the subtraction operation A = 3 - 2. The fractional error of A $\sigma' = \sigma'_A/\sigma_A = \sigma \cdot \sqrt{1^2 + 3^2 + 2^2} \simeq \sigma \cdot 3.74$, a loss of nearly <u>2 bits</u> of precision. Note however that the answer A is nearly exact <u>in terms of the constants given</u>. The representational error of the constants <u>themselves</u> is magnified in a <u>fractional</u> sense by reduction in the magnitude of the answer. In general, subtraction should be avoided where possible by the use of differential analog signal inputs or frequency preemphasis as suggested before. When it is necessary to include subtractions they should be performed prior to summations. For example:

$$\sum_{x=1}^{16} a(x) - \sum_{x=1}^{16} b(x)$$

should be rewritten as

$$\sum_{x=1}^{16} [a(x) - b(x)]$$

or better as

$$\sum_{x=1}^{4} \sum_{y=0}^{3} [a(x + 4 \cdot y) - b(x + 4 \cdot y)]$$

as explained before. Subtraction (or addition of opposite sign numbers) is the limiting operation in many instances, and so needs to be used with care or avoided by analog means where possible.

In the FOCUS system, multiplication and division are preferred operations. Not only are they the <u>fastest</u> computations, but they are exact, introducing <u>no roundoff</u> error. In the prior-art multiplication and division were avoided unless absolutely necessary, being slow and introducing roundoff or truncation. With FOCUS these operations should be used in preference to others.

With fixed-point systems, proper scaling at each computation node was of major concern to avoid loss of precision or the devastating effects of untrapped overflow. With the logarithmically uniform, underflow/overflow trapped FOCUS programs, signal scaling is of only cursory concern, and unexpected signal characteristics are routinely handled without rescaling.

Some operations need to be rethought with FOCUS. For example, when comparing the magnitude of two numbers, expediency has dictated a subtraction and subsequent test relative to zero. In FOCUS, division should replace subtraction, with a subsequent test relative to unity, easily performed in binary FOCUS coding. An arithmetic average is not a preferred operation in FOCUS, however a geometric average, usually avoided because of "complexities", like overranging and root extraction, is very simple and accurate in FOCUS.

Conclusion

Floating-point provides accuracy at the expense of speed. FOCUS has accuracy with speed. Speed has barred microcomputers from many signal processing areas, not only precluding their direct use in audio applications, but even at lower frequencies reducing their function to mere digital filters in competition with faster, inexpensive analog filters. Computers have an intrinsic ability to analyze and heuristically adapt, to exhibit an artificial intelligence, if given time to think. The FOCUS programs provide the numerical requirements for accurate control with the speed necessary for intelligent control. Accuracy with speed makes FOCUS the key to new microcomputer applications.

CHAPTER III

FOCUS SOFTWARE

With FOCUS, an 8080A can perform the equivalent of over 20,000 18-bit floating-point additions, subtractions, multiplications, and divisions in one second, and store the results in 16-bit words. FOCUS is more than a theory, it is a completed system providing near hardware speed, 18-bit accuracy, floating-point range, and 8-bit cost.

Accuracy and Speed

In every FOCUS arithmetic routine, the answer returned is the state nearest the true answer, without compromise under any condition. Implicit in this statement is the use of optimum roundoff instead of truncation, 4 quadrant arithmetic, and fix-up of overflow and underflow to the nearest available state. Because of logarithmetic features, 70% of FOCUS arithmetic routines can return a perfect state without roundoff of any kind.

Within the limits of uncompromising accuracy the programs are optimized for a combination of speed and memory weighted heavily on the side of speed. For the 16-bit programs it is believed that memory requirement could be reduced 40% with 20% increase in execution time. The routines are written for complete generality, and so can be shortened if certain assumptions can be made. For maximum speed, the FOCUS routines can be edited to specific-case mainline segments. For example, suppose it is desired to add the contents of the A and B registers with FOCUS.8. Suppose it can be assumed at a point in the program that (A) $\geq$ (B) > 0, there will be no overflow, and the most significant 8-bits of the FOCUS table address remains in the H register. Then the following mainline segment of code will generate the answer in the A register in only 20 cycles, which is over 4 times faster than the "fast" 8-bit FADD subroutine:

```
SUB  B    ;4 CYCLES
MOV  L,A  ;5 CYCLES
ADD  B    :4 CYCLES
ADD  M    ;7 CYCLES
```

Suppose it is desired to triple the 16-bit FOCUS number in the HL register pair by multiplying by the FOCUS.16 number 3 = 0 100000.011110100, and it is assumed there will be no overflow. Then the following mainline segment of code will generate the answer in the HL register pair in only 20 cycles, almost three times faster than the 16-bit FMUL subroutine:

```
LXI  D,0000000011110100B  ;10 CYCLES
DAD  D                    ;10 CYCLES
```

Both of the above examples, an add and a multiply, an 8-bit and a 16-bit operation, each can execute on an 8080 microcomputer in less than 10 microseconds. By the use of such specific-case editing to fit the program environment at key points, in some applications the FOCUS software system can provide floating-point character arithmetic at speeds comparable with a hardware multiply system operating with fixed-point arithmetic.

Explanation of terms used in table 3.1:

Step Size - Fractional quantum step relative to the adjacent number.

RMS Fractional Error - The RMS error of rounding an arbitrary number to a FOCUS state, incurred in FOCUS A/D conversion and each arithmetic operation requiring roundoff.

Instantaneous Signal/Noise - Representational error expressed in decibels signal to noise. This is not maximum signal vs background noise, rather the much more difficult specification of actual signal vs noise and distortion present coincident with the signal. Because of logarithmic coding:

1. As the signal approaches zero, so does the absolute noise, allowing a differential "virtual ground" to eliminate most steady state controller noise.
2. Overranging is virtually impossible, allowing analog frequency preemphasis to be used.
3. Gain adjustments are not needed to avoid noise or distortion.

Sequential Roundings for 2.5% Propagated Error - This is a measure of the relative number of series calculations permitted. Some functions, such as multiplication and division do not increase the propagated error, and others, like addition and subtraction can be arranged in tree form to allow an infinite series of numbers to be added (convolved) with a resultant error equivalent to only two series additions.

Range - Largest state / Smallest positive state

Speed - Average execution time of FADD, FSUB, FMUL, and FDIV on .33 μsec cycle 8085 machine. Includes "return", but does not include "call".

Parameter	FOCUS.8	FOCUS.16	FOCUS 10.10
Step size	0.087	0.0045	0.00225
RMS Fractional Error	2.5%	0.13%	0.065%
Instantaneous Signal/Noise	32 db	58 db	64 db
Sequential Roundings for 2.5% Propagated Error	1	400	1,600
Range	$10^{4.8}$	10^{64}	10^{32}
Speed	19 μsec	30 μsec	33 μsec

Table 3.1 Comparison of FOCUS Versions

16-bit FOCUS Programming on the 8080

The 8080 microprocessor is well suited for implementation of the 16-bit FOCUS formats. The 16-bit H and L register pair should be considered a pseudoaccumulator, hereafter referred to as the HL accumulator, and the D and E register pair as a 16-bit register referred to as the DE register. The FOCUS programs accept the two 16-bit operands in the HL accumulator and the DE register, and return the result in the HL accumulator, leaving the DE register unaltered.

The 8080 instruction set includes the 16-bit register pair instructions:

LXI	16-bit load immediate
XCHG	16-bit register pair exchange
SHLD, LHLD	16-bit store and load direct
PUSH, POP	16-bit stack operations

The combination of the FOCUS subroutines, the 8080's inherent 16-bit instructions, and several simple macros, cause the 8080 to appear to both the programmer and applications analyst much like an 18-bit hardware floating-point hardware multiply machine.

Description of FOCUS Routines

Summary

The FOCUS routines are summarized in table 3.2. Terms used in that table are defined below:

Code - Name of the subroutine must be defined in an "EQU" statement.

Operation - Symbolic explanation

Safe Registers - Registers not altered by the subroutine.

μSEC - Average execution time on .33 μsec cycle machine.

Roundoff - In the integer domain 2 + 2 = 4 is exact. If in translating to integer, 2.499 = 2 and 2.501 = 3, with the watershed always exactly halfway between states, then roundoff is defined as optimal.

Detailed Information

FADD, FSUB, FMUL, FDIV. With FOCUS, multiplication and division are preferred over addition and subtraction both for speed and freedom from all roundoff. This is opposite from all familiar number systems. The addition and subtraction routines execute slightly faster when the magnitude of the operand in the accumulator (or pseudoaccumulator) is greater than or equal to the magnitude of the other operand.
However the difference is substantially less than the time required to test and shift. If an addition or subtraction results in a true answer

Code	Operation	Safe Registers	μsec	Roundoff
FADD	HL ← HL + DE	DE	42*	Optimal
FSUB	HL ← HL − DE	DE	42*	Optimal
FMUL	HL ← HL * DE	BCDE	18	Exact
FDIV	HL ← HL / DE	B DE	18	Exact
		*48 with FOCUS 10.10		
FSQR	HL ← HL^2	BCDE	12	Exact
FSQT	HL ← $\sqrt{\lvert HL \rvert}$	BCDE	18	Optimal
FEXP	HL ← HL^A	B	100	Exact
FRCP	HL ← 1/HL	BCDE	15	Exact
FABS	HL ← |HL|	BCDE	8	Exact
FNEG	HL ← −HL	BCDE	8	Exact
FTST	Test HL	BCDEHL	6	-
FCMP	Compare HL,DE	BCDEHL	16	-
FIN	HL ← Decimal In	DE	-	Non-biased
FOUT	Decimal Out ← HL	DEHL	-	Non-biased
FBOUT	Binary Out ← HL	DEHL	-	Exact
FADD.8	A ← A + B	BCDE	25	Optimal
FMUL.8	A ← A • B	BCDEHL	13	Exact
FDIV.8	A ← A / B	BCDEHL	13	Exact

Table 3.2 FOCUS Routines

of exactly zero, the sign of the operand in the accumulator (or pseudo-accumulator) determines the sign of the result.

FSQT. This function has optimal roundoff but is not non-biased. Half of all solution states are exact, the other half are always exactly between available states, and are rounded down.

FEXP. The FOCUS number in HL is raised to the binary integer power of the number in the A register, $0 \leq A \leq 255$. Execution time is power-dependent, varying between 50 and 150 μsec.

FABS, FNEG, FTST. It is recommended these functions be implemented in-line as their length is of the order of a subroutine call.

FTST. After FTST, a conditional jump has the following responses:

JC = Jump if HL < 0 } Pure 0 does not exist
JNC = Jump if HL > 0 }

JM = Jump if |HL| ≥ 1

JP = Jump if |HL| < 1

		FOCUS.16	FOCUS 10.10
JZ = Jump if HL = 0	|Smallest State| =	10^{-32}	10^{-16}
JNZ = Jump if HL ≠ 0	Considered 0 if |HL| <	$3.16 \cdot 10^{-32}$	$1.78 \cdot 10^{-16}$

FCMP. After FCMP a conditional jump has the following responses:

JC = .GT. = Jump if HL > DE

JP = .GE. = Jump if HL ≥ DE

JNC = .LE. = Jump if HL ≤ DE

JM = .LT. = Jump if HL < DE

JZ = .EQ. = Jump if HL = DE

JNZ = .NE. = Jump if HL ≠ DE

FIN. FIN inputs a decimal number from an interactive terminal and converts it to the FOCUS equivalent. The number is returned in the HL accumulator. The DE register is unaltered.

FIN will accept almost anything that resembles a number. The following are valid inputs:

3.14159

128

+.00000001

E-8

-0.05

20E3

+6.02E+23

-0

-E12

1

When FIN is called, the symbol "?" is typed as a prompt. The user then enters his number. After a blank (space bar) is accepted the number is coded and execution continued.

FIN checks each character for context as it is entered. A character will not be accepted or echoed if it is out of context. An invalid number can not be entered.

If a wrong number is typed, "rubout" may be used. The erased character is echoed. If the entire entry is rubbed out, the prompt character will be printed in response to further "rubout"s.

As with other FOCUS routines, a number out of range will be substituted with the nearest available state. An exception occurs if the mantisa of an E format data is out of range, in which case the mantisa is first substituted with the nearest extreme state before adding the exponent. For example, in FOCUS.16

.00000000000000000000000000000000002E50

is assembled as $1 \cdot 10^{-32} \cdot 10^{50} = 10^{18}$, rather than $2 \cdot 10^{-35} \cdot 10^{50} = 2 \cdot 10^{15}$, since 10^{-32} is the smallest positive FOCUS.16 number. The simplest entries to specify the extreme states are: E99, 0, -0, and -E99 .

The program is ROM compatible in that no RAM is addressed by location, however balanced stack operations are used. The depth of stack operations is 5 + [number of characters saved]. A "+" is not saved, and "rubout" relieves storage of erased characters.

A complex FOCUS residue conversion system allows nearly optimal translation to the nearest available state. Non-biased rounding returns the nearer FOCUS state without truncation.

FOUT. FOUT outputs a decimal translation of the FOCUS number in the HL accumulator. Both HL and DE are unaltered. Typical output is given with "_" = blank. Constant print length simplifies formatting.

-3.14_E_05

10
← spaces →
always

The number is rounded, not truncated. A FOCUS residue conversion system allows nearly exact decimal conversion without losing the fraction of a quantum step accuracy of a normal arithmetic operation.

The fractional quantum step of a 3 digit decimal number equals that of FOCUS.16 at 2.22 and that of FOCUS 10.10 at 4.45 .

FBOUT. FBOUT outputs the FOCUS number in the HL accumulator in absolute binary. Both HL and DE are unaltered. Typical output is given with "_" = blank:

_0_100110.001111111_

← 20 spaces always →

FADD.8, FMUL.8, FDIV.8 . These are the FOCUS.8 routines. Subtraction can be performed by complementing the sign bit before addition.

Assembly and System Requirements

Memory Requirements

All FOCUS programs are ROM compatible. No routine uses memory read or write. No arithmetic routine uses stack operations, except for "return". IO routine usage of the stack is discussed in the previous section.

	FOCUS.16	FOCUS 10.10
FADD, FSUB, FMUL, FDIV, (SUA, ADA)	2907_{10}	5125_{10}
FSQR, FSQT, FEXP, FRCP, FABS, FNEG, FTST, FCMP .	194_{10}	194_{10}
FIN, FOUT, FBOUT, (IOA)	587_{10}	588_{10}
Total 8-bit bytes	3688_{10}	5907_{10}

Table 3.3 16-bit FOCUS Memory Requirements

Input-Output Requirements

CIO equates symbols CI and CO to the system character IO routines. The file CIO contains:

```
CI  EQU  ØF8Ø3H
CO  EQU  ØF8Ø9H
```

The routines should act as follows:

CI Input an ASCII character to the A register. A and PSW registers may be affected.

CO Output an ASCII character from the C register. A, C, and PSW registers may be affected.

Users may need to modify the file CIO to fit their systems.

FOCUS Modules

Table 3.4 lists FOCUS modules along with special considerations for selecting and sequencing. FOCUS.8 is the 8-bit version. Files connected by "or" are: FILE - for FOCUS.16 or FILE.10 - for FOCUS 10.10. All other files are compatible with either 16-bit version.

File Name	Assembly Requirements
SUA or SUA.10	Must start at multiple of 256 Length is a multiple of 256
ADA or ADA.10	Must start at multiple of 256 Length is not a multiple of 256
FMUL	
FDIV	Requires FMUL
FADD or FADD.10	Requires ADA and SUA
FSUB or FSUB.10	Requires ADA, SUA, and FADD
FSQR	
FSQT	
FEXP	
FRCP	
FABS	
FNEG	
FTST	
FCMP	
CIO	User modified Equates character IO routines
IOA or IOA.10	
FIN or FIN.10	Requires CIO, IOA, FMUL, FDIV, FADD
FOUT or FOUT.10	Requires CIO, IOA, FADD, and FSUB
FBOUT or FBOUT.10	Requires CIO
FOCUS.8	Must start at multiple of 256

Table 3.4 FOCUS Modules

SUA

```
SUA1    DB     1, 78,231, 65,129,178,218,252
        DB    25, 50, 73, 94,113,130,146,161
        DB   175,188,200,212,223,233,243,252
        DB     5, 14, 22, 30, 37, 45, 52, 59
        DB    65, 71, 78, 84, 89, 95,100,106
        DB   111,116,121,125,130,135,139,143
        DB   148,152,156,160,163,167,171,174
        DB   178,181,185,188,191,195,198,201
        DB   204,207,210,213,215,218,221,224
        DB   226,229,231,234,236,239,241,244
        DB   246,248,250,253,255,  1,  3,  5
        DB     7,  9, 11, 13, 15, 17, 19, 21
        DB    23, 25, 27, 28, 30, 32, 34, 35
        DB    37, 39, 40, 42, 44, 45, 47, 48
        DB    50, 51, 53, 54, 56, 57, 59, 60
        DB    62, 63, 64, 66, 67, 68, 70, 71
        DB    72, 74, 75, 76, 77, 79, 80, 81
        DB    82, 83, 84, 86, 87, 88, 89, 90
        DB    91, 92, 93, 95, 96, 97, 98, 99
        DB   100,101,102,103,104,105,106,107
        DB   108,109,109,110,111,112,113,114
        DB   115,116,117,118,118,119,120,121
        DB   122,123,123,124,125,126,127,127
        DB   128,129,130,131,131,132,133,133
        DB   134,135,136,136,137,138,138,139
        DB   140,141,141,142,143,143,144,145
        DB   145,146,146,147,148,148,149,150
        DB   150,151,151,152,153,153,154,154
        DB   155,156,156,157,157,158,158,159
        DB   159,160,161,161,162,162,163,163
        DB   164,164,165,165,166,166,167,167
        DB   168,168,169,169,170,170,171,171

        DB -128,-5,-5,-4,-4,-4,-4,-4,-3,-3,-3,-3,-3,-3,-3,-3
        DB   -3,-3,-3,-3,-3,-3,-3,-3,-2,-2,-2,-2,-2,-2,-2,-2
        DB   -2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2
        DB   -2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2
        DB   -2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2
        DB   -2,-2,-2,-2,-2,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1
        DB   -1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1
        DB   -1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1
        DB   -1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1
        DB   -1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1
        DB   -1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1
        DB   -1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1
        DB   -1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1
        DB   -1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1
        DB   -1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1
        DB   -1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1

        DB   -85,-84,-84,-83,-83,-82,-82,-81
        DB   -81,-80,-80,-80,-79,-79,-78,-78
        DB   -77,-77,-77,-76,-76,-75,-75,-75
        DB   -74,-74,-73,-73,-73,-72,-72,-72
        DB   -71,-71,-70,-70,-70,-69,-69,-69
        DB   -68,-68,-67,-67,-67,-66,-66,-66
        DB   -65,-65,-65,-64,-64,-64,-63,-63
        DB   -63,-62,-62,-62,-61,-61,-61,-60
        DB   -60,-60,-60,-59,-59,-59,-58,-58
        DB   -58,-57,-57,-57,-57,-56,-56,-56
        DB   -55,-55,-55,-55,-54,-54,-54,-53
        DB   -53,-53,-53,-52,-52,-52,-52,-51
        DB   -51,-51,-51,-50,-50,-50,-50,-49
        DB   -49,-49,-49,-48,-48,-48,-48,-47
        DB   -47,-47,-47,-46,-46,-46,-46,-46
        DB   -45,-45,-45,-45,-44,-44,-44,-44
        DB   -44,-43,-43,-43,-43,-42,-42,-42
        DB   -42,-42,-41,-41,-41,-41,-41,-40
        DB   -40,-40,-40,-40,-39,-39,-39,-39
        DB   -39,-38,-38,-38,-38,-38,-38,-37
        DB   -37,-37,-37,-37,-36,-36,-36,-36
        DB   -36,-36,-35,-35,-35,-35,-35,-35
        DB   -34,-34,-34,-34,-34,-34,-33,-33
        DB   -33,-33,-33,-33,-32,-32,-32,-32
        DB   -32,-32,-32,-31,-31,-31,-31,-31
        DB   -31,-30,-30,-30,-30,-30,-30,-30
        DB   -29,-29,-29,-29,-29,-29,-29,-28
        DB   -28,-28,-28,-28,-28,-28,-28,-27
        DB   -27,-27,-27,-27,-27,-27,-27,-26
        DB   -26,-26,-26,-26,-26,-26,-26,-25
        DB   -25,-25,-25,-25,-25,-25,-25,-24
        DB   -24,-24,-24,-24,-24,-24,-24,-24
```

```
        DB   -23,-23,-23,-23,-23,-23,-23,-23
        DB   -23,-22,-22,-22,-22,-22,-22,-22
        DB   -22,-22,-22,-21,-21,-21,-21,-21
        DB   -21,-21,-21,-21,-21,-20,-20,-20
        DB   -20,-20,-20,-20,-20,-20,-20,-19
        DB   -19,-19,-19,-19,-19,-19,-19,-19
        DB   -19,-19,-19,-18,-18,-18,-18,-18
        DB   -18,-18,-18,-18,-18,-18,-17,-17
        DB   -17,-17,-17,-17,-17,-17,-17,-17
        DB   -17,-17,-17,-16,-16,-16,-16,-16
        DB   -16,-16,-16,-16,-16,-16,-16,-16
        DB   -15,-15,-15,-15,-15,-15,-15,-15
        DB   -15,-15,-15,-15,-15,-15,-15,-14
        DB   -14,-14,-14,-14,-14,-14,-14,-14
        DB   -14,-14,-14,-14,-14,-14,-13,-13
        DB   -13,-13,-13,-13,-13,-13,-13,-13
        DB   -13,-13,-13,-13,-13,-13,-13,-12
        DB   -12,-12,-12,-12,-12,-12,-12,-12
        DB   -12,-12,-12,-12,-12,-12,-12,-12
        DB   -12,-11,-11,-11,-11,-11,-11,-11
        DB   -11,-11,-11,-11,-11,-11,-11,-11
        DB   -11,-11,-11,-11,-11,-10,-10,-10
        DB   -10,-10,-10,-10,-10,-10,-10,-10
        DB   -10,-10,-10,-10,-10,-10,-10,-10
        DB -10,-10,-9,-9,-9,-9,-9,-9,-9,-9,-9,-9,-9,-9,-9,-9
        DB    -9,-9,-9,-9,-9,-9,-9,-9,-9,-9,-9,-8,-8,-8,-8,-8
        DB    -8,-8,-8,-8,-8,-8,-8,-8,-8,-8,-8,-8,-8,-8,-8,-8
        DB    -8,-8,-8,-8,-8,-8,-7,-7,-7,-7,-7,-7,-7,-7,-7,-7

        DB    -7,-7,-7,-7,-7,-7,-7,-7,-7,-7,-7,-7,-7,-7,-7,-7
        DB    -7,-7,-7,-7,-7,-6,-6,-6,-6,-6,-6,-6,-6,-6,-6,-6
        DB    -6,-6,-6,-6,-6,-6,-6,-6,-6,-6,-6,-6,-6,-6,-6,-6
        DB    -6,-6,-6,-6,-6,-6,-6,-6,-6,-6,-5,-5,-5,-5,-5,-5
        DB    -5,-5,-5,-5,-5,-5,-5,-5,-5,-5,-5,-5,-5,-5,-5,-5
        DB    -5,-5,-5,-5,-5,-5,-5,-5,-5,-5,-5,-5,-5,-5,-5,-5
        DB    -5,-5,-5,-5,-5,-5,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4
        DB    -4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4
        DB    -4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4
        DB    -4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-4,-3,-3,-3
        DB    -3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3
        DB    -3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3
        DB    -3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3
        DB    -3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3,-3
        DB    -3,-3,-3,-3,-3,-3,-3,-3,-2,-2,-2,-2,-2,-2,-2,-2
        DB    -2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2,-2
```

ADA

```
ADA:    DB   154,154,153,153,152,152,151,151
        DB   150,150,149,149,148,148,147,147
        DB   146,146,145,145,144,144,143,143
        DB   142,142,142,141,141,140,140,139
        DB   139,138,138,137,137,136,136,135
        DB   135,135,134,134,133,133,132,132
        DB   131,131,131,130,130,129,129,128
        DB   128,127,127,127,126,126,125,125
        DB   124,124,124,123,123,122,122,121
        DB   121,121,120,120,119,119,119,118
        DB   118,117,117,116,116,116,115,115
        DB   114,114,114,113,113,112,112,112
        DB   111,111,110,110,110,109,109,109
        DB   108,108,107,107,107,106,106,105
        DB   105,105,104,104,104,103,103,102
        DB   102,102,101,101,101,100,100,100
        DB    99,99,98,98,98,97,97,97,96,96,96,95,95,95,94,94
        DB    94,93,93,93,92,92,92,91,91,91,90,90,90,89,89,89
        DB    88,88,88,87,87,87,86,86,86,85,85,85,84,84,84,83
        DB    83,83,82,82,82,82,81,81,81,80,80,80,79,79,79,79
        DB    78,78,78,77,77,77,76,76,76,76,75,75,75,74,74,74
        DB    74,73,73,73,72,72,72,72,71,71,71,71,70,70,70,69
        DB    69,69,69,68,68,68,68,67,67,67,67,66,66,66,66,65
        DB    65,65,65,64,64,64,64,63,63,63,63,62,62,62,62,61

        DB    61,61,61,60,60,60,60,59,59,59,59,59,58,58,58,58
        DB    57,57,57,57,56,56,56,56,56,55,55,55,55,54,54,54
        DB    54,54,53,53,53,53,53,52,52,52,52,51,51,51,51,51
        DB    50,50,50,50,50,49,49,49,49,49,48,48,48,48,48,48
        DB    47,47,47,47,47,46,46,46,46,46,45,45,45,45,45,45
        DB    44,44,44,44,44,43,43,43,43,43,43,42,42,42,42,42
        DB    42,41,41,41,41,41,41,40,40,40,40,40,40,39,39,39
        DB    39,39,39,38,38,38,38,38,38,37,37,37,37,37,37,37
        DB    36,36,36,36,36,36,35,35,35,35,35,35,35,34,34,34
        DB    34,34,34,34,33,33,33,33,33,33,33,33,32,32,32,32
        DB    32,32,32,31,31,31,31,31,31,31,31,30,30,30,30,30
        DB    30,30,30,29,29,29,29,29,29,29,29,28,28,28,28,28
        DB    28,28,28,27,27,27,27,27,27,27,27,27,26,26,26,26
        DB    26,26,26,26,26,25,25,25,25,25,25,25,25,25,25,24
        DB    24,24,24,24,24,24,24,24,23,23,23,23,23,23,23,23
        DB    23,23,23,22,22,22,22,22,22,22,22,22,22,21,21,21
```

```
DB   21,21,21,21,21,21,21,21,20,20,20,20,20,20,20,20
DB   20,20,20,20,19,19,19,19,19,19,19,19,19,19,19,19
DB   18,18,18,18,18,18,18,18,18,18,18,18,18,17,17,17
DB   17,17,17,17,17,17,17,17,17,17,17,16,16,16,16,16
DB   16,16,16,16,16,16,16,16,16,15,15,15,15,15,15,15
DB   15,15,15,15,15,15,15,15,14,14,14,14,14,14,14,14
DB   14,14,14,14,14,14,14,14,14,13,13,13,13,13,13,13
DB   13,13,13,13,13,13,13,13,13,13,12,12,12,12,12,12
DB   12,12,12,12,12,12,12,12,12,12,12,12,12,11,11,11
DB   11,11,11,11,11,11,11,11,11,11,11,11,11,11,11,11
DB   11,11,10,10,10,10,10,10,10,10,10,10,10,10,10,10
DB   10,10,10,10,10,10,10,10,10, 9, 9, 9, 9, 9, 9, 9
DB    9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9
DB    9, 9, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8
DB    8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 7, 7
DB    7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7

DB   7,7,7,7,7,7,7,7,7,7,7,7,7,7,7,6
DB   6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,6
DB   6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,6
DB   6,6,6,6,5,5,5,5,5,5,5,5,5,5,5,5
DB   5,5,5,5,5,5,5,5,5,5,5,5,5,5,5,5
DB   5,5,5,5,5,5,5,5,5,5,5,5,5,5,5,5
DB   5,4,4,4,4,4,4,4,4,4,4,4,4,4,4,4
DB   4,4,4,4,4,4,4,4,4,4,4,4,4,4,4,4
DB   4,4,4,4,4,4,4,4,4,4,4,4,4,4,4,4
DB   4,4,4,4,4,4,4,4,4,4,3,3,3,3,3,3
DB   3,3,3,3,3,3,3,3,3,3,3,3,3,3,3,3
DB   3,3,3,3,3,3,3,3,3,3,3,3,3,3,3,3
DB   3,3,3,3,3,3,3,3,3,3,3,3,3,3,3,3
DB   3,3,3,3,3,3,3,3,3,3,3,3,3,3,3,3
DB   3,3,3,3,3,2,2,2,2,2,2,2,2,2,2,2
DB   2,2,2,2,2,2,2,2,2,2,2,2,2,2,2,2
DB   2
```

FMUL

```
FMUL:  MOV   A,H
       DAD   D
       XRA   D
       MVI   A,11000000B
       JM    LM

       ADD   H
       MOV   H,A
       RP
LM0:   ADD   A
       LXI   H,0000H
       RM
       LXI   H,7FFFH
       RET

LM:    ADD   H
       MOV   H,A
       RM
LM1:   ADD   A
       LXI   H,8000H
       RM
       LXI   H,0FFFFH
       RET
```

FDIV

```
FDIV:  MOV   A,L
       SUB   E
       MOV   L,A
       MVI   A,01000000B
       SBB   D
       ADD   H
       MOV   C,H
       MOV   H,A
       XRA   C
       XRA   D
       RP

       XRA   H
       MOV   A,H
       JM    LM1
       JMP   LM0
```

FADD

```
FADD:  MOV   A,H
       XRA   D
       MOV   A,L
       JM    L1


L0:    SUB   E
       MOV   C,A
       MOV   A,H
       SBB   D
       JM    L01

L00:   SUI   00000100B
       JC    L00C
       DCR   A
       JZ    L00B
       RP
       INX   H
       MVI   A,01010110B
       CMP   C
       JC    L00A
       INX   H
L00A:  ORA   H
       XRA   D
       RP
       JMP   L00E
L00B:  MVI   A,01001011B
       CMP   C
       RC
       INX   H
       ORA   H
       XRA   D
       RP
       JMP   L00E

L00C:  ADI   ADA/256+4
       MOV   B,A
       LDAX  B
       ADD   L
       MOV   L,A
       ADC   H
       SUB   L
       MOV   H,A
       XRA   D
       RP
L00E:  MVI   L,11111111B
       CMA
       XRA   D
       ORI   01111111B
       MOV   H,A
       RET

L01:   CPI   11111100B
       JNC   L01C
       MOV   L,E
       MOV   H,D
       CPI   11111010B
       RC
       JZ    L01B
       INX   H
       MVI   A,10101001B
       CMP   C
       JNC   L01A
       INX   H
L01A:  ANA   H
       XRA   D
       RP
       JMP   L00E
L01B:  MVI   A,10110100B
       CMP   C
       RNC
       INX   H
       ANA   H
       XRA   D
       RP
       JMP   L00E

L01C:  CMA
       ADI   ADA/256
       MOV   H,A
       MOV   A,C
       CMA
       MOV   L,A
       INX   H
       MOV   L,M
       MVI   H,00000000B
       DAD   D
       MOV   A,H
       XRA   D
       RP
       JMP   L00E


L1:    SUB   E
       MOV   C,A
       MOV   A,H
       SBB   D
       JP    L10

L11:   ANI   01111111B
       JZ    L11Z
       SUI   00000100B
       JC    L11C
       DCR   A
       JZ    L11B
       RP
       DCX   H
       MVI   A,01011000B
       CMP   C
       JC    L11A
       DCX   H
L11A:  ORA   H
       XRA   D
       RM
       JMP   L11E
L11B:  MVI   A,01001100B
       CMP   C
       RC
       DCX   H
       ORA   H
       XRA   D
       RM
       JMP   L11E

L11C:  ADI   SUA/256+1+4
       MOV   B,A
       LDAX  B
       ADD   L
       MOV   L,A
       MVI   A,11111111B
       ADC   H
       MOV   H,A
       XRA   D
       RM
       JMP   L11E
```

```
L11Z: MVI  B,SUA/256
      LDAX B
      INR  B
      ADD  L
      MOV  L,A
      LDAX B
      ADC  H
      MOV  H,A
      XRA  D
      RM
L11E: MVI  L,00000000B
      CMA
      XRA  D
      ANI  10000000B
      MOV  H,A
      RET

L10:  MOV  A,E
      SUB  L
      MOV  L,A
      MOV  A,D
      SBB  H
      ANI  01111111B
      JZ   L10Z
      SUI  00000100B
      JC   L10C
      MOV  C,L
      MOV  L,E
      MOV  H,D
      DCR  A
      JZ   L10B
      RP
      DCX  H
      MVI  A,01011000B
      CMP  C
      JC   L10A
      DCX  H
L10A: ORA  H
      XRA  D
      RP
      JMP  L11E
L10B: MVI  A,01001100B
      CMP  C
      RC
      DCX  H
      ORA  H
      XRA  D
      RP
      JMP  L11E

L10C: ADI  SUA/256+1+4
      MOV  H,A
      MOV  L,M
      MVI  H,11111111B
      DAD  D
      MOV  A,H
      XRA  D
      RP
      JMP  L11E

L10Z: MVI  H,SUA/256
      MOV  C,M
      INR  H
      MOV  H,M
      MOV  L,C
      DAD  D
      ORA  H
      XRA  D
      RP
      JMP  L11E
```

FSUB

```
FSUB: MOV  A,H
      XRA  D
      MOV  A,L
      JP   S1


S0:   SUB  E
      MOV  C,A
      MOV  A,H
      SBB  D
      JP   S01

S00:  SUI  10000100B
      JC   S00C
      DCR  A
      JZ   S00B
      RP
      INX  H
      MVI  A,01010110B
      CMP  C
      JC   S00A
      INX  H
S00A: ORA  H
      XRA  D
      RM
      JMP  L00E
S00B: MVI  A,01001011B
      CMP  C
      RC
      INX  H
      ORA  H
      XRA  D
      RM
      JMP  L00E

S00C: ADI  ADA/256+4
      MOV  B,A
      LDAX B
      ADD  L
      MOV  L,A
      ADC  H
      SUB  L
      MOV  H,A
      XRA  D
      RM
      JMP  L00E


S01:  CPI  01111100B
      JNC  S01C

      LXI  H,8000H
      DAD  D
      CPI  01111010B
      RC
      JZ   S01B
      INX  H
      MVI  A,10101001B
      CMP  C
      JNC  S01A
      INX  H
S01A: ANA  H
      XRA  D
      RM
      JMP  L00E
S01B: MVI  A,10110100B
      CMP  C
      RNC
      INX  H
      ANA  H
      XRA  D
      RM
      JMP  L00E
```

```
S01C: CMA
      ADI  ADA/256+128
      MOV  H,A
      MOV  A,C
      CMA
      MOV  L,A
      INX  H
      MOV  L,M
      MVI  H,10000000B
      DAD  D
      MOV  A,H
      XRA  D
      RM
      JMP  L00E


S1:   SUB  E
      MOV  C,A
      MOV  A,H
      SBB  D
      JM   S10

S11:  JZ   S11Z
      SUI  00000100B
      JC   S11C
      DCR  A
      JZ   S11B
      RP
      DCX  H
      MVI  A,01011000B
      CMP  C
      JC   S11A
      DCX  H
S11A: ORA  H
      XRA  D
      RP
      JMP  L11E
S11B: MVI  A,01001100B
      CMP  C
      RC
      DCX  H
      ORA  H
      XRA  D
      RP
      JMP  L11E

S11C: ADI  SUA/256+1+4
      MOV  B,A
      LDAX B
      ADD  L
      MOV  L,A
      MVI  A,11111111B
      ADC  H
      MOV  H,A
      XRA  D
      RP
      JMP  L11E

S11Z: MVI  B,SUA/256
      LDAX B
      INR  B
      ADD  L
      MOV  L,A
      LDAX B
      ADC  H
      MOV  H,A
      XRA  D
      RP
      JMP  L11E
```

```
S10:    MOV  A,E
        SUB  L
        MOV  C,A
        MOV  A,D
        SBB  H
        JZ   S10Z
        SUI  00000100B
        JC   S10C
        LXI  H,8000H
        DAD  D
        DCR  A
        JZ   S10B
        RP
        DCX  H
        MVI  A,01011000B
        CMP  C
        JC   S10A
        DCX  H
S10A:   ORA  H
        XRA  D
        RM
        JMP  L11E
S10B:   MVI  A,01001100B
        CMP  C
        RC
        DCX  H
        ORA  H
        XRA  D
        RM
        JMP  L11E

S10C:   ADI  SUA/256+1+4
        MOV  B,A
        LDAX B
        ADD  E
        MOV  L,A
        MVI  A,01111111B
        ADC  D
        MOV  H,A
        XRA  D
        RM
        JMP  L11E

S10Z:   MVI  B,SUA/256
        LDAX B
        INR  B
        ADD  E
        MOV  L,A
        LDAX B
        ADC  D
        XRI  10000000B
        MOV  H,A
        XRA  D
        RM
        JMP  L11E
```

FSQR

```
FSQR:   DAD   H
        MVI   A,0C0H
        ADD   H
        MOV   H,A
        RP
        LXI   H,0000H
        RNC
        LXI   H,7FFFH
        RET
```

FSQT

```
FSQT:   MOV   A,H
        ANI   7FH
        ADI   40H
        RAR
        MOV   H,A
        MOV   A,L
        RAR
        MOV   L,A
        RET
```

FEXP

```
FEXP:   STC
        RAL
        JC    E1
        ADD   A
        JC    E1
        ADD   A
        JC    E1
        ADD   A
        JC    E1
        ADD   A
        JC    E1
        ADD   A
        JC    E1
        ADD   A
        JC    E1
        ADD   A
        RC
        LXI   H,4000H
        RET
E1:     MOV   E,L
        MOV   D,H
E2:     ADD   A
        RZ
        MOV   C,A
        JNC   E6
        DAD   H
        MVI   A,0C0H
        ADD   H
        MOV   H,A
        JP    E4
        LXI   H,0000H
        JNC   E3
        LXI   H,7FFFH
E3:     MOV   A,H
E4:     DAD   D
        MVI   A,0C0H
        ADD   H
        MOV   H,A
        XRA   D
        MOV   A,C
        JP    E2
        MOV   A,H
        ADD   A
        LXI   H,0000H
        JM    E9
        LXI   H,0FFFFH
        ORA   H
        JMP   E9
E6:     DAD   H
        MVI   A,0C0H
        ADD   H
        MOV   H,A
        MOV   A,C
        JP    E2
        LXI   H,0000H
        JNC   E8
        LXI   H,7FFFH
E8:     MOV   A,C
        ADD   A
        RZ
        MOV   C,A
        RAR
E9:     ANA   D
        RAL
        MOV   A,H
        RAL
        RRC
        MOV   H,A
        JMP   E8
```

FRCP

```
FRCP:   MOV   A,L
        CMA
        MOV   L,A
        MOV   A,H
        XRI   7FH
        MOV   H,A
        INX   H
        XRA   H
        RP
        XRA   H
        ORI   7FH
        MOV   H,A
        MVI   L,0FFH
        RET
```

FABS

```
FABS:   MVI   A,7FH
        ANA   H
        MOV   H,A
        RET
```

FNEG

```
FNEG:   MVI   A,80H
        XRA   H
        MOV   H,A
        RET
```

FTST

```
FTST:   MOV   A,H
        ADD   A
        RET
```

FCMP

```
FCMP:   MOV   A,H
        SUB   D
        JZ    C1
        RAR
        MOV   C,A
        MOV   A,H
        ORA   D
        XRA   C
        RM
        STC
        RET
C1:     MOV   A,L
        SUB   E
        RZ
        RAR
        XRA   H
        RM
        STC
        RET
```

CIO

```
CO      EQU     0F809H
CI      EQU     0F803H
```

IOA

```
IOA2:
IOA     EQU     IOA2-2
        DW              0000H
        DW      4000H,  0000H
        DW      409AH,  3A1FH
        DW      40F4H,  3B2FH
        DW      4134H,  3B53H
        DW      4166H,0BAE0H
        DW      418FH,0BC66H
        DW      41B1H,0BBFCH
        DW      41CFH,0BCB2H
        DW      41E9H,0BC7AH
        DW      7FFFH
```

FIN

```
FIN:    PUSH    D               ;SUBROUTINE INPUTS NUMBER
I00:    MVI     C,3FH
        CALL    CO              ;D=DECIMAL POINT FLAG
        LXI     D,0             ;E=EXPONENTIAL FLAG
        PUSH    D               ;0=END OF STACK
I01:    CALL    CI
        ANI     7FH
        CPI     20H             ;INPUT=' '
        JNZ     I02
        POP     PSW
        PUSH    PSW
        CPI     30H
        JC      I01
        CPI     3AH
        JNC     I01
        JMP     I11
I02:    MOV     C,A             ;INPUT='-'OR'+'
        CPI     2DH
        JZ      I03
        CPI     2BH
        JNZ     I04
I03:    POP     PSW
        PUSH    PSW
        ANA     A
        JZ      I07
        CPI     45H
        JZ      I07
        JMP     I01
I04:    CPI     2EH             ;INPUT='.'
        JNZ     I05
        MOV     A,E
        ORA     D
        JNZ     I01
        INR     D
        JMP     I07
I05:    CPI     45H             ;INPUT='E'
        JNZ     I06
        ANA     E
        ORA     E
        JNZ     I01
        INR     E
        JMP     I07
I06:    CPI     30H             ;INPUT='0'TO'9'
        JC      I09
        CPI     3AH
        JNC     I09
I07:    MOV     A,C             ;PUSH&ECHO
        CPI     2BH
        JZ      I08
        PUSH    PSW
I08:    CALL    CO
        JMP     I01
I09:    CPI     7FH             ;INPUT=RUBOUT
        JNZ     I01
        POP     PSW
        ANA     A
        JZ      I00
        MOV     C,A
        CPI     2EH
        JNZ     I10
        DCR     D
I10:    CPI     45H
        JNZ     I08
        DCR     E
        JMP     I08
I11:    LXI     H,4000H         ;COMPILE
        MOV     A,E
        ANA     A
        JZ      I16             ;COMPILE EXPONENT
        LXI     D,4100H
I12:    POP     PSW             ;DE=GAIN
        CPI     45H             ;HL=POWER
        JZ      I16
        CPI     2DH
        JNZ     I13
        MVI     A,7FH
        XRA     H
        INR     A
        MOV     H,A
        JMP     I12
I13:    SUI     30H
        JZ      I15
        MOV     B,A
I14:    CALL    FMUL
        DCR     B
        JNZ     I14
I15:    MVI     A,41H
        SUB     D
        MVI     D,4AH
        JZ      I12
        MVI     D,7FH
        JMP     I12
I16:    POP     PSW             ;COMPILE MANTISA
        ANA     A
        XCHG                    ;BC=GAIN
        LXI     B,4000H         ;DE=POWER
        LXI     H,4000H         ;HL=NUMBER
        JZ      I23
        CPI     2DH
        JZ      I20
        LXI     H,0000H
        JMP     I18
I17:    POP     PSW
        ANA     A
        JZ      I23
I18:    CPI     2EH
        JNZ     I19
        PUSH    D
        MOV     D,B
        MOV     E,C
        CALL    FDIV
        LXI     B,4000H
        POP     D
        JMP     I17
I19:    CPI     2DH
        JNZ     I21
I20:    MVI     A,80H
        ORA     H
        MOV     H,A
        JMP     I17
```

```
I21:    SUI     30H
        JZ      I22
        ADD     A
        ADD     A
        PUSH    D
        PUSH    B
        PUSH    H
        PUSH    B
        ADI     (IOA+2) MOD 256
        MOV     L,A
        ACI     (IOA+2)/256
        SUB     L
        MOV     H,A
        MOV     E,M
        INX     H
        MOV     D,M
        MOV     C,L
        MOV     B,H
        POP     H
        CALL    FMUL
        POP     D
        PUSH    B
        CALL    FADD
        MOV     B,H
        MOV     C,L
        POP     H
        DCX     H
        DCX     H
        MOV     D,M
        DCX     H
        MOV     E,M
        POP     H
        PUSH    H
        CALL    FMUL
        MOV     D,B
        MOV     E,C
        CALL    FADD
        POP     B
        POP     D
I22:    MVI     A,02H
        ADD     B
        MOV     B,A
        JP      I17
        LXI     B,7FFFH
        JMP     I17
I23:    CALL    FMUL
        CALL    FMUL
        POP     D
        RET
```

FOUT

```
FOUT:   PUSH    D
        PUSH    H
        ANA     H
        ORA     H
        MVI     C,20H
        JP      T1
        MVI     C,2DH
T1:     MVI     B,0FFH
        ANI     01H
        ORI     40H
        MOV     H,A
T2:     CALL    CO
T3:     PUSH    B
        MVI     A,04H
        MOV     B,H
        MOV     C,L
T4:     PUSH    PSW
        PUSH    H
        PUSH    B
        ADI     IOA MOD 256
        MOV     C,A
        ACI     IOA/256
        SUB     C
        MOV     B,A
        LDAX    B
        MOV     E,A
        INX     B
        LDAX    B
        MOV     D,A
        CALL    FSUB
        ORA     H
        ANA     A
        JM      T5
        POP     B
        MOV     B,H
        MOV     C,L
        POP     H
        POP     PSW
        ADI     04H
        JMP     T4
T5:     POP     H
        POP     PSW
        POP     PSW
        PUSH    H
        MOV     B,A
        RRC
        RRC
        ADI     2FH
        MOV     C,A
        CALL    CO
        MVI     A,(IOA-2) MOD 256
        ADD     B
        MOV     L,A
        ACI     (IOA-2)/256
        SUB     L
        MOV     H,A
        MOV     E,M
        INX     H
        MOV     D,M
        LXI     H,3B4EH
        CALL    FSUB
        POP     D
        CALL    FADD
        LXI     D,3203H
        DAD     D
        POP     B
        INR     B
        JNZ     T6
        MVI     C,2EH
        JMP     T2
T6:     MOV     A,B
        CPI     2
        JC      T3
        MVI     C,20H
        CALL    CO
        MVI     C,45H
        CALL    CO
        POP     H
        MOV     A,H
        ADD     A
        JM      T7
        MVI     C,2DH
        CALL    CO
        MOV     A,H
        CMA
        ADI     02H
        JMP     T8
T7:     MVI     C,20H
        CALL    CO
        MOV     A,H
T8:     RRC
        ANI     3FH
        XRI     20H
        MVI     B,30H
T9:     SUI     10
        JC      T10
        INR     B
        BMP     T9
T10:    ADI     3AH
        MOV     C,B
        MOV     B,A
        CALL    CO
        MOV     C,B
        CALL    CO
        POP     D
        RET
```

FBOUT

```
FBOUT:  PUSH    H
        PUSH    D
        MVI     B,16
B1:     MVI     C,20H
B2:     CALL    CO
B3:     DAD     H
        RAL
        ANI     01H
        ORI     30H
        MOV     C,A
        CALL    CO
        DCR     B
        JZ      B5
        MOV     A,B
        CPI     15
        JZ      B1
B4:     CPI     9
        JNZ     B3
        MVI     C,2EH
        JMP     B2
B5:     MVI     C,20H
        CALL    CO
        POP     D
        POP     H
        RET
```

SUA.10

```
SUA:    DB      1,104,156, 79,207, 50,130,198
        DB      1, 53, 99,141,179,215, -9, 21
        DB     49, 76,101,124,147,163,168,207
        DB    226,243,  4, 21, 36, 51, 66, 80
        DB     94,107,120,132,144,156,167,178
        DB    189,200,210,220,229,239, -8,  1
        DB     10, 19, 27, 36, 44, 52, 60, 67
        DB     75, 82, 89, 97,104,110,117,124
        DB    130,137,143,149,155,161,167,173
        DB    179,184,190,195,201,206,211,217
        DB    222,227,232,237,241,246, -5,  0
        DB      4,  9, 13, 18, 22, 26, 31, 35
        DB     39, 43, 47, 51, 55, 59, 63, 67
        DB     71, 75, 78, 82, 86, 89, 93, 96
        DB    100,103,107,110,114,117,120,124
        DB    127,130,133,136,139,143,146,149
        DB    152,155,158,161,163,166,169,172
        DB    175,178,180,183,186,189,191,194
        DB    196,199,202,204,207,209,212,214
        DB    217,219,222,224,226,229,231,233
        DB    236,238,240,243,245, -9, -7, -4
        DB     -2,  0,  2,  4,  6,  5, 11, 13
        DB     15, 17, 19, 21, 23, 25, 27, 29
        DB     31, 33, 35, 36, 38, 40, 42, 44
        DB     46, 48, 50, 51, 53, 55, 57, 59
        DB     60, 62, 64, 66, 67, 69, 71, 72
        DB     74, 76, 77, 79, 81, 82, 84, 86
        DB     87, 89, 90, 92, 94, 95, 97, 98
        DB    100,101,103,104,106,107,109,110
        DB    112,113,115,116,117,119,120,122
        DB    123,124,126,127,129,130,131,133
        DB    134,135,137,138,139,141,142,143

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        DB      207,208,209,210,211,212,213,214
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        DB      237,238,239,239,240,241,242,243
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ADA.10

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        DB      21,21,20,20,20,19,19,18,18,17,17,16,16,15,15,15
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        DB      216,216,216,215,215,214,214,214
        DB      213,213,212,212,212,211,211,211
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        DB      201,201,201,200,200,200,199,199
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DB      113,113,112,112,112,112,112,111
DB      111,111,111,110,110,110,110,110
DB      109,109,109,109,109,108,108,108
DB      108,107,107,107,107,107,106,106
DB      106,106,106,105,105,105,105,104
DB      104,104,104,104,103,103,103,103
DB      103,102,102,102,102,102,101,101
DB      101,101,101,100,100,100,100,100
DB       99, 99, 99, 99, 99, 98, 98, 98
DB      98,98,97,97,97,97,97,96,96,96,96,96,95,95,95,95
DB      95,94,94,94,94,94,93,93,93,93,93,93,92,92,92,92
DB      92,91,91,91,91,91,91,90,90,90,90,90,89,89,89,89
DB      89,88,88,88,88,88,88,87,87,87,87,87,87,86,86,86
DB      86,86,85,85,85,85,85,85,84,84,84,84,84,84,83,83
DB      83,83,83,83,82,82,82,82,82,82,81,81,81,81,81,81
DB      80,80,80,80,80,80,79,79,79,79,79,79,78,78,78,78
DB      78,78,77,77,77,77,77,77,76,76,76,76,76,76,76,75
DB      75,75,75,75,75,74,74,74,74,74,74,74,73,73,73,73

DB      73,73,72,72,72,72,72,72,72,71,71,71,71,71,71,71
DB      70,70,70,70,70,70,70,69,69,69,69,69,69,69,68,68
DB      68,68,68,68,68,67,67,67,67,67,67,67,66,66,66,66
DB      66,66,66,65,65,65,65,65,65,65,65,64,64,64,64,64
DB      64,64,63,63,63,63,63,63,63,63,62,62,62,62,62,62
DB      62,61,61,61,61,61,61,61,61,60,60,60,60,60,60,60
DB      60,59,59,59,59,59,59,59,59,58,58,58,58,58,58,58
DB      58,57,57,57,57,57,57,57,57,56,56,56,56,56,56,56
DB      56,56,55,55,55,55,55,55,55,55,55,54,54,54,54,54
DB      54,54,54,53,53,53,53,53,53,53,53,53,52,52,52,52
DB      52,52,52,52,52,51,51,51,51,51,51,51,51,51,50,50
DB      50,50,50,50,50,50,50,50,49,49,49,49,49,49,49,49
DB      49,48,48,48,48,48,48,48,48,48,48,47,47,47,47,47
DB      47,47,47,47,47,46,46,46,46,46,46,46,46,46,46,45
DB      45,45,45,45,45,45,45,45,45,45,44,44,44,44,44,44
DB      44,44,44,44,43,43,43,43,43,43,43,43,43,43,43,42
```

```
        DB      42,42,42,42,42,42,42,42,42,42,41,41,41,41,41,41
        DB      41,41,41,41,41,41,40,40,40,40,40,40,40,40,40,40
        DB      40,39,39,39,39,39,39,39,39,39,39,39,39,38,38,38
        DB      38,38,38,38,38,38,38,38,38,37,37,37,37,37,37,37
        DB      37,37,37,37,37,37,36,36,36,36,36,36,36,36,36,36
        DB      36,36,36,35,35,35,35,35,35,35,35,35,35,35,35,35
        DB      34,34,34,34,34,34,34,34,34,34,34,34,34,34,33,33
        DB      33,33,33,33,33,33,33,33,33,33,33,33,32,32,32,32
        DB      32,32,32,32,32,32,32,32,32,32,31,31,31,31,31,31
        DB      31,31,31,31,31,31,31,31,31,30,30,30,30,30,30,30
        DB      30,30,30,30,30,30,30,30,29,29,29,29,29,29,29,29
        DB      29,29,29,29,29,29,29,29,28,28,28,28,28,28,28,28
        DB      28,28,28,28,28,28,28,28,27,27,27,27,27,27,27,27
        DB      27,27,27,27,27,27,27,27,27,26,26,26,26,26,26,26
        DB      26,26,26,26,26,26,26,26,26,26,25,25,25,25,25,25
        DB      25,25,25,25,25,25,25,25,25,25,25,25,25,24,24,24

        DB      24,24,24,24,24,24,24,24,24,24,24,24,24,24,24,24
        DB      23,23,23,23,23,23,23,23,23,23,23,23,23,23,23,23
        DB      23,23,23,23,22,22,22,22,22,22,22,22,22,22,22,22
        DB      22,22,22,22,22,22,22,22,22,21,21,21,21,21,21,21
        DB      21,21,21,21,21,21,21,21,21,21,21,21,21,21,21,20
        DB      20,20,20,20,20,20,20,20,20,20,20,20,20,20,20,20
        DB      20,20,20,20,20,19,19,19,19,19,19,19,19,19,19,19
        DB      19,19,19,19,19,19,19,19,19,19,19,19,19,18,18,18
        DB      18,18,18,18,18,18,18,18,18,18,18,18,18,18,18,18
        DB      18,18,18,18,18,18,17,17,17,17,17,17,17,17,17,17
        DB      17,17,17,17,17,17,17,17,17,17,17,17,17,17,17,17
        DB      17,16,16,16,16,16,16,16,16,16,16,16,16,16,16,16
        DB      16,16,16,16,16,16,16,16,16,16,16,16,16,15,15,15
        DB      15,15,15,15,15,15,15,15,15,15,15,15,15,15,15,15
        DB      15,15,15,15,15,15,15,15,15,15,15,15,14,14,14,14
        DB      14,14,14,14,14,14,14,14,14,14,14,14,14,14,14,14

        DB      14,14,14,14,14,14,14,14,14,14,14,14,13,13,13,13
        DB      13,13,13,13,13,13,13,13,13,13,13,13,13,13,13,13
        DB      13,13,13,13,13,13,13,13,13,13,13,13,13,13,13,12
        DB      12,12,12,12,12,12,12,12,12,12,12,12,12,12,12,12
        DB      12,12,12,12,12,12,12,12,12,12,12,12,12,12,12,12
        DB      12,12,12,12,11,11,11,11,11,11,11,11,11,11,11,11
        DB      11,11,11,11,11,11,11,11,11,11,11,11,11,11,11,11
        DB      11,11,11,11,11,11,11,11,11,11,11,11,11,10,10,10
        DB      10,10,10,10,10,10,10,10,10,10,10,10,10,10,10,10
        DB      10,10,10,10,10,10,10,10,10,10,10,10,10,10,10,10
        DB      10,10,10,10,10,10,10,10,10,10, 9, 9, 9, 9, 9, 9
        DB       9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9
        DB       9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9
        DB       9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 8, 8, 8, 8
        DB       8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8
        DB       8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8

        DB      8,8,8,8,8,8,8,8,8,8,8,8,8,8,8,8
        DB      8,8,8,8,7,7,7,7,7,7,7,7,7,7,7,7
        DB      7,7,7,7,7,7,7,7,7,7,7,7,7,7,7,7
        DB      7,7,7,7,7,7,7,7,7,7,7,7,7,7,7,7
        DB      7,7,7,7,7,7,7,7,7,7,7,7,7,7,7,7
        DB      7,7,7,7,6,6,6,6,6,6,6,6,6,6,6,6
        DB      6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,6
        DB      6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,6
        DB      6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,6
        DB      6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,5
        DB      5,5,5,5,5,5,5,5,5,5,5,5,5,5,5,5
        DB      5,5,5,5,5,5,5,5,5,5,5,5,5,5,5,5
        DB      5,5,5,5,5,5,5,5,5,5,5,5,5,5,5,5
        DB      5,5,5,5,5,5,5,5,5,5,5,5,5,5,5,5
        DB      5,5,5,5,5,5,5,5,5,5,5,5,5,5,5,5
        DB      5,5,5,5,5,5,5,5,5,4,4,4,4,4,4,4

        DB      4
```

FADD.10

```
FADD:   MOV     A,H             ;ENTER
        XRA     D
        MOV     A,L
        JM      L1

L0:     SUB     E               ;ADD
        MOV     C,A
        MOV     A,H
        SBB     D
        JM      L01
```

```
L00:    JZ      L00E            ;HL>DE
        SUI     00001000B
        JC      L00D

        MOV     B,H
        JNZ     L00A            ;GROUP 8
L00S:   INX     H
        INX     H
        INX     H
        MVI     A,01101000B
        CMP     C
        JC      L00B1
        INX     H
        JMP     L00B1

L00A:   DCR     A               ;GROUP 9
        JNZ     L00B
        INX     H
        MVI     A,11100010B
        CMP     C
        BC      L00A1
        ANX     H
L00A1:  ANA     H
        XRA     B
        RP
        JMP     L00F

L00B:   DCR     A               ;GROUP 10
        JNZ     L00C
        INX     H
L00B1:  ORA     H
        XRA     B
        RP
        JMP     L00F

L00C:   DCR     A               ;GROUP 11
        RNZ
        MVI     A,11001011B
        CMP     C
        RC
        INX     H
L00C1:  ANA     H
        XRA     B
        RP
        JMP     L00F

L00D:   ADI     ADA/256+8       ;GROUP 1-7
        MOV     B,A
L00D1:  LDAX    B
        ADD     L
        MOV     L,A
        ADC     H
        SUB     L
        MOV     H,A
        XRA     D
        RP
        JMP     L00F

L00E:   MVI     B,ADA/256       ;GROUP 0
        MVI     A,01110000B
        CMP     C
        JC      L00D1
        LDAX    B
        ADD     L
        MOV     L,A
        ADC     H
        SUB     L
        INR     A
        MOV     H,A
        XRA     D
        RP

L00F:   MVI     L,11111111B     ;OVERFLOW
        MVI     A,80H
        ANA     H
        CMA
        MOV     H,A
        RET
```

```
L01:    INR     A               ;DE>HL
        JZ      L01E
        ADI     00000111B
        JC      L01D

        MOV     B,H
        MOV     L,E
        MOV     H,D
        INR     A
        JNZ     L01A            ;GROUP 8
L01S:   INX     H
        INX     H
        CMP     C
        JZ      L01A1
        INX     H
        MVI     A,10010111B
        CMP     C
        JNC     L00C1
        INX     H
        JMP     L00C1

L01A:   INR     A               ;GROUP 9
        JNZ     L01B
        INX     H
        MVI     A,00011101B
        CMP     C
        JNC     L01A1
        INX     H
L01A1:  ORA     H
        XRA     B
        RP
        JMP     L00F

L01B:   INR     A               ;GROUP 10
        JNZ     L01C
        INX     H
L01B1:  ORA     H
        XRA     B
        RP
        JMP     L00F

L01C:   INR     A               ;GROUP 11
        RNZ
        MVI     A,00110100B
        CMP     C
        RNC
        INX     H
        ORA     H
        XRA     B
        RP
        JMP     L00F

L01D:   CMA                     ;GROUPS 1-7
        ADI     ADA/256+8
        MOV     H,A
        MOV     A,C
        CMA
        MOV     L,A
        INX     H
        MOV     L,M
        MVI     H,00000000B
        DAD     D
        MOV     A,H
        XRA     D
        RP
        JMP     L00F

L01E:   MVI     H,ADA/256       ;GROUP 0
        MOV     A,C
        CMA
        MOV     L,A
        INX     H
        MOV     L,M
        CPI     01110000B
        ADC     C
        INR     A
        MOV     H,A
        DAD     D
L01E1:  MOV     A,H
        XRA     D
        RP
        JMP     L00F
```

```
L1:     SUB     E               ;SUBTRACT
        MOV     C,A
        MOV     A,H
        SBB     D
        JP      L10

L11:    ANI     01111111B       ;HL>DE
        JZ      L11F
        DCR     A
        JZ      L11E
        SUI     00000111B
        JC      L11D

        MOV     B,H
        JNZ     L11A            ;GROUP 8
L11S:   DCX     H
        DCX     H
        DCX     H
        MVI     A,01101100B
        CMP     C
        JC      L11B1
        DCX     H
L11A1:  MOV     A,H
        XRA     B
        RP
        JMP     L11G

L11A:   DCR     A               ;GROUP 9
        JNZ     L11B
        DCX     H
        MOV     A,C
        CPI     11100101B
        JNC     L11C1
        DCX     H
        CPI     00000010B
        JNC     L11A1
        DCX     H
        JMP     L11B1

L11B:   DCR     A               ;GROUP 10
        JNZ     L11C
        DCX     H
L11B1:  ORA     H
        XRA     B
        RP
        JMP     L11G

L11C:   DCR     A               ;GROUP 11
        RNZ
        MVI     A,11001100B
        CMP     C
        RC
        DCX     H
L11C1:  ANA     H
        XRA     B
        RP
        JMP     L11G

L11D:   ADI     SUA/256+9       ;GROUPS 2-7
        MOV     B,A
L11D1:  LDAX    B
        ADD     L
        MOV     L,A
        MVI     A,11111111B
        ADC     H
        MOV     H,A
        XRA     D
        RM
        JMP     L11G

L11E:   MVI     B,SUA/256+2     ;GROUP 1
        MOV     A,C
        CPI     01101111B
        JNC     L11D1
        LDAX    E
        ADD     L
        MOV     L,A
        MVI     A,11111110B
        ADC     H
L11E1:  MOV     H,A
        XRA     D
        RM
        JMP     L11G

L11F:   MVI     B,SUA/256       ;GROUP 0
        LDAX    B
        INR     B
        ADD     L
        MOV     L,A
        LDAX    B
        ADC     H
        MOV     H,A
        XRA     D
        RM

L11G:   MVI     L,00000000B     ;UNDERFLOW
        MVI     A,7FH
        ORA     H
        CMA
        MOV     H,A
        RET

L10:    MOV     A,E             ;DE>HL
        SUB     L
        MOV     L,A
        MOV     A,D
        SBB     H
        ANI     01111111B
        JZ      L10F
        DCR     A
        JZ      L10E
        SUI     00000111B
        JC      L10D

        MOV     C,L
        MOV     L,E
        MOV     H,D
        MOV     B,H
        JNZ     L11A
        JMP     L11S

L10D:   ADI     SUA/256+9       ;GROUPS 2-7
        MOV     H,A
        MOV     L,M
        MVI     H,11111111B
        DAD     D
        MOV     A,H
        XRA     D
        RP
        JMP     L11G

L10E:   MVI     H,SUA/256+2     ;GROUP 1
        MOV     A,L
        MOV     L,M
        CPI     01101111B
        SBB     A
        DCR     A
        MOV     H,A
        DAD     D
        ANA     H
        XRA     D
        RP
        JMP     L11G

L10F:   MVI     H,SUA/256       ;GROUP 0
        MOV     C,M
        INR     H
        MOV     H,M
        MOV     L,C
        DAD     D
        ORA     H
        XRA     D
        RP
        JMP     L11G
```

FSUB.10

```
FSUB:   MOV     A,H
        XRA     D
        MOV     A,L
        JP      S1

S0:     SUB     E
        MOV     C,A
        MOV     A,H
        SBB     D
        JP      S01

S00:    ANI     7FH
        JZ      S00E
        SUI     00001000B
        JC      S00D
        MOV     B,H
        JNZ     L00A
        JMP     L00S

S00D:   ADI     ADA/256+8
        MOV     B,A
S00D1:  LDAX    B
        ADD     L
        MOV     L,A
        ADC     H
        SUB     L
        MOV     H,A
        XRA     D
        RM
        JMP     L00F

S00E:   MVI     B,ADA/256
        MVI     A,01110000B
        CMP     C
        JC      S00D1
        LDAX    B
        ADD     L
        MOV     L,A
        ADC     H
        SUB     L
        INR     A
        MOV     H,A
        XRA     D
        RM
        JMP     L00F

S01:    ADI     10000001B
        JZ      S01E
        ADI     00000111B
        JC      S01D
        MOV     B,H
        LXI     H,8000H
        DAD     D
        INR     A
        JNZ     L01A
        JMP     L01S

S01D:   CMA
        ADI     ADA/256+8
        MOV     H,A
        MOV     A,C
        CMA
        MOV     L,A
        INX     H
        MOV     L,M
        MVI     H,80H
        DAD     D
        MOV     A,H
        XRA     D
        RM
        JMP     L00F

S01E:   MVI     H,ADA/256
        MOV     A,C
        CMA
        MOV     L,A
        INX     H
        MOV     L,M
        CPI     01110000B
        ADC     C
        ADI     10000001B
        MOV     H,A
        DAD     D
        ANA     H
        XRA     D
        RM
        JMP     L00F

S1:     SUB     E
        MOV     C,A
        MOV     A,H
        SBB     D
        JM      S10

S11:    JZ      S11F
        DCR     A
        JZ      S11E
        SUI     00000111B
        JC      S11D
        MOV     B,D
        JNZ     L11A
        JMP     L11S

S11D:   ADI     SUA/256+9
        MOV     B,A
S11D1:  LDAX    B
        ADD     L
        MOV     L,A
        MVI     A,0FFH
        ADC     H
        MOV     H,A
        XRA     D
        RP
        JMP     L11G

S11E:   MVI     B,SUA/256+2
        MOV     A,C
        CPI     01101111B
        JNC     S11D1
        LDAX    B
        ADD     L
        MOV     L,A
        MVI     A,0FEH
        ADC     H
        MOV     H,A
        XRA     D
        RP
        JMP     L11G

S11F:   MVI     B,SUA/256
        LDAX    B
        INR     B
        ADD     L
        MOV     L,A
        LDAX    B
        ADC     H
        MOV     H,A
        XRA     D
        RP
        BMP     L11G

S10:    MOV     A,E
        SUB     L
        MOV     C,A
        MOV     A,D
        SBB     H
        JZ      S10F
        DCR     A
        JZ      S10E
        SUI     00000111B
        JC      S10D
        LXI     H,8000H
        DAD     D
        MOV     B,H
        JNZ     L11A
        JMP     L11S

S10D:   ADI     SUA/256+9
        MOV     B,A
S10D1:  LDAX    B
        ADD     E
        MOV     L,A
        MVI     A,7FH
        ADC     D
        MOV     H,A
        XRA     D
        RM
        JMP     L11G

S10E:   MVI     B,SUA/256+2
        MOV     A,C
        CPI     01101111B
        JNC     S10D1
        LDAX    B
        ADD     E
        MOV     L,A
        MVI     A,7EH
        ADC     D
        MOV     H,A
        XRA     D
        RM
        JMP     L11G

S10F:   MVI     B,SUA/256
        LDAX    B
        INR     B
        ADD     E
        MOV     L,A
        LDAX    B
        ADC     D
        XRI     80H
        MOV     H,A
        XRA     D
        RM
        JMP     L11G
```

IOA.10

```
IOA2:
IOA     EQU     IOA2-2
        DW              0003H
        DW      4000H, 0000H
        DW      4134H, 343EH
        DW      41E8H, 365DH
        DW      4268H, 36A7H
        DW      42CCH,0B5D9H
        DW      4310H,03572H
        DW      4362H,0B7F7H
        DW      439DH,0B67EH
        DW      43D1H, 35D9H
        DW      7FFFH
```

FIN.10

```
FIN:    PUSH    D       ;SUBROUTINE INPUTS NUMBER
I00:    MVI     C,3FH
        CALL    CO      ;D=DECIMAL POINT FLAG
        LXI     D,0     ;E=EXPONENTIAL FLAG
        PUSH    D       ;0=END OF STACK
I01:    CALL    CI
        ANI     7FH
        CPI     20H     ;INPUT=' '
        JNZ     I02
        POP     PSW
        PUSH    PSW
        CPI     30H
        JC      I01
        CPI     3AH
        JNC     I01
        JMP     I11
I02:    MOV     C,A     ;INPUT='-'OR'+'
        CPI     2DH
        JZ      I03
        CPI     2BH
        JNZ     I04
I03:    POP     PSW
        PUSH    PSW
        ANA     A
        JZ      I07
        CPI     45H
        JZ      I07
        JMP     I01
I04:    CPI     2EH     ;INPUT='.'
        JNZ     I05
        MOV     A,E
        ORA     D
        JNZ     I01
        INR     D
        JMP     I07
I05:    CPI     45H     ;INPUT='E'
        JNZ     I06
        ANA     E
        ORA     E
        JNZ     I01
        INR     E
        JMP     I07
I06:    CPI     30H     ;INPUT='0'TO'9'
        JC      I09
        CPI     3AH
        JNC     I09
I07:    MOV     A,C     ;PUSH&ECHO
        CPI     2BH
        JZ      I08
        PUSH    PSW
I08:    CALL    CO
        JMP     I01
I09:    CPI     7FH     ;INPUT=RUBOUT
        JNZ     I01
        POP     PSW
        ANA     A
        JZ      I00
        MOV     C,A
        CPI     2EH
        JNZ     I10
        DCR     D
I10:    CPI     45H
        JNZ     I08
        DCR     E
        JMP     I08
I11:    LXI     H,4000H ;COMPILE
        MOV     A,E
        ANA     A
        JZ      I16     ;COMPILE EXPONENT
        LXI     D,4200H
I12:    POP     PSW     ;DE=GAIN
        CPI     45H     ;HL=POWER
        JZ      I16
        CPI     2DH
        JNZ     I13
        MVI     A,7FH
        XRA     H
        INR     A
        MOV     H,A
        JMP     I12
I13:    SUI     30H
        JZ      I15
        MOV     B,A
I14:    CALL    FMUL
        DCR     B
        JNZ     I14
I15:    MVI     A,42H
        SUB     D
        MVI     D,54H
        JZ      I12
        MVI     D,7FH
        JMP     I12
I16:    POP     PSW     ;COMPILE MANTISA
        ANA     A
        XCHG            ;BC=GAIN
        LXI     B,4000H ;DE=POWER
        LXI     H,4000H ;HL=NUMBER
        JZ      I23
        CPI     2DH
        JZ      I20
        LXI     H,0000H
        JMP     I18
I17:    POP     PSW
        ANA     A
        JZ      I23
I18:    CPI     2EH
        JNZ     I19
        PUSH    D
        MOV     D,B
        MOV     E,C
        CALL    FDIV
        LXI     B,4000H
        POP     D
        JMP     I17
I19:    CPI     2DH
        JNZ     I21
I20:    MVI     A,80H
        ORA     H
        MOV     H,A
        JMP     I17
```

```
I21:    SUI     30H
        JZ      I22
        ADD     A
        ADD     A
        PUSH    D
        PUSH    B
        PUSH    H
        PUSH    B
        ADI     (IOA+2) MOD 256
        MOV     L,A
        ACI     (IOA+2)/256
        SUB     L
        MOV     H,A
        MOV     E,M
        INX     H
        MOV     D,M
        MOV     C,L
        MOV     B,H
        POP     H
        CALL    FMUL
        POP     D
        PUSH    B
        CALL    FADD
        MOV     B,H
        MOV     C,L
        POP     H
        DCX     H
        DCX     H
        MOV     D,M
        DCX     H
        MOV     A,M
        POP     H
        PUSH    H
        CALL    FMUL
        MOV     D,B
        MOV     E,C
        CALL    FADD
        POP     B
        POP     D
I22:    MVI     A,04H
        ADD     B
        MOV     B,A
        JP      I17
        LXI     B,7FFFH
        JMP     I17
I23:    CALL    FMUL
        CALL    FMUL
        POP     D
        RET
```

FOUT.10

```
FOUT:   PUSH    D
        PUSH    H
        ANA     H
        ORA     H
        MVI     C,20H
        JP      T1
        MVI     C,2DH
T1:     MVI     B,0FFH
        ANI     03H
        ORI     40H
        MOV     H,A
T2:     CALL    CO
T3:     PUSH    B
        MVI     A,04H
        MOV     B,H
        MOV     C,L
T4:     PUSH    PSW
        PUSH    H
        PUSH    B
        ADI     IOA MOD 256
        MOV     C,A
        ACI     IOA/256
        SUB     C
        MOV     B,A
        LDAX    B
        MOV     E,A
        INX     B
        LDAX    B
        MOV     D,A
        CALL    FSUB
        ORA     H
        ANA     A
        BM      T5
        POP     B
        MOV     B,H
        MOV     C,L
        POP     H
        POP     PSW
        ADI     04H
        JMP     T4
T5:     POP     H
        POP     PSW
        POP     PSW
        PUSH    H
        MOV     B,A
        RRC
        RRC
        ADI     2FH
        MOV     C,A
        CALL    CO
        MVI     A,(IOA-2) MOD 256
        ADD     B
        MOV     L,A
        ACI     (IOA-2)/256
        SUB     L
        MOV     H,A
        MOV     E,M
        INX     H
        MOV     D,M
        LXI     H,369DH
        CALL    FSUB
        POP     D
        CALL    FADD
        LXI     D,0400H
        DAD     D
        POP     B
        INR     B
        JNZ     T6
        MVI     C,2EH
        JMP     T2
T6:     MOV     A,B
        CPI     2
        JC      T3
        MVI     C,20H
        CALL    CO
        MVI     C,45H
        CALL    CO
        POP     H
        MOV     A,H
        ADD     A
        JM      T7
        MVI     C,2DH
        CALL    CO
        MOV     A,H
        CMA
        ADI     04H
        JMP     T8
T7:     MVI     C,20H
        CALL    CO
        MOV     A,H
T8:     RRC
        RRC
        ANI     1FH
        XRI     10H
        MVI     B,30H
T9:     SUI     10
        JC      T10
        INR     B
        JMP     T9
T10:    ADI     3AH
        MOV     C,B
        MOV     B,A
        CALL    CO
        MOV     C,B
        CALL    CO
        POP     D
        RET
```

FBOUT.10

```
FBOUT:  PUSH    H
        PUSH    D
        MVI     B,16
B1:     MVI     C,20H
B2:     CALL    CO
B3:     DAD     H
        RAL
        ANI     01H
        ORI     30H
        MOV     C,A
        CALL    CO
        DCR     B
        JZ      B5
        MOV     A,B
        CPI     15
        JZ      B1
B4:     CPI     10
        JNZ     B3
        MVI     C,2EH
        JMP     B2
B5:     MVI     C,20H
        CALL    CO
        POP     D
        POP     H
        RET
```

FOCUS.8

```
FAR:    DB      8,8,7,7,6,6,5,5,5,4,4,4,3,3,3,3
        DB      3,2,2,2,2,2,2,1,1,1,1,1,1,1,1,1
        DB      1,1,1,1,0,0,0,0,0,0,0,0,0,0,0,0
        DB      0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0
        DB      0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0
        DB      0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0
        DB      0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0
        DB      0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0
        DB      127,29,21,17,14,12,10,9,8,7,6,6,5,5,4,4
        DB      3,3,3,2,2,2,2,2,2,1,1,1,1,1,1,1
        DB      1,1,1,1,1,0,0,0,0,0,0,0,0,0,0,0
        DB      0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0
        DB      0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0
        DB      0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0
        DB      0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0
        DB      0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0
```

```
FADD:  MVI   H,FAR/256
       XRA   B
       JM    L1
       XRA   B
       JM    L11
       SUB   B
       JM    L001
       MOV   L,A
       ADD   B
       ADD   M
       RP
       MVI   A,01111111B
       RET
L001:  CMA
       INR   A
       MOV   L,A
       MOV   A,B
       ADD   M
       RP
       MVI   A,01111111B
       RET
L11:   SUB   B
       JM    L111
       MOV   L,A
       ADD   B
       ADD   M
       RM
       MVI   A,11111111B
       RET
L111:  CMA
       INR   A
       MOV   L,A
       MOV   A,B
       ADD   M
       RM
       MVI   A,11111111B
       RET
```

```
L1:    XRA   B
       JM    L10
       SUB   B
       JM    L011
       CMA
       INR   A
       MOV   L,A
       MOV   A,B
       SUB   M
       RM
       MVI   A,10000000B
       RET
L011:  MOV   L,A
       ADD   B
       SUB   M
       RP
       MVI   A,00000000B
       RET
L10:   SUB   B
       JM    L101
       CMA
       INR   A
       MOV   L,A
       MOV   A,B
       SUB   M
       RP
       MVI   A,00000000B
       RET
L101:  MOV   L,A
       ADD   B
       SUB   M
       RM
       MVI   A,10000000B
       RET
```

```
FMUL:  XRA   B
       JM    LM
       XRA   B
       ADD   B
       SUI   01000000B
       RP
       ADD   A
       MVI   A,00000000B
       RM
       MVI   A,01111111B
       RET
LM:    XRA   B
       ADD   B
       SUI   01000000B
       RM
       ADD   A
       MVI   A,10000000B
       RM
       MVI   A,11111111B
       RET
```

```
FDIV:  XRA   B
       JM    LD
       XRA   B
       SUB   B
       ADI   01000000B
       RP
       ADD   A
       MVI   A,00000000B
       RM
       MVI   A,01111111B
       RET
LD:    XRA   B
       SUB   B
       ADI   01000000B
       RM
       ADD   A
       MVI   A,10000000B
       RM
       MVI   A,11111111B
       RET
```

CHAPTER IV

SOFTWARE OPERATION OF THE MICRO-OPTICAL TOMOGRAPH

Introduction to Flying Spot Scanners

The Micro-Optical Tomograph is also a high quality general purpose digital imager using the flying-spot principle to read and write visual data. Flying-spot scanners were born with television. They were used in the first regular television transmissions beginning in 1928. These early broadcasts scanned a scene with a carbon arc and a mechanically rotating disk, as described by Nipkow in 1884. Today flying-spot scanners using a CRT light source are widely used for motion picture pick up in commercial TV.

When outputting an image, a computer program through this scanner sequentially builds a picture as thousands of dots, or pixels, exposing one at a time by choosing an X and Y coordinate and a beam intensity. This slowly formed image is integrated on a photographic film or paper yielding a permanent record in black and white or color.

When inputting an image, a computer program through the scanner sequentially chooses X and Y coordinates and reads various channels indicating density, color, etc. of the subject at the chosen point.

A flying-spot camera is complementary to a conventional television camera, as it now explained. In a television studio lamps are stationary while behind a lens a light-sensitive spot rapidly scans the scene. However the reciprocal nature of light allows the roles of source and sensor to be reversed. Behind a lens a spot of light could rapidly scan, projecting a "flying spot" over the scene. Photosensors replace the lamps, receiving light serially reflected from each point of the scene. On a monitor, the perspective would be as viewed from the light source. The light sensors would cast shadows and be reflected as specular highlights just as would lamps in conventional photography. When using the scanner for image input, it may be convenient to think of

1. the photosensors as light sources and
2. the CRT light source as a scannable photodetector.

No lights other than the photosensors can be used. Illuminating the subject with a conventional lamp will only produce an overall fog. Fog canceling software can use the flying-spot scanner to obtain an image of what would appear if all the lights in the universe, except for its own, were blackened. Thus it is possible to photograph a flame or lamp filament free from all self-luminescence.

There are no knobs, meters, or flashing lights, only a power switch. Except for alignment a mechanical focusing, everything is driven from software. Even alignment and focus can be checked entirely from software, a surprising and powerful feature for such a complex system.

Philosophy of the Instruction Set

The best example of an elegantly simple instruction set is Quantum Mechanics, which God designed to control the physical world.

Examples of the other extreme are well documented in most equipment manuals. An example comes to mind of a data acquisition system which languishes in a drawer because no one can figure it out. The manual says it is useful for many purposes such as meteorological data gathering. After painstakingly assembling the command set (tucked away throughout the thick manual like Easter eggs in the middle of paragraphs and in footnotes), it was apparent that to use it for other than meteorological data gathering would require programming worthy of Rube Goldberg to overcome its automatic features.

Two pitfalls seem almost universal:

1. Design for one application, resulting in a system that is inapplicable when the problem changes, and
2. Design for every application that pops to mind, resulting in a system that becomes a part of the problem.

With this in mind, the scanner design was founded on these points:

1. Operation must be simple, with few instructions, each intuitively obvious.
2. Operation must be generally applicable, free from tricks and special cases.
3. Quality must not be compromised.

After much effort results in an instruction set sufficiently simple and obvious to appear simply obvious, the harder task is designing hardware that won't cast a veto. Some of the commands in the set result in unexpected hardware difficulties. Others would have been impossible to implement in the prior-art.

Summary of the Command Set

The microcomputer program communicates with the scanner through both output ports and selected memory locations. Commands are given via output ports and data is transferred via memory.

The scanner responds to 16 bytes of memory read or write. These 16 bytes may be base addressed at any multiple of 16 bytes, defined by 12 switches on the Bus Logic Board. The chosen 16 bytes shadow RAM if the two are coincident, thus they may be placed over active memory. The 16 bytes form 8 2-byte 16-bit words. The most significant byte of each word is stored at the higher address. This ordering is consistent with computer convention, but is opposite from printing for which the most significant digit is to the left. Typical assembly language code is given below:

```
X       EQU     8000H
         .
         .
        LHLD    X       ; Increment the beam
        DAD     B       ; X position by the
        SHLD    X       ; number in the BC register
         .
         .
```

The scanner responds to 32 output ports, based at any multiple of 32 as fixed by 3 switches on the Bus Logic Board. In most cases there is no data transfer, rather it is the act of calling a port that evokes a particular response. Sample assemble language code is given below:

```
CLEAR   EQU     80H
         .
         .
        OUT     CLEAR ; Clear all integrators
         .
         .
```

Address	Code	Description
Memory base + 0	X	Read & Write 2's compliment X position
" 2	Y	Read & Write 2's compliment Y position
" 4	XEND	Read & Write FOCUS stroke endpoint offset X
" 6	YEND	Read & Write FOCUS stroke endpoint offset Y
Memory base + 8	LIGHT	Write FOCUS coded beam intensity read modified number
" 10	SENSE	Read FOCUS coded A/D sensing
" 12		Auxiliary
" 14		Auxiliary

Table 4.1 Memory Data Transfer

I/O Base + 0	CLEAR	Clear and restart all integrators
" 1	LOOK	Look at and hold all colors (integration continues)
" 2	ON1	Pulse the beam on for 1 μsec
" 3	ON10	Pulse the beam on for 10 μsec
" 4	ON100	Pulse the beam on for 100 μsec
" 5		
" 6		
" 7		
" 8		
" 9		Stepper motors
" 10		and accessories
" 11		
" 12		
" 13		
" 14		
" 15		
I/O Base + 16	TIME	
" 17	CRTO	
" 18	CRTB	
" 19	WHITE	
" 20	RED	
" 21	BLUE	"COLOR" commands
" 22		
" 23		Select channel and
" 24		start A/D conversion.
" 25		Channel connections easily
" 26		changed to suit application.
" 27		
" 28		
" 29		
" 30		
" 31	ALIGN	

Table 4.2 Output Port Commands

Memory Transfer Commands

It is hoped the user will read the entire manual, however essential points of use are spotlighted in this section.

"X" and "Y"

These behave like ordinary memory locations to computer read/write operations, however the data in them controls beam positioning electronics. The hardware views the data as 16-bit words, with the most significant byte stored in the highest address. The data is viewed in 2's complement, thus 0000H addresses the middle of the screen.

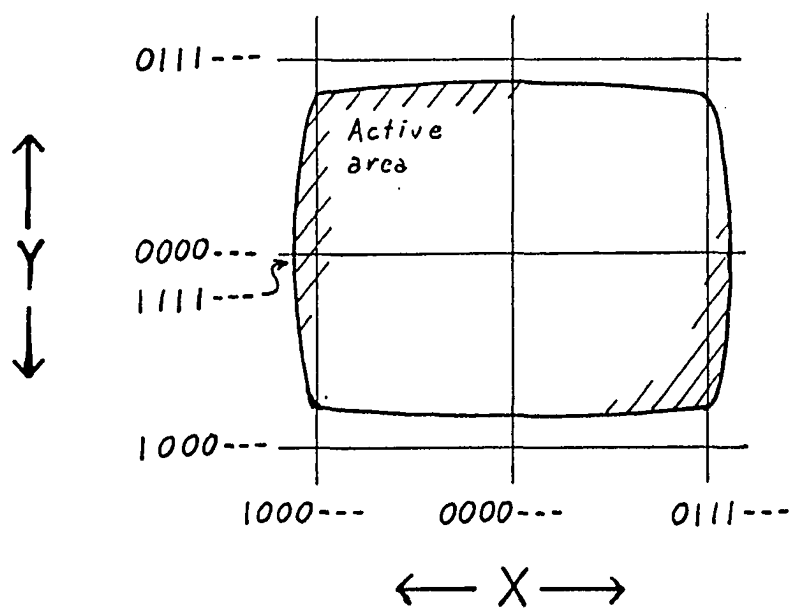


Figure 4.1 Cartesian Addressing

Data may be written to or read from one or both bytes of each word at any time or in either sequence, however for best results

1. If both bytes of a word are changed, they should be changed within at most 5 μsec of each other.

2. At least 10 μsec idling time should be allowed between updates.
3. When scanning is completed, returning the beam to the center (0000H) minimizes component strain.

Settling time is primarily limited by the deflection yokes. Some points:

1. The yoke in use may allow more rapid X settling than Y.
2. Residual transients remain after the main transients have settled, thus precision random scan requires much longer settling than uniform scanning.
3. Very slight components drifts may still effect precision gray-scale reproduction if several minutes elapse at a boundary. Think of the image as being painted, and build the image uniformly so fresh paint is never seamed over paint that has already dried.
4. Slew limitations necessitate longer settling times for larger changes.

The method of random scanning controlled entirely by two memory words is very simple to understand and use, and is responsible for much of the universality of the scanner. However in key points, such as D/A differential linearity, yoke amplifier small-signal settling time, transient suppression, and high voltage drift, the random scan system must have up to 1000 times closer tolerance to obtain equivalent gray-scale reproductive quality compared to a common fixed uniform scan system. The scanner meets these requirements without high cost. Some of the difficulties are documented with the X-Position D/A Board.

"XEND and "YEND"

These proposed commands would behave like ordinary memory locations to computer read/write operations, however the FOCUS coded data in them is added to the position defined by the X and Y words, defining a new END point. The beam is then deblanked and moved uniformly from the old END point to the new one. The width of the screen is defined as 1. The beam can be moved to any point on the screen from any X and Y, however resolution is "FOCUSed" on the point defined by X and Y.

This system adds speed for real-time vector graphics, pattern recognition, and text transcription research. Speed comes from both the integration of many points into one line and also from allowing use of FOCUS arithmetic to control scanning patterns. The system is effectively disabled by setting XEND = YEND = 0.

"LIGHT" or "Z"

The desired spot intensity is output to the 16-bit word LIGHT as a FOCUS coded number. The screen remains dark until one of the ON commands, to be discussed. Settling time is less than the computer instruction time so no waiting is needed before an ON command, however for predictable results Z should not be updated while the beam is on.

The system's behavior to FOCUS coded LIGHT values is shown:

Range of LIGHT	Brightness Attempted	Response to Memory Read
$10^4 < Z < 10^{16}$ (max)	10^{+4}	10^{+4}
$10^{-4} < Z < 10^4$	Z	Z
$-10^{+16} < Z < 10^{-4}$	10^{-4} & ON inhibit	$+10^{-16}$ (+ Zero)

Unusual circuitry allows the electron beam intensity to accurately track a logarithmic control over orders of magnitude, however the user should be aware of:

1. Saturation effects at high LIGHT
2. Residual nonlinearities at low LIGHT
3. Phospher burning dangers with high LIGHT for long times
4. Varying phosphor efficiency across the CRT face

"SENSE"

The result of an A/D conversion is read from the 16-bit SENSE. Old data remains valid during a conversion, and is updated when the conversion is completed. The output of the 12-bit A/D converter is hardware translated to 16-bit FOCUS coding, and is immediately usable with all FOCUS routines. The range of conversion is:

$$10^{-4} < \text{SENSE} < 10^{4}$$

Auxiliary Channels

Output could be to two D/A converters which are used for purposes such as self-aligning dynamic focus, detailed in the section on alignment.

Out Port Commands

"ON1", "ON10", and "ON100"

Calling one of these ports pulses on the electron beam for 1, 10, or 100 μsec. The FOCUS coded number in the Z memory bytes establish the beam intensity during the on time. Data transferred by the out command is ignored. The time multiples of 10 harmonize with base-10

FOCUS. Longer exposure times, with proportionally less LIGHT, improve sharpness, and because of P-4 persistence do not require much longer sensing times.

For special purposes repeated calls can extend the on time arbitrarily beyond 100 μsec by retriggering the timer during its count. This should be done only with extreme caution as it is possible to burn the phosphor with maximum brightness for maximum time and with repeated calls to cut through the glass, causing an implosion. The self-terminating nature of the command set protects the CRT and operator from inopportune interrupts and many program bugs.

"CLEAR", "LOOK", and 16 "COLOR" Commands

Noise ultimately limits image enhancement, therefore it is essential to obtain the purest signal possible in the presence of quantum noise. Normally this is done by averaging the signal with a low-pass filter which severely limits generality. Other problems are caused by the many anomolies of phosphor. The scanner provides a powerful and general system of noise suppression and phosphor correction. With only three easily understood commands, schemes of arbitrary complexity can be implemented in software and changed at will to fit the application.

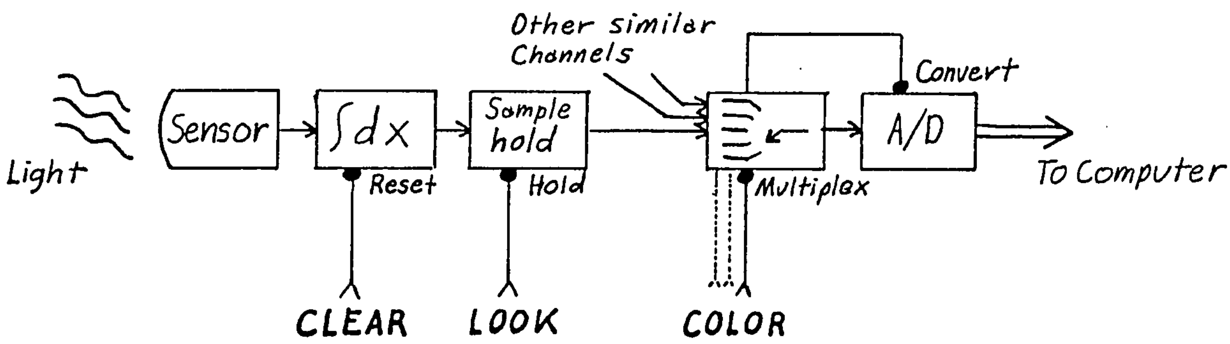


Figure 4.2 Light Sensing System

The system is illustrated above in block form. Basic operation is:

1. CLEAR the integrators. All are cleared and restarted with the single out instruction.
2. After a desired interval LOOK at the results, simultaneously freezing all channels.
3. Sequentially call each desired COLOR. Every call selects the desired channel and starts the A/D converter. The result is read from the SENSE memory bytes. Each color appears as it was at the last LOOK command.

For the moment let us sweep under the rug the fact that the output of the integrators can vary as much as 12 orders of magnitude, and the logarithm can not be validly taken till after the integration step. Assume for the moment that the system works by magic. Isn't it general and yet simple? By using the speed and range of FOCUS computations, the following are possible at speeds limited as much by phosphorescence decay as by software speed:

Direct averaging is implemented by calling CLEAR, after some time LOOK, then COLORS of both a photosense channel and a TIME channel, which actually senses a constant. Dividing the two gives the average. Simple wiring of the differential log inputs also programs the hardware to do the division, with the result read through another COLOR channel. Useful combinations include:

1. A photosense channel/Time = Average.
2. Specimen photosense/CRT photosense = Density of specimen independent of phosphor defects.
3. One color/Another color = True chroma-only signal.

Precision exposure is implemented by calling CLEAR, then ON, and after some time LOOK and COLOR. The exposure is read from SENSE and compared with that desired. Without calling CLEAR, a new value of LIGHT is loaded, and ON, LOOK, and COLOR repeated. The program then tests if the total exposure is still short of that desired for the pixel and responds accordingly. The program could test dark current and residual phosphorescence prior to calling ON. Then knowing TIME at each test, these can be corrected. Further refinements for decay effects and other anomolies are possible without being limited by the hardware.

Other possibilities include RMS averaging and photon counting, both applicable for unusual applications for which the background noise is greater than the signal. Any single COLOR can be updated 5 or 10 times faster than the background count, allowing various photon-counting schemes to be investigated in ultra-low light applications.

These examples illustrate that detection and control systems of any desired complexity can be researched in software and changed at will. The hardware remains relevent and the command set is part of the solution rather than the problem.

Timing limitations are summarized below. Times given are design values for which margin should be allowed in the software.

CLEAR Clears and restarts all integrators. Sample and holds remain in the hold state. CLEAR may be given at any time, even during an A/D conversion. CLEAR is effective virtually instantaneously unless given within 10 μsec after LOOK, in which case it will take effect 10 μsec after LOOK. This allows clearing at the effective sampling instant. Integration is accurate from 1 μsec to over 1 second.

LOOK Freezes all sample & holds. The effective sampling time occurs 10 μsec after the LOOK command when the S/Hs return to the hold state. LOOK should not be given within 14 μsec after or 7 μsec before a COLOR command else the data to the A/D converter will change during a conversion. Integration continues, and may be monitored with a new LOOK command without an intervening CLEAR. Alternately the integrators can be cleared at the effective instant of sampling for complete data continuity by calling CLEAR within 10 μsec of LOOK.

COLOR Selects a specified frozen channel and starts conversion. Which of 16 COLOR commands determines which of 16 differential channels. A conversion requires 14 μsec, during which time the old data remains valid in the SENSE memory bytes and may be read, giving the program something to do while waiting. The new data is transferred to SENSE at the conclusion of the conversion. If a new COLOR command is received during conversion, the conversion is approximated, the approximation put in SENSE, and a new conversion started normally. A method of monitoring conversion vs software speed is given with the A/D Board. COLOR should not be given less than 7 μsec after or 14 μsec before a LOOK command or the analog data will change during conversion. For best accuracy, COLOR should not be given more than 1/20 second after the MARK command.

On the 8080 the following program allows a burst conversion rate of 36 KHz:

```
setup          [ OUT     CLEAR
block          [   (37 cycle wait)

               [ OUT     LOOK
start          [ OUT     CLEAR
block          [ OUT     WHITE
               [   (27 cycle wait)

               [ OUT     LOOK      ; Sample and hold
repeat         [ OUT     CLEAR     ; Integral reset waits till S&H opens
this block     [ OUT     WHITE     ; Choose color, start conversion
N-1 times      [ LHLD    SENSE     ; Read result of last conversion
               [ PUSH    H         ; Store result of last conversion

               [   (0 cycle wait)
end            [ LHLD    SENSE
block          [ PUSH    H
```

CHAPTER V

HARDWARE OPERATION OF THE MICRO-OPTICAL TOMOGRAPH

Intermodule Connections

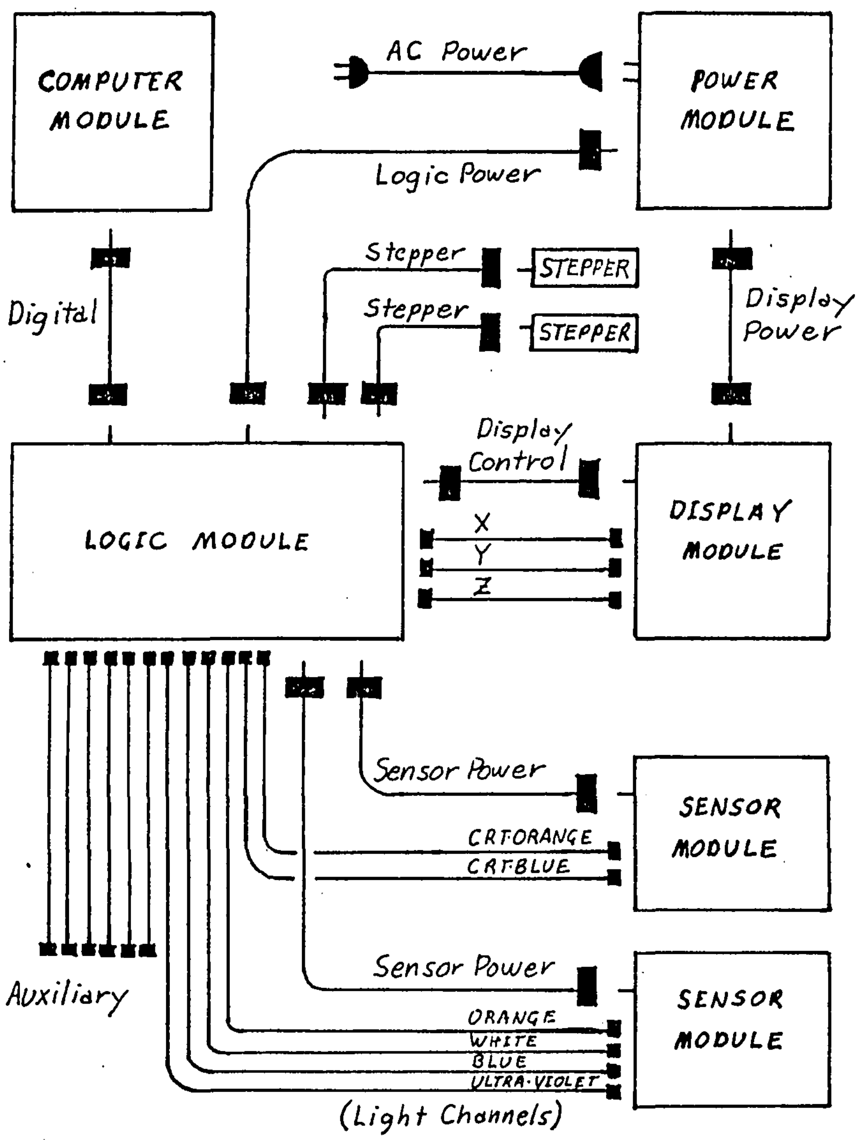
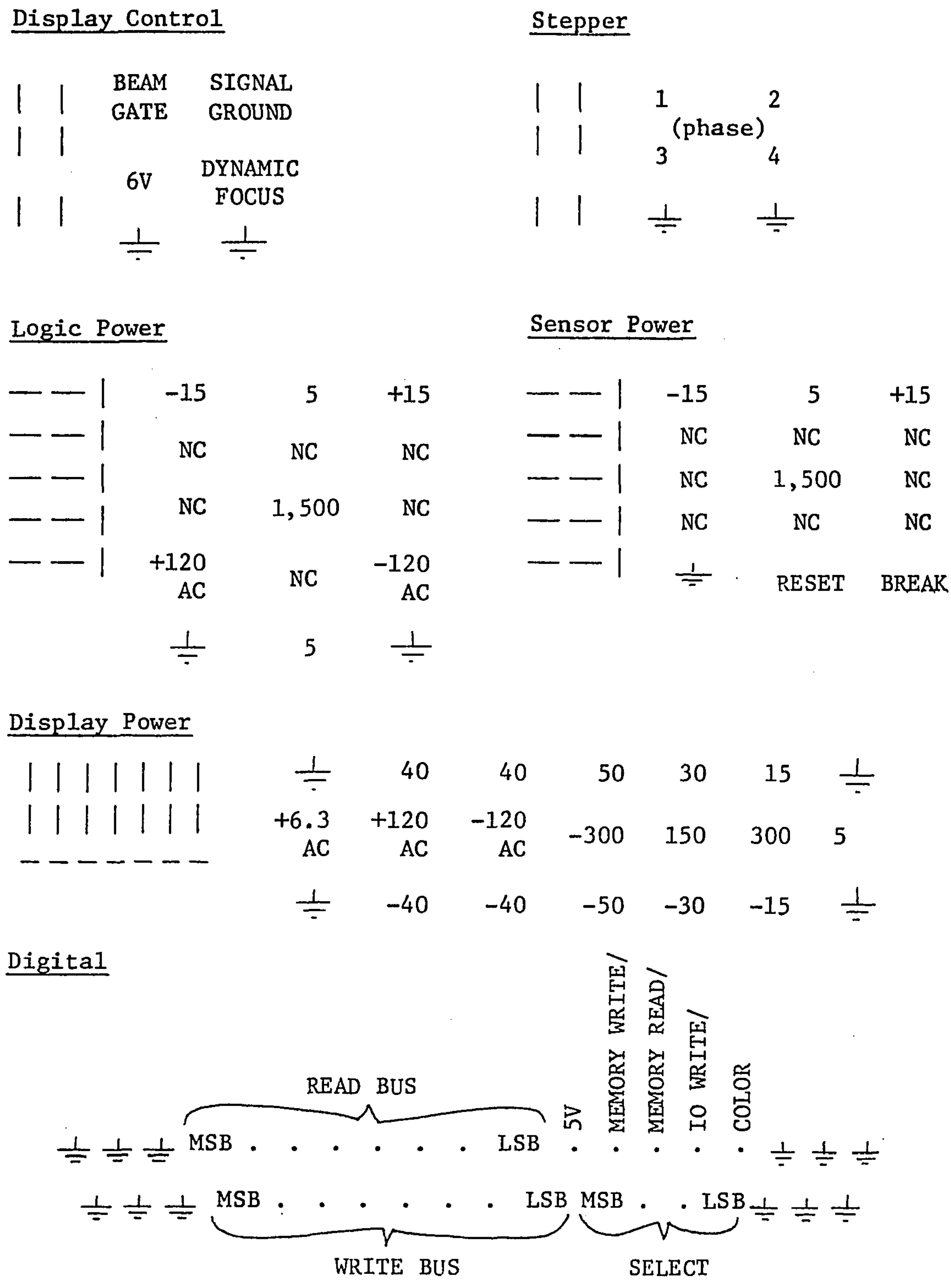


Figure 5.1 Intermodule Cables



Pinouts illustrated oriented looking into female connectors

Figure 5.2 Intermodule Cable Pinouts

Computer - Logic Modules Connections

READ BUS 8-bit positive logic word outputs data from Display Module

WRITE BUS 8-bit positive logic word outputs data from Computer Module

SELECT 4-bit positive logic address outputs from Computer Module

MEMORY WRITE/ Digital output from Computer Module. When low, register in Logic Module determined by SELECT receives data from WRITE BUS.

IO WRITE/ Digital output from Computer Module. When low, the Logic Module executes command determined by SELECT.

COLOR Digital output from Computer Module. When high, the analog channel determined by SELECT is converted by the Logic Module.

MEMORY READ/ (Not used) When low, the computer is reading data on the READ BUS. The Logic Module multiplexes the proper byte based on SELECT

+5V (Not used) For sequencing purposes the Computer Module supply is output. This is not a power source.

Logic - Display Modules Connections

X POSITION Precision analog output of Logic Module defines horizontal beam position. Range = $\pm$ 10V, -10V = right.

Y POSITION Precision analog output of Logic Module defines vertical beam position. Range = $\pm$ 10V, -10V = up.

ANALOG BEAM INTENSITY (Z) Logarithmic analog output of the Logic Module defines the beam intensity. Range = $\pm$ 5V, $10^{\pm 4}$ equivalent beam intensity.

BEAM GATE/	Digital output of Logic Module. When low, the beam is to be unblanked.
DYNAMIC FOCUS	Analog output of Logic Module controls DC coupled CRT focus grid voltage. Range = $\pm$ 12V
6V	Precision reference output of Logic Module fixes CRT anode voltage.

The X,Y, and Z inputs to the Display Module are differential relative to each cable's ground. The DYNAMIC FOCUS and 6V are differential relative to SIGNAL GROUND of the Display Control Cable. Power ground is looped through the Logic Power Cable, Display Control Cable, and Display Power Cable.

Logic - Photosense Modules Connections

LIGHT	Up to 12 analog outputs of the photosense Modules = 5/4 $\log_{10} \int$ light dt + C. Range = $\pm$ 10V. The LIGHT inputs of the Logic Module can also be used as auxiliary differential A/D channels, differential range = $\pm$ 5V.
RESET	Digital output of Logic Module. 0 $\rightarrow$ 1 transition causes integration to be reset in Photosense Modules.
1,300V	Stable supply to Photosense Modules.
BREAK/	Open collector digital output of Photosense Modules. When a photomultiplier is overloaded, BREAK/ goes low. The Logic Module then interrupts 1,300V.

Computer Module

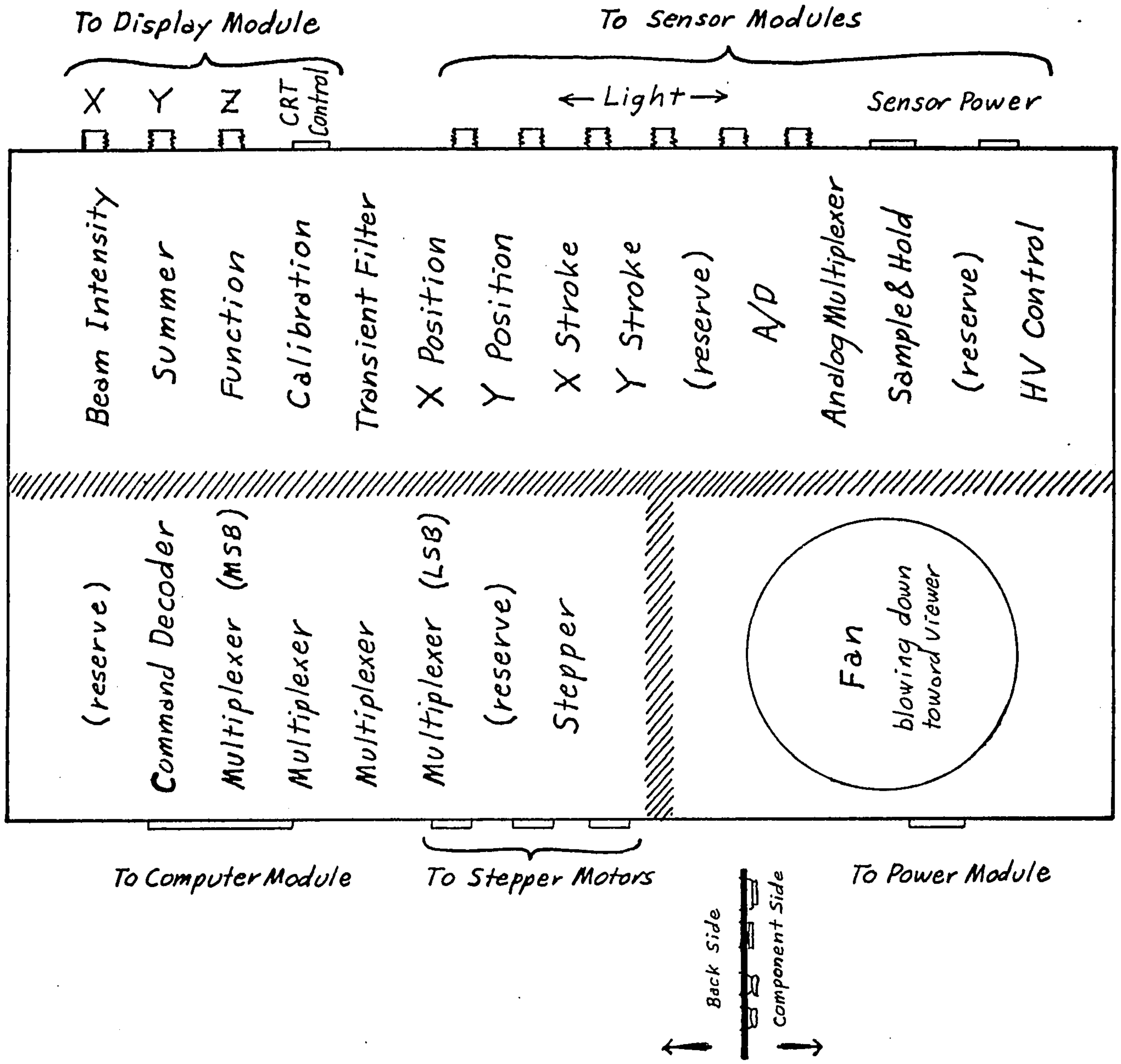
The scanner operates from an 8-bit computer using the FOCUS 10.10

number system. Several systems possibilities:

1. The minimum requirement to use the scanner is a microcomputer with a mass storage peripheral, such as a disk drive. Depending on resolution and other factors, 1 to 10 or more disks are needed to store each image. In our present case the scanner is driven by an Intel MDS800 system. The Bus Logic Board, located within the computer main frame, communicates between the scanner and computer bus.
2. A single computer can drive two scanners, one analogous to a camera receives an image, and the other analogous to an enlarger records an image. This duality would allow each CRT, phosphor color, and optical mechanics to be specialized for its application. Many circuit elements would serve both units.
3. A small microcomputer can perform the basic phosphor and optical corrections, timing, and scanning, then report to a large computer operating in either real-time or batch mode. The CEC computer remote could interface the IBM 370 with the scanner via intermediate storage on floppy disk. This would add precision graphics and full color imaging for the entire university. Transmission time would be of the order of a medium-long line printer output.

Logic Module

This module provides D/A and A/D conversions, digital and analog logics, timings, and controls of the Display and Photosense Modules.



Viewed from the chassis base

Figure 5.3 Logic Module Physical Layout

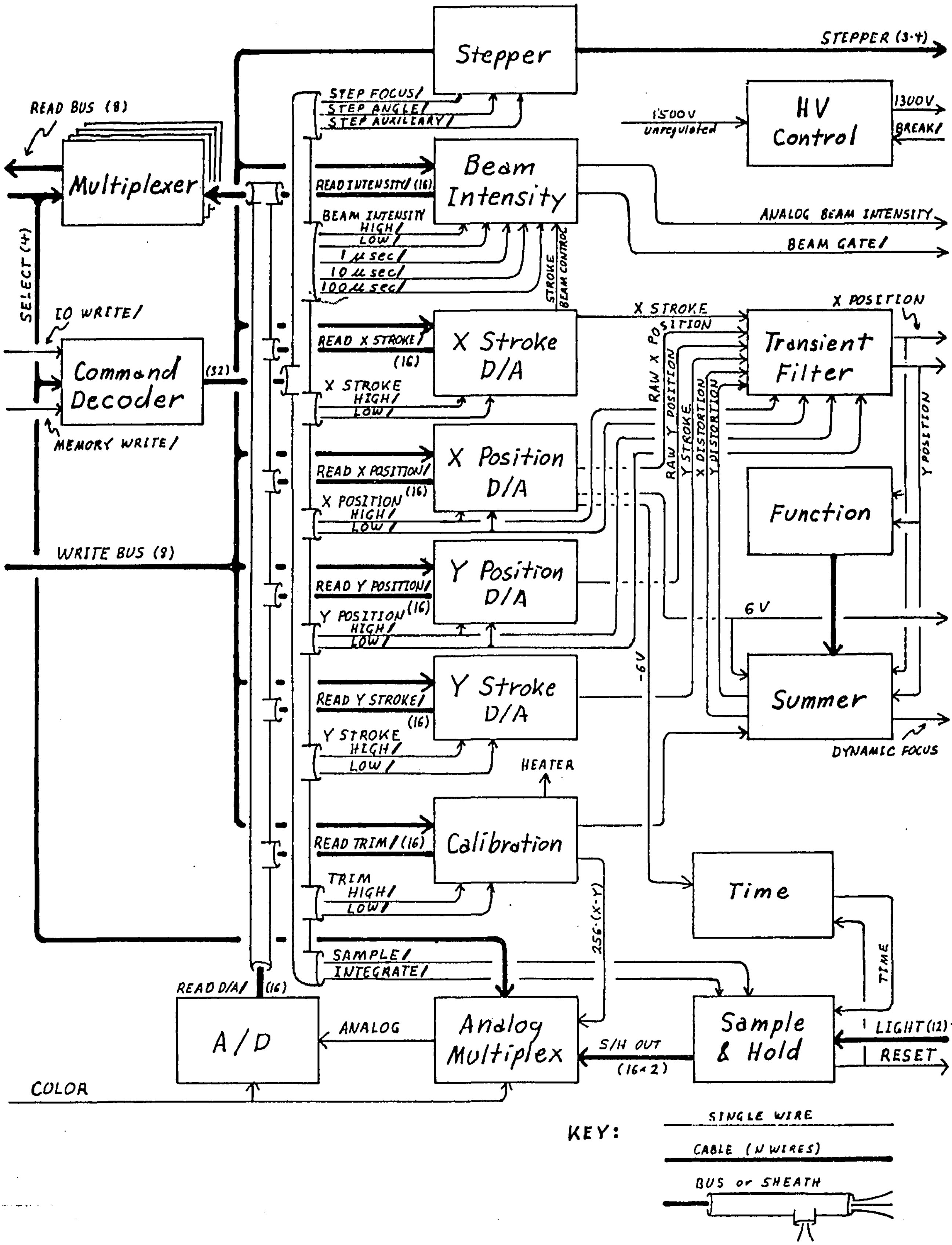
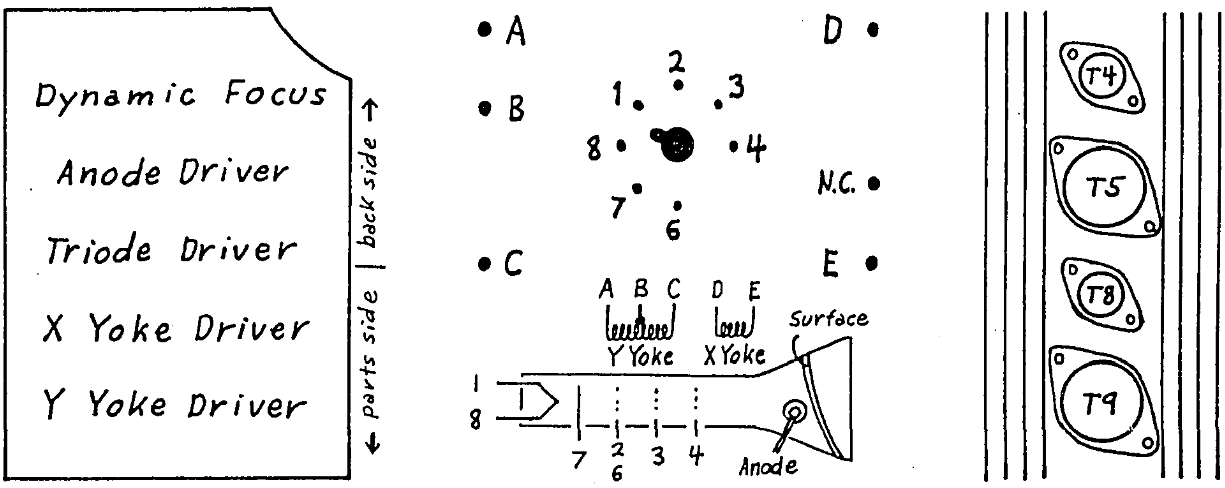


Figure 5.4 Logic Module Boards Interconnections

Display Module

The Display Module is an ultra-precision specialized oscilloscope. It positions an image on a 19" screen with a drift of about 20 micro meters. The spot area relative to screen size is about 1/30 that of a typical oscilloscope, and can be reduced to 1/1000 by use of a high-resolution CRT, which the circuitry has the quality to support. The beam intensity is logarithmically controllable over many orders of magnitude.

The display module is mounted on a copy-camera modified for easy mounting of diverse experimental apparatus.



PCB Placement viewed from above

19VERP4 CRT & Yoke viewed from back

Transistors (one of two) viewed from outside

Figure 5.5 Display Module Physical Layout

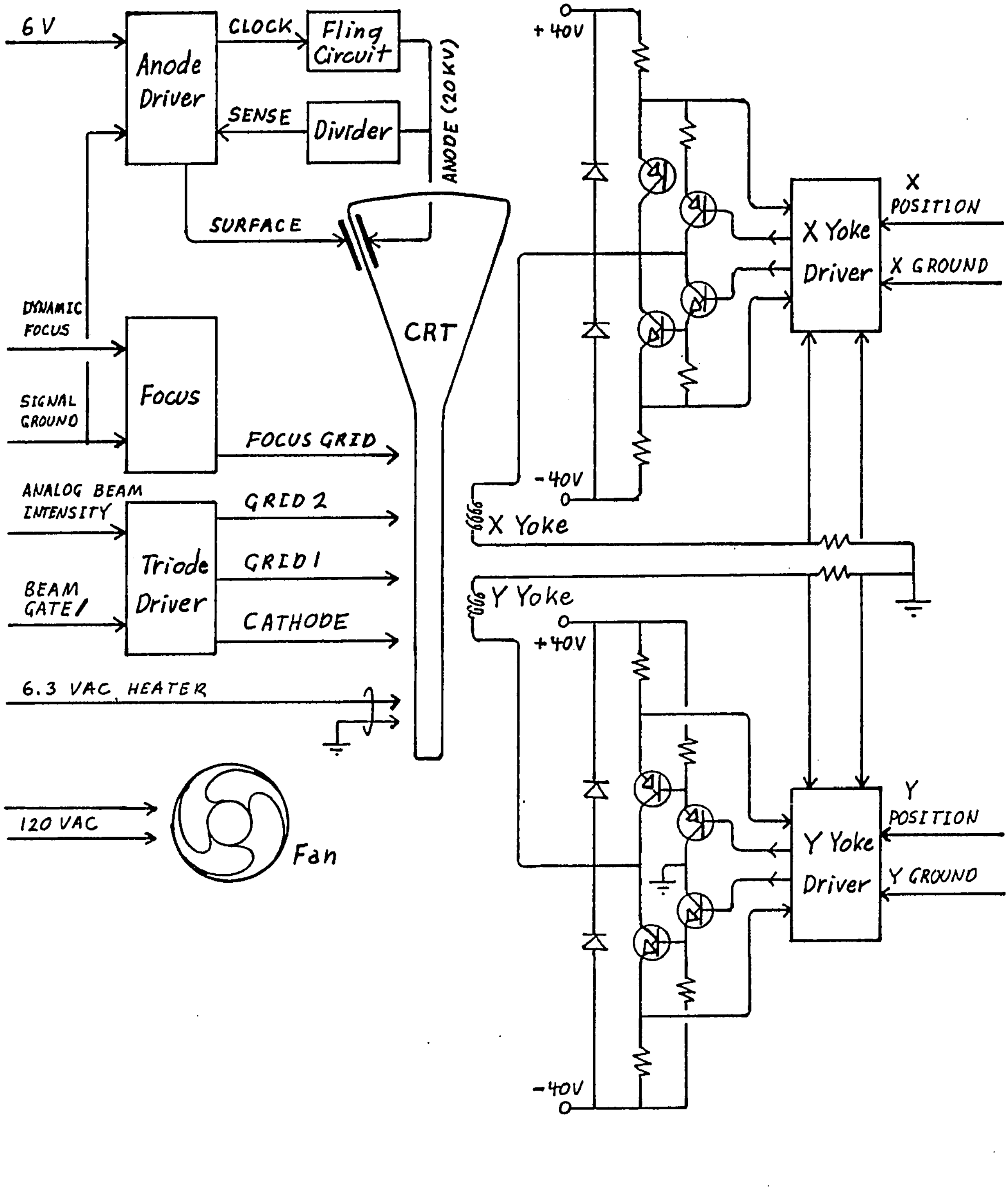
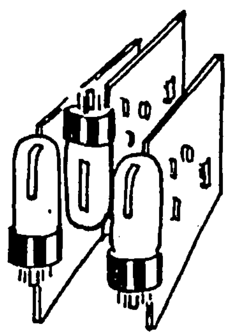


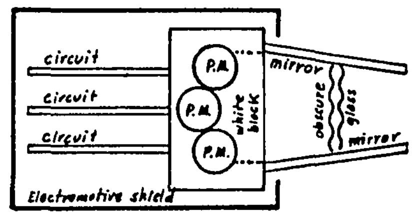
Figure 5.6 Display Module Interconnections

Photosense Modules

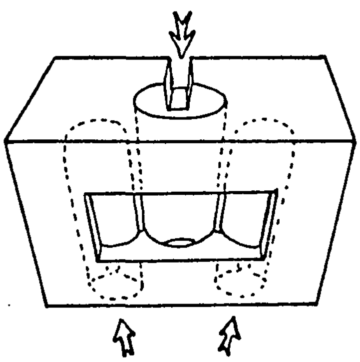
There are at least two Photosense Modules, each containing one or more photomultipliers and associated Photosense Boards. Each module senses illumination at one or more colors, angles, polarizations, etc, integrates illumination on command, and outputs a high-level analog signal to the Logic Module.



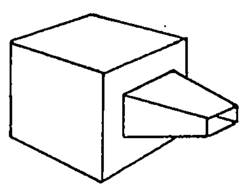
Photomultipliers very close to each other and circuit boards



Arrangement of circuit boards, photomultipliers, white block, EMI shield, and mirror light guide and integrator



Light conserving white block into which photomultipliers are inserted



Completed module

Figure 5.7 Photomodules Physical Layout

Power Module

For protection of the scanner, voltages supplied by the Power Module should have the following characteristics:

During powerup. The +340V source is held at ground for 30 seconds to allow logic stabilization and cathode warmup before beam current is drawn. The -340V source should however rise rapidly.

During powerdown. The +340V source should be rapidly grounded to prevent failing voltages from deblanking the beam. The -340V source should fail slowly.

Always +15V > +5V, and +5V, and 15V, and -15V should be overvoltage protected. Other voltages may be unregulated from the power line through transformers and therefore can not go appreciably overvoltage. Series fused relays should:

1. Fuse the logic supply section (+5V, +15V, +30V, +50V, -15V, -30V, -50V)
2. Fuse and allow deflection supply section (+40V, -40V) only if the logic supply section is operating. ±30, ±50 are relative.
3. Fuse and allow the high voltage section (+150V, +340V, -340V, +1,500V) only if the deflection supply section is operating. If deactivated, +340V should be rapidly grounded, -340V should fail slowly.

Requirements on the +340 volt supply are satisfiable with an SPDT relay. Fuse sequences are satisfiable with three fuses and one SPST relay.

Need for 16-Bit Positional Control

With a high-resolution CRT, the spot size will be 1/4000 the image height, coincidentally the step size of a 12-bit converter. Why are two very expensive 16-bit converters needed? The answer is not found in resolution limits, but rather in grey-scale reproduction. The converter will introduce a textile-like pattern. The seriousness of this problem will now be estimated.

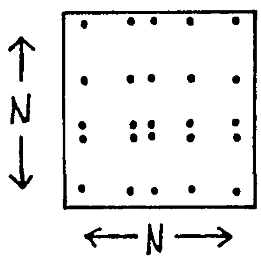
Working in units of one LSB, quantization errors of the D/A converter are:

RMS Arithmetic Error = $1/2\sqrt{3}$ (pure rounding error)

Differential Linearity Error = $1/2\sqrt{3}$ (uniformly distributed $-\frac{1}{2}$ to $+\frac{1}{2}$)

Total error = $1/\sqrt{6}$

To calculate noise, consider a block of N X N elementary pixels. The positional uncertainty can be considered an uncertainty in integration limits, because the error is not cumulative.



mean brightness = N^2 = signal

$$\text{Uncertainty} = \sqrt{4 \cdot \left(N \cdot \frac{1}{\sqrt{6}}\right)^2} = \frac{2N}{\sqrt{6}} = \text{noise}$$

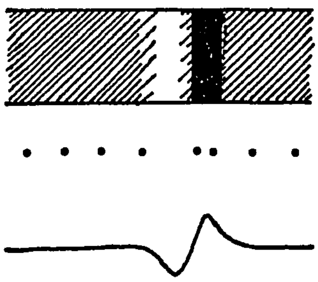
$$\frac{\text{noise}}{\text{signal}} = \frac{2}{N\sqrt{6}} \propto \frac{1}{\sqrt{\text{Area}}}, \quad \therefore \text{noise is white.}$$

Kodak measures film granularity with a 48 μm circular aperture, an area equivalent to 1/564 the height of a 35 mm film. In such a linear dimension there are 87 LSB steps from a 16-bit converter, from which the RMS noise/signal can be calculated from the above formula to be

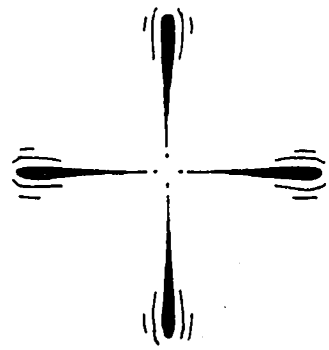
9.4×10^{-3}, comparable with 35 mm Kodachrome 64 color slide film. The textile pattern will be just perceptable.

The same answer can be obtained by calculating the RMS noise of an elementary pixel by assuming constant light spread over a variable two-dimensional step size. Because the error is non-cumulative, the error in one axis is "blue" noise, and that in the other is "pink", the two effects canceling.

The RMS noise calculation is more involved than presented above, and many assumptions need to be made. Each elemental error produces a double impulse, as shown below.



This produces a 6db/octive boost of the higher spatial frequencies up to the sampling frequency. The 2D spatial frequency noise spectrum is thus:



The integral of the noise in a circle of equal frequency is proportional to the frequency, demonstrating that the noise is white.

Note that the Fourier transform of the square aperture also contains perpendicular arms matching the noise response. In fact, if the equations had been presented for the RMS noise in the square rotated 45^o, the noise would have faded to insignificance. The calculation of noise using a semi-matched filter is justified because the pattern recognition mechanism of the eye performs a similar function, as demonstrated by astronauts' ability to detect straight patterns from space that would normally be considered below the noise level. This scanner will allow research such as this to be given an empirical basis.

Some final comments:

1. In linear scan the RMS error is reduced by $\sqrt{2}$.
2. If the D/A is well trimmed, this is reduced further.
3. The discussion above applies to outputting an image. The effect on an input image is much less and more subtle. It is analogous to aperture error time in A/D sampling.

Sensing Color

A direct approach of sensing color selects distinct orthogonal spectral bands by filtering. Commonly bright red, green, and blue filters are used. God did not choose this approach in designing the human eye. Instead of finding three brightly colored dyes in the color sensitive comes of the eye, researchers found unexpected and weak colors. The spectral sensitivity of the red and green sensors of a standard observer are plotted below with arbitrarily normalized red deemphasized to illustrate:

1. Red and Green sensors have a constant sensitivity ratio in red light, which is experimentally verified to extend to the ultimate visual threshold deep in infra-red.

2. This response suggests two equal "yellow" sensors, one with no filter, the other with an orange, not red, filter.
3. Pure red is apparently visualized via algebraic separation.

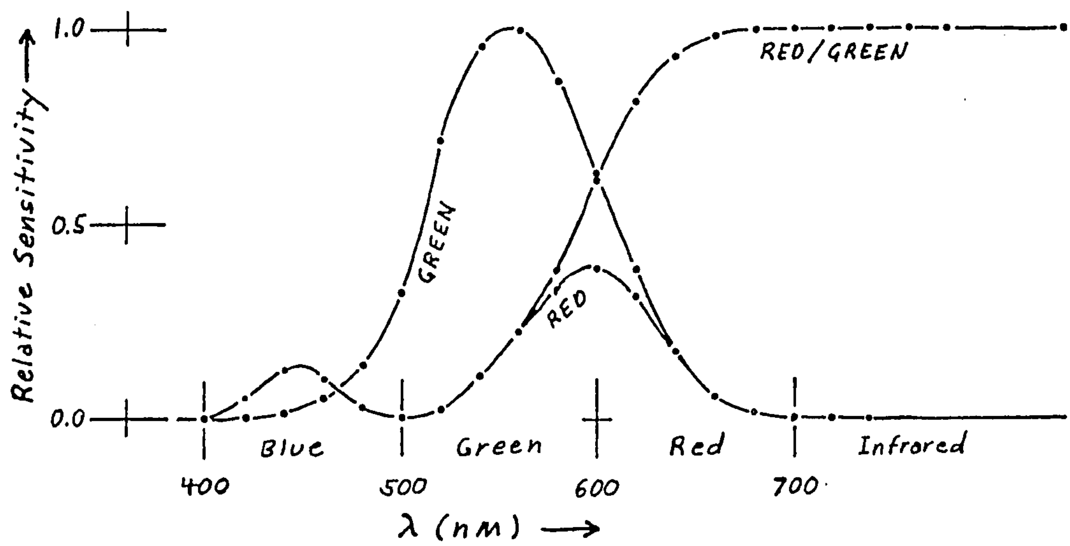


Figure 5.8 Standard Trichrometric Observer

The use of these weak filters with algebraic reconstruction provides less noise, or "grain", at a given level of illumination. To illustrate this mathematically, the problem environment is first established:

1. Three identical sensors are available. Consider only their response to red and green light. A phosphor-photocathode combination is sensitive to 1 part green and .25 part red.
2. A red filter passes 100% red and no green. A typical green filter passes 50% green and no red.
3. Red, green, and yellow sensors are formed by obvious combinations of sensor and filters.
4. From any two sensors, red, green, and yellow channels can be

produced by algebraic manipulation.

5. Quantum noise $\propto \sqrt{\text{illumination}}$ (It is interesting to note that when the photo-signal falls below the background signal then quantum noise approaches a constant. Fractional noise then rises twice as fast with failing light, explaining a rather abrupt "threshold" of photosensors.)

Three sensors are now available:

Sensor		Sensitivity (Red)	Sensitivity (Green)	Relative Absolute Noise
Red	(R)	.25	.0	$\sqrt{.25} = N_R$
Green	(G)	.0	.5	$\sqrt{.5} = N_G$
Yellow	(Y)	.25	1.0	$\sqrt{1.25} = N_Y$

We can produce three channels from the R and G sensors:

Color	Mixture	Relative Fractional Noise
Red	4·R	$4 \cdot N_R/1 = 2$
Green	2·G	$2 \cdot N_G/1 = 1.4$
Yellow	2·R + 1·G	$\sqrt{(2 \cdot N_R)^2 + (N_G)^2}/1 = 1.2$

We can produce three channels from the R and Y sensors:

Color	Mixture	Relative Fractional Noise
Red	4·R	$4 \cdot N_R/ 1 = 2$
Green	1·Y − 1·R	$\sqrt{N_Y^2 + N_R^2}/ 1 = 1.2$
Yellow	.5·Y + 1.5·R	$\sqrt{(.5 \cdot N_Y)^2 + (1.5 \cdot N_R)^2}/1 = .9$

The above demonstrates an improvement in signal to noise ratio by using the indirect approach of R and Y sensors with algebraic reconstruction. The critical luminence (Y) channel signal to noise ratio is improved over 2 dB. Near threshold, the gain is greater. This simplified example assumes discrete colors. Taking advantage of color blending, further improvement is possible, although precise color tracking is complicated.

The filters chosen are determined by the phosphor - photocathode combination. As a guide, the following combinations are suggested:

1. White sensor and orange filter (RED)
2. White sensor and no filter or yellow filter (WHITE)
3. Blue sensor and no filter or pale purple filter (BLUE)

For technical purposes "false color" sensitivity combinations often display information not apparent under true color. In aerial and medical photography the combination of green, red, and infrared is often used. In microscopy, many specimens are excessively transparent to red light, and vital resolution is extended by ultraviolet. The combination orange, blue-green, and ultraviolet is suggested.

Alignment

Operation of proposed key software alignment programs is outlined. By allowing alignment to be checked and aided with software, the hardware design gives the user a powerful tool to easily maintain peak performance. The scanner supports diverse alignment programs to be generated as needed.

Rectilinearity Alignment

A precision grid is scanned to determine the Cartesian address of each node. Such scanning is simplified by contextual random search estimating the next node. Based on this data, the resistors in the matrix of the Summer Board giving the best fit to the precision grid can be mathematically determined. Alignment encompasses the entire optical system.

Dynamic Focus Alignment

An auxiliary D/A output injected to the Summer Board allows the software to incrementally modify the focus anode voltage. By using a standard image grid, the modulation transfer function of the scanned spot can be calculated, and using this the optimum focus voltage can be found for each point. The resistors in the Summer Board giving the best focus fit can then be mathematically determined. A modification of this procedure allows mechanical focus to be checked or adjusted with a stepper motor.

16-Bit D/A Alignment

Grey-scale reproduction is limited by the differential linearity of the two 16-bit D/A converters, therefore alignment is critical. Software can output a value for X and Y that will produce approximately equal voltages after distortion correction. Then by reading the 256 · (X-Y) channel, with allowance for slow settling caused by high gain, software can determine the step size of either converter. By knowing the step size of 15 key states at the four highest order carries, software can inform the user how much to turn each of the trimming potentiometers in the 16-bit converters.

Beam Intensity Alignment

The Beam Intensity Board allows both the logarithmic slope, via P1 controlled log gain, and low intensity linearity, via P2 controlled V_C, to be adjusted. Software can monitor logarithmic tracking of beam intensity and guide adjustment of each potentiometer. As beam intensity is varied over many orders of magnitude, exposure is maintained in a useable range by varying the deblanking time. The program must not test current levels sufficient to burn the phosphor with the minimum deblanking time, and must allow sufficient time between high intensity pulses for heat dissipation. The program should randomly select test points to randomize aging, but must use the same point for testing all intensities in one sequence. An alternative scheme pulses the beam while it is slewing.

CHAPTER VI

CIRCUITRY OF THE MICRO-OPTICAL TOMOGRAPH

This chapter attempts to clearly document and explain all of the scanner circuitry. Significant advances to the state of the art are also disclosed that permit the scanner characteristics defined in previous chapters. Theoretical development of advances provide interest transcending that of specific circuits.

All circuit layouts are drawn freehand at 2.5x on graph paper, with no straight edge, hole guide, or transfers used at any time, giving a unique and aesthetically pleasing style. This method gives the designer total freedom to dynamically balance interconnect density, resistance, and capacitance, and in cost-critical production applications to extend etchant life several fold. The reader may also note the scarcity of crossovers, shortness of most conductor paths, protection of critical analog signals, and closed looping of most ground nets.

Bus Logic Board

This board interfaces the MDS-800 microcomputer bus with the scanner.

Connections

READ BUS — 8-bit positive logic data is inverted and placed on computer bus when a correctly addressed Memory Read

	command is executed
WRITE DATA BUS	8-bit data on computer bus is inverted and output in positive logic
MEMORY WRITE/	Low when a correctly addressed Memory Write command is executed
MEMORY READ/	Low when a correctly addressed Memory Read command is executed
IO WRITE/	Low when a correctly addressed IO Write command is given
COLOR	High when a correctly addressed IO Write command is given
SELECT	4-bit positive logic address selects proper peripheral device to respond
+5V	Output power from computer bus. This is not a power input.

Operation

The scanner sees two one-way data buses: The WRITE bus, named from the computer's viewpoint, carries 8-bits of data from the computer. The READ BUS carries 8-bits of data to the computer. A 4-bit SELECT acts as an address, which with the four commands listed above evoke various responses from the scanner.

The 8080 computer views the scanner through the Bus Logic Board as 32 output ports and 16 memory locations from which data may be read or to which data may be written.

The Bus Logic Board provides the necessary interface, including

1. base address selection
2. response to addresses in range only
3. transfer-acknowledge logic and optimal advance-acknowledge
4. inhibition of RAM at 16 coincident addresses

5. command decoding
6. output buffering to drive longer transmission lines
7. low logic drain to satisfy bus requirements

A memory read evokes the following responses if memory base ≤ address ≤ memory base + 15

1. XACK to computer bus
2. optional AACK to computer bus
3. INHI to computer bus
4. 8-bit READ DATA from scanner inverted to computer bus
5. MEMORY READ/ to scanner goes low

A memory write evokes the following responses if memory base ≤ address ≤ memory base + 15

1. XACK to computer bus
2. optional AACK to computer bus
3. MEMORY WRITE/ to scanner goes low

An IO write evokes the following responses if IO base ≤ address ≤ IO base + 15

1. XACK to computer bus
2. IO WRITE/ to scanner goes low

An IO write evokes the following responses if IO base + 16 ≤ address ≤ IO base + 31

1. XACK to computer bus
2. COLOR to scanner goes high

Continuously the following occurs

1. 8-bit DATA/ from computer bus inverted to WRITE BUS of scanner
2. 4 least significant bits from 16-bit ADR/ address from computer bus inverted to SELECT of scanner

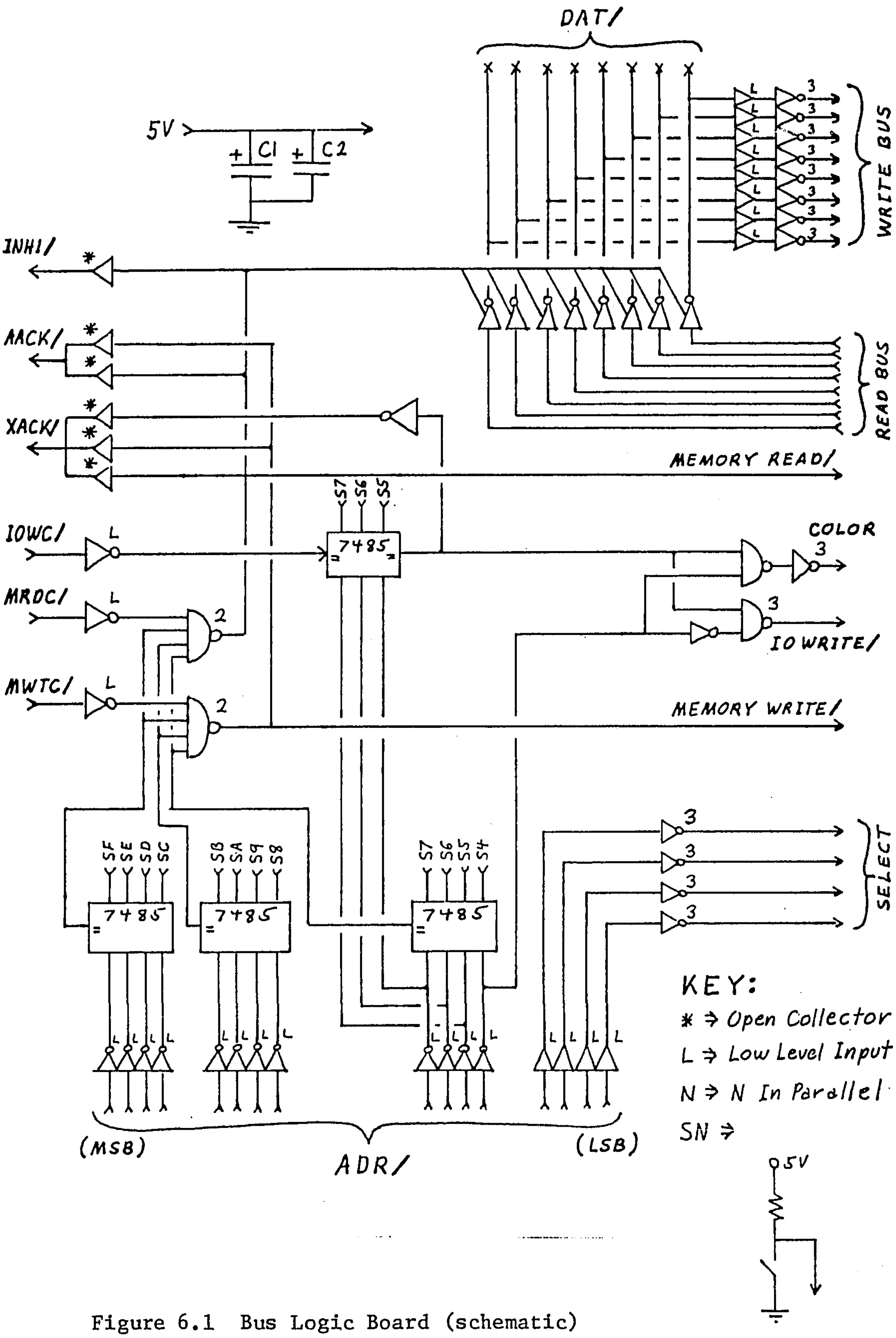


Figure 6.1 Bus Logic Board (schematic)

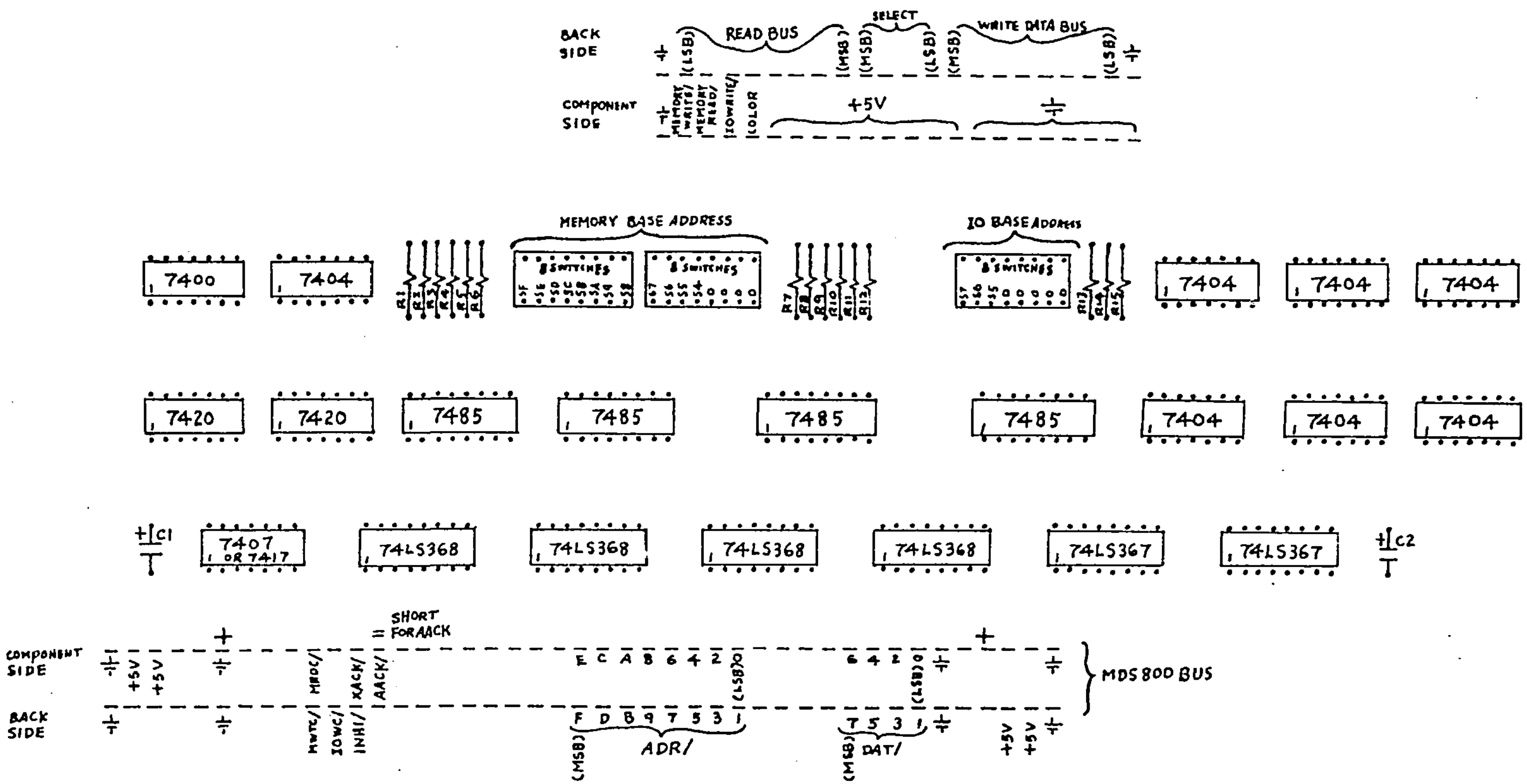


Figure 6.1 Bus Logic Board (components)

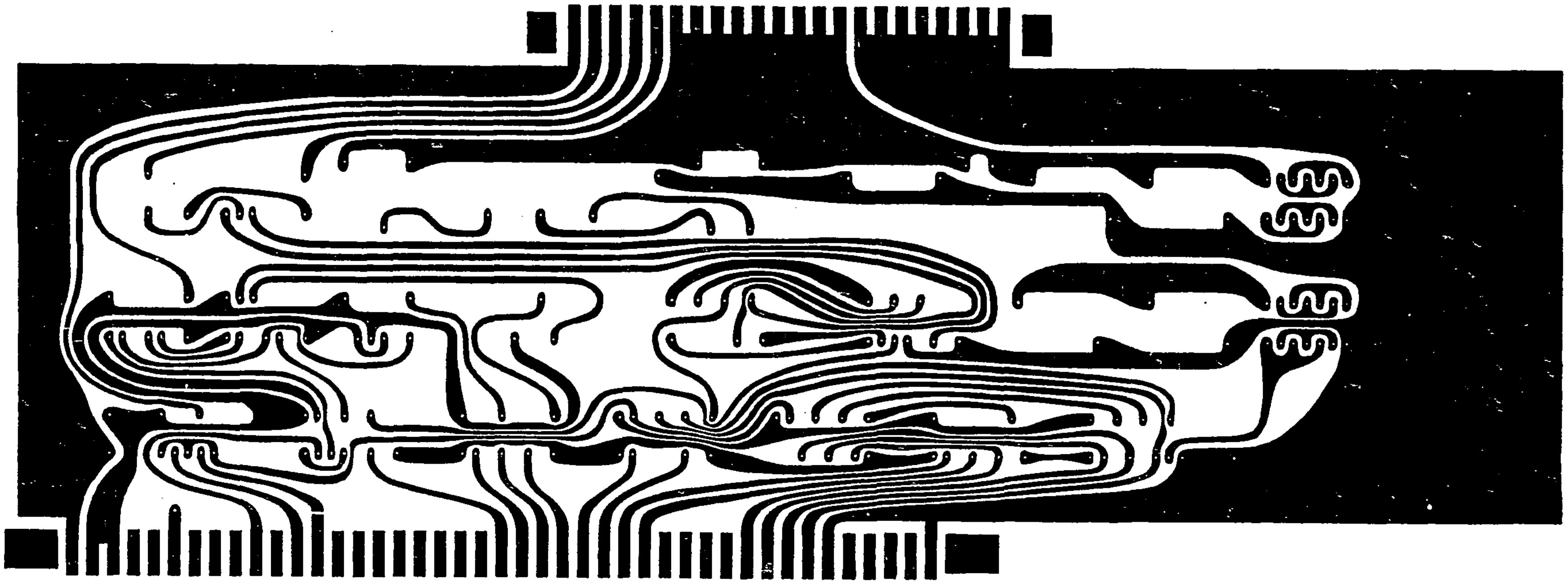


Figure 6.1 Bus Logic Board (parts side)

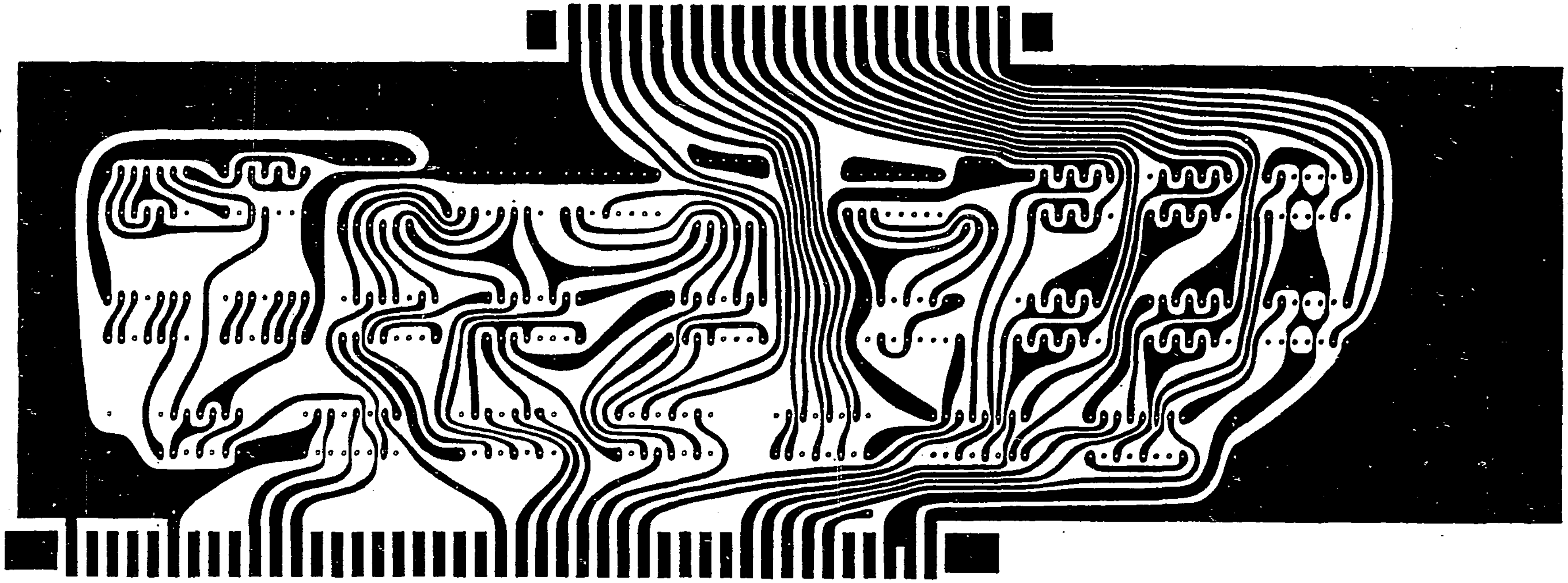


Figure 6.1 Bus Logic Board (back side)

Adjustments

Memory base address = MMMMMMMM MMMM0000

IO base address = SSS00000

where "M" and "S" are switch selectables. See PCB layout for switch locations.

AACK may be suppressed by breaking connection at point shown in the PCB layout. This delays memory I/O commands an additional cycle, ~ 0.5 μsec.

Multiplexer Boards

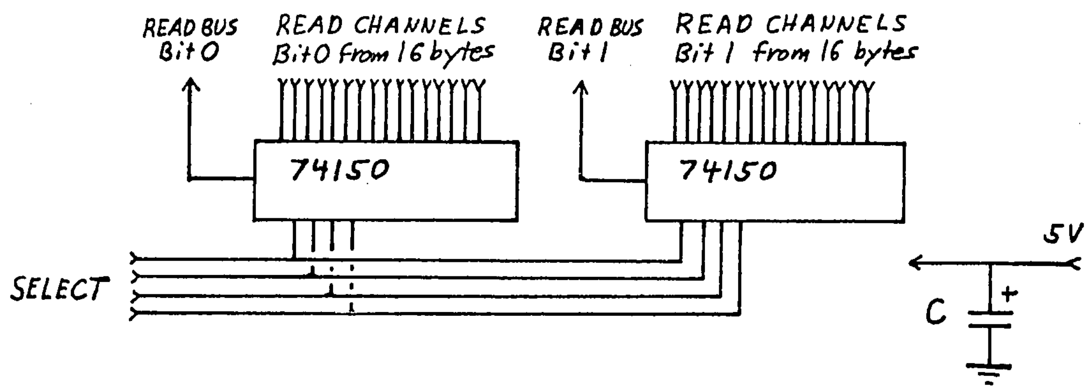
One of 16 8-bit bytes is selected by the 4-bit SELECT and placed on the READ BUS. Each of the 4 boards multiplexes a 2-bit slice.

Connections

SELECT 4-bit positive logic address. "0000" selects READ CHANNEL 0.

READ CHANNELS Each side of the board presents a 1-bit slice of 16 bytes. When 4 boards are arranged in parallel, all 8-bits of each byte are linearly aligned

READ BUS Each side of the board presents the corresponding single bit of the READ BUS. The multiplexer boards invert the data, therefore, although Scanner Module boards will input positive logic from the WRITE BUS, they will output negative logic to the READ BUS through the Multiplex Boards.



Repeated for bits 2-3, bits 4-5, and bits 6-7 for 4 boards

Figure 6.2 Multiplexer Boards (schematic)

Command Decoder Board

The 4-bit SELECT address with IO WRITE/ and MEMORY WRITE/ are decoded into one of 32 possible commands that can be given to the scanner.

Connections

SELECT	4-bit positive logic address. "0000" selects COMMAND 0
MEMORY WRITE/	Low activates a MEMORY WRITE COMMAND, one of 16
IO WRITE/	Low activates an IO WRITE COMMAND, one of 16
MEMORY or IO WRITE COMMANDS/	Together comprise 32 possible commands. The one selected goes low.

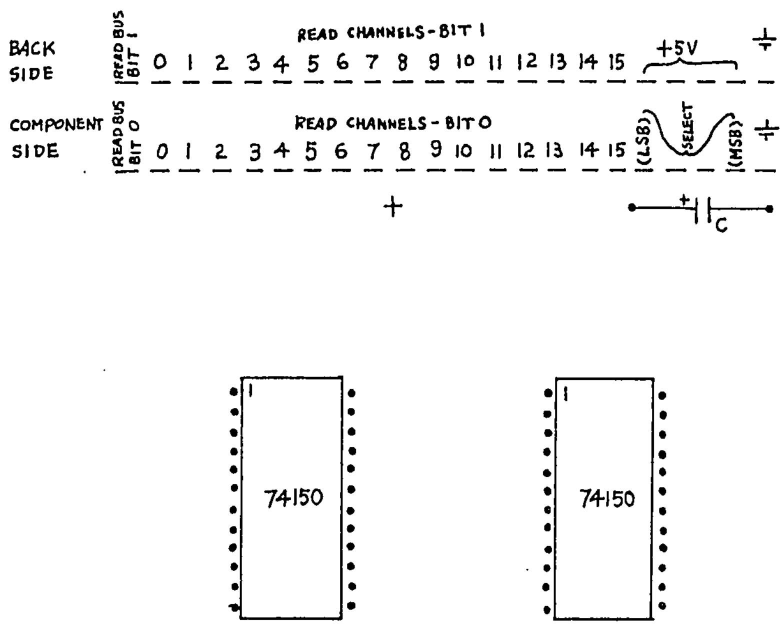


Figure 6.2 Multiplexer Boards (components)

Figure 6.2 Multiplexer Boards (parts side)

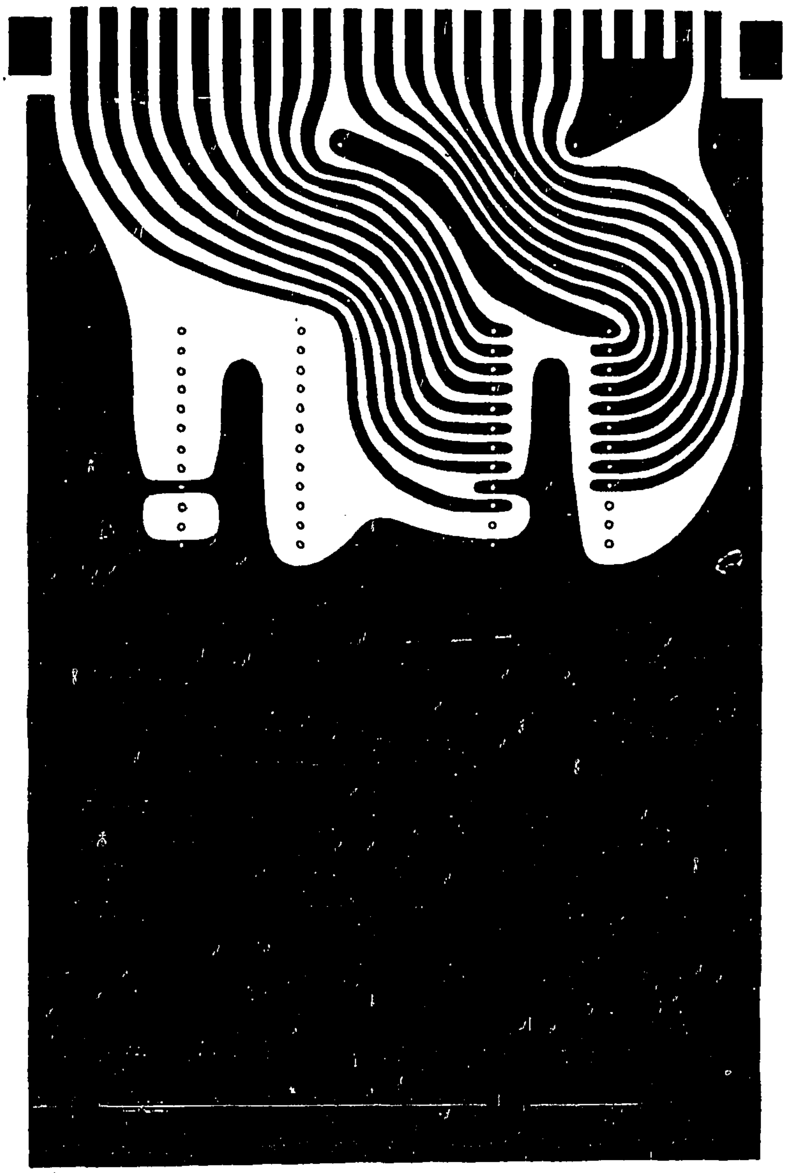


Figure 6.2 Multiplexer Boards (back side)

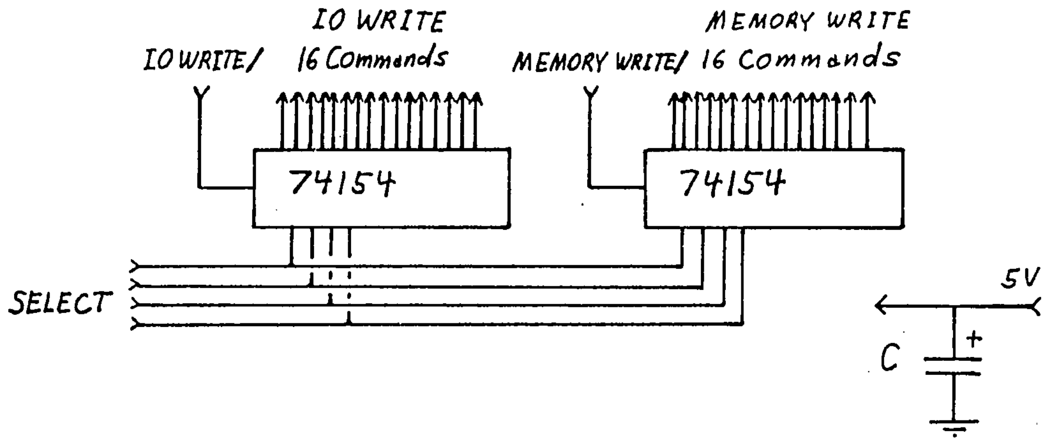


Figure 6.3 Command Decoder Board (schematic)

Beam Intensity Board

This board provides D/A conversion for CRT spot intensity. It inputs a two-byte FOCUS 10.10 coded number and 4 CRT beam-control commands. It outputs to the CRT associated circuitry a logarithmic analog signal for controlling CRT beam intensity and a digital bit to gate the CRT beam on or off. The FOCUS-coded input number is returned modified to reflect the conversion range.

Connections

WRITE BUS	8-bit positive logic input data port
BEAM INTENSITY HIGH BYTE	When low, WRITE BUS is transferred into high byte of 16-bit beam intensity data register.

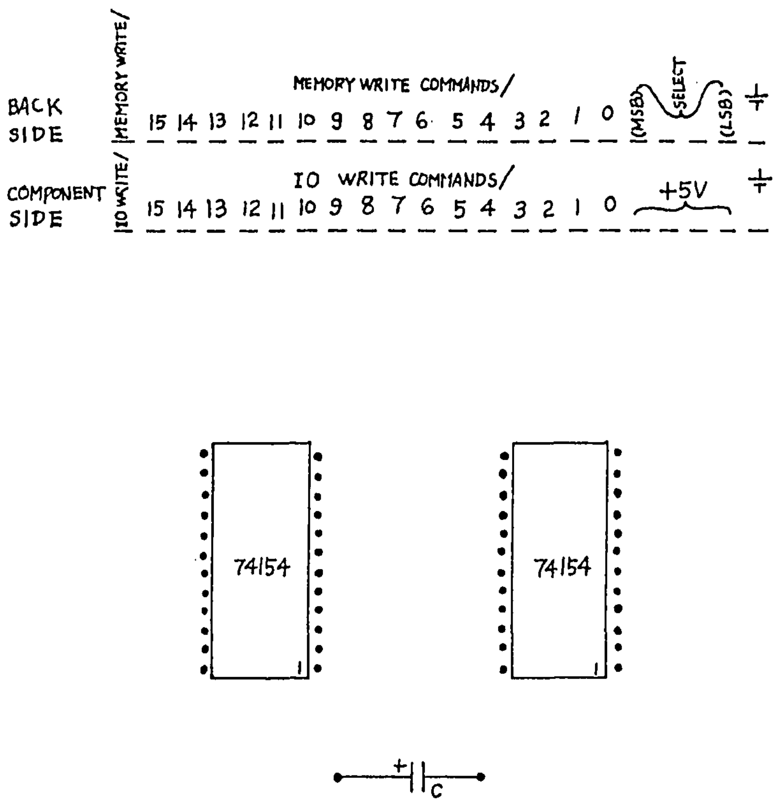


Figure 6.3 Command Decoder Board (components)

Figure 6.3 Command Decoder Board (parts side)

Figure 6.3 Command Decoder Board (back side)

BEAM INTENSITY LOW BYTE	When low, WRITE BUS is transferred into low byte of 16-bit beam intensity data register.
READ INTENSITY/	16-bit, 2-byte negative logic output of data in beam intensity register. If the number is out of range, it is modified in certain ways described later.
ANALOG BEAM INTENSITY	Analog output to CRT associated circuitry. A higher voltage implies a brighter beam. The dynamic range is -5V to +5V, logarithmic, with 5V implying 4 orders of magnitude.
BEAM GATE/	Digital output to Display Module. When low, CRT beam is to be unblanked.
STROKE BEAM CONTROL	When high, the beam is to be unblanked for as long as it remains high. Care should be taken to protect this input from an open circuit.
1 USEC BEAM PULSE/	On the falling edge, the beam is unblanked for 1 μsec
10 USEC BEAM PULSE/	On the falling edge, the beam is unblanked for 10 μsec
100 USEC BEAM PULSE/	On the falling edge, the beam is unblanked for 100 μsec. The beam inhibit of the next section suppresses all 4 of the above controls.

Operation

As viewed from the 8080 computer through the bus logic circuit, the beam intensity board appears as two adjacent bytes of memory to which data can be written or from which data can be read, individually or sequentially in any order. The data is modified to reflect the allowable range of beam intensities, and the modified number passed to the D/A and back to the computer when a read is executed. The data modifications, applying to FOCUS 10.10 coding, are shown:

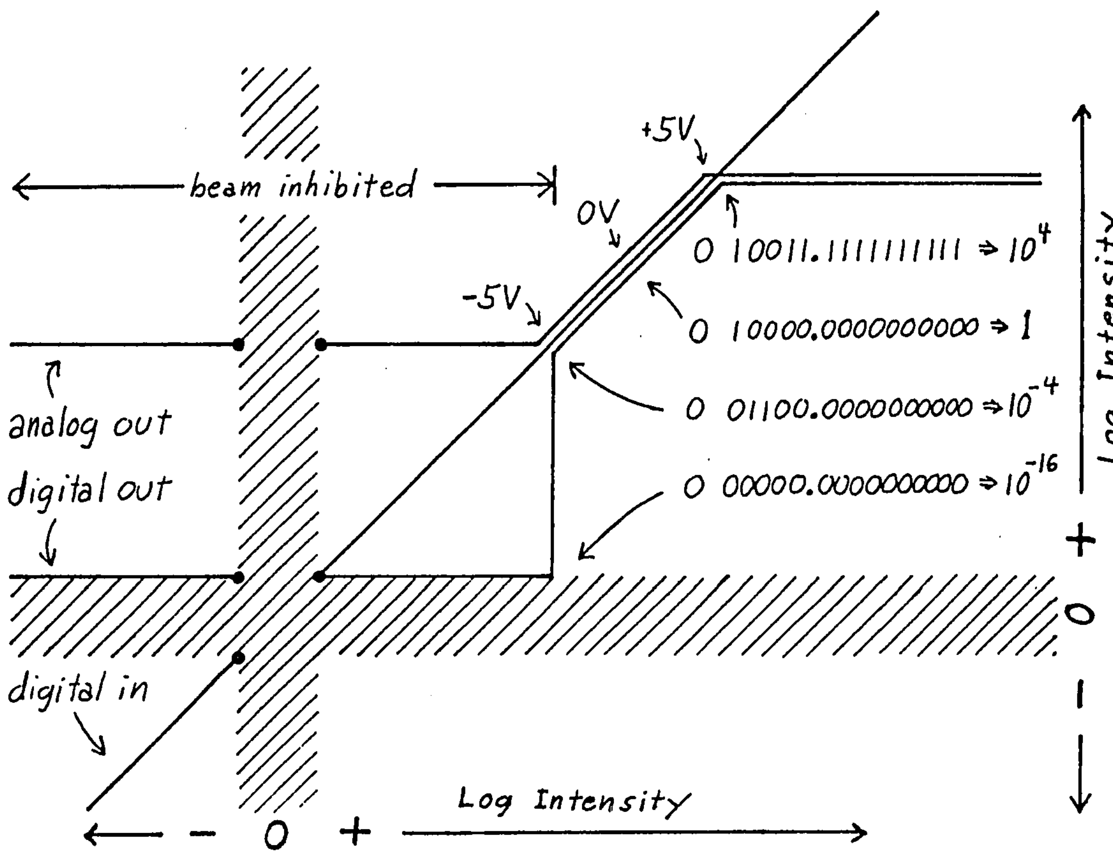


Figure 6.4 Beam Intensity D/A I/O Relationships

The digital output indicates the actual beam intensity that can be delivered to the phosphor screen. The suppression of modulus jumping to the D/A provides rapid settling for intensities transecting threshold.

After setting the 16-bit intensity, the beam is unblanked for a specified interval by calling one of the three output ports. The data is ignored. The deblanking times of 1, 10, and 100 μsec provide uniformly scaled steps on a logarithmic scale equivalent to adding or subtracting 00000100 to the most significant byte of the 16-bit FOCUS 10.10 coded intensity data. By allowing lower beam currents, the 100 μsec option provides the sharpest image, however with high beam currents this is sufficient time to burn the phosphor.

The separate intensity and timed gate beam controls provide the following advantages over other choices of control:

Safety — If the beam were software toggled and either a turn-off instruction were omitted or the computer interrupted before the instruction was executed, the CRT phosphor could be burned within 100 μsec. The undeflected beam can cut through the glass faceplate in a few seconds causing an implosion with potential personal injury. For certain applications the automatic turn-off can be suppressed by pulsing the retriggeable timer in a loop, however this requires additional steps to be added, rather than a step forgotten as with a toggled system, and so is unlikely to be done accidentally.

Accuracy — Separate intensity and gating controls allow a moment for the D/A and special gamma correction circuits in the CRT associated circuitry to settle grid 1 voltage before the beam is deblanked by grounding the cathode. Because of logarithmic coding and $\frac{7}{2}$ gun power characteristics, small overshoots or D/A "glitches" would otherwise have large and unpredictable effects.

Speed — Because the beam intensity is often held invarient, a single instruction can pulse the beam.

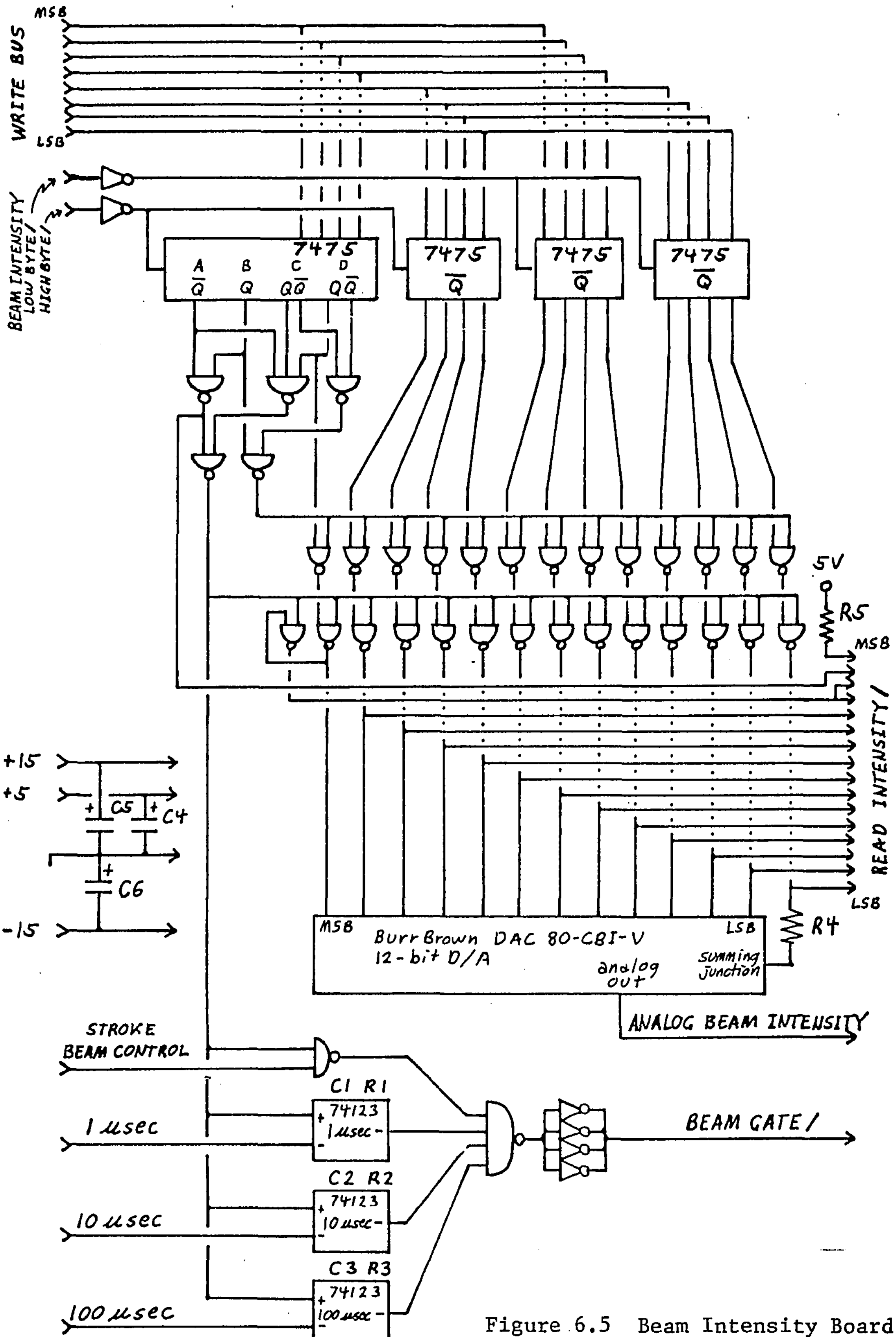


Figure 6.5 Beam Intensity Board (schematic)

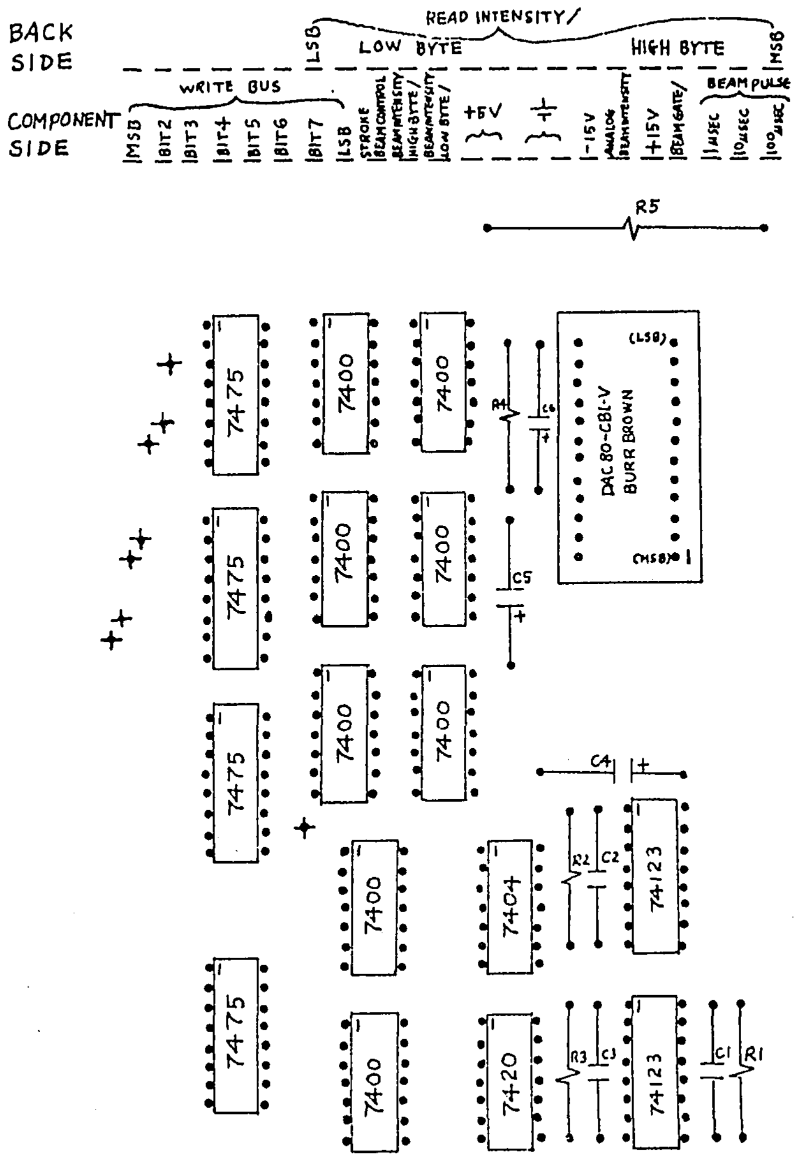


Figure 6.5 Beam Intensity Board (components)

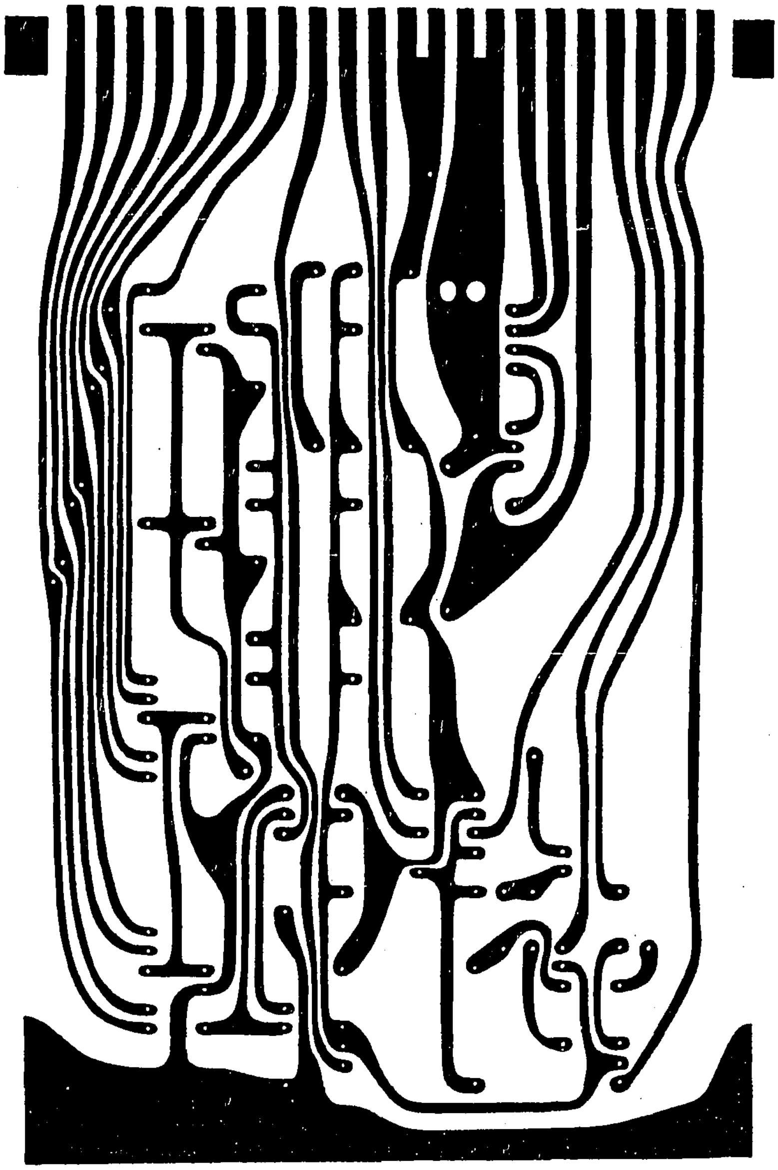


Figure 6.5 Beam Intensity Board (parts side)

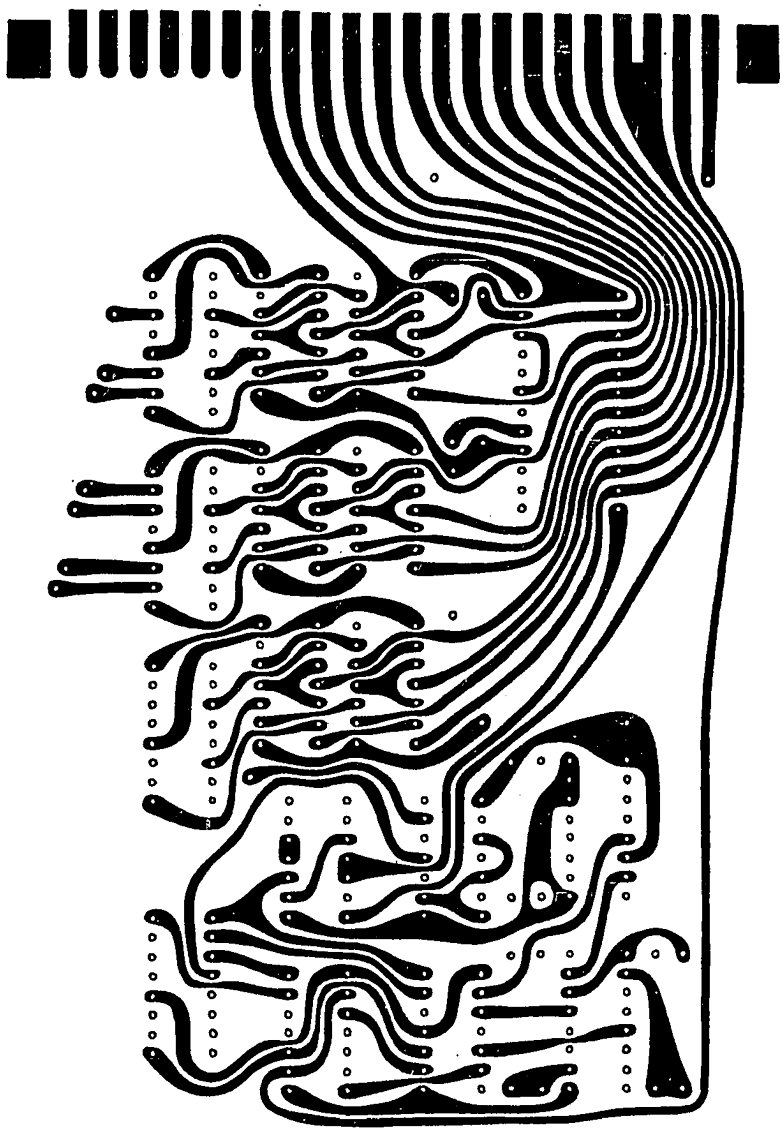


Figure 6.5 Beam Intensity Board (back side)

With FOCUS 10.10 the specified range of beam intensity requires a 13-bit D/A converter. Because the least significant bit is below the detection and computational noise it may be ignored, allowing use of a 12-bit D/A. The 13th bit of resolution is added with a resistor to the summing junction, however the differential accuracy remains that of the 12-bit converter.

X-Position D/A Board

This board and the similar Y-Position D/A Board provide precision 16-bit D/A conversion of the spot position. Special timing allows maximum input flexibility and is compatible with the Transient Filter Board. Standard reference voltages are buffered and output.

Connections

WRITE BUS	8-bit positive logic input data
X POSITION HIGH BYTE/	When low, WRITE BUS is transferred into high byte of 16-bit X-position register
X POSITION LOW BYTE/	When low, WRITE BUS is transferred into low byte of 16-bit X-position register
READ X POSITION/	Negative logic 16-bit output of X-position register
+6V OUT	Buffered output of D/A converter's precision reference voltage
-6V OUT	Inverted +6V precision reference
RAW X POSITION	Analog output converted from 2's complement input: IN = 1000000000000000 OUT = -10V IN = 0000000000000000 OUT = 0V IN = 0111111111111111 OUT = +10V

Operation

As viewed from the 8080 computer through the bus logic circuit, the X-Position D/A Board appears as two adjacent memory locations. Data may be output to either memory location individually or to both in either sequence. Restrictions are:

1. If both bytes are changed, for best results the two bytes should be written within 5 μsec of each other (SHLD instruction).
2. At least 10 μsec idle time should be allowed before a new position is specified.

After ½ μsec the data may be read back unaltered as from any other memory location. The spot moves to the position specified by the 2's complement concatenation of both memory locations with the highest address supplying the most significant byte.

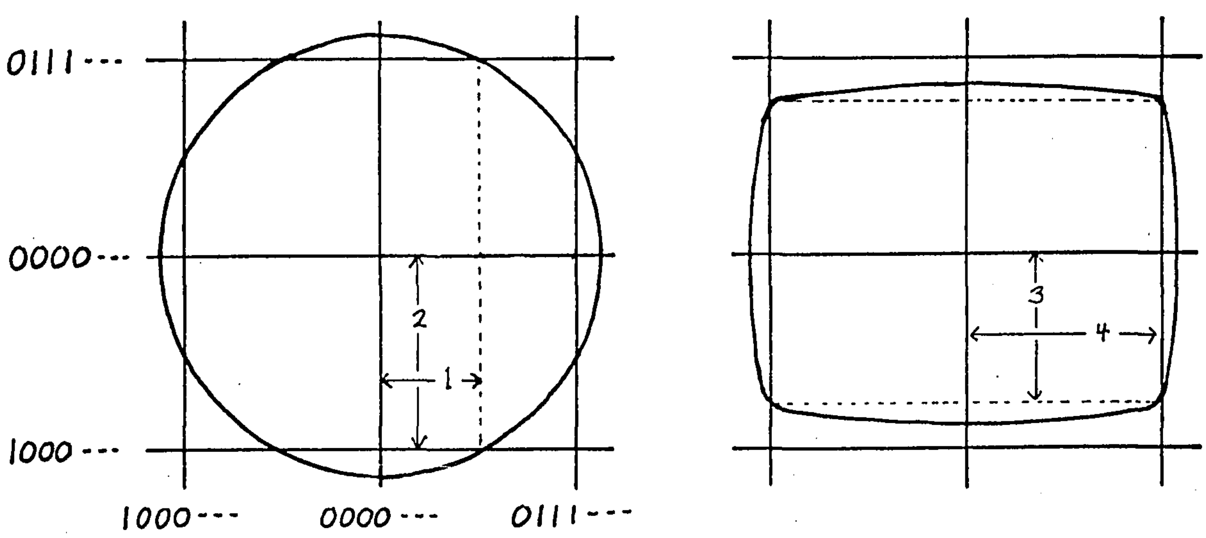


Figure 6.6 Addressable Range

Timing

Diagrams presented in this section describe the combined effects of the X Position D/A and Transient Filter Boards.

Accuracy and response speed characteristics have some unique requirements in image processing. They are discussed in increasing order of importance:

1. Positional distortion of the D/A circuit has no noticeable effect on the image. An introduction of even 10,000 ppm X^2, for example, is not visibly apparent.
2. Settling time is important in random scan applications, or during retrace, however in normal scanning, a 50% settling is quite adequate to initiate sensing. In flying-spot scanners the beam never settles, but is always moving.
3. Uniform switching transients effectively widen the spot size if in effect during sensing, however if they are less than the spot width, they can be lived with.
4. Random transients are catastrophic to image quality. As shown in the section "Need for 16-Bit Positional Control" in Chapter V, they should be settled to within ½ LSB = 0.001 % prior to exposure. Unfortunately, D/A converters have strong random transients generated because different bits switch at unpredictably different times. Once these transients reach the deflection yokes they take a very long time to settle to the required level.

Point 4 is almost eliminated by the Transient Filter Board. The open-loop differential sample & holds eliminate the random transients of closed-loop designs, and also substantially reduce the uniform transients of point 3 normally associated with S/Hs. The transient Filter

Board isolates the D/A from the yoke circuitry about 180 nsec after the falling edge of either X POSITION LOW BYTE/ or X POSITION HIGH BYTE/, and remains open for 6 μsec. The 6 μsec timer is retriggerable, so if two bytes are transferred, there will be 6 μsec wait after the last byte for the D/A to settle. The X-Position D/A Board has two 16-bit registers. The first is used to separate and store the incoming 8-bit bytes. The second is a buffer that remains fixed during the first 500 nsec after a command is received to allow time for the Transient Filter Board to interrupt the signal path. The register then opens, allowing the new

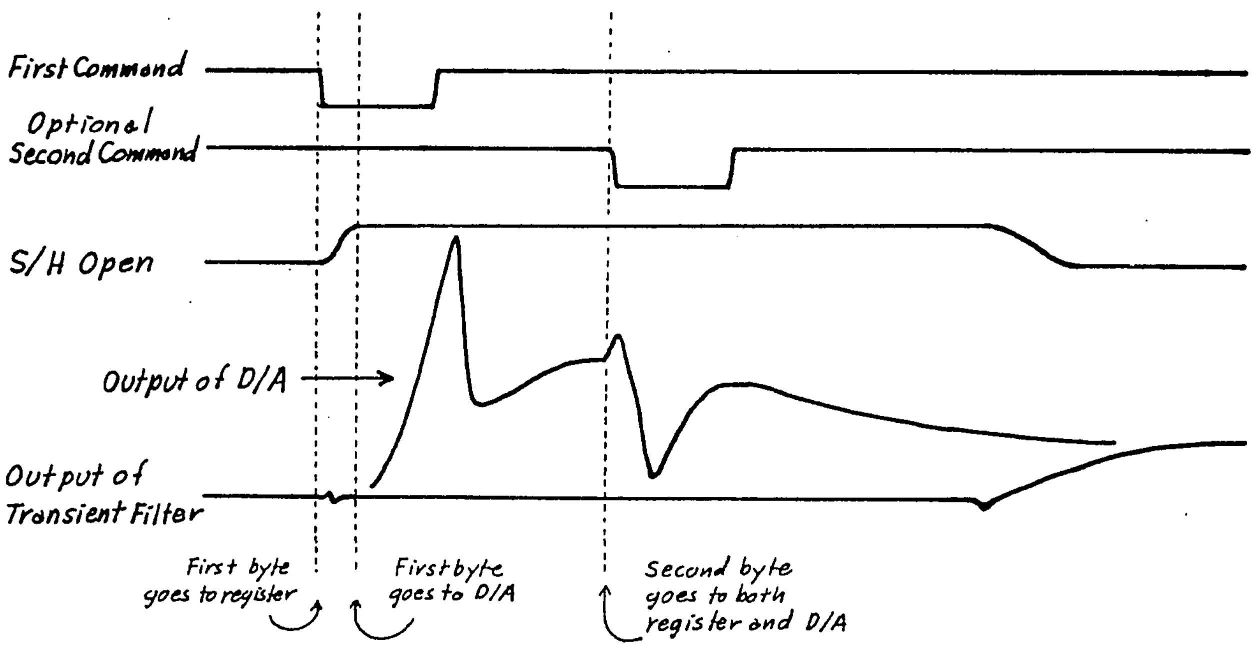


Figure 6.7 Positional D/A Timing

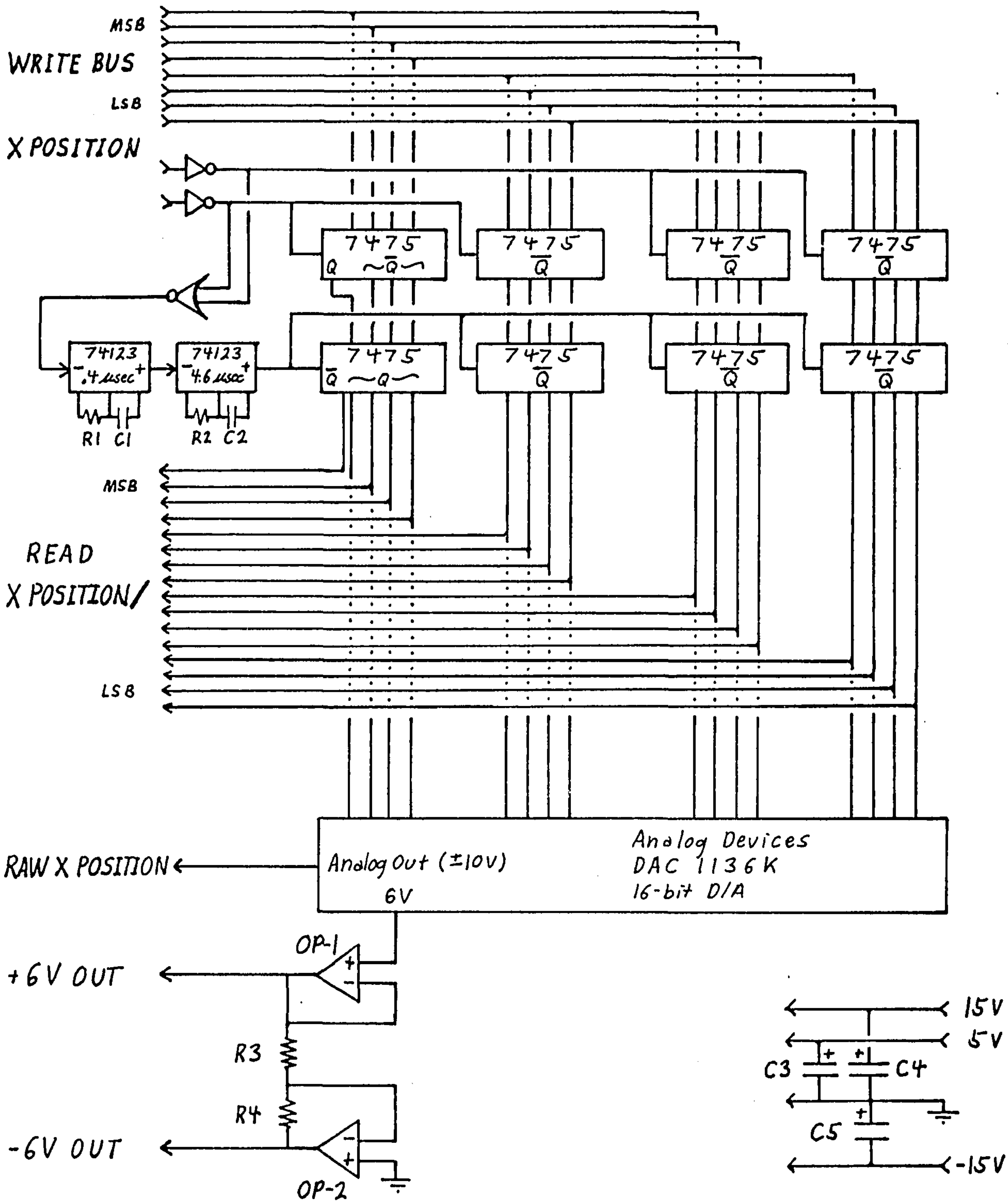


Figure 6.8 X Position D/A Board (schematic)

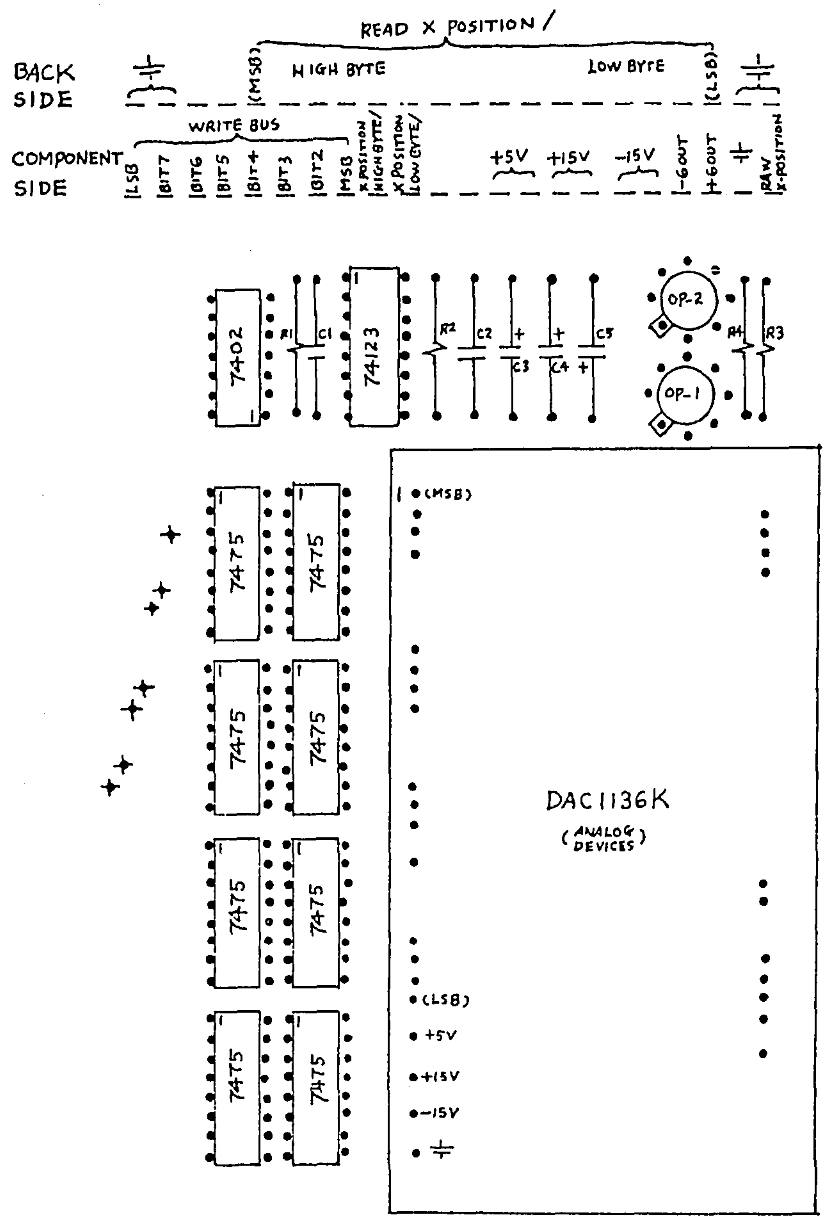


Figure 6.8 X Position D/A Board (components)

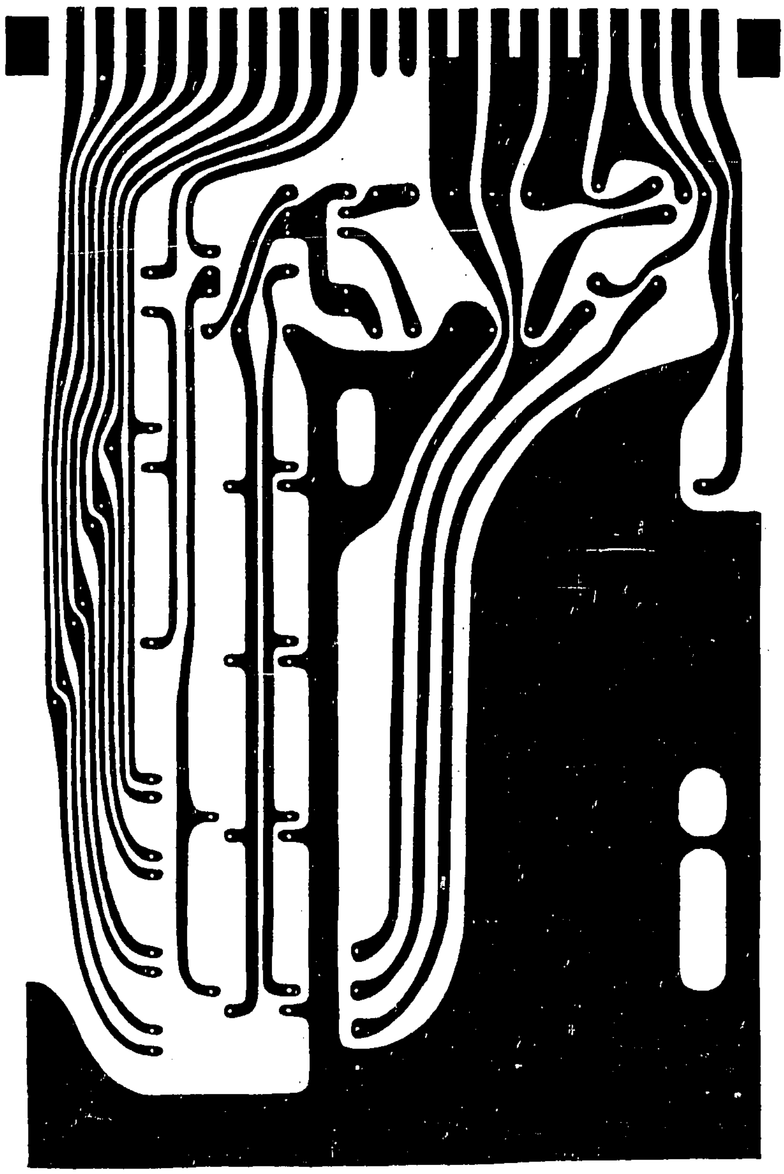


Figure 6.8 X Position D/A Board (parts side)

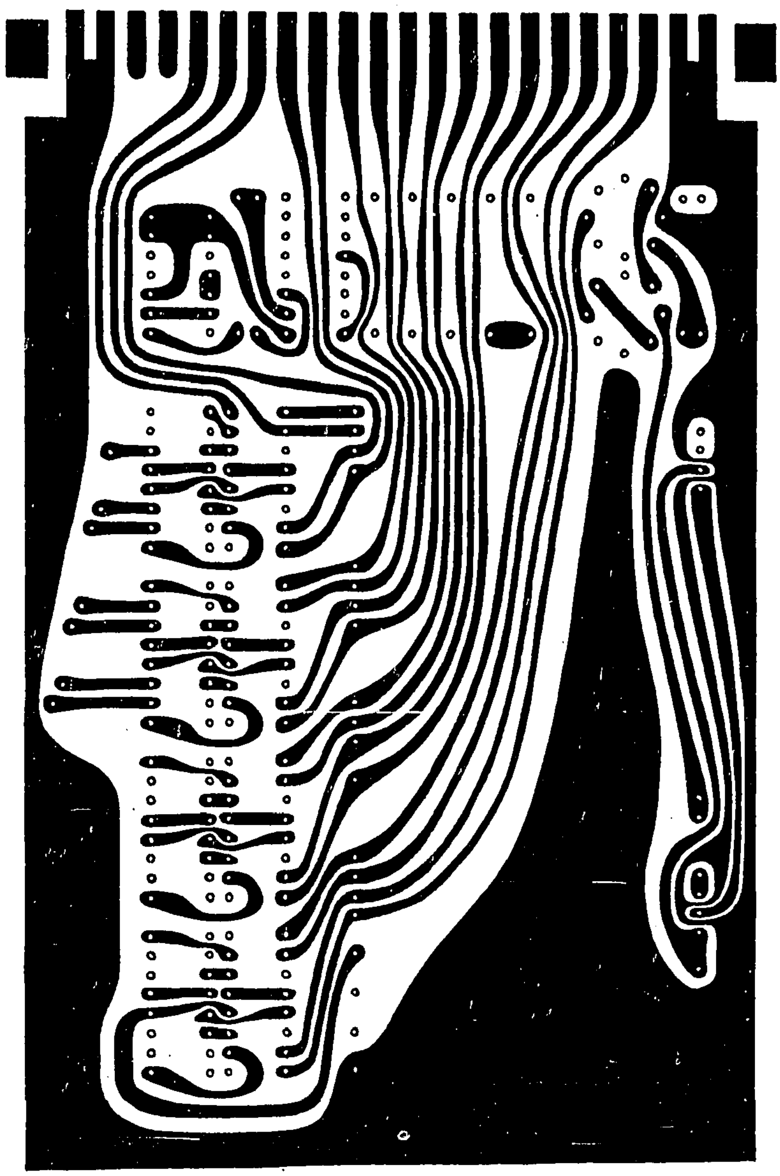


Figure 6.8 X Position D/A Board (back side)

number to enter the D/A. The register remains open for 4½ μsec, 5 μsec after either command, to allow the next optional byte immediate entry, as the sample & hold is already open.

Transient Filter Board

This board prevents random transients during state transitions of the D/A converter from reaching the yoke control circuits. It also sums stroke and distortion controls into the positional control signals.

Connections

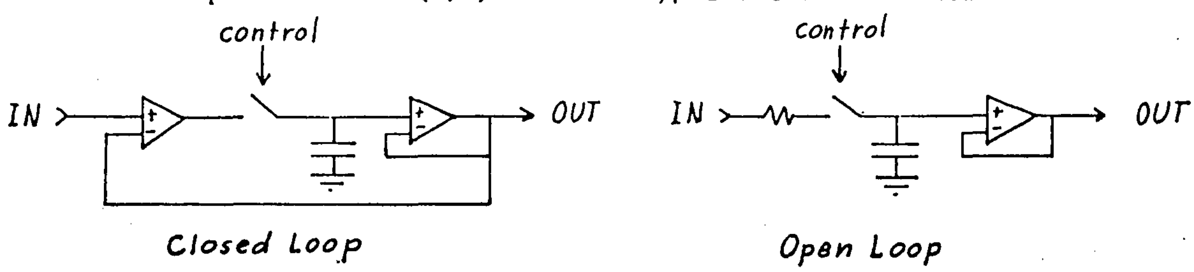
RAW X POSITION	Signal from D/A converter, +10V to -10V range.
X POSITION HIGH BYTE/ X POSITION LOW BYTE/	A retriggerable 6 μsec timer starts on the negative-going edge of either of these two exclusive controls, isolating RAW X POSITION from the output.
STROKE X POSITION	Signal from Stroke driver, +12V to -12V range. A 12V transition can move the beam from the screen bottom to top, equivalent to a 20V transition from RAW X POSITION, allowing any part of the screen to be reached from any origin specified by RAW X POSITION.
X DISTORTION	Signal from distortion correction circuitry, +12V to -12V range. An input to X DISTORTION has 1/3 the magnitude of effect as an input to RAW X POSITION.
X POSITION	Output = $-1 \cdot$ RAW X POSITION $+ 2 \cdot \frac{10}{12} \cdot$ STROKE X POSITION $+ \frac{1}{3} \cdot$ X DISTORTION

(Similar connections for Y channel)

Operation

The randomness of the transients of the D/A conversion make them devastating to image quality, far more so than would repeatable transients. This effect is discussed in the section "Need For 16-Bit positional Control". The spot position can be settled to an accuracy tolerable of repeatable transients in a relatively short time, but orders-of-magnitude longer times are needed to settle the residual poles to a tolerance required if random transients are allowed to enter the yoke driving circuitry. The reasons for the long, low error tail is that, even though current can be rapidly stabilized, the inductive nature of the yokes require some time for all variables to settle to the steady state. Including the spot position in the feedback loop is not possible because, even with gray-coding, the spot size is too large to define the location with the required accuracy (see Section "Need for 16-Bit Positional Control" in Chapter V). Also the spot would be exposing while it is being settled. Including magnetic field directly in the feedback loop is not possible because the noise and drift of Hall effect transducers are too high. Even if the field could be measured at a point, inhomogeneity in the yoke causes field uniformity to vary during settling. The residual transients will remain. Therefore the offending random transients of D/A conversion must be removed with S/H circuitry.

Two sample and hold (S/H) circuit types are shown below:



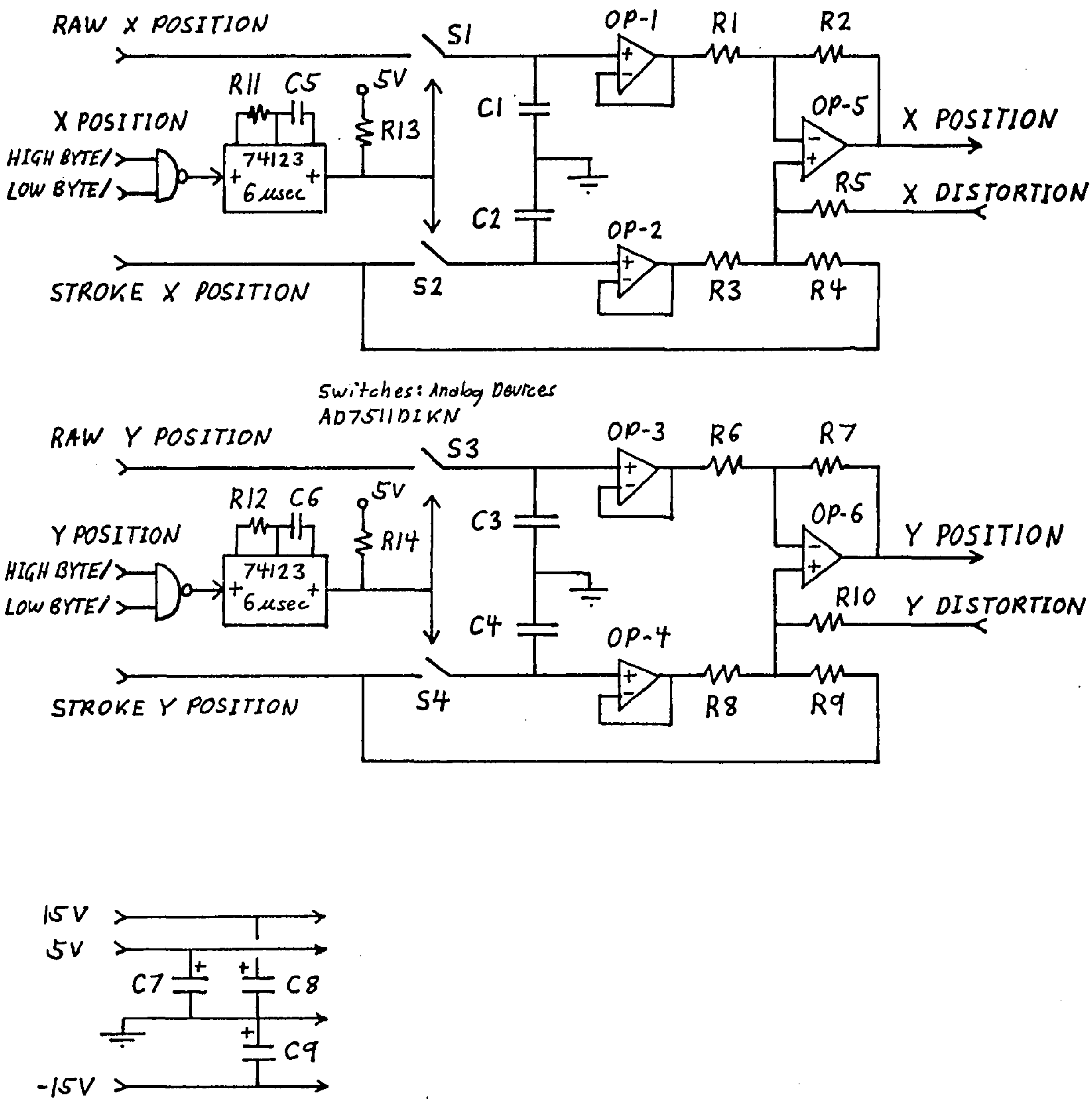


Figure 6.9 Transient Filter Board (schematic)

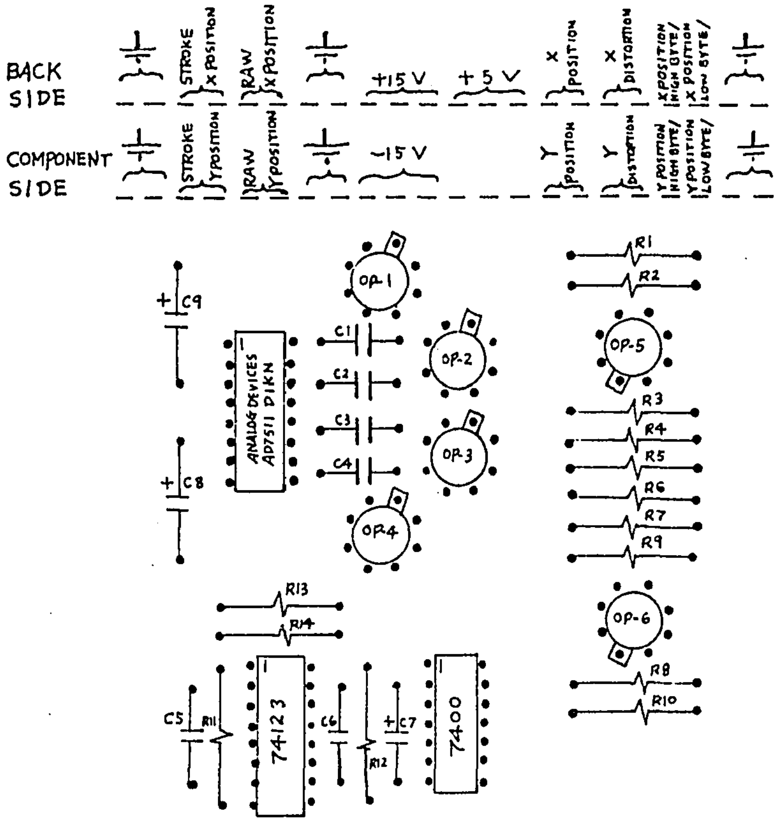


Figure 6.9 Transient Filter Board (components)

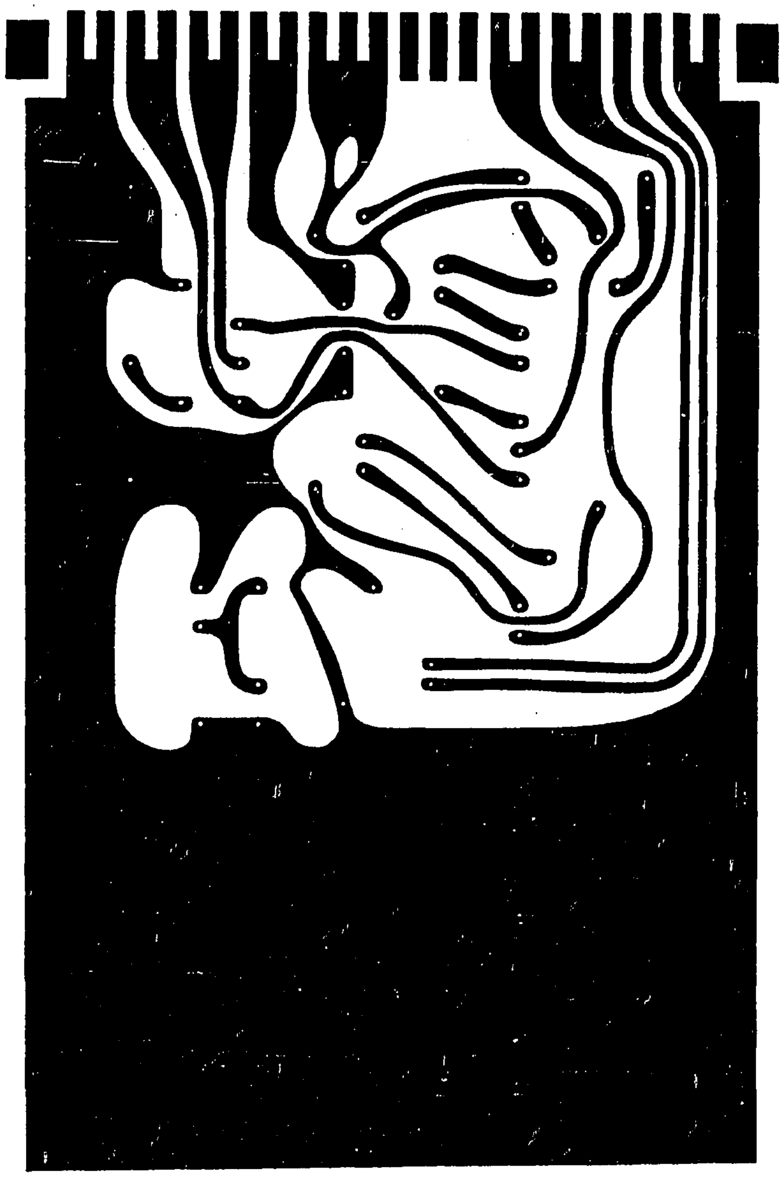


Figure 6.9 Transient Filter Board (parts side)

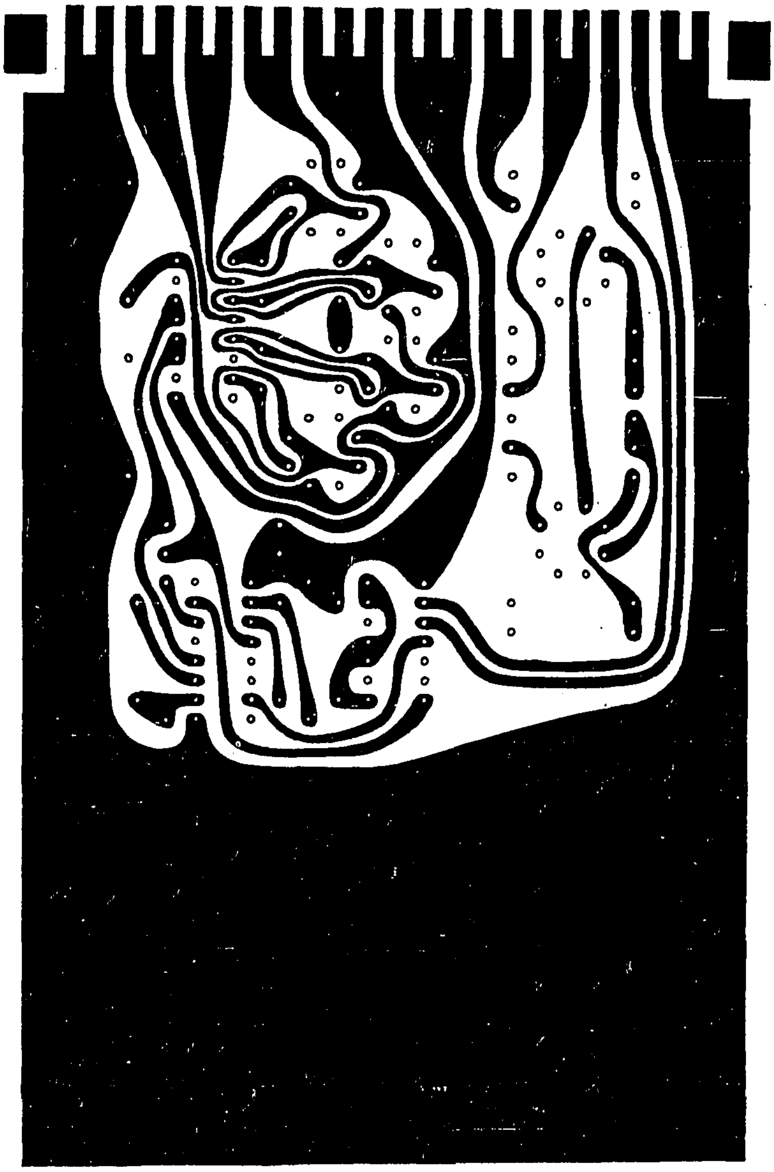


Figure 6.9 Transient Filter Board (back side)

The closed loop design has better linearity and faster settling, but the random transients that result make it unacceptable in this application.

Referring to the actual circuit, S1, C1, and OP-1 configure an open loop type sample and hold. Assuming for the moment that STROKE X POSITION is grounded, S2, C2 and OP-2 form a second symmetric S/H with similar charge transfer and leakage. OP-5 is connected in a differential configuration to cancel the transient effects of the two S/Hs. Not only are the random transients of the D/A removed, but even the uniform transients of the S/H are substantially reduced.

The circuit connects the RAW X POSITION to the most accurate inverting input of the differential amplifier, with gain dependent on the ratio of only the two resistors R1 and R2. Two other summing inputs provide: for the STROKE X POSITION a gain near two, allowing the stroke control to move the beam from any defined origin to any point of the screen; and a low-gain trimming input from the distortion correction circuitry.

Adjustments

The ratio of R3 and R4 should be adjusted to null S/H switching noise. This adjustment should be done with the board in circuit because it is affected by the impedance characteristics of RAW X POSITION and STROKE X POSITION sources. The value of $R3 \| R4$ ($\propto R3 + R4$ because $R3 \simeq R4$) should be held relatively constant.

Function Board

Up to 9 analog multipliers may be accommodated. Normally the X and Y positions are input and the resulting functions provide corrections for geometric distortions of the CRT, dynamic focus, and so forth.

Connections

IN A to IN G	Inputs connected as chosen. See PCB layout.
OUT 1 to OUT 9	Outputs of the 9 analog multipliers. Inputs to ICs are ±10V, the outputs are ±10V. 10V·10V = +10V output, therefore ±10V = ±1 unit, positive logic.
+6V, -6V	High impedance reference voltage inputs.

Normally connections are made as follows:

X	Y	X^2	X^3	Y^2	Y^3	$X \cdot Y$	$X^2 \cdot Y$	$X \cdot Y^2$	$X^2 \cdot Y^2$
IN A	IN B	OUT 1	OUT 2	OUT 3	OUT 4	OUT 5	OUT 6	OUT 7	OUT 8

Adjustments

The multipliers are designed to be trimmed with 20K potentiometers between +15 and -15V. A variant is used in this circuit with two resisters, one to ground, and the other to either buffered +6V or -6V reference. This method has advantages:

1. much lower impedence for less drift
2. less drift with, and noise from, supply voltages
3. hard wired for permanence

and disadvantages

1. longer setup time
2. difficult retrimming

Accurate trimming is not critical as residual effects add to longer errors in the CRT and are in turn trimmed by the Summer Board. Most

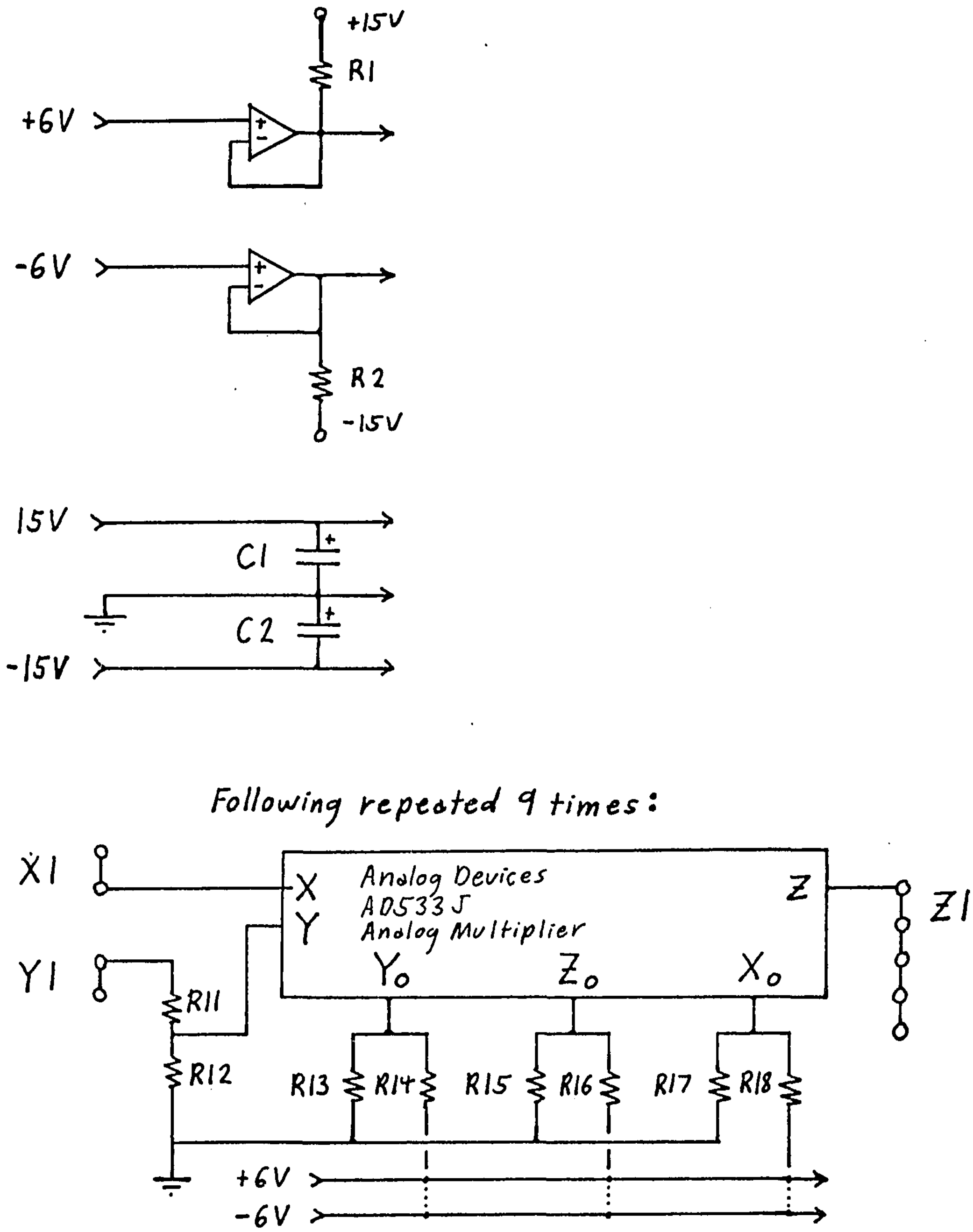


Figure 6.10 Function Board (schematic)

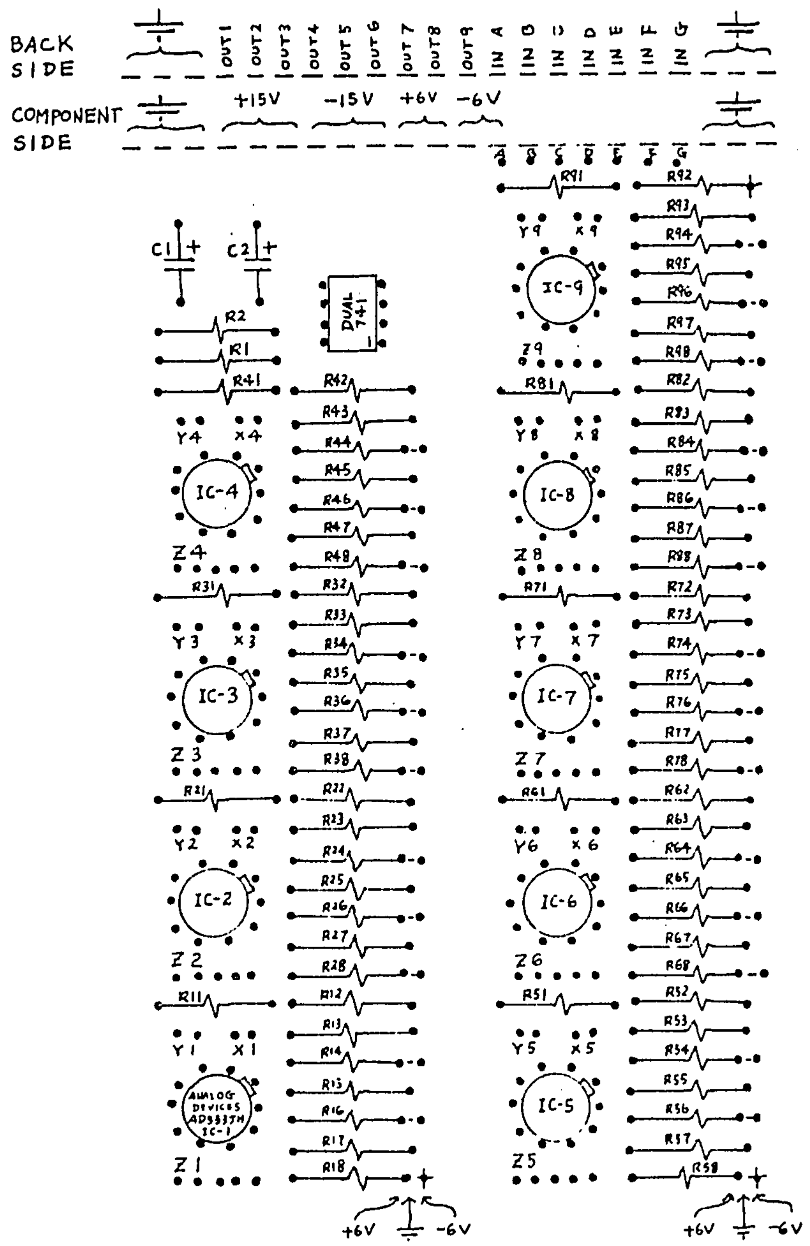


Figure 6.10 Function Board (components)

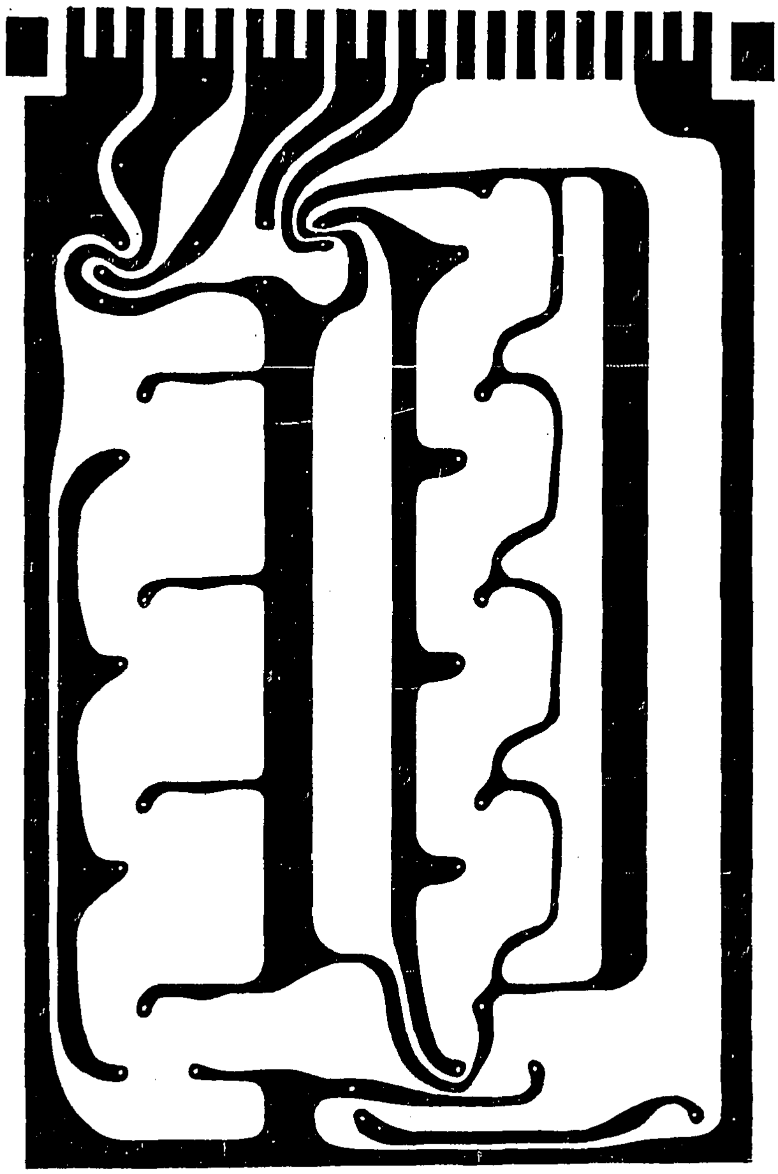


Figure 6.10 Function Board (parts side)

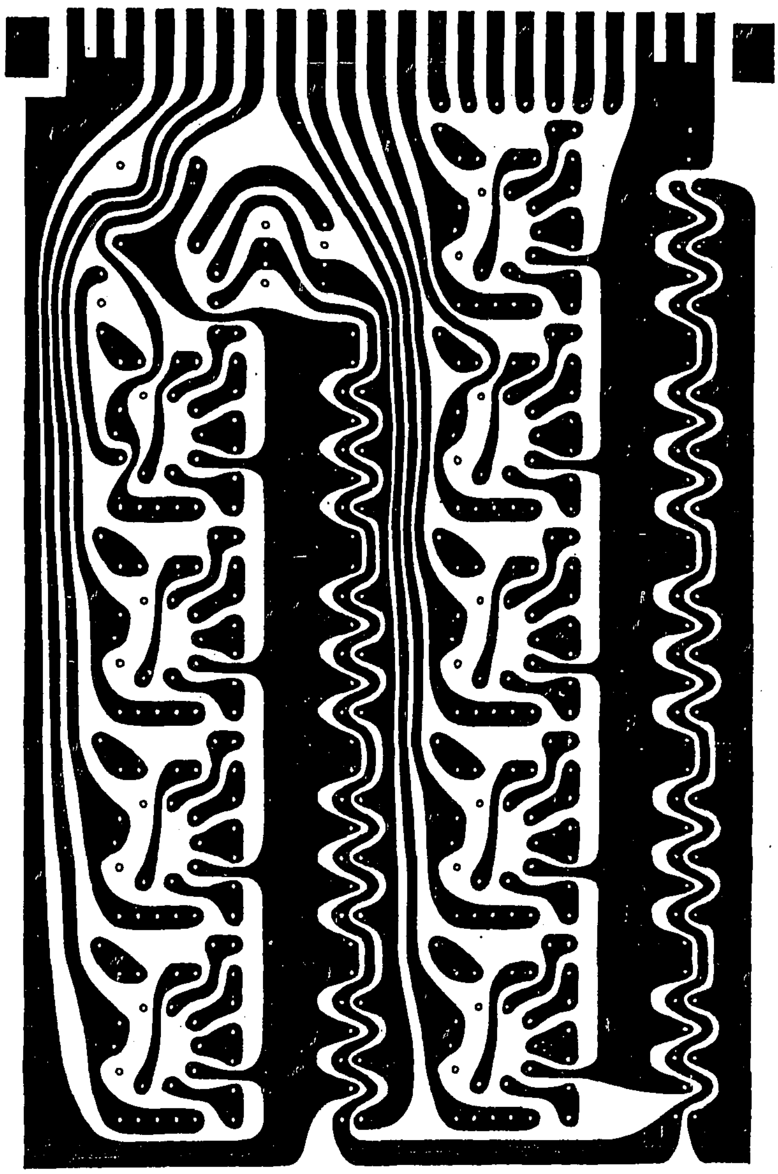


Figure 6.10 Function Board (back side)

of the ICs have sufficiently low errors as to be negligible, allowing most trimming inputs to be shorted to ground, and certainly not requiring retrimming. Both disadvantage points are thus not important drawbacks. On the other hand, the function circuits introduce potentially the most damaging temperature and supply drift of any scanner board, thus advantage points 1 and 2 are welcome. For higher cost, lower drift ICs could be specified.

The trimming inputs appear as a 50KΩ resistor to ground. When floating, they remain near ground. The trimming inputs may thus be safely shorted to +6V, ground, -6V, or left temporarily open during testing with no ill effects. A typical correction voltage is < 0.1V, with 0.5V being a maximum. Trimming procedure is:

1. with X = Y = 0, adjust Z_o with potentiometer to ~0V output
2. with X = 0, Y = 20V p-p (50 Hz) adjust X_o for minimum AC out
3. with Y = 0, X = 20V p-p (50 Hz) adjust Y_o for minimum AC out
4. with X = Y = 0, adjust Z_o for 0V out
5. with X = exactly 10V, Y = 20V p-p (50 Hz) adjust gain for OUT = Y

The operational amplifiers buffering the reference voltage are aided with pull-up and pull-down resisters R1 and R2, which should be chosen to bear about 3/4 of the current.

Summer Board

12 input signals may be summed or subtracted into 4 channels. The summing constants are resistor-adjustable. Normally the input signals are from the function board and the outputs include corrections for X and Y positions and dynamic focus.

Connections

IN 1 to IN 12 Unattenuated inputs. Range = +10V to -10V

A OUT to D OUT Outputs of the 4 bi-polar summers

Normally connections are made as follows:

X	X^2	X^3	Y	Y^2	Y^3	$X \cdot Y$	$X^2 \cdot Y$	$X \cdot Y^2$	$X^2 \cdot Y^2$	+6V	AUX D/A
IN 1	IN 2	IN 3	IN 4	IN 5	IN 6	IN 7	IN 8	IN 9	IN 10	IN 11	IN 12
A OUT - X DISTORTION	B OUT - Y DISTORTION	C OUT - DYNAMIC FOCUS	D OUT - Auxiliary								

X and Y inputs are X POSITION and Y POSITION from Transient Filter Board

+6V is from X Position D/A Board

AUX is D/A from Alignment Board

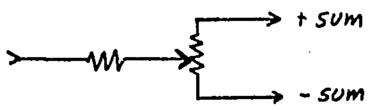
The rest are from the Function Board

In the normal circuit environment, if X = Y = +10V, then the spot will be in the lower left corner, and all function inputs = +10V. An output of -1/3 volts moves the spot 1% of the image width toward the upper right.

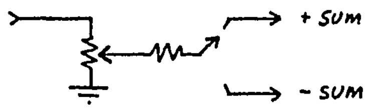
Trimming

Discrete resistor trimming was chosen because:

1. Bipolar corrections are required, over orders of magnitude, with no skip at zero. Also, excessive conductance and extra operational amplifiers should be avoided to minimize drift. The circuits below were rejected because:



insufficient range and nulling distortions



insufficient range and excess total impedence

2. With a utility program the computer can test the scanner and specify resistance values giving sufficient correction in a single wiring iteration.

3. Fixed resistors are both less expensive and provide better long term reliability.

In the normal circuit environment the Summer Board operates within a positive feedback loop. The effects on quality are negligible given the normally very small gain and fast response of the board. The alignment program should consider the mathematical DC effects.

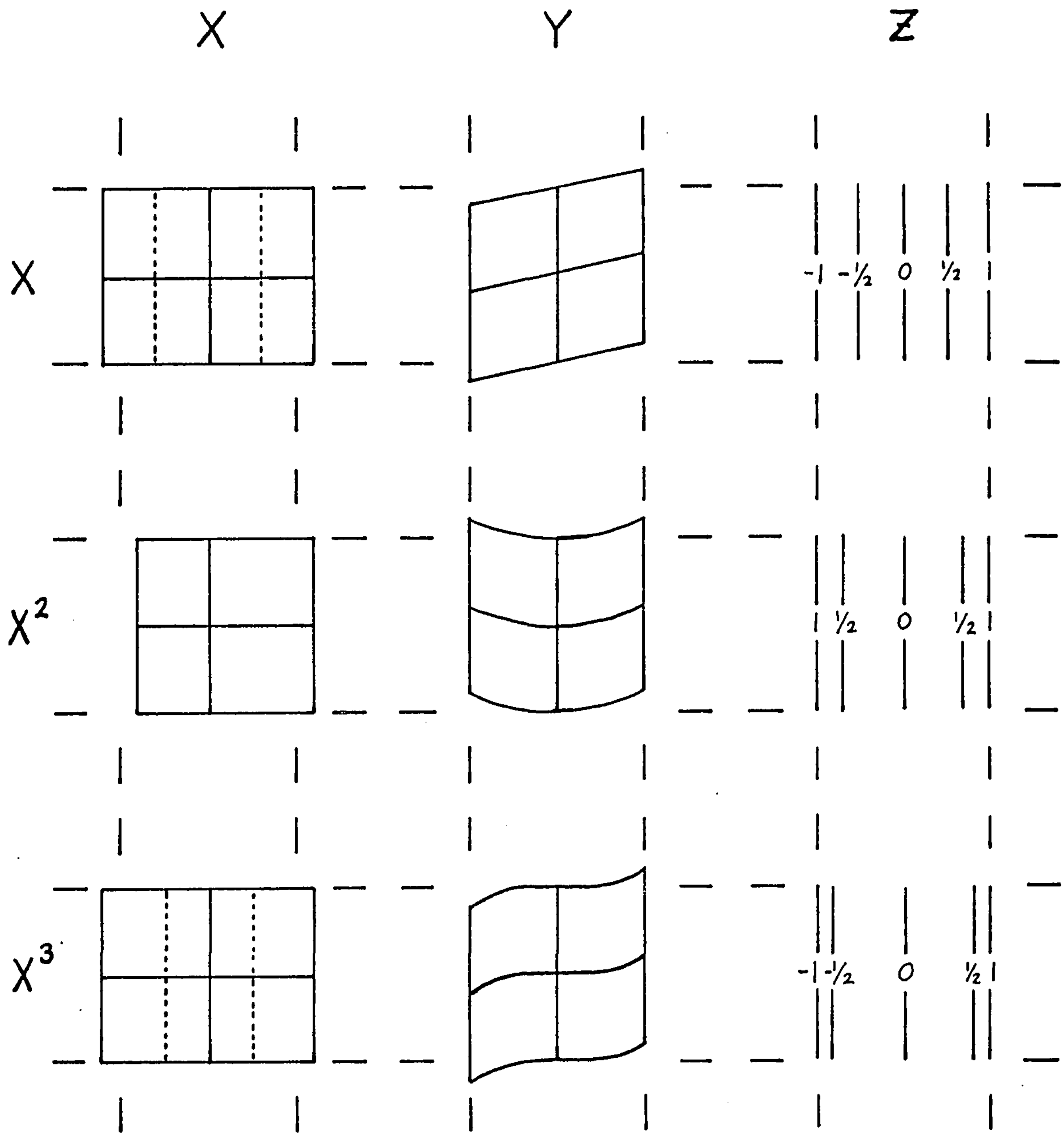
Image size should be adjusted to within 5% at the Yoke Driver Board. Only minor corrections should be made at the Summer Board:

1. To maintain fully scaled position signals
2. To minimize transients and drift

However, when using some corrections a balance is desirable for the same reasons above. For example, when adding substantial X^3 to the X position, subtraction of some X is desirable.

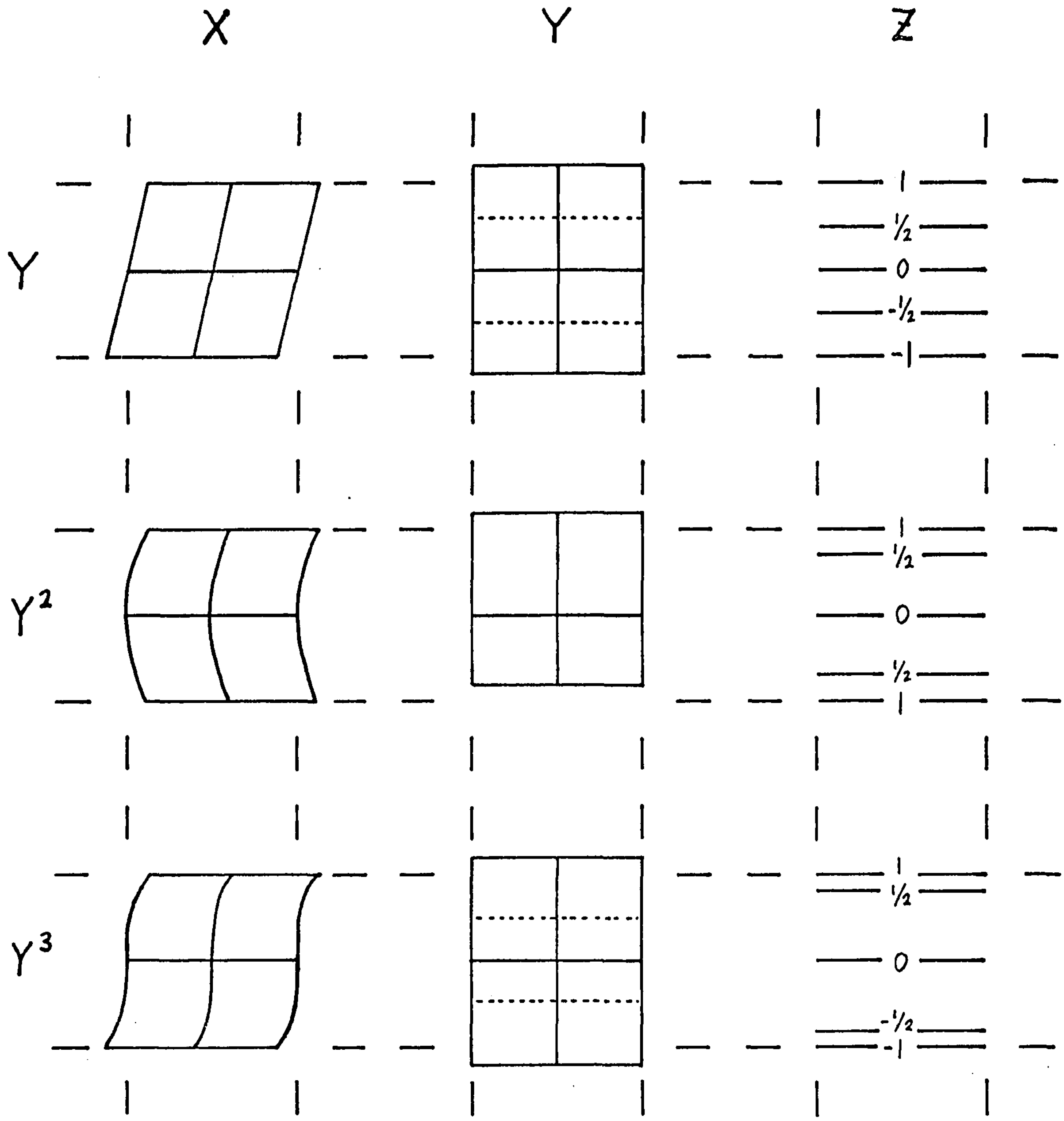
Under extreme conditions the first op-amp could saturate before the second. In normal usage neither will saturate.

The bias current drift in OP-1 cancels that of OP-2 to the extent the two are uniform. Even without this nulling effect, the specified op-amps and resistances give a bias current drift effect sufficiently less than offset voltage drift to obviate differential biasing resistors.



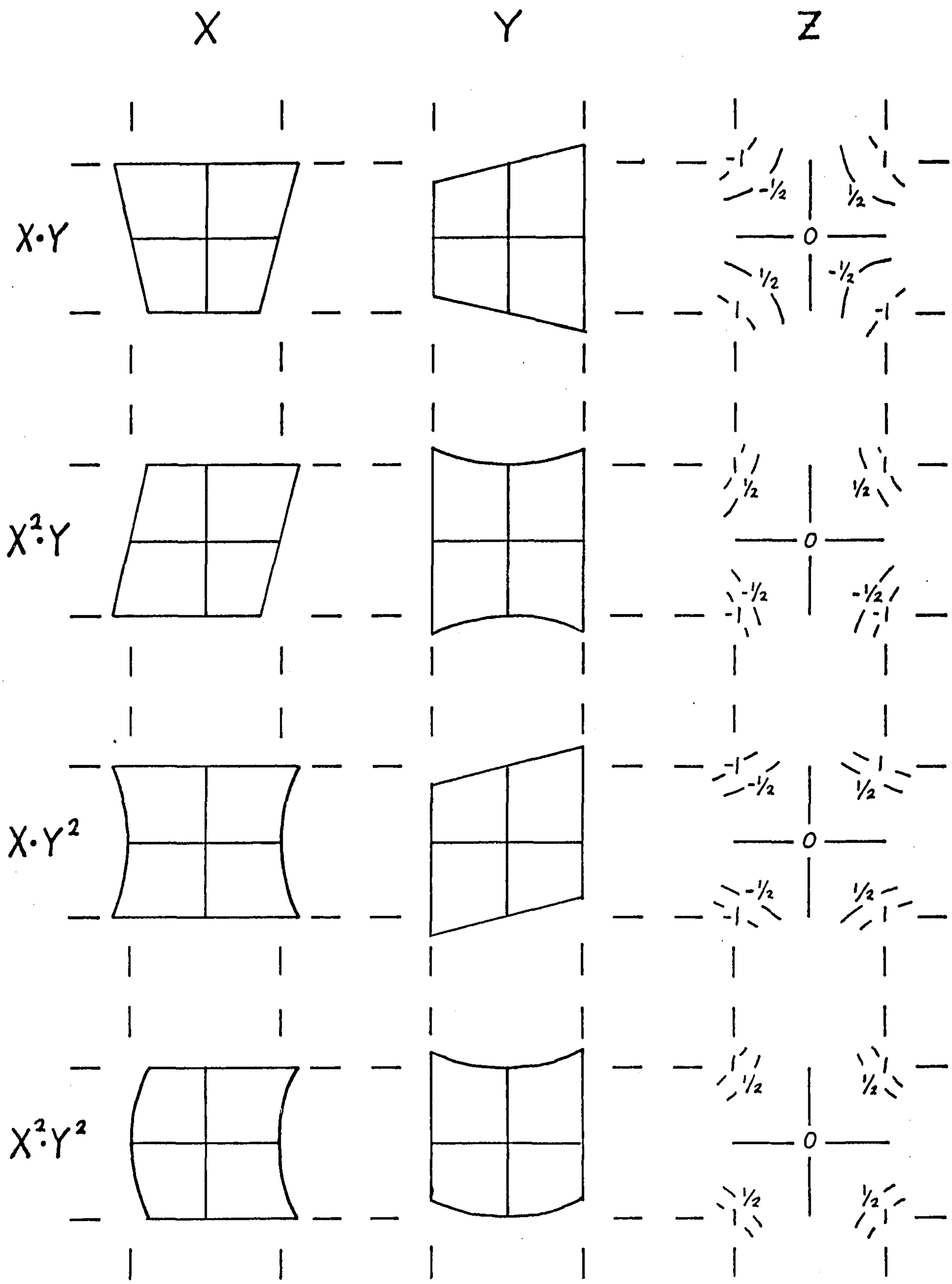
Effect of adding 20% X, X^2, or X^3 to X, Y, or Z channels

Figure 6.11 Distortion Corrections



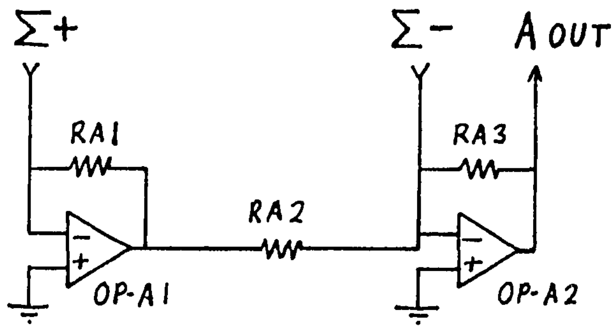
Effect of adding 20% Y, Y^2, or Y^3 to X, Y, or Z channels

Figure 6.11 (continued)



Effect of adding 20% X Y, X^2 Y, X Y^2, or X^2 Y^2 to X, Y, or Z channels

Figure 6.11 (continued)



Complete circuit includes above repeated 4 times

plus summing matrix

Figure 6.12 Summer Board (schematic)

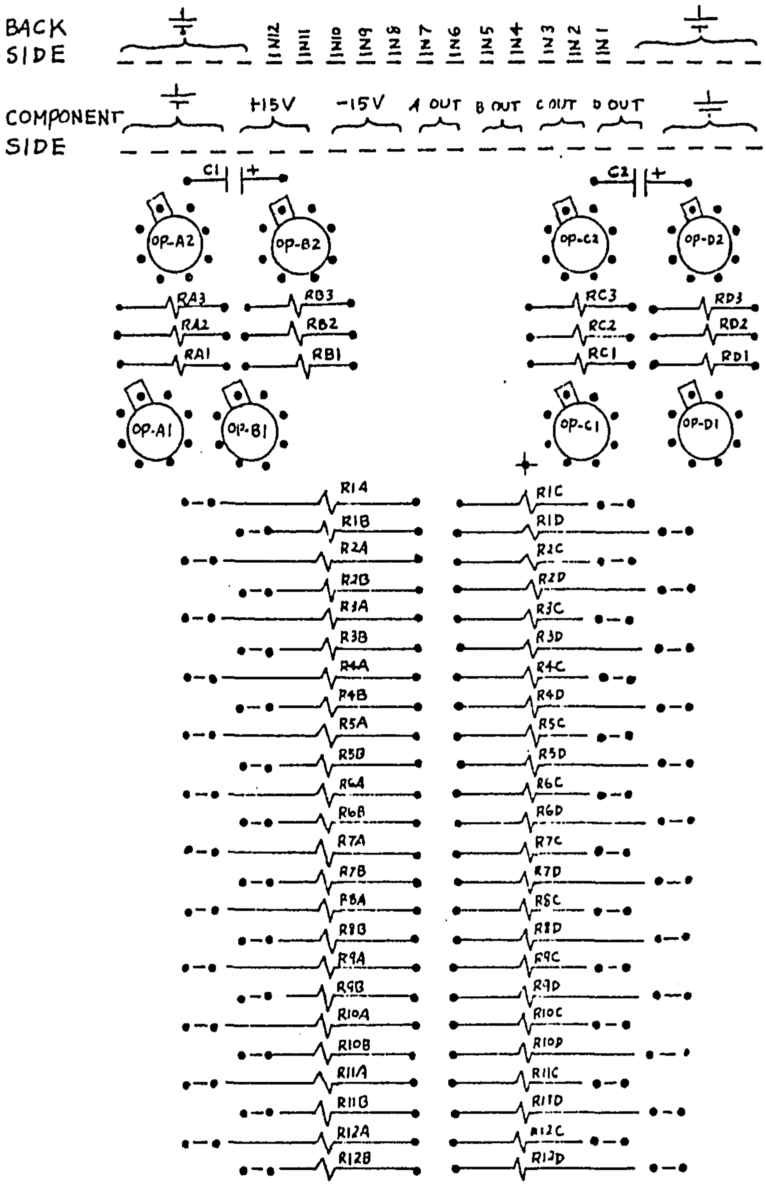


Figure 6.12 Summer Board (components)

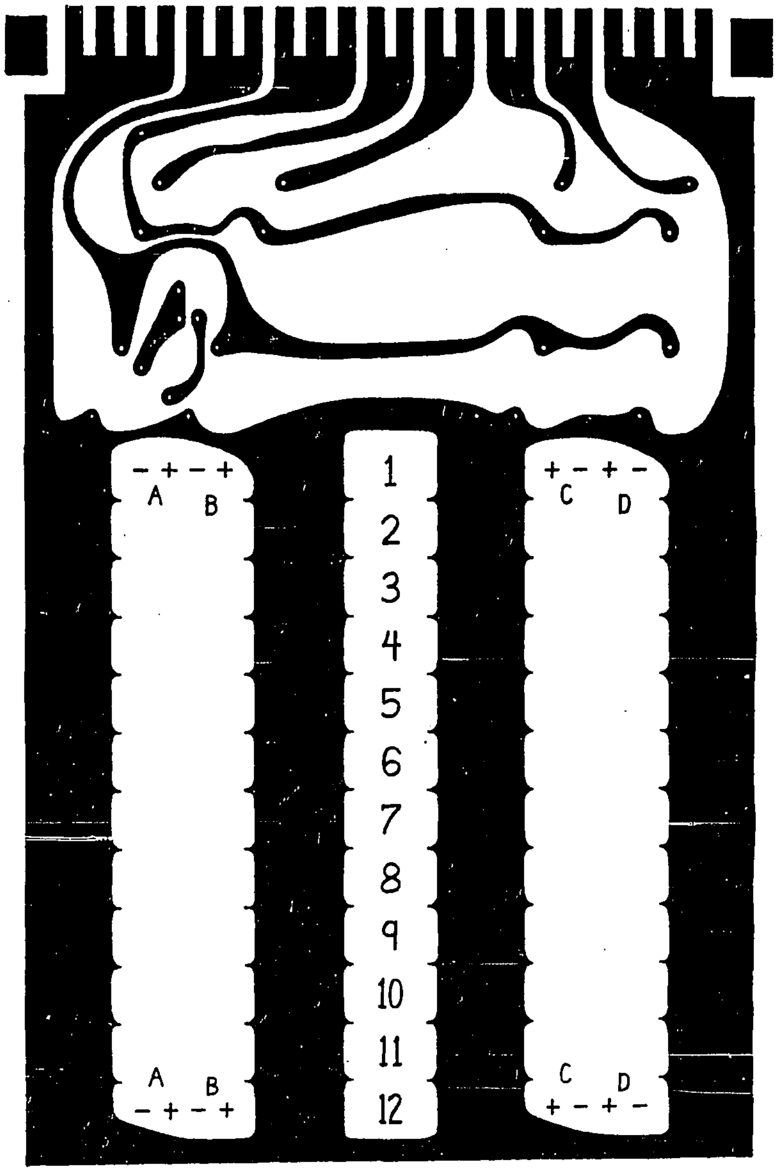


Figure 6.12 Summer Board (parts side)

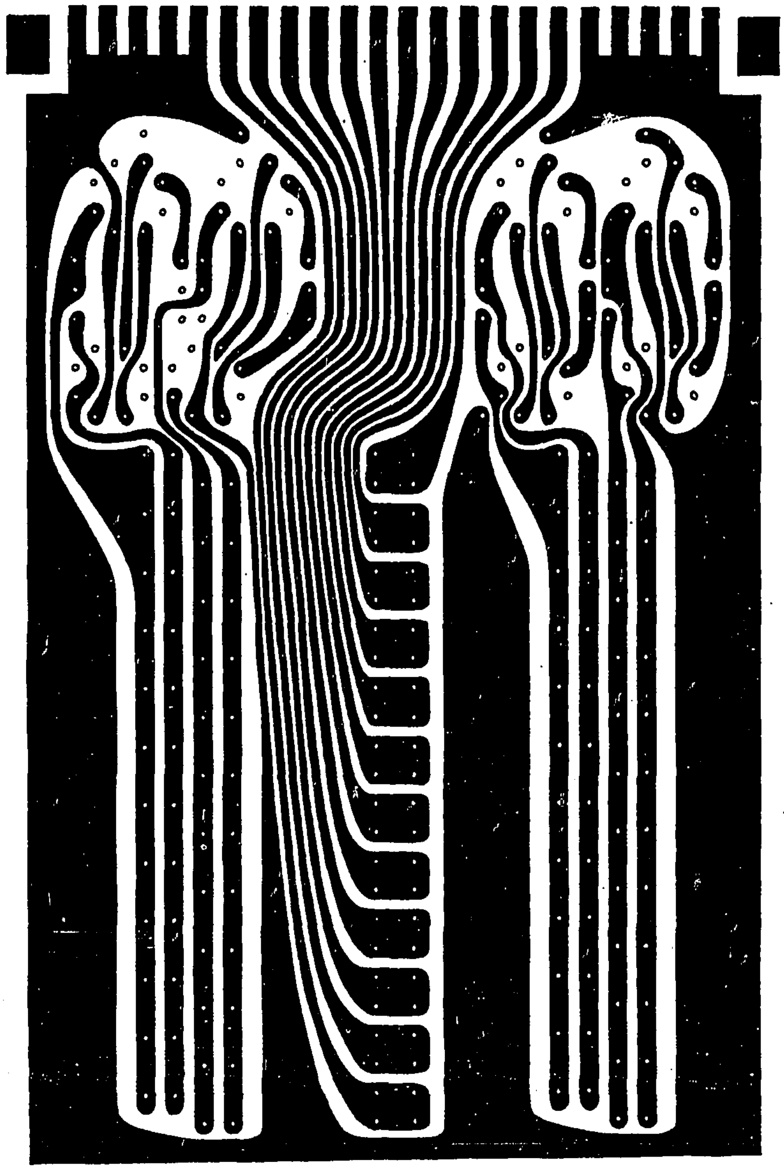


Figure 6.12 Summer Board (back side)

The auxiliary D/A allows the computer to manipulate the focus grid voltage, both to optimize it in real time, and also to allow a utility program to specify required resistor values.

Some useful combinations include:

$K(X^2 + Y^2 - \frac{X^2Y^2}{25})$ to dynamic focus
for correction of flat-faced CRT

$-K(X^2 \cdot Y)$ to Y position and $-K(X \cdot Y^2)$ to X position
for pincushion correction of flat-faced CRT

$-KY^3$ to Y position and $-KX^3$ to X position
for on-axis linearity of flat-faced CRT

$\pm KX$ to Y position and $\pm KY$ to X position
to correct orthogonality of axis

$\pm KX$ to Y position and $\pm KY$ to X position
rotation of image (gross correction by rotating CRT or yoke)

$\pm KY$ to Y position and $\pm KX$ to X position
adjustment of size and aspect ratio (gross adjustment at Yoke Driver Boards)

By inserting a precision grid in the image plane, the computer can precisely map the nonuniformities of the scanner and optical system. With this data the computer can calculate the resistor matrix needed for the best RMS fit.

Time Board

This board provides a logarithmic indication of time, acting as would a Photosense Module viewing a constant light source. The Time Board is a Photosense Board with the following modifications:

1. No photomultiplier, zener bridge, high voltage, or overrange circuitry.
2. In place of the photomultiplier is a constant current source derived from the -6V reference using a resistor.

The Photosense Module section contains the schematic and description of a Photosense Board.

Sample & Hold Board

Up to 12 analog channels may be frozen simultaneously. The board also provides interrelated timing for sampling and integration reset.

Connections

S/H IN	12 high impedance inputs to the S/H modules
S/H OUT	12 low impedance outputs from the S/H modules. Transfer gain from respective S/H IN is +1.
SAMPLE/	Sampling mode entered on 1 → 0 transition of SAMPLE/, Effective sampling instant occurs when hold mode reentered 10 μsec later.
INTEGRATE/	Integration is reinitiated at a 1 → 0 transition of INTEGRATE/. The command is retained and allowed to pass only in the hold mode.
RESET	Buffered output to Photosense Boards commanding an integration reset as a 1 μsec positive pulse.

Operation

Common practice uses a single sample & hold (S/H) module following a multiplexer to freeze the input to an A/D, allowing only sequential sampling of several channels. However, in most multi-channel applications, as in the scanner, mathematical processing of channel interrelations requires that all channels be sampled simultaneously. The advent of low-cost IC S/H modules allow the placement of a plurality of S/Hs prior to a multiplexer. The cost of this arrangement is further lowered by a relaxing of acquisition time requirements.

When fully populated, 12 S/H channels may be accommodated. A pin of module 9, marked as a crossover, must be noted if station 9 is not filled. Other unmarked crossovers need to be observed if the first 5 stations are not populated. As discussed elsewhere, a typical installation requires at least 9 channels.

Timing is illustrated:

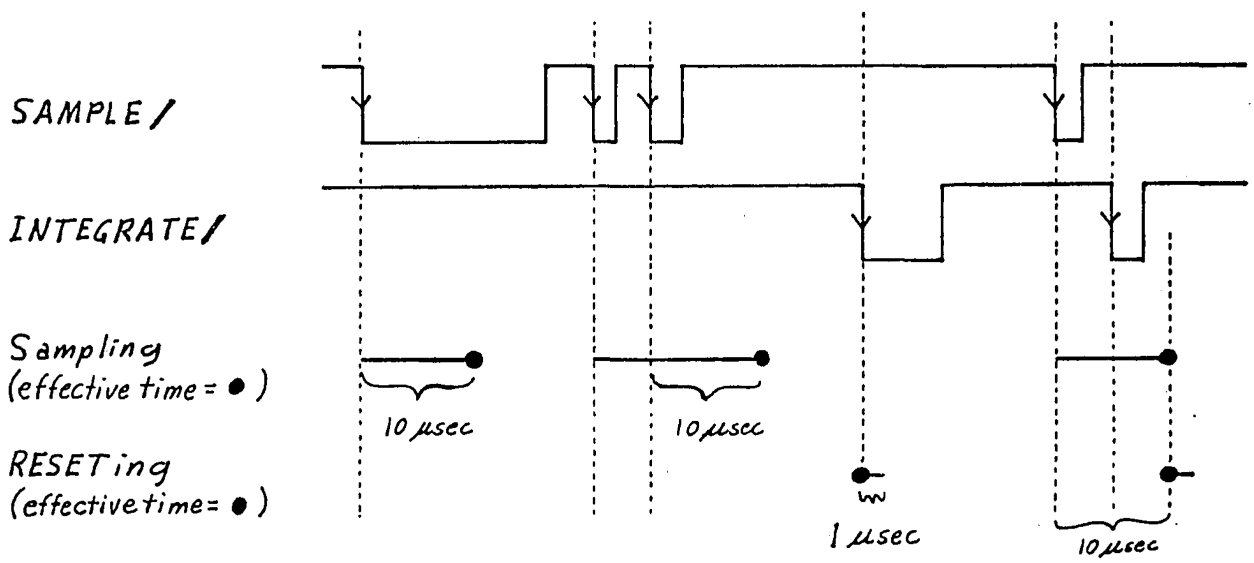


Figure 6.13 Sample & Hold Timing

The negative going edge of SAMPLE/ opens the S/H modules for 10 μsec, during which time each S/H OUT attains and tracks the respective S/H IN. At the end of this time the modules return to the hold mode, retaining the signal as it was 10 μsec after the SAMPLE command. Two series SAMPLE commands effectively extend the sampling time. A SAMPLE command should not be given between 7 μsec before and 14 μsec after any COLOR command so that the analog remains constant 1 μsec prior to, and during, the 10 μsec A/D conversion. Note that even if the raw channels are stable, there is a small sample-to-hold offset error. Data should be converted within 1/20 second of SAMPLE to insure $<\frac{1}{2}$ LSB drift error.

A negative-going transition of INTEGRATE/ evokes a 1 μsec positive pulse on Reset, which is output to the integrating circuitry on the Photosense Board. If the S/Hs are in the hold state then the pulse is transferred immediately. However if the S/Hs are open then the command is retained in an SR flip-flop until after the sampling terminates.

Two modes of operation are possible:

1. Monitor total exposure buildup by resetting the integral only once per pixule, or
2. Monitor exposure vs. time by repetitively resetting and sampling. An INTEGRATE command immediately following a SAMPLE command is intercepted by the hardware and released on the RESET line about 50 nsec after the S/H returns to the hold mode. Combined with the 50 nsec aperature time of the S/H and small delays at the Photosense Board, less than 0.1 μsec is lost to a "blind spot." A loop is possible:

→ OUT Sample (LOOK)
OUT Reset (CLEAR)
OUT Color (WHITE)
(Read past conversion)
(Store)
(Enough?)

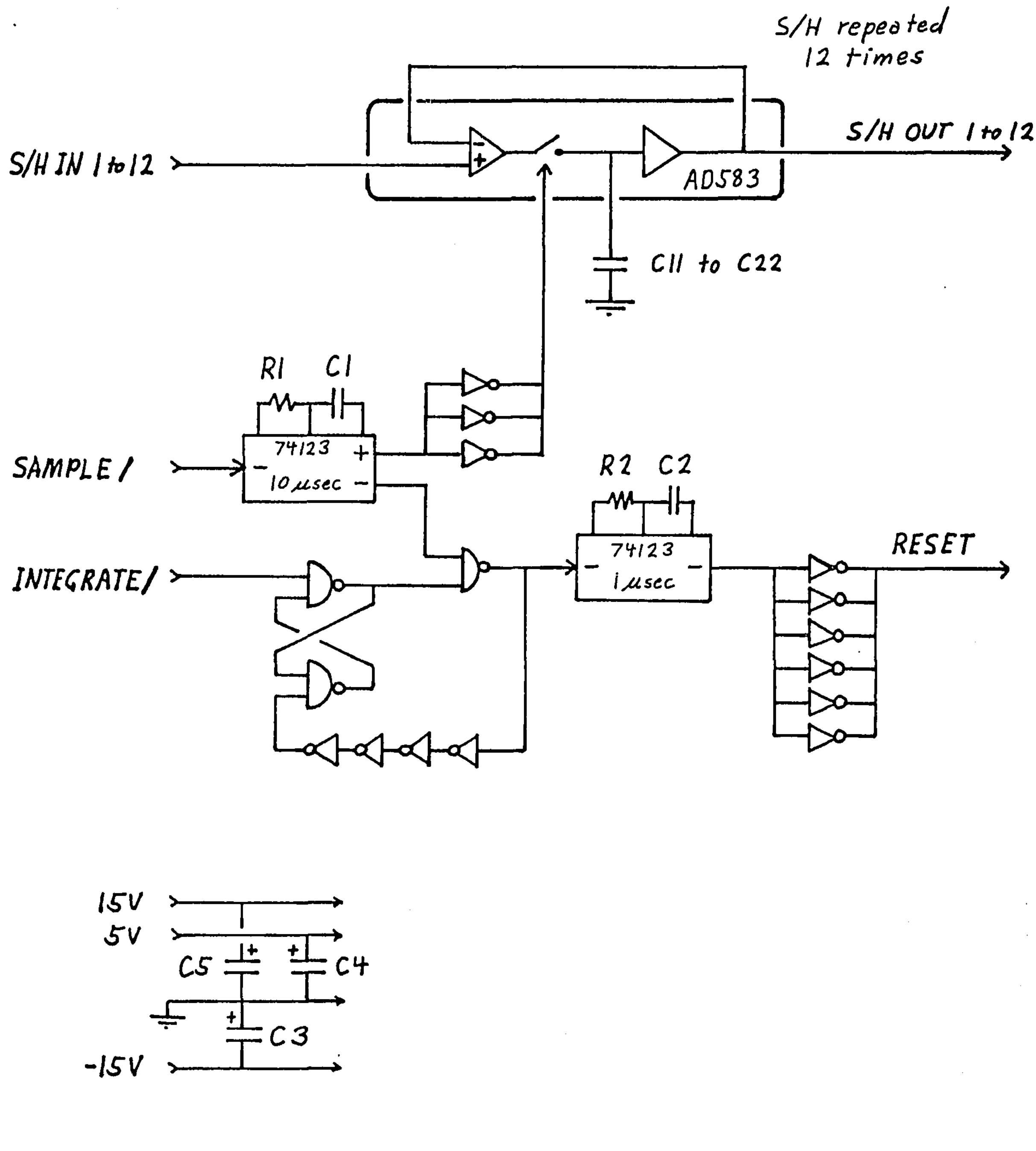


Figure 6.14 Sample & Hold Board (schematic)

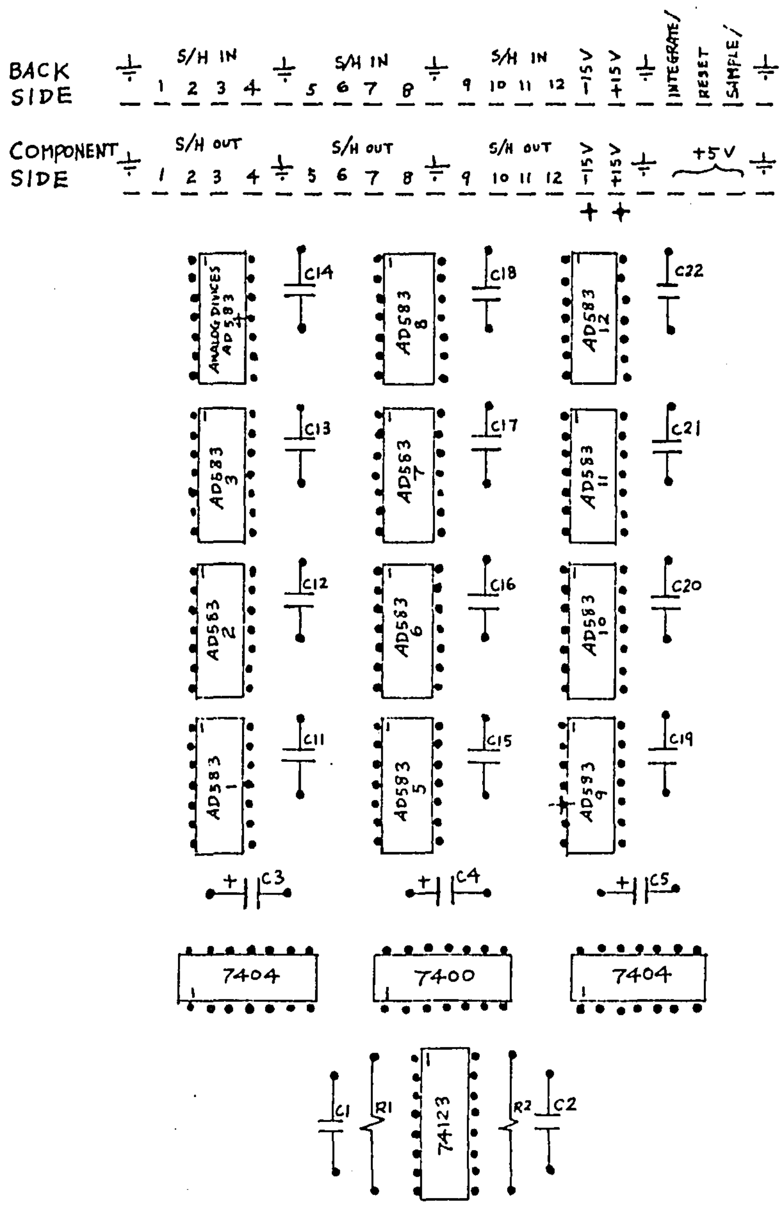


Figure 6.14 Sample & Hold Board (components)

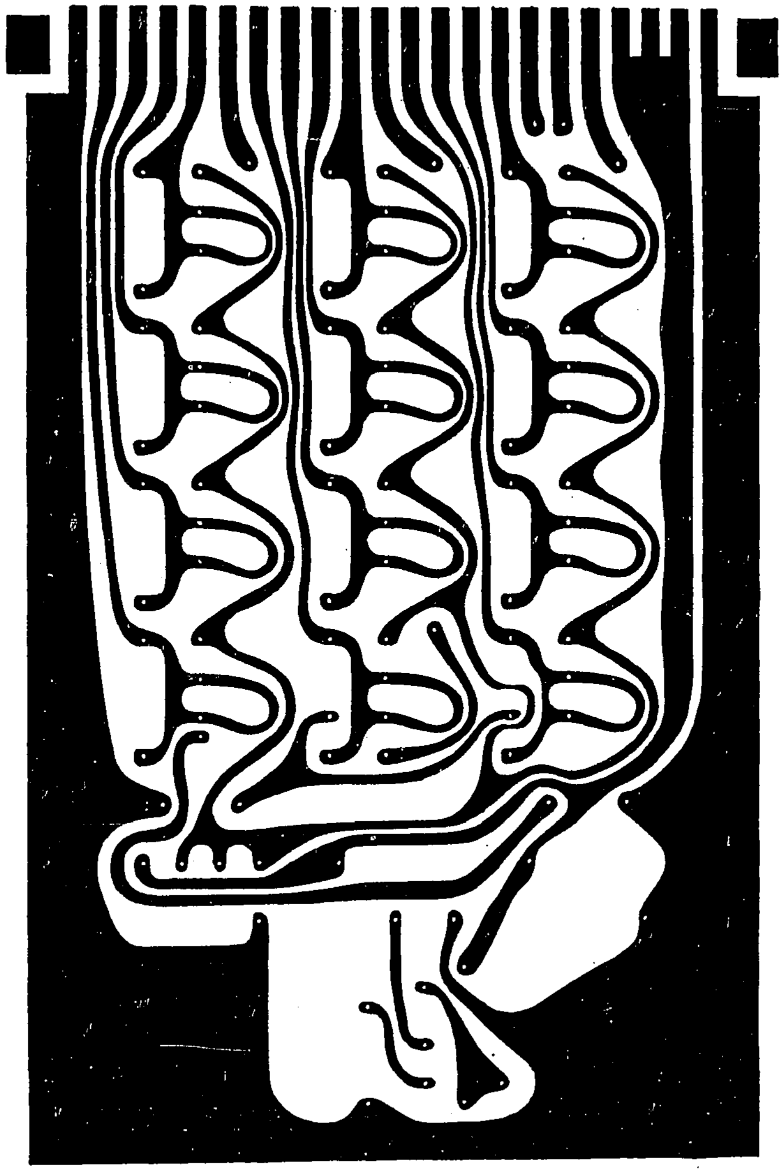


Figure 6.14 Sample & Hold Board (parts side)

Figure 6.14 Sample & Hold Board (back side)

Analog Multiplex Board

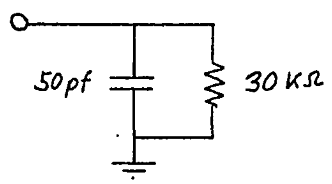
This board receives 16 differential low-impedance analog inputs, switches to the one chosen by the 4-bit SELECT address as strobed by the COLOR clock, performs analog subtraction on the chosen differential channel, and outputs a single rail ANALOG.

Connections

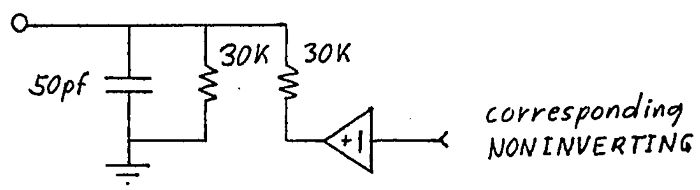
SELECT 4-bit positive logic address selecting one of 16 channels

COLOR When COLOR is high, SELECT is passed through a holding register and retained when COLOR is low

NONINVERTING 16 analog inputs which add to the output, each labeled for its SELECT address. The input equivalence:



INVERTING 16 analog inputs which subtract from the output, each labeled for its SELECT address. The input equivalence:



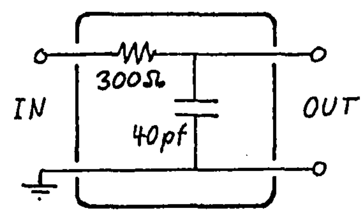
ANALOG Single rail analog output

(SELECTed NONINVERTING) - (SELECTed INVERTING)

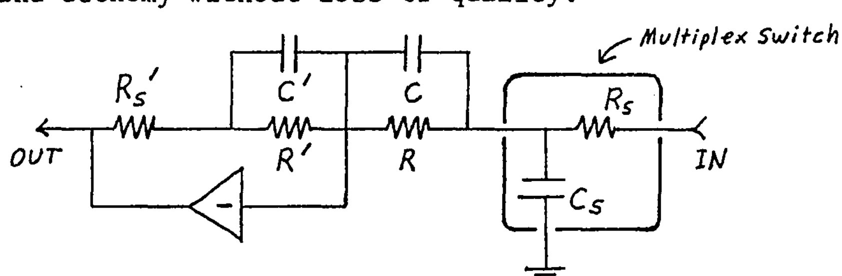
Note: All signal inputs should be <+15V and >-15V supply. When the supplies are off, so should all signal inputs. A diode insures the +15V supply always ≳+5V supply to partially protect digital inputs during power down if +15V falls faster than +5V.

Operation

The terminal equivalent of the two multiplexers is:



Although common practice includes buffering amplifiers on each rail prior to the differential amplifier, this arrangement does not remove the 40 pf capacitance from the signal input. All scanner channels can drive 40 pf, and it is felt any source capable of driving 40 pf can also drive the 30 K load of the difference amplifier. By modifying the difference amplifier circuit, the buffer amplifiers can be omitted, enhancing reliability and economy without loss of quality.



Without buffer amplifiers, the difference amplifier impedances must be high enough to make the switch resistance R_s drift negligible. High feedback impedances, combined with differential input capacitance of the very fast op-amp, lead to instabilities, which are cured with very small resistor-bypassing capacitors, as in the circuit above. An apparently destabilizing pole in the above circuit is at such a high frequency as to be negligible. Although the bridge is not balanced due to the C_s, provided the primed and unprimed components are matched the imbalance is not from a pole-zero misalignment, but rather from a single high frequency pole primarily arising from R_s and C_s. The former

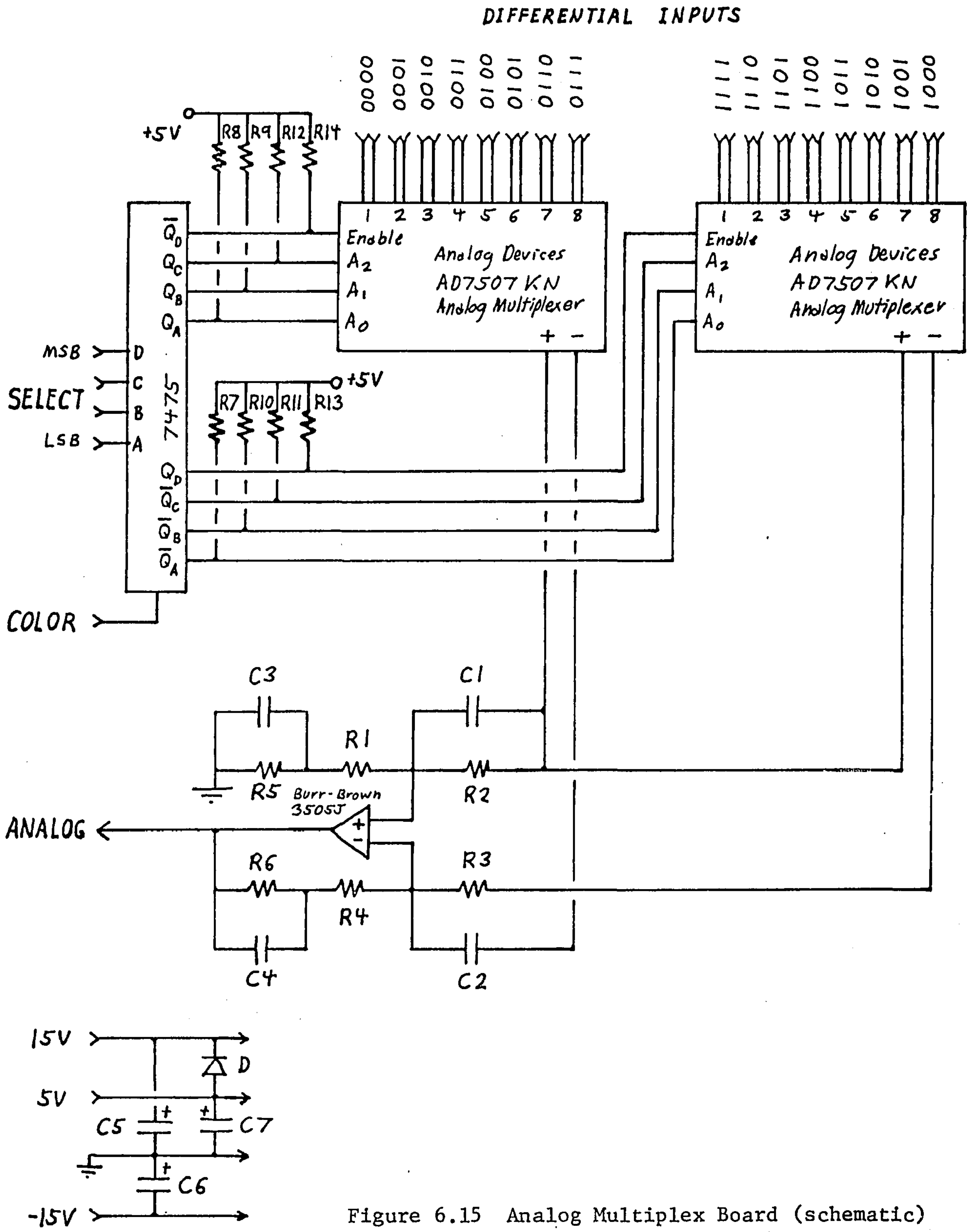


Figure 6.15 Analog Multiplex Board (schematic)

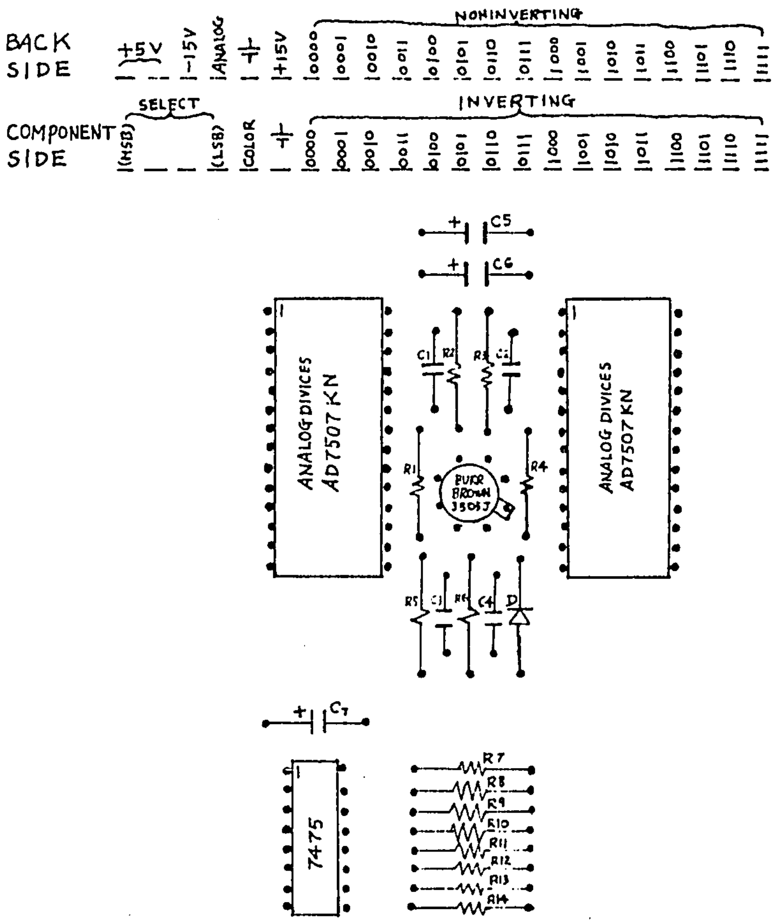


Figure 6.15 Analog Multiplex Board (components)

Figure 6.15 Analog Multiplex Board (parts side)

Figure 6.15 Analog Multiplex Board (back side)

would give a small but long-lasting transient error, the latter actual case a larger but rapidly dissipated error.

High resistance limits on R include:

1. Offset current drift vs. offset voltage of op-amp
2. Error transients from C vs. C' mismatch and other stray capacitance

Low resistance limits are:

1. R_s drift
2. Input loading

A/D Board

This board provides analog to digital conversion. The 16-bit output is compatible with the FOCUS number system. Timing features remove constraints to simplify software development.

Connections

ANALOG	Analog voltage to be converted. Range = ±5V.
COLOR	Conversion sequence is initiated at positive-going edge of TTL logic input COLOR.
READ A/D/	Number resulting from conversion of ANALOG. The output is 16-bit, FOCUS compatible, negative logic.

Operation

The following relationships hold. Note that the binary output shown below in positive logic appears at READ A/D/, in negative logic. Also see section on adjustments.

Analog In	Binary Out	FOCUS 10.10
≥5 Volts	0 10011.1111111110	10^4
+0.0024 V	0 10000.0000000010	1.0045
0.0	0 10000.0000000000	1.0
-0.0024 V	0 01111.1111111110	0.9955
≤-5 Volts	0 01100.0000000000	10^{-4}

Normal 2's complement with sign extension is easily obtained by changing the wiring to the board. The conversion can also be done in software on the 8080 with this sequence:

```
RLC
RLC
CMC
RAR
CMC
RAR
```

The timing sequence is given:

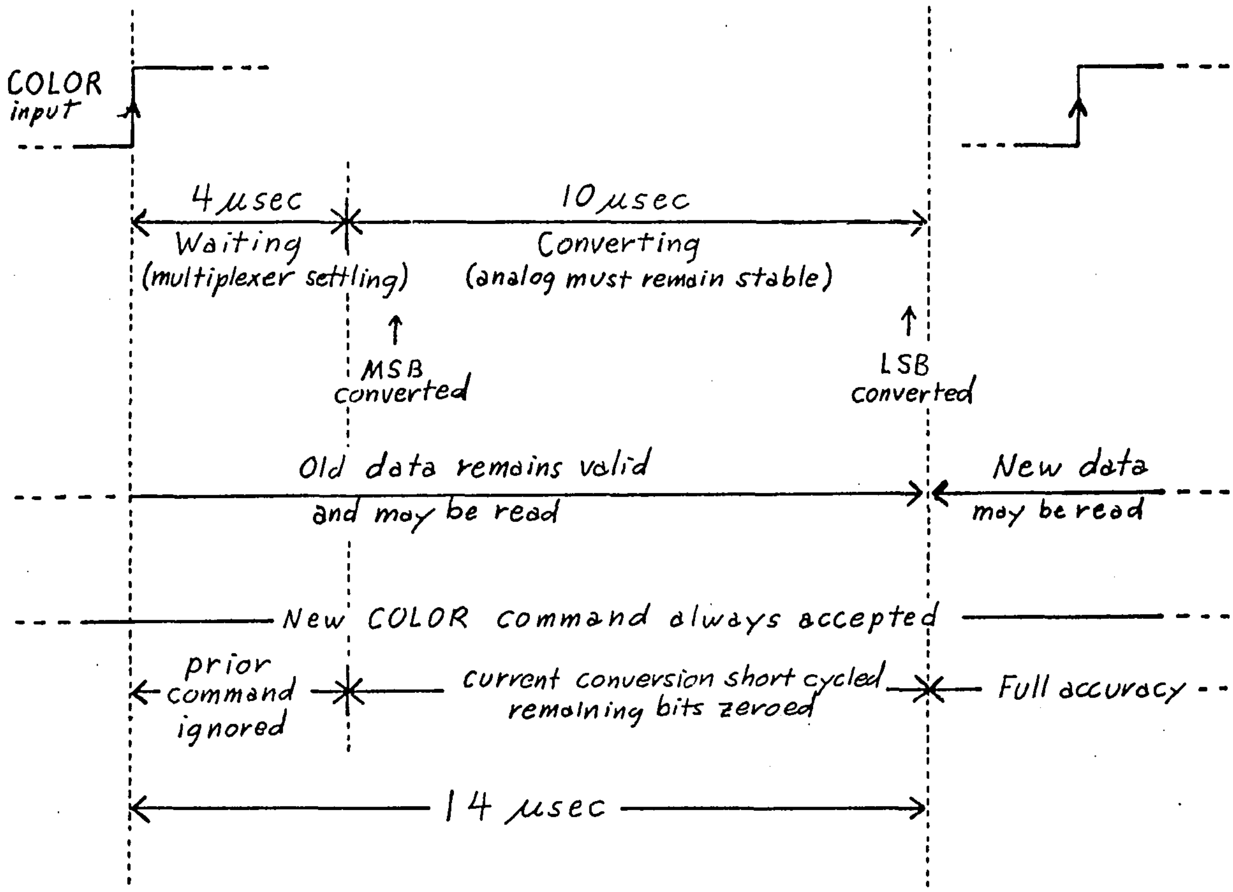


Figure 6.16 A/D Conversion Timing

If a new COLOR command is received during conversion, the timing logic short cycles the converter, filling the remaining less significant bits with 0, and immediately transfers the abbreviated word to READ A/D/ output. A normally timed cycle is then initiated, including the 4 μsec wait as the analog input changes. If the new COLOR command is received during the wait cycle, the previous command is ignored, timing is relative to the new command, and the old data remains valid. Thus two identical COLOR commands within 4 μsec of each other effectively extend the wait cycle. The timing logic allows a valid conversion to be initiated at any time without regard to program history. The old conversion is salvaged, and may be used as an approximation or ignored.

The conversion proceeds so rapidly that with a minimum of program prearrangement the data will be ready before it is needed. The software overhead necessary to execute an interrupt from an unknown program environment would at least triple the effective conversion time. Because the old data may be read after a new COLOR command, the following sequence is possible:

Start color 1

Finish old business

Start color 2

Read and then store or process color 1

Start color 3

Read and then store or process color 2

Read and store or process color 3

The speed of conversion relative to software execution can be monitored with the Alignment Board by taking advantage of the short

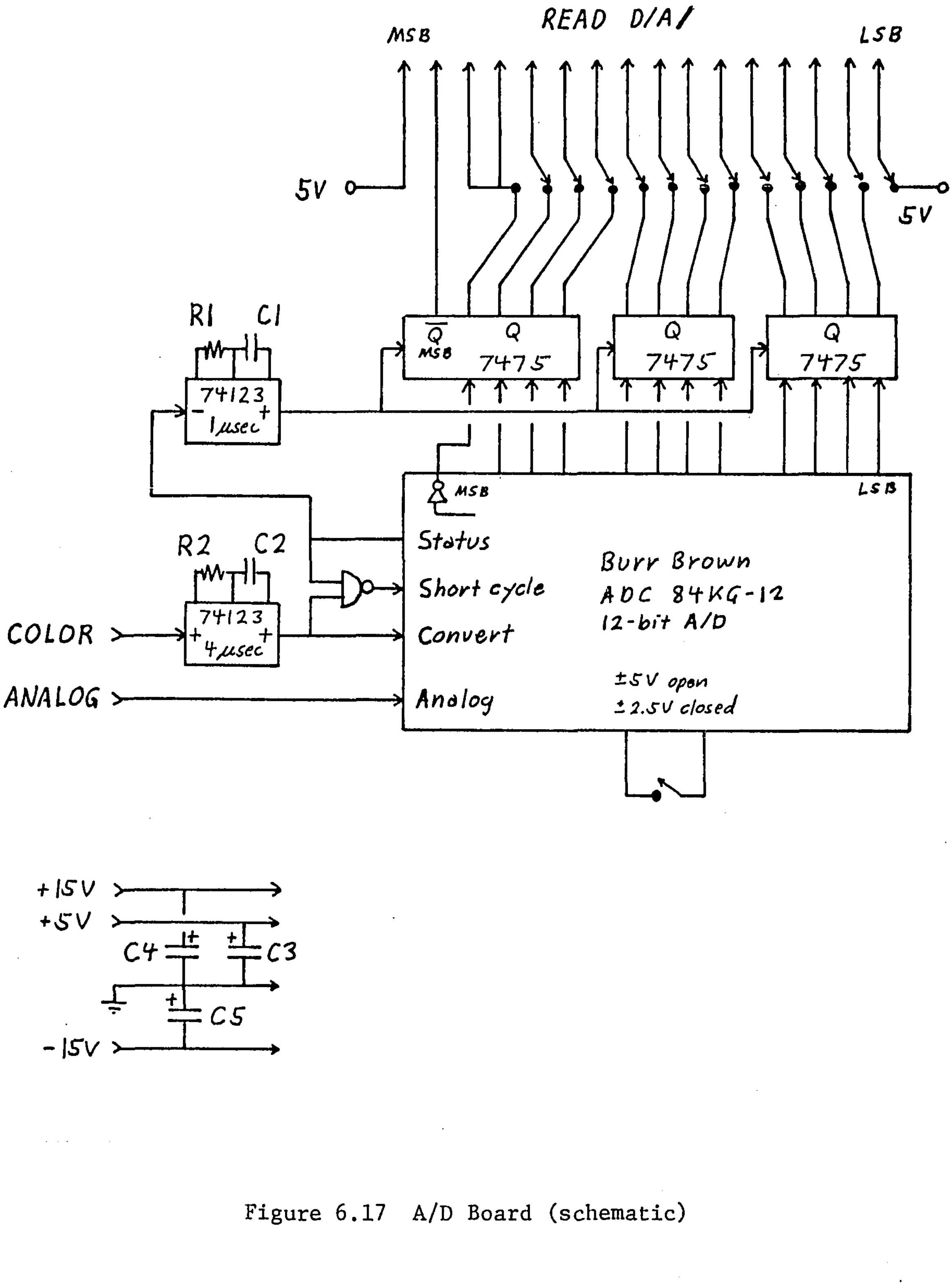


Figure 6.17 A/D Board (schematic)

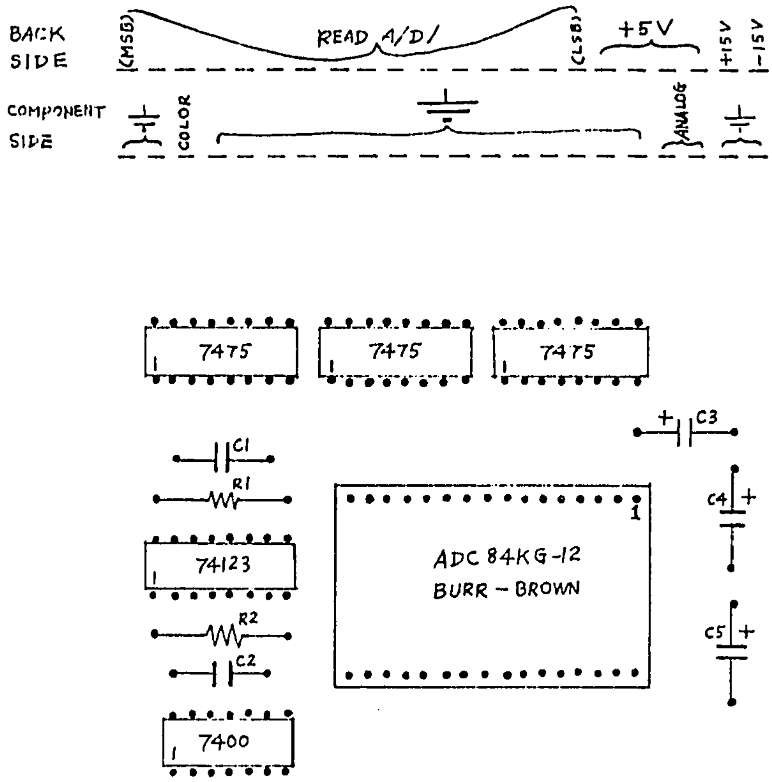


Figure 6.17 A/D Board (components)

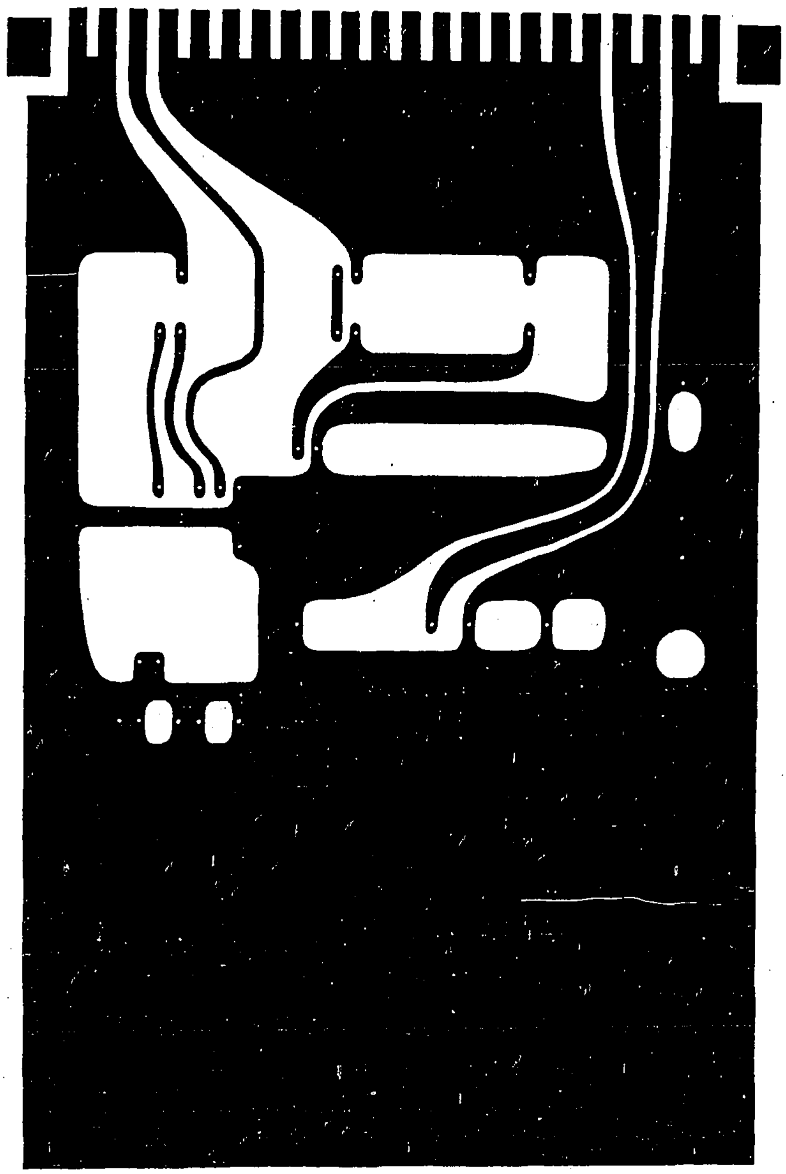


Figure 6.17 A/D Board (parts side)

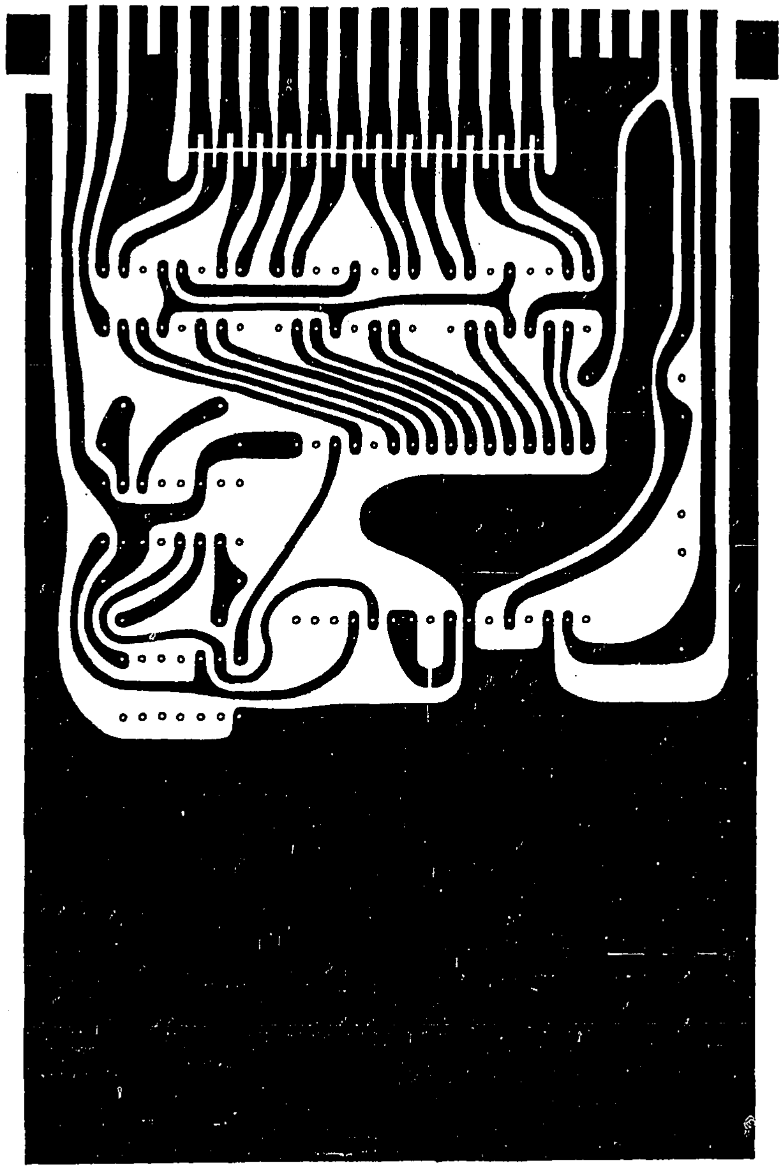


Figure 6.17 A/D Board (back side)

cycle provision. For example, set X POSITION = +1 and Y POSITION = -1. Then the 256·(X-Y) channel will be normally converted as:

0 10011.1111111110

If, however, the number

0 10011.1111111000

is read instead, then there was insufficient time to complete the last two bits of conversion.

Adjustments

The schematic shows 13 solder-jumpable switches. When soldered as shown, the board will have the range and accuracy specified. Changing all will:

1. Halve the range (±2.5V in, FOCUS 10.10 10^2 to 10^{-2} OUT)
2. Halve the step size, doubling the accuracy
3. Will not affect software for signals in range

The noise in the photomultipliers (a quantum calculation performed but mercifully omitted) and in subsequent arithmetic make the last bit of resolution meaningless. In its place we buy the luxury of 8 orders of magnitude input range, which, with 32 orders of magnitude computational range, allows scaling factors to be virtually ignored.

Triode Driver Board

This board drives the CRT electron gun to produce the desired spot intensity. Inputs include a logarithmic analog signal specifying desired beam intensity, a digital bit to control beam blanking, and unregulated high-voltages. Outputs include voltages to the CRT electron gun. The board provides rapid translation of the logarithmic-coded input to the correct drive voltage, very rapid beam switching, interrelated voltage regulation, and protection for the CRT.

Special Features

The complex gamma correction translating FOCUS number system logarithmic coding to the 7/2 power relationship of the beam current and drive voltage is performed with high accuracy at video speeds.

Connections

ANALOG BEAM INTENSITY	Logarithmic analog input to control beam intensity. The normal range is -5V to +5V corresponding to an attempted relative beam intensity of 10^{-4} to 10^{4}. The input impedance is 10 KΩ.
BEAM GATE/	The beam will be unblanked when this input goes low. The input is TTL compatible with load of 4 standard circuits. A 1 KΩ pull-up resistor insures the beam will be blanked if this input becomes open circuited.
+340V, -340V	Unregulated but well smoothed, low current supply inputs.
CATHODE	Output to CRT cathode. This voltage will be +50 volts for blanking, 0.1 volt when the beam is unblanked, and is a function of BEAM GATE/
GRID 1	Output to CRT control grid. Normally -20V to -100V. A function of ANALOG BEAM INTENSITY and CRT specifications. It is clamped to ground against positive voltages.

GRID 2 — Output to CRT isolation grid. Voltage is fixed at +100V to +300V, depending on CRT specifications. It is zenar-clamped against high voltage transients, provides normally a low dynamic impedance, but relatively high impedance when shorted to ground.

Electron Optics

To understand the operation of the Triode Driver Board some explanation of electron optics is first needed. The review of this field and subsequent discussion of the operation of the circuit is purposefully at a basic level. Features are not discussed for which complexity of explanation outweighs the importance.

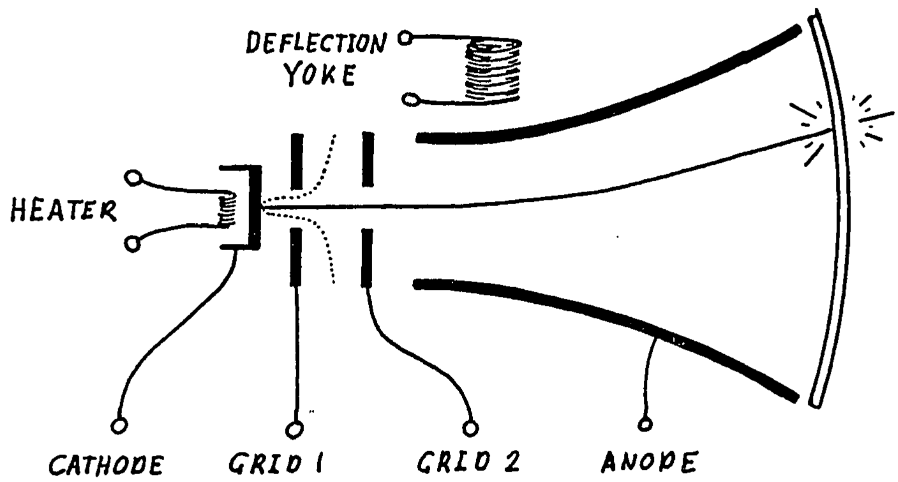


Figure 6.18 Simplified CRT

HEATER — A "warming pad" to raise the cathode to emission temperature. Typically 6.3 VAC is applied. Its potential should not deviate more than about 100 volts from the cathode to prevent a vacuum diode effect.

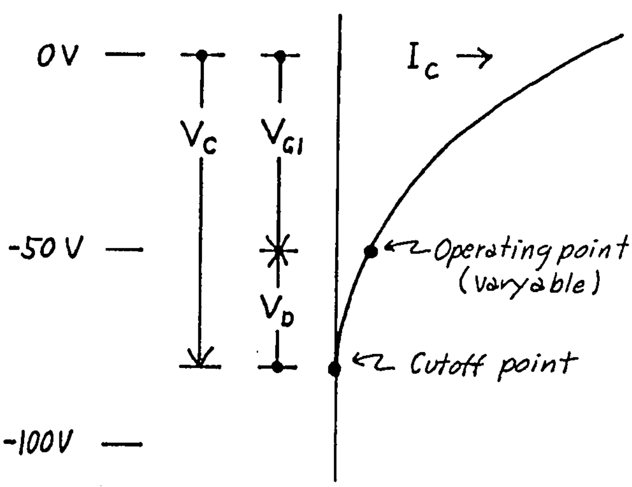
CATHODE	A source of electrons. It is assigned a reference potential of zero. The effects of other potentials can be visualized by allowing all other voltages to change relatively.
GRID 2	Positively charged attraction for cathode electrons. It isolates cathode from anode to provide better control and safety in case of discharge. It should be fixed at a potential of typically 200 volts, dependent on the CRT.
GRID 1	Negatively charged control of beam intensity. If charged strongly negative, cathode electrons are repulsed, but if neutrally charged, a potential "finger" from grid 2 reaches through the hole in grid 1 to pull electrons from the cathode. A typical grid 1 potential is -50V and variable according to desired beam current.
ANODE	Accelerating attraction for the electron beam. The image is brightened and sharpened by higher potentials, however above +15 KV soft X-rays become a biological hazard. A typical operating potential is +20 KV.
DEFLECTION YOKE	Magnetically bends the beam to move the image. A typical yoke requires 1 amp for full deflection and appears as a 1 mH inductive load, limiting band width and settling time. Some CRTs use the much faster electrostatic deflection, however

because of the attendantly required low anode voltages, such tubes are inherently dim and of low resolution. They are used in oscilloscopes where high speed is essential but a beam that can cut through the glass in a few seconds if undeflected is not a desirable trait.

FOCUS

Some CRTs use magnetic focus. Others introduce a third grid dividing the anode, called the focus grid, or grid 3. Grid 3 potentials for an electrostatic focus CRT may be from 0 to 6 KV, with 200V typical. In many CRTs, focus changes as a function of position, so Grid 3 voltage must become a function of deflection yoke currents.

Some parameters and their interrelations are defined:



V_{G1} the negative voltage of grid 1

V_{G2} the positive voltage of grid 2

V_C cutoff voltage--the negative grid 1 voltage at which the spot is totally extinguished

V_D drive voltage--the actual voltage of grid 1 above V_C

I_C cathode current

V_A anode voltage

Figure 6.19 CRT V/I Interrelations

I_C is generally taken as a linearly proportional indicator of screen brightness, however 3 effects result in suppressed intensity at higher current levels. These are:

1. At low levels 100% of I_C reaches the anode, but in restricted aperture CRTs, this drops to about 50% at high current levels.
2. At low levels typically 60% of the current measured in the anode circuit actually reaches the phosphor screen. This efficiency drops to about 20% at high current levels.
3. Phosphors exhibit saturation effects.

Some useful formulas are given, with equalities meaning "nearly equal":

$$I_C = \frac{K \cdot V_D^{7/2}}{V_C^2} \mu A \quad \text{typically } K \simeq 3$$

$$V_C \propto V_{G2}$$

Information $\propto$ 1/spot size^2 (approximations)

$\propto I_C^{-.26} \propto \text{brightness}^{-.26}$ } constant V_A and V_C

$\propto V_A^{2.3}$ } constant brightness

$\propto V_C^{.8}$

Control of Spot Intensity

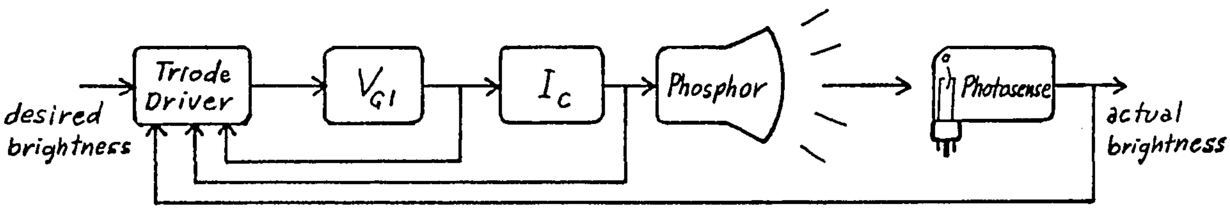


Figure 6.20 Brightness Control Block Diagram

The block diagram above represents the CRT imaging system. The computer output is a desired brightness which the system causes to be output as radiant energy. In choosing the parameter to be directly controlled, $V_{Cathode}$, V_{G1}, and V_{G2} are considered. $V_{Cathode}$ should be invariant to minimize image size change, and V_{G1} requires less modulation at a lower voltage than V_{G2} with the same general effect. Therefore the system establishes V_{G1}, which effects I_C. We can measure I_C which affects screen brightness, and we can measure screen brightness.

Consider including the photosensor in the feedback loop. This provides the truest control, but requires overcoming many obstacles including:

1. Phosphor time constants of between 1.5 and 60 μsec, which are nonlinear.
2. Residual phosphorescence that continues exposure, but cannot be terminated by a "negative" control.
3. Nonlinear effects vary open loop gain orders of magnitude, affecting stability and settling.

Final brightness will be controlled and compensated through software that allows necessarily complex algorithms to be implemented and changed at will. The phosphor-limited speed is computer compatible. However, the Triode Driver must still provide a reasonable approximation of unity gain to aid the software.

Consider a system controlling I_C as a reasonable approximation of screen brightness. This parameter is easily measured, but trouble occurs when the loop is closed at this point. Typically an I_C of 10 μA is produced by V_{G1} rising 20 volts above V_C. A 10 pf capacitance between grid 1 and cathode introduces an error with a time constant of 20 μsec. Because I_C decreases much faster than V_{G1}, the time constant can be an order of magnitude worse at low I_C.

I_C is quite accurately controlled by V_G according to the formula

$$I_C \propto V_C^{7/2}$$

After the fractional power is computed, V_{G1} can be established very rapidly, and what transients exist can be settled before the beam is unblanked allowing I_C to start flowing.

A typical plot of radiant power vs. V_{G1} is shown:

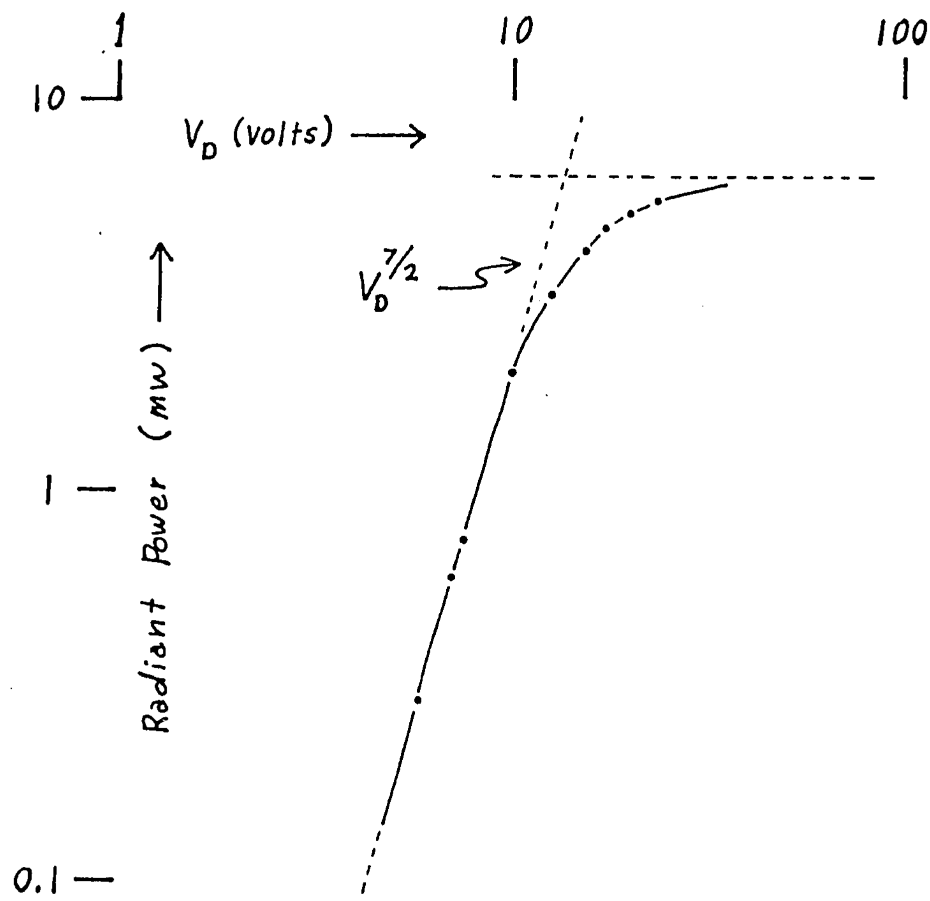


Figure 6.21 Phosphor Brightness vs Drive Voltage

Gamma is a photographic term expressing change in photographed brightness per change in scene brightness. A high contrast film has a high gamma. Gamma varies as a function of exposure, eventually falling to zero at both extremes. So called gamma correction circuits are used in precision CRT displays to make the screen brightness linearly proportional to a control signal. In the scanner, the circuitry is complicated by:

1. The control signal is logarithmic.

2. The control signal covers 8 orders of magnitude.

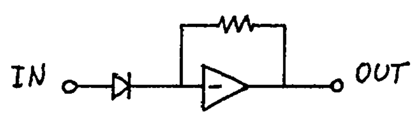
Assuming brightness $I_C \propto V_D^{7/2}$, then the brightness can be controlled by

1. computing the logarithm of the voltage representing the desired brightness,

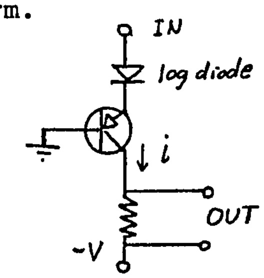
2. multiplying by 2/7, and

3. exponentiating to yield the required V_D.

Step 1 is obviated by the logarithmic coding of the input signal. Step 2 can be combined with the necessary scaling. Step 3 is easily performed at low frequencies using a logarithmic diode and operational amplifier, connected as shown below.



However, this circuit has serious frequency limitations because, as the gain $\frac{dOUT}{dIN}$ varies over orders of magnitude with the effective signal, so does the band width for amplification beyond unity gain. The very marginal video frequency response of the operational amplifier becomes worse as a function of signal level. The circuit used in the scanner is shown below in greatly simplified form.



Neglecting secondary effects, the basic response of this circuit is OUT = i = e^{IN}. With reasonable current levels, the circuit performs well at video frequencies throughout the range of input signals.

Grid 1 Supply

Referring to the actual circuit, R2 and R3 form a voltage divider to scale the input by:

$$\frac{\frac{59.2 \text{ mV/transistor}}{\text{decade}} \times 3 \text{ transistors}}{\frac{\pm 5 \text{ volt range}}{\pm 4 \text{ decade range}}} \cdot \frac{2}{7} \simeq \frac{1}{25}$$

The thermistor and R1 provide 3-point temperature compensation. C6 is a peaking adjustment. P1 trims the 7/2 power relationship without affecting the adjustment of temperature compensation. Given the specified 10 K input impedance and the 1/25 voltage division, the Thevenin resistance of the divider network is 400 Ω. With the collector of T1B connected to +5V rather than in a diode configuration, this 400 Ω becomes effectively 1½ Ω, half the specified error inherent in the 3 series log transistors, an error far below nonlinearities in the CRT. The error could be reduced further by similarly connecting the collector of T2B to +5 V, however, unlike the case with T1B, in this second case bandwidth would suffer. By designing a circuit compatible with a simple resistive divider network, fidelity, reliability, and economy are all improved.

Transistors T1A to T3A provide offset biasing. OP-1 transfers this offset compensation and also provides rapid correction for V_{BE} of T4. Note especially that OP-1 is not in series with the signal path and therefore does not limit the high-frequency response. Zener D1 connected to OP-1 together with R5 provides a voltage-independent reference current.

R6 will also supply reference current as explained later. The limitations of this arrangement are:

1. Some base current flows through T4
2. T4 also acts as a log component

The effect of point 1 is negligible in this application. The effect of point 2 is cancelled by OP-1 as soon as it can act. The 25% attenuation of very high frequencies is balanced somewhat by C6. Both the HF attenuation and offset error in OP-1 are lessened proportionate to the number of series log elements.

The voltage desired for V_{G1} is developed across R8 from the exponential current through T4. This arrangement also translates the desired signal from ground-reference to variable V_C-reference, to which R8 is terminally connected. Zener D2 reduces voltage and power stresses on T4 and also limits maximum V_D. T5, connected in a voltage-follower configuration allows the voltage of the capacitive load of GRID 1 to be pulled up at video-compatible slew rates. R10 biases T5 with a nearly constant current for the proper "muscle tone" in the steady state. The voltage follower T6 is connected in a unique arrangement with C7 and R9 to provide with T5 a HF push-pull output with few parts but no compromise in fidelity. The arrangement works if the charge transferred from C7 to the capacitive load lowers the voltage across C7 less than about 20 mV, corresponding to a multiplicative halving in current through T6. This constraint is trivial because:

1. C_{G1} is very small, $\simeq$ 20 pf with wiring capacitances
2. C7 operates at low voltage
3. C7 leakage is not critical

Note that T6 has no direct effect on offset in the steady state. The small current through R10 and T5, although negligible in its drift-effect on the voltage across R8, is also balanced by the small current through R9 and T6.

R7, connected between ground and T3A, provides a temperature-inclusive $3 \cdot V_{BE}$ reference current reaching R8 through T4. When R7 = 3·R8 then the additional current into R8 produces a voltage balancing V_{BE} of T5. This unique arrangement provides benefits over the standard practice of balancing V_{BE} with a second transistor:

1. Fewer parts, but more important...
2. Current through T4 remains above a level set by R7, thereby maintaining fast and accurate response at all signal levels.

Grid 2 Supply

R13 with series zeners D4 and D5 provide voltage for GRID 2. This disarmingly simple arrangement has unsuspected sophistication, as explained in the section on "Safety," and is possible because errors in V_{G2} are compensated.

V_C of the CRT is directly proportional to V_{G2}. Rather than accurately regulate V_{G2} and reference V_C, their ratio is regulated. R14 and R15 with trimmer P2 provide a voltage divider whose center node becomes zero volts when V_C has the proper voltage relative to V_{G1}. T7 and R11 provide a current source pulling node V_C against the current from R12 with a current proportional to the output of OP-2. C8 completes an integrator. C9 adds a zero root to stabilize the loop through OP-2. Wide stability margines are obtainable with good control. Zener D3 reduces the substantial power to T7.

There remains a second effect of changes in V_C as set by V_{G2}, as shown:

$$I_C \propto \frac{V_D^{7/2}}{V_C^{2}} \Rightarrow V_D \propto V_C^{4/7} \qquad \Bigg|_{I_C = \text{constant}}$$

Thus if the magnitude of V_{G2} and thus V_C increases by 7%, V_D should increase by 4%. The apparently difficult analog multiplication of V_D is easily performed while the signal is still logarithmic. The reference current into T3A multiplies V_D by the proper amount by choosing R6 and R5 such that the current through R6 is 4/7 of the total current through both resistors.

Cathode Supply

The beam is switched by controlling the cathode voltage. This method has advantages:

1. Relatively low voltages are involved.
2. Deblanking by ground-clamping minimizes transient overshoot.

Points of caution are:

1. The cathode-heater voltage difference must not be excessive.
2. During transition, the cathode-anode voltage, and hence the image size, will change.

Point 1 of cautions is easily controlled. Point 2 is considered negligible if transitions are fast. At 20 KV anode voltage, a 10 volt cathode transient will move the spot 1/4000 of its radial distance from the center of the screen, an amount both less than the spot size and more important, consistent.

Parallel TTL gates output to T8 through R17 and impulse capacitor

C10. As T8 switches on, T9, normally off, remains off as V_{BE} goes ½V negative. T8 will overcome the small current through R18 to pull down the capacitive load CATHODE through D12. When CATHODE is within ½ volt of ground, R19 provides the final discharge path. When T8 opens, R18 provides a current through R19. Given I_{R18} = 2 ma and R19 = 1 K, 1.5 ma will flow through the base of T9, rapidly slewing CATHODE. When CATHODE reaches the voltage set by D6, R19 carries V_{BE} of T9 to zero, switching off T9 to allow the fastest response to the next command. R20, C11, D7, and D13 provide voltage for T9.

Safety

The circuit provides safety for the CRT and for itself.

The impedance characteristics of the GRID 2 output are nearly ideal. It is zener clamped against high voltage discharge from the anode to protect the cathode and external circuitry, it has high impedance when shorted to ground to protect the cathode from secondary discharge, and yet it provides low dynamic impedance in normal operation.

The GRID 1 output is diode clamped through D8 to ground to protect the anode from a positive GRID 1 voltage in case of internal discharge.

D9, D10, D11, and T11 protect the circuit and OP-2 from each other when one or both of the ±340V sources are inactive.

It is the responsibility of other circuitry to insure the beam is not deblanked for an excessive time. However should the BEAM GATE/ connection be lost, R16 insures the beam will be blanked. D6 and D14 voltages should be low enough to protect the cathode-heater relationship, but high enough to absolutely insure blanking.

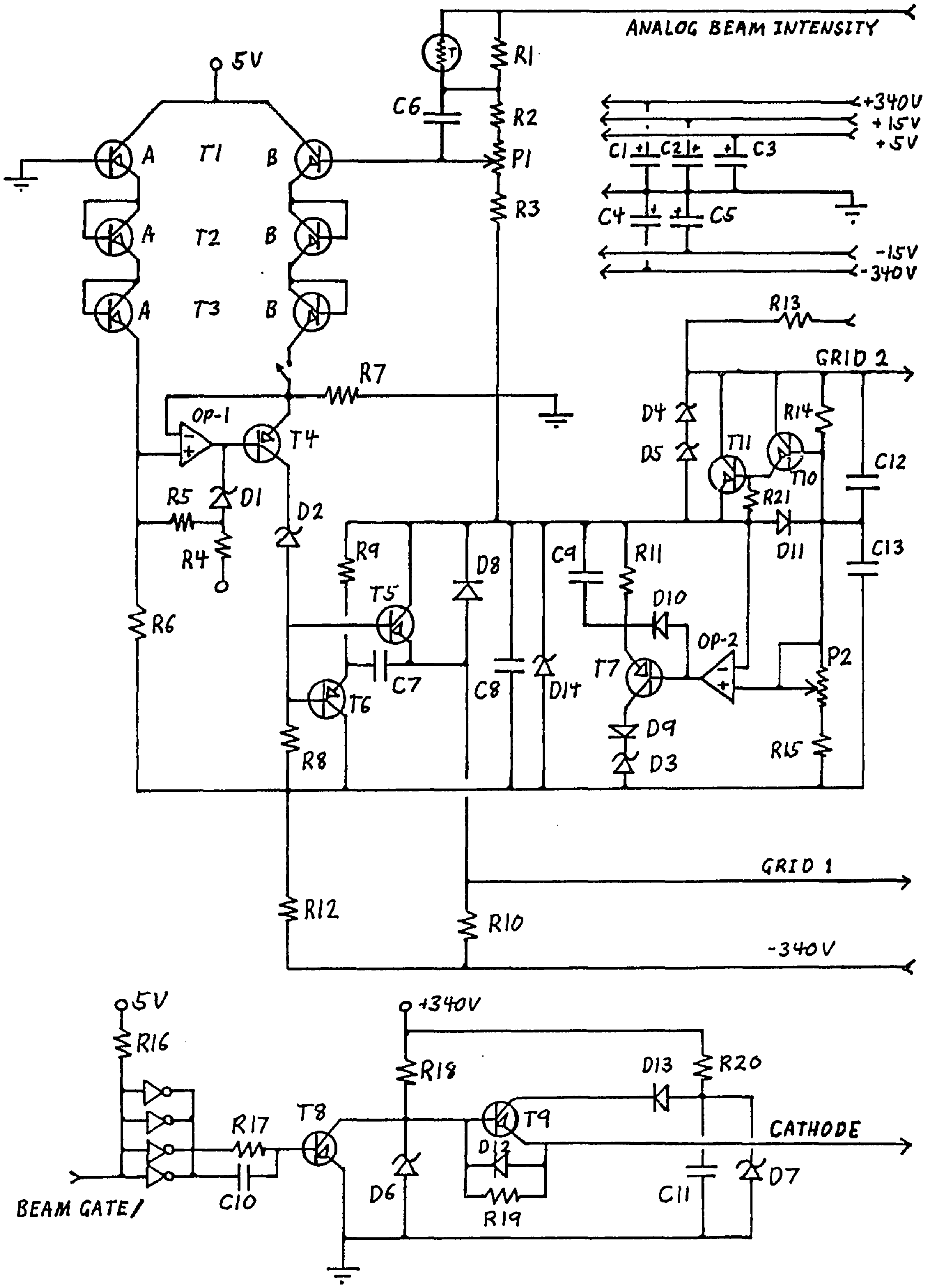


Figure 6.22 Triode Driver Board (schematic)

Trimmer P2 is connected such that momentary loss of contact will reduce rather than increase the beam for protection during V_C adjustment. If for any reason, such as failure of the -340V source, warmup transient, excess current in R8, or component failure, V_C rises beyond the set point, T10, T11, and R21 will pull down the GRID 2 accelerating voltage to prevent an uncontrolled deblanking.

During power up and down, the +340V source is specified to rise last and fall first. D3 allows a residually negative GRID 1 voltage under these conditions, insuring cutoff.

With 20 KV that can travel along signal wires like lightning and an electron beam that can cause implosion cutting in seconds, a multi-thousand dollar CRT may not be all that is saved through safety precautions.

X-Yoke Driver

The yoke driver boards translate the positional voltage control signal into a current signal that induces a magnetic field in the yokes, thereby deflecting the electron beam.

Special Features

The circuit provides a precision current source controlling ±40V up to ± 10 A into an inductive load. Multiple internal feedback paths with feed forward provide very fast, low distortion open loop characteristics for very rapid settling in closed loop. True differential signal ground input and low drift allow 16-bit compatibility. The circuit is surprisingly sparce and economical.

Connections

X POSITION and X GROUND — Input controls spot position. Range = +10V to -10V, with -10V moving the spot far right, +10V far left. Input impedance = 10 KΩ. Differential input allows separate signal ground.

Several external modules require interconnection. See schematic. Also see section labeled "Power" for description of voltage requirements.

Operation

As with other boards, the Yoke Driver has been redesigned several times to yield a powerful circuit of deceptive simplicity.

The basic operation is illustrated with the circuit below:

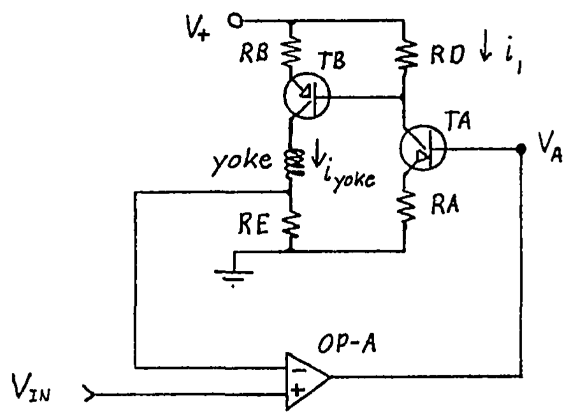


Figure 6.23 Simplified Yoke Driver Schematic

A voltage at open-loop input A is transformed to a current i_1 by TA and RA. i_1 generates a voltage across RD, which is used by TB and RB to control the yoke current. The yoke current is measured by RE and compared with the desired response given by V_{IN}, allowing OP-A to close the loop.

Referring now to the actual circuit, the yoke current $i_{yoke} = i_+ - i_-$ should be proportional to the open loop input V_{IN}. However, the individual currents i_+ and i_- are not linear with respect to V_{IN}.

The figure below depicts the relationships of i_+, i_-, i_{yoke}, and V_A.

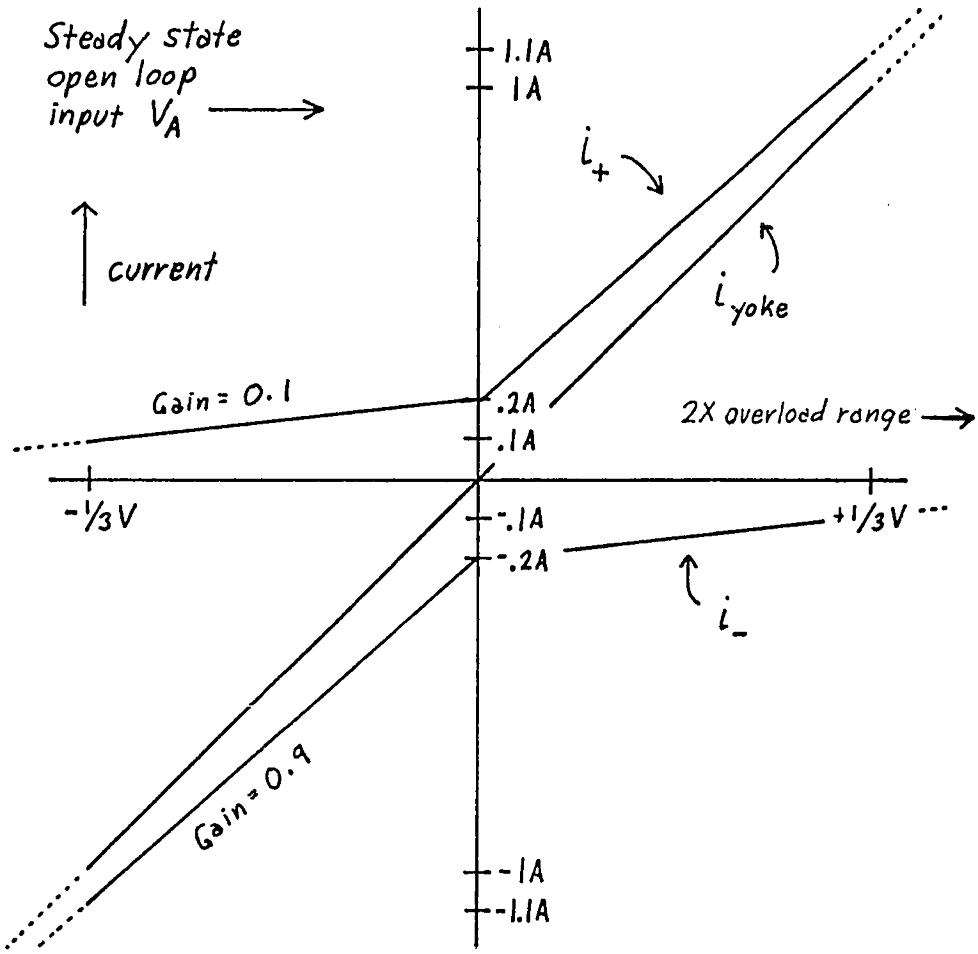


Figure 6.24 Yoke Driver Bipolar Characteristics

Some points:

1. Compared to DC biasing, range is increased and power saved
2. i_{yoke} will be linear even transecting zero, as presented later
3. i_+ and i_- remain non-zero to maintain "muscle tone," prevent switching transients, and allow some reserve, as seen later.

The non-linear biasing arrangement has disadvantages:

1. HF characteristics change with polarity due to mismatching
2. Serious troubles with HF response when transecting zero

Both of these drawbacks are obviated by the arrangement below in which

i_+ and i_- share in reproducing high frequencies:

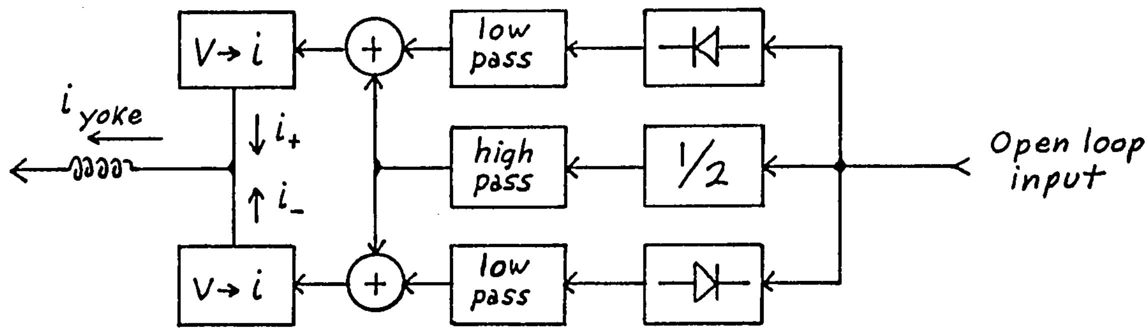


Figure 6.25 High Frequency Crossover Diagram

This arrangement allows:

1. Uniform HF characteristics
2. Fast response by sharing the load. Although the slew rate is fixed by supply voltage, the circuit can pull into and out of slew rate changes faster.

A sample response is shown below. Note the HF load sharing and smooth zero transition:

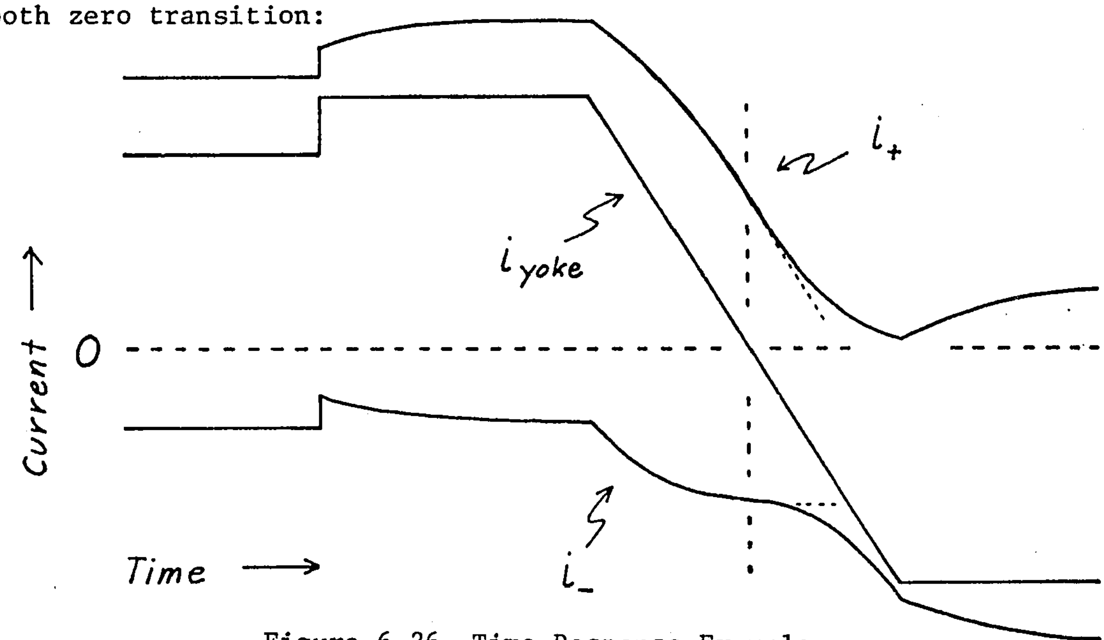


Figure 6.26 Time Response Example

The circuit contains internal feedback to track even signals transecting zero, feed forward bypassing slower op-amps, and two differential feedback inputs. These and other features are now detailed.

The positive portion of the open loop input at V_A is passed by T1A and offset balancing T1B to R6. By using a diode connection for T1A and a transister connection for T1B, both the nonlinear load of R6 and the biasing current through R7 are insignificant viewed from V_A. In this arrangement I_E of T1A can be about $\sqrt{\beta}$ times less than I_E of T1B for equivalent V_{BE}. R8 provides a small coupling to negative excursions of V_A as required, and will also cancel the loading effect of R21 and R22.

Voltage follower OP-2 imposes the proper potential across R12 + R13, and thus via T2 to R15 translates this voltage into the +40V reference section of the circuit. V_{BE} of T2 is within the feedback loop, and is thus negated.

R9 and R10 act as a voltage divider, allowing most of V_A to pass directly to the base of T2. The nonlinear biasing and HF specifications require the gain from V_A through R9, and R10 to be about half of the gain from R6 voltage, and R9, R10, R12, and R13 are chosen accordingly. The gain from OP-2 to T2 must be sufficient to bias T2 throughout the normal range of V_A.

The low pass block presented earlier is provided by C5. This method does limit the slow rate of OP-2, however feedforward and OP-3 virtually eliminate the bad effects, and the circuit is simplified to a surprising degree. The high pass block is not directly implemented, but exists implicitly as OP-2 seeks to cancel the low frequency residue.

R21 and R22 provide a voltage proportional to $i_+' - i_-'$, which will be translated to the yoke current. OP-3 acts to maintain this measure proportional to V_A, thus providing an exactly complementary biasing curve free from deadband, and also correcting all anamolies up to the response speed of OP-3. D5 allows OP-3 to increase i_+' after reducing i_-' to zero, thus giving OP-3 total control to null errors. The D5 arrangement also prevents saturation of OP-3 with attendent long recovery times. It can be shown such a limiting arrangement is not needed with OP-2. The specified op-amp allows a +3V Jump before encountering slew-limitations, allowing the D5 arrangement to oeprate very quickly. OP-3 is compensated for greater-than-unity gain, and remains stable with the gain through D5.

R19 provides a direct path from V_A to the base of T6. With proper resistor values there will be almost no HF error, leaving OP-3 to act on residual anomolies and lower frequency nonlinearities. The gain of V_A through R18 shunted by R19 to T6 is chosen to be less than that to T2 from V_A to allow higher transmission from OP-3 for optimum distortion correction. This necessitates a lowering of R20 relative to R12 + R13 and a non-symmetric R21, R22 bridge. The common scaling factor for R19 and R18 is chosen so that the output of OP-2, as viewed from V_A through R9 and R10, is balanced with the output of OP-3 viewed through R18 and R19 to present to V_A a linear resistive load. R14 and R23 provide DC biasing. C7 and C8 cancel capacitive effects of the transistors at very high frequencies.

The circuit presented thus far develops across R15 and R24 voltages representing the desired currents i_+ and i_-. Complementary power stages translate voltages into currents. One stage is discussed.

The voltage across R15 is impressed across R28 via voltage follower stages consisting of OP-4, T3, T4, and T5. The voltage across R28 is nearly proportional to i_+ up to about 3 MHz, providing a feedback path to high-speed OP-4, correcting transistor offsets and other anomolies. C9 provides intermediate feedback to insure stability while retaining some feedback at the highest frequencies. D6 protects T3 and prevents OP-4 from saturating. R29 protects T3 from excess current. D7 protects T5, T9, and the user from high inductively induced voltages.

The inductive load viewed through the collector-base capacitances of the Darlington coupled transistors appears as a very large Norton capacitance. R26 is connected to +V to provide a uniformly high biasing current at all signal levels. Depending on transistor characteristics, it may be desirable to reduce this capacitance by connecting the collecter of T4 directly to ground, and R27 to either ground, or better, +V.

So far the circuit accurately transforms V_A into the yoke current. To attain the extreme accuracy desired, an overall loop is closed via OP-1.

Resistor R1 translates i_{yoke} into a voltage that OP-1 compares with X POSITION. In order to provide an accuracy no worse than that of the 16-bit converter, the resistance must not drift by more than:

$$\frac{\frac{1}{2}\text{ LSB}}{\text{Full range of D/A}} \times \frac{\text{Full diameter of CRT}}{\text{Effective average radial distance from center}}$$

$$\simeq 20 \text{ ppm}$$

Unlike temperature drifts elsewhere in the circuit, this is spot-position dependent due to self heating, and thus contains random transients that do not stabilize with equipment warmup. Three precautions are appropriate:

1. Use an ultra-low drift resistor. ± 30 ppm/°C is barely acceptable. TC cancelation will not work due to time effects.
2. Use a high-power resistor. 50 watts is barely acceptable. Heat sinking reduces longer transients, but not shorter ones. An electronic thermostat may control a heat source of the same sink.
3. Use a very low test voltage. At 1/3 volt, the drift of R1 exceeds the drift and noise of very low drift OP-1.

R1 is the weakest link in the feedback chain, followed by OP-1 and R2 and R4. All must be precision.

Requirements are made of the feedback circuitry:

1. Because of R1 $\simeq 1/3\Omega$, high ground currents, low voltages, and required precision, differential sensing connections are essential.
2. Because of high ground currents between the scanner and yoke driver, X POSITION input must also have differential inputs.
3. Bandwidth must be adjustable.
4. The circuit must provide integral control, but should respond to a step input with a step output without waiting for feedback, thus passing higher frequencies open-loop to the limits of the op-amp, while controlling lower frequencies.
5. For minimum drift, only one operational amplifier should be used.

The OP-1 circuit satisfies all these requirements. D3 and D4 with D1 and D2 prevent OP-1 from saturating, and also prevent excessive V_{EB} at T6 and with proper R9 at T2, and prevent excessive V_{CE} at T1B.

Adjustments

As given, component values result in a range of ±1A yoke current in response to a ±10V input. For a range of ±KA, divide R28, R33, and R1 by K.

Small changes in gain are accomplished by changing R1 only. Larger resistances can be added in parallel until the desired gain is reached. Note the required ultra low drift of the composite R1.

DC bias of i_+ is adjusted by R14, of i_- by R23. A change in these values should be followed by modification of R8 to prevent negative biasing up to a 2x overrange value of V_A.

C3 controls feedback bandwidth. C4 should be matched with consideration for op-amp bandwidth.

Power

Power requirements are listed:

+40V -40V	20 to 50V, low precision but well filtered. Higher voltage gives faster beam slewing, but voltage and power limits of transistors should not be exceeded. Current ≃ yoke current, typically 1 Amp (up to 5A with original television CRT unit).
+50V +30V -30V -50V	12 to 15V, low precision but well filtered supplies floating relative to, and drained toward, their respective center voltage. Max current ≃50 mA
+15V -15V	Precision voltage supplies from scanner. Current ≃ 20 mA

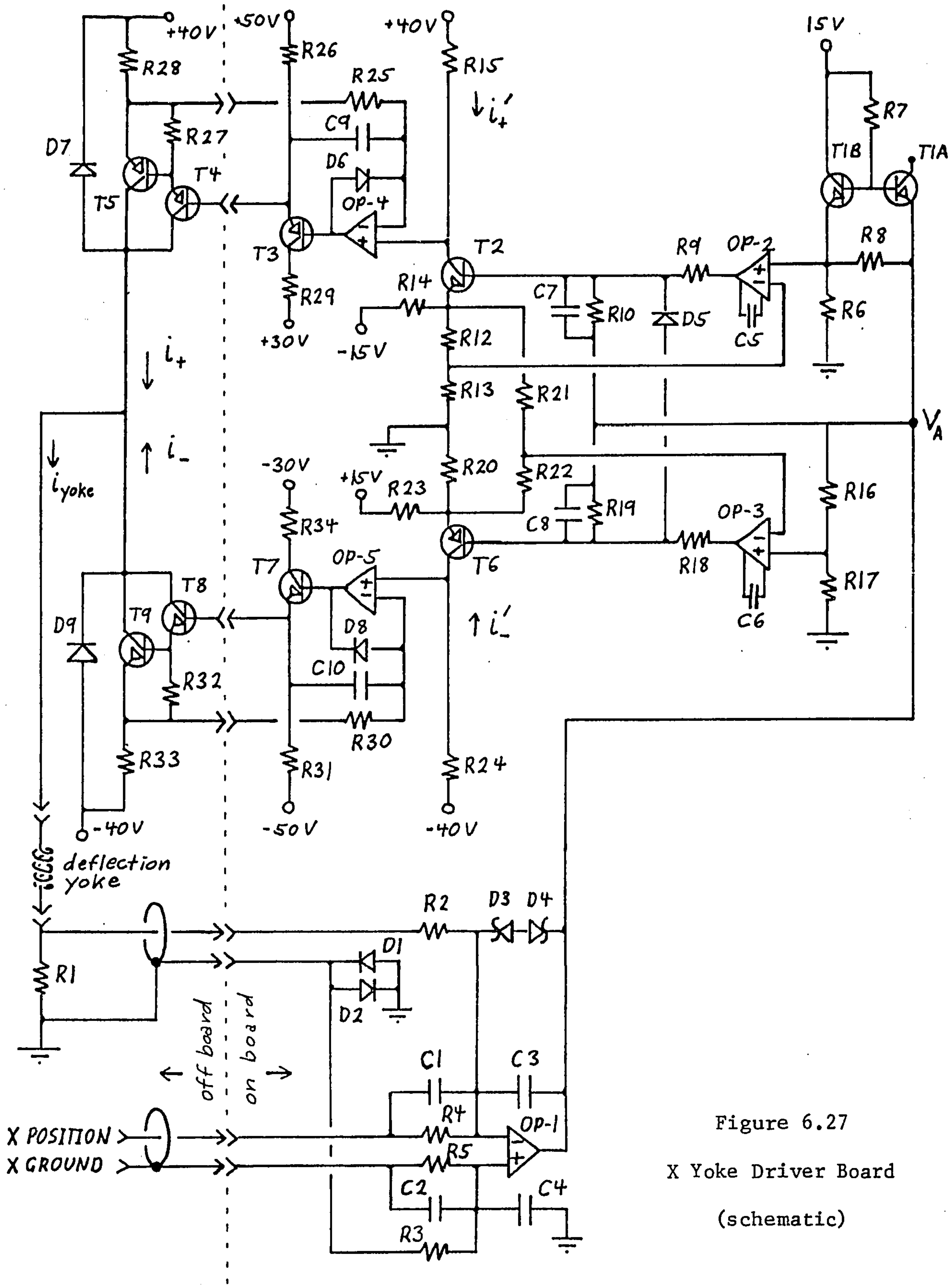


Figure 6.27

X Yoke Driver Board

(schematic)

Photosense Board

Each Photosense Board mounts a photomultiplier, inputs a digital integral RESET command, and outputs an analog signal. Functions are:

1. Precisely amplify the photomultiplier anode current
2. Low-pass filter, with dynamically varying optimum cutoff
3. Integrate and reset on command
4. Derive the logarithm of the integrated signal
5. Supply and regulate photomultiplier dynodes
6. Protect the photomultiplier from overload

Special Features

The order of integration and logarithmic extraction is important. The sequence

$\int \log[f(x)]dx$ Out ← [$\int dx$] ← [Log] ← In

yields an unusable signal because a datum is weighted in inverse proportion to its magnitude, thus if "In" is momentarily zero then "Out" corresponds to zero for the rest of time. Also the time component of the signal is not logarithmic. The order

$\text{Log}[\int f(x)dx]$ Out ← [Log] ← [$\int dx$] ← In

yields the required characteristics, but in the prior art resulted in a severely limited range. The circuit presented does provide the character of an integrate-first system, but allows [signal x time] to be accurately tracked over <u>12 orders of magnitude</u>. From the Photosense Board through the A/D conversion to the FOCUS number system there is virtually complete freedom from scaling. The scanner requires no "volume control."

Other special features and specifications:

1. Dynamically adjusted HF characteristics are optimized to filter quantum effects.
2. Anode current range: 1 nA to 10 mA.
3. Integration range: 1 μsec to 1 second.
4. Reset time: <200 nsec to 1 ppm residue.

Connections

LIGHT Low impedance analog output $\pm$10V at $\pm$1mA

$$= \frac{5}{4} \cdot \mathrm{Log}_{10} \left[\frac{\text{Anode Current}}{\mu\text{A}} \cdot \frac{\text{Integration Time}}{\text{msec}} \right]$$

RESET Digital input, integration is reset on the positive-going edge.

BREAK/ Open-collecter digital output goes low when the photomultiplier is overloaded with light. The BREAK/ of several boards may be combined on one return cable because of the open collector.

Dynamically Adjusted HF Characteristics

FET-input OP-1 and log transistor T1A take the logarithm of the photo-current from the anode of the photomultiplier, I_A. C2 stabilizes OP-1 at low I_A for which the dynamic impedance z_{T1A} of T1A is insufficient to overcome the capacitive loading on the feedback loop from the photomultiplier anode. The choice of C2 is made with two factors in mind:

1. What can C2 be?

   If $C2 \gg C_{ANODE}$ then the feedback loop will have unity gain at all frequencies, including DC at which the photomultiplier appears as a current source. Smaller values of C2 obviously improve response time, however a pole and accompanying zero are introduced, separated in frequency by the ratio

$C1/(C1+C_{ANODE})$. The worst-case phase margin must be considered as the pole-zero pair slides menacingly through the frequency domain as a function of Z_{T1A} inversely proportional to I_A.

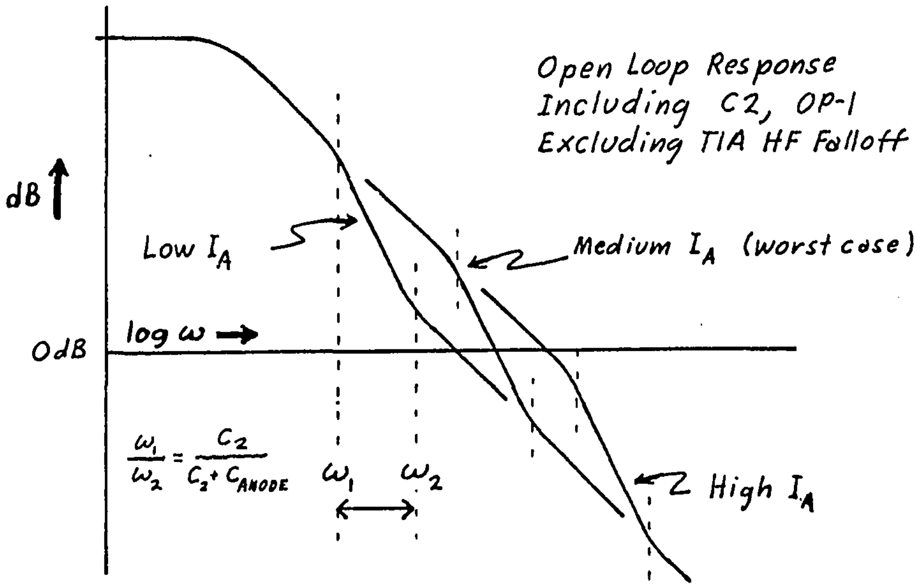


Figure 6.28 Bode Plot Illustrating Stability

If OP-1 has a good phase margin and T1A has very high cutoff frequency for small signals, $C2 \geq C_{ANODE}/10$ is reasonable.

2. What should C2 be?

Assuming OP-1 has infinite gain and is stable, then the output of OP1 $\propto$ Log(X), where X is related to I_A by a single pole low-pass function with $\tau \propto Z_{T1A} \cdot C2$, where Z_{T1A} is the dynamic impedance of T1A $\propto 1/I_A$. How convenient! The fractional quantum noise of the photomultiplier is $\propto 1/\sqrt{I_A}$, while $\tau \propto I_A$ provides a low pass filter attenuating white noise by $1/\sqrt{I_A}$. We can specify tolerable fractional noise permitted in the log signal, the bandwidth varies automatically proportional to photo-current to maintain our specification. Let us now calculate an ideal C2.

$$V_{BE_{T1A}} = \frac{KT}{9} (\ln I_A) + \text{temperature dependent constant.}$$

Then

$$Z_{T1A} = \frac{dV_{BE}}{dI_A} = \frac{KT}{9I_A} = \frac{1}{39I_A}$$

$$\tau = Z_{T1A} \cdot C2 = \frac{C2}{39I_A}$$

Assume the current amplification in the photomultiplier to be 4×10^6, then (with certain approximations of minor effect on this calculation) charge arrives at the anode in packets of $4 \times 10^6 \cdot q = -.64 \times 10^{-12}$ coulombs. Assuming $N_{Arrivals} > 1$, the fractional quantum noise is

$$\approx \frac{1}{\sqrt{\text{number of packets arriving in time interval } \tau}}$$

$$= \frac{1}{\sqrt{\frac{I_A \cdot \tau}{.64 \times 10^{-12}}}} = \frac{8 \times 10^{-7}}{\sqrt{I_A \cdot \tau}} = \frac{8 \times 10^{-7}}{\sqrt{I_A \cdot \frac{C2}{39I_A}}}$$

Let us choose fractional noise = 1. This is an engineering choice, but it can be shown to provide the "best estimate" under certain conditions. Because the only purpose of this prefilter is to prevent wild fluctuations which would not integrate well, a high level of noise is chosen. Then

$$1 = \frac{8 \times 10^{-7}}{\sqrt{I_A \cdot \frac{C2}{39I_A}}}$$

$$C2 = 25 \text{ pf}$$

Because $C_{Anode} < 45$ pf, C2 = 25 pf is seen from part 1 to provide good stability, and so is used. C2 must have extremely low leakage.

Logarithmic Integration Characteristics

Log transistor T1B, matched to T1A, balances the temperature offset of T1A, and also in conjunction with C1 develops the integral equation of the form

$$\mathrm{Log} \int I_A \, dt$$

not

$$\int \mathrm{Log}(I_A) \, dt$$

which would be incorrect. The surprising power of this simple arrangement is now presented.

From elementary circuit theory

$$V_C(t) = \frac{1}{C1} \int_0^t I_C(t) dt + V_o \qquad 1$$

Because of the logarithmic characteristic of T1

$$I_C(t) = K \cdot e^{39[V_B(t) - V_C(t)]} \qquad 2$$

Thus

$$V_C(t) = \frac{K}{C1} \int_0^t e^{39[V_B(t) - V_C(t)]} dt + V_o \qquad 3$$

We wish to show that

$$V_C(t) = \frac{1}{39} \ln\left[\int_0^t e^{39\, V_B(t)} dt + e^{V_o} \right] + V_D \qquad 4$$

Differentiating equations 3 and 4, questioning equality

$$\frac{dV_C(t)}{dt} = \frac{K}{C1} e^{39[V_B(t) - V_C(t)]} dt \overset{?}{=} \frac{e^{39V_B(t)}}{39 \int_0^t e^{39V_B(t)} dt + e^{V_o}}$$

Now assume equation 4 is valid and use it for the instantaneous value $V_C(t)$ on the left above. In doing this, we are assuming equations 3 and 4 are equal at one arbitrary t, and show that then their time derivatives are equal, and therefore by induction they remain equal for all time.

$$\frac{K}{C1} e^{39[V_B(t) - \frac{1}{39} \ln[\int_0^t e^{39V_B(t)} dt + e^{V_o}] + V_D]} dt \stackrel{?}{=} \frac{e^{39V_B(t)}}{39 \int_0^t e^{39V_B(t)} dt + e^{V_o}}$$

$$\frac{\frac{K}{C1} e^{39V_D} \cdot e^{39V_B(t)}}{\int_0^t e^{39V_B(t)} dt + e^{V_o}} \stackrel{?}{=} \frac{e^{39V_B(t)}}{39 \int_0^t e^{39V_B(t)} dt + e^{V_o}}$$

$$\frac{K}{C1} e^{39V_D} \stackrel{\checkmark}{=} \frac{1}{39}$$

In the above equality, K and 39 are constants expressing the logarithmic characteristics of the diode. C1 is user selectable, determining V_D. V_D is the voltage difference between V_B and V_C resulting from the integration of a constant signal for one time unit.

Let $V_B(t)$ = constant = V_B and $V_o = -\infty$, i.e., 0 in the logarithmic domain, corresponding to resetting the integral at t = 0. We now find $I_C(t)$ as a function of C1, aiding the selection of a value for C1.

From elementary circuit theory

$$I_C(t) = \frac{dV_C(t)}{dt} \cdot C1$$

Combining with equation 4

$$I_C = \frac{e^{39V_B} \cdot C1}{39 \int_0^t e^{39V_B} dt + e^{-\infty}}$$

$I_C = \frac{C1}{39 \cdot t}$	constant signal and integration reset at t = 0

In choosing C1, consider that:

1. Current at maximum time is not too small compared to leakage.
2. Current in some interval less than minimum time is not too large for T1B to supply.
3. $\overline{I_C} \simeq \overline{I_A}$ for best cancellation of secondary temperature nonlinearities. Primary temperature effects are compensated in the amplifier stage, so this is a very non-critical consideration.
4. C1 is small enough for rapid reset.
5. C1 is large enough to avoid stray noise.
6. C1 has extremely low leakage.

0.1 μF polystyrene is specified for the present circuit.

Varients of the circuit provide interesting effects, as is now discussed.

1. "RMS" integration is performed by adding a second log element in series with T1A, and a balancing constant voltage offset in series with T1B. Varying post-amplification gain allows sum of squares, square root of sum of squares, or any other exponential power by varying inter-log gain. A simple transistor bridge allows bipolar RMS measuring. The circuit retains its phenomenal range, far exceeding the present state of the art "square first" type RMS equipment. Subtracting output from a parallel circuit viewing a constant input effectively divides by time for true RMS.
2. A constant current "leaked" from C1 will transform the system from a pole-at-the-origin integrator to a pole-off-the-origin low pass filter. The time constant τ is directly proportional to current. It is easy to control current over many orders of

magnitude, thus providing a voltage controlled low-pass filter whose break frequency can be varied continuously from milliseconds to hours. Variation in DC gain is easily compensated in the logarithmic domain by subtraction of the output of a complementary stage inputting a constant reference. RMS averaging is as compatible with low-pass filtering as with pure integration.

Integral Reset Circuitry

The integral is reset by reducing the voltage across C1. A perfect reset would drop V_C to Log(0) = $-\infty$ volts, which is impractical. As a compromise one can:

1. Instantly reset V_C by clamping to some low initial voltage. This is equivalent to starting the integration with a small initial non-zero bias. Aside from the initial error, initial I_C may be excessive at large signal levels, causing a large error from retarded integration.
2. Drop V_C by a fixed step by charge transfer. This is equivalent to dividing the signal in the integrator by a large constant. This method may produce excess I_C for large signals and insufficient erasures of long integration times.
3. Pull a current from C1 for a fixed time. This temporarily configures a low-pass filter causing the past to be exponentially forgotten. The current drawn must be limited to that which T1B can supply, limiting the decay speed. Because a worst-case previous reset may have occurred seconds ago, it is necessary to wait about 20 time constants to assure erasure.
4. Pull a very large current from C1, larger than I_{MAX} that can be

countered by T1B. As C1 is rapidly discharged, V_C falls, and thus via T1B I_C rises exponentially. When I_C is observed to reach I_{MAX} the process is terminated. This is equivalent to starting the integration with an initial bias of a constant times the signal prevailing at the time the reset is terminated. Choosing I_{MAX} = 25 ma and C1 = 0.1 μF, this constant is 100 nsec, which conveniently is about the time needed for the reset cycle. Because the input signal changes little in 100 nsec, the signal prevailing at t = 100 nsec is a good estimate of the average signal for $0 < t < 100$ nsec. By starting integration at 100 nsec with an initial bias = signal at 100 nsec · 100 nsec, a nearly ideal system is implemented. This method allows extremely rapid and accurate reset without excess I_C under all conditions of signal level and history. It is used on the photosense board.

Referring now to the schematic, on the rising edge of RESET the edge-triggered flip-flop clocks the grounded D onto the Q output. As Q falls, T6 is activated allowing C1 to discharge limited by R13. D3 lowers Q about 2 volts. C4 transfers the high-current pulse. R12 and T6 gain are sufficient so that I_C can be > I_{MAX} even when C4 is discharged, to avoid a trapped state during power-up. R11 must more than balance current through R12 to allow Q to be pulled > 3V when Q is high. As V_C drops, I_C increases exponentially. I_C passing R9 + R10 causes SET voltage to drop. When $I_C = I_{MAX} = \frac{4V}{R9+R10}$ then the flip-flop sets. It may be desirable to select R10 larger than indicated by this equation for "anticipation" at the high speeds involved. As Q goes high, it is pulled farther by R11 but limited by the base-collecter diode in T5. T5 turns on, allowing I_C to surge to $>>I_{MAX}$, limited by R9, for integral tracking.

Amplifier Circuit

FET OP-2 could potentially severely limit bandwidth because of a required gain of over 20 to amplify the small logarithmic signal from T1B to that specified for output. R14, R15, R16, D4, D5, and C5 provide a voltage amplification stage allowing OP-2 to function near its frequency limit. R18 and R19 provide the voltage dividing feedback and also with R17 and thermister R20 provide 3-point temperature compensation of the logarithmic elements.

Photomultiplier Voltage Supply

The use of a zener bridge compared to a conventional resistive bridge provides advantages:

1. Less bridge current is required for lower temperature.
2. Better stabilization of lower dynode stages.
3. Reduced effect from HV ripple, quite critical due to both exponential gain dependance and capacitive effects.
4. HF suppression capacitors can be used. They cannot be used with a resistive bridge when an accurate DC-coupled signal is required.
5. When the HV supply is suddenly grounded in response to BREAK, the zener reverse conduction both protects capacitors from imbalance-generated overvoltage and also prevents reverse biasing of the critical photocathode or any other dynode stage.

The higher cost is minor and the very slow temperature drift can be compensated in software. A separate bridge for each photomultiplier obviates multiple HV cables and reduces noise pickup. The lower capacitors should be large to allow large anode transients. D6 allows rapid discharge when the HV supply is grounded. The combination R1 and R6 insure that, with a slowly recovering HV supply, the photocathode stage will be the last to turn on in case of a remaining overload which must be immediately sensed. For protection, $R6 < \frac{V_{D7}}{T_{A\ MAX\ SUSTAINED}}$ to insure sufficient tripping current into the final dynode stages under all conditions where a signal may be present.

Overload Protection Circuitry

Nearly all of I_A passes $R2 \parallel C3 + R3$, generating a voltage across V_{BE} of T2. R2 and R3 averages the current to a voltage over several seconds. The maximum anode current is specified as "averaged over any interval of 30 seconds." In addition a small resistance R3 provides sensing for very large transients, no matter how short, to which T1A and OP-1 are not protected. When the voltage across R2 + R3 exceeds about half a volt, T2, T3, R4, and R5 provide a digital alarm signaling the Logic Module to ground the High Voltage Supply. An optional galvinometer is shown.

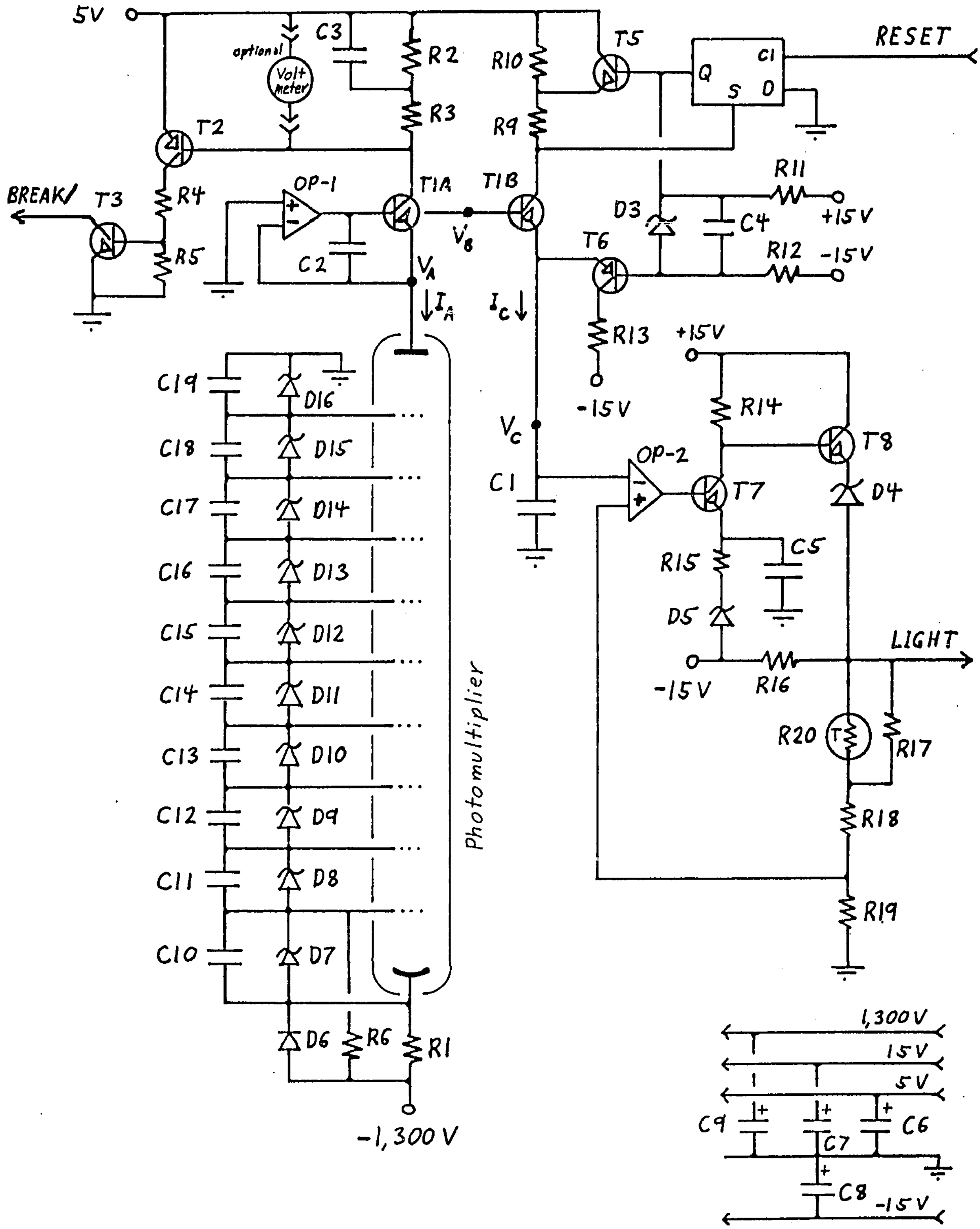


Figure 6.29 Photosense Board (schematic)

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