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Graduate College

DEVELOPMENT OF A THERMOELECTRICALLY-COOLED IV-VI SEMICONDUCTOR DIODE LASER USING EPITAXIAL LIFT-OFF TECHNIQUES

A Dissertation

SUBMITTED TO THE GRADUATE FACULTY

in partial fulfillment of the requirements for the

degree of

Doctor of Philosophy

By

KEVIN RAY LEWELLING
Norman, Oklahoma
1997

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DEVELOPMENT OF A THERMOELECTRICALLY-COOLED IV-VI SEMICONDUCTOR DIODE LASER USING EPITAXIAL LIFT-OFF TECHNIQUES

A Dissertation APPROVED FOR THE SCHOOL OF ELECTRICAL AND COMPUTER ENGINEERING

BY

Patrick J. McCann, Chair

Ryan E. Doezema

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William L. Kuriger

Michael B. Santos

Acknowledgment

During the course of my Ph.D. work I have grown in understanding and patience. For this growth, I owe several people acknowledgment and thanks. The people that have affected me range from schoolmates to friends and family members.

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Abstract

IV-VI semiconductor (lead-salt) lasers are well suited for infrared spectroscopy as the light emission covers the 3 μm to 30 μm spectral range; several molecules have strong absorption bands in this range. The problem hindering widespread use of these lasers is the need for cooling with liquid nitrogen or helium during use. By removing the need for cryogenic cooling, remote sensing applications such as atmospheric spectroscopy and smoke stack pollution monitoring could be further developed. Another application that has received much attention is use in medical testing through non-invasive breath analysis. One test design allows analysis of human breath for the *Helicobacter pylori* bacterium, which has been linked with stomach ulcers.

Thermoelectric cooling (TEC) modules can provide a heat sink temperature of 220 K. If a IV-VI semiconductor laser could operate in continuous wave mode while mounted on a TEC module, an electrically cooled spectrometer could be developed. Using molecular beam epitaxy and modern photolithography techniques, a 1995 PbEuSeTe\PbTe separate confinement buried heterostructure laser operated in continuous wave mode at a heat sink temperature of 223 K. This does not leave a sufficient temperature tuning range

for spectroscopic applications, suggesting new approaches to the problem should be investigated.

A potential solution to the operating temperature problem is to employ epitaxial lift-off techniques in order to transfer the semiconductor device from its thermally resistive substrate to copper, a superior thermal conductor. Finite element thermal models predict this transfer will increase the operating temperature by 63°. The 63° increase will allow a 40° tuning range for high resolution infrared spectroscopy without the need for cryogenic cooling.

This dissertation presents thermal models showing the dramatic increase in operating temperature gained by transferring the laser structure. Also, significant progress towards constructing a copper mounted IV-VI semiconductor laser by means of a new patented fabrication procedure is documented. This dissertation contains scanning electron microscopy micrographs showing cleaved epilayer structures mounted on copper. Supporting data of non-linear current versus voltage scans and x-ray diffraction peaks of lifted-off epilayers without degradation of crystal quality are included.

Chapter 1

Introduction and Background Information

1.0 Introduction

IV-VI semiconductor (also known as lead-salt) lasers possess several attributes which make them useful devices for various applications. (1) They have an emission range from 3 μm to over 30 μm [1,2]; a range that cannot be accessed with III-V semiconductor lasers. (2) Their output emission can be changed by manipulating the alloy composition of the active region [3,4]. (3) The laser output radiation can be tuned by controlling the heat sink temperature for a particular alloy composition [5]. These characteristics make IV-VI semiconductor lasers useful for high resolution infrared spectroscopy applications. One problem that has hindered the widespread acceptance of IV-VI semiconducting lasers is the need for cryogenic cooling during use. Cryogenic cooling prohibits many remote sensing applications and complicates laboratory use. If the need for cryogenic cooling can be removed, many new applications could be developed such as remote air pollution detection, real-time chemical process control, and non-invasive medical diagnostics through breath analysis [6]. This work concerns the development of a new IV-VI semiconductor laser fabrication process that will

remove the need for cryogenic cooling thus enabling these and other potential applications.

Currently, IV-VI semiconductor lasers are grown on PbTe or PbSe substrates which are very poor thermal conductors. After structure growth, the substrate/structure is cleaved along the (100) planes to form resonant cavities needed for lasing. The laser is mounted on an indium plated copper heat sink which also serves as an electrical contact. A second contact is applied to the substrate side of the device. Since the thermally resistive substrate resides between a heat sink and the active region of the device, heat will readily build up as current flows through the structure. It has been shown that in gallium arsenide (III-V semiconductor) lasers, this heat can cause thermal runaway leading to facet damage and ultimately device failure [7].

203 K is the highest continuous wave (cw) heat sink temperature for a IV-VI semiconductor buried-heterostructure laser in which high resolution infrared spectroscopy has been performed on low-pressure CO_2 gas samples [1]. This was achieved by thinning the thermally resistive PbTe substrate to ~250 μm. The device can be damaged by the mechanical removal procedure, thus limiting

the extent of the substrate thinning process. A less damaging chemical removal of the substrate is virtually impossible due to chemical similarities between the substrate and the laser structure.

Considerable work has been done on growing good quality IV-VI semiconductor epilayers on BaF_2 substrates using liquid phase epitaxy (LPE) [8-10]. The thermal expansion coefficients between BaF_2 and IV-VI semiconductor epilayers are approximately matched. This ensures epilayer quality will not be degraded when structures are cooled down from high growth temperatures. It has also been shown that IV-VI semiconductor ternary [8] and quaternary [9] layers can be lattice matched with BaF_2, allowing growth of high quality double heterostructures [16]. Lattice matching reduces non-radiative recombination defect centers at the heterojunction interface which is critical for good laser operation.

BaF_2 is chemically different from IV-VI semiconductors and can be dissolved in water or a water/HCL solution without damaging the semiconductor material; this would allow complete chemical removal of the substrate thus enabling transfer of the laser structure to a more thermally conductive material. Similarly, epitaxially-

lift-off (ELO) and "flip-chip" technologies have been used to remove the growth substrate and transfer the viable structure to a new host substrate, improving certain device operation parameters.

ELO techniques have been used to transfer gallium arsenide (GaAs) devices from growth to host substrate. Yablonowitch et al. [11] have shown that III-V semiconductor laser performance is not degraded after transfer from a gallium arsenide substrate to a glass host; this was demonstrated by the fact that threshold current density remained unchanged after transferring the device to a glass substrate. This ELO technique involves coating the epilayer(s) with black wax and chemically attacking with dilute hydrofluoric acid (HF) an aluminum arsenide (AlAs) release layer that is placed (during growth) between the substrate and the epilayer. The released device structure, which is fixed to a layer of black wax, can then be cleaved and bonded to a new host substrate using epoxies or "Van der Waals forces" to allow hybrid device packaging [11,12].

"Flip-Chip" is another technique that has been developed for transferring a semiconductor device structure to a dissimilar substrate. This technique involves bonding the device structure face down on a host substrate before

removing the original growth substrate. After bonding the sample face down, the substrate is thinned by mechanically polishing to reduce overall thickness; this is followed by a wet chemical etching to remove the remainder of the growth substrate. The device structure is protected from the chemical etchant by a "stop layer" that is placed during epitaxial growth between the substrate and device structure. This technique has been successfully used; a ZnSSe/ZnSe/CdZnSe light-emitting diode has been transferred from a GaAs substrate to a reflector-coated Si substrate [13]. In this effort, it was shown the transfer did not degrade device performance, but improved the external quantum efficiency by a factor of two.

As explained in Ref. [17], a technique that combines elements of both ELO and "Flip-Chip" technologies can be employed to increase the operating temperature of IV-IV semiconductor lasers by at least 50°C [22]. This 50°C increase in operating temperature will enable laser cooling by thermoelectric elements, removing the need for liquid nitrogen.

1.1 IV-VI Semiconductor Background Information

Figure 1.1 depicts the relationship between lattice constants and bandgaps of various IV-VI semiconductor materials and BaF_2. It shows how lattice constants and bandgaps can be varied by changing the composition of the IV-VI semiconductor material; tellurium (Te) concentration primarily affects lattice parameter while tin (Sn) or europium (Eu) concentration primarily affects the bandgap. Lattice matching conditions were confirmed by X-ray diffraction studies [8,9] while bandgaps were determined by infrared absorption and photoluminescence studies [14]. This basic research has provided the information needed to develop and fabricate lattice-matched IV-VI semiconductor laser structures on BaF_2 substrates [16].

Photoluminescence (PL) tests have shown that LPE-grown epilayers are quite suitable for laser fabrication; strong PL peaks at 100 meV (12.4 μm) and at 175 meV (7.1 μm) are observed when temperatures are held under 10 K for ternary and 5% Sn quaternary layers, respectively [14]. Figure 1.2 summarizes PL energies and absorption edge energies, as determined by Fourier transform infrared spectroscopy (FTIR) studies, for these two materials. Note the temperature dependence of the absorption edges for these two materials. These data can be used to design and

fabricate a temperature-tunable double heterostructure (DH) laser covering the 6 to 9 μm spectral range.

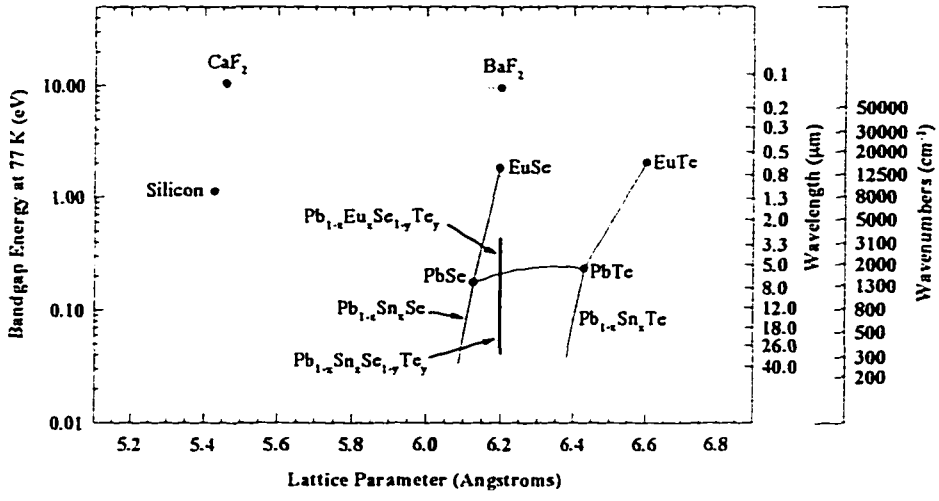


Figure 1.1 IV-VI semiconductor lattice parameters and bandgap energies.

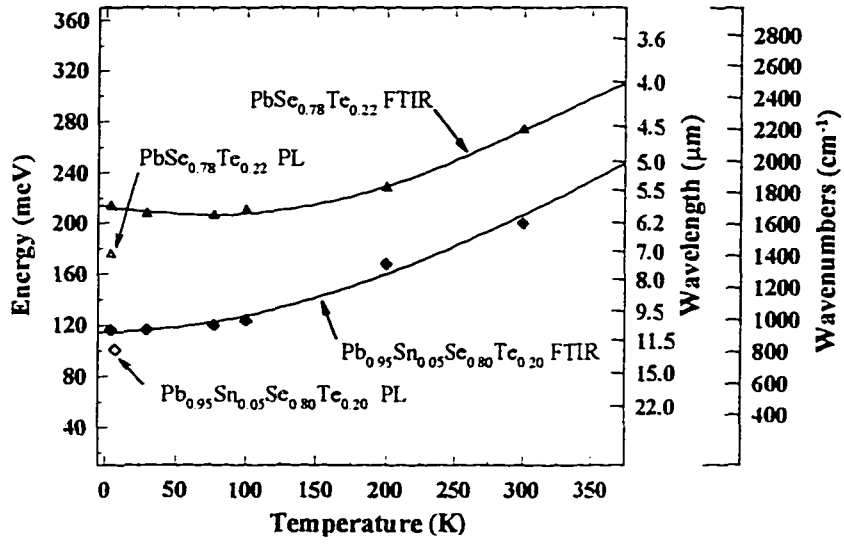


Figure 1.2 Photoluminescent\FTIR absorption edges of ternary and quaternary IV-VI epilayers grown on BaF_2 [14].

1.2 Characteristics of $PbSe_{0.78}Te_{0.22}$ [8]

Growing lattice matched ternary epilayers by LPE demands knowledge of the relevant portion of the Pb-Se-Te liquid-solid phase diagram. For example, it has been experimentally determined the Te concentration in the melt must be 60% in order to incorporate 22% into the epilayer. Figure 1.3 shows that a 22% Te concentration in the solid is needed to obtain lattice-matching conditions to (100) BaF_2.

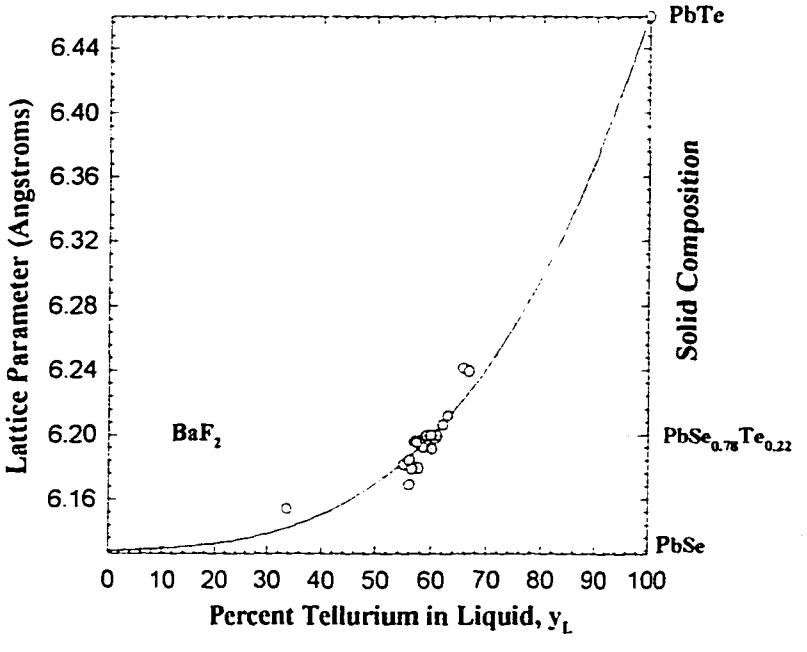


Figure 1.3 Measured lattice parameters, as determined by x-ray diffraction, for ternary $Pb(Se_{1-y}Te_y)$ epilayers grown by LPE [8]. Note that 60% Te in the liquid yields epilayers that are lattice matched with (100) BaF_2 [8].

The requirement for high Te melt concentration is attributed to the larger atomic size of Te relative to the space in the host crystal [21]. Also, the epilayer growth is limited by the diffusion of Se and Te through the lead-rich melt; therefore, the growth rate is non-linear with respect to time. Typical layer thicknesses of 3 μm are obtained for a 10 minute growth period.

Varying the pseudo-binary, $Pb_{1-z}(Se_{1-y}Te_y)_z$, composition parameter z allows control of the liquidus temperature. Figure 1.4 is a graph showing the relationship between z and the liquidus temperature for $Pb_{1-z}(Se_{0.40}Te_{0.60})_z$.

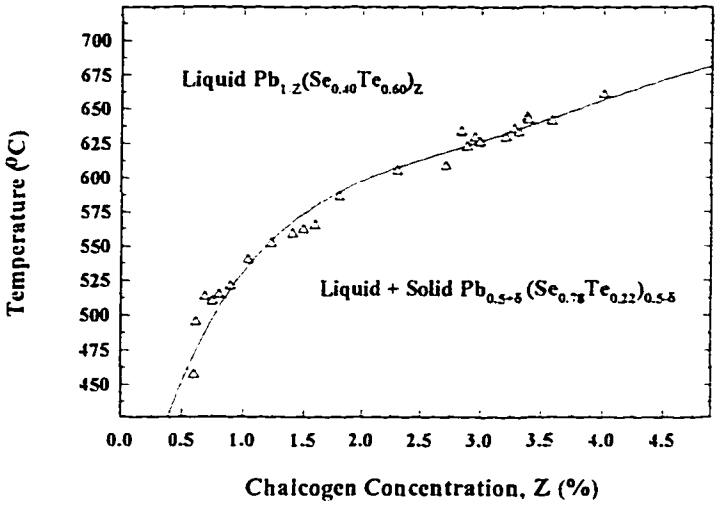


Figure 1.4 Measured liquidus temperatures for $Pb_{1-z}(Se_{0.40}Te_{0.60})_z$ solutions for different z concentrations [20].

Figure 1.4 illustrates that as z increases, the liquidus temperature also increases; the documented range is from 450-650°C for z between 0.5-3.0%, respectively [8]. The critical temperature for good epilayer growth on bare BaF_2 is greater than 610°C , but less than 660°C which corresponds to $3.5 \leq z \geq 2.5\%$. Studies of PbSe growth on BaF_2 have shown that in this temperature range a continuous barium-selenide (BaSe) layer forms on the surface of the bare BaF_2 substrate due to selenium vapor exposure from the lead-rich melt [18]. It is believed the thin (~one monolayer) chalcogenide reaction layer reduces deposit/substrate interface energy or increases substrate surface energy [18,19] which promotes two-dimensional layer growth. A barium-chalcogenide reaction layer formation is believed to be promoted by use of a properly designed graphite boat; this boat in essence traps the growth solution vapor over the BaF_2 substrate prior to growth which promotes the reaction layer formation needed for good epitaxy [20].

It has been determined by Hall effect measurements that ternary epilayers are n-type with electron concentrations of approximately $4X10^{18}$ cm^{-3}[10]. The n-type behavior is attributed to Se and Te vacancies which act as donors [8,15]. Much work has been done in finding a

suitable p-type dopant for this ternary crystal. To date, thallium (Tl) has proven to be the most suitable acceptor impurity yielding hole concentrations as high as $2.2X10^{18}$ cm^{-3} [10]. Figure 1.5 shows a plot of carrier concentration and material type against Tl melt concentration.

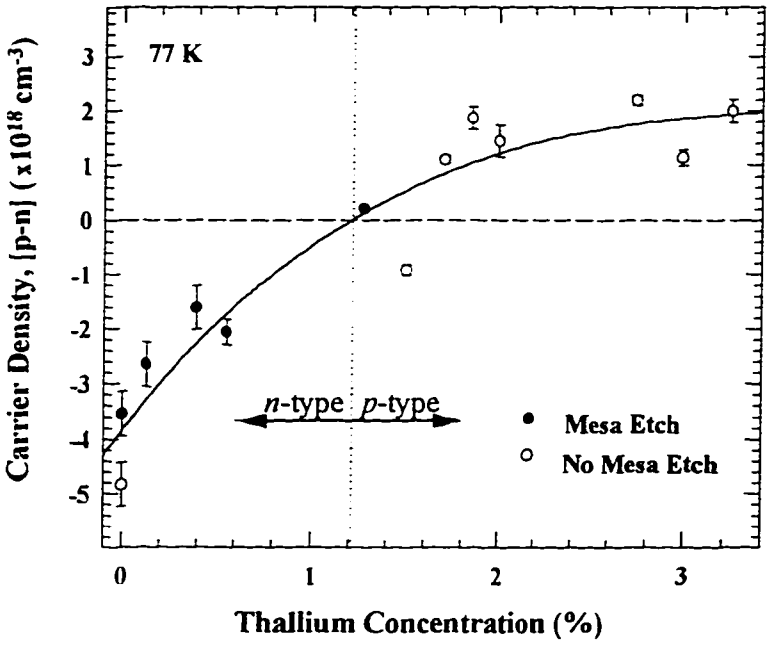


Figure 1.5 Measured carrier concentrations of $PbSe_{0.78}Te_{0.22}$ epilayers on BaF_2 as a function of Tl concentration in the growth solution [10].

With melt concentrations of 1.2 atomic percent and greater, Tl converts the native n-type ternary epilayer to a p-type material. The Tl impurities are believed to occupy group

IV lattice sites and introduce local impurity states approximately 200 meV below the valence band edge.

1.3 Characteristics of $Pb_{1-x}Sn_xSe_{1-y}Te_y$ [9]

LPE growth of lattice-matched $Pb_{1-x}Sn_xSe_{1-y}Te_y$ epilayers demands knowledge of the relevant portion of the Pb-Sn-Se-Te liquid-solid phase diagram. Lattice-matching of $Pb_{1-x}Sn_xSe_{1-y}Te_y$ to BaF_2 was experimentally determined by X-ray diffraction studies. Although Figure 1.1 suggests increasing the Sn content will require higher Te melt concentrations to maintain a constant lattice parameter, experimental results actually show the opposite. Experimental results show that as Sn is added to the IV-VI melt, Te incorporated into the solid is increased slightly. Therefore, the amount of Te added to the melt must be decreased when using Sn. This is due to decreasing chemical potential for Te in the quaternary solid as Sn occupies the Pb sites in the IV-VI lattice. Sn, a smaller atom, takes less room in the lattice than Pb and allows better incorporation of Te into the IV-VI epilayer.

The Sn (Tin) concentration can also be varied to control the bandgap of the quaternary epilayer. The bandgap is theoretically predicted to vary from 185 to -63.5 meV corresponding to X_s=0% to 60%, respectively; as

the Sn concentration increases, the bandgap shrinks and inverts. However, FTIR absorption edge measurements show the bandgap does not decrease below 80 meV with additional Sn [16]. Nevertheless, compositional control of the bandgap provides sufficient flexibility in designing lasers that can cover the 6 μm to 20 μm spectral range. An additional advantage of using $Pb_{1-x}Sn_xSe_{1-y}Te_y$ lattice-matched quaternary alloy is that the liquidus temperature is varied as the chalcogen content z is changed, permitting epilayer growth over a range of temperatures. This degree of freedom allows quaternary epilayer growth on bare BaF_2 at high temperatures (~620°C) and other lattice-matched IV-VI semiconductor layers at lower temperatures (~450°C) without concerns of interfacial interdiffusion.

1.4 Focus and Dissertation Outline

Using the collected LPE growth data discussed above, it is possible to grow high quality DH laser structures on BaF_2 substrates [16]. The focus of this work is to develop a new laser fabrication procedure thus building upon the experimental results covered in this chapter. Device structure growth is combined with a new, patented [17] bonding/cleaving technique to produce a temperature tunable IV-VI semiconductor laser that is predicted to operate at

least 50°C higher than presently available IV-VI semiconductor lasers. This dissertation describes in detail a new laser fabrication technique; both theory and experiment predict significant improvements in IV-VI semiconductor laser performance are possible.

Chapter One has served as an introduction to IV-VI semiconductors and the limitations of presently available lead-salt laser devices. Chapter Two will briefly describe liquid phase epitaxy, concentrating on growth of IV-VI laser structures. Chapter Three presents the results of finite element thermal models that compare commercially available IV-VI semiconductor lasers to those that will be fabricated using the new procedure. Chapter Four discusses a critical processing step in the new laser fabrication procedure, the formation of a metallic bonding medium between the IV-VI semiconductor epilayer and a copper heat sink. Chapter Five chronicles the overall progress made in developing this new laser fabrication procedure. Techniques for BaF_2 substrate removal, epilayer cleaving, and device packaging are shown. Chapter Six discusses preliminary electrical and x-ray diffraction characterization results for IV-VI semiconductor structures processed using the new techniques. Chapter Seven

summarizes this work and suggests possible directions for future research.

References

[1] Z.Feit, D.Kostyk, R.J.Woods, and P.Mak, "Single-Mode Molecular Beam Epitaxy Grown PbEuSeTe/PbTe Buried Heterostructure Diode Lasers for CO_2 High-Resolution Spectroscopy". *Appl.Phys.Lett.* **58**, 343 (1991).

[2] P.J.McCann and L.Li, "$Pb_{1-x}Sn_xSe_{1-y}Te_y$ Alloys Lattice Matched with BaF_2: A New Material System for Far-Infrared Device Fabrication", International Device Research Symposium, Charlottesville, VA. December 1-3, 1993.

[3] P.J. McCann, J. Fuchs, Z.Feit, and C.G.Fonstad, "Phase Equilibria and Liquid Phase Epitaxy Growth of PbSnSeTe Lattice Matched to PbSe", *J.Appl.Phys.* **62**, 2994 (1987).

[4] W.W.Anderson, "Gain-Frequency-Current Relations for PbSnTe Double- Heterostructures", *IEEE J. Quantum Electron* **QE-13**, 532 (1977).

[5] Y.Nishijima and K.Shinohara, "Single-Mode PbSeTe laser with a Buried Heterostructure", *Applied Optics.* **32**, 4485 (1993).

[6] P.S. Lee, R.M. Schreck, F.A. Hare, and J.J. McGrath, "Biomedical Applications of Tunable Diode Laser Spectrometry", *Annals of Biomed. Eng.* **22**, 120 (1994).

[7] R.Schatz and C.G.Betha, "Steady State Model for Facet Heating Leading to Thermal Runaway in Semiconductor Lasers", *J.Appl.Phys.* **76**, 2509 (1994).

[8] P.J.McCann and C.G.Fonstad, "Growth of $PbSe_{0.78}Te_{0.22}$ Lattice-Matched with BaF_2", *Thin Solid Films* **227**, 185 (1993).

[9] P.J.McCann and D.Zhong, "Liquid Phase Growth of $Pb_{1-x}Sn_xSe_{1-y}Te_y$ Alloys Lattice Matched with BaF_2", *J.Appl.Phys.* **75**, 1145 (1994).

[10] P.J.McCann, S.K.Aanegola, J.E.Furneaux, "Growth and Characterization of Thallium- and Gold-Doped $PbSe_{0.78}Te_{0.22}$ Layers Lattice Matched with BaF_2 Substrates", *Appl.Phys.Lett.* **65**, 2185 (1994).

[11] E.Yablonovitch, K. Kapon, T.J.Gmitter, C.P. Yun, and R.Bhat, "Double Heterostructure GaAs/AlGaAs Thin Film

Diode Lasers on Glass Substrates", *IEEE Photon. Tech. Lett.* **1**, 41 (1989).

[12] E.Yablonovitch, T.J. Gmitter, J.P. Harbison, and R. Bhat, "Extreme Selectivity in the Lift-Off of Epitaxial GaAs Films", *Appl.Phys.Lett.* **51**, 2222 (1987).

[13] X.Li, I.W. Tao, and W.I. Wang, "Flip-Chip Transfer of ZnSSe/ZnSe/CdZnSe LED Films", *Electronics Letts.* **31**, 491 (1995).

[14] P.J. McCann, L.Li, J.E.Furneax, and R. Wright, "Optical Properties of Ternary and Quaternary IV-VI Semiconductor Layers on (100) BaF_2 Substrates", *Appl.Phys.Lett.* **66**, 1355 (1995).

[15] G.Pratt.Jr., "Vacancy and Interstitial States in the Lead Salts", *J. Nonmetals* **1**, 103 (1973).

[16] I. Chao, S. Yuan, and P.J. McCann, "Growth and Characterization of PbSeTe/PbSnSeTe/PbSeTe Double Heterostructures", International Device Research Symposium, Charlottesville, VA., December 6-8, 1995. Published in Proceedings 1995 International

Semiconductor Device Research Symposium, Volume II, P.505, University of Virginia, Charlottesville, VA (1995).

[17] P.J. McCann "High Temperature Semiconductor Diode Laser", US Patent # 5,454,002, Issued Sept. 26, 1995.

[18] P.J. McCann, C.G. Fonstad, "Auger Electron Spectroscopic Analysis of Barium Fluoride Surfaces Exposed to Selenium Vapor", *J. Electron. Mater.* **20**, (1991) 915.

[19] P.J. McCann, "The Role of Substrate Surface Reactions in Heteroepitaxy of PbSe on BaF_2", *Mater. Res. Soc. Symp. Proc.* **221**, 289 (1991).

[20] P.J. McCann, S.K. Aanegola, "The Role of Graphite Boat Design in Liquid Phase Epitaxial Growth of $PbSe_{0.78}Te_{0.22}$ on BaF_2", *J. Crystal Growth* **141**, 376 (1994).

[21] P.J. McCann, "The Effect of Composition Dependent Lattice Strain on the Chemical Potential of Tellurium in $Pb_{1-x}Sn_xSe_{1-y}Te_y$ Quaternary Alloys", *Mat. Res. Soc Symp. Proc.* **311**, 149 (1993).

[22] P.J. McCann and K.R. Lewelling, "Prospects of High Operating Temperature IV-VI Semiconductor Tunable Diode Lasers", *Optical Remote Sensing for Environmental and Process Monitoring Sym. Proc.* **VIP-55**, 26 (1995).

Chapter 2

IV-VI Device Structure Growth Using Liquid Phase Epitaxy and Discussion

Liquid Phase Epitaxy (LPE) is a low cost method of growing high quality semiconductor materials. It is based on fundamental principles of thermodynamics in which thin crystalline layers are grown from saturated liquid solutions on a prepared substrate [23]. The IV-VI semiconductor crystal growth procedure begins with weighing out appropriate amounts of the constituent materials (Pb, Sn, PbSe, and PbTe) which comprise the saturated solution. In this process, the substrate acts as a template on which oriented crystal layers are grown. The term epitaxy is used to describe this process which means "to arrange upon". The substrate is placed on a slider and the weighed materials are placed in the well(s) of a graphite LPE boat assembly, see Figure 2.1 [20]. If more than one epitaxial layer is to be grown, successive wells must be loaded with their respective growth solution materials.

After loading the substrate and growth solution materials, the LPE boat is placed in a furnace, which is pumped with a cryogenic sorption pump to a pressure of approximately one mtorr. After pumping, the sealed furnace is back-filled with flowing purified hydrogen to create a

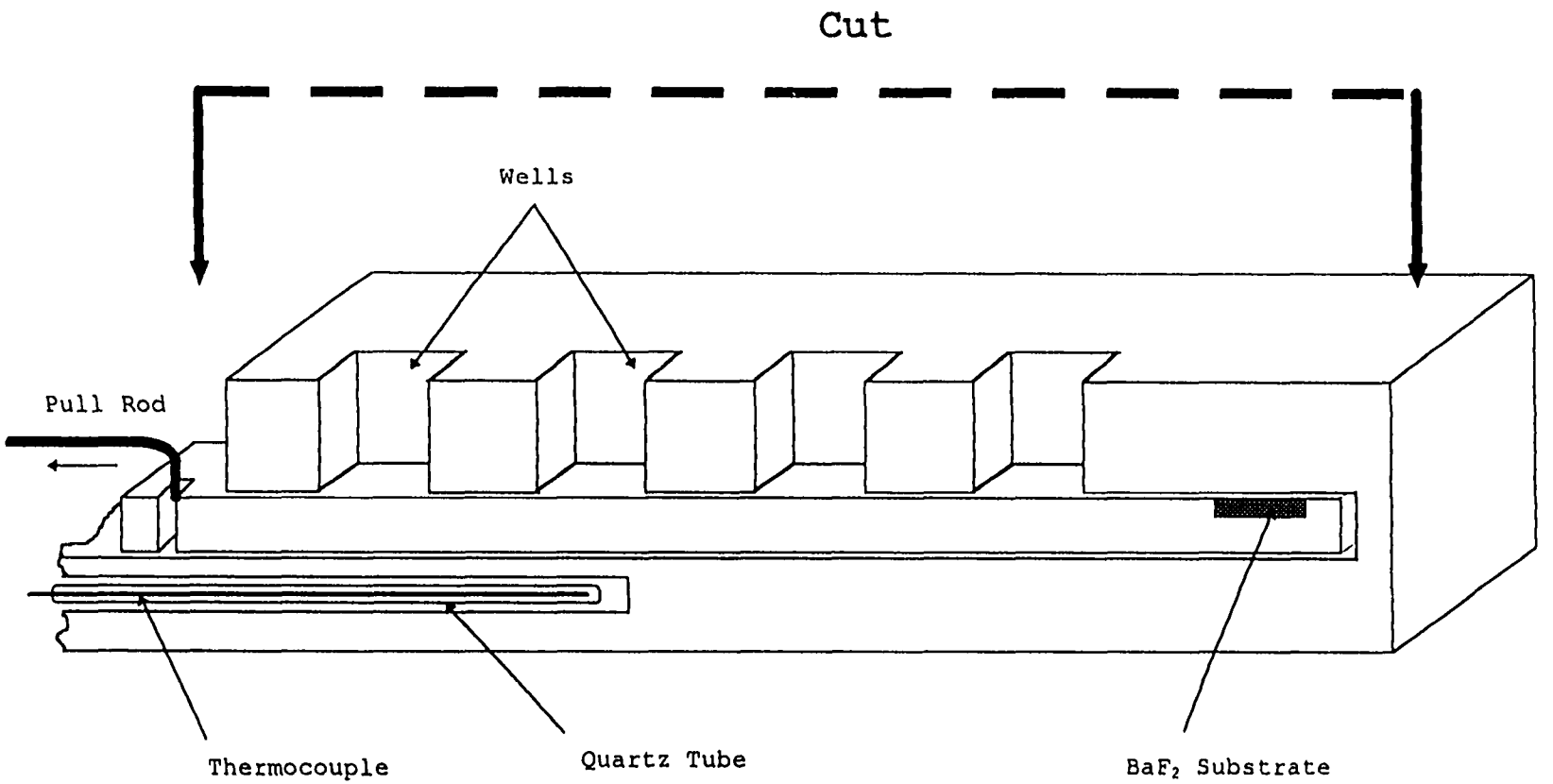


Figure 2.1 Cross-sectional cut-a-way view of a graphite boat used for liquid phase epitaxy growth of IV-VI semiconductor layers on BaF_2 substrates.

reducing atmosphere, minimizing oxidation of the materials involved. The furnace is heated to melt the lead and tin, which then dissolves the PbSe and PbTe pieces.

After the pieces of PbSe and PbTe are thoroughly dissolved, the furnace temperature is cooled at two degrees per minute to determine the nucleation temperature, T_n; T_n is the temperature at which solid crystallites form on the surface of the growth solution. The furnace temperature is then elevated to re-dissolve the solidified crystallites. After dissolving the crystallites, the furnace is cooled at two degrees per minute, and at approximately one degree above T_n the slider is pulled placing the substrate underneath the growth solution. This initiates crystal formation on the substrate surface. Crystal growth is terminated by pulling the slider which removes the substrate from underneath the growth solution. Multiple epitaxial layers can be grown by positioning the substrate underneath adjacent growth solutions in the graphite boat. LPE can thus be used to grow multi-layered device structures by successive growth steps. This brief overview explains the growth method used at the University of Oklahoma in fabricating IV-VI laser structures using LPE [16].

The ability to manipulate T_n by controlling the chalcogen (Se and Te) content in the growth solution is important when growing successive epitaxial layers. A low T_n is desired for growth of multiple layers because it reduces interdiffusion thus producing more abrupt hetero-junction interfaces needed for efficient optoelectronic device operation [5]. Table 2.1 lists the LPE growths performed by the author during the course of this research. Note how manipulating the z parameter affects the nucleation temperature of the growth solution.

A IV-VI DH laser structure can be fabricated by first growing an undoped n-type $PbSe_{0.78}Te_{0.22}$ layer on a bare BaF_2 substrate at ~620°C. This temperature is needed to form the barium-chalcogenide reaction layer discussed in the previous chapter [8]. This is followed by growth of an undoped quaternary layer with a nucleation temperature approximately 100°C lower, ~520°C. Finally, a thallium-doped p-type ternary layer is grown at an even lower nucleation temperature, ~460°C; this terminates the epitaxial growth sequence. Table 2.1 includes three laser structures grown by the author (KRL#8, 9, 10) using this method. Figure 2.2 shows a sketch of a IV-VI DH laser structure grown on a BaF_2 substrate.

Table 2.1

LPE Growth of $Pb_{1-z}(Se_{1-y}Te_y)_z$ and $(Pb_{1-x}Sn_x)_{1-z}(Se_{1-y}Te_y)_z$ Layers

Sample	Structure layer#1 layer#2 layer#3	Growth Parameters(%) x	y	z	T_n (°C)	Quality	Comments
KRL#1	ternary quaternary	0.00 5.03	60.00 60.00	3.19 1.00	616 513	no epitaxy	did not use
KRL#2	ternary quaternary	0.00 4.99	59.99 60.01	3.20 1.00	623 480	no epitaxy	did not use
KRL#3	ternary quaternary	0.00 5.00	60.00 59.97	3.20 1.00	626 516	poor growth	did not use
KRL#4	ternary quaternary	0.00 4.99	60.02 59.93	3.20 1.00	626 519	poor growth	did not use
KRL#5	ternary quaternary	0.00 4.99	60.02 60.04	3.20 1.00	627 517	good growth	bonded
KRL#6	ternary quaternary	0.00 5.00	60.01 60.02	3.20 1.00	626 518	good growth	bonded
KRL#7	ternary quaternary	0.00 4.97	60.00 60.49	3.20 1.01	627 518	good growth	bonded
KRL#8	ternary quaternary *p-ternary	0.00 5.01 0.00	60.02 60.04 59.99	3.20 1.00 0.40	625 515 450	good growth	bonded
KRL#9	ternary quaternary *p-ternary	0.00 5.01 0.00	60.02 60.06 60.61	3.20 1.00 0.50	625 517 465	good growth	bonded
KRL#10	ternary quaternary *p-ternary	0.00 5.01 0.00	59.97 59.84 59.76	3.20 1.00 0.50	624 516 466	good growth	bonded
KRL#11	quaternary ternary	5.00 0.00	59.98 60.10	3.10 1.00	616 522	no epitaxy	bonded
KRL#12	quaternary ternary	5.00 0.00	59.99 59.96	3.10 1.00	616 523	poor growth	bonded
KRL#13	did not load					did not grow	
KRL#14	ternary	0.00	59.93	3.19	627	poor growth	bonded
KRL#15	ternary	0.00	64.45	3.57	628	good growth	cleaved
KRL#16	ternary	0.00	59.99	3.20	627	good growth	did not use
KRL#17	ternary	0.00	60.18	8.51	no T_n		did not use
KRL#18	ternary	0.00	60.05	3.20	627	poor growth	did not use

Sample	Structure layer#1 layer#2 layer#3	Growth Parameters(%) x	y	z	T_n (°C)	Quality	Comments
KRL#19	ternary	0.00	60.05	3.20	624	excellent growth	cleaved
KRL#20	ternary	0.00	60.04	3.23	626	fair growth	bonded
KRL#21	ternary	0.00	60.03	3.20	625	unknown	bonded
KRL#22	ternary	0.00	60.04	3.20	627	good growth	bonded
KRL#23	*p-ternary ternary	0.00 0.00	62.56 32.31	3.51 0.42	620 458	poor growth	bonded
KRL#24	*p-ternary ternary	0.00 0.00	60.05 64.77	3.30 0.47	620 462	good growth	bonded
KRL#25	*p-ternary ternary	0.00 0.00	60.00 60.14	3.40 0.30	622 438	unknown	bonded
KRL#26	*p-ternary ternary	0.00 0.00	59.99 64.39	3.40 0.46	622 456	poor growth	bonded
KRL#27	*p-ternary ternary	0.00 0.00	60.05 65.16	3.40 0.62	622 477	poor growth	did not use
KRL#28	*p-ternary ternary	0.00 0.00	60.00 64.20	3.40 0.77	620 491	good growth	bonded
N012996	ternary quaternary	0.00	60.04 60.08	3.20 1.00	625 515	poor growth	did not use
N020996	ternary	0.00	60.08	3.19	624	poor growth	did not use
N021996	ternary	0.00	60.02	3.20	626	poor growth	did not use
N022896	quaternary ternary	5.01 0.00	60.00 60.10	3.20 1.00	619 521	fair growth	bonded
N030396	ternary ternary	0.00 0.00	60.02 60.08	3.45 1.00	625 522	fair growth	did not use
N030696	ternary	0.00	60.01	3.20	623	excellent growth	did not use
N032296	ternary	0.00	60.01	3.20	625	no growth	substrate misaligned
N032596	ternary	0.00	59.97	3.20	626	good growth	bonded
N032796	ternary	0.00	60.04	3.20	623	poor growth	did not use
N032896	ternary	0.00	59.98	3.20	626	unknown	bonded
N040196	ternary	0.00	60.00	3.20	627	good growth	bonded
N040596	ternary	0.00	60.02	3.20	625	good growth	bonded
N041296	ternary	0.00	59.99	3.20	625	good growth	bonded
N050196	*p-ternary ternary	0.00 0.00	60.02 46.34	3.30 0.22	620 436	good growth	bonded
N052196	*p-ternary ternary	0.00 0.00	59.96 60.38	3.40 0.30	623 434	poor growth	did not use

Sample	Structure layer#1 layer#2 layer#3	Growth Parameters (%) x	 y	 z	T_n (°C)	Quality	Comments
N052296	*p-ternary ternary	0.00 0.00	59.98 45.45	3.40 0.22	623 432	poor growth	did not use
N052496	*p-ternary ternary	0.00 0.00	59.99 59.50	3.40 0.30	616 559	poor growth	did not use
N052996	*p-ternary ternary	0.00 0.00	59.98 60.54	3.40 0.30	623 438	good growth	bonded
N060496	*p-ternary ternary	0.00 0.00	60.01 60.01	3.40 0.30	623 434	poor growth	vacuum problem
N061396	*p-ternary ternary	0.00 0.00	59.99 60.20	3.40 0.30	623 437	poor growth	did not use
N061896	*p-ternary ternary	0.00 0.00	59.76 60.25	3.38 0.30	623 439	poor growth	did not use
N062696	ternary	0.00	60.04	3.2	618	good growth	bonded
N071096	ternary	0.00	59.81	3.31	628	good growth	did not use
N071296	ternary	0.00	60.03	3.30	615	good growth	did not use
N071696	ternary	0.00	59.97	3.30	612	good growth	did not use
N082796	*p-ternary ternary	0.00 0.00	60.02 60.06	3.40 0.29	621 435	good growth	bonded
N090396	*p-ternary ternary	0.00 0.00	60.01 59.56	3.32 0.30	621 428	good growth	
N091196	*p-ternary	0.00	59.97	3.40	613	poor growth	did not use
N091996	*p-ternary	0.00	60.03	3.50	622	good growth	photolitho -graphy
N100290	*p-ternary ternary	0.00 0.00	59.97 60.37	3.50 0.30	623 428	not grown	did not use
N100796	*p-ternary ternary	0.00 0.00	60.01 60.31	3.50 0.30	623 418	good growth	I-V tests
N110896	*p-ternary ternary	0.00 0.00	60.00 59.65	3.50 0.30	623 434	good growth	I-V tests
N112196	*p-ternary ternary	0.00 0.00	60.01 59.88	3.50 0.30	620 402	excellent growth	I-V tests

*All p-ternary layers contain approximately 3% Thallium concentration by weight. Samples listed in this table stating with a capitol N were grown by Nisha Victor.

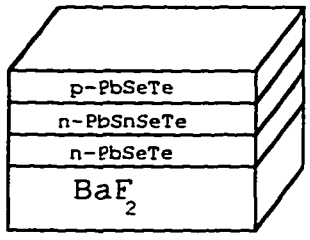


Figure 2.2 A Double Heterostructure grown on BaF_2.

Holloway et al. [26] have produced an injection IV-VI semiconductor laser on BaF_2 by evaporating Pb and Pt strips across an epitaxially grown PbTe layer. Using this arrangement, light was produced underneath the Pb strip; therefore, emitted radiation was obstructed by the Pb contact. This obstruction was remedied by evaporating the Pb at a small angle to the epilayer surface, leaving one laser facet unobstructed. BaF_2 is an insulating material, Eg ~10 eV; this is the reason both electrical contacts were made on the surface of the PbTe epilayer in the Holloway et al. experiment. The device arrangement shown in Figure 2.2 would also require a poor electrical contact to the active device through a highly resistive BaF_2 substrate. This would make practical laser operation impossible. Also, efficient laser cooling is compromised because of the thermally resistive BaF_2 substrate residing between a heat sink and the device structure; thermal conductivity of BaF_2

is 0.117 watt/cm-K, 34 times smaller than copper. An additional complicating factor is that BaF_2 preferentially cleaves along the (111) planes of the crystal while IV-VI semiconductors preferentially cleave along the (100) crystal planes; therefore, cleaving a Fabry-Perot resonant cavity with this stacked material system is impossible using standard techniques. These reasons give motivation for removing the electrically/thermally resistive BaF_2 substrate and transferring the IV-VI semiconductor laser structure to a new host.

Figure 2.3 depicts a proposed equilibrium DH laser band diagram for the device shown in Figure 2.2. Group VI vacancy defect levels in the conduction band cause the native ternary layer to be n-type. Accordingly, thallium impurities occupy group IV sites which introduces quasilocal states 200 meV below the top of the valence band, explaining the p-type behavior of this material.

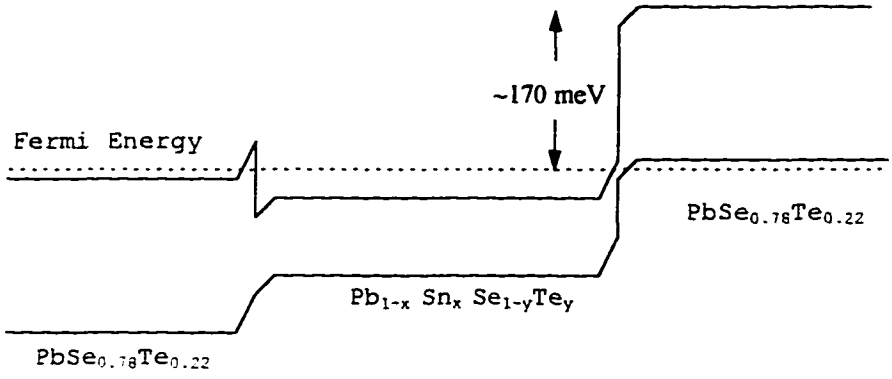


Figure 2.3 Equilibrium energy band diagram for the triple-layer structures grown by LPE. Group VI vacancy defect levels in the conduction band and thallium defect levels in the valence band are believed to cause both n-type and p-type layers, respectively, to be degenerate [16].

Wavelength emission from the VI-VI semiconductor laser shown in Figure 2.2 can be controlled by manipulating the quaternary alloy Sn concentration in the active region. Increasing the Sn concentration shrinks the quaternary bandgap, thus shifting the output emission to longer wavelengths. Varying the Sn concentration allows fabrication of IV-VI semiconductor lasers covering the 6 μm to 20 μm range.

The n-type quaternary layer has a larger index of refraction and smaller bandgap than the ternary layers [24,14]. Sandwiching a quaternary layer between native n-type and thallium-doped p-type ternary layers [25,16] enables optical and electron/hole confinement during device operation. This confinement reduces the threshold current density, thus greatly increasing the internal quantum efficiency of the emitter.

If the proposed IV-VI DH laser is placed under forward bias, the barriers at the p-n junction will be reduced; the equilibrium p-n junction conduction band barrier height is calculated to be approximately 170 meV for 5% Sn in the quanternary layer from 4 K values plotted in Figure 1.2. Forward bias will increase the injected hole concentration on the quaternary-side of the p-n junction. As shown in Figure 2.3, there is a large equilibrium electron population in the conduction band of the quaternary semiconductor. The forward bias will further increase the quaternary conduction band electron population. The conduction band barrier will help confine electrons injected from the n-side, thus increasing the likelihood of electron availability for recombination. Due to a large electron concentration near the p-n junction, holes

injected from the p-side should radiatively recombine with these electrons in close proximity to the p-n junction.

Bonding, cleaving, applying electrical contacts, and packaging completes the fabrication process which renders a useful device. The remaining chapters of this dissertation explain how electrical contacts are applied and describe a new method of device structure cleavage to form Fabry-Perot resonant cavities needed for laser operation.

References

[20] P.J. McCann and S.K. Aanegola, "The Role of Graphite Boat Design in Liquid Phase Epitaxial Growth of $PbSe_{0.78}Te_{0.22}$ on BaF_2", *J. Crystal Growth* **141**, 376 (1994).

[23] B.G.Streetman Solid State Electronic Devices Printice-Hall, Inc., Englewood Cliffs, New Jersey 07632, 1990.

[24] G.Bauer and H.Krenn Handbook of Optical Constants of Solids, Academic Press, Inc., pp. 517-523, 535-546, 1985.

[25] M.Oron, A.Zussman, and A.Katzir, "Dielectric Constants and Optical Confinement in Homostructure PbSnTe Diode Lasers", *Infrared Phys.* **22**, 317, (1982).

[26] H. Holloway, W.H. Weber, E.M. Logothethis, A.J. Varga, and K.F. Yeung, "Injection Luminescence and Laser Action in Epitaxial PbTe Diodes", *Appl. Phys. Lett.* **21**, 5 (1972).

Chapter 3

Thermal Aspects of Diode Lasers

3.0 Introduction

Computer simulation is an effective way of analyzing possible improvements in thermal properties of semiconductor diode lasers. Dimensions and injection current values for IV-VI semiconductor diode lasers are available from previously published work. Figure 3.0 shows a sketch of a double heterostructure (DH) laser fabricated by Feit et al. [36]. This laser structure will be used in the finite element thermal models found in this chapter.

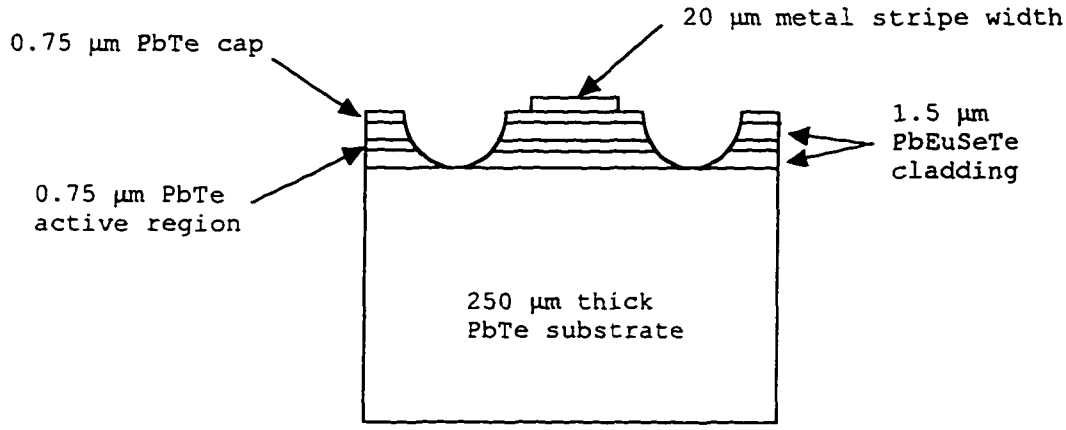


Figure 3.0 IV-VI double heterostructure laser constructed by Feit et al. This laser is able to operate with a heat sink temperature of 175 K. The threshold current density at 175 K is 6 KA/cm^2 [36].

During III-V laser operation, the active region can be several hundred degrees hotter than the substrate (discussed in section 3.2). The active region is on the order of 1 μm thick, making experimental temperature measurements along the facet difficult. One technique that has been successfully used to measure localized temperatures in III- V semiconductor lasers is Raman spectroscopy. Raman microprobe spectroscopy has been used to measure facet and stripe temperatures of gallium arsenide devices. Results from Raman microprobe studies on III-V devices will be used to understand and explain the IV-VI semiconductor laser finite element thermal modeling results found in this chapter.

3.1 Raman Spectroscopy

Raman spectroscopy has been employed in molecular and crystal research, enabling the researcher to investigate certain molecular rotations/vibrations and crystal phonons. The Raman setup consists of a source laser (for example, an Argon laser), a monochromator, and a detector. Raman spectroscopy involves irradiating the sample using the source laser. The sample scatters the source radiation resulting in light consisting of two signals, one that is higher in energy and one that is lower in energy. The two

Raman signals are referred to as the Stokes and Anti-Stokes. The Stokes signal corresponds to the scattered photons in which the sample has absorbed quantized energy from the source while the Anti-Stokes corresponds to the sample giving quantized energy to the scattered photons. The intensity of the Raman signals is dependent on temperature. The equation below shows the temperature dependence of the ratio of Anti-Stokes to Stokes intensities [27]

$$\exp\left(-hcv/kT\right) = \frac{I_{AS}(v)(\mu+v)^4}{I_S(v)(\mu-v)^4}$$

where I_S and I_{AS} are the Stokes and Anti-Stokes signal intensities, respectively. The excitation source frequency (μ) and Raman shift (v) are given in cm^{-1}; T is the temperature in Kelvin. The Anti-Stokes/Stokes intensity ratio increases exponentially with temperature and has been used to measure surface temperature of crystals with a spot size of approximately 1 μm in diameter [28]. The measurement of localized temperatures using Raman microprobe spectroscopy has been employed in III-V semiconductor laser facets and contact stripe temperature profiling, which will be covered in the following section.

3.2 Temperature Measurements Made on Semiconductor Lasers

Both channeled substrate planar and single-quantum-well AlGaAs semiconductor lasers have been studied for operational heat and have been thermally profiled using Raman microprobe spectroscopy [29-31]. The sketches below show the two device geometries.

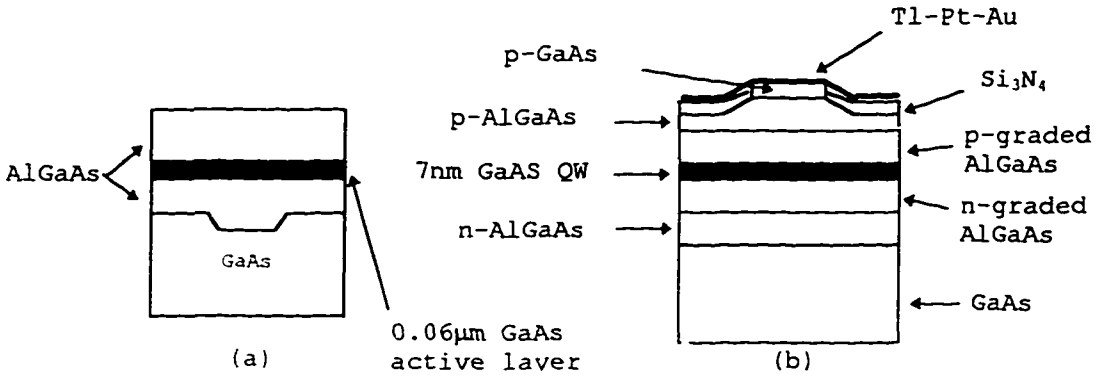


Figure 3.1 (a) Channeled substrate planar visible laser [29] and (b) Single-quantum-well ridge laser [28].

Raman microprobe studies of both III-V semiconductor lasers shown above have provided some valuable insight into device degradation and failure. Both lasers can operate at 30 mW/facet and heat sink temperatures between 50-100°C. The III-V semiconductor laser ages and degrades in two regimes. The first regime is slow, taking several hundred operational hours to increase the threshold current by 10 percent. The second regime takes only a few hours to

catastrophically damage the device by melting spots on the laser facets.

In the first stage of heating, Raman microprobe experiments determined the active region is approximately 100°C warmer than the device substrate. The temperature rise is attributed to Joule heating [28]. Figure 3.2 shows an approximate 120°C temperature difference in the channeled substrate device between the active region and a point 40 μm into the GaAs substrate. This indicates that device heating is mainly confined to the active region of the laser.

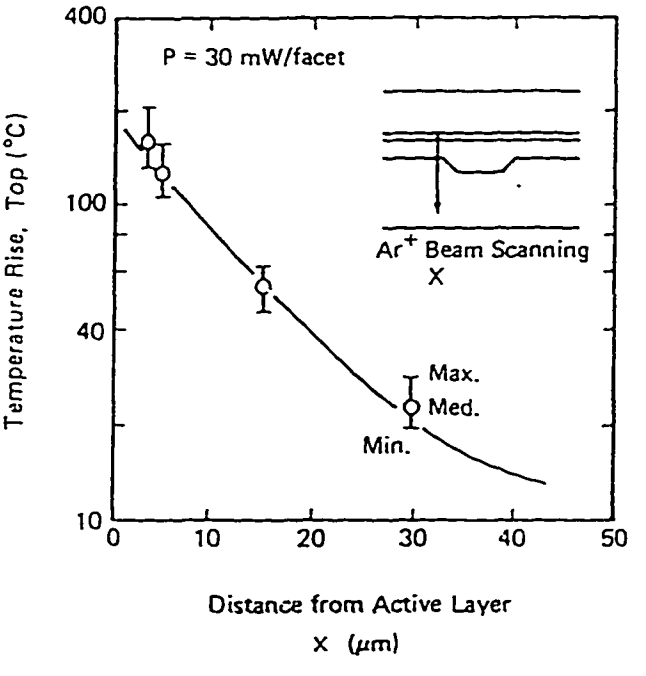


Figure 3.2 Temperature change from active region to substrate for a GaAlAs channeled substrate laser [29].

This research suggests most of the device heating is confined to the active region of the laser. The thermal conductivity of GaAs is over 20 times greater than PbTe; therefore, the PbTe DH laser being investigated in this chapter will not dissipate the heat as efficiently as the GaAs laser shown above. This information is helpful when evaluating heat dissipation properties of semiconductor lasers.

In the second regime, hot spots (~1000°C) are formed along the facet of the device leading to catastrophic failure. The hot spots are attributed to optical absorption near the facets of the laser; the heating problem is compounded by III-V material bandgap shrinkage as temperature increases, leading to additional photon absorption. This thermal behavior has been demonstrated by high power GaAs semiconductor laser failure due to thermal runaway [32].

Temperature profiling along the device contact stripe of III-V semiconductor lasers has also been performed; this work showed significantly cooler temperatures as the probe moved away from the device facets (see Figure 3.3) [28,29]. This strengthens the argument that second regime heating is confined to the facet area of the active region.

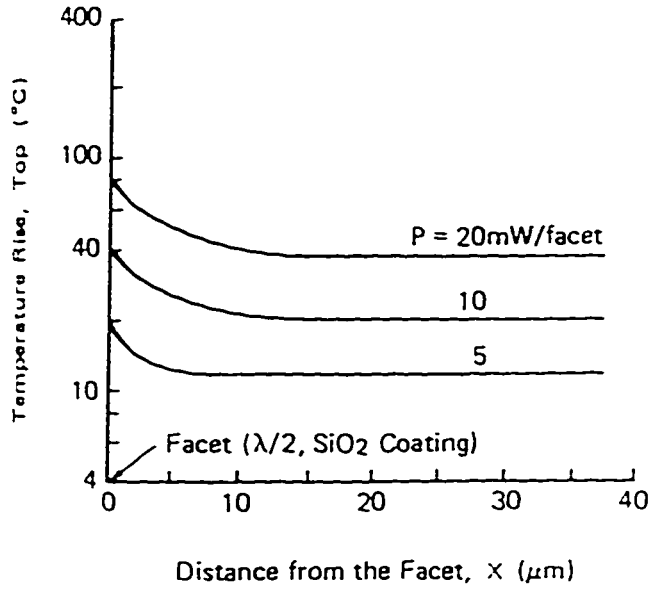


Figure 3.3 Temperature change along stripe of GaAlAs diode lasers [28,29].

Theoretical work on these lasers has also been done; it quantified the dependence of active region temperature on distance from heat sink and material thermal conductivities [32]. This theoretical work predicted the two heating regimes observed in experiments.

Bandgaps of PbSeTe and PbSnSeTe increase with temperature as shown in Figure 1.2 which reduces concerns about hot spots forming on IV-VI semiconductor laser facets. This suggests IV-VI semiconductor lasers are inherently more reliable than III-V lasers from a thermal runaway aspect. Raman microprobe research on III-V lasers

will be used to design and interpret thermal models of IV-VI semiconductor lasers described in this dissertation.

3.3 IV-VI Semiconductor Lasers

Most commercially available IV-VI semiconductor lasers emit a few hundred microwatts of optical power per mode and require a heat sink temperature of 100 K or less. In 1995, a molecular beam epitaxy (MBE) grown PbEuSeTe/PbTe separate confinement buried heterostructure (SCBH) diode laser operated in continuous wave (cw) mode with a heat sink temperature of 223 K; however, the laser spectrum at this temperature could not be taken due to its very low output power [33]. In 1988, a MBE-grown PbSe\PbSrSe DH diode laser operated in cw mode at 169 K and in pulsed mode at 290 K [34]. Theoretical predictions by Rosman et al. [35] also suggest substantial improvements in operating temperature for IV-VI devices. These improvements could be greater than those described above which suggest IV-VI materials can lase at temperatures higher than 223 K.

Thermoelectric cooling (TEC) modules can achieve temperatures of approximately 220 K (Melcor, Inc., Trenton, N.J.). Successful infrared spectroscopy applications using TEC modules would require laser operation at heat sink temperatures of approximately 250 K, allowing an adequate

temperature tuning range for high resolution infrared spectroscopy. The next section compares a thermal model of a presently available IV-VI semiconductor laser to a new laser design in which copper is used as a host substrate of the emitter.

3.4 Thermal Models of Proposed Laser Design [39]

Several years of research have been spent to develop a reliable IV-VI semiconductor laser that can operate at TEC temperatures. Although substantial improvements toward TEC devices have been made in recent years, it is apparent that new methods of fabrication must be explored to achieve these devices. The remaining parts of this section will explore the advantages of one such design.

Copper has a thermal conductivity that is approximately 200 times larger than PbTe or PbSe. Therefore, if IV-VI semiconductor laser structures are transferred from the thermally insulating IV-VI substrates to a copper substrate, heat dissipation should be drastically improved. Table 3.1 lists thermal conductivities of various materials found in the IV-VI semiconductor laser being modeled in this chapter.

Table 3.1

Region	Thickness or Width (μm)	Thermal Conductivity (W/K-m) at 200 K and 300 K	
Active (PbTe)	0.75	3.0	2.3
Cladding (PbEuSeTe)	1.5	2.7	2.1
Capping (PbTe)	0.75	3.0	2.3
Contact Stripe (Sn)	20	70.1	62.5
Substrate (PbTe)	250	3.0	2.3
Substrate (Copper)	250	413	398

Note the 23% decrease in thermal conductivity of PbTe from 200 K to 300 K. In comparison, the thermal conductivity of copper decreases only 3.6% in the same temperature range. This emphasizes the fact that copper is a superior heat sinking material when devices are operated at or near room temperature.

Grafting semiconducting devices onto foreign substrates has generated numerous windows of opportunity for dissimilar/mismatched material systems as mentioned in Chapter One (e.g. gallium arsenide on silicon, etc.). Modified gallium arsenide ELO\flip-chip techniques [11] may be employed to lift-off IV-VI laser structures and transfer them to a copper heat sink.

The finite element modeling software used in these studies is QuickField 3.40, by Tera Inc. The software solves two dimensional heat flow, electrostatics, current flow, stress analysis, etc. problems by constructing a mesh throughout the model. The program solves two-dimensional differential equations at the mesh intersection points using adjacent nodes as boundary conditions. Figure 3.4 shows the mesh constructed by QuickField 3.40. This mesh is used for the thermal modeling results shown in Figure 3.5 and 3.6.

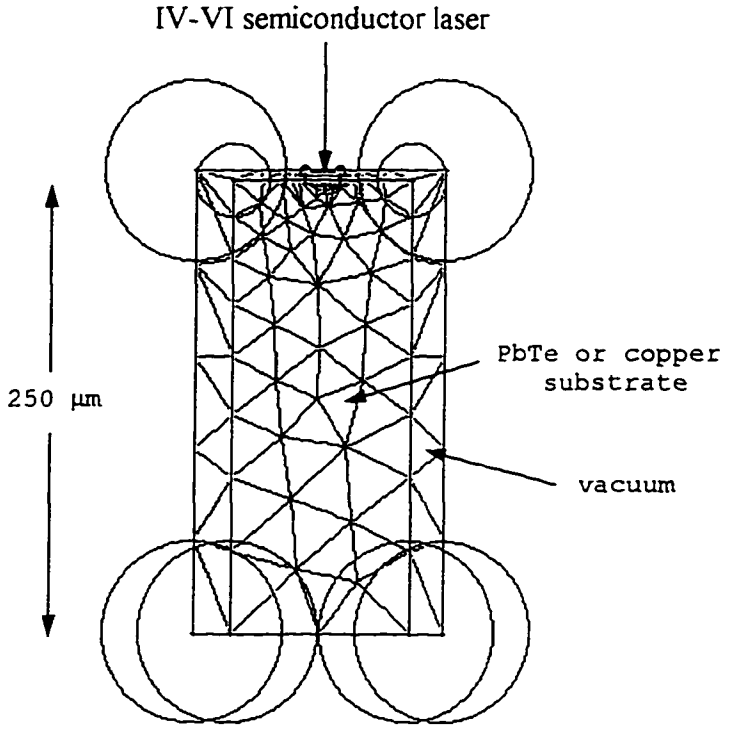


Figure 3.4 Two dimensional mesh generated by QuickField 3.40 for analyzing heat transfer in Figures 3.5 and 3.6.

Figure 3.5 shows the results from a finite element thermal model of a PbTe\PbEuSeTe DH diode laser with a 250 μm thick PbTe substrate, 250 μm long cavity, 20 μm contact stripe, 1.5 μm thick cladding layers, 0.75 μm thick cap layer, and 0.75 μm thick active layer; this was the laser described by Feit et al. [36] which had a threshold current density of 6 KA/cm^2 at a heat sink temperature of 175 K in cw mode. Assumptions of heat generation confined to the active region of the device, supported by III-V Raman research, and of linear heat flow will be used in all the following models. Since the thermal conductivity values for copper and PbTe are near-linear in the 200 K to 300 K range, linear values were used in the finite element models. Figure 3.5 below shows isotherms produced in the DH laser by 6 KA/cm^2 (threshold) and 20 KA/cm^2 (three times threshold). Note that increasing the current density from threshold to 20 KA/cm^2 will increase the active region temperature by 87°.

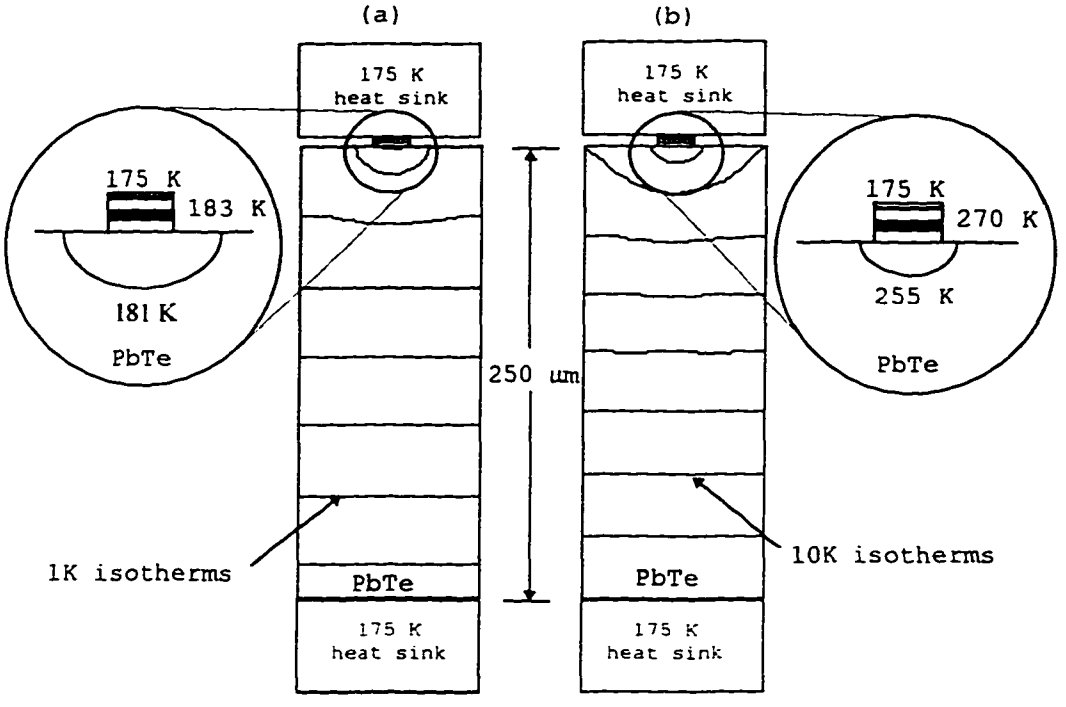


Figure 3.5 Isotherms produced in a PbTe\PbEuSeTe DH diode laser with (a) 6 KA/cm^2 and (b) 20 KA/cm^2 current density. The heat sink temperature is 175 K and the active region for (a) is 183 K and for is (b) 270 K. Note for (b) there is a 95° temperature difference between the active region and heat sink.

Figure 3.5a shows an 8° difference between active region and heat sink temperatures; Figure 3.5b shows a 95° temperature difference between active region and heat sink, illustrating the effects of increasing the current density. The 6 KA/cm^2 current density used in Figure 3.5a corresponds to 300 mA of current through the DH laser structure. Note that the PbTe substrate essentially forms

a thermal trap impeding efficient heat dissipation away from the active region of the laser, illustrated clearly in Figure 3.5b. The next model illustrates the same device after removing the PbTe substrate and transferring it to a copper heat sink.

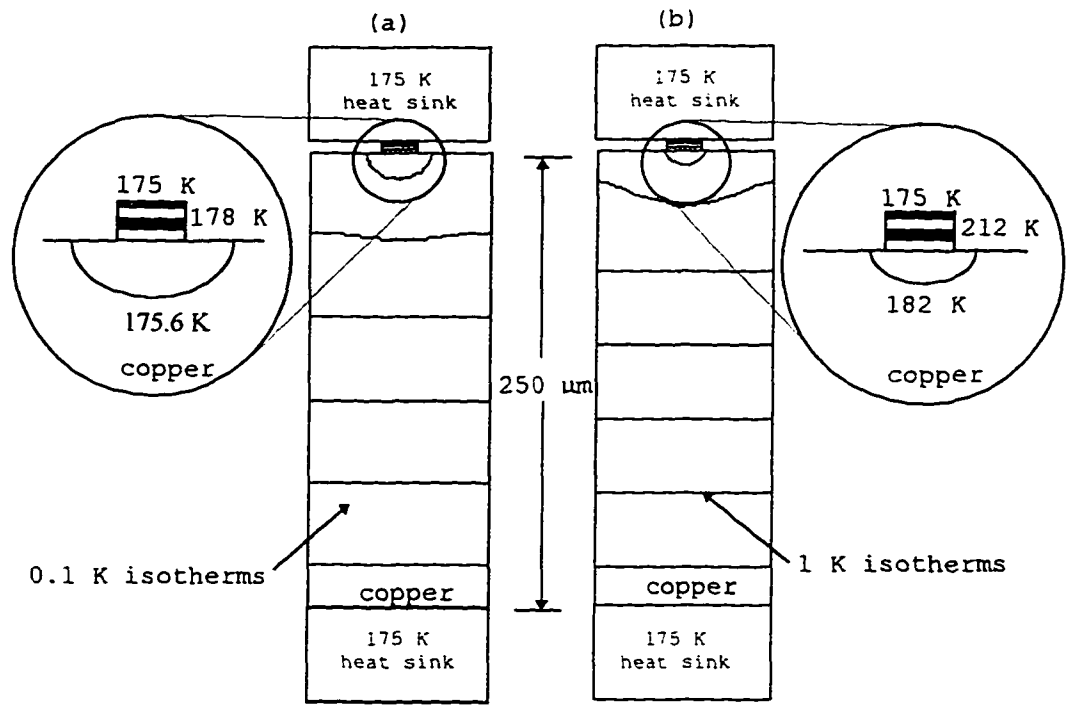


Figure 3.6 Isotherms produced by (a) 6 KA/cm^2 and (b) 20 KA/cm^2 current density in a PbTe\PbEuSeTe DH diode laser after transferring it from a PbTe substrate to copper. The heat sink temperature is 175 K and the active region is (a) 178 K and (b) 212 K, respectively. A 58° decrease in active region temperature is realized at a current density of 20 KA/cm^2 by replacing the lead-salt substrate with a copper one.

Figure 3.6a shows only a 3° temperature difference between the heat sink and the active region at a current density of 6 KA/cm^2. As illustrated in Figure 3.6b, the temperature difference between the active region and the heat sink increases to 37° when the current density in increased to 20 KA/cm^2. Note the 58° decrease in active region temperature by comparing the modeling results presented in Figure 3.5b and 3.6b.

Similar buried heterostructure (BH) IV-VI lasers have operated in cw mode with a heat sink temperature of 180 K [38]. Also, Spangler et al. [34] have demonstrated a PbSe\PbSrSe DH laser operating in pulse mode at 290 K. The active region of this device is PbSe. The PbSe\PbSrSe DH laser was operated with a repetition rate of 1 KHZ and a pulse width of 200 ns; the duty cycle for this laser is 0.02%. In pulse mode, the PbSe\PbSrSe DH emitter lased less than 1% of the time. Using this duty cycle, the active region of the laser has sufficient time to reach thermal equilibrium with the 290 K heat sink; the PbSe active region is much warmer than the heat sink during lasing, as indicated by III-V semiconductor laser Raman microprobe research. This suggests the PbSe active region could be well over 300 K during lasing. Therefore, 290 K is a conservative estimate of the maximum active region

temperature during lasing. The 290 K active region temperature limit will be used as an important thermal model evaluation criteria.

To gain a deeper understanding of the heat dissipation improvements that can be realized by this device transfer, Figure 3.7 shows the active region temperature response as the heat sink temperature is increased while the current density remains constant (20 KA/cm^2).

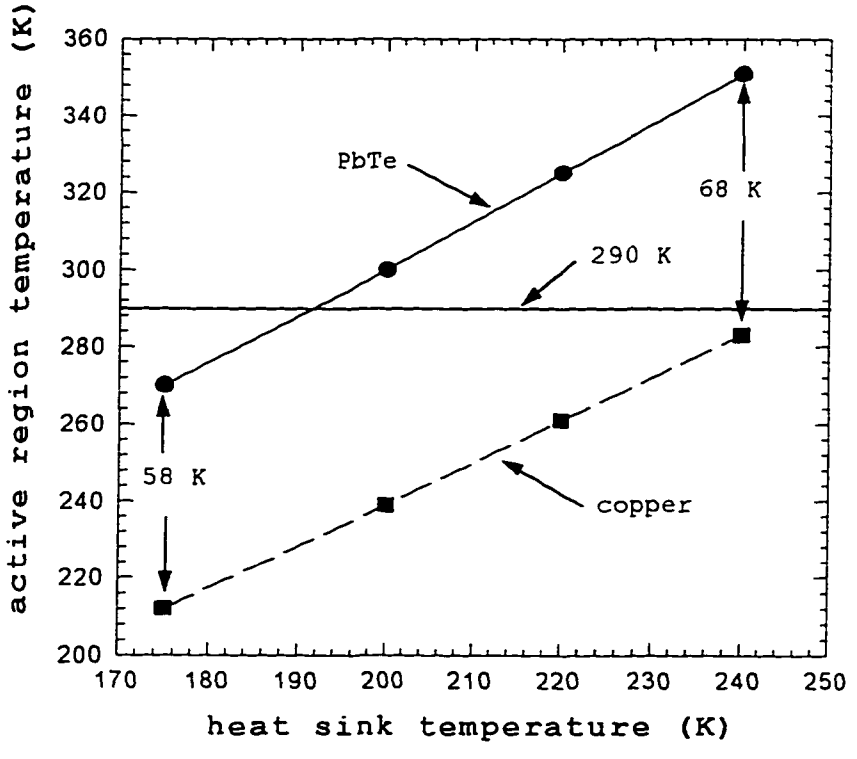


Figure 3.7 Active region temperature versus heat sink temperature for a laser with a 20 KA/cm^2 injection current density. The heat sink temperature changes from 175 K to 240 K. The average difference in active region temperature over this range is 63°. The assumed maximum temperature for the active region is 290 K.

In the 175 K to 240 K temperature range displayed in Figure 3.7, an average 63° decrease in active region temperature is realized by changing the substrate from PbTe to copper. With a 20 KA/cm^2 injection current density and 175 K heat sink temperature, the active region of the on-copper laser shows a 58° decrease over the PbTe arrangement. If the heat sink temperature is increased to 240 K, the on-copper arrangement shows a 68° decrease in active region temperature. As noted in Figure 3.7, the on-copper arrangement dissipates heat more efficiently as the heat sink temperature is increased. This stems from the fact that the thermal conductivity of PbTe decreases 23% while copper only decreases 3.6% over the displayed 200 K to 300 K heat sink range. The DH laser in the above simulation was modeled with a constant current density; in reality the threshold current density increases with heat sink temperature thus increasing the active region temperature, making the on-copper heat dissipation improvements more pronounced.

The active region temperature of the simulated Feit et al. DH laser reached 290 K with a current density of 20 KA\cm^2 and a heat sink temperature of 190 K. This 100° difference between active region and heat sink is consistent with the III-V Raman temperature profiling

discussed in Section 3.2. Figure 3.8 shows Quickfield temperature profiling results for the two DH laser arrangements. In the simulation, the current density and the heat sink temperature are held constant at 20 KA/cm^2 and 175 K, respectively.

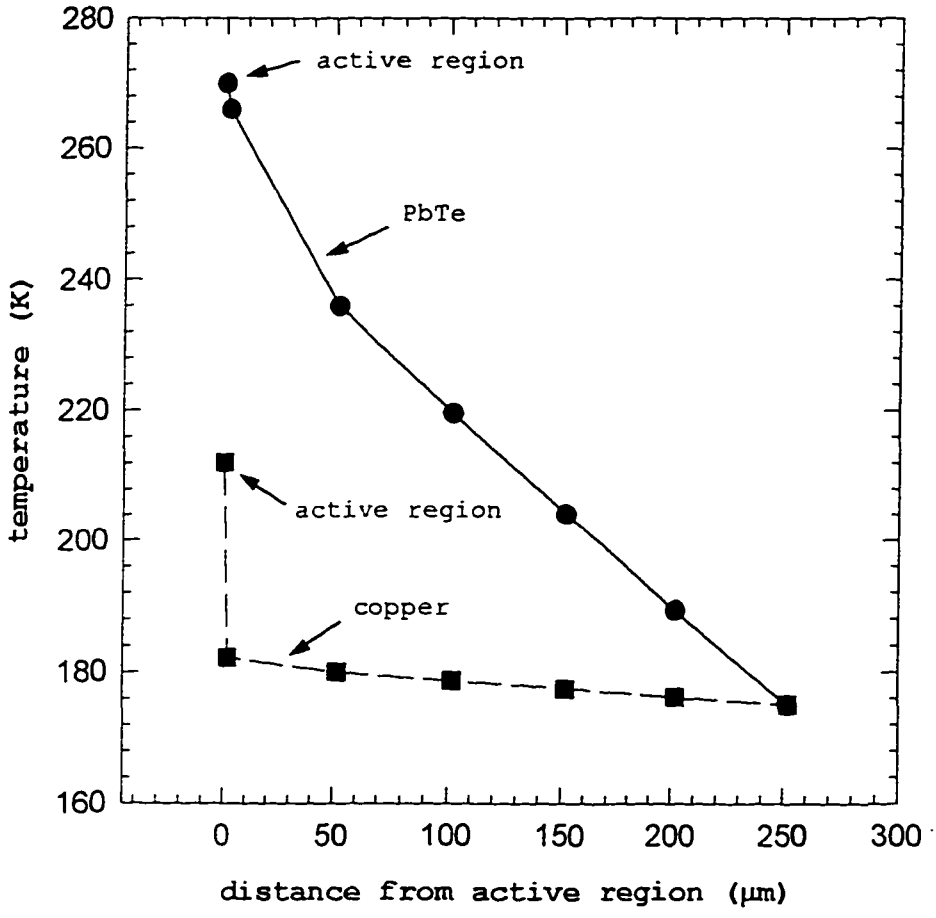


Figure 3.8 Temperature versus distance from the active region, a constant 20 KA/cm^2 current density and 175 K heat sink temperature were used in this model. Note the 30° drop in temperature between the active region and contact point with the substrate for the on-copper laser.

Figure 3.8 displays the temperature change as a function of distance from the active region for the two laser arrangements under identical operating conditions of 20 KA/cm^2 current density and 175 K heat sinks. For the DH laser on PbTe there is a 95° decrease in temperature from the active region to the heat sink and a 4° decrease from the active region to the growth substrate. This 95° difference is in good agreement with the Raman microprobe research mentioned in Section 3.2. The on-copper laser shows a 30° drop in temperature from active region to copper substrate. For the copper arrangement, there is only a 7° decrease in temperature from the substrate/semiconductor interface to the heat sink. This figure supports the conjecture that the PbTe material forms a thermal trap, impeding efficient heat removal from the active region. Figures 3.7 and 3.8 illustrate the significant improvement in operation temperature by transferring the Feit et al. DH laser structure from PbTe to copper.

An important result of these computer simulations is understanding the heat dissipation properties of the two laser arrangements when the emitter is mounted on a thermoelectric cooling module. This type of heat sink mounting will allow laser operation without the necessity

of liquid nitrogen or helium. Figure 3.9 illustrates how the PbTe and the on-copper active region temperatures change as the current density is varied from 6 KA/cm^2 to 25 KA/cm^2 with a constant TEC heat sink temperature of 220 K.

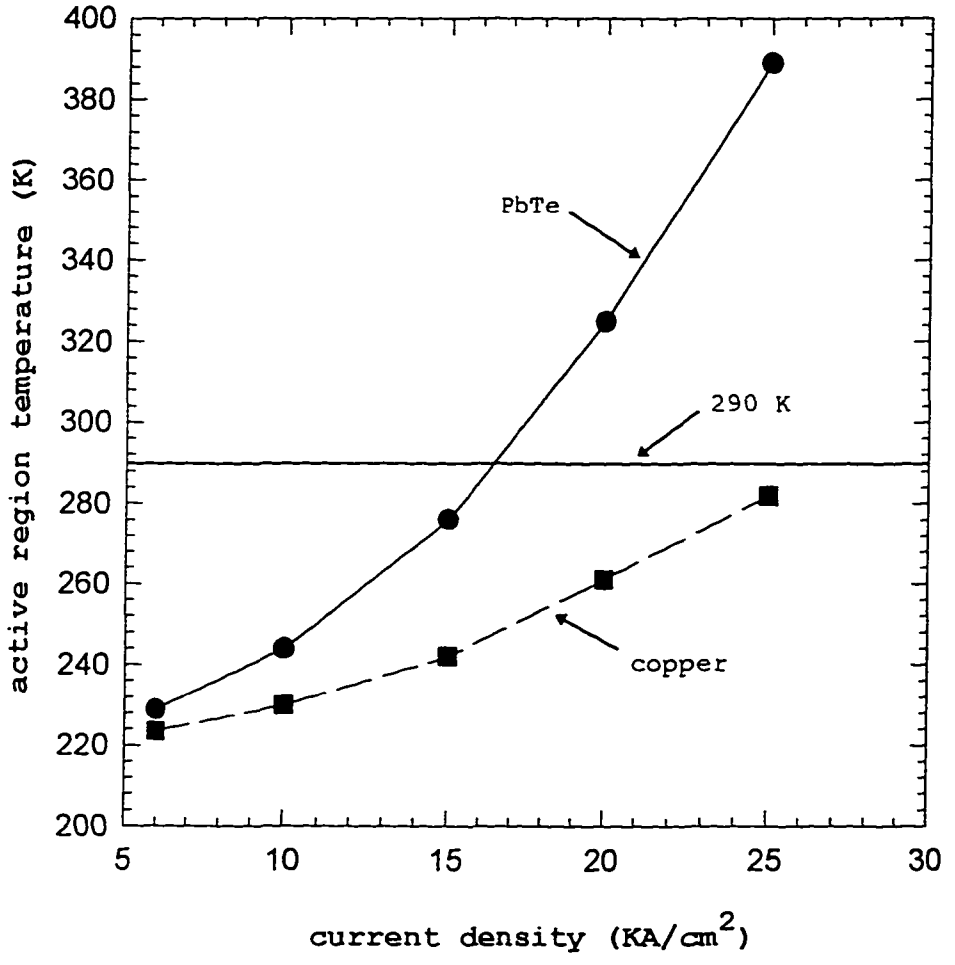


Figure 3.9 Active region temperature of PbTe and on-copper substrate lasers versus current density. The current density is varied from 6 KA/cm^2 to 25 KA/cm^2 while the heat sink remains constant at 220 K. Note the on-copper heat dissipation is greater at higher current densities.

Figure 3.9 displays computer simulation results of the Feit et al. DH laser mounted on a 220 K heat sink; a significant decrease in active region temperature is noted for the on-copper laser with current densities greater than 10 KA/cm^2. As the current density is increased, the on-copper device dissipates heat more efficiently; at 25 KA/cm^2 the active region reaches approximately 282 K for the on-copper emitter and 386 K for the PbTe device, yielding an active region temperature difference of over 100° between the two device arrangements. For injection current densities greater than 16 KA/cm^2, the active region temperature of the PbTe laser is over the 290 K limit. In comparison, a 1995 BHSC diode laser constructed by Feit et al. [37] lased with a threshold current density of 50.6 KA/cm^2 and a heat sink temperature of 215 K, double the current density value attained in the Quickfield models. The 1995 BHSC laser results add validity to the assumptions used in the computer simulations.

3.5 The Effects of Metallic Bonding Layer Thickness

Until this point, QuickField thermal models have excluded a metallic bonding layer that can be used to adhere the device to the copper heat sink. This section will include a metallic bonding layer in the model and investigate its effects on the active region temperature.

All other device dimensions will remain as in the previous section. The sketch below shows the DH diode laser mounted on a copper heat sink; a 40-60 eutectic lead-tin alloy is used as the metallic bonding medium. The thermal conductivity of 40-60 lead-tin is 21 times larger than PbTe. The top press-fit contact can be made of gold; its thickness is less than 3000 Å. The models in this section will neglect the effects of the gold contact.

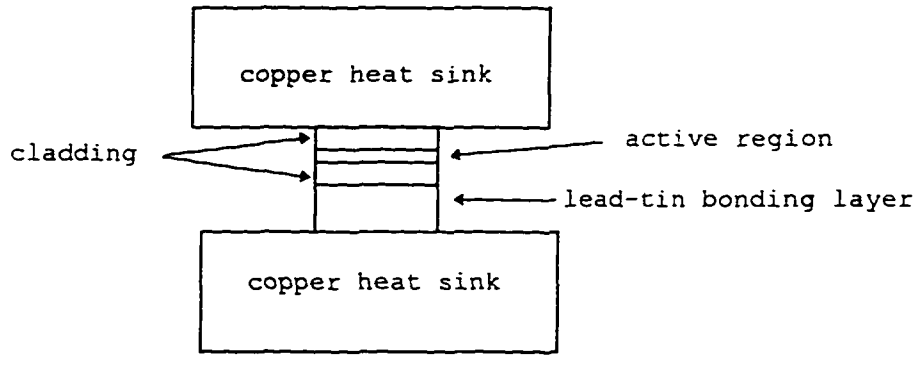


Figure 3.10 A IV-VI semiconductor DH diode laser mounted to a copper heat sink by a 40-60 eutectic lead-tin bonding layer.

QuickField simulations were performed on various lead-tin bonding layer thicknesses. In these models, the heat sink temperature is 220 K and the current density is 20 KA/cm^2. A 3.9 K increase in active region temperature was attained when changing the bonding layer thickness from 0

to 5 μm, with only 0.16 K difference between 0 and 1 μm. Figure 3.11 shows the nonlinear active region temperature response to changing bond layer thicknesses. The undulations in Figure 3.11 are due to different mesh positions as bond layer thicknesses are changed.

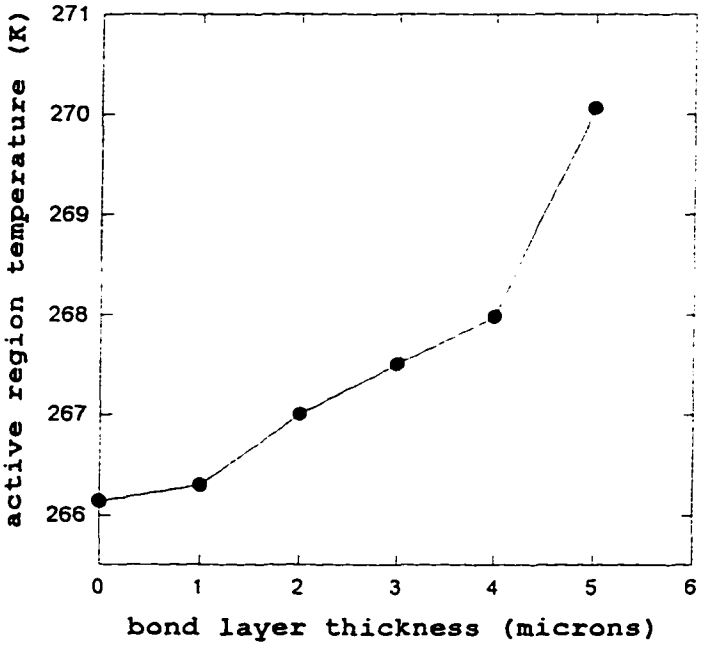


Figure 3.11 Active region temperature changes as metallic bond layer thickness is changed from 0 to 5 μm. The heat sink temperature is 220 K and the current density is 20 KA/cm^2 for these models.

From these simulations, it is apparent the lead-tin bond layer thickness has little effect on active region temperature when held under 4 μm. The active region temperature increases 1.78 K when the bond layer thickness is changed from 0 to 4 μm, and 2.14 K when bond layer thickness is changed from 4 to 5 μm. As shown in Figure 3.11, the active region temperature increases significantly when the lead-tin bond layer is over 4 μm thick.

3.6 The Laser Diode Array

Commercially available IV-VI semiconductor lasers usually provide a few hundred μw of optical power per mode. If greater output power is needed, a planar array of semiconductor lasers focused through an appropriate lens could be used. This complicates thermal management as more than one diode laser resides on the same substrate. In order to improve the thermal properties of this type of device, the array could be assembled on a copper heat sink as discussed in the previous sections. Figure 3.12 is an isotherm plot of five PbTe DH lasers on a single copper heat sink. The diode lasers have the same dimensions as given in section 3.4. and are spaced 20 μm apart. The thermal simulation takes into account a 1 μm thick tin bonding layer between the laser's cladding and copper heat

sink. As explored in the previous section, the 1 μm bonding layer thickness has little effect on active region temperature. 20 KA/cm^2 is the injection current density through each active region.

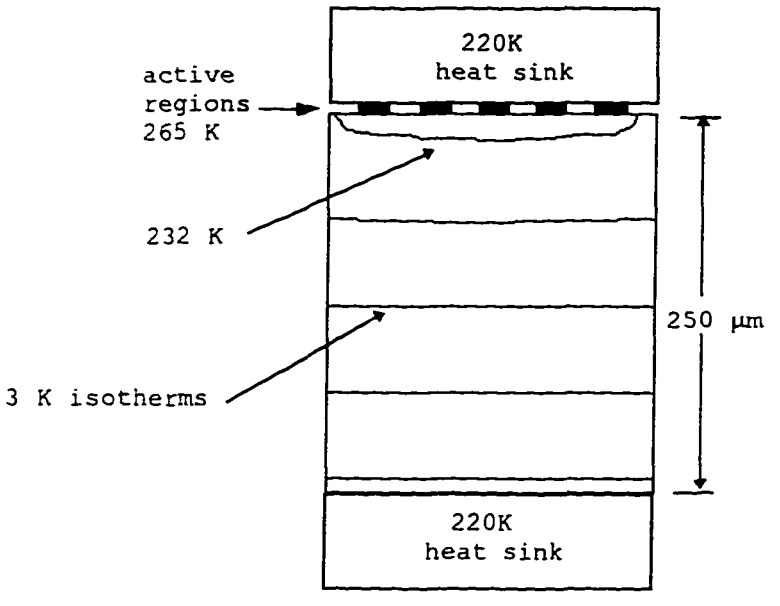


Figure 3.12 An array of five diode lasers on a single heat sink. The active region temperature is 265 K with less than one degree variance between lasers.

For an array of five DH lasers on a 220 K heat sink, the average active region temperature for the device is 265 K. This is five degrees warmer than a single active region device. Less than one degree variance is present between active regions of the individual lasers; the center laser

being a few tenths of a degree warmer than the outside ones. Due to the close spacing of the isotherms near the active regions, the isotherms could not be adequately displayed. An active region temperature of 265 K still allows TEC operation and falls 25° below the conservative maximum active region temperature limit of 290 K. For a better understanding of the active region heating of the array, Figure 3.13 plots the average active region temperature as the heat sink temperature is changed from 175 K to 240 K.

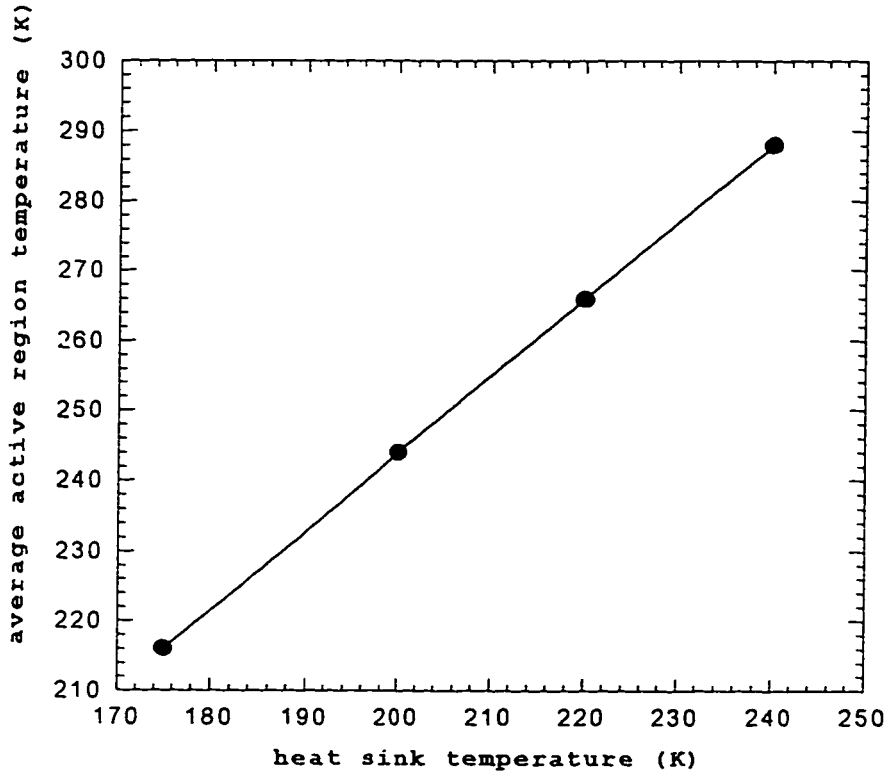


Figure 3.13 Average active region temperature versus heat sink temperature of a device containing five lasers on a single heat sink. The injection current density of each laser of the array is 20 KA/cm^2.

The average active region temperature of the array increased from 216 K to 288 K at a heat sink temperature 175 K and 240 K, respectively. Figure 3.13 predicts the laser array can operate with a 240 K heat sink temperature and stay below the 290 K active region maximum limit set forth.

The thermal models presented in this chapter predict the on-copper device geometry offers heat dissipation properties that may not be achieved by other means. As modeling suggested, transferring IV-VI semiconductor lasers from their lead-salt substrates should allow TEC operation. The effects on III-V semiconductor lasers should also be investigated for possible improvements in heat dissipation. The theoretical predictions put forth in this chapter serve as motivation in constructing such a IV-VI device.

Chapter Four presents techniques used in fabricating the on-copper IV-VI DH laser structures studied in this chapter. Analyzing the metallic bonding layer used to adhere the IV-VI semiconductor laser to the copper heat sink will be the main focus of the next chapter.

References

[11] E.Yablonowitch, E.Kapon, T.Gmitter, C.Yun, and R.Bhat, "Double Heterostructure GaAs/AlGaAs Thin Film Diode Lasers on Glass Substrates", *IEEE Photonics Tech. Lett.* **1**, 41 (1989).

[27] C.Kittel, Introduction to Solid State Physics John Wiley and Sons, Inc., page 308, 1986.

[28] H.Brugger, P.Epperlein, "Mapping of Local Temperatures on Mirrors of GaAs/AlGaAs Laser Diodes", *Appl. Phys. Lett.* **56**, 1049 (1990).

[29] S.Todoroki, M.Sawai, and K.Aikj, "Temperature Distribution Along the Striped Active Region in High-Power GaAlAs Visible Lasers", *J. Appl. Phys.* **58**, 1124 (1985).

[30] W.Tang, H.Rosen, P.Vetttiger, and D.Webb,"Evidence for Current-Density-Induced Heating of AlGaAs Single-Quantum-Well Laser Facets", *Appl. Phys. Lett.* **59**, 1005 (1991).

[31] F.Gfeller, and D.Webb, "Degradation and Lifetime Studies on High-Power Single-Quantum-Well AlGaAs Ridge Lasers", *J. Appl. Phys.* **68**, 14 (1990).

[32] R.Schatz, and C.Bethea, "Steady state Model for Facet Heating Leading to Thermal Runaway in Semiconductor Lasers", *J. Appl. Phys.* **76**, 2509 (1994).

[33] Z.Feit, M.McDonald, R.Woods, V.Archambault, and P.Mak, "Low Threshold PbEuSeTe/PbTe Separate Confinement Buried Heterostructure Diode Lasers", *Appl. Phys. Lett.* **68**, 738 (1996).

[34] B.Spanger, U.Schiessl, A.Lambrecht, H.Bottner, and M.Tacke, "Near-Room-Temperature Operation of $Pb_{1-x}SrSe$ Infrared Diode Lasers Using Molecular Beam Epitaxy Technique", *Appl. Phys. Lett.* **53**, 2582 (1988).

[35] R.Rosman, and A.Datzir, "Lifetime Calculations for Auger Recombination in Lead-Tin-Telluride", *IEEE J. of Quantum Elec.* **QE-18**, 814 (1982).

[36] Z.Feit, R.Woods, D.Kostyk, and W. Jalenak, "Low-Threshold PbEuSeTe Double-heterostructure Laser Grown

by Molecular Beam Epitaxy", *Appl. Phys. Lett.* **55**, 16 (1989).

[37] Z.Feit, D.Kostyk, R.Woods, and P.Mak, "Molecular Beam Epitaxy-Grown Separate Confinement Buried Heterostructure PbEuSeTe-PbTe Diode Laser", *IEEE Phont. Tech.* 7, 1403 (1995).

[38] Z.Feit, D.Kostyk, R.Woods, and P Mak, "PbEuSeTe buried Heterostructure Lasers Grown by Molecular-Beam Epitaxy", *J. Vac. Sci. Tech. B* **8**, 200 (1990).

[39] K.R. Lewelling and P.J. McCann, "Finite Element Modeling Predicts Possibility of Thermoelectrically-Cooled Lead-Salt Diode Lasers", *IEEE Phont. Tech.*, to be published in March 1997.

Chapter 4

Metallic Bonding Layer Formation and Barium Fluoride Removal Procedure Used with IV-VI Epilayer Lift-Off Processing

4.0 Introduction

This chapter describes a metallic bonding layer and BaF_2 substrate removal process needed to fabricate IV-VI semiconductor lasers grown on polished BaF_2 substrates. The metallic layer secures the epi-structure to a rigid support while the BaF_2 growth substrate is removed. This metallic layer becomes part of the device packaging as was thermally modeled in the previous chapter; therefore, careful consideration must be given to the thermal and electrical properties of the bonding material. Many challenges were confronted during this phase of laser development, which will be mentioned to clarify research direction when needed.

4.1 Choice of a Bonding Medium

4.1.1 Evaluation Criteria

Several criteria must be considered when choosing an appropriate bonding medium. Table 4.1 is a list of metals and alloys that have been evaluated by the author for use with IV-VI semiconductor contacts and bonding.

Table 4.1

material	melting point (°C)	mechanical hardness (brinell)*	thermal conductivity W/ m-K*	electrical resistivity (μΩ-cm)*
gold	1063	25	318	2.125
lead	327.43	4.2	35.3	20.65
tin	231.9	3.9	66.8	11
indium	156.17	0.9	147	8.37
copper	1083	40	401	1.68
silver	960.8	36	429	1.586
lead-tin (40-60)	183	10.7	49	15
indium-silver(90-10)	144	2.68	~156	5.69

* near room temperature values

Thermal and electrical conductivity, mechanical hardness, low melting temperature, and wettability are important considerations when choosing a good bonding/contact medium.

Thermal and electrical conductivities directly affect the heat dissipation and power consumption of the operating device. A high thermal conductivity of the bonding medium is imperative for enhanced heat dissipation of the active region for IV-VI semiconductor DH lasers studied in this work. Wettability is important to ensure good bonding layer adherence to the semiconductor and copper substrate. A low melting temperature reduces concerns of impurity diffusion into the semiconductor while applying the metallic bonding layer. A high bonding layer mechanical hardness provides smoother breaks in the metallic adherence medium; the need for this characteristic is discussed in the cleaving procedure section of Chapter Five.

Copper and silver, materials listed in Table 4.1, are not widely used for bonding media; although copper has been successfully used for electrical contacts and interconnects for silicon devices [40]. As thermally modeled in the previous chapter, the bonding layer thickness could range from 1 μm to 4 μm; therefore, gold and silver are unattractive choices due to high melting temperatures and expense. Elemental metals also suffer from dendritic crystal formation when cooling [41]. These dendrites, which are referred to as "whiskers", can detrimentally affect device processing. The next section describes and evaluates experimental results from tests performed on the remaining candidates listed in Table 4.1.

4.1.2 Elemental Lead Bonding Medium

Lead is a viable bonding layer candidate; it has a relatively low melting temperature and is the main constituent in the LPE growth melt making it chemically similar to the epilayer. As shown in Figure 4.1, the lead bonding layer must adhere to both the copper substrate and IV-VI epilayer. Lead has successfully formed ohmic contacts to n-type IV-VI semiconductors [42]. Also, lead was used by Holloway et al. [26] to construct a laser by thermally evaporating a lead strip on a p-type PbTe layer grown on

BaF_2. This research indicates lead readily adheres to the IV-VI semiconductor layer surface.

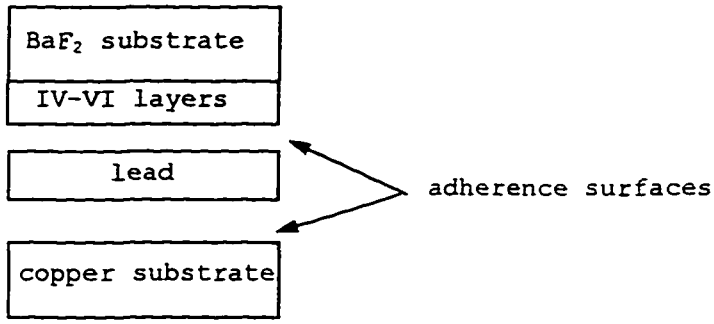


Figure 4.1 The lead bonding layer lies between the IV-VI semiconductor surface and the copper substrate surface.

Although lead forms a good contact to the IV-VI epilayer, it does not readily wet the surface of copper; therefore, the copper surface must be "tinned" prior to the application of lead for good adherence [43]. The additional "tinning" process further complicates the bonding procedure.

In several experiments, lead was thermally evaporated onto both semiconductor and "un-tinned" copper surfaces. After the device structure and copper substrate were mated, a small mechanical pressure was applied; refer to Figure 4.1 for layer arrangement. The mated sample assembly was then placed in a vacuum and evacuated to ~10^{-6} torr. After the vacuum pressure stabilized, the sample was heated with a high intensity lamp to melt the lead. This process did not

yield good adherence to the copper substrate upon inspection. More details for this process can be found in Appendix A.

4.1.3 Elemental Tin Bonding Medium

Tin was investigated for its bonding properties. Tin melts at 226°C, a relatively low melting temperature, and has been successfully used to form ohmic contacts to n-type IV-VI semiconductor layers [42]. These two attributes reduce concerns about the tin-semiconductor interface and diffusion of tin into the semiconductor layer. Tin easily alloys with copper, forming a Cu_6Sn_5 interface layer [41]. This interface layer ensures good adherence of the epilayer structure to the copper substrate through the tin bonding medium.

Two methods of applying the tin bonding medium were investigated. One method involved thermally evaporating the tin; the other consisted of applying a tin layer as the last step of the LPE growth sequence.

The thermal evaporation method did not yield good results as the mounted sample would delaminate upon application of pressure or during BaF_2 substrate removal. Investigations on delaminated samples using optical

microscopy revealed inconsistent bonding across the entire interface; the unbonded areas will be referred to as bonding voids. It is believed the bonding voids are a result of IV-VI semiconductor surface undulation. 1 μm undulations are typical for IV-VI layers grown using LPE at the University of Oklahoma. The undulations appear to be growth steps resulting from mis-oriented BaF_2 substrates. The thermal evaporation method is described in Appendix A.

The second method entails applying a thick coating of tin on the IV-VI semiconductor structure as the last step of the LPE growth sequence. This method allows formation of the tin-semiconductor interface without exposure to an oxidizing environment. After epilayer growth and tin coating, the sample is removed from the LPE furnace. The tin coated sample is then inverted and placed in contact with the copper substrate. This arrangement is shown in Figure 4.1, with tin replacing the lead. A small downward force is applied to maintain close contact as the apparatus is heated to melt the tin. The heating cycle takes place in an open air environment.

Using the second method, complete epilayer lift-off was achieved for the first time. Figure 4.2 is a photograph showing the first complete epilayer lift-off by bonding the

epilayer to a copper substrate using tin. Notice the excess tin that is extruded around the edges of the semiconductor layer.

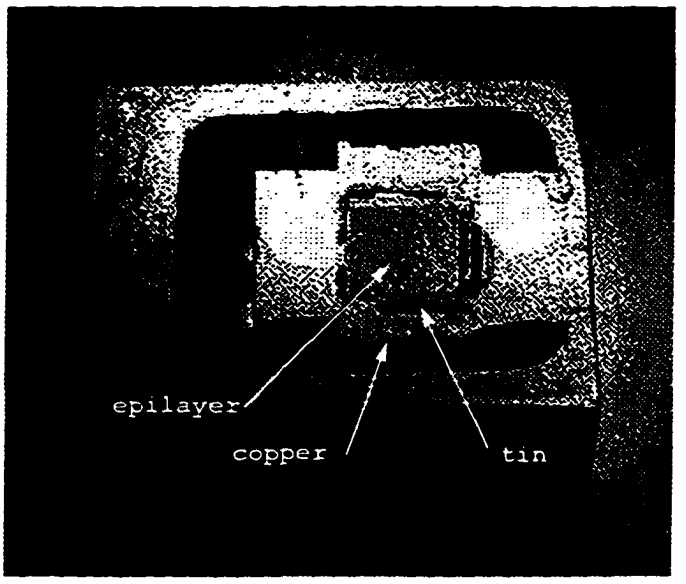


Figure 4.2 The first successful lift-off of a complete 1 cm^2 IV-VI epilayer. The PbSeTe n-type semiconductor layer was grown on a polished (100) BaF_2 substrate using the LPE technique covered in Chapter Two. The bonding layer of tin is approximately 10 μm thick.

Examining the formed tin bond by SEM microscopy revealed "whisker" like structures between the copper substrate and epilayer. These structures are dendritic crystals formed during the bonding medium cooling cycle. Figure 4.3 is a SEM micrograph showing the tin dendrites.

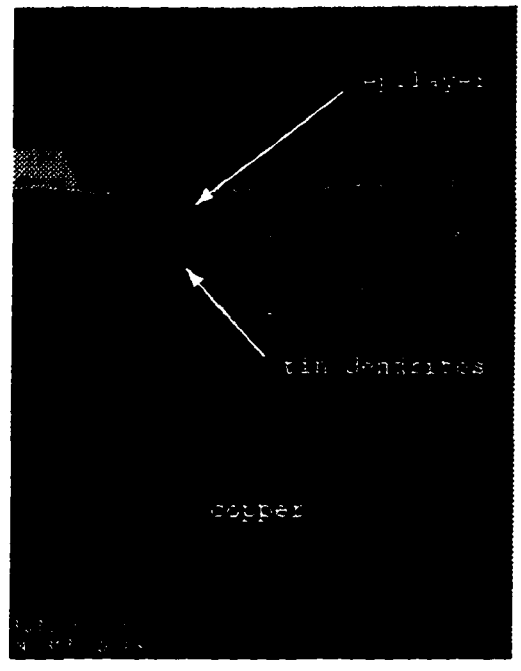


Figure 4.3 Epilayer bonded to copper substrate by using a layer of tin deposited in the LPE furnace. During the cooling cycle, tin dendrites form which prohibit close contact between the epilayer and copper substrate.

The height of the tin dendrites is approximately 10 μm, prohibiting the laser structure from forming a closer contact with the copper substrate. The dendrites adversely affect epilayer structure cleavage, making tin a less favorable candidate.

4.1.4 97-3 Indium-Silver and 60-40 Tin-Lead

Both 97-3 indium-silver and 60-40 tin-lead are eutectic alloys with low melting temperatures under 200°C. Eutectic

alloys are attractive candidates as their melting temperatures are below the constituent elements. Eutectic alloys form congruent melts, reducing concerns about solid phase precipitates forming in the bonding layer. The solid precipitates can prevent the formation of a close contact between epilayer structure and copper substrate. Mechanical hardness is also affected by alloying different metals; for example, 97-3 indium-silver and 60-40 tin-lead alloys are two times harder than the constituent elements. Mechanical hardness improves smoothness of metal breaks during the cleaving procedure as discussed in Chapter Five.

The 97-3 indium-silver bonding layer was applied to both semiconductor and copper substrate using thermal evaporation techniques. Due to the difference in partial pressures between indium and silver, the alloy could not be thermally deposited from a single source. Therefore, elemental metals were deposited in discrete layers. A thin, 200 Å silver layer was deposited between two thicker, 0.5 μm indium layers on both semiconductor and copper substrate surfaces. The metal coated semiconductor and copper substrate were removed from the vacuum chamber before alignment and mating; Figure 4.1 shows the mating arrangement with the lead replaced by alternating indium and silver layers. After a small mechanical force is applied to

maintain alignment, the assembly is placed in the vacuum. Heat from a high intensity lamp melts the indium which dissolves the silver and forms the sought after 97-3 alloy. The epilayer structure adhered to the copper substrate with a total bonding layer thickness of 2 μm or more; however, it suffered critical delamination in the substrate removal process. This is probably a result of poor indium-copper interface alloying effects [44].

60-40 tin-lead has many characteristics that make it superior to the other bonding materials discussed thus far. With a relatively low melting temperature of 183°C, the 60% tin in the alloy helps form a Cu_6Sn_5 interface layer needed for good bonding to copper. Although the alloy has a smaller thermal conductivity than tin or indium, it is superior to the lead-salt semiconductor it replaces. Also, the 60-40 tin-lead does not suffer from dendritic crystal formation.

Experiments carried out using a 60-40 tin-lead bonding layer applied in the LPE furnace have shown promising results. This method involves coating the copper substrate with approximately 1 μm of tin using an electroless stannous chloride bath prior to the mating and bonding steps. The tin-copper interface layer ensures a good bonding surface

for the tin-lead coated IV-VI epilayer. Using this method, almost 100 percent of the samples had the BaF_2 substrate removed without critical epilayer delamination.

4.2 Barium Fluoride Removal Procedure

After the epilayer structure is bonded face down to a copper substrate as illustrated in Figure 4.1, the BaF_2 substrate must be removed before forming electrical and thermal contacts to the top side of the semiconductor device. BaF_2 is soluble in water [45]; therefore, the BaF_2 substrate was initially removed by soaking the bonded sample assembly for approximately two weeks in room temperature deionized water. This time consuming process slowed research efforts, necessitating the need for a faster removal process. The time needed for removal was reduced by soaking the sample in a HCL acid solution. Corrosion to the copper and bonding layer surfaces resulted from soaking the bonded sample assembly in the HCL acid solution. The corrosion degrades the adherence of the epilayer to the copper substrate resulting in critical delamination.

The corrosion problem was addressed using two complementary approaches. Sealing all exposed metals surfaces with a non-reactive substance and reducing the length of time the bonded sample is exposed to the HCL acid solution by improving the BaF_2 etch rate were employed.

Black wax is not attacked by a HCL acid solution; therefore, all exposed metal surfaces were coated with it to reduce metal corrosion. If the entire bonded assembly is submerged in the acid solution, all surfaces must be coated with black wax for protection. The amount of black wax coating was reduced by sealing a glass tube over the 1 cm^2 sample to create a small reservoir for the HCL acid solution. Figure 4.4 is a schematic showing a bonded sample with a reservoir in place.

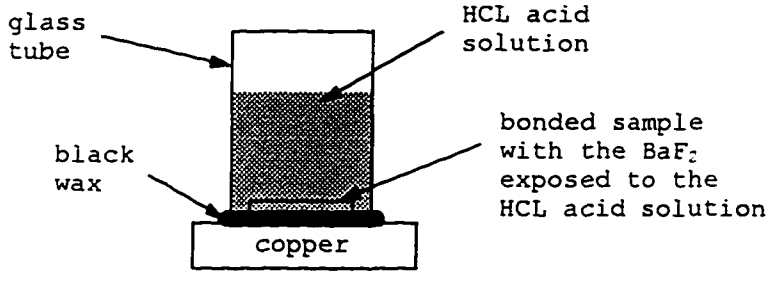


Figure 4.4 A small reservoir is created by sealing a glass tube over the bonded sample with black wax. The reservoir is filled with a 30% HCL acid solution to dissolve away the BaF_2 substrate and leave behind the epilayer structure bonded to the copper support.

The 50 mL reservoir in conjunction with the black wax sealing has virtually eliminated the detrimental corrosion problem.

The BaF_2 removal process can take up to two weeks using an un-agitated room temperature deionized water bath. Although the process is reduced to three days by using a 30%

HCL solution; it is still time consuming and slows research efforts. One method used to etch the polished growth surface of BaF_2 is to submerge the substrate in stirred deionized water; stirring reduces the time needed to etch the BaF_2 substrate prior to LPE growth. Although stirring the HCL acid solution by magnetic means is awkward due to the size of the sealed glass tube and position of the mounted sample, it was decided some means of agitation would speed the substrate removal process. The result of this effort is schematically shown in figure 4.5.

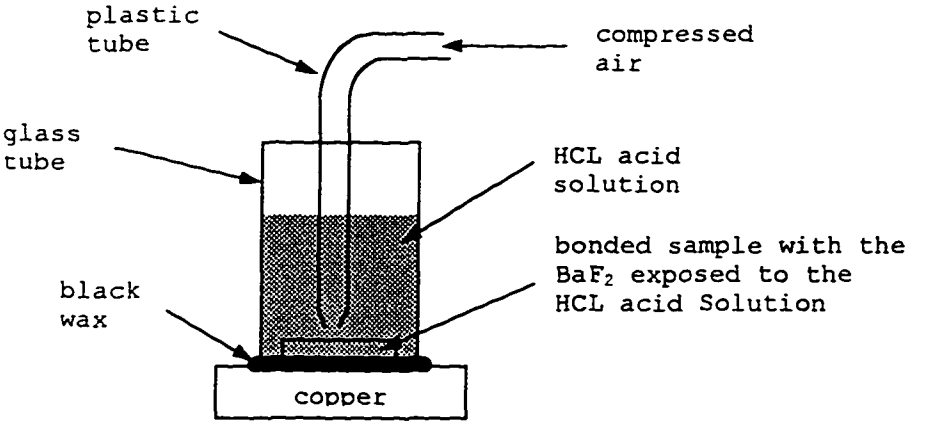


Figure 4.5 Compressed air is forced through the plastic tube aerating the BaF_2 substrate surface. The agitation provided by the aeration has decreased the substrate removal time to approximately five hours.

Compressed air is forced through a plastic tube resulting in an effervescent action at the BaF_2 substrate surface. This form of agitation has decreased the substrate

removal time from three days to five hours. Dissolving gases into the HCL acid solution may also be another reason for the improved etch rate. The solubility of BaF_2 increases with temperature [45]; therefore, the time required to complete the substrate removal process was again reduced by heating the HCL acid solution to 85°C. Using this new process, BaF_2 substrates can be removed in under five hours, facilitating epitaxial lift-off device research efforts.

Chapter Five describes the lift-off process used for laser fabrication, building on the information covered in this chapter.

References

[26] H. Holloway, W.H. Weber, E.M. Logothethis, A.J. Varga, and K.F. Yeung, "Injection Luminescence and Laser Action in Epitaxial PbTe Diodes", *Appl. Phys. Lett.* **21**, 5 (1972).

[40] S.P. Murarka, S.W. Hynmes, "Copper Metallization for ULSI and Beyond", *Crit. Rev. in Solid State and Material Sci.* **20** 87 (1995).

[41] ASM Handbook on Welding, Brazing and Soldering ; D.L. Olson, T.A. Siewert, S. Liu, et al..; Library of Congress-in-Production Data, **6** 127 (1993).

[42] K.W. Nill, J.N. Walpole, A.R. Calawa, and T.C. Harmon, "metal-Semiconductor Contacts on $Pb_{1-x}Sn_xTe$", Proceedings on The Physics of Semimetals and Narrow-Gap Semiconductors, Dallas, TX. March 20-21 1970.

[43] Lead Industries Association, Lead in Modern Industry, Lord Baltimore Press, 420 Lexington Avenue, New York, N..Y., 1952.

[44] M.T. Ludwick, Indium, The Indium corporation of America 60 E. 42nd St., NYC

[45] H. Stephen and T. Stephen, Solubilities of Inorganic and Organic Compounds, Vol. 1, Part 1, Pergamon Press NYC, NY, page 281, (1963).

Chapter 5

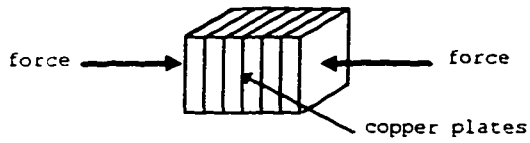
IV-VI Laser Fabrication Using Epitaxial Lift-Off

5.0 Introduction

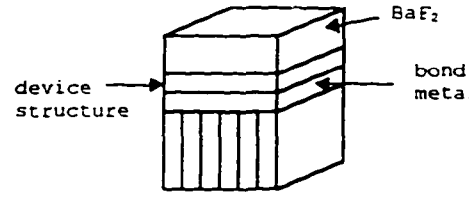
Epitaxial lift-off (ELO) techniques have been used to integrate dissimilar semiconductor materials, for example, gallium arsenide on silicon [46]. These hybrid integrations provide attributes that may not be attained by other means. As theoretically predicted in Chapter three, poor thermal properties of IV-VI semiconductor lasers can be improved by transferring the laser structure from its growth substrate to a copper heat sink [22]. This chapter describes the new ELO process used for hybrid thermal integration. Information presented in Chapter Four on epilayer bonding and substrate removal will be used as background information for critical processing steps needed in the new ELO device fabrication procedure.

5.1 Process Overview

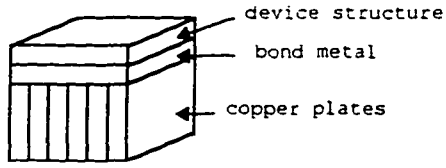
The following flow chart gives an overview of the new epitaxial lift-off process used in transferring the semiconductor device structure from its BaF_2 growth substrate to copper plates. The drawings below are not to scale.



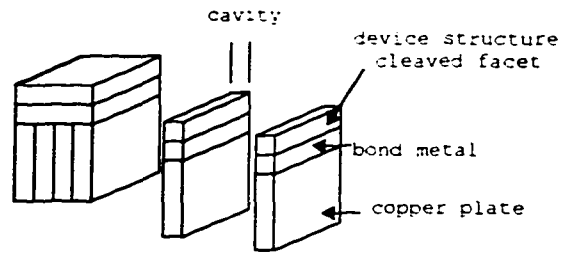
1) The copper plate assembly consists of a series of thin copper plates that are mechanically vised together.



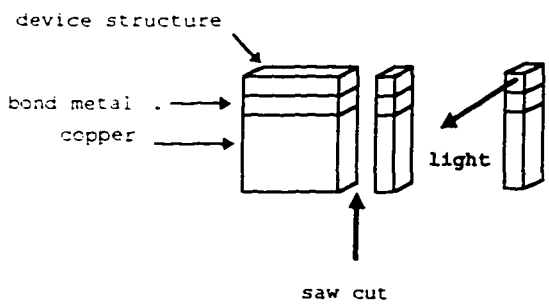
2) After the device is grown in the LPE furnace it is coated with a lead-tin alloy and bonded to a copper plate assembly as shown in this figure.



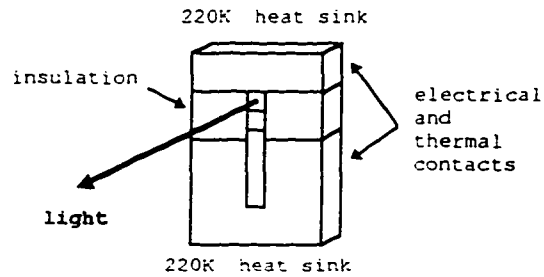
3) The BaF_2 substrate is removed using a hydrochloric acid solution which does not damage the device structure.



4) The mechanical vise is loosened allowing the individual plates to be separated which cleaves the laser structure forming the resonant cavity.



5) Sawing individual lasers from thin copper plates yields the final dimensions of the device.



6) Hybrid packaging of the laser forms both electrical and thermal contacts for the device.

Figure 5.1 Sequential flow chart of the new laser fabrication process. The new process takes advantage of epitaxial lift-off techniques to improve thermal properties of IV-VI semiconductor lasers.

The preceding flow chart gives a simplified overview of the new laser fabrication process that has been developed by the author. The details of each step will be covered in the remaining sections of this chapter along with discussion and reasoning.

5.2 Copper Plate Assembly and Cleaving Jig

The copper plate assembly is mechanically supported with the cleaving jig as shown below.

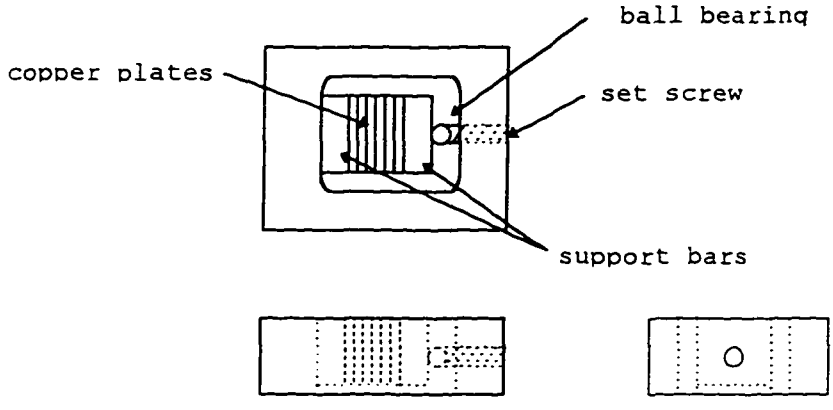


Figure 5.2 Assembled cleaving jig.

The copper plates are mechanically vised together between two support bars by using a set screw and ball bearing to maintain plate alignment. The jig is further processed by placing it on a milling machine to cut a flat top surface for device bonding. After milling, the jig is boiled in methanol 10-15 minutes to remove all grease that results from machining. Residual scratches deeper than 1 μm are

removed by lapping on an emery cloth before polishing with a 10% nitric acid slurry and felt pad. The nitric acid slurry aids in dissolving copper particles lodged in the felt pad, which could re-adhere to the polished surface adversely affecting the polishing procedure [47]. The polished surface ensures a uniform bond metal thickness, which resides between the copper and semiconductor surfaces; as described in section 5.6, the bonding layer uniformity reduces concerns about detrimental effects on the cleaving action. The jig is then ultrasonically agitated in deionized water with a surfactant to remove any residual polishing compound retained from lapping. After rinsing, the jig is submerged for 20 seconds in a 15% sulfuric acid solution followed by a deionized water rinse which removes oxides from the jig's polished surface. Oxide removal is necessary to allow coating of the jig with tin for the next step of processing.

Approximately 1 μm of tin is applied to the jig's surface by submerging it in an 82°C stannous chloride bath for five minutes. The tin atoms replace the copper surface by means of an ionic reduction, in this case the reducing agent is the copper substrate itself [48]. Thiourea is the ingredient used to capture the free copper ions. After the copper surface is replaced with tin, the process stops. The

electroless immersion plating solution used in this experiment was obtained from Transene, Rowely, MA. After removing the jig from the stannous chloride bath, it is rinsed thoroughly with deionized water. The resulting tin layer is an excellent surface for device structure bonding as it is easily wetted by several solders and pure metals. As mentioned in Chapter Four, several metallic media were investigated for their bonding properties. Successful epilayer bonding was attained by using pure tin and a 60-40 tin-lead alloy. The bond is considered successful if the BaF_2 substrate can be completely removed without critical delamination at either semiconductor to bond metal or bond metal to copper interfaces.

The freshly tin-coated jig is then lapped 5-10 times on a new damp felt pad to remove any tin dendrites that may have formed during the electroless tining process. Figure 5.3 shows a SEM micrograph of some tin dendrites which had formed on the jig's surface after a heating cycle.

Figure 5.3 SEM micrograph of tin dendrites that have formed on the jig's surface after a reflow heat cycle. The tin dendrites must be removed before further processing.

The tin dendrites are approximately 10 μm in height, which would prohibit the laser structure from forming a close contact with the jig's surface if the dendrites are not completely melted in the bonding heat cycle; the dendrites adversely affect the upcoming cleaving step. After dendrite removal, the jig is rinsed and ultrasonically agitated in deionized water to clean the surface before drying in an oven. The jig is ready for the bonding process, which will be described following a discussion of the laser structure metalization.

5.3 Laser Structure Preparation

Many attempts at bonding the semiconductor epilayer structure to the copper plate assembly resulted in failure. One failed technique included thermally depositing indium or 97-3 indium-silver on the jig and semiconductor surfaces, mating them, then applying pressure and heat. Appendix A contains details of this technique. Optical microscopy revealed the thermally evaporated bond metal was not adhering properly to the semiconductor surface. The thermal evaporation technique required the semiconductor structure be moved from the hydrogen filled LPE furnace to a vacuum chamber for metal deposition. During this move, the semiconductor surface was exposed to the atmosphere where

oxygen and other contaminants are present. This exposure is believed to significantly degrade adherence of the evaporated bonding metal to the epilayer. A technique used in eliminating the open air exposure is to apply the bond metal to the semiconductor surface as the last step of the LPE growth sequence.

A 60-40 tin-lead bonding medium was selected for LPE application to the IV-VI semiconductor surface for three distinct reasons. It forms a eutectic alloy, has a low melting temperature of 183°C resulting in minimal tin diffusion into the semiconductor [5], and both lead and tin are already present in the growth furnace minimizing contamination problems. The laser structure is coated by pulling the exposed epilayer surface underneath a well filled with a 60-40 tin-lead alloy and then allowing the metal to solidify. This method forms a good bond to the semiconductor surface; the integrity of the bond can be demonstrated by mechanically lapping to remove the BaF_2 substrate without critical delamination problems.

Using this method, an excess amount of bonding metal is placed on the surface of the epi-structure. One way of removing the excess tin-lead from the semiconductor surface is by placing it face down on a clean glass slide and

heating until the metal melts. The semiconductor structure is then pressed against the glass slide by applying a force with clean tweezers. This results in the excess metal being extruded around the edges of the sample. Experiments have shown a smooth bonding layer of tin-lead is left measuring approximately 500 μm following this step. After metal solidification, the extruded metal is cut off with a sharp razor blade. Another method of reducing the excess bond metal is by slowly removing it using a milling machine. The milling process could introduce defects into the semiconductor device structure; therefore, it is a less attractive method.

Using either metal reduction method, it is important to note the semiconductor surface is covered by metal or molten metal during the open air processing. It is believed this significantly slows oxygen or contaminate diffusion to the semiconductor-metal interface [50].

5.4 Epilayer Alignment and Semiconductor to Copper Plate Assembly Bond

Bonding the semiconductor structure to the copper plate assembly is begun by carefully aligning the semiconductor's crystal planes with the copper plate edges. One alignment method entails butting the BaF_2 substrate edge against a

copper spacer that is parallel to the copper plate edges. Figure 5.4 depicts the mechanical alignment of the semiconductor structure. Semiconductor alignment is necessary to achieve good parallel cleaves.

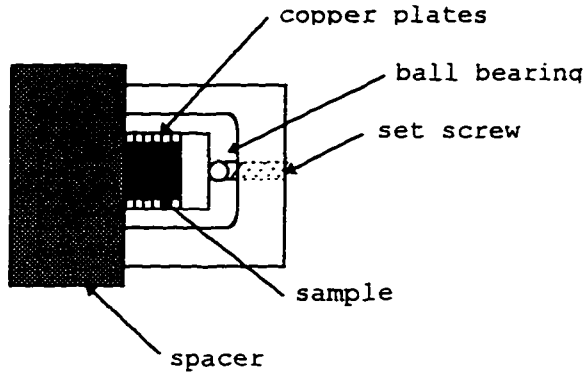


Figure 5.4 Mechanical alignment by using a copper spacer.

After careful alignment, a stainless steel piston weighing 323 grams is placed on the sample. The piston is held vertical by a concentric cylinder which is perpendicular to the jig surface. The piston applies 4.59 lb/in^2 to the sample; it forces the semiconductor structure closer to the copper surface as the bonding metal is melted. As shown in Figure 4.2, the excess bonding metal is extruded around the edges on the 1 cm^2 sample.

The bonding process includes two 10 minute heating cycles in which the jig temperature is elevated to approximately 240°C. Between the two heating cycles, the

bonding metal is allowed to solidify and the sample is checked to determine if proper alignment has been maintained. Figure 5.5 represents the bonding heat cycles.

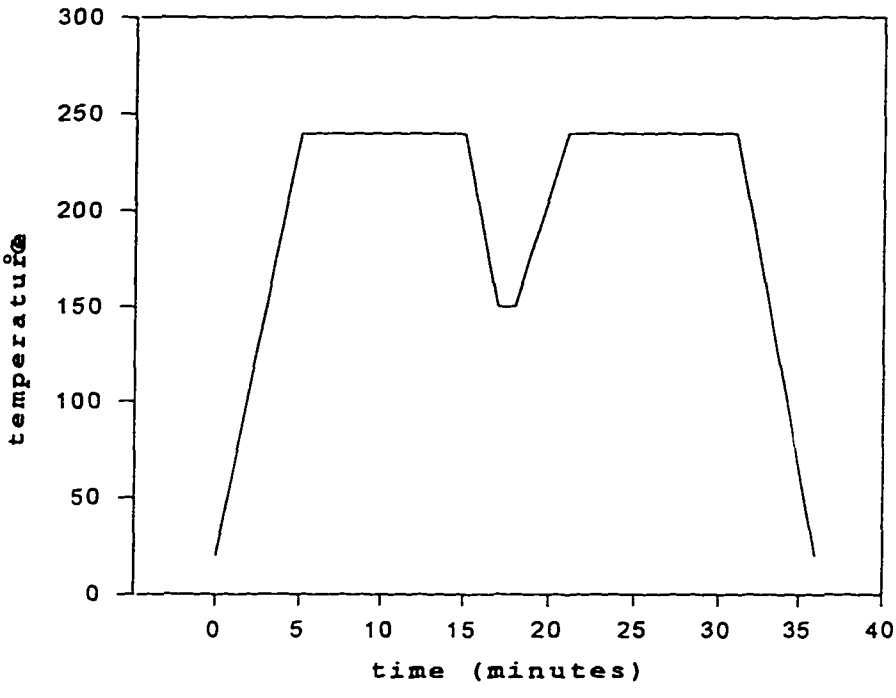


Figure 5.5 Bonding heat cycle used to adhere IV-VI epilayers to copper substrates using a 60-40 tin-lead medium.

Low amplitude vibrations applied during the heating cycle may reduce voids in the bond layer; ultrasonic processing has been demonstrated to reduce voids in IC circuit bonding applications [49].

5.5 Cleaving the Device Structure

After bonding and BaF_2 substrate removal (Chapter Four), the fragile device structure is held on the edge of the copper plate assembly, ready for cleaving. The cleaving process begins by removing the set screw and carefully lifting the copper plate assembly from the supporting jig. The individual plates are separated by a pivoting motion. Figure 5.6 illustrates this motion.

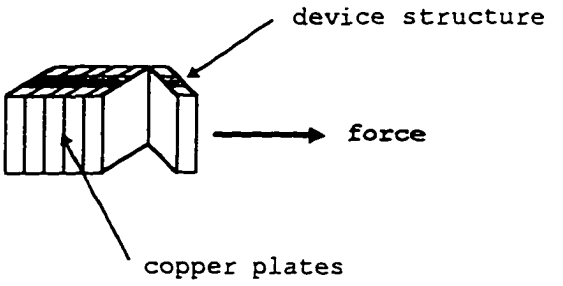


Figure 5.6 Pivoting motion used to cleave semiconductor laser structure.

This motion cleaves the device structure along the copper plate edges forming the Fabry-Perot resonant cavities needed for lasing. Note, the laser cavity dimensions can be changed by varying the copper plate thickness. If the device structure is aligned improperly during the bonding process, poor cleaves will result. Figure 5.7 is a SEM micrograph showing a zipper-like cleave along the copper plate edge resulting from improper epilayer alignment.

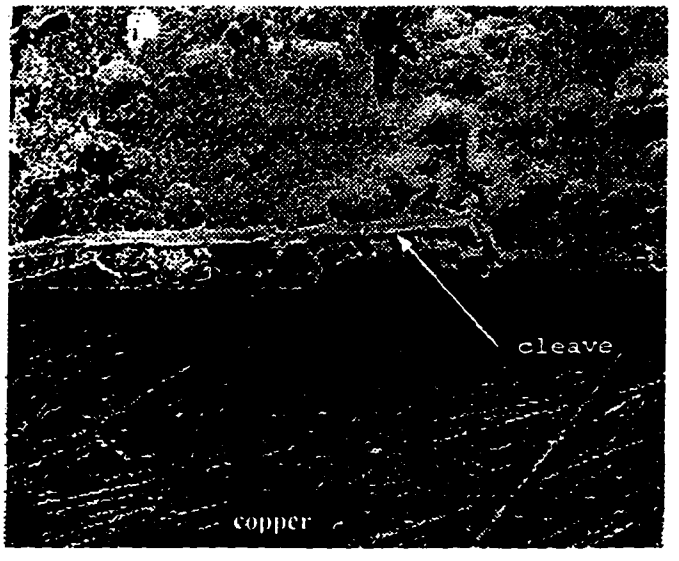


Figure 5.7 Poor epilayer alignment is demonstrated by the "zipper-like" cleave. Proper alignment should induce straight cleaves.

Pulling the copper plates apart cracks the metallic bonding layer while cleaving the device structure. For a straight cleave to propagate the length of the 1 cm^2 sample, the metallic layer must break smoothly. The quality of the metallic break is affected by its mechanicial hardness. See Table 4.1 for comparisons. Soft materials such as indium alloys suffer from "taffy-like" deformations when pulled

apart [50], making it neccessary to use a harder bonding medium. The mechanical hardness of 60-40 tin-lead is approximately three times that of tin and 97-3 indium-silver, making it a more favorable bonding medium to acheive good cleaves.

Two other cleaving motions were tried without success; both motions are depicted in the Figure 5.8.

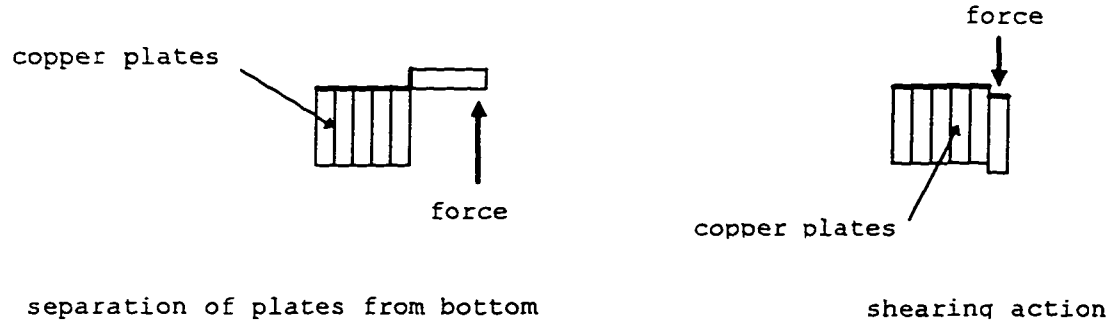


Figure 5.8 Unsuccessful cleaving techniques.

If the plates are separated from the bottom to top, SEM micrographs show the epilayer is lifted resulting in cracks in the epilayer. If the plates are forced down one at a time (sheared), the resulting edges are jagged along the individual copper plates. Figure 5.9 shows both unsuccessful cleaving scenarios.

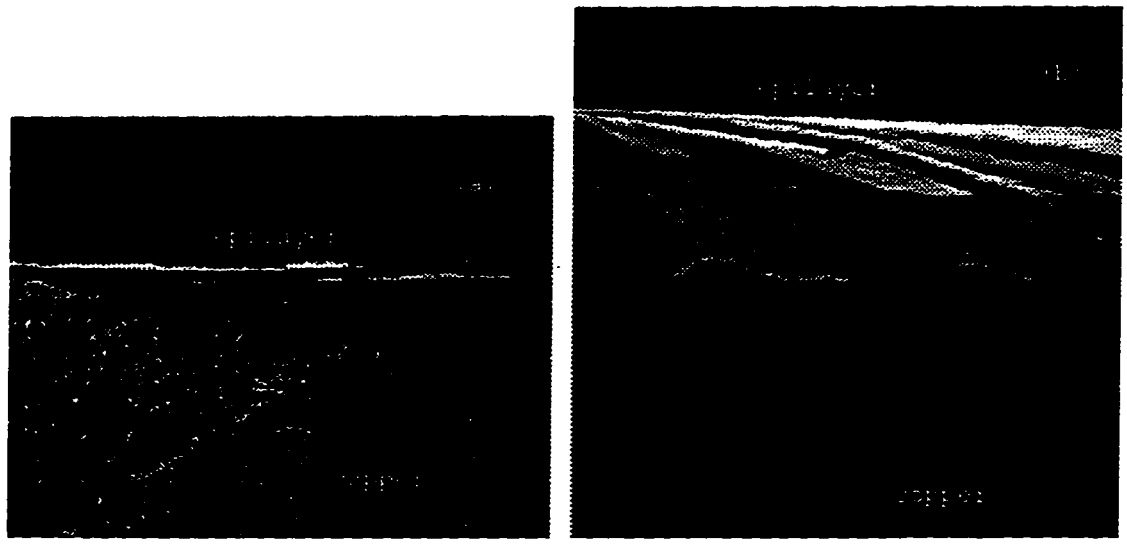


Figure 5.9 **Epilayer is cleaved by (a) a bottom separation motion and (b) a shearing motion. The bottom separation motion lifts and cracks the bonded epilayer. The shearing motion causes severe damage along the copper plate edge, rendering a useless structure.**

If the device structure is properly aligned and the pivoting motion is employed, good quality cleaves should result. Figure 5.10 is a series of SEM micrographs showing a 1 mm long cleaved section along the edge of a copper plate obtained using this technique.

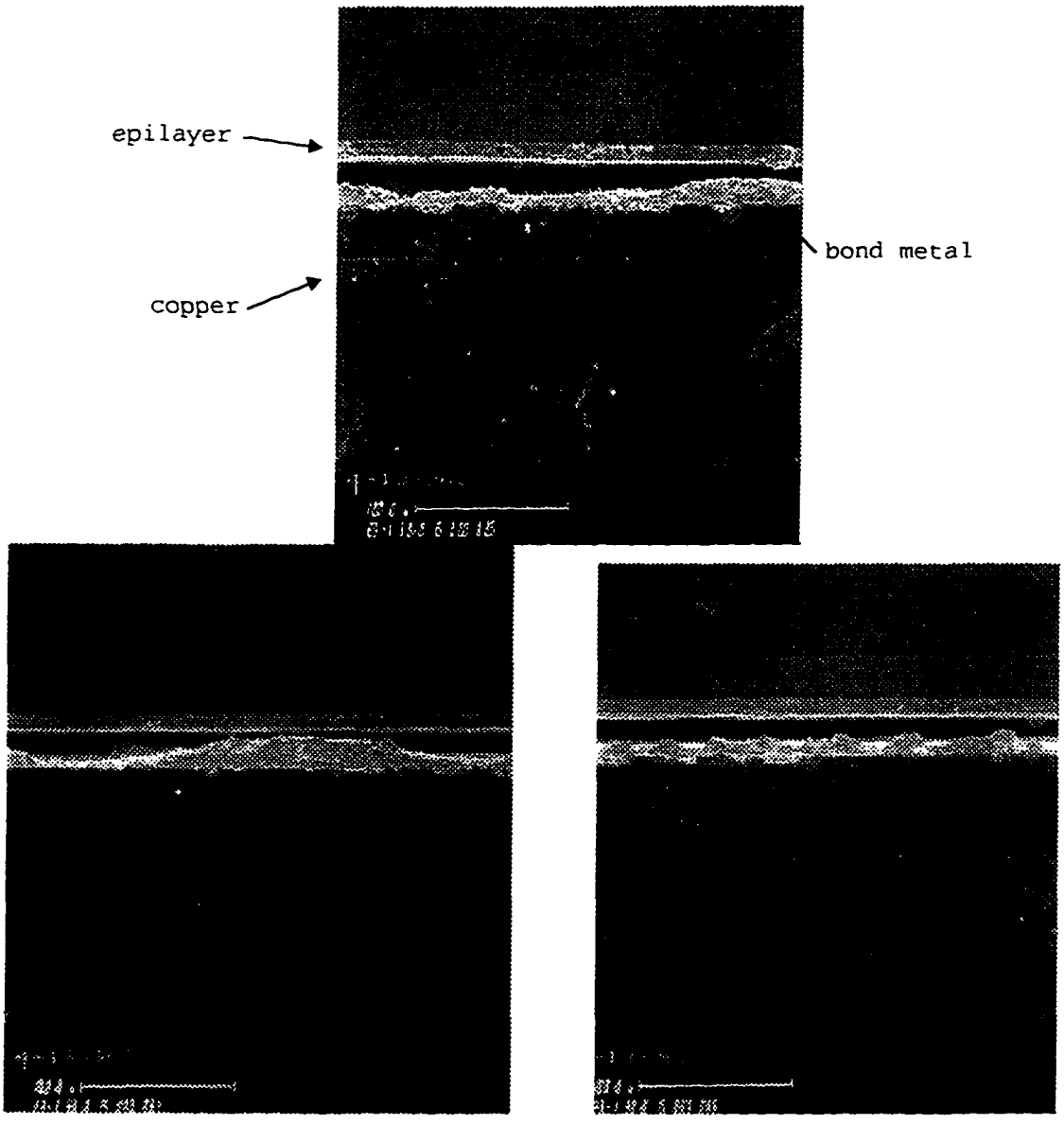


Figure 5.10 1 mm cleave along the copper plate edge.

Figure 5.10 shows an approximate 15 μm void between the epilayer and copper plate after the cleaving step. It is believed the voids are a result of oxidation that occurs while the bonding layer is melted in the open air. The voids may be reduced by reflowing the bonding metal in a hydrogen ambient furnace.

5.6 Bonding Layer Problems

Bonding layers consisting of 40% lead and 60% tin form near eutectic alloys with a melting temperature of 183°C. As described in an earlier section, the bonding material is applied in the LPE furnace after epilayer growth. Since the tin-lead alloy has a low melting temperature compared to PbSe and PbTe, interdiffusion should not be a problem. However, it was noted after conducting several experiments, by applying the bonding alloy above 350°C $Pb_{1-z}(Se_{1-y}Te_y)_z$, crystallites form in the bonding layer which prohibit the epilayer from forming a close contact with the copper surface. Figure 5.11 is a SEM micrograph showing the crystallites randomly fixed in the bond layer.

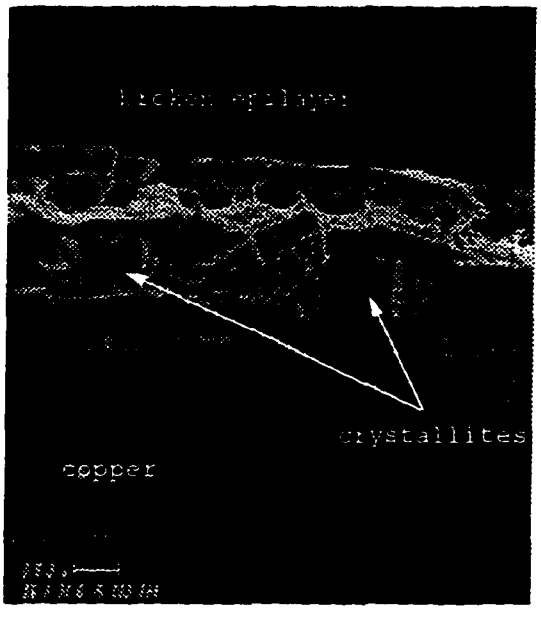


Figure 5.11 It is believed the $PbSe_{1-x}Te_x$ crystallites shown above formed during the application of the 60-40 tin-lead bonding layer. The bond layer was applied at 350°C.

The average dimension of the random crystallite is 10 μm. If two or more are stacked on each other the distance between epilayer and copper plate could be greater than 20 μm, too large for good cleavage. This problem was adressed by decreasing the exposure time of semiconductor surface to molten tin-lead alloy. Two measures were taken to decrease the exposure time; first placing the semiconductor sample underneath the molten tin-lead alloy approximately 20°C above its melting temperature and second cooling the LPE furnace rapidly by continually flowing air over its exterior.

5.7 Forming the Second Electrical Contact

Since lead and tin form good ohmic contacts to n-type IV-VI epilayers, the 60-40 tin-lead bonding layer is applied to the n-type epilayer, leaving the p-type epilayer surface exposed after BaF_2 substrate removal. The surface is then cleaned in preparation for application of a second thermal\electrical contact. Cleaning entails a brisk 10 second 30% HCL acid solution wash followed by a deionized water rinse to remove all BaF_2 precipitates. This is followed by a 10 second dip in a 50%/50% acetic acid-hydrogen peroxide bath. The sample is then rinsed thoroughly with deionized water before it is electroplated

with 1 μm of gold. It is unclear if gold forms an ohmic contact to p-type IV-VI semiconductors. It has been experimentally shown that platinum forms an ohmic contact to the p-type layer. The resulting gold layer is malleable and can be pressed against another gold coated copper plate forming a good thermal\electrical contact. Figure 5.12 shows the arrangement of the contacts.

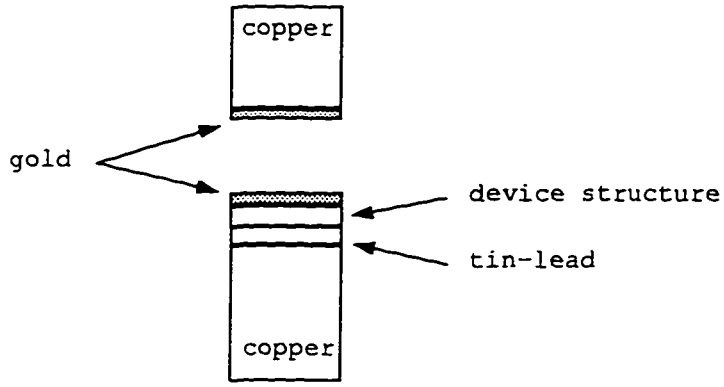


Figure 5.12 The two gold surfaces are pressed together to form a good thermal and electrical contact.

This chapter has provided details for the new ELO process used with IV-VI semiconductor laser structures grown on BaF_2 substrates. Table 5.1 gives a list of sequential processing steps in the new ELO technique. Appendix A discusses failed experiments; these failed experiments provide insight and reasoning for the presently developed process. Chapter Six presents x-ray data of lifted-off epilayers and current versus voltage plots for the resulting devices.

Table 5.1 Lift-Off Procedure

Step	Jig Preparation	Semiconductor Sample Preparation	Alignment and Bonding/Substrate Removal/Gold contact
1	clean sides of copper plates	grow device structure	allign coated sample on tinned jig
2	vise jig together	place it underneath a LPE well filled with a 60-40 tin-lead melt at 220°C, cool furnance rapidly with compressed air	place appropriate weight on sample
3	mill top surface of jig	reduce tin-lead by melting or milling	use heating cycle to bond sample to jig
5	lap on 400 and 600 emery cloth		after cooling, seal glass tube over sample
5	boil 10-15 min. in methanol		fill sealed tube with 30% HCL, heat to 85°C, provide aeration
6	lap on felt pad with 3 and 0.5 μm compound, reduce scratches to less than 1 μm		after substrate is removed, wash surface briskly with 30% HCL, followed by a brisk DI rinse
7	ultrasonically clean with surfactant for 10 min.		wash surface with 50-50 acetic acid-hydrogen peroxide, followed by a DI rinse
8	rinse well with DI water		electroplate gold on resulting surface
9	dip jig for 20 sec. in 15%		pattern using photolithograph,

	sulfuric acid solution		use bromine/ hydrobromine to etch IV-VI semicondouctor
10	rinse with DI water		
11	submerge jig for 5 min in 82°C stannous chloride bath for tin coating		
12	rinse well with DI water		
13	dry in 50°C oven for 1 hr.		

References

[5] Y.Nishijima and K.Shinohara, "Single-Mode PbSeTe laser with a Buried Heterostructure", *Applied Optics*. **32**, 4485 (1993).

[22] P.J. McCann and K.R. Lewelling, "Prospects of High Operating Temperature IV-VI Semiconductor Tunable Diode Lasers", *Optical Remote Sensing for Environmental and Process Monitoring Sym. Proc.* **VIP-55**, 26 (1995).

[46] E. Yablonlovitch, D.M. Hwang, T.J. Gmitter, L.T. Florez and J.P. Harbinson, "Van der Waals Bonding of GaAs Epitaxial Liftoff Films onto Arbitray Substrates", *Appl. Phy. Lett* **56**, 171 (1990).

[47] J.M. Steigerwals, S.P. Murarka, J. Ho, R.J. Gutmann, and D.J. Duquette, "Mechanisms of Copper Removal During Chemical Mechanical Polishing", *J. Vac. Sci. Technol. B* **13**, 2215 (1995).

[48] F.A. Lowenheim Electroplating McGraw-Hill, Inc., New York, p. 410 (1978).

[49] J.E. Krzansowski and N. Murdeshwar,"Defromation and Bonding Processes in Aluminum Ultrasonic Wire Wedge Bonding", *J. of Elect. Materials* **19**, 919 (1990).

[50] L.C. Chin, Y.W. Chen, and G. Matijaseric, "Advances in Bonding Technology for Electronic Packaging", *Journal of Elect. Packaging* **115**, 201 (1993).

Chapter 6

X-ray Diffraction Studies and Electrical Tests

6.0 Introduction

This chapter examines the quality of the lifted-off epi-structures by using x-ray diffraction techniques. Also, preliminary electrical tests on p-n junction devices are presented. Current versus voltage scans were performed to detect non-linear characteristics which indicate homo- or hetero-junction quality.

One concern about lift-off device processing is the damage incurred to the semiconductor during handling. II-VI semiconductor devices such as ZnSe LEDs and lasers suffer short life spans due to defects migrating into the active region of the emitter [51,52]; defects introduced into these soft II-VI semiconductors are partially a result of handling the device structure with tweezers. PbSeTe structures could possibly suffer similar problems; therefore, the IV-VI epi-structure is handled carefully during the lift-off procedure. Using careful handling procedures, induced defect levels are expected to be acceptable for device operation. This assumption can be investigated with future device lifetime studies; if there

is defect migration into the active region of the laser, device lifetime will be shortened.

6.1 X-ray Diffraction Studies [53]

After the BaF_2 substrate is removed, the crystal quality of the lifted-off epi-structure can be examined before the second electrical contact is made to the freshly exposed IV-VI epilayer. X-ray diffraction studies are capable means of evaluating the crystal's lattice parameter and quality.

Since the top epilayer consists primarily of lead a high Z number element with a thickness over 3 μm, the underlying layers cannot be studied with x-ray diffraction. Therefore, diffraction studies were primarily confined to epi-structures with the top epilayer being 3 μm or less. Figure 6.1 shows the (400) omega-2theta diffraction peaks of a 3% thallium doped $PbSe_{0.78}Te_{0.22}$ epilayer on BaF_2. This figure will be used for lifted-off sample comparison.

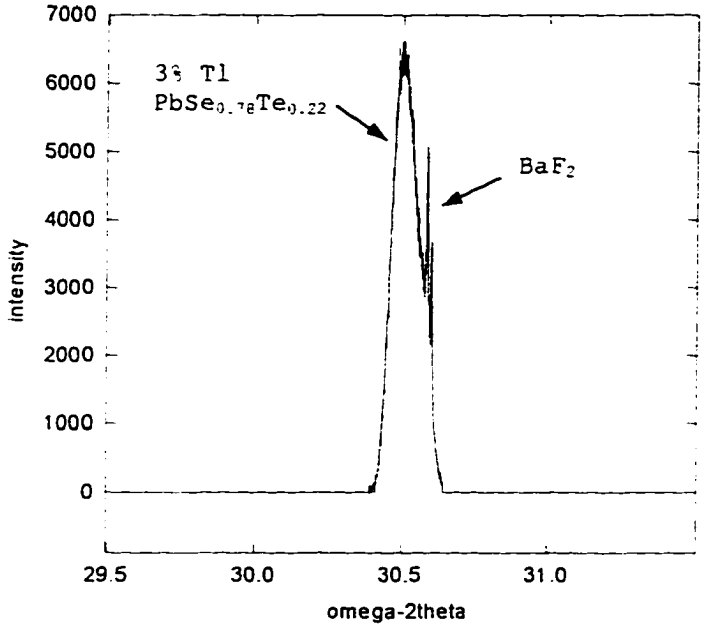


Figure 6.1 (400) omega-2theta x-ray diffraction peaks of a 3% Tl-doped epilayer grown on a BaF_2 substrate. The two peaks account for the epilayer and substrate. The rocking curves indicate a 0.23% lattice constant difference between the BaF_2 substrate and epilayer.

The two diffraction peaks shown in Figure 6.1 originate from the 3% Tl-doped $PbSe_{0.78}Te_{0.22}$ epilayer and the BaF_2 substrate. As illustrated in this figure, there is an apparent 0.23% lattice mismatch between the epilayer and the substrate. One theory suggests the mismatch is caused by the 3% Tl-doping to convert the epilayer to p-type material, while another proposes errors were made in

weighing the growth materials. The full-width-half-maximum (FWHM) of the epilayer peak is approximately 400 arcseconds. The FWHM of the BaF_2 is usually under 100 arcseconds. This indicates the epilayer quality is not as good as the BaF_2 substrate; a decrease in epilayer crystal quality is common.

Figure 6.2 shows the (400) omega-2theta diffraction peaks of a lifted-off p-n junction with the 3% Tl-doped epilayer exposed to the x-ray source. The Tl-doped ternary epilayer is grown first on the polished BaF_2 substrate followed by an un-doped ternary epilayer. After the sample is bonded face down to a rigid support and the BaF_2 substrate is removed, the Tl-doped epilayer is revealed for x-ray diffraction studies. Using a 15 minute LPE growth period, the Tl-doped epilayer is believed to be approximately 3 μm thick. Accurate epilayer thickness measurements could not be made on this sample as evenly stacked epilayers resulted in a structure without a step for measurement.

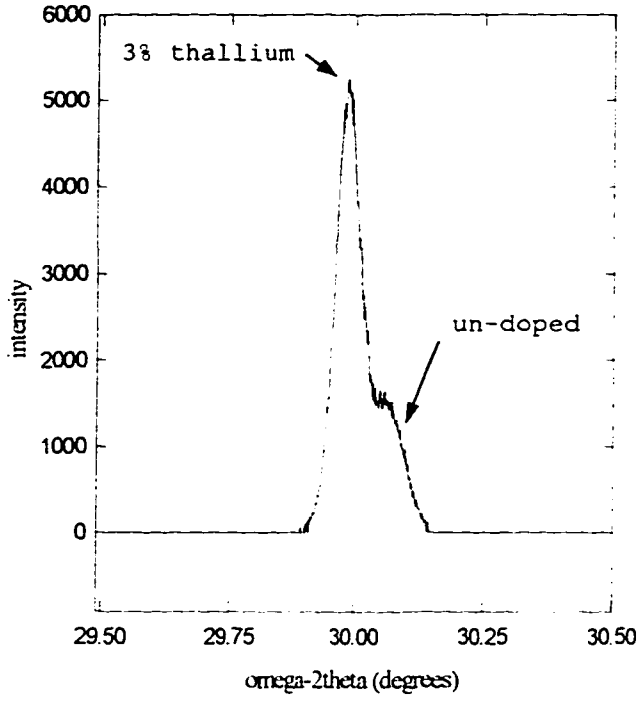


Figure 6.2 (400) omega-2theta diffraction peaks of $PbSe_{0.78}Te_{0.22}$ and 3% Tl-doped $PbSe_{0.78}Te_{0.22}$ epilayers. The strong peak results from the Tl-doped epilayer and the right shoulder peak is believed to result from the underlying un-doped epilayer.

The strong peak shown in Figure 6.2 is due to the Tl-doped ternary epilayer while the right shoulder peak is possibly due to the underlying un-doped ternary epilayer. This results in an approximate 0.3% lattice mis-match between the two epilayers. The two diffraction peaks observed in Figures 6.1 and 6.2 are believed to be linked to the Tl-doping or errors made when weighing the growth solution

materials. Figure 6.3 shows the diffraction peak of a p-n junction structure on a BaF_2 substrate.

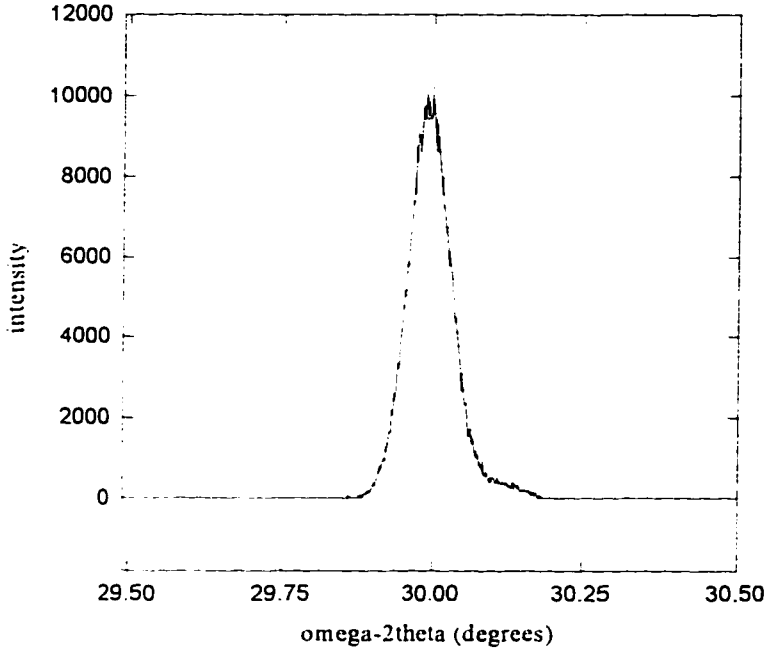


Figure 6.3 (400) omega-2theta diffraction peak of a p-n junction structure on a BaF_2 substrate.

Since the rocking curves vary from sample to sample, this indicates errors were probably made while weighing the melt materials.

Preservation of crystal integrity during lift-off processing is critical for good device performance. The FWHM of the lifted-off sample shown in Figure 6.2 is

approximately 300 arcseconds. This is comparable to the diffraction peak presented in Figure 6.1 in which the epilayer is not removed from the BaF_2 substrate. This indicates the lift-off procedure did not critically damage the semiconductor. The diffraction peak intensities are roughly the same for the samples examined in Figures 6.1 and 6.2. This also indicates the lift-off procedure did not significantly damage the IV-VI epilayer structure, suggesting that devices can be built using the described lift-off technique.

6.2 Electrical Testing

After the BaF_2 substrate is removed and the resulting surface is cleaned using a 30 second acetic acid/hydrogen peroxide rinse, a second electrical contact can be made to the device structure. A typical growth arrangement results in the p-type Tl-doped epilayer being grown on the bare BaF_2 substrate. Upon substrate removal, the Tl-doped layer is exposed and a gold layer is thermally evaporated or electroplated over the entire surface. In order to reduce the possibility of lead inclusions being present between the gold and tin/lead contacts which can form electrical shorts, the gold surface is patterned with an array of square dots using an ultraviolet photolithography process and etched using a bromine/hydrobromic acid solution. This

process results in a series of mesa structures with dimensions of 0.16 mm^2. Figure 6.4a is an optical photograph of an etched mesa structure in which voids are present. The voids can result from lead inclusions or other epilayer defects. Figure 6.4 is an optical photograph of an etched mesa structure without voids. This etched structure is appropriate for current versus voltage testing.

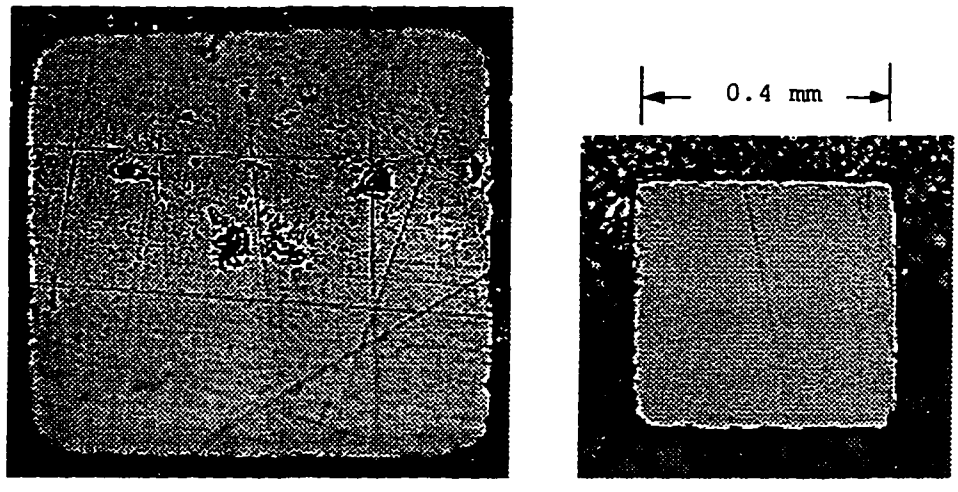


Figure 6.4 **Gold contacts made to the Tl-doped side of the p-n junction diode are shown above. Figure (a) shows a contact in which voids are present; Figure (b) shows a good contact without voids.**

The scratches observed in Figure 6.4 result from scratches in the polished BaF_2 substrate. The sample surface was covered with 4000 Å of gold applied by thermal evaporation.

After the gold contacts are patterned, the sample is ready for current versus voltage testing. The test equipment is capable of driving ± 100 mA through the sample. A separate voltmeter independently measures the voltage across the structure. Both current and voltage readings are displayed in real time and recorded in a file for further processing. Figure 6.5 shows the first non-linear I-V plot of a p-n junction diode structure processed in the described manner.

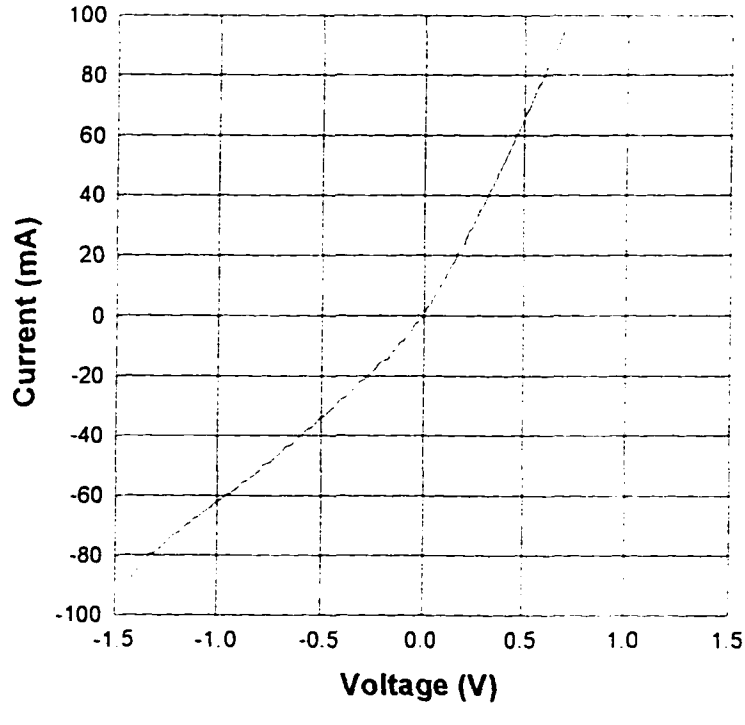


Figure 6.5 Current versus voltage plot of a p-n junction diode after processing with the new lift-off procedure. Note the non-linear nature of the plot which may indicate a leaky Schottky contact with the semiconductor.

The displayed curve is atypical for Schottky contacts or standard p-n junction diodes; this suggests there is parallel and series resistance in the lifted-off structure. Figure 6.6 is a proposed circuit model of the lifted-off structure.

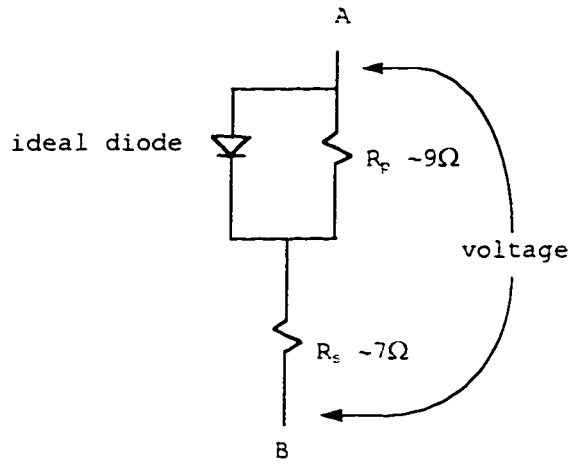


Figure 6.6 Proposed circuit model of the lifted-off diode structure. Resistance values were calculated from experimental data presented in Figure 6.5.

As current flows from B to A, there is a voltage drop across both R_p and R_s, as the ideal diode is in the off state. However, when current flows from A to B, the ideal diode is on and the effective resistance is only R_s. R_s is the contact resistance of the structure. The origin of R_p

unclear, it could result from semiconductor defects that thread through the device. Values for both R_s and R_p were calculated from data presented in Figure 6.5. This simplified model offers an explanation for the results observed in Figure 6.5 and appears typical of four samples processed in a similar manner.

These results strongly indicate that devices can be fabricated using the new lift-off technique. In order to fabricate efficient lead-salt lasers, several issues must be addressed; these issues will discussed in Chapter Seven.

References

[51] S. Guha, H. Cheng, M.A. Haase, J.M. DePuydt, J. Qiu. B.J. Wu, and G.E. Hofler, "⟨100⟩ Dark Line Defect in II-VI Blue-green Light Emitters", *Appl. Phys. Lett.* **65**, 801 (1994).

[52] D.B Eason, Z. Yu, W.C. Hughes, W.H. Roland, C. Boney, J.W. Cook, Jr., J.F. Schetzina, G. Cantwell, and C. Harsch, "High-brightness Blue and Green Light-emitting Diodes", *Appl. Phys. Lett.* **66**, 115 (1995).

[53] K.R. Lewelling and P.J. McCann, "Progress Towards Development of a Thermoelectically-Cooled Lead-Salt Semiconductor Laser", *Optical Remote Sensing for Environmental and Process Monitoring Sym. Proc.*, (to be published spring 1997).

Chapter 7

Conclusions and Future Work

7.1 Conclusions

As finite element models predicted in Chapter Three, there should be a 60° improvement in operating temperature when IV-VI semiconductor lasers are transferred from a thermally resistive lead-salt substrate and mounted on a copper heat sink. The improvement in operating temperature should allow continuous wave lasing use without the necessity of cryogenic cooling. Using the Feit et al. [1] laser that operated with a heat sink temperature of 203 K as a benchmark, there should be a 40° tuning range for infrared spectroscopic applications. The possibility of such a substantial improvement in operating temperature motivates this work and future work on this project.

SEM micrographs and optical photographs presented in Chapters Four and Five show that IV-VI epi-structures such as p-n junction diodes can be lifted-off their original BaF_2 growth substrate and transferred to a copper plate assembly for cleaving. Also, SEM micrographs show that cleaved edges needed for Fabry-Perot resonant cavities can be formed using the copper jig described in this dissertation. X-ray diffraction studies presented in

Chapter Six illustrate that the lift-off procedure can be used without degrading the crystal quality. The non-linear current versus voltage results in Chapter Six show the new fabrication method allows good electrical contacts to be placed on the device structure. The combined results are encouraging and offer substantial proof that the concept is sound and merits further work.

7.2 Future Work

Tests to be performed and issues that need to be addressed before commercialization of a IV-VI semiconductor laser fabricated using this new method are (1) eliminating voids present in the epilayer-to-copper bond medium, (2) improvement in the epilayer quality grown by LPE techniques, and (3) testing the cleaved laser structures by photoluminescence and electroluminescence experiments.

Bonding voids may be reduced by melting the bonding medium in a hydrogen ambient furnace to reduce oxidation. Another possible solution to the void problem is to reduce the surface area of the semiconductor sample by breaking it into smaller pieces. This will decrease the likelihood of voids being present between the sample and copper surface.

The BaF_2 substrate quality needs to be improved before long lived devices can be grown using LPE methods. The two substrate quality problems that need to be addressed are reduction in off axis sawing to produce true (100) growth surfaces and elimination of large grains in the bulk BaF_2. Achieving these results will require considerable work with the BaF_2 substrate vendor.

Figure 7.1 is a schematic showing the experimental setup for photoluminescence testing of the cleaved laser structure.

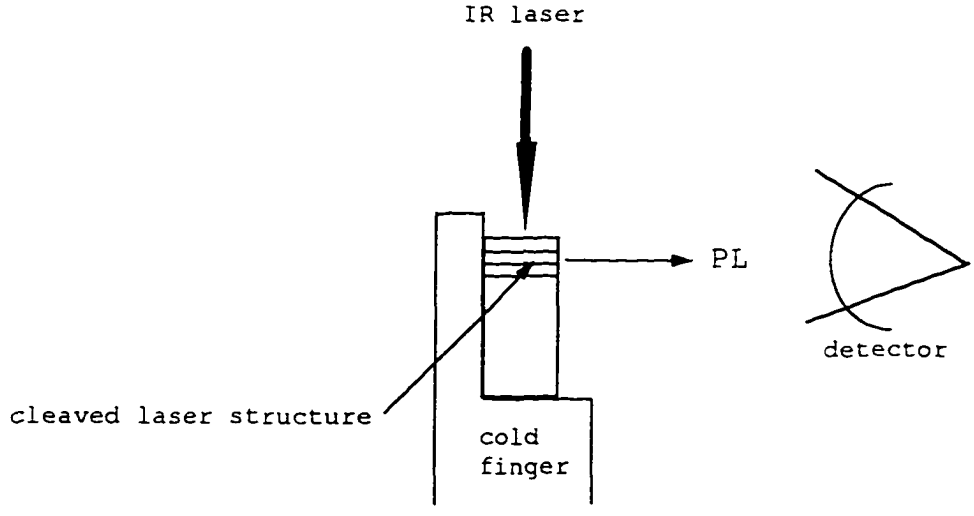


Figure 7.1 **Test arrangement for photoluminescence experiments on lifted-off IV-VI semiconductor laser structures. This test will provide information needed in further design of the new laser.**

Calculations predict the pump laser power must be at least 1 W to generate a detectable photoluminescence signal. Implementation of the techniques described previously could produce a marketable photo-pumped device and allow usage in a host of high temperature applications. This arrangement would not require the bonding layer be void free, therefore, simplifying the fabrication process. The photo-pumped laser could be sold in an effort to develop a good market base while the electroluminescence laser is under further development. The major contribution of this work is the feasibility of producing higher operating temperature lead-salt semiconductor lasers that will revolutionize remote infrared spectroscopic applications ranging from smoke stack pollution detection to automobile exhaust monitoring. With the need for operational cryogenic cooling removed, user friendly infrared spectrometers will allow medical doctors to diagnose certain disease by means of non-invasive breath analysis [54]. With a 60° boost in operating temperature, the potential applications are yet to be imagined.

References

[1] Z.Feit, D.Kostyk, R.J.Woods, and P.Mak, "Single-Mode Molecular Beam Epitaxy Grown PbEuSeTe/PbTe Buried Heterostructure Diode Lasers for CO_2 High-Resolution Spectroscopy". *Appl.Phys.Lett.* **58**, 343 (1991).

[54] P.J. McCann and W. Potter, Proposal for a Improved Tunable Diode Lasers for Helicobacter Pylori Infection Breath Testing.

Compiled References

[1] Z.Feit, D.Kostyk, R.J.Woods, and P.Mak, "Single-Mode Molecular Beam Epitaxy Grown PbEuSeTe/PbTe Buried Heterostructure Diode Lasers for CO_2 High-Resolution Spectroscopy". *Appl.Phys.Lett.* **58**, 343 (1991).

[2] P.J.McCann and L.Li, "$Pb_{1-x}Sn_xSe_{1-y}Te_y$ Alloys Lattice Matched with BaF_2: A New Material System for Far-Infrared Device Fabrication", International Device Research Symposium, Charlottesville, VA. December 1-3, 1993.

[3] P.J. McCann, J. Fuchs, Z.Feit, and C.G.Fonstad, "Phase Equilibria and Liquid Phase Epitaxy Growth of PbSnSeTe Lattice Matched to PbSe", *J.Appl.Phys.* **62**, 2994 (1987).

[4] W.W.Anderson, "Gain-Frequency-Current Relations for PbSnTe Double- Heterostructures", *IEEE J. Quantum Electron* **QE-13**, 532 (1977).

[5] Y.Nishijima and K.Shinohara, "Single-Mode PbSeTe laser with a Buried Heterostructure", *Applied Optics.* **32**, 4485 (1993).

[6] P.S. Lee, R.M. Schreck, F.A. Hare, and J.J. McGrath, "Biomedical Applications of Tunable Diode Laser Spectrometry", *Annals of Biomed. Eng.* **22**, 120 (1994).

[7] R.Schatz and C.G.Betha, "Steady State Model for Facet Heating Leading to Thermal Runaway in Semiconductor Lasers", *J.Appl.Phys.* **76**, 2509 (1994).

[8] P.J.McCann and C.G.Fonstad, "Growth of $PbSe_{0.78}Te_{0.22}$ Lattice-Matched with BaF_2", *Thin Solid Films* **227**, 185 (1993).

[9] P.J.McCann and D.Zhong, "Liquid Phase Growth of $Pb_{1-x}Sn_xSe_{1-y}Te_y$ Alloys Lattice Matched with BaF_2", *J.Appl.Phys.* **75**, 1145 (1994).

[10] P.J.McCann, S.K.Aanegola, J.E.Furneaux, "Growth and Characterization of Thallium- and Gold-Doped $PbSe_{0.78}Te_{0.22}$ Layers Lattice Matched with BaF_2 Substrates", *Appl.Phys.Lett.* **65**, 2185 (1994).

[11] E.Yablonovitch, K. Kapon, T.J.Gmitter, C.P. Yun, and R.Bhat, "Double Heterostructure GaAs/AlGaAs Thin Film

Diode Lasers on Glass Substrates", *IEEE Photon. Tech. Lett.* **1**, 41 (1989).

[12] E.Yablonovitch, T.J. Gmitter, J.P. Harbison, and R. Bhat, "Extreme Selectivity in the Lift-Off of Epitaxial GaAs Films", *Appl.Phys.Lett.* **51**, 2222 (1987).

[13] X.Li, I.W. Tao, and W.I. Wang, "Flip-Chip Transfer of ZnSSe/ZnSe/CdZnSe LED Films", *Electronics Letts.* **31**, 491 (1995).

[14] P.J. McCann, L.Li, J.E.Furneax, and R. Wright, "Optical Properties of Ternary and Quaternary IV-VI Semiconductor Layers on (100) BaF_2 Substrates", *Appl.Phys.Lett.* **66**, 1355 (1995).

[15] G.Pratt.Jr., "Vacancy and Interstitial States in the Lead Salts", *J. Nonmetals* **1**, 103 (1973).

[16] I. Chao, S. Yuan, and P.J. McCann, "Growth and Characterization of PbSeTe/PbSnSeTe/PbSeTe Double Heterostructures", International Device Research Symposium, Charlottesville, VA., December 6-8, 1995. Published in Proceedings 1995 International

Semiconductor Device Research Symposium, Volume II, P.505, University of Virginia, Charlottesville, VA (1995).

[17] P.J. McCann "High Temperature Semiconductor Diode Laser", US Patent # 5,454,002, Issued Sept. 26, 1995.

[18] P.J. McCann, C.G. Fonstad, "Auger Electron Spectroscopic Analysis of Barium Fluoride Surfaces Exposed to Selenium Vapor", *J. Electron. Mater.* **20**, (1991) 915.

[19] P.J. McCann, "The Role of Substrate Surface Reactions in Heteroepitaxy of PbSe on BaF_2", *Mater. Res. Soc. Symp. Proc.* **221**, 289 (1991).

[20] P.J. McCann, S.K. Aanegola, "The Role of Graphite Boat Design in Liquid Phase Epitaxial Growth of $PbSe_{0.78}Te_{0.22}$ on BaF_2", *J. Crystal Growth* **141**, 376 (1994).

[21] P.J. McCann, "The Effect of Composition Dependent Lattice Strain on the Chemical Potential of Tellurium in $Pb_{1-x}Sn_xSe_{1-y}Te_y$ Quaternary Alloys", *Mat. Res. Soc Symp. Proc.* **311**, 149 (1993).

[22] P.J. McCann and K.R. Lewelling, "Prospects of High Operating Temperature IV-VI Semiconductor Tunable Diode Lasers", *Optical Remote Sensing for Environmental and Process Monitoring Sym. Proc.* **VIP-55**, 26 (1995).

[23] B.G.Streetman Solid State Electronic Devices Printice-Hall, Inc., Englewood Cliffs, New Jersey 07632, 1990.

[24] G.Bauer and H.Krenn Handbook of Optical Constants of Solids, Academic Press, Inc., pp. 517-523, 535-546, 1985.

[25] M.Oron, A.Zussman, and A.Katzir, "Dielectric Constants and Optical Confinement in Homostructure PbSnTe Diode Lasers", *Infrared Phys.* **22**, 317, (1982).

[26] H. Holloway, W.H. Weber, E.M. Logothethis, A.J. Varga, and K.F. Yeung, "Injection Luminescence and Laser Action in Epitaxial PbTe Diodes", *Appl. Phys. Lett.* **21**, 5 (1972).

[27] C.Kittel, Introduction to Solid State Physics John Wiley and Sons, Inc., page 308, 1986.

[28] H.Brugger, P.Epperlein, "Mapping of Local Temperatures on Mirrors of GaAs/AlGaAs Laser Diodes", *Appl. Phys. Lett.* **56**, 1049 (1990).

[29] S.Todoroki, M.Sawai, and K.Aikj, "Temperature Distribution Along the Striped Active Region in High-Power GaAlAs Visible Lasers", *J. Appl. Phys.* **58**, 1124 (1985).

[30] W.Tang, H.Rosen, P.Vetttiger, and D.Webb,"Evidence for Current-Density-Induced Heating of AlGaAs Single-Quantum-Well Laser Facets", *Appl. Phys. Lett.* **59**, 1005 (1991).

[31] F.Gfeller, and D.Webb, "Degradation and Lifetime Studies on High-Power Single-Quantum-Well AlGaAs Ridge Lasers", *J. Appl. Phys.* **68**, 14 (1990).

[32] R.Schatz, and C.Bethea, "Steady state Model for Facet Heating Leading to Thermal Runaway in Semiconductor Lasers", *J. Appl. Phys.* **76**, 2509 (1994).

[33] Z.Feit, M.McDonald, R.Woods, V.Archambault, and P.Mak, "Low Threshold PbEuSeTe/PbTe Separate Confinement

Buried Heterostructure Diode Lasers", *Appl. Phys. Lett.* **68**, 738 (1996).

[34] B.Spanger, U.Schiessl, A.Lambrecht, H.Bottner, and M.Tacke, "Near-Room-Temperature Operation of $Pb_{1-x}SrSe$ Infrared Diode Lasers Using Molecular Beam Epitaxy Technique", *Appl. Phys. Lett.* **53**, 2582 (1988).

[35] R.Rosman, and A.Datzir, "Lifetime Calculations for Auger Recombination in Lead-Tin-Telluride", *IEEE J. of Quantum Elec.* **QE-18**, 814 (1982).

[36] Z.Feit, R.Woods, D.Kostyk, and W. Jalenak, "Low-Threshold PbEuSeTe Double-heterostructure Laser Grown by Molecular Beam Epitaxy", *Appl. Phys. Lett.* **55**, 16 (1989).

[37] Z.Feit, D.Kostyk, R.Woods, and P.Mak, "Molecular Beam Epitaxy-Grown Separate Confinement Buried Heterostructure PbEuSeTe-PbTe Diode Laser", *IEEE Phont. Tech.* 7, 1403 (1995).

[38] Z.Feit, D.Kostyk, R.Woods, and P Mak, "PbEuSeTe buried Heterostructure Lasers Grown by Molecular-Beam Epitaxy", *J. Vac. Sci. Tech. B* **8**, 200 (1990).

[39] K.R. Lewelling and P.J. McCann, "Finite Element Modeling Predicts Possibility of Thermoelectricically-Cooled Lead-Salt Diode Lasers", *IEEE Phont. Tech.*, to be published in March 1997.

[40] S.P. Murarka, S.W. Hynmes, "Copper Metallization for ULSI and Beyond", *Crit. Rev. in Solid State and Material Sci.* **20** 87 (1995).

[41] ASM Handbook on Welding, Brazing and Soldering ; D.L. Olson, T.A. Siewert, S. Liu, et al..; Library of Congress-in-Production Data, **6** 127 (1993).

[42] K.W. Nill, J.N. Walpole, A.R. Calawa, and T.C. Harmon, "metal-Semiconductor Contacts on $Pb_{1-x}Sn_xTe$", Proceedings on The Physics of Semimetals and Narrow-Gap Semiconductors, Dallas, TX. March 20-21 1970.

[43] Lead Industries Association, Lead in Modern Industry, Lord Baltimore Press, 420 Lexington Avenue, New York, N..Y., 1952.

[44] M.T. Ludwick, Indium, The Indium corporation of America 60 E. 42nd St., NYC

[45] H. Stephen and T. Stephen, Solubilities of Inorganic and Organic Compounds, Vol. 1, Part 1, Pergamon Press NYC, NY, page 281, (1963).

[46] E. Yablonlovitch, D.M. Hwang, T.J. Gmitter, L.T. Florez and J.P. Harbinson, "Van der Waals Bonding of GaAs Epitaxial Liftoff Films onto Arbitray Substrates", *Appl. Phy. Lett* **56**, 171 (1990).

[47] J.M. Steigerwals, S.P. Murarka, J. Ho, R.J. Gutmann, and D.J. Duquette, "Mechanisms of Copper Removal During Chemical Mechanical Polishing", *J. Vac. Sci. Technol. B* **13**, 2215 (1995).

[48] F.A. Lowenheim Electroplating McGraw-Hill, Inc., New York, p. 410 (1978).

[49] J.E. Krzansowski and N. Murdeshwar,"Defromation and Bonding Processes in Aluminum Ultrasonic Wire Wedge Bonding", *J. of Elect. Materials* **19**, 919 (1990).

[50] L.C. Chin, Y.W. Chen, and G. Matijaseric, "Advances in Bonding Technology for Electronic Packaging", *Journal of Elect. Packaging* **115**, 201 (1993).

[51] S. Guha, H. Cheng, M.A. Haase, J.M. DePuydt, J. Qiu. B.J. Wu, and G.E. Hofler, "⟨100⟩ Dark Line Defect in II-VI Blue-green Light Emitters", *Appl. Phys. Lett.* **65**, 801 (1994).

[52] D.B Eason, Z. Yu, W.C. Hughes, W.H. Roland, C. Boney, J.W. Cook, Jr., J.F. Schetzina, G. Cantwell, and C. Harsch, "High-brightness Blue and Green Light-emitting Diodes", *Appl. Phys. Lett.* **66**, 115 (1995).

[53] K.R. Lewelling and P.J. McCann, "Progress Towards Development of a Thermoelectically-Cooled Lead-Salt Semiconductor Laser", *Optical Remote Sensing for Environmental and Process Monitoring Sym. Proc.*, (to be published spring 1997).

[54] P.J. McCann and W. Potter, Proposal for a Improved Tunable Diode Lasers for Helicobacter Pylori Infection Breath Testing.

Appendix A

A.1 A Less Successful Bonding Technique

Bonding the LPE grown IV-VI epilayer to a copper cleaving jig was first accomplished by using Indium and Indium/Silver (In/Ag) eutectic media. Lead and tin were also used in subsequent experiments following the same procedure describe in this appendix. The $In_{97\%}/Ag_{3\%}$ (by atomic weight) bonding compound has provided comparable results to In alone. The first experiments using the In/Ag eutectic were performed as follows. In and Ag slugs are weighted, melted, and stirred in a graphite container prior to loading into a vacuum system for deposition. The In/Ag alloy is thermally evaporated on the jig and IV-VI sample, under high vacuum ($\approx 5X10^{-7}$ torr). After the first few experiments following this procedure, it was discovered that the In/Ag eutectic material was not depositing in the right ratio due to partial pressure differences. Therefore, the deposition steps were modified to achieve the proper ratio.

If correct thickness In and Ag layers are deposited, the sought after eutectic alloy will be formed due to diffusion of Ag into the In when the In layer is re-heated

to melting temperatures in the bonding process. Figure A.1 shows the bonding layers, jig, and epilayer in correct position for the bonding procedure.

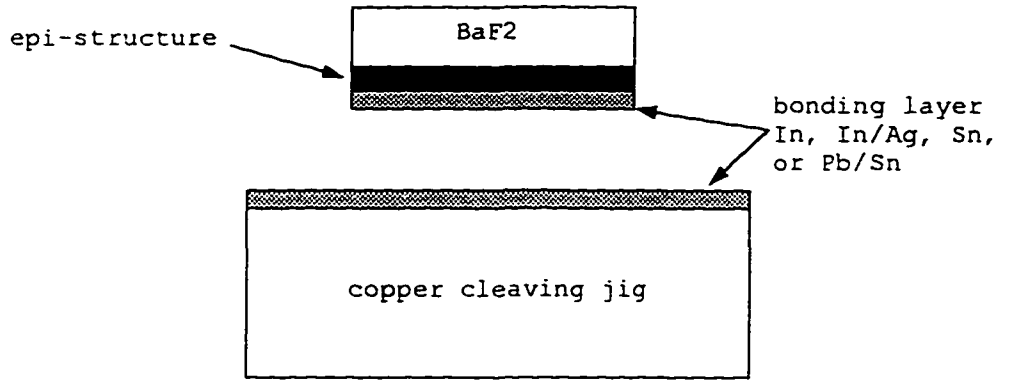


Figure A.1 Layer layout of bonding medium prior to alignment and re-heating to melt the thermally deposited In, In/Ag, Pb, or Sn.

After the bonding layers are applied to the sample and jig, the sample is aligned on the cleaving jig using the fixture shown in Figure A.2.a. A small mechanical pressure is applied to the sample to stabilize and aid in bonding. One method of applying the needed pressure is by using an apparatus shown in Figure A.2.b. The sample/jig is then placed under vacuum (≈5 mtorr) and heated with a high intensity lamp. While the sample/jig is being heated, it is believed that ultrasonic agitation can be applied to reduce voids in the metal bond; ultrasonic vibration has

previously been used in semiconductor contact application [1] to reduce voids. Figure A.2.c shows the setup used to heat the jig/sample.

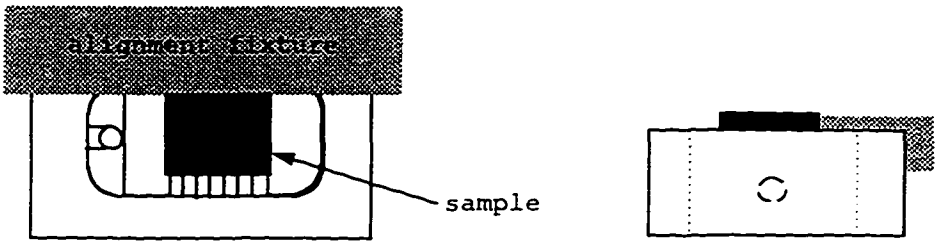


Figure A.2.a This fixture is used to align the semiconductor sample to edges of the copper plates. This is accomplished by mechanically butting the sample against the lip of the copper alignment fixture.

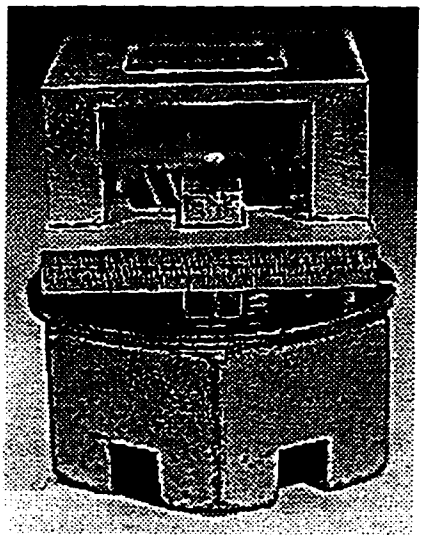


Figure A.2.b The pressure assembly shown above is used to clamp the metalized sample to the coated copper cleaving jig. The large nut at the bottom is tightened to force the sample closer to the jig's surface. The cross members are supported by springs to allow for even pressure to be applied as the metal melts. Occasionally LPE lead droplets prohibit the sample from lying flat on the cleaving jig surface. As the droplets melt, the springs force the sample evenly onto the cleaving jig forming a consistent bonding layer thickness.

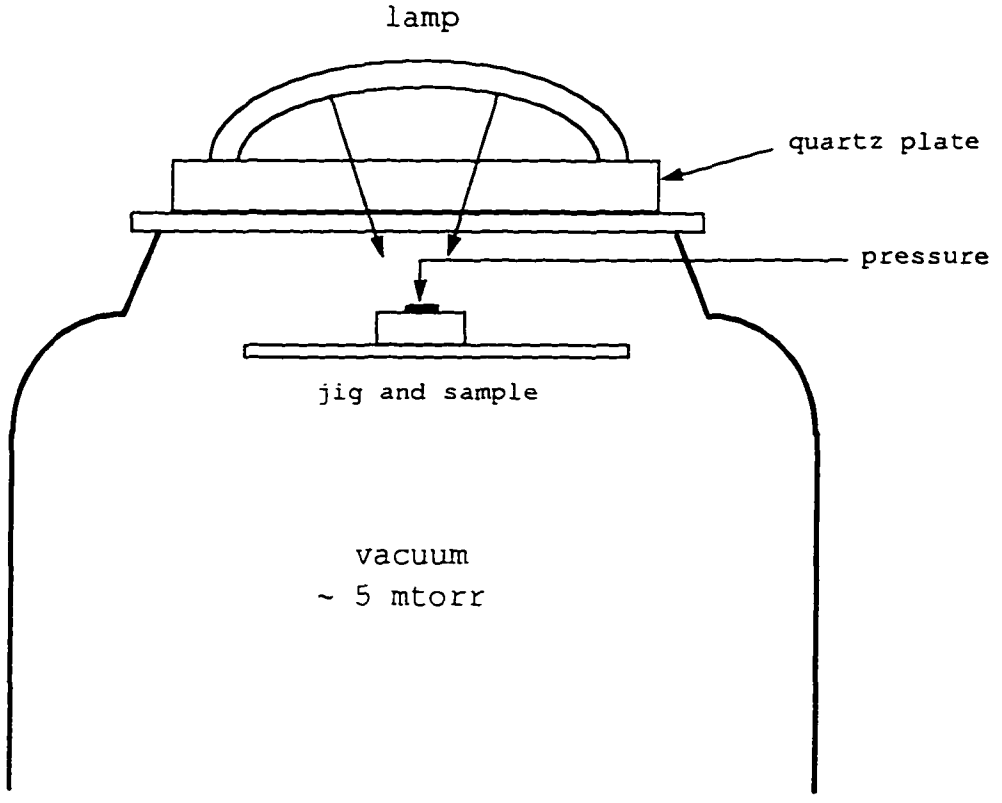


Figure A.2.c After the vacuum chamber is pumped to approximately 5 mtorr, the layers are melted with a high intensity lamp to form a bond. The indium layers melt first, readily dissolving the thin silver layers to form the desired eutectic. Similar eutectics can be formed with gold/indium and gold/tin. The hot jig/sample is left under vacuum until cooled to room temperature.

The 5 mtorr vacuum may aid in the bonding process; the metal layer thickness is theoretically reduced by creating a pressure gradient around the edges of the sample. The

vacuum pulls metal from between the jig and sample, allowing for closer contact.

The temperature cycle for this bonding procedure is shown in figure A.3. It is believed that ultrasonic agitation applied during this heating cycle will reduce voids in the bonding alloy. Experiments to investigate this idea were difficult to construct as the sample is in a vacuum environment. Also, application of agitation would risk losing sample alignment with the copper plates. Due to these reasons, the investigation was not pursued.

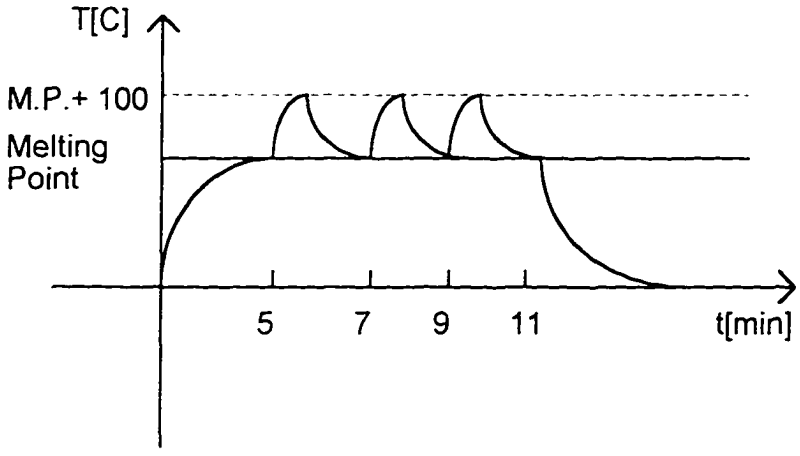


Figure A.3 The heat cycle used to bond the semiconductor sample to the copper cleaving jig.

After the bonding alloy solidifies, the bonded sample is allowed to cool to room temperature under vacuum to reduce oxidation.

Upon removal of the bonded sample from the vacuum, the edges of the BaF_2 substrate are sealed with black wax to protect the metal surfaces from the hydrochloric acid solution used in dissolving the substrate. Chapter Four explains the substrate removal process in detail.

Over 80% of the samples bonded using the In/Ag eutectic layer method described in this appendix suffered critical delamination problems. The poor success rate curtailed aggressive experiments using this bonding method. It was concluded that the bonding method may work, but different alloys must be used such as In/Ag and Sn/Ag. Unwanted oxides formed on the thermally evaporated layers when the sample and cleaving jig were removed from the vacuum for alignment. The oxides prohibit good bonding and may be the origin of unwanted voids. The gold alloys mentioned above are arranged with the gold layer exposed to the room atmosphere; gold is less reactive with ambient oxygen than indium or tin. This bonding alloy change may reduce the delamination problems suffered by the In/Ag alloy.

References

[49] J.E. Krzansowski and N. Murdeshwar,"Deformation and Bonding Processes in Aluminum Ultrasonic Wire Wedge Bonding", *J. of Elect. Materials* **19**, 919 (1990).