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MICROFABRICATION OF ACTIVE PHOTONIC DEVICES

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Abstract

This thesis focuses on the optimization of microfabrication processes used in photonic devices, specifically GaAs wet etching and silicon thermal oxidation. These processes are important for defining patterns and building material platforms for device fabrication.

In the first part, wet chemical etching of GaAs was optimized to achieve controlled material removal in both nanometer and micrometer ranges. Different etching recipes based on citric acid and hydrogen peroxide were tested, and their etch rates were measured. The process also includes the optimization of photolithography, particularly the coating conditions and exposure parameters. The results show that wet etching is a reliable method for controlling etch depth in GaAs substrates, while minimizing surface damage, which is important for near-surface quantum dot structures.

In the second part, dry thermal oxidation of silicon and silicon-on-insulator (SOI) substrates was studied to develop a multilayer structure consisting of $Si/SiO_2/YSZ/CeO_2$. The oxidation conditions were optimized to control the growth of SiO_2, including oxidation through a crystalline YSZ layer. Structural characterization using X-ray diffraction (XRD), X-ray reflectivity (XRR), and electron microscopy confirmed the formation of the multilayer structure.

The results show that oxygen can diffuse through the YSZ layer and oxidize the silicon underneath, although at a slower rate than direct oxidation. A multilayer structure was successfully fabricated by combining pulsed laser deposition (PLD) and thermal

oxidation processes.

Overall, this work demonstrates a fabrication approach that combines optimized etching and oxidation processes for the development of photonic material platforms.

Chapter 1

Introduction

Microfabrication processes require precise control of fabrication parameters, as small variations can lead to errors and inconsistencies in the final devices. Well-defined fabrication recipes must be carefully calibrated for each laboratory, as these processes are highly sensitive to small variations in experimental conditions. Therefore, establishing reliable and reproducible fabrication protocols is essential for the development of photonic and optoelectronic devices.

This thesis focuses on the optimization of microfabrication processes used in the development of photonic devices, specifically gallium arsenide wet etching and silicon thermal oxidation. These processes are essential for defining device geometry and enabling the integration of functional material platforms for photonic applications.

Gallium arsenide (GaAs) is widely used as a platform for quantum dot devices due to its direct band gap and favorable optoelectronic properties. In this context, wet chemical etching provides a method for pattern transfer that minimizes surface damage, which is critical for preserving near-surface structures. On the other hand, silicon oxidation enables the fabrication of multilayer structures, such as $Si/SiO_2/YSZ/CeO_2$, which are suitable for photonic applications, including planar waveguides, due to the refractive index contrast between the different layers.

This work is divided into two main parts. The first part focuses on the optimization of GaAs wet etching, including a brief introduction to the photolithography process required for pattern definition. The methodology is presented together with experimental results for three etching recipes, covering both nanometer- and micrometer-scale etching regimes. This section also includes a summary of practical considerations and recommendations for reproducible processing.

The second part of this thesis addresses silicon thermal oxidation and the development of a multilayer material platform. It includes a discussion of the theoretical background of silicon and silicon-on-insulator (SOI) substrates, oxidation mechanisms, and the pulsed laser deposition (PLD) technique. The methodology describes wafer preparation, cleaning procedures, and furnace setup for dry thermal oxidation. Experimental results are presented for the optimization of oxidation parameters, followed by the deposition of YSZ and CeO_2 layers to achieve the desired $Si/SiO_2/YSZ/CeO_2$ structure.

This study demonstrates the feasibility of combining optimized etching and oxidation processes to fabricate structures relevant for photonic device applications, while also identifying key limitations and providing recommendations for future process improvements. The results of this work contribute to the development of reliable microfabrication processes for future photonic and optoelectronic device integration.

Chapter 2

Microfabrication

Microfabrication is the fabrication of structures at the micrometer scale. These structures include integrated circuits such as chips, sensors, micro electromechanical systems (MEMS), and other microdevices. The fabrication of a micro device requires a multi-step procedure, including solutions to possible problems during the process.
This chapter describes the key microfabrication processes used in this work, including photolithography, wet etching and it also mention metal deposition.

2.1 Introduction to photolithography

2.1.1 Pattern Design

Microdevice fabrication begins with the design stage, in which device geometries are defined in a file format that can be read by exposure equipment, such as GDS. This design determines the patterns that will be transferred onto the substrate during photolithography. Various approaches can be used to generate these layouts, including graphical editors and programmatic tools. Python-based libraries, such as PHIDL [4], enable parametric and high-precision design, while graphical editors like KLayout allow visualization and manual modification of layouts. These tools provide flexibility in defining structures across a wide range of length scales, from micrometer to nanometer dimensions.

2.1.2 Substrate

Microfabrication is performed on a support called a substrate. The most commonly used substrates are semiconductors such as silicon (Si), gallium arsenide (GaAs), and indium phosphide (InP) [5]; however, there are also insulating substrates such as glass, quartz, sapphire (Al_2O_3) or silicon dioxide (SiO_2); as well as metals used in Microelectromechanical Systems (MEMS), in ceramics, and soft materials such as polymers or, in emerging applications, textiles [6]. In this chapter, the focus is on semiconductor substrates, specifically silicon and gallium arsenide.

Semiconductor materials are widely used in microelectronics and can be classified into three categories according to their atomic structure: single-crystal, amorphous, and polycrystalline materials [7]. Single-crystal materials are characterized by a highly ordered atomic arrangement, where atoms occupy well-defined positions in a periodic lattice. In contrast, amorphous materials do not exhibit long-range order, as their atoms are arranged in a disordered manner with variations in bond lengths and orientations. Polycrystalline materials consist of a collection of small crystalline regions (grains), each with a well-defined lattice structure but randomly oriented with respect to one another. Common crystallographic orientations include (100), (110), and (111), which influence surface properties, etching behavior, and thin-film growth.

The semiconductor wafers of silicon or gallium arsenide are single-crystalline materials. Silicon is a group IV element; it has four valence electrons and requires four more to complete its valence shell [7]. It has a diamond cubic structure, as shown in Fig. 2.1 a) . Gallium arsenide (GaAs) is a III–V compound semiconductor that adopts the zinc blende crystal structure, which is similar to the diamond structure but consists of

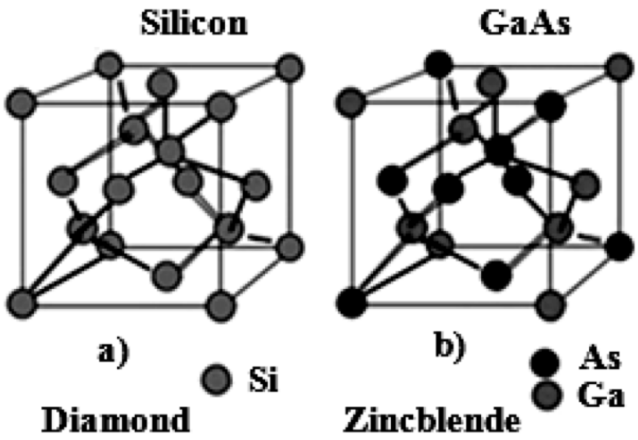

Figure 2.1: Structure of silicon and gallium arsenide [2]

alternating gallium and arsenic atoms, as shown in Fig. 2.1 b).

Silicon wafers are widely used in microelectronics due to their compatibility with oxidation processes, low cost, and well-established fabrication technology, which makes it ideal for large-scale electronic integration. In contrast, GaAs wafers are typically used in optoelectronic and high-speed devices due to their direct band gap and higher electron mobility. Silicon has an indirect band gap (1.1 eV), while GaAs has a direct band gap (1.42 eV), which enables efficient electron–hole recombination and light emission [2]. Additionally, the higher electron mobility in GaAs allows faster carrier transport, making it advantageous for high-frequency and high-speed devices [2].

They are fabricated generally by first growing a crystal ingot and then slicing and chemically polishing it, resulting in thin wafers with thickness in the range of approximately 100-500 μm and diameters of 100-450 mm, depending on the application. This material can be doped by adding impurities (dopants) so that it can be either p-type (positive charge carriers, holes) or n-type (negative charge carriers, electrons). In this work, wafers with (100) orientation and undoped materials were used.

For any device fabrication, the wafer can be cut in the desired dimension and then cleaned using solvent-based procedures.

In microfabrication, it is necessary to use a process of pattern transfer. The most common method is photolithography, which uses UV light, where the wavelength determines the minimum feature size that can be formed in the photoresist.

2.1.3 Photoresist

The photolithography process starts with a wafer coated with photoresist, a light-sensitive material. The typical components of a photoresist are: resin or base (a binder that provides physical properties such as adhesion), sensitizer or photoactive compound (PAC) and solvent (which keeps the resist liquid)[7]. The photoresist can be categorized into positive and negative. In the positive photoresist, the region exposed to light dissolves faster after the exposure and during development, making the unexposed region remain intact; this is caused by the PAC that changes from inhibitor to a sensitizer, increasing the dissolution rate of the exposed photoresist. On the other hand, the negative photoresist behaves oppositely; the exposed region remains intact. There are some metrics for photoresist, but the most common are the sensitivity and resolution. The sensitivity refers to the amount of light energy required to change the chemical properties of the resist. The more sensitive the photoresist is, the less time and exposure intensity are required. Resolution refers to the smallest features that the photoresist can replicate; this factor also depends on the machines used during the exposure system.

To apply a photoresist, the wafer must be clean to guarantee a uniform application

and good adhesion of the resist to the wafer. Then, the wafer is mounted inside a spin coater and is held by a vacuum. With the help of a pipette, the wafer is covered with the liquid photoresist and then the spin coater rapidly accelerates and rotates, usually between 2000-6000 rpm, for a specific time. The parameters such as acceleration, revolutions per minute (rpm) and time determine the thickness of the photoresist. The thickness and uniformity are critical parameters for a good photolithography process [5]. Different photoresist and machines require different parameters. After spinning, the wafer is soft-baked with a temperature generally around 90-110°C for a specific time, typically around one minute, to drive off the solvent and establish the exposure characteristics of the resist.

Some limitations of spin coating include non-uniform photoresist thickness near the edges of the sample, commonly referred to as edge bead formation. This effect is more pronounced at low spin speeds and can be partially optimized for circular wafers. However, for non-circular substrates, such as rectangular or square samples, edge bead formation becomes more significant due to non-uniform rotation and increased air turbulence [8].

In practice, these edge effects result in thickness variations near the samples' borders, as shown in Fig. 2.2. Such non-uniformity can affect exposure and development, leading to reduced pattern quality at the edges. For this reason, an additional margin (1–2 mm) is typically excluded when designing devices on the wafer.

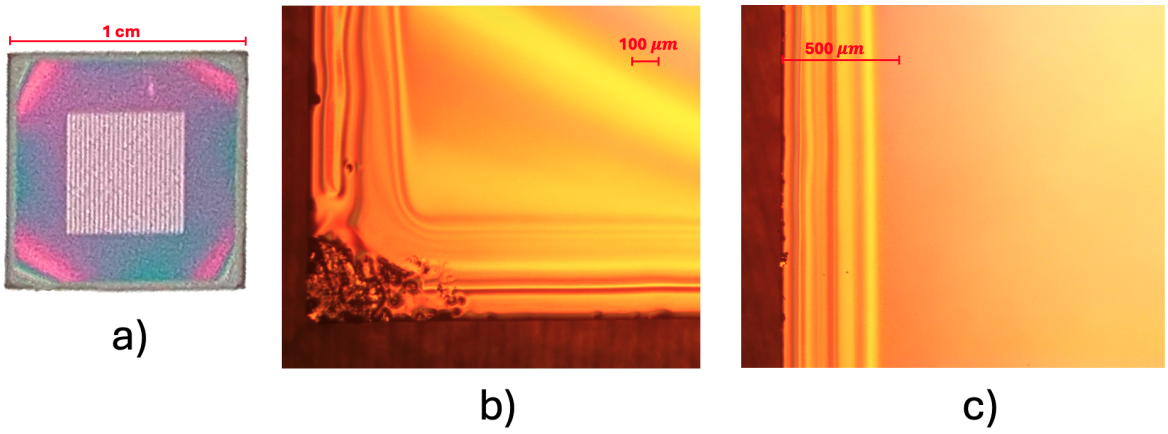

Figure 2.2: (a) Optical image of a 1 cm × 1 cm sample after photolithography. The red–purple region corresponds to the photoresist, while the central square is exposed GaAs. Color variations near the edges indicate non-uniform photoresist thickness (edge bead), and these regions are typically excluded from patterning. (b) Optical image of a sample corner showing the scribe line used for cleaving and non-uniform photoresist coverage. (c) Comparison of photoresist uniformity: non-uniform thickness at the edge (left) and uniform coating in the central region (right).

2.1.4 Exposure

After the soft bake, the photoresist is ready to be exposed to UV light. Two possible options are to use a mask aligner or writing with a laser beam writer.

2.1.4.1 Mask writer

With a mask aligner, it is necessary to use a photomask, which is made of glass and a top layer of chromium. The exposed areas (only glass) show the desired design (for positive photoresist) to be transferred to the photoresist and the rest remain covered (glass and chrome), allowing the UV light to pass only through the patterned regions of the photomask. Therefore, only these specific areas will be transferred to the photoresist and then can be removed, during the developing process. This can be applied to negative photoresist.

The main parameter to define in this process is the exposure time, which is typically on

the order of seconds. This system has the benefit of processing many samples in a short time, since after the alignment, the exposure takes only a few seconds, independently of the size of the design. However, it requires a photo mask, which must be fabricated beforehand by a third party and requires an investment.

A challenge in this process is achieving a proper alignment between the photomask and the desired exposure region on the wafer. This becomes more difficult in multi-step photolithography processes, where alignment must be performed with high precision. In these cases, alignment markers are commonly used, which are placed outside the active device area. As shown in Fig. 2.3 a-b), a multi-step photolithography process may involve sequential patterning steps (e.g., step A followed by step B), where both patterns must be accurately aligned with respect to each other. In this design, a margin frame was used as an alignment mark; however, these markers can also be small features such as cross (+) symbols located at the corners or edges of the sample, as shown in Fig. 2.3 c-d).

2.1.4.2 Laser Writer

The other option to expose a pattern is to use a laser writer. This machine is typically used to fabricate photomasks, but it can also be used to write designs directly onto a wafer using a focused laser beam to expose the photoresist. The pattern is generated from a digital GDS file and then written by scanning the laser across the sample with high positional accuracy, exposing the design line by line. This process does not require a photomask, which is a good alternative for testing designs or samples. Additionally, due to the use of the equipment's camera and a motorized stage, improved alignment accuracy can be achieved in multi-step photolithography processes. However, since this process writes the pattern line by line, the exposure time is significantly longer, typi-

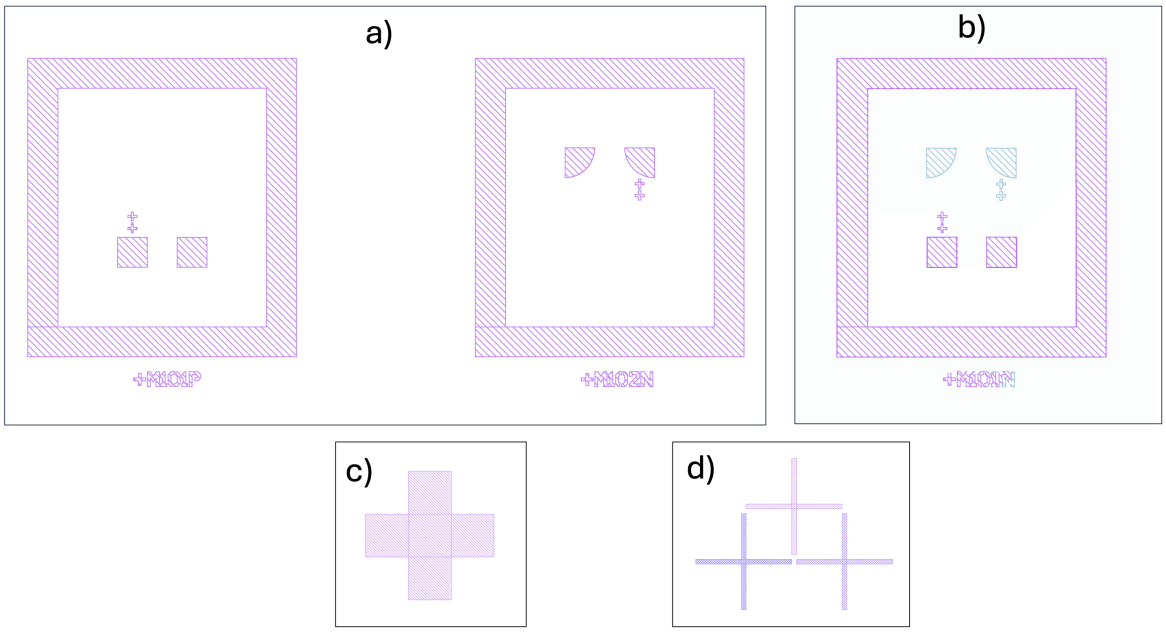

Figure 2.3: Alignment mark strategies for sequential photolithography. (a) Two-step sequential patterning using a frame as an alignment reference. (b) Final result after both patterning steps are completed. (c–d) Alternative alignment mark designs, where markers are placed either at the four corners or at the center of each edge of the pattern. (d) These markers can be implemented as individual features or as stacked (overlapping) structures.

cally ranging from minutes to several hours depending on the design size, complexity and writing parameters.

The exposure process in this machine includes several parameters: the exposure dose, which indicates the energy delivered to the photoresist (typically in units of mJ/cm^2 or as a percentage of laser power); the laser power, which determines the intensity of the beam (in mW); the writing speed; and the defocus, which is used to adjust the effective beam size and therefore the feature dimensions.

In laser writers such as the Heidelberg μPG101, the energy mode controls how the exposure dose is delivered over time by combining multiple exposures and speed reduction. It is commonly expressed as 1×4, where the first number indicates the

number of exposures applied to the same area, and the second number represents the speed reduction factor. In this way, the same region is exposed for a longer time, either depositing more energy or delivering the same energy more gradually. This improves edge quality and pattern resolution, but increases the total exposure time [1]. This can be clarified with an example shown in Table 2.1.

Energy mode	
1×2	There will be one exposure, but the speed is reduced by a factor of 2, increasing the exposure time and deposited energy per spot by a factor of 2.
3×4	There will be three exposures in a row, and the speed is reduced by a factor of 4, increasing the exposure time and deposited energy per spot by a factor of 4. The effective energy is $3 \times 4 = 12$.

Table 2.1: Example of energy mode values in the Heidelberg μPG101 laser writer [1].

2.1.5 Developing

After exposure, the photoresist undergoes a chemical change that allows selective removal to reveal the pattern. To do this, the wafer is submerged in a developing solution for a specific time, followed by rinsing with deionized (DI) water and drying. It is important to have sufficient development time to remove the exposed photoresist, but not excessive time that could damage or remove the remaining resist.

This process must be verified to determine whether the exposure pattern was correctly transferred, since the exposure parameters and the photoresist thickness affect the final result. The goal is to obtain a pattern on the wafer that accurately reproduces the original GDS design. This can be verified using an optical microscope by measuring whether the fabricated features match the intended dimensions.

If the process is not optimized, defects such as overexposure or underdevelopment can occur. In an overexposed pattern (Fig. 2.4 c), features appear enlarged or distorted due to excessive energy delivered to the photoresist. This can be mitigated by reducing the exposure dose or time, or by using a thicker photoresist layer. In contrast, in an underdeveloped pattern (Fig. 2.4 a), residual photoresist remains in areas that should be cleared, indicating insufficient removal during development. This can be improved by increasing the exposure dose or time, or by using a thinner photoresist layer. Additionally, it is important to verify that the development process itself is properly optimized, since it can be difficult to distinguish whether defects are due to overexposure or improper development if the development process is not properly controlled.

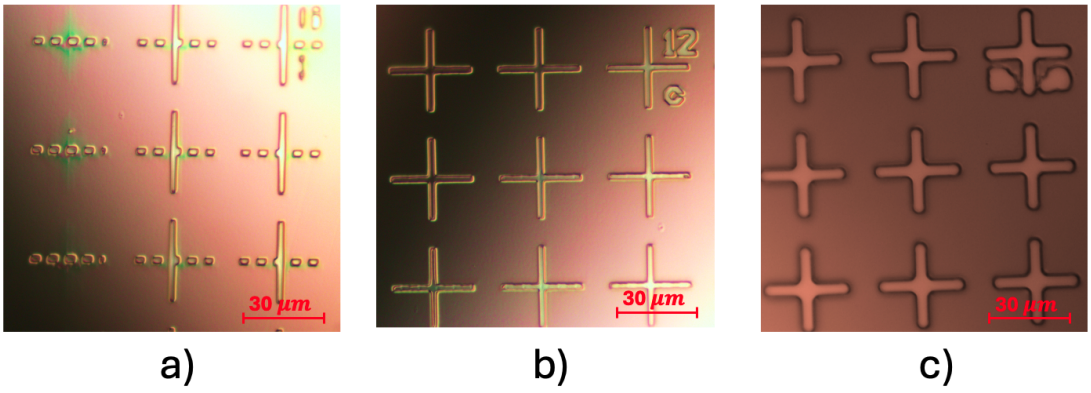

Figure 2.4: Optical microscope images illustrating photolithography exposure conditions: (a) underexposed, (b) correctly exposed, and (c) overexposed patterns. The cross markers have a designed linewidth of 2 µm and are used as a reference.

For this reason, parameters such as photoresist thickness, exposure dose, and development time must be carefully controlled to ensure accurate pattern transfer. These parameters can be suggested by the manufacturer, but still require careful optimization during processing. If all previous processes are optimized correctly, pattern transfer is

successfully achieved, and the sample can proceed to the next microfabrication steps, such as etching or metal deposition.

2.2 Etching

After the photoresist pattern has been formed, the next step could involves removing (etching) the exposed areas of the wafer. The etching process depends on the substrate material, crystal orientation, and etching method.

Etching can be characterized by the lateral etch rate (R_L) and vertical etch rate (R_V). The anisotropy A is defined as show in Eq. 2.2 [7].

$$A = 1 - \frac{R_L}{R_V} \tag{2.1}$$

An ideal process is fully anisotropic ($A = 1$), where the lateral etch rate is zero. However, most practical processes exhibit partial anisotropy, as shown in Fig. 2.5.

Silicon, which has identical Si–Si bonds in all directions, exhibits similar bond energies throughout the lattice. This results in a more isotropic etching behavior and allows for more uniform control. In contrast, GaAs has alternating Ga–As bonds in its lattice, leading to asymmetry, different bond strengths, and variations in electronegativity. As a result, etching in GaAs is typically anisotropic, with etch rates that depend on the crystallographic direction. In this project, GaAs wafers with a (100) orientation and undoped substrates are considered.

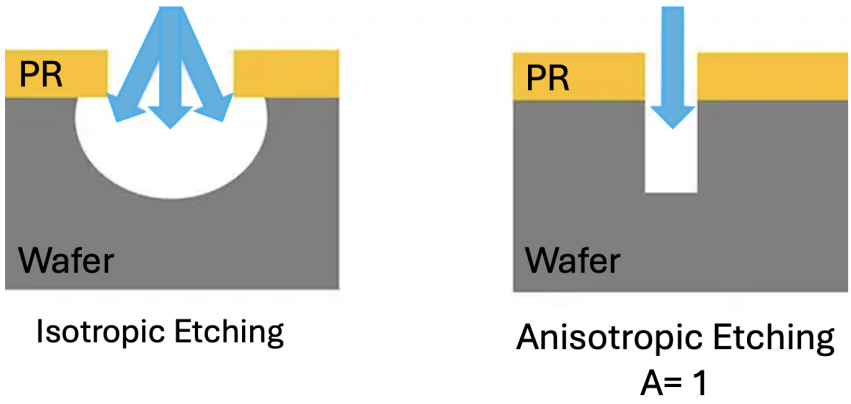

Figure 2.5: Left: typical isotropic etching profile; right: ideal anisotropic etching profile. Adapted from [3]

In etching processes, several parameters are important, including etch rate, selectivity (the difference in etch rate between materials), potential surface damage, and safety considerations for the operator and environment. A controlled etch rate is desired; therefore, slower etching rates are often preferred because they allow better process control.

There are two main types of etching: dry etching and wet etching. In this work, the focus is on wet etching, as it is the technique used in the experimental part of the project because it minimizes surface damage compared to dry etching.

2.2.1 Dry etching

Dry etching is a plasma-phase etching technique that includes processes such as plasma etching, ion milling, and reactive ion etching (RIE). It has the advantage of a high degree of anisotropy and good process control; however, it typically has low selectivity and can cause substrate damage and possible chemical contamination after the etching

process.

In a plasma system, the gas is broken down into active species (ions, radicals, and electrons). These species diffuse to the wafer surface, where they are adsorbed. Then, surface reactions occur between the reactive species and the substrate, forming volatile products that are released and transported out of the etching chamber. An example of silicon etching uses fluorine-based plasmas such as CF_4 and oxygen (O_2). In this case, CF_4 dissociates in the plasma to produce fluorine radicals:

$$CF_4 \rightarrow C + 4F$$

These fluorine radicals react with silicon to form volatile products:

$$Si + 4F \rightarrow SiF_4(g)$$

Oxygen reacts with carbon to form gaseous species:

$$C + O_2 \rightarrow CO(g) + CO_2(g)$$

where (g) indicates gaseous (volatile) products. These species are removed from the system, reducing polymer formation and increasing the availability of fluorine radicals, thereby increasing the etching rate [7].

Ion milling does not involve chemical reactions. Instead, it relies on physical sputtering by energetic ions, providing high directionality and being applicable to many materials. However, it has low selectivity and low throughput, and it can cause significant surface damage.

Reactive ion etching (RIE) combines physical ion bombardment with chemical reactions. Chlorine-based plasmas (e.g., Cl_2, BCl_3) are commonly used to anisotropically etch silicon and GaAs. In GaAs, chlorine reacts with gallium and arsenic to form

volatile species such as $GaCl_3$ and $AsCl_3$. Compared to plasma etching and ion milling, RIE provides a balance between anisotropy and etch rate by combining chemical and physical mechanisms [7].

$$GaAs + Cl_2 \rightarrow GaCl_3(g) + AsCl_3(g)$$

2.2.2 Wet etching

Wet etching is a liquid-phase technique characterized by high selectivity and minimal damage to the wafer surface. However, it typically exhibits low anisotropy, limited process control, and may lead to particle contamination. As a result, it is not well suited for fabricating small features and can generate chemical waste. The etching process consists of three main steps: (i) transport of etchant species to the wafer surface, (ii) chemical reaction with the exposed material to form soluble byproducts, and (iii) transport of reaction products away from the surface [7].

For GaAs, wet etching commonly follows an oxidation–dissolution mechanism. Strong oxidizing agents first oxidize the surface, followed by dissolution of the oxide layer by acids, and subsequent removal of the reaction products. A common oxidizing agent is hydrogen peroxide (H_2O_2) [9], which reacts with GaAs to form gallium oxide (Ga_2O_3) and arsenic oxide (As_2O_3). A simplified representation of the oxidation step is:

$$GaAs + (\text{oxidizer}) \rightarrow GaO_x/AsO_y$$

These oxides are then removed by acids such as sulfuric acid (H_2SO_4), phosphoric acid (H_3PO_4), or citric acid, which dissolve the oxide layer into soluble species. To give ions Ga^{3+} and arsenic-containing species in solution [10].

$$GaO_x/AsO_y + (\text{acid}) \rightarrow Ga^{3+} + \text{soluble arsenic species}$$

Deionized (DI) water facilitates the transport of dissolved species away from the surface, allowing the etching process to proceed continuously. Overall, the etching behavior is governed by the balance between oxidation and dissolution by the acidic solution, which determines the etch rate, uniformity, and surface morphology.

In addition to chemical composition, process parameters such as temperature and agitation influence the etching behavior. Increasing temperature generally enhances the etch rate by accelerating both oxidation and dissolution reactions, although it may also increase surface roughness and reduce process control. Agitation improves mass transport by enhancing reactant delivery and removal of reaction products, leading to more uniform etching.

2.3 Metal deposition

Metal deposition allows the fabrication of metal contacts. After photolithography, the whole wafer is coated with a thin layer of the desired metal. Then, during the lift-off step, the regions with photoresist are removed along with the deposited metal, and only the regions without photoresist remain covered with metal.

There are, in general, two types of metal deposition: physical vapor deposition (PVD) and chemical vapor deposition (CVD). PVD includes techniques such as thermal evaporation, where the metal is heated until it evaporates and the vapor travels in a straight line to the substrate, and sputtering, which uses plasma to remove atoms from a target that are then deposited onto the substrate. In CVD, the film is formed through chemical reactions of gaseous precursors at the substrate surface, including

methods such as thermal CVD [7].

PVD techniques are widely used due to their simplicity and compatibility with photolithography; however, they can present limitations in step coverage, especially for vertical or high-aspect-ratio structures (height-to-width ratio). Careful optimization and verification are therefore required.

Even though this work does not directly include the fabrication of metal contacts, some mask designs incorporate this step, as shown in Appendix B, where the complete fabrication sequence—photolithography, wet etching, and metal deposition—is illustrated.

2.4 Possibles microdevices

To illustrate some microdevices that can be fabricated using microfabrication techniques, one important example is the formation of p-type and n-type contacts.

2.4.1 P- and n-type contacts

P- and n-type contacts are essential components in semiconductor devices, as they enable electrical injection and extraction of carriers (holes and electrons). These contacts are typically defined through photolithography and metal deposition processes, as described in the mask designs provided in Appendix B.

In many cases, the p- and n-type contacts must be fabricated at different vertical levels. This is particularly important when accessing buried layers or when electrical connections must be made without short-circuiting adjacent regions. Wet etching is

commonly used to selectively remove material and create these stepped or recessed structures, allowing contacts to be formed at different depths.
This approach can be applied both in bulk wafers and in more complex structures such as quantum dot devices, where precise control of geometry and layer access is required.

2.4.2 Quantum dots as substrate

Quantum dots are typically grown in GaAs-based wafers, commonly in GaAs/AlGaAs heterostructures, and are widely used in photonic devices because they behave like artificial atoms, with discrete energy levels that allow the emission of single photons. When fabricating microstructures on these wafers, it is important to preserve the quality of the quantum dots. Since they are often located close to the surface, they are highly sensitive to defects and surface damage, which can degrade their optical properties and reduce emission efficiency.

For this reason, any etching process used to pattern the GaAs substrate must be carefully controlled. In particular, the etching should minimize surface roughness and avoid introducing defects that could affect carrier recombination. This is especially important when working at nanometer and micrometer scales, where small variations can significantly impact device performance. Wet etching is preferred over dry etching techniques because it produces less surface damage and smoother surfaces. In addition, when an appropriate etching recipe is used, wet etching can be selective between GaAs and AlGaAs layers, enabling controlled removal of material without damaging the quantum dot region. This makes it especially suitable for fabricating microstructures in GaAs/AlGaAs quantum dot platforms.

Chapter 3

Wet Etching of GaAs: Methodology and Results

Wet chemical etching was employed for pattern transfer in GaAs substrates. In this work, wet etching was selected over dry etching to minimize surface damage and preserve the integrity of near-surface quantum dot structures for future device fabrication. The etching process was optimized to achieve controlled removal in both the nanometer and micrometer regimes.

This chapter describes the wet etching of GaAs, including sample preparation, photoresist coating parameters, and photolithography with optimized exposure conditions. The etching procedures and corresponding etch rates are presented for three developed recipes in the nm and μm ranges. In addition, other tested recipes that did not yield satisfactory results are discussed.

3.1 Preparation of the sample

3.1.1 Cleaving and Cleaning sample

First, the undoped GaAs wafer (100) was cleaved into samples of approximately $1\ cm \times 1\ cm$. Cleaving was performed manually using a diamond scribing pen to

create a small scratch of approximately 1 mm in length. The scribe was repeated 3-5 times along the same direction to define the cleaving line. Gentle pressure was applied during this process, as GaAs is a brittle material, and excessive force can lead to wafer damage or undesired fractures. The wafer was then cleaved by applying gentle pressure along the scribed line using CleanBreak™ cleaving pliers (LatticeGear, USA) as shown in Fig. 3.1. Any small fragments generated during cleaving were carefully removed and properly disposed of to prevent surface scratching.

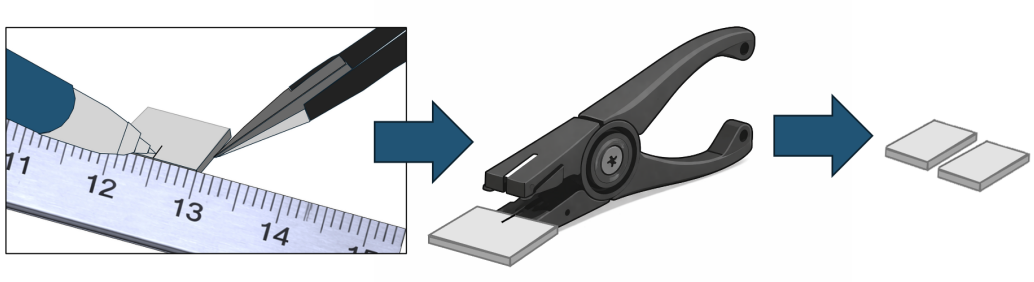

Figure 3.1: GaAs wafer cleaving procedure using a diamond scribe and cleaving pliers. This method allows hight-precision cleaving of GaAs samples, including pieces as small as approximately 3 mm in lateral dimensions.

The samples were subsequently cleaned using a standard solvent-based cleaning procedure consisting of four steps. The cleaning sequence began with two consecutive baths in acetone, followed by methanol and then isopropyl alcohol (IPA). Each step was performed in an ultrasonic bath for 5 minutes, ensuring that cavitation bubbles were observed on the surface during cleaning. The samples were then rinsed with deionized (DI) water and dried using a nitrogen gun. Finally, the samples were treated with an oxygen plasma asher at 300 W for 5 minutes.

The solvent cleaning steps were used to remove organic contaminants such as oils, organic residues and residual photoresist (in reused samples) from the surface of the

wafers. While solvent effectively removes these contaminants, they can also leave residual traces. Therefore, a deionized (DI) water rinse was used to eliminate solvent residues. The plasma oxygen asher step was employed as a final step to remove any remaining trace organic on the sample surface after the DI water rinse.

Used wafers may be reused, provided they are not damaged or previously etched, and are thoroughly cleaned using this procedure. Additionally, the solvent-based cleaning and oxygen plasma treatments were performed in batch mode, allowing multiple samples to be processed simultaneously.

3.1.2 Coating and Photolithography

After the sample was cleaned, the photoresist coating and photolithography process were performed. Unlike the cleaning steps, which can be carried out in batch mode, spin-coating and photolithography were performed on individual samples. Two photolithography recipes were used: one for the mask aligner, which requires a physical hard mask to transfer the desired pattern using UV exposure, and another for a mask writer, which enables direct-write lithography without the use of a hard mask. The machine used for direct-write lithography improved alignment in multilayer patterning and between successive photoresist steps in comparison to the mask aligner. Both recipes are described below.

Although not universally adopted, refrigerated storage of photoresist was used in this cleanroom to extend shelf life and maintain resist consistency. Before spin coating, the photoresist was allowed to warm to room temperature for at least 15 minutes.

3.1.2.1 MJB3-Mask Aligner

For this equipment, AZ5214 positive photoresist was used. The photoresist was spin-coated at 2500 revolutions per minute (rpm) with an acceleration of 300 (rpm/s) for 60 seconds, resulting in a thickness of approximately 1.9 μm. After coating, the samples were soft-baked at 95°C for one minute. The coated samples were then exposed to UV light for 10 seconds and subsequently developed for 50 seconds using MIF726 developer. After development, the samples were rinsed with (DI) water and dried using a nitrogen gun. An important detail of this equipment is that, based on previous experiments, the minimum feature size that the MJB3 mask aligner can reliably expose is approximately 4 μm.

3.1.2.2 Mask writer - Heidelberg μPG101

For this equipment, AZ1505 positive photoresist was used. The parameters of this recipe were optimized to obtain a photoresist thickness of approximately 0.57 μm, which is close to the recommended thickness value of 0.5 μm [1]. The photoresist was spin-coated at 4000 revolutions per minute (rpm) with an acceleration of 500 (rpm/s) for 60 seconds. After coating, the samples were soft-baked at 100°C for 50 seconds.

Photolithography parameters for the Heidelberg μPG101 were optimized through multiple experimental iterations, starting from the recommended conditions provided by the cleanroom staff (power 42% of 20 mW, defocus 10, energy mode 1 $\times$ 1). Each parameter was varied independently. Some parameters tested are shown in Fig. 3.2. The wet etching test pattern consisted of a grating with 100 μm line widths and 100 μm spacing over an area of 0.5 cm^2.

However, smaller features can also be used; based on previous experiments, the minimum feature size that the Heidelberg μPG 101 can successfully expose is approximately 1-2 μm.

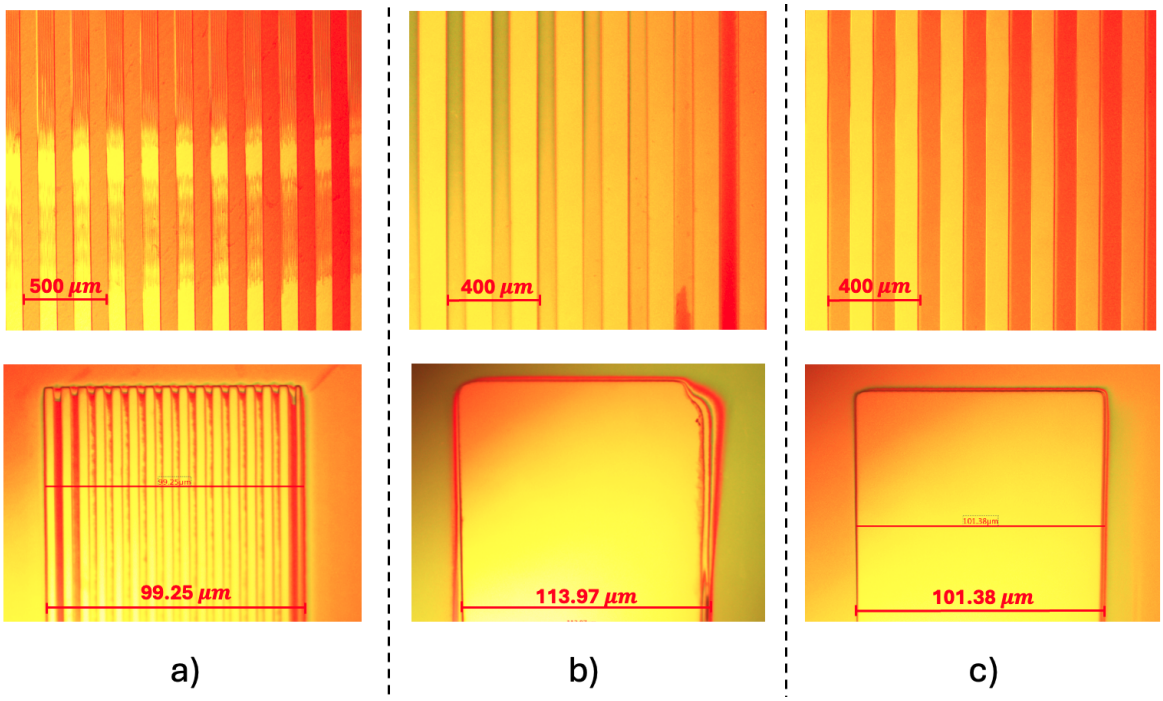

Figure 3.2: Examples of exposure optimization using the Heidelberg μPG101:
(a) underexposed pattern (power 10% of 20 mW, defocus 10, writing mode 1 $\times$ 2);
(b) overexposed pattern (power 46% of 20 mW, defocus 10, writing mode 1 $\times$ 4);
(c) correctly exposed pattern (power 10% of 20 mW, defocus 10, writing mode 1 $\times$ 4).

The writing mode, which determines the writing time, was found to be the most critical parameter. Longer writing times required reduced exposure power to avoid overexposure, while changes in defocus had minimal effect.

Alternative parameter sets with shorter writing times were also identified, in addition to the optimized condition presented above (see Table 3.1, Optimizations 1 and 2). However, these resulted in lower resolution, particularly at pattern edges, despite

Optimization	Power [mW]	%	Defocus	Energy Mode	Total Time [min]
1	20	46	10	1x1	5
2	20	26	10	1x2	10
3	20	10	10	1x4	20

Table 3.1: Optimized photolithography parameters for the Heidelberg μPG101 system for three different writing modes. The total writing time corresponds to a pattern with a characteristic size of 100 μm over an area of 0.5 cm $\times$ 0.5 cm.

requiring less writing time, as shown in Fig. 3.3 . Therefore, Optimization 3 was selected for all etching processes.

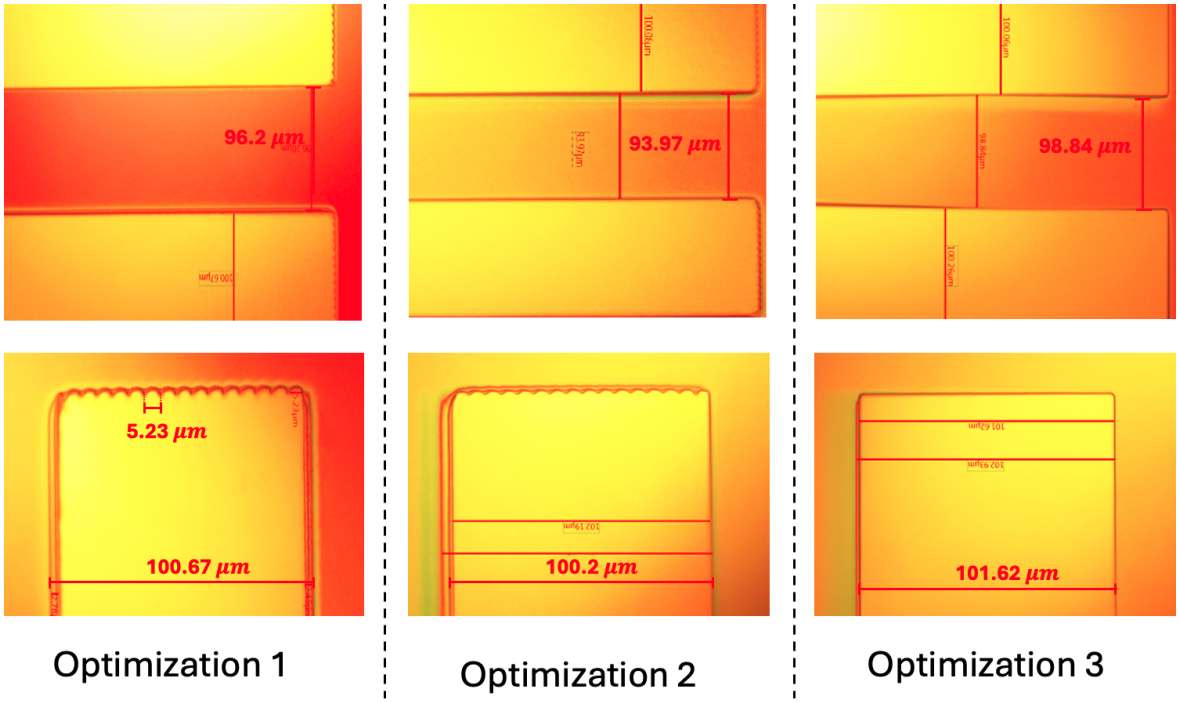

Figure 3.3: Optimized photolithography parameters for the Heidelberg μPG101 system at three writing modes. Edge definition improves with higher writing modes, while all conditions produce acceptable pattern quality.

A slight increase in feature size after writing was observed. This effect can be compensated by reducing the GDS design dimensions by approximately 1–2 μm, as also recommended in the system manual [1]. Additionally, variations between consecutive

writing processes were noted; therefore, short resting periods between runs are recommended to improve reproducibility.

The required dose was set to 10% of a 20 mW source, with a defocus of 10 and mode 1×4. After exposure, the sample was developed for 50 seconds using AZ726MIF developer. After development, the samples were rinsed with (DI) water and dried using a nitrogen gun.

In both photoresist processes, after development, the samples were inspected under an optical microscope to verify the success of the photolithography process. In case of unsuccessful photolithography or intermediate processing steps, samples were reused by removing the photoresist with acetone, followed by the standard cleaning procedure described previously.

3.2 Wet etching

Before wet etching, the samples were inspected under optical microscope to ensure a well-defined profile, where the exposed areas were fully developed, ensuring that no remaining photoresist interfered with the surface during etching.

First, the etchant needed to be prepared by mixing the desired acids and chemicals. Chemical mixing was performed in a fume hood. The etchant preparation followed the standard safety procedure of adding acid to water, as acid-water reactions are exothermic. All pouring was performed slowly, and the etchant solution was mixed using a magnetic stir for at least 15 minutes at a speed that ensures uniform mixing without splashing.

3.2.1 Citric Acid

For any depth range etching required, the solution of citric acid may be needed. Citric acid is in the form of powder; for that reason, with the help of filter paper to hold the powder it is weighed using a scale. A measure of X gr was measured. Then, a beaker containing Y ml of (DI) water was placed on a magnetic stirrer and mixed at a safe speed that ensures proper mixing without splashing. The citric acid powder was poured slowly into the water and mixed for at least 30 minutes until all grains of citric acid were dissolved. The mixture was stored in a container with a lid and labeled with the mixing ratio X:Y and preparation date. This solution can be stored and used for up to two weeks.

3.2.2 Preparation of etcher

For any recipe, the mixture was stirred for at least 15 minutes to ensure homogeneity of the etchant at a speed marked on the magnetic stirrer. After preparation, the etchant was allowed to stabilize for two hours prior to initial use. The solution was subsequently stored in a sealed, labeled container and used within two weeks. Since some components, such as hydrogen peroxide (H_2O_2), degrade over time [10], this can affect etch consistency.

Depending on the number of steps required for the etching process, multiple beakers were prepared: an initial beaker for sample preparation (if needed), a beaker containing the etchant, and at least two beakers containing deionized (DI) water to stop the etching process. The sample was submerged in the etchant for the desired time and then immediately immersed in the next beaker with deionized water for one second, followed by immersion in the last beaker with deionized (DI) water for one minute

to ensure that the etching process was completely stopped. The sample to be etched was held using Teflon tweezers, or tweezers with Teflon-coated tips, ensuring that the metal part was not in contact with the solution. The immersion of the sample can be performed by simply dipping the sample without agitation in the etchant, or with the etchant being stirred at the same speed marked on the stirrer, depending on the recipe utilized. Agitation increases the etching rate.

The sample was dried using a nitrogen gun and inspected under an optical microscope to verify that the photoresist remained intact. If the photoresist was removed or damaged during the etching process, this indicated issues in the coating or photolithography steps, and the sample could not be used for further analysis. If the photoresist remained intact, it was subsequently removed using acetone while gently stirring the sample for approximately 10 seconds. The sample was then rinsed with deionized (DI) water, dried with a nitrogen gun, and inspected again under an optical microscope to observe whether the desired pattern had been successfully etched.

Before etching new samples, the DI water beakers were rinsed three times and refilled to avoid contamination. The etching solution could be reused.

3.2.3 Etching Characterization

After the samples were etched, independent of the recipe used, they were analyzed using a profilometer (KLA Tenco Alpha-Step D-500) and an AFM (Park NX10 AFM) to evaluate the etched profile and characterize the etching rate.

Profilometer measurements were performed over scan lengths between 0.1 and 0.5 mm to improve the resolution and minimize large-scale variation, as longer scans were

found to reduce measurement reliability, although they could provide a qualitative idea of the profile. Scan speeds of 0.01 and 0.05 mm/s were used, range of 2.5 microns or 10 microns (depending on the depth of the sample) with a stylus force of 0.2 mg. The data were extracted as XML file and processed using a Python script that applies local polynomial smoothing to obtain a continuous profile. The step height was determined using a percentile-based level separation of the fitted profile, and RMS (Root Mean Square) noise was calculated from the difference between the raw data and the fitted curve (see Appendix A).

In addition, AFM was used to characterize the surface height and roughness. The measurements were analyzed using XEI software (Park Systems) to calculate the RMS surface roughness from the extracted height data. An optical microscope (Nikon 2000) was employed throughout the fabrication and characterization process.

3.2.4 Etching with a depth of micrometers (μm)

For etching in micrometers range, two recipes were developed and used:

- Recipe 1

For this recipe, citric acid was prepared in a 1 : 1 ratio with DI water, as described in subsection 3.2.1. The etchant solution was prepared in a beaker by first adding deionized (DI) water, followed by slowly pouring phosphoric acid (H_3PO_4), then the citric acid solution was added, followed by 30% hydrogen peroxide (H_2O_2).

- Recipe 2

The etchant solution was prepared in a beaker by first adding deionized (DI) water,

followed by slowly pouring phosphoric acid (H_3PO_4), and then finally the 30% hydrogen peroxide (H_2O_2).

The mixing ratios of both recipes are listed in Table 3.2, where the chemicals are listed in the order in which they were poured for safety and stability. Acid was always added to water, and hydrogen peroxide was added last.

Recipe	Components	Notes
1	$H_2O : H_3PO_4 : CitricAcid : H_2O_2$ $7.5 : 7.5 : 10 : 60$	$CitricAcid$ $1 : 1$
2	$H_2O : H_3PO_4 : H_2O_2$ $45 : 4 : 1$	

Table 3.2: Wet Etching recipes for μm

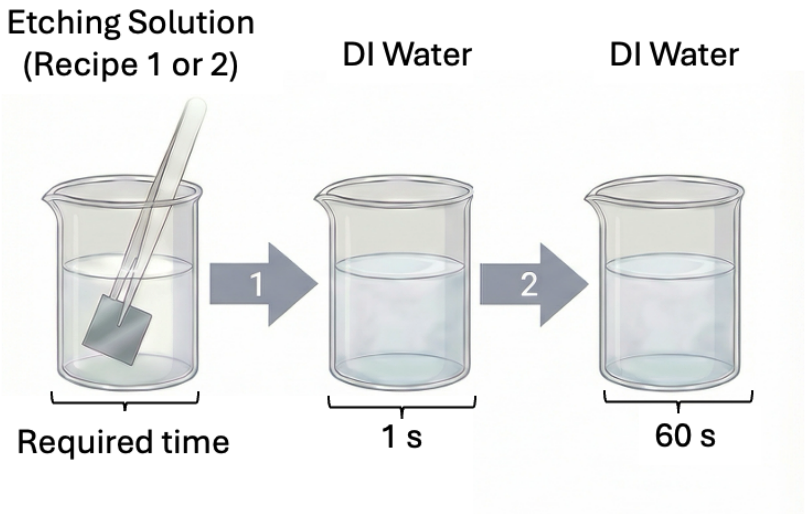

Figure 3.4: Etching workflow for μm range. Using sequential immersion in prepared beakers. Sample is handle with Teflon tweezers.

The result obtained for the etching in μm is shown in Fig. 3.5.

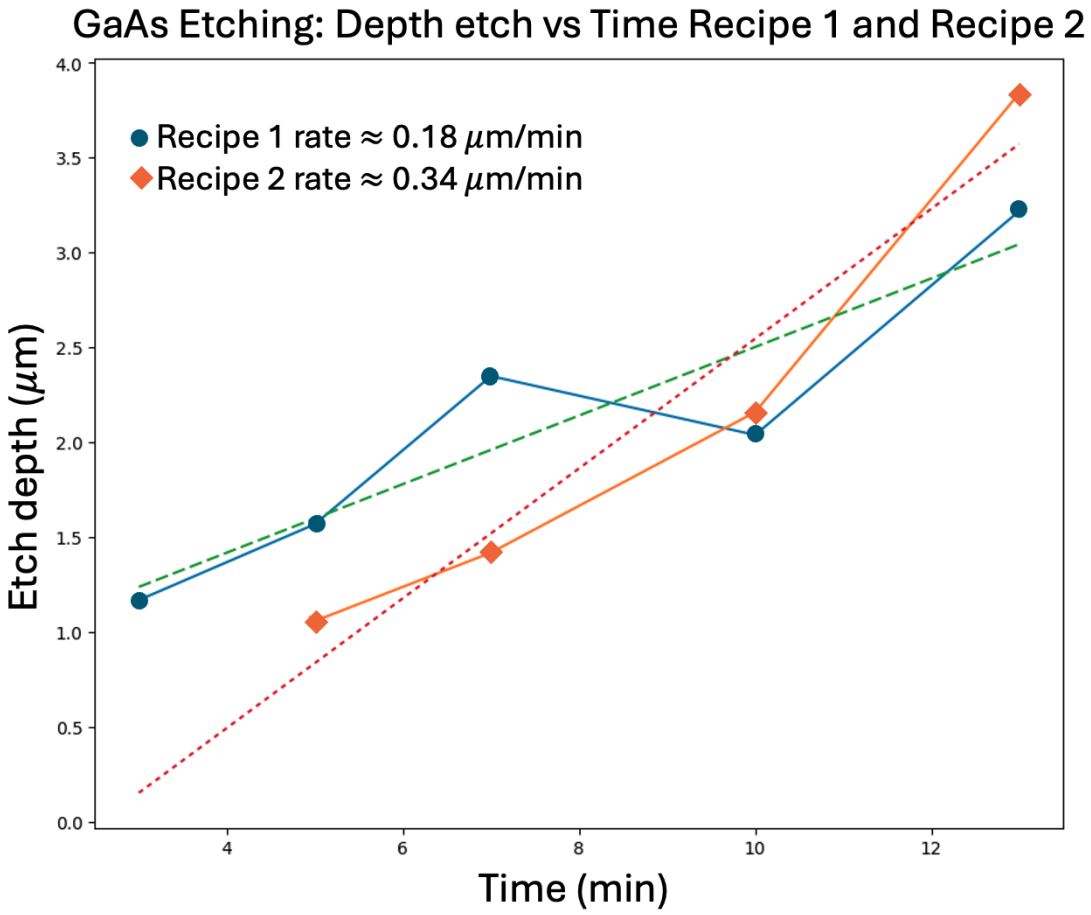

Figure 3.5: Etched depth as a function of time for GaAs using Recipe 1 (circles) and Recipe 4 (diamonds). Dashed lines indicate linear fits for estimating the etch rates. Error bars (± 10 nm) from the profilometer are not visible at this scale.

The etch depth increases approximately linearly with time for both recipes, indicating a stable etching process. Recipe 4 exhibits a higher etch rate (0.34 µm/min) compared to Recipe 1 (0.18 µm/min), suggesting a more aggressive etching behavior. Some deviation from linearity is observed at intermediate times, which may be attributed to variations in reaction kinetics or surface conditions. Overall, Recipe 4 provides faster etching, while Recipe 1 offers more controlled material removal.

3.2.5 Etching with a depth of nanometers (nm)

Since nanometer-scale etching requires a slower and more controlled reaction rate, a more dilute solution of citric acid was prepared. A solution of 10 : 100 citric acid to deionized (DI) water was prepared, as described in subsection 3.2.1.

For this etching, the citric acid solution was mixed with 30 % hydrogen peroxide (H_2O_2) which was added slowly.

Recipe	Components	Notes
3	$CitricAcid : H_2O_2$ 20 : 1	$CitricAcid$ 10 : 100

Table 3.3: Wet Etching recipes for nm

The mixing ratios of this recipes are listed in Table 3.3, where the chemicals are listed in the order in which they were poured for safety and stability. Acid was always added to water, and hydrogen peroxide was added last.

To etch the sample, a similar process as described in the previous section was utilized; however, in this case, a slower etching rate was used, and an additional step was added to remove the native oxide layer of GaAs using hydrochloric acid (HCl). Five beakers were prepared: the first containing HCl, the second containing DI water, the third containing the etching solution (Recipe 3) which was stirred at a safe speed that ensured proper mixing without splashing during the etching process (this stirring condition was maintained for all etching processes using a marked setting in the stirrer), and finally the fourth and fifth beakers containing deionized (DI) water, as shown in Fig. 3.6.

The sample was submerged in the first beaker with HCl for 30 seconds, then immersed in the second beaker with water for five seconds, followed by the standard etching sequence described above.

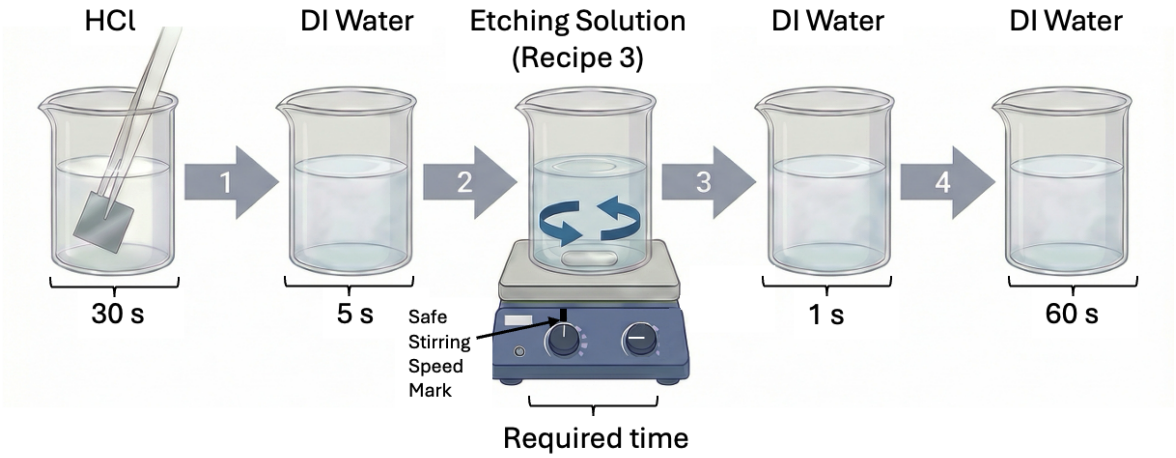

Figure 3.6: Etching workflow for *nm* range. Using sequential immersion in prepared beakers. The sample was handle with Teflon tweezers. The etching solution was stirred at a fixed speed, and the stirring velocity was marked on the equipment to ensure reproducibility

Before using Recipe 3, the optimal ratio between citric acid and H_2O_2 was investigated. Since this recipe was not taken from the literature, the objective was to achieve a controlled etch rate while maintaining a smooth surface. Fig. 3.7 shows the etch depth after 60 seconds for different citric acid concentrations; as the concentration of citric acid in the solution increases, the etch rate decreases.

AFM roughness measurements were used as a qualitative comparison between the 20:1 and 40:1 citric acid : H_2O_2 ratios. The surface roughness values correspond to the RMS roughness obtained from AFM analysis, which represents the standard de-

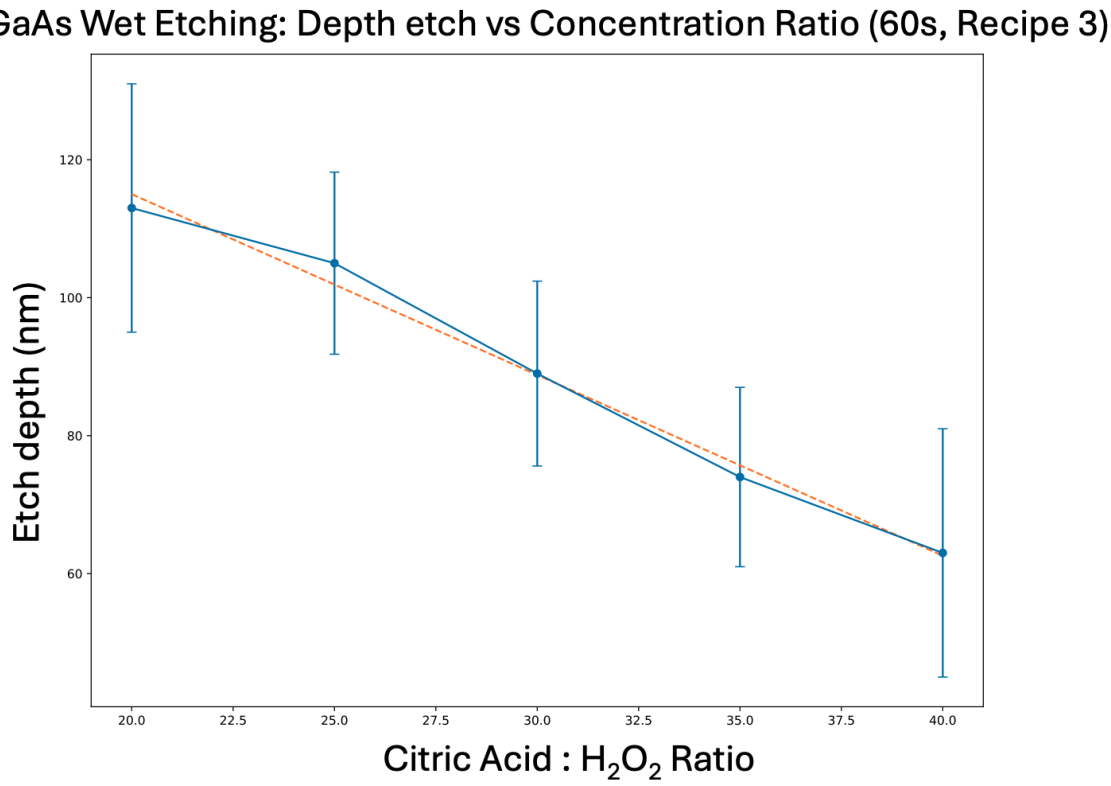

Figure 3.7: Etch depth after 60 s for different citric acid : H_2O_2 ratio concentrations for Recipe 3. The dashed line represents a linear fit used to estimate the dependence of etch rate on concentration. Error bars ($\sim \pm 10$ nm) correspond to the resolution limit of the profilometer, estimated from the RMS of the residuals obtained from the data fitting using a custom analysis code (Appendix A).

viation of the surface height distribution of single measurements. The 20:1 samples showed consistent roughness values (5.3 and 5.3 nm), whereas the 40:1 samples exhibited greater variation (4.6 and 8.8 nm). Therefore, the 20:1 ratio was considered more stable and was selected for the etch-rate analysis.

Fig. 3.8 shows the etch rate for a citric acid:H_2O_2 ratio of 20:1. The data are approximated by a linear fit, $y(cm) = 1.5(nm/s) \times t(s) + 25(nm)$, indicating an approximately constant etch rate in this regime.

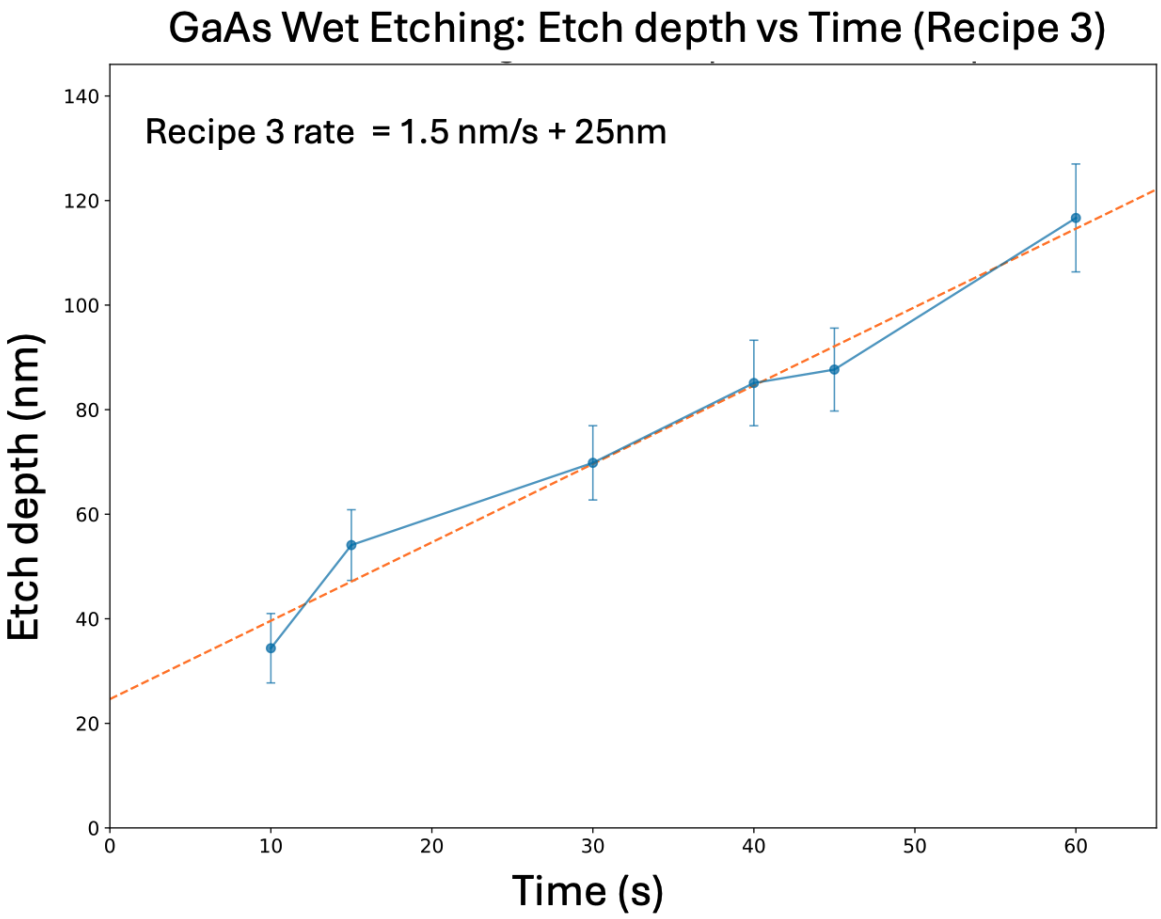

Figure 3.8: Etch rate as a function of citric acid to H_2O_2 ratio 20 : 1 for Recipe 3. The dashed line represents a linear fit used to estimate the dependence of etch rate on concentration. Error bars ($\sim \pm 10$ nm) correspond to the resolution limit of the profilometer, estimated from the RMS of the residuals obtained from the data fitting using a custom analysis code (Appendix A)

3.2.6 Unsuccessful recipes tested

Several additional etching recipes were explored during process development; however, they did not yield satisfactory results. Some recipes produced no measurable etching, while others showed inconsistent behavior, where certain samples etched and others did not. In some cases, wafer discoloration was observed, suggesting undesirable chemical modifications of the surface. All tested recipes are summarized in Table 3.4.

Recipe	Components	Expected Etch rate [nm/min]	Reference
I	$H_2O : H_3PO_4 : CitricAcid : H_2O_2$ 60 : 7.5 : 10 : 7.5	500	[11]
II	$H_2SO_4 : H_2O_2 : H_2O$ 1 : 4 : 50	2-2.5	[12]
III	$H_3PO_4 : H_2O$ and $H_2O_2 : CitricAcid$ 1:5 and 30 : 1	1	[12]
IV	$H_2O : H_3PO_4 : H_2O_2$ 1 : 1 : 45	600	[10]
V	$H_2O_2 : CitricAcid$ 1 : 1	600	[10] [9]
VI	$H_2SO_4 : H_2O_2 : H_2O$ 1 : 1: 100	N/A	Modify from recipe i
VII	$CitricAcid : H_2O_2$ x : 1 ; x= 20, 25, 30, 35	N/A	Modify from recipe v

Table 3.4: All recipes tested from GaAs etching.

Recipe I was effective for etching in the micrometer range but was not suitable for nanometer-scale etching, as the etch rate was insufficient for shorter processing times. Recipe II showed inconsistent etching behavior in the nanometer regime. Recipe III did not produce any observable etching, while Recipe IV resulted in noticeable surface discoloration. Recipe VI exhibited relatively high etch rates (40 nm/min) and increased surface roughness, with height variations of approximately 10 nm across the etched area, making it unsuitable for controlled nanometer-scale etching. Finally, variations of Recipe VII (cases X = 25, 30, and 35) were discarded because they resulted in higher surface roughness than the selected 20:1 ratio.

Overall, these recipes were not considered suitable for controlled and reproducible etching and were therefore excluded from further analysis.

Chapter 4

Summary and Conclusions

4.0.1 Summary of Key Findings

The spin-coating and exposure parameters used for both photolithography processes are summarized in Tables 4.1 and 4.2.

Machine	Photoresist	Spin Speed	Acceleration	Spin time	Soft bake
MJB3-Mask Aligner	AZ5214	2500 (rpm)	300	60 s	95°C, 60 s
Heidelberg μPG 101	AZ1505	4000 (rpm)	500	60 s	100°C, 50 s

Table 4.1: Coating parameters for photoresist

Machine	Photoresist	Exposure	Developer
MJB3-Mask Aligner	AZ5214	10 s	MIF726, 50s
Heidelburg μPG 101	AZ1505	10% of $20mW$, defocus:10, mode: 1x4	AZ726MIF, 50 s

Table 4.2: Exposure parameters for photoresist optimized

The etched rate and recipes optimized in this project are shown in Table 4.3.

Recipe	Components	Notes	Etch rate
1	$H_2O : H_3PO_4 : CitricAcid : H_2O_2$ 7.5 : 7.5 : 10 : 60	$CitricAcid$ 1 : 1	0.18 μ/min
2	$H_2O : H_3PO_4 : H_2O_2$ 45 : 4 : 1		0.34 μ/min
3	$CitricAcid : H_2O_2$ 20 : 1	$CitricAcid$ 10 : 100	1.5 nm/s + 25 nm

Table 4.3: Etching rates for Wet Etching recipes for GaAs

4.1 Limitations of the study

4.1.1 Discussion of Unsuccessful Recipes

Several factors were considered to explain the lack of reproducibility and effectiveness of the alternative etching recipes. Initially, the degradation of phosphoric acid (H_3PO_4) due to light exposure was suspected as a possible cause. However, this was ruled out by preparing fresh solutions and storing them in dark containers, which did not improve the etching performance. Additional tests were performed using similar recipes with different ratios of citric acid and ($H2O_2$) ; however, these variations also failed to produce consistent results. This suggests that the observed issues are not solely related to reagent degradation or simple concentration adjustments. It is important to note that wet etching processes can be highly sensitive to experimental conditions, including solution preparation, temperature, and surface state of the samples. Additionally, etchant can become saturated during use, which may further affect the etching rate and reproducibility. As a result, variations between processes can lead to significant differences in etching behavior.

4.2 Recommendations for future research

4.2.1 Important Process Parameters

The preparation and aging of the etchant solution were found to significantly influence the etching behavior. The citric acid solution was typically prepared one day prior to etching, while the complete etchant mixture (including H_2O_2) was allowed to stabilize for approximately 2 hours before use. The etchant was then used within a time frame of up to two weeks.

However, variations in etch rate were not studied over time. In principle, the process could be further optimized by precisely defining the timing between etchant preparation and use, both over days and within hours after mixing. These observations indicate that the etching process is sensitive to solution aging and suggest that tighter control of preparation timing is required for improved reproducibility.

4.2.2 Manipulation of Samples

Proper sample handling is critical to ensure reproducible wet etching results. Several practical considerations should be taken into account during the process.

First, cross-contamination of chemicals must be avoided. Tweezers should be rinsed between etching steps, and water containers must be cleaned and refilled between samples.

Second, when a sample is held with tweezers and submerged into the etching solution, this step—particularly for short etching times—should be performed as uniformly

as possible. Ideally, the entire wafer should come into contact with the etchant simultaneously. However, slight variations due to manual handling may still occur.

Finally, achieving consistent etching results also depends on a well-optimized photolithography process, with clean and properly prepared surfaces prior to etching. Therefore, inspecting the photoresist under a microscope before etching is a very important step.

Chapter 5

Theoretical Background

In this second part of the thesis, we discussed another process in microfabrication, the process of thermal oxidation of silicon to grow silicon dioxide SiO_2. Furthermore, we explore how this process can be integrated with pulsed laser deposition (PLD) to fabricate layered structures with material such as yttria stabilized zirconia (YSZ, ZrO_2) and cerium dioxide CeO_2, as well as their potential application in photonic devices.

5.1 Silicon and Silicon Dioxide

Silicon is one of the materials that is most widely used in microelectronics and photonics due to its stability and its central role in the semiconductor industry. In addition to its electronic properties, silicon is also important for photonic applications due to its relatively high refractive index compared to dielectric materials such as silicon dioxide. The contrast in refractive index between silicon (n $\approx$ 3.48 ; for λ = 1550 nm [13]) and silicon dioxide (n $\approx$ 1.44 ; for λ = 1550 nm [13]) is particularly important for photonic device applications, as it enables optical confinement in layered structures such as waveguides.

Silicon dioxide (SiO_2) is an insulating material, and can be formed on the surface of silicon in two ways: naturally, when silicon is exposed to air; or in a controlled manner through thermal oxidation processes.

5.1.1 Native Oxide and its Removal

At room temperature, when exposed to air, silicon can naturally grow a native oxide layer, called the native layer, which is an amorphous SiO_2 layer, typically with a thickness of a few nanometers (~ 2 nm) [14] and acts as a passivation or insulating layer that slows further oxidation. In microfabrication, the native layer is often considered an undesirable contaminant, but it can be removed using a dilute solution of hydrofluoric acid (HF) or a buffered hydrofluoric acid (BHF), which consist of HF and ammonium fluoride(NH_4F) [7][15]. The removal of SiO_2 occurs though the reaction:

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \tag{5.1}$$

The reaction produces hexafluorosilicic acid (H_2SiF_6), which is highly soluble in water, allowing the removal of silicon dioxide from the silicon surface. However, the concentration of HF decreases over time during the etching process.

In a buffered solution ($BHF = NH_4F + HF$), ammonium fluoride NH_4F acts as a buffering agent, maintaining a stable concentration of active fluoride ions (F^-), allowing a slower and more controlled removal of oxide and minimizes the attack on the photoresist layer [7][15].

5.1.2 Thermal Oxidation of Silicon

However, silicon dioxide can also be grown under controlled conditions, allowing precise control of its thickness. Thermally grown SiO_2, is commonly used in CMOS and MEMS technologies used as an insulating layer due to its excellent electrical properties[7].

One of the most common methods for forming a high-quality silicon dioxide is thermal oxidation at elevated temperatures. Thermal oxidation of silicon is performed inside a furnace at high temperatures (750-1100 °C) [16]. The growth rate and quality of SiO_2 depend on several parameters, including temperature, oxidation time, silicon crystal orientation, dopant concentration, oxidizing species and oxidizing species pressure.

Two primary oxidation methods are commonly used: dry and wet thermal oxidation. In dry thermal oxidation, oxygen gas is used as the oxidant,

$$\text{Dry thermal oxidation: } Si + O_2 = SiO_2$$

While, for wet oxidation, water vapor serves as the oxidizing agent;

$$\text{Wet thermal Oxidation: } Si + 2H_2O = SiO_2 + 2H_2$$

Wet thermal oxidation generally results in faster oxide growth rates, but the density and interface quality are lower compared to dry thermal oxidation. Due to the higher interface quality and equipment available, we use dry thermal oxidation in this project.

5.1.3 Oxidation Kinetics (Deal–Grove Model)

Silicon oxidation occurs when oxidizing species, such as O_2 or H_2O, diffuse through the oxide layer to react with silicon at the $Si - SiO_2$ interface. As the oxide layer thickens, the oxidant must travel a longer distance through the SiO_2 to reach the interface where the chemical reaction occurs. Therefore, growth mechanics involves two coupled processes: diffusion of the oxidizing species thought oxide and the reaction at the silicon interface [17].

The oxidation kinetic of silicon were first described by Deal and Grove in 1965 [18][7], which combines the diffusion and reaction mechanism, where in a simplified form, oxide thickens x follows:

$$x^2 + Ax = B(t + \tau) \tag{5.2}$$

where A and B are constants are related to the reaction rate and diffusion coefficient, and τ refer to the initial oxide thickens. This model describes two regimes: a linear region for short times,

$$x \approx \frac{B}{A}(t + \tau)(\text{thin oxide}) \tag{5.3}$$

and a parabolic regime at longer times.

$$x^2 \approx B(t + \tau)(\text{thick oxide}) \tag{5.4}$$

In this formulation, B/A corresponds to the linear rate coefficient, whereas B corresponds to the parabolic rate coefficient [7]. In this work, the focus remains on the experimental process parameters, these coefficients were not calculated

5.2 Silicon on Insulator (SOI) Platform

5.2.1 Structure and Fabrication Methods

SOI or Silicon-On-Insulator, is a platform composed of two layer of silicon, that sandwich a silicon dioxide layer. The top layer, called the device layer, is conformed by a thin layer of silicon. The second layer, or the buried oxide later is fromed of crystalline form silicon dioxide SiO_2. And the bottom layer is the handle layer, is again a layer of crystalline silicon, as shown in Fig. 5.1 .

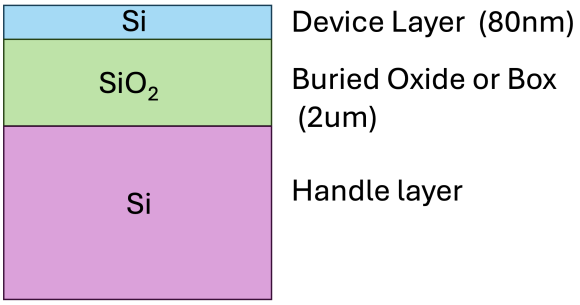

Figure 5.1: General Structure of a Silicon-On-Insulator (SOI)

SOI wafers are typically made by implanting oxygen into silicon to form a buried oxide layer (SIMOX) or by bonding two wafers and transferring a thin silicon later (Smart cut) [19].

5.2.2 Electrical and Photonic Advantages

SOI wafer is used in microfabrication as the buried layer (SiO_2) acts as isolating layer between the top layer and the substrate. This is generally used to avoid leaked current and reduce parasitic capacitance, allowing high-speed electronics [19]. However, it is also possible to use this platform in photonic systems, since SiO_2 provides optical confinement form the substrate since the high refractive index contrast between Si and SiO_2 (n_{si}>n_{SiO_2}), which can be used in integrated photonic circuits or photonic crystals [19].

As is well know, this is the condition required for the total internal reflection, show in Fig. 5.2

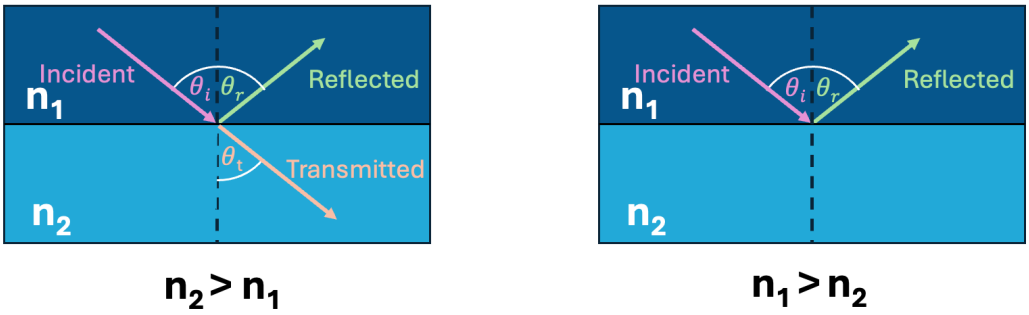

Figure 5.2: Behavior of light wave incident on a interface with $n_2 > n_1$ and $n_1 > n_2$ when refractive index of internal media is larger

5.3 Silicon-Based Multilayer Oxide Platforms

The design of multilayer oxide platforms relies on the structural compatibility and refractive index contrast between the constituent materials. Table 5.1 summarizes the key structural and optical properties relevant for this work.

Material	Structure	lattice constant [Å]	n ($\lambda = 1550$ nm)	Ref
Si	Diamond cubic	a=5.431	3.48	[13]
SiO_2	Amorphous	a=4.91, c=5.41	1.44	[20] [21] [7]
YSZ	Cubic Fluorite	a= 5.12	2.11-2.16	[22]
CeO_2	Cubic Crystal	a=5.41	2 - 1.9	[23] [21]

Table 5.1: Approximate values of crystal structure, lattice constant, and refractive index for silicon, silicon dioxide, YSZ, and cerium dioxide.

5.3.1 Yttria-Stabilized Zirconia (YSZ) Thin Films

Yttria-stabilized zirconia (YSZ) is a crystalline material with a cubic fluorite structure. This material cannot be grown epitaxially on SiO_2, which is an amorphous material, due to lattice mismatch, resulting in low adhesion and interfacial defects. However, YSZ can be grown on silicon (with a lattice mismatch of approximately 3.7–5.5% [24]), which is also a crystalline material with a diamond cubic structure and a relatively

similar lattice constant, as shown in Table 5.1.

YSZ is widely used as a buffer layer in oxide heterostructures due to its thermal stability and ionic conductivity. At elevated temperatures, YSZ exhibits oxygen ion transport [24], which plays a key role in enabling oxidation processes through the film. This property is particularly important for integrating oxide layers on silicon substrates.

5.3.2 Cerium oxide (CeO_2) Thin Films

Cerium dioxide (CeO_2) is a crystalline oxide with a cubic fluorite structure, similar to yttria-stabilized zirconia (YSZ), which enables good lattice compatibility between both materials. Due to this structural similarity, CeO_2 can be grown epitaxially on YSZ substrates with relatively low lattice mismatch (~ 5 %), making YSZ an effective buffer layer for subsequent oxide deposition. CeO_2 cannot be grown epitaxially on SiO_2, since it is an amorphous material. Although silicon is crystalline, its diamond cubic structure differs from the fluorite structure of CeO_2, as shown in Table 5.1, which limits the epitaxial quality of direct growth. Therefore, YSZ acts as an intermediate layer that improves the crystalline quality of CeO_2 grown on silicon.

5.3.3 Multilayer Structure: Si/SiO_2/YSZ/CeO_2

Due to the oxygen ion conductivity of YSZ at high temperatures, silicon can be oxidized through the YSZ film [24], forming a multilayer structure of Si/SiO_2/YSZ. A multilayer structure of Si/SiO_2/YSZ/CeO_2 is thus proposed. In this structure, silicon in the SIO wafer serves as the substrate, while thermally grown SiO_2 acts as an insulating and low-refractive-index layer. YSZ provides a crystalline template for oxide growth, and

CeO_2 functions as the high-refractive-index top layer. This multilayer configuration enables the integration of oxide materials with silicon technology.

5.3.4 Optical Confinement and Refractive index Contrast

The resulting multilayer structure, combined with the refractive index contrast between CeO_2, YSZ, and SiO_2 (see Table 5.1), enables optical confinement through total internal reflection, making it suitable for photonic device applications.

The operation of photonic devices in layered structures relies on the confinement of light within a high refractive index medium surrounded by lower index materials. When light propagates in a medium with refractive index n_1 and encounters an interface with a lower refractive index n_2, total internal reflection occurs if the incident angle exceeds the critical angle.

In multilayer structures such as $Si/SiO_2/YSZ/CeO_2$, the refractive index contrast between layers enables vertical optical confinement. This allows the structure to function as a planar waveguide, where light is guided within the higher-index layers while being confined by lower-index surrounding materials.

This refractive index engineering is essential for the design of integrated photonic devices, where controlling light propagation and confinement is required for applications such as waveguides, resonators, and optical interconnects.

In addition, precise control of layer thickness and refractive index enables the design of waveguides that support single optical modes, which is important for minimizing dispersion and improving device performance. For planar waveguides, this condition

can be described using the normalized frequency parameter V:

$$V = \frac{2\pi}{\lambda} t \sqrt{n_{\text{core}}^2 - n_{\text{clad}}^2} \tag{5.5}$$

where t is the thickness of the guiding layer, λ is the wavelength of light, and n_{core} and n_{clad} are the refractive indices of the core and surrounding materials, respectively. Single-mode operation occurs when $V < \pi$.

This relation in equation 5.5 [25] shows that controlling the thickness of thin films is essential for defining the optical behavior of the structure. Therefore, thin film deposition and oxidation processes are critical for achieving the desired optical confinement and mode control in photonic devices.

5.4 Thin Film Deposition Technique

Thin films can be deposited using various techniques, such as sputtering, chemical vapor deposition (CVD) [7]. However, in this work, PLD is chosen due to its ability to preserve stoichiometry and enable high-quality growth of complex oxide materials. High-quality thin films are essential for photonic devices, as defects, roughness, or deviations in composition can introduce optical losses and degrade light confinement.

5.4.1 Pulsed Laser Deposition (PLD)

Pulsed laser deposition (PLD) is a physical vapor deposition technique used for thin film deposition and multilayer growth [26]. The process begins with the removal of material from a solid target through laser ablation. The laser energy and pulse duration drive this process, generating a highly energetic plasma plume composed of atoms,

ions, and clusters. This plume expands toward the substrate, where the material condenses to form a thin film. The process is carried out in a chamber with a controlled atmosphere, such as vacuum or low-pressure oxygen.

PLD is particularly suitable for the deposition of complex oxide materials such as YSZ and CeO_2, as it enables good stoichiometric transfer from the target to the film. It also allows precise control of key parameters, including substrate temperature, oxygen pressure, laser fluence, and repetition rate, which directly affect film quality and crystallinity. In this work, PLD is used to grow YSZ and CeO_2 thin films on silicon-based substrates, enabling the fabrication of the multilayer structure described in Section 2.3 for photonic applications.

5.5 Application in Photonic Devices

The multilayer structure $Si/SiO_2/YSZ/CeO_2$ can be used as a platform for planar waveguides due to the refractive index contrast between its constituent layers. In such systems, light is confined within a high-refractive-index layer and guided along the structure through total internal reflection. In this configuration, CeO_2 acts as the high-refractive-index layer, while SiO_2 provides a lower-index surrounding medium. This index contrast enables vertical confinement of light, allowing propagation along the plane of the film. Planar waveguides are fundamental components in integrated photonic circuits, as they enable controlled transmission of optical signals with low loss. The ability to engineer refractive index profiles in multilayer oxide systems makes this platform particularly suitable for such applications. This platform can be further integrated with microfabrication techniques, such as reactive ion etching (RIE), to define photonic structures including waveguides and graded-index geometries.

Chapter 6

Silicon Oxidation: Methodology, Optimization and Results

This chapter describes the fabrication process and experimental procedures used to develop the $Si/SiO_2/YSZ/CeO_2$ platform. The focus is on the optimization of dry thermal oxidation parameters and the subsequent fabrication of the complete multi-layer structure.

The chapter is organized as follows. First, an overview of the complete fabrication process is presented. Then, the wafer specifications and preparation are described followed by detailed descriptions of the dry thermal oxidation process, pulsed laser deposition (PLD), and characterization procedures.

6.1 Process Overview

The objective of this work was to develop and evaluate a fabrication process for a multilayer platform consisting of $Si/SiO_2/YSZ/CeO_2$. This process involves three main steps: (i) deposition of YSZ by pulsed laser deposition (PLD), (ii) dry thermal oxidation (DTO) of the silicon substrate, and (iii) deposition of CeO_2 by PLD; as illustrated in Fig. 6.1.

However, to establish the oxidation conditions, a series of experiments were first

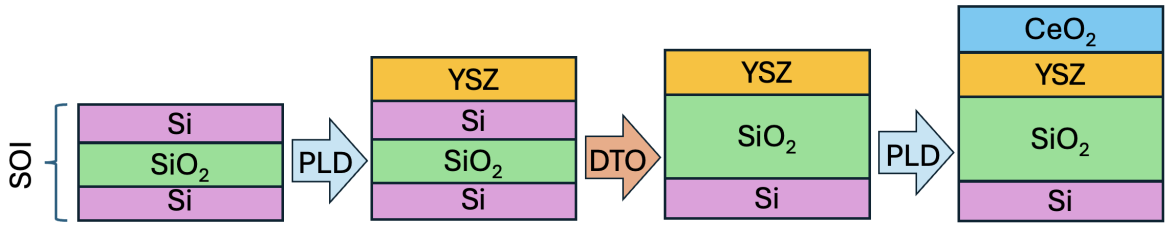

Figure 6.1: Schematic of the complete fabrication process for the $Si/SiO_2/YSZ/CeO_2$ multilayer structure using pulsed laser deposition (PLD) and dry thermal oxidation (DTO).

performed on silicon and silicon-on-insulator (SOI) substrates, which were oxidized using dry thermal oxidation, as shown in Fig. 6.2. Silicon substrates were primarily used for parameter optimization due to their lower cost and availability, allowing for systematic testing before applying the optimized conditions to SOI structures. These tests were used to determine the parameters required to achieve controlled SiO_2 growth, particularly for the oxidation of the top silicon layer in SOI structures.

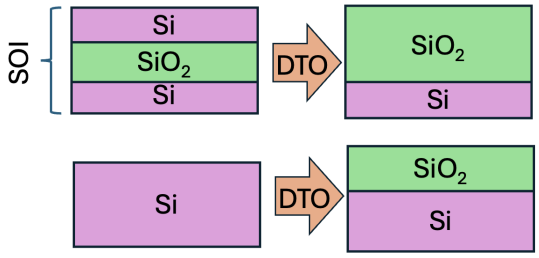

Figure 6.2: Schematic of the dry thermal oxidation (DTO) process used for parameter optimization on silicon and silicon-on-insulator (SOI) substrates.

Once the oxidation parameters were identified, a single sample was processed through the complete fabrication sequence. In this case, YSZ was first deposited on the substrate, followed by dry thermal oxidation, and finally CeO_2 deposition. This sample serves as a proof of concept for the proposed multilayer structure.

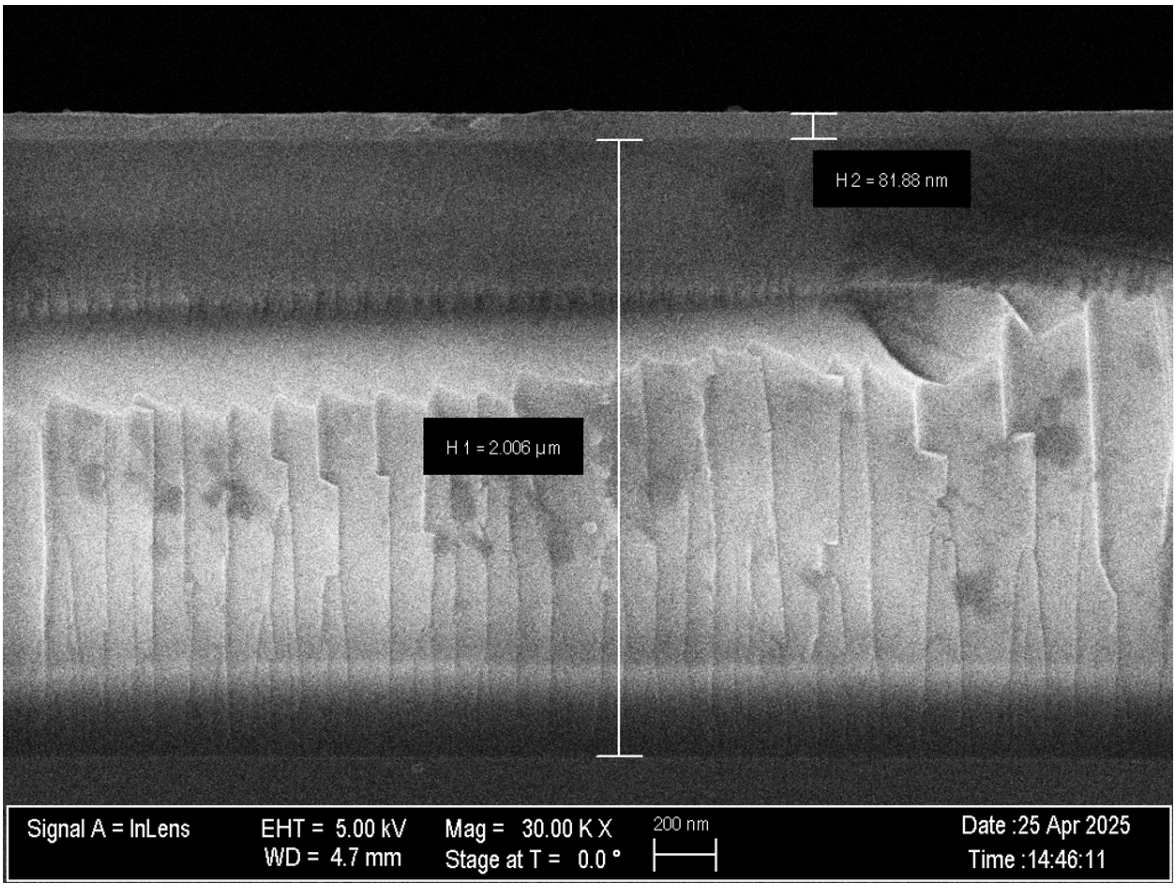

Figure 6.3: SEM measurement of cross section of SOI. Top region refers to the top layer of silicon (Si). Second region, refers to buried oxide or box layer of silicon dioxide (SiO_2). Third region is not observed and correspond to the handle layer of silicon (Si)

6.2 Wafer Specifications and Preparation

6.2.1 Silicon-On-Insulator (SOI)

SOI samples were characterized using cross-sectional imaging, as shown in Fig. 6.3, where the thicknesses of the device layer ($\sim$80 nm) and the buried oxide layer ($\sim$2 μm) were confirmed. These values are summarized in Table 6.1.

Layer	Material	Thickness
Device layer	Si	80 nm
Buried Oxide	SiO_2	2 μm
Handle layer	Si	$\sim 722\mu m$

Table 6.1: SOI dimension obtained from SEM measurements

6.2.2 Cleaving Samples

The wafers were cut into squares of 0.5 cm x 0.5 cm. Some samples were cut using a wafer dicer system using the following parameters: (mode: 10; index 1: 90 mm; index 2: 90 mm; Height: 0.3 mm; Thickness: 0.975 mm; Angle: 90 degrees; cutting speed: 4.0 mm/sec; cut increment: 1.270 mm; spindle speed: 20,000.0 RPM). Other samples were manually cleaved.

The silicon wafers (thickness 0.5 mm) were easily cleaved due to their crystalline structure. For manual cleaving, a straight scribe line was made across the entire area that needed to be cleaved using a diamond scribing pen. The scribing motion was repeated 2-4 times along the same line and in the same direction to ensure a well-defined fracture path. After scribing, the wafer was held using both index fingers and thumbs, and the scribed line was positioned on a cleaving pin. By applying a controlled, gentle downward force, the wafer was cleanly fractured along the scribed line. This is shown in Fig. 6.4 a).

In contrast, silicon-on-insulator (SOI) wafers are more robust (0.75 mm) due to their layer structure, making manual cleaving more difficult. Therefore, a modified breaking technique was employed. After the scribing line was defined with a diamond scribing pen, the sample was placed between two microscope glass slides. The wafer was positioned such that the scribed line was aligned with the edge of the supporting

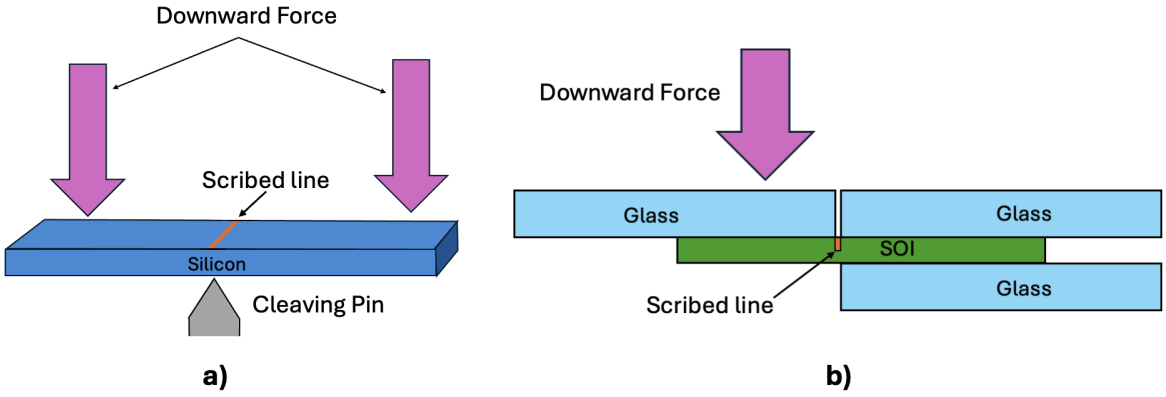

Figure 6.4: Schematic representation of the manual cleaving procedures for a) Cleaving pin method used to cleaved Silicon and b) Glass stack method used to cleaved Silicon-on-insulator SOI wafer

glass slide, leaving the portion to be cleaved slightly suspended. A third glass slide was then placed on top of the suspended wafer region. By applying uniform, controlled pressure using the whole index finger on the upper glass slide, a downward bending force was introduced along the scribed line, resulting in a clean cleave of the SOI sample. This method is shown in Fig. 6.4 b).

This method of cleaving was used to prepare small samples for cross-sectional measurements in both silicon and SOI samples for subsequent processing and characterization.

6.2.3 Cleaning samples

The samples were cleaned using a standard solvent-based cleaning procedure consisting of four steps. One bath of deionized (DI) water, followed by acetone, then isopropyl alcohol (IPA) and finally another bath of deionized (DI) water. Each step was performed in an ultrasonic bath for 5 min, ensuring that cavitation bubbles were observed on the surface during the cleaning process. Finally, each sample was dried using a nitrogen gun. This was the recipe used in the laboratory outside the cleanroom that did not

have a plasma asher. However, the recipe mentioned in section 3.1.1 is also suitable for these samples.

6.3 Dry Thermal Oxidation System and Process

6.3.1 System Furnace Configuration

For dry thermal oxidation, a Lindburg Tube Furnace capable of operating up to 1500°C was used. The furnace contains a tube where samples are placed and uniformly heated. The furnace was connected on one side to oxygen (O_2) and argon (Ar) gas cylinders, and on the opposite side a removable outlet was connected via a hose to a water-filled bubbler system. The system was equipped with valves and flow meters to regulate and monitor the gas flow entering the furnace. A power source was used to set and control the heating parameters of the furnace.

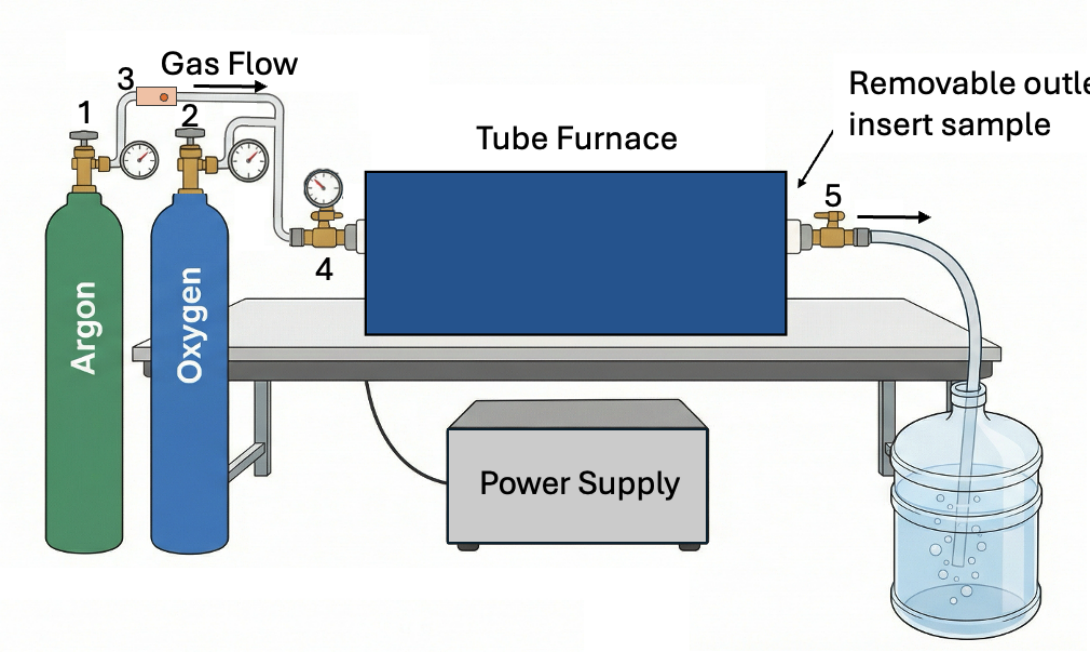

Figure 6.5: Schematic setup of the tube furnace system, including gas cylinder and bubbler. The valves are numbered for easy identification

As observed in Fig.6.6 a), each gas cylinder had a gas pressure regulator (valves 1 and 2). The argon gas cylinder was also connected to a Brooks Instrument MR300 Series variable flow meter (valve 3). Then, both gas cylinders were connected to the same hose, which led to the inlet valve of the tube furnace (valve 4); where the pressure of the incoming gas can be monitored. After the gas passes through the furnace, the gas is released through a final valve (valve 5) and, via a hose is directed to the bubbler system, which helps to regulate the gas flow, allows cooling of the hot exhaust gas, and dissolves possible chemical residues in the gas.

Further details about the bubbler system are provided in Appendix C.

6.3.2 Gas Flow Regulation and Bubbler System

During the oxidation process, the furnace was operated and the system required a continuous gas flow. However, because the exhaust gas leaving the furnace was at high temperature, a slow gas release is desired to avoid melting the hose connected to the bubbler system.

The release rate was monitored using the bubbler system by observing the number of bubbles per second. A high gas release rate produced many bubbles and may melt the hose. For this reason, valve 5 is kept slightly open, approximately 1-2 degrees, resulting in only a few bubbles, about one bubble per second. The hose is submerged close to the bottom of the container. Because the outlet pressure is kept low, the gas inlet must also remain low. Therefore, valve 4 is also slightly opened, approximately one quarter of a turn. Since valve 4 is open further than valve 5, the gas pressure inside the furnace increased toward the desired pressure. Thus, the valves must be carefully adjusted to maintain a stable flow of argon and oxygen inside the furnace

while ensuring a low exhaust flow rate.

The oxidation procedure was established for the following process parameters: argon pressure of 0.02 MPa and oxygen pressure of 0.05 MPa. More details about this calibration are discussed in the Results section. Under these conditions, valve 1 was set to 0.02 kPa and valve 2 to 0.06 kPa, while valve 3 was set to 0.1. Although the valve calibration may vary, the internal gas pressures must follow the values defined in the process parameters and the exhaust flow must remain low to avoid melting the plastic hose. These values are summarized in Table 6.2

Valve	Parameter
1	0.02 KPa
2	0.06 KPa
3	0.1
4	Open less 1/4 rotation
5	Open around 1-2 degrees

Table 6.2: Valve settings used to obtain the process pressures of argon (0.02 MPa) and oxygen (0.05 MPa).

6.3.3 Sample Insertion Procedure

The cleaned sample was placed at the center of a ceramic crucible, where the temperature is most uniform. Each crucible is stored covered with aluminum foil and is used to process the same type of sample to avoid contamination. To insert the sample, valve 5 is removed and the sample is carefully introduced into the furnace. The crucible is pushed inside using a metal rod that has a mark indicating the position corresponding to the center of the furnace, where the temperature is more uniform and reaches the highest value, this is illustrated in Fig. 6.6 a). While the crucible is being pushed inside, it may rotate, as shown in Fig. 6.6 c). This can be corrected by gently pushing

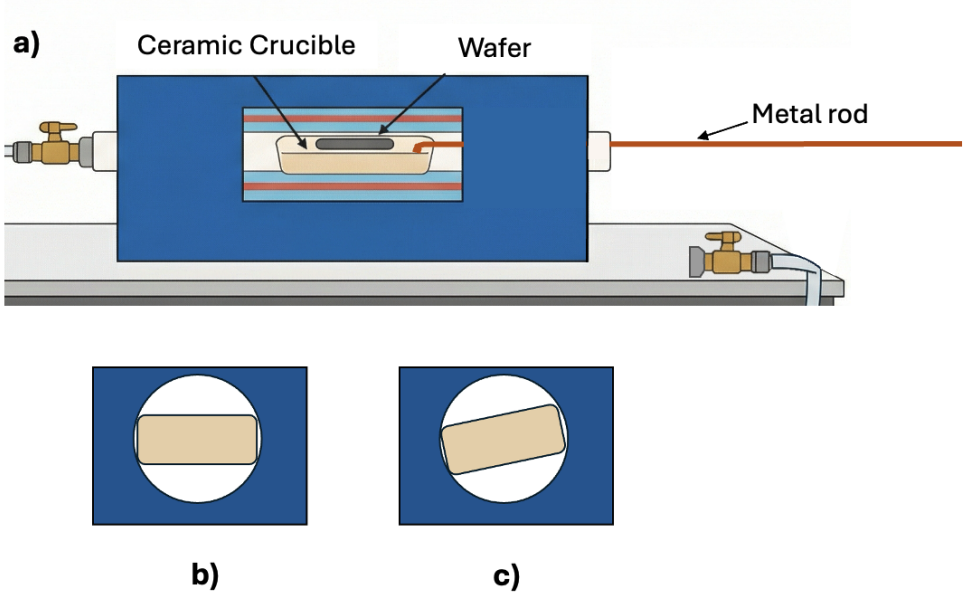

Figure 6.6: a) Interior furnace with the sample inside. A metal row is used to insert and remove the sample from the furnace (b and c) View and interior of the ceramic tube (b) Correct position of the crucible, aligned parallel to the grown (c) Incorrect position of the crucible, it rotated while been pushed into the furnace

the side of the crucible until it reaches the correct orientation, as shown in 6.6 b). It is important to perform this step gently and avoid touching the walls of the tube furnace, since the tube is fragile and can fracture if excessive pressure is applied.

After the sample is positioned, the metal rod is carefully removed, making sure not to touch the walls of the furnace tube. Finally, valve 5 is placed back in position. It is important to ensure that it is properly tightened to avoid gas leaks. This can be checked if bubbles are formed in the bubbler system.

After oxidation the sample cools down over approximately 12 hours, the sample can be removed. Valve 5 is removed, and the crucible is pulled outside the furnace using the bent part of the metal rod. The sample is stored in a separate container, and the ceramic crucible is stored covered in aluminum foil to avoid contamination.

6.4 Dry Thermal Oxidation Process

6.4.1 Characterization Techniques

The growth of silicon oxide and the structural properties of the multilayer platform were characterized using X-ray diffraction (XRD) and X-ray reflectivity (XRR) with a Rigaku SmartLab X-ray diffractometer. The XRR data were analyzed using GenX software to extract film thickness. Additional thickness measurements and structural analysis were carried out using scanning electron microscopy (SEM), based on cross-sectional images obtained with a Zeiss Neon FE-SEM/FIB dual-beam system. For samples with the complete $Si/SiO_2/YSZ$ structure, transmission electron microscopy (TEM) was used to further analyze the layer interfaces and overall structure. These techniques were used to analyze all oxidation and deposition results presented in the following sections.

6.4.2 Optimization of Parameters

To start oxidizing the sample, the power source is set to increase the temperature from room temperature (RT $\approx$ 23°C) to the desired temperature at a rate of 300°C/hr or 5°C/min. The sample is heated to the target temperature, where it is held at the maximum temperature for a required time **t** depending on the desired silicon oxide thickness. In the furnace control system, this hold time is referred to as the "dwell." Then, the furnace heating process is stopped, allowing the sample to cool down until it reaches room temperature again.

First, oxidation experiments were conducted at 1100 °C considering only oxygen flow (Table 6.3). Under these conditions, oxidation occurred rapidly due to the high

oxygen concentration.

Table 6.3: Thermal oxidation results for Si samples at 1100 °C only oxygen flow.

Sample	Material	t [min]	O_2 [MPa]	XRR [nm]	SEM [nm]	[nm/ min]
MA1	Si	5	0.10	138	150	28.8
MA2	Si	60	0.05	NP	370	6.2

Dry thermal oxidation of silicon requires both oxygen and elevated temperatures (700–1200°C). Since the sample is intended to be oxidized only during the maximum temperature stage, argon gas (0.02 MPa) is used to avoid any oxide formation while the sample is heating. Then, when the temperature reaches the target (maximum) temperature, the argon valve is closed and the oxygen valve is opened. With the oxygen gas (0.05 MPa), the maximum temperature is maintained for the defined time **t**. Finally, to cool down the sample, the oxygen valve is closed and the argon valve is opened again until the sample cools down to 400°C, where it is no longer possible to grow oxide. At this point, the argon valve is closed to avoid wasting extra gas.

Subsequently, oxidation experiments were conducted at 1100 °C with both oxygen and argon flow, as summarized in Table 6.4.

Table 6.4: Thermal oxidation results for Si samples at 1100 °C with argon flow of 0.02 MPa.

Sample	Material	t [min]	O_2 [MPa]	XRR [nm]	SEM [nm]	[nm/min]
MA4	Si	1	0.05	39	40	40
MA3	Si	10	0.05	80	80	8

However, the oxidation rate at 1100 °C remained too high for the desired level of control, as slower oxidation rates are typically associated with improved oxide quality. Therefore, additional experiments were performed at a lower temperature of 900 °C

with controlled argon and oxygen flow (Table 6.5), resulting in a more suitable and controllable oxidation rate. Therefore, this condition was selected as the optimal parameter.

Table 6.5: Thermal oxidation results for Si and SOI samples at 900 °C, with argon flow of 0.02 MPa and oxygen flow of 0.05 MPa.

Sample	Material	t [min]	XRR [nm]	SEM [nm]	[nm/min]
MA6	Si	2	9	10	5
MA5	Si	10	22	23	2.3
SOI-2	SOI	20	30	-	1.5

The temperature profile of the oxidation process and gas utilized are shown in Fig. 6.7, and summarized in Table 6.6.

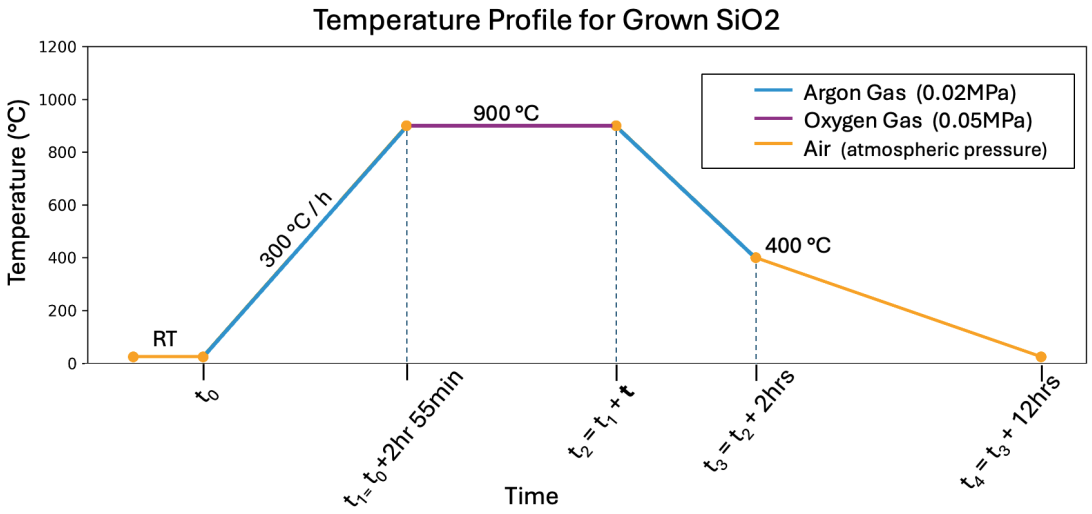

Figure 6.7: Temperature profile for the growth of silicon oxide by dry thermal oxidation. Thickness of SiO_2 grown depends on the time **t** at 900 °C and in contact to Oxygen. The sample is allowed to cool overnight before being removed from the furnace

Argon	0.02 MPa
Oxygen	0.05 MPa
Ramp rate	300°C/hr or 5°C/min
Target temperature	900°C

Table 6.6: Process parameters for silicon oxidation for a time **t** .

6.5 Pulsed Laser Deposition of YSZ and CeO_2

6.5.1 Yttria-stabilized zirconia (YSZ)

The SOI sample used in this study (PP181) was coated with yttria-stabilized zirconia (YSZ) thin films prior to the oxidation process. The deposition parameters are summarized in Tables 6.7.

Post-deposition annealing was performed at the same temperature as the final stage of the temperature profile.

Parameter	Value
Film	YSZ
Substrate	SOI
Chamber	RHEED
Target-to-substrate distance	$\sim 4.8cm$
Temperature Profile sequence 1	500°C - 20°C/min
Temperature Profile sequence 2	850°C - 15°C/min
Temperature Profile sequence 3	940°C - 10°C/min
Vacuum before oxygen flow	1.20×10^{-5} Torr
Substrate temperature	800°C
Annealing with Oxygen	30 min at 10 mTorr
Expected thickness	9nm

Table 6.7: PLD growth parameters for the YSZ deposition on sample PP181

The sample was then oxidized using the optimized parameter for grown of silicon dioxide. The process was repeated two times, as summarized in Table 6.8.

Table 6.8: Thermal oxidation of sample PP181 (SOI/YSZ).

Process	Material	t [hr]	XRR [nm]	TEM [nm]	XRD
1	SOI/YSZ	2	N/A	4(YSZ) 8 (YSZ) 40 (SiO_2)	YSZ (100) Si (400) YSZ (200)
2	SOI/YSZ	8	N/A	N/A	YSZ (002) YSZ (004)

An initial annealing step of 2 hours was insufficient to fully oxidize the silicon, as indicated by the XRD measurement Fig. 6.8 and TEM measurement Fig. 6.9. This suggests that oxygen diffusion through the YSZ layer is slower than through SiO_2, but not inhibited.

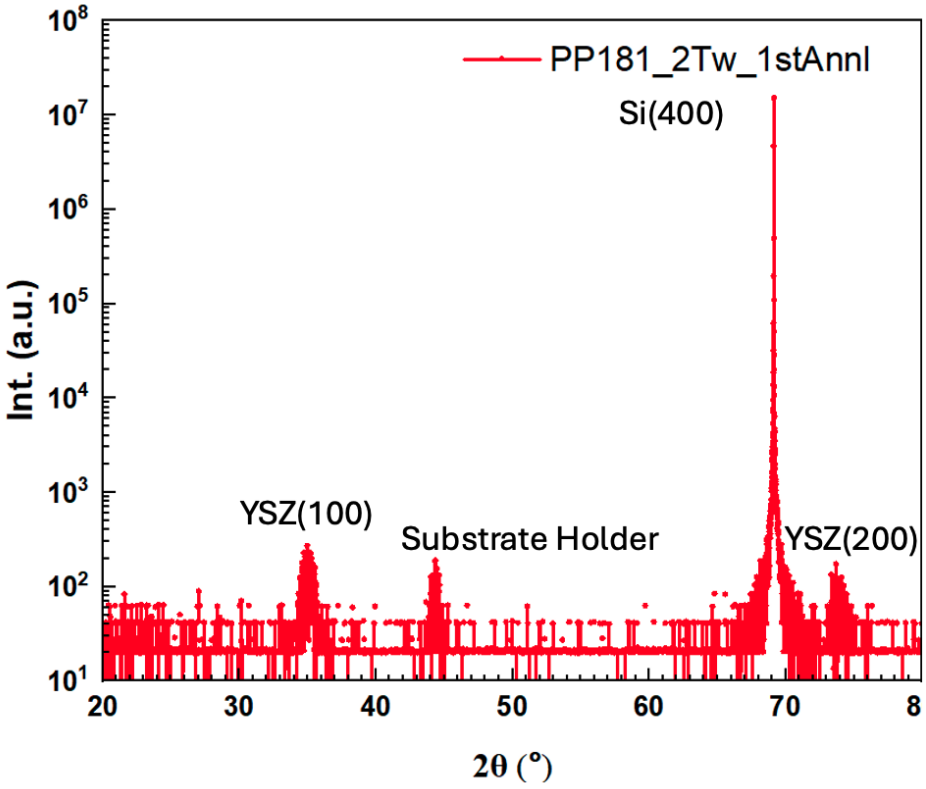

Figure 6.8: XRD measurement of sample PP181 after pulsed laser deposition of YSZ, dry thermal oxidation for a total of 2 hours

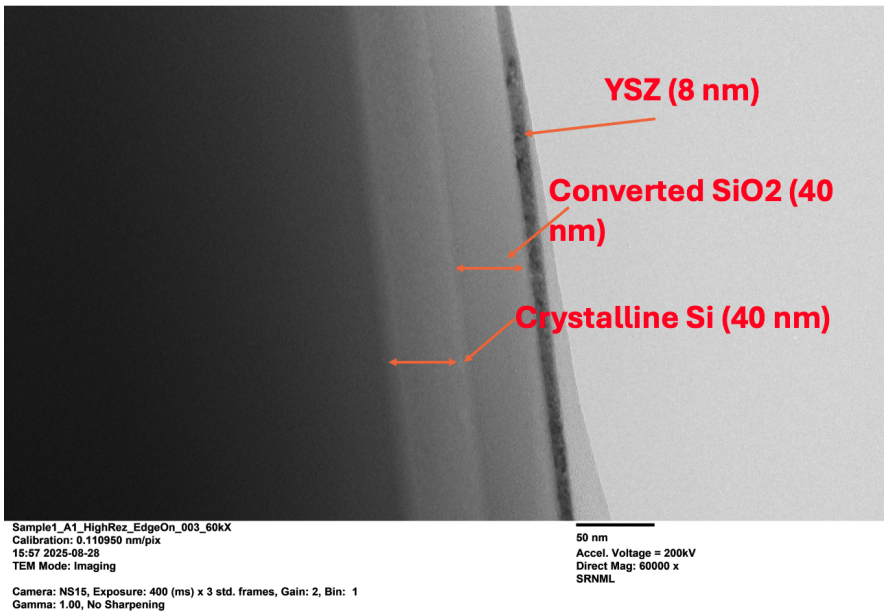

Figure 6.9: TEM image of the $Si/SiO_2/YSZ$ structure after oxidation for a total of 2 hours

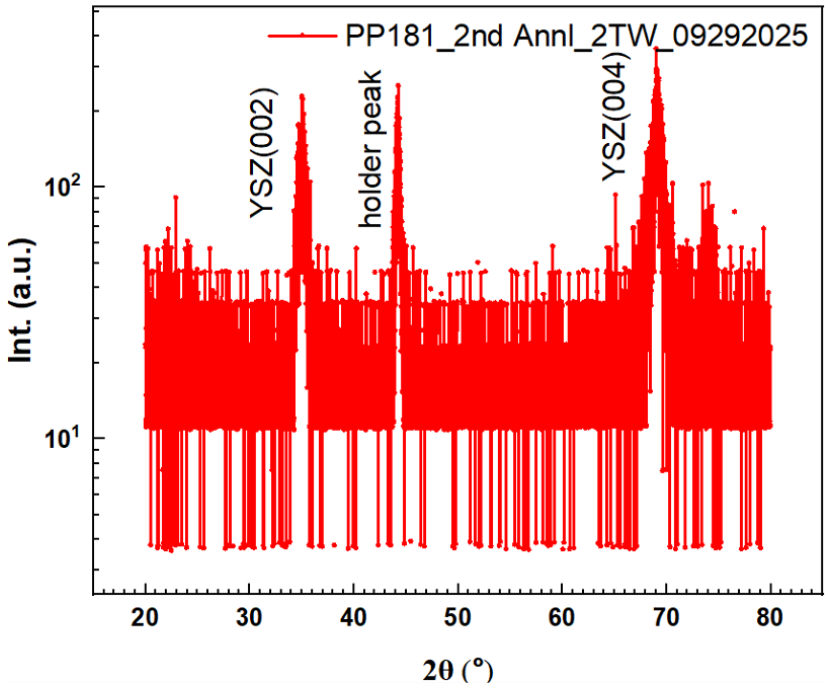

Figure 6.10: XRD measurement of sample PP181 after pulsed laser deposition of YSZ, dry thermal oxidation for a total of 10 hours

A second annealing step of 8 hours was then performed, which resulted in complete oxidation of the silicon device layer, forming a $Si/SiO_2/YSZ$ structure. This was confirmed by X-ray diffraction (XRD), which showed only the presence of YSZ at the surface (Fig. 6.10).

6.5.2 Cerium Dioxide

Finally, a CeO_2 layer was deposited on sample PP181 with parameters shown in Table 6.9.

Parameter	Value
Film	CeO_2
Substrate	YSZ , Si(100)
Chamber	RHEED
Target-to-substrate distance	$\sim 5.5cm$
Temperature Profile sequence 1	500°C - 20°C/min
Temperature Profile sequence 2	850°C - 15°C/min
Temperature Profile sequence 3	940°C - 10°C/min
Vacuum before oxygen flow	1.20×10^{-5} torr
Substrate temperature	800°C
Annealing with Oxygen	30 min at 10 mTorr
Expected thickness	6nm

Table 6.9: PLD growth parameters for the CeO_2 deposition on sample PP181.

XRR measurements confirmed the presence of the CeO_2 thin film on the surface, shown in Fig. 6.11.

It is important to note that XRR is primarily sensitive to surface and near-surface layers, making it difficult to accurately determine the thickness of buried SiO_2 when covered by YSZ. In such cases, transmission electron microscopy (TEM) is required for direct thickness measurement. However, only XRD measurements were obtained for this last part of the sample process.

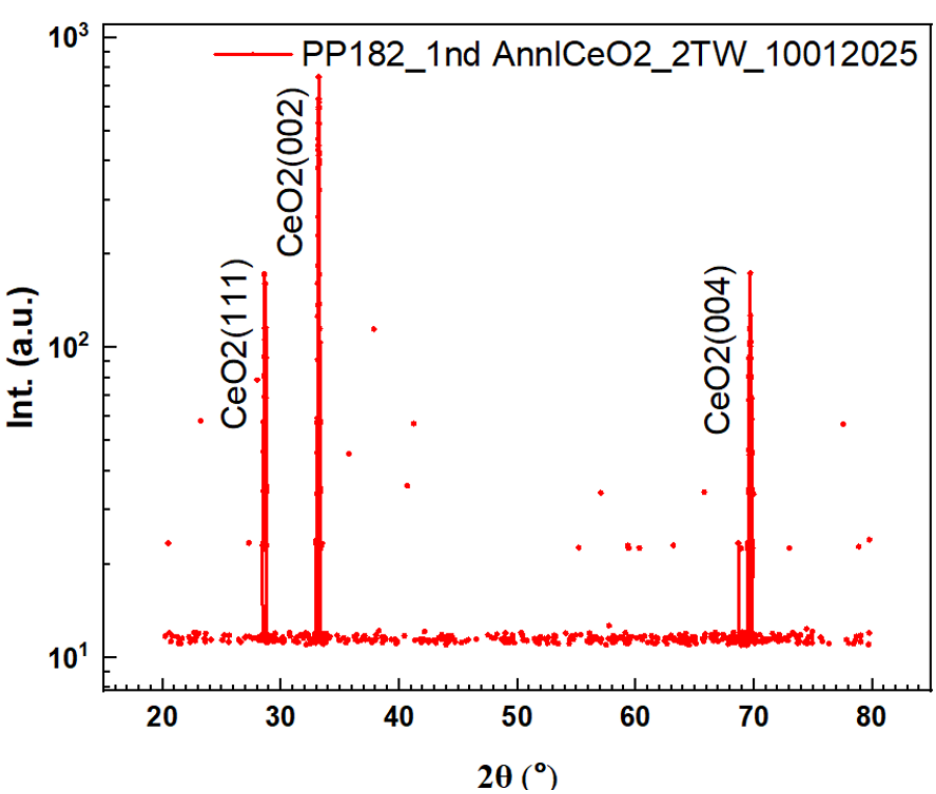

Figure 6.11: XRD measurement of sample PP181 after pulsed laser deposition of YSZ, dry thermal oxidation for a total of 10 hours, and final deposition of CeO_2.

Chapter 7

Conclusions and Discussion

7.1 Conclusion

It was demonstrated that it is possible to thermally oxidize a silicon-on-insulator (SOI) wafer through a YSZ layer. The results indicate that oxygen diffusion through the YSZ layer is slower than through SiO_2; however, oxidation is not inhibited. This behavior is consistent with reports in the literature [24], where oxidation through YSZ occurs but requires longer annealing times.

XRD measurements confirmed that crystalline YSZ and CeO_2 layers were successfully deposited, indicating that the structural quality of the multilayer system was preserved during processing.

A quantitative analysis of oxidation kinetics, including extraction of the linear (B/A) and parabolic (B) rate constants from the Deal–Grove model, was not achieved. This was due to the limited number of samples and the experimental constraints associated with characterization. In particular, while oxidation in bare SOI samples can be monitored using XRD, samples with YSZ layers require TEM analysis to accurately determine the SiO_2 thickness, which significantly increases measurement time and limits throughput.

Despite these limitations, it was observed that a total annealing time of approximately 10 hours was sufficient to fully oxidize the silicon device layer through the YSZ film, enabling the subsequent deposition of CeO_2 and the formation of a $Si/SiO_2/YSZ/CeO_2$ multilayer structure.

Overall, this work demonstrates the feasibility of integrating thermal oxidation with crystalline oxide layers, providing a pathway toward the development of silicon-based photonic platforms.

7.2 Discussion

The results obtained from sample PP181 represent an initial demonstration of the feasibility of this multilayer platform. While structural characterization confirms successful oxidation and deposition, further studies are required to evaluate the functional properties of the system.

In particular, optical characterization (e.g., refractive index, optical losses) and electrical measurements will be necessary to assess the suitability of this platform for photonic device applications.

The limited oxidation kinetics analysis highlights a key experimental challenge: the need for multiple samples and efficient characterization techniques. Future work should focus on developing faster or alternative methods to estimate oxide thickness in buried structures, reducing reliance on time-intensive TEM measurements. In particular, it would be valuable to evaluate whether cross-sectional SEM can serve as a suitable al-

ternative for thickness estimation in place of TEM.

7.3 Alternative Materials for the Platform

Other materials with oxygen ion conductivity similar to YSZ, such as calcia-stabilized zirconia (CSZ), may also be considered as potential platforms for multilayer structures [27]. These materials could provide similar functionality in enabling oxidation through a crystalline oxide layer. However, further investigation is required to evaluate their structural compatibility, oxidation behavior, and integration with silicon-based systems.

7.3.1 Additional Considerations

Since thermal oxidation occurs in all directions of the silicon substrate, it may be desirable to prevent oxidation of the bottom surface. This can be achieved by protecting the silicon with a silicon nitride (Si_3N_4) layer, which acts as an oxidation barrier [24].

Appendix A

Python Script for Profilometer Data Processing

This appendix provides the Python script used to process profilometer XML data, using local polynomial smoothing, calculate step height using percentile-based level separation, and determining RMS measurement uncertainty associated with the profilometer resolution.

A.1 Profilometer Data Processing

The following Python script was used to process the profilometer data.

```
import numpy as np
import xml.etree.ElementTree as ET

# --- Load profilometer data from XML
(x in mm, y in Angstroms) ---
tree = ET.parse("input_file.xml")
root = tree.getroot()

x_vals, y_vals = [], []
```

```
for elem in root.iter():
    tag = elem.tag.lower()
    if tag.endswith("x") and elem.text:
        x_vals.append(float(elem.text))
    if tag.endswith("z") and elem.text:
        y_vals.append(float(elem.text))

x = np.array(x_vals)
y = np.array(y_vals)

# ── Local polynomial smoothing of the profile ──
def smooth_fit(xv, yv, window, deg):
    if window % 2 == 0:
        window += 1
    half = window // 2
    y_fit = np.zeros_like(yv)

    for i in range(len(yv)):
        i0 = max(0, i - half)
        i1 = min(len(yv), i + half + 1)
        xs = xv[i0:i1]
        ys = yv[i0:i1]

        x0 = xs.mean()
        coeff = np.polyfit(xs - x0, ys, deg)
        y_fit[i] = np.polyval(coeff, xv[i] - x0)
```

```
    return y_fit

y_fit = smooth_fit(x, y, window=41, deg=1)

# --- Convert Angstroms to Nanometer ---
ANGSTROM_TO_NM = 0.1

# --- RMS residual in nm (from residuals) ---
residuals = y - y_fit
RMS_residual_nm = np.sqrt(np.mean(residuals**2)) *
ANGSTROM_TO_NM

# --- Step height in nm using percentile-
based level separation ---
low_percentile = 10
high_percentile = 90

low_vals = y_fit[y_fit <=
np.percentile(y_fit, low_percentile)]
high_vals = y_fit[y_fit >=
np.percentile(y_fit, high_percentile)]

low_level = np.median(low_vals)
high_level = np.median(high_vals)
height_nm = (high_level - low_level) * ANGSTROM_TO_NM
```

Appendix B

Mask P and N Connector

All masks were generated using Python with the PHIDL library [4], which produces GDS files that were subsequently visualized using KLayout. This approach was selected for its precision and flexibility, particularly when defining small features.

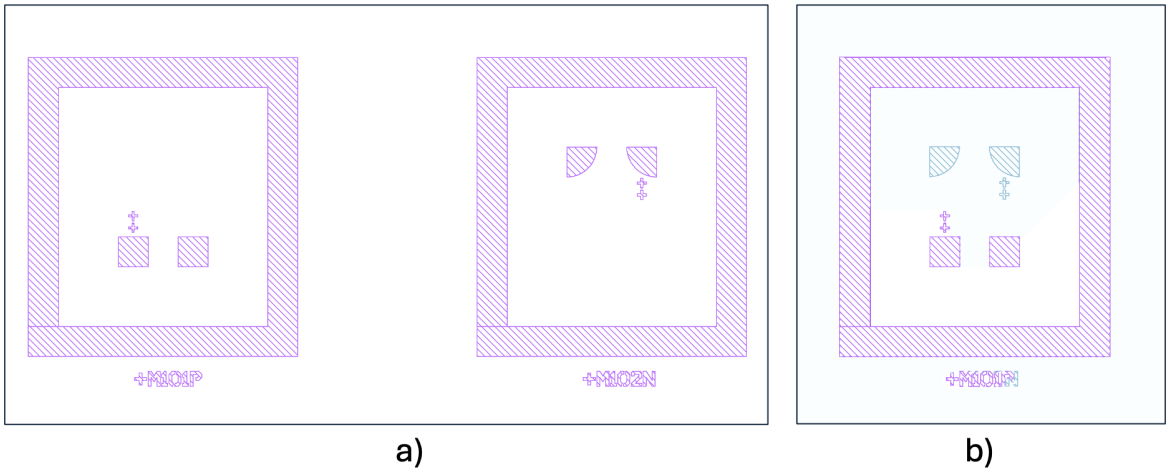

Figure B.1: a) GDS file of Mask #1 visualized in Klayout showing Design 1 of p-type (square) and n-type (half circle) contacts. b) P-type (square) and N-type (half-circle) contacts with overlap. The frame serves as an alignment/reference mark for layer overlap. The p- and n-contact etch steps are performed separately, enabling the deposition of different metals for each contact

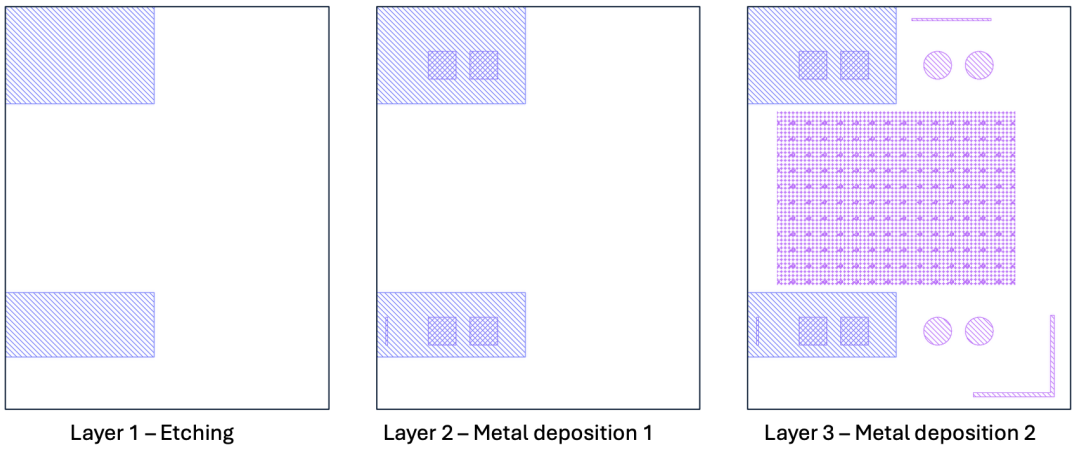

Figure B.2: Schematic of Mask #2. This mask contains three steps. Layer 1 defines the area for wet etching; layer 2 define p-type (square) contact; Layer 3 defines the n-type (circle) contacts and markers (+) grid . The p- and n-contact regions are developed in separate steps, allowing the deposition of different metals for each contact.

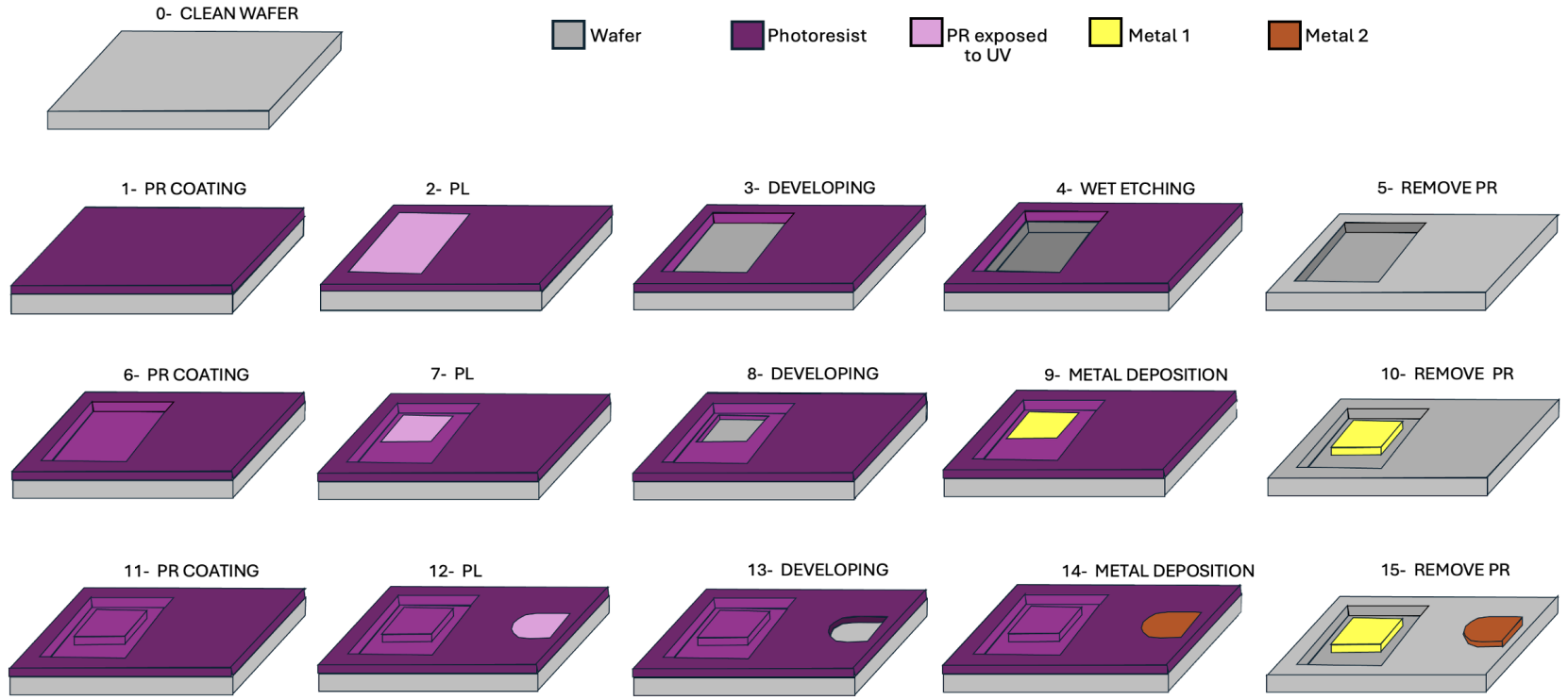

Figure B.3: Simplified schematic of Mask #2 illustrating the complete fabrication process, including coating, photolithography, development, wet etching and metal deposition. The second line shows the wet etching step; the third line illustrates the fabrication of the p-type (square) contact and the fourth line shows the fabrication of the n-type (half-circle) contact. The p-contact was deposited in the etched regions. The p-type and n-type connectors are fabricated with different metals. This sequence is shown using positive photoresist. The same process can also be applied in Mask#1 by skipping the first line corresponding to the wet etching step.

Appendix C

Bubbler system in Dry Thermal Oxidation Furnace

As mentioned in the section 6.3.1, the furnace used for dry thermal oxidation is connected to a bubbler system, which allows controlled release of gases during the oxidation process.

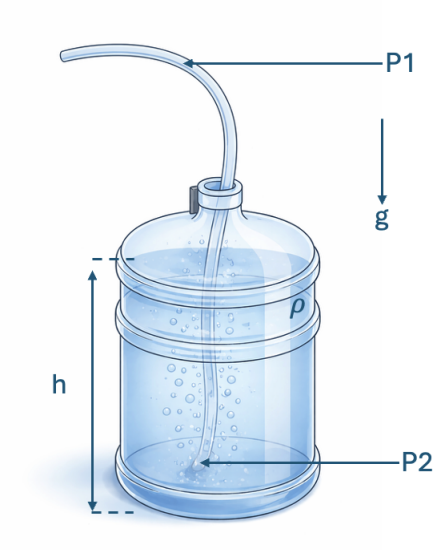

Figure C.1: Bubbler system

The bubbler system also acts as a hydraulic valve that prevents air from flowing back into the furnace when the system cools down. When the furnace temperature decreases, the gas pressure inside the tube also decreases according to the ideal gas law:

$$PV = nRT \tag{C.1}$$

If the volume and the number of moles remain approximately constant, the pressure is proportional to the temperature:

$$P \propto T \tag{C.2}$$

As the temperature decreases, the pressure inside the furnace drops, which could

potentially allow air to enter the system. However, the bubbler prevents this backflow because any incoming air would need to push through the water column in the bubbler.

In addition, the bubbler system helps to control exhaust gas. For gas to be released and bubbles to form, the pressure inside tube $P1$ must overcome to the the hydrostatic pressure inside the water $P2$.

$$P1 \geq P2 \tag{C.3}$$

This pressure required for the gas to exit through the bubbler is determined by the hydrostatic pressure of the water column:

$$P2 = \rho g h \tag{C.4}$$

where ρ represent the density of water, g is the gravitational acceleration of earth, and h is the depth of the tube submerged in the water. Therefore, the deeper the hose is submerged in the water, the greater the pressure required for the gas to exit the system.

If it is necessary to rapidly release gases from the chamber without opening valve 5, this can be achieved by temporarily removing the hose from the water column.

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