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A COMPARISON OF CAVITIES WITH INTEGRATED HIGH GAIN TIME-VARYING CAPACITIVE AND TRANSISTOR BASED REFLECTION AMPLIFIERS

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WILLIAM VAN HOUTEN
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A COMPARISON OF CAVITIES WITH INTEGRATED HIGH GAIN TIME-VARYING CAPACITIVE AND TRANSISTOR BASED REFLECTION AMPLIFIERS

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BY THE COMMITTEE CONSISTING OF

Dr. Jessica Ruyle, Chair

Dr. Hjalti Sigmarsson

Dr. Russell Kenney

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Abstract

In an increasingly contested and congested frequency spectrum [1] it is necessary to minimize noise generated throughout radiating systems. One approach to this problem has been through finding design techniques for integrated structures [2], [3]. These procedures reduce noise generated within a system by eliminating the transmission and matching structures needed between components, improving overall system signal-to-noise performance.

The work in this thesis specifies a design technique which integrates an active circuit into a resonator, a fundamental building block for many more complex microwave components. This is accomplished through the coupling of a reflection amplifier into a microwave cavity. By presenting a known input impedance, a one-port amplifier is capable of reflecting a signal back into the cavity at a greater magnitude than incident from the generator, eliminating several matching or transmission structures between amplifier, cavity, and other components in a potential system. First, a three port evanescent mode cavity is designed with strong coupling at the first and second port and an arbitrary weak coupling at the third port. Next, a single port reflection amplifier is designed, using both a transistor and varactor based approach, prioritizing the generation of a low bandwidth, low negative resistance response. Then, the structure of the third port of the cavity is adjusted to present an impedance which will allow for high gain to be delivered from the amplifier with stable operation. The finished structure using parametric amplification demonstrates stability with a high gain of 19.99dB and noise figure of 4.3dB.

Chapter 1

Introduction

1.1 Overview

In an increasingly congested frequency spectrum [1], spectrum overcrowding has become a key issue for radiating systems. While advancements in both hardware and software [4], [5], [6], [7] have made strides to enable the more efficient allotment of frequency bands, an ever increasing demand for more data to be transmitted over the air means the available frequency spectrum and our efficiency of its use is not sufficient. As such, further research is warranted to find techniques which improve the performance of radiating systems beyond current capabilities, allowing for more precise use of the limited spectrum.

It is necessary in any communication system to have some hardware dedicated to receiving a signal. As an example, a super-heterodyne receiver [8] is made up of an antenna, filter, amplifier, and mixer. This setup allows for the reception of a signal at some low power, which is then amplified, narrowed down to a target frequency, and mixed down to an intermediate frequency which is easier to demodulate and extract data from. The components of this receive chain are usually designed individually with matching networks which present a standard reference impedance, usually 50Ω, so all transmission lines connecting components on chip are terminated in a known impedance. This piecewise approach to designing the receive chain reduces overall design complexity. However, to

present that reference impedance additional circuitry is introduced into each component transforming the natural impedance at every external connection point to the standard 50Ω value. This nonideality leads to a drawback in the design where the extra circuitry introduces additional loss and noise to the final design [9]. By choosing to forgo individual designs, we can increase the potential maximum performance of a given system at the cost of requiring the complete design, manufacturing, and testing of a bespoke communications system.

1.2 Integrated Designs

Many thrusts have been made to integrate increasingly many components in a single design [2], [3], [10]. While ideally all hardware between components would be eliminated, replaced with a direct connection, the behavior of those components is heavily dependent on what impedance they see, also called a load. For this reason, there must still be something in-between which matches the load presented by one piece to the load expected by another across frequency. Figuring out how best to design these matching networks to maximize performance is one of the core issues around integrated designs and an area of ongoing research.

One such thrust [2] has been the co-design of an antenna and filter, called a filtenna. A filtenna combines the resonances of an antenna and a coupled cavity, providing a filter response to any signal transmitted or received by the unit. This structure unifies a filter and antenna into a tunable, light-weight component, minimizing volume while maintaining power handling in a single cohesive structure. In the course of this thesis, the study of another integrated structure, an amplified cavity, will be applied to act as a foundation for future developments in integrated designs.

1.3 Transistor Based Reflection Amp Cavities

It is unavoidable that any passive structure will have a small loss due to the imperfect conductors making up that structure, whether that structure is made of lumped, distributed, or wave-based components [11]. This and other losses have been mitigated by the introduction of active circuits into the structure. In [10], an active resonator using a defected ground structure is proposed. By replacing a passive capacitance with a negative resistance and capacitance presenting active circuit, the insertion loss of the resonator is mitigated by the gain of the active device. A similar application has been introducing an active circuit to a resonating cavity [3]. By coupling a reflection amplifier into a cavity, a portion of the signal within the cavity is intercepted, amplified, and reflected back. The loss of the cavity is canceled by the equal or slightly higher gain of the amplifier. The greatest issue with this approach is the limit to the maximum gain the amplifier can provide. Previous theory [3] states that the equivalent negative resistance of the amplifier is likely to go unstable if that resistance is greater than the equivalent load resistance of the insertion loss of the cavity, with a small gain achievable by pushing the negative resistance slightly greater than that loss, but amplifier theory disagrees [12]. A negative resistance amplifier is only stable if the negative resistance produced is properly stabilized across frequency by a greater load resistance [12]. This discredits the idea that low gain can be produced by a negative resistance slightly greater than the equivalent loss resistance, as this situation should instead be unstable. Additionally, high gains have been shown with negative resistance devices [13]. Therefore, it should be possible to produce a cavity with coupled active circuit capable of producing gain much greater than previously reported in literature.

1.4 Thesis Outline

This thesis aims to describe a method to successfully design a cavity with attached active circuit which has the maximum possible gain at its center frequency. This maximum gain is verified by analysis of the negative resistance presented by the amplifier and the input impedance presented by the cavity over a band of frequencies. The stability of the device is ensured through transient analysis, which checks the stability of the device at all frequencies. The methods to design each part of the system and the coupling structures between are discussed in full. The design is verified through the design of a 3GHz evanescent mode cavity and attached reflection amplifier using Keysight's Advanced Design System's (ADS) transient and harmonic balance solvers. Finally, a comparison between the presented design and similar designs by other authors will be made to highlight the increase in maximum gain from previous iterations and noise performance, as well as several potential improvements relegated to future work. In the course of this work I will identify the conditions leading to instability is actively loaded resonators, present a design procedure for integrating active circuits into resonators, demonstrate an actively loaded resonator with gain of 19.99dB and noise figure of 4.22dB in simulation, and analyze the conditions contributing to large noise figures in capacitive generation transistor amplifiers.

Chapter 2

Cavity Theory

The ultimate goal of combining the amplifier and cavity is to reduce losses caused by the cascading of components in a potential system. By removing the transmission lines and matching networks between a cavity and amplifier, the portion of losses caused by those components' transmission lines and connectors is eliminated [9]. The losses contributed by the resonator itself are minimized by selecting a topology with high quality factor [11]. As such, an evanescent mode cavity is selected for its high Q and lower volume, making it attractive for size limited applications [14]. By capacitively loading a cylindrical cavity, the center frequency greatly decreases, allowing smaller cavities to be used at lower frequencies. This capacitive loading is achieved by a a ring-gap capacitance, where a via connects the ceiling and floor of the cavity at its center and a ring is cut from the copper layer around the top of the post. The cavity will need three ports; an input, output, and one for amplifier coupling. The input and output will be strongly coupled, to present a 50Ω input impedance, while the amplifier will be weakly coupled to allow a specific input impedance to be presented to the amplifier, as seen later in Chapter 4.

2.1 Evanescent Mode Cavity

An evanescent mode cavity is a capacitively loaded cavity resonator [15]. The capacitive loading of the cavity decreases the center frequency of the resonator. "Evanescent" refers to how the cavity resonates with signals which are much lower in frequency than what the size of the cavity should allow.

To demonstrate why an evanescent mode cavity is attractive, we must first determine our criteria for choosing a topology. The goal of this project is to design a cavity with gain by introducing an active circuit into the structure. This circuit will tap into and amplify a microwave signal, reflecting it back into the cavity and the output. There are two ways which work in tandem to approach an effective increase in gain for the cavity. We must both increase the gain available from the amplifier and decrease losses introduced by the resonator structure. Only the amplifier will be able to provide active gain, so the cavity should be designed to minimize losses. Generally, this is done by applying a topology with high quality factor, Q, which denotes low losses within the resonator [11]. Additionally, a small size would contribute to an overall smaller footprint which is beneficial in size limited applications.

The original design for an evanescent mode cavity involved extending a post from the floor to just shy of the roof of a cavity. The gap formed between post and ceiling capacitively loads the cavity, driving the center frequency lower [15]. An alternate design has been proposed wherein the post is connected to the roof and an annulus is cut around it from the top copper wall to create the capacitive gap [16]. An example of both cavity topologies is shown in Fig. 2.1.

2.1.1 Theoretical Design Models

The evanescent mode cavity is designed from an equivalent cavity inductance L_{cav} and ring-gap capacitance C_{ring}. Equations for the design of these quantities for a ring-gap loaded cavity are presented in [17]. The inductance of the cavity is estimated as

$$L_{cav} = \frac{60}{\omega\sqrt{\epsilon_r}} \tan\left(\frac{\omega h\sqrt{\epsilon_r}}{c}\right) \ln(b/a) \tag{2.1}$$

where ϵ_r is the dielectric constant of the substrate filling the cavity, h is the height of that substrate, b is the cavity radius, a is the post radius, and c is the speed of light. The capacitance of the ring-gap is given by

$$C_{ring} = \frac{2\pi r\epsilon_0(1+\epsilon_r)}{\ln(1+\frac{\omega_r}{r})} \int_0^\infty [J_0(\zeta r) - J_0(\zeta(r+\omega_r))] \frac{J_1(\zeta r)}{\zeta} d\zeta \tag{2.2}$$

where r is the inner radius of the gap, ω_r is the width of the gap, and J_n is the nth-order Bessel function of the first kind. A visual representation of these quantities is given in Fig. 2.2. Adjusting the size of the cavity, post, ring-gap, or changing the dielectric filling the cavity will define the effective inductance and capacitance of the resonator. The center frequency of the resonator is defined using that inductance and reactance, by the relation

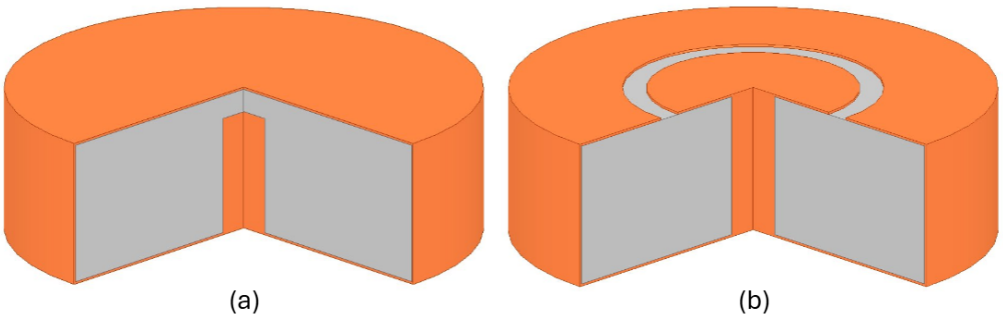

Figure 2.1: A classical evanescent mode cavity with a gap between the top of the post and ceiling (a) and the modern evanescent mode cavity with capacitive annulus (b).

$$\omega_0 = \frac{1}{\sqrt{C_{ring} L_{cav}}}. \tag{2.3}$$

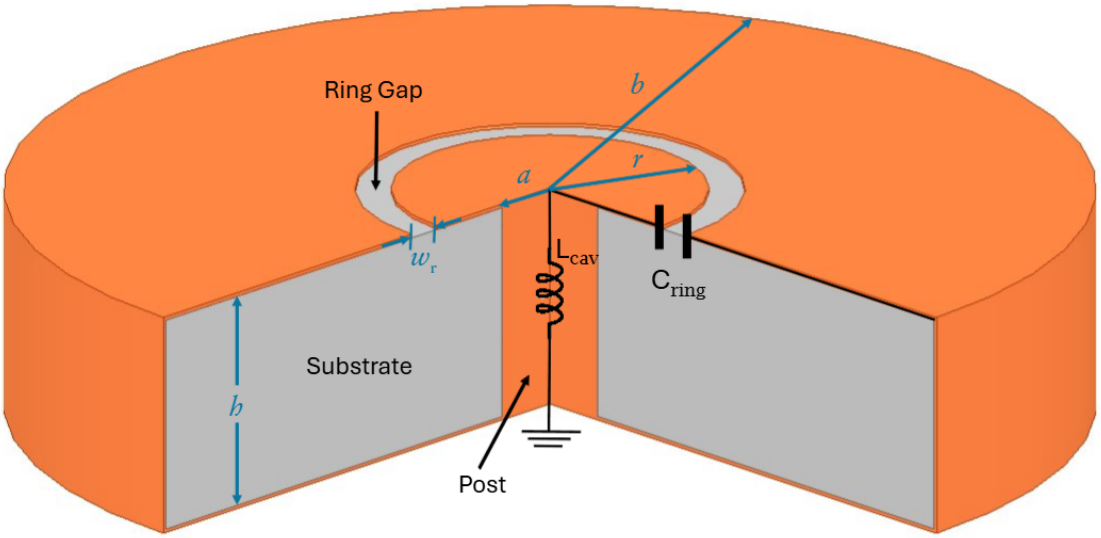

Figure 2.2: An evanescent mode cavity with dimensions labeled by their relevant variable.

2.1.2 Quality Factor

The quality factor of a resonant circuit is an indicator of loss within that circuit [11]. A higher Q usually indicates a less lossy resonator, keeping in mind that other factors such as the specific coupling into the cavity can contribute loss not intrinsic to the resonator. The theoretical model of the evanescent mode cavity, and the equations necessary to extract quality factor, finds Q based on three losses caused by the physical non-idealities of the cavity [17]. These are the conductive loss, dielectric loss, and radiation loss, correlating with the factors Q_{rad}, Q_{die}, and Q_{cond}. The radiation loss, represented by Q_{rad}, is caused by the fields within the cavity leaking through the ring-gap. This loss is calculated using Ansys High Frequency Simulation Software (HFSS) by modeling the full cavity with lossless dielectric and perfect conductor using the eigenmode solver. The dielectric and conductor

losses are calculated as

$$Q_{die,min} \approx \frac{1 + 1/\epsilon_r}{\tan(\delta)} \tag{2.4}$$

and

$$Q_{cond} = \frac{377 \tan\left(\frac{\omega h \sqrt{\epsilon_r}}{c}\right) \ln(b/a)}{R_s \sqrt{\epsilon_r}(h/a + h/b + 2\ln(b/a))} \tag{2.5}$$

where $\tan(\delta)$ is the loss tangent of the dielectric and Q_{die} is estimated with respect to infinitely thin copper making up the ring-gap. Q_{die} improves as copper thickness increases, making the above equation an underestimate. Ideally, the cavity will have minimal losses, or a maximal total Q. That total Q is found by the equation

$$Q_{tot} = \left(\frac{1}{Q_{rad}} + \frac{1}{Q_{die}} + \frac{1}{Q_{cond}}\right)^{-1}. \tag{2.6}$$

2.1.3 Substrate Integrated Waveguide and Manufacturing

The design techniques used for the cavity must be conducive to integration with the amplifier. A useful approach to achieve this is the substrate integrated waveguide (SIW) cavity [18]. An SIW cavity is designed to be manufactured into a sheet of dielectric with a layer of copper above and below the sheet. By connecting the top and bottom layer of copper through the dielectric with a wall of vias, you can form a dielectric-filled cavity. The necessary distance between vias to form an effectively solid, conducting wall at the cavity's center frequency is

$$d < p < 0.25\lambda \tag{2.7}$$

where d is the diameter of the via, p is the distance, or pitch, between vias from center to center, and λ is the wavelength of the center frequency of the cavity [18]. In clearer terms,

this means the vias must not intersect and the distance between vias must be smaller than a quarter wavelength of the center frequency. Typically, for a structure this small at such a low enough frequency, the one quarter wavelength maximum is far too large to sufficiently define the bounds of the cavity, so the distance between vias is much closer to the via diameter than the quarter wavelength. As an example, the evanescent mode cavity designed here has a perimeter of approximately 50mm, but the quarter wavelength of 3GHz is 25mm. If the cavity was designed to use the minimum number of vias, using the maximum spacing of 25mm, the cavity wall would be defined by two vias, which isn't physically capable of forming the circular base making up the cylindrical cavity. These vias are drilled through the substrate along with the central post and copper plated to produce the conductive metal wall. Coupling into the cavity is accomplished by creating a gap in the via wall and designing a coupling structure into either the top or bottom layer of copper over the filling dielectric. An example of such a cavity is seen in Fig. 2.3.

After the drilling and plating of vias, the coupling structure and ring-gap are milled from the top and bottom layers of copper, completing the production of the SIW cavity.

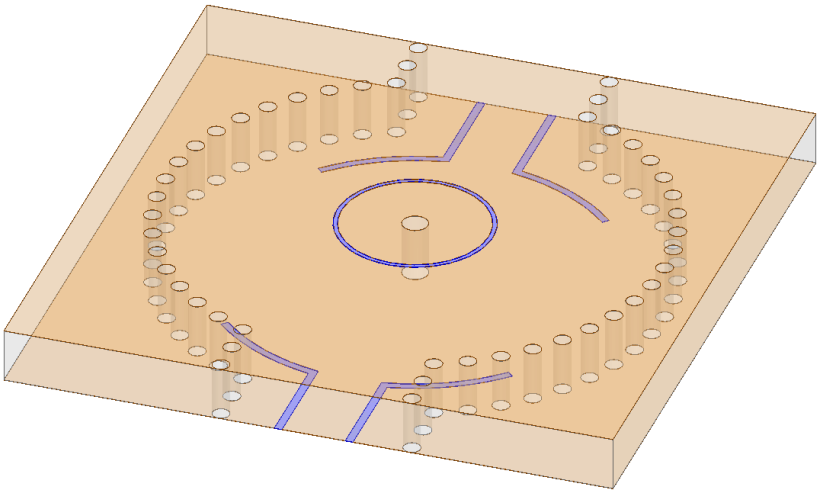

Figure 2.3: An evanescent mode cavity with via wall, center post, and coupling structures. The capacitive annulus lies in the top copper layer with coupling structures on the bottom layer, both in blue.

2.1.4 CPWG Coupling Structures

If the cavity design included only the via wall, we would have no way to send a wave into or out of the cavity. To make the resonator capable of being loaded by the amplifier, a structure is needed which allows coupling into the cavity at a needed coupling strength [11]. This coupling strength determines the input impedance seen looking into the cavity port. If we assume the transmission line making up part of the coupling structure has an intrinsic impedance of 50Ω and the impedance expected by the generator and load circuits is also 50Ω, then the input and output ports require critical coupling which presents 50Ω. Critical coupling is a condition typical to many two port cavities to achieve maximum power transfer, representing the point where the intrinsic impedance of the line and the input impedance presented by the port are conjugately matched [11]. Additionally, the generator and load ports must be equally coupled so the amplifier is able to receive and deliver power equally well from the generator and to the load. However, an issue arises from introducing a third port for the amplifier. In a two port cavity, the only path a signal may take when input from port one is to reflect back to the first port or transmit to the second port. Critical coupling works in such a way that no power reflects back to the first port, or that all power is transmitted through the second. When the third port is introduced, another path opens. If power from the first port is delivered to the third, then that power necessarily cannot be delivered to the second. This means that the total coupling between ports within a cavity is limited, and not all ports can be critically coupled, though all ports could be equally coupled. Therefore, it is necessary to consider how coupling strength is designed and determined.

The first method used to couple the generator and load into the cavity is a shorted grounded coplanar waveguide (CPWG) feed [16]. This works by creating an opening in the vias constituting the cavity wall and milling the gaps which isolate the center conductor of the CPWG line into the ceiling of the cavity, leaving the end of the line inside the cavity

shorted. The gaps move some distance into the cavity before diverging, continuing along a constant radius and thickness around the cavity, forming wings. The CPWG taps into and couples to the resonator like a current probe [16]. The other side of the trace continues outside of the cavity connecting to a load, generator, or other circuitry. The gap width and center conductor width of the line leading up to the wings determine the intrinsic impedance of both the line and the larger cavity port, following design procedures for a standard CPWG transmission line. An example coupling structure for the evanescent mode cavity and its design dimensions are shown in Fig. 2.4.

The dimensions of concern for CPWG coupling are the angle, radius, and width of the isolating gaps. The affects for various designed couplers are explored in [19] and generalizations can be made to preserve the Q of the cavity. Q is best preserved when the feed radius is maximized and the feed angle is minimized [19]. Feed width has minimal impact on Q. The primary means of controlling the coupling strength into the cavity is the feed angle, where a greater angle provides stronger coupling as seen in Fig. 2.5. The feed

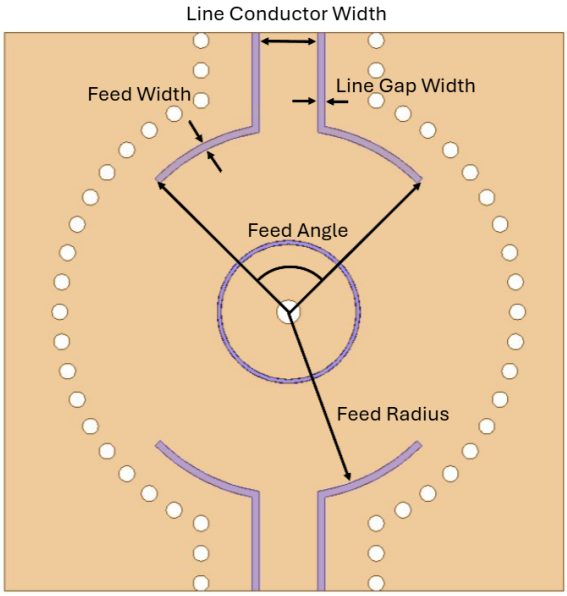

Figure 2.4: An evanescent mode cavity port with coplanar waveguide coupling structure and its relevant dimensions labeled.

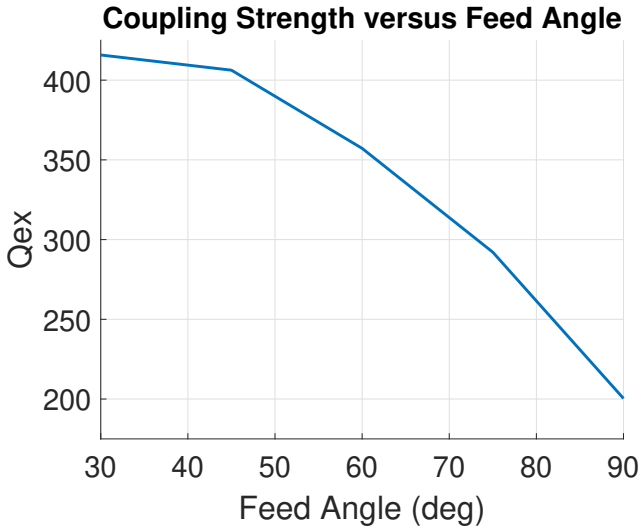

Figure 2.5: External quality factor of a symmetrically coupled two port evanescent mode cavity with varying coupling structure angles. Qex is a measure of coupling strength.

angle also disturbs the center frequency of the cavity, so the cavity dimensions must be adjusted to compensate.

The wings of the CPWG feed, if large enough, will physically disrupt the typical current distribution on the walls of the cavity by altering the path those currents would take. To mitigate this, an alternate coupling structure is used to connect the amplifier at the third port. Instead of shorting the CPWG line to the cavity wall directly, a via connects the line's center conductor to the opposite copper layer through the cavity dielectric. This forms a loop out of the CPWG center conductor, via, and cavity ground plane, allowing the amplifier to magnetically couple to the cavity [20]. The diameter and placement of the coupling via determines the coupling strength, with a greater via radius closer to the center of the cavity being more greatly coupled as seen in Section 2.1.4. A diagram denoting these physical dimensions is seen in Fig. 2.7.

Coupling strength is defined here by the depth of the null in reflection at ports one and two, where a depth greater than -20dB is considered critically coupled. Conversely, the weak coupling of port three is seen by the depth of reflection null at port three being less

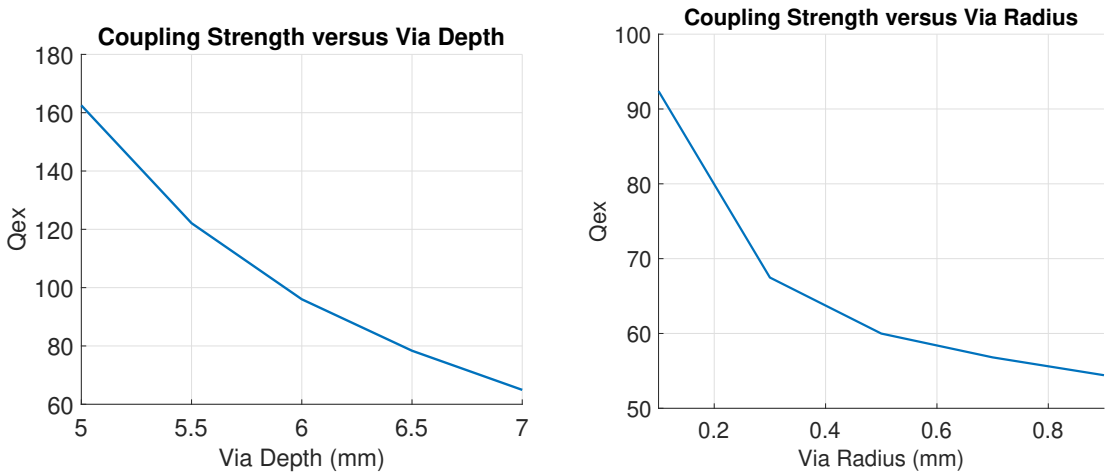

Figure 2.6: S-Parameters for transmission in a 3 port evanescent mode cavity. The impact on coupling due to the location of the via relative to the cavity center (left) and via radius (right).

than -5dB. When plotting on the Smith chart, as in Fig. 2.8, it is seen that by varying the location of the coupling via, and therefore the coupling strength, that the input impedance presented by port three radically shifts. The distance of the plotted input impedance from the center of the smith chart decreases with stronger coupling and vice versa, which can be used to purposefully modify the magnitude of the impedance presented at port three. By

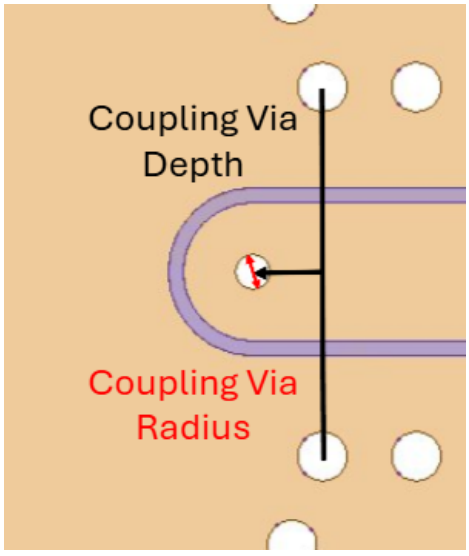

Figure 2.7: Diagram of the dimensions for the amplifier coupling scheme.

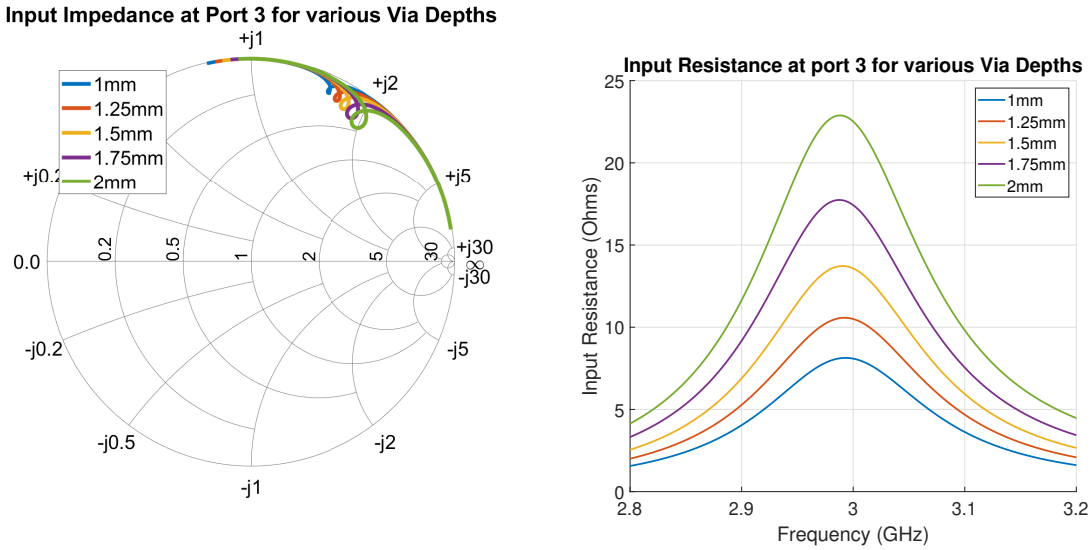

Figure 2.8: A smith chart and plot displaying multiple input impedances at port three for varying via depths. A greater via depth confers greater coupling strength up to the point where the ring gap and coupling structure intersect. By using a phase shifting element after the port, a wide range of input impedances can be presented by the port.

pairing this magnitude tuning property with a phase shifting transmission line, port three is able to present any target input impedances.

2.2 Cavity Design and Specifications

Using the previously described techniques, a three port, 3GHz evanescent mode cavity resonator is designed. TMM3 substrate was chosen for its ready availability, applicability to in-house manufacturing technologies, and low dielectric loss at high frequencies [21]. An eigenmode simulation of the resonator with solid copper walls was used to confirm the center frequency of the cavity before coupling structures were added, with a perfect H boundary covering all air gaps. Moving to a modal network solution file, the CPWG coupling structures and via wall are added and the transmission S-Parameters are inspected to ensure equally strong coupling at the input and output ports. Some small adjustments are made to the resonator dimensions to account for frequency drift introduced by the coupling

structures. Finally, the via wall is parted between ports one and two to introduce the via coupled third port. A model of the resonator can be found in Fig. 2.9 with design dimensions found in Table 2.1.

The figures of merit for a cavity resonator in this thesis are the bandwidth and quality factor of the cavity. Bandwidth is measured as

$$BW = \Delta f \tag{2.8}$$

where Δf is the width of frequencies with at least half the power of the center frequency [11]. The loaded quality factor of the cavity is found by dividing the center frequency of the device by its bandwidth [11]. The bandwidth and Q of the cavity, as simulated using HFSS, are listed in Table 2.2.

Strong coupling at ports one and two and weak coupling at port three is verified by examination of the S-Parameters of the cavity for all ports being terminated in 50Ω loads, as presented in Fig. 2.10. The S-Parameters of the cavity will radically shift once the amplifier has been integrated; the 50Ω load configuration is only meant to extract the input impedance of the third port before integration. The specific input impedance necessary for amplifier function has not yet been determined, so an arbitrary weak coupling is chosen for port three. The arbitrary impedance presented by port three is shown in Fig. 2.11

2.3 Conclusion

A design process and its execution for the creation of a 3-port, 3GHz evanescent mode cavity resonator has been presented. The methods to design the cavity and its coupling structures are discussed. The resulting cavity, its dimensions, and its operating characteristics are noted. Some modification to the amplifier coupling remain and will be solved once a target input impedance has been established.

Table 2.1: Dimensions of the evanescent mode cavity. Design dimensions defined in Fig. 2.2, Fig. 2.4, and Fig. 2.7

Cavity Radius	b	14 mm
Post Radius	a	0.75 mm
Cavity Height	h	125 mil
Ring Width	w_r	0.25 mm
Ring Radius	r	4.39 mm
Feed Radius	f_r	11.75 mm
Feed Angle	f_θ	90°
Feed Width	w_f	0.45 mm
GCPW Line Gap Width		0.45 mm
GCPW Line Conductor Width		3.675 mm
3rd Port Via Radius		0.35 mm
3rd Port Via Length Into Cavity		1.4 mm

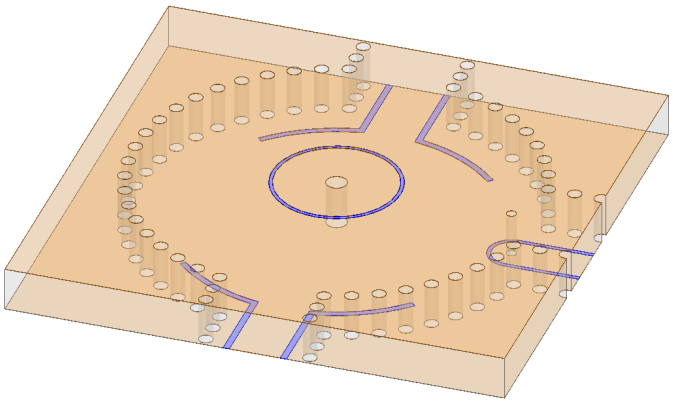

Figure 2.9: The 3-port, 3GHz evanescent mode cavity resonator with a pair of strongly coupled CPWG coupling structures for the generator and load, and weakly coupled loop scheme for the amplifier. Design dimensions given in Table 2.1 are defined in Fig. 2.2, Fig. 2.4, and Fig. 2.7

Table 2.2: Operating characteristics of the evanescent mode cavity.

Center Freq	f_c	3 GHz
Unloaded Quality Factor	Q_u	272.72
Bandwidth	BW	194 MHz

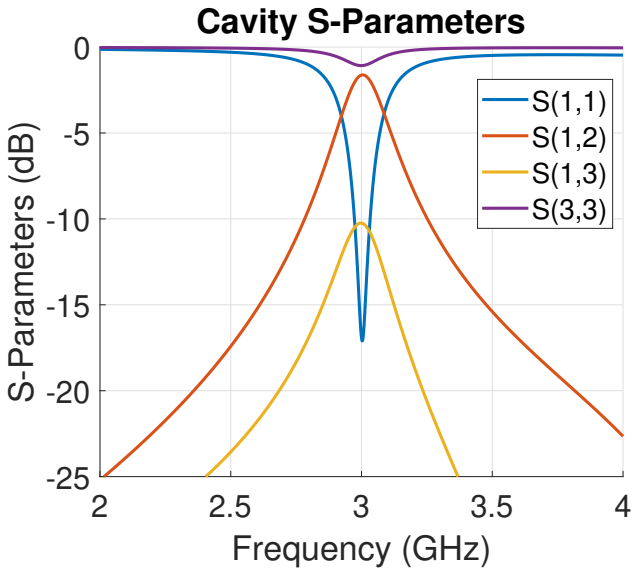

Figure 2.10: The 3-port S-Parameters of the evanescent mode cavity resonator.

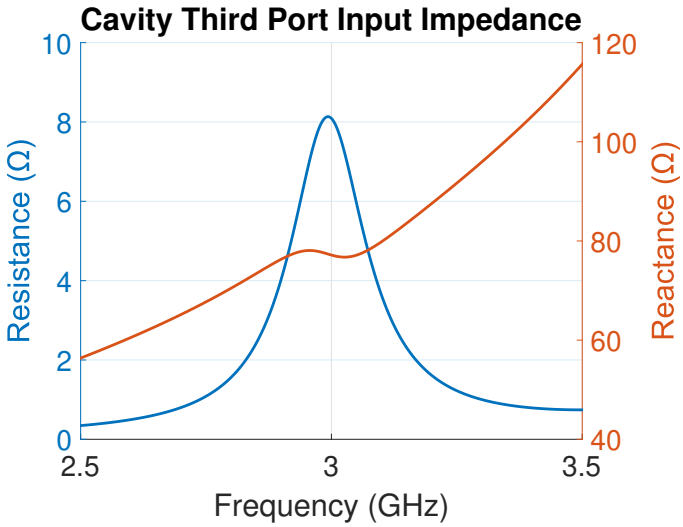

Figure 2.11: The arbitrary input impedance presented by the third port of the cavity.

Chapter 3

Amplifier Theory

Previous works have seen active circuits coupled into filters [22] and cavities [3] with some gain less than 4dB. Both of these systems work off of the same general principle; an active circuit is introduced, either replacing a component in a filter or coupling through a separate port. These active circuits reflect a greater amount of power than is incident on the circuit. This large reflection from the active device is generated due to its biasing and feedback structures and can be equated to a negative resistance. By keeping this negative resistance close to but below the positive load seen by the amplifier, a stable, high gain reflection is observed [23].

3.1 Reflection Amplifiers

A reflection amplifier is a one port device with a reflection coefficient Γ greater than one [23]. This means that any signal input to the amplifier reflects out with greater amplitude. To accomplish this, an active component such as a diode or transistor is biased or given feedback to present an effective negative resistance [23]. Whereas a positive resistance will consume power from an input wave, a negative resistance will deliver power by reflecting the input wave back to its source with greater amplitude. If the effective negative resistance of the device is greater than the total load resistance seen looking out of the device, the

device is unstable and will oscillate [23]. If the load resistance is greater, then the device will be stable and act as a one port amplifier [23].

The gain of the one port amplifier is determined by the difference between load and negative resistance [24]. As the smaller negative resistance approaches the load value, the gain produced by the active device exponentially increases. Theoretically, when the negative resistance and load are equal, infinite gain is achieved. Realistically, when the absolute value of the negative resistance is approximately equal to or greater than the load resistance, the active device will go unstable and oscillate. To explore the qualities and downsides of negative resistance devices, we start with a transistor based negative resistance.

3.2 Transistor Based Negative Resistance

To explain the theoretical model for the transistor based reflection amplifier [25] we start with the Colpitts oscillator [26]. Generally, an oscillator is an active device which outputs a certain known waveform. This is done by employing feedback to push a transistor to instability at a specific frequency [11]. The Colpitts oscillator uses capacitive feedback to produce instability. We can understand how instability is produced through examination of the equivalent circuit of the oscillator. A common-emitter npn BJT can be modeled by the base-emitter impedance Z_1 and a voltage dependent current source from collector to emitter [25]. By adding an additional impedance Z_2 between the emitter and ground, we come to the circuit model shown in Fig. 3.1. We must find the input impedance looking into the base of the transistor. To do this we note the voltage and current relations

$$Z_{in1} = \frac{v_{in}}{i_{in}} = \frac{v_{in}}{i_1}, \qquad v_2 = i_2 Z_2, \text{ and} \qquad i_{in} = i_1 = \frac{v_{in} - v_2}{Z_1} \tag{3.1}$$

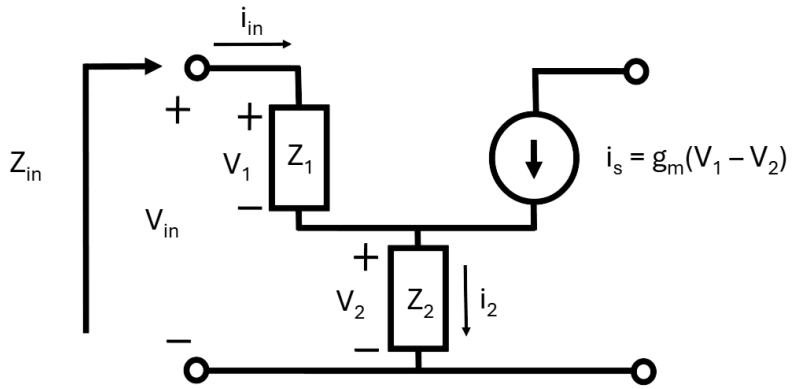

Figure 3.1: A heavily simplified equivalent circuit for a BJT transistor with emitter feedback; base-to-emitter impedance Z_1, the collector-to-emitter voltage dependent current source with current i_s, and post-emitter impedance Z_2.

with voltages, currents, and impedances defined in Fig. 3.1. Solving for input impedance, we find

$$Z_{in1} = Z_1 + Z_2 + Z_1 Z_2 g_m \tag{3.2}$$

where g_m is the transconductance of the transistor. If we substitute the generalized impedances Z_1 and Z_2 for transistor parasitic capacitance C_{be} and feedback capacitor C_e, we find the input impedance

$$Z_{in1} = \frac{1}{j\omega C_{be}} + \frac{1}{j\omega C_e} + \left(\frac{-g_m}{\omega^2 C_{be} C_e}\right). \tag{3.3}$$

The third term of Eq. (3.4) is a negative resistance, and defines the negative resistance presented by the device

$$R = \frac{-g_m}{\omega^2 C_{be} C_e}. \tag{3.4}$$

This model explains how we generate a negative resistance, but there are several complications caused by the parasitics ignored in the transistor model [25]. The adjusted circuit

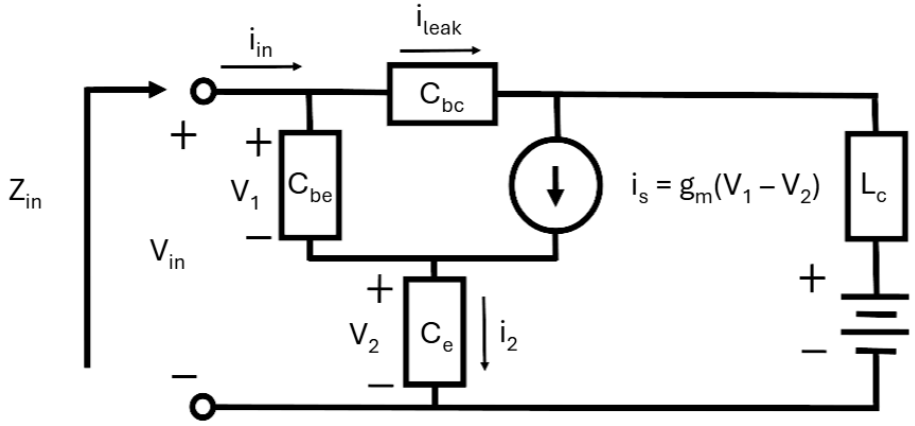

Figure 3.2: A simplified model representing a Colpitts oscillator with parasitic capacitance C_{bc} and collector loading structure.

schematic which accounts forr these complications is shown in Fig. 3.2. The most notable of these is the parasitic base-collector capacitance C_{bc}. This additional capacitance allows a path from base to collector, causing an inefficiency where some of the input signal will leak out [25]. A new parameter α is used to describe the final input impedance of the amplifier based on this new leakage path, defined as

$$\alpha \equiv \frac{\frac{C_{bc}}{C_{be}} + \frac{C_{bc}}{C_e} + sC_{bc}(\omega_T L_c + R)}{1 - \omega^2 C_{bc} L_c} \tag{3.5}$$

with the input impedance, including α, becoming

$$Z_{in} = Z_{in1}\left(\frac{1}{1+\alpha}\right). \tag{3.6}$$

ω_T is the radial transition frequency for the transistor, L_c is the inductance used to isolate the DC biasing generator from the transistor, and R is the negative resistance determined from Eq. (3.4). The input impedance is now dependent on the load presented to the collector. This complicates the physical design of the oscillator since we do not know what load the DC generator presents to the collector. To bypass this issue, a resonant LC tank is placed between the DC generator and transistor and an alternate known impedance is placed in

parallel to load the collector of the transistor. Leakage parasitic C_{bc}, the band-stop structure, and collector load R_c are depicted in Fig. 3.2. The 3GHz signal is blocked by the resonant tank so only the relatively small parallel load is seen by the transistor. With a known collector load the negative resistance presented by the amplifier can be calculated using Eq. (3.5). Further, by loading the amplifier with a resistance greater than the negative resistance presented by the amplifier, stability can be established [23].

3.2.1 Establishing Stability

The difference between an oscillator and amplifier is the stability of the circuit. The stability of a negative resistance device is largely dependent on which is greater, the absolute value of the negative resistance or the load resistance [23]. When the load resistance is greater, then the total resistance of the system is a positive real number, representing that the power delivered to the load is greater than the power produced by the device and that a wave reflecting between the two will eventually die out. An equal or greater negative resistance would see the reflected wave continue to bounce between load and amplifier, with that wave growing each time it reflects from the amplifier. This is not physically possible as that requires the amplifier to both receive infinite DC power and supply infinite AC power, a problem of supply, demand, and power handling. Instead, a lack of power increasingly demanded by the reflected wave causes the amplification to collapse entirely, and the built up power drains from the device, creating oscillation. Therefore a negative resistance device is only stable if the negative resistance presented is less than the positive resistance seen by the device. This stability condition must be maintained at all frequencies to prevent any oscillation within the amplifier [12].

Fig. 3.3 shows the normalized negative resistance across frequency presented by two transistor based reflection amplifiers centered at 3GHz. One amplifier presents a large,

250Ω negative resistance while the other presents 5Ω of negative resistance. Both amplifiers can produce a high gain if the positive load resistance is slightly greater than the absolute value of the generated negative resistance [24]. However, the negative resistance of each amplifier rolls off slowly as frequency diverges from 3GHz, especially so for the 250Ω amplifier. This will not be an issue for either amplifier with a well matched, wideband, lumped resistive load, but it will become an issue more quickly for the 250Ω amplifier if connected to a structure with narrow-band input impedance, such as for the evanescent mode cavity previously designed. While the amplifier might be well matched and stable at 3GHz, the lesser load resistances in the nearby frequency band may cause instability and produce unwanted oscillation. As such, it is beneficial to limit the negative resistance generated to low values when using a narrow-band load, allowing that resistance to gracefully decline over frequency and maintain all-band stability.

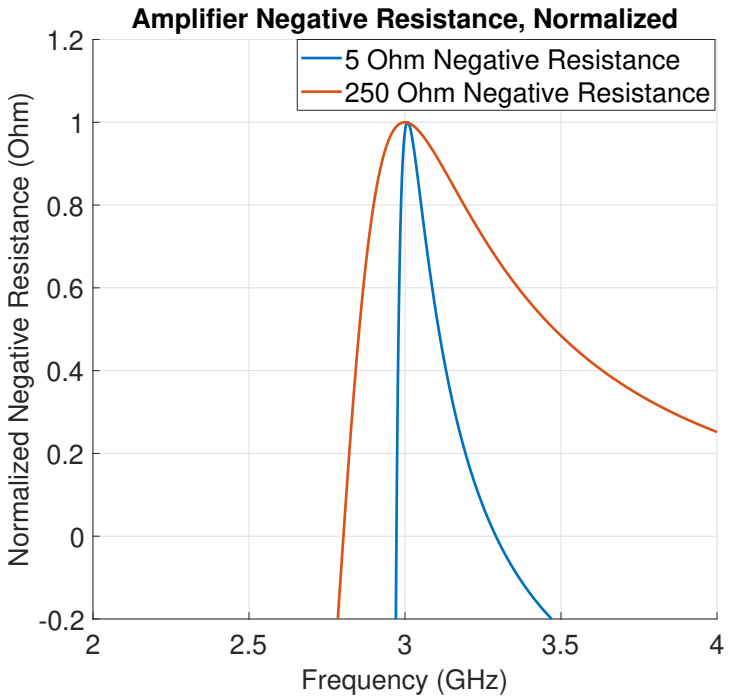

Figure 3.3: Negative resistance presented by two reflection amplifier across frequency, centered at 3GHz. The left amplifier presents a large, 250Ω negative resistance while the right presents 5Ω.

3.2.2 Biasing Scheme

Biasing refers to establishing a constant DC current or voltage on the pins of an active device to set a specific operating point [26]. For a two port amplifier, the bias determines the class of amplifier by choosing a baseline position on a characteristic IV curve. For a transistor based reflection amplifier, the bias determines the parasitic capacitances of the transistor, and therefore the specific negative resistance and capacitance presented by the amplifier [25]. Those parasitic capacitances are determined by the DC base current and collector voltage. To ensure that the DC biasing circuitry does not impact system performance at the center frequency, several structures are placed to isolate DC signals to the pins of the transistor, as seen in Fig. 3.4

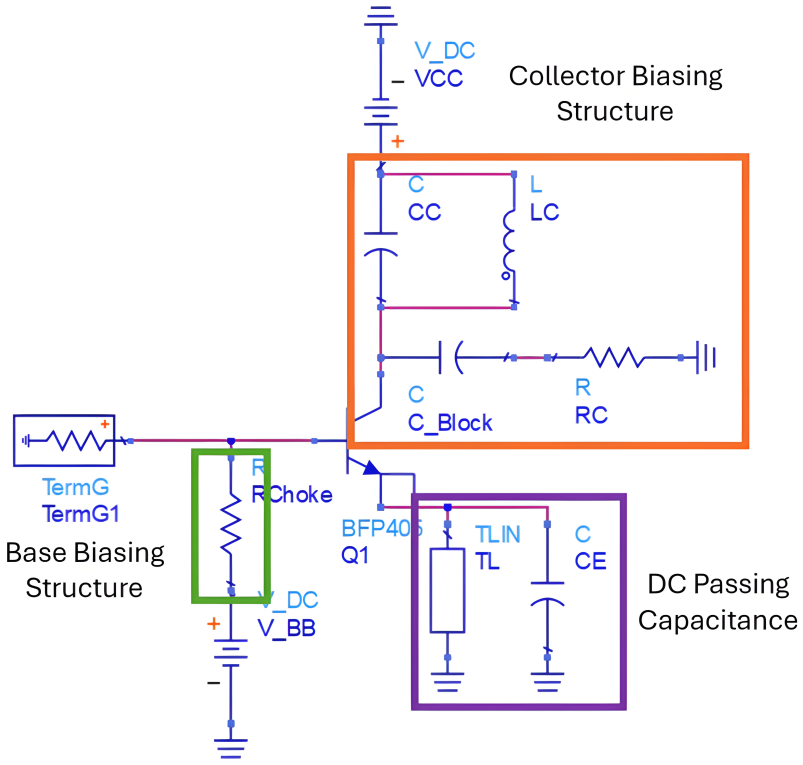

Figure 3.4: A schematic of the transistor based negative resistance device and its biasing structures.

Base Biasing

While directly connecting a DC generator to the collector and base pins of the transistor would be ideal, those connections would become leakage points for any RF signal traveling on those pins. So, to bias the transistor we need some structures which passes DC energy and blocks everything else. The most immediate answer is to use a large, series inductor to act as a low-pass filter. This would work, but I could not find any sufficiently large commercially available lumped inductors with great enough value and self-resonant frequency. Instead, for the base current biasing, a resistive choke is chosen. While this approach does isolate the AC signal from the DC generator, it will introduce some noise and lower overall amplifier efficiency due the resistive element in the bias path consuming power.

The base bias condition is dependent solely on the DC current going into the base of the transistor, meaning we can use a large resistance to choke RF signals without impacting bias conditions. The RF signal, coming or going from either the RF signal path or amplifier, will always find the arbitrarily large resistor in parallel with a relatively much smaller load, and most of the signal will flow away from the choke. The RF signal path is DC blocked using a large capacitor, so the only applicable path for the DC generator signal is through the transistor. A small leakage current flows through the transistor, so a heavily resistive path forms through the resistive choke and the effective resistance between the base and emitter. This leakage current, moderated by the resistive choke, constitutes the base bias current. These effects allow the DC and RF signals to travel to and from the transistor base without unwanted leakage into the cavity or generator.

Emitter Capacitance Structure

Because the bias current is dependent on the base-emitter leakage current through the transistor, and therein being able to flow out of the emitter to ground [26], it is necessary to

design a DC passing structure with known capacitance to complete the circuit relative to the base biasing generator. The capacitance of this structure is necessary to load the emitter and form the Colpitts oscillator [25]. This is accomplished through a shorted transmission line. The input impedance of a shorted transmission line with length greater than one-quarter wavelength is capacitive. However, at 3GHz such a line would have to be longer than 25mm, which is greater than the diameter of the cavity resonator. Instead, a capacitor is placed in parallel with the shorted transmission line. This parallel capacitor contributes a large reactance to the combined cap and line load, so the DC passing transmission line can be shortened to any given physically manufacturable length while presenting the target capacitance.

Collector Biasing

Now, with the base bias established, we move on to the collector biasing. We must know what load is presented to the collector to know the amplifier's input impedance [25]. While it would be ideal to use an inductive or resistive choke, we do not know what load the DC generator would present at 3GHz behind the choke. The generator load would shift the presented impedance so an alternate structure must be used. By placing a DC passing band-stop filter between generator and transistor, the generator is isolated from AC signals passing through the transistor. A DC blocking load can be placed in parallel to act as the collector load. RF energy would be stopped by relatively large load presented by the band-stop filter, and so only the parallel load would be apparent to the collector. The collector bias is based on the DC voltage apparent on the collector pin of the transistor, which is why the band-stop filter must be DC passing. Applying a DC voltage to the collector is done directly from the generator as there is nothing to impede the DC signal between generator and transistor. With the biasing topology selected, we now move on to choosing the bias point.

3.2.3 Selecting Bias Point and Collector Loading

The bias point of the transistor in this negative resistance configuration mainly establishes the shape of the negative resistance curve, while it works in tandem with the collector load to determine its magnitude. This is done by manipulating the parasitic capacitances presented by the transistor [25]. The goal for selecting a bias point is to provide a small peak negative resistance which falls off quickly as input frequency diverges from the center frequency of the amplifier. This allows the amplifier to deliver maximum gain at its center frequency while remaining stable at surrounding frequencies. The negative resistance of an amplifier with several bias points is shown in Fig. 3.5.

Referring to Fig. 3.5, if the transistor is under-biased, no negative resistance is produced, as with the purple trace where bias voltages are low. Over-biasing leads to a wide-band negative resistance which will not roll-off quickly enough for a narrow-band load to stabilize.

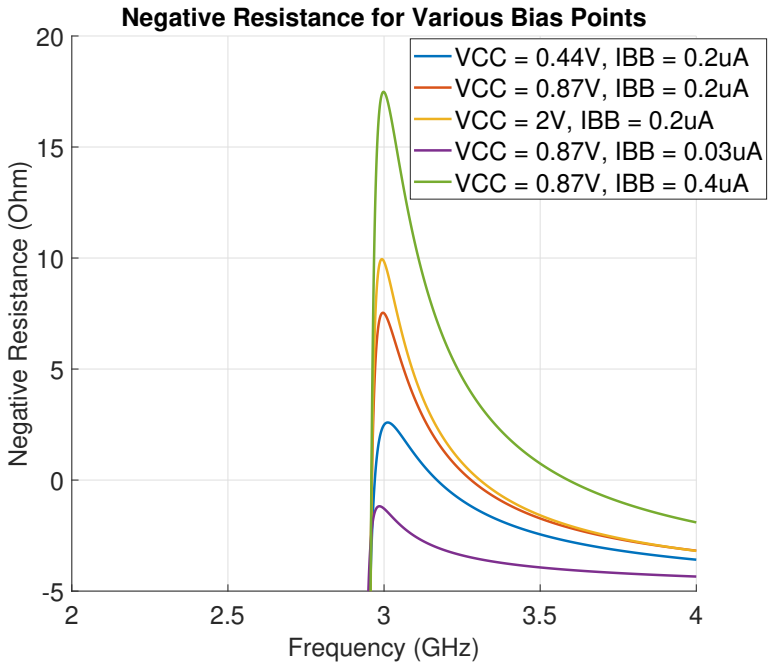

Figure 3.5: The negative resistance presented by a reflection amplifier for various base and collector bias points. Here, the negative resistance generated increases and decreases with the bias voltage or current. The bandwidth with some negative resistance increases with bias conditions as well.

As seen with the green trace, the high bias voltages leads to a negative resistance from 2.95GHz to 3.6GHz. This frequency range is large when compared to the more moderately biased orange trace which presents a negative resistance from 2.95GHz to 3.3GHz. There is a point in between these over and under-biased extremes which leads to an easily stabilized narrow-band negative resistance. The negative resistance is also greatly affected by the load presented to the collector. A purely real load tends to scale the negative resistance produced. A capacitive load will increase the magnitude of negative resistance but introduce an additional peak in negative resistance at lower frequencies. An inductive load will decrease the magnitude of negative resistance and introduce a null at higher frequencies. An example of various real and complex collector loads is shown in Fig. 3.6.

While it was previously stated that the negative resistance of the device is selected by the emitter capacitance chosen, we can now see how that negative resistance is selected from another angle. The emitter capacitance impacts negative resistance by shifting the peak of the negative resistance curve established by the bias point and collector load towards lower

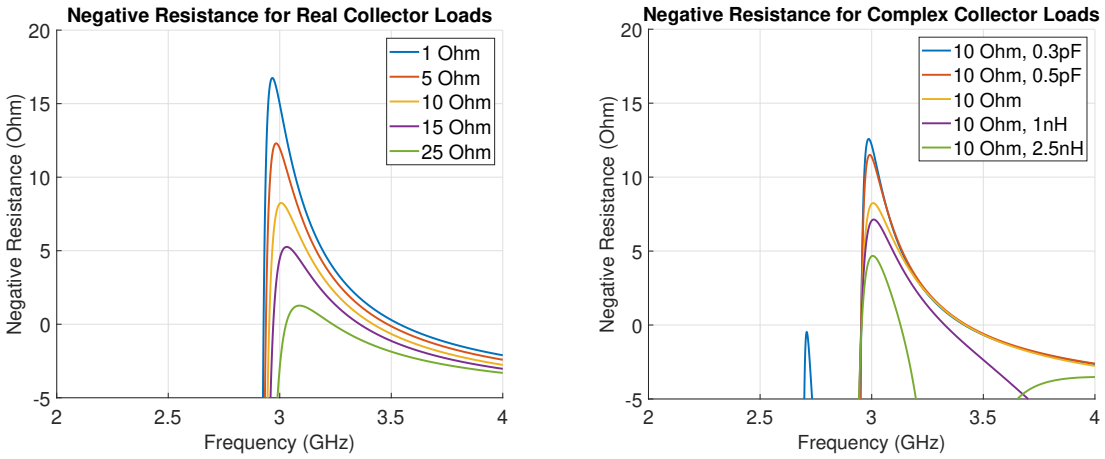

Figure 3.6: The negative resistance presented by a reflection amplifier for various base and collector bias points. Negative resistance increases as load resistance decreases (left). When capacitively loaded, negative resistance increases but a second maxima is generated at lower frequencies (right). When inductively loaded, negative resistance decreases but a null is introduced at higher frequencies (right).

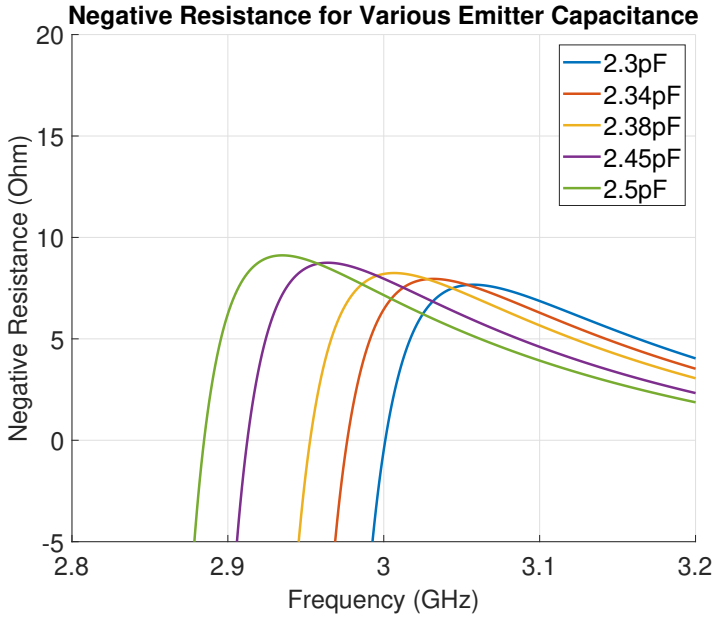

Figure 3.7: The negative resistance presented by a reflection amplifier for various emitter capacitances.

or higher frequencies, seen in Fig. 3.7. Shifting the peak of the negative resistance curve to the center frequency of the amplifier maximizes potential gain at the center frequency with regard to stability with a narrow-band load. If the peak of negative resistance does not rest at the center frequency of the cavity, then that peak must be slightly higher or lower in frequency and matching to that shifted frequency would present a greater gain instead.

3.2.4 Reflection Gain

The reflection Γ generated by the amplifier has similar behavior to the reflection on a lossless, terminated line [24], which is described by the formula

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{3.7}$$

where Z_L is the terminating load and Z_0 is the characteristic impedance of the line. For the amplifier, its more apt to say Z_L is the amplifier impedance and Z_0 is the impedance

seen by the amplifier. When applying Eq. (3.7) for the terminated line, you expect that as the load impedance and characteristic impedance diverge, reflection on the line increases. However, passive impedances are never able to affect a reflection coefficient $|\Gamma| > 1$, where the reflected signal is greater than the input. Getting gain on reflection is possible with a negative resistance device. Power is delivered rather than absorbed with the negative load, which results in an incident wave being reflected back with gain. The pole in the denominator, when $Z_L = -Z_0$, represents the theoretical infinite gain achieved when the negative and load resistances are equal. In reality, the DC and RF power available to the device is unable to support infinite gain, so oscillation occurs instead.

3.2.5 Reactance Matching

Until now, the capacitance presented by the amplifier has been neglected. Of course, a large reactive mismatch will lead to inefficiency in the amplifier by diverging from the conjugate match necessary to deliver maximum power [11]. As such, it is best to cancel the large capacitance presented by the amplifier with a heavily inductive load. By resonating the amplifier's capacitance with an inductive load, the peak in gain will be maintained at the intended center frequency of the device and maximum power transfer is achieved [11]. The affect of reactance mismatch when connected to a cavity is shown in Fig. 3.8. Now, with the theory of the amplifier well described, the transistor based amplifier is designed.

3.2.6 Transistor Based Reflection Amplifier Design

The Infineon BFP405 npn BJT transistor [27] was chosen for the transistor-based amplifier due to its familiarity to the author and readily available transistor models hosted on the manufacturer's website. The design starts in ADS where the transistor model is used to extract device parasitic capacitances with an arbitrary bias point. The parasitic capacitances,

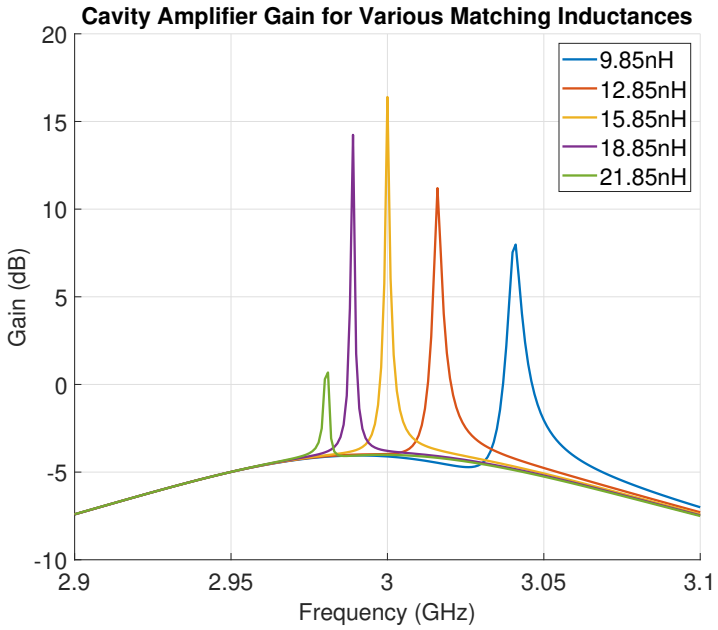

Figure 3.8: Amplifier gain versus matching inductance. The peak in gain shifts in frequency, increasing as reactance decreases.

an arbitrary emitter capacitance, and an arbitrary collector load are input into Eq. (3.4), Eq. (3.5), and Eq. (3.6) to estimate the negative resistance generated by the amplifier. Next, The biasing structure for the collector and the emitter capacitance is then designed. With an estimate made, all values are input into the ADS model shown in Fig. 3.4. Here, the S-Parameters of the device and an estimate of the effective negative resistance across frequency can be extracted, with S-Parameters being directly reported from the simulator and amplifier input impedance found using the equation for input resistance [11]

$$R_{in} = Re\left(Z_0 \frac{1 + S(1,1)}{1 - S(1,1)}\right). \tag{3.8}$$

The bias point and collector load are amended to alter the negative resistance curve shape and magnitude. The emitter capacitance is adjusted to shift the peak of the negative resistance curve to 3GHz and the matching inductance is adjusted to best match the amplifier to the same. Note that stability is not measured with the S-Parameters solver, so care should

be given to make sure that the negative resistance presented is less than the load. Here, we now have an amplifier with 7.5Ω of negative resistance centered at 3GHz matched to a wide-band 12.2Ω load. The impedance presented by the amplifier and the gain of the device for a 12.2Ω load are given in Fig. 3.9, while the component values for the amplifier design are shown in Table 3.1. The design will continue in chapter 4 with the integration of amplifier and cavity, how stability and gain are measured in such a system, and the complications in designing this structure.

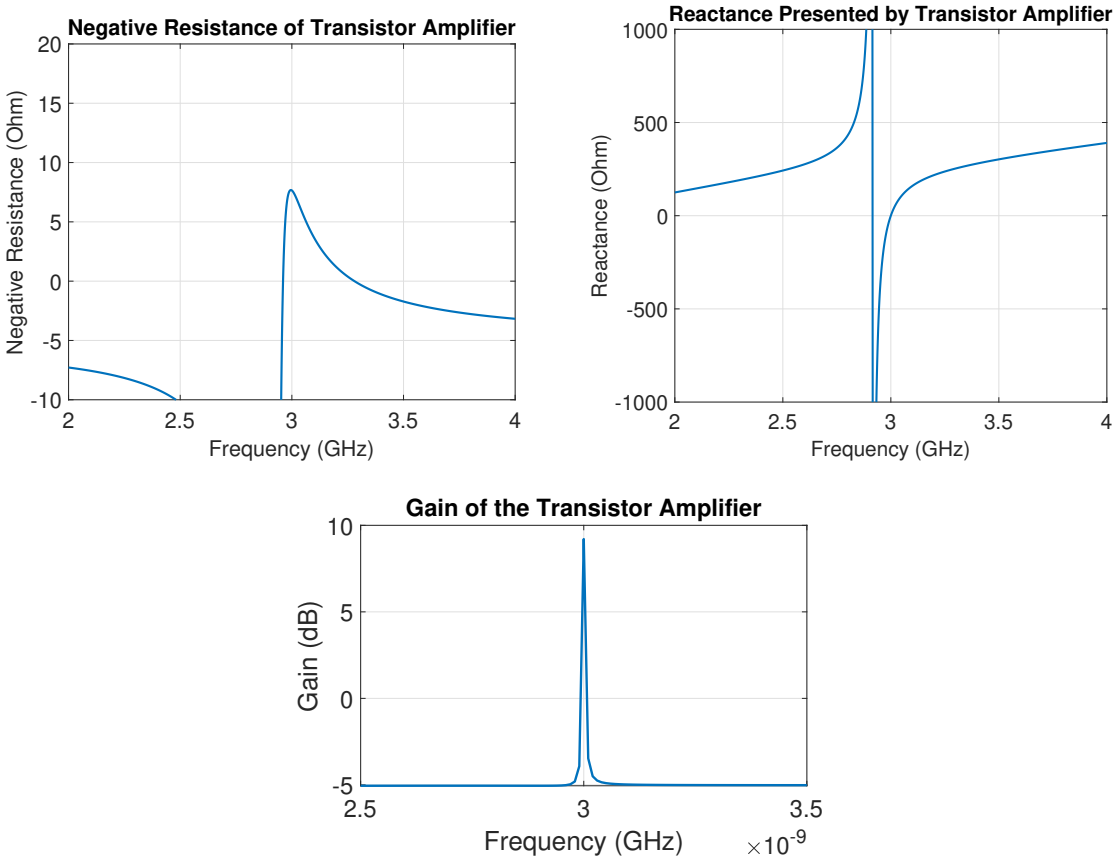

Figure 3.9: Input impedance presented by the transistor based negative resistance device and its resulting Gain for a reactance matched 12.2Ω load.

Table 3.1: Component values for the transistor based reflection amplifier.

Base Bias Current	I_{BB}	0.2 uA
Collector Bias Voltage	V_{CC}	0.87 V
Collector Load	R_c	0 Ω (Shorted)
Emitter Transmission Line Length	l_{TL}	24.4°
Emitter Capacitance	C_e	2.32 pF
Matching Inductance	L_{match}	18.2 nH
Collector Resonator Capacitance	C_{BPF}	2.8 pF
Collector Resonator Inductance	L_{BPF}	1 nH

3.3 Parametric Amplifiers

An alternative negative resistance device to be explored is the parametric amplifier discussed in [28]. A parametric amplifier is capable of presenting a very narrow-band negative resistance [28], so the wide-band stability issues involved with the transistor based amplifier may be avoided by using a time varying capacitance instead. By introducing a signal to a time-varying capacitance, energy is redistributed between the mixing products of the signal frequency and the frequency at which the capacitance varies [28]. It is possible to distribute that power back to the signal frequency, creating an effective negative resistance. Working off of many of the principles of the reflection amplifier already explored, the parametric amplifier presents a low-noise, narrow-band negative resistance. This narrow-band negative resistance rolls off quickly [28], potentially alleviating some issues caused by the wide-band negative resistance of the transistor based amplifier.

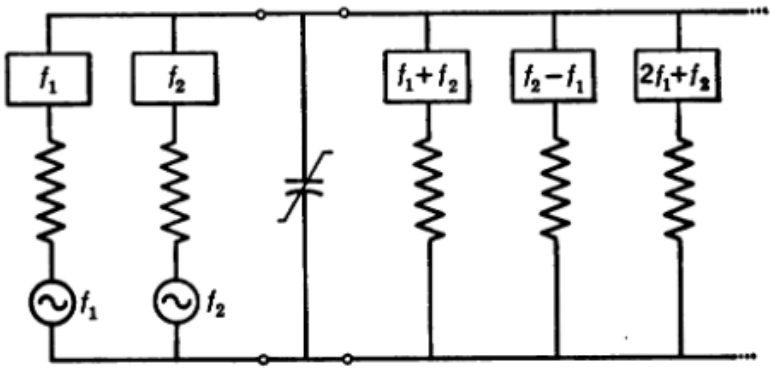

Figure 3.10: Two voltage generators, their resistances, and a band-pass filter at their signal frequencies lie in parallel to a non-linear capacitance in addition to a number of loads with band-pass filters tuned to the sum and differences of the generator signal frequencies (f1 + f2, f1 - f2, 2*f1 + f2, etc. Figure taken from [28]

3.3.1 The Manley Rowe Relation and Parametric Amplification

The Manley-Rowe power relation [28] is a set of equations relating power flowing into and out of an ideal nonlinear reactance. Take the circuit in Fig. 3.10. There are two voltage generators and their associated resistances at f_1 and f_2 together with band-pass filters placed across a non-linear capacitor. Additionally, there is an infinite series of loads with band-pass filters tuned to the sum and difference frequencies of f_1 and f_2 which arise due to the non-linear reactance. The Manley-Rowe relation states that, due to this non-linear reactance,

$$\sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty}\frac{mP_{m,n}}{mf_1+nf_2}=0 \tag{3.9}$$

and

$$\sum_{n=0}^{\infty}\sum_{m=-\infty}^{\infty}\frac{nP_{m,n}}{mf_1+nf_2}=0 \tag{3.10}$$

where $P_{m,n}$ is the power flow into the reactance at frequency mf_1 and nf_2. In more clear terms, this means that the power delivered at f_1 and f_2 will be redistributed among the sums and differences of the signal frequencies and delivered to the various loads. Consider the situation where we only allow three of these frequencies to exist. A signal generator at f_1, a

pump source, the voltage of which causes the time varying capacitance, at f_3, and a load at f_2, the difference of f_1 and f_3. Eq. (3.9) and Eq. (3.10) become

$$\frac{P_1}{f_1} + \frac{P_3}{f_3} = 0 \tag{3.11}$$

and

$$\frac{P_2}{f_2} + \frac{P_3}{f_3} = 0. \tag{3.12}$$

If the circuit is designed so that the time varying reactance delivers much greater power than the signal generator, then Eq. (3.11) implies that power is able to mix down from the pump frequency to the signal frequency. If this is the case, then the signal generator branch must see some reflection greater than the signal it delivers to the device. In this way, a negative resistance is formed. This type of operation is known as negative resistance parametric amplification.

3.3.2 The Negative Resistance Parametric Amplifier

To design a negative resistance amplifier, we start with the generalized circuit model of Fig. 3.11 [13]. This circuit gives the basic layout for the parametric amplifier. SRC_1 and R_1 make up the signal generator and its impedance and while R_2 and R_3 represent the signal and idler loads. There is separate gain for each of these loads and either can be considered the amplifier output. However, to act as a reflection amplifier, we assume that the signal branch is the output, and so R_2 is our output load. Later, when integrated with the cavity, SRC_1, R_1, and R_2 will be dependent on the signal incident to the cavity and the input impedance presented by its port. SRC_2 and R_4 make up the pump generator and its impedance. L_1, C_1, L_2, C_2, L_3, and C_3 form resonant circuits which restrict the signal, idler, and pump circuit frequencies to their respective branches. NonlinC and R_5 represent a

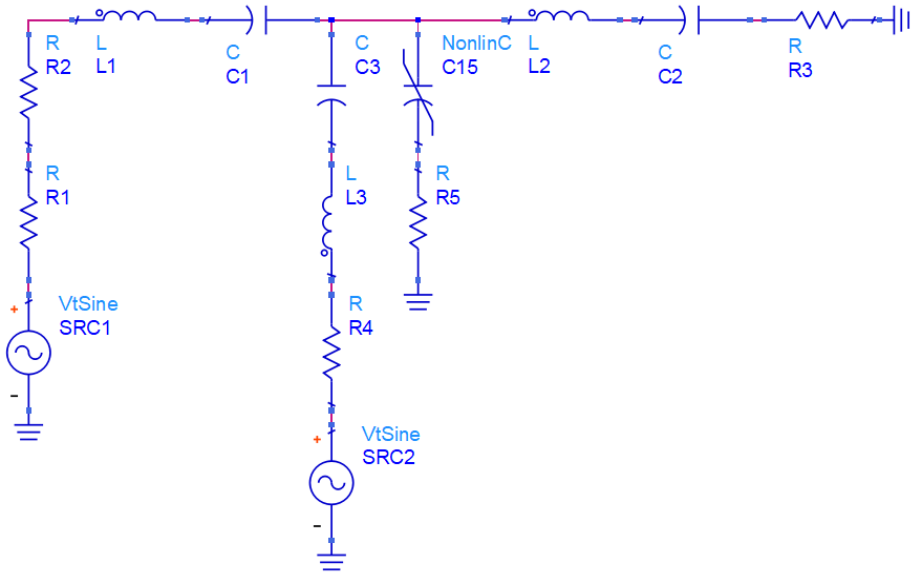

Figure 3.11: A general schematic for parametric amplification. From [13].

time-varying varactor and its loss. The negative resistance generated by the system is

$$R_{Neg} = \frac{M^2}{\omega_i \omega_s (C_0(1-M^2))^2 (R_3 + R_5)} \tag{3.13}$$

where M is the modulation index, a measure of the time-varying capacitance, C_0 is the average capacitance presented by the time-varying varactor, and C_{11} is the difference between the maximum and average value of the capacitance presented by the varactor. M is defined by the equation

$$M = \frac{C_{11}}{2C_0}. \tag{3.14}$$

Note that the modulation index cannot exceed 1 as that implies the time-varying capacitance at times presents a negative capacitance. The analytically derived gain of the device in this basic configuration is

$$g_t = \frac{4R_1R_2}{(R_1 + R_2 + R_5 - R_{Neg})^2}. \tag{3.15}$$

The resonators for the signal, idle, and pump branches are necessary to isolate other signals from those branches. The design of these resonators is complicated by the time-varying nature of the varactor capacitance. Since the capacitance presented by the varactor is changing over time, an effective capacitance to represent the varactor as a static component is calculated instead [13]. A set of design equations for those resonators with respect to the non-linear capacitance is presented as

$$C_{eq1} = (1/C_1) + \frac{1}{(1-M^2)C_0}, \tag{3.16}$$

$$C_{eq2} = (1/C_2) + \frac{1}{(1-M^2)C_0}, \tag{3.17}$$

$$L_1 = \frac{C_{eq1}}{\omega_s^2}, \tag{3.18}$$

$$L_2 = \frac{C_{eq2}}{\omega_i^2}, \text{ and} \tag{3.19}$$

$$L_3 = \frac{1}{C_3\omega_p^2} \tag{3.20}$$

where ω_p is the radial pump frequency and C_{eq1} and C_{eq2} are the equivalent capacitance for resonator design. C_1, C_2, and C_3 can be arbitrarily chosen, so if the inductor values necessary to form the resonator are unreasonable, then another capacitance can be chosen to compensate. The gain of the device can be found in simulation by taking the ratio of the power available from the generator to the power delivered to the load resistance

$$G_A = \frac{P_{out}}{P_{av}} = \frac{4i_s^2 R_g R_l}{V_S^2} = \frac{4i_s^2 R_1 R_2}{V_S^2} \tag{3.21}$$

where i_s is the current through the signal branch and V_S is the voltage produced by the signal generator $SRC1$. With this, we can now design the parametric amplifier.

3.3.3 Parametric Amplifier Design

Parametric amplifier design begins by selecting the signal, pump, and resulting idler frequencies. The signal frequency is the center frequency of 3GHz, while the pump frequency is chosen to be 8.95GHz, with a resulting idler frequency of 5.95GHz. Next, a varactor must be chosen. Varactors are voltage dependent devices which present a capacitance when reverse biased. Parametric amplifier design is greatly influenced by the capacitance range presented by the varactor, so it is best to choose a commercially available varactor as a basis for design. The capacitance generated by the varactor with respect to the reverse bias voltage is not linear. One assumption made in the design equations for a parametric amplifier is a highly linear time varying capacitance, so a voltage range should be chosen with a mostly linear set of capacitances. Once a varactor is chosen, the resistance representing varactor loss R_5 is know and a set of voltages can be defined for average capacitance C_0 and the time-varying capacitance amplitude C_{11}, thus defining our modulation factor M. For this amplifier, the Macom MAVR-000120-14110P varactor [29] is chosen for its exceedingly low capacitance range of 0.15pF to 0.9pF, its equivalent loss resistance of 0.88Ω, and its readily available SPICE model. From that capacitance range, an average capacitance of 0.5pF and capacitance swing of 0.079pF is chosen, giving a modulation factor of 0.079. The idler load R_3 is assumed to be 5Ω, to be adjusted later should it be needed as the idler load does affect the negative resistance presented by the device and can be increased or decreased to compensate for a slight miss. The signal generator resistance and load resistance, R_1 and R_2 are assumed to be equal as a criteria for Eq. (3.15), and are varied to determine the gain presented by the amplifier for various load resistances. Finally, the branch resonators are

designed using Eq. (3.16) through Eq. (3.20), ensuring that the capacitances chosen allow for a realistic inductor value to match.

With all values selected, an ADS simulation using harmonic balance is used to extract operating characteristics from the device. The circuit described is displayed in Fig. 3.12, with negative resistance versus input impedance given in Fig. 3.14 and the gain and noise figure of the parametric amplifier for a load resistance of 21.8Ω given in Fig. 3.14. The negative resistance generated by the device has the same value as the point in load resistance where the gain curve reaches an asymptote, corresponding with the theoretical infinite gain of equal load and negative resistance. However, it should be noted that the amplifier sees the generator and load impedances in series as one total load. Due to this, the cavity which later replaces these resistances will need to present an impedance equal to the total value of the load which it replaces, that being the generator and load resistances together. The signal branch resonator had previously been designed to deliver maximum power to the load, occurring when the load is conjugately matched to the amplifier. As such, the reactance presented by the amplifier at 3 GHz is approximately zero.

3.4 Conclusion

The design procedures and their executions for the design of two 3GHz reflection amplifiers, using both a transistor and varactor based approach, has been presented. The methods to properly load, bias, and match the transistor, as well as the design of the time-varying capacitance, pumping circuit, resonators, and loading of the parametric circuit have been discussed. The input impedance of the resulting amplifiers will be used to determine the necessary coupling for the third port of the microwave cavity, which will further determine the specific gain and noise figure presented by the full cavity-amplifier system.

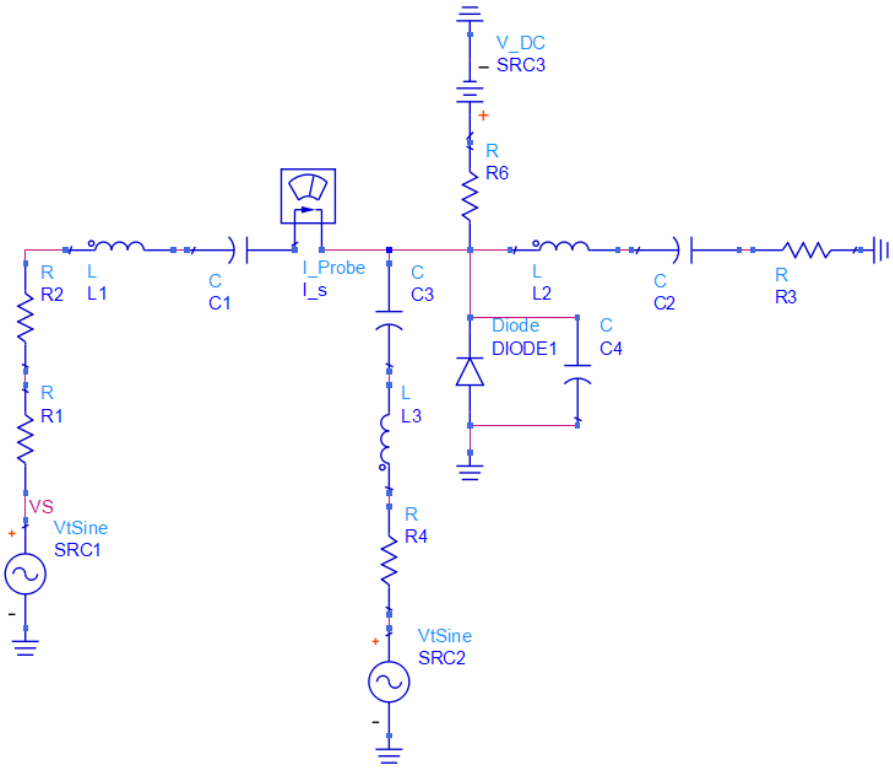

Figure 3.12: The ADS schematic for parametric amplifier design using harmonic balance. DIODE1 and C4 constitute an equivalent varactor model.

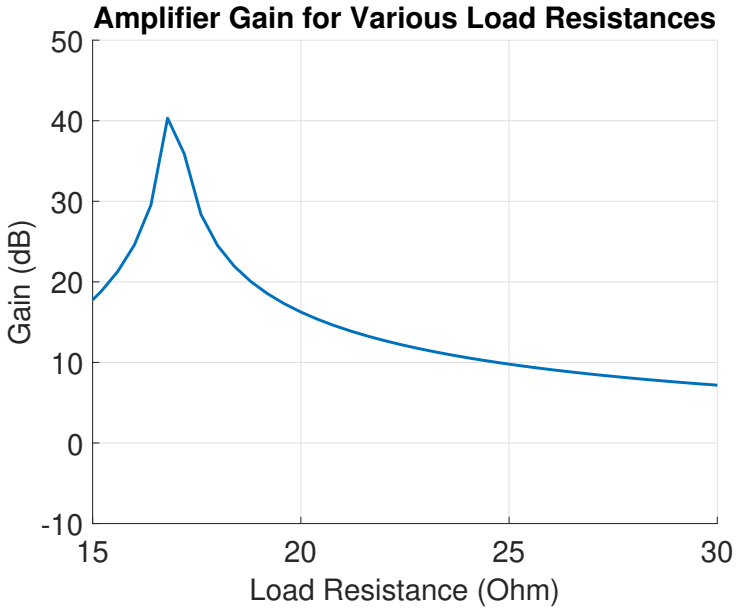

Figure 3.13: The gain of the parametric amplifier with varying load resistances.

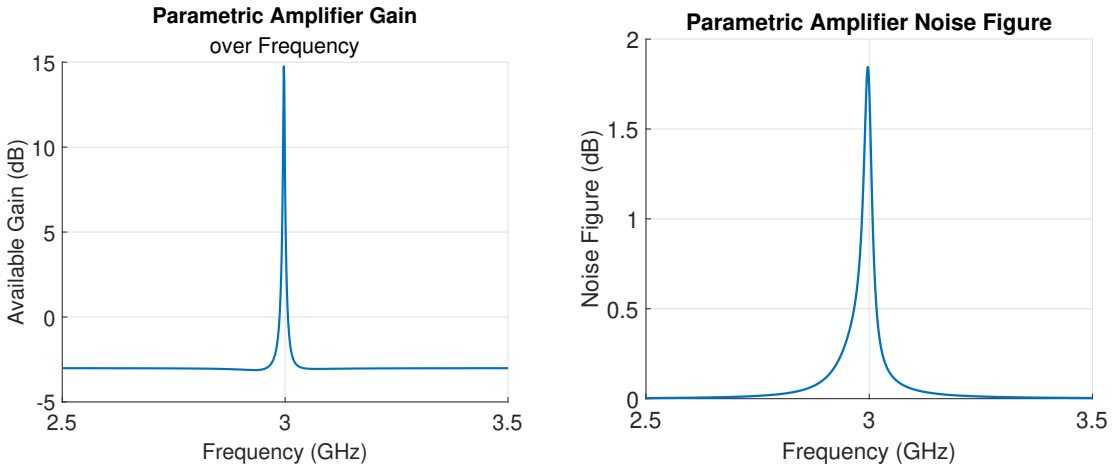

Figure 3.14: The noise figure and gain of the parametric amplifier with for a 21.8Ω load resistances.

Chapter 4

Cavity-Amplifier Integration

While it may be possible to design the cavity and amplifier separately to present potentially stable input impedances at 3GHz, this does not guarantee stable performance of the device [23], [12]. This instability would be caused by the wide-band performance of the amplifier being neglected and instability in the band near to the center frequency. By accounting for this wide-band performance and properly loading the amplifier across frequency, gains of 10dB or greater are achievable in simulation with stable operation at all frequencies.

Until now, the reflection amplifier and cavity resonator have been designed separately. The cavity is at the correct center frequency, but an arbitrary weak coupling presented to the amplifier has yet to be properly designed. The transistor amplifier has been roughly designed so that the negative resistance exists over a small band and rolls off quickly, peaking at 3GHz. An estimate of the total impedance presented by the amplifier is available through the simulation of this design. The varactor based amplifier has been designed, but what loads the amplifier must be determined. For both amplifiers, the cavity coupling must be adjusted to present a target load. This load will be used as a basis to adjust the amplifier, maximizing gain while maintaining stability at all frequencies. The specific load presented by the amplifier may need to be adjusted to extract the best stable gain from each amplifier. Redesigning and simulating the cavity is time consuming, so lumped impedances are used to adjust the presented cavity impedance instead. Once the amplifier design has finalized

based on the narrow-band load, the cavity is given one final adjustment and the design is complete. Simulation is completed through the ADS harmonic balance and transient solvers with good agreement between both.

4.1 Cavity Adjustment

At this point, the amplifiers and cavity are not able to be integrated as the load presented by the cavity is unlikely to be sufficient to stabilize the device across frequency and return the maximum gain from the amplifier at the center frequency. The cavity parameters must be adjusted into a range which the amplifier can be designed around. Using the S-Parameter data from the amplifier simulations, we have found a target input impedance to be presented by the cavity for each amplifier. Here, two options for presenting a valid cavity input impedance present themselves. Either the resistance presented by the cavity port is corrected and the reactance necessary to match the amplifier will be presented by series lumped elements, or the total target impedance can be presented entirely by the port. The first method offers an option to tune the reactance match later by switching out the lumped element in simulation, but relying on the lumped element may reduce the bandwidth or other operating statistics of the structure if used in the final design. Therefore, the final design of the cavity will have the total impedance presented by the cavity. This is done in three parts.

First, an input impedance presented by the amplifier, $Z_{amp} = -X - jY = -a - jb$, has already been found for both amplifiers in chapter three. The expected amplifier load is then $Z_{expected} = 1.5a + jb$, creating a conjugate matched load with much greater resistance for stability. The negative resistance presented by the amplifier will later be adjusted to maximize gain while maintaining stability for the specific impedance presented by the cavity. Here, we plot the expected load and the current cavity input impedance at 3GHz onto a smith chart. The initial cavity impedance is likely to be on another VSWR circle than the expected

load. A greater VSWR implies under-coupling, while lesser VSWR implies over-coupling. By adjusting the coupling via depth, coupling is amended and the cavity impedance can be moved to the correct VSWR circle. Now, the load phase must be corrected. An angle can be drawn from the current cavity impedance, to the center of the smith chart and through to the expected load impedance. The electrical length of the transmission line necessary to move the cavity impedance to the expected load impedance can be found by measuring that angle. Once the transmission line is in place, the impedance presented by the cavity matches the expected load impedance. The S-Parameters of the cavity can then be exported as a touchstone file. An example of tuning the cavity impedance as described is now presented. This process is shown visually in Fig. 4.1.

4.1.1 Transistor Amp Based Integration

Integration begins by finding the estimated load necessary for the amplifier. The impedance presented by the amplifier is $Z_{amp} = -7.648 - j342.907$, as seen in Fig. 3.9, so the expected load is $Z_{expected} = 11.472 + j342.907$. By plotting both the expected load and current cavity input impedances in Fig. 4.1, the cavity is seen to be over-coupled, being closer to the center of the chart. The input impedance of port three was previously shown in Fig. 2.11. The coupling via depth is adjusted to bring the cavity load to the VSWR circle of the expected load.

It should be noted here the difficulty of accurately adjusting cavity coupling to present a specific load. Since the expected load is on the edge of the smith chart and close to an open circuit, microwave structures attempting to present specific impedances become especially sensitive to small changes. The coupling structure must weakly couple into the cavity to not disturb the strong coupling of the first and second port, so care must be taken to present the correct input impedance. With the cavity impedance and expected load on the same

VSWR circle, a transmission line can be used to correct the phase of the input impedance. The angle between input impedance, chart center and expected load is about 37.08°, the electrical length required to correct the input impedance phase. With a transmission line placed between cavity port and amplifier, the cavity now presents the expected load which the amplifier can adjust around to provide stable, high gain operation. The S-Parameter data of the cavity is exported from HFSS as a touchstone file and imported into ADS. A similar process is carried out for the parametric amplifier.

4.2 Harmonic Balance

With the cavity adjusted to provide a viable load to the amplifier, we now move on from the S-Parameter solver to the harmonic balance solver. Harmonic balance allows for the study of amplifier stability and noise while being more accurate to physical circuit operation overall.

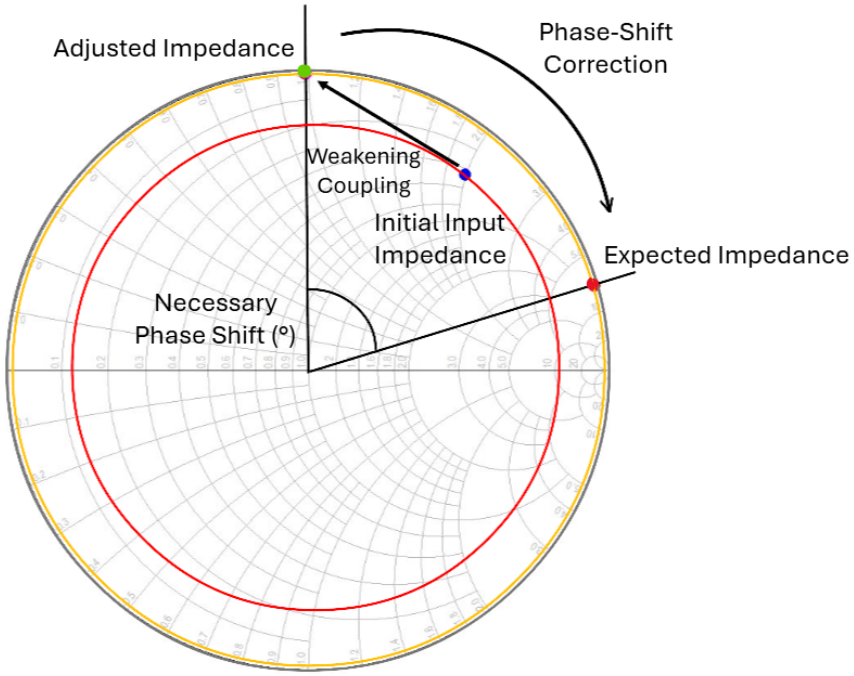

Figure 4.1: Visual representation of the process necessary to adjust the arbitrary impedance presented at port three to an impedance capable of loading the amplifier with low gain and stability.

This accuracy comes from the evaluation of the harmonics of device input frequencies and their mixing products if applicable.

4.2.1 Transistor Amplification with Harmonic Balance

The first measurements to look at when using harmonic balance is the transistor operating conditions. If the voltages or currents at the pins of the transistor are greater than the what can be tolerated, it is likely that the model will produce unrealistic results. With the transistor model safely within limits, we can begin calculating device gain. Typically, the voltages and currents at the input and output of the system are extracted to calculate input and out power, but the reflection amplifier output shares the same transmission line as its input. This leads to the input and amplified signal existing on the same branch, constructively or destructively interfering at the generator where the input power would be extracted. As such, you cannot extract voltage and current at the generator to determine input power. Instead, the available gain of the system is found with Eq. (3.21).

As the amplifier is connected to the cavity, some gain should immediately be seen, although it is unlikely to be at the correct frequency due to an imperfect match between the cavity and amplifier reactances. First, we will correct the location of the peak in frequency. Referring back to Fig. 3.8, the frequency shift is likely to be caused by a mismatch between cavity and amplifier reactances. By placing or adjusting a reactive element between the cavity and amplifier the mismatch can be corrected. Once the amplifier and cavity designs has been finalized, the cavity coupling will be adjusted to include the reactance of the corrective element into the input impedance of the cavity port if a corrective element is not desired in the final design. With the reactances matched for the center frequency, the emitter capacitance should be varied to ensure the maximum negative resistance, and therefore the maximum gain, is presented at 3GHz, as in Fig. 3.7. If after the previous

steps have been taken the desired gain has not been achieved, the base bias voltage can be adjusted to increase or decrease the negative resistance, and therefore the gain, generated by the amplifier. Thinking back to Fig. 3.5, increasing the base bias voltage will increase the negative resistance presented by the amplifier, so gain should increase as bias voltage increases. If the opposite occurs, the device is operating in an unstable regime. Harmonic balance does not verify stability, so the load resistance must be manually swept and the gain of the device for each load must be noted. If gain increases as load resistance decreases, up to the point where load and negative resistance are equal, then the device should be operating in a stable region. Otherwise, the load resistance is less than or equal to the negative resistance presented by the device and the system is unstable. As the bias conditions and emitter capacitance change, the capacitance presented by the amplifier will also change so the reactance match must be checked again. It should be noted that while high gains are theoretically achievable using the harmonic balance solver, the next step is to switch to the transient solver and a shift in the negative resistance generated by the circuit is likely. Should that shift increase the negative resistance, then the stability of the system may be broken.

4.2.2 Parametric Amplification with Harmonic Balance

Parametric amplification in harmonic balance is mainly dependent on two things, the time-varying capacitance and the resonators which separate the signal, idler, and pump branches. The resonators are dependent on the time-varying capacitance, so we ensure the diode model is working as intended first. To do so, we go back to the S-Parameters solver and extract the capacitance presented by the diode model for various reverse bias voltages, comparing these to datasheet values at their relevant test frequency. Next, the DC and pump voltages incident on the diode are verified. The voltages across frequency at the cathode of the varactor must

be inspected to ensure that the range of capacitance presented by the diode is as expected. If so, the branch resonators may be slightly out of tune and in need of adjustment. If this is the case, the inductance of each resonator should be varied slightly until gain is produced, starting with the signal resonator inductance. Resonator tuning should continue until the desired gain is achieved at the device's center frequency. If the target gain cannot be found, then the negative resistance generated by the device may not be large enough or may be too large. A lumped load should be attached to the amplifier and its value varied to determine the negative resistance generated by the device, and design specs adjusted accordingly.

4.3 Transient

At this point, the cavity and amplifier have been connected and a desired gain has been achieved across the input and output ports of the cavity in harmonic balance. Now, we move on to a time domain solver to more accurately assess the gain and wide-band stability of the physical device. Using a time domain solver, the stability of the device is assessed at all frequencies. If there is instability at any frequency, then noise generated by the device will spur oscillation at the unstable frequency [23]. It should be noted that all equations previously used for the S-Parameter or harmonic balance simulations are still valid, but care must be taken to translate time-domain data to frequency-domain using a Fourier transform.

The stability of the device is verified by inspection of the voltage and current at the cavity output. A well stabilized amplifier will output the center frequency of the device at a constant amplitude. If the matching reactance is off, a transient oscillation at the beginning of the time domain signal will appear which slowly decays away with a long enough time span, eventually reaching a steady state response. This transient oscillation will be exacerbated as the amplifier's negative resistance approaches the loading resistance. If the device is unstable, the oscillation will remain strong regardless of how much time passes. An example

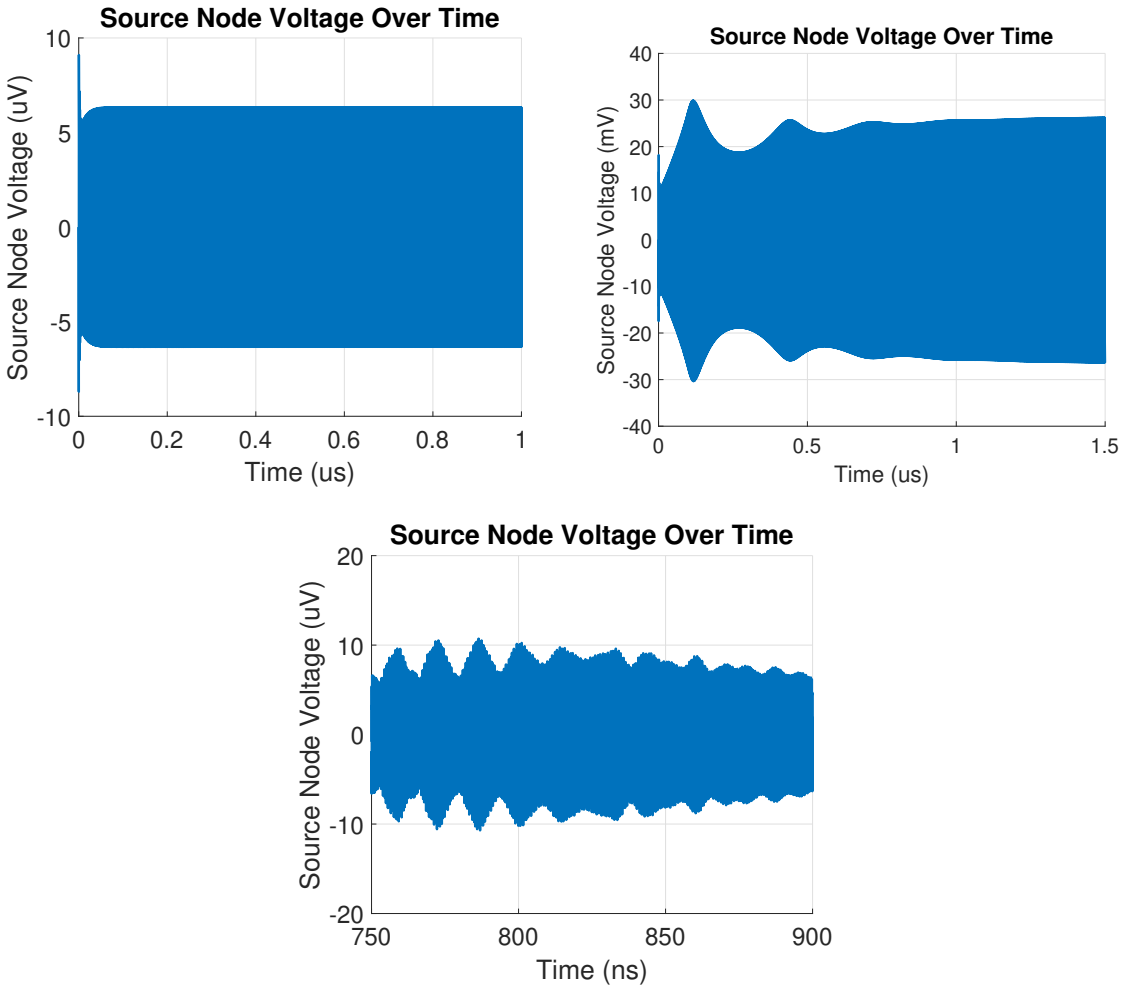

Figure 4.2: Example matched, unmatched, and unstable voltage and current waveforms. The well match amplifier (top left) generates a waveform with short lived transient effects. A reactance mismatch (top right) causes some transient effect, but eventually settles into a steady state response. An unstable amplifier (bottom) will continue to oscillate indefinitely.

of these behaviors is shown in Fig. 4.2. Once stability is confirmed, device gain must be verified. It is likely that the switch to transient solver has lowered the negative resistance presented substantially. Similar modifications as discussed in Section 4.2 may be used again to modify device center frequency, peak negative resistance, and available gain.

4.4 Conclusion

An overview of methods used to integrate and simulate the amplifier-cavity unit has been presented. By taking the impedance presented by an arbitrary amplifier, the input impedance presented by the cavity has been adjusted to a point viable for amplifier integration. The amplifier has then been adjusted to deliver the greatest stable negative resistance applicable to the narrow-band cavity input impedance. the stability and gain of the completed structure will be verified using the harmonic balance and transient solvers in Agilent's ADS circuit simulator. In the next chapter, the performance of the transistor and varactor based amplifiers is compared and a fatal design flaw regarding the noise generated by the transistor based amplifier is investigated. Additionally, the parametric amplifier-cavity will be compared to previous works from literature to highlight the increase in stable gain delivered by the amplifier

Chapter 5

Comparison of Amplifier Technologies

5.1 Design Results

5.1.1 Parametric Amplification

Starting with the parametric amplifier, Table 5.1 lists all component values related to the final design of the amplifier, while Table 5.2 lists all dimensions relevant to the final cavity design. The device characteristics are extracted using the harmonic balance and transient solvers. Specifically, harmonic balance and transient are used to find available gain, noise is reported directly from harmonic balance simulation, bandwidth is calculated via harmonic balance by sweeping input signal frequency, and stability is verified by inspection of the voltage and current waveforms at the output of the cavity in the transient solver. These operating statistics at 3GHz are relayed in Table 5.3 and noise and gain are displayed across frequency in Fig. 5.1.

5.1.2 Transistor Amplification

Now, the transistor based amplifier is discussed. All measurements taken for parametric amplified cavity are taken again for the transistor version. Table 5.4 lists all component values related to the final design of the amplifier, while Table 5.5 lists all dimensions relevant

Table 5.1: Component values for integrated parametric amplifier.

Signal Frequency	f_s	3 GHz
Pump Frequency	f_p	8.95 GHz
Idler Frequency	f_i	5.95 GHz
Varactor Loss	R_5	0.88 Ω
Average Capacitance	C_0	0.5 pF
Capacitance Amplitude	C_{11}	76.8 fF
DC Bias Voltage		2.925 V
AC Pump Voltage		0.705 V
Pump Generator Resistance	R_4	10 Ω
Signal Resonator Capacitance	C_1	0.1 pF
Signal Resonator Inductance	L_1	34.25 nH
Idler Resonator Capacitance	C_2	10 fF
Idler Resonator Inductance	L_2	73.03 nH
Pump Resonator Capacitance	C_3	10 fF
Pump Resonator Inductance	L_3	31.99 nH

to the final cavity design. Operating statistics at 3GHz are reported in Table 5.6 and noise and gain are displayed across frequency in Fig. 5.2.

5.2 Short Comparison

Both amplifiers achieved the design goals of having a 3GHz center frequency and a stable available gain greater than 10dB, though the parametric amplifier was capable of achieving a much greater 19.99dB of gain. The bandwidth of the transistor and parametric amplifiers are both small, which is due to the limited bandwidth of the cavity, matching of large reactances between transistor amplifier and cavity, and the bandwidth of the resonators in the parametric

Table 5.2: Component values for parametric amplifier integrated cavity. Design dimensions defined in Fig. 2.2, Fig. 2.4, and Fig. 2.7

Cavity Radius	b	14 mm
Post Radius	a	0.75 mm
Cavity Height	h	125 mil
Ring Width	w_r	0.25 mm
Ring Radius	r	4.39 mm
Feed Radius	f_r	11.75 mm
Feed Angle	f_θ	90°
Feed Width	w_f	0.45 mm
GCPW Gap Width		0.45 mm
GCPW Conductor Width		3.675 mm
3rd Port Via Radius		0.35 mm
3rd Port Via Length Into Cavity		1.95 mm

amplifier [28]. The parametric amplifier has a relatively much lower noise figure than the transistor amplifier, achieving a noise figure of 4.22dB.

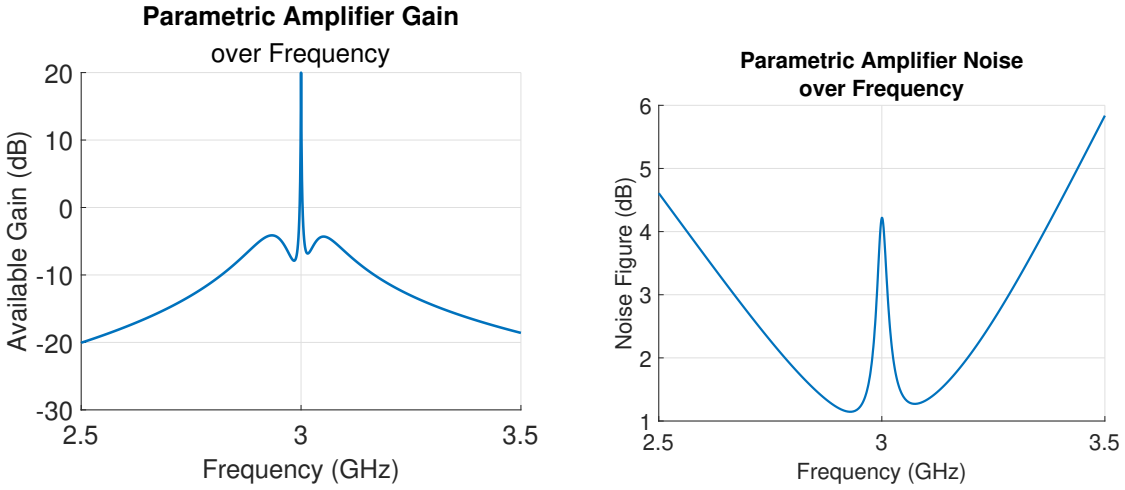

Figure 5.1: Noise and gain reported by ADS for final varactor based amplifying cavity.

Table 5.3: Parametrically Amplifying Cavity Operating Statistics at 3GHz

Center Frequency	f_c	3 GHz
Available Gain	G_A	19.99 dB
Noise Figure	NF	4.22 dB
Bandwidth	BW	0.639 MHz
Stability		Stable

Table 5.4: Component values for integrated transistor amplifier.

Center Frequency	f_s	3 GHz
Base Bias Current	I_{BB}	0.343 μA
Collector Bias Voltage	V_{CC}	0.87 V
Emitter Transmission Line Length		24.4°
Emitter Lumped Capacitance		2.3 pF
Collector Load	R_c	0.1 Ω

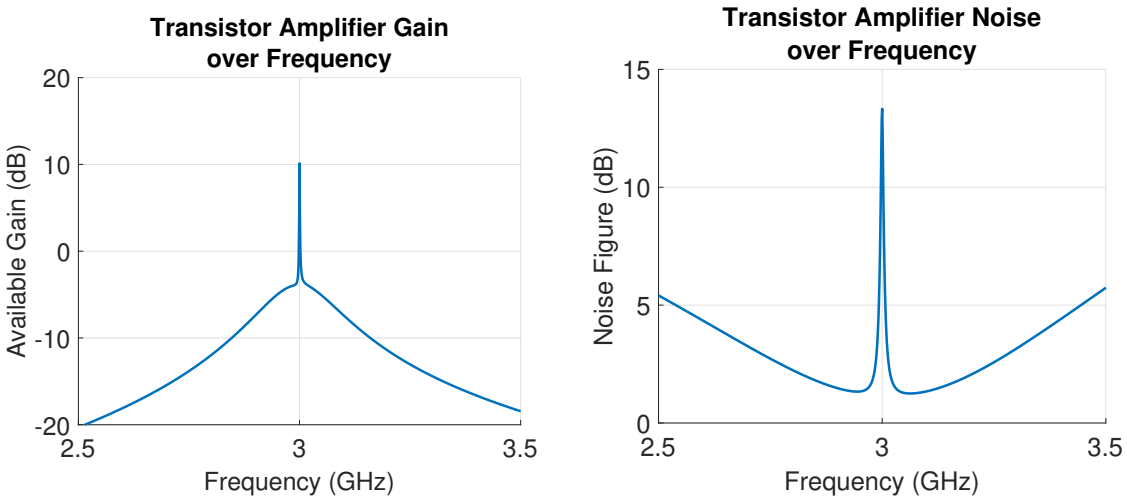

Figure 5.2: Noise and gain reported by ADS for final transistor based amplifying cavity.

Table 5.5: Component values for transistor amplifier integrated cavity. Design dimensions defined in Fig. 2.2, Fig. 2.4, and Fig. 2.7

Cavity Radius	b	14 mm
Post Radius	a	0.75 mm
Cavity Height	h	125 mil
Ring Width	w_r	0.25 mm
Ring Radius	r	4.39 mm
Feed Radius	f_r	11.75 mm
Feed Angle	f_θ	90°
Feed Width	w_f	0.45 mm
GCPW Gap Width		0.45 mm
GCPW Conductor Width		3.675 mm
3rd Port Via Radius		0.35 mm
3rd Port Via Length Into Cavity		1.4 mm

Table 5.6: Transistor Based Amplifying Cavity Operating Statistics at 3GHz

Center Frequency	f_c	3 GHz
Available Gain	G_A	10.11 dB
Noise Figure	NF	13.33 dB
Bandwidth	BW	0.97 MHz
Stability		Stable

5.3 Transistor Amplifier Noise

Taking a cursory look at the statistics of each amplifier design, it is immediately noticeable that the transistor based amplifier has a prohibitively large noise figure. In fact, with such limited gain and high noise figure, there would seem to be no point in designing an amplifier

Table 5.7: A comparison of presented and previous actively loaded structures.

Source	T. Amp	P. Amp	[3]	[10]	[22]
Center Frequency	3 GHz	3 GHz	2.5 GHz	137 MHz	95 MHz
Gain	10.11 dB	19.99 dB	1.5 dB	3.48 dB	-0.1 dB
Noise Figure	13.33 dB	4.22 dB	N.R.	4.9 dB	2.4 dB

like so. Other published transistor based reflection amplifiers [30] have shown similar gain with much lower noise figure. So, an investigation is made into the noise figure of the transistor based amplifier, what other authors have published, and why the noise figure of the transistor amplifier is unavoidably noisy given the constraints of the proposed design.

To begin, lets look back at the constraints necessary for the integration of the amplifier and cavity. It is necessary for the stability of the amplifier that the real input resistance presented by the cavity is greater than the negative resistance generated by the amplifier at all frequencies. Given that the input impedance presented by the cavity, which loads the amplifier, rolls off as frequency diverges from it's center, this means that the peak negative resistance generated by the amplifier must coincide at the center frequency of the cavity. Otherwise, the first constraint would likely be violated. If these precepts are not followed, then stable operation can only be achieved with very low gain. The operating statistics of several of these systems found in literature have been summarized in Table 5.7

With the limited number of examples in Table 5.7, there is not enough evidence to make a definitive conclusion, but the data available suggests that the noise figure produced by structures with integrated reflection amplifier is commonly an issue. To rectify the low sample count, a parametric sweep of many possible amplifier designs was conducted, with the gain and noise figure of each design at 3GHz being plotted in Fig. 5.3 to potentially find any amplifier configuration with decent characteristics. Several variation which were

unstable at 3GHz have been removed from the dataset.

Although many variations perform poorly due to mistuning, there appears to be a grouping of amplifiers with much greater gain and lesser noise figure than previously presented. While these designs may appear promising, a closer look at their performance across frequency highlights why they are not viable arrangements. The negative resistance curve and noise figure across frequency for the variation presenting 21dB of gain and 4.4dB of noise figure is presented in Fig. 5.4.

Now we can see the flaw in this low noise design is its wide-band stability. While the load presented to the amplifier of 12Ω is unstable for the 12.922Ω of negative resistance at 3GHz, the more damning fact comes from looking at wideband performance. The peak in negative resistance of 23.026Ω is firmly detached from the center frequency of the amplifier. As such, this amplifier would be strongly unstable even if the load resistance was increased to compensate for instability at the center frequency. This instability is confirmed in Fig. 5.5. We can see that if the negative resistance peak is shifted back to 3GHz, as in Fig. 5.6, then

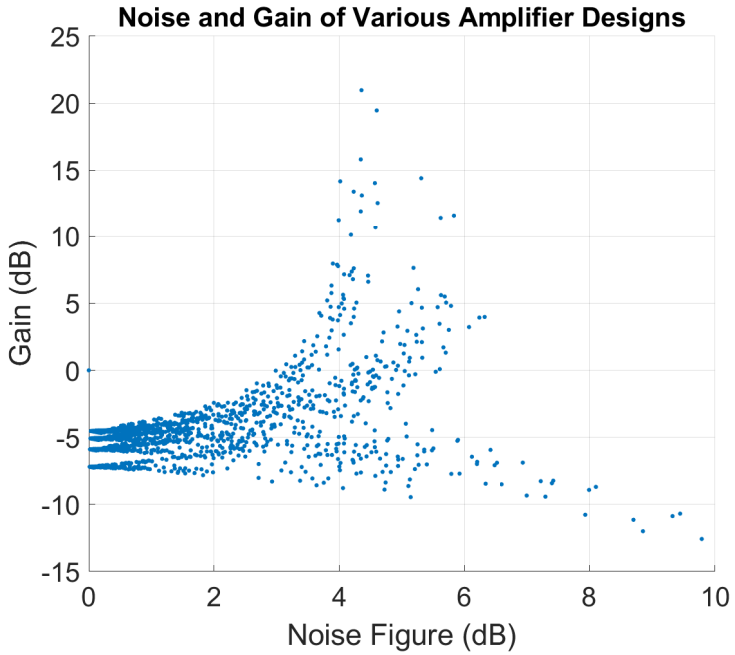

Figure 5.3: Gain and noise figure of various transistor based amplifier designs.

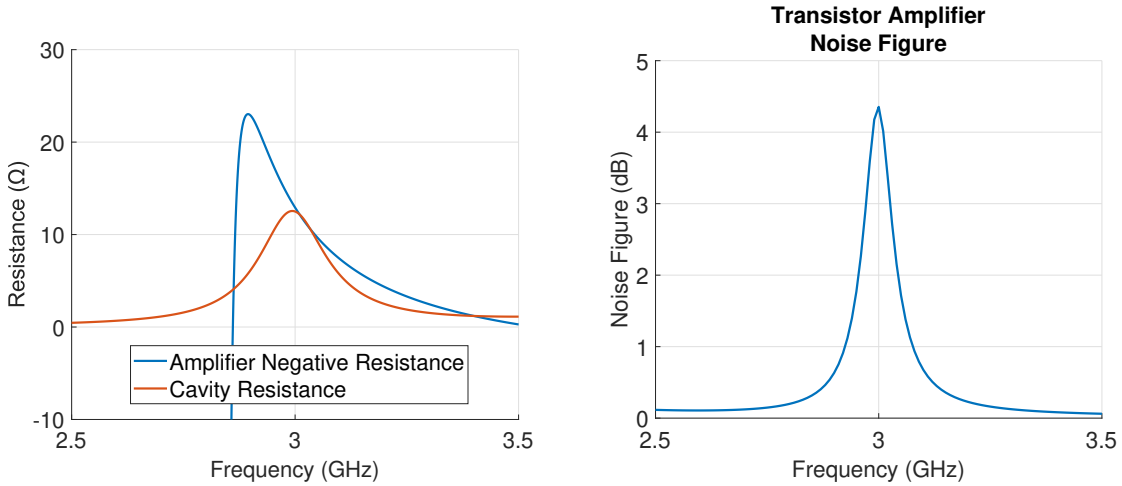

Figure 5.4: Negative resistance and noise figure of the "best" transistor based amplifier variation.

the high noise of the amplifier returns. Further, if the base bias current is adjusted so the negative resistance is stabilized at all frequencies by the previously designed cavity, the gain and noise figure of the initial amplifier is approximately replicated, as seen in Fig. 5.7. A new cavity could be designed to accommodate the large negative resistance, but it is unlikely that the negative resistance generated would be stabilized at all frequencies and the stronger coupling required may degrade the coupling strength of the first and second cavity port.

With this investigation completed, the reasoning has become clear. Due to the narrow bandwidth with which the cavity can stabilize the amplifier properly, the amplifier design is obligated to be pushed to a heavily noisy operating point. Further, the maximum gain of the device is limited due to the wide-band stability conditions again imposed by the cavity.

5.4 Conclusion

The results of executing the previously described integration techniques has been presented. The high gain and low noise figure of the parametric amplifier, 19.99dB gain and 4.22dB noise figure, exemplify the success of the design, with the alternative transistor based design delivering 10.11dB of gain and 13.33dB of noise figure. With this, it has now been shown in

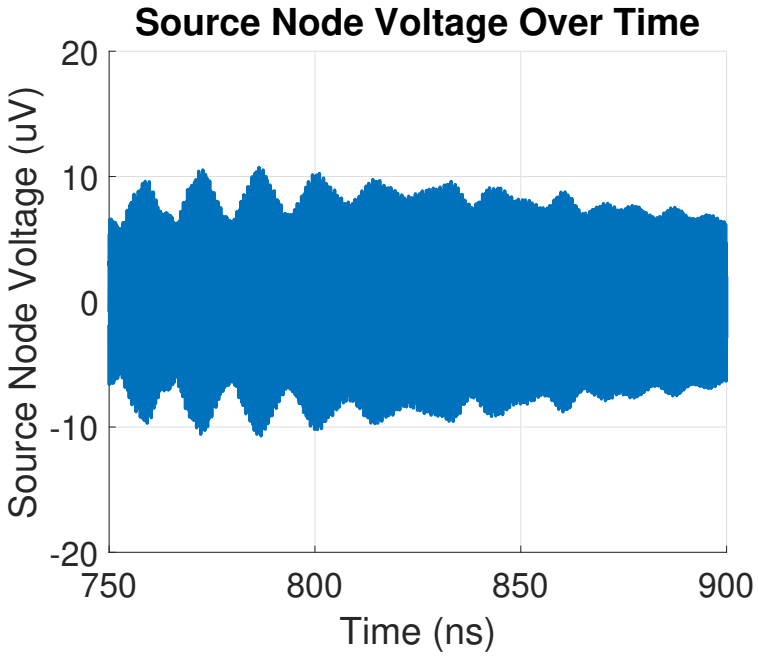

Figure 5.5: Unstable voltage waveform generated by the "best" transistor based amplifier variation.

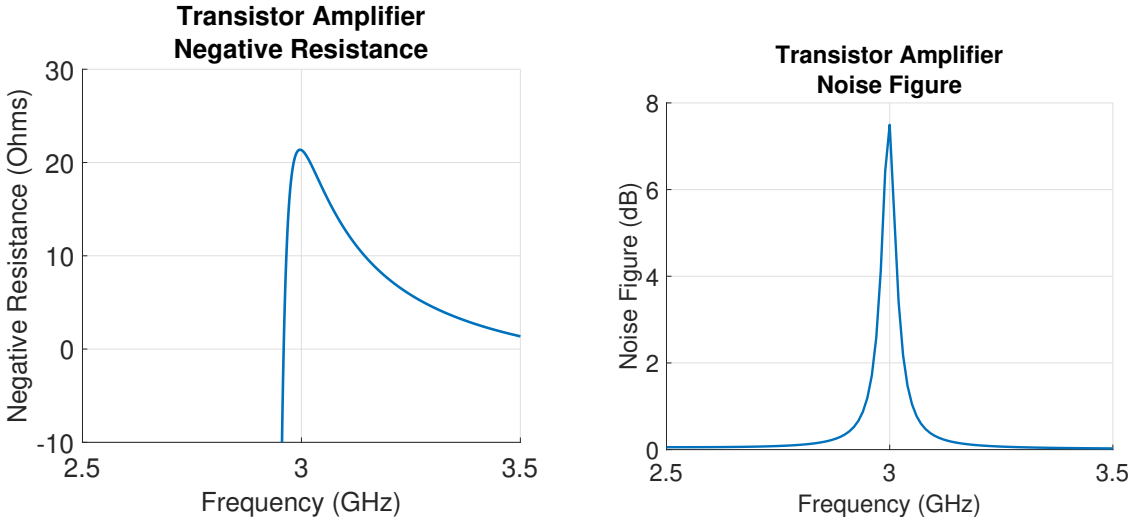

Figure 5.6: Gain and noise figure of transistor amplifier variant with negative resistance curve maximum shifted to 3GHz.

simulation how to present the maximum gain possible in an actively loaded resonator.

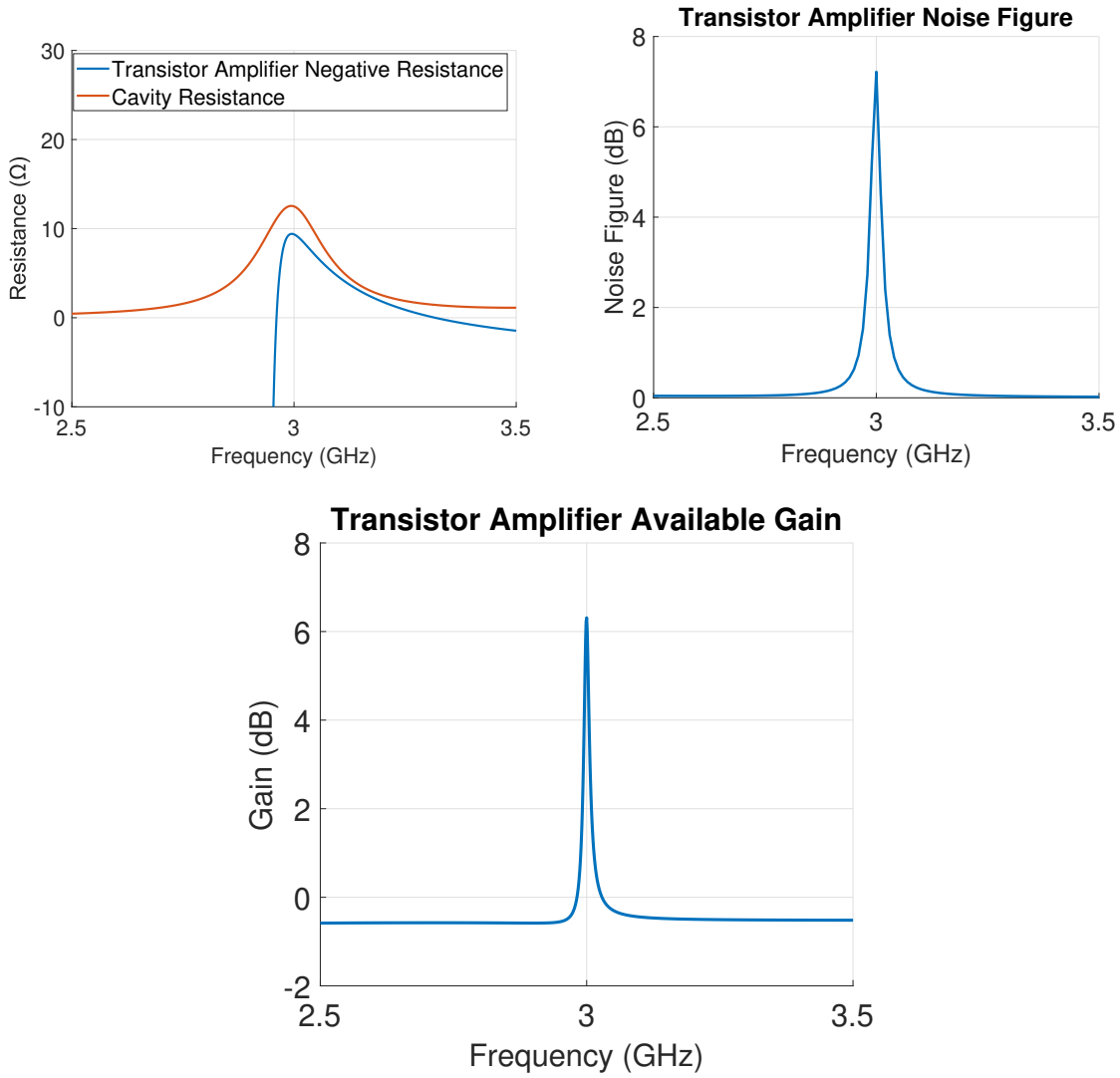

Figure 5.7: Gain and noise figure of transistor amplifier variant adjusted for stable operation.

Chapter 6

Conclusion

6.1 Summary of Work

The goal of this thesis was to integrate an active device into a cavity resonator with arbitrarily high gain to act as a foundation for the integration of active devices into other distributed structures using resonators such as antennas, filters, couplers, and so on. This was accomplished through the integration of several reflection amplifiers. A comparison between the amplifier topologies was made, and the conditions which contributed to excessive noise generation were discussed. As a result, the maximum stable gain provided by actively loaded structures has been increased substantially.

The method in this work was completed as follows. First, a cavity and reflection amplifier were independently designed. The coupling structures of the cavity were adjusted to present an impedance capable of stabilizing the amplifiers. Next, the amplifier was fine tuned to present the maximum possible gain at the center frequency of the cavity. This was done by maximizing negative resistance at the center frequency while minimizing negative resistance elsewhere to maintain the overall stability of the structure. Finally, as the amplifier and cavity were directly connected, the performance of each system was determined, and an investigation into the excessive noise produced by one topology was presented.

6.2 Novel Contributions

The work presented in this thesis contributed to the field of integrated microwave devices as follows:

- Identification of conditions leading to instability in actively loaded resonators.
- Design procedure for the integration of active circuits into resonators.
- Demonstration of actively loaded resonator with novelly high gain of 19.99 dB and noise figure for cavity and amplifier of 4.22dB in simulation.
- Analysis of conditions contributing to large noise figures for capacitive degeneration transistor amplifiers.

6.3 Future Work

Fabrication and Verification of Designs

The next step for the presented work is the physical verification of the proposed amplifying cavities. To do so, it would be prudent to break this verification into several steps. First, the cavity resonators should be individually manufactured and their input impedance verified. Although not presented previously, some time was taken to physically verify the proposed cavities. Measurements of these prototypes led to the conclusion that manufacturing tolerances must be considerably tight, as a shift in the gap width of the CPWG lines or capacitive ring-gap leads to a significant alteration to the actual input impedance of the cavity. Second, impedance presented by the amplifiers should be individually tested. As with any application, differences between the simulated and manufactured circuits are bound to exist, and a radical shift in either the resistance or reactance presented by the amplifier will lead

to serious degradation of performance. Only once both parts of the structure are verified independently should the combined design be tested.

Reflectionless Load Moderating Structures

The main constraining factor for the noise and gain performance of the transistor based amplifier presented is the impedance presented by the microwave cavity and its strong roll off. If a wide-band resistance could be presented to the amplifier, then the design should be able to be pushed into a high gain, low noise operation similar to the parametric amplifier. There is already a known structure with potential to do just that. A reflectionless band-pass filter [31] placed between amplifier and cavity would be capable of presenting an impedance great enough to stabilize the amplifier outside of its center frequency. The filter will not affect the normal performance of the amplifying cavity otherwise. With this structure, the amplifier can operate with the peak in negative resistance far from the center frequency of the device, decreasing overall noise figure and potentially increasing the maximum stable gain achievable with this topology.

Expansion into Amplifying Filters

The most immediate next step to progress towards a fully monolithic RFFE would be the integration of an amplifying cavity into a cavity-based filter. This would combine the amplifying and filtering portions of the receiver. Typically, a cavity based filter connects two or more passive microwave cavities, and the coupling between them is controlled to form a filter response. By introducing amplification to one or both of these cavities, a monolithic amplifier-filter can be formed. This can be taken further still by the introduction of an antenna. A combined antenna-filter structure has already been demonstrated [2], so the integration of all three components is feasible.

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