POWER MODELING OF CMOS DIGITAL CIRCUITS

WITH A PIECEWISE LINEAR MODEL

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LIST OF PHYSICAL CONSTANTS AND PROCESS PARAMETERS

ε_0 $= 8.85 \times 10^{-14}\ F/m$

ε_{ox} $= 3.97$ for silicon dioxide

k $= 1.3803 \times 10^{-23}\ Joule/^0K$

kT $= 4.1409 \times 10^{-21}$ Joule for room temp. at 27^0

q $= 1.6 \times 10^{-19}$ Coulomb

C_{ox} $= \dfrac{\varepsilon_{ox} \cdot \varepsilon_0}{t_{ox}} = \dfrac{3.51 \times 10^{-11}\ F/m}{t_{ox}(m)}$ (for the gate oxide on silicon)

β_n $= \mu_n \cdot C_{ox}$

β_p $= \mu_p \cdot C_{ox}$

LIST OF SYMBOLS

Symbol	Meaning	Unit
a_n	Ratio of conductance and trans-conductance for the nMOS transistor	
a_p	Ratio of conductance and transconductance for the pMOS transistor	
β	Effective transistor strength	$A.V^{-2}$
$\mathbf{C}$	Capacitance matrix	F
C_d	Depletion layer capacitance	F
C_{GG}	Linearized parasitic capacitance on the gate of the transistor	F
C_{GS}	Linearized parasitic capacitance on the gate-source of the transistor	F
C_{gdo}	Voltage independent gate-drain overlap capacitance per unit gate width	$F.m^{-1}$
C_{gso}	Voltage independent gate-source overlap capacitance per unit gate width	$F.m^{-1}$
C_{OX}	Oxide capacitance per unit area	$F.m^{-2}$
$E_{I_{vdd}}$	Energy dissipation due to the short-circuit current and dynamic current	J
$E_{i_{vdd}}$	Energy dissipation due to the first-order channel capacitive currents	J
G_m	Conductance of the m-th transistor	S
$\mathbf{G}$	Conductance matrix	S
E/T	Energy dissipation per switching cycle	J/S
ε_0	Permittivity of vacuum	$F.m^{-1}$
ε_{ox}	Relative permittivity of oxide	
I_{vdd}	Zero-order power supply current in the piecewise linear transistor model	A
i_{vdd}	First-order power supply current in the piecewise linear transistor model	A
I_{Sm}	Zero-order piecewise linear switching source current of the m-th transistor	A
i_{Sm}	First-order piecewise linear switching source current of the m-th transistor	A
I_{Dm}	Zero-order piecewise linear switching drain current of the m-th transistor	A
i_{Dm}	First-order piecewise linear switching drain current of the m-th transistor	A
I_{SC}	Short-circuit current	A

k	Boltzman's constant	$J.K^{-1}$
τ	Delay time	second or s
τ_r	Delay time for rising signal	second or s
τ_f	Delay time for falling signal	second or s
μ_n	Channel electron mobility	$m^2 V^{-1} s^{-1}$
μ_P	Channel hole mobility	$m^2 V^{-1} s^{-1}$
P_{avg}	Average power dissipation	W
$P_{dynamic}$	Dynamic power dissipation	W
P_{SC}	Short circuit power dissipation	W
P_{OFF}	Off-state leakage power dissipation	W
I_T	Zero-order quasi-static current in the transistor channel	A
i_T	First-order quasi-static current in the transistor channel	A
V_{DSsat}	Drain-source saturation voltage of the transistor	V
V_T	Transistor threshold voltage	V
$\tilde{V}$	Approximated output voltage in the steady state	V
$\dot{\tilde{V}}$	First-order terms for the approximated output voltage	V
$\ddot{\tilde{V}}$	Second-order terms for the approximated output voltage	V
V	Output voltage of the resistive connected node	V
S	Sub-threshold slope	mV/decade
T_{Tin}	Input transition time	s
t_{ox}	Gate oxide thickness	m
x_{Part}	Parameter for the channel charge partition	
ϕ_B	Built-in potential of the bottom wall junction capacitance	V
ϕ_{BSW}	Built-in potential of the isolation side sidewall junction capacitance	V
ϕ_{BSWG}	Built-in potential of the gate side sidewall junction capacitance	V

CHAPTER 1

INTRODUCTION

1.0 Purpose of the Study

Power dissipation is one of the major concerns for high speed very large scale integrated circuits (VLSI) design. Power dissipative components in CMOS circuits consist of off-state leakage power, glitch power, and switching transient power. This paper presents a piecewise linear modeling of switching transient power of CMOS digital circuits, which includes the short-circuit power, dynamic power, and switching power of parasitic capacitors. The piecewise linear power model takes a simplified approach to compute average power (or energy per cycle) without solving differential equations with large matrices. Even thought SPICE (Stanford Program for Integrated Circuit Emulation) can handle the accurate and nonlinear behaviors of transistors with more than one hundred fitting parameters, it usually takes a great amount of computation time for a large circuit simulation. Another competing circuit simulator is the switch level simulator, IRSIM, which is a tool for simulating digital circuits. It is a switch-level simulator, because the transistors are treated as ideal switches, and the extracted capacitances and resistances are used to find the RC time constants for the ideal switches

to predict the relative timing events [34]. Thus, it is an ideal transistor model, and is not accurate in computing transient switching power. The proposed piecewise linear model, as an improved switch resistor model, closes the performance gap between SPICE and switch-level simulators in power estimation.

1.1 Significance of the Study

Dynamic power dissipation is well known and defined for CMOS digital circuits. Analytical works, more recently, for power modeling are focused on short-circuit power modeling with slope effects, velocity saturation and gate-to-drain capacitive coupling effects, propagation delay and short channel effects. Analytical works in off-state leakage power modeling are also popular as the transistor size shrinks into the deep submicron realm. However, channel capacitive currents induced power dissipation is not addressed in other transistor models [4] [6] [7] [13]. Therefore, the proposed piecewise linear model not only includes the first-order capacitive currents but also takes into account the effect of the slope of the input waveform in average power estimation. Most fast simulators [34] [39] assume a step input, so that the piecewise linear model is at least an improved yet simplified nonlinear transistor model to replace the traditional resistor model in fast simulators. The piecewise linear model is verified in the submicron AMI CMOS 0.5μm and deep submicron TSMC 0.18μm process.

1.2 Limitation of the Piecewise Linear Model

The model is constructed with *I-V* and *C-V* models approximating the complex BSIM (Berkeley Short-Channel Insulated gate field effect transistor Model) model [4] for CMOS transistors as switches. The current–voltage (*I–V)* model describes the zero–order (dc) behavior of a quasi-static current between the source and drain terminals, and the capacitance–voltage (*C–V)* model describes the first-order dynamic behavior of channel capacitive currents associated with transistor parasitic capacitances. The piecewise linear *I–V* model approximates the physical transistor current with different piecewise linear regions in cutoff, ohmic, and saturation. The proposed model shows that its accuracy is within 3 to 5 % of SPICE for fast inputs in AMI 0.5μm and TSMC 0.18μm processes, and the accuracy may reach 15 to 20 % error for input transition times greater than 2000 pico-second in AMI 0.5μm process and 1000 pico-second in TSMC 0.18μm process. However, very slow input occurs not very often in submicron technologies and can usually be speeded up with circuit design techniques.

1.3 Introduction to the CMOS logic families

1) Standard CMOS logic gates

A standard CMOS logic gate has the same number of pFETs and nFETs with the transistors connected in a complementary manner. A standard CMOS inverter, NAND, and NOR may be designed with different sizes to meet speed and power requirements. Most power dissipation of CMOS circuits comes from the switching transient power, which includes the short-circuit power, and dynamic power. A piecewise linear model to calculate the average power dissipation of a CMOS inverter (Fig.1.1), a two-input NAND

gate (Fig.1.2), and a three-input OAI (Or-And-Invert) digital circuit (Fig.1.3) driving a constant capacitor or driving various sizes of inverter loads, are chosen to compare modeling accuracy with the average power of the power supply as predicted by SPICE.

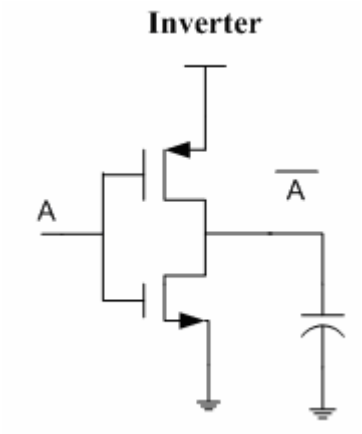

Figure 1.1 CMOS inverter

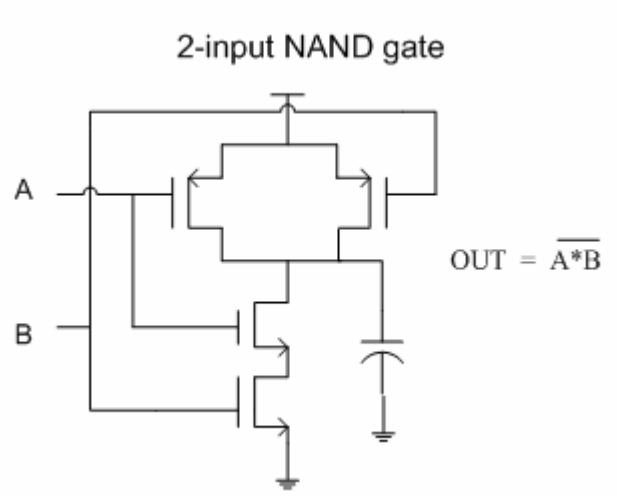

Figure 1.2 CMOS two input NAND gate

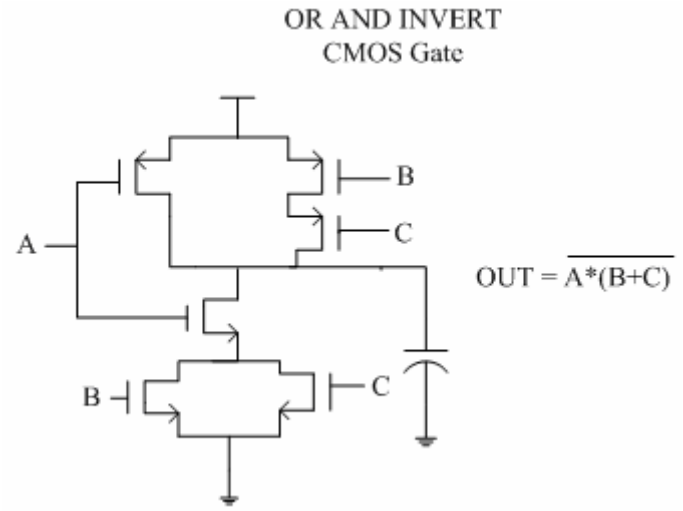

Figure 1.3 CMOS OAI gate

1.4 Organization

In chapter two, conventional power models are introduced along with literature reviews of off-state leakage power, short circuit power, glitch power, and dynamic power models. In chapter three, the piecewise linear switching current–voltage (I-V) model and channel storage charge or channel capacitance–voltage (C-V) model are introduced. I-V and C-V models in the piecewise linear model are used to demonstrate the model in computing average power from the power supply currents. In chapter four, computing average power with the piecewise linear model is coded in C++ language for an inverter. In chapter five, more complex circuits are chosen. Average power evaluations for two-input NAND and Or-And-Inverter (OAI) with various transistor sizes and loads are presented. Findings and conclusion are presented in chapter six.

CHAPTER 2

CONVENTIONAL TRANSISTOR MODELS FOR POWER ESTIMATION

2.0 Definitions: Energy or Power

The use of power as a performance measure is often misleading. In battery operated devices, the amount of energy needed for operations may be a more useful measure because a battery stores a finite amount of energy, not power [35]. Energy per operation or average power is often used to evaluate energy efficiency of CMOS circuits. Definition of instantaneous power and average power (or energy per cycle), is summarized as follows.

The instantaneous power $P(t)$ is proportional to the power supply current $I_{vdd}(t)$ and the supply voltage [8], which is written as

$$P(t) = I_{vdd}(t) \cdot V_{dd} \tag{2.1}$$

The average power dissipation P_{avg} is defined as an integration of instantaneous power $P(t)$ over some time interval T. Also, the average power dissipation is equivalent to the energy consumed over some interval T [8] and is written as

$$P_{avg} = \frac{1}{T}\int_0^T I_{vdd}(t) \cdot V_{dd}\ dt = \frac{E}{T} \tag{2.2}$$

Energy 'E' is calculated from the integration of instantaneous power supply current during the period when the instantaneous power supply current enters the circuit [8].

2.1 Sources of CMOS Power Dissipation

Transistor dissipative power is mainly due to the currents from the channel inversion layer traveling in a resistive channel between source and drain terminals. Unfortunately, the power supply current into the transistor channel is a nonlinear function of terminal voltages. Transistor channel currents are, in fact, space-averaged quasi-static currents in the channel [6], which includes the voltage-dependent quasi-static current component and a time-varying charging current component [25]. Conventional transistor models [25] show that quasi-static currents in the channel consist of the following components.

$$I_T = h_T(V_D, V_G, V_B, V_S) \tag{2.3}$$

$$i_T(t) = h_T(v_D(t), v_G(t), v_B(t), v_S(t)) \tag{2.4}$$

The channel current I_T expressed in (2.3) is a function of the terminal voltage on the gate, source, drain, and substrate of the transistor [25] without time-varying voltages. Thus, the expression for I_T is, in fact, a zero-order quasi-static DC model. Channel capacitive currents which are equivalent to "charging currents" [25] in (2.4) are function of the time derivatives of the channel charge storage, which depends on the time-varying voltages associated with each terminal [25] [33], therefore, it is the first-order quasi-static capacitive currents associated with voltage-dependent parasitic capacitances. Figure 2.1 illustrates the FET device with parasitic capacitances. Five distinct types of transistor current contribute to the power dissipation of a CMOS circuit.

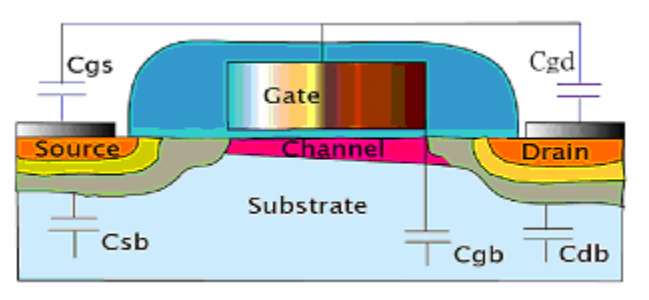

Figure 2.1 Four terminal MOSFET device and its parasitic capacitances

I. Transistor off-state sub-threshold leakage currents

II. Switching transient currents, which include

   1) Load capacitor charge and discharge through pFET and nFET network.

   2) Short-circuit current conduction between the power and ground nodes through both FET's simultaneously.

III. Channel capacitive currents due to switching transistors

IV. Glitch currents due to unequal arrival of signals to the circuit.

2.1.1 Off-State Leakage Power of the Transistor

For CMOS logic families and memory circuits, the performance factors include the ratio of off-state leakage current (sub-threshold conduction current) to turn-on current (I_{OFF} / I_{ON}), power, delay, and reliability [15]. Leakage current comes from gate, source, and drain terminals. Gate leakage occurs due to the scaling of gate oxide thickness and the resulting tunneling current from the gate to channel in the transistor as illustrated in Figure 2.2. A study [15] has shown that the gate oxide thickness T_{OX} can be thinned down to 2nm before the leakage current becomes unacceptable for CMOS circuits.

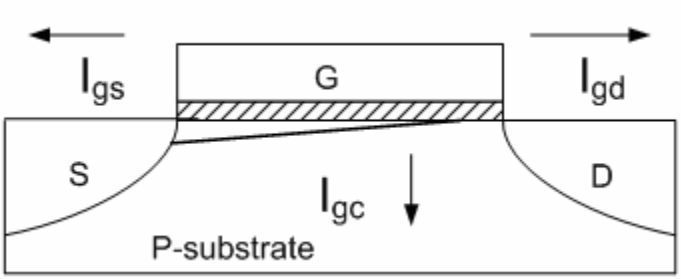

Figure 2.2 Off-state currents from the transistor gate to its conducting channel

The other concern for scaling oxide thickness thinner than 2 nm is that threshold voltage V_T can not be scaled down proportionally with the channel length. The primary barrier is a leakage current dependent sub-threshold slope, S, which is a measure of transistor turn-off rate from the gate voltage versus sub-threshold leakage current. *S* should be small in order to reduce leakage current. The sub-threshold slope is written as

$$S \cong \left(\frac{d}{dV_G}(\log \cdot I_{DS})\right)^{-1} = \frac{\ln 10(kT)}{q}\left(1 + \frac{C_D}{C_{OXIDE}}\right) \tag{2.5}$$

where q denotes the electron charge, $k = 1.38 \bullet 10^{-23}$ (J/K) Boltzmanns constant, T the absolute temperature in Kelvin, C_D the incremental capacitance of the depletion layer per unit area, and C_{OXIDE} is the capacitance of the gate oxide per unit area. The depletion capacitance is a non-linear function of the gate to bulk voltage. When V_{GB} increases, the value of C_D/C_{OXIDE} may become negligible. In other words, the sub-threshold slope is largely driven by thermally excited electrons in the channel and has no physical controllability from the manufacturing process. Even though CMOS scaling causes off-state power to increase, a study has shown that the off-state power is 0.01% of active power dissipation in a 1um process while 10% in a 0.1um process [15]. Although off-state power is not included in the piecewise linear approximation in this research, the simple off-state transistor power from equation (2.6) [15] can be approximated with the

currents of the transistors connected to the power supply for each piecewise linear region of operation, where W_{TOTAL} is the total turned-off transistors width with V_{DD} across them, and I_0 is the parameter for off-state current per device width, and V_T is the worse case threshold voltage.

$$P_{OFF} \cong W_{TOTAL} \cdot V_{DD} \cdot I_0 \cdot \exp(\frac{-qV_T}{kT}) \tag{2.6}$$

2.1.2 Switching Transient Power in CMOS Transistors

There are two components to the switching transient power: dynamic power dissipation and short-circuit power dissipation [8] [28], and the models are reviewed as follows.

1. Dynamic Power Dissipation in CMOS Transistors

Dynamic switching power occurs when the pFETs connected to the power supply turns on and a direct current path is established from the power supply to load capacitances. For standard CMOS circuits, the dynamic current consumption is dominated by the power supply current necessary to charge up node capacitances, and the dynamic power consumption $P_{dynamic}$ is proportional to the power supply current and the square of the supply voltage [8]. $P_{dynamic}$ is expressed as (2.7) [28].

$$\begin{aligned} P_{dynamic} &= \frac{1}{T_{sw}} \int_0^{T_{SW}} i_{vdd}(t)v(t)dt \\ &= \frac{1}{T_{sw}} \int_0^{T_{SW}/2} I_{Dp}V_{DSp}dt + \frac{1}{T_{sw}} \int_{T_{SW}/2}^{T_{SW}} I_{Dn}V_{DSn}dt \end{aligned} \tag{2.7}$$

where

$$I_{Dp} = -C_{load}\frac{dV_{out}}{dt} \tag{2.8}$$

$$V_{DSp} = -(V_{dd} - V_{out}) \tag{2.9}$$

$$I_{Dn} = -C_{load}\frac{dV_{out}}{dt} \tag{2.10}$$

$$V_{DSn} = V_{out} \tag{2.11}$$

Therefore, average dynamic power is the sum of power computed from the power supply current charging the load capacitance by the pull-up pFET network and discharging the same current by the pull-down nFET network for the second half of cycle. Such that,

$$\begin{aligned} P_{dynamic} &= \frac{1}{T_{sw}}\int_{0}^{T_{SW}/2} C_{load}\frac{dV_{out}}{dt}(V_{dd} - V_{out})dt + \frac{1}{T_{sw}}\int_{T_{SW}/2}^{T_{SW}} -C_{load}\frac{dV_{out}}{dt}dt \\ &= \frac{1}{T_{sw}}\int_{0}^{V_{dd}} C_{load}(V_{dd} - V_{out})dV_{out} + \frac{1}{T_{sw}}\int_{V_{dd}}^{0} -C_{load}V_{out}dV_{out} \\ &= \frac{C_{load}}{T_{sw}}V_{dd}^{2} \end{aligned} \tag{2.12}$$

For a general circuit topology with transistors and capacitors only, total dynamic power dissipation is often computed for switching of all of the nodes according to the switching activity (α_i) at the i^{th} capacitive node within a circuit, such that

$$P_{dynamic} = \frac{1}{T_{sw}}\sum_{i=1}^{N}\alpha_i \cdot C_i \cdot (V_i^{t_1} - V_i^{t_0})^2 \tag{2.13}$$

Dynamic power dissipation assumes that $v_i^{t_0}$, $v_i^{t_1}$ are full swing signal between ground and V_{dd} during a complete charge-discharge cycle. Since most gates do not switch every

clock cycle, it is convenient to write the switching frequency as switching activity factor times the clock frequency f_{sw} [8].

$$P_{dynamic} = \frac{1}{T_{sw}} \cdot V_{dd}{}^2 \cdot \sum_{i=1}^{N} C_i \cdot \alpha_i = f_{sw} \cdot V_{dd}{}^2 \cdot \sum_{i=1}^{N} C_i \cdot \alpha_i \quad (2.14)$$

2. Short Circuit Power Dissipation in CMOS Transistors

Short-circuit power is usually neglected in power calculations by switch-level simulators [34] [39], which often assume a step input response for fast simulation. Due to the intrinsic resistance and parasitic capacitances in a transistor channel, any transistor circuit takes a finite time to rise or fall to its final value at any given node. Therefore, real circuits are usually driven by input with a finite transition time, and consequently, short-circuit power can be as significant as the dynamic power [17] and cannot be neglected in power calculation. The short circuit power dissipation component is proportional to the input transition time and the load capacitance when a direct current path is established between the power supply and ground. Evaluation of the short circuit power component requires information about input transition times (input rise and fall times), transistor sizes, and the load driven by the circuit.

There are many analytical evaluations of the short-circuit power dissipation component for a simple inverter gate [17], [18], [19], and [20]. The first closed-form expression for the short-circuit power component for a CMOS inverter without load capacitor was from Veendrick in 1984 [17] [23]. The short-circuit power expression Veendrick derived assumed that the short-circuit current was symmetric for each input transition with a matched transistor's mobility and threshold voltage, with equal input rise and fall time τ in a periodic signal T as shown in Fig. 2.4.

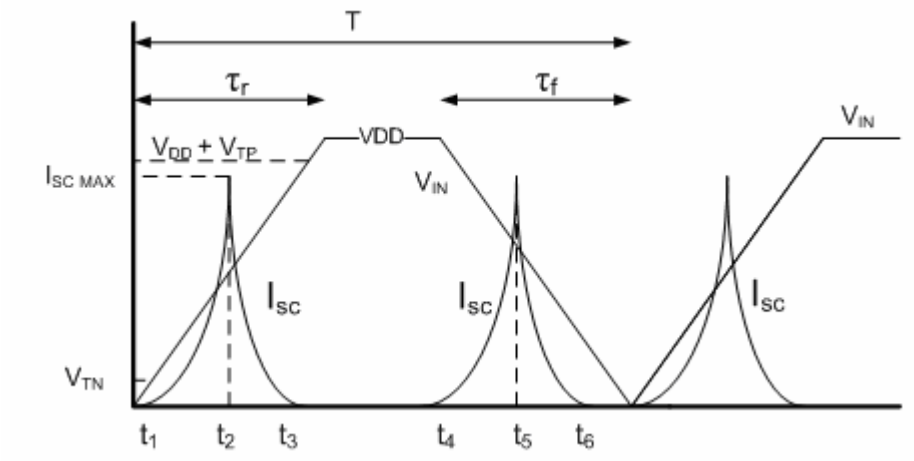

Figure 2.3 Veendrick's short-circuit current model of an inverter without load

Under Veendrick's assumption, short-circuit current component in an inverter was approximated by transistors in the saturation, such that

$$I = \frac{\beta}{2}(V_{IN} - V_T)^2 \qquad 0 \le I \le I_{SC\ MAX} \tag{2.15}$$

Since the inverter is symmetric about t_2, $I_{SC\ MAX}$ occurs at half of the supply voltage. The mean short circuit current is determined by integrating the instantaneous current from 0 to time T and divided by T. $2/T$ is the average number of transition per second.

$$I_{MEAN} = \frac{1}{T}\int_0^T I(t)dt = 2\frac{2}{T}\int_{t_1}^{t_2}\frac{1}{2}\beta(V_{IN}(t) - V_T)^2 dt$$

$$= 2\frac{2}{T}\int_{t_1}^{t_2}\frac{\beta}{2}\left(\frac{V_{DD}}{\tau}t - V_T\right)^2 d\left(\frac{V_{DD}}{\tau}t - V_T\right)$$

$$= \frac{1}{12}\frac{\beta}{V_{DD}}(V_{DD} - 2V_T)^3 \cdot \frac{\tau}{T} \tag{2.16}$$

where

$$\beta_N = \beta_P = \beta$$

$$\tau_r = \tau_f = \tau$$

$$V_{Tn} = -|V_{Tp}| = V_T$$

$$V_{IN}(t) = \frac{V_{DD}}{\tau} t$$

$$t_1 = \frac{V_T}{V_{DD}} \cdot \tau$$

$$t_2 = \frac{\tau}{2}$$

Therefore, following is the short-circuit power of a CMOS inverter with no load capacitance:

$$P_{SC} = \frac{\beta}{12}(V_{DD} - 2 \cdot V_T)^3 \cdot \frac{\tau}{T} \qquad (2.17)$$

The short circuit power expression (2.17) was solved as a function of the input rising and falling transition time (τ) without a load capacitance, and the result may lead to a pessimistic prediction of the short-circuit power dissipation, because Veendrick's short circuit power model assumed transistors operated in saturation region only, which cannot accurately predict short-circuit current as transistors in ohmic region. However, formula (2.17) clearly illustrates that the short-circuit power is proportional to design parameters β and input transition times (τ) of an inverter's input signal. For an inverter with a load capacitance, the transistor β values are determined by the required output rise and fall times [8]. Therefore, dependency of short-circuit power on the input rise and fall times is still valid when an inverter drives a load capacitance. More recently (1996), a closed form expression presented by Bisdounis et al. for short-circuit power dissipation was based on an output waveform expression with a square-law current transistor model [17]. Instead of using a square-law current model, Sakurai and Newton [22] suggested an α-power

model for the evaluation of short-circuit power dissipation component. Afterward, Vemuru and Scheinberg [23] developed a short-circuit power equation by adopting Sakurai and Newton's α-power MOS model. α-power model and the square law model were proved to be fairly accurate power models, but implementing the higher-order current model takes a fairly large computation time. Hirata, A., et al., [24] reported a piecewise linear function for the short-circuit power dissipation component in an inverter, but the model can not be extended to predict short-circuit power for other circuit topologies.

2.1.3 Glitch Power Dissipation in CMOS Transistors

It is well known that dynamic power dissipation is directly related to the number of signal transitions in full swing, but spurious transitions (or glitches) caused by unequal arrivals of propagation delays of input signals to the gate often occur in many static ICs [42]. Glitch power is often modeled by using the dynamic power dissipation model as equation (2.13) where $(V_i^{t_1} - V_i^{t_0})$ is the incomplete transition during a complete charge-discharge cycle [40] [41] [42]. Power estimation tools can simulate glitches at the gate level for medium size circuits, but the accuracy of glitch power predictions for large circuits is inadequate [42].

2.2 Summary

Modeling average power dissipation in CMOS circuits, at least, should include the following components for CMOS technologies.

I. Short-circuit power.

II. Dynamic power.

III. Switching power of parasitic capacitances.

Not all transistor models are capable of computing each power dissipation component. For instance, the switch-resistor model in IRSIM [13] [39] simulator can evaluate dynamic power dissipation only. Surprisingly, the HSPICE simulator, one of the most accurate SPICE circuit simulators, does not include the power dissipation caused by nonlinear parasitic capacitors [3]. Many researchers [19] [20] [22] [23] [24] [31] extend the α-power model to compute short-circuit power dissipation component, but none of the models has addressed the significance of channel capacitive currents in a power evaluation. Besides, the α-power model usually has a non-integer value for α, which is not efficient enough to be implemented in a fast simulator. The main difference of the proposed piecewise linear model from previous models in the literature is to compute the average power supply current provided to the circuit instead of evaluating individual power dissipative components for each transistor. In order to compute average power from the power supply current, including channel capacitive currents for a fast simulator, an efficient yet simple transistor model is essential. A simplified (piecewise linear) zero-order quasi-static switching current model and channel storage charge model are developed to serve the goal and are presented in the following chapter.

CHAPTER 3

A PIECEWISE LINEAR TRANSISTOR MODEL

3.0 Background

The circuit simulator, SPICE, was designed primarily to evaluate circuit performance during the explosive growth of integrated circuits in the late 1960's and early 1970's [38]. A fast simulator, RSIM, was built in the late 1980's and early 1990' became competitive with SPICE for its efficiency but not accuracy in simulating large integrated circuits [39]. The RSIM is a switch-level simulator with speedups of over three orders of magnitude over SPICE [13] [39]. Unfortunately, the switched-resistor model used by RSIM renders it incapable of simulating certain CMOS digital circuits [39] and does not compute power dissipation components other than dynamic power [34]. More recently, a piecewise linear gate modeling of CMOS circuits [36] has improved the switched-resistor model by incorporating a piecewise linear saturation current model and the effects of short-circuit current and channel capacitive currents into gate delay modeling. Also, the model with a fast algorithm for circuit dynamic analysis can predict gate delay within 10% average error of SPICE regardless of circuit topologies [36]. The goal of this research is to extend the same piecewise linear model to compute average power dissipation in CMOS circuits by evaluating average power supply current. The piecewise linear switching current model and part of the circuit dynamic analysis [36] are reviewed in the following section as an essential step to power estimation.

3.1 Evaluation of Average Power Dissipation with the Piecewise Linear Model

Rather than attempting to evaluate instantaneous power from each transistor device for each power dissipation component described at the end of chapter two, the proposed piecewise linear model evaluates average power by evaluating average power supply current from transistor(s) connected to the power supply. With the zero-order switching current-voltage (I-V) model and the channel charge storage or capacitance-voltage (C-V) model introduced in the following section, the average power from the power supply current is evaluated instead of evaluating each transistor with instantaneous current and voltage as functions of time.

During switching transients that turn off transistors connected to the power supply, only short-circuit current is included in $I_{vdd}(t)$ calculation because the discharging current for the node capacitance flows through the turn-on nFET network. In contrast, the sum of the dynamic current and the short-circuit current is included in $I_{vdd}(t)$ calculation when the transistors connected to the power supply turn on, because the charging current from the power supply for the node capacitance flows through the turned-on pFET network and the short-circuit current from the turning-off nFET network flows simultaneously. The switching power of any implicit parasitic capacitance is estimated from $i_{vdd}(t)$ with the channel storage charge (C-V) model. The power supply current is, in fact, the sum of the currents of every transistor and any explicit capacitance that is directly connected to the power supply. The instantaneous power, $P(t)$, in (2.1) is re-written as (3.1) for the average power evaluation from the piecewise linear model (3.2).

$$P(t) = \left[I_{vdd}(t) + i_{vdd}(t) \right] \cdot V_{dd} \tag{3.1}$$

$$P_{avg} = \frac{1}{T}\int_0^T \left[I_{vdd}(t) + i_{vdd}(t) \right] dt = \frac{E}{T} \tag{3.2}$$

The notation I_{vdd} is used to indicate the power supply current which contributes power dissipation due to the short-circuit current and dynamic current in CMOS circuits [10]. i_{vdd} will be used to indicate the power supply current which comes from the first-order switching power due to any implicit parasitic capacitance from transistors connected to the power supply.

$I_{vdd}(t)$ is evaluated by the model from the sum of each individual transistor source current $\mathbf{I_{S_m}}$, which represents the short-circuit current (or turn-off current) during input (0→1) transitions and also represents the power supply current required to charge the node capacitance (or turn-on current). Whereas $i_{vdd}(t)$ is estimated from the sum of the individual channel capacitive currents, $\mathbf{i_{S_m}}$, of each switching transistor connected to the power supply. The subscript stands for the source terminal of m-th transistor(s) connected to the power supply. The turn-off current and turn-on current will be used throughout the paper when the average power supply current is approximated with the piecewise linear model in each switching cycle. The method of computing average power dissipation can be extended for any multi-stage circuit that is partitioned into individual sub-circuit as shown in Figure 3.1.

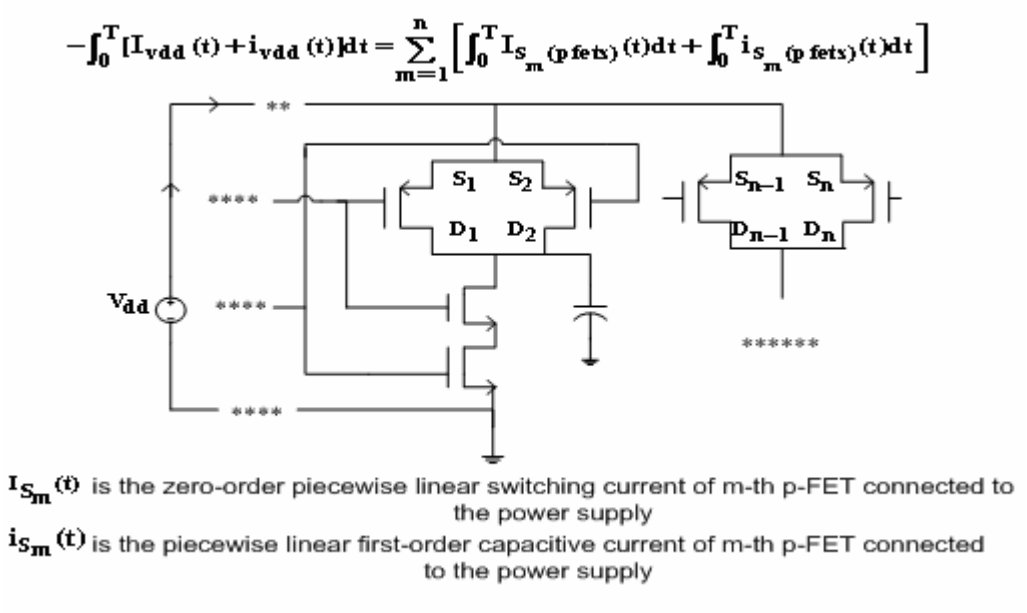

Figure 3.1 Evaluation of average power from the power supply current

3.1.1 Piecewise Linear Switching Current Model

The piecewise linear model for transistor switching is a voltage controlled switch with a series resistance. The simple linear model simplifies the circuit dynamics once the switches have reached their final states. Although the switched resistor model [13] has been used very successfully in circuit simulation [39], it is not adequate to describe the finite time required to switch the transistors on to off. Also, the saturation behavior of the transistors has a significant impact on the switching waveform and average power evaluation. Unfortunately, there is no linear model that can include cutoff, ohmic, and saturation behaviors simultaneously. Complex transistor behavior is simplified to three piecewise linear regions of operation as shown in Figure 3.2. The piecewise linear model is as follows.

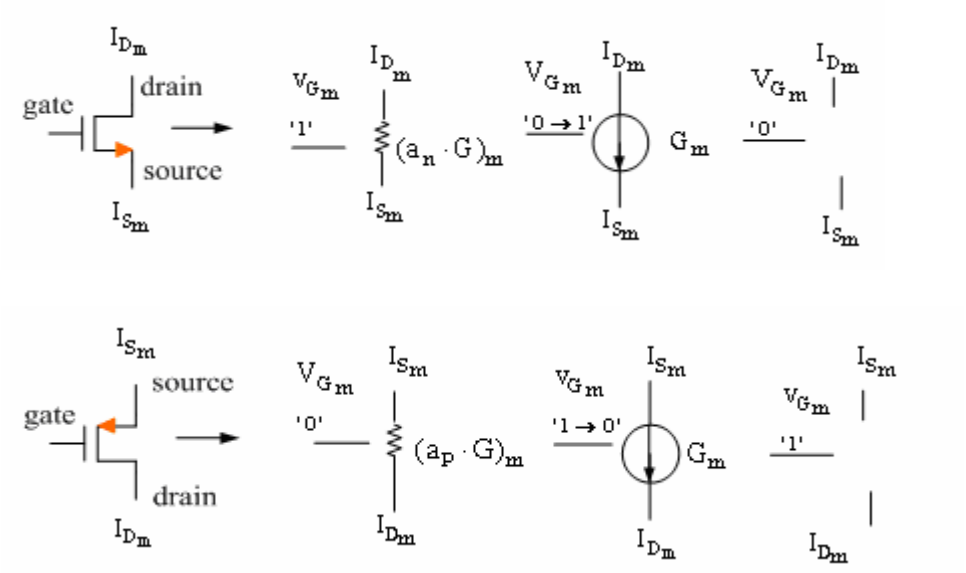

Figure 3.2 Transistor switch models in ohmic, saturation, and cutoff region respectively

The zero-order quasi-static switching current denoted as I_{Dm} and I_{Sm} (Fig. 3.2) for the drain and source terminal of the m-th transistor connected to the power supply and has the following properties.

$$I_{D_m} = -I_{S_m} \tag{3.3}$$

$$I_{G_m} = I_{B_m} = 0 \tag{3.4}$$

Equations (3.4) assumes that there is no leakage current flowing through the substrate and gate. Therefore, zero-order quasi-static switching current has the following definitions in the cutoff, ohmic and saturation region for the nFET and pFET transistor in (3.5) and (3.6).

$$\begin{pmatrix} I_{Dm(off)} \\ I_{Dm(ohmic)} \\ I_{Dm(sat)} \end{pmatrix} = \begin{pmatrix} 0, & V_{GSN} < V_{Tn} \\ (a_n \cdot G \cdot V_{DSN})_m, & V_{GSN} > V_{Tn}, V_{DSN} < V_{DSsatn} \\ [G \cdot (V_{GSN} - V_{Tn})]_m, & V_{GSN} > V_{Tn}, V_{DSN} > V_{DSsatn} \end{pmatrix}, V_{DSsatn} = \frac{V_{GSN} - V_{Tn}}{a_n} \tag{3.5}$$

$$\begin{pmatrix} I_{Dm(off)} \\ I_{Dm}(ohmic) \\ I_{Dm}(sat) \end{pmatrix} = \begin{pmatrix} 0, & V_{GSP} > V_{Tp} \\ (a_p \cdot G \cdot V_{DSP})_m, & V_{GSP} < V_{Tp}, V_{DSP} > V_{DSsatp} \\ [G \cdot (V_{GSP} - V_{Tp})]_m, & V_{GSP} < V_{Tp}, V_{DSP} < V_{DSsatp} \end{pmatrix}, V_{DSsatp} = \frac{V_{GSP} - V_{Tp}}{a_p} \quad (3.6)$$

$$\begin{pmatrix} a_n \\ a_p \end{pmatrix} = \begin{pmatrix} \frac{G_{nohmic}}{G_{nSat}} \\ \frac{G_{pohmic}}{G_{pSat}} \end{pmatrix} \quad (3.7)$$

$(a_P \cdot G)_m$ is the conductance of the m-th pFET transistor in the ohmic region and the G_m is the trans-conductance of the m-th transistor in the saturation region. The sign of transistor current at the drain given by (3.5) and (3.6) is determined by the terminal voltages of the transistor. Current going into a terminal indicates a positive drain current and negative current if the current exits from the terminal. a_n, a_p, V_{Tn}, and V_{Tp} are process constants and process dependent variables. All parameters are positive except the threshold voltage V_{Tp}. a_n, a_p are greater than one. Conductance of the pFET and nFET transistor for G_{ohmic} and G_{sat} are determined from average sheet resistance extrapolated from I/V curves from the transistors used in the test circuits. The piece-wise linear model is a reasonably good approximation to current in saturation, and less accurate for current in the ohmic region as shown in Fig 3.3 and 3.4 when comparing the piecewise linear switching currents with SPICE simulation. However, as illustrated in [39], modeling errors in regions of low drain current usually produce smaller timing errors than errors in regions of high drain current. Therefore, the current mismatch errors in regions of low drain current is not critical for the timing accuracy of the piecewise linear transistor model. Furthermore, additional accuracy for the low drain current can be obtained by adding more piecewise linear regions to better approximate the transistor current in the

ohmic region, but adding more regions to the model makes solving for circuit dynamics more time-consuming because the node voltage must be checked at each moment in time to decide which piecewise linear model to use for each transistor in a circuit. The piecewise model is at least a more accurate switching current model than the traditional switched resistor model [13].

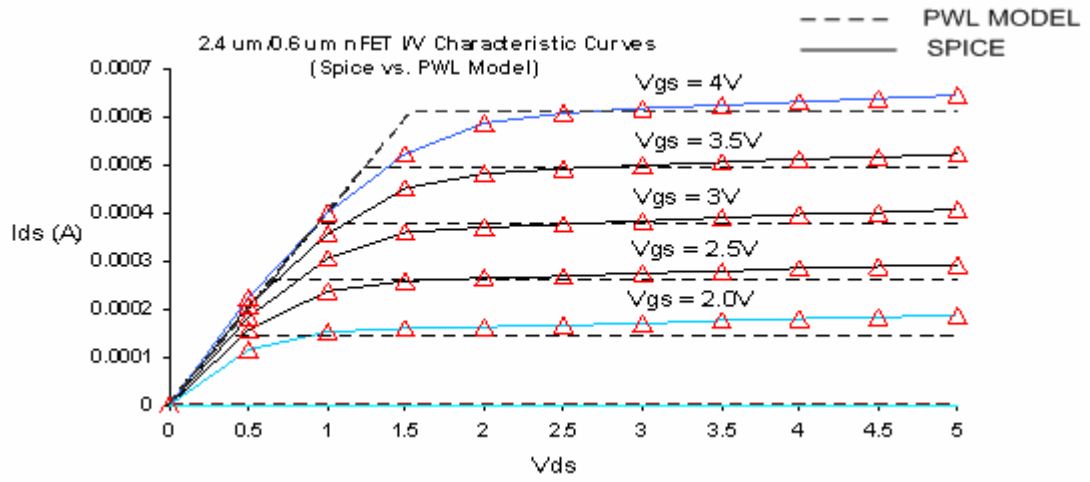

Figure 3.3 Accuracy of the piecewise linear switching current model for 2.4µm/0.6µm nFET

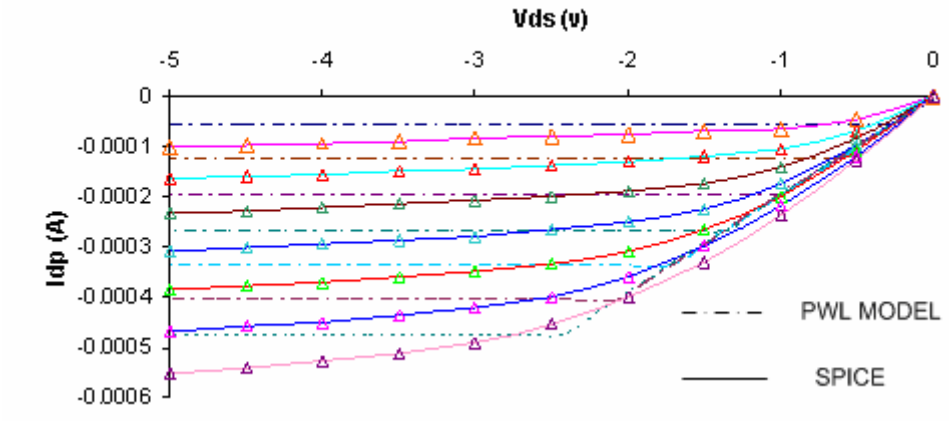

Figure 3.4 Accuracy of the piecewise linear switching current model for 4.8µm/0.6µm pFET

As illustrated in Figure 3.1, the averaged power dissipation is computed from the sum of the switching current of every pFET connected to the power supply. Figure 3.5 illustrates the sign convention for the zero-order quasi-static switching current component into the transistors. The first-order channel capacitive currents into the transistor(s) connected to the power supply are evaluated separately by the channel storage charge model presented in the following section.

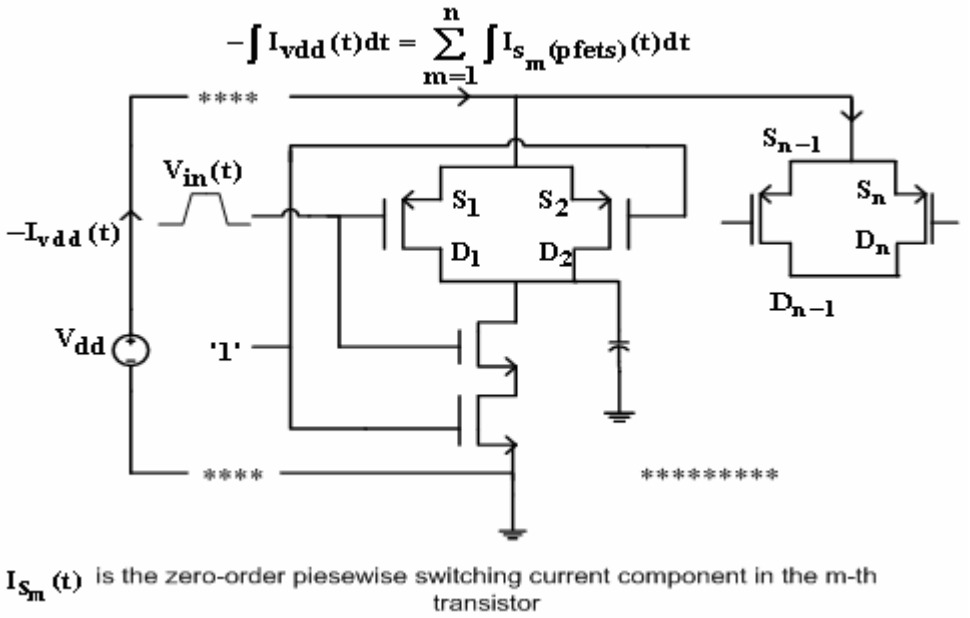

Figure 3.5 Sign convention for zero-order switching in transistors

3.1.2 Channel Storage Charge Model

Besides the zero-order quasi-static switching current in the transistor channel, channel currents also contain a first-order channel capacitive current, which come from the channel charge stored in the nonlinear parasitic capacitances. Channel capacitive currents are denoted as i_D, i_S, i_G, and i_B in order to differentiate from the zero-order quasi-static switching current for I_D, I_S, I_G, and I_B. Most transistor models [4] [5] [7] [26] are

not energy conserving due to the neglect of the first-order channel capacitive currents when calculating power consumption [37], and therefore, parasitic capacitances of the transistor are treated as normal capacitors, which do not dissipate power. Particularly, a SPICE simulator assumes that parasitic capacitors are normal capacitors in nature and do not include them in a power calculation [3]. In order to correct the problem by including the nonlinear channel capacitive currents in a power calculation, the channel storage charge is partitioned as seen in Figure 3.6 between the source and drain to obtain a simple lumped parameter model for the dynamic behavior of the transistor. Charge conservation requires that the total channel charge to be conserved, such that

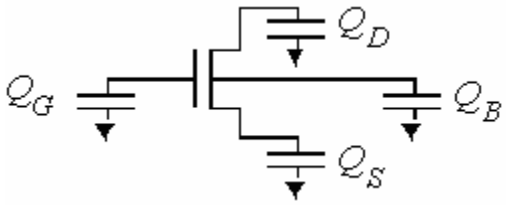

Figure 3.6 Channel storage charge model

$$Q_G = -(Q_S + Q_D + Q_B) \tag{3.8}$$

It should be emphasized that these are not linear capacitances since the charges are functions of all of the transistor terminal voltages. Channel capacitive currents can be written in terms of time derivatives of the channel storage charge on each transistor terminal. It is convenient to use these equations written in terms of the individual terminal voltages V_G, V_S, V_D, and V_B.

$$i_G = \frac{dQ_G}{dt} = C_{GG}\frac{dV_G}{dt} - C_{GS}\frac{dV_S}{dt} - C_{GD}\frac{dV_D}{dt} - C_{GB}\frac{dV_B}{dt} \tag{3.9}$$

$$i_S = \frac{dQ_S}{dt} = -C_{SG}\frac{dV_G}{dt} + C_{SS}\frac{dV_S}{dt} - C_{SD}\frac{dV_D}{dt} - C_{SB}\frac{dV_B}{dt} \tag{3.10}$$

$$i_D = \frac{dQ_D}{dt} = -C_{DG}\frac{dV_G}{dt} - C_{DS}\frac{dV_S}{dt} + C_{DD}\frac{dV_D}{dt} - C_{DB}\frac{dV_B}{dt} \tag{3.11}$$

$$i_B = -(i_G + i_S + i_D) \tag{3.12}$$

C_{ij} $(i \neq j)$ are all non-linear capacitors and functions of the terminal voltages given by

$$C_{ij} = \frac{\partial Q_i}{\partial V_{ij}} \quad i, j = G, D, S, B \tag{3.13}$$

where

$$C_{GG} = C_{GS} + C_{GD} + C_{GB} \tag{3.14}$$

$$C_{SS} = C_{SG} + C_{SD} + C_{SB} \tag{3.15}$$

$$C_{DD} = C_{DG} + C_{DS} + C_{DB} \tag{3.16}$$

The sign convention used for the first-order channel capacitive current (3.10) into the source terminal of transistor(s) connected to the power supply is shown in Figure 3.7.

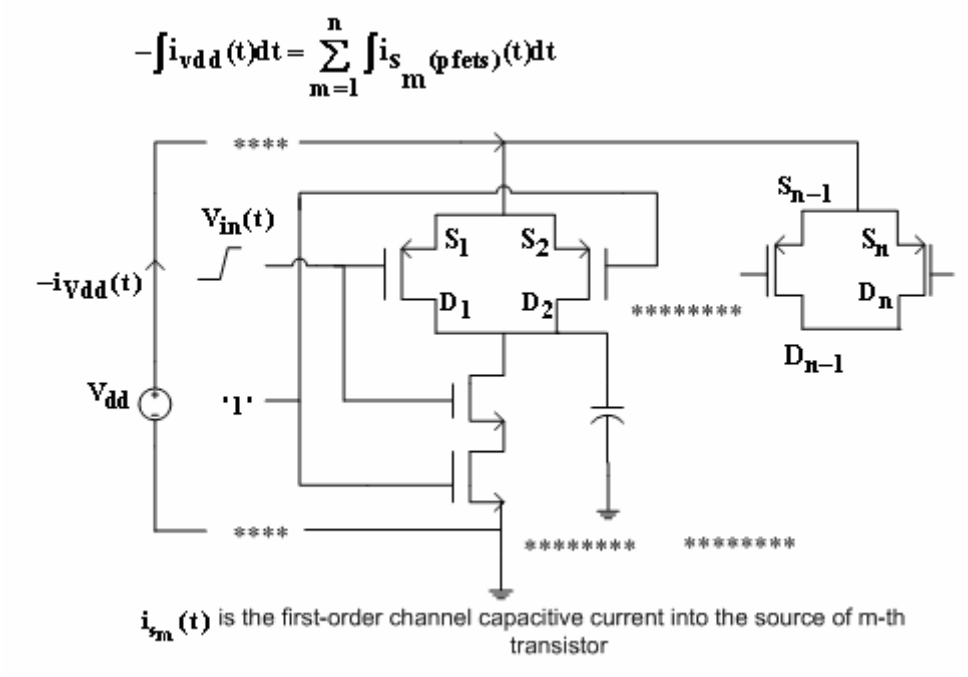

Figure 3.7 Sign convention for channel capacitive currents in transistors

In digital applications, the substrate terminal is biased at a constant voltage so that the last column in equations (3.9)-(3.11) can be ignored. Integration of the channel capacitive current equations gives the channel charge expressions (3.17)-(3.19), which make the evaluation of channel storage charge convenient for piecewise linear approximations of the first-order channel capacitive currents into each transistor terminal.

$$\Delta Q_G = C_{GG}\Delta V_G - C_{GS}\Delta V_S - C_{GD}\Delta V_D - C_{GB}\Delta V_B \tag{3.17}$$

$$\Delta Q_S = -C_{SG}\Delta V_G + C_{SS}\Delta V_S - C_{SD}\Delta V_D - C_{SB}\Delta V_B \tag{3.18}$$

$$\Delta Q_D = -C_{DG}\Delta V_G - C_{DS}\Delta V_S + C_{DD}\Delta V_D - C_{DB}\Delta V_B \tag{3.19}$$

The channel storage charge model (3.17)-(3.19) requires linearized capacitances in each linear region of operation in order to evaluate average power dissipated by parasitic capacitors. The following is a piece-wise linear approximation of the BSIM capacitance model.

Ohmic Region:

$$Q_{Gohm} = C_{ox}(V_{GS} - V_T) - (a_S + a_D)C_{ox}V_{DS} + b_{SB}C_{ox}(V_{SB} + V_T - V_{FB}) \tag{3.20.1}$$

$$-Q_{Sohm} = \frac{1}{2}C_{ox}(V_{GS} - V_T) - a_S C_{ox}V_{DS} \tag{3.20.2}$$

$$-Q_{Dohm} = \frac{1}{2}C_{ox}(V_{GS} - V_T) - a_D C_{ox}V_{DS} \tag{3.20.3}$$

Saturation Region:

$$Q_{Gsat} = b_{GS}C_{ox}(V_{GB} - V_{FB}) + b_{SB}C_{ox}(V_{SB} + V_T - V_{FB}) \tag{3.21.1}$$

$$-Q_{Ssat} = (1 - x_{part})b_{GS}C_{ox}(V_{GS} - V_T) \tag{3.21.2}$$

$$-Q_{Dsat} = x_{part}b_{GS}C_{ox}(V_{GS} - V_T) \tag{3.21.3}$$

Cutoff Region:

$$Q_{Goff} = b_{SB}C_{ox}(V_{GB} - V_{FB}) \tag{3.22.1}$$

$$-Q_{Soff} = 0 \tag{3.22.2}$$

$$-Q_{Doff} = 0 \tag{3.22.3}$$

Using continuity of charge at the ohmic-saturation boundary, we find

$$a_S = a(\frac{1}{2} - (1 - x_{part})b_{GS}) \tag{3.23}$$

Similarly,

$$a_D = a(\frac{1}{2} - x_{part}b_{GS}) \tag{3.24}$$

Using continuity of charge at the cutoff-saturation boundary, we find

$$Q_G = b_{SB}C_{ox}(V_{GB} - V_{FB}) = b_{GS}C_{ox}(V_{GS} - V_T) + b_{SB}C_{ox}(V_{SB} + V_T - V_{FB}) \tag{3.25}$$

is satisfied when $V_{GS} = V_T$, putting the values for a_S and a_D back into (3.20) gives

$$Q_{Gohm} = C_{ox}(V_{GS} - V_T) - a(1 - b_{GS})C_{ox}V_{DS} + b_{SB}C_{ox}(V_{SB} + V_T - V_{FB}) \tag{3.26.1}$$

$$-Q_{Sohm} = \frac{1}{2}C_{ox}(V_{GS} - V_T) - a(\frac{1}{2} - (1 - x_{part})b_{GS})C_{ox}V_{DS} \tag{3.26.2}$$

$$-Q_{Dohm} = \frac{1}{2}C_{ox}(V_{GS} - V_T) - a(\frac{1}{2} - x_{part}b_{GS})C_{ox}V_{DS} \tag{3.26.3}$$

The charge storage currents are:

$$i_{Goff} = \frac{dQ_{Goff}}{dt} = b_{SB}C_{ox}\frac{dV_G}{dt} \tag{3.27.1}$$

$$i_{Gohm} = C_{ox}\left[\frac{dV_G}{dt} - (1 - b_{SB} - a(1 - b_{SB})\frac{dV_S}{dt} - a(1 - b_{GS})\frac{dV_D}{dt}\right] \tag{3.27.2}$$

$$i_{Sohm} = C_{ox}\left[-\frac{1}{2}\frac{dV_G}{dt} + (\frac{1}{2} - a(\frac{1}{2} - (1 - x_{part})b_{GS}))\frac{dV_S}{dt} + a(\frac{1}{2} - (1 - x_{part})b_{GS})\frac{dV_D}{dt}\right] \tag{3.27.3}$$

$$i_{Dohm} = C_{ox}\left[-\frac{1}{2}\frac{dV_G}{dt} + (\frac{1}{2} - a(\frac{1}{2} - x_{part}b_{GS}))\frac{dV_S}{dt} + a(\frac{1}{2} - x_{part}b_{GS})\frac{dV_D}{dt}\right] \tag{3.27.4}$$

$$i_{Gsat} = b_{GS}C_{ox}\frac{dV_G}{dt} - (b_{GS} - b_{SB})C_{ox}\frac{dV_S}{dt} \tag{3.27.5}$$

$$i_{Ssat} = C_{ox}\left[-(1 - x_{part})b_{GS}\frac{dV_G}{dt} + (1 - x_{part})b_{GS}\frac{dV_S}{dt}\right] \tag{3.27.6}$$

$$i_{Dsat} = C_{ox}\left[-x_{part}b_{GS}\frac{dV_G}{dt} + x_{part}b_{GS}\frac{dV_S}{dt}\right] \tag{3.27.7}$$

Comparing the derivatives of (3.27) with (3.9)-(3.12) gives the following linearized results for the transistor capacitances.

Table 1 Linearized Parasitic Transistor Capacitances with Overlap Capacitance

	Cutoff	Ohmic	Saturation
C_{GG}	$b_{SB}C_{OX} + C_{GSO} + C_{GDO} + C_{GBO}$	$C_{OX} + C_{GBO}$	$b_{GS}C_{OX} + C_{GSO} + C_{GDO} + C_{GBO}$
C_{GS}	C_{GSO}	$(1 - b_{SB} - a(1 - b_{GS}))C_{OX} + C_{GSO}$	$(b_{GS} - b_{SB})C_{OX} + C_{GSO}$
C_{GD}	C_{GDO}	$(1 - b_{GS})aC_{ox} + C_{GDO}$	C_{GDO}
C_{SG}	C_{GSO}	$(1/2)C_{ox} + C_{GSO}$	$(1 - x_{part})b_{GS}C_{OX} + C_{GSO}$
C_{SS}	C_{GSO}	$(1/2 - a(1/2 - (1 - Xpart)b_{GS}))C_{OX} + C_{GSO}$	$(1 - x_{part})b_{GS}C_{OX} + C_{GSO}$
C_{SD}	0	$-a(1/2 - (1 - x_{part}b)b_{GS})C_{OX}$	0
C_{DG}	C_{GDO}	$(1/2)C_{ox} + C_{GDO}$	$x_{part}b_{GS}C_{OX} + C_{GDO}$
C_{DS}	0	$(-1/2 + a(1/2 - x_{part}b))C_{ox}$	$-X_{part}b_{GS}C_{OX}$
C_{DD}	C_{GDO}	$a(1/2 - X_{part}b_{GS})C_{OX} + C_{GDO}$	C_{GDO}

The gate to drain and gate to source overlap capacitances shown in Figure 3.8 are becoming more significant in submicron and deep submicron technologies, therefore gate overlap capacitances are included in the linearized capacitance model in Table 1. The gate to substrate overlap capacitance, C_{GBO}, is negligible in modern processes but is included for the sake of completeness. The BSIM model for the overlap capacitance is

$$C_{GSO} = WC_{gso} \tag{3.28}$$

which must be added to C_{GG}, C_{GS}, C_{SS}, and C_{SG} to the previous expression (3.27), so

$$C_{GDO} = WC_{gdo} \tag{3.29}$$

which must be added to C_{GG}, C_{GD}, C_{DD}, and C_{DG} to the previous expression (3.27), so

$$C_{GBO} = 2LC_{gbo} \tag{3.30}$$

which must be added to C_{GG} to the previous expression (3.27).

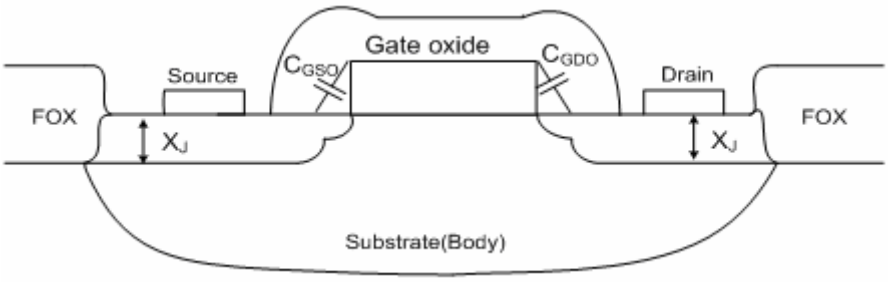

Figure 3.8 Gate overlap capacitances for FETs

With the linearized capacitance model, average power supply current into the parasitic capacitances can be evaluated by integrating the first-order channel capacitive currents into the transistor(s) connected to the power supply, which is usually the transistor source current(s). From the linearized capacitance model, it is essential to understand that the linearized capacitances are valid only within each piecewise linear region while the first-order channel capacitive current into the source node of the transistors is computed. Therefore, the initial and final terminal voltages in each piecewise linear region, associated with the transistor(s) connected to the power supply, must be computed before the average power dissipation can be evaluated. Approximate solutions for circuit dynamics has been used very successfully in predicting instantaneous

voltage waveforms [36], and the approximate solution for circuit voltage is extended beyond the gate delay predictions to compute the average power dissipated from the power supply with the piecewise linear switching current–voltage (I-V) model and capacitance–voltage (C-V) model.

3.2 Ramp Input Approximation

Rather than attempt an arbitrary input, the piecewise linear model assumes the input signal is a simple ramp with finite transition time as show in Figure 3.9.

$$V_{in}(t) = \begin{cases} V_{in}(t_{in0}) & t < t_{in0} \\ V_{in}(t_{in0}) + \dot{V}_{in}(t - t_{in0}) & t_{in0} < t < t_{in0} + t_{Tin} \\ V_{in}(t_{Tin}) & t > t_{in0} + t_{Tin} \end{cases} \tag{3.31}$$

where the slope of a ramp input is

$$\dot{V}_{in} = \frac{V_{in}(t_{in0} + t_{Tin}) - V_{in}(t_{in0})}{t_{Tin}} \tag{3.32}$$

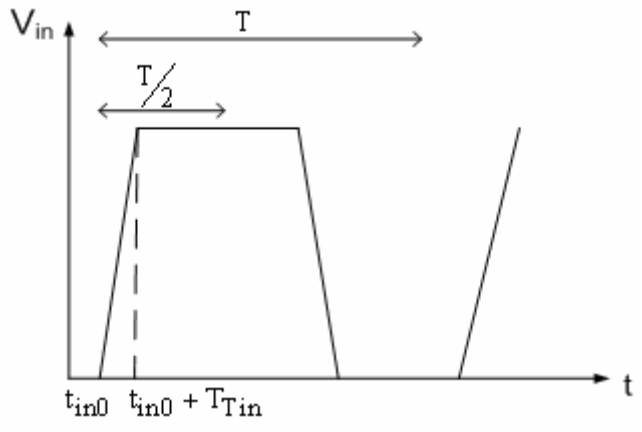

Figure 3.9 Input ramp approximations

Under Veendrick's assumption, the short-circuit power is proportional to the input rise and fall times and the load capacitance. Hence, it is essential to approximate the input

signal with a ramp approximation to evaluate short-circuit current induced power dissipation. Also, the simple ramp approximation includes the short-circuit current into the gate delay evaluation, which is essential to predict rise and fall time at any capacitive node [19] [36]. For a more general input approximation than the input expression of (3.31), the input to each resistance connected region is approximated as a series of piecewise linear segments as shown in Figure 3.10.

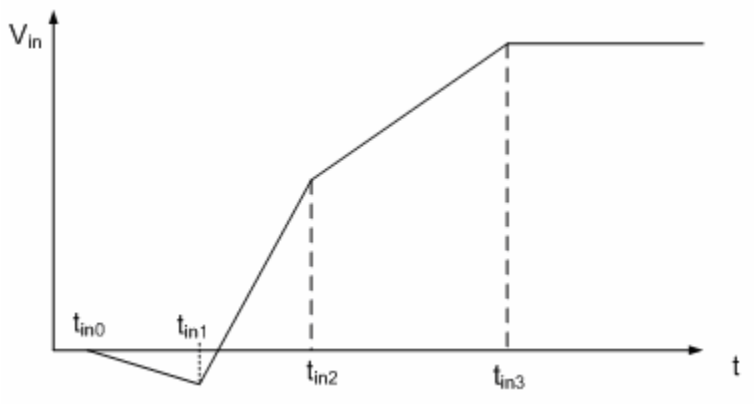

Figure 3.10 Piecewise linear approximation of input ramps in resistance connected regions

$$V_{in}(t) \approx \begin{cases} V_{in}(t_{in_0}) & t < t_{in_0} \\ V_{in}(t_{in_k}) + \dfrac{V_{in}(t_{in_{k+1}}) - V_{in}(t_{in_k})}{t_{in_{k+1}} - t_{in_k}}(t - t_{in_k}) & t_{in_k} < t < t_{in_k} + t_{in_{k+1}} \\ V_{in}(t_{in_{k\max}}) & t > t_{in_{k\max}} \end{cases}$$

(3.33)

$V_{in}(t_{in_k})$ is determined by approximating the input waveform at a finite number of times, t_{in_k}. The accuracy of the approximation increases with the number of time points. However, adding time points increases the amount of calculation necessary to

determine the voltages in the resistance connected region. First, we will find the approximate solution for circuit voltage with a ramp input (3.31).

3.3 Approximate Solution for Circuit Voltage

3.3.1 Resistive Connected Regions

A resistive connected region is defined as a set of circuit nodes connected by paths through the source or drain terminals of transistors in the ohmic region of operation. A resistive connected region can be described with a conductance matrix, **G**, when the zero-order switching current is calculated. **G** is a matrix for a resistive connected region and should not be confused with trans-conductance G_m for the m-th transistor. When the m-th transistor is in saturation, it is modeled as gate voltage controlled current source between the drain and source and has the effect of decoupling source and drain into separate resistive connected regions [36].

The steady state solution of circuit voltage in delay modeling encompasses non-singular **G** and singular **G** cases [36]. However, solving for the steady state solution of circuit voltage when the **G** matrix is singular can be avoided in computing average power dissipation, because the power supply current into the transistor(s) in saturation is determined by gate controlled current source, which is independent of drain-source bias. Thus, the approximate solution for circuit voltage at each drain node is considered only with a non-singular **G** matrix only for average power estimate.

Instead of solving for all circuit node voltages at once, the complexity of the circuit is reduced by approximating the solution in each resistive connected region connected to the power supply.

3.3.2 Approximate Solution for Circuit Voltage with Non-Singular **G** Matrix

It is assumed that the circuit of interest consists of transistors and capacitors only. The m-th transistor is connected to circuit nodes S_m, G_m, and D_m, and the c-th capacitor is connected to nodes A_C and B_C as shown in Figure 3.11.

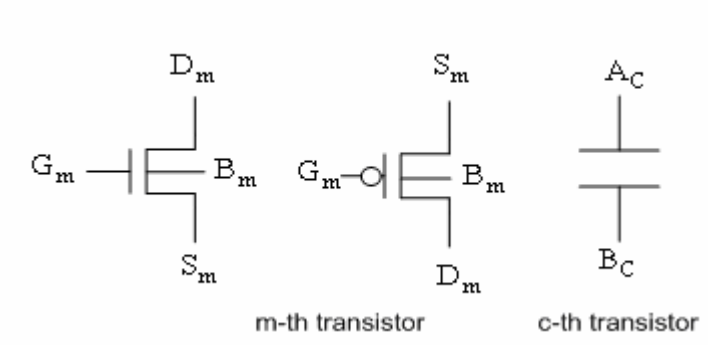

Figure 3.11 Notation for transistor number "m" and circuit node names

Large CMOS circuits can be partitioned into many resistively connected groups of nodes. Using the ramp approximation from equation (3.31) for the input nodes, the circuit dynamic equation can be generalized regardless of circuit topologies [36].

$$\mathbf{C}\frac{dV}{dt} + C_{in}\dot{V}_{in} + \mathbf{G}V + G_{in}(V_{in}(t_0) + \dot{V}_{in}(t - t_0)) + G_{Tn}V_{Tn} + G_{Tp}V_{Tp} + G_{dd}V_{dd} = 0 \qquad (3.34)$$

where **G** and **C** in bold letters represent two-dimensional matrices and C_{in}, G_{in}, G_{Tn}, G_{Tp}, and G_{dd} are column vectors. It helps to simplify the circuit dynamic equation if the column vectors $I_{in}(t_0)$ and $\dot{I}_{in}$ are defined as

$$I_{in}(t_0) = C_{in}\dot{V}_{in} + G_{in}V_{in}(t_0) + G_{Tn}V_{Tn} + G_{Tp}V_{Tp} + G_{dd}V_{dd} \qquad (3.35)$$

$$\dot{I}_{in} = G_{in}\dot{V}_{in} \qquad (3.36)$$

The circuit dynamic equation (3.34) can be re-written as

$$\mathbf{C}\frac{dV}{dt} + \mathbf{G}V + I_{in}(t_0) + \dot{I}_{in}(t - t_0) = 0 \tag{3.37}$$

where the **G** matrix is now the on-diagonal sub-block for a single resistance connected region and the **C** matrix is rectangular in general, and includes capacitive coupling from nodes inside the resistance connected to all other circuit nodes including those inside and outside the resistance connected region [36]. The steady state solution, $\tilde{V}$, after the exponential components die out has the form of equation (3.38).

$$\tilde{V}(t) = \tilde{V}(t_0) + \dot{\tilde{V}}(t - t_0) + \ddot{\tilde{V}}\frac{(t - t_0)^2}{2} \tag{3.38}$$

The steady state solution for a general circuit must satisfy the dynamic equation which can be written as

$$\mathbf{G}\tilde{V} = -\left[\mathbf{C}\frac{d\tilde{V}}{dt} + \dot{I}_{in} + I_{in}(t_0)\right] \tag{3.39}$$

Collecting terms of the same power of t, which leads to

$$\mathbf{G}\ddot{\tilde{V}} = 0 \tag{3.40}$$

$$\mathbf{G}\dot{\tilde{V}} = -(\mathbf{C}\ddot{\tilde{V}} + \dot{I}_{in}) \tag{3.41}$$

$$\mathbf{G}\tilde{V}(t_0) = -(\mathbf{C}\dot{\tilde{V}} + I_{in}(t_0)) \tag{3.42}$$

The conductance matrix **G** for the resistance connected region will be non-singular as long as the region includes the power or ground node. When **G** is non-singular, $\mathbf{G}^{-1}$ can be used to find

$$\ddot{\tilde{V}} = 0 \tag{3.43}$$

The equation (3.41) can be re-written as

$$\dot{\tilde{V}} = -\mathbf{G}^{-1} \cdot \dot{I}_{in} \tag{3.44}$$

$$\tilde{V}(t_0) = -\mathbf{G}^{-1}(\mathbf{C}\dot{\tilde{V}} + I_{in}(t_0)) \tag{3.45}$$

$\tilde{V}(t_0)$ can be re-written after substituting $\dot{\tilde{V}}$, such that

$$\tilde{V}(t_0) = \mathbf{G}^{-1}(\mathbf{C}\mathbf{G}^{-1}\dot{I}_{in} + I_{in}(t_0)) \tag{3.46}$$

G is a small dimension matrix describing a single resistance connected region, so that $\mathbf{G^{-1}}$ is not difficult to compute. It is possible to find a steady state solution in each resistance connected region knowing only the piecewise linear approximation(s) to V_{IN}. Thus, solving the circuit dynamic equation with a ramp input, the approximate voltage at each node D_m in a resistively connected region can be written as

$$V_{D_m}(t) = \tilde{V}_{D_m}(t) + [V_{D_m}(t_0) - \tilde{V}_{D_m}(t_0)] \cdot \exp(-\frac{t - t_0}{\tau_{D_m}}) \quad t > t_0 \tag{3.47}$$

The column vectors for the approximate voltages at each resistively connected node D_m are re-written as

$$\tilde{V}_{D_m}(t) = \tilde{V}_{D_m}(t_0) + \dot{\tilde{V}}_{D_m}(t - t_0) \tag{3.48}$$

$$\tilde{V}_{D_m}(t_0) = [\mathbf{G}^{-1}(\mathbf{C}\mathbf{G}^{-1}\dot{I}_{in} + I_{in}(t_0))]_{D_m} \tag{3.49}$$

$$\dot{\tilde{V}}_{D_m} = -[G^{-1} \cdot \dot{I}_{in}]_{D_m} \tag{3.50}$$

Therefore, the equation (3.48) is re-written as

$$\tilde{V}_{D_m}(t) = [\mathbf{G}^{-1}(\mathbf{C}\,\mathbf{G}^{-1}\dot{I}_{in} + I_{in}(t_0)) - \mathbf{G}^{-1}(\dot{I}_{in}(t - t_0))]_{D_m} \tag{3.51}$$

Unfortunately, **G** and **C** are not constant in general, but change as the switching transistors go into their various regions of operation. It is assumed that the solution beginning at t_0 does not "know" that it will become invalid later, but can be extended

indefinitely forward in time with a constant **G** and **C**. This allows the upper limit in the integrals to be extended to infinity when the average power is evaluated.

3.4 Average turn-off Energy Evaluation with the Zero-order Switching Current Model

In a CMOS circuit, average turn-off energy occurs due to short-circuit current flows during the time when the pFET and nFET network are on simultaneously. It is necessary to compute the power supply current into the source of every pFET for the time period when short-circuit current occurs. Average turn-off energy is evaluated from the sum of short-circuit currents in each piecewise linear region for any turning-off pFET connected to the power supply. Each turning-off transistor may cross through each region of operation, cutoff, ohmic, and saturation. Given the slope of the input waveform (or gate voltage $V_{G_m}(t)$) and the slope of the output waveform (or drain voltage $V_{D_m}(t)$) as functions of time from solving circuit dynamic equations, short-circuit current drawn from the power supply current into each transition can be approximated with the zero-order piecewise linear switching current, such that,

$$-\int_0^{\frac{T}{2}} I_{vdd(off)}dt = \sum_{m=1}^{n}\left[\int_{t_0}^{t_1} I_{S_m(ohmic)}dt + \int_{t_1}^{t_2} I_{S_m(sat)}dt + \int_{t_2}^{\frac{T}{2}} I_{S_m(off)}dt\right] \tag{3.52}$$

where t_0 is the time when the nFETs reach $V_{GSN} = V_{Tn}$, and the power supply current into the source of pFETs are proportional to each drain to source bias pf pFETs connected to the power supply. Average turn-off (short-circuit) energy is evaluated when the input has reached $V_{GSN} = V_{Tn}$, and pFETs are operated in the ohmic and saturation regions and is computed as

$$E_{I_{vdd(off)}} = V_{dd} \cdot \int_{t_0}^{\frac{T}{2}} -I_{vdd(off)} dt \qquad \text{for rising transitions} \tag{3.53}$$

where the subscript 'm' in (3.52) is the transistor number of turning-off transistor(s) connected to the power supply. Each term in (3.52) comes from each piecewise linear approximation to the zero-order quasi-static switching current into turn-off transistor(s) in ohmic, saturation, and cutoff regions which are evaluated individually in the following sections.

3.4.1 Zero-Order Turn-off Current in Ohmic Region:

The power supply current $I_{vdd}(t)$ going into the source of every turning-off transistor(s) in ohmic is the zero-order quasi-static current in ohmic region, and is computed as follows.

$$\begin{aligned}
&\left[\int_{t_0}^{t_1} I_{S_m(ohmic)} dt\right] = -\left[\int_{t_0}^{t_1} I_{D_m(ohmic)} dt\right] \\
&= -a_{P_m} G_m \left[\int_{t_0}^{t_1} V_{D_m S_m} dt\right] \\
&= -a_{P_m} G_m \left[\int_{t_0}^{t_1} \left(V_{D_m}(t) - V_{dd}\right) dt\right] \qquad t_1 > t_0 \\
&= -a_{P_m} G_m \int_{t_0}^{t_1} \left[\left(\tilde{V}_{D_m}(t) + [V_{D_m(t_0)} - \tilde{V}_{D_m(t_0)}] \cdot e^{-\frac{t-t_0}{\tau_{D_m}}}\right) - V_{dd}\right] dt
\end{aligned} \tag{3.54}$$

where $\tilde{V}_{D_m}(t)$ in (3.54) has a constant term and a time dependent term, so that the solution of equation (3.54) is written as

$$= a_{P_m} G_m \left[\left(e^{-\frac{t_1 - t_0}{\tau_{D_m}}} - 1 \right) \left(V_{D_{m(t_0)}} - \tilde{V}_{D_{m(t_0)}} \right) \tau_{D_m} + \left(t_1 - t_0 \right) \left(V_{dd} - \tilde{V}_{D_{m(t_0)}} - \frac{1}{2} \dot{\tilde{V}}_{D_m} (t_1 - t_0) \right) \right] \qquad t_1 > t_0 \qquad (3.55)$$

where $\tilde{V}_{D_m}(t_0)$ and $\dot{\tilde{V}}_{D_m}$ are defined in (3.49) and (3.50) and are the column vector for each resistively connected node in the linear ohmic region from the time period between t_0 and t_1. The delay time constant (τ_{D_m}) has a general form for a resistive connected node [36], which is written as follows.

$$\tau_{D_m} = \frac{[G^{-1} C \left| V(t_0) - \tilde{V}(t_0) \right|]_{D_m}}{\left| V_{D_m}(t_0) - \tilde{V}_{D_m}(t_0) \right|} \qquad (3.56)$$

3.4.2 Zero-Order Turn-off Current in saturation region

Before the transistor turns off completely, it may operate in saturation, and the power supply current $I_{vdd(t)}$ going into the source node of turning-off transistor(s) in saturation is the zero-order current in saturation, which is proportional to the gate voltage (or the slope of input waveform) and the zero-order current in saturation is computed as follows.

$$\left[\int_{t_1}^{t_2} I_{S_m(sat)}\,dt\right] = -\left[\int_{t_1}^{t_2} I_{D_m(sat)}\,dt\right]$$

$$= -G_m\left[\int_{t_1}^{t_2} V_{G_m} - V_{S_m} - V_{Tp_m}\,dt\right]$$

$$= -G_m\left[\int_{t_1}^{t_2}\left[\left(\frac{V_{dd}}{T_{Tin}}t - V_{dd}\right)\right] - V_{Tp_m}\;\;dt\right]$$

$$= G_m(t_2 - t_1)\left(\frac{-(t_2 + t_1)V_{dd}}{2\,T_{Tin}} + V_{dd} + V_{Tp_m}\right), \quad t_2 > t_1 \tag{3.57}$$

3.4.3 Zero-Order Turn-off Current in Cutoff Region

The power supply current into the source of transistor(s) in cutoff region is zero and is included for the sake of completeness.

$$\int_{t_2}^{T/2} I_{S_m(off)}\,dt = 0 \tag{3.58}$$

In the piecewise linear model, average power supply current for the zero-order component into the source of turn-off transistor(s) is zero after the input reaches a steady state value or the end of input transition time 'T_{Tin}'.

3.5 Average Turn-on Energy Evaluation with the Zero-order Piecewise Linear Current Model

The power supply current $I_{vdd}(t)$ into the source of turning-on pFET is the sum of the dynamic current for charging the load capacitance and the short-circuit current of turning-off nFETs. It is worth to mention that the average turn-off energy of nFETs is already included when the average turn-on energy of pFETs is evaluated directly from

the power supply current. It is one of the advantages of evaluating average power by computing power supply current instead of evaluating current and voltage for each turn-off transistor(s) individually. For arbitrary slopes of input and output waveforms at the drain and gate, and including all operation regions, the power supply current $I_{vdd}(t)$ into the source of turn-on pFETs in a resistive connected region can be formulated as,

$$-\int_{\frac{T}{2}}^{T} I_{Vdd}(on)\ dt = \sum_{m=1}^{n}\left[\int_{\frac{T}{2}}^{t_{si}} I_{S_m}(off)dt + \int_{t_{si}}^{t_3} I_{S_m}(Sat)dt + \int_{t_3}^{T} I_{S_m}(ohmic)dt\right] \tag{3.59}$$

where t_{si} is the time when an input signal ramps down to $V_{GSP} = V_{Tp}$ of transistor(s) connected to the power supply. As the input continues to ramp down, the pFETs go into saturation region from the time t_{si} to t_3, and so on until pFETs turns off after the input reaches the steady state "Low". Average turn-on energy during the input falling transition period is then computed as

$$E_{I_{vdd}(on)} = V_{dd} \cdot \int_{\frac{T}{2}}^{T} -I_{vdd}(on)\ dt \tag{3.60}$$

It is assumed that the solution beginning at $\frac{T}{2}$ and can be extended indefinitely forward in time with a constant G and C. This allows the upper limit in the integral to be extended to infinity.

The power supply current $I_{vdd}(t)$ going into each turn-on transistor in each piecewise linear operation can be computed as follows.

3.5.1 Zero-Order Turn-on Current in Cutoff Region

$$\int_{\frac{T}{2}}^{t_{si}} I_{S_m\,(off)}\,dt = 0 \tag{3.61}$$

3.5.2 Zero-order Turn-on Current in Saturation Region

The power supply current $I_{vdd}(t)$ going into the source of pFETs in saturation is a zero-order quasi-static current in saturation, and is computed as follows.

$$\int_{t_{si}}^{t_3} I_{S_m\,(sat)}\,dt = -\int_{t_{si}}^{t_3} I_{D_m\,(sat)}\,dt = -\int_{t_{si}}^{t_3} G_m\,(V_{G_m} - V_{S_m} - V_{Tp_m})\,dt$$

$$= -G_m\left[\int_{t_{si}}^{t_3}\left(V_{dd} - \frac{V_{dd}}{T_{Tin}}t\right) - V_{dd} - V_{Tp_m}\,dt\right]$$

$$= G_m\,(t_3 - t_{si})\left[\frac{(t_3 + t_{si})V_{dd}}{2\,T_{Tin}} + V_{T_{pm}}\right], \qquad t_3 > t_{si} \tag{3.62}$$

3.5.3 Zero-Order Turn-on Currents in Ohmic Region

In the ohmic region, the zero-order drain current or the source current of a transistor is independent of the gate voltage. Therefore, the zero-order turn-on currents from the power supply $I_{vdd}(t)$ into the sources of pFET are evaluated using the same equation as (3.55) regardless of rising or falling inputs, but with the sign changes in the $\dot{\tilde{V}}$ expression. In other words, the zero-order turn-on current is proportional to the approximate drain voltage of each pFET transistors connected to the power supply. Approximated voltage at each drain node depends on the column vectors $\dot{I}_{in}$ and $I_{in}(t_0)$ in each piecewise linear region from which a positive or a negative input slope ($\dot{V}_{in}$) is given.

3.5.4 Resistive Connected Region with Steady State Input

When the transistor is driven by a steady state input, the slope of input waveform or $\dot{V}_{in}$ is zero. The power supply current $I_{vdd}(t)$ going into the source of pFETs in ohmic and saturation regions with a steady state input has to be re-evaluated.

3.5.4.1 Zero-Order Turn-on Current in Saturation

When the driving input to the transistor(s) connected to the power supply is in the steady state of the input falling transitions, the zero-order turn-on current for transistor(s) in saturation is re-evaluated as follows.

$$\int_{t_{si}}^{t_3} I_{s_m(sat)} dt = -\int_{t_{si}}^{t_3} I_{D_m(sat)} dt \qquad t_3 > t_{si}$$

$$= -G_m \int_{t_{si}}^{t_3} (V_{G_m} - V_{dd} - V_{Tp_m})\, dt$$

where V_{G_m} has a $\dot{V}_{in}$ component equal to zero, which leads to the solution as

$$= G_m(t_3 - t_{si}) \cdot (V_{dd} + V_{Tp_m}) \tag{3.63}$$

3.5.4.2 Zero-Order Turn-on Current in Ohmic Region

With the input in steady state, the column vector $\dot{I}_{in}$ becomes

$$\dot{I}_{in} = G_{in} \dot{V}_{in} = 0 \tag{3.64}$$

And the steady state solution for circuit voltage in a resistive connected region has to be re-evaluated as follows [36].

$$\dot{\tilde{V}}_{Dm}(t - t_0) = -\mathbf{G}^{-1}(\mathbf{C}\,\ddot{\tilde{V}} + \dot{I}_{in}) = -G^{-1}\dot{I}_{in} = 0 \tag{3.65}$$

$$\tilde{V}_{Dm}(t) = \tilde{V}_{Dm}(t_0) + \dot{\tilde{V}}_{Dm}(t - t_0) = \tilde{V}_{Dm}(t_0) \tag{3.66}$$

The approximate solution for the circuit voltage at the drain node after the input is in the steady is re-written as follows.

$$V_{Dm}(t) = \tilde{V}_{Dm}(t_0) + [V_{Dm}(t_0) - \tilde{V}_{Dm}(t_0)] \cdot \exp(-\frac{t - t_0}{\tau_{Dm}}) \tag{3.67}$$

Where $\tilde{V}_{D_m}(t_0)$ is already defined by (3.49). Thus, zero-order turn-on current in the ohmic region is then re-written for input in steady state. Yet, the **G** and **C** matrices are not constant in general, but remain constant in the ohmic region, so that the solution for the approximate circuit voltage at the drain terminal can be extended forward in time with a constant **G** and **C** matrix in the ohmic region, which allows the integrals to be extended to a specific time boundary or to infinity in time as seen in equations (3.68) and (3.69).

$$\int_{t_3}^{T} I_{s_m(ohmic)} dt = -\int_{t_3}^{T} I_{D_m(ohmic)} dt$$

$$T > t_3$$

$$= -a_{P_m} G_m \int_{t_3}^{T} (V_{D_m}(t) - V_{dd})$$

$$= a_{P_m} G_m \left[-\tilde{V}_{D_{m(t_0)}} (T - t_3) + V_{dd} (T - t_3) + \left(e^{-\frac{T-t_3}{\tau_{D_m}}} - 1 \right) \left(V_{D_{m(t_3)}} - \tilde{V}_{D_{m(t_3)}} \right) \tau_{D_m} \right] \tag{3.68}$$

Here in (3.68), it can be proved that the quasi-static state voltage $\tilde{V}_{D_m}$ at the output node follows the steady state value V_{dd} as t_1 goes to infinity, so that the first two terms would cancel out. Thus, if an input reaches a steady state voltage, the boundary to the final region of operation of pFETs in the ohmic can be extended to infinity. Such that,

$$\int_{t_3}^{\infty} I_{s_m(ohmic)} dt = -\int_{t_3}^{\infty} I_{D_m(ohmic)} dt$$

$$= -a_{P_m} G_m \int_{t_0}^{\infty} (V_{D_m}(t) - V_{dd})$$

$$= a_{P_m} G_m \left[-t_3 V_{dd} - V_{D_{m(t_3)}} \tau_{D_m} + \tilde{V}_{D_{m(t_3)}} (t_3 + \tau_{D_m})\right]$$

$$= a_{P_m} G_m \left(V_{dd} - V_{D_{m(t_3)}}\right) \tau_{D_m} \tag{3.69}$$

3.6 Switching Energy in the Transistor Parasitic Capacitances

The parasitic capacitors from transistors connected directly to the power supply also contribute power dissipation, because dissipative current flows in the channels of the switching transistor(s) as channel charge is redistributed within the channel. Therefore, the switching current induced energy is evaluated by integrating over a cycle of channel capacitive currents into the source of every pFET connected to the power supply and is written as follows.

$$E_{i_{vdd}} = V_{dd} \cdot \int_{t_0}^{T} -i_{vdd}(t) = V_{dd} \cdot \sum_{m=1}^{n} \left[\int_{t_0}^{T/2} i_{s_m} + \int_{T/2}^{T} i_{s_m}\right] dt \tag{3.70}$$

where $E_{i_{vdd}}$ is the average switching energy drawn from the power supply current due to the nonlinear capacitive currents of the switching transistor(s) connected to the power supply. Lower case current ‘i’ is used to differentiate from “I” in zero-order quasi-static current when average turn-off and turn-on energy are evaluated. Expression from (3.70) is then evaluated in equation (3.71) and (3.72) individually which has the same integration boundaries of the zero-order switching energy evaluated in equations (3.52) and (3.59).

$$\sum_{m=1}^{n}\int_{t_0}^{T/2} i_{s_m}\,dt = \sum_{m=1}^{n}\left[\int_{t_0}^{t_1} i_{s_m(ohmic)}dt + \int_{t_1}^{t_2} i_{s_m(sat)}dt + \int_{t_2}^{T/2} i_{s_m(off)}dt\right] \tag{3.71}$$

$$\sum_{m=1}^{n}\int_{T/2}^{T} i_{s_m}\,dt = \sum_{m=1}^{n}\left[\int_{2/T}^{t_{si}} i_{s_m(off)}dt + \int_{t_{si}}^{t_3} i_{s_m(sat)}dt + \int_{t_3}^{T} i_{s_m(ohmic)}dt\right] \tag{3.72}$$

The average power supply current into the channel storage elements is the first-order current and is a piecewise linear approximation of channel capacitive currents of the transistor in the cutoff, ohmic, and saturation so that the integral can be computed with the same technique, knowing only the initial and final voltage at the drain of each pFET connected to the power supply. C_{SG_m}, C_{SS_m}, C_{SD_m}, and C_{SB_m} are the lumped capacitances in Table 1 associated with each transistor terminal in the m-th transistor(s) connected to the power supply. ΔV_{S_m} and ΔV_{B_m} are zero, because the source and body (substrate) voltages do not change for pFET that are directly connected to the power supply in digital CMOS circuit applications. Therefore, equation (3.71) and (3.72) are simplified to each component of integration individually as expressed in (3.73), (3.74), and (3.75).

$$\int_{t_0}^{t_1} i_{s_m(ohmic)}dt = \int_{t_0}^{t_1}\left(-C_{SG_m}\frac{dV_{G_m}}{dt} + C_{SS_m}\frac{dV_{S_m}}{dt} - C_{SD_m}\frac{dV_{D_m}}{dt} - C_{SB_m}\frac{dV_{B_m}}{dt}\right)_{ohmic} dt \tag{3.73}$$

$$= \left[-C_{SG_{m(ohmic)}}\cdot V_{G_m}\,|_{t_0}^{t_1} - C_{SD_{m(ohmic)}}\cdot V_{D_m}\,|_{t_0}^{t_1}\right]_{ohmic}$$

$$= -\left[C_{SG_{m(ohmic)}}\cdot\left(V_{G_{m(t_1)}} - V_{G_{m(t_0)}}\right)\right]_{ohmic} - \left[C_{SD_{m(ohmic)}}\cdot\left(V_{D_{m(t_1)}} - V_{D_{m(t_0)}}\right)\right]_{ohmic}$$

It should be noted that the lumped capacitors are not constant as the transistors switch from ohmic to saturation. Thus, the lumped terminal capacitors from the m-th transistor in (3.73) for ohmic region are different from the lumped terminal capacitors in (3.74) for

transistor in saturation as shown by the linearized lumped capacitors in Table 1. When pFET in saturation, the channel capacitive current is computed as

$$\int_{t_1}^{t_2} i_{s_m}(sat)dt = \int_{t_1}^{t_2} \left(-C_{SG_m} \frac{dV_{G_m}}{dt} + C_{SS_m} \frac{dV_{S_m}}{dt} - C_{SD_m} \frac{dV_{D_m}}{dt} - C_{SB_m} \frac{dV_{B_m}}{dt} \right)_{sat} dt \qquad (3.74)$$

$$= \left[-C_{SG_m(sat)} \cdot V_{G_m} \Big|_{t_1}^{t_2} - C_{SD_m(sat)} \cdot V_{D_m} \Big|_{t_1}^{t_2} \right]_{sat}$$

$$= \left[-C_{SG_m(sat)} \cdot \left(V_{G_m(t_2)} - V_{G_m(t_1)} \right) - C_{SD_m(sat)} \cdot \left(V_{D_m(t_2)} - V_{D_m(t_1)} \right) \right]_{sat}$$

Where C_{SG_m} and C_{SD_m} changes as transistors switch from ohmic to saturation. Similarly, in the cutoff region,

$$\int_{t_2}^{T/2} i_{s_m}(off)dt = \int_{t_2}^{T/2} \left(-C_{SG_m} \frac{dV_{G_m}}{dt} + C_{SS_m} \frac{dV_{S_m}}{dt} - C_{SD_m} \frac{dV_{D_m}}{dt} - C_{SB_m} \frac{dV_{B_m}}{dt} \right)_{off} dt \qquad (3.75)$$

$$= \left[-C_{SG_m(off)} \cdot V_{G_m} \Big|_{t_2}^{T/2} - C_{SD_m(off)} \cdot V_{D_m} \Big|_{t_2}^{T/2} \right]_{off}$$

$$= \left[-C_{SG_m(off)} \cdot \left(V_{G_m(T/2)} - V_{G_m(t_2)} \right) - C_{SD_m(off)} \cdot \left(V_{D_m(T/2)} - V_{D_m(t_2)} \right) \right]_{off}$$

(3.72) is evaluated using the same approach for the other half cycle. The computation to the channel capacitive current contributed to the energy dissipation is simplified to the calculation of the initial and final voltage at drain and gate for each piecewise linear region with the linearized capacitance model.

3.7 Summary

The piecewise linear transistor model consists of a zero-order switching current model and a channel storage charge model. The zero-order switching current model

evaluates the average power supply current at the time period when a CMOS circuit dissipates short-circuit current and dynamic current. Equation (3.56) and (3.70) are derived from the generalized circuit dynamic equation with the zero-order switching current model to predict the power supply current into the transistors connected to the power supply during the transistors in the ohmic region. When the transistors connected to the power supply are in saturation, the power supply current is proportional only to integral of the gate controlled current sources connected to the power supply which simplifies the computation because the current sources are independent of the drain voltages of the transistors in saturation. Total power supply current or total average power can be evaluated much quicker with the simplified solutions of the integrals of transistor switching transient currents to account for the short circuit current, dynamic current, and channel capacitive current into a total power calculation. In the following chapter, the power supply current into an inverter circuit driving different load capacitances will be evaluated, and the integral of each switching transient current and the solutions for each piecewise linear region will be used to obtain a total average power from the inverter driving different load capacitances.

CHAPTER 4

AVERAGE POWER ANALYSIS OF INVERTER WITH A PIECEWISE LINEAR MODEL

4.0 Introduction

A piecewise linear transistor model was introduced in the previous chapter. In this chapter, the piecewise linear model will be used to evaluate the average power dissipation of a simple inverter gate. The average power will be computed from the power supply current into the source of pFET of the inverter, which is the sum of zero-order quasi-static switching current and first-order channel capacitive currents. The model computes average power of inverter by integrating zero-order switching current and first-order channel capacitive currents over a switching cycle. The integration of each switching transient current is simplified to a solution compatible with the efficient piecewise linear delay model [36]. Average power evaluation by the model is compared with SPICE simulation of the same circuit over a wide range of input slopes, transistor sizes, and different capacitive loads.

4.1 Average Power Analysis of Inverter Driving Load Capacitance

An inverter has one drain node between the power supply and ground, so that the average turn-off (short circuit) energy, average turn-on energy, and switching energy

of the transistors parasitic capacitances are evaluated based on the approximate circuit voltages at the drain and gate of pFET in the inverter, and the input slope were approximated by an efficient piecewise linear delay model [36].

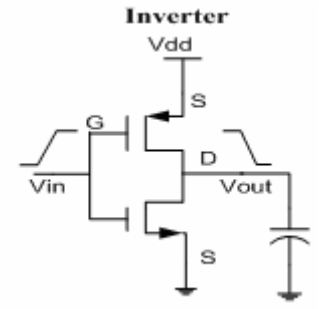

Figure 4.1 Inverter driving load capacitance with input ramp approximation

Using the ramp input approximation to the circuit dynamic equation of the inverter, Figure 4.2 is the graphical representation of piecewise linear approximation to the circuit voltages at the drain with transistors transitional boundaries and operation regions [36]. There are nine boundary lines and eight piecewise linear regions, which are derived from the piecewise linear switching current equations and the circuit dynamic equation for the inverter. It is necessary to define the terminals of the pFET, which is connected to the power supply, a driving input node, and drain node of inverter to facilitate average power calculation, so that we may write $V_{GSN} = V_{IN}$, $V_{DSN} = V_{OUT}$, $V_{GSP} = V_{IN} - V_{DD}$, and $V_{DSP} = V_{OUT} - V_{DD}$. Boundaries of each piecewise linear region as functions of time in ohmic, saturation, and cutoff (t_{si}, t_1, t_2, t_3, T_{Tin}), terminal voltages (V_{DS}, V_{GS}), and each piecewise linear regions ($R_0 \rightarrow R_8$) for the pFET and nFET in inverter are also shown in Figure 4.2.

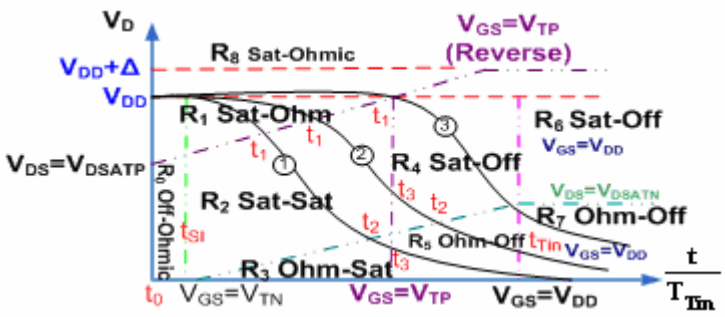

Figure 4.2 Inverter transient analysis with boundaries and operation regions with rising input ramp approximation

In Figure 4.2, a ramp input is assumed in the inverter for the first half cycle, and the output waveform is plotted against t/T_{Tin} from the closed form solution of the circuit dynamic equation (Eq. 3.37). Regions of operation in the inverter are denoted as "R_1 Sat-Ohm" which indicates region 1 with nFET in saturation and pFET in the ohmic region, and "$V_{GS} = V_{DD}$" on x-axis is the end of the input transition time "T_{Tin}". Fig. 4.4 uses the same definitions of the piecewise linear region in the cutoff, ohmic and saturation and the model parameters. It should be noted that a fast input ramp is equivalent to a short input transition time "T_{Tin}", so that curve 3 in Fig. 4.2 and Fig.4.4 is corresponding to a fast input ramp and curve 1 is the output waveform approximation of a slow input ramp [36].

4.1.1 Turn-off Energy Analysis

In an inverter gate, turn-off (short-circuit) energy is evaluated from the pFET transistor, connected to the power supply, when it turns off. Turn-off energy is proportional to the input transition time on the gate and the zero-order switching off current of pFET provided from the power supply during input (0→1) transition during the load capacitance discharge cycle. Turn-off energy is then evaluated by integrating the zero-order switching off current provided by the power supply into the source of pFET

from the time period when it is on to off. If an input is a slow rising input ramp, the voltage waveform at drain node as shown in waveform *1* (Figure 4.2) is a possible solution. Then, given the input slope and the output waveform, the zero-order current into the source of the turning off pFET is evaluated from the sum of pFET current from its on (ohmic) state to off state across the ohmic region from initial time t_0 to t_1 and across saturation region from t_1 to t_2 respectively, which is written according to the integration of the zero-order switching current in each respective operating region in equation (3.52).

$$E_{I_{vdd(off)}} = V_{dd}\int_{t_0}^{\frac{T}{2}} -I_{vdd(off)}dt = V_{dd}\left[\int_{t_0}^{t_1} I_{sm(ohmic)}dt + \int_{t_1}^{t_2} I_{sm(sat)}dt + \int_{t_2}^{\frac{T}{2}} I_{sm(off)}dt\right]$$

$$= V_{dd}\left\{a_{P_m} G_m\left[\left(e^{-\frac{t_1-t_0}{\tau_{D_m}}}-1\right)\left(V_{D_{m(t_0)}} - \tilde{V}_{D_{m(t_0)}}\right)\tau_{D_m} + \left(t_1-t_0\right)\left(V_{dd} - \tilde{V}_{D_{m(t_0)}} - \frac{1}{2}\dot{\tilde{V}}_{D_m}(t_1-t_0)\right)\right] + G_m(t_2-t_1)\left(\frac{-(t_2+t_1)V_{dd}}{2\,T_{Tin}} + V_{dd} + V_{Tp_m}\right)\right\}$$

Where $t_1 > t_0$ and $t_2 > t_1$ (4.1)

When the input is a fast ramp, the pFET may turn off before it goes into saturation region. The slope of the voltage waveform at the drain node shown in the waveform 3 (Figure 4.2) is a possible solution, such that the short-circuit energy drawn from the power supply is re-evaluated for ohmic region only as in equation (4.2).

$$E_{I_{vdd(off)}} = V_{dd}\int_{t_0}^{\frac{T}{2}} -I_{vdd(off)}dt = V_{dd}\left[\int_{t_0}^{t_2} I_{sm(ohmic)}dt + \int_{t_2}^{\frac{T}{2}} I_{sm(off)}dt\right] \quad t_2 > t_0 \quad (4.2)$$

$$= V_{dd}\left\{a_{P_m} G_m\left[\left(e^{-\frac{t_2-t_0}{\tau_{D_m}}}-1\right)\left(V_{D_{m(t_0)}} - \tilde{V}_{D_{m(t_0)}}\right)\tau_{D_m} + \left(t_2-t_0\right)\left(V_{dd} - \tilde{V}_{D_{m(t_0)}} - \frac{1}{2}\dot{\tilde{V}}_{D_m}(t_2-t_0)\right)\right]\right\}$$

It should be noted that turn-off energy is evaluated only when the input is rising or the transistor(s) connected to the power supply turns off.

4.1.2 Turn-on Energy Analysis

Turn-on energy is evaluated during input (1→0) transition when the pFET of the inverter, connected to the power supply, turns on and conducting the zero-order switching current during the load capacitance charging cycle. The power supply current is the sum of the zero-order switching currents for charging the load capacitance and the short-circuit current of turning-off nFET. Resembling turn-off energy evaluation, output waveform approximation in Figure 4.4 is derived to compute turn-on energy.

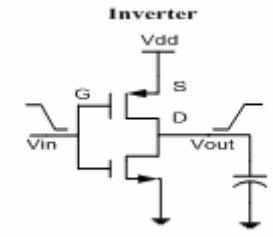

Figure 4.3 Inverter driving load capacitance with input falling ramp approximation

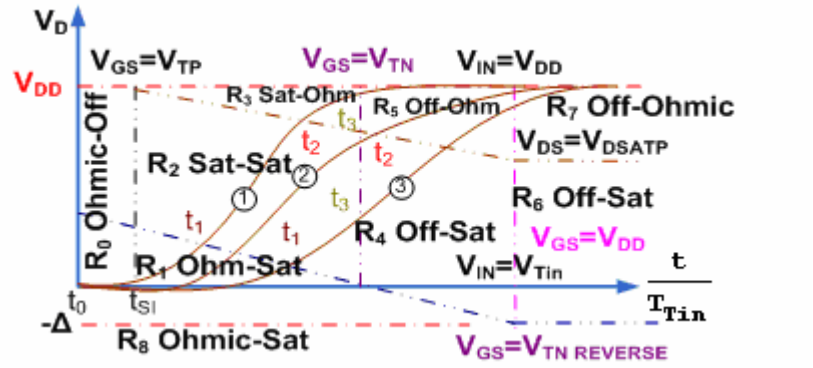

Figure 4.4 Inverter transient analysis with boundaries and operation regions with input falling ramp approximation

Turn-on energy is computed from the sum of zero-order switching current of pFETs connected to the power supply and the short circuit current of turning-off nFET connected with pFETs. It should be noted that short-circuit current of nFET is drawn

from the power supply current from the channel of turning-on pFET. Therefore, evaluation of turn-on energy is simplified to the calculation of total current into pFETs only. Equation (4.3) shows the turn-on energy evaluated from the current of pFETs connected to the power supply during pFETs turning-on period.

$$E_{I_{vdd(on)}} = V_{dd}\int_{\frac{T}{2}}^{T} -I_{vdd\,(on)}dt = V_{dd}\left[\int_{\frac{T}{2}}^{t_{si}} I_{S_m\,(off)}dt + \int_{t_{si}}^{t_3} I_{S_m\,(sat)}dt + \int_{t_3}^{T} I_{S_m\,(ohmic)}dt\right]$$

$$= V_{dd}\left\{G_m\,(t_3 - t_{si})\left[\frac{(t_3 + t_{si})V_{dd}}{2\,T_{Tin}} + V_{T_{Pm}}\right] + a_{P_m}G_m\left[-\tilde{V}_{D_{m(t_0)}}\left(T - t_3\right) + V_{dd}\left(T - t_3\right) + \left(e^{-\frac{T-t_3}{\tau_{D_m}}} - 1\right)\left(V_{D_{m(t_3)}} - \tilde{V}_{D_{m(t_3)}}\right)\tau_{D_m}\right]\right\}$$

Where $t_3 > t_{si}$ and $T > t_3$ (4.3)

4.1.3 Switching Energy in the Transistor Parasitic Capacitances

The power supply current into the parasitic capacitances of pFET, connected to the power supply, is the first-order channel capacitive currents in the transistors. Switching power of the parasitic capacitances is evaluated by integrating the first-order channel capacitive currents over a switching cycle to measure if the channel capacitive currents draw energy from the power supply. Equation (3.70) can be re-written for a simple inverter gate, such that switching energy of the parasitic capacitances of the pFET can be computes as

$$E_{i_{vdd}} = V_{dd}\cdot\int_{t_0}^{T} -i_{vdd}(t) = V_{dd}\cdot\left[\int_{t_0}^{T/2} i_{s_m} + \int_{T/2}^{T} i_{s_m}\right]dt$$

$$= V_{dd}\left[\int_{t_0}^{t_1} i_{s_m(ohmic)}dt + \int_{t_1}^{t_2} i_{s_m(sat)}dt + \int_{t_2}^{T/2} i_{s_m(off)}dt + \int_{2/T}^{t_{si}} i_{s_m(off)}dt + \int_{t_{si}}^{t_3} i_{s_m(sat)}dt + \int_{t_3}^{T} i_{s_m(ohmic)}dt\right]$$

$$
\begin{aligned}
= V_{dd}\ \{ & -\left[C_{SG_m(ohmic)} \cdot \left(V_{G_m(t_1)} - V_{G_m(t_0)} \right) \right]_{ohmic} - \left[C_{SD_m(ohmic)} \cdot \left(V_{D_m(t_1)} - V_{D_m(t_0)} \right) \right]_{ohmic} - \\
& \left[C_{SG_m(sat)} \cdot \left(V_{G_m(t_2)} - V_{G_m(t_1)} \right) \right]_{sat} - \left[C_{SD_m(sat)} \cdot \left(V_{D_m(t_2)} - V_{D_m(t_1)} \right) \right]_{sat} - \\
& \left[C_{SG_m(sat)} \cdot \left(V_{G_m(t_3)} - V_{G_m(t_{si})} \right) \right]_{sat} - \left[C_{SD_m(sat)} \cdot \left(V_{D_m(t_3)} - V_{D_m(t_{si})} \right) \right]_{sat} - \\
& \left[C_{SG_m(ohmic)} \cdot \left(V_{G_m(T)} - V_{G_m(t_3)} \right) \right]_{ohmic} - \left[C_{SD_m(ohmic)} \cdot \left(V_{D_m(T)} - V_{D_m(t_3)} \right) \right]_{ohmic} \}
\end{aligned}
\tag{4.4}
$$

Where the lumped capacitors C_{SG_m} and C_{SD_m} in ohmic region are different from C_{SG_m} and C_{SD_m} in saturation as shown in Table 1. The simplified form in (4.4) allows a direct evaluation to the channel capacitive currents knowing only the initial and final voltage at drain and gate terminal with the linearized channel capacitances model.

4.2 Energy per cycle Calculation

Total energy dissipation in the inverter is computed from the sum of turn-off energy, turn-on energy, and switching energy of parasitic capacitors of transistors connected to the power supply. Average power in (4.5), approximated by the piecewise linear model for a CMOS circuit, is equivalent to energy per cycle. Therefore, energy per cycle is used interchangeably with the average power.

$$
P_{avg} = \frac{1}{T} \cdot \left(E_{I_{vdd}(off)} + E_{I_{vdd}(on)} + E_{i_{vdd}} \right) \tag{4.5}
$$

4.2.1 Energy Per Cycle Evaluation by the Model

Table 2 is an example of computing energy per cycle from the power supply for the inverter in Figure 4.5. Energy per cycle simulation of the inverter was calculated by the program in appendix III. The program computes the energy of the power supply

current from the sum of piecewise linear transistor current across each operating region for a complete cycle. Turn-off energy is denoted as $E_{Ivdd(off)}$, and Turn-on energy is denoted as $E_{Ivdd(on)}$, and switching energy of the parasitic capacitances is denoted as E_{ivdd}. Sum of turn-off energy, turn-on energy, and switching energy of parasitic capacitors is the average power.

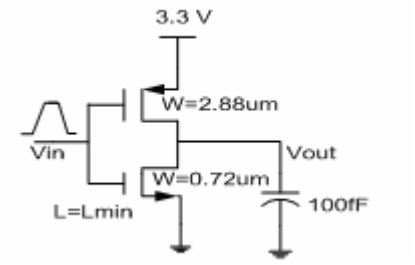

Figure 4.5 Energy per cycle calculation of inverter by the model with TSMC 0.18μm process

T_{Tin} (Picosec.) Input Transition	$E_{Ivdd(off)}$ (0→1)	$E_{Ivdd(on)}$ (1→0)	E_{ivdd} (0→1)	E_{ivdd} (1→0)	∑ E (Energy per cycle predicted by Model)
1000	5.00E-13	1.34E-12	-4.57E-14	2.66E-14	**1.821E-12**
900	4.37E-13	1.32E-12	-4.57E-14	2.66E-14	**1.741E-12**
800	3.76E-13	1.31E-12	-4.57E-14	2.66E-14	**1.662E-12**
700	3.15E-13	1.29E-12	-4.57E-14	2.66E-14	**1.583E-12**
600	2.54E-13	1.27E-12	-4.57E-14	2.66E-14	**1.506E-12**
500	1.96E-13	1.25E-12	-4.57E-14	2.66E-14	**1.431E-12**
450	1.67E-13	1.25E-12	-4.57E-14	2.66E-14	**1.395E-12**
400	1.39E-13	1.24E-12	-4.57E-14	2.66E-14	**1.360E-12**
350	1.12E-13	1.23E-12	-4.57E-14	2.66E-14	**1.327E-12**
300	8.63E-14	1.23E-12	-4.57E-14	2.66E-14	**1.294E-12**
250	6.21E-14	1.22E-12	-4.57E-14	2.66E-14	**1.264E-12**
200	4.02E-14	1.22E-12	-4.57E-14	2.66E-14	**1.237E-12**
150	2.13E-14	1.21E-12	-4.57E-14	2.66E-14	**1.213E-12**
130	1.48E-14	1.21E-12	-4.57E-14	2.66E-14	**1.205E-12**
110	9.24E-15	1.21E-12	-4.57E-14	2.66E-14	**1.198E-12**
100	6.78E-15	1.21E-12	-4.57E-14	2.66E-14	**1.195E-12**
90	4.59E-15	1.21E-12	-4.57E-14	2.66E-14	**1.192E-12**

Table 2 Energy per cycle simulation of inverter in Fig.4.5 using PWL model for various input transition time $\mathbf{T_{Tin}}$ from 1000ps to 20ps

4.2.2 Energy per cycle simulation in SPICE

In SPICE, energy per cycle of a circuit can be simulated from the power supply or the transistor devices in the circuit. In Table 3, the SPICE shows an inconsistency of energy per cycle evaluated from the power supply and devices in the same circuit. Since the BSIM3v3 is a charge-conserving transistor model, the average power supply current from the power supply in SPICE is used as a reference to confirm the model's accuracy.

$T_{Tin(Picosec.)}$	Simulated energy per cycle from inverter transistors	Simulated energy per cycle from inverter power supply	Energy per cycle predicted by Model
1000	1.914e-12	1.895e-12	1.821E-12
900	1.822e-12	1.803e-12	1.741E-12
800	1.734e-12	1.712e-12	1.662E-12
700	1.647e-12	1.623e-12	1.583E-12
600	1.563e-12	1.537e-12	1.506E-12
500	1.482e-12	1.455e-12	1.431E-12
450	1.444e-12	1.416e-12	1.395E-12
400	1.408e-12	1.377e-12	1.360E-12
350	1.373e-12	1.341e-12	1.327E-12
300	1.340e-12	1.306e-12	1.294E-12
250	1.309e-12	1.274e-12	1.264E-12
200	1.281e-12	1.245e-12	1.237E-12
150	1.258e-12	1.220e-12	1.213E-12
130	1.250e-12	1.211e-12	1.205E-12
110	1.243e-12	1.204e-12	1.198E-12
100	1.240e-12	1.200e-12	1.195E-12
90	1.238e-12	1.197e-12	1.192E-12

Table 3 Comparisons of energy per cycle predictions in SPICE and PWL model for the inverter in Fig.4.5

4.3 Model Accuracy of An Inverter Driving Load Capacitance

An inverter driving different load capacitances is used to test for the accuracy of piecewise linear model for the average power evaluation. The model accuracy is measured with reference to the SPICE energy per cycle simulation from the power supply

in a standard 0.5μm process and a deep submicron 0.18μm process. The first circuit is the inverter driving a100 *fF* load capacitance, and the second circuit is the inverter driving inverter load. There are two reasons of choosing a large output capacitor and a small capacitive load. First, the large load capacitance has much larger impact on the transistor zero-order switching current than the channel storage charge in the channel, so that the zero-order switching current model can be measured for its accuracy in predicting the turn-off (short circuit) power and average turn-on power. Also, the accuracy of the model parameters for the zero-order switching current can be justified while the effect of the channel capacitances is not included. However, adjusting the model parameters only for the short-circuit current as predicted in the SPICE would also affect the model accuracy to evaluate the turn-on energy. Therefore, the model parameters are not optimized for the individual zero-order and first-order switching currents, but the model parameters are averaged to evaluate an average switching transient currents drawn from the power supply.

4.3.1 Model Accuracy in AMI CMOS 0.5μm Process (L_{min} = 0.6μm)

K is a ratio of pFET transistor width to nFET transistor width. K has 1, 2, and 4 for different inverter transistor ratio. Figure 4.6, 4.7, and 4.8 is the energy per cycle simulation predicted by the model in comparisons with the SPICE.

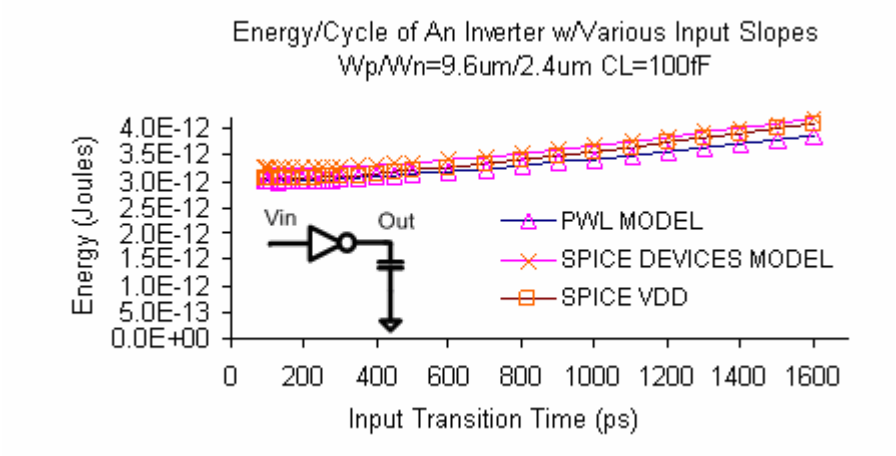

Figure 4.6 Accuracy of the PWL model in inverter gate (K = 4) driving 100fF load

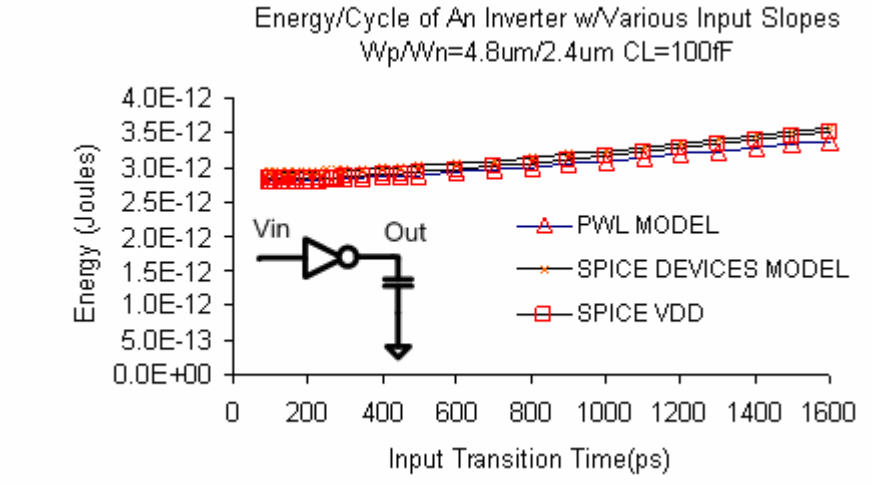

Figure 4.7 Accuracy of the PWL model in inverter gate (K = 2) driving 100fF load

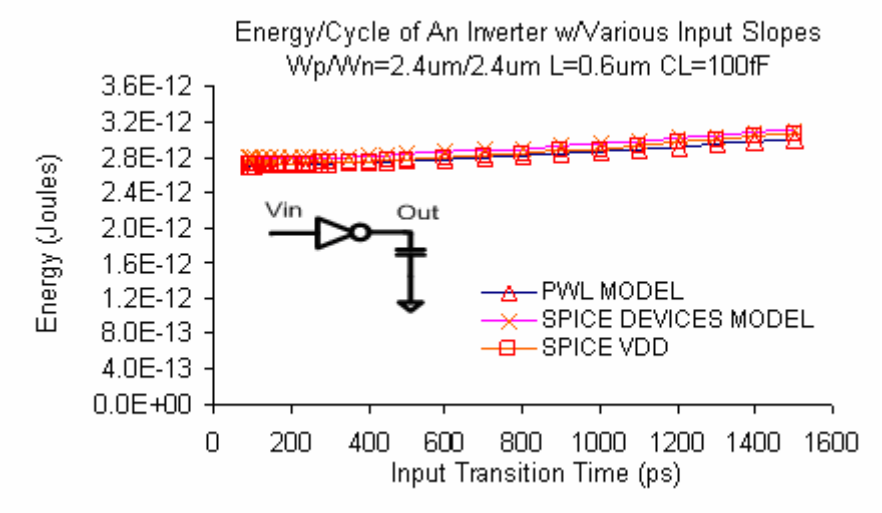

Figure 4.8 Accuracy of the PWL model in inverter gate (K = 1) driving 100fF load

4.3.2 Model Accuracy in TSMC CMOS 0.18µm Process (L_{min} = 0.18µm)

Testing the accuracy and validity of the model in different CMOS process is to confirm the portability of the piecewise linear model. Accuracies of the piecewise linear model shows the excellent agreements in high frequencies with the SPICE's predictions in TSMC 0.18µm process while a different set of model parameters for TSMC 0.18µm process are used.

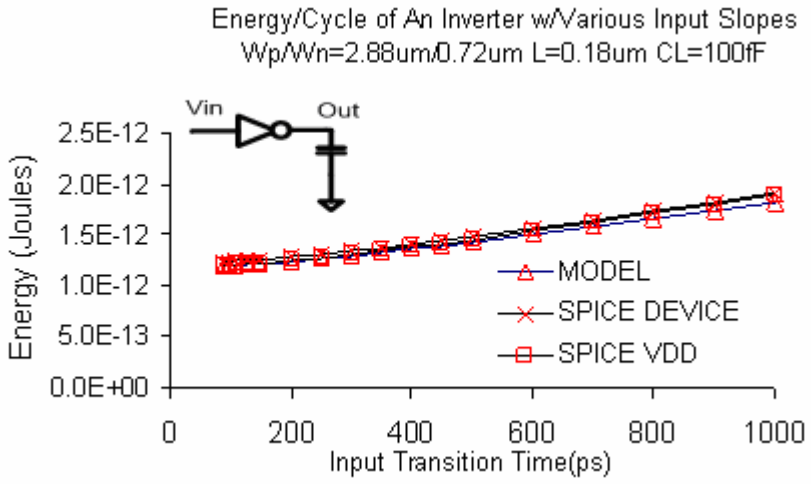

Figure 4.9 Accuracy of the PWL model in inverter gate (K = 4) driving 100fF load

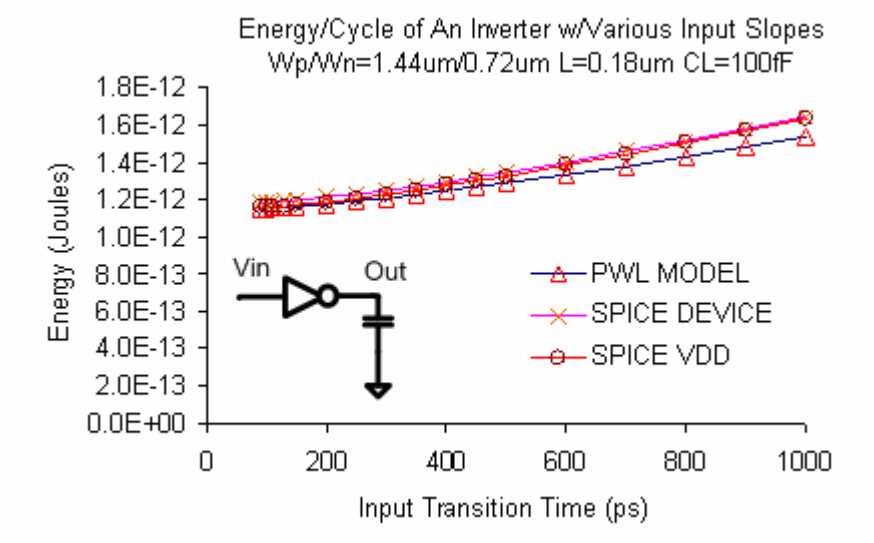

Figure 4.10 Accuracy of the PWL model in inverter gate (K = 2) driving 100fF load

The piecewise linear model shows that average power prediction for large input transitions at low switching frequencies is less accurate than small transition time in the high frequencies. The results indicate that the short-circuit current is dominant and underestimated for slow inputs. Inaccuracy of the piecewise linear model for slow inputs is two-folds. First, the zero-order switching current underestimates the current waveform predicted by SPICE due to an approximated transistor current model less accurate in ohmic region than the current predicted by the SPICE. Second, the conductance and transconductance is chosen to match the I-V characteristics of the SPICE BSIM3v3 model in a region of large current and a region of small current, thus, the accuracies of the average power predictions in some circuit topologies may be better than the others for the same input slopes. However, overall accuracy for slow inputs is fairly well controlled within 10% error of SPICE in average for all circuits under tests.

4.4 Model Accuracy of Inverter Driving Inverter Gate Load

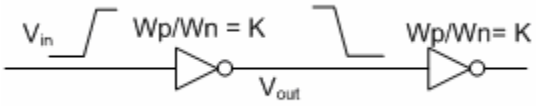

Figure 4.11 Inverter driving gate load

Load capacitance is not the dominant factor any more since the inverter gate capacitance is comparable to the driver inverter size. The channel capacitive current from the parasitic capacitances is comparable to the zero-order switching current drawn from the power supply current when the inverter driving a small load, and now the channel capacitive current has more impacts on the average power than previous case for the inverter driving large capacitance load.

4.4.1 Model Accuracy in AMI CMOS 0.5µm Process (L_{min} = 0.6µm)

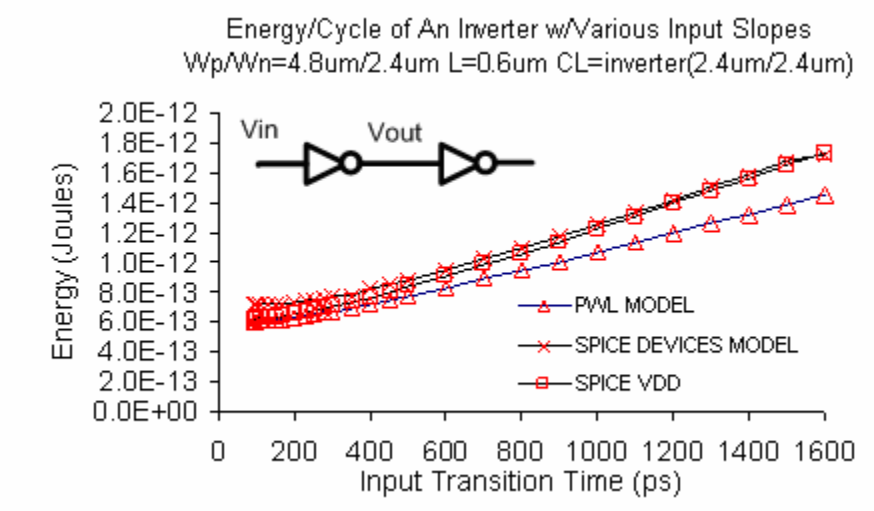

Figure 4.12 Accuracy of the PWL model in inverter gate K = 2 driving inverter load (W_P/W_n=2.4µm/2.4µm L=0.6µm)

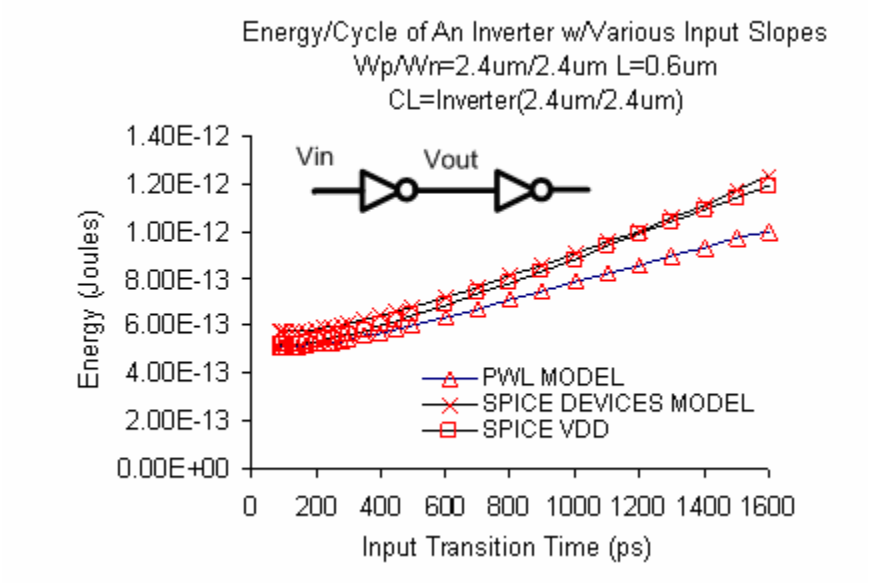

Figure 4.13 Accuracy of the PWL model in inverter gate K=1 driving inverter load (W_P/W_n=2.4µm/2.4µm L=0.6µm)

4.4.2 Model Accuracy in TSMC CMOS 0.18µm Process (L_{min} = 0.18µm)

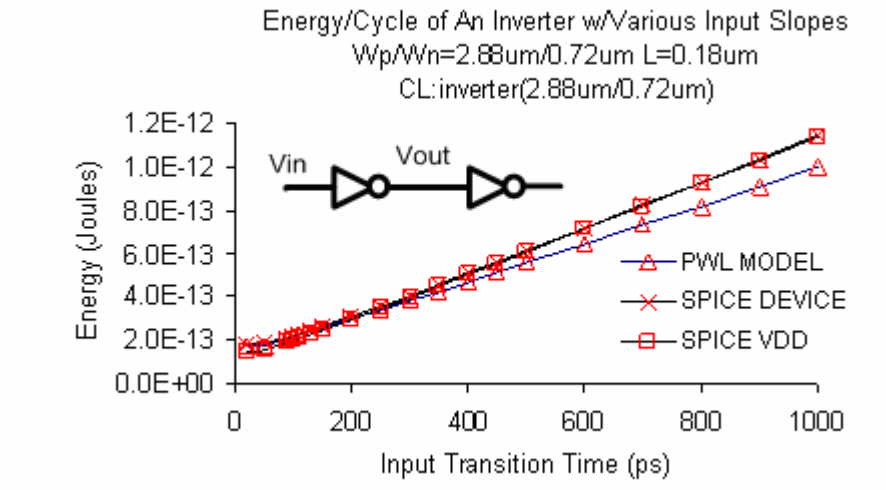

Figure 4.14 Accuracy of the PWL model in inverter gate driving inverter load (K = 4)

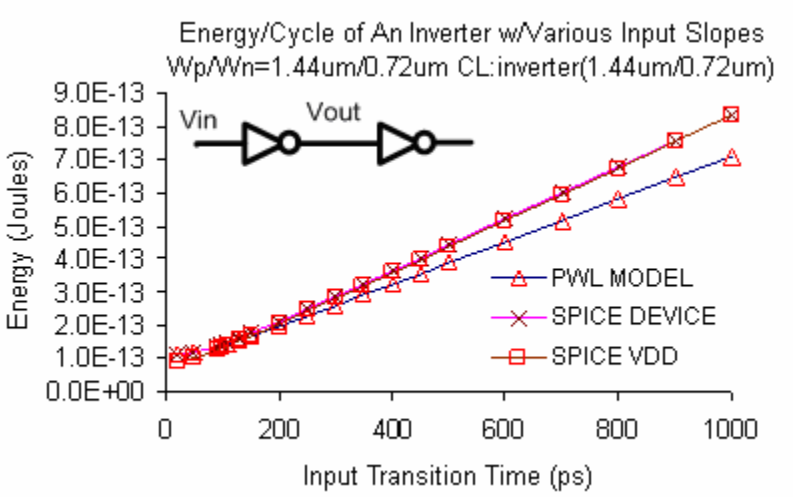

Figure 4.15 Accuracy of the PWL model in inverter gate driving inverter load (K = 2)

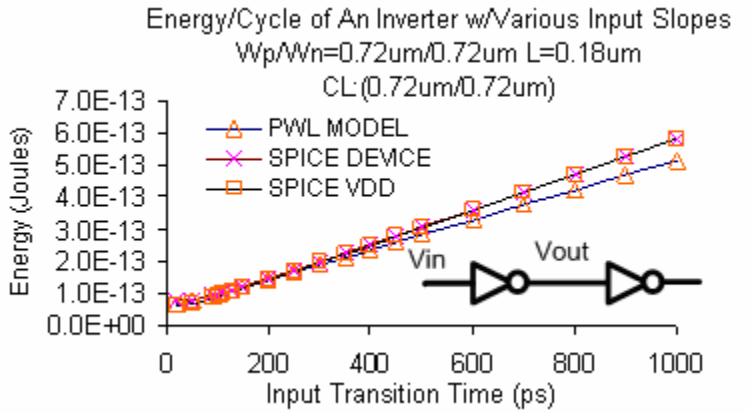

Figure 4.16 Accuracy of the PWL model in inverter gate driving inverter load (K = 1)

4.5 Summary

This chapter has illustrated the simplified transistor switching current model in predicting the average power dissipation of the inverter driving different load capacitances. As indicated by [8], modeling of the CMOS transistors as series of resistances and capacitances can approximate the transistor performances very accurately in digital CMOS applications. Even though the transistor in the ohmic region is not as accurate as the transistor in saturation, the piecewise linear model has achieved average power predictions within 5% of errors of SPICE for input transition times below 500pico

second. It is encouraging that the simplified switching current (I-V) and (C-V) models can achieve the target accuracy when the input is switching in a high speed, which is common for most large integrated circuits.

There are two discrepant average power simulations from SPICE in each plot. The average power predicted by the piecewise linear model is much closed to the SPICE's average power evaluated from the power supply current than from the total transistor devices. The discrepancies in the average power simulations from the SPICE are reduced when the transistors shrink to a 0.18μm process from a 0.5μm process.

CHAPTER 5

AVERAGE POWER ANALYSIS OF COMPLEX GATES WITH A PIECEWISE LINEAR MODEL

5.0 Introduction

In Chapter four, the piecewise linear model is applied to the inverter gate, and the piecewise linear model for the average power evaluation is within 10% average error of SPICE for a wide range of input slopes, different capacitor loads, different transistor sizes and load capacitances, and different process technologies in submicron AMIS 0.5μm and deep submicron TSMC0.18μm process. The piecewise linear model is applicable not only to predict a simple inverter gate, but also extendable to other circuit topologies. The piecewise linear model has shown its scalable and portable among submicron and deep submicron processes by using different set of model parameters. Appendix II includes model parameters used in piecewise linear model for AMIS 0.5μm and TSMC 0.18μm processes.

5.1 Average Power Analysis of Two-input NAND Gate

In this chapter, the applications of the piecewise linear model are extended beyond an inverter gate analysis. Complex gates, such as a two-input NAND gate and an OAI gate are common digital CMOS circuits and are used as the test circuits in this

chapter. NAND gate uses the same model as to evaluate the power supply current into the circuit, but the two dimensional *G* and *C* matrices is written according to the drain nodes in each piecewise linear region. Similar to the inverter analysis, the power supply current drawn from the supply into the circuit is evaluated from pFETs that are switching. The average power predicted by the model is compared with SPICE by varying input slopes, different transistor sizes, output loads, and process technologies.

5.1.1 Two-input NAND Gate Driving Load Capacitance

Fig. 5.1 is the two-input NAND gate with input signals *A* and *B*. The gate drives a constant 100fF load. Average power of NAND gates is evaluated when only input A is switching for a complete cycle. Multiple inputs can be handled by making V_{in} a column matrix, but the output node driving the load is critical for evaluating average power from the power supply. The pull-up parallel connected transistors are the same size and so does the pull-down series connected transistors. The width ratio of the PMOS transistor to NMOS transistor changes from K = 4, 2, and 1.

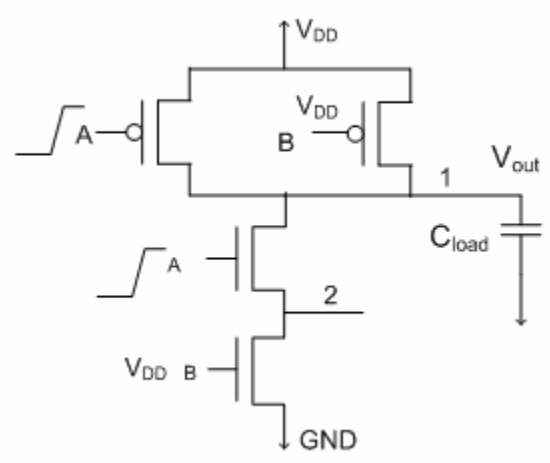

Figure 5.1 Two-input NAND driving load capacitance

Energy per cycle is calculated with different input transition time and a different load for the two-input NAND with the input signal 'A' switched from a cycle. Switching input signal '*B*' resemble an inverter driving a capacitive load. Therefore, switching *B* is not discussed.

5.1.2 Model Accuracy of Two-input NAND in AMI 0.5µm Process (L_{min} = 0.6µm)

The average power of NAND gate is evaluated when the input *A* is switching for a complete cycle and the input of the lower NMOS transistor stay high. Fig. 5.2 shows the average power of NAND gates against various input slopes. Input rise time varies from 50ps to 1500ps and width ratio of PMOS transistors to NMOS transistors varies from K = 4, 2, and 1. Average error was within 3% of SPICE for small input slopes at the high switching frequencies and within 10% for large input slopes at the slower switching frequencies.

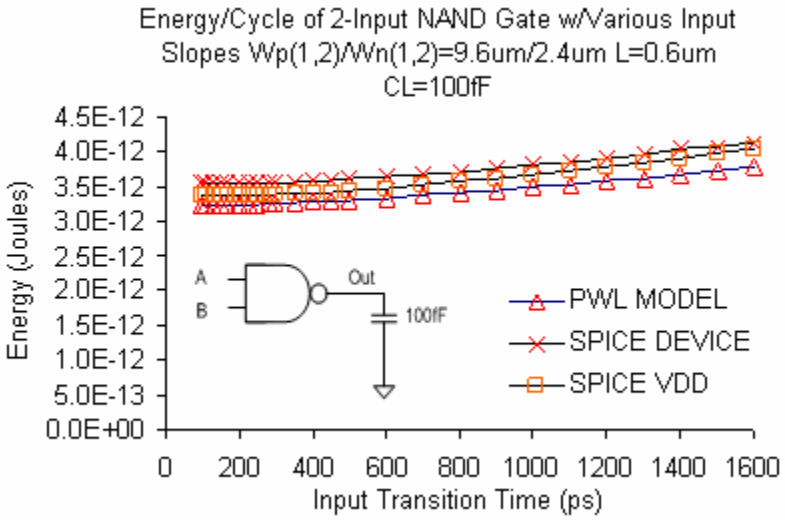

Figure 5.2 Accuracy of the PWL model for two-input NAND K = 4 (Wp/Wn = 9.6µm/2.4µm) driving 100fF load

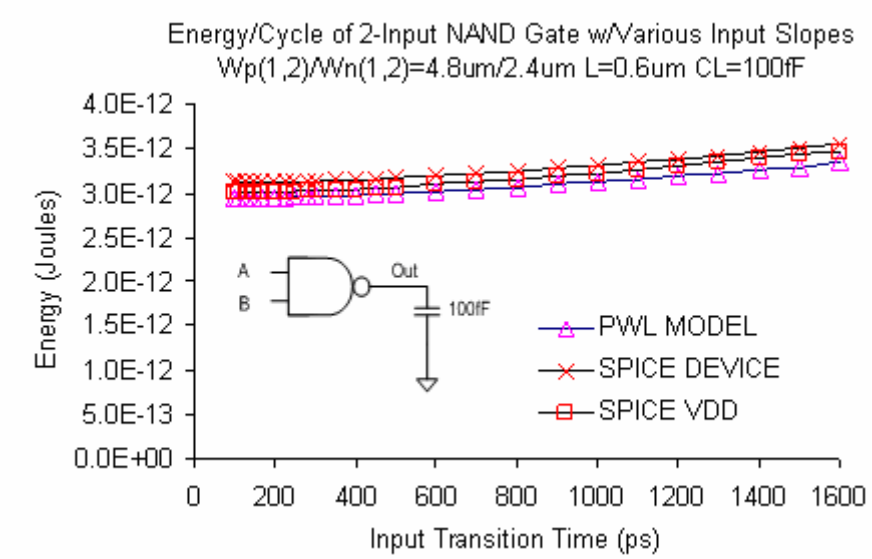

Figure 5.3 Accuracy of the PWL model for two-input NAND K = 2 (Wp/Wn = 4.8µm/2.4µm) driving 100fF load

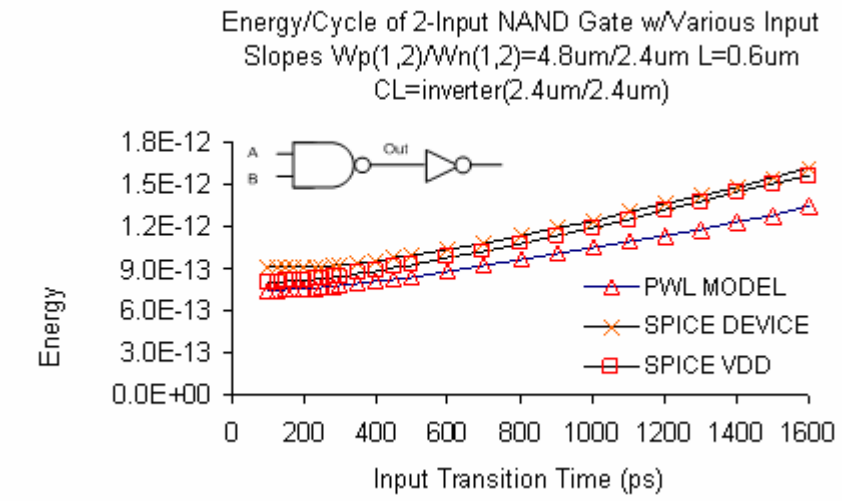

Figure 5.4 Accuracy of the PWL model for two-input NAND gate K = 2 (Wp/Wn = 4.8µm/2.4µm) driving inverter load

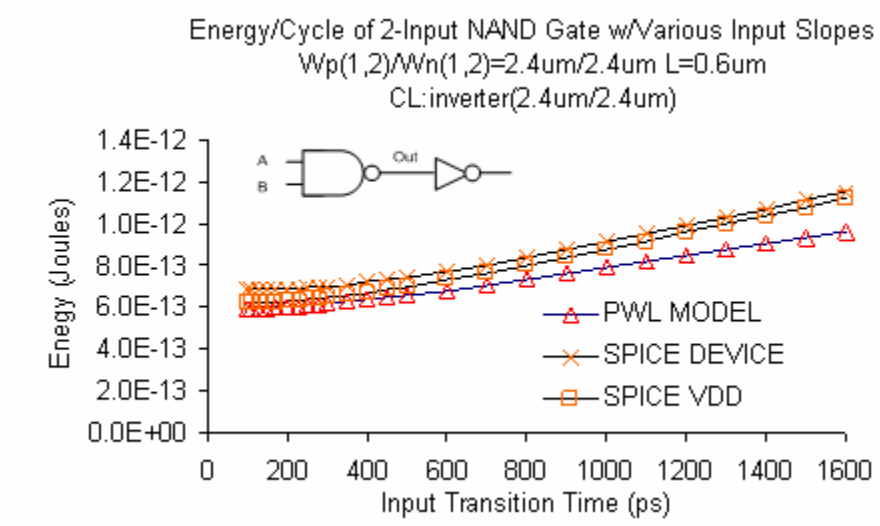

Figure 5.5 Accuracy of the PWL model for two-input NAND gate K = 1 driving inverter load (Wp/Wn = 2.4µm/2.4µm)

5.1.3 Model Accuracy of Two-input NAND in TSMC 0.18µm Process

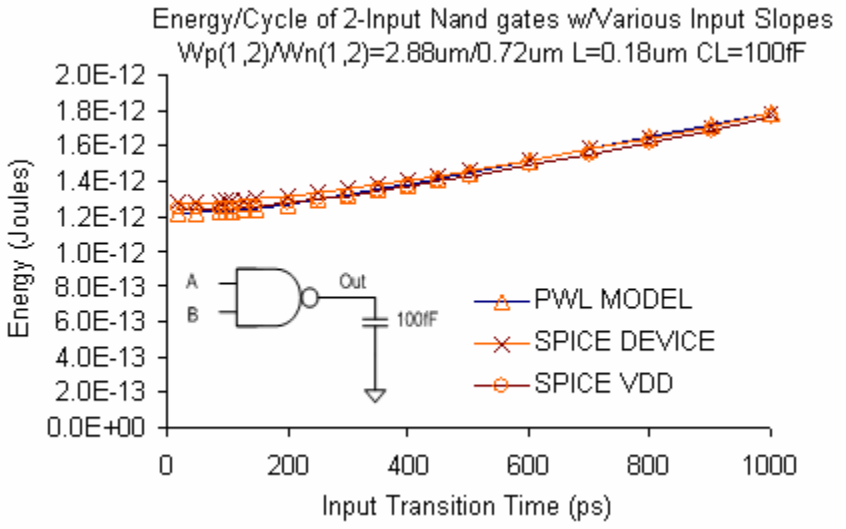

Figure 5.6 Accuracy of the PWL model for two-input NAND gate K = 4 (Wp/Wn = 2.88µm/0.72µm) driving 100fF load

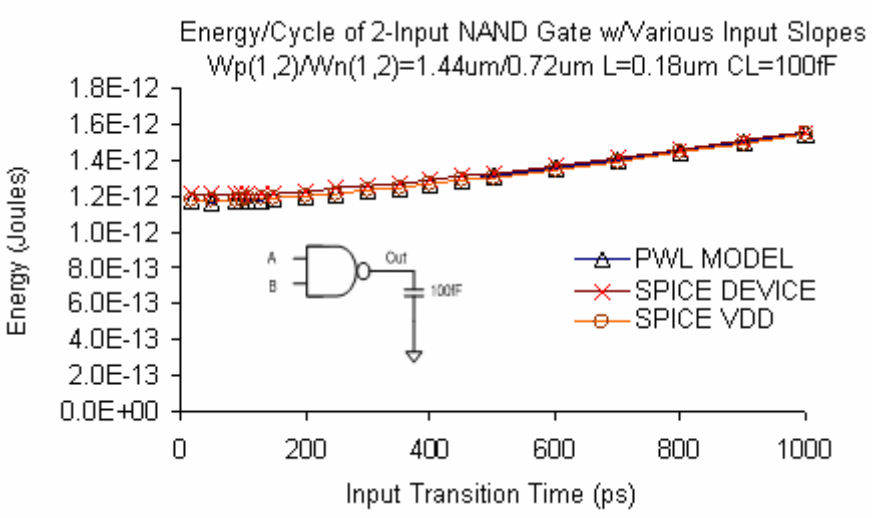

Figure 5.7 Accuracy of the PWL model for two-input NAND gate K = 2 (Wp/Wn = 1.44µm/0.72µm) driving 100fF load

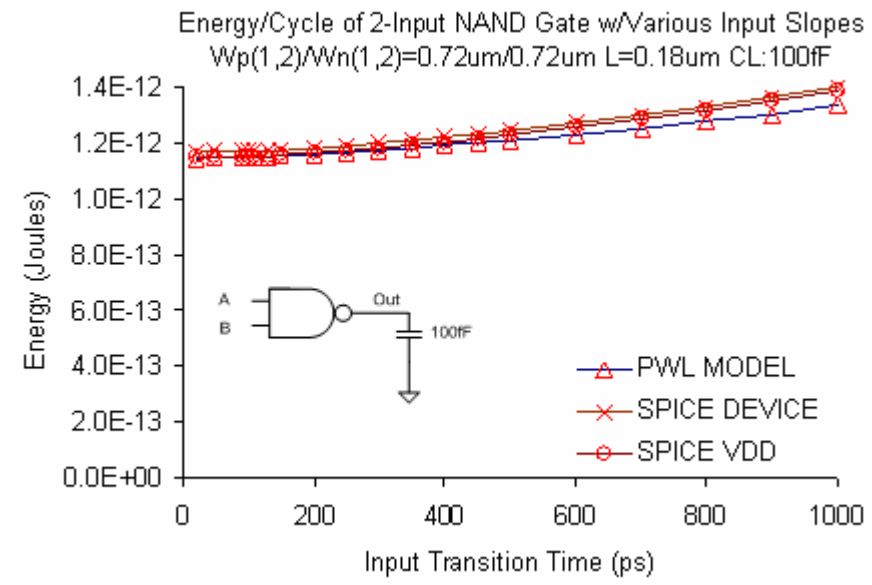

Figure 5.8 Accuracy of the PWL model for two-input NAND gate K = 1 (Wp/Wn = 0.72µm/0.72µm) driving 100fF load

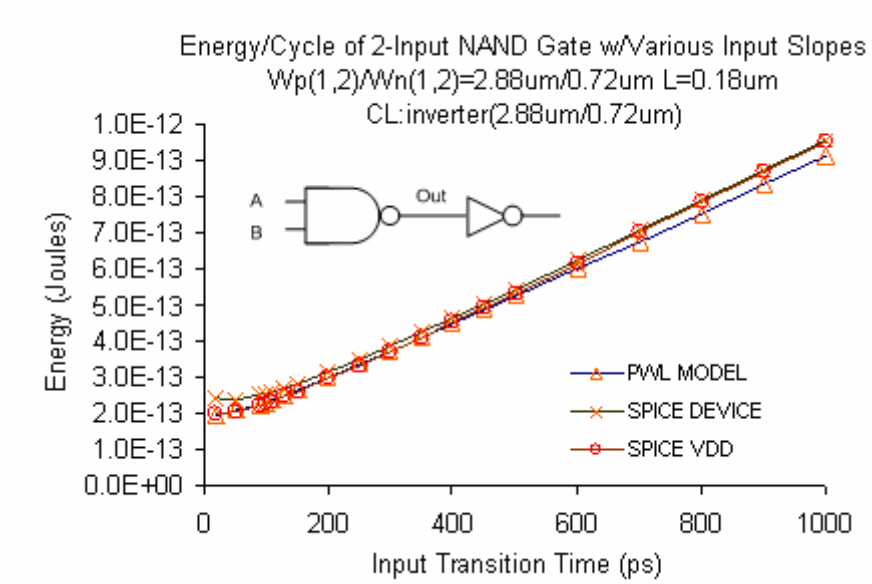

Figure 5.9 Accuracy of the PWL model for two-input NAND gate K = 4 driving inverter load (Wp/Wn=2.88µm/1.44µm L=0.18µm)

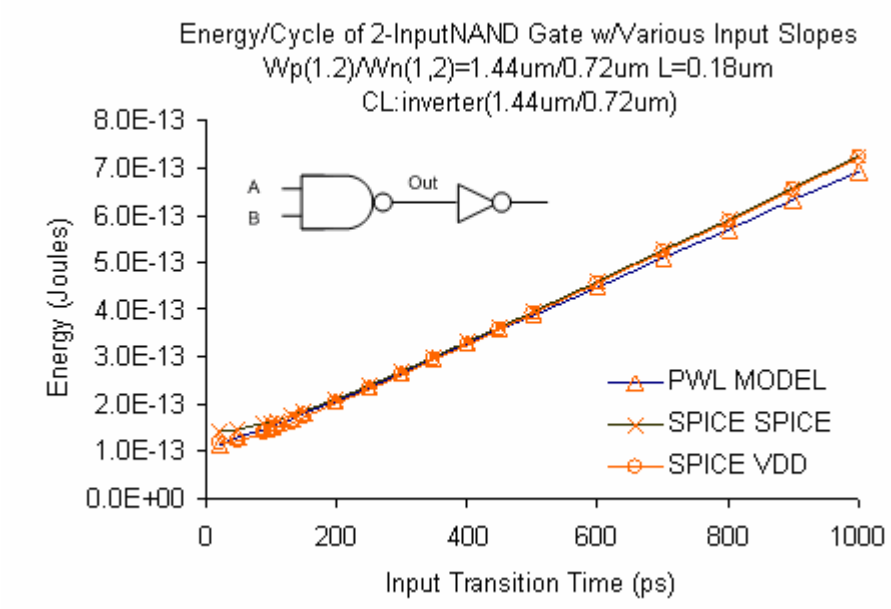

Figure 5.10 Accuracy of the PWL model for two-input NAND gate K = 2 driving inverter load (Wp/Wn=1.44µm/0.72µm L=0.18µm)

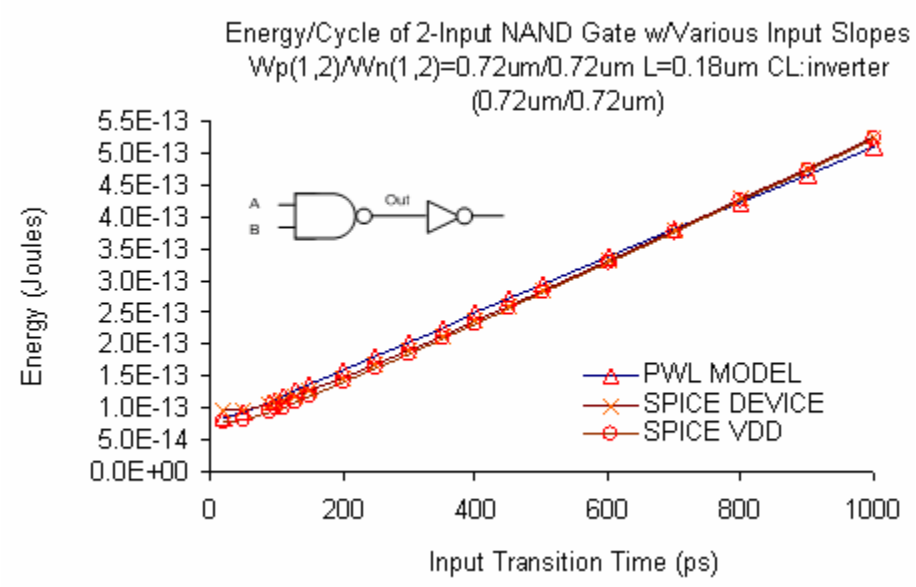

Figure 5.11 Accuracy of the PWL model for two-input NAND gate K = 1 driving inverter load (Wp/Wn=0.72µm/0.72µm L=0.18µm)

5.2 Average Power Analysis of OAI Gate

Fig. 5.12 is an OAI gate with input *A*, *B*, and *C*. Input A = 0→1, B = 1, and C = 0 are assumed when the average power of OAI gates is evaluated. The model allows multiple inputs by making V_{IN} as a column matrix, but only the supply node and the drain of pFET connected to the power supply are necessary for evaluating average power from the power supply. The width of PMOS transistors to NMOS transistors varies from K = 4, 2, 1 driving a constant 100fF load with different input slopes. A submicron 0.5µm process and deep submicron 0.18µm process parameters are used to confirm the model's accuracy.

5.2.1 Average Power Analysis of OAI Gate Driving Load Capacitance

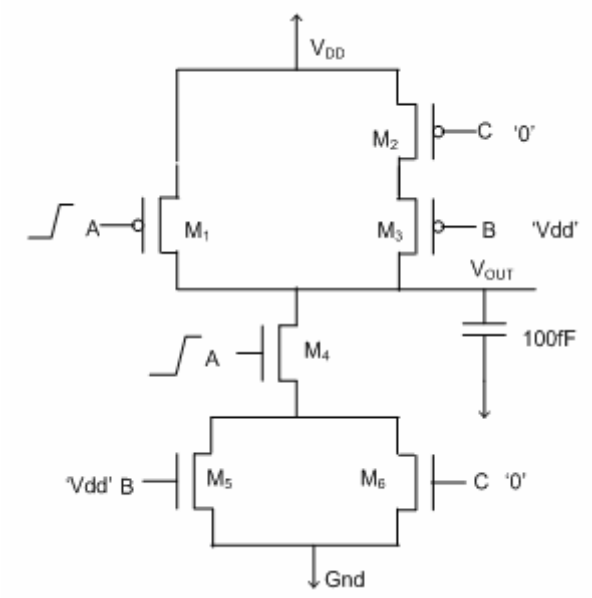

Figure 5.12 OAI gate driving 100fF load

5.2.1.1 Model Accuracy of OAI gate in AMI 0.5μm Process

Average power of OAI gate is evaluated based on one switching cycle. Inputs A switches for a complete cycle while the input B is tied to V_{DD} and the input C is tied to ground. Accuracy for OAI gates driving a constant 100fF with different transistor K ratio is still within 3% error of SPICE for small input slopes and in 10% error of SPICE for large input slopes in average.

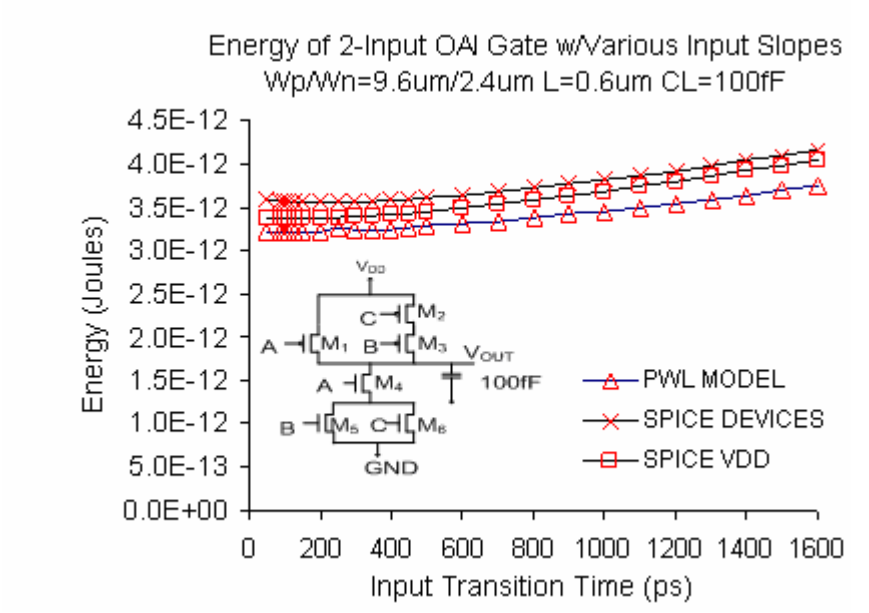

Figure 5.13 Accuracy of the PWL model in OAI gate K = 4 (Wp/Wn = 9.6µm/2.4µm) driving 100fF load in 0.5µm process

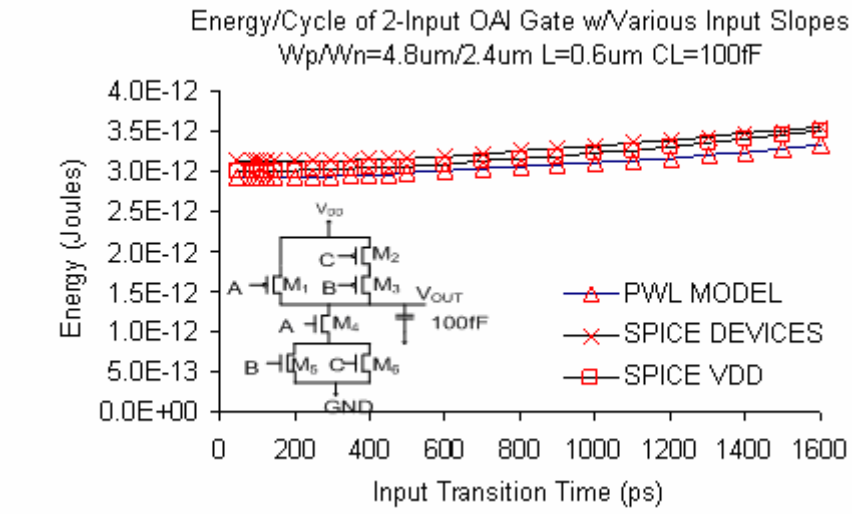

Figure 5.14 Accuracy of the PWL model in OAI gate K = 2 (Wp/Wn = 4.8µm/2.4µm) driving 100fF load in 0.5µm process

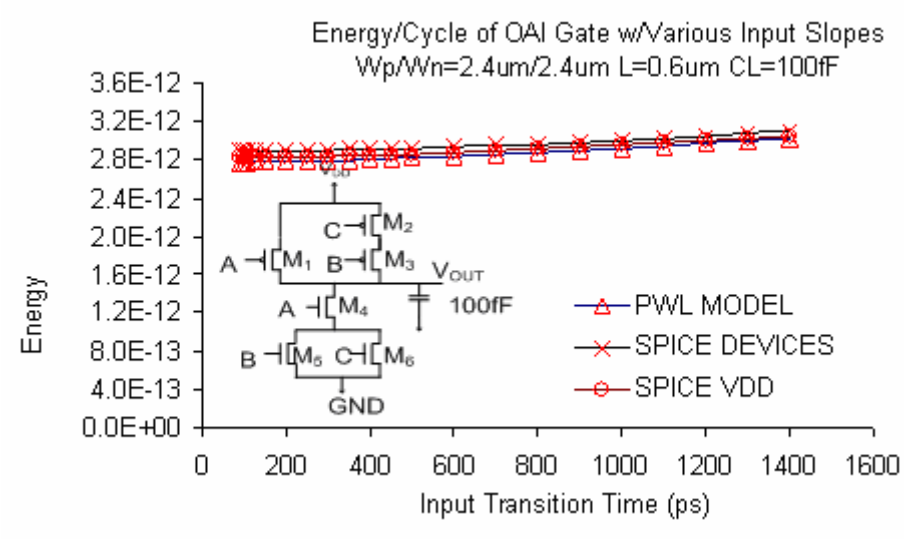

Figure 5.15 Accuracy of the PWL model in OAI gate K = 1 (Wp/Wn = 2.4µm/2.4µm) driving 100fF load in 0.5µm process

5.2.1.2 Model Accuracy of OAI Gate in TSMC 0.18µm Process

Three-input OAI gate is tested in TSMC 0.18µm process as well to measure the model's accuracy in different process technologies. Accuracy of OAI gate driving a constant 100fF with different transistor K ratio is within 5% of SPICE for small input slopes and within 10% of SPICE for large input slopes.

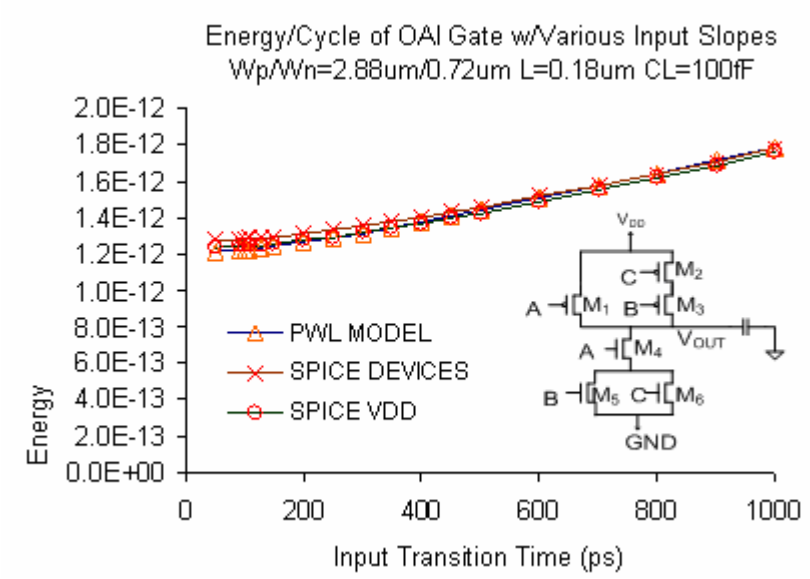

Figure 5.16 Accuracy of the PWL model in OAI gate K = 1 (Wp/Wn = 2.88µm/0.72µm) driving 100fF load in 0.18µm process

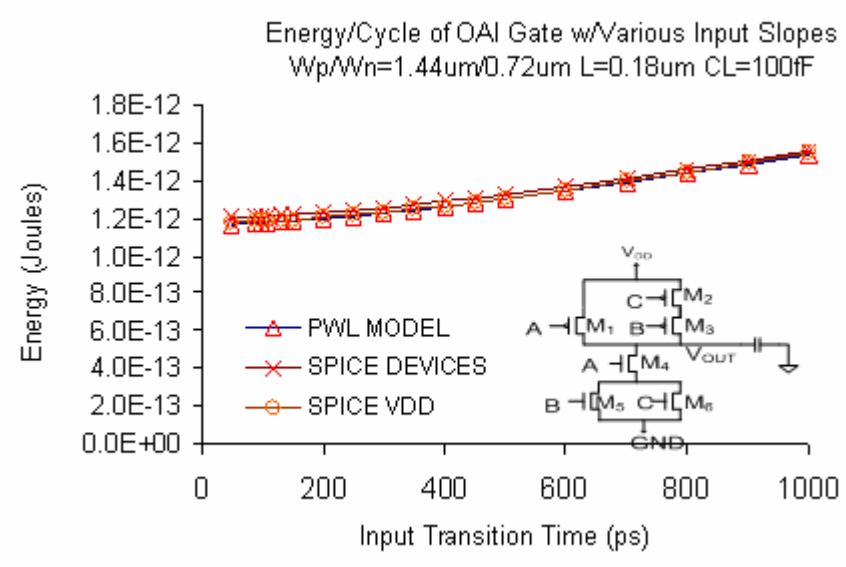

Figure 5.17 Accuracy of the PWL model in OAI gate K = 2 (Wp/Wn = 1.44µm/0.72µm) driving 100fF load in 0.18µm process

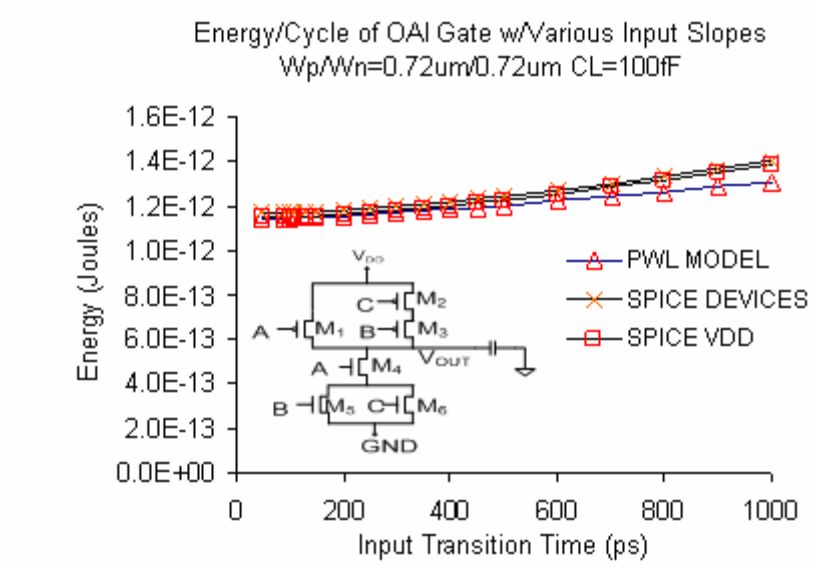

Figure 5.18 Accuracy of the PWL model in OAI gate K = 1 (Wp/Wn = 0.72µm/0.72µm) driving 100fF load in 0.18µm process

5.2.2 Average Power Analysis of OAI Gate Driving Inverter Load

In this case, average power of OAI gate is evaluated with input, A, which switches for a complete cycle whiles input, B, tied to V_{DD} and input, C, and tied to the ground. Accuracy of the OAI gates driving inverter with different inverter ratio of K = 4, 2, and 1 is compared with SPICE with the same designs. Averaged error is within 3% of SPICE for small input slopes and within 10% of SPICE for large input slopes.

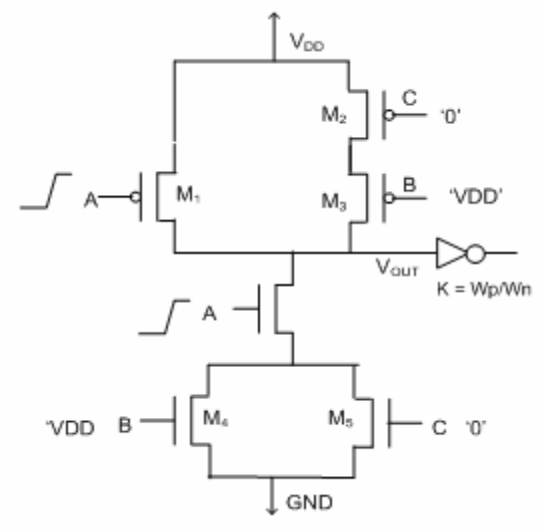

Figure 5.19 OAI gate driving different inverter loads

5.2.2.1 Model Accuracy of OAI Gate in AMI 0.5µm Process

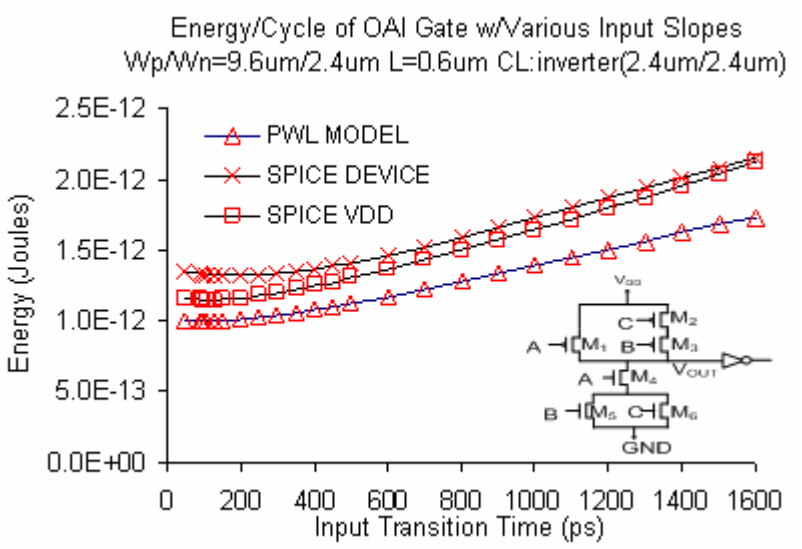

Figure 5.20 Accuracy of the PWL model in OAI gate K = 4 (Wp/Wn = 9.6µm/2.4µm) driving inverter load K=1 in 0.5µm process

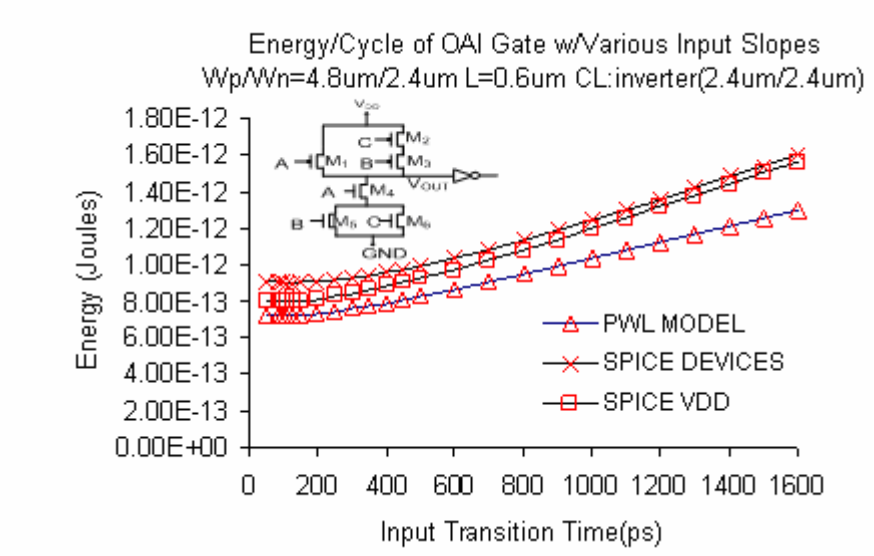

Figure 5.21 Accuracy of the PWL model in OAI gate K = 2 (Wp/Wn = 4.8µm/2.4µm) driving inverter load K=1 in 0.5µm process

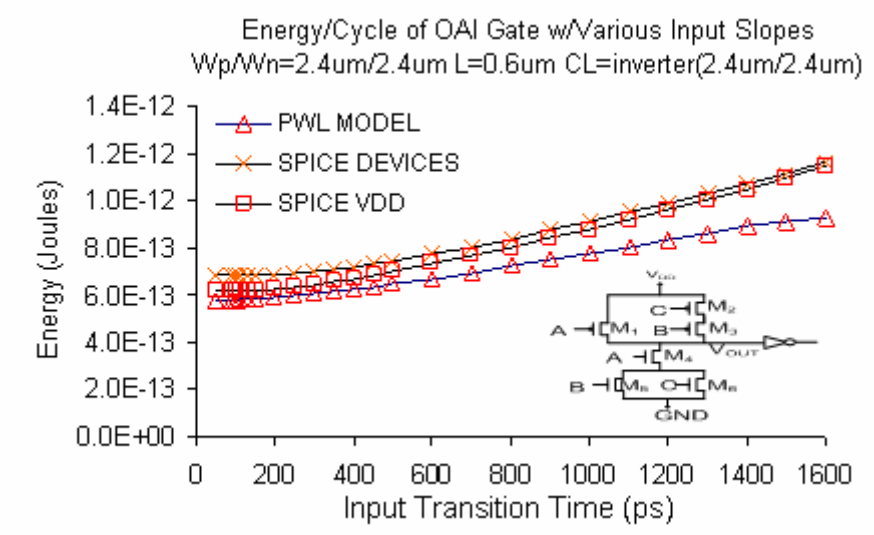

Figure 5.22 Accuracy of the PWL model in OAI gate K = 1 (Wp/Wn = 2.4µm/2.4µm) driving inverter load K=1 in 0.5µm process

5.2.2.2 Model Accuracy of OAI Gate in TSMC 0.18µm Process

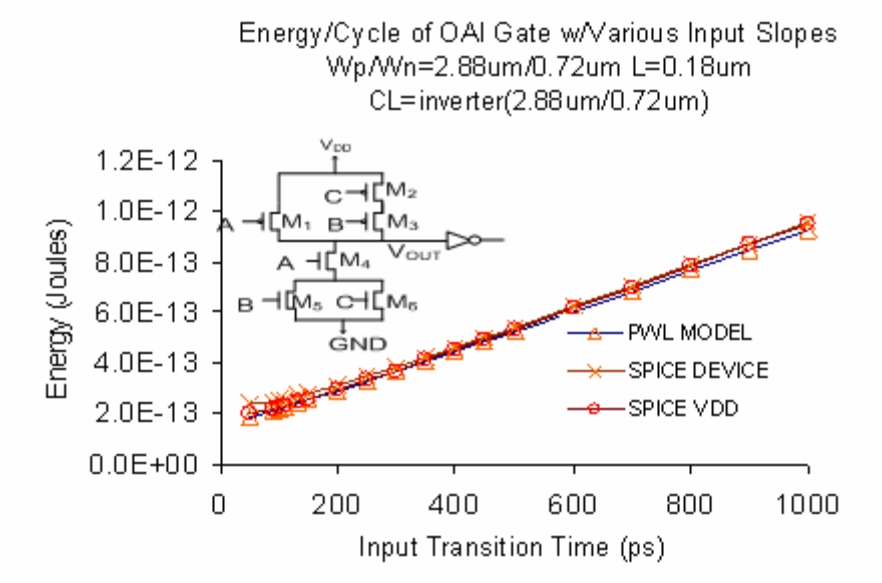

Figure 5.23 Accuracy of the PWL model in OAI gate K = 4 (Wp/Wn = 2.88µm/0.72µm) driving inverter load K= 4 in 0.18µm process

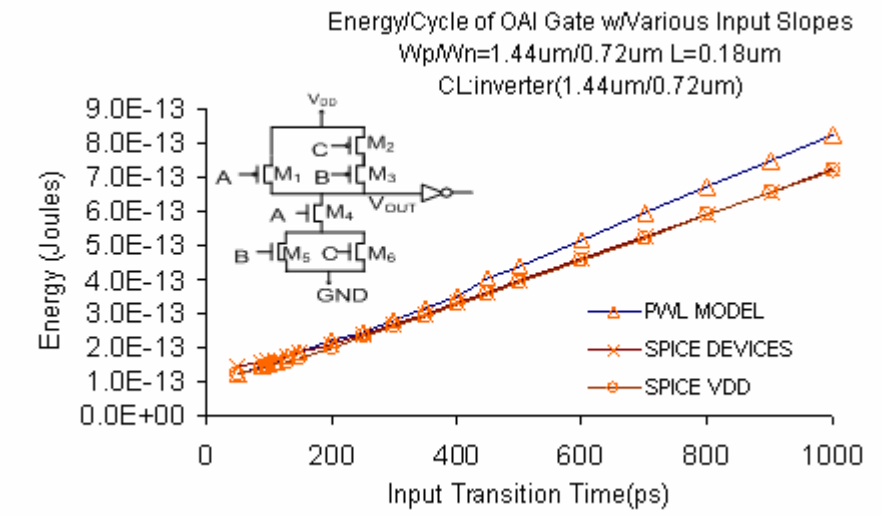

Figure 5.24 Accuracy of the PWL model in OAI gate K = 2 (Wp/Wn = 1.44µm/0.72µm) driving inverter load K= 2 in 0.18µm process

CHAPTER 6

6.0 CONCLUSION

The scaling of semiconductor process technologies has been the fuel that boosts millions of transistors to be incorporated in a single digital integrated circuit, and power dissipation is becoming a critical issue when more transistors are integrated and operated in high frequencies. Unfortunately, as the complexity of integrated circuits increases, simulating circuits with an accurate yet simple transistor model becomes very challenging. In general, lower levels of simulation utilize more detailed transistor model and provide greater accuracy, such as SPICE. However, increased accuracy is usually achieved at the expense of long computation times.

This dissertation has proposed a piecewise linear transistor model to evaluate the total power dissipation from the power supply current into the circuits. The piecewise linear model includes the effect of signal input slope into the short-circuit power and dynamic power computation. The innovation of the model in power evaluation is to include the first-order channel capacitive currents from the transistor parasitic capacitances into a power calculation.

Extensive comparisons have been done between the piecewise linear model and the SPICE BSIM3v3 model in the circuit simulation. The test circuit included an inverter gate, a two-input NAND gate, and an OAI gate driving different load capacitances. Excellent accuracies of the piecewise linear model have been achieved for the average

power predictions under those test circuits for both AMI 0.5μm process and the deep submicron TSMC 0.18μm process. The proposed model has the advantage of simulation speed over SPICE running BSIM3 model, because the piecewise linear model is used to compute the power supply current into a large circuit partitioned into many resistively connected regions with only a few number of transistors and capacitors. Therefore, matrices operation is necessary only when solving the power supply current into the resistively connected nodes from the transistors connected to the power supply. However, simulation speed of the proposed model will be slower than the switched-resistor model in IRSIM since the switched-resistor model has not modeled the transistors in saturation, input slope effects, and accurate circuit dynamics comparable to SPICE's prediction, but the proposed model will be much accurate than the switched resistor model in a power calculation.

6.1 FINDINGS

Simulation inconsistencies were found in SPICE when simulating the average power dissipation by the power supply and simulating average power consumption by the transistor devices in the inverter driving different load capacitances. Discrepancies exist when more complex gates were simulated for average power, such as a two-input NAND gate and OAI gate driving different loads. The average power provided to the circuit from the power supply is less than the sum of the average power dissipated by every transistor device in the same circuit. The discrepancies of average power from SPICE simulations come from the zero-order transistor model in SPICE, which computes instantaneous power with the product of the zero-order instantaneous current and drain-source voltage.

Solving the power simulation problem in SPICE requires an energy conserving transistor model, which is beyond the scope of this dissertation. Since the BSIM3v3 model is a well known charge conserving transistor model, accuracies of the proposed model were tested with references to the power supply current entering the circuits or the total average power of the power supply from the SPICE simulation. That is the same approach with the piecewise linear model to evaluate the total average power of a circuit from the power supply current. The piecewise linear approximations of average power to an inverter gate, a two-input NAND gate and an OAI gate driving different load capacitances with various transistor sizes were validated by comparing the model predicted average power with the average power simulation from the power supply in SPICE, and the accuracies were within 5% average error of SPICE for fast inputs and within 10% for most slow inputs. More complex gates, three-input OAI gate with different transistor sizes and driving different load conditions in a standard CMOS 0.5μm and 0.18μm technologies, were also verified with the same range of model accuracy.

6.2 FUTURE WORKS

The main focus of this dissertation is the accuracy of the simple piecewise linear current transistor model in predicting the average power supply current and power for a standard CMOS circuit. Comprehensive tests are done for simple CMOS circuits to verify the proposed model functionality to compute the switching transient power consumption. However, the gate induced sub-threshold leakage current has become a major power dissipation contributor of the total power dissipation, and in many scaled technologies leakage contributes 30% to 50% of the overall power under nominal

operating conditions, and leakage is becoming significant compared to switching transient power [38]. Therefore, modeling leakage current is significant for scaled CMOS technologies.

The piecewise linear model is applicable for average power evaluation to any general CMOS circuits. More works are needed to verify the proposed model with a very large CMOS circuit.

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APPENDICES

Appendix A

I. AVERAGE POWER SIMULATIONS IN SPECTRE SPICE

I.1 SPICE Simulation Inconsistency of Average Power

In the SPICE, average power measured from the power supply or from devices is computed from the integration of instantaneous power waveform over one switching cycle. We ran into simulation discrepancies in SPICE between simulating average power dissipation from the power supply and from the transistor devices in the same circuit (Figure A.1 and A.2). SPICE shows that average power dissipation by the devices is higher than the average power actually drawn from the power supply. The discrepancies may come from the zero-order quasi-static SPICE transistor model, which computes power consumption from a quasi-static zero-order instantaneous current multiplied by drain-source voltage. Over-estimation of average power in SPICE transistor models leads to the issue of non-energy conserving transistor model in SPICE, which neglects of the first-order channel capacitive currents. The transistor model (BSIM) and Spectre simulator has the same problem by not taking into account of the first-order channel capacitive currents into the transistor parasitic capacitances as indicated in HSPICE simulator manual [3].

Average power dissipation simulation from the power supply can be written as equations (I.1), and the average power simulation from devices can be written as equation (I.2).

$$P_{avg(vdd)} = \frac{1}{T}\int_0^T i_{vdd}(t) * V_{DD}(t)dt = \frac{E}{T} \tag{I.1}$$

$$P_{avg(device)} = \frac{1}{T}\sum_{m=1}^{n}\int_0^T i_{Dnn}(t) * V_{Dnn}(t)dt + \frac{1}{T}\sum_{m=1}^{n}\int_0^T i_{Dpn}(t) * V_{Dpn}(t)dt \tag{I.2}$$

SPICE simulation discrepancies are shown in Figure A.1 and A.2. Figure A.3 and A.4 demonstrate the simulation tool of SPECTRE SPICE in simulating the average power of inverter from the power supply and the transistor devices respectively.

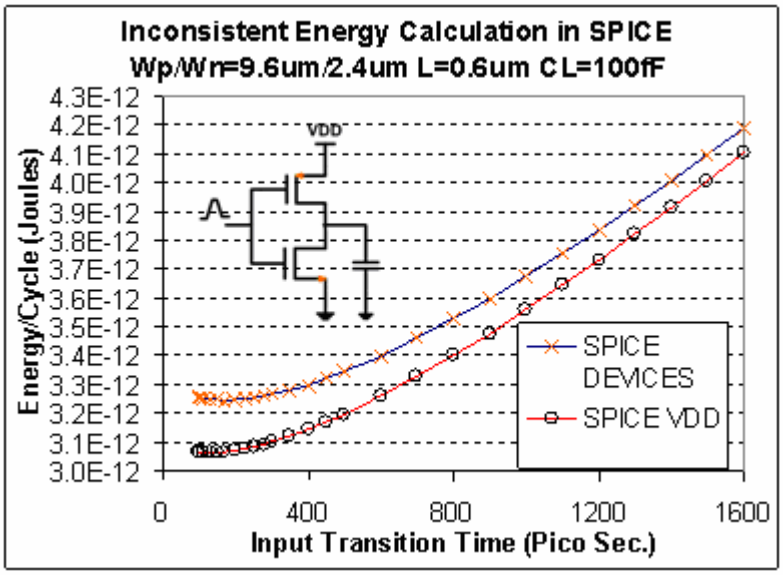

Figure A.1 Average Power Simulation of Inverter in SPICE

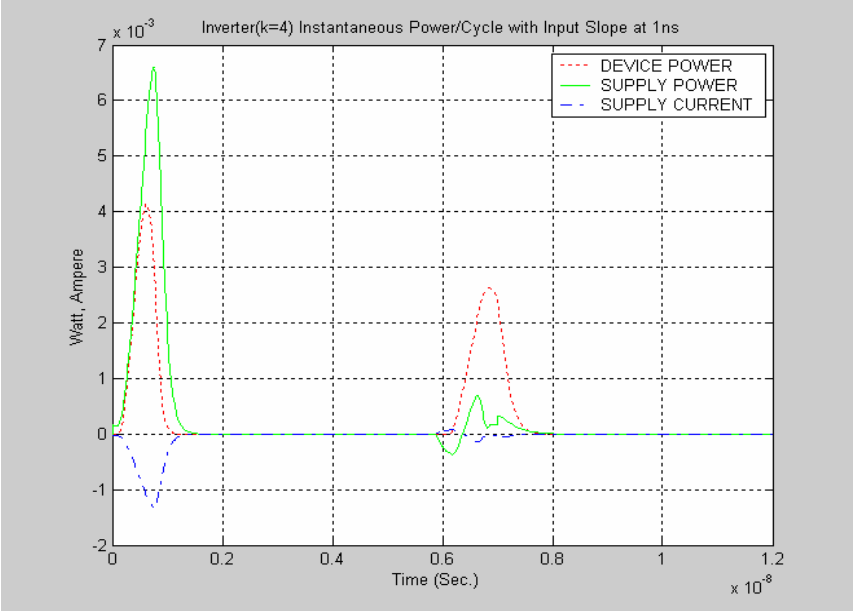

Figure A.2 SPICE power waveform/cycle of Fig.A.1 with 1ns input slope. Dot in red: total device power; solid green line: supply power. Dash-dot in blue: the supply current.

I.2 SPECTRE SPICE circuit net list for an inverter driving 100fF load

```
simulator lang=spectre

model ami06N bsim3v3 type = n
+version = 3.1          tnom    = 27          tox     = 1.41E-8

model ami06P bsim3v3 type = p
+version = 3.1          tnom    = 27          tox     = 1.41E-8

// Library name: inverter_lib
// Cell name: inverter
// View name: extracted

_inst0 (OUT IN ps pb) ami06P w=9.6e-06 l=6e-07 as=1.44e-11 ad=1.44e-11 \
      ps=1.26e-05 pd=1.26e-05 m=1 region=sat
_inst1 (OUT IN gnd gnd) ami06N w=2.4e-06 l=6e-07 as=3.6e-12 ad=3.6e-12 \
      ps=5.4e-06 pd=5.4e-06 m=1 region=sat
_inst2 (OUT gnd) capacitor c=100e-15 m=1

// power supplies
VPWR(vdd 0) vsource dc=5.0
VGND(gnd 0) vsource dc=0.0
```

```
// inputs
  VIN(IN 0) vsource dc=5.0 type=pulse val0=5 val1=0\
  period=13n rise=1500p fall=1500p width=5n

// current test meter
VTEST1(vdd ps) vsource dc=0.0 type=pulse val0=0 val1=0
VTEST2(vdd pb) vsource dc=0.0 type=pulse val0=0 val1=0

opts1 options pwr=total save=all
setting1 options save=all
opts options currents=all
opts2 options pwr=total save=all
save _inst0:pwr
save _inst1:pwr
save VPWR:pwr
save VGND:pwr

// controls
inverter tran step=1p start=0n stop=13n errpreset=conservative

save OUT IN
```

I.3 Average Power Simulation in SPECTRE

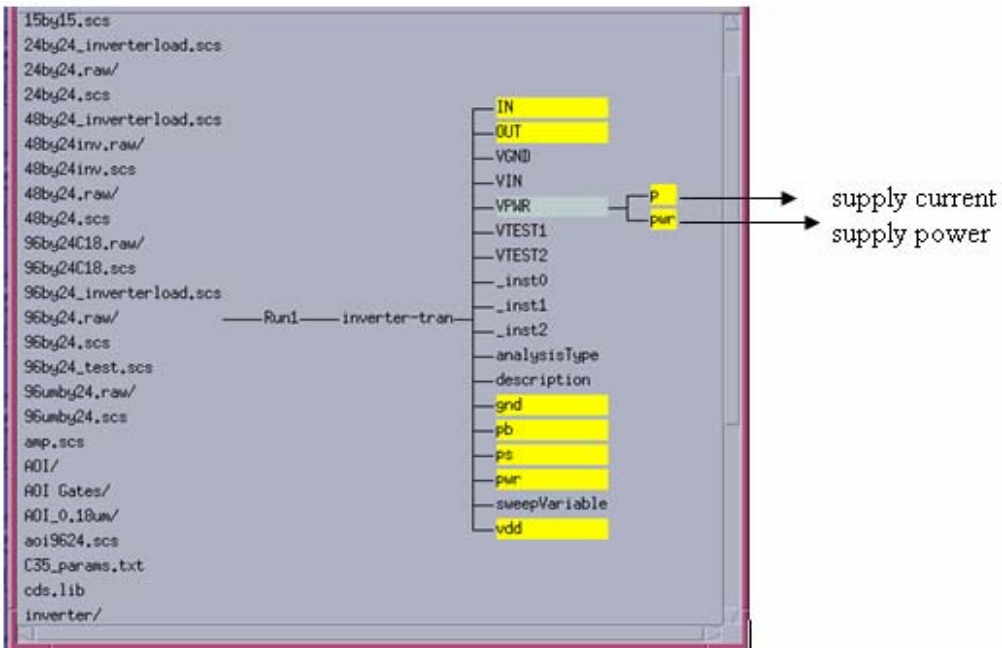

Figure A.3 Average Power Simulation from the Power Supply in SPECTRE

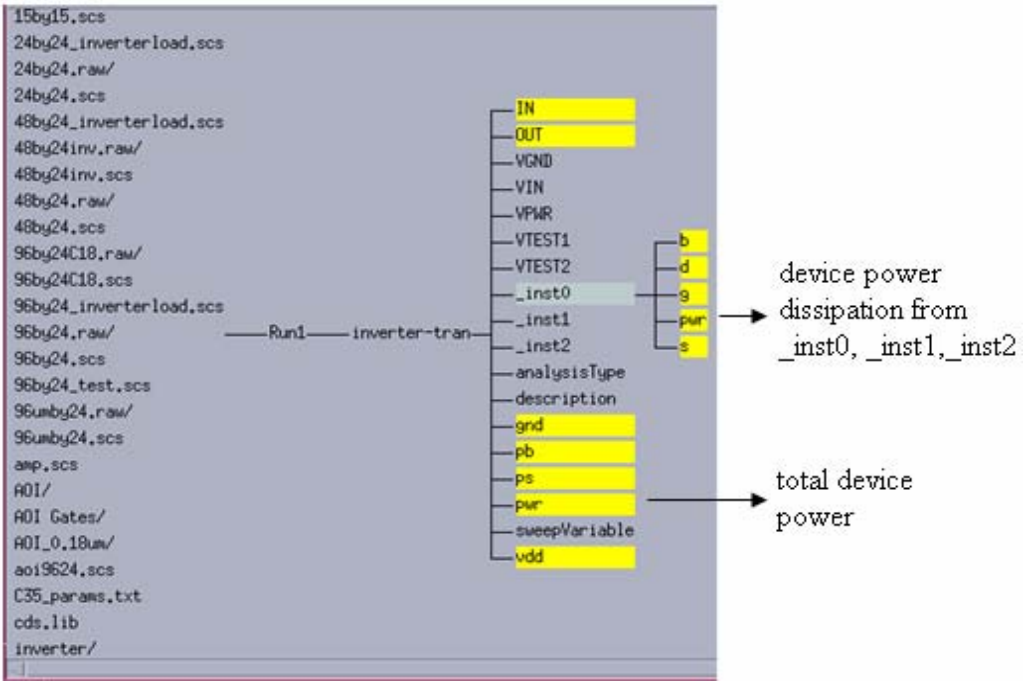

Figure A.4 Average Power Simulation from Total Device Power in SPECTRE SPICE

Appendix B

MODEL PARAMETER EXTRACTIONS FOR AMI 0.5μm AND TSMC 0.18μm PROCESSES

I. Model Parameters Extraction

The piecewise linear current model has a total of six parameters: a_n, a_p, V_{Tn}, V_{Tp}, G_{sat}, and G_{ohmic}. The parameters of a piecewise linear transistor model can be extracted directly from SPICE $I_D - V_{GS}$ and $I_D - V_{DS}$ curves for transistors used in the circuit. There are many techniques associated with V_{Tn} and V_{Tp} extractions from transistor I/V curves from [4]. The V_{Tn} and V_{Tp} in the piecewise linear model are extrapolated from SPICE $I_D - V_{GS}$ family curves at the maximum slope of V_{GS} curves to $I_{DS} = 0$ point. The tangent line across $I_{DS} = 0$ is the threshold voltage on the V_{GS} curve as shown in Fig.B.1 and Fig. B.2. An averaged V_{Tn} and V_{Tp} in equation (B.1) are computed from the threshold voltages extrapolated from $I_D - V_{GS}$ curves.

$$V_T = \frac{V_{T1} + V_{T2} + V_{T3} + V_{T4} \ldots . V_{Tm}}{m} \qquad \text{(B.1)}$$

Transistor $I_D - V_{GS}$ curves are generated in SPICE with BSIM3v3 transistor model in a region of greatest current, for AMIS 0.5μm process, $2.5 < V_{GS} < 5.0$ and $2.5 < V_{DS} < 5.0$.

The rationale is that most of change of voltage at the output of CMOS circuit is proportional to the output transistor biased in the high current range [39], because the rate of voltage change at the output depends on the magnitude of the current. The modeling errors in regions of low drain current (when the transistor in the ohmic region) usually produce smaller timing errors than errors in regions of high current (when the transistor is in saturation) [39]. Hence, the proposed piecewise linear transistor model uses an average value for each parameter to minimize the timing error in regions of high current as indicated in [39].

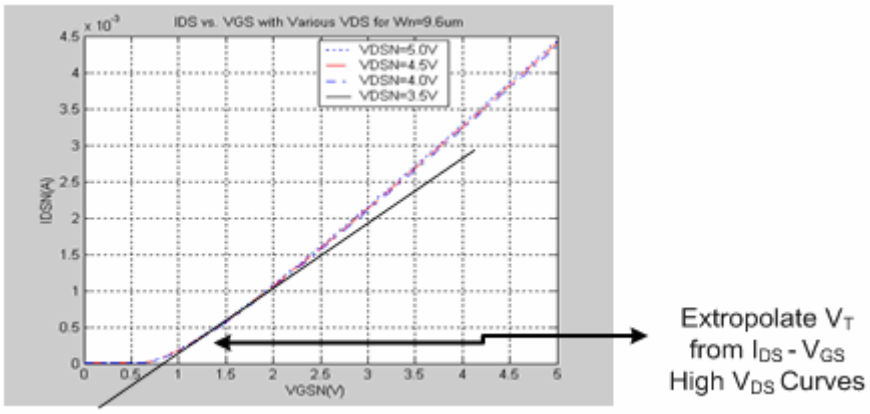

Figure B.1 Threshold voltage extraction from high V_{DSN} curves in 0.5µm process

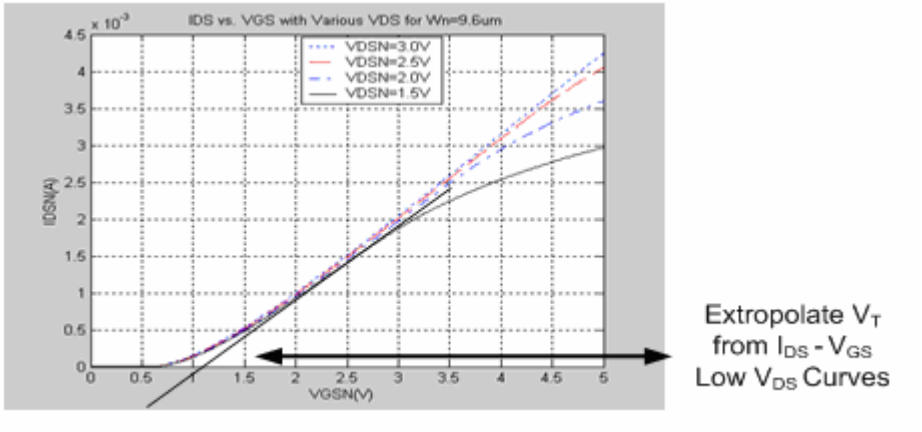

Figure B.2 Threshold voltage extraction from low V_{DSN} curves in 0.5µm process

The maximum slope of the $I_D - V_{GS}$ curve is the large signal transconductance of the transistor G. An averaged transconductance was determined by taking the average slopes from $I_D - V_{GS}$ curves at high V_{DS} and low V_{DS} curves. Since five $I_D - V_{GS}$ curves were plotted at a high V_{DS} and five $I_D - V_{GS}$ curves were plotted for a low V_{DS}, a total of four extrapolated $G_{(N)SAT}$ and $G_{(P)SAT}$ were averaged to obtain an average G_{NSAT}, G_{PSAT}. The conductance at the ohmic region for nFET and pFET devices, $G_{(N)OHM}$, and $G_{(P)OHM}$, were derived using the same approach with $I_D - V_{DS}$ curves. In this case, the average conductance can be computed as equation (B.3) from $I_D - V_{DS}$ curves and as shown in Figure 3.3 and Figure 3.4. Similarly, average transconductance (slopes of curves) can be extracted from $I_D - V_{GS}$ curves shown in Figure B.1 and Figure B.2.

$$G_{n(p)sat} = \frac{G_{nsat1} + G_{nsat2} + \ldots + G_{nsat4}}{4} \tag{B.2}$$

$$G_{n(p)ohm} = \frac{G_{ohmic1} + G_{ohmic2} + \ldots + G_{ohmic4}}{4} \tag{B.3}$$

Quasi-static dc current scaling factors a_n and a_p for nFET and pFET are computed by

$$a_{n(p)} = \frac{G_{n(p)ohm}}{G_{n(p)sat}} \tag{B.4}$$

Appendix II includes all parameters extracted from SPICE simulations in AMI 0.5μm and TSMC 0.18μm process for the piecewise linear model.

The model parameters for the piecewise linear (PWL) model were extracted from I/V family curves of various transistor sizes from the AMI CMOS 0.6um submicron technology and a TSMC 0.18μm deep submicron technology.

i. Extracted PWL transistor parameters for AMI 0.5μm process

W_p (um)	R_{sp} ($\Omega/\square$)	V_{Tp} (V)	a_p
1.2	2.1×10^4	-1.8	1.251763
2.4	2.1×10^4	-1.6	1.396283
4.8	2.1×10^4	-1.49	1.348792
9.6	2.1×10^4	-1.386	1.352994

Table B.1 Falling input PMOS parameters for AMI 0.5μm process

W_p (um)	R_{sp} ($\Omega/\square$)	V_{Tp} (V)	a_p
1.2	3.3×10^4	-1.292	2.9
2.4	3.3×10^4	-1.241	2.8
4.8	3.3×10^4	-1.243	2.0
9.6	3.3×10^4	-1.161	1.2

Table B.2 Rising input PMOS parameters for AMI 0.5μm process

W_n (um)	R_{sn} ($\Omega/\square$)	V_{Tn} (V)	a_n
1.2	1.7×10^4	1.34	1.38442
2.4	1.7×10^4	1.1	1.64235
4.8	1.7×10^4	0.99	1.03714
9.6	1.7×10^4	0.96	1.43759

Table B.3 Falling input NMOS parameters for AMI 0.5μm process

W_n (um)	R_{sn} ($\Omega/\square$)	V_{Tn} (V)	a_n
1.2	1.3×10^4	1.6	1.747667
2.4	1.3×10^4	1.24	1.726266
4.8	1.3×10^4	1.2	1.741734
9.6	1.3×10^4	1.09	1.706108

Table B.4 Rising input NMOS parameters for AMI 0.5μm process

ii. Technology dependent parameters in AMI 0.5μm process used by the PWL model

$C_{ox} = 2.449\times10^{-3}\,F/m^2$ Gate oxide capacitance per unit area

$C_{GBO} = 0$ Gate to substrate overlap capacitance per unit area

$C_{GSO} = 2.07*10^{-10}$ N-channel Gate to source overlaps capacitance per unit area

$C_{GDO} = 2.07*10^{-10}$ N-channel Gate to drain overlaps capacitance per unit area

$C_{GSO} = 2.3 * 10^{-10}$	P-channel Gate to source overlaps capacitance per unit area
$C_{GDO} = 2.3 * 10^{-10}$	P-channel Gate to drain overlaps capacitance per unit area
$x_{partn} = 0.3$	N-channel charge partition parameter
$x_{partp} = 0.3$	P-Channel charge partition parameter
$\delta = 0.6$	Substrate cutoff boundary
$V_{DD} = 5.0$	Power supply voltage

iii. Extracted PWL transistor parameters for TSMC 0.18µm process

W_p (um)	R_{sp} ($\Omega/\square$)	V_{Tp} (V)	a_p
0.72	1.5×10^4	-0.55	1.70
1.44	1.5×10^4	-0.60	1.90
2.88	1.5×10^4	-0.50	1.90

Table B.5 Falling input PMOS parameters for TSMC 0.18µm process

W_p (um)	R_{sp} ($\Omega/\square$)	V_{Tp} (V)	a_p
0.72	0.8×10^4	-0.55	2.9
1.44	0.8×10^4	-0.60	1.2
2.88	0.8×10^4	-0.60	1.0

Table B.6 Rising input PMOS parameters for TSMC 0.18µm process

W_n (um)	R_{sn} ($\Omega/\square$)	V_{Tn} (V)	a_n
0.72	0.6×10^4	0.30	1.90

Table B.7 Falling input NMOS parameters for TSMC 0.18μm process

W_n (um)	R_{sn} ($\Omega/\square$)	V_{Tn} (V)	a_n
0.72	0.5×10^4	0.30	1.50

Table B.8 Rising input NMOS parameters for TSMC 0.18μm process

iv. Technology dependent parameters in TSMC 0.18μm process in the PWL model

$C_{ox} = 8.628\times10^{-3}\,F/m^2$ Gate oxide capacitance per unit area

$C_{GBO} = 0$ Gate to substrate overlap capacitance per unit area

$C_{GSO} = 7.90*10^{-10}$ N-channel Gate to source overlaps capacitance per unit area

$C_{GDO} = 7.90*10^{-10}$ N-channel Gate to drain overlaps capacitance per unit area

$C_{GSO} = 6.36*10^{-10}$ P-channel Gate to source overlaps capacitance per unit area

$C_{GDO} = 6.36*10^{-10}$ P-channel Gate to drain overlaps capacitance per unit area

$x_{partn} = 0.3$ N-channel charge partition parameter

$x_{partp} = 0.3$ P-Channel charge partition parameter

$\delta = 0.6$ Substrate cutoff boundary

$V_{DD} = 3.3$ Power supply voltage

II. Source/Drain Diffusion Capacitance Model

The source and drain diffusion capacitances come from the bottom and sidewalls of the source and drain area of a transistor as illustrated in Figure B.3. The BSIM model does not compute for the area and perimeter of the transistors inside the model. Instead, the diffusion capacitances are extracted from the layout extractor, which actually measure the width and perimeter from the transistor layout and generate a circuit net-list for SPICE simulation. Figure B.3 shows the equations used by the piecewise linear model to find the transistor geometry parameters. The geometry of transistor, A_S, A_D, P_S, and P_D, is computed from the equation shown in Figure 3.10 for the model and SPICE while comparing model accuracy with SPICE. Equation (B.5) is the BSIM diffusion capacitance model [4], from which the piecewise linear diffusion capacitance model is derived.

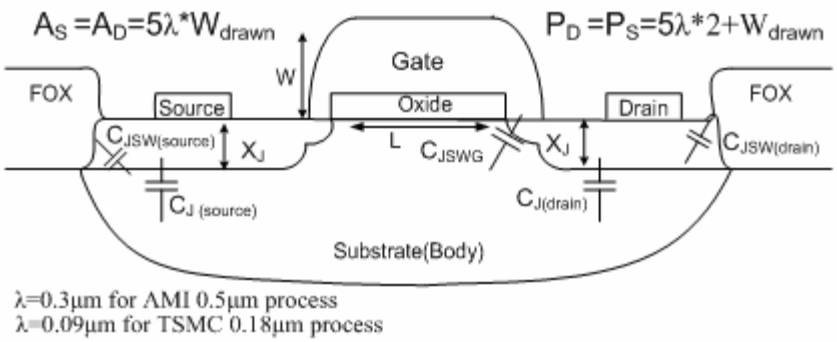

Figure B.3 Transistor diffusion capacitance model

$$C_{dS} = A_S C_j \left(1 + \frac{V_{SB}}{\phi_B}\right)^{-m_j} + (P_S - W) C_{JSW} \left(1 + \frac{V_{SB}}{\phi_{BSW}}\right)^{-m_{jsw}} + W C_{JSWG} \left(1 + \frac{V_{SB}}{\phi_{BSWG}}\right)^{-m_{jswg}} \quad \text{(B.5)}$$

Drain to substrate capacitance is calculated by placing *S* with *D* in the diffusion capacitance model. A typical BSIM diffusion capacitance with respect to substrate bias would look like Figure B.4.

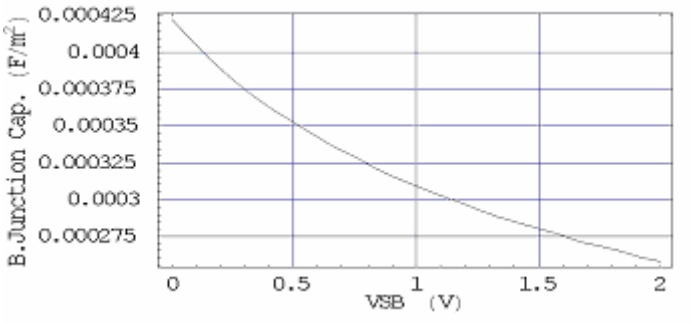

Figure B.4 Source junction capacitance versus body bias

To obtain a piece-wise linear capacitance model, one should average the diffusion capacitance over the range of $V_{SB} = -\phi_B$ to 0, $V_{SB} = 0$ to $V_{SB} = V_{DD}/2$, and $V_{SB} = V_{DD}/2$ to $V_{SB} = V_{DD}$. The junction capacitances in the piecewise linear model is summarized according to junction capacitance in each piecewise linear region.

$$\overline{C}_{dS} = \begin{pmatrix} \dfrac{Q_{dS}(0)}{\phi_B}, -\phi_B < V_{SB} < 0 \\ \dfrac{Q_{dS}(V_{DD}/2) - Q_{dS}(0)}{V_{DD}/2}, 0 < V_{SB} < V_{DD}/2 \\ \dfrac{Q_{dS}(V_{DD}) - Q_{dS}(V_{DD}/2)}{V_{DD}/2}, V_{DD}/2 < V_{SB} < V_{DD} \end{pmatrix} \quad \text{(B.6)}$$

Let $\overline{C}_{dS}$ in equation (B.6) be written in terms of averaged source/drain to substrate junction capacitance, sidewall capacitance, and sidewall to gate capacitance.

$$\overline{C}_{dS} = \overline{C}_{dSj} + \overline{C}_{dSjsw} + \overline{C}_{dSjswg} \quad \text{(B.7)}$$

$$\overline{C}_{dSj} = \frac{A_S C_j}{(1-m_j)} \begin{cases} 1, -\phi_B < V_{SB} < 0 \\ \frac{2\phi_B}{V_{DD}}((1+\frac{V_{DD}}{2\phi_B})^{1-m_j} - 1), 0 < V_{SB} < V_{DD}/2 \\ \frac{2\phi_B}{V_{DD}}((1+\frac{V_{DD}}{\phi_B})^{1-m_j} - (1+\frac{V_{DD}}{2\phi_B})^{1-m_j}), V_{DD}/2 < V_{SB} < V_{DD} \end{cases} \quad \text{(B.8)}$$

$$\overline{C}_{dSj_{SW}} = \frac{(P_S - W)C_{JSW}}{(1-m_{JSW})} \begin{cases} 1, -\phi_{BSW} < V_{SB} < 0 \\ \frac{2\phi_{BSW}}{V_{DD}}((1+\frac{V_{DD}}{2\phi_{BSW}})^{1-m_{JSW}} - 1), 0 < V_{SB} < V_{DD}/2 \\ \frac{2\phi_{BSW}}{V_{DD}}((1+\frac{V_{DD}}{\phi_{BSW}})^{1-m_{JSW}} - (1+\frac{V_{DD}}{2\phi_{BSW}})^{1-m_{JSW}}), V_{DD}/2 < V_{SB} < V_{DD} \end{cases} \quad \text{(B.9)}$$

$$\overline{C}_{dSj_{SWG}} = \frac{WC_{JSWG}}{(1-m_{JSWG})} \begin{cases} 1, -\phi_{BSWG} < V_{SB} < 0 \\ \frac{2\phi_{BSWG}}{V_{DD}}((1+\frac{V_{DD}}{2\phi_{BSWG}})^{1-m_{JSWG}} - 1), 0 < V_{SB} < V_{DD}/2 \\ \frac{2\phi_{BSWG}}{V_{DD}}((1+\frac{V_{DD}}{\phi_{BSWG}})^{1-m_{JSWG}} - (1+\frac{V_{DD}}{2\phi_{BSWG}})^{1-m_{JSWG}}), V_{DD}/2 < V_{SB} < V_{DD} \end{cases} \quad \text{(B.10)}$$

The diffusion capacitance associated with the output node has great influence on the output waveform because the signal delay time constant τ determines a piecewise linear output waveform according to the operating region of each transistor in a circuit.

Appendix C

CODING AND IMPLEMENTATION

This appendix presents simplified example of C++ program used to compute average power dissipation of a simple inverter. The same piecewise linear model is used to compute the gate delay with the average power according to each piecewise linear region of operation defined in Figure 4.2 and Figure 4.4.

```
for (input rise time){
  if(input slope>0){
    Read in model parameters for rising input
    Define boundaries for each piece-wise linear regions.}
  else{
    Read in model parameters for falling input
    Define boundaries for each piecewise linear regions.}
   for(time=0.0;time<4000ps;time+=1.0ps){
      time11=tsi; "vgs=vtn and vgs=vtp for rising/falling input."
     if(t3star>time11){
       if(time<time11)
          vi=vdd or 0.0 "5.0/0.0 for rising/falling input."
    Determine tsi,time1,time2, output voltages at time1 and time2.
      tsi=time11;
      time1=region[1].newton(bound[0],vmax,region[1].gettildvi(tsi),tsi,0);
      vi1= region[1].getvout(tsi,time1,vmax,region[1].gettildvi(tsi));
      time2=region[0].getRegion[0].getRegion0time2(time1,vi1);
      vi2= region[0].getRegion0vi2(time2);
```

```
  if((time<=time1)&&(time>tsi)){
Calculate vi from tsi to time1 in the region1.
   vi=region[1].getvout(time11,time,vdd-vin.gets0(),tildvi(tsi);
Calculate average power from tsi to time1 in the region1.}

  if (time2<=t3star) "For most of slow Inputs"
  {
   "Determing New time3"
   time3=t3star;
   "Determine output voltages at time3 with previous region time2,vi2."
   vi3=region[3].getvout(time2,time3,vi2,region[3].gettild
      vi(time2));

    if((time<=time2)&&(time>time1)){
   "Calculate output voltages between time1 and time2 in the region0."
    vi=region[0].getvoutRegion0(time1,time,vi1);
   "Determine average power at the same piecewise region
    region0_staticQp_sat=region[0].getStaticRegion0_Qp(time1,time2);
     }

  if((time<=time3)&&(time>time2)){
   Determine output voltages from time2 to time3 in the region3;
   Calculate average power between time2 and time3 in the region3;
   }
  if((time<=ttin)&&(time>time3)){
   Determine output voltage from time3 to ttin in the region5;
   Calculate average power between time3 and ttin in the region5;
   }
 "Determing output voltages at time4 with previous region of time3 and vi3"
  vi4=region[5].getvout(time3,ttin,vi3,region[5].gettildvi(time3));

  if(time>ttin){
   Determine output voltages beyond input transition time in the region7;
   Calculate average power from ttin to infinity in the region7;
    }

   else "time2>t3star" " for most of fast inputs."
   {
      Re-define time3 and new output voltages at time3 in the region0
       time3 = t3star ;
       vi3=region[0].getRegion0vi3(time1,vi1,time3);

      if((time<=time3)&&(time>time1)){
      Determine output voltages between time1 to time3 in the region0;
      Calculate average power from time1 to time3 in the region0;}

      Determine New time2 and vi at time2 for region2
       time2=region[2].getRegion0time2(time3,vi3);
```

```
     vi2=region[2].getRegion0vi2(time2);

    Determine time2>ttin or time2<ttin
     if(time2>ttin){
     Determine New vi at time4 for region2
     vi4=region[2].getRegion0vi3(time3,vi3,ttin);

     if((time<=ttin)&&(time>time3)){
     Calculate output voltages from time3 to ttin in the region2
      vi=region[2].getvoutRegion2(time3,time,vi3);
     Calculate average power from time3 to ttin in the region2.}

 Determine time2 and output voltage at time2 in the region6
 time2=region[6].getRegion6time2(ttin,vi4);
 vi2=region[6].getRegion6vi2();

if((time<=time2)&&(time>ttin)){
 Calculate output voltages from ttin to time2 in the region6
 Calculate average power from ttin to time2 in the region6
 vi=region[6].getvoutRegion6(ttin,time,vi4);}

 if(time>time2){
 Calculate output voltages from time2 to infinity in the region7
 vi=region[7].getvoutRegion7(time2,time,vi2,region[7].gettildvi());
    Calculate average power from time2 to infinity in the region7 }
 }
 else "ttin>time2"
 {
   if((time<=time2)&&(time>time3))
    Calculate output voltages from time3 to time2 in the region2.
      vi=region[2].getvoutRegion2(time3,time,vi3);
    Calculate average power from time2 to time3 in the region2.

   if((time<=ttin)&&(time>time2))
   Calculate output voltages from time2 to ttin in region5.
      vi=region[5].getvout(time2,time,vi2,region[5].gettildvi(time2));
   Calculate average power from time2 to ttin in the region5

   Determine vi at time4
     vi4=region[5].getvout(time2,ttin,vi2,region[5].gettildvi(time2));

  if(time>ttin){
  Calculate output voltages from ttin to infinity in the region7
       vi=region[7].getvoutRegion7(ttin,time,vi4,region[7].gettildvi());
  Calculate average power from ttin to infinity in the region7}
}
    }
  }
```

```
    }
}
```

VITA

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Doctor of Philosophy

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Title of Study: POWER MODELING OF CMOS DIGITAL CIRCUITS WITH A PIECEWISE LINEAR MODEL

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Major Field: Electrical and Computer Engineering

Scope and Method of Study:

This paper presents the average power modeling of CMOS digital circuits with a piecewise linear (PWL) model. The innovation of the piecewise linear model in the average power evaluation against previous power models is to include, for the first time, the effects of the first-order channel capacitive currents into a power calculation. Also, the model in the evaluation of the average power supply current predicts the currents contributed to the short-circuit power, dynamic power, and switching power of parasitic capacitances. A first-order channel storage charge model is derived to compute the power consumption caused by the nonlinear parasitic capacitances in a transistor channel. The PWL modeling of average power was validated by comparing SPICE average power simulation from the power supply current. The proposed model was validated with a submicron CMOS 0.5μm process and a deep submicron 0.18μm process to test its portability as a technology-independent model.

Findings and Conclusions:

The simulation discrepancies were found when the SPICE simulating the average power dissipation from the power supply current and the average power consumed by the devices in the same circuit. The average power consumed by the devices in a circuit is more than provided by the power supply current. The discrepancies come from the zero-order quasi-static SPICE transistor model, which computes the instantaneous power from the zero-order quasi-static transistor current and multiplied by its drain-source voltage. It has been well defined that the BSIM is a charge-conserving transistor model, so the average power dissipated by the power supply current into the circuit is the true power in SPICE which was used to test the accuracy of the PWL model. The PWL approximation to the average power of an inverter gate and a two-input NAND gate with various transistor sizes and loads were within 3 to 5% averaged error of SPICE for fast inputs and within 10% for slow inputs. Complex OAI gates were also verified with the same range of accuracy.

ADVISER'S APPROVAL: Dr. Louis G. Johnson