MODELING, ANALYSIS AND DESIGN OF RELIABLE DIGITAL IMAGING SYSTEM

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CHAPTER 1

INTRODUCTION

Digital imaging systems have replaced film-based photographic systems in most scientific or commercial application areas such as digital x-ray systems, electronic microscopes, space telescopes, military vision systems, and digital cameras. The digital camera has prevailed in the current market over the film based camera.

As the need for higher resolution and more sensitive Image Sensors grows, high yield and solid reliability are becoming stringent requirements for Image Sensors. In this context, the soft-test/repair method is proposed in this dissertation in order to achieve a high yield and reliability for Image Sensors[1][2][3][7][11][12].

Emerging as stringent requirements increases in chip size and number of pixels as well as decreases in noise level and manufacturing costs are works of modern semiconductor technology.

Charge Coupled Devices (CCD) are widely used in scientific, medical or special purpose imaging systems due to the high dynamic ranges, high quantum efficiencies, low dark noise and large sensing areas. Because of the powerful image sensor characteristics (i.e., high performance), CCD is popularly used in high-end image sensing device such as digital cameras, digital camcorders and digital x-ray diagnosis systems.

Recently *Active Pixel Sensor* (APS) or *Complementary-Symmetry Metal Oxide Semiconductor* (CMOS) Image Sensors are replacing low-end and consumer products such as digital cameras or cheap camera systems because it is based on CMOS technology that is cost-efficient for mass production.

The quantum efficiency is determined by the physical dimensions of an image

pixel. In order to keep both a pixel size large and an increase the number of pixels, the die should be large. Increased die size lowers the yield of image sensors. This is the dilemma of high-end imaging systems such as digital x-ray systems or scientific aerospace telescopes.

The yield of an image sensor by size is given as follows[33]:

$$Y_N = Y_{SA}^N \tag{1.1}$$

where Y means yield and Y_N is expected yield for N times larger than small area $Y_{SA}(1K \times 1K)$.

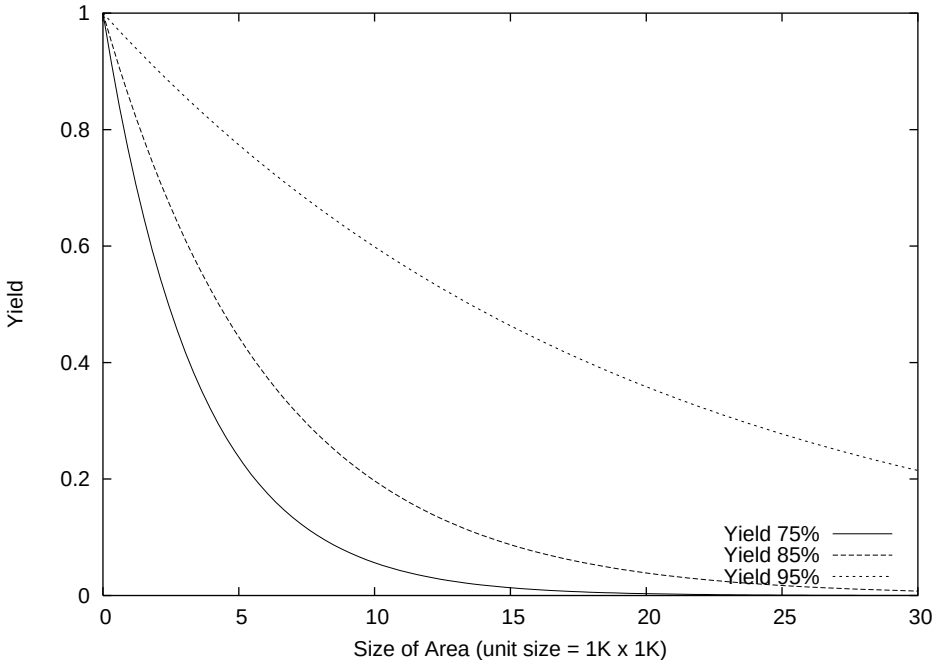

Figure 1.1: Yield by N times area

Figure (1.1) could be drawn from the Equation (1.1). If the size of image sensor is 16 times of Y_{SA} (i.e., $Y_N = 4K \times 4K$), then the anticipated yield from the graph is less than 10% (when $Y_{SA} = 85\%$), and the yield is not affordable for mass production. In other words, the manufacturers can fabricate $1K \times 1K$ image sensors in adequate yield (i.e. above 85%), however, it is hard to get a high yield for large size image sensors such as $4K \times 4K$ image sensors without reducing the pixel size.

- Soft-test/repair in CCD based Digital X-ray system

Modern x-ray imaging systems are evolving toward digitization for reduced cost, faster time-to-diagnosis and improved diagnostic confidence. For digital x-ray systems, CCD technology is commonly used to detect and digitize optical x-ray images. This work presents a novel soft-test/repair approach to overcome the defective pixel problem in CCD-based digital x-ray systems through theoretical modeling and analysis of the test/repair process. There are two possible solutions to cope with the defective pixel problem in CCD; one is the hard-repair approach and another is the proposed soft-test/repair approach. The hard-repair approach employs a high-yield, expensive CCD to minimize the impact of hard-defects on the CCD., These occur in the form of noise propagated through the A/D converter to frame memory. Therefore, less work is needed to filter and correct the image at the end-user level while it may be exceedingly expensive to practice. On the other hand, the proposed soft-test/repair approach detects defective pixels at the digitized image level; therefore it is inexpensive in practice and on-line repairs can be done for non-interrupted service. It tests the images to detect detective pixels and filter noise at the frame memory level, and it caches them in flash memory in the controller for future repair. The controller cache keeps accumulating all of the noise coordinates, and preprocesses the incoming image data from the A/D converter by repairing them. The proposed soft-test/repair approach is particularly devised to facilitate hardware level implementation ultimately for real-time tele-diagnosis. Parametric simulation results demonstrate the speed and virtual yield enhancement by using the proposed approach. Therefore highly reliable, yet inexpensive soft-test/repair of CCD-based digital x-ray systems can be ultimately realized.

- Clustered faults and repair in CCD

Pixels on a CCD may suffer from defective or faulty pixels due to numerous causes such as imperfect fabrication, excessive exposure to light, radiation and sensing element aging to mention a few. As the use of high-resolution CCDs increases, defects and fault tolerances of such devices demand immediate attention. In this context, this study proposes a testing and repair technique for defects/faults in such devices with inability of on-device fault tolerance, referred to as *off-device fault tolerance*. Digital image sensor devices such as CCD can, by their nature, not readily utilize traditional on-device fault tolerance techniques because each pixel on the device senses a unique image pixel coordinate. No faulty pixel can be replaced nor repaired by a spare pixel as any displacement of an original pixel coordinate can not sense the original image pixel. Therefore, to effectively provide and enhance the reparability of such devices with inability of on-device fault tolerance, a novel testing and repair method for defects/faults on CCD is proposed based on the *soft testing/repair* method proposed in Chapter 2 under both single and clustered distribution of CCD pixel defects. Due to unwanted diffusion clustered fault models should be considered as a practical models and compared with single fault models. Also, a novel defect/fault propagation model is proposed to effectively capture the on-device defects and faults off of the device for an effectiveness and practicality of testing and repair process. The efficiency and effectiveness of the method is demonstrated with respect to yield enhancement by the soft-testing/repair method under a clustered fault model as well as single fault model, referred to as *soft yield*. Extensive numerical simulations are conducted.

- BIST/BISR design for soft-test/repair

Built-in self-test (BIST) is an upcoming testing method that makes a circuit test itself without using expensive ATE. BISTs could have more advantages than ATEs in many aspects such as having a larger test bandwidth, being more suitable for stress testing, and eliminating complicated patterns preparation, and functional testing. Defective

pixels of CCD are one of the troublesome problems since no CCDs may be free from them. Moreover, the number of defective pixels could be increased by mechanical and/or electrical shock during the normal operation or operation in harsh conditions such as under radiation. In order to efficiently test and repair the defective pixels in CCDs, BIST/BISR architecture and design is proposed and implemented by the soft-test/repair algorithm. The proposed BIST/BISR is designed without increasing complexity and cost by reusing and sharing existing the functional logics with the CCD controller. As the proposed BIST/BISR operates concurrently with normal CCD operations, overall testing and repair performance are enhanced. Furthermore, BIST employs a parallel testing architecture in order to reduce testing time for bulky data. Verilog HDL simulation is performed in order to validate the design and architecture of BIST/BISR. The efficiency and effectiveness of the proposed BIST/BISR is demonstrated by an enhancement of yield and various simulation results.

The main objective of this work is to propose soft-test and repair methods for defective pixels in imaging sensor system, thereby realizing more reliable and cost-effective imaging sensor Systems. The following specific problems will be addressed and resolved.

- *Soft-Test/Repair* : Soft-Test and Repair techniques for image sensor systems will be proposed to model and evaluate the yield improvement. This technique can be used in both CCD and CMOS image sensors.

- *BIST/BISR Design and Simulation* : Cost efficient and reasonable performance BIST/BISR design and architecture is proposed for imaging sensor system and the performance of the designed BIST/BISR is analyzed through verilog HDL simulation.

- False detection technique is proposed and verified through real image simulations.

The organization of this dissertation is as follows. In Chapter 2, generalized CCD defective pixel models and repair methods are proposed. Theoretical and practical soft-test methods are employed to improve CCD yield and reliability. In Chapter 3, clustered defective pixel model and repairing methods are proposed. It proposes how to test and find clustered defective pixel, and repair methods will be proposed. Then in Chapter 4, a cost efficient BIST/BISR for CCD will be proposed. Unlike conventional BIST, the proposed BIST/BISR concurrently operates with other CCD control circuitry. Finally, the Discussion and Conclusions is presented in the last chapter.

CHAPTER 2

CCD Yield Model and Soft-Repair

2.1 Introduction

Modern x-ray imaging systems evolve toward digitization for reduced imaging cost and higher diagnostic confidence [2]. To provide faster and efficient processing and manipulation of image data, digitization of image data is emerging as a promising alternative technology over conventional analog data-based image processing technology [3]; examples include digital x-ray-based systems such as flat panel, CR (Computed Radiography), and DR (Digital Radiography). Digital x-ray technology is rapidly replacing conventional film-based x-ray techniques. Today's *filmless digital imaging technology* is emerging as a standard in medical applications such as *telemedicine and teleradiology*, due to its promising perspectives such as cost-effectiveness, improved lifetime, reliability, and maintainability [4]. For example, military medical systems require convenient, real-time and efficient medical imaging solutions for their stringent mission-critical purposes [4]. Conventional x-ray films require huge amount of storage, which is very sensitive and vulnerable to temperature and humidity, and hazardous chemical processing for x-ray film development, which also may result in toxic environmental contamination. Furthermore, exposure of patients to x-ray is limited to certain angular setups, which further limits the effectiveness of conventional film-based x-ray medical imaging. Therefore, migration to digital x-ray technology is highly desired.

One of the most critical issues in CCD-based imaging system such as digital x-ray system is how to detect and repair *dark current* (or so-called *black noise*) to

assure quality of service [5, 6]. Generally, digital x-ray system operates an electric or mechanical shutter for about 1000 milli-seconds and sometimes even for longer than 1 second. During that time period, the dark current could accumulate in CCD pixels without flushing; the phosphor cannot properly emit enough light so that the corresponding analog signal becomes too weak to sensor. As a result, the black noise can appear on the resulting x-ray image. Therefore, the dark current should be kept as low as possible by cooling or choosing a better quality and more expensive CCD with low dark current characteristics.

Timely x-ray film read/processing is also one of the most critical requirements to provide high quality service. Under certain harsh environments such as geographical isolation and tactical emergency, x-ray films should be remotely sent to radiologist for timely diagnosis. Filmless digital x-ray system can solve this problem by efficiently transmitting digital x-ray image data over the network to radiologist virtually in real time. Hence, filmless digital x-ray systems provide a promising solution especially for processing and delivery of time-sensitive medical cases, still yet a few problems to be resolved such as hardware reliability and slow software level calibration.

Besides the speed factor of x-ray processing, another critical factor is the *reliability* of the image for higher diagnostic confidence. Excessive x-ray exposure possibly damages CCD pixels and make them defective [7, 8]. Hence, it is required for digital x-ray systems to be maintained regularly by using costly and time-consuming software-based image calibration and tuning. Once a defective pixel hit by all means, the pixel creates a salt-and-pepper noise on target image, since it cannot receive and sense any photon; therefore, a noticeable darker noise point than any other image pixels becomes visible [9, 10]. The reliability is determined either by software or hardware factor. In reality, most CCDs suffer from defective pixels; therefore performance degradation is also experienced consequentially [10]. High-yield CCDs with less defects help resolve this problem at excessive cost in conjunction with complex calibration procedure

[11]. The calibration procedure is generally practiced on software level and off-line for detecting/correcting defective pixels and performing optical corrections such as barrel correction. The approach proposed in [10] removes defective pixels on CCD of a digital camera by periodically executing new off-line calibrations to update old calibration results under a new exposure. However, conventional off-line software-level calibration may create an excessive delay on digital x-ray image processing, which may not be acceptable under stringent processing constraints of today's digital x-ray applications [12, 13].

There also have been a few works proposed to build a reliable CCD-based digital signal processing system from hardware's standpoint in [14, 15, 9, 16]. Digital camera uses high resolution color CCD. In [9], it was proposed that defects on color CCD can be detected and repaired such that a defective CCD pixel can be detected by checking which color has been corrupted among the three colors (i.e., red, green and blue) and repair the pixel by replacing with a spare CCD pixel provided. The approaches relying on spare rows and columns of CCD pixels and, hence, are impractical to implement since it imposes additional cost to the already expensive CCDs [16, 9]. In [14, 15], a self correcting hardware design was presented, in which, unlike the global replacement of defective CCD pixels, spare pixels can replace defective or dead pixels located only on locally neighboring rows or columns. Since each CCD pixel is a sensing device with its predetermined image position to receive a photon from, replacement of a CCD pixel with a spare pixel will result in an irrelevant image data reception after all; thus, serious post image reconstruction must be done.

Cost- and performance-effective testing and repair of CCD pixel defects are critical and essential requirements to realize high quality digital x-ray systems. Currently, the capacity of black and white CCD for a digital x-ray has reached larger than 6 mega pixels resulting in geometric increase in processing speed requirement, even with a simple filtering algorithm. For effective and efficient processing of huge amount of

digital x-ray image pixel data, digital x-ray systems require ultra-high speed data processing with low noise-rate.

This work has been partially presented in [12, 13].

The main objective of this work is to propose a new cost and performance-effective approach to detect and repair CCD hardware pixel defects by proposing a novel yet effective theoretical model for yield and repair rate. Unlike the legacy hard-repair approaches, the proposed repair approach mainly depends on post-processing of the digitized x-ray image data in a real-time processing environment implemented on a FPGA (Field Programmable Gate Arrays). Performance characteristics of the proposed CCD soft-repair approach and benefits from implementation of the proposed hardware-oriented approach will be also investigated through extensive parametric simulations. Note that the proposed work is not to develop new filtering or calibration algorithms, but to propose a hardware-oriented image quality enhancement approach with respect to speed and hardware reliability-driven quality of service. For implementation purpose, any off-the-shelf image processing algorithms can be employed and realized on hardware level. An ultimate implementation plan would be on single chip-level fabrication (i.e., System-on-chip (SoC)) to utilize the performance benefits of SoC technology. Fast run-time dynamic filtering of digital image data on SoC-level is the ultimate goal of the proposed approach.

This work is organized as follows. In the next section (Section 2.2), previous works are reviewed, and basic principles of the proposed approach are introduced. In Section 2.3, the proposed soft-testing and repair process is evaluated. In Section 2.4, a parametric analysis with respect to CCD yield and soft-repair rate is provided. Conclusions and discussions are presented in Section 2.5.

2.2 Review and Preliminaries

A typical digital x-ray system is shown in Figure (2.1). The optical block captures the light generated by phosphor which emits light when it receives x-ray. The CCD image sensor contains numerous pixels and each of which senses photons using electronic well. CCD converts accumulated photons in the electronic well to a corresponding voltage. Then, an analog amplifier, such as OP-Amp, amplifies the signals before it directs the signals to A/D converter for digitization. Thereafter, the sensed image data is propagated all the way to the frame memory through the A/D converter under the coordination of the controller. The size of the frame memory is determined by the required digital image quality. For example, if a 1 Mega pixel CCD is used, 2M byte RAM is needed for the frame memory when gray-scale color depth of 16 bits is required (i.e., $1024 \times 1024 = 1Mpixel$, each pixel needs 16 bit (2 Byte), therefore 2 M Bytes needs for 1 M pixel).

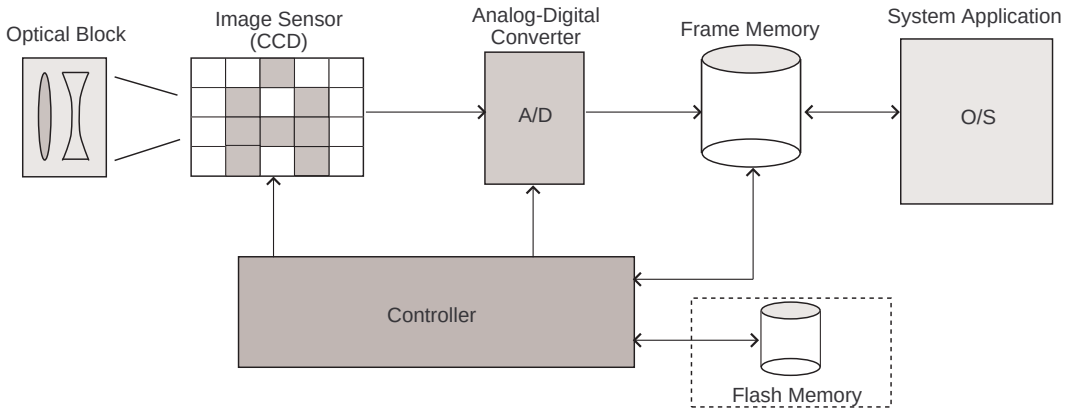

Figure 2.1: Block Diagram of Digital X-ray CCD System

Unfortunately, CCDs are not free from hardware defects. Imperfect fabrication and improper processing may induce defects (referred to as *hard-defects*) on the photo-sensitive pixels and supporting system components in CCD. In [15], the main causes of CCD hard-defects are categorized as follows.

1. Failure of row/column pixels (either line or readout/control transistors/circuit).
2. Failure of row select/reset shift register.
3. Failure of column sense amplifiers.
4. Failure of A/D converter.
5. Failure of buffers.
6. Failure of read-out/reset transistors on each photo-diode.

In practice, all the defects of the above mentioned types affect the quality of the raw image data on the frame memory, since the hard-defects that propagated all the way from the CCD to the frame memory through the A/D converter as shown in Figure (2.1). The effect of a hard-defect observed on the frame memory is referred to as *soft-defect*. Notably, a soft-defective pixel on the frame memory usually shows an abnormal value compared to its neighboring pixel values. Without loss of generality, one-on-one correspondence between a hard-defect on the CCD and a soft-defect on the frame memory can be assumed, unless other component failures than CCD failures are taken into account. In this context, it is feasible to test and repair (i.e., soft-testing/repair) CCD hard-defects on soft memory-mapped level in the form of soft-defects on the frame memory. This work only deals with *permanent* CCD hard-defects.

The A/D converter reads analog image data (i.e., voltage) and convert it to corresponding digital values onto the frame memory storage. In reality, CCDs may contain the mega-scale number of pixels, and they may be either bad or defective (e.g. dead) pixels. In safety-, mission-, and deadline-critical applications, defective pixels may result in devastating consequences. However, defective CCD pixels cannot be effectively replaced by using traditional approach which relies on redundant defect-free pixels, because each CCD pixel can sense only the image pixel on its exact and unique physical position. Therefore, reliability and quality enhancement efforts should be

practiced on some other level such as A/D converter or frame memory [10]. Once the raw image data is stored in the frame memory, it is more efficient to manipulate the image data in digital form since post data processing techniques such as calibration, filtering and image processing algorithms can be applied. A few image processing algorithms have been proposed for the digitized images with defective pixels. In the proposed soft-repair process of the pixels with soft-test, 3×3 *average filter* (or *3x3 mean filter*) is considered. A non-volatile flash memory is employed in the proposed approach to cache and cumulate defect locations, referred to as *noise history data map*. By using the noise history data map stored in the flash memory, the repair process for soft-defect pixels hit on the frame memory can be implemented in a few different ways such as hardware, software, or firmware-level. In the proposed system, SoC-based hardware implementation is considered for the performance benefits of the SoC technology. the proposed approach can be effectively extended[12, 13].

The main idea of the proposed approach is to capture and detect noises (i.e., soft-defects) hit on the frame memory in digital x-ray system, which have been propagated all the way from CCD (i.e., hard-defects) through A/D converter to frame memory as shown in Figure (2.1). A run-time writable flash memory is also used to store and keep track of up-to-date and cumulative *noise history data map*, which is used to pre-process incoming image data to enable skipping testing and repairing previously identified noise pixel positions. The proposed soft-testing and repair approach can be performed in a dynamic manner, since the proposed approach dynamically updates the pixel noise map on flash memory cache, while conventional software-level calibration or filtering approaches can be categorized as static. Thus, the dynamic pixel noise map in the flash memory can be constructed in an acceptable amount of execution time referred to as *pixel noise saturation time*. Having the proposed approach implemented on hardware, especially the whole system implemented on a single chip, the critical issues, such as processing speed and yield of CCD as a measure of the

reliability of the hardware structure of digital x-ray system as addressed before, can be effectively circumvented. The improvements due to the proposed hardware implemented soft-repair approach is referred to as *virtual CCD yield enhancement* and it can be implemented at a minimal hardware cost of flash memory caching without costly extra calibration procedures.

2.3 The Proposed Soft-Test/Repair Process

Notations

D_n	number of defective pixels at the n_{th} test/repair cycle
D_T	total number of soft-defects hit on the frame memory
F_{sh}	number of stuck high pixels
F_{sl}	number of stuck low pixels
F_{hs}	number of high sensitive pixels
F_{ls}	number of low sensitive pixels
F_{fault}	number of defective pixels
F_{repair}	number of repaired pixels
F_{test}	number of tested pixels
p	insensitivity ratio
$P(n)$	n_{th} pixel under test and repair
r_{defect}	decrease ratio of the number of defects after each repair cycle
R_n	number of repaired pixels during the $n'th$ repair cycle
r_{repair}	repair ratio
T_{test}	test time
T_{repair}	repair time
$T_{net\ repair}$	time for repairing a defective pixel
W_T	window (i.e., time for test and repair)
Y_H	hard yield

Y_V virtual yield

A general calibration process in digital x-ray systems considered in this work is shown in Figure (2.2).

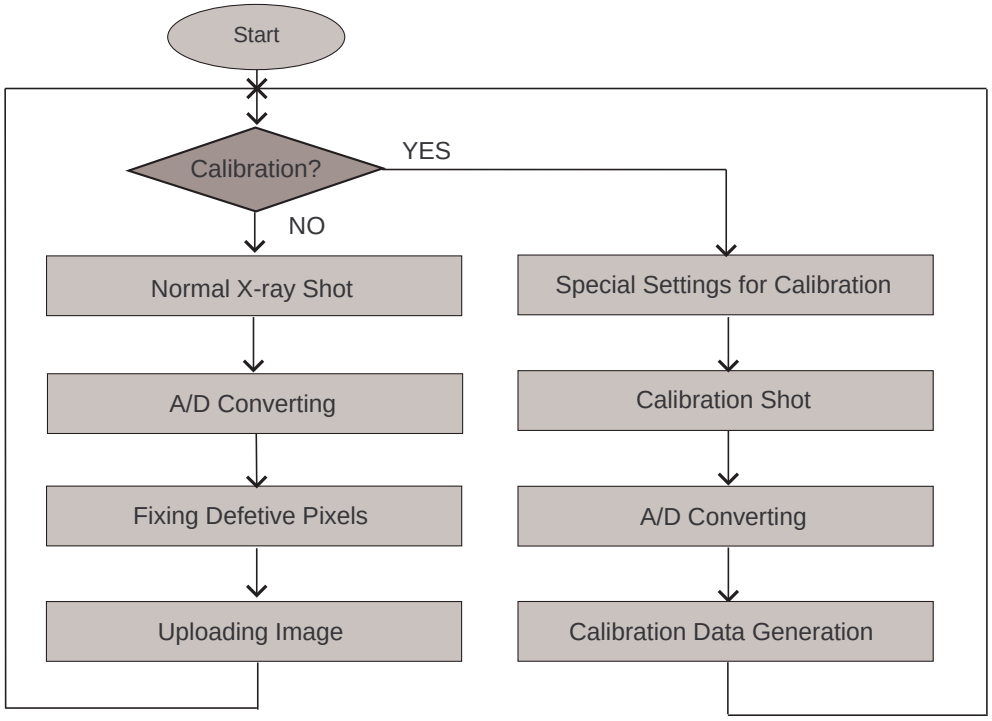

Figure 2.2: Flow Chart of the Calibration CCD System

Based on the reference calibration process shown in Figure (2.2), the main characteristics of the proposed soft-repair process are summarized as follows.

1. The hard-defects on the pixels on CCD is assumed to follow the Poisson distribution (i.e., $e^{-\lambda t}$). Note that clustered defects are not considered in this work.

2. It is assumed that only CCD contains defective pixels (i.e., dead pixels or hard-defects), and all other components (i.e., the A/D converter, the frame memory and the flash memory) are assumed to be defect-free.

3. Without loss of generality, it is also assumed that the defective pixels are prop-

agated from the CCD to the frame memory (i.e., soft-defects) through the A/D converter.

In this work, a simple mean filter as a criterion is used as shown in Figure (2.3).

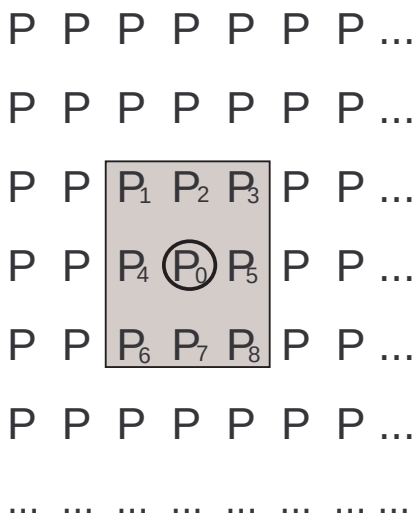

Figure 2.3: an example of 3×3 Filter

The proposed soft-test equation is given as follows.

$$\left| \frac{\sum_{k=1}^{N} P(k)}{N} - P(0) \right| \leq C \tag{2.1}$$

where $P(1) \cdots P(N)$ are the surrounding pixels of the tested pixel $P(0)$. The constant C is the threshold for determining whether it is defective or not in testing (e.g., 10%). This means the average value and the tested pixel value have almost same value. If Equation (2.1) holds, then the tested pixel is diagnosed as normal, otherwise it is a defective pixel. It indicates that the tested pixel is too bright or too dark compared to its neighboring pixels. Actually, only a defective pixel cannot be too much bright or dark than their neighboring pixels because of the Gaussian effect (i.e., each nine pixel contains each other's shading information).

After testing and repair process completed, the controller updates the noise history data map in the cache (i.e., non-volatile memory such as flash memory or E^2PROM).

The proposed noise history data map caching technique allows for at-speed repair with minimal overhead as shown in soft-test/repair cycles in Figure (2.4).

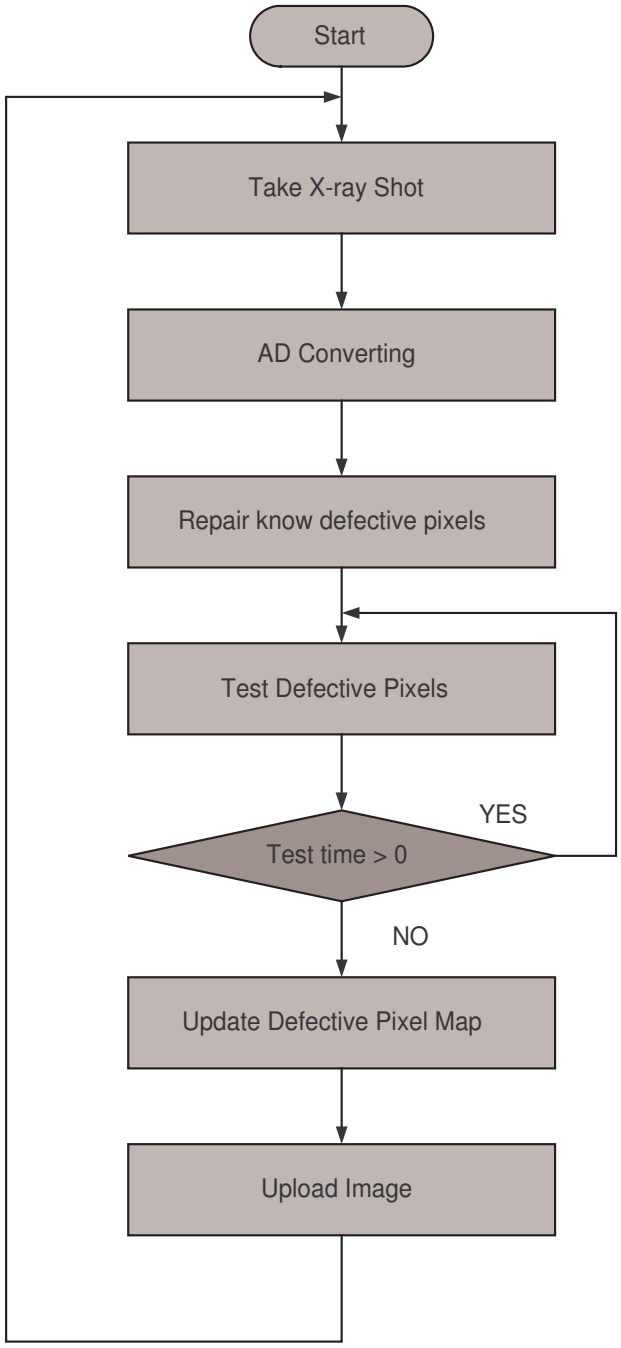

Figure 2.4: Flow Chart of Proposed the Caching CCD System

Equation (2.1) may not effectively take into account some defective pixels if they

are adjacent to pixels of similar gray-scale colors. Since different input images are to be stored and processed in the frame memory at each test cycle successively, the defective pixels, in general, can be detected within a certain finite number of test/repair cycles.

There are generally three possible failure modes such as low sensitivity, stuck low, and stuck high [16]. On the frame memory, defective pixels are relatively brighter or darker to result in relatively larger or smaller digitized data words compared to its neighboring pixels, which can be used for testing purpose.

Each pixel on the frame memory can be cached in two bits of flash memory. The states of caching a pixel on the flash memory can be defined as follows.

1. 00 state : stuck low (i.e., F_{sl})

   Ex) Photodiode shorted, gate to photodiode path cut, transistor stuck off

2. 01 state : low sensitivity (i.e., F_{ls})

   Ex) something covered part on photodiode, leakage in the photodiode, poor transfer characteristic of the transistor, etc

3. 10 state : stuck high (i.e., F_{sh})

   Ex) Photodiode always charged because of the malfunction of flushing circuit, transistor stuck on

4. 11 state : high sensitive (i.e., F_{hs})

   Ex) bad lens above the part on photodiode, too high gain of the transistor, etc.

The co-relation between each type of defective pixels and the total number of defective pixels, i.e. F_{fault}, can be defined as follows.

$$F_{fault} = F_{sl} + F_{ls} + F_{sh} + F_{hs} \tag{2.2}$$

The detection approaches and threshold equations for different type of defective pixel can be shown as follows.

1. 00 state: the stuck low pixels can be detected by the following two equations:

$$\left|\frac{\sum_{k=1}^{N} P(k)}{N}\right| \geq C_{011} \tag{2.3}$$

$$P(0) \leq C_{012} \tag{2.4}$$

where C_{011} and C_{012} are 50% and 10% respectively. This means that the stuck low pixels displays near zero range yet the average value displays more than 50% of the range. The constant value could be changed smaller value for tight detection. Basically, this constant value depends on the characteristic of system. If both Equation (2.3) and (2.4) hold, the pixel can be categorized as a stuck low pixel.

2. 01 and 11 state: low and high sensitive pixels can be detected by the following equation.

$$\left|\frac{\sum_{k=1}^{N} P(k)}{N} - P(0)\right| \geq C \tag{2.5}$$

where $C = 10\%$. 10% means 10% of the maximum digital value converted from A/D converter, (e.g. in case of 16 bit A/D converter, the 10% is 65535/10). This means that a low sensitive pixel displays out of the range of the average value over 10% tolerance. This constant value depends on the characteristic of system. If Equation (2.5) holds, then the pixel can be categorized as a low sensitive pixel.

3. 10 state: the stuck high pixels can be detected by the following equation.

$$\left|\frac{\sum_{k=1}^{N} P(k)}{N}\right| \leq C_{101} \tag{2.6}$$

$$P(0) \geq C_{102} \tag{2.7}$$

where the reference C_{101} and C_{102} are 50% and 90% respectively. The constant value can be varied from the give value depending on the system and quality

level. If both Equation (2.6) and (2.7) hold, then the pixel can be tested as a stuck high pixel.

Stuck low and stuck high pixels (i.e., State 00 and 10) can be repaired by replacing the defective pixel values by using the following equation. Since a defective pixel does not have any repair information, the defective pixel value is to be replaced by the average value of its neighboring pixel values.

$$P(0) = \frac{\sum_{k=1}^{N} P(k)}{N} \tag{2.8}$$

Note that the repair for a defective pixel defect of the state 01 depends on how much the pixel is insensitive. Thus, the following equation can be used to take into account the insensitivity.

$$P(0) = (1-p) \cdot \frac{\sum_{k=1}^{N} P(k)}{N} + P(0) \tag{2.9}$$

where p ($0 \leq p \leq 1$) is the insensitivity ratio of the defective pixel under test. The insensitivity ratio p can be defined as following equation.

$$p = \frac{P(0)}{\frac{\sum_{k=1}^{N} P(k)}{N}}$$

where the denominator ($\frac{\sum_{k=1}^{N} P(k)}{N}$) is the reference value.

The proposed CCD soft-testing/repair process scans for the soft-defects on the frame memory for a certain amount of time (i.e., referred to as T_{test}). The proposed soft-test/repair process repeats as many times as the total number of pixels within a temporal window of the process (i.e., within time T_{test} in Equation (2.10)). The pixels on the frame memory detected as soft-defects are repaired, and then the locations are cached and accumulated in the flash memory. The time for each test/repair process cycle is referred to as *window* (W_T), and can be expressed as follows.

$$W_T = T_{test} + T_{repair} \tag{2.10}$$

where T_{test} is the time for testing and detecting the defective pixels and T_{repair} is the time for repairing defective pixels. Within a certain number of test/repair cycles, all pixels will be tested (and repaired, if needed). If the system capacity allows, it can test and repair all pixels in one cycle (i.e., if W_T is long enough to test and repair all pixels captured and stored on the frame memory).

The image data is stored in the frame memory, pixel by pixel. D_n is the number of defective pixels propagated from the CCD at the n_{th} test/repair cycle, and can be calculated as follows.

$$D_n = D_T \cdot {r_{defect}}^{n-1} \tag{2.11}$$

where D_T is the total number of soft-defects hit on the frame memory, and r_{defect} is the decrease rate of D_n after each repair cycle. Since D_T is the total number of defective pixels, the following equation can be derived as well.

$$D_T = D_n + R_n \tag{2.12}$$

where R_n is the number of repaired pixels which are detected by the soft-test, and D_T is a constant assumed to be a known characteristic of the CCD. On the other hand, F_{test} is the number of pixels that can be tested within the test time T_{test}, and W_T is the window size (i.e., $T_{repair} + T_{test}$). Also, the number of defective pixels (i.e., F_{fault}) can be expressed as follows.

$$F_{fault} = F_{test} \cdot (1 - Y_H) \tag{2.13}$$

Therefore, the F_{repair} can be expressed by dividing T_{repair} by $T_{net\ repair}$ as follows.

$$F_{repair} = \frac{W_T - T_{test}}{T_{net\ repair}} \tag{2.14}$$

where $T_{net\ repair}$ is the repair time for a defective pixel, and F_{repair} is the number of repaired pixels that can be repaired within $W_T - T_{test}$. From Equation (2.13) and

(2.14), the repair ratio (i.e., $r_{repair}(n)$) can be expressed as follows.

$$r_{repair}(n) = \frac{min(F_{repair}, F_{fault})}{F_{fault}} \quad (2.15)$$

$$= \frac{min(F_{repair}, F_{fault})}{F_{test} \cdot (1 - Y_H)} \quad (2.16)$$

The decrease ratio r_{defect} can be defined as follows.

$$r_{defect} = 1 - r_{repair}(n) \quad (2.17)$$

Then, the number of repaired pixels after n cycles, R_n of the CCD system can be given as follows.

$$R_n = \sum_{k=1}^{n}(D_{k-1} - D_k) \quad (2.18)$$

$$= (D_T - D_T \cdot r_{defect}) + (D_T \cdot r_{defect} - D_T \cdot {r_{defect}}^2) + (D_T \cdot {r_{defect}}^2 - D_T \cdot {r_{defect}}^3)$$

$$+ \cdots + (D_T \cdot {r_{defect}}^n - D_T \cdot {r_{defect}}^{n-1}) \quad (2.19)$$

$$= D_T(1 - {r_{defect}}^{n-1}) \quad (2.20)$$

Also, Equation (2.20) can be derived from Equation (2.11) and (2.12). By definition of normalization, $\overline{R}_n$ can be formulated as follows.

$$\overline{R}_n = \frac{Number\ of\ Repaired\ Pixel}{Total\ Number\ of\ defective\ Pixel} \quad (2.21)$$

$$= \frac{D_T(1 - {r_{defect}}^{n-1})}{D_T} \quad (2.22)$$

$$= 1 - {r_{defect}}^{n-1} \quad (2.23)$$

From Equation (2.17) and (2.16), the repair rate can be calculated as follows.

$$\overline{R}_n = 1 - \left[1 - \frac{min(F_{repair}, F_{fault})}{F_{test} \cdot (1 - Y_H)}\right]^{n-1} \quad (2.24)$$

$$= 1 - \left[1 - \frac{min(F_{repair}, F_{sl} + F_{ls} + F_{sh} + F_{hs})}{F_{test} \cdot (1 - Y_H)}\right]^{n-1} \quad (2.25)$$

Therefore, the virtual yield Y_V is given by

$$Y_V(n) = Y_H + (1 - Y_H) \cdot C_{st} \cdot \overline{R_n} \quad (2.26)$$

$$= Y_H + (1 - Y_H) \cdot C_{st} \cdot (1 - {r_{defect}}^{n-1}) \quad (2.27)$$

where Y_H is the CCD Hard Yield, and C_{st} is the Soft-Test Coverage (i.e., the rate of detecting defective pixels out of the total number of actual defective pixels). Therefore, from Equation (2.17) and (2.16), the overall virtual yield can be re-expressed as follows.

$$\begin{aligned} Y_V(n) &= Y_H + (1 - Y_H) \cdot C_{st} \cdot \left[1 - \left(1 - \frac{min(F_{repair}, F_{fault})}{F_{test} \cdot (1 - Y_H)} \right)^{n-1} \right] \quad (2.28) \\ &= Y_H + (1 - Y_H) \cdot \\ &\quad C_{st} \cdot \left[1 - \left(1 - \frac{min(F_{repair}, F_{sl} + F_{ls} + F_{sh} + F_{hs})}{F_{test} \cdot (1 - Y_H)} \right)^{n-1} \right] \quad (2.29) \end{aligned}$$

2.4 Parametric Analysis

In this section, the effect of the proposed soft-test/repair process on the virtual yield of CCD will be evaluated through numerical simulations based on Y_V derived in the previous section.

CCDs of 6 Mega pixels (2K×3K) are assumed in this simulation. Three CCDs containing 10%, 7% and 3% defected pixels are considered, respectively (i.e., 10% is $(2048 \times 3072)/10$). From Equation (2.23), the repair rates are calculated as shown in the Figures (2.5), (2.7), and (2.9). $Y_H = 90\%$, $Y_H = 93\%$ and $Y_H = 97\%$ CCDs are used for Figures (2.5), (2.7), and (2.9), respectively. Also, the CCDs of $Y_H = 90\%$, $Y_H = 93\%$ and $Y_H = 97\%$ are used for Figures (2.6), (2.8), and (2.10), respectively based on Equation (2.27). Note that three CCDs with 90%, 93% and 97% hard yields are also considered for the purpose of comparison.

For the simulation, we assumed that the large window size is given by the time to scan and fix defective pixels for 30% of total pixel (i.e., 2048×3072). In the same way, the medium window size is given for 20% and the small window size is given for 10%.

A very *High Yield* (i.e, 99.5%) CCD is adopted for the purpose of comparison in Figures (2.6), (2.8), and (2.10). Note that the conventional method uses a defective

pixel map on PC or workstation not in hardware level. So, we compare proposed soft-test repair approach with very High Yield(99.5%) without repair.

By comparing the results of Figures (2.5)-(2.10), the following observations can be drawn.

1. The proposed soft-test/repair approach is beginning to outperform the conventional calibration approach after a certain number of test/repair cycles in terms of virtual yield. In Figure (2.9), the repair rate approaches 100% at n=5 with large window size. Therefore, just a certain number of initial image shots are needed to repair the defective pixels building a complete noise history data map on the cache. Thereafter, it will be just a matter of preprocessing incoming image data with reference to the complete noise history data map on the cache. In Figure (2.5), the convergence to 100% is delayed to $n = 20$ with large window size. The increase rate of the repair rate is determined by r_{defect} based on Equation (2.23).

2. The proposed approach achieves high Virtual Yield after a certain point compared to the conventional approach regardless of the Hard-Yield and expensive CCDs being used in the conventional approach, as shown in Figures (2.6), (2.8), and (2.10) in which the CCDs have $Y_H = 90\%$, $Y_H = 93\%$ and $Y_H = 97\%$, respectively. In Figure (2.6), the virtual yield of the proposed repair process with small window size is starting to exceed the repair rate of high yield with large window at n=8. After the number of repair cycles exceeds n=8, the virtual yield converges to 100%. It is higher than the high yield CCD (i.e., 99.5%) and improved by 10%. This is very significant virtual yield enhancement by all means, which is very desirable in high resolution digital x-ray systems.

3. In Figures (2.5), (2.7), and (2.9), the hard yield Y_H affects the repair rate. All the yields approach up to 100% regardless of the low initial hard yields.

However, this does not mean that any low hard yield such as $Y_H = 30\%$ can virtually be enhanced to 100%. CCDs may or may not have reparable defects (i.e., not clustered defects). Actually, the criterion of acceptable image depends on the requirement of the system such as the resolution of system (i.e., lpm (Line Per Millimeter) or dpi (Dot Per Inch)), since some systems cannot tolerate clustered defective pixels. However, most medical systems use the binning mode (i.e., combining the pixel by hardware or software) for gathering more photons and increasing the image quality.

4. In Figures (2.5), (2.7), and (2.9), the increase rate of the repair rate is shown and it depends on the window size. The higher hard-yield CCD quickly approaches 100% repair rate. However, even the small window size can achieve 100% repair rate just in a few more repair cycles. From this result, even if new defective pixels hit, the repair rate can achieve 100% by using the proposed soft-test/repair process. In practice, a CCD price depends on its grade which is determined by the number of defective pixels. Therefore, this approach can reduce the cost of products while increasing the image quality.

5. The resulting virtual yields are shown in Figures (2.6), (2.8), (2.10) based on Equation (2.27). The hard yields determine the initial virtual yields. After a certain number of repair cycles, all the virtual yields converge to 100%.

From the results and findings shown so far, it can be concluded that the hard-defects which mapped on the frame memory can be effectively repaired by the proposed soft-test/repair approach. Also, the repair rates and the virtual yields approach 100% in a small number of repair cycles. Furthermore, the proposed approach can enhance the repair rate as high as up to 100%, even though new defective pixels hit due to physical shocks or exposing to excessive x-ray.

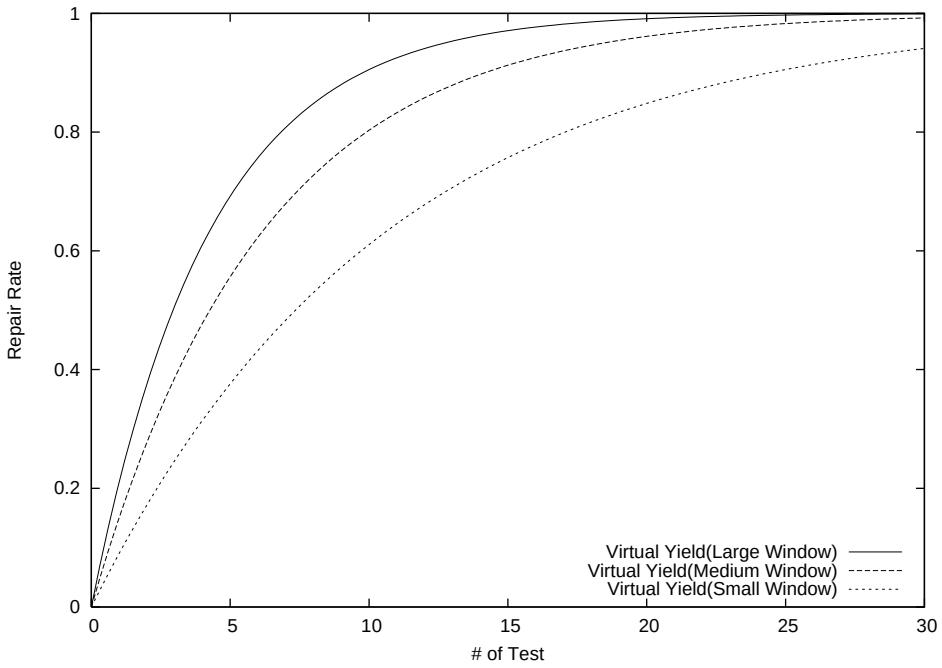

Figure 2.5: Repair Rate (Hard-Yield 90%)

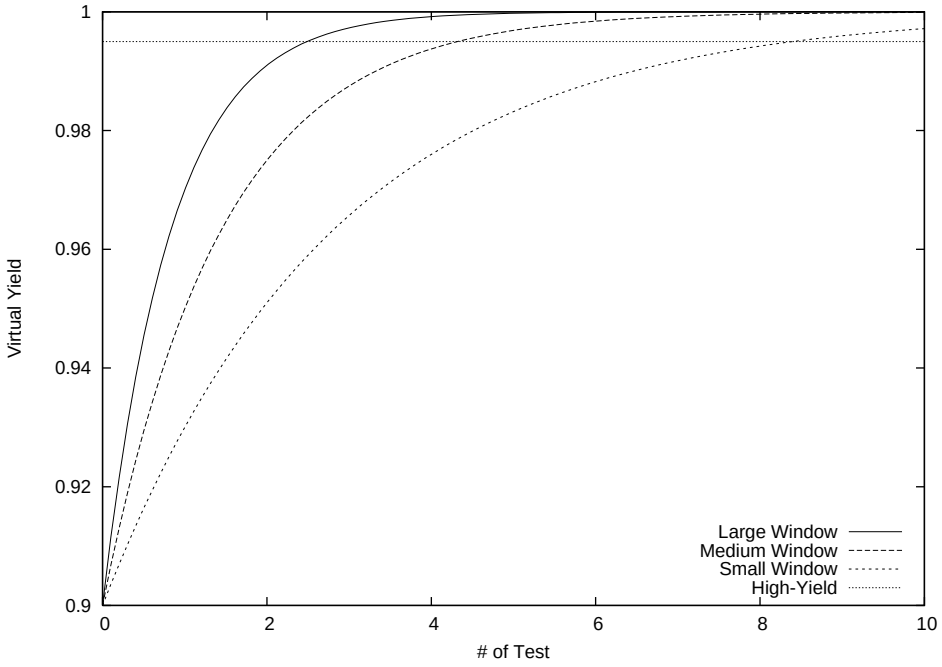

Figure 2.6: Virtual Yield (Hard-Yield 90%)

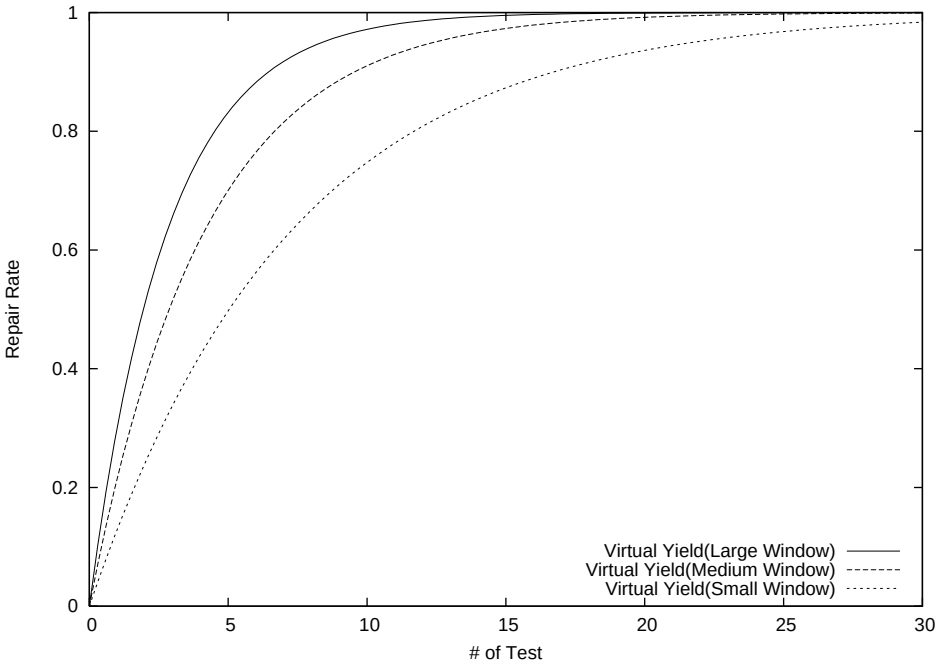

Figure 2.7: Repair Rate (Hard-Yield 93%)

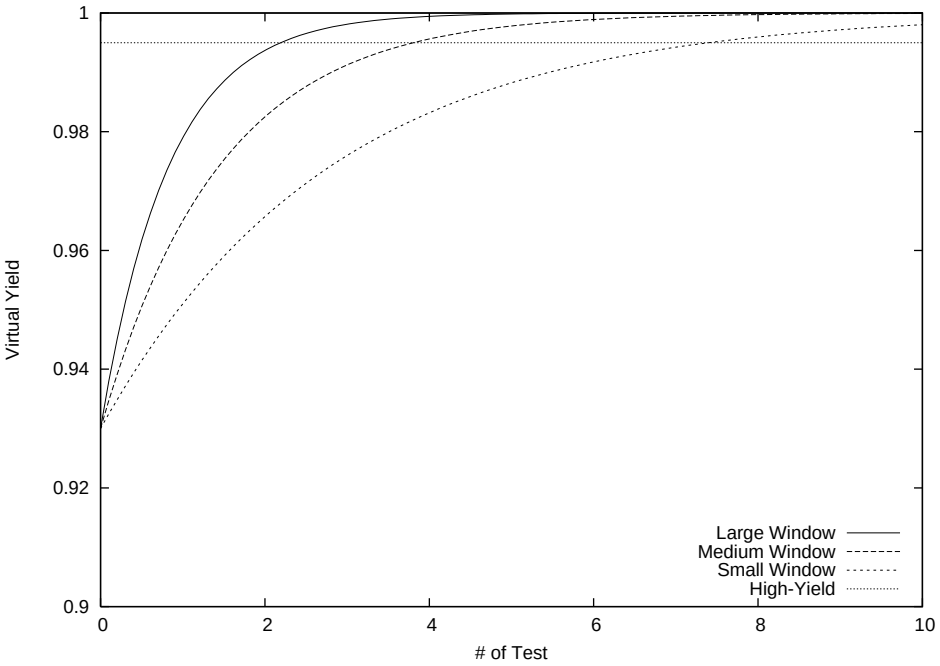

Figure 2.8: Virtual Yield (Hard-Yield 93%)

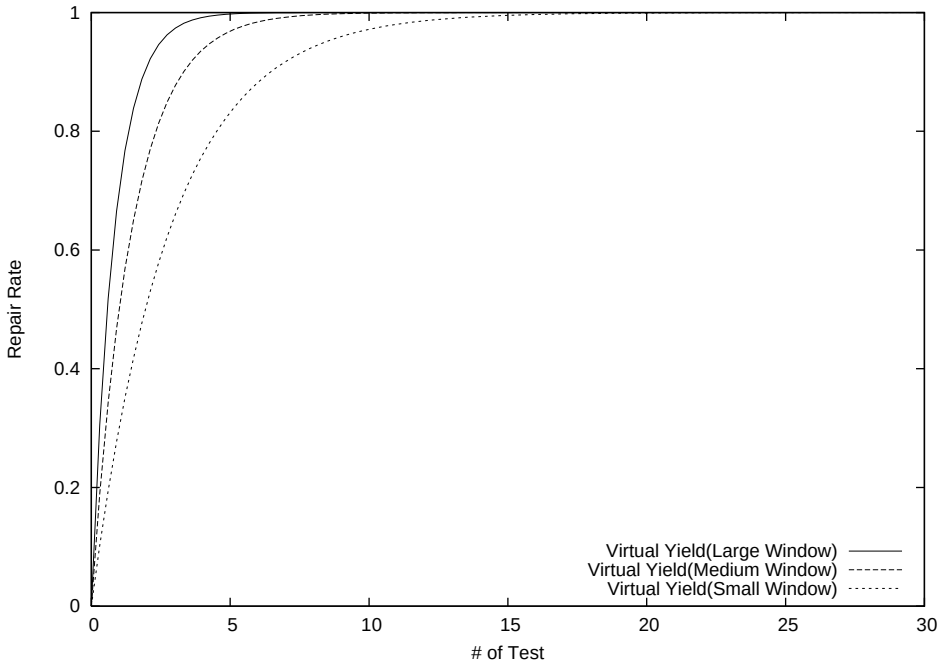

Figure 2.9: Repair Rate (Hard-Yield 97%)

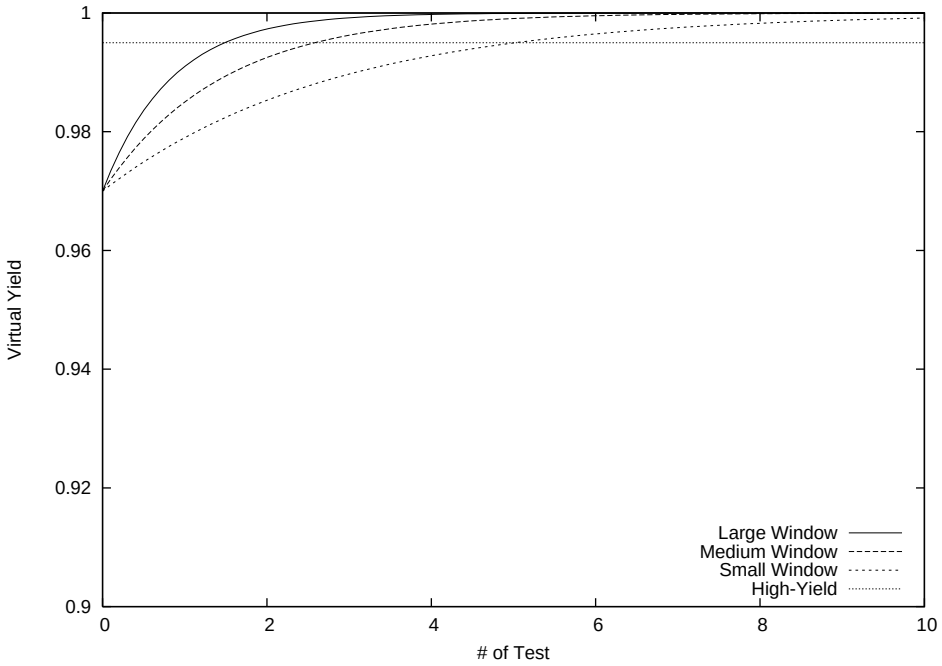

Figure 2.10: Virtual Yield (Hard-Yield 97%)

2.5 Discussion and Conclusions

This work has presented a soft-test/repair approach for CCD-based digital x-ray systems through sound establishment of a novel theoretical modeling and analysis of the proposed test/repair procedure. It has been revealed that the yield of the CCD is one of the most critical components affecting the QoS (Quality of Service) of a digital X-ray system. There are two possible solutions to cope with the defective pixel problem in CCD; one is the hard-repair approach and another is the proposed soft-repair approach. The proposed soft-repair approach is to circumvent defective pixels at the digitized image level; thereby it is inexpensive to practice and on-line repair can be done for non-interrupted service. It tests the images to find the defective pixels and filter the defects at the frame memory level, and caches them in a flash memory in the controller for future use. The controller cache keeps accumulating all the noise coordinates, and preprocesses the incoming image data from the A/D converter by repairing them. The algorithms can be implemented on hardware level (i.e., on the controller) to speed up the process. Unlike the calibration approaches shown in [9, 10], the proposed approach stores the noise history map dynamically on hardware level and always keeps the up-to-date data within proper window size. Numerical simulations have revealed that the proposed soft/hard approach using the proposed soft-testing and repair process will outperform the conventional hard approach after a certain break-even point in terms of virtual yield, thereby ultimately realizing high QoS of digital x-ray systems.

In the following Chapter 3, clustered fault models of CCDs and repair methods will be studied with simulation. In Chapter 4, practical designs and implementations regarding soft-test/repair will be presented. In addition, various parametric simulations such as testing and repair time analysis and parallel testing processing will be

presented in verilog HDL level.

CHAPTER 3

CCD Clustered fault

3.1 Introduction

Many applications of digital imaging technology can be found in such system as digital cameras, digital camcorders and digital x-ray diagnosis systems to mention a few. Among the currently available digital optical sensing devices, CCDs and APSs (Active Pixel Sensors) are the two most commonly used ones. In practice, pixels on such digital image sensing devices may contain defective pixels due to various causes such as improper fabrication, excessive exposure to light and radiation, and aging of sensing element. Therefore, in high-resolution digital imaging sensors, defect and fault tolerance is stringently required to assure quality of service.

Extensive works have been conducted on defect modeling, testing, and repair in semiconductor devices which in general, 2-dimensional array architecture can be assumed to model such devices. Traditionally, most of the techniques employ a method of replacement of faulty cells or blocks with spare cells or blocks, respectively. However, the traditional technique cannot be effectively employed for image sensing devices for testing and repair. No displacement is allowed for CCD pixels because each pixel has a unique x-y coordinate that cannot be backed up or replaced in case of a defect. Thus, the traditional redundancy-based repair techniques for memory systems cannot be applied to digital image sensing devices.

Our previous work [12] for testing and repairing defective CCD pixels is an efficient and practical method for testing and repairing faulty CCDs. There also have been a few hardware-based methods proposed to design a reliable CCD based on digital

signal processing system [14, 15, 16, 9]. Digital cameras employ high resolution color CCD for high resolution image sensing. [9] proposed that defects on color CCD can be detected by checking which color is corrupted among the three colors (i.e. red, green and blue), and repaired by replacing a faulty color pixel with a spare CCD pixel provided. These hardware redundancy-based approaches rely on spare row and column-replacement of CCD pixels, and are thus impractical to be practiced for the displacement of image sensing pixels and the additional cost to the already expensive CCDs [16, 9].

Unlike traditional test/repair methods, the proposed soft-test/repair of CCDs is performed by software yet targetting at hardware-defect/fault testing/repair. The overall yield enhancement of CCD has been demonstrated by the soft-test/repair methods with efficiency and effectiveness from our previous work [12].

In this work, a propagation of the hardware-defects/faults (i.e., defective pixels) from CCD to frame memory is modeled based on practical *clustered defective pixels* in comparison with the single defect/fault model in our previous work [12, 17, 13]. Clustered defect/fault model for testing and repair process is to be considered for realistic and practical faulty pixels. The objective of this work is to propose a testing and repair method for CCD imaging system with inability of on-device repair (i.e., off-device fault tolerance) under clustered CCD pixel defect/fault model. To effectively capture the on-device pixel defects and faults off the device intact, a novel propagation-tracing method of the defects and faults is proposed. The efficiency and effectiveness of the proposed methods is demonstrated by enhancement of yield (i.e., soft-yield) under clustered defect/fault model as well as single fault model.

This work has been partially presented in [17].

This work is organized as follows. In the next section (Section 3.2), previous works are reviewed, and basic principles of the proposed approach are introduced. In Section 3.3, the proposed soft-testing and repair process for single and clustered

faulty pixels is evaluated. In Section 3.4, parametric simulations with respect to CCD yield, soft-repair rate are shown. Then, conclusions and discussions are presented in Section 3.5.

3.2 Review and Preliminaries

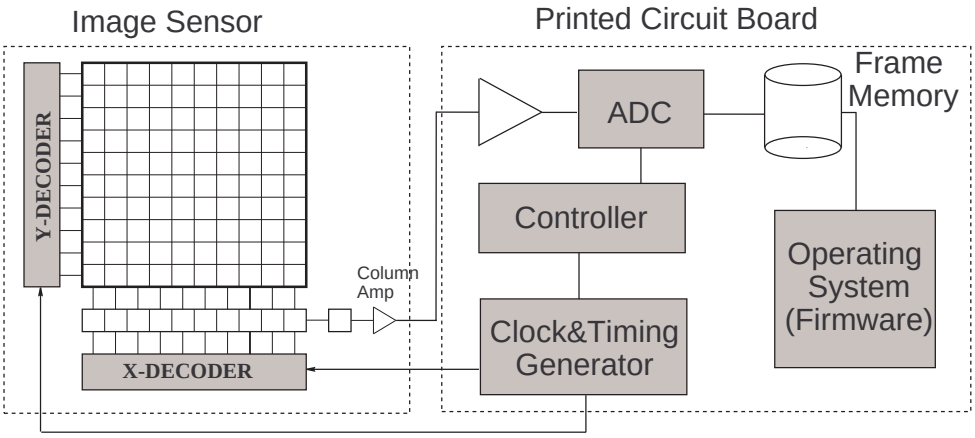

Figure 3.1: Block Diagram of CCD System

In this work, a CCD imaging system will be modeled considering not only single faults but also clustered faults. CCDs are the most widespread image sensors for digital imaging systems and are becoming more prevalent these days, because of its many advantages such as high-resolution, manufacturability and image quality, to mention a few. Unfortunately, CCDs are not free from hardware faults like other semiconductors and the faults could increase the overall cost (i.e., both manufacturing and maintenance costs). Imperfect fabrication and improper processing may induce defects (referred to as *hard-defects*) on the photo-sensitive pixels and supporting system components in CCDs. In [15], the main causes of CCD hard-defects are categorized as follows.

1. Failure of row/column pixels (either line or readout/control transistors/circuit).
2. Failure of row select/reset shift register.
3. Failure of column sense amplifiers.
4. Failure of A/D converter.
5. Failure of buffers.

6. Failure of read-out/reset transistors on each photo-diode.

In practice, all the defects of the above-mentioned types affect the quality of the raw image data on the frame memory, since the hard-defects that propagated all the way from the CCD to the frame memory through the A/D converter as shown in Figure (3.1). The effect of a hard-defect observed on the frame memory is referred to as *soft-defect*. Notably, a soft-defective pixel on the frame memory usually shows an abnormal value compared to its neighboring pixel values. Without loss of generality, one-on-one correspondence between a hard-defect on the CCD and a soft-defect on the frame memory can be assumed, unless other component failures than CCD failures are taken into account. In this context, it is feasible to test and repair (i.e. soft-testing/repair) CCD hard-defects on soft memory-mapped level in the form of soft-defects on the frame memory.

From our previous work [12], following equations were derived.

$$\begin{aligned} Y_V(n) &= Y_H + (1 - Y_H) \cdot \\ &\quad C_{st} \cdot \left[1 - \left(1 - \frac{min(F_{repair}, F_{fault})}{F_{test} \cdot (1 - Y_H)} \right)^{n-1} \right] \qquad (3.1) \\ &= Y_H + (1 - Y_H) \cdot C_{st} \cdot \\ &\quad \left[1 - \left(1 - \frac{min(F_{repair}, F_{sl} + F_{ls} + F_{sh} + F_{hs})}{F_{test} \cdot (1 - Y_H)} \right)^{n-1} \right] \qquad (3.2) \end{aligned}$$

where Y_H is the CCD Hard Yield, Y_V is the CCD virtual Yield, C_{st} is the Soft-Test Coverage, F_{test} is the number of tested pixels and F_{repair} is the number of repaired pixels. F_{sl}, F_{ls}, F_{sh}, and F_{hs} are the number of stuck low pixels, the number of low sensitive pixels, the number of stuck high pixels, and the number of stuck high sensitive pixels, respectively.

The previous model just handled with single faults. Hence, in case of clustered faults, it is indispensable to consider clustered fault model for more precise modeling. Next section will describe the proposed soft-test/repair model extended to clustered

fault model.

3.3 The Proposed Soft-Test/Repair Model

Each pixel of image sensors can be modeled as an electron well in Figure (3.2) in general. Photons (i.e. light) are accumulated in electron well when it light come through the window. By electric field, the potential wells are controlled.

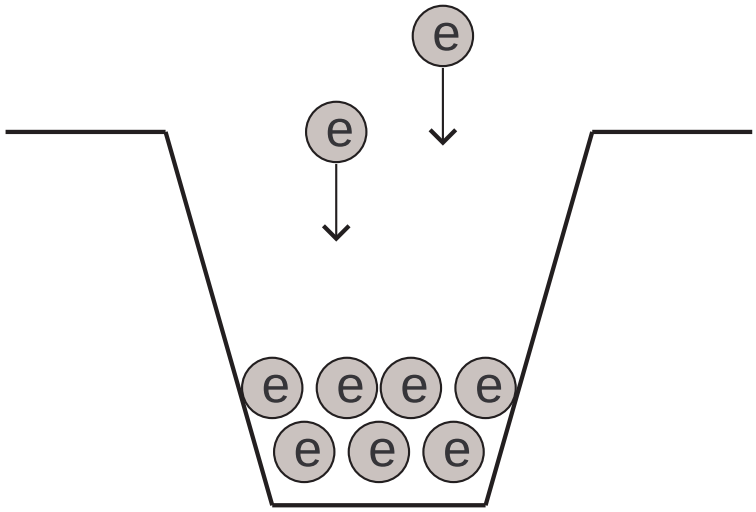

Figure 3.2: Electron (Potential) Well

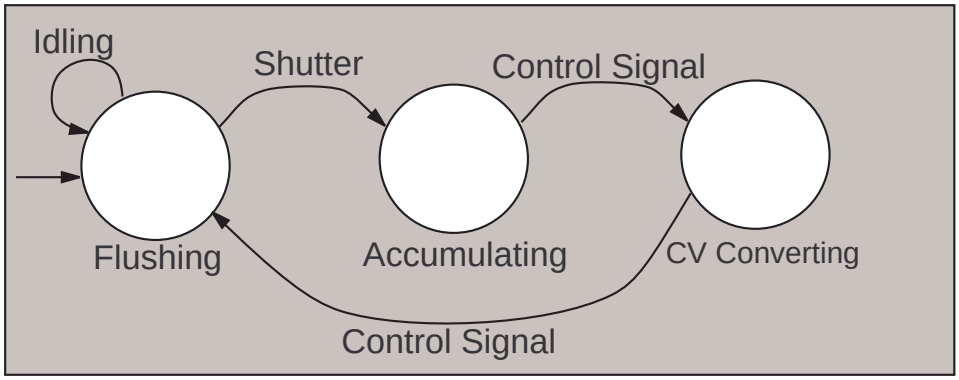

Figure 3.3: State Diagram of CCD

In general, CCD operation can be modeled as shown in Figure (3.3). Initially, CCD is in the flushing state where it is discharging electrons before accumulating for

next shot. During the flushing state, CCD cannot accumulate electrons as shown in Figure (3.2). Then, by electronic or mechanical shutter operation, the electrons are being accumulated in an electron (potential) well during exposure time. The number of accumulated electrons, Q, can be expressed as follows.

$$Q(x, y, t) = \int_0^t \Big[n(x, y, t) \cdot e \Big] dt \tag{3.3}$$

where $n(x, y, t)$ is the number of electrons at each pixel, e is a unit electron (photon), x and y are the coordinates of the electronic well, and t is the exposure time manipulated by the shutter (from 0 to t). Once the exposure is completed, the charged electrons are transfer to the column amplifier from the electron wells (i.e., pixels) by the controller as shown in Figure (3.1). The charged electrons in each pixel are then converted to a voltage value by column amplifier as follows.

$$v(x, y) = Q(x, y, t) \cdot A_c \tag{3.4}$$

where $v(x, y)$ is the voltage (i.e., analog) value of a pixel (i.e., electron well), and A_c is the gain of charge-to-voltage converter. By the ADC (Analog to Digital Converter), each pixel voltage value is converted to a digital value $V(x, y)$ as follows.

$$V(x, y) = v(x, y) \cdot A_d \tag{3.5}$$

where A_d is the analog to digital gain determined by the characteristics of the image sensors. Note that $v(x, y)$ is a floating number and $V(x, y)$ is an integer number. From Equation (3.3),(3.4) and (3.5), the final digitized voltage value can be derived as followings.

$$V(x, y) = A_c \cdot A_d \cdot \int_0^t \Big[n(x, y, t) \cdot e \Big] dt \tag{3.6}$$

$V(x, y)$ of each pixel is propagated to and then stored in the frame memory as shown in Figure (3.1). $V(x, y)$ can be characterized into five sets.

1. $Q_{sh} = \{V|V$ is high-stuck-pixels$\}$

   A high-stuck-pixel cannot sense the amount of electrons and always display high value even for dark light.

2. $Q_{sl} = \{V|V$ is low-stuck-pixels$\}$

   A low-stuck-pixel cannot sense the amount of electrons and always display low value even for bright light.

3. $Q_{hs} = \{V|V$ is over-sensitive-pixels$\}$

   A over-sensitive-pixel can sense the amount of electrons but too sensitive (i.e., out of tolerance). In this case, compare to other normal pixels, it has always higher value than normal pixel.

4. $Q_{ls} = \{V|V$is under-sensitive-pixels$\}$

   A under-sensitive-pixel can sense the amount of electrons but less sensitive (i.e., out of tolerance). In this case, compare to other normal pixels, it has always lower value than normal pixel.

5. $Q_n = \{V|V$ is normal pixel$\}$

   A normal pixel can sense exact (i.e., within tolerance) amount of electrons.

Each set of pixels can be tested as follows.

1. Q_{sh} : Test Input : No light to CCD and take a shot.

   Test Output : Raw Image

   All the pixel values V should be $min(V)$. Others can be classified as high-stuck-pixels in Figure (3.4). In the figure, only the high-stuck-pixels can clearly be decided. The found defective pixel map should be saved on non-volatile memory such as flash memory for later use.

2. Q_{sl} : Test Input : Use very bright light and take a shot.

   Test Output : Raw Image

All the pixel values V should be near $max(V)$. Others can be classified as low-stuck-pixels in Figure (3.5). In the figure, only the low-stuck-pixels can surely be decided. The found defective pixel map should be saved on non-volatile memory such as flash memory for later use.

3. Q_{hs} : Test Input : Use mid light and take a shot.

   Test Output : Raw Image

   In this case, the pixel value distribution should be like in Figure (3.6). For detecting over-sensitive-pixels, very high quality light source is needed such as parallel and even light. In the figure, the over-sensitive-pixel is out range, especially right bound, of the normal value. The found defective pixel map should be saved on non-volatile memory such as flash memory for later use.

4. Q_{ls} : Test Input : Use mid light and take a shot.

   Test Output : Raw Image

   In this case, the pixel value distribution should be like in Figure (3.6). For detecting under-sensitive-pixels, very high quality light source is needed such as parallel and even light. In the figure, the under-sensitive-pixel is out of range of the normal value. The found defective pixel map should be saved on non-volatile memory such as flash memory for later use.

5. Q_n : Test Input : Use mid light and take a shot.

   Test Output : Raw Image

   In this case, the pixel value distribution should be like in Figure (3.6). For detecting under-sensitive-pixels, very high quality light source is needed such as parallel and even light. In the figure, the window of normal value should be generally 10% of $(max(V) - min(V))$. It is depend on the light source and optical characteristics of CCD.

In addition, V(x,y) can be divided into two clustering categories.

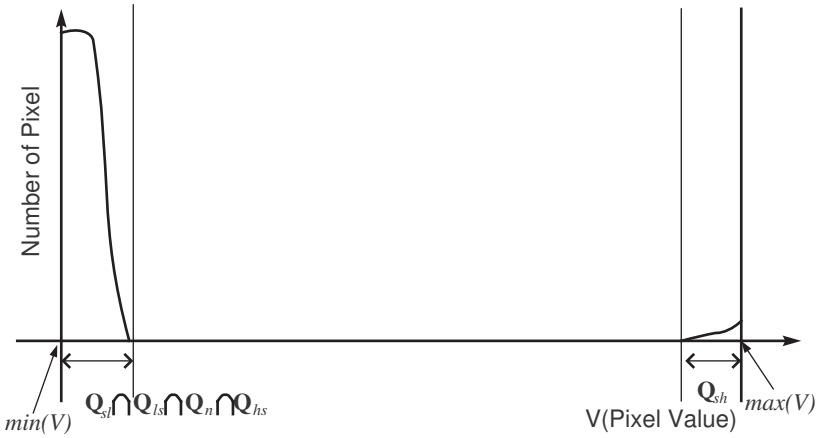

Figure 3.4: Distribution of CCD pixel values; Q_{sh} is separated.

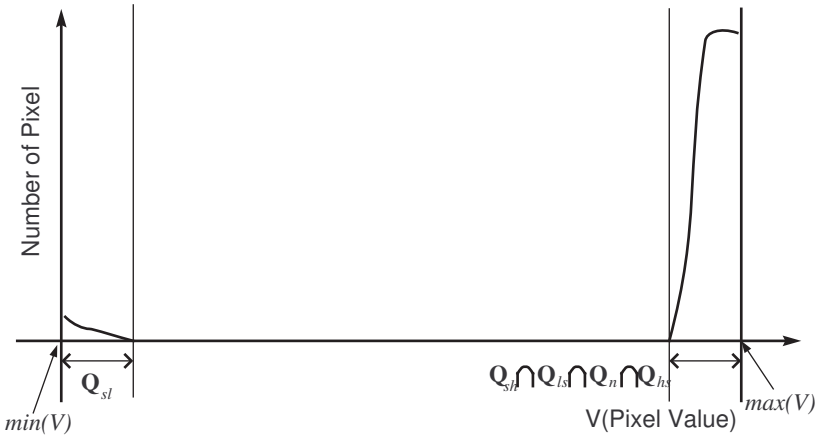

Figure 3.5: Distribution of CCD pixel values; Q_{sl} is separated.

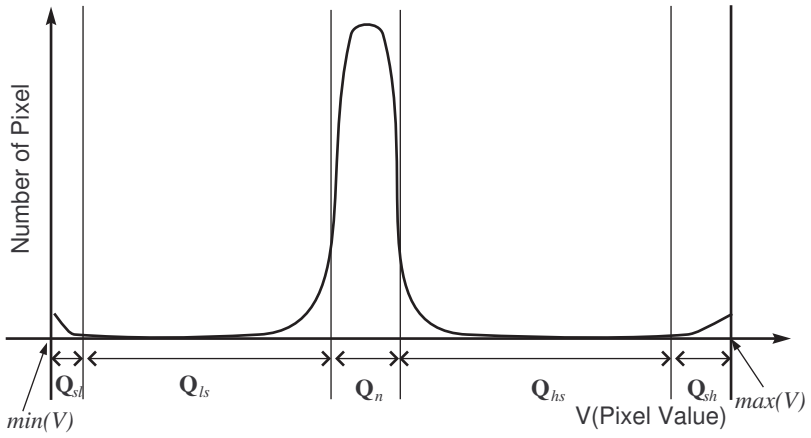

Figure 3.6: Distribution of CCD pixel values; all combined.

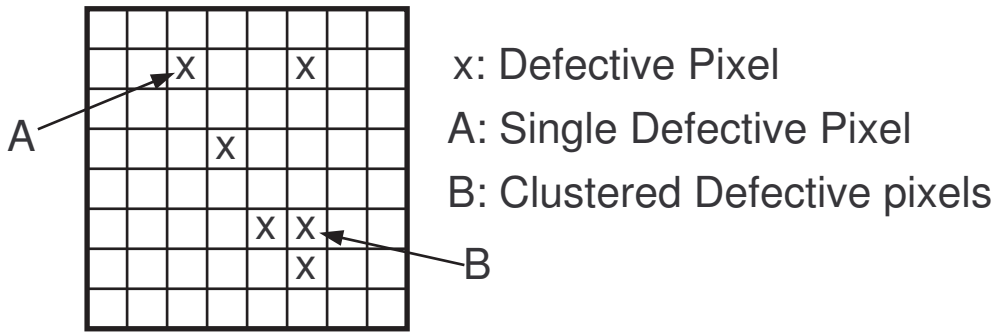

Figure 3.7: Clustered Fault Pixels and Single Fault Pixels

1. Clustered Fault : a pixel has any kind of functional fault and its adjacent pixels also have kinds of functional fault like label B in Figure (3.7).

2. Single Fault : a pixel has any kind of functional fault yet its neighboring pixels have no functional faults. In Figure (3.7), label A is an example.

It is important because clustered faults cannot be repaired perfectly.

From the union of functional and clustering categories, there will be four kinds of fault as follows.

$$Q_{sl} = Q_{sl,c} \cup Q_{sl,r} \tag{3.7}$$

$$Q_{sh} = Q_{sh,c} \cup Q_{sh,r} \tag{3.8}$$

$$Q_{ls} = Q_{ls,c} \cup Q_{ls,r} \tag{3.9}$$

$$Q_{hs} = Q_{hs,c} \cup Q_{hs,r} \tag{3.10}$$

$$\tag{3.11}$$

where $Q_{sl,c}$ is a set of low stuck and clustered pixels (i.e., each of pixel in the set of $Q_{sl,c}$ is not only a defective pixel but also having at least a neighboring defective pixel). The subscript c stands for clustered and r stands for single pixels. Theoretically, the following three equations can be formulated as follows.

$$Q_c = Q_{sl,c} \cup Q_{sh,c} \cup Q_{ls,c} \cup Q_{hs,c} \tag{3.12}$$

$$Q_r = Q_{sl,r} \cup Q_{sh,r} \cup Q_{ls,r} \cup Q_{hs,r} \tag{3.13}$$

$$Q = Q_c \cup Q_r \cup Q_n \tag{3.14}$$

From the definition of the yield, the hard yield Y_H can be expressed as follows.

$$Y_H = \frac{\int_{section Q_n} P(V)dV}{\int_{min(V)}^{max(V)} P(V)dV} \tag{3.15}$$

$$= 1 - \frac{|Q_{sl,c}| + |Q_{sh,c}| + |Q_{ls,c}| + |Q_{hs,c}|}{|Q|}$$

$$- \frac{|Q_{sl,r}| + |Q_{sh,r}| + |Q_{ls,r}| + |Q_{hs,r}|}{|Q|} \tag{3.16}$$

$$= 1 - \frac{|Q_c| + |Q_r|}{|Q|} \tag{3.17}$$

where P is the distribution of pixel number.

Repair methods should be considered both the single and clustered faults. Followings are just for single fault repairing. Clustered faults will be explained later.

- Stuck-low and stuck-high pixels (i.e. Q_{sl} and Q_{sh}) can be repaired by replacing the defective pixel scale values. Since a defective pixel does not have any significant information, the defective pixel value is to be replaced by the average value of its neighboring pixel values.

$$V(0) = \frac{\sum_{k=1}^{N} V(k)}{N} \tag{3.18}$$

  where $V(0)$ is the center pixel which is tested, the $\sum_{k=1}^{N} V(k)$ means the sum of neighboring pixel and the N is the number of neighboring pixel in Figure (3.8).

- The repair for a defective pixel of in Q_{hs} and Q_{ls} depends on how much the pixel is insensitive or oversensitive. Thus, the following equation can be used to take into account the insensitivity and oversensitive.

$$V(0) = p \cdot V(0) \tag{3.19}$$

  where p is a gain factor for fixing pixels in Q_{hs} and Q_{ls}. To fix the pixel in Q_{hs} and Q_{ls}, the gain factor has to be stored in memory in advance.

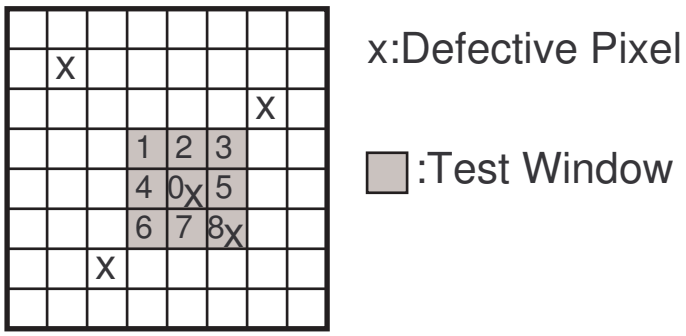

Figure 3.8: Repairing of Clustered Fault

Repair of the clustered fault should be considered the neighboring pixels whether they are defective or not. Otherwise, the repairing results in diffusion of the defective area because of fake repair. In Figure (3.8), the repairing pixel V(0) should not be replaced by Equation (3.18). Instead, it should be replaced by following equation.

$$V(0) = \frac{\sum_{k=1}^{8} V(k) - V(8)}{N-1} \tag{3.20}$$

To generalize this equation, it can be expressed as follows.

$$V(0) \quad = \quad \frac{\sum_{k=1}^{N} V(k) - \sum_{l}^{M} D(l)}{N-M} \tag{3.21}$$

where N is the number of pixel in testing area and M is the number of defective pixels in testing area. M is referred to as *Acceptance Level (AL)*. AL means how many defective pixels will be accepted for testing area. As see in Equation (3.21), M should not equal to N, which means the repairing pixel cannot be repaired from all defective pixels because no other pixels have any information about repairing pixel. Proper AL should be smaller than 4, which means at least half of the pixels in testing area are normal. Note that the defective pixel values (i.e., $D(l)$ is removed (i.e., subtracted) for preventing diffusion effect.

The soft yield Y_S can be derived as follows. Single defective pixels can be repaired by soft-repair method. Therefore, the single defective pixel repair ratio can be 1.

$$Y_S = \quad 1 - \frac{|Q_{sl,c}| \cdot (1 - R_{sl,c}) + |Q_{sh,c}| \cdot (1 - R_{sh,c})}{|Q|}$$

$$
\begin{aligned}
& - \frac{|Q_{hs,c}| \cdot (1 - R_{hs,c}) + |Q_{ls,c}| \cdot (1 - R_{ls,c})}{|Q|} \\
& - \frac{|Q_{sl,s}| \cdot (1 - R_{sl,s}) + |Q_{sh,s}| \cdot (1 - R_{sh,s})}{|Q|} \\
& - \frac{|Q_{ls,s}| \cdot (1 - R_{ls,s}) + |Q_{hs,s}| \cdot (1 - R_{hs,s})}{|Q|} \qquad (3.22) \\
= \quad & 1 - \frac{|Q_{sl,c}| \cdot (1 - R_{sl,c}) + |Q_{sh,c}| \cdot (1 - R_{sh,c})}{|Q|} \\
& - \frac{|Q_{ls,c}| \cdot (1 - R_{ls,c}) + |Q_{hs,c}| \cdot (1 - R_{hs,c})}{|Q|} \qquad (3.23) \\
= \quad & Y_H + \frac{|Q_s|}{|Q|} + \frac{|Q_{sl,c}| \cdot R_{sl,c} + |Q_{sh,c}| \cdot R_{sh,c}}{|Q|} \\
& + \frac{|Q_{ls,c}| \cdot R_{ls,c} + |Q_{hs,c}| \cdot R_{hs,c}}{|Q|} \qquad (3.24)
\end{aligned}
$$

3.4 Parametric Simulation

The impact of the clustered fault model on the soft yield (i.e., Y_S) is shown in this section by using the proposed off-device testing/repair methods. In the simulation the defect/fault propagation model is used to capture the impact of the on-device defects and faults off the device intact.

A CCD of 6 Mega pixels (2K×3K) is assumed in this simulation. Three CCDs of such capacity and each of which 8%, 5% and 2% defective pixels are considered respectively (i.e. 5% is $(2048 \times 3072)/20$). For the simulation, a map of defective pixels is generated using a single defect/fault model as shown in Figure (3.9).

The defective pixel map is generated by single number generation of built-in function in C language. The consecutive two random numbers are assigned to the coordinate of the defective pixel. This process continues until the number of defect pixel meets. If the generated pixel is out of bound or duplicated with other pixels already mapped then the generated pixel is discarded.

From the results in Figure (3.10)-(3.11), the following observations can be drawn.

1. Figure (3.10)-(3.11) show not only the single faults (i.e., AP=1) but also clustered fault (i.e., AP $>$ 1). Where AL (Acceptance Level) is the number of defective pixel contained in testing window except the testing pixel.

2. Repair rate of single defective pixels (exclude clustered defective pixels) was 51% for 92% hard yield CCD, 66% for 95% hard yield CCD, and 85% for 98% hard yield CCD. Where the single defective pixel means a pixel which has no other defective pixels in the test window (i.e., 3X3 in this simulation) like the pixel labeled A in Figure (3.7). From this simulation and theoretically, high yield CCDs have less clustered defective pixel.

3. Repair rate for just single defective pixel is too low than the expectation. In

other words, 49% for 92% hard yield CCD, 44% for 95% hard yield CCD, and 15% for 98% hard yield CCD are clustered fault. This means that there exist many clustered defective pixels and considering the clustered fault model is indispensable.

4. AL (Acceptance Level) = 4 for the size of 3×3 window is enough for achieving perfect repairing in the clustered model for high yield CCDs. It is very important factor in clustered fault model. If it were impossible and had to use larger filter, the detect/repair time would be increased exponentially. If the AL=4 were not secured, adopting larger testing window would be unavoidable.

5. From the simulation results, the size of 3×3 of the area under test is still very sufficient for repairing clustered faults. This means real time implementation is possible in low performance hardware.

6. Soft-test/repair results in increase the soft yield. From Figure (3.10), all test model secured 100% repair rate from AL=3. Optimal yield (i.e., reparable by soft-test/repair) CCD could be used more widely and decrease the cost of CCD without degrading image quality.

3.5 Discussion and Conclusions

This work has presented a testing and repair technique for defects/faults on CCD image system with inability of on-device fault tolerance, referred to as *off-device fault tolerance*. Digital image sensor devices such as CCD are, by their nature, can not readily utilize traditional on-device fault tolerance techniques because each pixel on the device senses a unique image pixel coordinate. No defective/faulty pixel can be replaced nor repaired by a spare pixel as any displacement of an original pixel coordinate can not sense the original image pixel. Therefore, to effectively provide and enhance the reparability of such devices with inability of on-device fault tolerance, a novel testing and repair method for defects/faults on CCD is proposed based on the *soft testing/repair* method proposed in our previous work [12] under both single and clustered distribution of CCD pixel defects. Also, a novel defect/fault propagation model is proposed to effectively capture the on-device defects and faults off the device for an effectiveness and practicality of testing and repair process. The efficiency and effectiveness of the method is demonstrated with respect to the yield enhancement by the soft-testing/repair method under a clustered fault model as well as single fault model, as referred to as *soft yield*. Extensive numerical simulations are conducted, and it has been demonstrated that the clustered fault model has a significant impact on the soft yield in comparison with the soft yield of the single fault model.

In Chapter 4, practical implementations regarding soft-test/repair will be presented. In addition, various parametric simulations in verilog HDL level such as testing and repair time analysis and parallel testing processing will be presented.

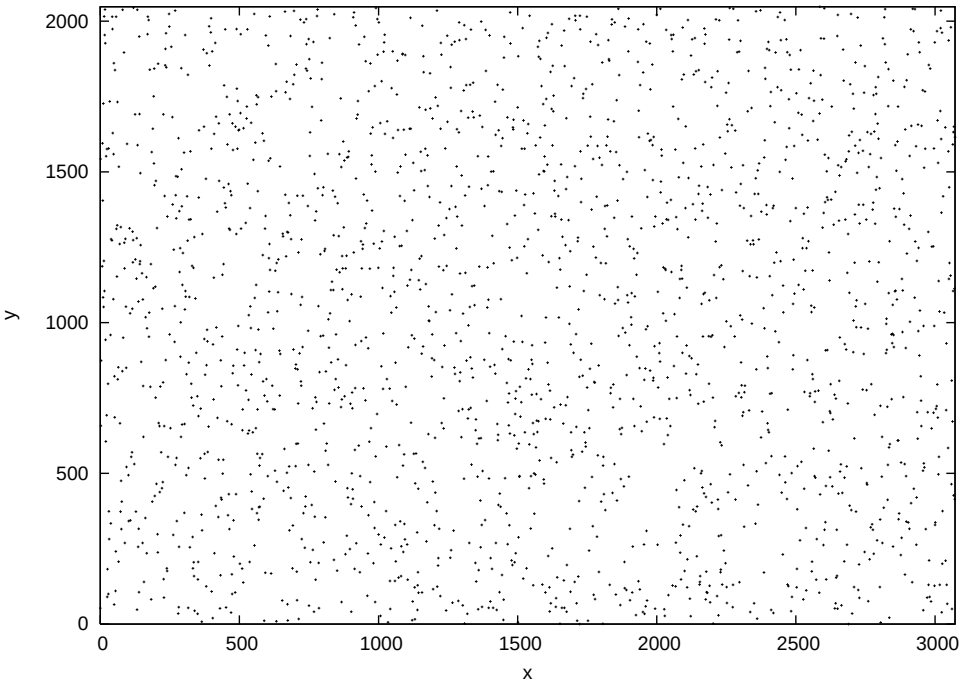

Figure 3.9: Defective Pixel Map

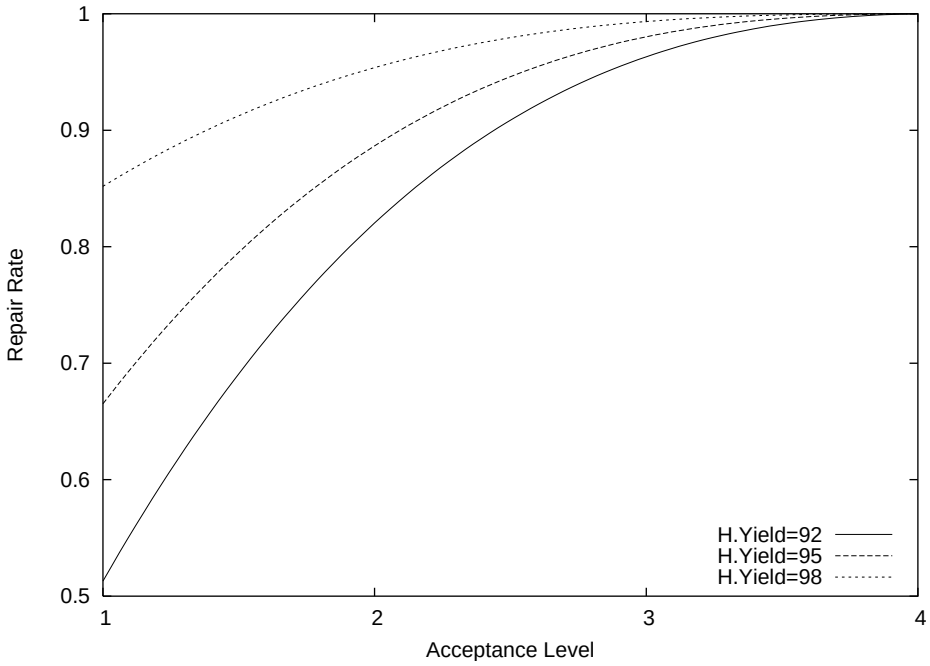

Figure 3.10: Repair Rate

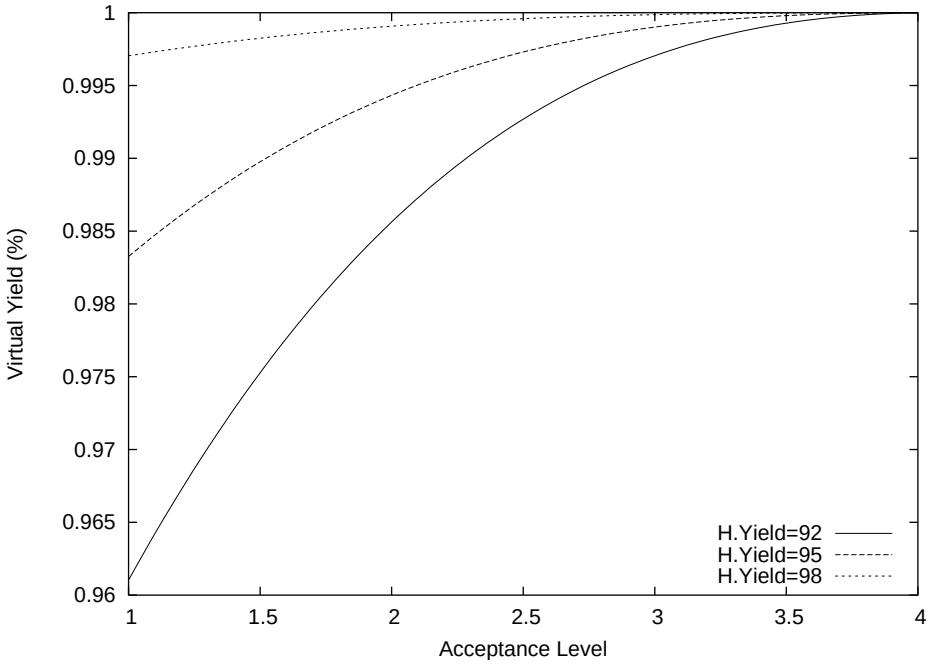

Figure 3.11: Virtual Yield

CHAPTER 4

BIST/BISR Design for the Proposed Soft-Test/Repair

This chapter presents a new cost and performance-efficient approach to the design and implementation of testing and repair of CCD hardware defective pixels by the proposed BIST/BISR design to improve yield. The theoretical yield improvement by soft-test/repair presented in Chapter 2 will be validated by a practical implementation of BIST/BISR. Performance characteristics of the proposed BIST/BISR approach and benefits from implementation of the proposed design will be also investigated through the extensive parametric simulations. Note that the proposed work is not to develop new filtering or calibration algorithms, but to propose a hardware-oriented image quality enhancement approach with respect to speed and hardware reliability-driven quality of service. For implementation purposes, Verilog *Hardware Description Language* (HDL) is used for *Register Transfer Level* (RTL) design and simulation.

This work is organized as follows. In the next section, the proposed BIST architecture, design, algorithm and performance analysis will be proposed. In Section 4.2, the effect of the scanning sequence for CCD image sensor will be investigated through numerical experiments. In Section 4.3, the relation between images and repair rates will be investigated through the image simulations. In Section 4.4, the proposed BISR architecture and design will be proposed. In Section 4.5, simulations with respect to CCD yield will be proposed. In Section 4.6, reliability model and a parametric analysis for BIST/BISR are provided. In Section 4.7, simulations for soft-test/repair method are presented and compared with other general graphic filtering methods. Conclusions and discussions are presented in Section 4.8.

4.1 Design of the Proposed Soft-Testing Circuitry

In this section, a design for the circuitry to realize the proposed soft-testing is proposed. Built-in self-test (BIST) circuitry will be developed and employed in order to demonstrate the validity of the proposed theoretical soft-testing/repair on the level of circuit design and simulation. The BIST performs a self-testing function online without intervention with the normal CCD operations. In general, the advantages that BIST can offer are: it does not need an access to an expensive external automatic test equipment; and it may reduce the circuit complexity by eliminating the required complex test access points needed by external automatic test equipment.

As the proposed BIST operates concurrently with the normal operations (i.e., on-line), it is expected to reduce the overall turnaround time for testing as well as the required normal operational time. In certain circumstances, such as mission and safety critical military or medical image processing devices or systems, a stringent system turnaround time is required to guarantee the delay of image processing to stay within the required range. Therefore, the proposed on-line BIST is a correct design choice to meet the requirements in such devices or systems.

For the purpose of cost-effectiveness, BIST will be used in the CCD controller that performs the normal operations in order to utilize the existing control modules as much as possible to maintain the complexity and overhead of the circuit within an economically-justifiable range.

In order to address performance issues, a parallel BIST architecture will be employed. This will enable the BIST to catch up with the possibility of bulky data to be processed as the size of CCD increases. The cost will be justified versus its performance gain.

Furthermore, various testing strategies will be developed in an effort to exploit various possible optimal testing algorithms under the pixel-defect distributions. The efficiency and effectiveness of the testing algorithms depend on various test-design

factors such as test-scheduling, sampling of pixels for testing, and granularity of test-window, to mention a few. Each proposed testing algorithm will be evaluated with respect to the issues stated above and optimized in terms of various test-design factors.

In summary, the proposed BIST is expected to provide the following technical merits:

- Concurrent (or on-line) testing capability.
- Cost effectiveness by utilizing and sharing the existing CCD control circuitry.
- Performance enhancement by parallel BIST.

This section is organized as follows: In Section 4.1.1, the proposed BIST architecture and the design are presented. In Section 4.1.2, the design and implementation of the proposed soft-repair algorithm is presented. Various testing strategies are proposed in Section 4.1.3. In Section 4.1.4, performance analysis regarding the number of test circuits will be performed. In Section 4.2, various strategies for the soft-test/repair of CCD are proposed.

4.1.1 Proposed BIST for the Soft-Testing

There are various causes for the pixel defects on CCD. Imperfect fabrication and improper processing may induce defects (referred to as *hard-defects*) on the photo-sensitive pixels and supporting system components in CCD. In [15], the main causes of CCD hard-defects are the target defects in this work and can be categorized in Chapter 2.

The fault models simulated in this design are stuck high, stuck low, low sensitivity, and high sensitivity as identified and defined in Chapter 2.

As for the input test image for controlling the proposed fault model, an external test vector generator is employed to inject the test into the BIST, which is different from the internal test vector generation practiced in conventional BISTs.

The proposed method of manipulating the testing and repair process in a sequence of small windows of testing/repair enables the maintainability of the storages requirement for buffering pixel defect information of the entire CCD to the size of a window. Therefore, each round of the testing/repair process can detect and repair those pixels falling in the window, and, as more test inputs injected, the pixel defect-map will be cumulatively constructed in flash memory and eventually become stabilized. Note that this is one of the novel features the proposed soft-testing can offer since the pixel-defect map is determined by the physical and permanent defects of the pixels on the CCD and they are finite, therefore the soft-testing routine is expected to end in a finite amount time. This lets the proposed soft-testing method to substantially depart from the conventional off-line image filtering method, in which the filtering algorithms run against each different image off the processor and each different image downloaded must go through a new filtering process in an ad-hoc manner reaching no stabilized and finite database of the faults on the incoming supposedly infinite number of images.

Also, in order to validate the theoretical results on the impact of the distribution of the pixel defects on the yield, the random pixel defect distribution, as was investigated in Chapter 2, will be simulated and tested by using the following distribution function as reported in [16] and the clustered pixel defect distribution, as was investigated in Chapter 3, will be simulated and tested by using the following distribution function as reported in [16]

Regarding the observability of the tests, the required amount of buffers for the test output signatures can also be limited by the size of the window of testing/repair process. Each supposed-to-be normal test output signatures for each test input can be memorized in the BIST logic to test against the test output signatures either with or without a fault.

Furthermore, the testability of the soft-testing algorithms will be evaluated in

order to sort out the possible inability to detect a fault in the image mapped on memory (so-called test escape) due to defects that hit on a or multiple pixels required to be normal for a complete fault detection process. The testability is defined as the probability to be able to detect a fault induced and mapped by a pixel defect in CCD within a given testing/repair window. How many and which pixels to survive the defects for a normal soft-testing within a given window size will be analyzed. And in this regard the confidence-level of the soft-testing will be modeled and analyzed.

Regarding the controllability of the tests, the proposed BIST circuit cooperates with the CCD controller as depicted in Figure (4.1). It is one n bit input and one n bit output system which are controlled by BIST. The captured image input is supposed to stored in frame memory in Figure (4.1). Therefore, the BIST shares the stored image input with CCD controller for controllability. The testing is performed through the CCD controller by calculating the pixel values, which are stored in frame memory. Note that the objective of the testing is the CCD itself, not the memory. It is assumed that the memory does not have any kinds of faults.

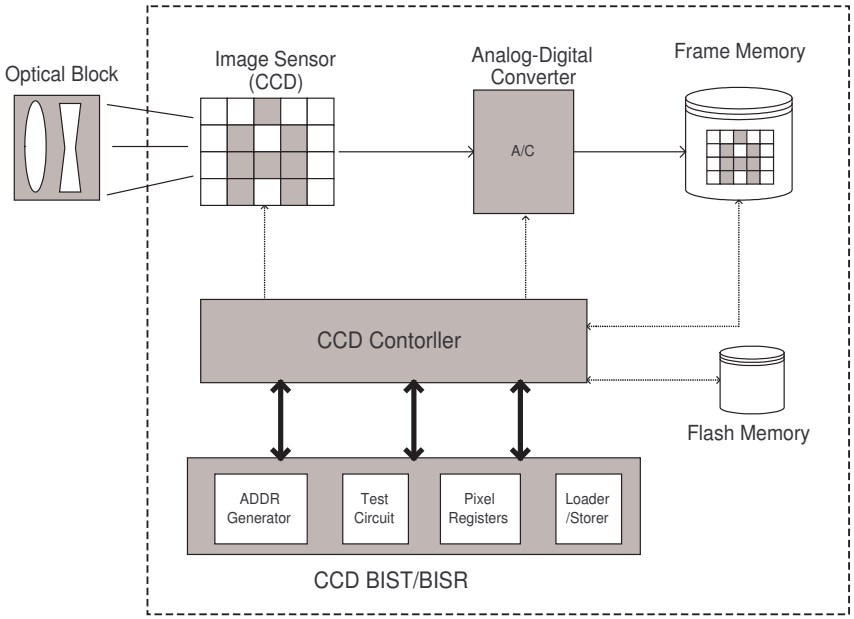

Figure 4.1: BIST/BISR Architecture

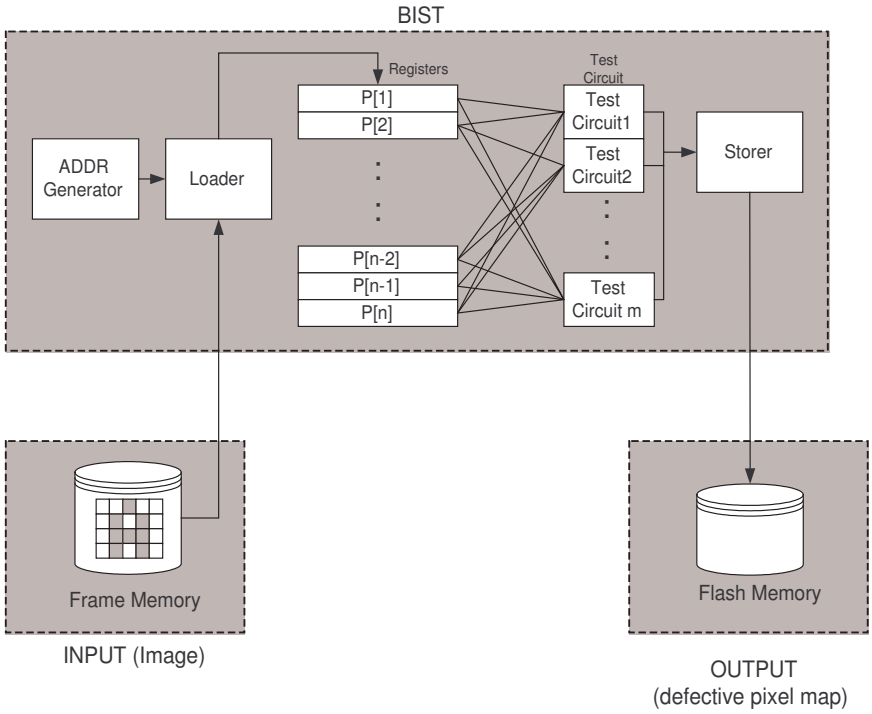

Figure 4.2: The proposed architecture for the soft-testing

In order to demonstrate the validity of the proposed theoretical soft-testing/repair on the circuit design and simulation level, testing circuitry is designed and presented as shown in Figure (4.1) and Figure (4.2).

As shown in Figure (4.1), the proposed BIST consists of the following primary modules.

- Address Generator
- CCD Controller
- Testing Circuit
- Frame Memory
- Flash Memory
- Loader/Storer

- Pixel Registers

An address generator computes an address to load a pixel value from the frame memory to a pixel register. The sequence of the addresses to be loaded is determined by the soft-testing/repair algorithm to be employed. The window size used in this work as a criterion is 3×3 involving total 9 pixels' values.

The Loader/Storer reads a pixel value from the frame memory and writes in a pixel register, respectively. Note that one read/write port is used on the frame memory as an ordinary SRAM.

The frame memory is the primary storage for the image captured by the CCD. The size of the frame memory is determined by the resolution of the ADC and the number of pixels. For example, if the system uses a 12-bit ADC and a 6 Mega pixel CCD, then the size of the frame memory is 12×6 Mega Byte.

The testing circuit computes the pixel values by the proposed testing algorithm in Section 4.1.2. In order to address the performance issue, a parallel BIST can be employed as detailed in Section 4.1.4.

The Pixel Registers hold the pixel values loaded from frame memory and the test circuitry retrieves the stored pixel values from the pixel registers. A pixel register can be accessed from several test circuits simultaneously by the parallel BIST.

Figure (4.2) shows a detailed structure of the proposed BIST along with the flow of operations. The number of m test circuitry access and retrieve the n pixel registers, P[n].

A single BIST-based architecture is shown in Figure (4.3).

The sort & select 4 module sorts the 8 pixel values surrounding the center pixel under the test, and then forward medium 4 pixel values to the adder. The algorithm and flow of the operations of the test circuitry will be detailed in Section 4.1.2.

The comparator decides if the center pixel under test is normal or abnormal based on the computed values by the proposed soft-test algorithm, and then the test result

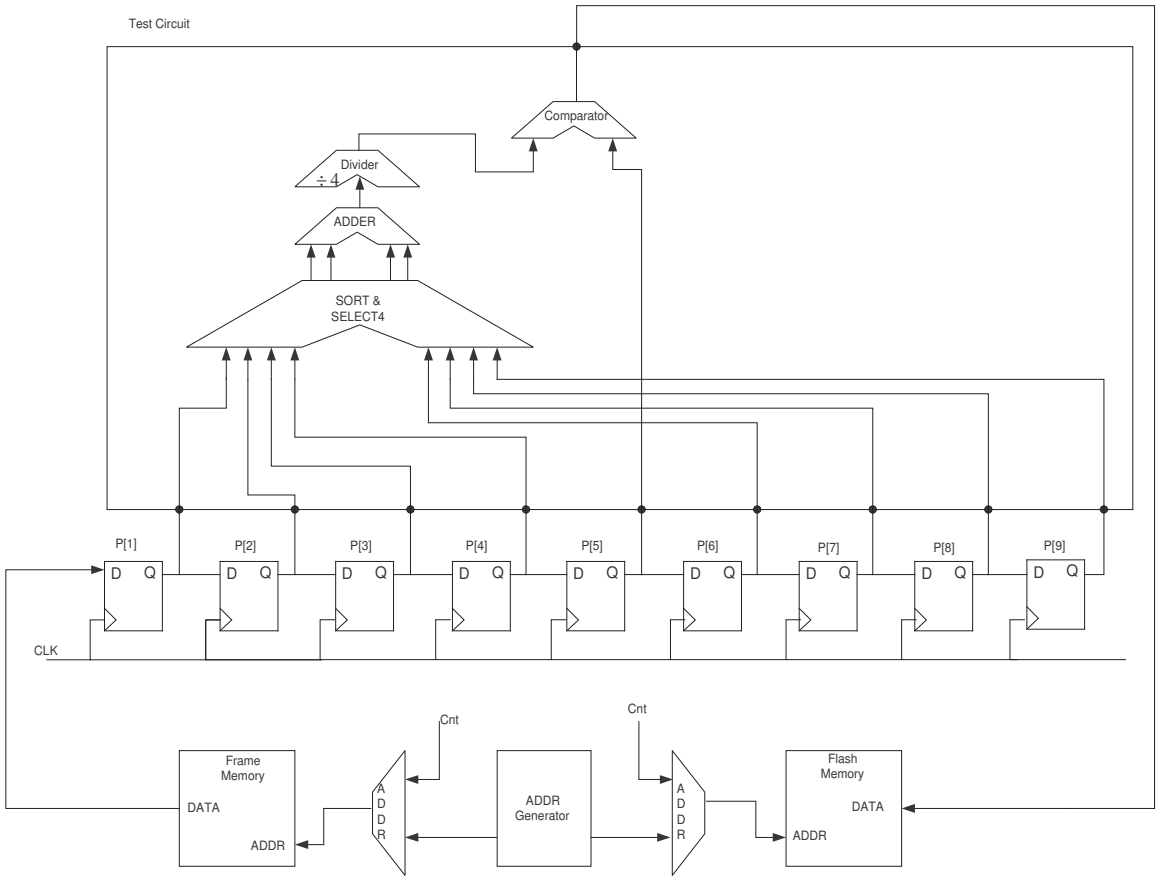

Figure 4.3: The proposed BIST circuit

will be stored (or marked) in the flash memory as a cumulative defective pixel map as follows:

- 000: Stuck Low
- 001: Low Sensitive
- 010: Stuck High
- 011: Stuck Low
- 100: Normal

Note that this map will be referenced in the following round of testing and repair.

Various testing algorithms will be further developed and presented with respect to various kinds of faults in Section 4.1.3.

4.1.2 Proposed Base Testing Algorithm

In this section, the design and implementation of the proposed soft-testing algorithm is presented based on the threshold testing model as was introduced in Chapter 2 and is shown below.

$$\left| \frac{\sum_{k=1}^{4} P(k) + \sum_{k=6}^{9} P(k)}{N} - P(5) \right| \leq C \tag{4.1}$$

where $P(1) \cdots P(N)$ are those pixels surrounding the pixel $P(5)$ under test; and notice that this is a BIST architecture with $N = 8$. A detailed principle has been presented in Chapter 2 and is based on the general observation in digital imaging systems that the pixels tend to exhibit similar values around the average. The constant C is the threshold for determining whether the testing pixel is defective. The constant C will be calculated by using *Mean Medium Four* (MMF) such that the brightest two pixels and the darkest two pixels are excluded in the computation for the average value. Then, the remaining 4 pixels participates in the computation for the average value.

The design and implementation algorithm of the the proposed BIST circuitry based on Equation (4.1)is as follows.

```
CCD-BIST
1  WHILE given time
2     DO PICK-WINDOW
3        SOFT-TEST
```

In line 2, PICK-WINDOW selects which testing window to be tested next. It is determined by various algorithms such as Coarse Random, Medium Random, Fine

Random, Random Avoidance and Round Robbin. Details of each algorithm will be presented in Section 4.2. along with simulations results.

In line 3, SOFT-TEST procedure is called and is implemented as follows.

```
SOFT-TEST(P[])
1 FOR j <- 1 to NO_OF_COLUMN_INWINDOW
2     DO FOR i <- to NO_OF_ROW_INWINDOW
3            DO LOAD(i,j,P[])
4               SORT(P[])
5               SUM <- P[3]+ P[4]+ P[6]+ P[7]
6               AVG <- SUM / 4
7               VAL <- ABS(AVG - P[5])
8               VAL <-  VAL / AVG
9               IF VAL < 0.1
10                  THEN STORE(i,j,NORMAL)
11                  ELSE STORE(i,j,ABNORMAL)
```

The computations to be taken in the above CCD-TEST procedure are described below: The for loop in line 1-2 iterates the test procedure as many times as the product of the number of columns and rows on the CCD pixel-matrix, in each iteration a specific window of pixels are processed as defined; In line 3, the pixel values are loaded from the frame memory into the register pixels as an array P[ ]; In line 4, those pixel values are sorted, and in line 5-6 computes the average value (AVG) of the four core pixels excluding the top 2 darkest and the bottom 2 brightest; in line 7 the difference of the pixel value of P[5] from the AVG and store the result in VAL; in line 8 the ratio of the the VAL over AVG is computed; in line 9 the VAL to the threshold constant C is compared ($C = 0.1$ is employed as an example) such that if the computed ratio is smaller than C, then a normal pixel value is stored in the defective pixel map, otherwise the detected abnormal value is stored in the defective

pixel map for use during the repair process later.

The implementation flow of the above testing algorithm along with the proposed BIST architecture is shown in Figure (4.4): In step 1 through 5, the values of the pixel under test as well as testing pixels are loaded in the pixel registers; and performs the computations as given in line 3 in the CCD-TEST procedure; in step 6 through 9, the sorting is performed as given in line 4 in the CCD-TEST procedure; in step 10, the selected 4 pixels participate in the computation for AVG as given in line 5-8 in the CCD-TEST procedure; in step 11, it determines whether the pixel under test is normal or abnormal and if the result is normal, the BIST stores 100 in the flash memory as given in line 9-11 in the CCD-TEST procedure.

Figure (4.5) shows the sequence of combined testing and repair cycles. Each unit cycle time of combined testing and repair determines the execution time of each round of such operation and is referred to as a *window*. Within each window, a repair process is performed and followed by a testing process. Initially, a null repair process is performed since there is no recording made in the defective pixel map in the flash memory. Once a defective pixel map starts to get recorded due to detected defective pixels, the repair cycle within each window starts to map those recorded defective pixels from the defective pixel map in the flash memory with normal data. Thus, new incoming pixels are tested with certain recorded-defective pixels repaired apriori in order to avoid redundant repair and testing processes.

4.1.3 Proposed Various Testing Algorithms

Various testing strategies are proposed and designed to exploit different test-design factors, such as test-scheduling, sampling of device-under-test, and granularity of test-window, versus various pixel defect distributions, e.g., random and clustered pixel defects.

Figure (4.6)(4.7)(4.8)(4.9) show the proposed testing process for stuck-high, stuck-

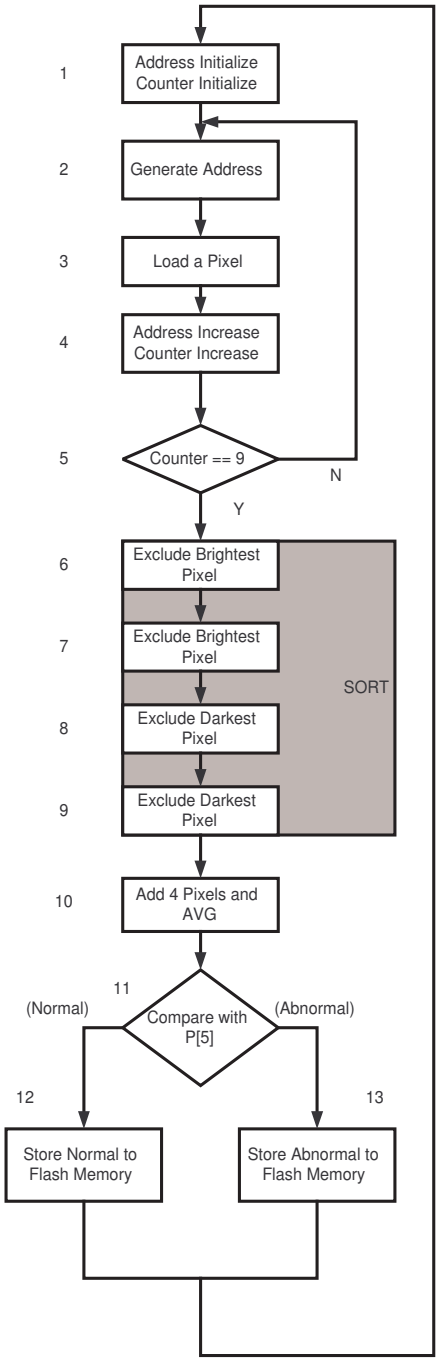

Figure 4.4: The soft-testing flow in the proposed testing circuitry

Figure 4.5: Sequence of combined soft-testing/repair cycles

low, low-sensitivity, and high-sensitivity, respectively.

Stuck-high pixels display very dark above a certain threshold value as compared to the neighboring pixels regardless of the input images as shown in Figure (4.6). Therefore, unless the neighboring pixels are also stuck-high, the test can detect the stuck-high as a defective pixel under the test if placed in the center.

Stuck-low pixels display very bright below a certain threshold value as compared to the neighboring pixels regardless of the input images as shown in Figure (4.7). Therefore, unless the neighboring pixels are also stuck-low, the test can detect a stuck-low defective pixel under test if placed in the center.

Low-sensitive pixels display a little bright below a certain threshold value as compared to the neighboring pixels according to input images as depicted in Figure (4.8). The difference between stuck low and low sensitive pixel is the latter is changing the pixel values according to the input while the former always shows same value.

High sensitive pixels display a little dark as compared to the neighboring pixels according to input images as depicted in Figure (4.9). The difference between stuck high and high sensitive pixel is the same as the difference between stuck low and low sensitive pixels.

As mentioned above, the same input images could not activate pixel faults. Therefore, it is required to select testing windows within a given testing time for the effectiveness of the test. Detailed simulation for the picking windows will be presented in the following section.

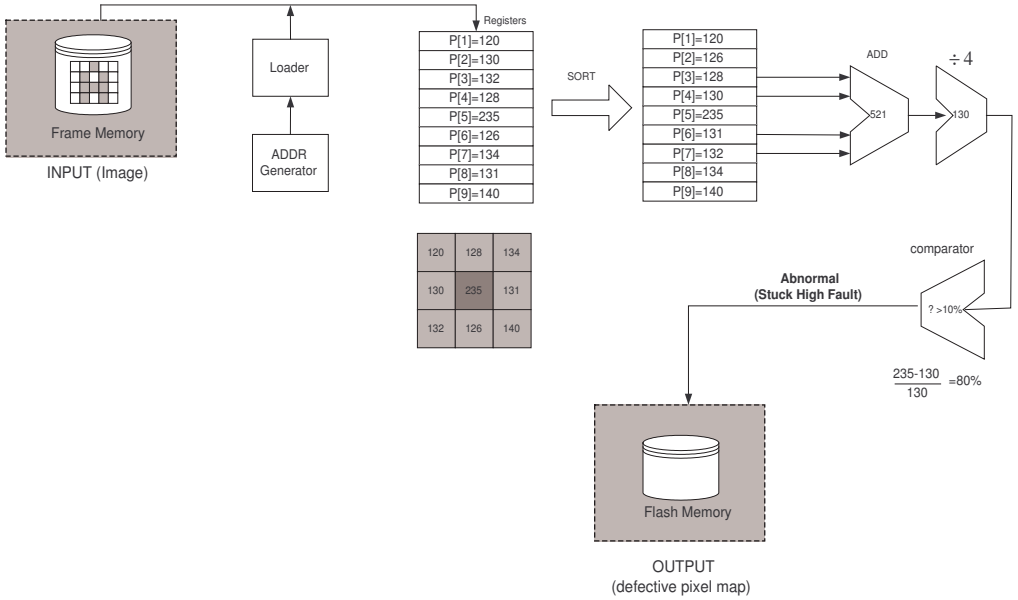

Figure 4.6: Detection of stuck high defective pixel

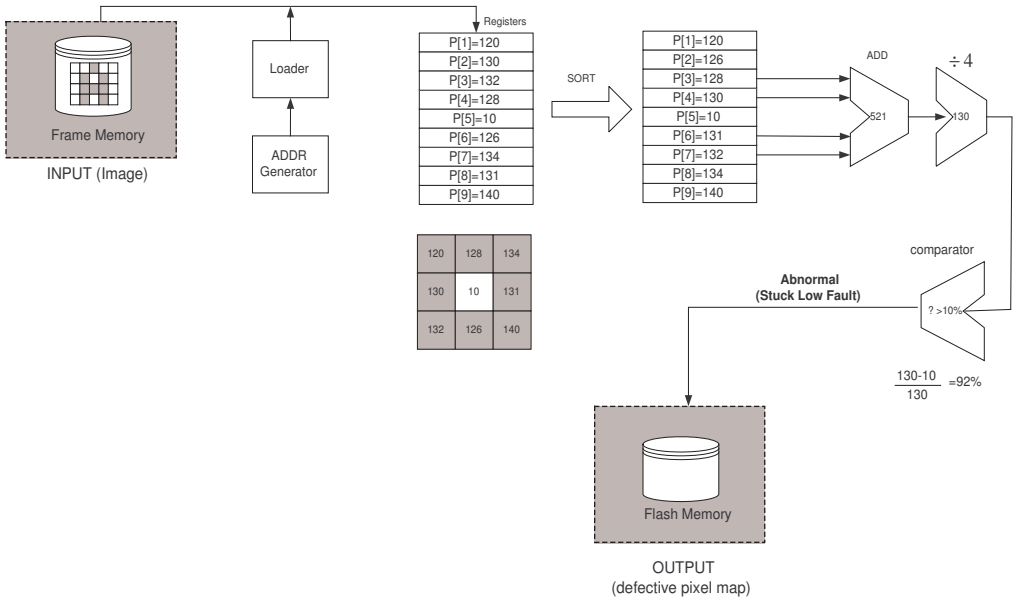

Figure 4.7: Detection of stuck low defective pixel

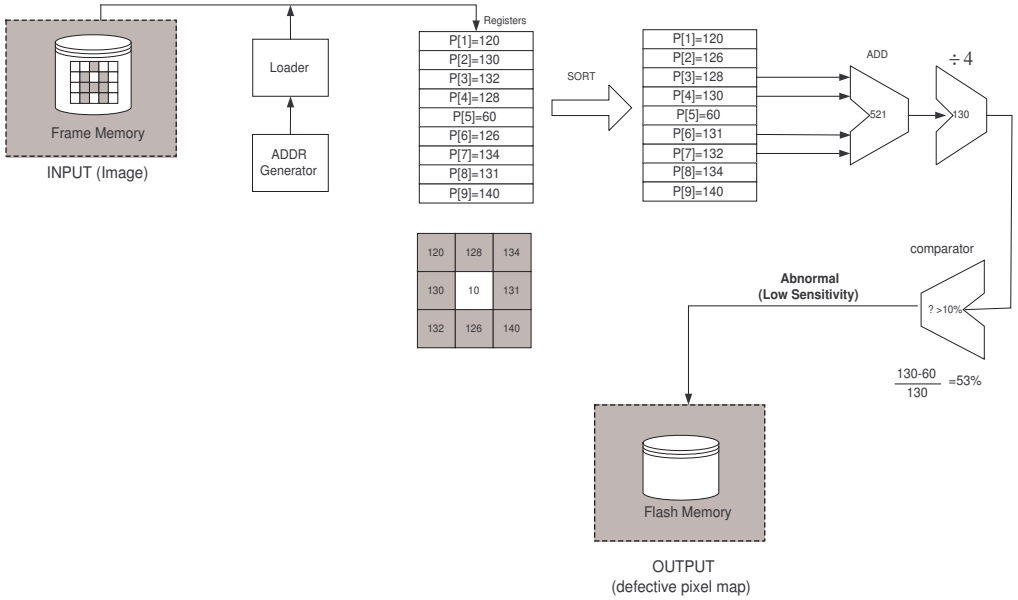

Figure 4.8: Detection of Low Sensitive pixel

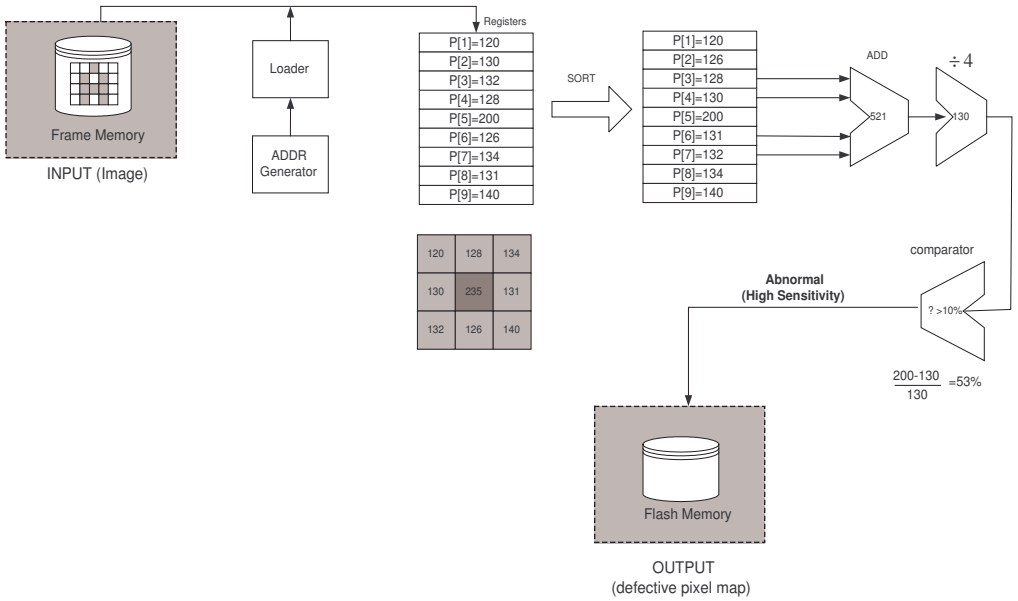

Figure 4.9: Detection of High Sensitive pixel

4.1.4 Performance Analysis

In order to address the performance, a parallel BIST architecture will be designed. This will enable the BIST to reduce testing time and catch up with the possibly bulky data to be processed depending on the size of the CCD within the given time. The number of CCD pixels currently using CCD is over 10 Mega pixels in general. Thus, the proposed BIST should consider this trend. The cost also will be justified versus its performance gain.

Flash memory is the sole overhead for the BIST. As the proposed BIST does not accommodate for the test pattern and testing signature, the total overhead is extremely low. Note that the proposed BIST shares many functional parts with CCD controllers.

In order to investigate the improvement by the parallel BIST, verilog HDL simulation is performed as follows:

1. Input the number of pixels of CCDs as follows: 64×64, 128×128, 256×256, 512×512, 1024×1024, 2408×2048, 4096×4096.

2. Generate 10% of defective pixels in each CCD model.

3. Input the number of test circuit : 1, 3, 5.

4. Test each CCD model.

5. Record testing time of the CCD model.

The simulation results are shown in Figure (4.10). Where a unit is 1 nano second. By analyzing the result of Figure (4.10), following features are observed.

- The single Test Circuit takes the longest time, and five Test Circuit takes the least time.

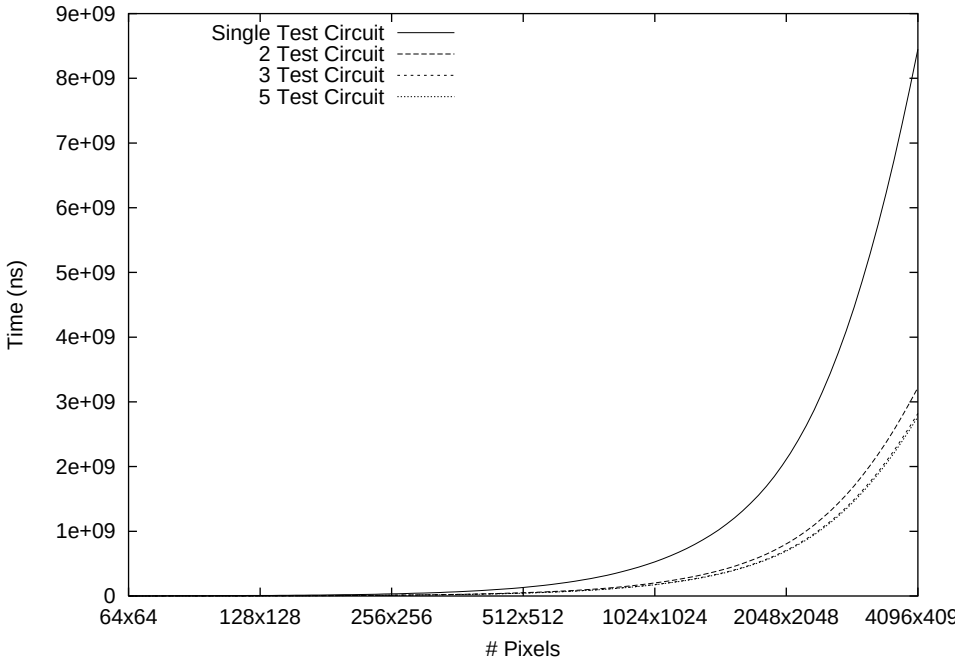

Figure 4.10: Testing Time of pixels by Test Circuits

- It is observed that there is no considerable difference between 3 Test Circuit and 5 Test Circuit. Therefore, 3 Test Circuit is cost efficient BIST structure without loosing significant performance.

- At 2048x2048 (4M pixels), the test time of single Test Circuit is twice of the test time 3 or 5 Test Circuits. However, at 4096x4096 (16M pixels), the test time of single Test Circuit is three times of the test time as 3 or 5 Test Circuits. From above example, most high resolution CCDs require pretty long test times. Thus, the parallel BIST is an effective test method to reduce testing time considerably.

From the above simulation result, a 3 Test Circuit BIST circuitry is presented as shown in Figure (4.11), which is implemented for high speed but minimal cost. The single Test Circuit BIST is already demonstrated the validity of proposed theoretical soft-testing repair on the circuit design and simulation level. The flow chart for the parallel BIST (3 Test Circuit BIST) ,which is extended design of the single Test Circuit BIST, is shown in Figure (4.12). The basic design concept for the parallel

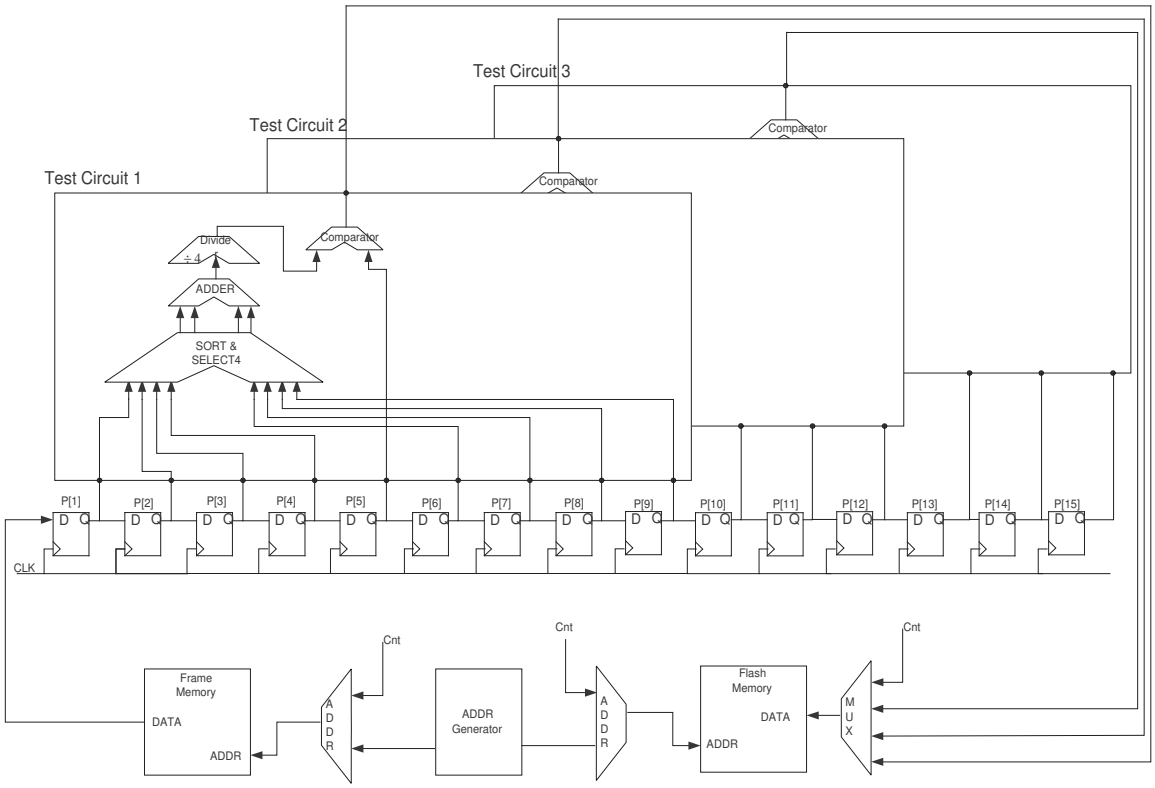

Figure 4.11: The proposed BIST circuit (3 Test Circuit)

BIST was already shown and studied in Section 4.1.2.

Figure (4.13) shows the sequence of loading pixel to the registers in 3 Test Circuit BIST systems. The reason to load in vertical sequence is to save time and share the loaded pixels with the Test Circuits. As shown in Figure (4.13), each Test Circuit shares 6 pixels with other Test Circuits.

The optimal number of registers is determined by the following equation. It is straightforward to induced from Figure (4.13).

$$N_{register}(N_{TestCircuit}) = 9 + 3(N_{TestCircuit} - 1) \tag{4.2}$$

Where $N_{register}(n)$ is the number of registers, and $N_{TestCircuit}$ is the number of Test Circuits and always $N_{TestCircuit} \geq 1$. From Figure (4.13), each Test Circuit loads nine pixels to test. However, the six pixels are overlapped as depicted in Figure (4.13).

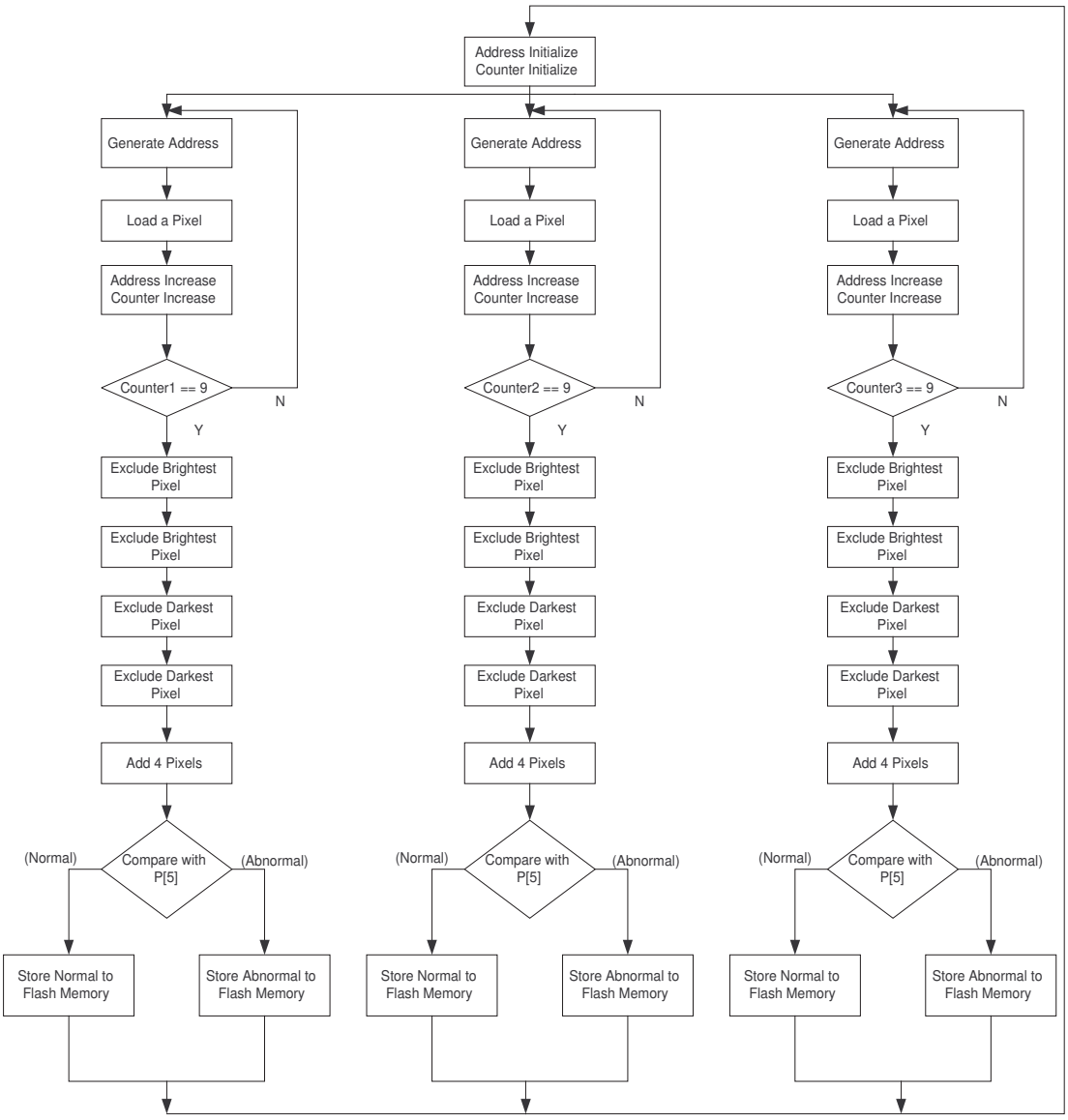

Figure 4.12: BIST 3 Test Circuit Flow Chart

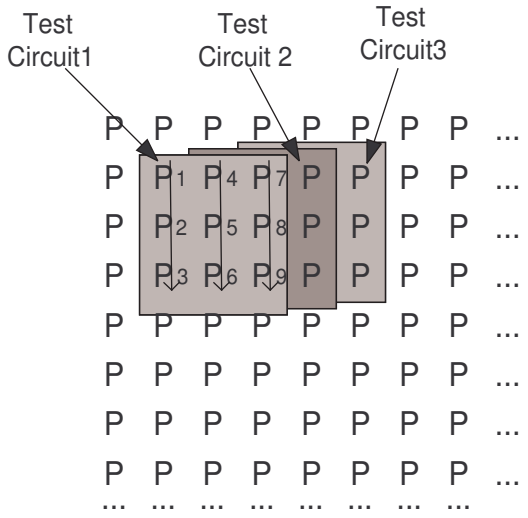

Figure 4.13: Pixel Loading Sequence (3 Test Circuits)

For example, in case of 3 Test Circuit BIST, $9 + 3 \times 2 = 15$ pixels have to be loaded.

4.2 Scanning Sequence Analysis

In this section, the effect of scanning sequence of soft-test for CCD image sensor is investigated through numerical experiments. As each window size does not cover the entire image in each round, it is necessary to determine the order of sequence of spacial location of the CCD pixels to be tested and repaired. The proposed various algorithms are presented as follows.

- Coarse Random: The window size is big and a single static window will be used until the window time expires. Figure (4.14) shows the sequence of coarse random algorithm.

- Medium Random: The window size is medium and multiple windows will be selected until end of the testing time. Since the testing time is same, the scanning area should be same as coarse and other scanning methods. Figure (4.15) illustrate the sequence of medium random scanning.

- Fine Random: The window size is smaller than medium and more windows will be chosen until testing time end. Figure (4.16) illustrate the sequence of fine random scanning.

- Round Robin: Same window size as Coarse random, however, just move to the next unoverlapped window. The distribution of defective pixels is assumed to be random. Figure (4.17) illustrate the sequence of round robin scanning.

- Random Avoidance: Same as coarse random, however, the next window should be off from the previous window by more than the window size. Figure (4.18) illustrate the sequence of random avoidance scanning.

Note that the total testing area of each scanning sequence is same. Coarse random, Medium random, and Fine random methods could select overlapped windows from

previous windows. Relatively, Round robin and Random avoidance could select un-overlapped windows.

CCDs of 16 Mega pixels (4K×4K) are assumed in this simulation. Three CCDs containing 10%, 7% and 3% defected pixels are considered, respectively .

The detection rates are simulated as shown in the Figures (4.19), (4.20), and (4.21). $Y_H = 90\%$, $Y_H = 93\%$ and $Y_H = 97\%$ CCDs are used for Figures (4.19), (4.20), and (4.21), respectively.

By comparing the results of Figures (4.19), (4.20), and (4.21), the following observations can be drawn.

- The round robin method outperforms the other scanning methods.
- The size of random windows result in as follows: Fine Random > Medium Random > Coarse Random. From these results, the window size should be small and sampling as many as possible.
- The Random Avoidance method is not effective as others. From the graphs, it places between Coarse Random and Medium Random methods.

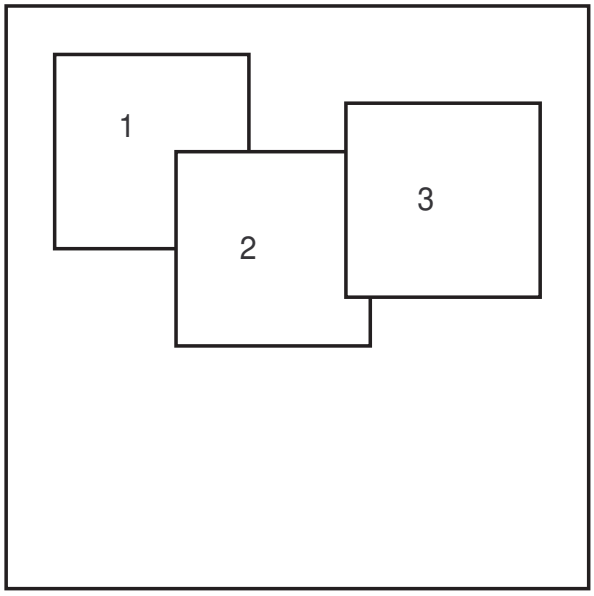

Figure 4.14: Coarse Random Scanning Sequence

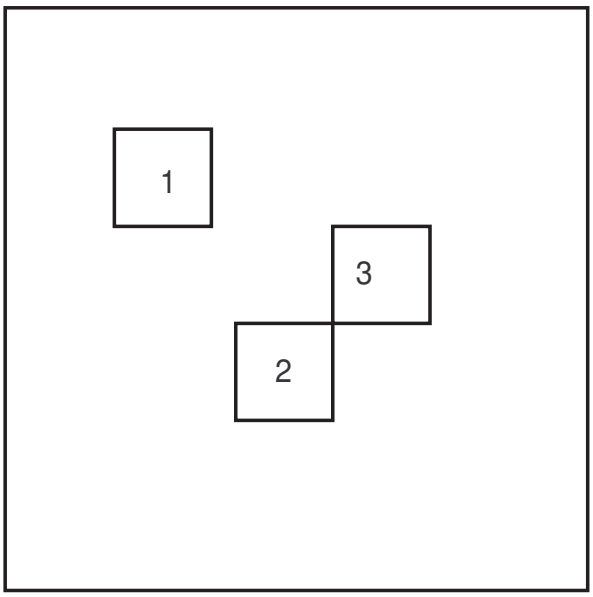

Figure 4.15: Medium Random Scanning Sequence

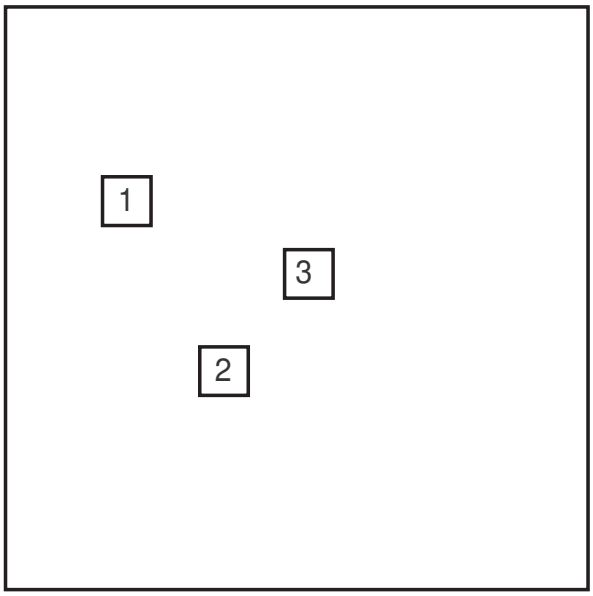

Figure 4.16: Fine Random Scanning Sequence

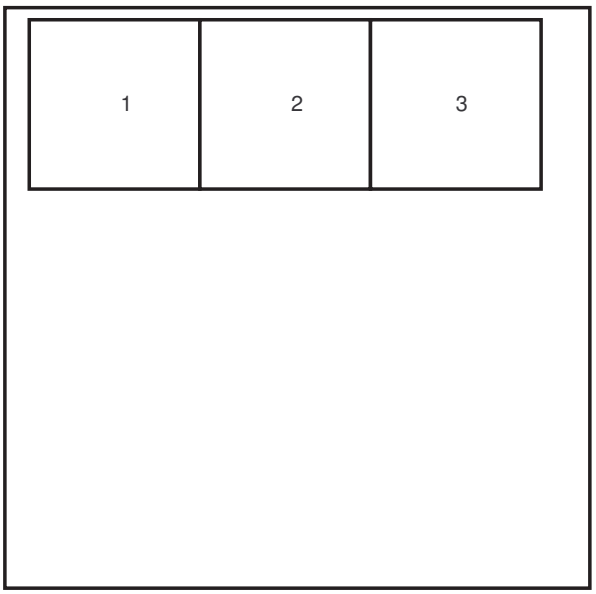

Figure 4.17: Round Robbin Scanning Sequence

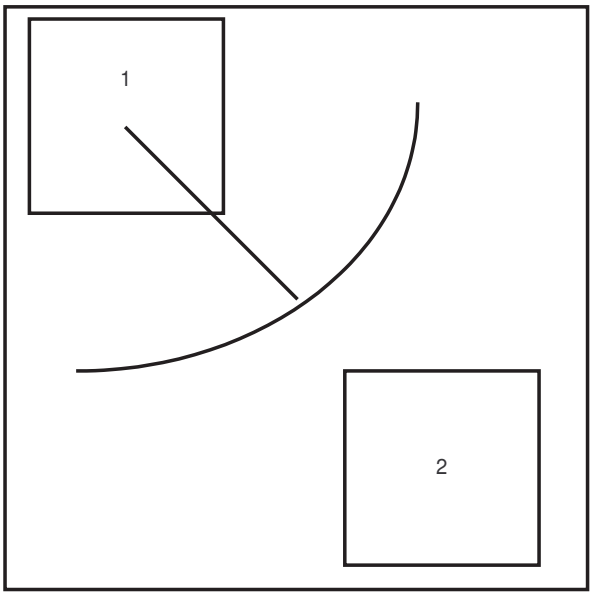

Figure 4.18: Random Avoidance Scanning Sequence

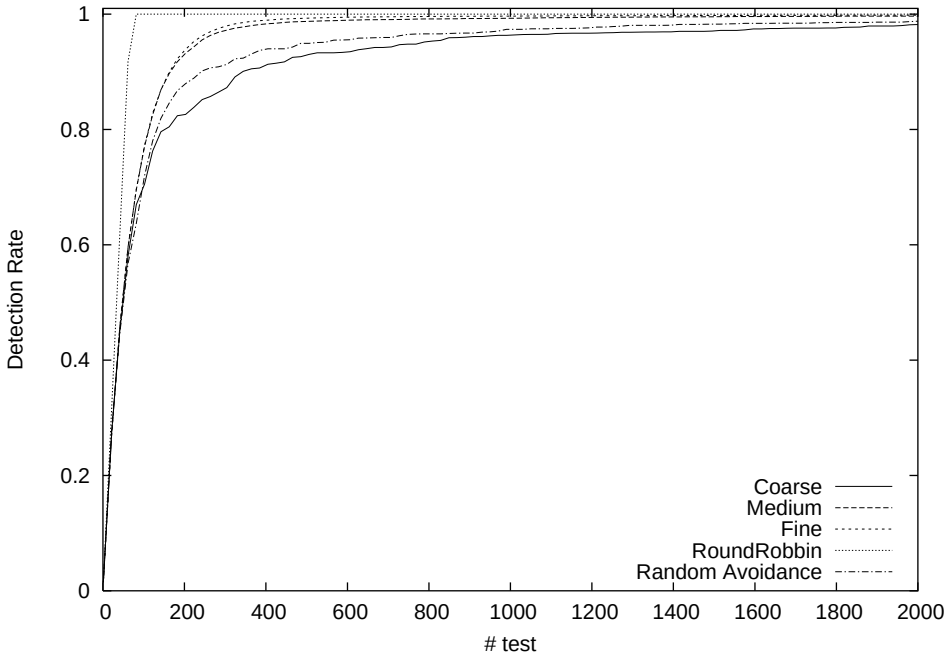

Figure 4.19: Scanning Sequence (Hard Yield 90%, $4K \times 4K$)

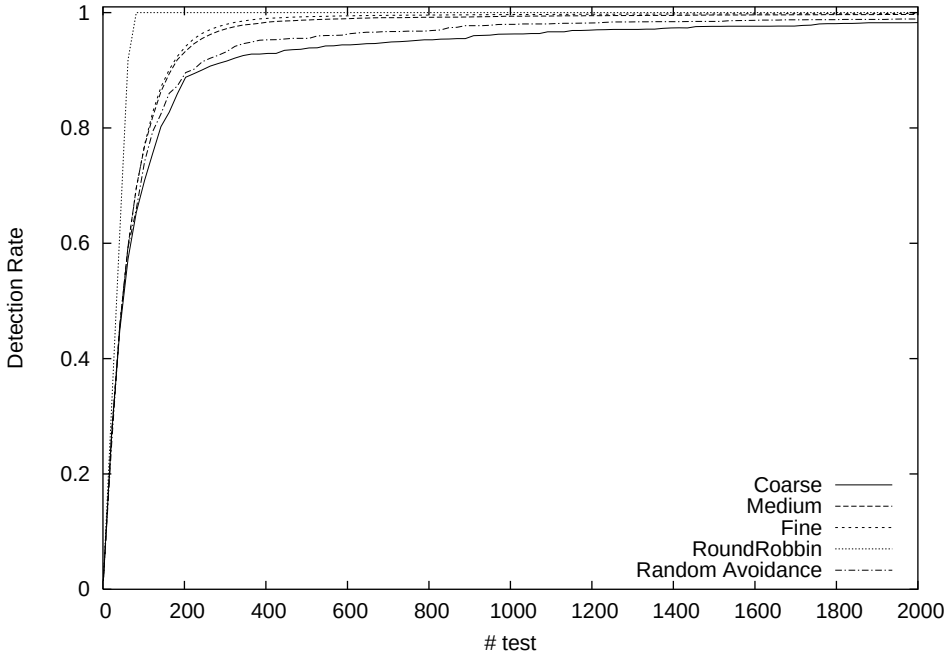

Figure 4.20: Scanning Sequence (Hard Yield 93%, $4K \times 4K$)

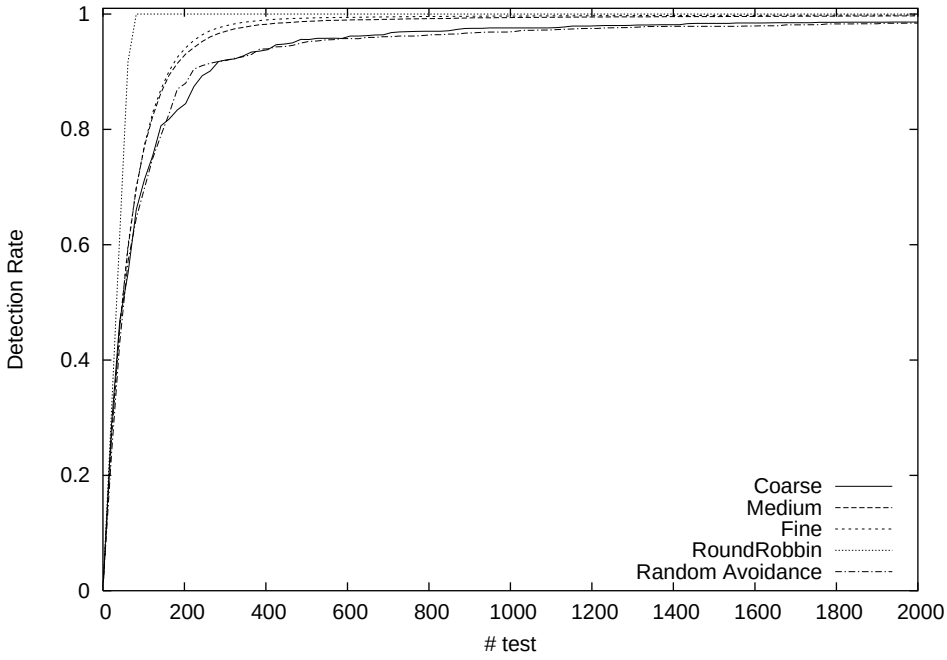

Figure 4.21: Scanning Sequence (Hard Yield 97%, $4K \times 4K$)

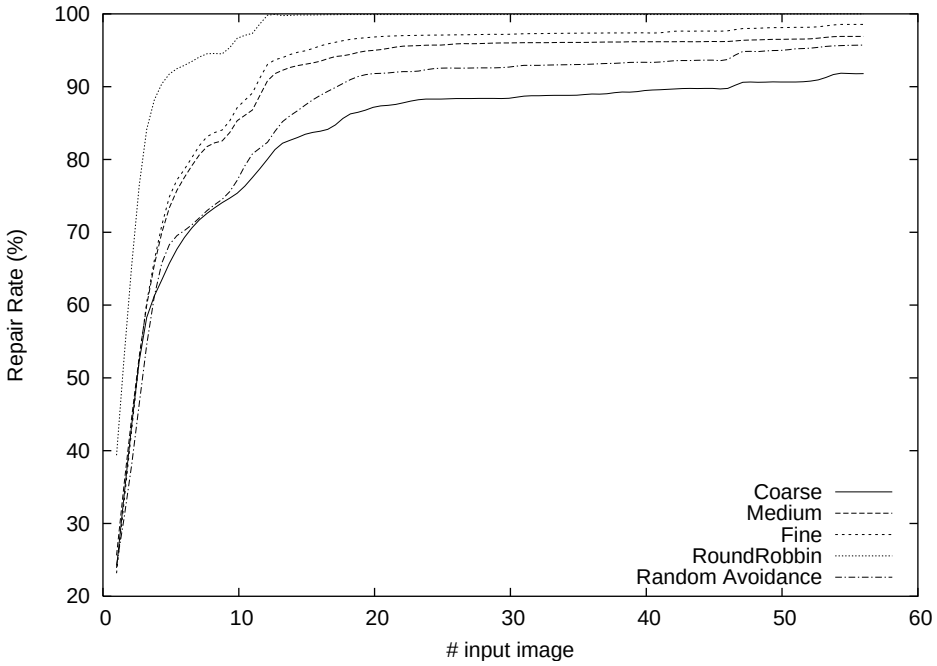

Figure 4.22: Scanning Sequence by Real Image (Hard Yield 90%, $4K \times 4K$)

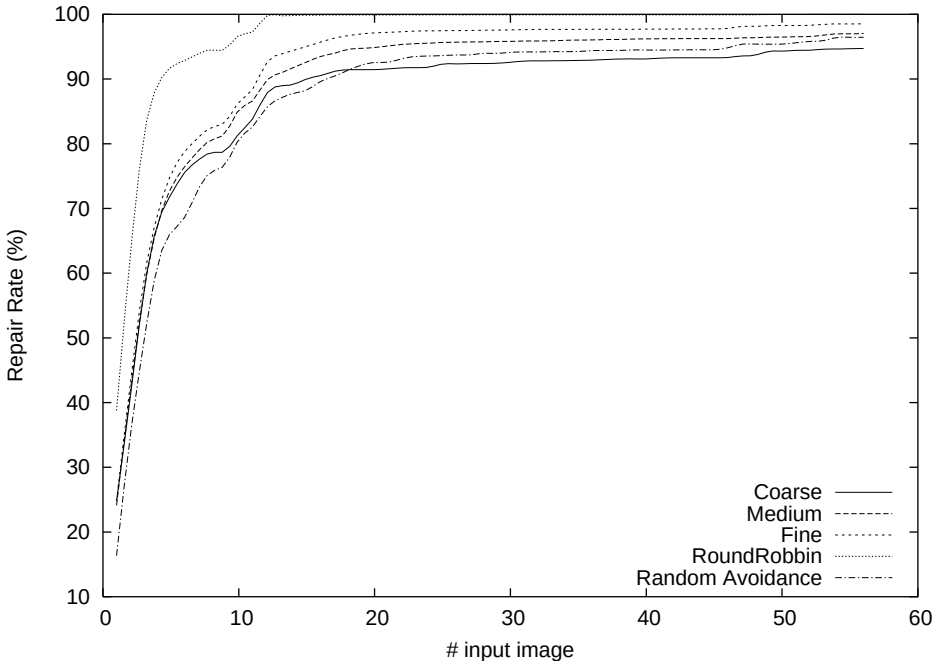

Figure 4.23: Scanning Sequence by Real Image (Hard Yield 93%, $4K \times 4K$)

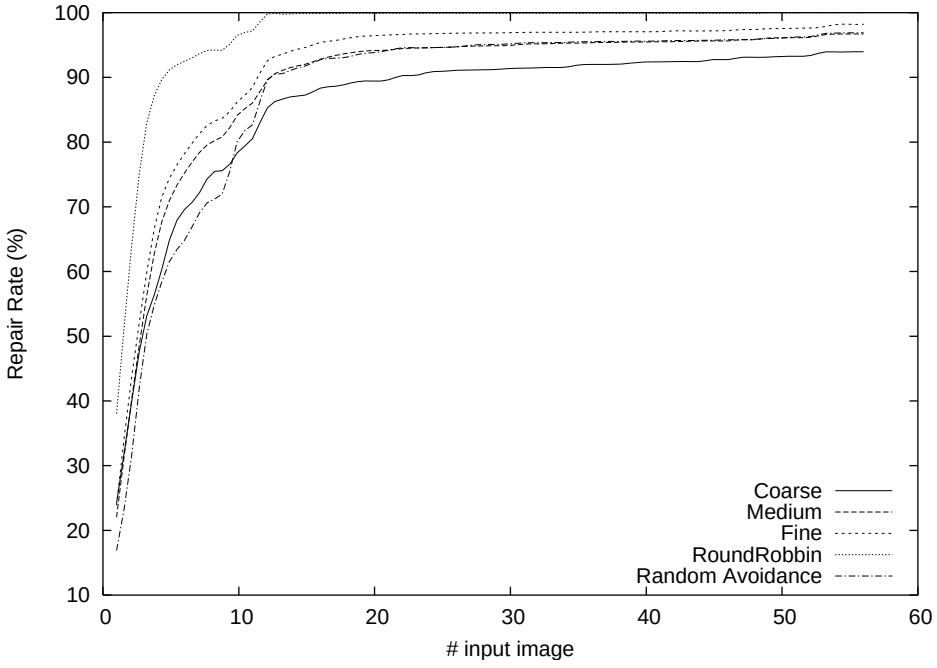

Figure 4.24: Scanning Sequence by Real Image (Hard Yield 97%, $4K \times 4K$)

4.3 Input Image Analysis

In this section, the effect of input images of soft-test for CCD image sensor is investigated through numerical experiments. The simulation was conducted under the following conditions.

- Optimal inputs : Optimal inputs consist of pure white, pure black, and gray colors. Each input is used repeatedly in sequence of pure white, pure black, and gray.

- Random Inputs : Random input consists of any images, such as pictures, etc. However, it is assumed a random image is not composed of single tone. In other words, random input excludes optimal inputs. In the simulation, the image was generated by a random number generation function.

CCDs of 1 Mega pixel (1K×1K) are assumed in this simulation. Three CCDs containing 10%, 7% and 3% defected pixels are considered, respectively . After generating inputs, the defective pixels are inserted in random positions.

The detection rates are simulated as shown in the Figures (4.25), (4.26), and (4.27). $Y_H = 90\%$, $Y_H = 93\%$ and $Y_H = 97\%$ CCDs are used for Figures (4.25), (4.26), and (4.27), respectively.

By comparing the results of Figures (4.25), (4.26), and (4.27), the following observations can be drawn.

- Random input outperforms Optimal input in the beginning. Since the input is tested by a small sized window, the random input has higher detection rate in the beginning. The reason is that the optimized input consists of pure white, pure black, and mixed input. Each optimal input should be tested multiple

times since the window size does not cover the whole image. However, in Figure (4.25), the optimal input outperforms random input from n=9 .

- A Slight difference could be observed from Figures (4.25), (4.26), and (4.27). However, the point that each input arrives 100% detection rate is almost the same, $n > 18$.

- From these analysis, it was verified that the input images does not affect the testing quality.

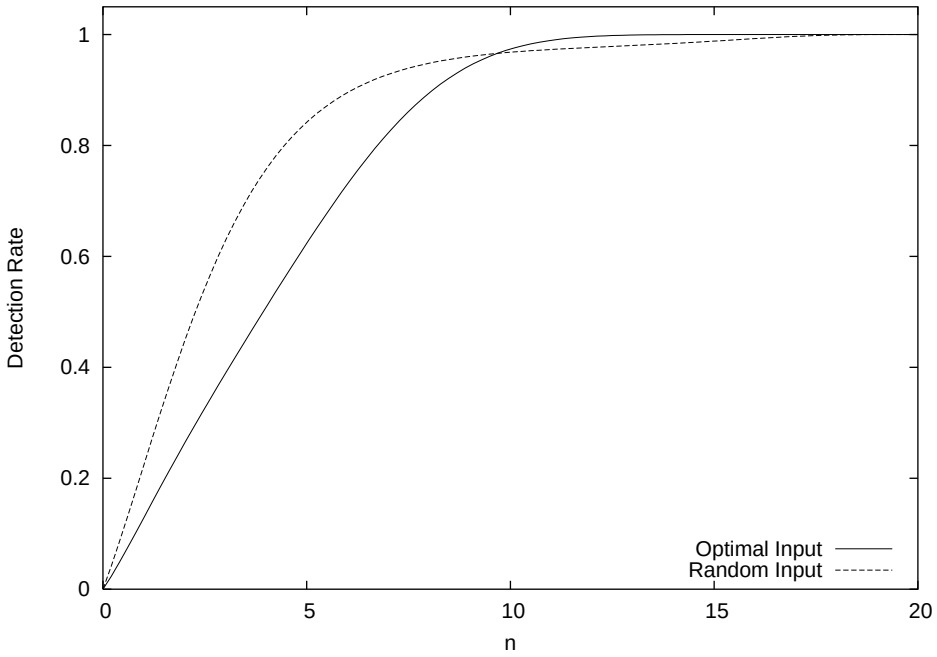

Figure 4.25: Optimal Input and Random Input (Hard Yield 90%, $1K \times 1K$)

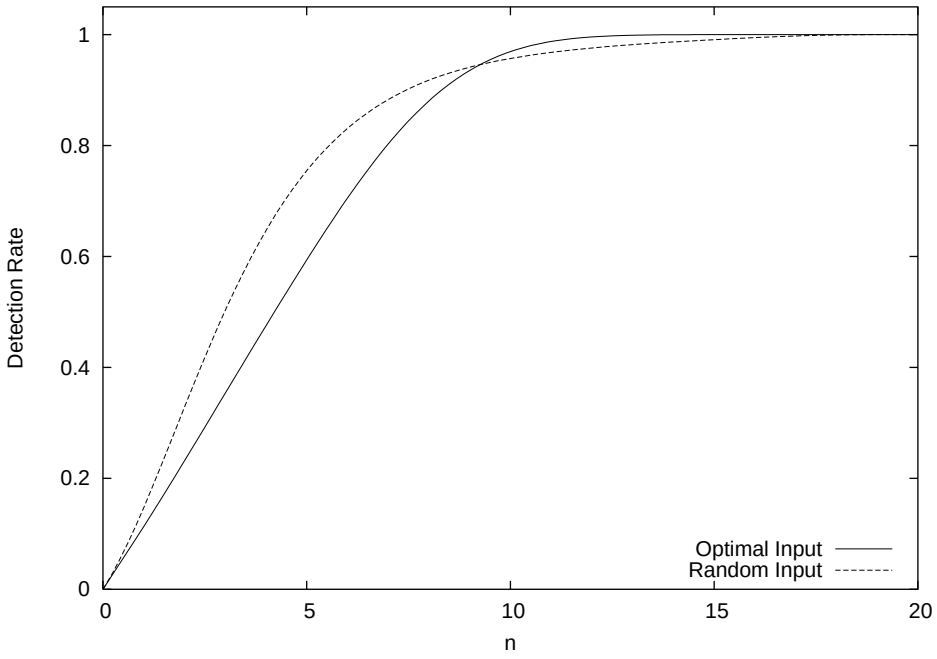

Figure 4.26: Optimal Input and Random Input (Hard Yield 93%, $1K \times 1K$)

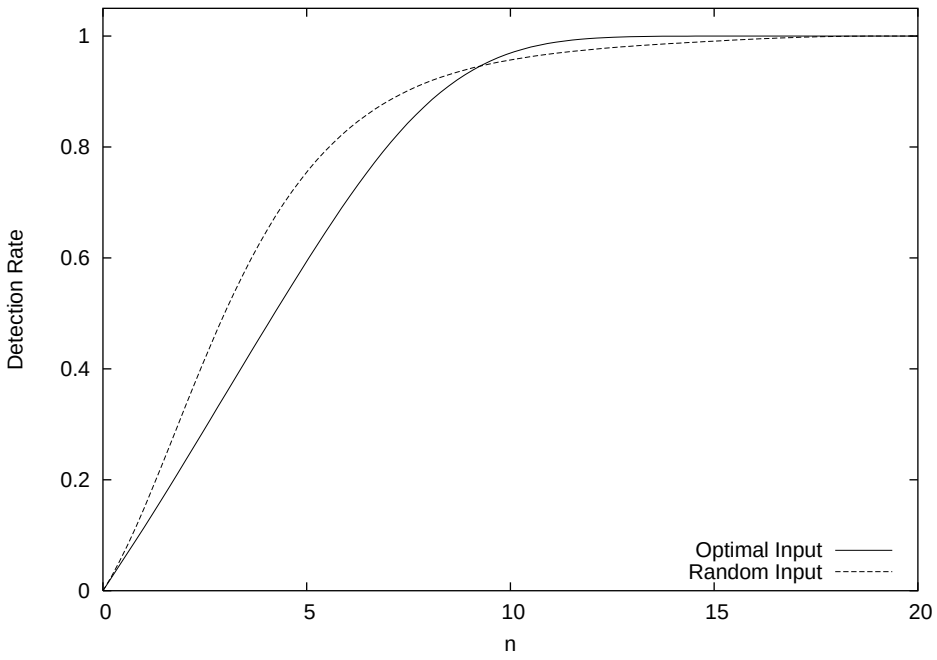

Figure 4.27: Optimal Input and Random Input (Hard Yield 97%, $1K \times 1K$)

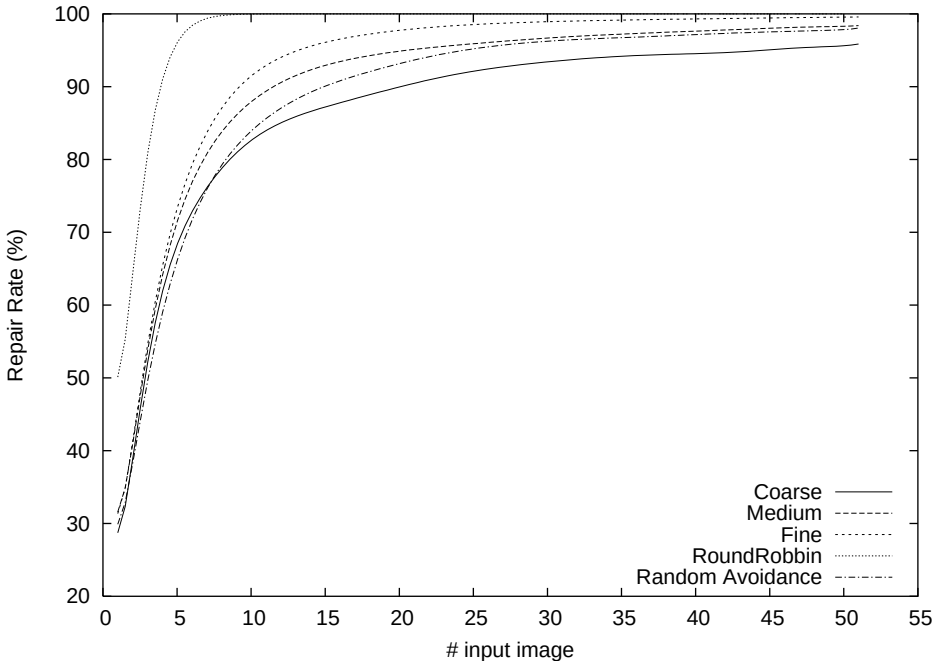

Figure 4.28: Optimal Input and Random Input (Hard Yield 90%, $1K \times 1K$)

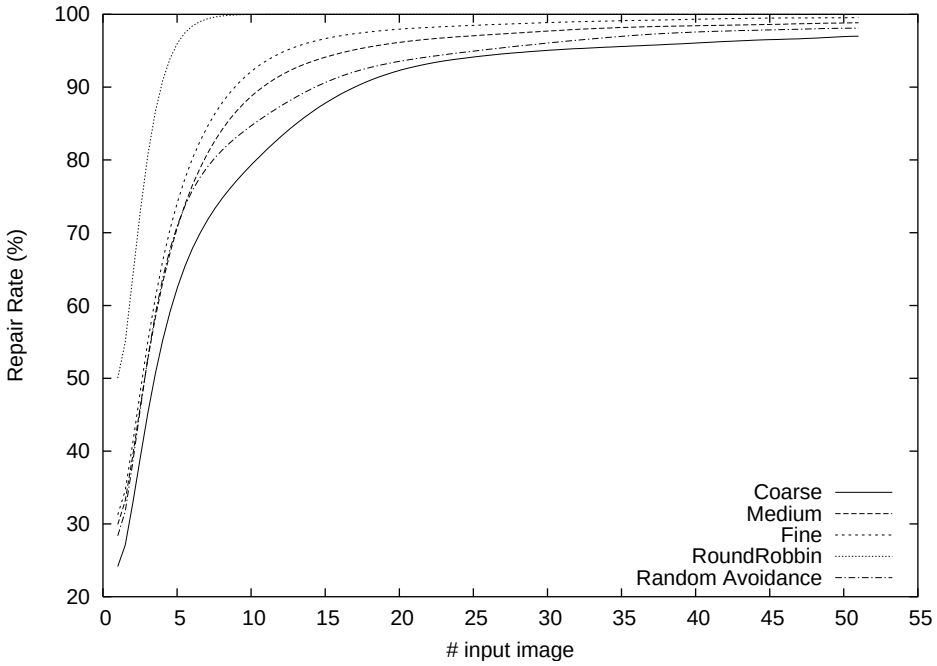

Figure 4.29: Optimal Input and Random Input (Hard Yield 93%, $1K \times 1K$)

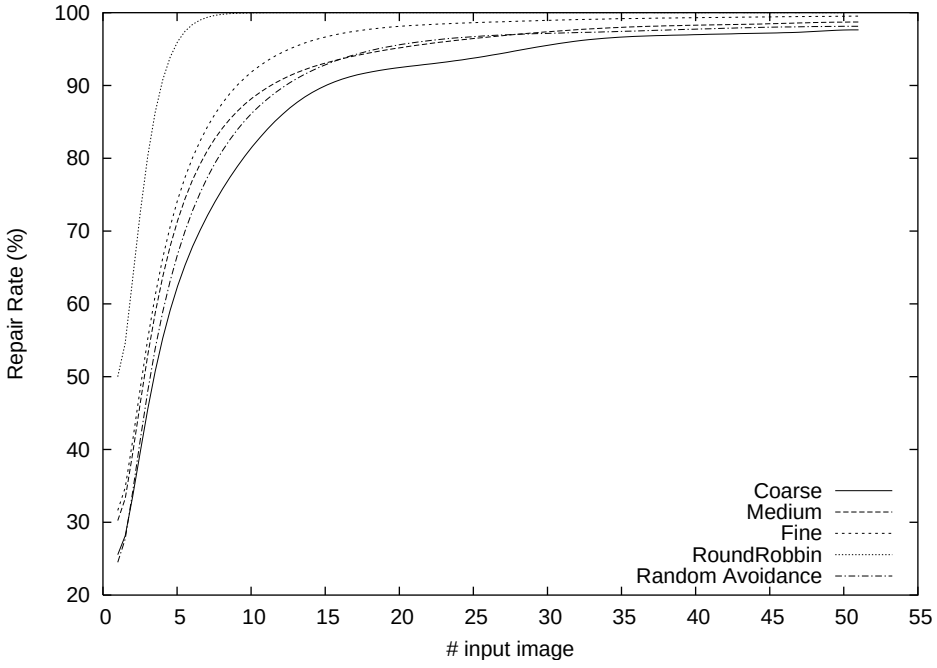

Figure 4.30: Optimal Input and Random Input (Hard Yield 97%, $1K \times 1K$)

4.4 Design of the Proposed Soft-Repair Circuitry

In this section, a circuit design for the proposed soft-repair is presented as a follow-on process to the soft-testing and as an integral part of the proposed design for reliability. The proposed soft-repair employs a *Built-In Self-Repair* (BISR) technique in orchestration with the circuitry for the BIST. The validity of the proposed theoretical soft-repair will be demonstrated through a circuit simulation. The BISR also performs a self-repair process online without intervention with the other normal CCD operations.

If a digital imaging system is deployed in a harsh environment without access to offline repair, online self-repair is an essential capability for successful fulfillment of a mission. CCD pixels are susceptible to excessive exposure to x-rays and can become defective [7, 8]. Therefore, the concurrent and combined on-line testing/repair capability in off-device mode will enable the BIST/BISR to provide a more stable and high-quality image than conventional on-device off-line-based image filtering methods.

The BIST tests for defective pixels based on input test image data and diagnoses it in order to build a cumulative map of the detected and diagnosed defective pixels, referred to as the *defective pixel map*. Then, the BISR performs a repair process with reference to the generated defective pixel map.

On the efficiency level, the BISR utilizes most parts designed for the existing functional modules arranged for the BIST, and the BISR also runs concurrently with the normal CCD operations. Hence, the circuit complexity can be moderately sustained without excessive increase in overhead cost. Cost-efficiency can also be achieved without sacrificing the performance of the entire system in terms of speed, and this will be theoretically and practically demonstrated.

In order to demonstrate reparability (i.e., the coverage of the repair process over

the number of defective pixels tested and diagnosed), the coverage of the proposed soft-repair at the circuit simulation level will be analyzed and evaluated concurrently with the soft-testing process and circuit simulation.

Finally, the theoretical yield improvement of the CCD shown in Chapter 2 will be validated through the simulation with the proposed BIST/BISR circuits.

This section is organized as follows: In Section 4.4.1, the proposed BISR architecture and the design are presented. In Section 4.4.2, the design and implementation of the proposed soft-repair algorithm is presented.

4.4.1 Proposed BISR for Soft-Repair

BIST circuitry is designed with the key functional modules such as pixel registers, adders, and comparators, and they are also utilized by the BISR for the design and performance efficiency as shown in Figure (4.31). In addition to those key functional modules, BISR accesses the defective pixel map that is generated by the BIST. The defective pixel map enables savings in the execution time of the overall soft-testing and repair process as it continues to cumulate and grow the map. The defective pixels captured in the map can be directly and selectively repaired without need for full re-test and diagnosis processes.

The operational flow of the BISR has additional steps to the flow of the BIST. While the storer, refer to Figure (4.31), in the BIST stores the test result into the flash memory, the storer in the BISR stores the repaired pixel values into the frame memory (thicker line in Figure (4.31)). Note that the proposed BISR design does not incorporate a parallel structure (i.e., only a single repair circuit) as shown in Figure (4.31) since the simulation results in Section 4.4.2 shows the repairing time is much shorter than the testing time.

Figure (4.32) shows the detailed circuit design for proposed BISR. The address generator computes an address to load a pixel value from the frame memory to a pixel

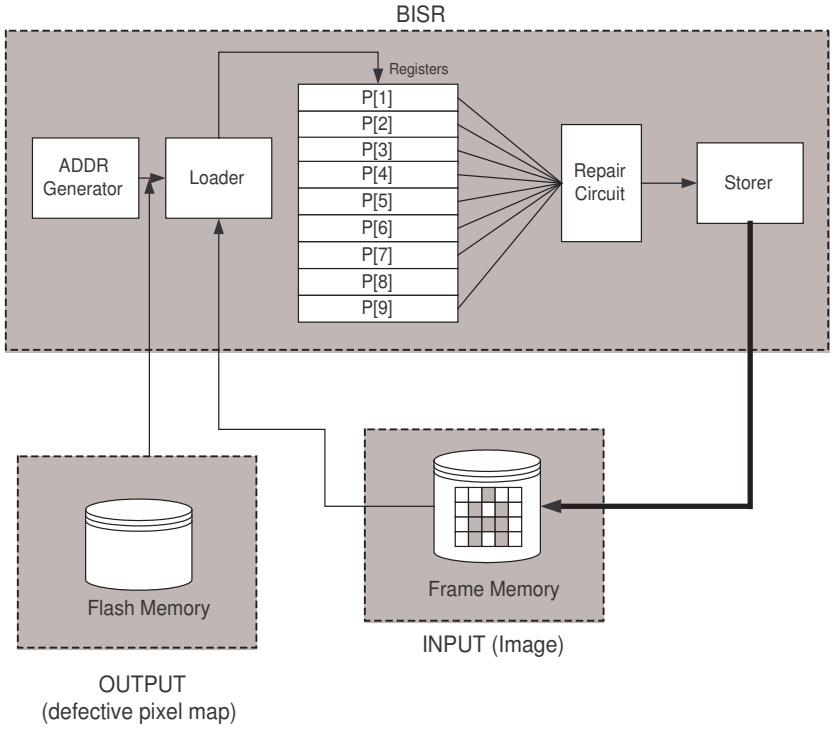

Figure 4.31: The proposed architecture for the soft-repair

register. The sequence of the addresses to be loaded is determined by the soft-repair algorithm to be employed. The SORT & SELECT 4 and DIVIDER are implemented to compute the threshold pixel value to be stored in the defective pixel map. Finally, the repaired pixel value will be stored back into the frame memory.

4.4.2 Proposed Base Repair Algorithm

The design and implementation of the proposed soft-repair algorithm is presented based on the repair model as was introduced in Chapter 2:

$$P(5) = \frac{\sum_{k=1}^{4} P(k) + \sum_{k=6}^{9} P(k)}{N} \tag{4.3}$$

where $P(1) \cdots P(4)$ and $P(6) \cdots P(9)$ are those pixels surrounding the pixel $P(5)$ under repair; and notice that this is a BISR architecture with $N = 8$. A detailed

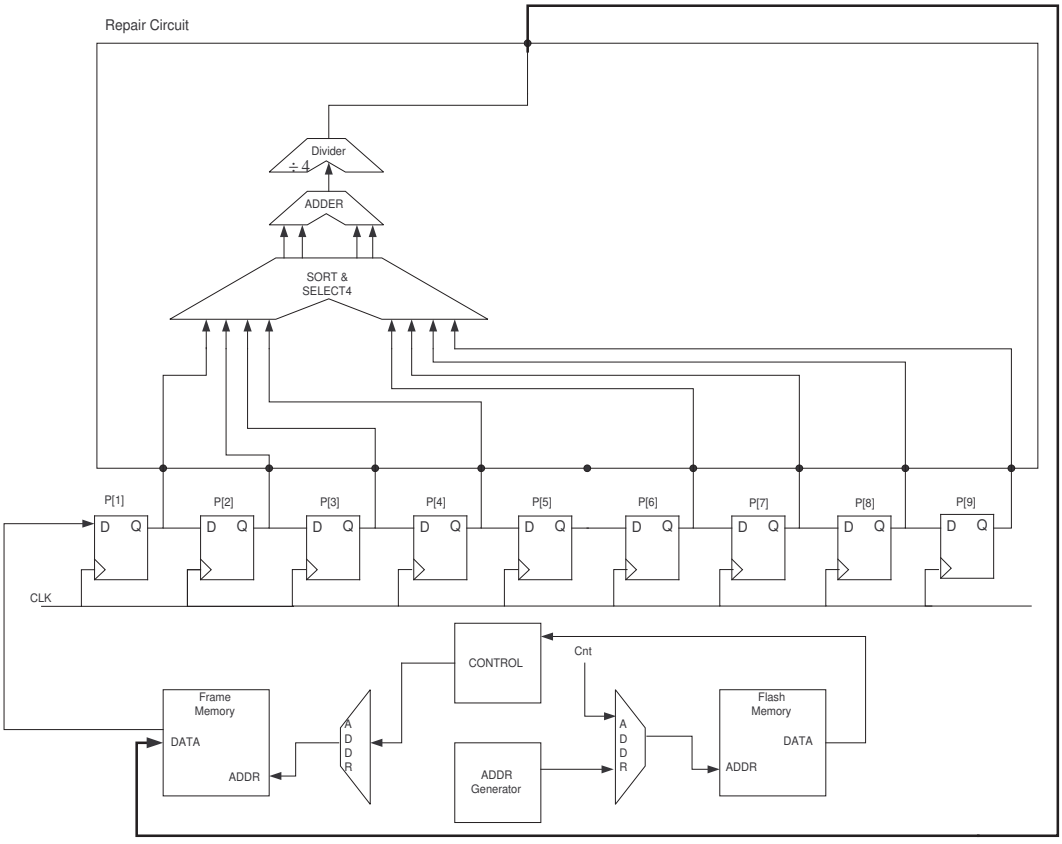

Figure 4.32: BISR Architecture

principle has been presented in Chapter 2 and is based on the general observation in digital imaging systems that the pixels tend to exhibit similar values around the average [9].

The design and implementation algorithms of the proposed BISR circuitry based on the Equation (4.3) is as follows:

```
CCD-REPAIR(P[])
1 for j <- 1 to NO_OF_CCD_COLUMN
2     do for i <- to NO_OF_CCD_ROW
3            do if LOOKUP(i,j)
4                   then LOAD(i,j,P[])
5                        SORT(P[])
6                        SUM <- P[3]+ P[4]+ P[6]+ P[7]
```

```
7                       AVG <- SUM / 4
8                       P[5] <- AVG
9                       STORE(i,j,P[5])
```

The for loop in line 1-2 iterates the repair procedure as many times as the product of the pixel number of columns of the CCD and the number of rows of the CCD (i.e., the entire CCD area); In line 3, LOOKUP function is called to refer to the defective pixel map by a coordinate (i,j); In line 4, the pixel values are loaded from the frame memory into the pixel registers P[ ]; In line 5, those pixel values are sorted, and in line 6-7, summation of the four core pixel values excluding the 2 darkest, the 2 brightest, and the average value (AVG) are computed; In line 8, the average value is stored back in P[5] for the pixel under repair; Finally, in line 9, the P[5] will be written back to the frame memory by STORE procedure.

The implementation flow of the above repair algorithm along with the proposed BISR architecture is shown in Figure (4.33). In step 1-2, an address under repair is generated. In step 3, the flash memory is referred to if the stored data is normal. If it is a normal pixel, it iterates back to step 1 to load the next pixel without a repair as given in line 3 in the CCD-REPAIR procedure; In step 4-6, the values of the pixel under test as well as the neighboring pixels are loaded into the pixel registers as shown in line 4 in the CCD-REPAIR procedure; In step 7 through 10, the sorting is performed as given in line 5 in the CCD-REPAIR procedure; In step 11, the selected 4 pixels (i.e., MMF) participate in the computation for AVG as given in line 6-7 in the CCD-REPAIR procedure; In step 12, the defective pixel is replaced with the average value that is calculated from step 11 as shown in line 8 and 9 in the CCD-REPAIR procedure.

Figure (4.34) shows the proposed repair process. The repair process repairs the defective pixels with the average of the medium four pixel values computed by the soft-repair. The address generator generates addresses of the entire CCD area. The

defective pixel map in the memory will be referred to determine if the pixels at the generated addresses are normal or defective, then only the defective pixels will be repaired. Note that the reasonable hard yield of CCD is more than 90%. Thus, the repair time is relatively short compared to the testing time since only 10% of pixels are to be repaired.

In order to evaluate the repair time by the BISR, a verilog HDL simulation is performed as follows:

1. Input the number of pixels of CCDs as follows: 64×64, 128×128, 256×256, 512×512, 1024×1024, 2408×2048, 4096×4096.
2. Input the hard yields of CCDs with 90%, 93%, 97%.
3. Generate 10% of defective pixels in each simulated CCD.
4. Repair each CCD.
5. Record repair time of the CCD.

The simulation results are shown in Figure (4.35).

By analyzing the result in Figure (4.35), the following can be observed.

- The hard yield CCD with 90% takes the longest repair time, and the hard yield CCD with 97% takes the shortest repair time since the repair time is increasingly proportional to the number of defective pixels.
- The longest repair time of CCD (90% 4096×4096) takes less than 2 second (1700 msec). From the above observation, it can be concluded that a parallel processing of BISR is not in urgent need.
- When window size is 5 sec, the BISR consumes 1700 msec, then 3300 msec will be used for testing. However, if the window size is less than 1700 msec, there will be no chance to find new defective pixels.

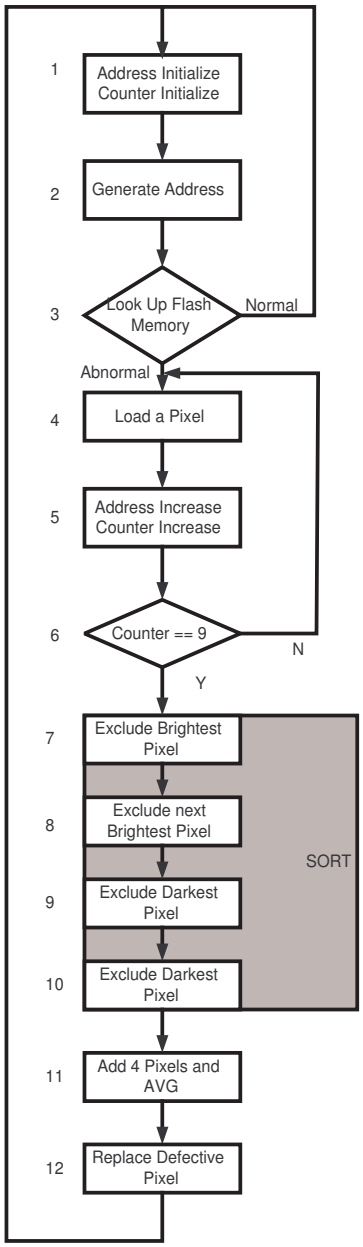

Figure 4.33: BISR Flow Chart

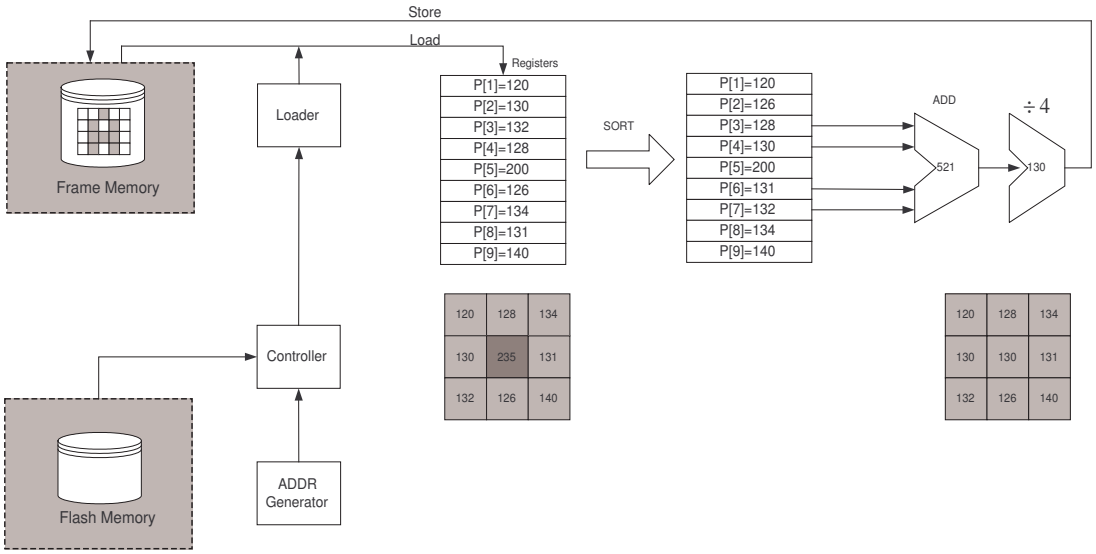

Figure 4.34: Repair of defective pixel

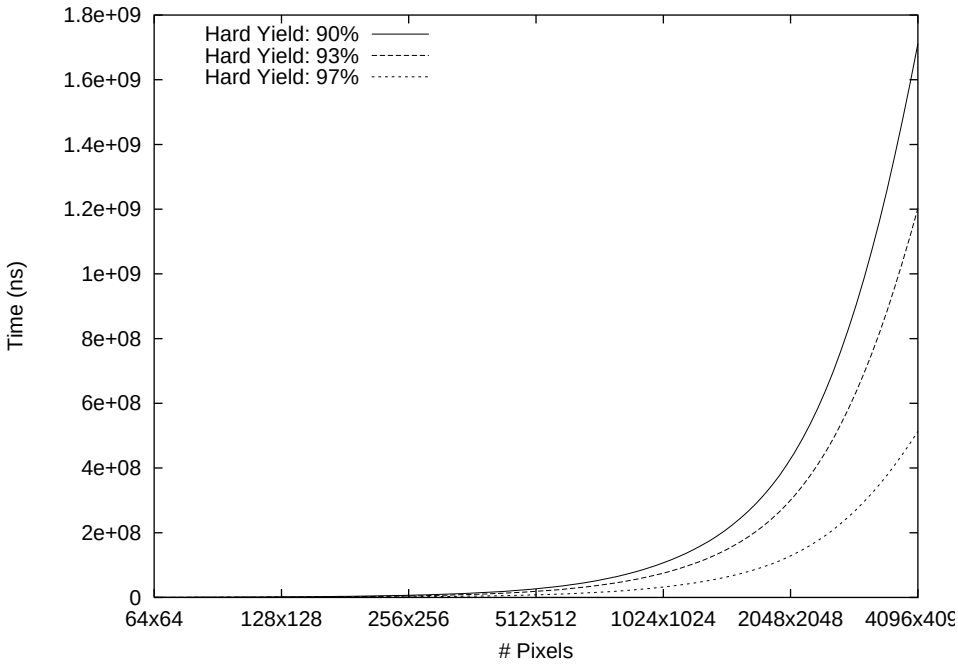

Figure 4.35: Repair Time by Number of defective pixels

4.5 Parametric Simulations

In this section, the effect of the proposed testing on the virtual yield of CCD will be evaluated through Verilog HDL simulation.

CCDs of 16 Mega pixels (4096×4096) are assumed in this simulation. Three CCDs containing 10%, 7% and 3% defected pixels are considered, respectively (i.e., 10% is $(4096 \times 4096)/10$). The defected images are generated as follows: Generate a random image; however, the image value should be in the medium range (i.e., gray color, not white, not black). Then, replace the normal pixel value with defective pixel value (i.e., white or black). The proportion of white and black is equal. For example, if a CCD contains 10% defective pixel, the CCD contains 5% of white and 5% of black pixel value.

For the simulation, six windows are used: $W = 5 \times 10^9 unit$, $W = 3 \times 10^9 unit$, $W = 1 \times 10^9 unit$, $W = 5 \times 10^8 unit$, $W = 3 \times 10^8 unit$, and $1 = 5 \times 10^8 unit$. Where a unit is one nano second.

It is revealed that the yield improvement of previous theoretical simulations in Chapter 2, Figures (2.6)(2.8)(2.10) show similar pattern with the yield of single Test Circuit BIST/BISR, Figures (4.36)(4.37)(4.38). Each simulation used the same factors. The exceptions are: 1. the number of pixels : Figures (2.6)(2.8) (2.10) are used 6 mega pixel CCDs and Figure (4.36)(4.37)(4.38) are used 16 mega pixel CCDs; 2. the window time: Figure (2.6)(2.8)(2.10) are simulated by three window scale and Figure (4.36)(4.37)(4.38) are simulated five window scale.

Figures (4.36)(4.37)(4.38) show the yield improvement by single Test Circuit for hard yield as 90%, 93%, 97% respectively. The higher hard yield CCD takes less time to approach 100% of yield. When smallest window is chosen, the yield improving time is 12 times longer than largest window chosen. Therefore, it is clear that a proper

window size should be chosen among various window sizes.

Figures (4.39)(4.40)(4.41) and Figures (4.42)(4.43)(4.44) show similar patterns with Figures (4.36)(4.37)(4.38) respectively. The speed up by multiple Test Circuit is remarkable. However, there is not much difference between 3 and 5 Test Circuit. From these simulations, it is revealed that 3 Test Circuit is enough to be both efficient and cost effective.

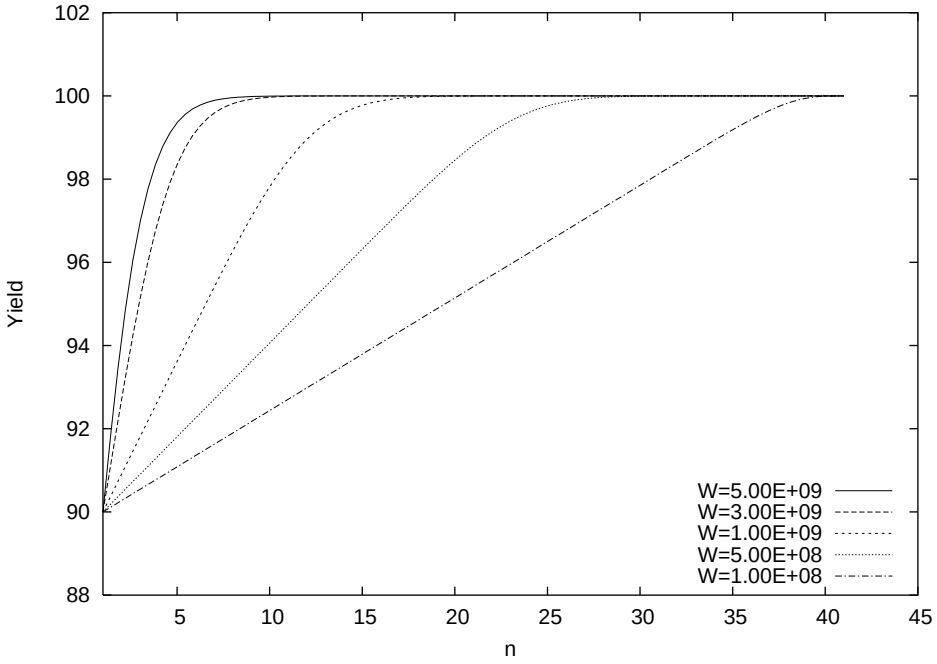

Figure 4.36: Test and Repair (Single Test Circuit and Hard Yield=90%)

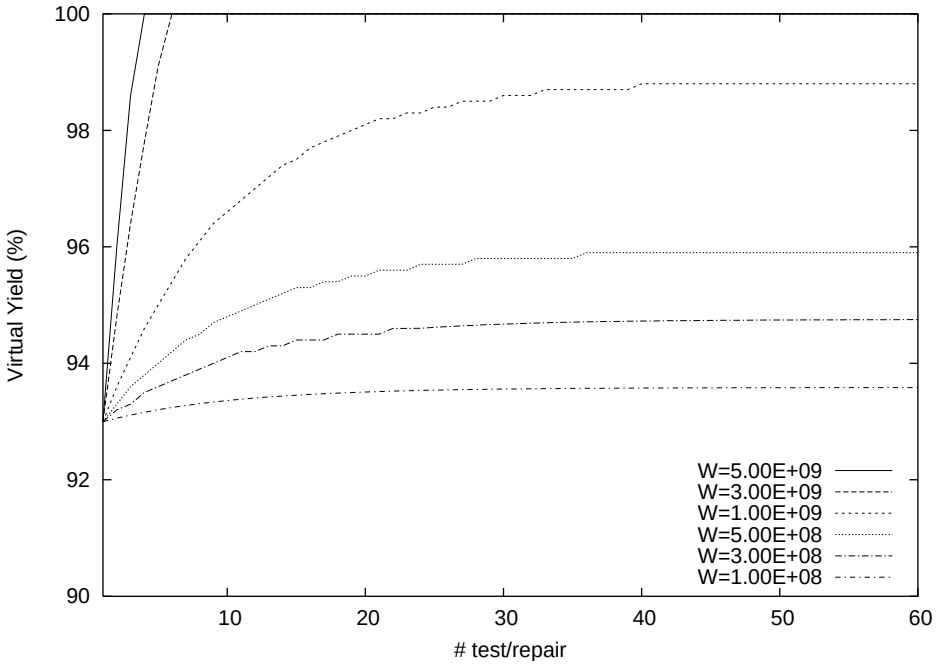

Figure 4.37: Test and Repair (Single Test Circuit and Hard Yield=93%)

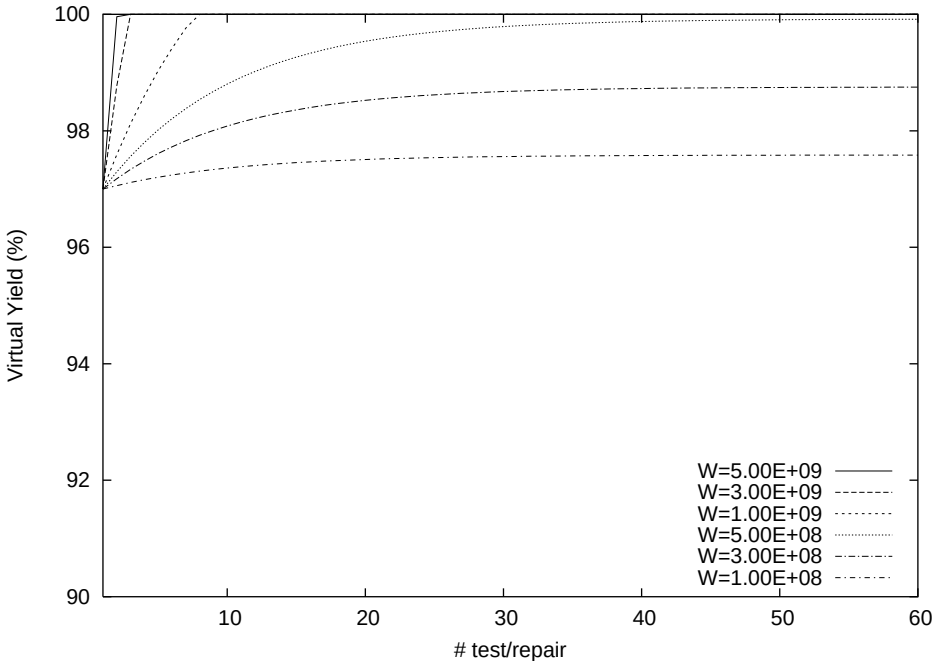

Figure 4.38: Test and Repair (Single Test Circuit and Hard Yield=97%)

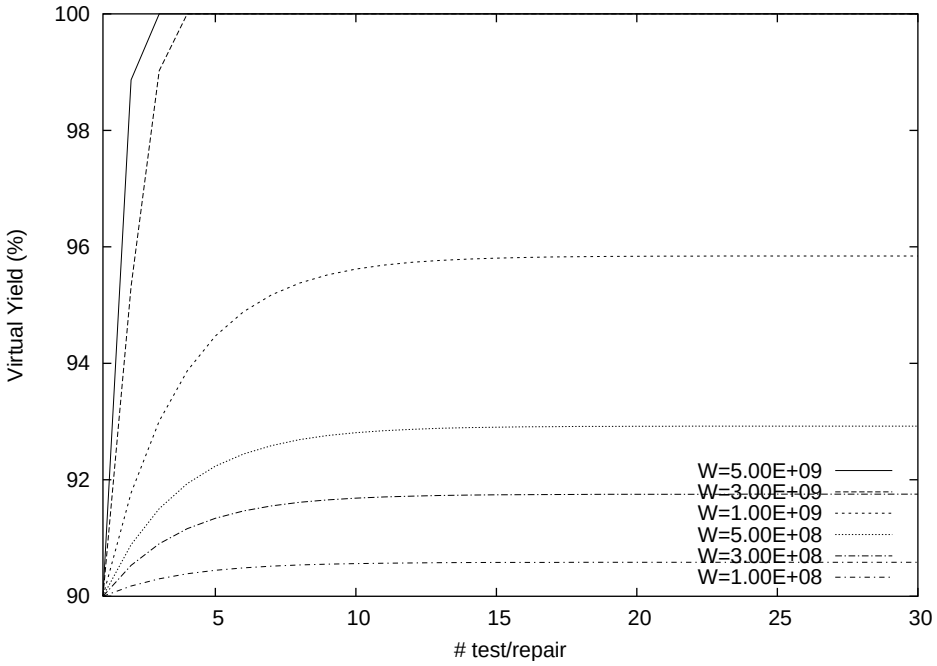

Figure 4.39: Test and Repair (3 Test Circuit and Hard Yield=90%)

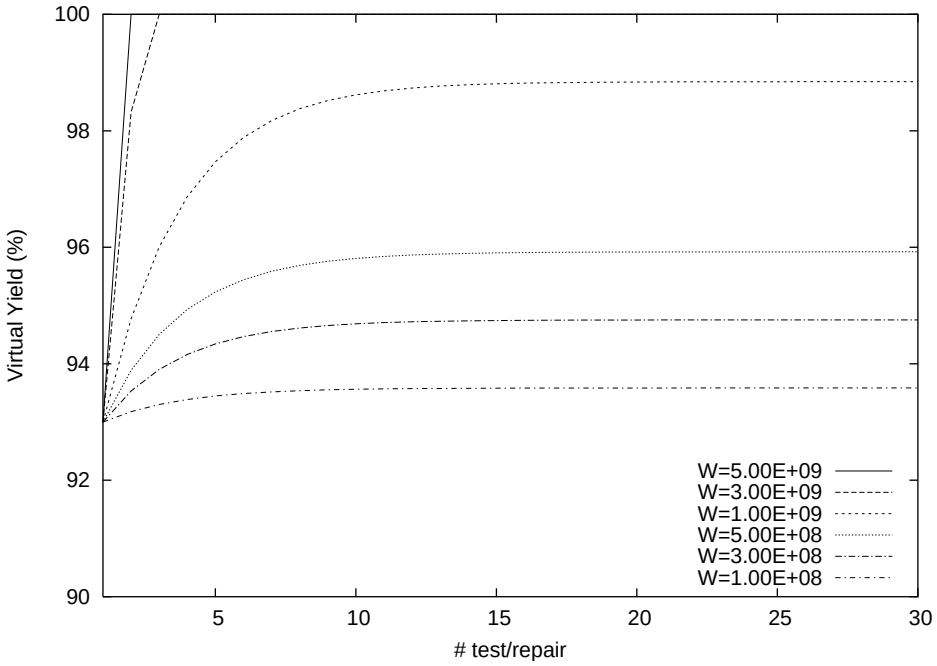

Figure 4.40: Test and Repair (3 Test Circuit and Hard Yield=93%)

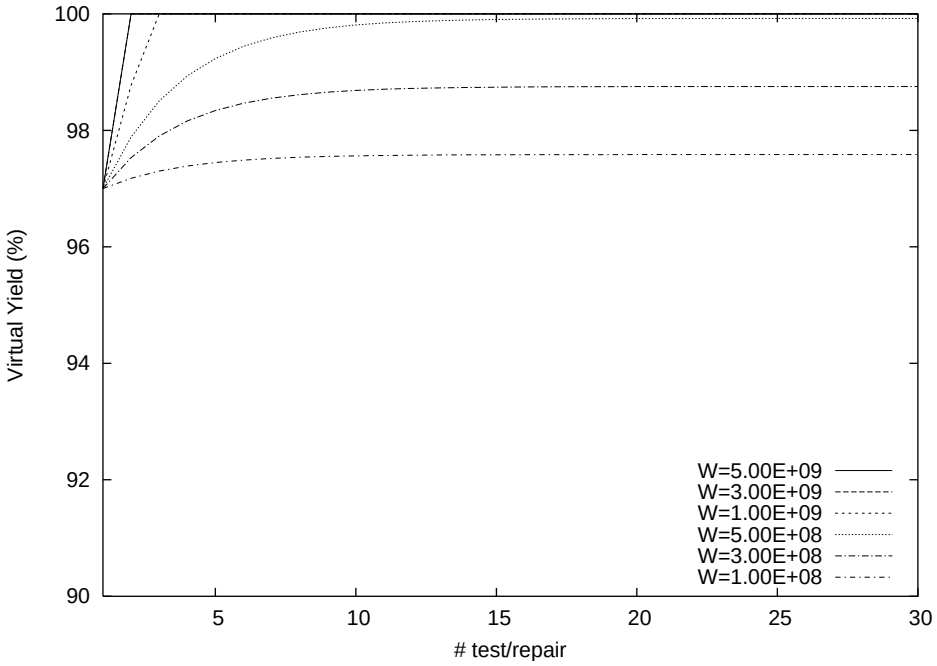

Figure 4.41: Test and Repair (3 Test Circuit and Hard Yield=97%)

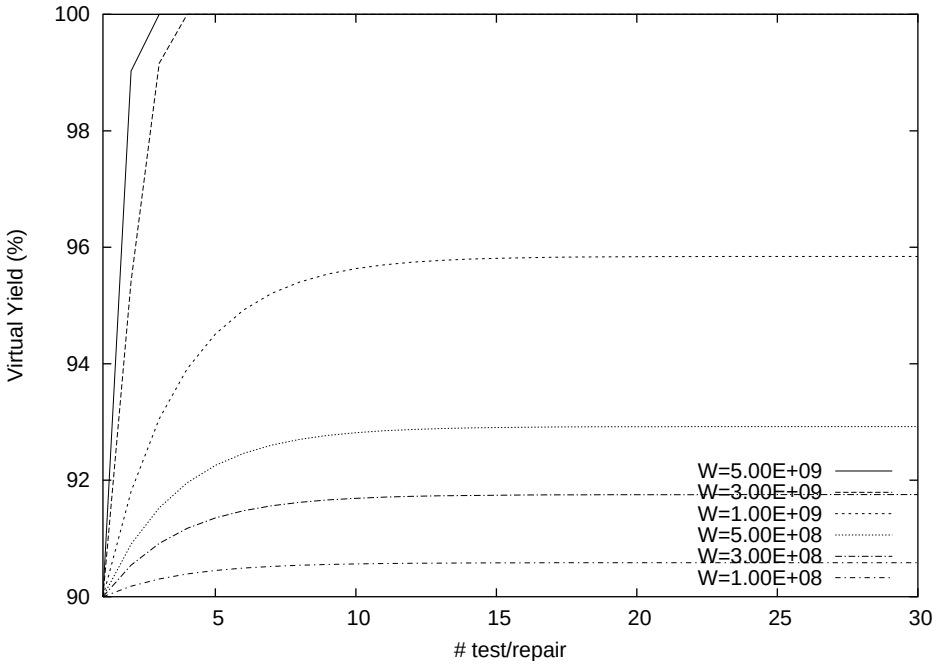

Figure 4.42: Test and Repair (5 Test Circuit and Hard Yield=90%)

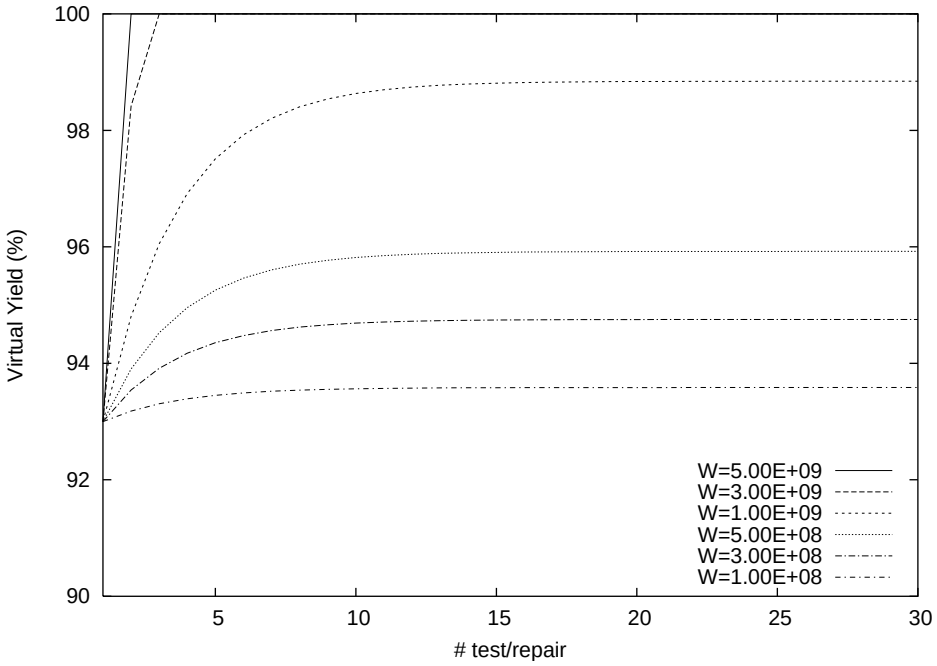

Figure 4.43: Test and Repair (5 Test Circuit and Hard Yield=93%)

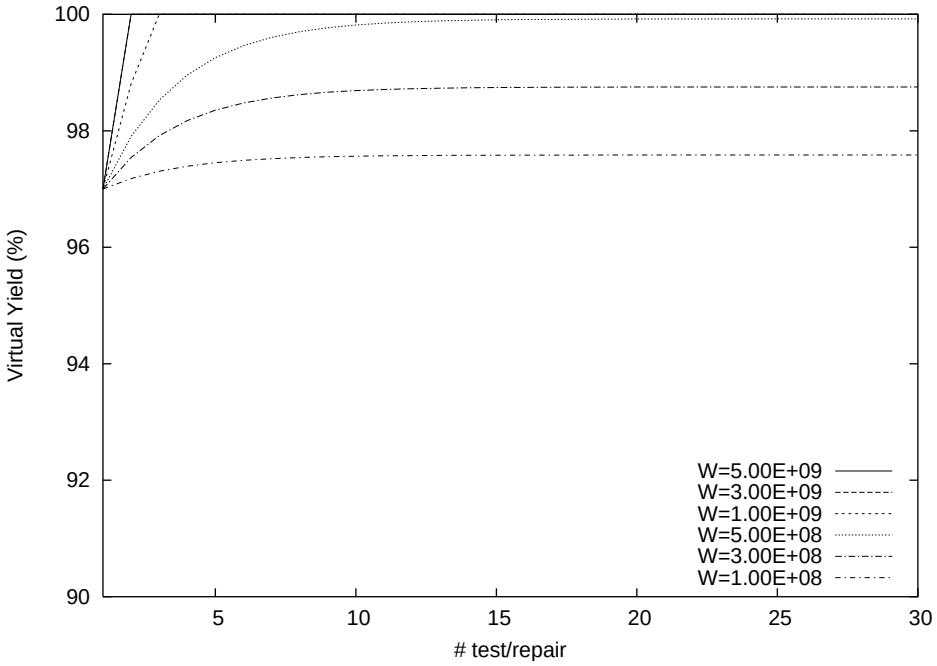

Figure 4.44: Test and Repair (5 Test Circuit and Hard Yield=97%)

4.6 Reliability

The reliability of the CCD pixels, especially in the proposed soft-test/repair model, could be modeled as M-of-N systems. The M-of-N system is a general model of an ideal parallel system. In CCD systems, the image pixels could be modeled as parallel systems since not all pixels should be working. However, certain numbers of neighboring pixels should be normal to test/repair. In M-of-N systems, M of total of N identical modules are required to function for the system.

The equation for the CCD pixel system could be given as follows:

$$R_{M-of-N}(t) = \sum_{i=0}^{N-M} \binom{N}{i} R^{N-i}(t)(1-R(t))^i \tag{4.4}$$

where

$$\binom{N}{i} = \frac{N!}{(N-i)!i!} \tag{4.5}$$

In case M is 4 and N is 8, the reliability will be as follows:

$$\begin{aligned} R_{4-of-8}(t) &= \sum_{i=0}^{4} \binom{8}{i} R^{8-i}(t)(1-R(t))^i & (4.6)\\ &= 38R^8(t) - 104R^7(t) + 224R^5(t) + 70R^4(t) & (4.7) \end{aligned}$$

R_{4-of-8} means that the CCD system can test/repair defective pixels up to 4 pixels out of 8. In other words, if the CCD system has 4 defective pixels, it is still considered as normal.

In case M is 4 and N is 8, the reliability will be as follows:

$$\begin{aligned} R_{4-of-8}(t) &= \sum_{i=0}^{4} \binom{8}{i} R^{8-i}(t)(1-R(t))^i & (4.8)\\ &= 38R^8(t) - 104R^7(t) + 224R^5(t) + 70R^4(t) & (4.9) \end{aligned}$$

R_{4-of-8} means that the CCD system can test/repair the defective pixels up to 4 pixels out of 8. In other words, if the CCD system has 4 defective pixels, it is still considered as normal.

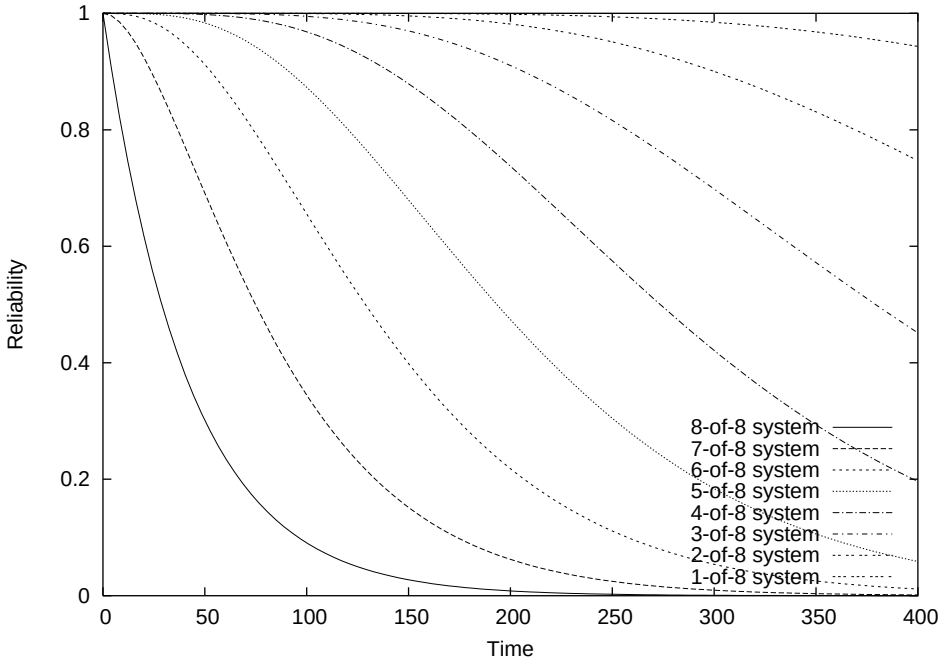

Figure 4.45: Reliability

4.7 Real Image Simulations

In this section, the real image simulation will be performed to prove the effectiveness and correctness of the proposed soft-test/repair method.

CCDs of 5 Mega pixels are used in this simulation. Three CCDs containing 10%, 7% and 3% defected pixels are considered, respectively. The defective pixels are added to the original images in randomly generated position.

The performance analysis of the proposed BIST/BISR was presented in a previous section (Section 4.5). In this section the real image simulation results will be provided, analyzed and compared with other graphic algorithms for the purpose of comparison.

By comparing the results in Figures (4.46)-(4.57), the following observations could be drawn.

1. The proposed soft-test/repair method repaired the defective pixels very clearly without showing any side effects regardless of the hard yield (i.e., 97%, 93% and 85%) as shown in Figure (4.49)(4.53)(4.57).

2. The average filtering partially repairs the defective pixels while experiencing severe side effects: The defective pixels are diffused to the neighboring pixels. In practice, the physically defected pixels might be considered to be repaired at certain levels while the neighboring pixels are corrupted by the defective pixels. As shown in Figure (4.47)(4.51)(4.55), the quality of image is not much improved.

3. The median filtering shows very good performance. The most common side effects of median filter, loosing small structures, are not showing in this simulation since the kenel size is 3x3. The pictures in Figure (4.48)(4.52)(4.56) show very strong noise suppressing effect. However, the filtering methods needs a

image mirror keeping the original image to avoid image corruption. This will hinder for hardware implementation.

4. The Peak Signal-To-Noise Ratio (PSNR) values are shown in Table 4.1. Soft-Test/Repair methods are superior to both filtering methods (i.e., AVG filtering, Median filtering) regardless of hard yield.

Table 4.1: Peak Signal-To-Noise Ratio (PSNR) of Images

H.Yield	AVG Filter	Median Filter	Soft-Test/Repair
97%	26.21 dB	30.08 dB	46.38 dB
93%	23.92 dB	29.27 dB	42.72 dB
85%	21.32 dB	27.99 dB	39.42 dB

From the above results and findings shown so far, it is very important to maintain a reliable design for imaging systems while suppressing side effect. The proposed image repair system shows very high reliability without side effects as well as high performance.

To suppress side effect, suppressing false detection is essential. In this simulation, the parameter C is utilized from Equation (2.1).

$$\left| \frac{\sum_{k=1}^{N} P(k)}{N} - P(0) \right| \leq C \tag{4.10}$$

where $P(1) \cdots P(N)$ are the surrounding pixels of the tested pixel $P(0)$ and the N is the number of surrounding pixels.

From the results in Figure (4.58)-(4.60), the following observations can be drawn.

1. The larger the value of C, the lower the detection rate as shown in Figure (4.58). In practice, the higher detection rate may also include the false detected

pixel ratio. Therefore, for accurate analysis, the false detection ratio should be considered.

2. The larger value of C lowers the false detection ratio as shown in Figure (4.59). From the result, a certain level of C value should be kept to suppress the false detection in the test/repair repair process.

3. Actually, the final yield of CCD, considering the false detection rate, is shown in Figure (4.60). At # test input = 30, the yield for C begins to decrease because of false detection. This means image quality could not be guaranteed.

4. As a result, it is revealed that the optimal C values without decreasing the yield of CCD are $C \geq 0.7$ from the Figure (4.58)(4.59)(4.60).

The virtual yield (Y_V) of CCD could be calculated as follows:

$$Y_V = Y_H + Y_{S,G} - Y_{S,B} \tag{4.11}$$

where Y_H is the hard yield of CCD, $Y_{S,G}$ is the improved yield by soft-test/repair, and $Y_{S,B}$ is the deteriorated yield by false detection. Figure (4.60) is drawn by Equation (4.11). The false detection term ($Y_{S,B}$) made a big difference from the theoretical CCD yield.

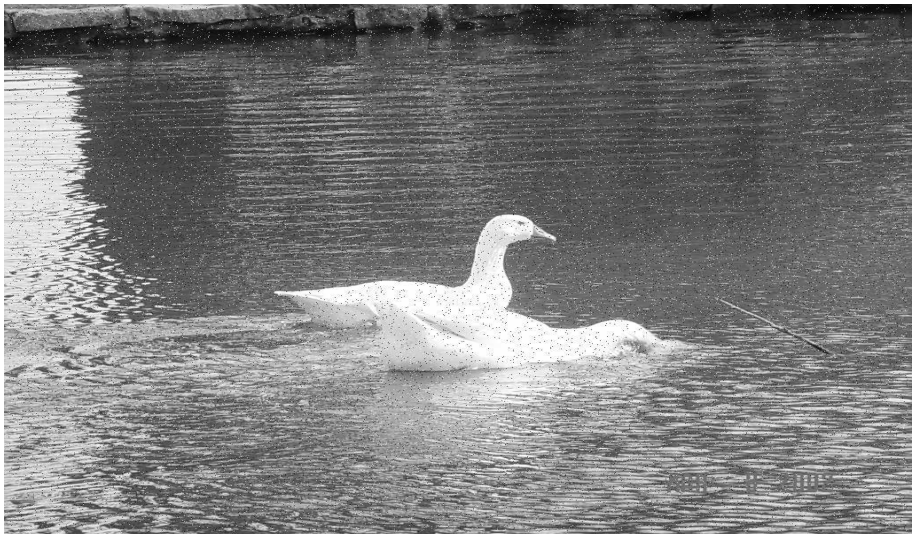

Figure 4.46: Faulty Image (H.Yield = 97%)

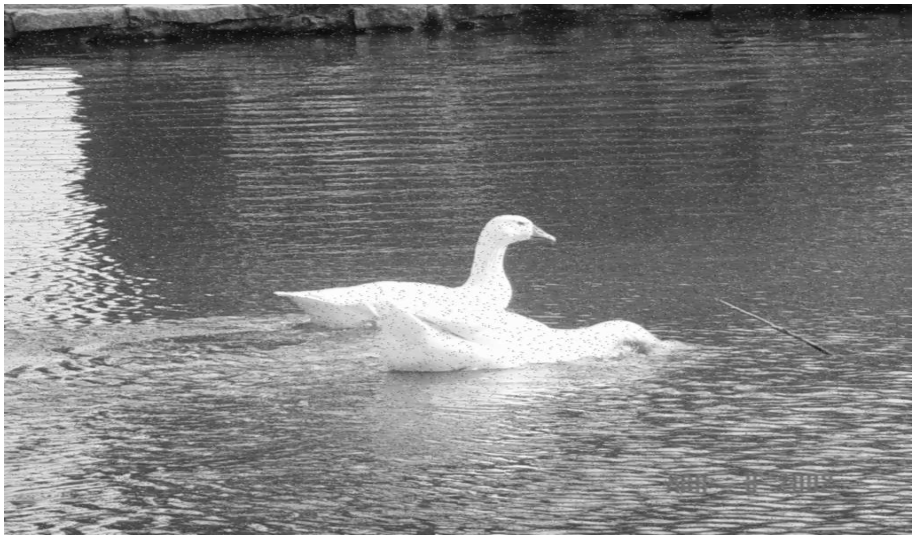

Figure 4.47: Image repaired by average filter (H.Yield = 97%)

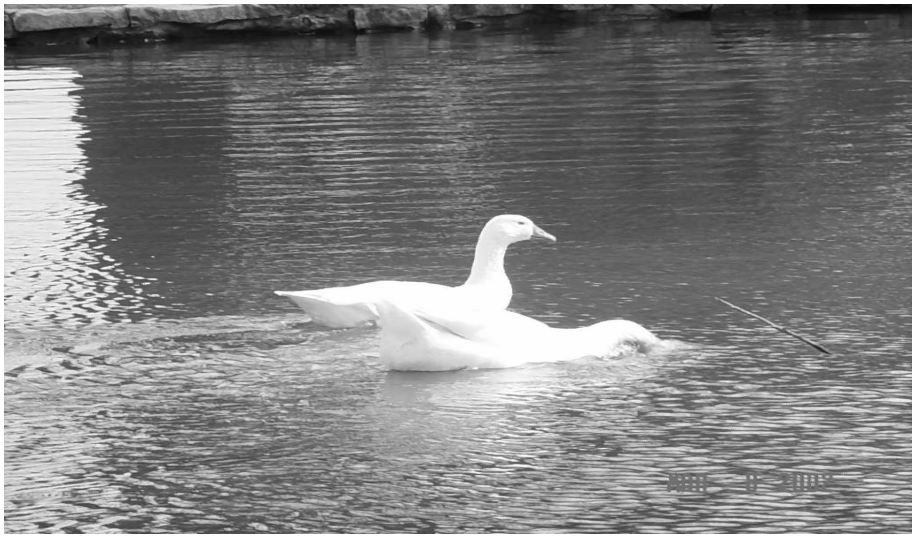

Figure 4.48: Image repaired by median filter (H.Yield = 97%)

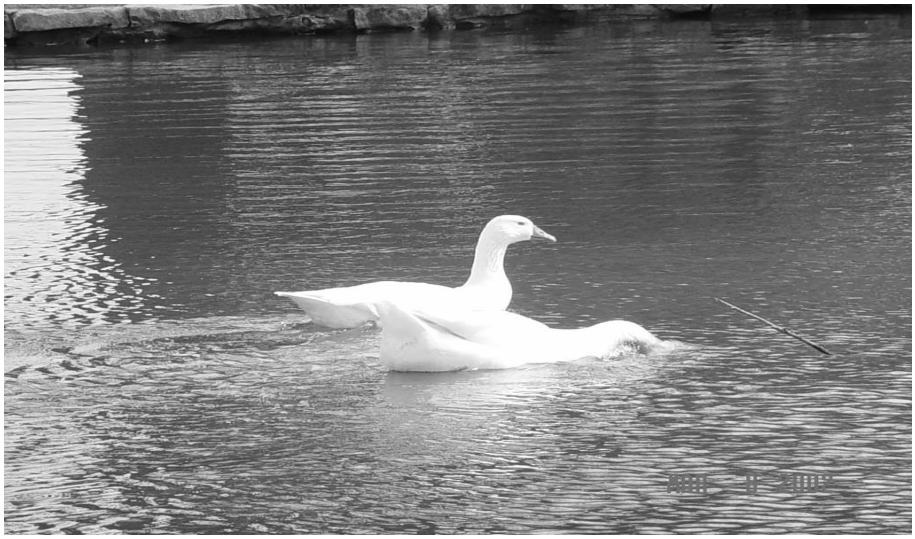

Figure 4.49: Image repaired by proposed algorithm (H.Yield = 97%)

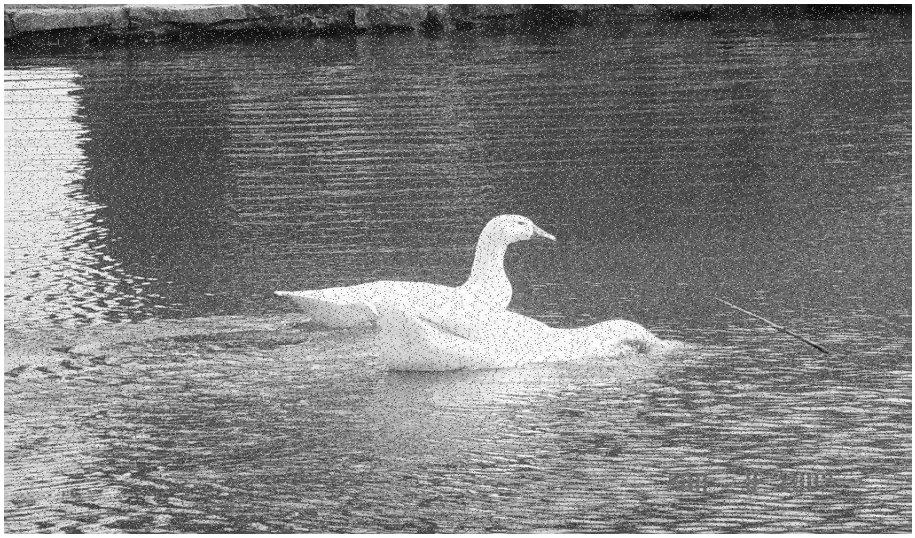

Figure 4.50: Faulty Image (H.Yield = 93%)

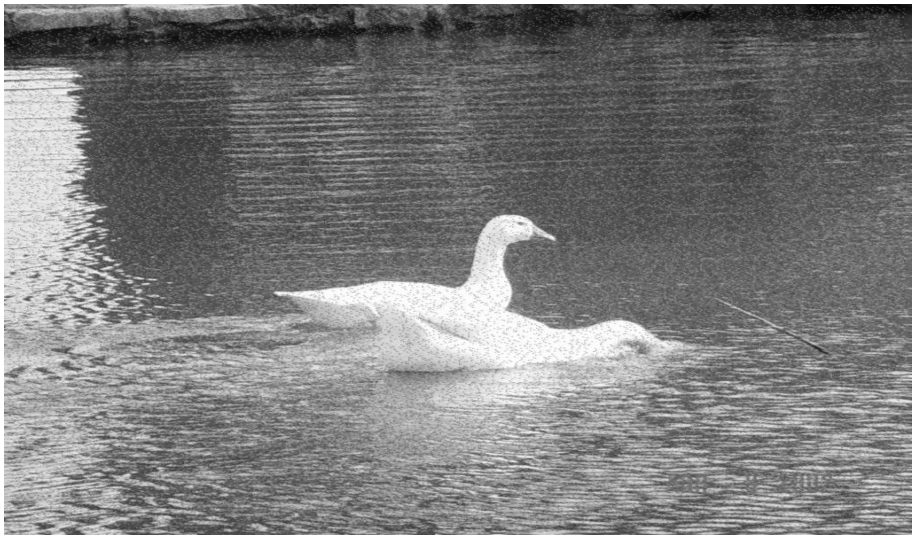

Figure 4.51: Image repaired by average filter (H.Yield = 93%)

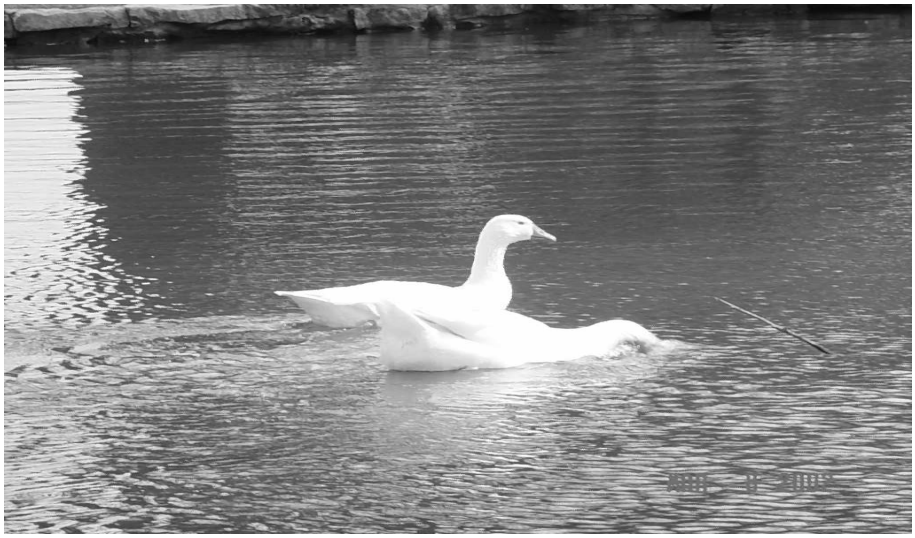

Figure 4.52: Image repaired by median filter (H.Yield = 93%)

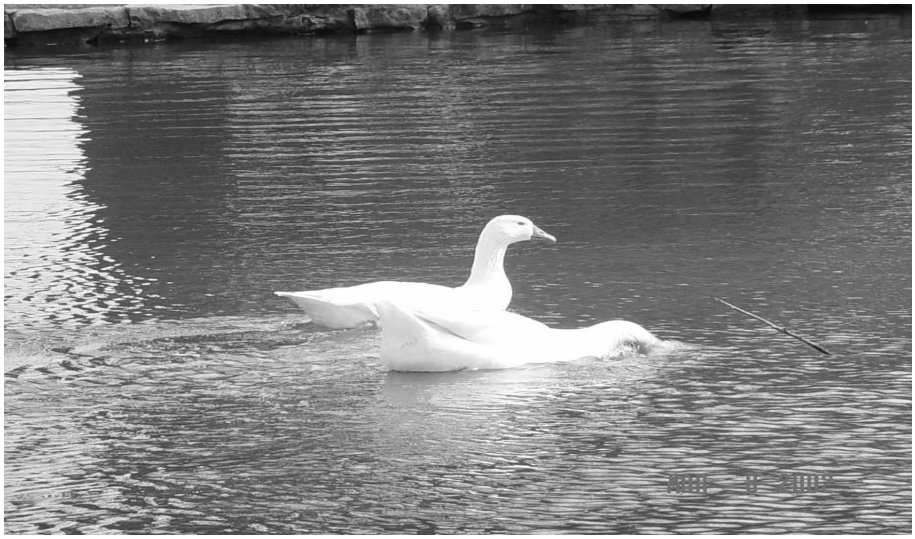

Figure 4.53: Image repaired by proposed algorithm (H.Yield = 93%)

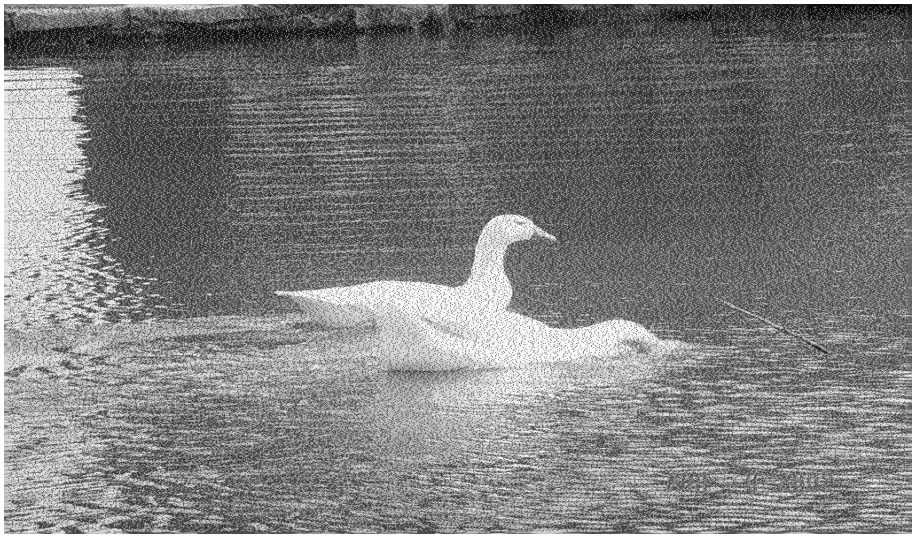

Figure 4.54: Faulty Image (H.Yield = 85%)

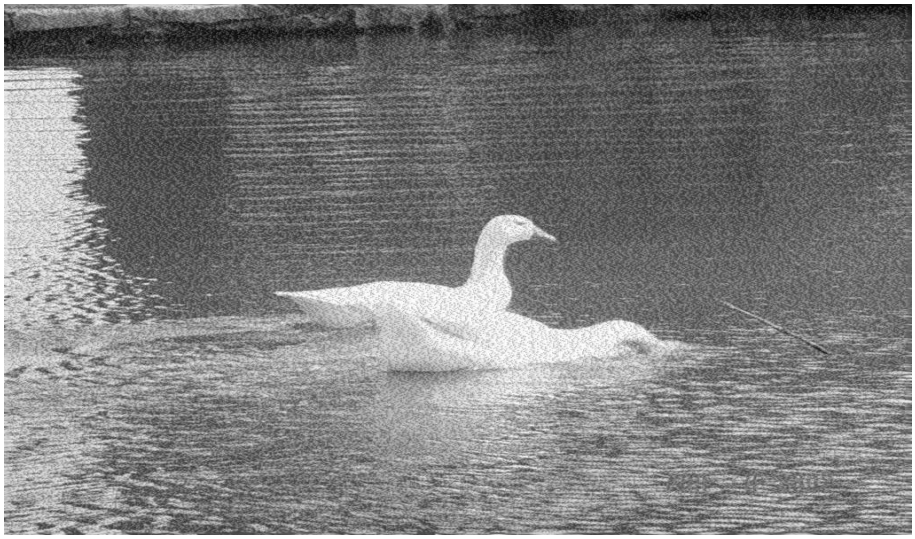

Figure 4.55: Image repaired by average filter (H.Yield = 85%)

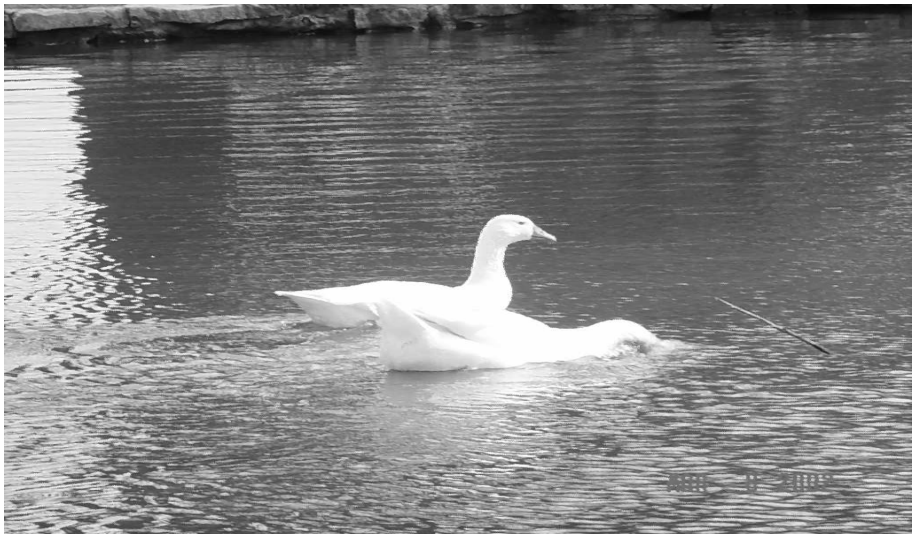

Figure 4.56: Image repaired by median filter (H.Yield = 85%)

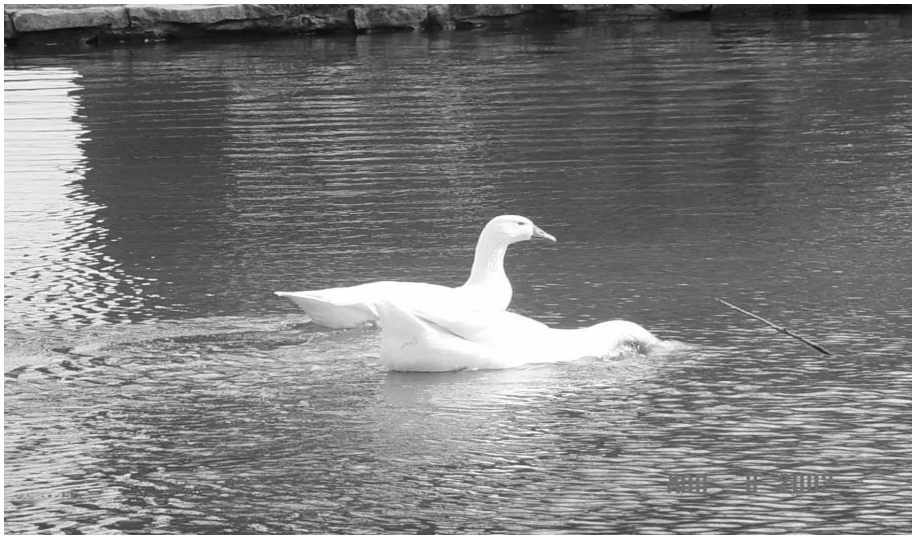

Figure 4.57: Image repaired by proposed algorithm (H.Yield = 85%)

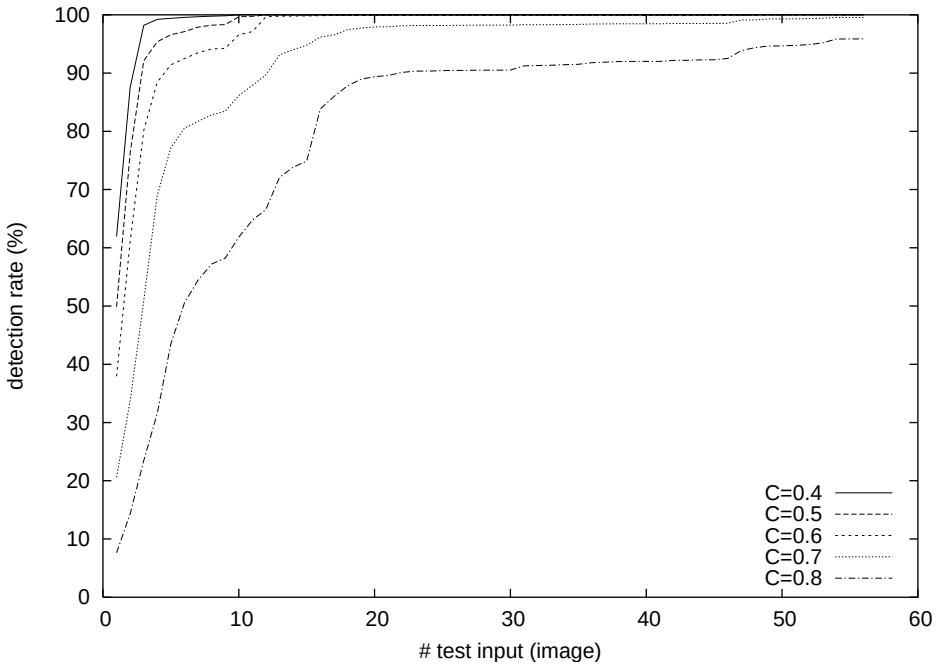

Figure 4.58: Detection Rate by C=0.4,0.5,0.6,0.7,0.8

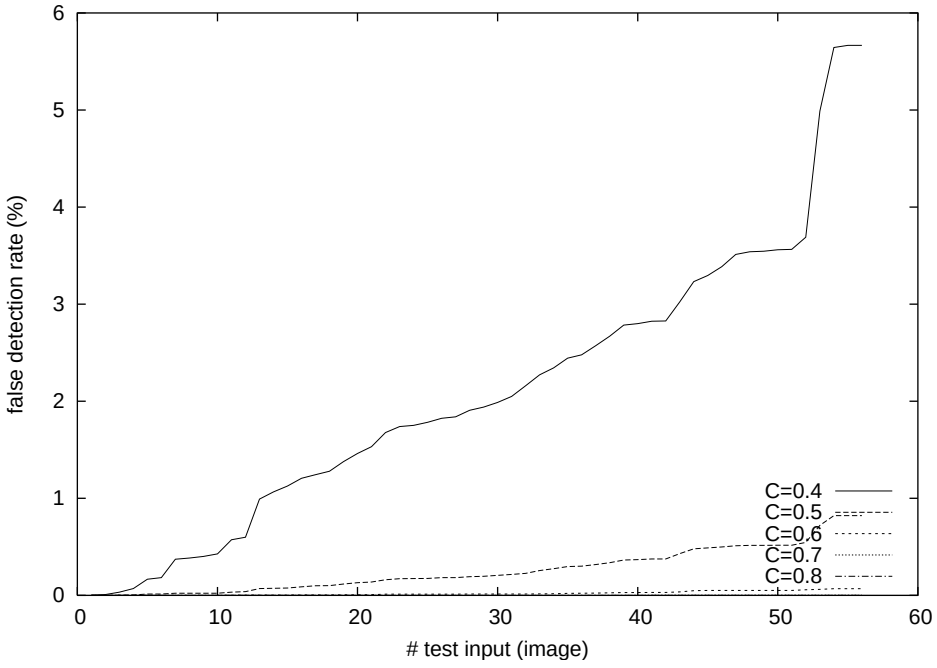

Figure 4.59: False Detection Rate by C=0.4,0.5,0.6,0.7,0.8

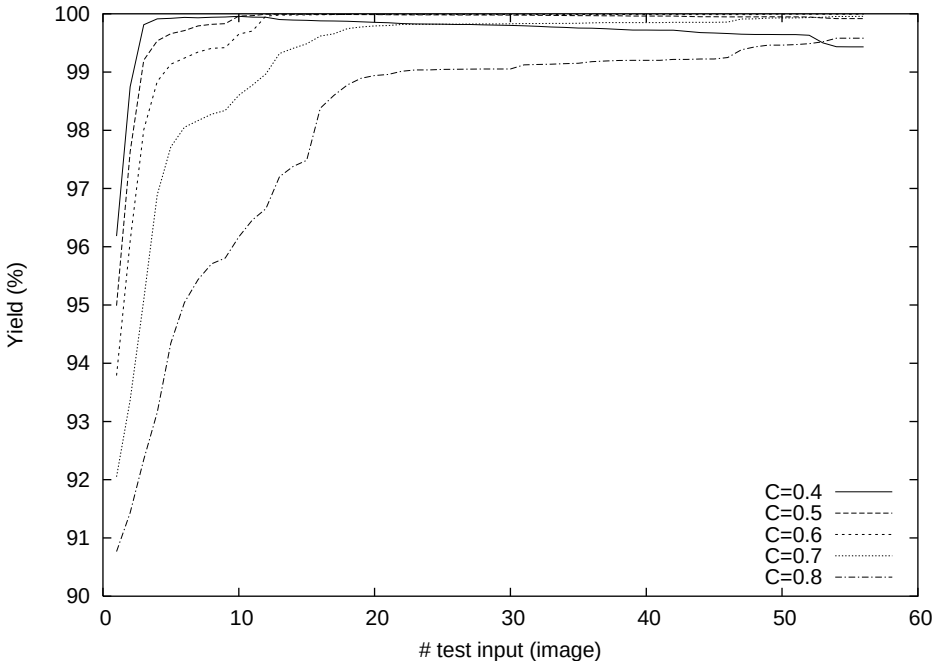

Figure 4.60: Yield of False Detection by C=0.4,0.5,0.6,0.7,0.8

4.8 Discussion

This work has presented a BIST/BISR design based on the soft-test/repair approach and various simulation results of the proposed BIST/BISR design. It has been revealed that BIST/BISR is the most efficient and cost effective testing methods in VLSI. There are many kinds of BIST/BISR; however, most of them are for memory or the combinational circuitry[18, 19]. The proposed BIST/BISR presents a novel and economic architecture on CCD testing and repair. To cope with huge image data, a multiprocessing technique is exploited. It is revealed that the proposed BIST/BISR design using the proposed soft-testing and repair process will outperform the conventional hard approach. From the simulation results, reliable designs of image systems while suppressing side effects are very critical. The proposed image repair system shows very high reliability without side effects.

CHAPTER 5

Discussion and Conclusions

In this dissertation, an extensive literature review of the CCD technology and its yield enhancement techniques has been conducted and a number of new issues associated with the CCD have been addressed and investigated. Fabricated CCDs must be manufactured in large quantities at competitive costs. Also, the CCDs must perform their function throughout their designed useful lifetime. Three specific research areas have been presented in this dissertation to demonstrate the importance of the CCD yield enhancement and reliability analysis by using the proposed soft-test/repair of CCD for yield improvement and the proposed CCD BIST/BISR architecture.

Chapter 2 presented a soft-test/repair approach for CCD-based digital x-ray systems through sound establishment of a novel theoretical modeling and analysis of the proposed test/repair procedure. It has been revealed that the yield of the CCD is one of the most critical components affecting the QoS (Quality of Service) of a digital X-ray system. There are two possible solutions to cope with the defective pixel problem in CCD. One is the hard-repair approach, and another is the proposed soft-repair approach. The proposed soft-repair approach circumvents defective pixels at the digitized image level. Therefore, it is inexpensive to practice and on-line repair can be done for non-interrupted service. It tests the images to find the defective pixels and filter the defects at the frame memory level, and caches them in flash memory in the controller for future use. The controller cache keeps accumulating all the noise coordinates, and preprocesses the incoming image data from the A/D converter by repairing them. The algorithms can be implemented on hardware level

(i.e., on the controller) to speed up the process. Unlike the calibration approaches shown in [9, 10], the proposed approach stores the noise history map dynamically on the hardware level and always keeps the up-to-date data within the proper window size. Numerical simulations have revealed that the proposed soft/hard approach using the proposed soft-testing and repair process will outperform the conventional hard approach after a certain break-even point in terms of virtual yield, thereby ultimately realizing a high QoS for digital x-ray systems.

In Chapter 3, clustered defective pixels modeling and repairing methods are proposed. It proposes how to test and find clustered defective pixel, and test methods have been presented. Digital image sensor devices such as CCD are, by their nature, can not readily utilize traditional on-device fault tolerance techniques because each pixel on the device senses a unique image pixel coordinate. No defective/faulty pixel can be replaced nor repaired by a spare pixel as any displacement of an original pixel coordinate can not sense the original image pixel. Therefore, to effectively provide and enhance the reparability of such devices with inability of on-device fault tolerance, a novel testing and repair method for defects/faults on CCD is proposed based on the *soft testing/repair* method proposed in our previous work [12] under both single and clustered distribution of CCD pixel defects. Also, a novel defect/fault propagation model is proposed to effectively capture the on-device defects and faults off the device for an effectiveness and practicality of testing and repair process. The efficiency and effectiveness of the method is demonstrated with respect to the yield enhancement by the soft-testing/repair method under a clustered fault model as well as single fault model, as referred to as *soft yield*. Extensive numerical simulations are conducted, and it has been demonstrated that the clustered fault model has a significant impact on the soft yield in comparison with the soft yield of the single fault model.

Chapter 4 has presented a CCD BIST/BISR design based on the soft-test/repair approach and various simulation results of the proposed CCD BIST/BISR design.

BIST/BISR is shown to be the most efficient and cost saving testing methods in VLSI. There are many kinds of BIST/BISR. However, most of them are used for memory or the combinational circuitry[18, 19]. The proposed BIST/BISR presents novel and economic architectures for CCD testing and repair. In order to process huge image data, concurrent and parallel processing techniques are exploited. It is revealed that the proposed CCD BIST/BISR design using the proposed soft-testing and repair process will outperform the conventional hard approach. The simulation results of real image testing/repair were performed and analyzed. It has been proved that the proposed soft test/repair methods is very efficient method for fixing defective pixels without loosing image quality.

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Scope and Method of Study: Charge Coupled Device (CCD) is one of the most popular imaging sensors such as digital camera, digital camcorders, and digital x-ray diagnosis systems to mention a few. As the need for high resolution and high sensitive CCDs, high yield and solid reliability are becoming critical requirements for CCDs. In this context, soft-test/repair method must be developed to achieve high yield and reliability for CCDs.

Findings and Conclusions: The purpose of this study was to propose soft-test and repair methods for defective pixels in CCD system, thereby realizing more reliable and cost-effective CCD Systems. Various test/repair algorithms are proposed and verified, and BIST/BISR architecture was proposed and the design was verified through verilog HDL simulation. Extensive parametric simulation results are also shown.

ADVISOR'S APPROVAL: Dr. Nohpill Park