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THE UNIVERSITY OF OKLAHOMA GRADUATE COLLEGE

DOWNHOLE DYNAGRAPH MEASUREMENT

A THESIS

SUBMITTED TO THE GRADUATE FACULTY

in partial fulfillment of the requirements for the

degree of

MASTER OF SCIENCE

By

GLENN DOUGLAS ALBERT

Norman, Oklahoma

1986

cop. 1

DOWNHOLE DYNAGRAPH MEASUREMENT

A THESIS

APPROVED FOR THE DEPARTMENT OF AEROSPACE, MECHANICAL

AND NUCLEAR ENGINEERING

By

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Also to Carl Adams for his assistance with the hardware development and Jesus Chacin for his work prior to the author's involvement, and continuous assistance and support throughout.

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Finally, to my beautiful wife, Joy, and loving children Jennifer and Blake, who are motivational by existance and whose support and loving tolerance made the successful completion of this project a reality.

GLENN D. ALBERT December, 1986

ABSTRACT

While various mathematical models exist for predicting downhole forces and motion in sucker rod type pumping systems, none have been thoroughly verified with actual measurements. In fact, downhole force measurements were last made in 1942.

This report documents the development and use of a downhole data acquisition system designed and built to dynamically measure force and displacement at the bottom of the hole.

The system consists of a microcomputer, memory storage, power supply, and transducers, designed to fit collectively in a volume slightly over one inch in diameter by five feet in length.

Downhole dynagraphs and other data recovered from over one mile in the ground are presented.

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DOWNHOLE DYNAGRAPH MEASUREMENT

CHAPTER I

INTRODUCTION

In the oil production industry there is a graphic method for observing the general pumping conditions, of an artificial lift type well, known as a dynagraph. A dynagraph is a display of the polish rod load versus the position in the pump stroke and is normally plotted over a single pump cycle as shown in Figure 1.1. For the past 60 years the dynagraph has been useful in measuring well performance and diagnosing trouble conditions downhole. More

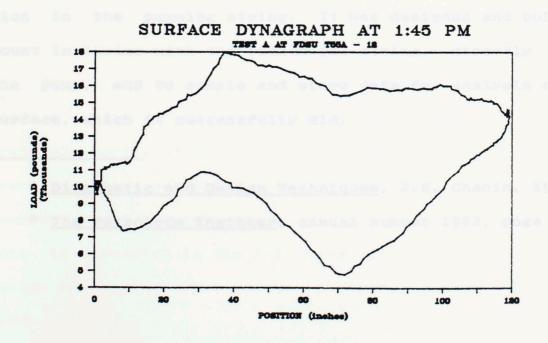


Figure 1.1 Surface dynagraph FDSU T55A - 12, 08-28-86

recently surface dynagraph data, with other well-specific parameters, has served as input to mathematical models for predicting downhole behavior, particularly a predicted dynagraph at the pump (which is located at the well bottom). Various computer programs to perform this task have been written (reference 1), none of which have been thoroughly verified empirically. In fact, no downhole measurements have been taken since 1942 by Lamberger and Langer (reference 2).

The task of this research was to conceive and build a modern apparatus to take downhole data to support or refute said models.

The resultant apparatus is a microcomputer-based data acquisition system that takes real-time measurements of multiple parameters, under the constraints of a downhole section in the pumping string. It was designed and built to mount in series with the sucker rod string, directly above the pump, and to sample and store data for analysis at the surface, which it successfully did.

Diagnostic and Design Techniques, J.E. Chacin, 1986

The Petroleum Engineer, annual number 1942, page 206.7

CHAPTER II

DESIGN SPECIFICATION

The primary motivation for this project was the need for experimental data to support Jesus Chacin's doctoral research work and computer program for predicting downhole behavior. As a result, the early design needs were already defined and the product definition resulted from our combined thoughts and discussions on what was important and feasible. Subsequent meetings with both Jesus and our mutual advisor, Dr. John C. Purcupile helped establish a good, practical approach to achieving these goals, specifically the hardware implementation.

2.1 Goals

The objective was to produce an apparatus that could be readily attached in series with the sucker rod, sent to crude oil depths of roughly 7,000 feet, withstand 10,000 pound tensile, and 2,000 pound compressive loads, and, of course, yield accurate data. (the quality and quantity of data is discussed in the following section). The inherent design constraints were space, pressure, temperature, and time.

2.2 <u>Constraints</u>

2.2.1 Space

Recognizing the potential hazard of introducing an unproven foriegn object into a well, standard oil field hardware was selected to contain the apparatus and attach it in the string. The standard Harbison-Fisher tubes and connectors detailed in appendix B are readily available in a variety of sizes and lengths and were the selection for this project. The dimension of primary concern and the main spatial constraint was the diameter of the tube which is 1.312 inches (1-5/16 inches, 33 mm). The design was virtually unconstrained in length though it was desirable to keep it short for handling and testing, and a stock length was desired to minimize cost.

2.2.2 Pressure

The apparatus had to be sealed to protect the electrical circuits and transducers from the external fluid being pumped. Having specified an adequate limit for the maximum depth of expected operation of 7,000 feet, the apparatus would have to withstand 3,000 psi static pressure and another 10% dynamic variation from pumping accelerations of approximately 0.10 g. The apparatus was designed and tested to 5,000 psi, sufficiently greater than the 2,500 to 3,000 psi experienced in the downhole test.

2.2.3 Temperature

The geothermal gradient in the first few miles of the crust of the earth is +1.6 degrees F per 100 feet (starting at 50 degrees just below the surface), with some variation for localized geothermal sources. At 7,000 feet a temperature of just over 160 degrees F could be expected which was an initial guideline for the temperature constraint. However, another line of constraint of great significance is the allowable operating temperature of the electrical components which are generally available in three temperature grades; 70, 85, and 125 degrees C. Besides the substantially higher cost of the higher temperature grade devices, initial parts sourcing revealed the availability of the chosen memory chips (to be discussed in the controller section) in only the lowest grade which forced the temperature specification of the apparatus to match. The temperature limitations of all other devices used, electrical and mechanical, would meet or exceed this limit of 70 degrees C.

2.2.4 Time

Today's low power, silicon technology provides the capacity for data storage of thousands of bytes on a single chip. The approach of a self-contained electronic apparatus with memory was conceptually superior to, and more practical than a tethered subassembly that received power, and trans-

mitted data over thousands of feet of cables, as was done in 1942. The device would then naturally be battery operated and, due to the exhaustable nature of batteries, this posed a time limitation on the useful duration of application of the apparatus.

A typical workover crew can run 7,000 feet of sucker rod, up or down, in one to two hours. Without adding to the fluid level from the surface it can take a well of this depth two to three hours to stabilize. If measurements of a stabilized well were desired and the apparatus were to require power the entire time it was in the ground, than a minimum of seven hours of battery life would be required. With the use of CMOS (Ceremic Metal Oxide Semiconductor) electrical components, wherever possible in the design, for extremely low power dissipation, the application of the only high-temperature dry cells (see Chapter 3.2) found on the market would exceed this duration goal by a factor of ten.

An added plus for the battery requirements here is the selection of the memory devices (GI-28C64 8kx8 EEPROM) which, are not only CMOS but also non-volatile, which means that once written to, they retain data indefinitely without presence of power. The benefit of this choice of memory is that the batteries need only last through the completion of the data taking period. Under normal operation this has little significance because of the excessive capacity of the batteries. But this feature is extremely valuable in the

event of a mishap that would strand the apparatus underground for several days, or if it were damaged during removal or dissassembly.

The Development section explains more fully how each of these constraints was addressed, designed and/or tested for before the downhole test.

CHAPTER III

DEVELOPMENT

The block diagram of the system in Figure 2.1 shows the three basic elements of the design; transducers, controller, and battery pack. The physical containment or case, with strain gages mounted to its inner wall, is itself a transducer.

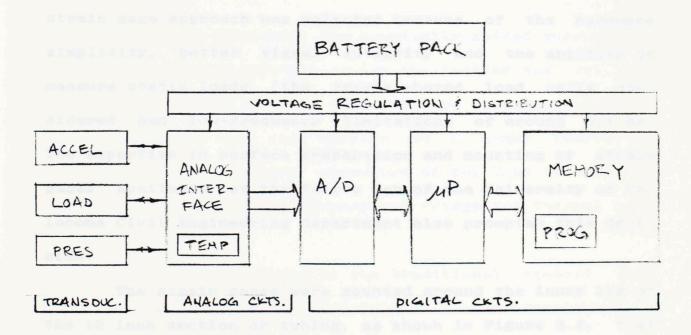


Figure 3.1 System Block Diagram

3.1 Transducers

Four variables, two primary and two secondary, are transduced within the apparatus; axial load, axial acceleration (to derive displacement), external pressure on the ap-

paratus, and internal temperature. The primary variables, load and displacement, were given the greatest development priority but since temperature and pressure could be readily obtained and it was not initially known in the development, whether these variables would have any affect on the primary transducers, it was decided to monitor these two environmental parameters as well.

3.1.1 Load

Two alternatives were considered for sensing load; a strain gage assembly or a piezo-electric load cell. The strain gage approach was selected because of the hardware simplicity, better signal integrity and the abililty to measure static loads (the crystal-based load cells considered had low-frequency limitations of around 0.1 Hz. The expertise in surface preparation and mounting of strain gages available at the Fear's Lab of the University of Oklahoma Civil Engineering department also prompted this decision.

The strain gages were mounted around the inner lip of the 12 inch section of tubing, as shown in Figure 3.2, that was chosen to contain all of the transducers. The first mounting attempt produced the strain sensing element used in the downhole test. Four strain gages were mounted to insure adequate testing.

The benefit of having multiple gages was that a high

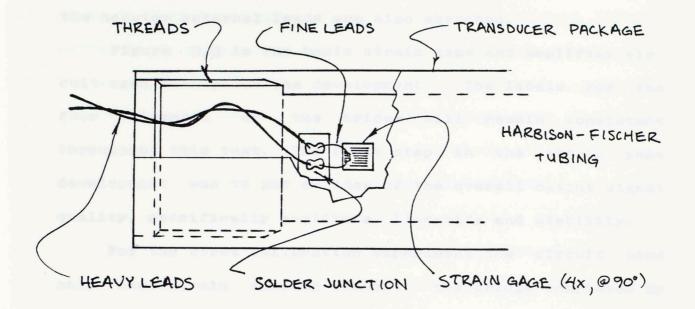


Figure 3.2 Strain gage mounting location.

degree of output linearity was eventually gained through the development of a Wheatstone bridge application that utilized two active strain gages, which will be discussed shortly. Two strain gages were also mounted on a dummy sample of steel that fit the inner curvature of the tube to serve as inactive legs used in the Wheatstone bridge for thermal compensation.

The Wheatstone bridge is the traditional circuit used for strain gage signal amplification. A brief discussion of this and the mentioned concept of thermal compensation is provided in Appendix A.

The gages were mounted reasonably close to the end of the tubing for ease of surface preparation and gage placement and also for access with a soldering iron to solder the fine gage leads to a surface pad (see Figure 3.2) to which the heavier external leads are also attached.

Figure 3.3 is the basic strain gage and amplifier circuit used throughout the development. The labels for the four elements of the bridge will remain consistent throughout this text. The first step in the strain gage development was to get an idea of the overall output signal quality, specifically amplitude, linearity and stability.

For the first calibration experiment the circuit used only one strain sensing element, the bridge completed by three circuit resistors (see Figure 3.3). At this point in the development it was safe enough to assume negligable temperature variation in the lab so no attempt was made to compensate the circuit thermally.

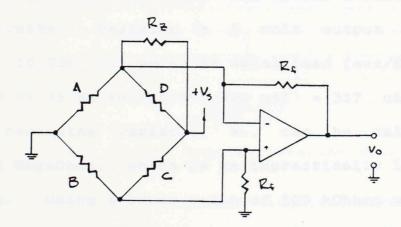


Figure 3.3 Basic Strain Gage Circuit Configuration

The equation for the output of this this circuit is:

Eq. 1
$$V_{cx} = (V_{mx}/2)*a*e*(R_{7}/R_{mx})$$

where V_{ϖ} =output voltage, V_{ϖ} =supply voltage, a=gage factor, e=strain, R_{π} =feedback resistance, and R_{ϖ} =strain gage resistance.

The gage factor accounts for the fact that the change in R_{\pm} , though linear, is not directly proportional to the change in e. This factor is generally between 1 and 2 and was assumed to be 1.5 for the initial analysis that follows.

The A/D converter was already designed at this point and the input range was specified as 0 to 5 volts. Therefore it was the goal to condition all transducer signals to be within that range and preferable span a large percentage of the 5 volt swing for maximum resolution of the digital data.

 R_{∞} was given as 350 Ohms, and V_{∞} was a factory recommended 5.0 volts. Desiring a 5 volt output swing for roughly a 10,000 lb swing in axial load (e=s/E =(L/A)/e=(10,000 lb /1.05 sq in)/30,000,000 psi = 317 uinch/inch), the only remaining variable, R_{f} , can be calculated as roughly 1.5 MegaOhms, which is an impractically large circuit value. Using a lower value of 500 kOhhms was still a concern, producing a differential amplifier gain of over 1000, large enough to yield unwanted stray effects in the output.

The first calibration data is shown in Figure 3.4. Readily apparant from this data are two forms of error, non-linearity and, of greater concern, a 200 mV shift in the

operating point occurring in just the short time between taking the two columns of data. Further observation during this test revealed subsequent shifts of greater than 500 mV and a sensitivity to air movement in the vicinity of the circuit.

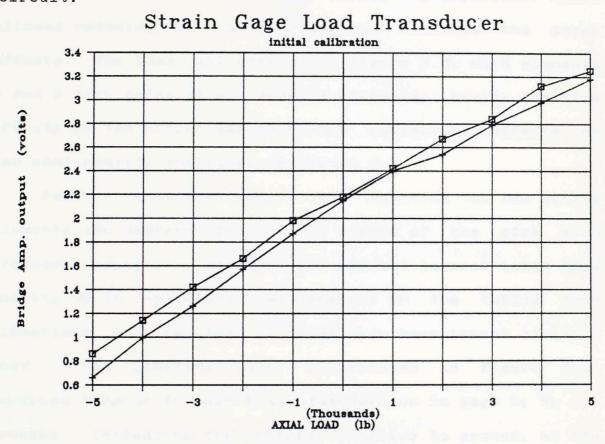


Figure 3.4 Single Gage Calibration Results

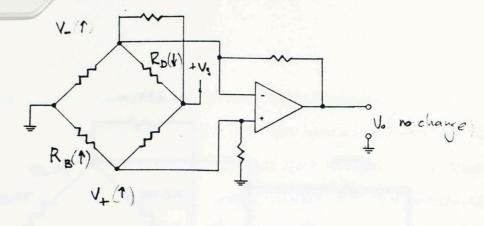
The two most important design decisions made, regarding the strain gage load transducer, resulted from the outcome of this first experiment.

First, the lead lengths in the elements of the bridge had to be made as short as possible because a 0.01 Ohm change in any part of the bridge produces a 150 mV change in the output. So, for the next step in development, all four

legs of the bridge would be mounted close together (ie, up inside the tube, near the strain gages).

Second, needing to reduce the gain of the amplifier and yet wanting a larger output swing, a method was devised to double the output of the bridge, before the amplifier, which allowed reducing the amplifier gain to minimize the stray effects. The idea, illustrated by Figure 3.3, with elements B and D both being strain-sensing elements, having additive effects on the output amplitude and cancelling effects on the nonlinearity exhibited in Figure 3.4.

Further analysis shows that mounting the two active elements 180 degrees apart on the inside of the pipe also produces cancelling effects that prevent lateral loads from showing up in the output (ie. moments on the tubing from vibrations and bending) allowing pure measurement of axial The limiting case, illustrated in Figure 3.5, produces tension in gage B and compression in gage D; Re increases, increasing the voltage, relative to ground, at the plus op-amp input, and Rp decreases which, by decreasing the voltage across RD that is referenced to +V, also increases the minus op-amp input, producing no net change at the output. In the other limiting case where the tubing is rotated 90 degrees, both gages are near the neutral fiber and they experience no change. For intermediate cases, gages B and D are always equidistant from the neutral fiber and consequently experience equal and opposite strain, producing no



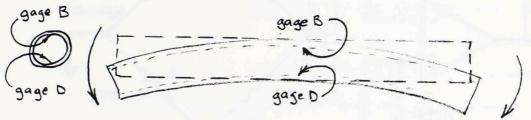


Figure 3.5 Gage Mounting for Lateral Load Insensistivity net effect on the output.

The circuit incorporating these changes and the resulting calibration data are shown in Figures 3.6 and 3.7. V_{ϖ} was increased to 6.2 volts for this experiment in an effort to increase output swing but returned to 5.0 volts in the final implementation.

The standard approach for thermal compensation was used, applying the same type of strain gages in the inactive legs as in the strain-sensing legs only mounted to a dummy piece of steel that does not come under stress. This matches resistive values in the bridge, but more importantly the thermal coefficients of the resistive material in the gages. Since the bridge circuit amplifies proportional changes of the elements, a uniform temperature change in all elements will generate no change in the output. The dummy is made of steel to match the thermal coefficient of expansion

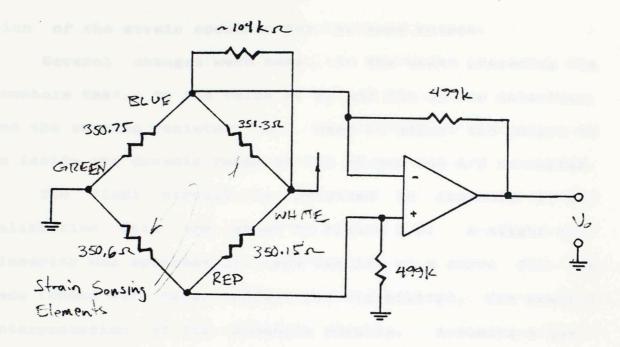


Figure 3.6 Dual Strain Sensing Element Configuration

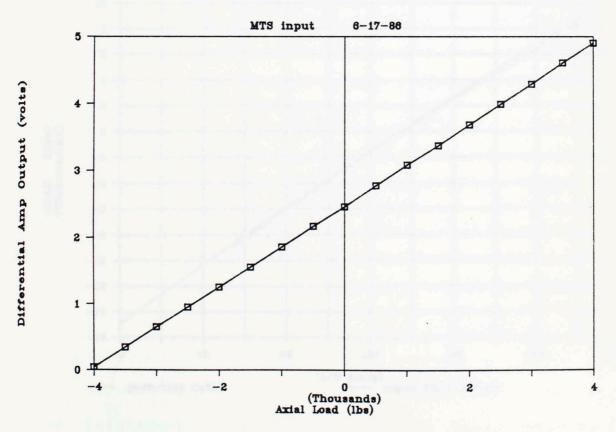


Figure 3.7 Dual Strain Sensing Element Data

sion of the strain specimen for the same reason.

Several changes were made, in the weeks preceding the downhole test, to the value of R_{f} and the op-amp selection, and the zeroing resistor, R_{g} , used to adjust the output to be inside the dynamic range of the op-amp and A/D converter.

The final circuit is provided in Appendix F and calibration data are shown in Figure 3.8. A slight non-linearity was apparant in these results so a curve fit was made (shown with data, offset for visibility), for precise interpretation of the downhole results. Assuming a quad-

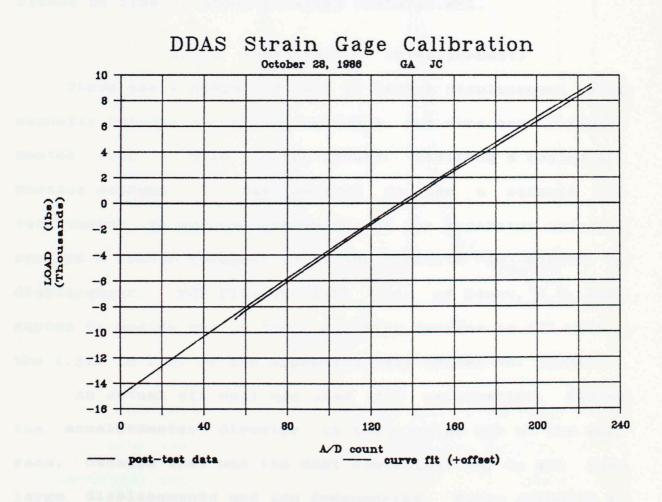


Figure 3.8 Calibration Data, Final Circuit Configuration

ratic relationship, the curve was fit, using tools available in Lotus 123, ver. 2, by creating a column reflecting the local slope of the data (on a point-to-point basis), performing a linear regression of this vs load, and then mathematically integrating the straight line result to produce the shown curve fit. Load is plotted vs A/D count because that is the form in which the data is stored. The 8-bit A/D used produces 256 levels of input between 0 and 5 volts, each level representing 19.0 mV of transducer signal. The data and analysis is saved in a Lotus 123 worksheet and stored on Disk 1, under filename FCALA282.WK1.

3.1.2 Acceleration (Displacement)

There are a number of ways to derive displacement using magnetic sensors or optical encoders, but none easily implemented over 1 mile in the ground. Desiring a sealed apparatus package, it was decided to use a seismic accelerometer to measure the motion of the apparatus and then perform a double integration on the results to arrive at displacement. PCB Piezotronics, Inc. of Depew, N.Y. consented to modify one of their existing designs to fit within the 1.312 in I.D. of the apparatus case (Model No. 393M11).

An actual oil well was used for calibration, fixing the accelerometer directly to the carrier bar at the surface, because that was the most convenient way to get such large displacements and low frequencies. Early attempts at

treme sensitivity to shock. The signal saturation and following decay shown in each cycle of Figure 3.9 resulted from a mechanical impulse to the sucker rod string about 5 inches into each upstroke. Figure 3.9 also includes the position signal, recovered from a Delta-X displacement potentiometer, for comparison to the position signal derived numerically from the accelerometer data.

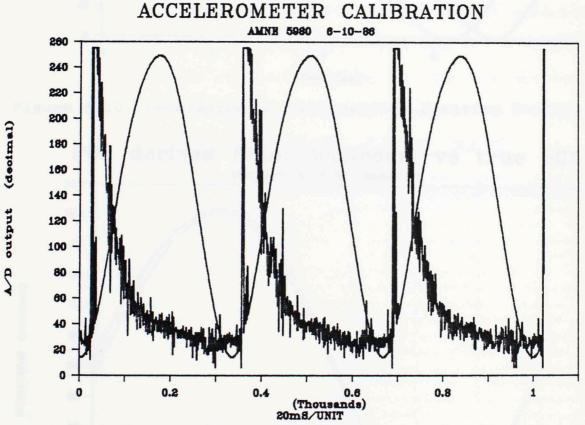


Figure 3.9 Accelerometer Calibration, First Attempt

PCB consented to fix the problem and eventually did. Testing continued with the accelerometer mounted in a spring-damper support. Figures 3.10 and 3.11 depict the results, both graphs containing the same true-position

POS derived from Acc. vs true POS test date: 6-17-86 Sooner #1 110 100 80 70 80 40 30 20 10

Figure 3.10 Accelerometer Calibration, Position Unadjusted

TIME (sec)

8

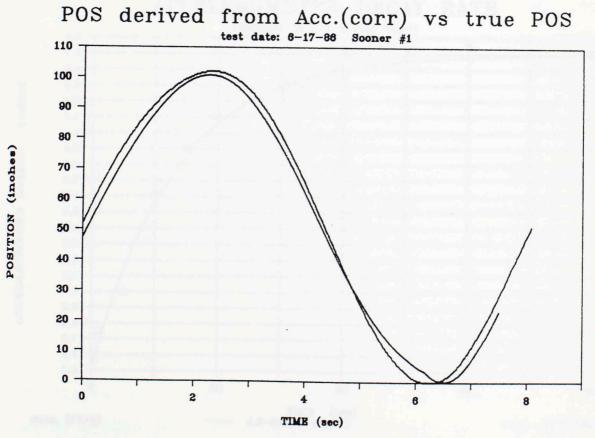


Figure 3.11 Accelerometer Calibration, Position Adjusted

the double numerical integration and the 1 V/g constant specified by the manufacturer. Figure 3.11 shows the same data, shifted in time and scaled to obtain a match with true position. At this point in the development these results provided adequate confidence in the accelerometer without having determined precise scale factors.

To establish the exact response of the accelerometer for compensation of the final data, I measured it's response to a 2 g step input (by letting it stabilize in a vertical orientation and then rapidly flipping it over and monitoring the output). The response is easily modeled by a single

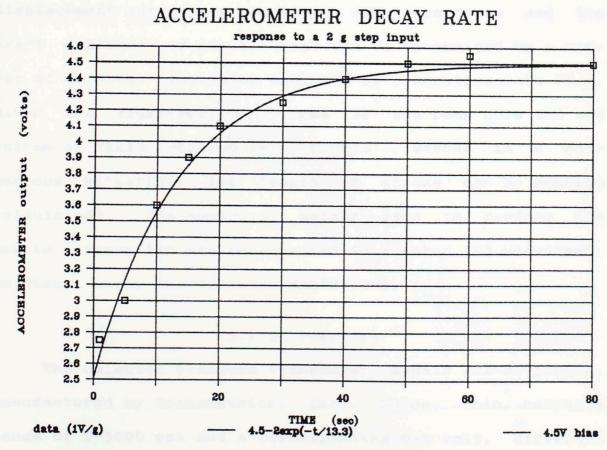


Figure 3.12 Accelerometer Response, Lab-measured

pole filter with a time constant of 13.3 seconds, which would produce roughly 5 degrees of phase lead in the output, at the pumping frequency of 0.125 Hz, and negligable attenuation. This analysis is shown in Figure 3.12. The exact electrical circuit to supply power to and recover signal from the transducer is shown in Appendix F.

A large variation in derived peak-to-peak displacement, from cycle to cycle, was observed in the analysis of the downhole data, which is not completely understood, but fully exhibited in Figures 4.18 through 4.24. This problem detracts from the validity of the displacement data but, in this case, is not completely detrimental. The shape of the displacement curves are consistent and repeatable and the exact amplitude of displacement can be determined by a number of methods, including analysis of production rate (i.e. given the cross-sectional area of the pump bore and the volume of fluid produced in a single stroke in a nongaseous situation, the length of stroke can be readily calculated). The numerical method used to perform the double integration was implemented in a Lotus 123 worksheet, on disk 1 under the filename MASTER. WK1.

3.1.3 Pressure

The selected pressure transducer, model# P21-BA-5000-A, manufactured by Transmetrics, Inc., Solon, Ohio, having a range of 0-5000 psi and a corresponding 0-5 volt, differen-

tial output.

The calibration of this very rugged, high-precision sensor was initially hampered by trying to implement it as a single ended device, grounding the minus output line and attempting to measure a pressure signal on the plus output. A 4 volt DC signal was measured regardless of the applied pressure. This problem was solved, after consulting with the Application Engineer at Transmetrics, by adding a differential amplification stage before the A/D converter. Calibration data is presented in Figure 3.13. The high level of noise is undesirable and, I believe, introduced by an oscillation in the mentioned differential amplifier which was potted in Epoxe at the base of the transducer connector. I could not

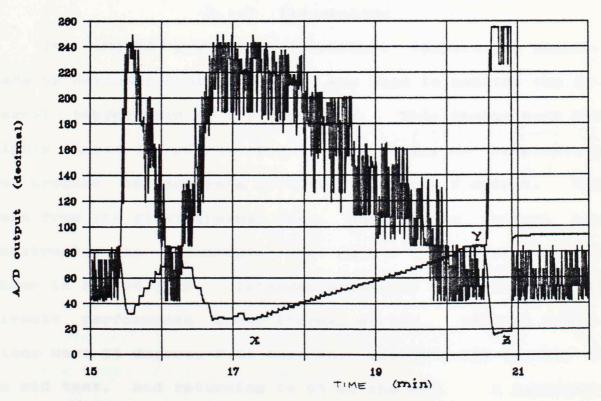


Figure 3.13 Pressure Transducer Calibration

Justify the rework required to improve this signal quality, (though, in hindsight, it could have been accomplished with a single-pole filter at the A/D input) since it was of relatively low importance and was adequate for the general needs of the downhole field test.

Also shown in the lower trace of Figure 3.13 is the strain gage sensitivity to external pressure. The information in this graph is interpretted by knowing at point X, pressure was 4000 psi, each step to the right is 100 psi, and the pressure at point Y being atmospheric. At point Z, pressure is 5000 psi. A shift in the load transducer output can be observed, beyond point Z, where the pressure was reduced rapidly from 5000 psi to atmospheric.

3.1.4 Temperature

The LM34CZ precision Fahrenheit temperature sensor, made by National Semiconductor, was used to monitor the internal temperature of the apparatus. This device uses the highly linear dependence of a transistor Vos on temperature to produce an accurate 10.0 mV per degree F output. The data from the first thermal test, done in the thermal box constructed to accommodate the near 6 foot apparatus, is shown in Figure 3.14. Intended primarily to verify digital circuit performance under thermal stress. Ambient conditions were 95 degrees F at turn-on, reaching 165 degrees F in mid test, and returning to 95 at the end. A compensa-

tion term of 25 degrees must be subtracted to account for the heat added by power dissipation in the electrical cir-

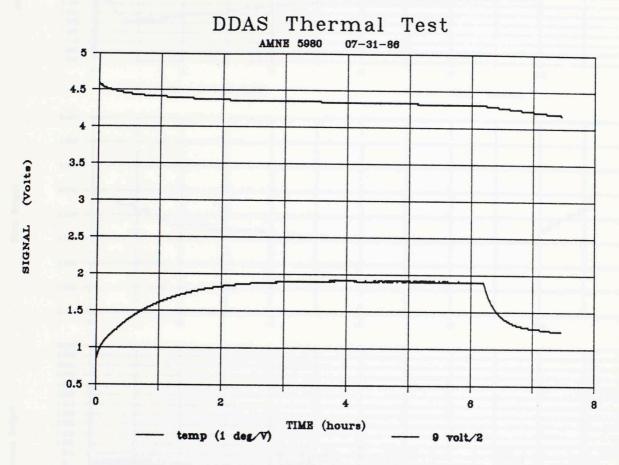


Figure 3.14 Temperature Sensor Output

cuits. This number comes from the difference between the measured starting temperature (no circuit dissipation yet) and the final asymptote.

Also shown is the battery pack monitor signal which represents the 9 volt unregulated supply divided by two.

Figure 3.15 shows the effect of temperature on each transducer, sampled during one of four overnight thermal dependence tests that were conducted.

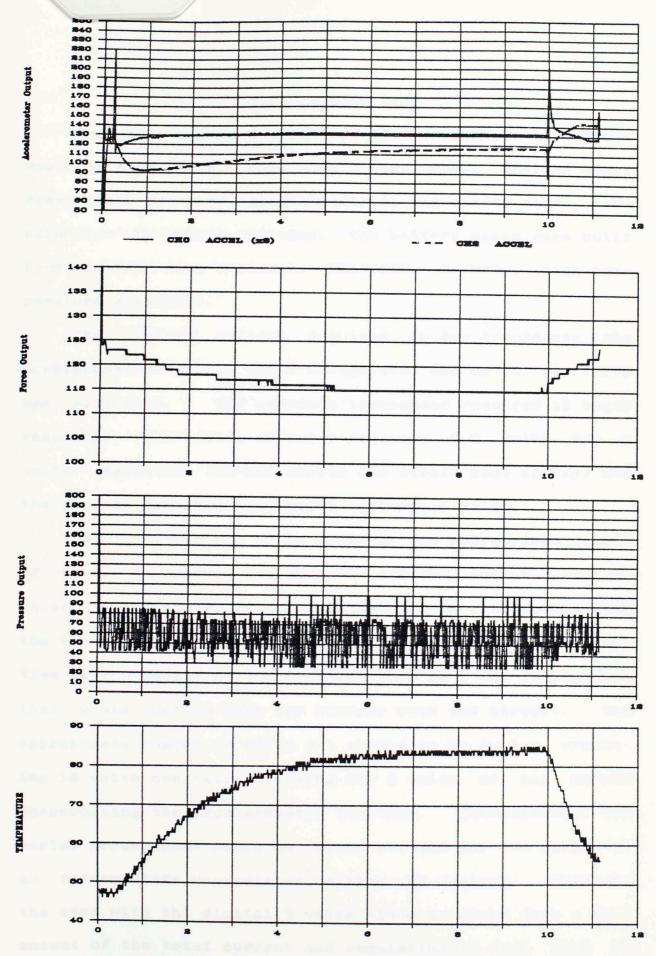


Figure 3.15 Transducer Thermal Dependence

3.2 BATTERY PACK

Certainly key to the success of the downhole experiment would be a reliable, unfailing battery pack. Wanting great flexibility of size, adaptability to the system needs, and selection of output voltages, the battery packs were built from scratch using Duracell, MN1400HT, Zn/MnO₂, high temperature alkalines.

The highest voltage required by any transducer (the accelerometer) was 15 volts unregulated and up to 24 volts was allowable. The pressure transducer required 12 volts regulated, the analog circuits required 8.2 volts and 5 volts regulated (op-amp supply and strain gage supply) and the digital dircuits required a separate 5 volts.

At 1.5 volts per cell, nominal, the appropriate number of cells, to produce the desired maximum output, can be chosen. The number of cells was chosen in conjunction with the known length of the printed circuit board and the selection of the length of tubing (available in 6 in. increments) that would contain both the battery pack and circuit. The appropriate number of cells was chosen to be twelve, producing 18 volts nominal, allowing for 3 volts of sag before jeapordizing the accelerometer function. Conveniently, the series arrangement could be tapped between any two cells if an intermediate unregulated voltage was desired. This was the case with the digital 5 volts since it would draw a fair amount of the total current and regulating it down from 18

volts would produce excessive dissipation in the regulator (power wasted=(V_{unreg} .- V_{reg} .)*I). Hence, the center of the series, or 9 volts unregulated, was also brought out for the input to the digital 5 volt regulator. This configuration is shown schematically in Appendix F.

The results of a battery life test are shown in Figure 3.16 where the upper trace indicates the presense of a 39 Ohm load across the 18 volts and the lower trace is the measured center-tap voltage, $V_{\rm et}$. The rapid decay prompted the pursuit of all CMOS circuitry. The eventual circuit current requirements were much less than this and one battery pack lasted for over 35 hours of preliminary testing in applications similar to the downhole test.

Desiring absolute integrity of the power supply, the cells were soldered in series and covered by several layers of heat shrink tubing (see Appendix C). The pack is retained axially, at both ends, within the plastic inner sleeve by lateral dowel pins.

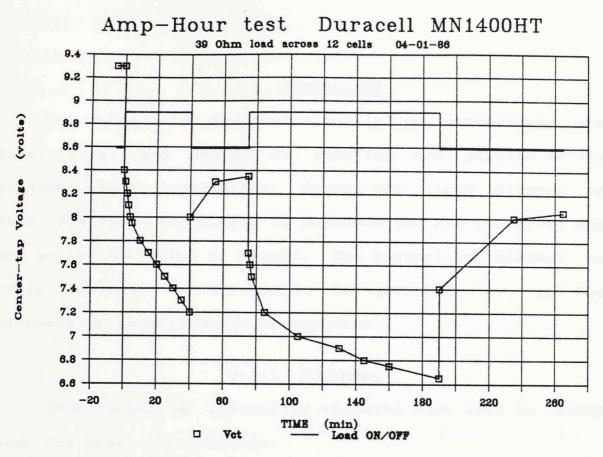


Figure 3.16 Battery life

3.3 CONTROLLER

The function of the controller is to orchestrate the time, rate, and amount of sampling and storage of the provided signal information. Though the block diagram of this function in Figure 18 includes the A/D converter and the entire 64k bytes of memory, the controlling element is truly contained in the single chip microcomputer, and the firmware or program which it executes.

3.3.1 Hardware

CMOS technology integrated circuits were used in every case for power conservation.

Microprocessor Selection of the Intel 8051 family was based on a good match with the system needs, the author's prior experience, and access to the necessary firmware development tools. The specific chip chosen was the 80C31 which has no internal ROM since the architecture was for instruction execution from external program memory. The entire system schematics are provided in Appendix F. The microcomputer/memory interface is standard and similar examples can be found in the Intel Micontroller Handbook.

Memory The logic behind the memory device selection

(28C64) is partially presented in the design specification in Chapter II. Another benefit of using EEPROMs is that, applied in the program memory space, program code can be changed, through the same interface that data is recovered, without an EPROM programmer or having to remove the program memory chip. This technique is known as in-system programming, and is not possible with any other form of silicon memory.

A/D The ADCO808 is a an 8-channel, 8-bit, microprocessor-compatible Analog-to-Digital converter, every stated feature of which is appropriate for this application. 8-channel meaning that 8 different signals can be selected independently, 8-bit A/D meaning it converts an analog signal into one of 256 (2^{cs}) possible discrete levels within a specified range. Convenient features such as address latching, strobe inputs to start conversions and enable internally latched digital outputs onto an 8-bit data bus make it microprocessor compatible.

Printed Circuit Board (PCB) With reasonable confidence in the digital design. I started the printed circuit board layout providing a breadboard area for the analog interface circuits which were not yet complete. The width of the board(s) (1.10 inches) was determined by the inner diameter of the plastic sleeve designed to contain and protect the

circuits and battery pack from the steel tubing wall. Laying out all the electrical components within the narrow width produced a length in excess of 23 inches, which is not a practical length for this narrow a board. This prompted the decision for a two-board design. After shuffling shapes around on paper, a natural partition emerged with the seven data storage chips on one board and the rest of the circuit on the other.

The artwork was generated with the aid of a PC-based, program for double-layer printed circuit board drafting, which, when compared to hand layout with tape or ink, is like comparing the word processor that this thesis was written on to a 1930's vintage typwriter. The 8 feet long, cut-and-pasted originals (see Appendix F), which Triangle A&E, Oklahoma City, reduced to the full-scale positives still took over 60 hours to make.

Three sets of boards were fabricated by Frontier Engineering, Oklahoma City. The first used in preliminary accelerometer calibration and general design debug, the second, built and refined to a level of quality sufficient for the final application, and the third used for experimentation with soldering and connector application. Problems with board quality in the later stages of development prompted the ordering of back-up boards from a second vendor, Protoquick, Dallas which were of similar cost but much higher quality (mil-spec fiberglass substrates, and reflow

soldered runs) but were not needed.

The final printed circuit board assembly is shown in Appendix F.

3.3.2 Firmware

Background The terms firmware and software both describe a form of computer program. Firmware differs from software in that it generally refers to microcode or the assembly language level of program that resides permanantly with the hardware in some sort of ROM (Read Only Memory). In this case the firmware resides in the program memory EEPROM.

The entire program uses just over 300 bytes of code for 134 instructions, and a table that explicitly defines the sampling session; number of sampling periods, channels to sample and rate of sampling during each period, and memory allocation for all sampled data.

The program resides in shared external memory and program memory space, address 0 to 1FF Hex or 0 to 511 decimal, which is in the program memory chip on the microprocessor board. The entire 64k bytes are commonly addressable as program memory or external memory, due to the hardware configuration (all chips have a common WR strobe and a common RD strobe which is the boolean sum of PSEN and the external memory RD. Unused program memory in the lowest 8k is not useful for data storage since the write cycle of the 28C64 disables the chip for 1 mS, which irrevocably dis-

rupts program execution.

Theory of Operation The flowchart for the downhole data acquisition program is shown in Figure 3.17. Examination of this and the firmware listing in Appendix H, will reveal that the program operates from a table containing key values specifying sampling and data storage locations.

Each line of the table on the second page of the firmware listing completely specifies a single data sampling period of which there were fifteen for the downhole test. Six sampling periods, labeled A through F are of the same mode and duration (CHO through CH3, 40 Hz, for 1 min). The last 21.6 seconds of information of each of these sampling periods is overwritten with data from the next sampling period. At the given sampling rate and number of channels, 6k bytes are stored in 38.4 seconds. Storing data for the remainder of each minute does no harm and serves to keep the overall sequence on one minute intervals without adding special routines to accomplish this.

The seventh sampling period, labeled G, samples channels 0 and 1 at 20 Hz for six minutes, sacrificing the upper 1984 bytes of memory. This was done because sampling for seven minutes would overflow legal address space and attempt to write to address 0000 (program memory) which would permanantly disrupt program execution. The purpose of this period was to observe settling of pumping conditions during

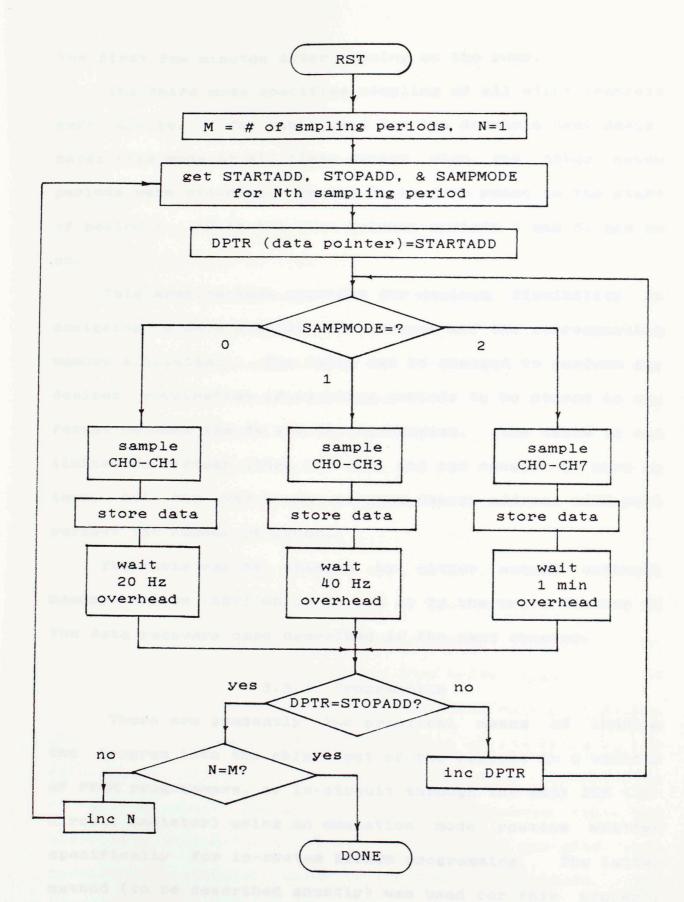


Figure 3.17 Controller Flowchart

the first few minutes after turning on the pump.

The third mode specifies sampling of all eight channels each minute. The table used for the downhole test designates this mode at all times except when the other seven periods were occuring. Period OA is from reset to the start of period A, AB is the time between periods A and B, and so on.

This architecture provides for maximum flexibility in designing a data acquisition sequence and the corresponding memory allocation. The table can be changed to perform any desired combination of sampling periods to be stored in any format between the 8k and 64k boundaries. The table is not limited to fifteen lines (0F Hex) and can consist of more or less, but the value in program memory address 033H must reflect the number of lines.

The table can be changed by either manual external memory writes (XBY) while in ICE or by the write feature of the data recovery card described in the next chapter.

3.3.3 Programming

There are presently two practical means of loading the program into the chip; out of the circuit in a variety of PROM programmers, or in-circuit through the 8051 ICE (In-Circuit Emulator) using an emulation mode routine written specifically for in-system EEPROM programming. The latter method (to be described shortly) was used for this project,

being more convenient and taking advantage of the in-system programmability feature unique to this device.

An ICE is simply a keyboard driven firmware development tool with a control cable that has a pinout identical to, and fully emulates the function of the microprocessor. The program in the ICE can be programmed to start and stop at any point and can be readily altered to aid in the firmware debug process. Once a program is debugged and fully functional it is generally stored on floppy disk for input to a separate PROM programming machine. Wishing to avoid this extra step and to take advantage of the in-system programmability of the 28C64, I wrote a short routine (found at the end of the firmware listing) that, under ICE control, copies the debugged program from ICE memory into the program memory space of the data acquisition board. There it can be executed by ICE (told to execute from external memory) or by a microprocessor in the normal mode of operation.

The BASIC program that runs the data recovery board (Appendix E) could be modified to also write large blocks of data (ie. a program from disk). Though used mainly, in this project, to recovery the large segments of stored data, the data recover board does have single byte write capabilities to enable minor changes to the sample pointer table and especially to the two bytes in addresses 080H and 081H that specify the initial delay in the sampling sequence. The data recovery system is detailed in Appendix D.

CHAPTER IV

RESULTS

4.1 Field Test

The downhole test was conducted on August 28, 1986. The producing oil well used was Chevron F.S.D.U. T55A - 12, located in Carter county near Ardmore, Oklahoma. The weather was excellent with temperatures in the low to mid 80's and clear skies the entire day. Present from the University of Oklahoma were students Carl Adams, Jesus Chacin, and myself and our advisor, Dr. John Purcupile of the AMNE department.

The workover crew had the entire sucker rod string out of the ground when we arrived at 10:00 a.m. The circuits were activated at precisely 10:15 a.m. in an office area and, after completing the hand assembly (see Appendix C), we delivered it to the well site. The crew tightened the apparatus with pipe wrenches (and 4 feet long extensions), which were then also used to attach the top of the apparatus to the bottom of the first sucker rod which, at that point, was laying out on the ground. Then, hoisted into position above the well opening, the bottom of the apparatus was wrenched onto the top of the pump section which was already in the hole, and then everything was lowered into the hole.

Fluid was added to bring the level to the surface, the surface pumping unit was completed and the (add the pump description here) was turned on at approximately 12:10 p.m.

Seven high-frequency sampling periods were specified in the controller program of one minute duration each (except the last period which was 6 minutes) commencing precisely 210 minutes after resetting the microprocessor at the surface, and ocurring at ten minute intervals (start-to-start). These sampling periods are labeled A through G. Samples of all parameters were made each minute throughout the test. Pumping ceased at approximately 3:25 p.m., the apparatus was brought back to the surface, removed from the string, cleaned with diesel fuel and opened for data recovery and to hopefully verify a successful test.

The first sign of good health was that the LED was still blinking on the minute (within 1 second which is very good considering the timing loops were developed empirically and not by absolute calculation) which indicated the controller had done, and was continuing to do its job and that if the transducers were still alive, the data was probably stored successully. Next the critical voltages were measured with the DMM and all channels into the A/D were observed to be responding as designed. However, the bias point on the load output had shifted from 2.0 volts to 1.2 volts, raising the question in my mind that part of the AC component may have been clipped at the bottom (0.0 volts),

especially if greater downward shifts had occurred at elevated temperatures downhole. Another cause for concern in the early observation was bared conductors in the accelerometer power and signal wires which were adjacent each other in a three-leaded ribbon cable. The insulation was apparantly pinched or rubbed away by contact with the plastic sleeve, but the wires were not touching nor was there any sign of arcing that might have occurred had the power supply line contacted the steel case which was at ground potential.

My personal moment of triumph was minutes later when the first data was recovered, for sampling period A, through the data recovery board which displays the columns of data on the monitor as it stores it onto a disk file. All memory locations had been written with zeroes prior to the test, and I could see legitimate data values being displayed in the respective columns. Real relief for the others present did not come until minutes after this when this data file was imported into a Lotus 123 worksheet and displayed graphically, both Jesus Chacin and Bill Foley recognizing certain features in the load trace that they had seen before in their models.

4.2 Recovered Data

Later, raw data from all sampling periods was recovered from the controller memory and stored in files, via the data recovery board, with .PRN extensions on floppy disk, copies of which accompany this thesis. PIC files were generated in Lotus 123 for all downhole data and those graphs are provided in this chapter. The conversion for A/D output is always 19.0 mV per count here. The load data and accelerometer data were further reduced and graphed in actual units to compose the axes of downhole dynagraph cards.

Due to their size, quantity and sequence, all graphs are grouped together at the end of this chapter, with explanations grouped in the preceding text.

Figures 4.1 through 4.6 show the raw data from the six, 4-channel, 40 Hz sampling periods labeled A through F. Channels 1, 2 and 3 (load, acceleration and pressure) are dislayed together in each case, conveniently and naturally spacing themselves in non-overlapping ranges. Channel 0 has been omitted since it is a multiple of channel 2 and only clutters the graph. The zebra effect on load in part of Figure 4.5 and all of Figure 4.6 is due to a flaw in the controller memory permanantly containing zeroes in every 32nd address. This probably happened while exceeding the recommended operating temperature in preliminary testing.

The conversion factors for these traces are:

CHO: AMPLIFIED ACCELERATION = .0065 (CT) [g's]

CH1: LOAD = .05xxx (CT)² + 118.5 (CT) + 2600 [1b]

CH2: ACCELERATION = 0.0195 (CT) [g's]

CH3: PRESSURE = 19.0 (CT) - 850 [psi]

CH4: TEMPERATURE = 1.90 (CT) [degrees F]

CH5: $5 V_{reg} (/2) = .038 (CT) [volts]$

CH6: 9 V_{best} (/2) = .038 (CT) [volts]

CH7: 18 V_{bestt} (/4) = .076 (CT) [volts]

where CT is the A/D \underline{C} oun \underline{T} or value.

Figures 4.7 and 4.8 are the acceleration (x3), and load (channels 0 and 1) taken at 20 Hz for the six minute sampling period G. The purpose of this test was to observe the transient response of the load signal envelope to start-up. The crew's difficulty in restarting the pump can be observed in the 2.5 to 3.0 minutes before periodicity was achieved.

Figures 4.9 through 4.13 are plots of samples taken of all channels, each minute throughout the test. Zeroes were left in the memory cells when sample periods A through G occurred to reference them in time with the overall test.

In Figure 4.10, the bias level of the load can be seen to drift down with increasing temperature and depth, positive and negative spikes can be seen at the seating and unseating of the pump at 95 and 305 minutes. The negative spike demonstrates the dynamic range of the opamp at its

spec of .030 volts or an A/D count of 2. The mentioned shift in bias level from start to finish can also be observed.

The global story on pressure is clearly observed in Figure 4.12, as is the adding of fluid from the surface between the 80 and 95 minute marks.

The temperature inside the apparatus stabilized at 122 degrees F throughout the pumping and the battery pack exhibited very little depletion during the six hours as can be observed in Figure 4.13. Channel 5 was omitted here and is simply a straight line at 127 through the entire test, as would be expected from a voltage regulator.

Figure 4.14 is a comparisons of measured and mathematically predicted load. Derivation of the predicted load and further analysis of this data are presented in J. Chacin's doctoral dissertation (reference).

4.3 Downhole Dynagraphs

The remaining graphs encompass data reduction required to construct a downhole dynagraph. The shape and amplitude of the load curve is extremely consistent and repeatable and the second cycle of sample periods C, D, and E are shown in Figures 4.16 through 4.18. The cycles are taken from a

Diagnostic and Design Techniques, J.E. Chacin, 1986 fixed window relative to the beginning of each sample

period, so the curves are not necessarily in phase from graph to graph. This is irrelevant in making a dynagraph.

For reasons not fully understood the accelerometer-derived displacement did not produce consistent or expected amplitudes as can be seen in Figures 4.18, 4.20, and 4.22. To make the best possible use of this information which clearly has some useful content, the five cycles from each sample period were averaged and normalized to 99 inches (a value established with confidence by other methods, noted on page 22) to produce a composite displacement curve having much less random noise content than any of the original cycles (see Figures 4.19, 4.21, and 4.23). The load traces were shifted 5 degrees to compensate for the phase lead of the accelerometer discussed in chapter 3, and plotted versus the three composite displacement curves to produce the three downhole dynagraphs of Figures 4.24 through 4.26.

As an added step toward making an accurate dohnhole dynagraph card, an average was made of all load and displacement traces of the three dynagraphs (see Figures 4.27 through 4.30) to further reduce the noise content and then the data was replotted to form the final composite dynagraph of Figure 4.31.

The preceding analyses (including the double numerical integration) were done in Lotus 123 worksheet MASTER.WK1.

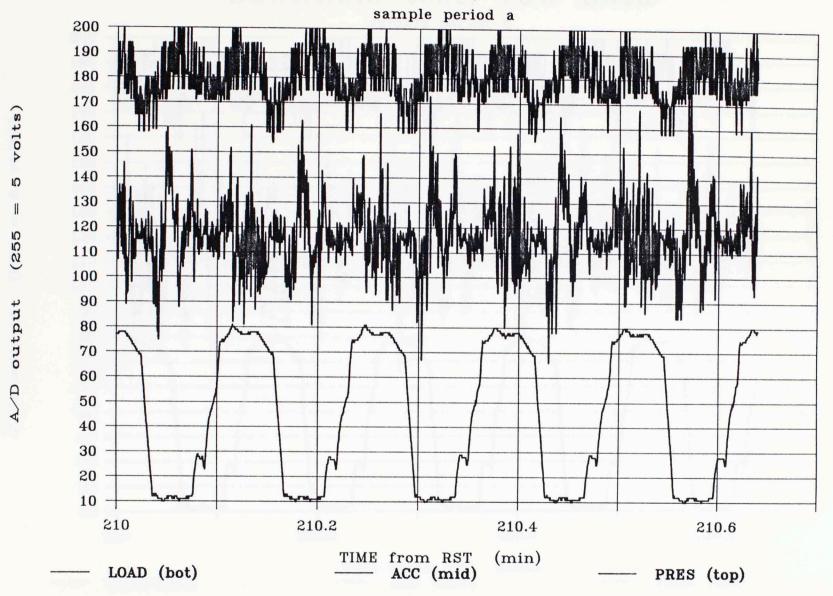


Figure 4.1 Downhole data, sample period A.

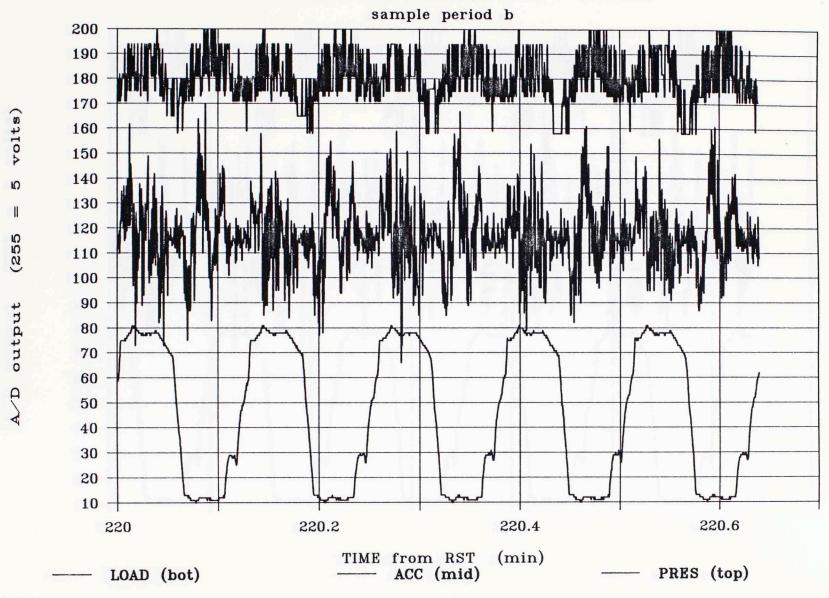


Figure 4.2 Downhole data, sample period B.

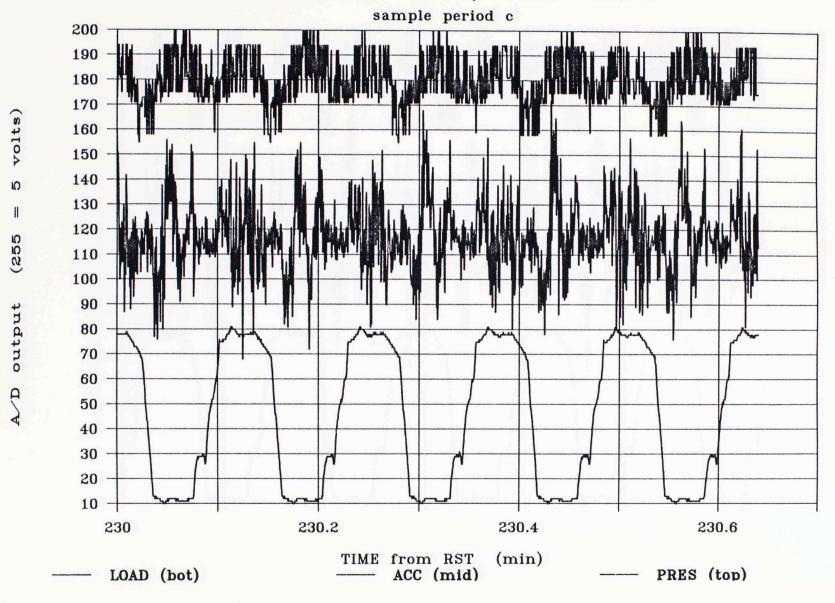


Figure 4.3 Downhole data, sample period C.

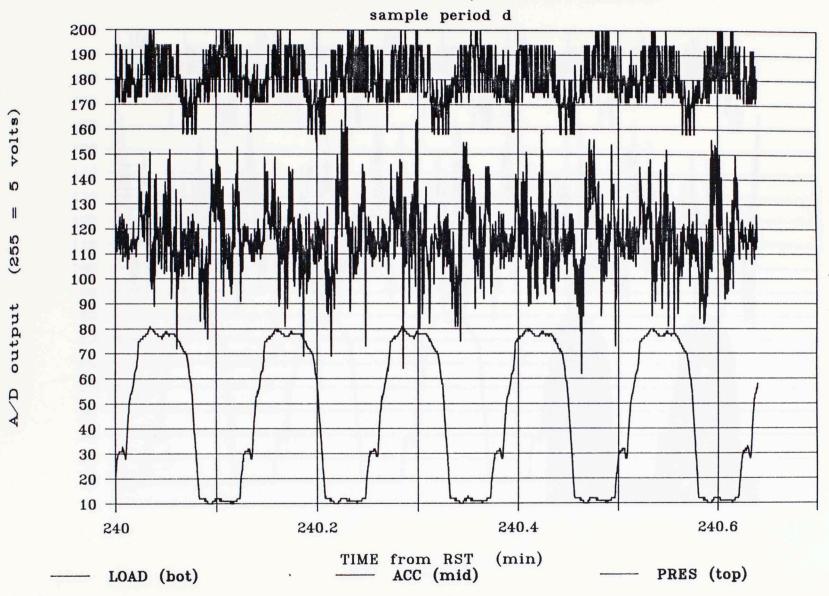


Figure 4.4 Downhole data, sample period D.

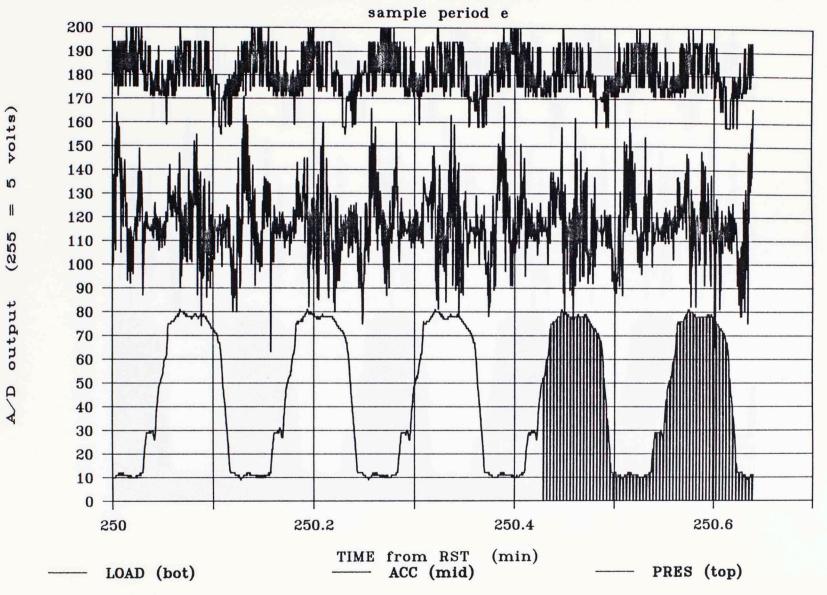


Figure 4.5 Downhole data, sample period E.

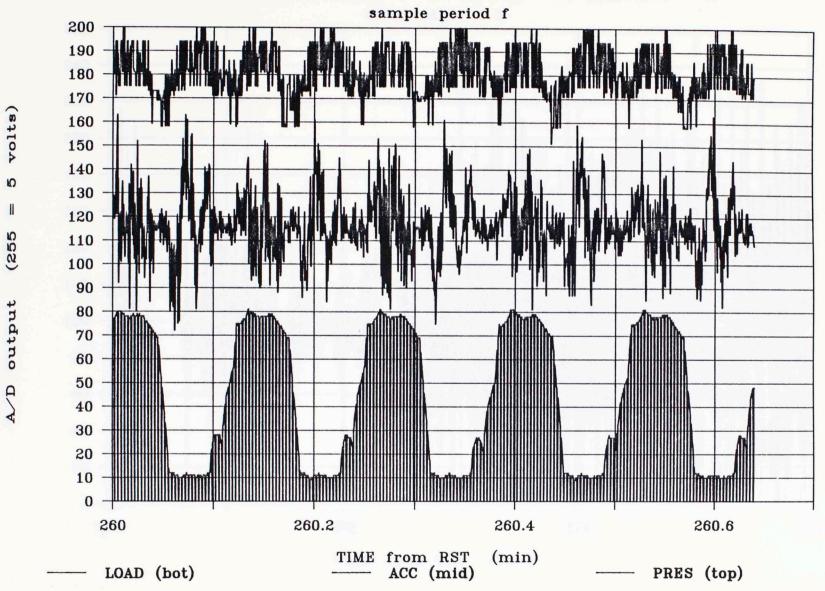


Figure 4.6 Downhole data, sample period F.

DOWNHOLE RAW DATA, PERIOD G acceleration x 3

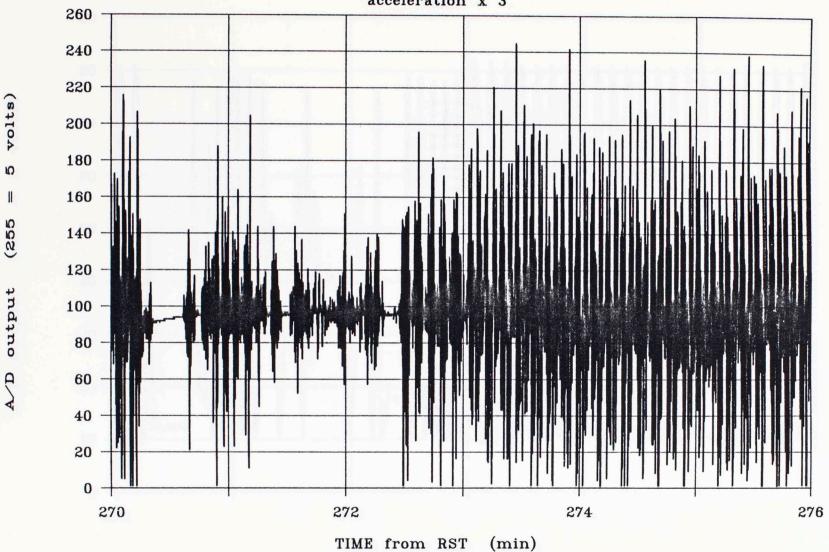


Figure 4.7 Downhole data, sample period G-CHO.

DOWNHOLE RAW DATA, PERIOD G LOAD 90 80 -70 -60 -(255)50 -40 -30 -20 -10 -0 -270 272 274 276 TIME from RST (min)

Figure 4.8 Downhole data, sample period G-CH1.

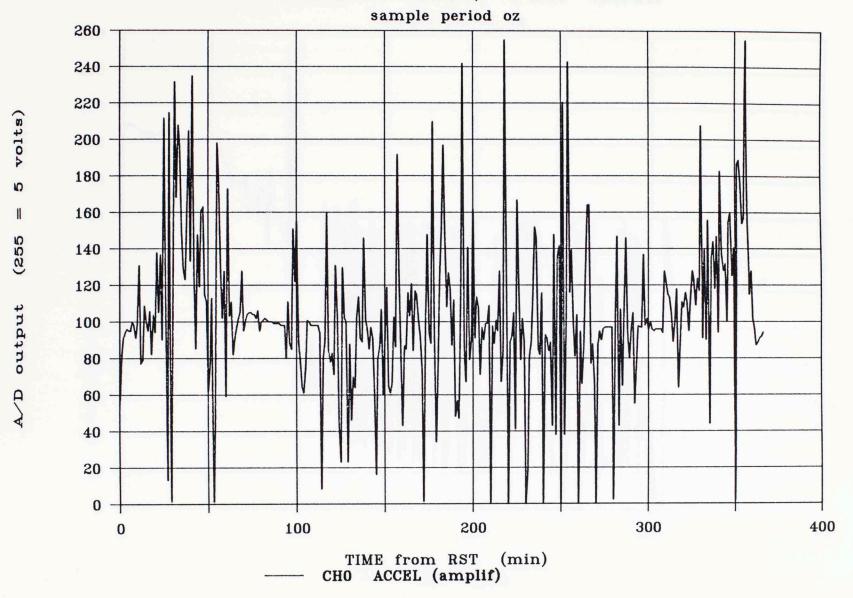


Figure 4.9 Throughout-test samples, CHO, Amplified Accel.

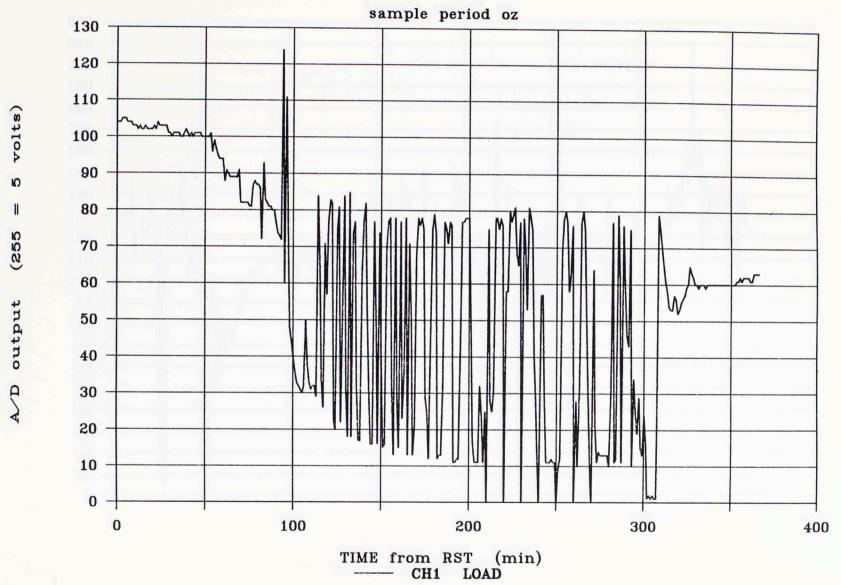


Figure 4.10 Throughout-test samples, CH1, Load

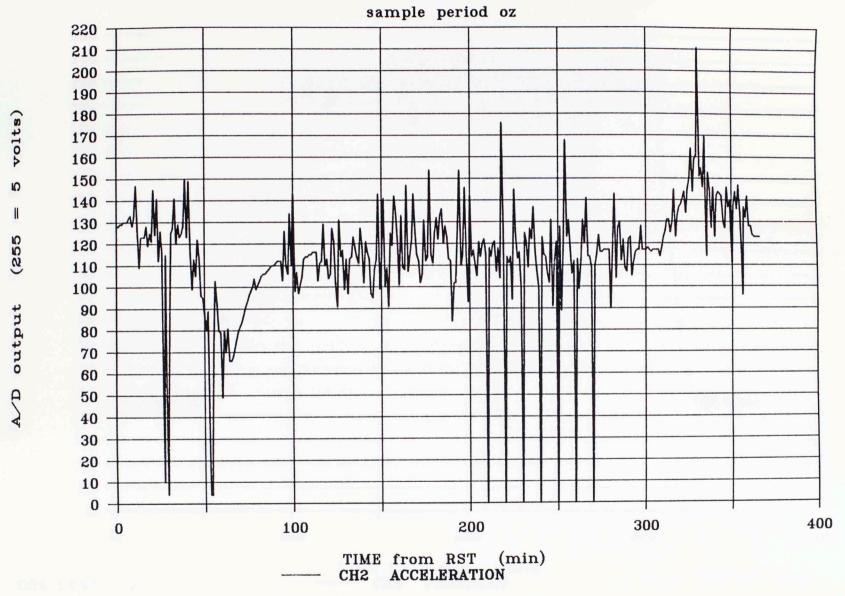


Figure 4.11 Throughout-test samples, CH2, Acceleration

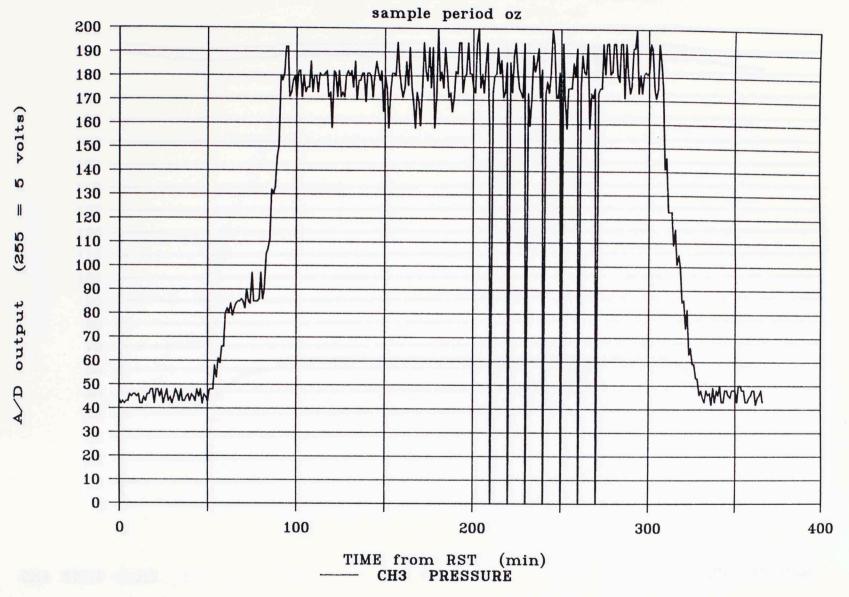


Figure 4.12 Throughout-test samples, CH3, Pressure

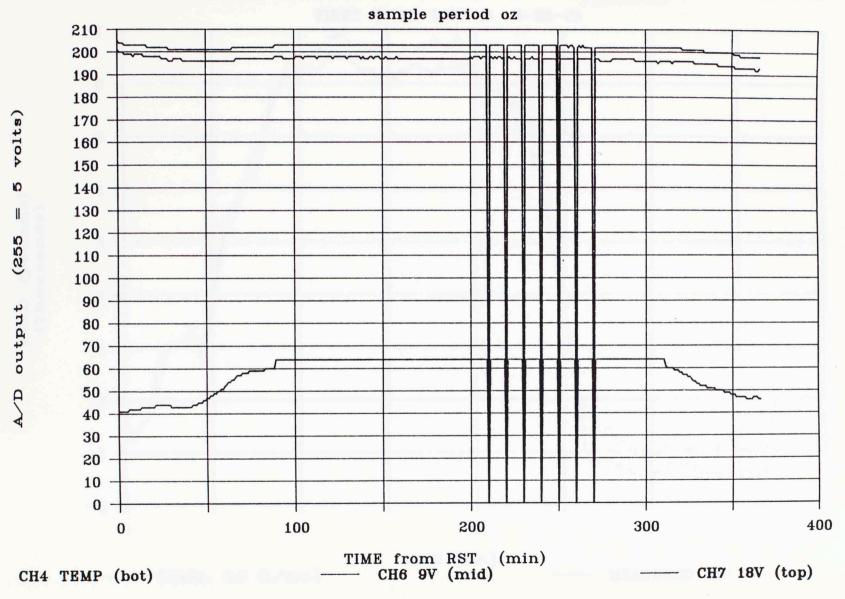


Figure 4.13 Throughout-test samples, CH4-7, Temp. and Volt.

COMPARISON MEASURED AND PREDICTED LOAD

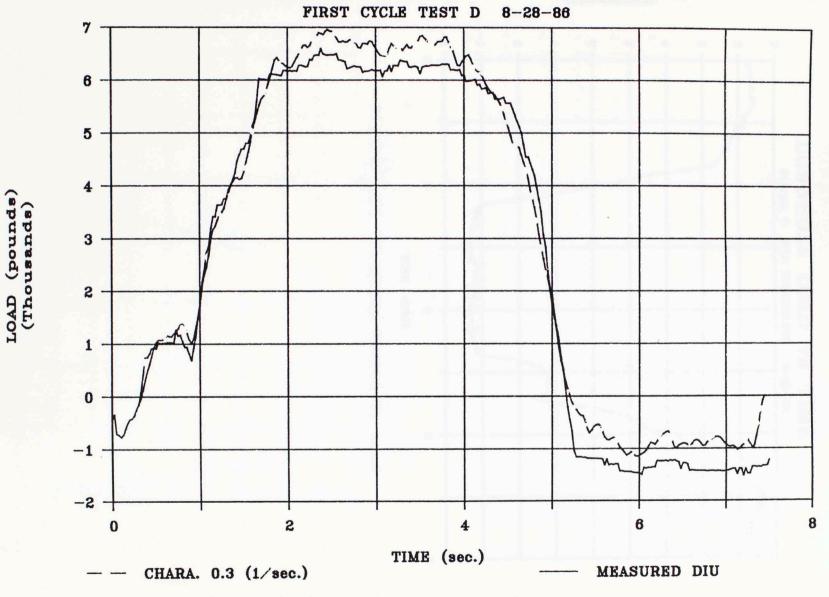


Figure 4.14 Measured and Predicted Load

DOWNHOLE LOAD vs TIME Sample C file: DYNCLD2.PIC 8-28-86

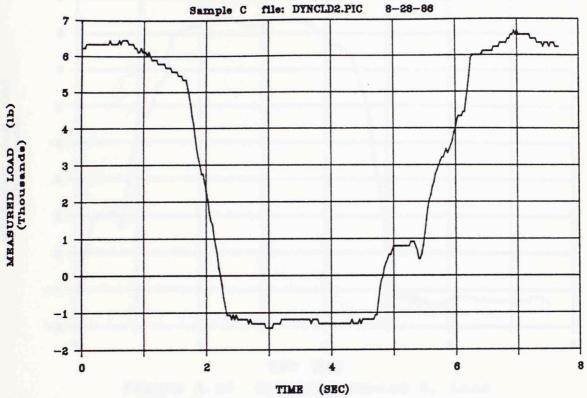


Figure 4.15 Sampling Period C. Load



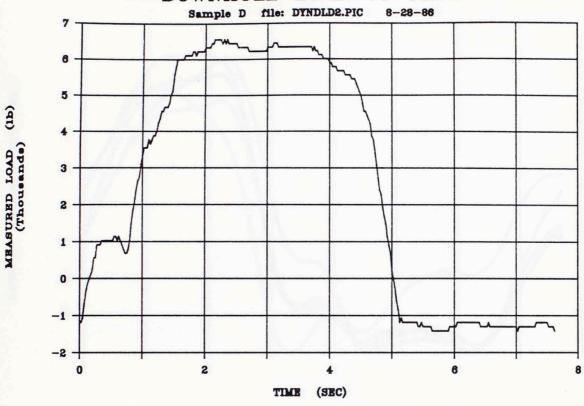
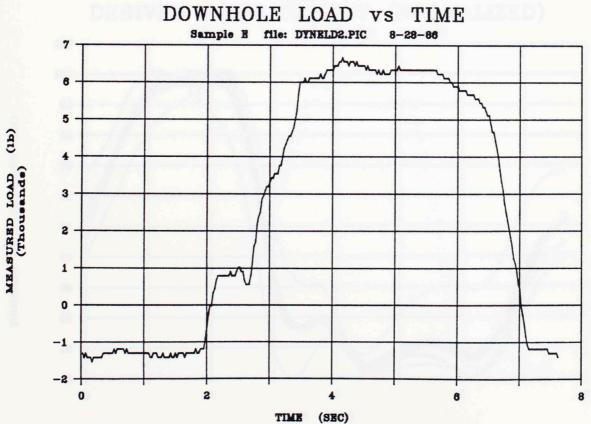


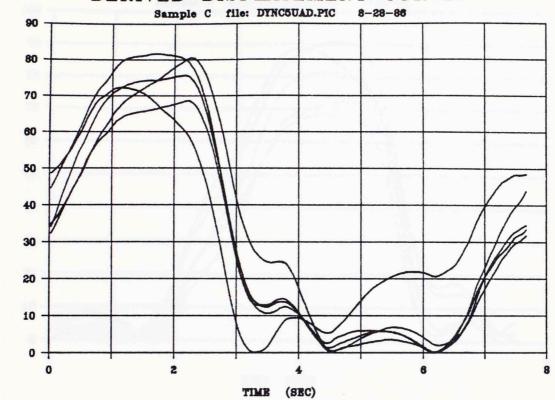
Figure 4.16 Sampling Period D, Load



60

Figure 4.17 Sampling Period E, Load

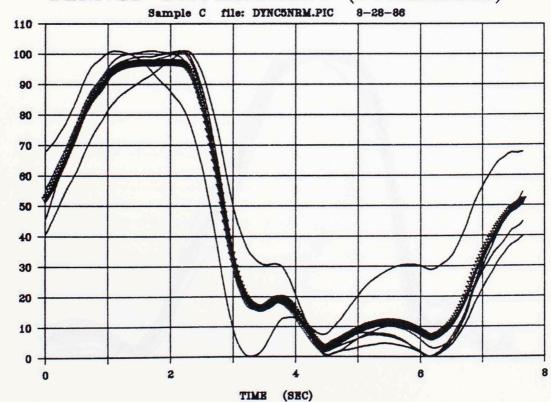
DERIVED DISPLACEMENT CURVES



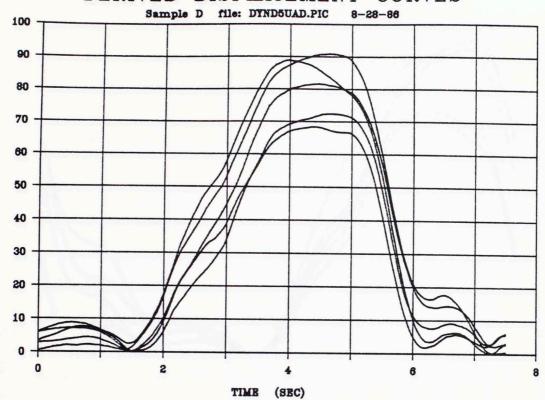
DERIVED DISPLACEMENT (IN)

DERIVED DISPLACEMENT (IN)

DERIVED DISPLACEMENT (NORMALIZED)



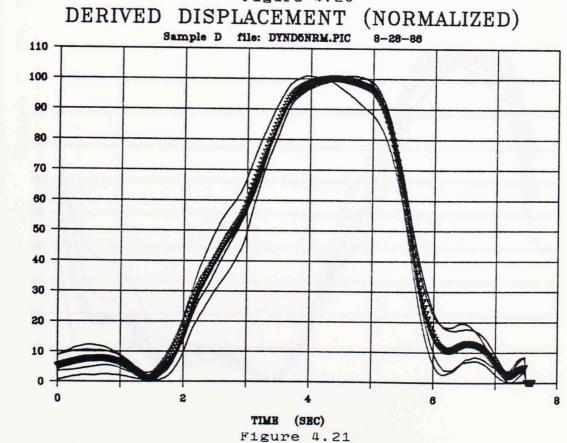




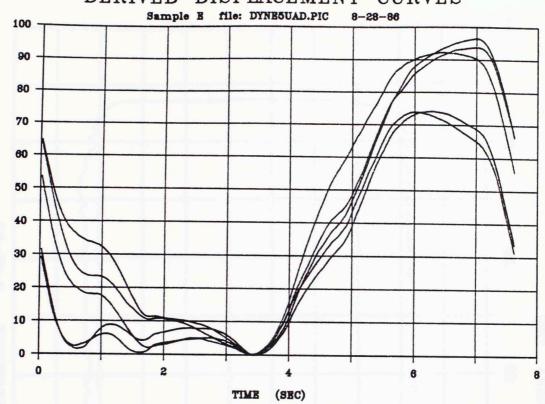
DERIVED DISPLACEMENT (IN)

DERIVED DISPLACEMENT (IN)

Figure 4.20



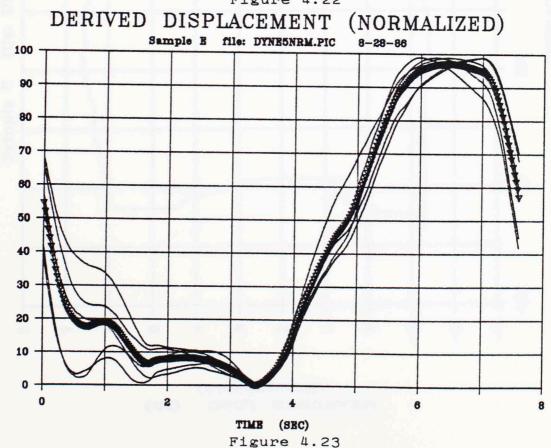




DERIVED DISPLACEMENT (IN)

DERIVED DISPLACEMENT (IN)

Figure 4.22



DOWNHOLE DYNAGRAPH

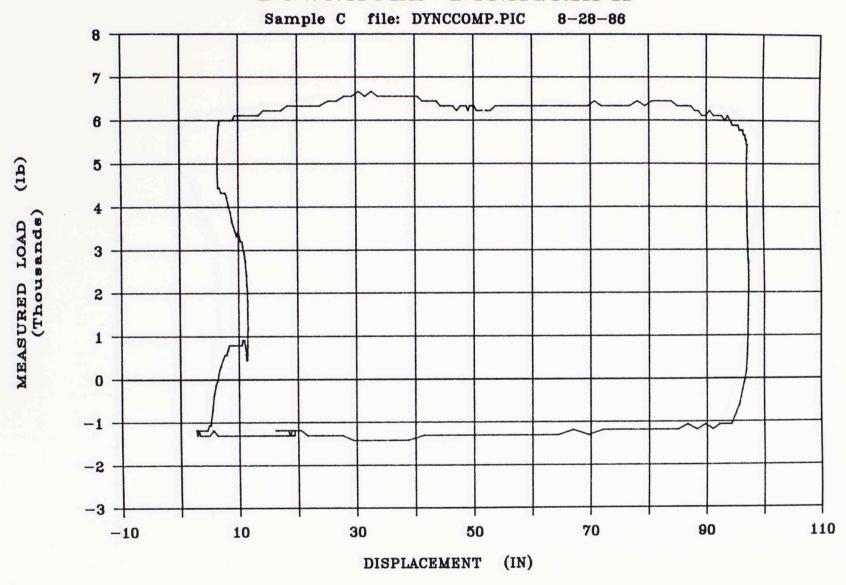


Figure 4.24 Sampling Period C. Downhole Dynagraph

DOWNHOLE DYNAGRAPH

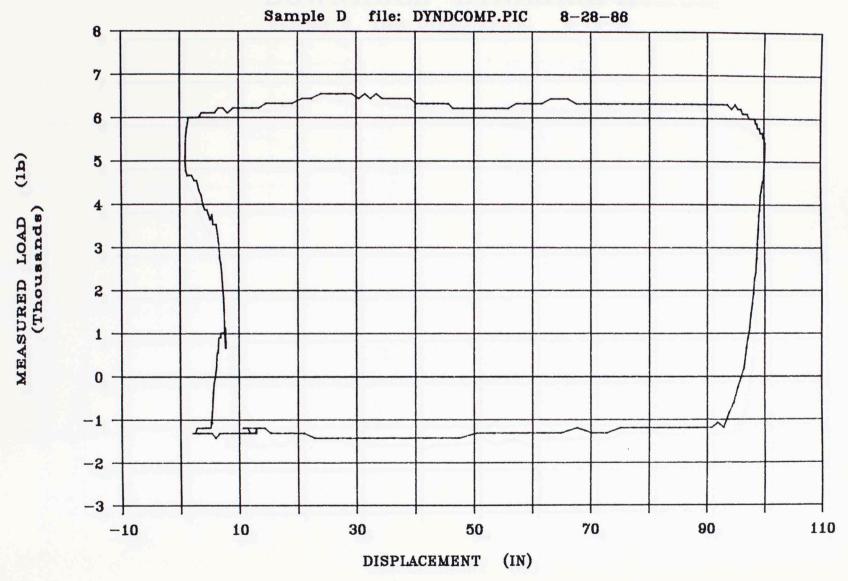


Figure 4.25 Sampling Period D, Downhole Dynagraph

DOWNHOLE DYNAGRAPH

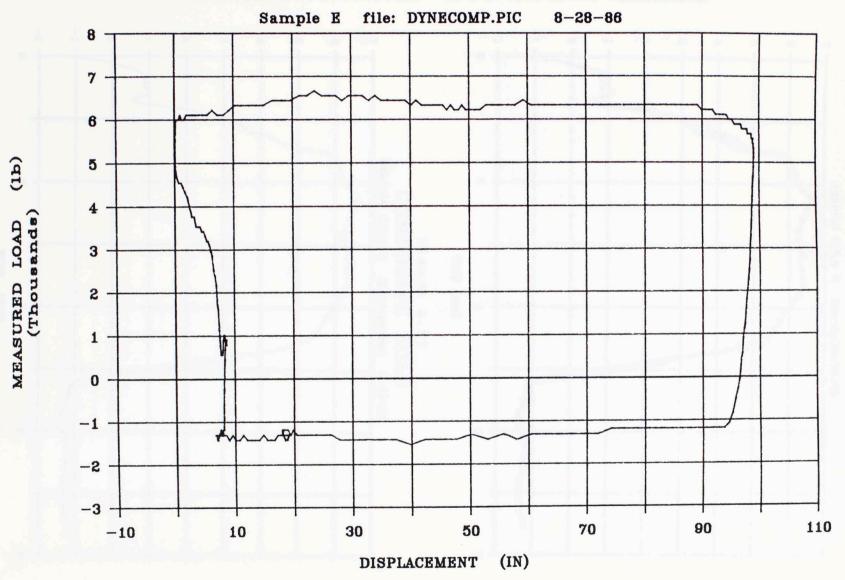
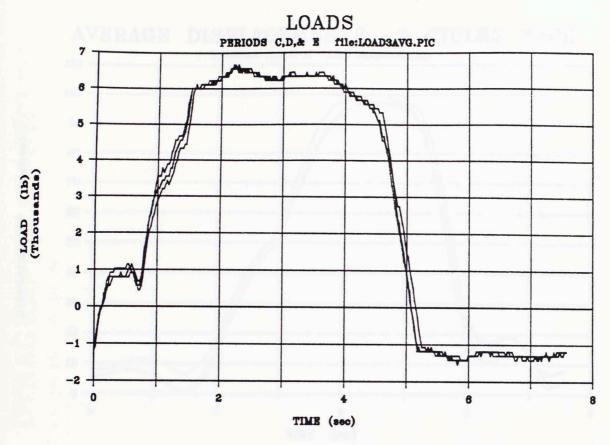
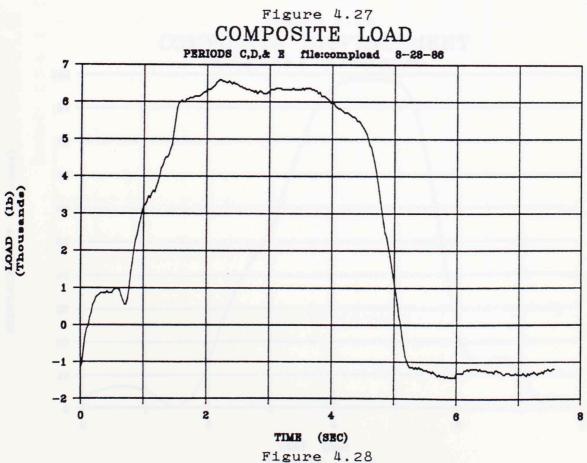
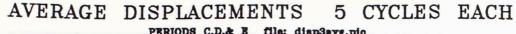
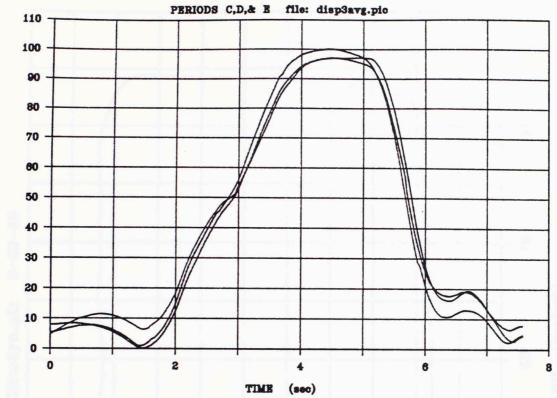


Figure 4.26 Sampling Period E, Downhole Dynagraph







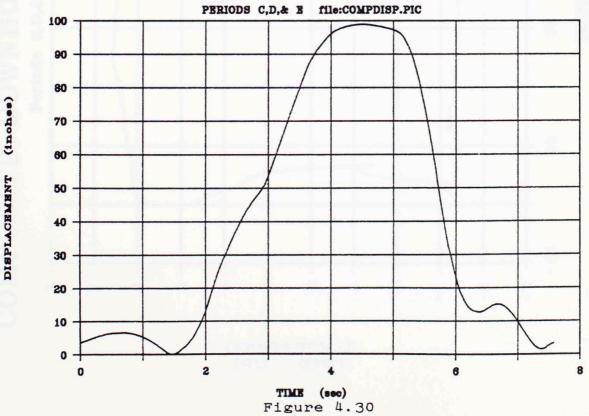


(Inohes)

DISPLACEMENT

Figure 4.29

COMPOSITE DISPLACEMENT



COMPOSITE DOWNHOLE DYNAGRAPH, 15 CYCLES

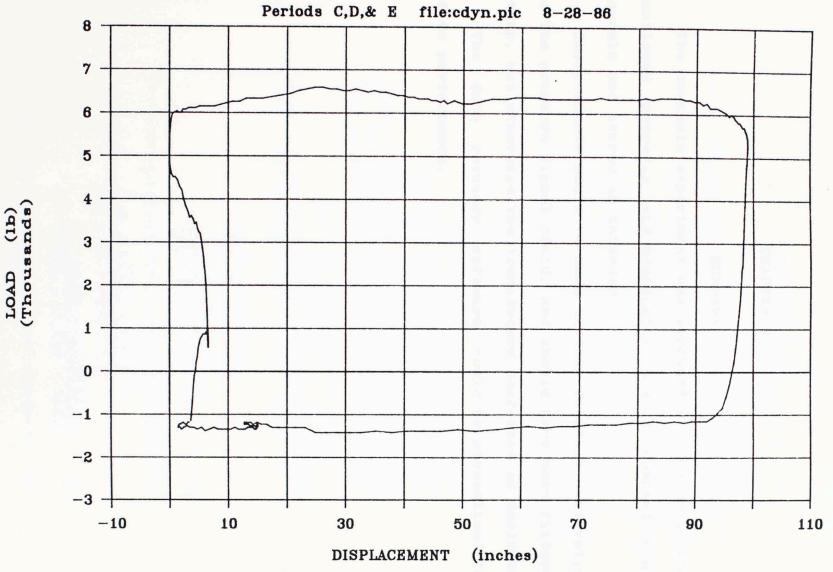


Figure 4.31 Composite Downhole Dynagraph

CHAPTER V

SUMMARY

The downhole experiment was successful. The controller functioned properly and meaningful data was sampled on all channels and stored as intended.

Improvements could be made in the position derivation and the pressure signal could, and should have been filtered better, but otherwise the transducers performed as desired.

The data recovery software could be streamlined for faster performance.

APPENDIX A

WHEATSTONE BRIDGE IN STRAIN GAGE APPLICATION

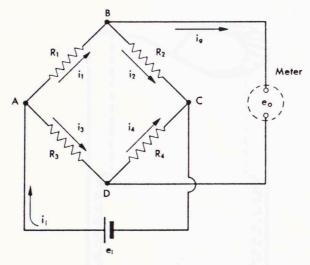


Fig. 7.13 Simple Wheatstone bridge circuit.

a) The voltage-sensitive Wheatstone bridge. Let us consider the simplest case first, in which the bridge output is connected directly to a high-impedance device, say an oscilloscope. Referring to Fig. 7.13, we find that

$$e_0 = i_{ABC}R_1 - i_{ADC}R_3,$$

and making use of relations developed in the derivation for null-balance condition and Ohm's law, we may write

$$\begin{split} e_{9} &= e_{i} \bigg(\frac{R_{1}}{R_{1} + R_{2}} - \frac{R_{3}}{R_{3} + R_{4}} \bigg) \\ &= e_{i} \bigg(\frac{R_{1}R_{4} - R_{2}R_{3}}{(R_{1} + R_{2})(R_{3} + R_{4})} \bigg). \end{split} \tag{7.42}$$

We will now assume that resistance $R_{\rm 1}$ changes by an amount $\Delta R_{\rm 1}$, or

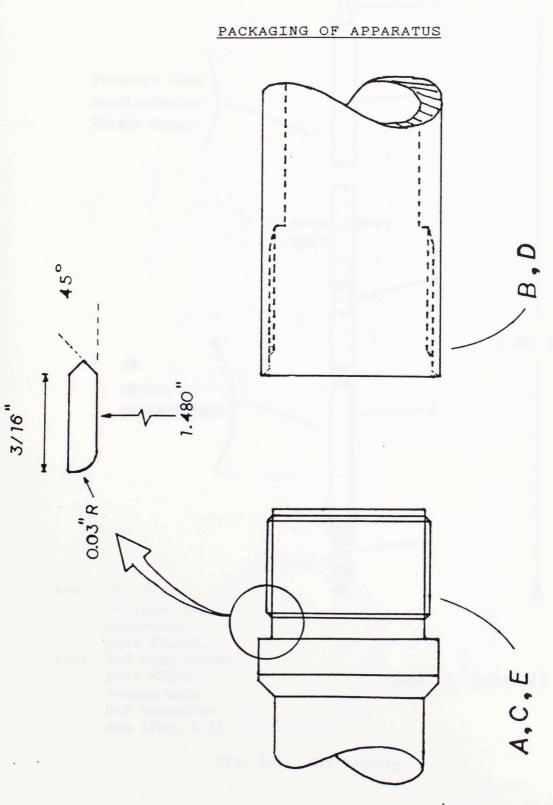
$$\frac{e_0 + \Delta e_0}{e_i} = \left[\frac{(R_1 + \Delta R_1)(R_4) - R_2 R_3}{(R_1 + \Delta R_1 + R_2)(R_3 + R_4)} \right]
= \left\{ \frac{1 + (\Delta R_1/R_1) - (R_2 R_3/R_1 R_4)}{[1 + (\Delta R_1/R_1) + (R_2/R_1)][1 + (R_3/R_4)]} \right\}.$$
(7.43)

The relation may be simplified by assuming all resistances to be initially equal (in which case $e_0 = 0$). Then

$$\frac{\Delta e_0}{e_i} = \frac{\Delta R_1/R}{4 + 2(\Delta R_1/R)}. (7.44)$$

(ref Mechanical Measurements) Addison Wesley pob.

APPENDIX B



(REF. J. CHACIN)

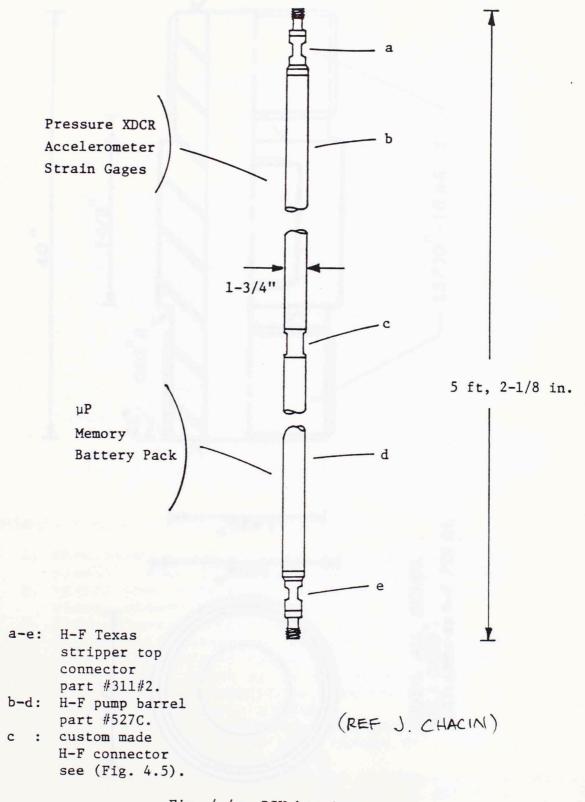
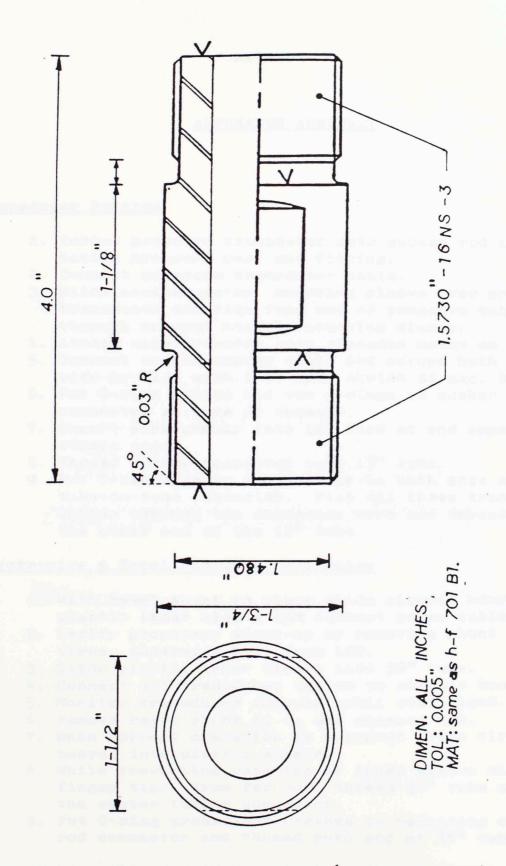


Fig. 4.4: DIU housing.



(REF. J. CHACIN)

APPENDIX C

APPARATUS ASSEMBLY

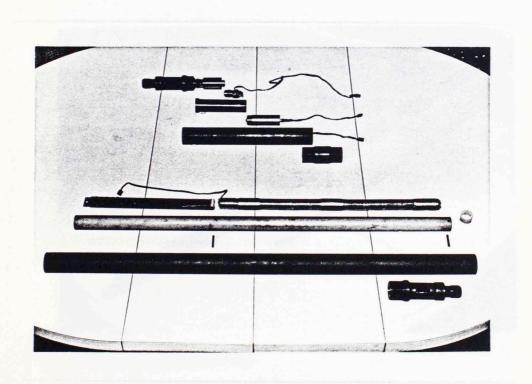
Transducer Portion

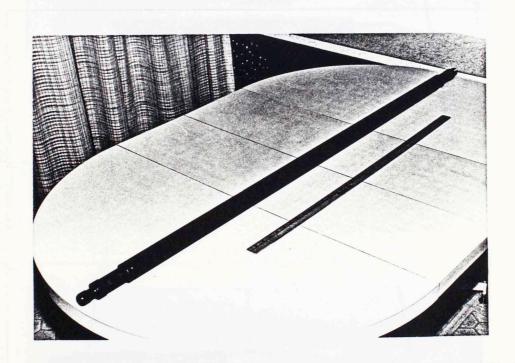
- 1. Torque pressure transducer onto sucker rod connector having pressure port and fitting.
- 2. Connect pressure transducer cable.
- 3. Slide accelerometer mounting sleeve over pressure transducer and fish free end of pressure cable through passage hole in mounting sleeve.
- 4. Attach accelerometer onto threaded mount on sleeve.
- 5. Connect accelerometer cable and secure both cables side-by-side with 1/4" heat shrink at acc. base.
- 6. Put O-ring grease and new O-rings on sucker rod connector at base of threads.
- 7. Insert subassembly into 12" tube at end opposite the strain gages.
- 8. Thread sucker connector into 12" tube.
- 9. Put O-ring grease and O-rings on both ends of the tube-to-tube connector. Fish all three transducer cables through the connector bore and thread onto the other end of the 12" tube.

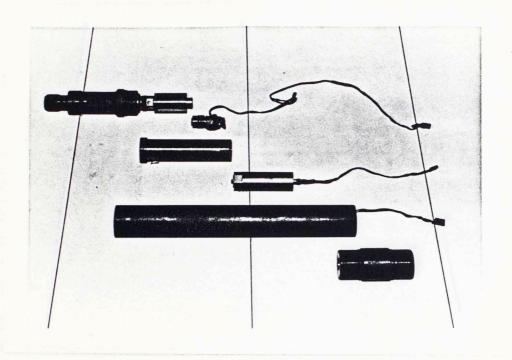
Electronics & Total Assembly Completion

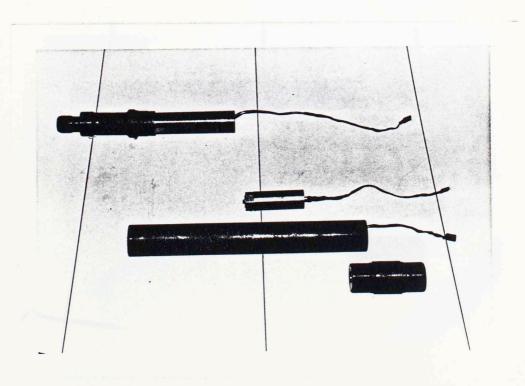
- 1. With reset shunt in place slide circuit board into plastic inner sleeve and connect power cable.
- 2. Verify processor start-up by removing shunt a few times, observing blip from LED.
- 3. Slide plastic inner sleeve into 36" tube.
- 4. Connect all transducer cables to circuit board.
- 5. Monitor transducer outputs until stabilized.
- 6. Remove reset shunt at to and observe LED.
- 7. When correct operation is observed slide circuit boards into plastic sleeve.
- 8. While preventing rotation of inner sleeve with finger tips, from far end, thread 36" tube onto the center tubing connector.
- 9. Put O-ring grease and O-rings on remaining sucker rod connector and thread onto end of 36" tube.

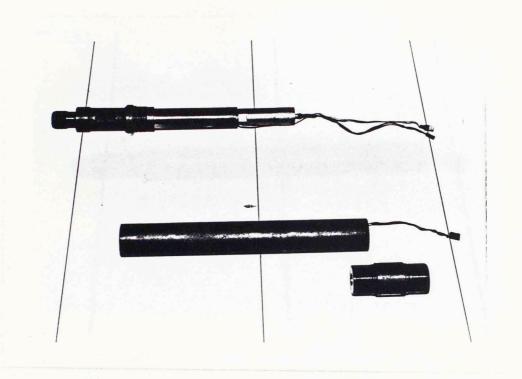
NOTE: Subassembly should be oriented with the pressure port down when mounted into string for correct accel. polarity.

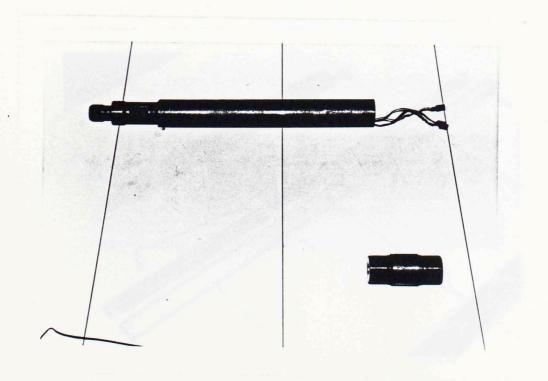


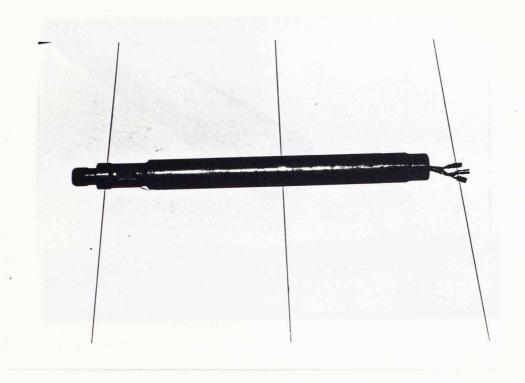


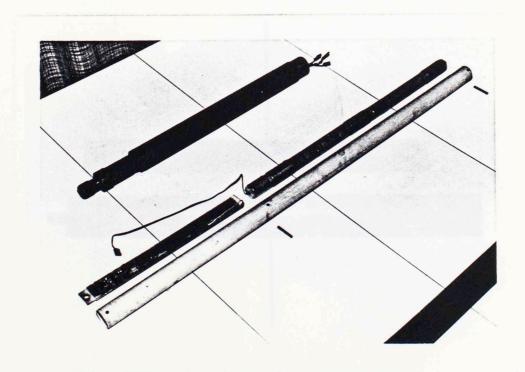


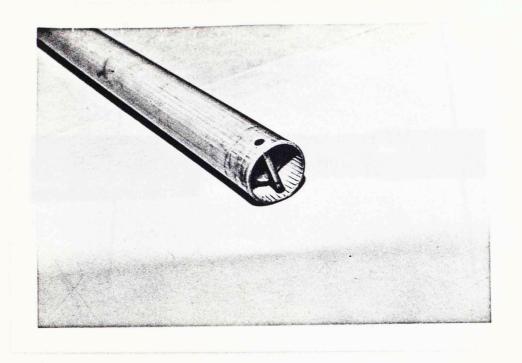


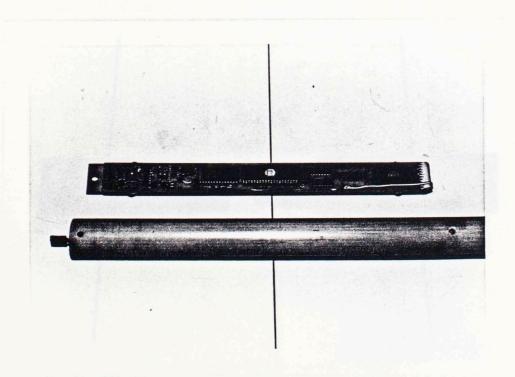


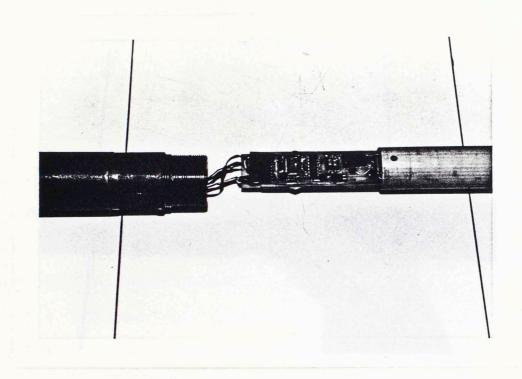


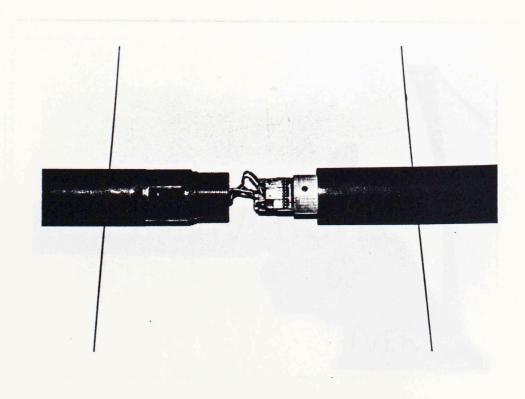


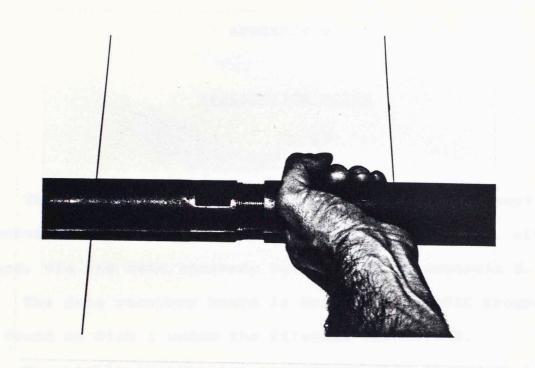














APPENDIX D

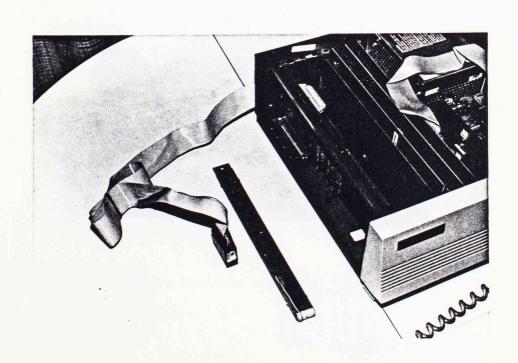
APPLICATION NOTES

The photographs on the next page show the correct configuration for reading and writing the apparatus circuit board, via the data recovery board shown in Appendix E.

The data recovery board is driven by a BASIC program to be found on Disk 1 under the filename DATREC.BAS.

The highly interactive program is also listed in Appendix E.

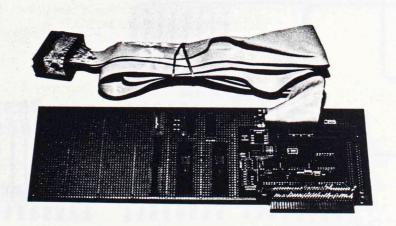


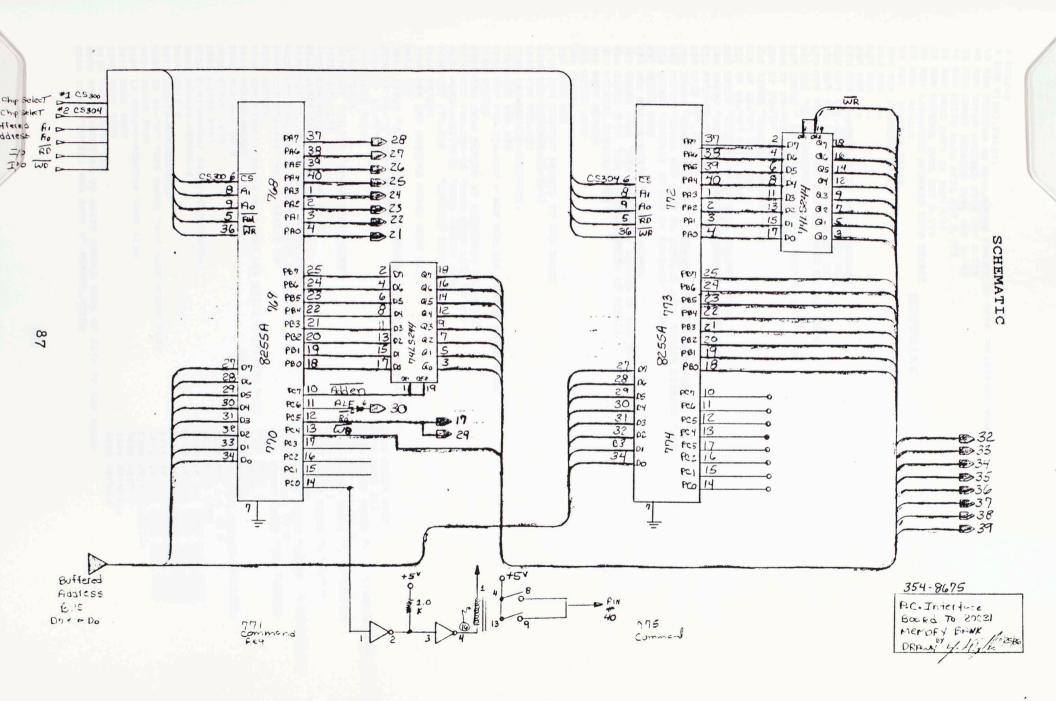


APPENDIX E

DATA RECOVERY BOARD

Below is a photograph of the data recovery board. The following pages include the schematics and program listing for the software mentioned in Appendix D.





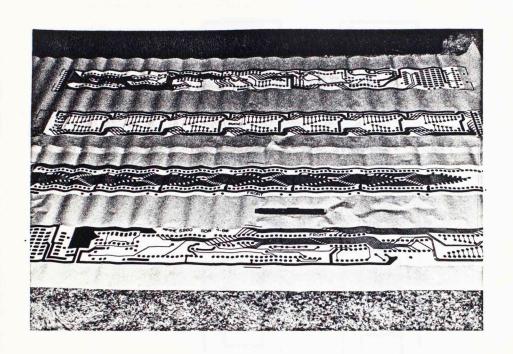
```
2 SKIP=0
5 DIM D(32).D$(32)
10 REM PROGRAM TO READ/WRITE MEMORY ON DATA COLLECTION BOARD
20 REM UPPER ADDRESS BYTE OUT X.768
30 REM LOWER ADDRESS BYTE OUT X. 769
40 REM WRITE DATA BYTE OUT X.772
50 REM READ DATA IN INP(773)
60 REM CONTROL BYTE OUT X,770
70 REM 128-LOWER ADDRESS BYTE ENABLE
                                        SOFTWARE
80 REM 64=ALE
90 REM
        32-READ PULSE
100 REM 16-WRITE PULSE
110 REM 8=
120 REM
130 REM
140 REM 1-POWER ON TO 40 PIN SOCKET
150 OUT 771.128 'SET UP OF 8255A U1
160 OUT 775.130 'SET UP OF 8255A U2
170 OUT 770,255 'SET CONTROL BYTE TO ALL ONES
180 CLS 'CLEAR SCREEN
190 INPUT " POWER ON TO 40 PIN SOCKET Y/N ", P$
200 IF P$="Y" THEN OUT 770,254
210 IF P$="N" THEN GOTO 190
215 INPUT "Read or Write? ",Q$
216 IF Q$="R" THEN 218
217 IF Q$="W" THEN 6000
218 INPUT "DESIRED # OF DATA COLUMNS >": N
220 INPUT "NAME OF FILE FOR STORAGE ON DISK ", F$
230 FIL$=F$+". PRN"
240 OPEN "O", #1, FIL$
250 INPUT "START AND STOP ADDRESSES >". MEMST, MEMSTOP
265 INPUT "WOULD YOU LIKE TO DISPLAY DATA BEFORE STORING ", P$
266 INPUT "DISPLAY IN Hex or Decimal? >".B$
267 GOSUB 5000
270 FOR MEMADD=MEMST TO MEMST+MEMRD
280 GOSUB 1000 'SUB TO CONVERT MEMADD TO TWO BYTES
290 GOSUB 2000 'SUB TO READ MEMORY AT MEMADD
300 PRINT#1. MEMADD: MEMDA
310 NEXT MEMADD
315 GOSUB 3000
320 CLOSE
330 GOTO 220
1000 REM CONVERT MEMADD TO TWO BYTES
1010 UBY=INT(MEMADD/256)
1020 OUT 768. UBY
1030 LBY=MEMADD-(UBY*256)
1040 OUT 769. LBY
1050 OUT 770.254-192 : OUT 770.254 'LATCH LOWER BYTE
1060 RETURN
2000 REM READ MEMORY AS ADDRESSED BY MEMADD
2010 OUT 770,254-32 'MAKE READ LINE GO LOW 2020 MEMDA=INP(773) 'READ MEMORY DATA
                     'RESTORE READ LINE
2030 OUT 770,254
2040 RETURN
3000 REM END READING POWER DOWN Y/N
3010 CLS
3020 INPUT "MEMORY READ OVER POWER DOWN SOCKET ? Y/N " .P$
3030 IF P$="N" THEN RETURN
3040 IF P$="Y" THEN 3100
                                                             6020 GOSUB 4000
                                                             6030 GOTO 215
                                                                                     "; HEX$ (MEMADD-N-SKIP);
                                                             7000 PRINT USING "
3050 GOTO 3020
3100 CLOSE
                                                             7010 FOR I=1 TO N
                                                             7020 PRINT USING "\ \"; D$(I);
3110 OUT 770,255 'POWER DOWN SOCKET
3120 GOTO 190
                                                             7030 NEXT I
4000 REM WRITING TO MEMORY
4010 GOSUB 1000 CONVERTS MEMADD TO TWO BYTES
                                                             7040 PRINT USING "\ ":" "
                                                             7050 RETURN
                                                             7100 PRINT USING "##### "; (MEMADD-N);
4020 OUT 772, WRTDA 'LOADS WRITE DATA
4030 OUT 770.254-16 'DROPS WRITE ENABLE
4040 OUT 770.254 'WRITE ENABLE UP
                                                             7110 FOR I=1 TO N
                                                             7120 PRINT USING "### ":D(I):
4050 RETURN
5000 REM SUBROUTINE TO READ MEM AND PRINT N COLUMNS WITH 7130 NEXT I
                                                 HEX ADDRESS 7150 RETURN
5010 MEMADD=MEMST
                                                              8000 PRINT#1.MEMADD-(N+SKIP);
5020 FOR M=1 TO N
5030 GOSUB 1000
                                                              8010 FOR I=1 TO N
5040 GOSUB 2000
                                                              8011 GOTO 8020
5050 D(M)=MEMDA: D$(M)=HEX$(MEMDA)
                                                              8012 IF I=1 THEN GOTO 8030
5060 MEMADD=MEMADD+1
                                                              8013 IF I=2 THEN GOTO 8030
5070 NEXT M
                                                              8014 IF I=3 THEN GOTO 8030
5075 MEMADD=MEMADD+SKIP
                                                              8015 IF I=5 THEN GOTO 8030
5080 IF B$="H" THEN GOSUB 7000 ELSE GOSUB 7100
                                                              8016 IF I=6 THEN GOTO 8030
5090 GOSUB 8000
                                                              8020 PRINT#1.D(I):
5100 IF MEMADD>MEMSTOP THEN 5130
                                                              8030 NEXT I
5110 GOTO 5020
                                                              8040 PRINT#1.
5120 GOTO 5020
                                                              8050 RETURN
5130 CLOSE: GOTO 215
6000 REM SUBROUTINE TO WRITE SINGLE BYTE OF DATA TO MEM BOARD
6010 INPUT "ENTER: ADD, DATA >", MEMADD, WRTDA
```

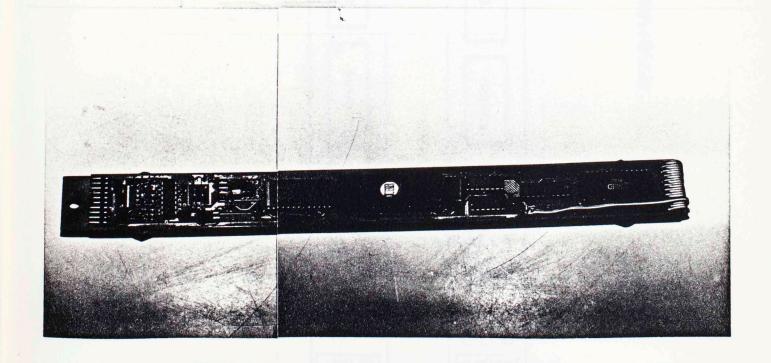
APPENDIX F

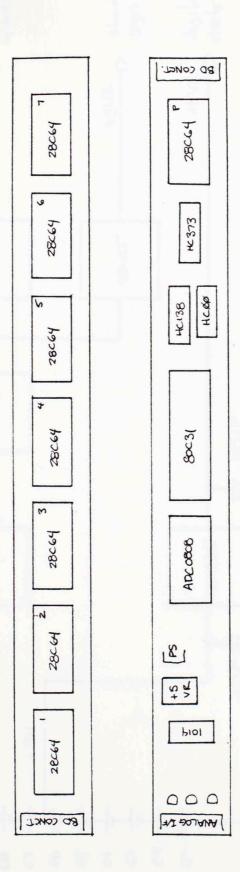
ELECTRICAL CIRCUITS

This appendix contains the complete circuit documentation, including schematics, assembly drawings, power distribution schematic, and printed circuit board artworks.

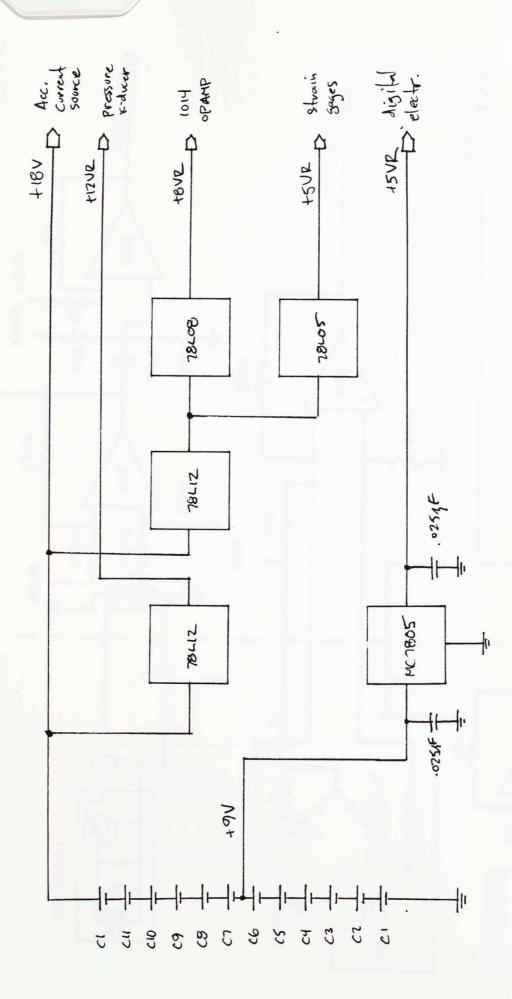
There are also photographs of the finished assembly and the 8:1 originals from which the artworks were made.



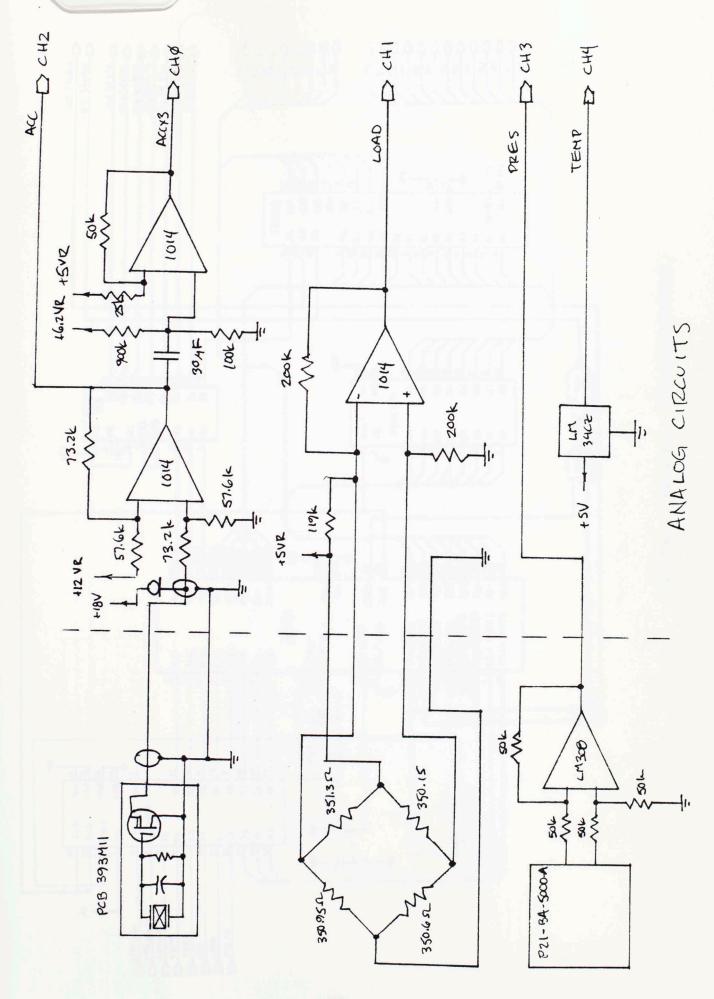


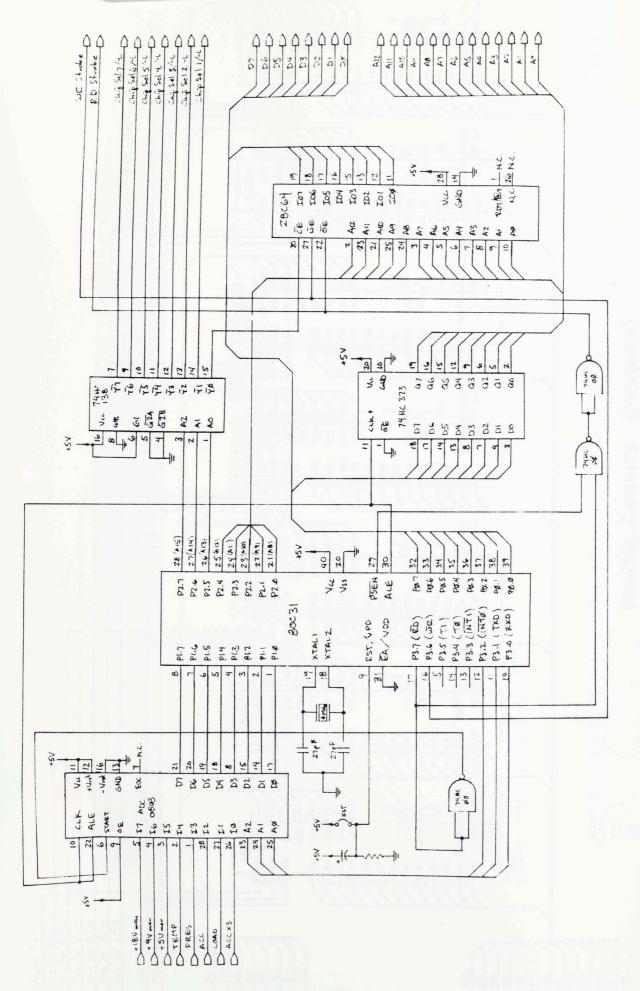


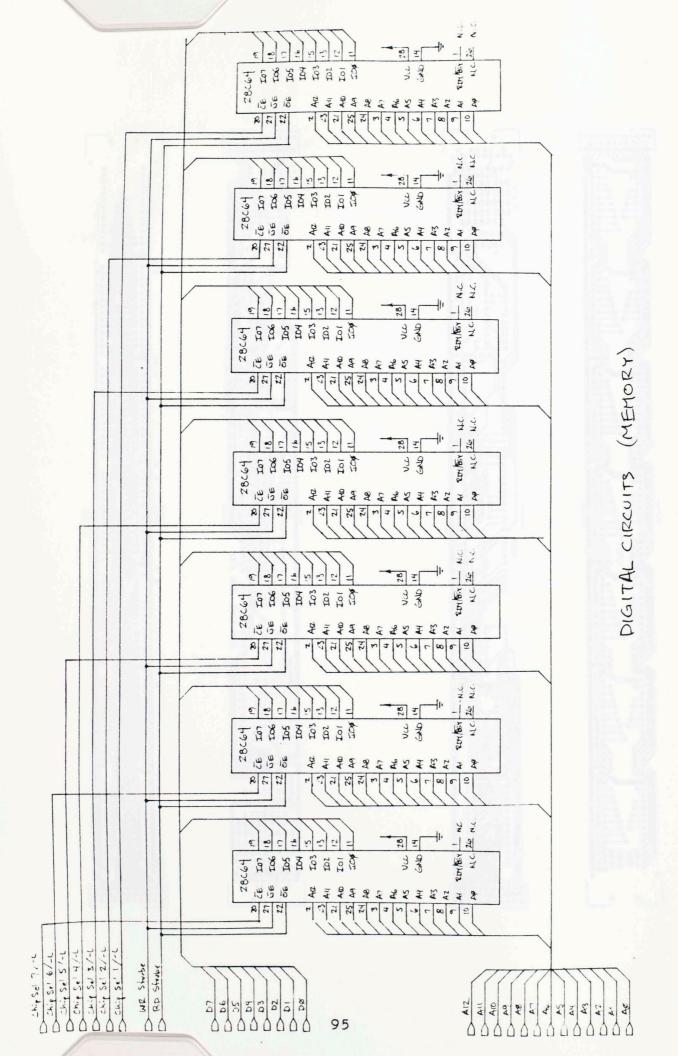
ASSEMBLY DRAWING

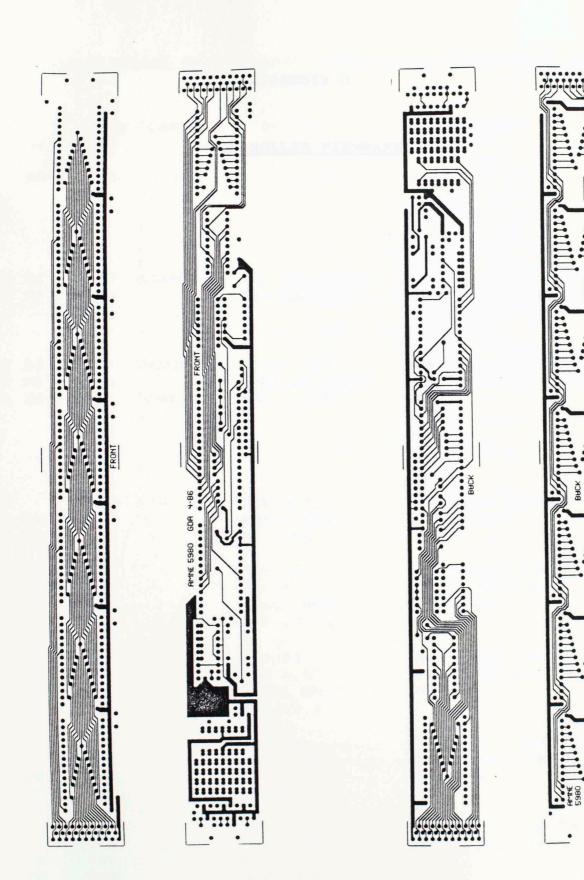


POWER DISTRIBUTION









APPENDIX G

CONTROLLER FIRMWARE

ASSEMBLY LANGUAGE PROGRAM for DOWNHOLE DATA ACQUISITION SYSTEM

	DE	ADD	LABEL	OPCODE	COMMENTS
B1	B2 B	3			
01	30	000	ORG:	AJMP START	
			;		
			;		
			;		
			;		
7B	01	030	START:	MOV R3, #02H	; Init. TABLE POINTER
7C	OF	032		MOV R4, #OFH	;Set # of lines (M) in
					:START/STOP/MODE table
			;		
11	50	034	REDOX:	ACALL DOX	Get Nth sampling period
DC	FC	036		DJNZ R4 REDOX	; information, N=max?
01	38	038	DONE:	AJMP DONE	; END
			;		
			:		
			; By		
			:		
EB		050	DOX:	MOV A,R3	; Fetch HI byte of
11	7E	051		ACALL MOVC	;STARTADD
	83	053		MOV DPH, A	, ormande
			;	nov Brin, n	
OB		055		INC R3	:increment TABPTR
EB		056		MOV A, R3	; Fetch LO byte of
11	7E	057		ACALL MOVC	;STARTADD
F5		059		MOV DPL, A	, STARTADD
				MOV DEL, A	
OB		05B		INC R3	.inonomont TARDED
EB		05C			;increment TABPTR
11	7 F	05D		MOV A, R3	; Fetch HI byte of
FA	7 1	05F		ACALL MOVC MOV R2, A	;STOPADD
1 11		OJI		MOV RZ, A	
ОВ		060	MARINITAL	INC DO	MARDER N
EB		061		INC R3	; increment TABPTR
11	7 E	062		MOV A, R3	; Fetch LO byte of
F9	, -	064		ACALL MOVC	;STOPADD
1 9		004		MOV R1, A	
ов		065	•	INC PO	
EB		066		INC R3	;increment TABPTR
11	7E	067		MOV A, R3	;Fetch MODE byte
F5	28	069		ACALL MOVC MOV 28,A	
1)			•	110 V 20, A	
31	00	06B		ACALL DO	
J-				ALL DO	Execute Nth samp period

OB	06D		INC R3	; advance TABPTR to next
OB	06E		INC R3	; line in table
OB	06F		INC R3	
OB	070		INC R3	
		;		
22	071		RET	;next N
		;		
		;		
83	07E	MOVC:	MOVC A,@A+PC	
22	07F		RET	
		;		
		; in the track of the		

SAMPLE POINTER TABLE_

ADD	SAMPLE	START	STOP	MODE	T 4 2	2
	FERTOD	DITE	DILE		Initial	Delay Set
		HI LO	HI LO			Initial
						Delay
080	OA:	XH XL	29 60	88 ;	XH XL	(min)
088	A:	30 00	48 00	24		
090	AB:	29 60	29 BO	24 ;	20 00	300
098	B:	48 00	60 00	24	20 FO	270
OAO	BC:	29 BO	2A 00	88 ;	21 E0	240
8A0	C:	60 00	78 00	24	22 DO	210
OBO	CD:	2A 00	2A 50	88	23 CO	180
0B8	D:	78 00	90 00	24	24 BO	150
OCO	DE:	2A 50	2A A0	88	25 AO	120
0C8	E:	90 00	A8 00	24		90
ODO	EF:	2A A0	2A FO	88		60
OD8	F:	A8 00	CO 00	24		30
OEO	FG:	2A FO	2E 40	88	29 10	10
OE8	G:	CO 00	00 00			1
OFO	GZ:	23 40	30 00	88	LEB SILEM	
	080 088 090 098 0A0 0A8 0B0 0B8 0C0 0C8 0D0 0D8 0E0	PERIOD 080 OA: 088 A: 090 AB: 098 B: 0A0 BC: 0A8 C: 0B0 CD: 0B8 D: 0C0 DE: 0C8 E: 0D0 EF: 0D8 F: 0E0 FG: 0E8 G:	PERIOD BYTE HI LO 080 OA: XH XL 088 A: 30 00 090 AB: 29 60 098 B: 48 00 0A0 BC: 29 B0 0A8 C: 60 00 0B0 CD: 2A 00 0B8 D: 78 00 0C0 DE: 2A 50 0C8 E: 90 00 0D0 EF: 2A A0 0D8 F: A8 00 0E0 FG: 2A F0 0E8 G: CO 00	PERIOD BYTE BYTE HI LO HI LO 080 OA: XH XL 29 60 088 A: 30 00 48 00 090 AB: 29 60 29 B0 098 B: 48 00 60 00 0A0 BC: 29 B0 2A 00 0A8 C: 60 00 78 00 0B0 CD: 2A 00 2A 50 0B8 D: 78 00 90 00 0C0 DE: 2A 50 2A A0 0C8 E: 90 00 A8 00 0D0 EF: 2A A0 2A F0 0D8 F: A8 00 C0 00 0E0 FG: 2A F0 2E 40 0E8 G: CO 00 00 00	PERIOD BYTE BYTE HI LO HI LO 080 OA: XH XL 29 60 88 088 A: 30 00 48 00 24 090 AB: 29 60 29 B0 24 098 B: 48 00 60 00 24 0A0 BC: 29 B0 2A 00 88 0A8 C: 60 00 78 00 24 0B0 CD: 2A 00 2A 50 88 0B8 D: 78 00 90 00 24 0C0 DE: 2A 50 2A A0 88 0C8 E: 90 00 A8 00 24 0D0 EF: 2A A0 2A F0 88 0D8 F: A8 00 C0 00 24 0E0 FG: 2A F0 2E 40 88 0E8 G: CO 00 00 00 42	PERIOD BYTE BYTE Initial HI LO HI LO 080 OA: XH XL 29 60 88 XH XL 088 A: 30 00 48 00 24 090 AB: 29 60 29 B0 24 20 00 098 B: 48 00 60 00 24 20 F0 0A0 BC: 29 B0 2A 00 88 21 E0 0A8 C: 60 00 78 00 24 22 D0 0B0 CD: 2A 00 2A 50 88 23 C0 0B8 D: 78 00 90 00 24 24 B0 0C0 DE: 2A 50 2A A0 88 25 A0 0C8 E: 90 00 A8 00 24 26 90 0D0 EF: 2A A0 2A F0 88 27 80 0D8 F: A8 00 C0 00 24 28 70 0E0 FG: 2A F0 2E 40 88 29 10 0E8 G: CO 00 00 00 42 29 58

MODE DEFINITION: 88=Channels 0-7, 1/60 Hz each 24=Channels 0-3, 40 Hz each

42=Channels 0-1, 20 Hz each

; DO is the main routine ; and executes calls to

CODE ADD LABEL

B1 B2 B3

; three routines that ; sample and save data and ; wait app. sampling delay 31 40 100 DO: ACALL SAMPSTOR 31 70 ACALL SAVE 102 31 20 104 ACALL BLINK 31 28 106 ACALL DELAY 108 MOV A, R2 :Test for DPTR=STOPADD. B5 83 05 109 CJNE A, DPH CHI ; first the HI bytes, if E9 10C MOV A,R1 ; equal, B5 82 04 10D CJNE A. DPL CLO ; then the LO 22 110 RET ; DPTR=STOPADD, exit DO ; 00 111 CHI: NOP ; continue since inequal 00 112 NOP ; balance path with that 00 113 NOP ; if HI bytes were equal 21 00 114 CLO: AJMP DO ; take another sample set C2 B4 120 BLINK: CLR P3.4 ;Blink LED (2mS) 31 BO 122 ACALL 2ms D2 B4 124 SET B P3.4 22 126 RET : 20 45 06 128 DELAY: JB 45 CALL40Hz ; Test MODE for sampling 20 46 06 12B JB 46 CALL20Hz ; rate (required overhead 20 47 06 12E JB 47 CALL60s ; wait) 31 CO 131 CALL40Hz: ACALL FILL40Hz ; call for 40 Hz overhead 22 133 RET ; delay 134 CALL20Hz: ACALL FILL20Hz ; call for 20 Hz overhead 31 DO 22 136 RET :delay

	DDE L B2			D LABEL	OPCODE	COMMENTS
_				•		
31 22	EC)	137 139	CALL60s:	ACALL FILL60s RET	;call for 60 second ;overhead delay
						:SAMPSTOR samples the ;A/D channels defined by ;the MODE byte and store
						; them temporarily in uP
					MOV A. 620 MOVE SOFTE. A	;RAM until they can be ;saved as a group in the ;EEPROM memory by SAVE
				; 15		, BETTOT MEMOTY BY BAVE
78	20		140	SAMPSTOR:	MOV RO, #20H	; initialize RAM pointer
74 48	F8		142 144	NEXSAMP:	MOV A, #F8H ORL A, RO	; mask upper five bits
				;	a debugi salamanna a alam	
F5 E0	ВО		145 147		MOVY A ADDTE	; output A/D address
EU			147		MOVX A,@DPTR	; latch add and activate ; WR strobe to start conv
31	AO		148		ACALL 200us	; wait for end of convrsn
	90		14A	FREELOCCE	MOV @RO, P1	;store data byte from A/
80			14C		INC RO	;inc RAM/ pointer and mo
E8			14D		MOV A, RO	;into ACC to test for CH
20	43	06	14E		JB 43 TESTACC3	; test MODE byte for CH#
			151		JB 42 TESTACC2	; desired per set and go
20	41	OE	154		JB 41 TESTACC1	; to appr. test branch
				•		
00			157	; TESTACC3:	NOP	;MODE said #CH=8, after
00			158	IESTACCS.	NOP	; balancing branch timing
00			159		NOP	; test ACC.3 to see if man
00			15A		NOP	:CH has been reached
30	EЗ	E4	15B		JNB ACC.3 NEXSA	MP ; If LO, sample next CH
22			15E		RET	; If HI, set done. Proceed
00			15F 160	TESTACC2:	NOP NOP	;repeat above for #CH=4
30	E2	DE	161		JNB ACC.2 NEXSA	MP
22			164		RET	
30 22	E1	DA	165 168	TESTACC1:	JNB ACC.1 NEXSA RET	MP ;repeat above for #CH=

; same logic as SAMPSTOR ; only to save in EEPROM ; the data stored sequen-:in RAM 78 20 170 SAVE: MOV RO, #20 E6 172 NEXSAVE: MOV A.@20 ; get data byte from RAM 173 MOVX @DPTR, A ; save it to EEPROM at ; data pointer address 31 BO ACALL 2msec ; wait 1+ EEPROM WR cycle A3 176 INC DPTR ; increment data pointer 08 177 INC RO ; (rest same as SAMPSTOR) E8 178 MOV A, RO 20 43 06 179 JB 43 TESTACC3 20 42 OB 17C JB 42 TESTACC2 20 41 OE 17F JB 41 TESTACC1 00 182 TESTACC3: NOP 00 183 NOP 00 184 NOP 00 185 NOP 30 E3 E9 186 JNB ACC. 3 NEXSAVE 22 189 00 18A TESTACC2: NOP 00 18B NOP 30 E2 E3 18C JNB ACC. 2 NEXSAVE 22 18F RET 30 E1 DF 190 TESTACC1: JNB ACC.1 NEXSAVE 22 193 RET

:Subroutine SAVE follows

7D 2E 1A0 200us: MOV R5, #2EH ; load least sig. tmr byte 7E 01 1A2 MOV R6, #01H ; load next sign. tmr byte 7F 01 1A4 MOV R7, #01H ; load most sign. tmr byte 31 FO 1A6 ACALL TIMER ; call timer to execute 22 1A8 RET ;200 microsecond delay

TIMERS

```
MOV R5, #EFH
7D EF
       1B0 2ms:
                     MOV R6, #02H
7E 02
        1B2
7F 01
                      MOV R7, #01H
                                     ; call timer to execute
        1B4
                      ACALL TIMER ;2 millisecond delay
        1B6
31 FO
                      RET
22
        1B8
       1CO FILL40Hz: MOV R5, #FFH
7D FF
                     MOV R6, #ODH
7E OD
        1C2
7F 01
        1C4
                     MOV R7, #01H
                     ACALL TIMER
31 FO
        1C6
                                     ; call timer to execute
                      RET
22
        1C8
                                     ; delay combining with
                                     : program overhead to
                                     ; produce 25 mS total
7D FF
        1D0 FILL20Hz: MOV R5, #FFH
7E 2A
        1D2
                     MOV R6, #2AH
7F 01
                      MOV R7, #01H
        1D4
31 FO
        1D6
                      ACALL TIMER
                                    ; execute 20 Hz (50 mS)
                      RET
22
                                     ; overhead
         FER LARRY
         BATRE
7D FF
        1EO FILL60s: MOV R5, #FFH
7E FF
        1E2
                     MOV R6, #FFH
7F E4
       1E4
                     MOV R7, #E4H
31 FO
        1E6
                                    ; execute 1/60 Hz (60 sec)
                      ACALL TIMER
22
                      RET
                                     ; overhead
          With a series of the
DD FE
        1FO TIMER: DJNZ R5 TIMER ; perform timer intervals
        1F2 DJNZ R6 TIMER ; by decrementing registrs
DE FC
                  DJNZ R7 TIMER ; until all zeroes.
DF FA
        1F4
22
        1F6
                 RET
```

ROUTINE FOR IN-SYSTEM PROGRAMMING OF PROGRAM MEMORY THROUGH ICE

-	00	00		START1:		;init data pointr to 0000
E4			203	CONT:	CLR A	; clear base register
93			204		MOVC A, @A+DPTR	;get program mem byt from
FO			205		MOVX @DPTR, A	;ICE mem and write to
31	BO		206		ACALL 2ms	; data acqu. bd. prog. mem
A3			208		INC DPTR	; get ready for next byte
E5	83		209		MOV A, DPH	; test data pointer for 1k
30	E2	F5	20B		JB E2 CONT	; copied. no, copy nex byt
31	20		20E		ACALL BLINK	; yes, blink LED & quit
61	10		210	DONE1:	AJMP DONE1	

APPENDIX H

DISK FILE LISTINGS

The following disk files can be found in the cover of this document.

Volume in drive A is DISK 1 Directory of A:\

MASTER WK1 116052 11-14-86 1:58a FCALA282 WK1 24166 1-01-80 1:10a DATREC BAS 2637 1-01-80 12:03a RUN828G PRN 139646 1-01-80 12:55a 4 File(s) 77824 bytes free

Volume in drive A is DISK 2 Directory of A:\

RUN828A PRN 41941 1-01-80 1:13a RUN828B PRN 41925 1-01-80 2:24a RUN828C PRN 41954 1-01-80 1:56a RUN828D PRN 41923 1-01-80 1:42a RUN828E PRN 41864 1-01-80 1:25a RUN828F PRN 41742 1-01-80 1:08a RUN828OA PRN 21437 1-01-80 12:18a 7 File(s) 89088 bytes free