OPTIMIZED MULTI-INPUT SINGLE-OUTPUT

ENERGY HARVESTING SYSTEM

By

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&

 I dedicate this work to my late father and my lovely mother who helped shape me into the person that I am!

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Abstract: The energy harvesting sources have been introduced as a promising alternative for battery power. However, harvested energy is inherently sporadic, unstable, and unreliable. For this reason, the non-volatile processor has been previously proposed to bridge the intermittent executions in frequent power losses. Nonetheless, recurrent power failures reduce overall system performance which has forced researchers to look into multi-input energy harvesting systems. The purpose of this study is to investigate the possible solutions to improve the reliability and functionality of battery-less devices. This study has two major objectives: (1) implementing periodic checkpointing on WISP5[1][2], and (2) proposing optimized multi-input single-output energy harvesting system. The WISP5 was acquired from the Sensor Systems Laboratory, University of Washington, as a viable RFID energy harvesting system to implement software checkpointing techniques. We performed the periodic checkpointing every 50ms based on the RFID power fluctuation style. Then, we explored a number of possible maximum power point tracking techniques to extract maximum power from harvesters. As a result, we verified that the open circuit voltage control is the most cost effective and efficient technique for both thermoelectric (TEG) and photovoltaic (PV) [12]. Also, we revealed that in low-level input voltages, following the fact that the maximum power extraction can be achieved at half of open circuit voltage does not result in maximum possible efficiency. Therefore, by adjusting the converter input voltage at about 66% of open circuit voltage, we improved power efficiency by about 18% [30].

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CHAPTER I

INTRODUCTION

Rapid advancements in semiconductor manufacturing and integrated circuits have brought ultra-low power microcontrollers into many implantable and wearable embedded systems. The future for wearable devices is promising and exciting because of their numerous applications in different areas, such as health monitoring, smart buildings, and automotive industry. However, as computation speed keeps growing in smaller scale microcontrollers, it leads to more power consumption. Indeed, battery power has been the power source for most of the embedded systems, but it is not a suitable choice for wearable devices because of its size, lifetime, safety and recharging concerns. Therefore, the need for an alternative power source is immediately obvious. One of the possible solutions lies in energy harvesting techniques to scavenge the ambient power and convert it as a viable power source. However, the harvested power has a downside in nature. They are intrinsically sporadic and intermittent. With unpredictable and unstable power supply, the computation cycles will be interrupted very often.

Energy harvesting extracts power from the ambient environment and can be used to deploy long lifetime batteryless devices. Solar [3][4][5][6], wind [3], footfalls [7][8], breathing [7], blood pressure [7], and body heat [9][10] are all promising sources of energy. They have different characteristics of predictability, controllability, and magnitude. For example, outdoor solar energy is a predictable source that can generate a large magnitude of power at a power density of 10mW/cm2.

For ultra-low power devices, the sources of low power densities, such as micro-solar, breathing (0.42W), and body heat (2.4~4.8W), are able to provide sufficient power to drive the devices at low-duty cycles [9][10][11][5]. Even though the power harvested is lower than the power required by the complete system, it is still possible to operate the system with proper energy management [9]. The most favorable microscale energy harvesting sources scavenge ambient indoor energy from temperature differentials, vibration, and light. Although radio frequency (RF) energy source is another interesting option, its available power compared to the last three sources is low.

Energy Source	Harvested Power
Vibration/Motion	
Human	4 μW/cm^2
Industry	100 μW/cm^2
Temperature Difference	
Human	25 μW/cm^2
Industry	1–10 mW/cm^2
Light	
Indoor	10 μW/cm^2
Outdoor	10 mW/cm^2
RF	
GSM	0.1 μW/cm^2
WiFi	0.001 μW/cm^2

Figure 1. Impedance adjustment technique in boost converter [9]

All the existing works target the energy source characterizations, energy model constructions, and the wearable system implementations ([12][13]). However, only a few of them considered the case that the program execution can be frequently terminated due to the **instability** of harvested energy [4]. With traditional CMOS-based technology, the program execution state is lost, if the power is off. Every time a program is terminated, the execution has to start from the beginning the next time the power is on. It not only is a waste of energy but also severely degrades performance. What is worse, a relatively large program might never finish since the intermediate results are not saved. In order to resolve this issue, NonVolatile Processor (NVP) has been

introduced which are invulnerable to power outage. In fact, the NVP can save any current state and resume execution after enough power becomes available again.

Non-volatile Processors

Non-volatile processors employ NV memories, such as flash memory, that can sustain the data even when the power if off. Other researchers have previously developed the NV memory based on-chip and off-chip memory solutions for energy-harvesting devices to store the execution state. Checkpointing has been shown to be an efficient methodology for saving the runtime state. These systems deploy flash memory to back up the processor state at the checkpoint. However, flash memory has a limited write endurance in the order of 10^5 and access to flash memory is quite slow. Therefore, the time and energy overhead are large. Instead of checkpointing the execution state into flash memory at a low speed, ferroelectric non-volatile register based processors present great potential to be deployed in energy-harvesting devices. They show many desirable characteristics of energy-harvesting systems, such as no battery and zero standby power. The access efficiency of FRAM can even catch up with that of SRAM, and it has superior endurance as long as 10^{14} write cycles.

In general, Non-volatile processor is involved in SW/HW based solutions to become immune and reliable in power failure situations. Hardware-based solutions investigate optimized hardware level checkpointing implementation despite software-based approaches which deploy several programming techniques to backup/restore current state.

In this thesis, we implemented/ported the checkpointing for WISP version 5. WISP5 is equipped with MSP430FR5969, 16 MHz Ultra-low-power microcontroller including 64 KB FRAM, 2 KB SRAM. MSP430FRxxxx models feature non-volatile FRAM memory which makes checkpointing possible.

The power supply for Wireless Identification and Sensing Platform (WISP) is harvested from RFID. However, since RFID is not easily accessible, we still need to investigate other energy sources. Thus, we need to look into other sources, such as photovoltaic, thermoelectric and piezoelectric, which are the most favorable indoor energy sources ([14]).

Because of sporadic and intermittent characteristics of energy harvesting sources, employing just a single energy source might not supply sufficient power for computationally intensive tasks which result in excessive checkpointing overhead. Therefore, in this study, I also looked into the multi-source energy harvesters to increase stability and reliability in wearable devices.

Multi-source Energy Harvesters

Energy harvesting extracts power from an unlimited energy source in nature and can be deployed in batteryless devices. In wearable devices, Photovoltaic (PV), Thermoelectric (TEG) and Piezoelectric (PZ) are the most popular indoor energy sources. However, the distinct features and variable characteristics of each energy source raise different challenges due to high dependency to environmental conditions, which include: 1) Wide range of input voltages, from 20 mV to 5 V, 2) wide range of input impedances and 3) end-to-end power efficiency. [14]
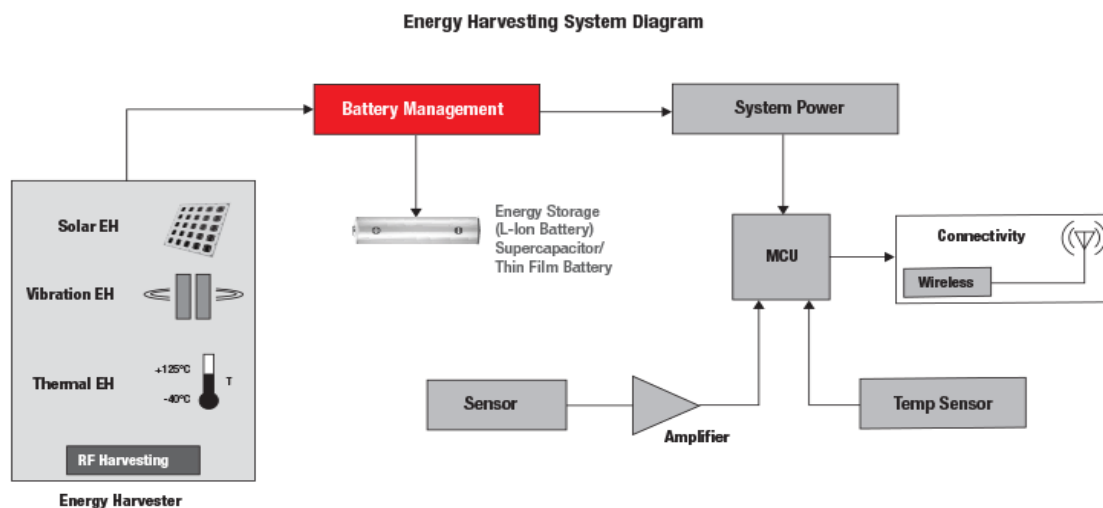
Figure 2. MISO Energy Harvesting System Diagram (Source: Texas Instruments)

The traditional energy harvesting architecture consists of two dc-dc converters. We usually assume that the harvester can be modeled by a dc voltage or current source and a circuit component (e.g. resistance) limiting the extractable power. The first stage is generally designed to scavenge the maximum extractable power and the second stage is deployed to regulate the output voltage.

By combining multiple indoor energy sources (e.g., PV, TEG, and PZ) to compensate for the limitation of a single-energy source and increase the overall power conversion efficiency, we are

able to realize a relatively stable and sufficient power source that supplies reasonably enough energy to power the nonvolatile processor.

In this thesis, we also collected power traces from PV and TEG and analyzed the obtained power traces. Consequently, we proposed a multi-input single-output energy harvesting system which particularly increase TEG harvester power efficiency by about 18%.

In sum, the **contributions** of this thesis include:

- Implementing the WISP5 periodic checkpointing
- Collecting and studying PV and TEG power traces sources
    - Verifying simple MPPT method functionality based on open circuit voltage for PV
    - Proposing an optimized MPPT algorithm for TEG.

In this thesis, Chapter II discusses RFID harvester and checkpointing implementation on WISP5. Chapter III looks into energy harvesting basics and several impedance matching techniques. Chapter IV explains the experimental results. Finally, Chapter V concludes this thesis.

CHAPTER II

RFID HARVESTER

In this section, I first explain how I set up the RFID workstation including WISP, RFID reader, and antenna. Next, some information regarding the different checkpointing techniques, such as unified memory space and periodic checkpointing, is provided. Finally, I present how I implemented the periodic checkpointing in WISP.

In this study, we acquired WISP (Wireless Identification and Sensing Platform) [1] to be used as the starting point of the proposed task. Developed by Intel Research Seattle in cooperation with the University of Washington, WISP is an open source, fully hackable, battery-free platform for experimentation with low power sensing, computation, and communication. It has a similar size to a quarter coin. It has the capabilities of RFID tags, but also supports sensing and computing. WISPs are powered by harvested energy from off-the-shelf UHF RFID readers. To an RFID reader, a WISP is just a normal EPC tag, but inside the WISP, the harvested energy is operating a 16-bit general purpose microcontroller. The microcontroller can perform a variety of computing tasks, including sampling sensors and reporting that sensor data back to the RFID reader. WISPs have been built with light sensors, temperature sensors, 3D-accelerometers, and strain gauges. They have a storage capacitor to sense without RFID reader. What is more important, WISPs have the extensible hardware to add new sensors, and industry standard development tools are also provided. WISP is a good starting point. However, it is still not eligible to be used for health monitoring devices due to several reasons. First, it can only harvest energy from the RFID reader and lacks other energy harvesting sources. Second, it also lacks the health care related sensors, such as electrocardiogram (ECG) and heart rate sensor. Third, the microcontroller is volatile and

can only execute a small program due to the fact that the microcontroller will be shut off every time the harvested energy is used up and intermediate results cannot be saved.

Figure 3. WISP 5

The primary objective of this part of the current study is providing comprehensive firmware capable of backing up current state in unstable power conditions. The energy harvesting device (WISP) obtains its required energy to operate from the RFID reader, and consists of a low-power MCU (MSP430FR5969) and a built-in FRAM, thereby making the study objective feasible. Therefore, the problem can be defined as a way to save the current state in the best time with the lowest possible energy consumption; however, the first approach which comes to mind for saving states is using unified FRAM memory space. Basically, the SRAM space which includes all the computation registers, I/O registers and stack can be mapped to the FRAM instead of the SRAM in the first place. However, the simplest approach is not always the best one. The unified memory space has two major problems. First, the FRAM write speed falls behind the SRAM speed in higher than 8 MHz frequencies which results in more power consumption and slower computation cycles. Second, the FRAM write instructions usually consume about 2 times more power than the SRAM write instructions. Therefore, the unified memory space could not be the most beneficial solution in wearable devices. Figure 4 provides different active mode supply currents obtained from the MSP430FR5969 online datasheet.

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PARAMETER	EXECUTION MEMORY	V_{CC}	FREQUENCY ($f_{MCLK} = f_{SMCLK}$)										UNIT
			1 MHz 0 wait states (NWAITSx = 0)		4 MHz 0 wait states (NWAITSx = 0)		8 MHz 0 wait states (NWAITSx = 0)		12 MHz 1 wait states (NWAITSx = 1)		16 MHz 1 wait states (NWAITSx = 1)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, FRAM\_UNI}$ (Unified memory)	FRAM	3.0 V	210		640		1220		1475		1845		µA
$I_{AM, FRAM}$(0%)	FRAM 0% cache hit ratio	3.0 V	370		1280		2510		2080		2650		µA
$I_{AM, FRAM}$(50%)	FRAM 50% cache hit ratio	3.0 V	240		745		1440		1575		1990		µA
$I_{AM, FRAM}$(66%)	FRAM 66% cache hit ratio	3.0 V	200		560		1070		1300		1620		µA
$I_{AM, FRAM}$(75%)	FRAM 75% cache hit ratio	3.0 V	170	255	480		890	1085	1155	1310	1420	1620	µA
$I_{AM, FRAM}$(100%	FRAM 100% cache hit ratio	3.0 V	110		235		420		640		730		µA
$I_{AM, RAM}$	RAM	3.0 V	130		320		585		890		1070		µA
$I_{AM, RAM only}$	RAM	3.0 V	100	180	290		555		860		1040	1300	µA

Figure 4. Power Consumption in different FRAM/SRAM combination

Because of the intermittent and erratic behavior of the RFID energy source, tracking the incoming RFID signals to mark the checkpointing spot in run-time isn't possible. Moreover, based on the RFID transmission protocol, zero signals can be caused by the QR request or any other request from RFID which starts with a delimiter (series of zeros) to specify the upcoming data stream that should be compiled and responded. Thus, this observation leads us to come up with the periodically backup cycles that can be programmed in a way to do their tasks in idle time or in a fixed number of cycles. Since registers are not the only values which are required for a safe shutdown and then coming back to the very last condition, all the required information and data in RAM will be marked and backed up in a smart manner. Thus, another potential research objective can be optimizing power consumption in the backup stage by decreasing the CPU cycles and required information for a safe shutdown.

Given the constraints of the RFID-scale devices, which are strongly environment-dependent, this study aims at addressing checkpointing methodology and multi-input energy harvester simultaneously.

Firstly, this study tackled a need for a general-purpose power failure recovery technique. Basically, I followed viable "Mementos" techniques [2], implemented on WISP4.1, which is equipped with a flash memory and then implemented on WISP5. This method adheres to two basic rules:

Rule 1: Compatible with Existing Hardware; There is no need for circuitry modification in order to perform the failure prediction, checkpointing and recovery functions.

Rule 2: Energy Estimation at Compile-time and Run-time; predictions based on power traces and limited sample programs at compile time in the previous works showed that such predictions are unreliable ([2]). The Mementos method estimates available energy at run-time. However, this method utilizes different microcontrollers with flash memory, which necessitates users to modify the original code to work with the newer WISP version with FRAM memory. Previous works on the WISP have shown that power failure experience for about every 100 ms is reasonable ([2]). However, placing a precise and safe location to checkpoint is not practical due to the sporadic behavior of the RFID harvester and may lead to incomplete checkpointing. Under such conditions, dealing with long-running and computationally intensive codes is impossible, since the task will be restarted from the beginning after each power failure.

Voltage measurement instrumentation is common in most computing devices with finite energy sources (e.g., batteries and energy harvesting systems). Therefore, we can exploit this circuitry to define an energy-aware state checkpointing. To this goal, we can put different energy-check instructions through the entire main program which estimates the available power by comparing the current voltage to the threshold voltage. Then, we are able to decide whether we should go to the checkpointing stage. However, in this thesis, in order to simplify the checkpointing procedure and decreasing the overhead, the checkpointing function was called every 50 ms. On the other hand, Voltage Supervisors components were not usable in the current study due to stack size

variability. It means that we need a variable threshold voltage which is defined and initialized based on power trace and length of the code.

At the checkpointing stage, all the registers and global variables on stack were pushed and the whole stack, which is located on SRAM to FRAM, was saved. In order to recover the very last successful checkpoint, I saved the whole checkpointing package size as a header and a magic number as a footer, so the beginning address plus the checkpointing data size needed to be equal to the magic number address in FRAM.

At the same time, I was working on optimizing the energy harvester circuitry due to energy limitation and voltage fluctuations in the RFID-based devices. In order to solve power restrictions, we can add piezoelectric and photovoltaic harvesters and use a separate converter for each source. Then, we can stack an individual storage capacitor or use a shared converter (sharing Inductor/ sharing Capacitor) and devote different time slots to each input based on power traces. Converter circuit parameters are highly dependent to energy harvesters DC model. Therefore, our main goal was designing an optimal control circuit which tunes converter components and fulfills sizing limitations.

Checkpointing Procedure in WISP 5 can be summarized into several steps:

1) Memory space modifications:

    a. Reserving memory space for backup

    b. Change microcontroller default settings to not reset the FRAM backup data section on startup.

    c. Changed working frequency to 2MHz (the Lowest possible active frequency)

2) Communication verification: Firstly, we need to download binary code to the WISP with MSP-FET Flash Emulation Tool. In fact, the emulation tool supply required power for WISP. In order to assure that the WISP is within RFID reader signal range. I generated a

random number and send it as RFID tag to RFID reader. The RFID reader can be
monitored with Multileader software via LAN connection. The workstation components
were illustrated in Figure 5
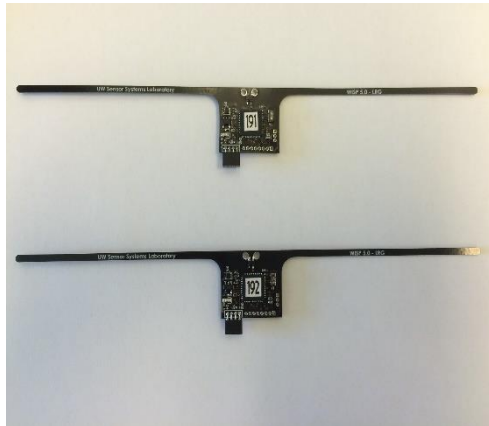
WISP 5.0 Hardware and MSP-FET430UIF programming and debugging tool

Impinj Speedway Revolution R420 UHF
RFID Reader (4 Port)
[The WISP can communicate with commercial-
off-the-shelf RFID readers, and is powered by
the carrier signal emitted by the reader.]

Laird S9028PCR (RHCP) Indoor RFID
Antenna (902-928 MHZ)

Figure 5. WISP Workstation

3) Backup/Restore Program: In order to save the current state, I moved all computation

registers to stack and then moved all stack contents into FRAM. These two tasks were

realized by defining two assembly functions. The restore function is called at the

beginning of the main program. But at the very first run, there is no valid checkpoints, so

the restore function copies all FRAM content to computational register which especially

screws up the program counter content. In order to solve this problem, I saved a magic

number (2 Bytes) which identify the end of successful checkpoint.

4) Define a Periodic Interrupt

I used Port A counter to generate program interrupt every 50ms.

5) Utilizing different MSP430 power modes based on program needs

To do so, I disabled FRAM controller and brought CPU into different power mode, when

the program is in idle time.

PARAMETER	EXECUTION MEMORY	V_{CC}	FREQUENCY ($f_{MCLK} = f_{SMCLK}$)										UNIT
			1 MHz 0 wait states (NWAITSx = 0)		4 MHz 0 wait states (NWAITSx = 0)		8 MHz 0 wait states (NWAITSx = 0)		12 MHz 1 wait states (NWAITSx = 1)		16 MHz 1 wait states (NWAITSx = 1)		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, FRAM\_UNI}$ (Unified memory)	FRAM	3.0 V	210		640		1220		1475		1845		µA
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$I_{AM, FRAM}$(50%)	FRAM 50% cache hit ratio	3.0 V	240		745		1440		1575		1990		µA
$I_{AM, FRAM}$(66%)	FRAM 66% cache hit ratio	3.0 V	200		560		1070		1300		1620		µA
$I_{AM, FRAM}$(75%)	FRAM 75% cache hit ratio	3.0 V	170	255	480		890	1085	1155	1310	1420	1620	µA
$I_{AM, FRAM}$(100%)	FRAM 100% cache hit ratio	3.0 V	110		235		420		640		730		µA
$I_{AM, RAM}$	RAM	3.0 V	130		320		585		890		1070		µA
$I_{AM, RAM only}$	RAM	3.0 V	100	180	290		555		860		1040	1300	µA

Figure 6. MSP430 Operating Modes

Register checkpointing is explained in the next page.

// push all the registers onto the stack (the saved PC in FRAM is the return address to the main

program):

```
asm volatile ("PUSH 2(R1)\n\t" // PC will appear at 28(R1)
        "PUSH R1\n\t"    // SP will appear at 26(R1)
        "ADD #6, 0(R1)\n\t" // to account for 2xPC + R1 itself
        "PUSH R2\n\t"    // R2  will appear at 24(R1)
      //"PUSH R3\n\t" // skip R3
        "PUSH R4\n\t"    // R4  will appear at 22(R1)
        "PUSH R5\n\t"    // R5  will appear at 20(R1)
        "PUSH R6\n\t"    // R6  will appear at 18(R1)
        "PUSH R7\n\t"    // R7  will appear at 16(R1)
        "PUSH R8\n\t"    // R8  will appear at 14(R1)
        "PUSH R9\n\t"    // R9  will appear at 12(R1)
        "PUSH R10\n\t"   // R10 will appear at 10(R1)
        "PUSH R11\n\t"   // R11 will appear at 8(R1)
        "PUSH R12\n\t"   // R12 will appear at 6(R1)
        "PUSH R13\n\t"   // R13 will appear at 4(R1)
        "PUSH R14\n\t"   // R14 will appear at 2(R1)
        "PUSH R15");     // R15 will appear at 0(R1)
```

// the baseaddr is the beginning address in FRAM for checkpointing, so the rest of the stack will

be saved after this part of the checkpointing procedure:

```
asm volatile ("MOV &%0, R14" ::"m"(baseaddr));
asm volatile ("POP 30(R14)\n\t" // R15
        "POP 28(R14)\n\t" // R14
        "POP 26(R14)\n\t" // R13
        "POP 24(R14)\n\t" // R12
        "POP 22(R14)\n\t" // R11
        "POP 20(R14)\n\t" // R10
        "POP 18(R14)\n\t" // R9
        "POP 16(R14)\n\t" // R8
        "POP 14(R14)\n\t" // R7
        "POP 12(R14)\n\t" // R6
        "POP 10(R14)\n\t" // R5
        "POP 8(R14)\n\t"  // R4
        // skip R3 (constant generator)
        "POP 6(R14)\n\t"  // R2
        "POP 4(R14)\n\t"  // R1
        "POP 2(R14)");    // R0
```

CHAPTER III

HARVESTER ARCHITECTURE (LITERATURE REVIEW)

In this section, I looked into the three most popular energy harvesters' models. Next, I summarized several related works to impedance matching techniques, multi-input energy harvesters' architecture and converter component selection. Then, I build up the optimized multi-input single-output energy harvesters in next chapter.

Energy Harvesting Basics:

Photovoltaic (PV) Harvesters:

The harvested power from the PV module for a particular light intensity depends on the cell voltage (V_{PV}). Figure 7 shows an equivalent circuit of a photovoltaic harvester. For a single cell PV, the supplied current (I_{PV}) is close to the current source if the cell voltage is absolutely less than diode threshold voltage (e.g., $V_{PV} < 0.2$). Thus, the output power is limited due to low cell voltage. However, for the higher voltages (e.g., $V_{PV} > 0.4$) parallel diode is switched on and drawn the supplied current into the ground which leads to supplied current reduction and limited output power. Therefore, there is an operating point which makes the output power maximum which is specified by V_{MP} and I_{MP} (Maximum Power output voltage and Maximum Power output current, respectively). [14]

Where:

- I_o = Diode Saturation Current
- q = Electron Charge
- k = Boltzmann Constant
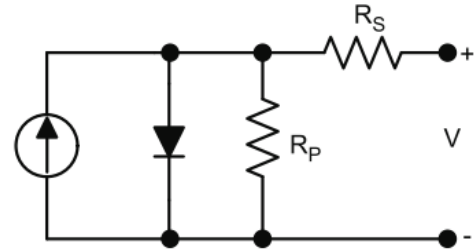- n = Ideality factor (from 1 to 2)
- T = Temperature

Figure 7. Simple PV Model [12]

$$I = I_{pv} - I_0 \times \left(e^{\frac{q \times (V + I \times R_S)}{n \times k \times T}} - 1\right) - \frac{V + I \times R_S}{R_P} \tag{1}$$

The parameters provided in PV datasheets typically (given for 25^C and $1000W/m^2$) are as follows:

Open circuit voltage (V_{OC}), short circuit output current (I_{SC}), V_{MP} and I_{MP}. R_S is the series resistance that is proportional to the reciprocal of irradiance. Figure 8 shows R_S vs 1/irradiance and it can be seen that the resistance range is about few ohms. Also, R_P is parallel leakage current normally greater than 100kΩ. Therefore, this circuit element can be neglected except for low light intensity conditions. [15]
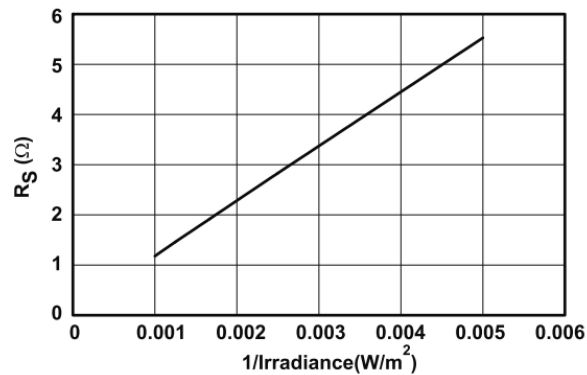
Figure 8. R_s Variation vs Light Intensity [16]

Another effective factor in PV cell output current which is often neglected is the angle of incident. If the angle of incident is not zero compared to the source, the effective irradiance will be reduced, which results in lower output current. Therefore, mobile systems which intrinsically have a continuously variable angle compared to the light source need a maximum power point tracking (MPPT) system with faster tracking speed. [15]

Figure 9. PV Output Current vs Angle of Incident [16]

Thermoelectric Harvester:

Thermoelectric (TEG) harvesters scavenge electrical power from surrounding heat energy sources. Figure *10* shows the thermoelectric harvester model which consists of a voltage source controlled by S (Seebeck coefficient of the material) and ΔT (temperature differential). The electrical resistance R_T controls the maximum extractable power from harvesters and its value is constant. Therefore, theoretically, the maximum power extraction can be achieved by setting the output voltage at half of the open circuit voltage, which means adjusting the input impedance equal to harvester's internal impedance.
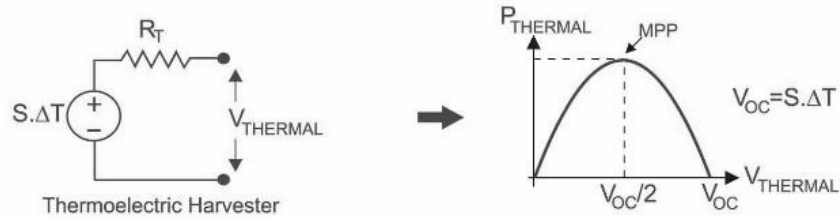
Figure 10. Simple Thermoelectric Harvester Model [10]

Piezoelectric Harvester:

The viable energy source for wearable devices which is subjected to movement and vibration is piezoelectric. Piezoelectric harvester can extract electrical power from mechanical energy generated by pressure, vibrations, or force. According to [14] the ac model of the harvester connected to the rectifier can be simplified to a dc voltage source along with a resistor:
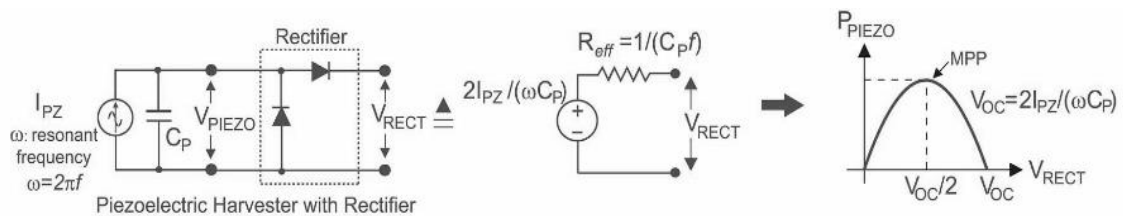

Figure 11. Piezoelectric Equivalent DC Model

Maximum Power Extraction:

Because of the intrinsic harvesting energy source characteristics, such as producing highly inconsistent and unstable output, the harvesting module could not be connected directly to the load. As mentioned before, the first stage connected to the harvested module is to draw out the maximum available power. In fact, a number of reasons led designers to utilize the switched inductive converters operating in discontinuous mode (DCM) rather than switch capacitors. Particularly, the charging of capacitors is an intrinsically lossy process, which becomes even worse in high output/input voltage ratios, due to power dissipation in capacitor internal resistance.

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The next reason which makes switched inductor converters superior is that their better performance with low-input current and voltage.

The maximum power transfer theorem states that the maximum extractable power for harvesters with linear model is achievable if circuit's input impedance connected to the harvester is the same as harvester internal impedance. In order to exploit the maximum extractable power, the first converter should be tuned dynamically to present the optimal input impedance.

The Maximum Power Point Tracking (MPPT) aims at automatically finding the unique operating point in which the maximum available PV power can be extracted from the harvester. Many MPPT methods have been proposed to maximize the generated power which vary in complexity, tracking speed, sizing, cost, and efficiency. Figure 12 shows a comparison among the most well-known MPPT techniques focused on efficiency vs hardware and computational cost presented in [16]:
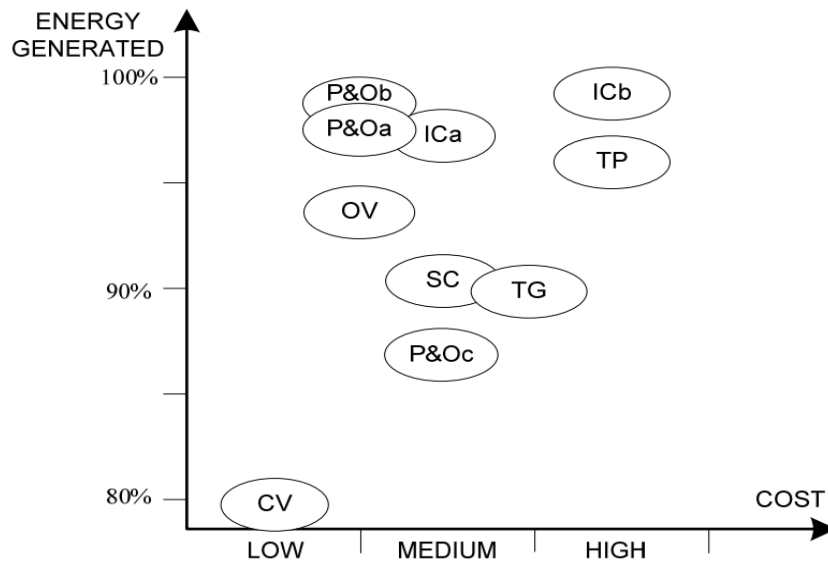

Figure 12. Different MPPT Algorithm Comparison. Generated Power vs HW/SW Cost

Next, I reviewed several impedance matching techniques to extract the maximum available power.

Impedance Matching Technique:

Converter's Input Impedance:

Considering a switched-inductor boost converter, the converter input impedance interfacing with the harvester can be formulated as converter input voltage over the average current. Figure 13 presents the impedance adjustment based on average current manipulation.
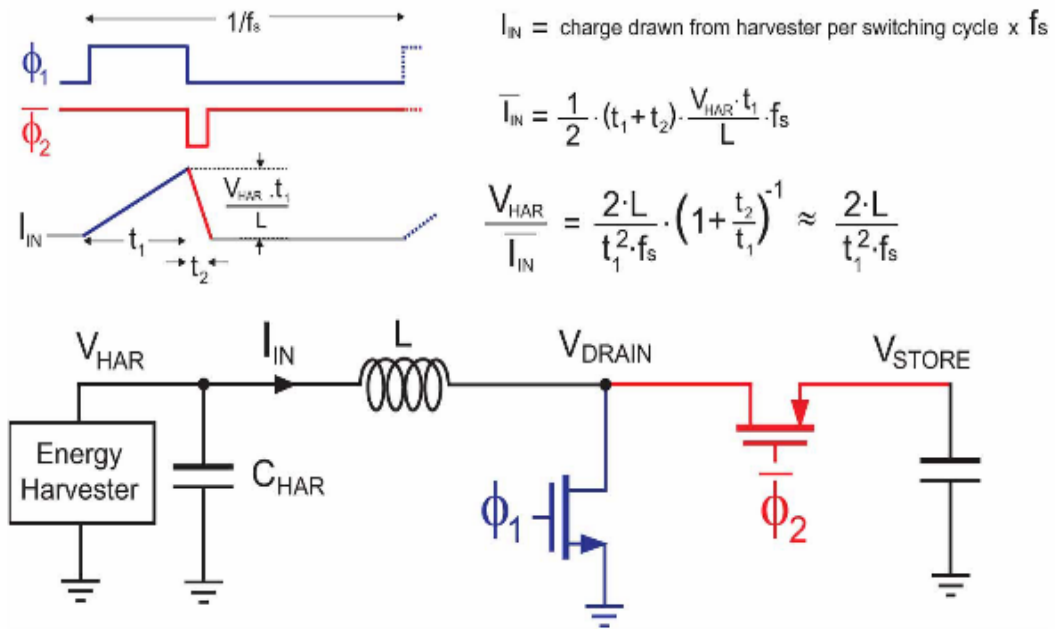

Figure 13.Impedance Adjustment Technique in Boost Converter [10]

The average current fed into the switching converter can be calculated as follow;

$$\bar{I}_{IN} = \frac{V_{HAR} \cdot t_1 \cdot (t_1 + t_2) \cdot f_s}{2 \cdot L} \qquad (2)$$

Where t_1, is the time duration of the switching phase φ_1, t_2, is the time duration of switching phase φ_2, L is the inductance value, and fs is the switching frequency. The input impedance of the converter can be measured as a result of the input voltage (V_{HAR}) over the average current (I_{IN}). Thus, the input impedance can be calculated as;

$$\frac{V_{HAR}}{\bar{I}_{IN}} = \frac{2 \cdot L}{t_1^2 \cdot f_s} \cdot (1 + \frac{t_2}{t_1})^{-1} \tag{3}$$

Based on the inductor volt-second rule the time duration of first and second switching cycle keep this relationship:

$$t_2 = \frac{V_{HAR} \cdot t_1}{V_{STORE} - V_{HAR}} \tag{4}$$

Which actually emphasizes the fact that the inductor current ramps down suddenly due to large ratio output voltage to input voltage $V_{STORE} \gg V_{HAR}$. Therefore, the second switching phase can be neglected in high conversion ratios and the input impedance equation approximated to:

$$\frac{V_{HAR}}{\bar{I}_{IN}} \approx \frac{2 \cdot L}{t_1^2 \cdot f_s} \tag{5}$$

Although at the most extreme case in which the output/input voltage difference becomes smaller, this approximation could result in less efficient power transfer schemes.

Basically, there are three controlling factors to adjust converter's input impedance which are duty cycle, switching frequency, and inductance value. To satisfy the sizing concerns, the inductance value should be kept as small as possible.

In the following section, four different approaches which distinctly attacked impedance matching problems are reviewed.

Pulse Counting Control:

Shi et al. [12] proposed the pulse counting approach. The thought behind the proposed idea indicates that an exact match to the target TEG resistance value can be significantly relaxed for a certain error tolerance. Therefore, an open loop method with approximate matching may be efficient in realizing near-maximum power extraction. Precise analog tuning or microcontroller-based tracking approaches are not required to configure TEG input impedance to be exactly the same as internal impedance. This reduces the system complexity and the control overhead. Hence, the input impedance of the interface circuit can be controlled by adjusting the duty cycle of the connected switches to the harvester. However, large differences between input and output voltage lead to long idle time, and also power stage switching results in extra power loss. Furthermore, this method can be applied to multi-input harvesting systems with harvesters with variable internal impedance (e.g. Photovoltaic). Figure *14* shows that 95% of the maximum extractable power in TEG harvesters can be exploited even with a large difference between converter input impedance and harvester internal impedance.
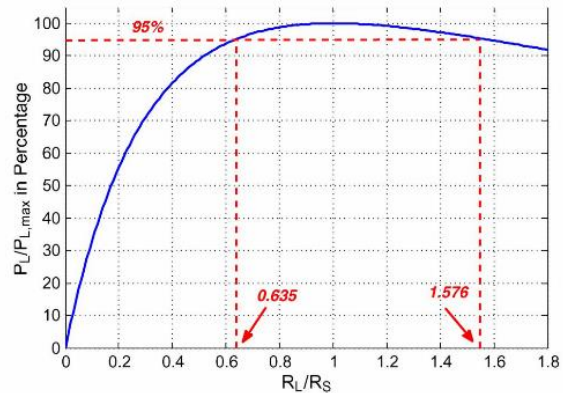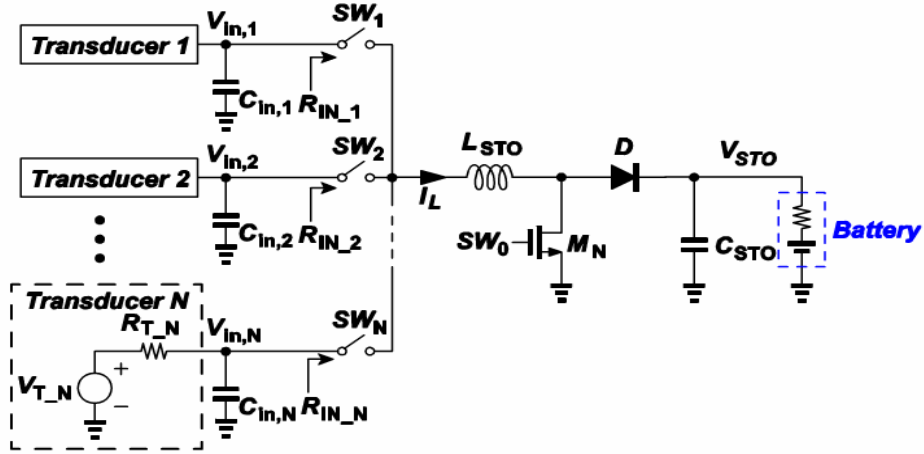

Figure 14. Impedance Matching Flexibility

Figure 15. Pulse Counting Control Scheme [2]

Assuming that the fixed duty-cycle for SW_0 is used, the corresponding input impedance for the ith input harvester can be found as:

$$R_{IN\_i} = \frac{8 \cdot L_{STO}}{\left(\dfrac{N_{PHi} \cdot T_s}{N_{Total}}\right)} = (8 \cdot L_{STO}) \cdot f_{SWi} = R_{T\_i} \tag{6}$$
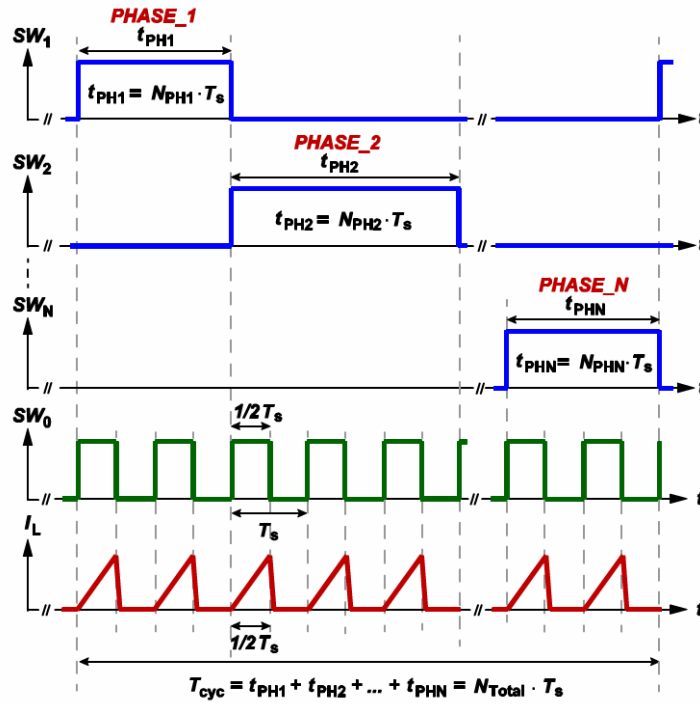

Figure 16. Impedance Matching Technique based on Pulse Counting Control [12]

Effective Switching Frequency:

Bandyopadhyay and Chandarkasan [14] proposed a novel hybrid energy harvester which consists of an auto-adjustable multi-input converter that collects harvested power from three different sources. Table 1 shows different harvester characteristics used in the article:

Harvester Type Parameters	Thermal	Solar	Vibration
Material, Size, Conditions	BiTe, 50cm² ΔT~2-5K	Si (1-2 series) 500-2000lux	PZT (1-2 parallel) >1g
Harvester Voltage (open ckt)*	50-300mV	200-900mV	3-10V
Impedance to be presented for optimal power transfer	5-10Ω	0.05-2kΩ	10-150kΩ
Maximum Power Extraction	one time setting	tracking	one time setting

Table 1. TEG, PV, and PZ Energy Harvester Characteristics

The researchers used sharing inductor converter topology which resulted in reduced circuit complexity and sizing. Then, they tried to attack the maximum power extraction problem with an enhanced MPPT approach. Moreover, they exploited different switching cycle durations in order to manipulate average current fed into the converter circuit to adjust the input resistance equal to the energy harvester resistance which brought maximum possible power from source into the load. Thus, the authors defined switching matrix in a way that devoted different time slots to change the average current and adapt the converter input resistance. In the proposed architecture, the excess energy exploited from harvester was stored in backup capacitor through the secondary converter. The one-stage architecture combined different harvester and simplified two-stage traditional harvester to one stage. However, a complex photovoltaic MPPT approach, extra capacitor and switches, high switching frequency and resistive sensing imposed on the circuit, may result in more power loss in microcontroller and converter circuitry.
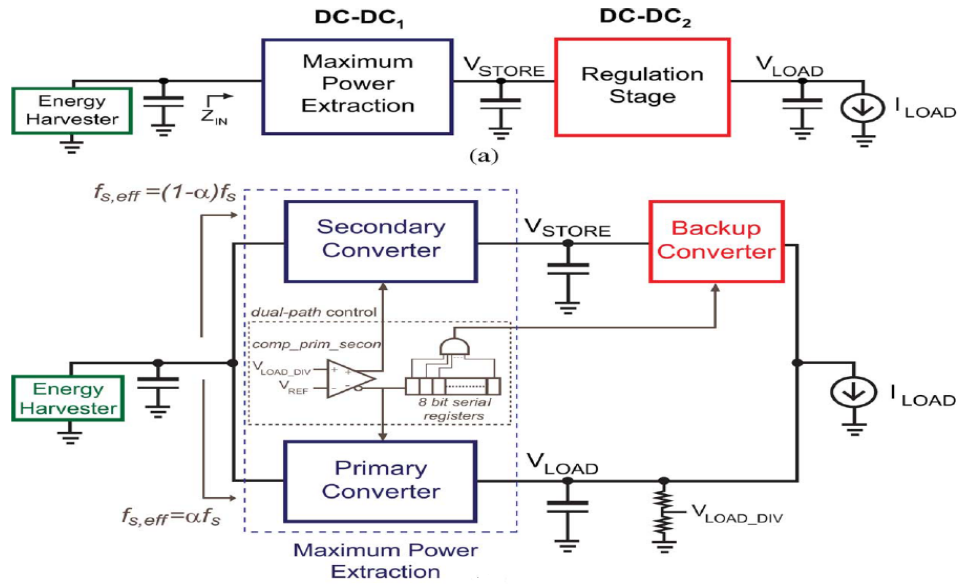
Figure 17. Traditional Two-stage Converter vs Proposed Dual-path Converter [10]
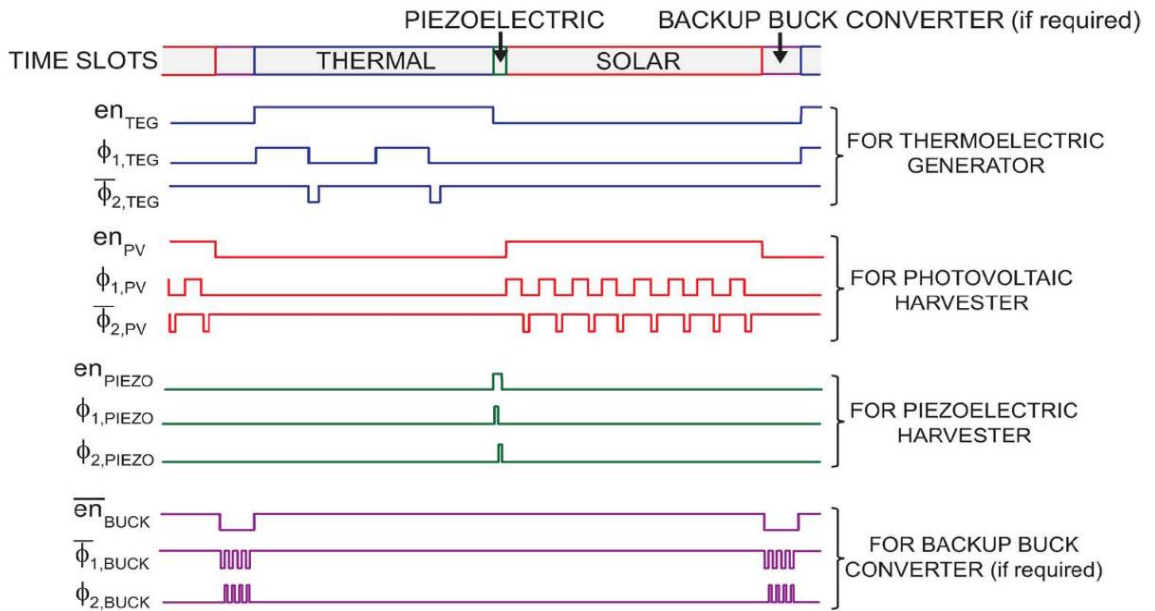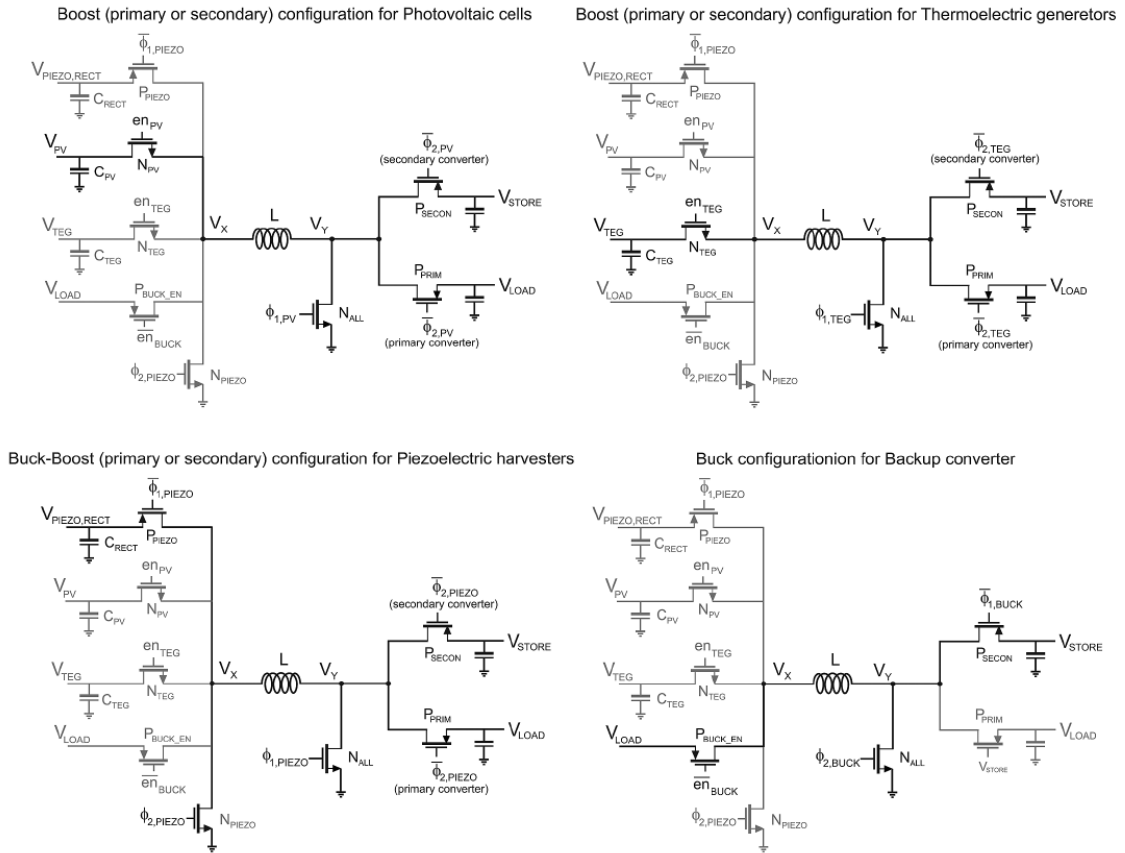

Figure 18. Time and Frequency Allocation to Different Harvesters [10]

In Figure 19, the authors illustrated different switch matrix states and their corresponding configuration:

Figure 19. Reconfigurable Switch Matrix and its Corresponding Converter Configuration [10]

Duty-Cycle-Based Impedance Matching:

In [13], the authors tried to keep the switching frequency constant and tune the input impedance by changing the duty cycle. In this paper, the researchers proposed a combined harvesting/regulating architecture which used sharing inductor scheme in both stages.
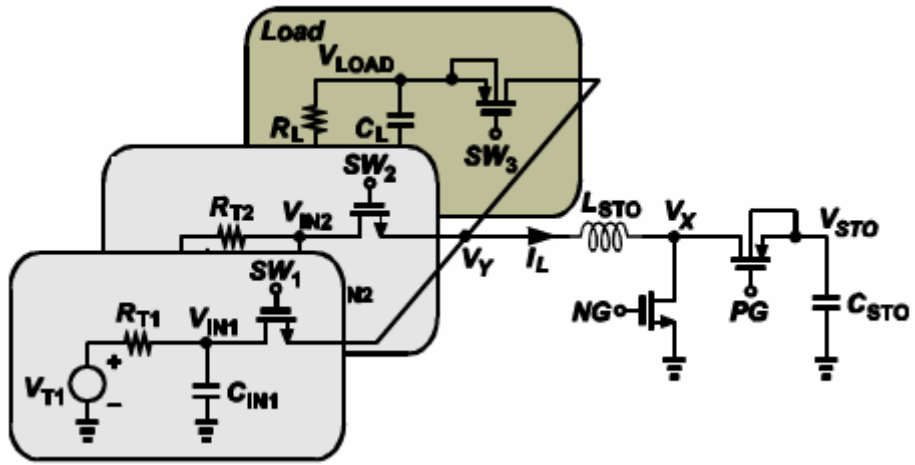
26

Figure 20. Combined Harvesting/Regulating Architecture [12]

In fact, the inductor current ramps down so quickly due to high output/input voltage difference. Thus, the inductor idle time was used to regulate the output voltage.

It can be understood that the proposed multi-input single-output power converter utilized the idle time, but the regulation stage frequency operation is constrained due to limited time and fixed frequency.
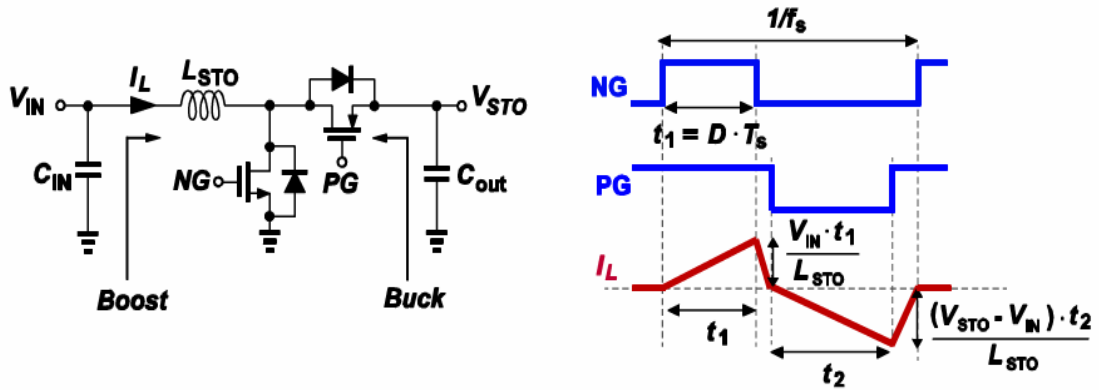

Figure 21. Utilizing inductor idle time with sharing inductor in Harvesting and Regulating Mode

Reconfigurable TEGs connections:

Zarate-Roldan et. Al. [17][18] delved into TEG low input voltage and impedance matching. The authors proposed multi-array TEG harvester with the reconfigurable connection. The proposed idea was aimed at keeping the internal harvester impedance at a reasonable range and simultaneously increase the input voltage with connecting a number of TEG harvesters in series.
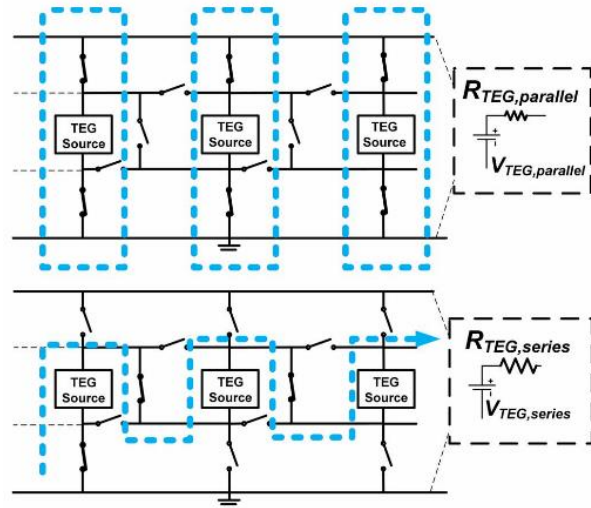

Figure 22. Multi-TEG Reconfigurable Connection Array

Based on the empirical results in [17], the 3*3 TEG array internal impedance in different connection setting could vary from 1.53 kΩ to 19Ω and input voltage altered from 50 mV to 200 mV.

This approach can be used to compensate for low input voltage impact on converter efficiency; however, the multi-array harvester can result in larger circuitry which fails to meet the sizing criteria. Moreover, the connection reconfiguration never has been explained, since it needs a microcontroller which adds more power loss and control circuitry to energy harvesting systems. In this paper, the authors tried to solve the impedance matching issue by keeping the duty cycle fixed at 50% and adjusting the switching frequency. They also illustrated the switching frequency vs inductance value to determine the possible coverable impedance range with the selected settings and component values.

Figure 23. Possible Impedance Range based on Switching Frequency & Inductor Values
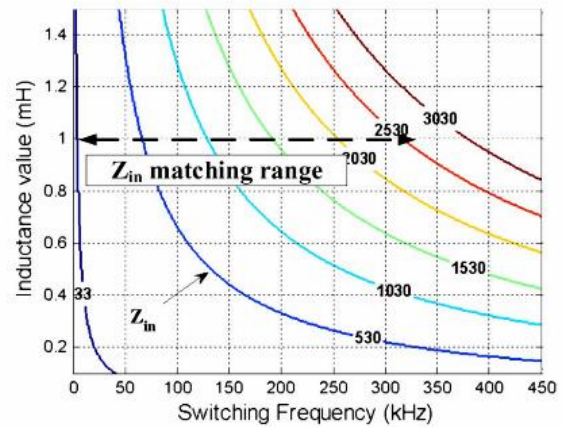
The inductor-switched converter consists of different components such as an inductor, capacitor, and a couple of switches. In order to maximize the converter's efficiency, these components should be chosen sensibly. In the following section, I elaborate on converter optimization based on different component selections and operating switching frequencies.

Converter optimization:

Almost all advanced digital systems are composed of separate components and peripherals with different operating voltage. Hence, the power supply needs to provide different regulated voltage levels.[19]

Figure 24. Different Required Voltage Levels for Embedded Devices
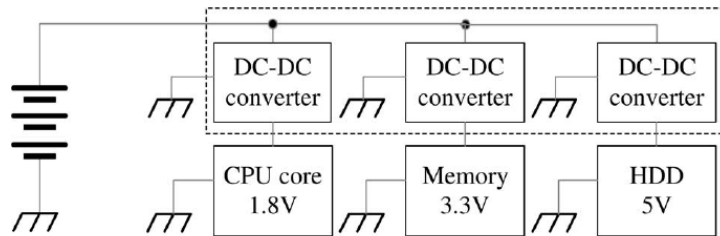
Basically, there are two ways to regulate the output voltage. The first is linear voltage regulator (used in[14]) which suffers from inevitable power dissipation. Second, the switching regulator which is more efficient and can be used in low-power situations. However, the linear regulators are much cheaper and produce less noise.

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Power management units with an associated dynamic voltage scaling (DVS) scheme, which constantly change the supply voltage, are usually employed in modern embedded systems. In fact, there is always a significant power loss in the converter stage. Therefore, in order to supply the variable input voltage, the regulation output voltage needs to be scheduled to minimize the overall power efficiency.

Generally, the converter power loss is caused by three main factors:

$$P_{dc-dc} = P_{Conduction} + P_{MOSFET} + P_{Controller} \tag{7}$$

1) Conduction power dissipation:

All the electrical components used in converter circuitry are non-ideal and have their own internal resistance (e.g., capacitor, inductor, switches). This results in power loss in corresponding resistors. Based on [19] conduction power dissipation in PWM dc-dc converter mainly depends on the output voltage, (output/input voltage ratio) and the output current.

$$P_{conduction} = I_O^2 \cdot (D \cdot R_{SW1} + (1 - D) \cdot R_{SW2} + R_L)$$
$$+ \frac{1}{3} \cdot \left(\frac{\Delta I_L}{2}\right)^2 \cdot (D \cdot R_{SW1} + (1 - D) \cdot R_{SW2} + R_L + R_C) \tag{8}$$

$$\Delta I_L = \frac{V_O \cdot (1 - D)}{L \cdot f_s}, \quad D = \frac{V_O}{V_I} \tag{9}$$

2) MOSFET Power Dissipation:

This power loss is mainly caused by the charging up internal switches capacitance which makes the corresponding switch ON. The power dissipated in converter switches is roughly related to the switching frequency, input voltage and MOSFET gate width sizing:

$$P_{MOSFET} = V_I \cdot f_s \cdot (Q_{SW1} + Q_{SW2}) \tag{10}$$

Where Q_{sw1} and Q_{sw2} are the gate charges of the converter switches.

1) Controller power Dissipation:

Power used to run control circuitry is constant and unrelated to operating conditions. In the converter idle time, the controller power dissipation is usually dominated by the other two factors.

The minimization of the dc-dc converter power's consumption can be achieved with two considerations:

- Finding the most efficient task and voltage scheduling to minimize the total energy consumption of the system. Generally, the power and energy consumption for a specific task in a CMOS circuit can be formulated as:

$$P_i = C_{CPU,i} \cdot V_{dd,i}^2 \cdot f_i + V_{dd,i} \cdot I_{static} + P_{on} \tag{11}$$

$$E_i = N_i \cdot P_i \tag{12}$$

Where V_{dd} is the supply voltage, I_{static} is the leakage current, f_i is the operating frequency, N_i the total number of cycles needed for a specific task, and C_{CPUi} is the average switched capacitance.

Basically, circuit delay is relatively proportional to the supply voltage, which implies that the processor's frequency is determined by the supply voltage. After combining the processor energy consumption and the dc-dc converter power consumption, it can be concluded that the total energy consumption is the monotonically increasing function of the dc-dc output voltage, which means the lowest possible voltage does not necessarily result in minimum power consumption.

$E(v)$

Operating range

$E_{tot}(v)$
$E_{CPU}(v)$

$$\left. \frac{dE_{tot}(v)}{dv} \right|_{v=v_{OPT}} = 0$$

v_{OPT} (f_{OPT})

Relative energy consumption

v
(f)

0	1	2	3
(0)	(125)	(250)	(375)

Supply voltage (V)
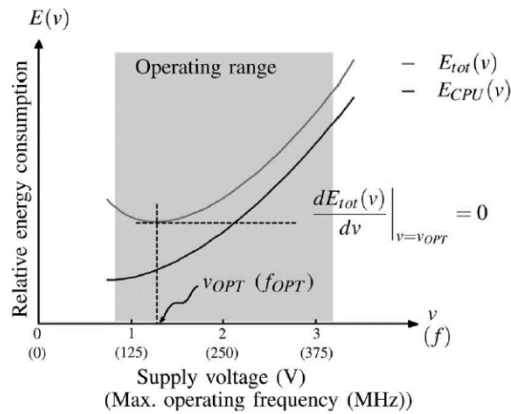(Max. operating frequency (MHz))

Figure 25. Relative Energy Consumption vs Supply Voltage

However, this thesis focused on improving the maximum power extraction stage efficiency, so these minimization techniques are beyond the thesis's scope.

- Converter components optimization: The size (width) of MOSFET switches will also affect the conversion efficiency, i.e., a wide MOSFET switch will increase energy consumption of ON/OFF switching while a narrow MOSFET switch will increase its internal resistance. Figure 26 shows total consumption vs supply voltage with different switch sizing. Based on the empirical results in [20], the PV output power can be improved by 15% in an optimized architecture.
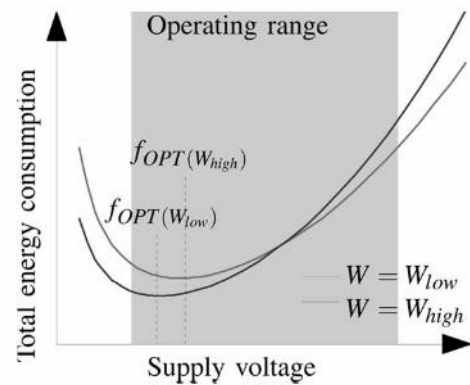
Figure 26. Relative Energy Consumption vs MOSFET Gate Sizing

Operating range

Total energy consumption

$f_{OPT(W_{high})}$

$f_{OPT(W_{low})}$

$W = W_{low}$
$W = W_{high}$

Supply voltage

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Converter Component sizing:

In fact, the converter optimization techniques to find the best operating voltage range for MPPT converter is not applicable, since the duty cycle is adjusted to extract the maximum available power. Furthermore, the input voltage has a wide range of values, and due to its inherent ambient energy characteristics, it is highly fluctuated. Therefore, the output voltage is tractable.

Besides, the power dissipation is not just caused by the operating voltage and switch sizing; the power conduction depends on inductor values, capacitor values, and switching frequency in the converter.

The necessary converter components can be selected based on four main factors [21]: input voltage range, average output voltage, maximum output current and integrated circuit technology used in circuit fabrication. Basically in energy harvesting systems, one of the main concerns is about decreasing the circuit size. It can be reached with inductor value decrease; however, the inductor size is restricted to lower bound. Because the inductor size has a direct impact of the inductor current variation, the higher inductor value decreases inductor current ripple and consequently causes an increase in the maximum output current. [21]

$$\Delta I_L = \frac{V_{IN\_min} \times D}{f_s \times L} \tag{13}$$

$$I_{MAX\_OUT} = \left(I_{L\_min} - \frac{\Delta I_L}{2} \right) \times (1 - D) \tag{14}$$

As stated in Equation 11, the conduction power dissipation is proportional to the output current. Based on [21], when the recommended values is not provided, a suitable inductor value can be calculated as follow:

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{\Delta I_L \times f_s \times V_{OUT}} \tag{15}$$

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Which implies that the inductor selection, operating frequency, and duty cycle choices are intertwined factors either of which should be selected with the other factors considerations. Thus, the intuitive approach which keeps the inductor and frequency as low as possible and increases the duty cycle is not possible. Even worse, the duty cycle expansion has an upper bound from which point the saved energy in inductor becomes saturated and power dissipated in internal circuit impedances[22]. Converter power consumption model was simulated in MATLAB. Hence, based on the provided code, the converter components can be optimized for a specific configuration and purpose.

CHAPTER IV

PROPOSED ENERGY HARVESTING SYSTEM

In this thesis, I combined three common indoor energy harvesters which are photovoltaic,

thermoelectric and piezoelectric. The main objective is optimizing the MPPT converter. To do so,

I proposed a control circuitry which continuously adjust the PV and TEG input impedance based

on the open circuit voltage of the corresponding harvesters. Regarding the piezoelectric harvester

model, the converter input impedance can be adjusted during installation by setting the converter

input impedance equal to the piezoelectric internal impedance. Figure 27 shows the optimized
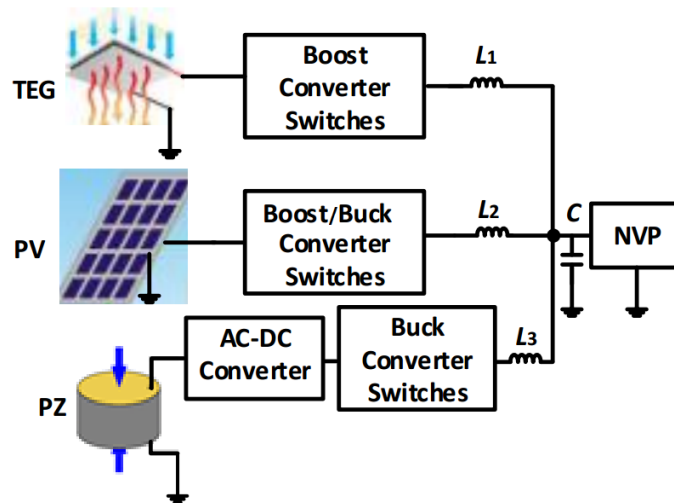
MISO energy harvesting system architecture:

Figure 27. The Proposed MISO Energy Harvesting System

Photovoltaic MPPT algorithm

As shown in Figure 28, we measured different indoor PV power traces under different indoor lights: filament lamps and daylight lamps. TES 1333 was Solar Power Meter [31] was selected to measure their irradiation intensity, which can be translated into power harvesting trace based on our previously extracted PV models [23].
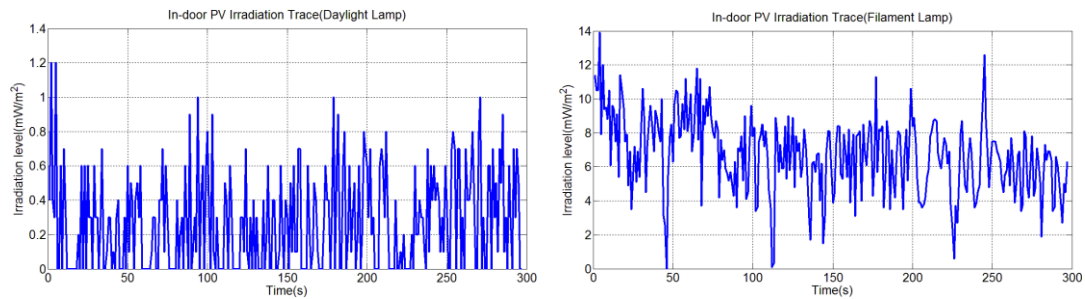

Figure 28.Sampled Power Trace under Filament Lamp & Daylight Lamp

In our experiments, we tuned the DC-DC converter duty ratio such that the PV panel could be tested in different operating voltages starting from $0.6V_{OC}$ to $0.9V_{OC}$, and monitor the output power using our PV module and DC-DC converter simulation setup. In this observation, the obtained PV power traces from filament lamp and daylight lamps were imported into the PV model to achieve the corresponding output voltage and current of the PV module, which can be used to simulate DC-DC converter later. The output power traces of the PV harvesting module regarding different operation voltage levels are shown in Figure 29.
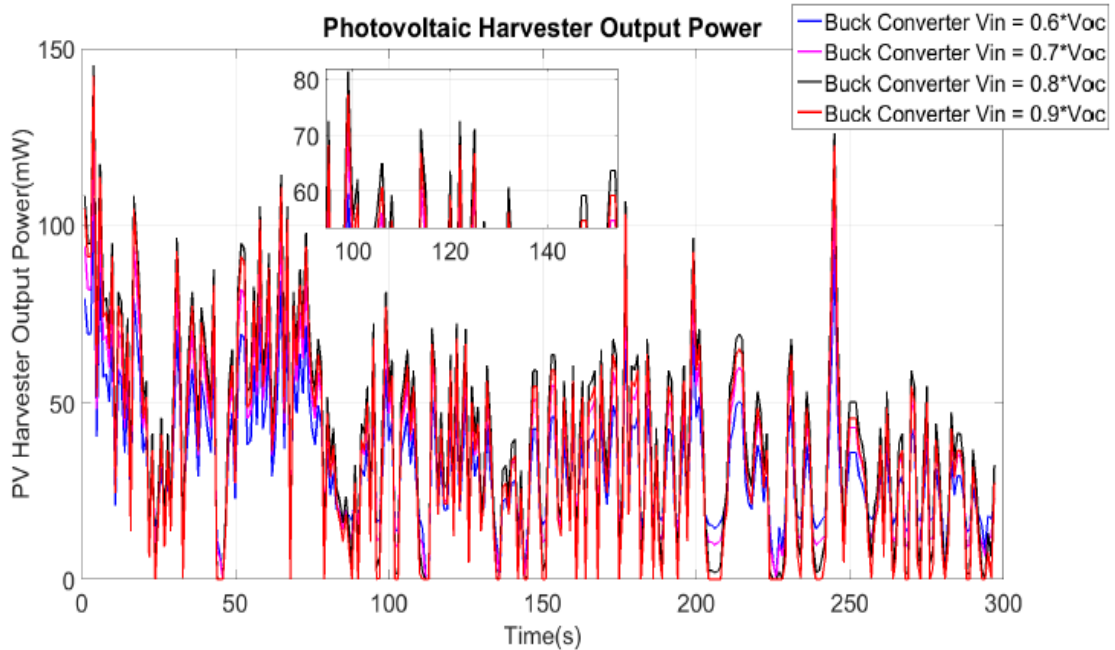
Figure 29. Photovoltaic Harvester Output Power

It can be verified that the maximum power extraction can be attained by setting the converter input voltage to 80% of the open circuit voltage.

In fact, V_{MPP} and V_{OC} in photovoltaic harvester can be estimated as follow:

$$V_{MPP} \approx k \cdot V_{OC} \tag{16}$$

where k is a constant which is determined by the PV array characteristics. The proportional factor k has been stated to be between 0.7 and 0.8 [24] and can be found by testing the PV array in different irradiance and temperature levels and testing the V_{MPP} and V_{OC} relationship. Based on the comparison in Figure 12 [16], the most efficient and simplest MPPT techniques is the open voltage method, since there is no need for a microcontroller to do computation and find the maximum power point. However, the main downside of this technique is the need to measuring the open circuit voltage for a given condition which makes the harvester disconnect

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from the converter momentarily and cause temporary power loss. Also, the techniques are not

completely accurate and is based on the estimation that V_{MPP} is a constant fraction of V_{OC}.

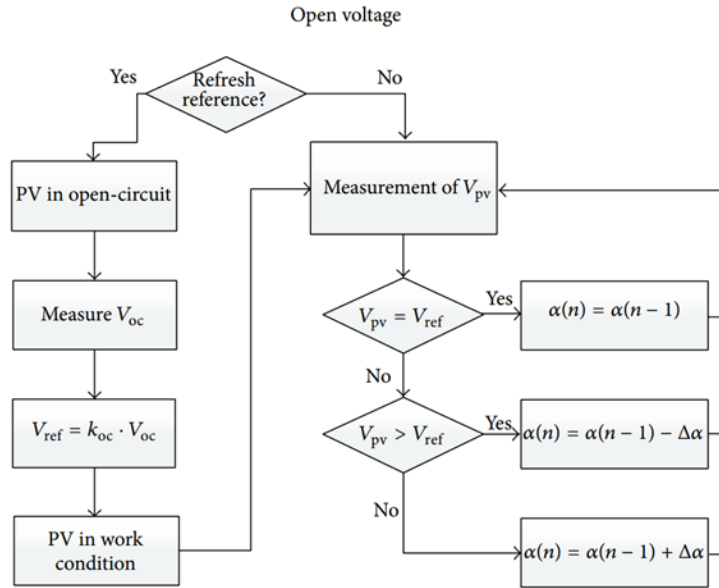The basic principle of the Open Circuit Voltage (OV) can be illustrated as follow;

Figure 30. Open Circuit Voltage MPPT Control flowchart

As can be observed in the corresponding block-diagram, if the solar panel output voltage, V_{PV}, is

higher than the reference value, V_{ref}, then the duty cycle, α, should be decremented, as indicated

in the Boost-converter analysis. Otherwise, if $V_{PV} < V_{ref}$, it will have to be increased to obtain the

opposite effect.

Figure 31 show the sample PV Current/Voltage sensors [25]. Therefore, as mentioned earlier, the two main concerns in wearable devices are sizing and power budget. Thus, deploying the PV voltage sensor is more beneficial due to less complexity and power leakage.
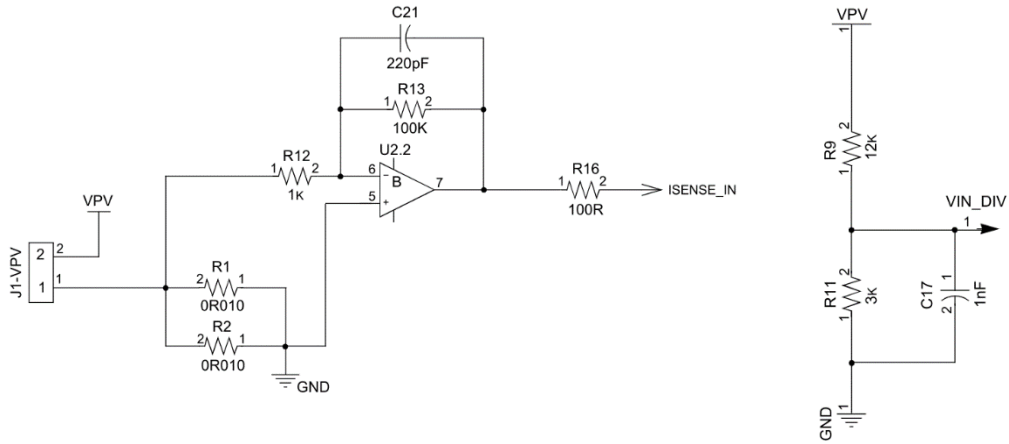

Figure 31. Sample PV Current and Voltage Sensors (left to right)

In this thesis, I simulated the photovoltaic model and converter power consumption in MATLAB. Then, by importing the generated power trace, the photovoltaic output power was estimated. Table 2 illustrates the resultant average output power for the buck converter in PV harvester as a function of different converter input voltages of the converter.

Input Voltage of the Converter	0.6 V_{OC}	0.7 V_{OC}	0.8 V_{OC}	0.9 V_{OC}
Average Output Power (mW)	32.6435	36.6172	40.9483	36.7555

Table 2. Open Circuit MPPT Control Results

The proposed techniques were imposed at maximum 0.05% power deficiency in photovoltaic harvester compared to the complex MPPT tracking method such as perturb and observe (P&O) or Hill Climbing Methods [16][26]. However, it reduced the computation overhead by simplified MPPT algorithm and deducted the constant power consumption of MPPT microcontroller.

TEG MPPT Algorithm

Furthermore, based on [14], [17], the temperature gradient in a wearable device is about 0.23-2.1
^{C} which results in low input voltage. In this situation, the maximum power extraction is not
achievable at half of the open circuit voltage. Therefore, in this thesis, by tracking OC voltage,
the input impedance was tuned based on the temperature gradient.

Figure 32 shows the measured power trace which was produced from Micropelt TE-CORE /RF
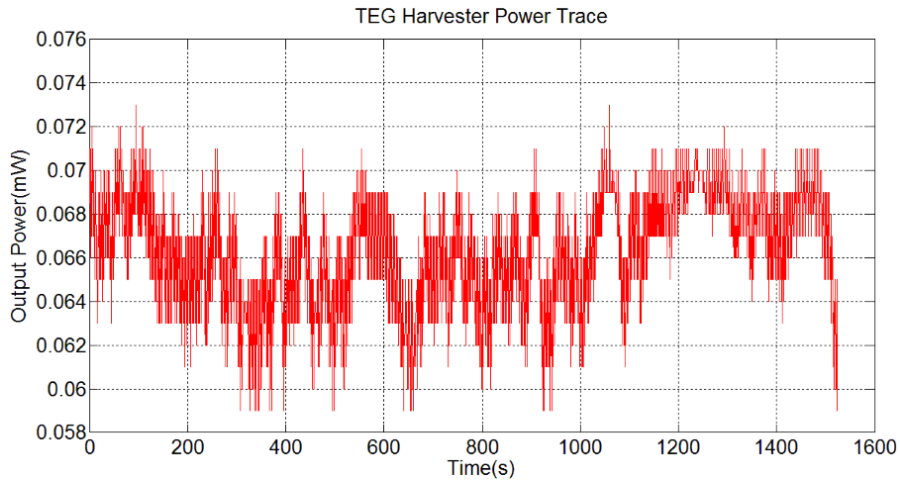(Micropelt TEG evaluation board).

Figure 32. TEG Harvester Power Trace

Assuming that the DC-DC converter configuration regulated the harvester output voltage at a k
percent of the V_{OC} and converter efficiency is a linear function of its input voltage by α. Thus, the
saved power to the storage component (e.g., output capacitor) can be calculated by:

$$P_{OUT} = k \cdot V_{OC}^2 \cdot \frac{(1-k)}{R_T} \cdot \text{Conv Eff} \approx k \cdot V_{OC}^2 \cdot \frac{(1-k) \cdot \alpha \cdot V_{OC}}{R_T} \qquad (17)$$

$$\frac{\partial P_{OUT}}{\partial k} = 0 \rightarrow k = \frac{2}{3} \qquad (18)$$

From Equations 17 and 18, it can be easily understood that the maximum power operating point
for low-level input voltages is about two-third of the open circuit voltage.

In the TEG harvester, based on Equation 17, 18.5% output power improvement can be expected. However, as the input voltage increases, the input voltage effect on converter efficiency grows weaker and finally the V_{MPP} converges at half of V_{OC} [30].
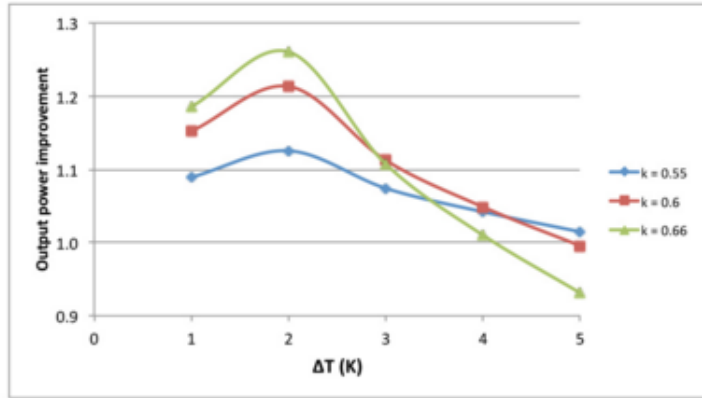

Figure 33. TEG Output Power Improvement vs Temperature Gradient

The BQ25505 (Ultra Low Power Harvester Power Management) also verified the fact that in low input voltage the maximum power extraction cannot be achieved at half of the open circuit voltage.
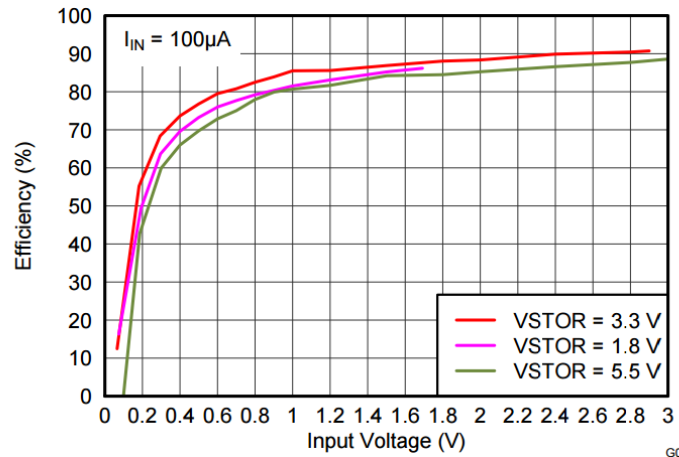
Figure 34. BQ25505 Efficiency vs Input Voltage

After obtaining maximum power point for either TEG or PV harvesters, the time duration (duty cycle ratio) were adjusted to match the required input impedance. Regarding the regulation stage several papers delved into the switched capacitor architecture due to its high efficiency and scalability. Therefore, the On-Chip capacitor can be utilized for regulation which results in very small scale regulation stage.[27][28][29]

CHAPTER V

CONCLUSION

In this work, I delved into the batteryless wearable devices' computation challenges from both software and hardware perspectives. The thesis set out to explore the concept of checkpointing in non-volatile processors to bring more reliability and flexibility into wearable devices. The study has also sought to know the optimized energy harvesting hardware configurations with maximum power extraction capability. The thesis sought to answer these main challenges:

1. Periodic checkpointing implementation for WISP version 5.
2. Optimizing existing Multi-input single out energy harvesting architecture.

The main empirical and programming results are chapter specific: Chapter II, Chapter V. The answers to those main study questions can be summarized as:

1. Answer: I implemented the periodic checkpointing every 50ms based on the RFID power traces to make the non-volatile processor immune to a power failure with saving the current state.

2. Answer: I proposed an optimized multi-input single-output energy harvesting system which employed open circuit voltage monitoring to extract the maximum available power for PV and TEG. Specifically, the proposed methodology for TEG obtained 18% power extraction improvement.

However, the Software periodic checkpointing imposed huge computation overhead to the system. The periodic checkpointing approach can grow more enhanced with more sensible

checkpointing tactics such as input voltage monitoring, stack size monitoring, nested function calls, and loops.

Hardware-wise, the proposed architecture has been threatened with one specific restriction, sizing. Therefore, we will focus on optimizing the converter component such as capacitors, inductors, and switches. Despite the fact that the TEG harvester maximum output power operating voltage point is about half of the open circuit voltage of the converter, the empirical results showed that in low-input voltages, half of the open circuit voltage may not be the optimal point.

In future, I can look into designing real multi-input energy harvester prototypes with optimized configuration. Moreover, I will work on smarter checkpointing techniques with lower overhead and more compatible with multi-core microcontrollers.

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