FRONT END OF A 900MHz RFID FOR BIOLOGICAL SENSING

By

REHAN AHMED

Master of Science in Electrical and Computer Engineering
Oklahoma State University
Stillwater, Oklahoma
2009

Submitted to the Faculty of the
Graduate College of the
Oklahoma State University
in partial fulfillment of
the requirements for
the Degree of
DOCTOR OF PHILOSOPHY
December, 2015

FRONT END OF A 900MHz RFID FOR BIOLOGICAL SENSING

Dissertation Approved:

Dr. Chriswell G. Hutchens

Dissertation Adviser

Dr. James E. Stine, Jr.

Dr. Weihua Sheng

Dr. R. Russell Rhinehart

ACKNOWLEDGEMENTS

I would like to first thank my advisor Dr. Chris Hutchens for giving me this great opportunity to work toward a Ph.D degree under his supervision. It has been a privilege to do research under his guidance. His constant guidance and encouragement provided me a clear path for my study, and I have truly enjoyed working with him over these years of acquiring knowledge and wisdom that will help me in future. I am equally grateful to my committee members. Dr. James E. Stine, Dr. Weihua Sheng and Dr. R. Russell Rhinehart

I feel very fortunate to have worked together with all my colleagues Srinivasan Venkatarman, Ran liao, Guanglei An, Zhe Yuan, Aniket, Kanishka de , Arpit and many thanks goes to them .

At last I want to thank my parents Borhan Uddin Ahmed and Luthfanessa Ahmed and my sister Shabnam Ahmed for their love and support.

Name: REHAN AHMED

Date of Degree: DECEMBER, 2015

Title of Study: FRONT END OF A 900MHz RFID FOR BIOLOGICAL SENSING

Major Field: ELECTRICAL ENGINEERING

Abstract: This thesis presents the front end of a 900MHz passive RFID for biological sensing. The components blocks of the front end consist of power harvester, switch capacitor voltage regulator, phase lock loop and a modulator and demodulator. As the RFID is passive so the power resource is limited hence the main focus while implementing all the block was low power and high efficiency power conversion. All the individual block were optimized to provide maximum efficiency. For the harvester to achieve high efficiency and high output voltage a design approach is discussed by which the device sizes are optimized and the values of the matching network components are solved. The efficiency achieved with this approach is 34% while supplying 74μA@1.2V.
The switch capacitor voltage regulator would supply power to the digital core of the RFID, which will operate at subtheshold or moderate inversion. The switch capacitor implemented in this work is a adaptive voltage regulator, as I intend to use the dynamic supply voltage scaling technique to compensate for the reduction in reliability of performance of the circuit due to variation of V_{TH} across process due to random doping effects and temperature in subthreshold.
The phase lock loop (PLL) block in this front end provide the system clock synchronized with the base station to all the backend blocks like the digital controller, memory, and the analog to digital converter ADC and the switch capacitor voltage regulator. The PLL is a low power with jitter of 24nsec and is capable of clock data recovery from EPC gen 2 protocol format data and consumes 3μW of power
Finally a ultra low power AM (amplitude modulation) demodulator is presented which is consumes only 100nW and is capable of demodulating a double-sideband amplitude modulated (DSB-AM) signal centered at 900MHz and the modulating frequency is 160KHz. The demodulator can demodulate signal having as low as -5dBm power and 50% modulation index. The modulation for transmitting signal is achieved by BPSK(back scatter phase shift keying).

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Figure Page

Figure Page

CHAPTER I

INTRODUCTION

1.1 Introduction

The term radio frequency identification is commonly known as RFID refers to a very broad spectrum of devices which are used to automatically identify or gather important information about objects, location and individual without any need of manual intervention and then transmitting that information to a computing system wirelessly. RFIDs have been around since 1970 [1] and until recently were used mainly for object tracking, identification, inventory, and detection of a wide variety of objects [2] . The RFID technology has a number of improvements over the barcode technology as they can be used to track a variety of objects in real time, do not have the constraint of line of sight, they have longer range of operation and can operate and withstand harsh environment. Hence this usage of tracking or identifying are extensively used in supply chain management where low cost passive UHF RFID tags are used to track and keep inventory of a variety of stored items. Due to advancements in technologies including, low power circuit design, innovative circuit architectures and high efficiency antennas, RFIDs can now be combined with a sensory system, which open the path for a variety of applications. Passive smart RFIDs with enhanced signal processing and greater functionality are becoming more accessible to the end user. Emerging smart RFID applications beyond the field of inventory and security are

applied to record storage environment data for temperature sensitive food and medicine during transport [3, 4], continuously monitor health of a structure to detect any damage to verify performance and/or safety of the structure [5], use to gather home and work environment data to make smart energy efficient homes [6, 7]. RFIDs can also be used in medicine and health care where RFID can be used as a implantable or wearable device to collect information or monitor bio-signals wirelessly and unobtrusively. Bio-signals examples include; temperature, blood pressure, heart rate, blood glucose level, and neural activity which can be used to study complex biological systems, effect of various disease and treat or monitor patients [8, 9] . These are some of the many applications playing a critical role in promoting smart passive RFID research and development.

From a power prospective an RFID can be categorized in two basic forms.

a) Active

b) Passive

1.1.1 Active RFID tags have an integrated power source (internal battery) and behave the same manner as passive devices but with increased performance. The integrated battery increases the cost of the tag, limits the tag life time, limits the size of the tag and also raises safety concern in case of bio-implant. These disadvantages of the active transponders limit the applications where these tags can be used.

1.1.2 Passive RFID tags are without an internal power source (battery) and harvest their own power. The source of their power supply can be acoustic, thermal, solar, mechanical or the RF field generated by the reader. Most of the RFIDs used come under this category. Compared to the

former by being battery free these RFIDs are more cost effective, smaller in size, greater in lifespan, and safer for bio-implantation. For sensor network and tracking applications the main advantage of being battery free is the cost, size, and safety. In case of biomedical applications these RFID must have low power consumption, high power conversion efficiency, long life span, and they must be unobtrusive to the user.

1.2 Research Objective

The basic working principle of the RFID is presented in Figure 1.1. The passive RFID system as presented in the figure consists of a Reader and a Tag. The Reader or Transceiver is the unit acting as the master and supplies the RFID tag with energy via the RF field and initiates the communication signals to command the tag to execute the requested action to be executed. The reader control can be either via a computer terminal or a mobile device.

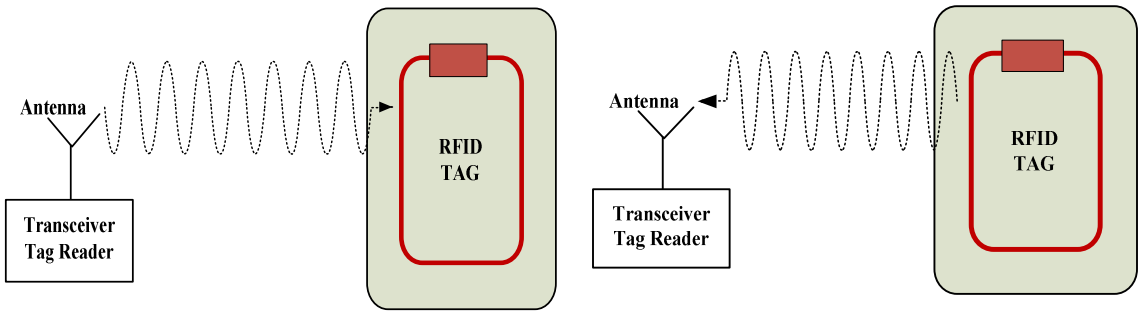


Figure 1.1 RFID system working principle.

The Transponder or Tag act as the identification device, receives and decodes RF signals coming from the reader. In this thesis the front end for a analog dominant passive RFID working at 900MHz is presented to be used for biological sensing. The RFID has the capability of addressability and also follows EPC gen 2 protocol. The RFID will have a band pass amplifier, a

8bit analog to digital converter (ADC), digital controller with memory will be capable of amplifying and processing the bio-signals and communicating with the base station. Since the research published by Karthaus [10], a very influential and widely cited paper in 2003, there has been a tremendous advance in research on passive smart RFIDs. A number of the previous works which has some commonality with this work are reviewed below and summarized in table 1.1

Table 1.1 Some of the published RFID tag features

Author	**Power Consumption**	**Sensors**	**Technology**	**Clock**
Daniel [11]	9µA@1V	Amp+8bit ADC	130µm	3MHz
Cho [12]	3.5µA@1.5V	Temperature	250µm	330KHz
Shen [13]	15.4µA@1.2V	8bit ADC	350µm	-
Kim [14]	15µA@2V	Temperature	250µm	-
Barret [15]	2.75uA@1.5V		130µm	1.28MHz

The work presented by Daniel, et al.[11] is similar to our work, they were the first to implement EPC gen 2 protocol in smart RFID. The RFID was developed for the purpose of biological sensing, having a chopper amplifier of less than 1 KHz bandwidth and 8bit ADC. The sensors presented by Cho, et al. [12] and Kim, et al. [14] respectively were both developed for environmental sensing both the RFIDs had temperature sensor and light sensor in them while the RFID developed by Cho was completely passive; the RFID by Kim was semi-passive. The RFID developed by Shen, et al [13] was also for the purpose of environmental monitoring it contained a temperature sensor and a low power successive approximation 8bit ADC with a sampling rate of 120 KHz however it does not follow the EPC gen 2 protocol. This work presents the front end of a passive smart RFID consisting of RF-DC rectifier, PLL, adaptive switch capacitor voltage regulator, demodulator and modulator. As a smart passive RFID going to be used for biological

sensing, so must harvest its own power. The main focus in this work is to lower power consumption and achieving higher efficiency and reduce system size. To meet this goal each of the block presented in this circuit were individually optimized so that the efficiency of the total front end is improved and the area minimized. The RF_DC rectifier is optimized to maximize the harvested voltage with a single stage to attain greater SNR-BW/Watt while attaining greater power harvest efficiency. With this design approach, the RF front harvester achieved an efficiency of 34% at -6dBm while supplying 70μA@1.2V. The generated DC voltage is unregulated as the incoming RF energy is variable, hence its needs to be regulated and limited before it can be used as the supply voltage for the Analog Front End (AFE) circuitry, logic and communications system blocks the AFE consists of 8bit ADC, Amplifier and voltage references. The power regulation is performed by a LDO for the analog and for the digital block, supply voltage is regulated by an adaptive switch capacitor (SC) voltage regulator. The SC voltage regulator is capable of supplying voltage between 350mV and 500mV. The adapting capability of the SC regulator compensates for the V_{th} (threshold voltage variation) across process and temperature. While supplying 6μA@400mV the SC regulator achieves a conversion efficiency of 86% with +/-12mV ripple. The tag needs to process the data received and the data to be transmitted to the receiver. As a result there must be a digital controller, memory storage and a packet forming pie coder for communication. The clock for the controller and the memory are provided by the PLL. The PLL presented in this work is low power and perform clock and data recovery from pie encoded data while it consumes 3.1μW and provides a systems clock frequency of 5.12MHz. Finally for both inbound and outbound communication we have a demodulator and modulator. The demodulator presented operates with as little as -5dBm and a 50% modulation index while consuming only 0.1μW The block diagram of the whole smart RFID is presented in figure 1.2

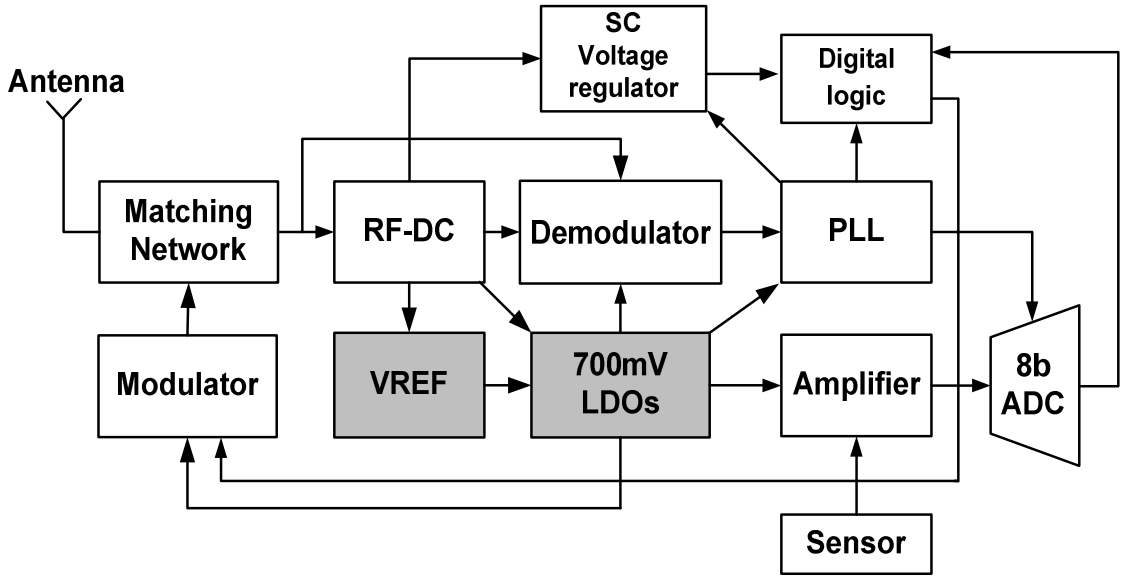


Figure 1.2 Block diagram of the total RFID system.

1.3 Dissertation Organization

Chapter 2 discusses the RFID power harvester. The power harvester consists of two significant pieces beyond the antenna, the matching network and the RF to DC rectifier. In this chapter different matching network options and their pros and cons are psesented. After the matching network the rectifier is discussed in detail different types of rectifier are reviewed. The sizing of the rectifying devices is dealt with in detail. Finally simulation results are presented along with comparison of other wireless power harvester works.

Chapter 3 presents the adaptive switch capacitor power regulator which supplies regulated power to the digital controller block. Digital control is designed to operate at or near subthreshold voltage. In this chapter the problems due to the variation of V_{th} for digital circuitry operating nesr subthreshold are discussed in detail. To resolve the problem of system failure or yield issues due to V_{th} variation a adaptive switch capacitor voltage regulator is developed and presented. In adaptive voltage regulator first a critical path monitoring circuit to determine the appropriate

supply voltage for the proper functioning of the digital block is presented. After which a over view of the different types of voltage regulator are discussed along with their advantages and disadvantages. Among different types of regulator, the switch capacitor regulator is chosen for it high efficiency.

Chapter 4 presents the optimization process of the power loss in switch capacitor voltage regulator and the different simulation results.

Chapter 5 presents the system phase lock loop (PLL). The primary function of the PLL is to provide data recovery and a system clock to the RFID tag synchronized with the base station clock. As power efficiency is of utmost important for passive RFIDs, the PLL presented is a low power PLL. The different blocks of the PLL; phase frequency detector (PFD), charge pump, low-pass filter, voltage controlled oscillator (VCO), frequency divider is discussed in detail. The PLL clock data recovery circuit capable of extracting the embedded clock from the EPC gen 2 protocol data is also discussed in detail in this chapter. The chapter concludes with the presentation of simulation and measured data of the PLL, Finally power and jitter performance are compared with previous works.

Chapter 6 presents the AM (amplitude modulation) demodulator and the BPSK (binary phase shift keying) modulator of the tag which are the critical block to receiving and transmitting data to and from the reader. As previously mentioned power is a premium. A 100nW demodulator is presented. The BPSK modulator presented does not actively transmit radio signal however, it reflects back the incident energy from the reader by BPSK, this is also known as signal back scattering.

Chapter 6 presents the conclusion of this work and suggests future research areas concentrations.

CHAPTER II

POWER HARVESTER

2.1 Introduction

In this work we present an implantable smart passive RFID, passives RFID have no internal power and must harvest power to perform any measurement and data transport task. There are various method of power or energy harvesting including solar, mechanical, piezoelectric or acoustic, thermal via the Sebeck effect and finally electromagnetic or electrostatic of radio frequency energy. An implantable neural RFID must be unobtrusive so it needs to be wireless and battery free making it low volume, safe and assists in avoiding repeated surgery for battery replacement. There are three main approaches for wireless power transfer (WPT) a) inductive coupling, b) electrostatic coupling which are used in near-field WPT and c) electromagnetic coupling in for far field WPT. The boundary that separates near field and far field is $\lambda/2\pi$ where λ is the wavelength of the concerned wave, for 900MHz which is approximately (5.3cm in air or 76mm in neural tissue) [16]. Beyond this boundary the near reactive field degrades rapidly.

2.1.1 Near Field: Due to its simplicity and safe, transmission inductive coupling is popular for near field WPT. In inductive coupling the primary and the secondary coil are tuned to resonate at the desired frequency. Coils having identical resonant frequencies are strongly coupled and power is transferred via magnetic resonance induction. The limitation of inductive coupling is that power transfer ratio degrades rapidly beyond $\lambda/2\pi$ and although this approach works well at close

proximity it requires accurate coplanar alignment. Also the near field harvesters mainly operate in the lower frequency range of tens of megahertz, as lower carrier frequencies results in reduced power loss in the media. As a result of low carrier frequencies the passive LC components required to implement inductive coupling become large in volume and the data rates low as well. Inductive coupling WPT was first commercialized successfully by the medical electronics industry [17, 18]. This harvesting approach is used to charge "pads", cell phones, laptops, as well as medical appliances [19].

2.1.2 Far filed: In case of far field the power is transferred from a transmitting antenna to a receiving antenna via radiating electromagnetic (EM) wave. For far field operation the transmitter typically emits the EM wave in the ISM band 900MHz-950MHz [20] and in case of microwave applications at 2.42GHz or 5.725GHz. WPT by far field does not require precise alignment as in near field. High power levels are limited in the far field approach due to potential health hazard from EM radiation [21], neural tissue heating, and also to avoid interference with other wireless system in proximity. To confine tissue heating within safety power limits transmitted power densities must be limited to ensure less than a 1C° /cm^3 rise in neural tissue. According to power absorption and temperature changes reported by authors Sun Mingui et al .in [22], Ibrahim et al.in [23] and Kennedy in [24]; the safe limit of incident power is 3mW before a rise of 1ºC/cm^3 in neural tissue temperature occurs. The maximum average specific absorption rate (SAR) allowed by FCC commissions is 1.6 W/kg in 1 gram of tissue [25, 26]. A study of an ingestible wireless device by Xu and Meng considering conductivity and permittivity of the human body tissue [27] reported an acceptable SAR level of 0.89W/Kg (≈ 0.89mw/ cm^3) for an input power level of 25mW at 430MHz. The work further demonstrates that the deeper the device is implanted in tissue less signal is received by the device. The SAR distribution further illustrates that in close proximity to the transmitting antenna greatest electromagnetic power absorption occurs. All the above studies demonstrate that with RF power along with today's circuit technology the

biomedical community has the capability to develop passive RFIDs capable of harvesting useful power from a far field source and sufficient to perform a variety of functions like temperature, pressure measurement, heart rate, blood glucose level and acquiring neural signal, amplify that and digitizing the acquired signal for finally communication to the base station. Key advantageous of far field harvesting are; small antenna size, high data rates and standoff distance. The efficiency of the harvester is determined by the efficiency of the components including the matching network, the rectifier. The safe power levels determines the maximum distance the harvester can operate. In next section of the far-field electromagnetic energy harvester is addressed.

2.2 Objective of the far field harvester designing approach

Most of the passive RFIDs can be classified into two groups. The first category are used for inventory control, carry out read or write of memory primarily responding to base station or reader interrogation with an identification number and are used mainly for identification or tracking. The power requirements of these RFIDs are a few micro watts [28, 29]. The second category of RFIDs known as smart RFIDs, are capable of sensing, processing and acquiring a signal along with communication sensor data. These RFIDs frequently consists of multiple system blocks beyond power harvesting; they consist blocks for power management, voltage references, amplification, and an Analog to digital converter (ADC) for digitizing the signal. These blocks together are referred as the Analog front end (AFE); they also include a PLL (also near constant current load), digital controller and circuits for in bound and out bound communication (very light loading). The power requirements of smart RFIDs are thus frequently dominated by the (AFE) which require a near constant current and require greater power compared to the first category of RFID, where load varies with the task as these are dominated by the digital state machine power requirement [30]. A summary of the power budget for the implantable smart neural RFID presented in this thesis is in table 2.1. Designing a power

harvester for implantable passive smart RFID is a challenging task first due to the high power requirement of smart RFID compared to an inventory RFID. Second due to the limit on the incident power allowed for ensuring a safe SAR level. To overcome the above disadvantages high efficient harvesters are essential to minimizing the incident power and preventing tissue damage and also to increase the depth of field of operation.

Table 2.1 Power budget for the micro neural RFID

Block name	Supply Voltage (V)	Quiescent current(μA)	Power Consumed(μW)
RF-DC converter	Input power		250
Voltage reference	0.9	9.85	8.865
LDO1	0.9	4.05	3.645
LDO2	0.9	1.27	1.143
PLL	0.7	4.43	3.1
Demodulator	0.7	0.138	0.096
Modulator	0.7	0.107	0.075

In case of digital CMOS circuits the power consumption is written as in (2.1)

$$P_{TOT} = Leakage\ Power + Dynamic\ Power \tag{2.1}$$

$$P_{TOT} = I_L V_{DDD} + C V_{DDD}^{\ 2} f \tag{2.2}$$

$$P_{TOT} = V_{DDD}(I_L + C V_{DDD} f) \tag{2.3}$$

Where P_{TOT} is the total digital power V_{DDD} is the digital supply voltage and I_L is the leakage current, C and f are the total or effective switched capacitance load and switching frequency

respectively. From (2.3) power consumption of the digital circuits can be minimized by reducing the V_{DDD} supply voltage while meeting the switching speed of the circuit. In case of analog circuit which are constrained by bandwidth (BW) and signal to noise ratio (SNR) of the system. The bandwidth and SNR are given by (2.4) and (2.5) respectively

$$I_D = BWnU_T C_C$$
$$I_D \propto BWC_C \tag{2.4}$$

$$SNR = \frac{V_{DDA} - 10U_T}{\sqrt{\frac{kT}{C_C}}}$$
$$\propto (V_{DDA} - 10U_T)\sqrt{C_C} \tag{2.5}$$

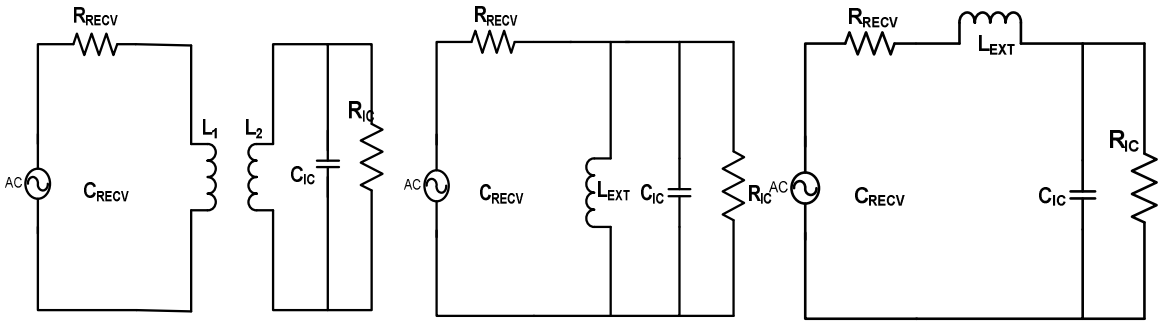
In the above equations I_D is the load current, n is the ideality factor, U_T is the thermal voltage and Cc is the amplifier compensation capacitance for the multiplying digital to analog converter MDAC, voltage reference, PLL, LDO blocks etc. and V_{DDA} is the analog supply voltage. The $10U_T$ values preserves headroom to avoid signal clipping or distortion. From (2.5) we see scaling V_{DDA} by 2 more than doubles SNR. An equal improvement in SNR can also be achieved by increasing the C_C by four times, however supply current would need to be increased four times to meet the bandwidth requirements. Thus increasing C_C would increase power consumption quadratically while increasing V_{DDA} linearly achieves the same result. Given a desired SNR and BW V_{DDA} should be increased verses increasing C_c to optimize power savings. It is concluded for smart RFIDs being AFE power consumption dominant, achieving as high a harvested voltage within the limits of the process is desired. A higher harvested voltage allows a higher V_{DDA}, and thus a lower analog load current and a greater SNR-BW/Watt. The efficiency of a power harvester is presented as in (2.6) where P_{hav} is the power loss in the harvester due to the diode drop loss, and P_{out} is the output power.

$$\eta_{hav} = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{hav} + P_{out}} \tag{2.6}$$

The harvester efficiency depends on a) harvested voltage, b) harvester load or harvester currents, c) matching network efficiency d) bandwidth of the rectifier switches, and e) available input power level. Higher voltages are preferred over lower currents for mixed signal RFIDs while for inventory or WORM/ROM/EPROM based RFID are power optimized at lower VDDs and constrained by their maximum current.

2.3 Matching Network

From the maximum power transfer theorem the harvester impedance must match the antenna impedance to ensure maximum power transfer from the antenna to the harvester. Other than the impedance matching some of the other requirements of matching network for this work are voltage boosting, setting up the bandwidth requirement and finally help in outbound communication by BPSK modulation. First we will discuss about the different types of matching network with their pros and cons and then decide which one to select.



(a) (b) (c)

Figure 2.1 Three different matching network.

There are simple three methods of impedance matching networks a) transformer matching b) shunt matching c) series inductor matching all of which are shown in figure 2.1(a), (b) and (c)respectively.

Transformer matching: The transformer matching is suitable when the antenna is a differential nature such as a quarter wave dipole while the rectifier rectifies the whole full wave that is both positive half and the negative half of a cycle. The advantage of this full wave rectification is they have less ripple (1/2) . In transformer matching to achieve high input voltage at the input of rectifier, the ratio between primary and secondary needs to be high resulting in both large inductor values and area. Hence this matching network has a larger foot print and in addition a lower Q. The resulting area and low Q efficiency makes on chip integration both difficult and in efficient. Other than this matching also requires close proximity and alignment of the primary and the secondary for good performance both of which are more easily and efficiently achieved off chip.

Shunt matching: In case of shunt matching as in figure 2.1(b) the added shunt inductor combined with the effective shunt capacitor tunes the circuit to the desired resonance frequency. Shunt matching provides a DC short for low frequency. This results in excellent ESD performance, but in case of shunt matching because of the absence of real part transformation there is little or no voltage boosting. In absence of any voltage boosting the input power and the antenna impedance would need to be high enough to develop sufficient voltage to turn on the rectifying devices and develop enough output voltage for RFID to work. One other disadvantage of this matching network is that it requires the antenna and the rectifier to be designed simultaneously as in absence of any impedance transformation they cannot be matched separately.

Series matching: Finally in case of the series matching network of figure 2.1(c) the series inductor resonates out the effective capacitor. This type of matching provides us with a voltage boosting when the antenna impedance is low relative to the rectifier impedance. This will be explained in detail later. One other advantage of this matching network is that it gives freedom to design the antenna and the rectifier independent of each other and their impedance can be matched using this network. In general this is not recommend as optimization across the system though more difficult is more optimal when considering the antenna, matching, rectifier and the load type. Among different topologies of series matching network like T, π and the L match network is prefered as it provides better efficiency compared to the other two [31] while boosting the input voltage of the rectifier by Q, where Q is quality factor of the network. Other benefit of using an L matching network is that it helps in absorbing the inductance of the bond wire, $L_{BOND,}$ and the capacitor C_{Pad} of the pad in a constructive manner as shown in the figure 2.2. In figure 2.2 R_{BOND} is the bonding wire resistance, C_M is the tuning capacitor, C_{IN} is the effective capacitor of the rectifier and R_{IN} is the effective load.

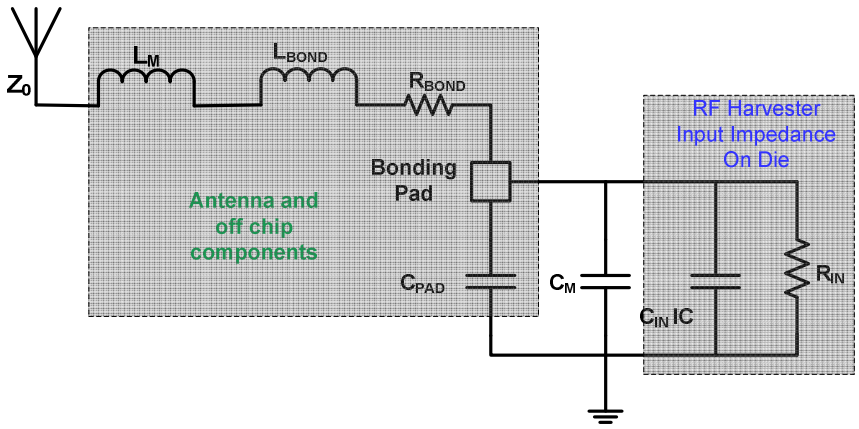


Figure 2.2 The L matching network adopted allow to exploit circuit parasitic constructively.

2.3.1 L matching network

There are two basic L matching, low pass and high pass which are used to step up and step down load impedance respectively depending which port is connected to the source and which one is connected to the load [32, 33]. The L matching network is shown in figure 2.3 where R_{IN} is the load resistance due to the input impedance of the rectifier and R_{ant} (Zo_{ant} the lossless impedance of the antenna) is the antenna impedance. L_{Match} is the sum of tuning inductor L_M and bondwire inductor L_{BOND}. The capacitor C_{Match} is the sum of C_{PAD} tuning capacitor C_M and rectifier equivalent capacitor C_{IN}IC. From the maximum power transfer theorem the network has to match the impedance connected to the right hand port to the impedance at the left hand port [31, 34] hence.

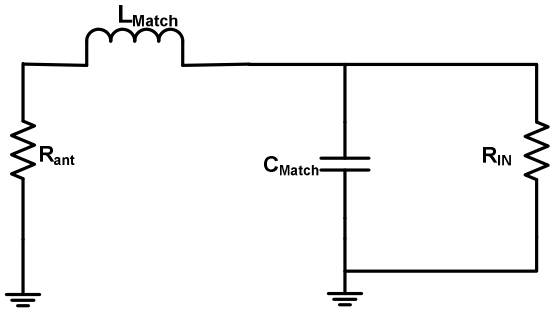


Figure 2.3 Low-pass L matching network with inductor L_{Match} and capacitor C_{Match} shown explicitly.

$$R_{ant} + jX_L = \frac{1}{\frac{1}{R_{IN}} + \frac{1}{jX_C}} \tag{2.7}$$

Where X_L is the impedance due to L_{Match} and X_C is the impedance due to capacitor C_{Match} so equating the real and the imaginary parts

$$R_{ant} = \frac{R_{IN} X_C^2}{R_{IN}^2 + X_C^2} \tag{2.8}$$

$$X_L = \frac{R_{IN}^2 X_C}{R_{IN}^2 + X_C^2} \tag{2.9}$$

$$Q_s = \frac{X_L}{R_{ant}} = \frac{R_{IN}^2 X_C}{R_{IN} X_C^2} = \frac{R_{IN}}{X_C} = Q_p = Q \tag{2.10}$$

From equation (2.10) and (2.9)

$$R_{ant} = \frac{X_L}{R_{IN}} X_C = \frac{X_C}{R_{IN}} \left(\frac{R_{IN}^2 X_C}{R_{IN}^2 + X_C^2} \right) \tag{2.11}$$

Dividing both the numerator and denominator by X_c^2 we get

$$R_{ant} = R_{IN} \frac{1}{\left(\frac{R_{IN}^2}{X_C^2} + 1 \right)} = R_{IN} \left(\frac{1}{Q^2 + 1} \right) \tag{2.12}$$

$$Q = \sqrt{\left(\frac{R_{IN}}{R_{ant}} - 1 \right)} \tag{2.13}$$

$$\frac{X_C}{X_L} = \frac{Q^2 + 1}{Q^2} \tag{2.14}$$

In the above equations X_L and X_C are the series and shunt reactance of the inductor and capacitor respectively. At resonance condition with the Q>>1 for the transformation the match reactance are $X_C \approx X_L$.

$$\eta_{mn} = 1 - \frac{Q}{Q_L} = 1 - \frac{\sqrt{\left(\frac{R_{IN}}{R_{ant}} - 1\right)}}{Q_L} \tag{2.15}$$

Where η_{mn} is the network efficiency, R_{IN} is the real part of the rectifier impedance seen from the antenna side and R_{ant} is the antenna impedance seen from the rectifier side. From equation 2.15 the efficiency of the matching network depends on the ratio of Q and Q_L [33]. To achieve higher efficiency high quality inductors are required. Therefore an off chip inductor is needed to be used in series matching network to achieve high efficiency. As mentioned in section 2.2 the series matching network provides Q times boost to the input voltage thus

$$Q = \frac{V_{\max}}{V_{in}} \tag{2.16}$$

In the above equation V_{max} is the peak input voltage at input of the rectifier and V_{in} is the peak voltage at the antenna, I_{DC} is the DC current, using the maximum power transfer theorem where P_{in} is the input power and R_{ant} is the antenna impedance, the defining RFID equation are

$$P_{in} = \frac{V_{in}^2}{4R_{ant}} = \frac{1}{2\eta} V_{out} I_{DC} \tag{2.17}$$

$$Q \approx \sqrt{\frac{R_{IN}}{R_{ant}}} = \frac{\omega L_{Match}}{R_{IN}} \tag{2.18}$$

$$R_{IN} = \alpha \frac{V_{out}}{I_{DC}} \tag{2.19}$$

$$\omega = \frac{1}{\sqrt{L_{Match} C_{Match}}} \tag{2.20}$$

In the above equation and value of η is the efficiency and α is a constant to mimic diode drop given by The above equation (2.17) and (2.18) depicts for a particular P_{in} and R_{ant} peak input voltage V_{max} varies linearly with Q. Another factor which is affected by Q in a resonance circuit is its bandwidth which is

$$2Q < \frac{f}{\Delta f} \tag{2.21}$$

Where Δf is the bandwidth and f is the resonance frequency. This band width requirement must also satisfy capacitance variation across process, which puts a limit on the Q value that can be utilized. To achieve high harvester efficiency we need to maximize the Q to the allowable limit and R_{IN} by determining the optimum NMOS width for the rectifier and the R_{ant} while maintaining the desired bandwidth as communication protocol demands. For a smart RFID; P_{in}, ω, Q, and I_{DC} are typically known. Solving (2.17-2.20)

$$V_{out} = 2\eta \frac{P_{in}}{I_{DC}} \tag{2.22}$$

$$R_{ant} = \eta \alpha \frac{2P_{in}}{I_{DC}^2 Q^2} \tag{2.23}$$

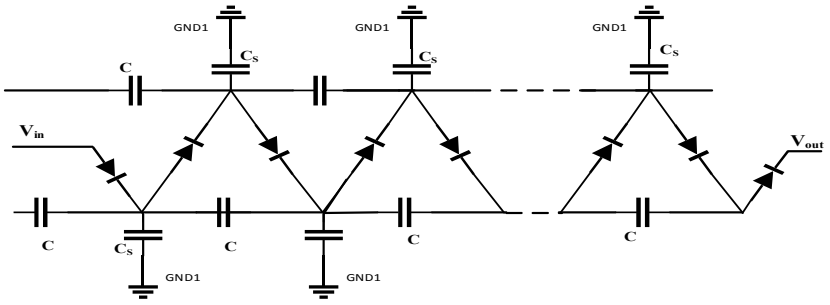
$$L_{match} = \frac{2\alpha\eta P_{in} Q}{I_{DC}^2 \omega} \tag{2.24}$$

$$C_{match} = \frac{I_{DC}^2 Q}{2\alpha\eta P \omega} \tag{2.25}$$

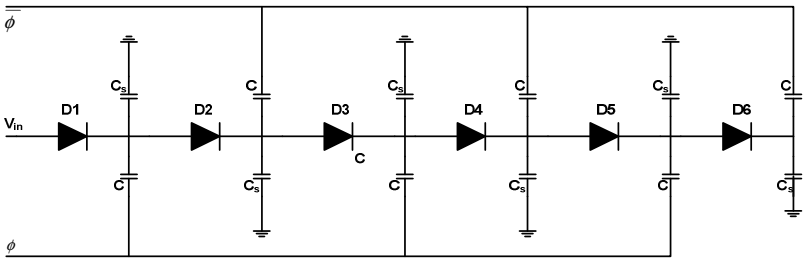
Where the constants η and α must be solved/optimized by simulation. Observe that for a passive smart RFID V_{out} solve for by setting I_{DC} as opposed to a digital dominant RFID setting V_{out} and achieving a maximum I_{DC}

2.4 Harvester design

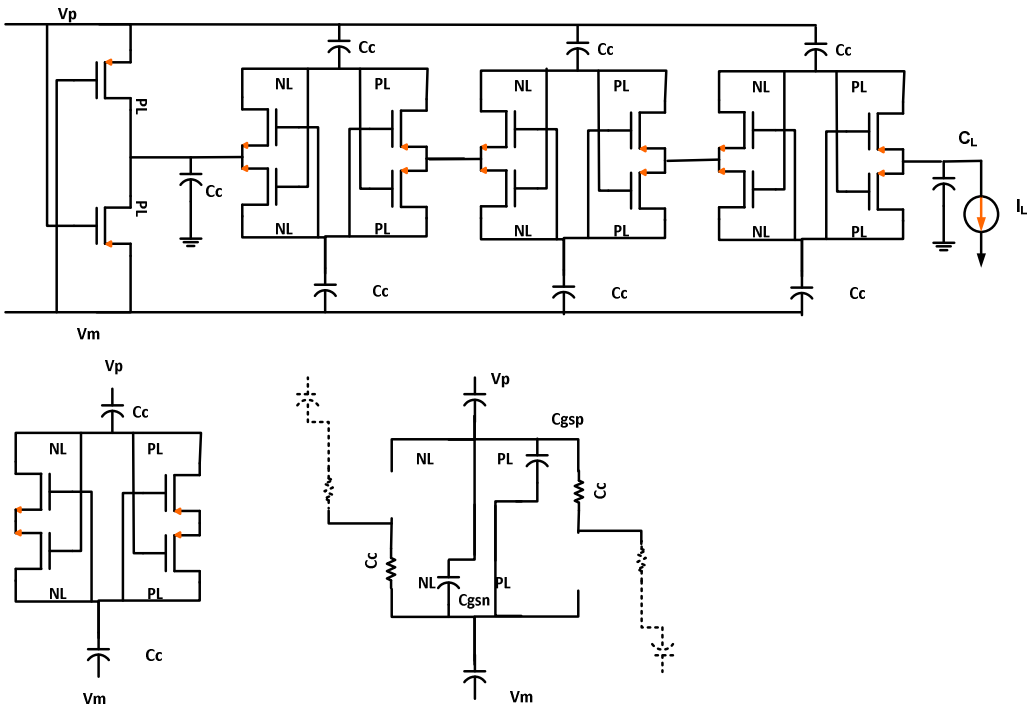
To harvest energy from the Radio frequency wave by far field approach the RF energy radiated from the base station is converted in to DC power, for which we need the rectifier. The rectifier power efficiency directly affects the performance of the system. There are various different design technique for voltage rectifier some of which are a) Cockcroft-walton voltage multiplier [35], b) Dickson Voltage multiplier [36] c) Mandal-Sarpeskar [37] voltage multiplier and d) Bergeret voltage multiplier [38] . For this work the harvester used is a modified Dickson charge pump topology. The regular Dickson voltage multiplier with diode is presented in figure 2.4. Dickson voltage multiplier is simple in architecture and its advantage over the Cockcroft Walton voltage multiplier is that in Dickson multiplier both the coupling capacitor C and the stray capacitor C_S are driven by the RF signal and all the stray capacitor are connected in parallel. Where as in Cockcroft the stray capacitors are connected in series with the coupling



(a) Cockcroft-walton voltage multiplier.



(b) Dickson Voltage multiplier.



(c) Mandal-Sarpeskar voltage multiplier.

Figure 2.4 Dickson voltage multiplier with diodes.

capacitors, this affects the efficiency greatly when C_S and C become comparable.

While designing the harvester the fundamental requirement we need to consider for having efficient harvester are a) $I_{ON} >> I_{OFF}$ that is the on current of the rectifier device must be much higher than the off or leakage current, b) The Q of the matching network need to be high at least greater than 6 to 8 but constrained by the communication bandwidth, c) bandwidth of the rectifying devices must be high to support harmonics of the rectified current. d) it is preferable to operate the rectifying device in subthreshold as in this region as current varies exponentially with the overdrive voltage. The g_m efficiency decreases as one moves from subthreshold to moderate inversion to strong inversion where the current varies as linear of the over drive voltage. Hence strong inversion is the least preferred region of operation. The rectifying device used in the harvester can be either a Schottky barrier diode (SBD), or diode connected MOS. The preferred device is the one which supports greater f_T and greater log slope. In [10, 39] the rectifier is

implemented with Schottky barrier diodes (SBD) which offers very good performance, as it has fast switching and low substrate leakage. The main limitation of the schottky diode is that all CMOS process do not support SBD and those that do are typically more costly.

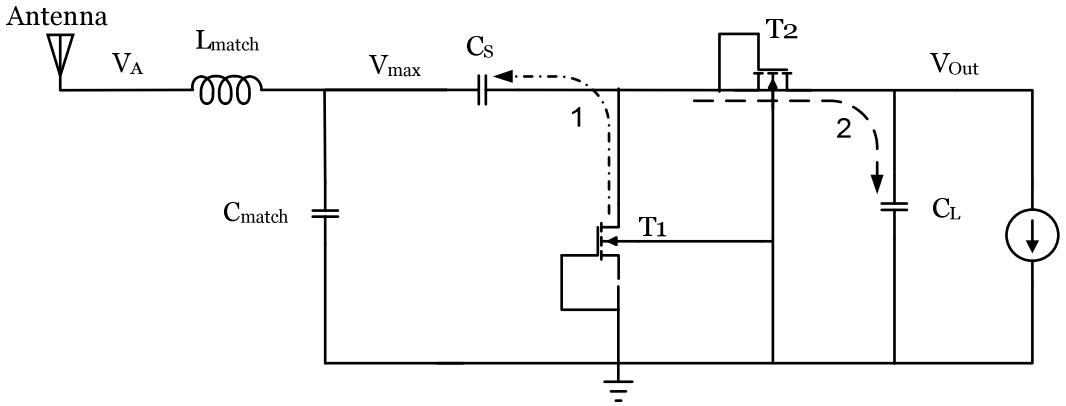


Figure 2.5 Schematic of one stage modified Dickson Charge pump.

To avoid SBD problem one solution is to use the diode connected MOSFET in place of the SBD. At 180nm or shorter node geometries the choice of the device depends on the availability. In this thesis the switches or diode are implemented using NMOS "diode" connected transistors as presented in figure 2.5. The multiplication action of the charge pump can be described as follows, in the negative half cycle C_S, the coupling capacitor, where $C_S >> C_{match}$ charges through T_1 to $(V_{max}-V_d)$. In the positive cycle a voltage equal $(2*V_{max}-V_d)$ turn on T_2 and charges capacitor C_L to $V_{out} = 2*(V_{max} - V_d)$. Where V_d is the minimum transistor turn on voltage at f_C the carrier frequency. In case of a N stage Dickson charge pump the steady state voltage is given by

$$V_{out} = 2N(V_{max} - V_d) \tag{2.26}$$

Where V_{out} is output voltage of the rectifier V_{max} is the amplitude of input sinusoid at the rectifier input and N the number of stages. Equation 2.26 portrays that to have higher V_{out} a lower turn on

voltage V_d is needed and also V_{max} needs to be higher. One of the fundamental requirement of an efficient harvester is f_T as expressed earlier in this section. The f_T of the MOS diode can be expressed as

$$f_{TNMOS} \approx \frac{1}{2\pi}\left(\frac{ID}{nU_T C_{gg}}\right) \tag{2.27}$$

$$= \frac{1}{2\pi}\left(\frac{I_S e^{\left(\frac{V_G - V_{TN}}{n\,U_T}\right)}}{n\,U_T C_{gg}}\right)$$

$$= \frac{\mu_n U_T}{\pi L^2 C_{OX}}\left(e^{\left(\frac{V_G - V_{TN}}{n\,U_T}\right)}\right) =$$

The significant things to notice from 2.27 are; the f_T is independent of the width and is inversely proportional to square of the length. To depict the dependence of f_T on V_{GS} a plot of f_T vs V_{GS} is presented in figure 2.6. The plot shows to support a particular f_T one cannot go below a certain V_{GS} and also f_T increases log linearly in the subthreshold region. As mentioned previously in the beginning of this section that to achieve high efficiency we need to have low $V_{GS.}$ This dictates a low V_T as well but still high enough to ensure an acceptable I_{OFF}.

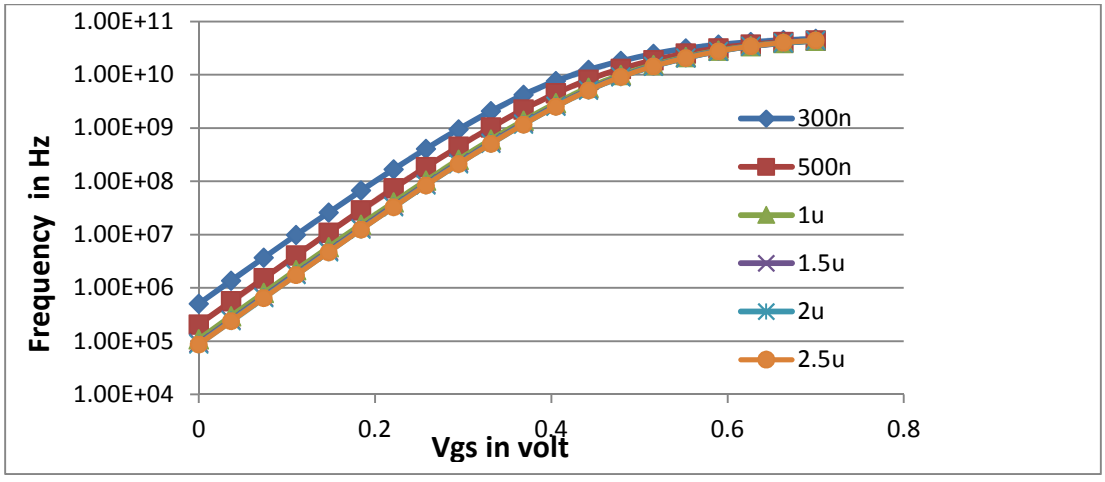


Figure 2.6 f_T versus V_{GS} plot for a minimum length and different width geometry transistor

During steady state harvesting the average charge harvested per cycle is constant. The average area under a single current pulse during steady state will thus remain constant, so current pulse amplitude varies inversely with the device width and the duty cycle increases with the device width. When a FFT is performed on the current train pulses it is observed that greater amplitude and narrow pulses support higher frequency components than shorter and wider pulses. A plot of the steady state current train pulses and its FFT is presented in figure 2.7. From 2.6 to support an additional seven harmonics V_d must increased by $2nU_T$. A plot of harmonic efficiency $\Delta i/\Delta P$ vs the component (harmonic) number is presented in figure 2.8 where Δi is the increment in current due to the nth harmonic and ΔP is the incremental power cost of harvesting the nth harmonic. From figure 2.8 we observe harvest efficiency increases with transistor width until the current pulse is such that 2 to 3 harmonic components are harvested after which we cross a point of diminishing returns. Current harmonics continue to be harvested but at a higher and higher cost. Thus we should increase the width of the device so that the resulting V_d in steady state support 2 to 3 harmonics. As presented in the power budget table, this smart RFID requires around 50μAof load current at a DC voltage of 900mV or higher. High efficiency of harvesters allows for a greater depth field of operation. As efficiency is dependent on V_d we select the device sized with minimum length, L_{min} but sufficiently wide enough to support the desired current density and the required "MOS diode" bandwidth.

The L matching network provides voltage boost to the harvester input voltage by a factor of Q , given by (2.16) where R_{IN} is the input resistance of the rectifier and R_{ant} is the antenna impedance. To achieve high harvester efficiency we need to maximize the Q, and R_{ant} by determining the optimum NMOS geometry for the rectifier and the R_{ant} while maintaining the desired communication bandwidth. The communication bandwidth standard must be satisfied across process capacitance variation.

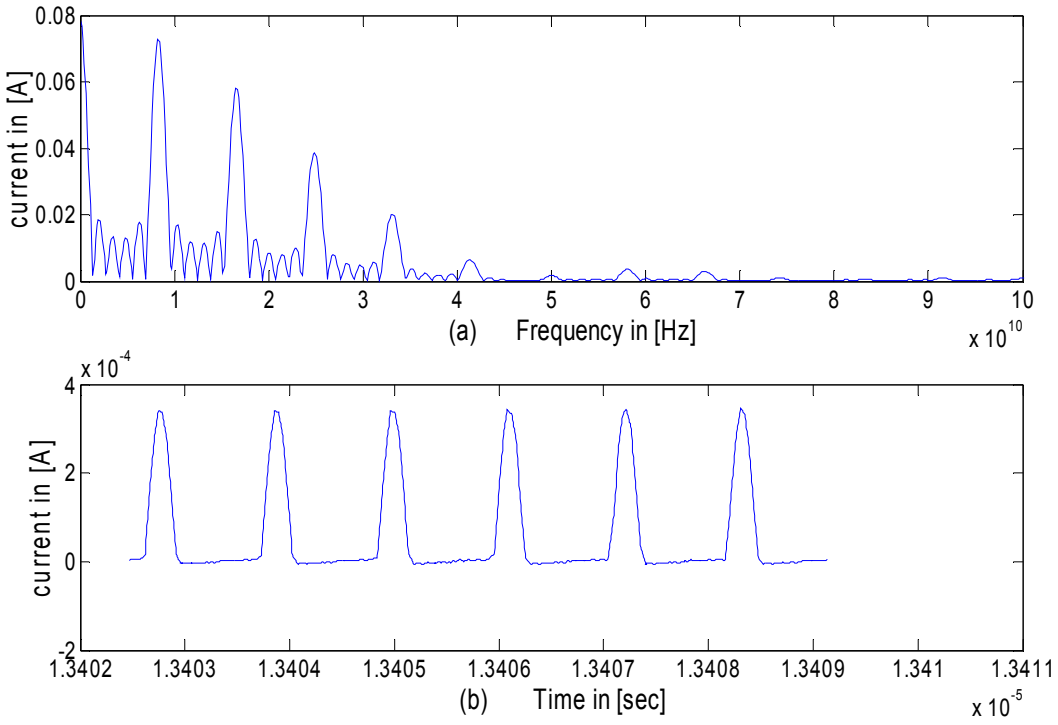


Figure 2.7 (a) MATLAB FFT of the rectifier current during steady state.

(b) Rectifier current waveform in steady state.

.

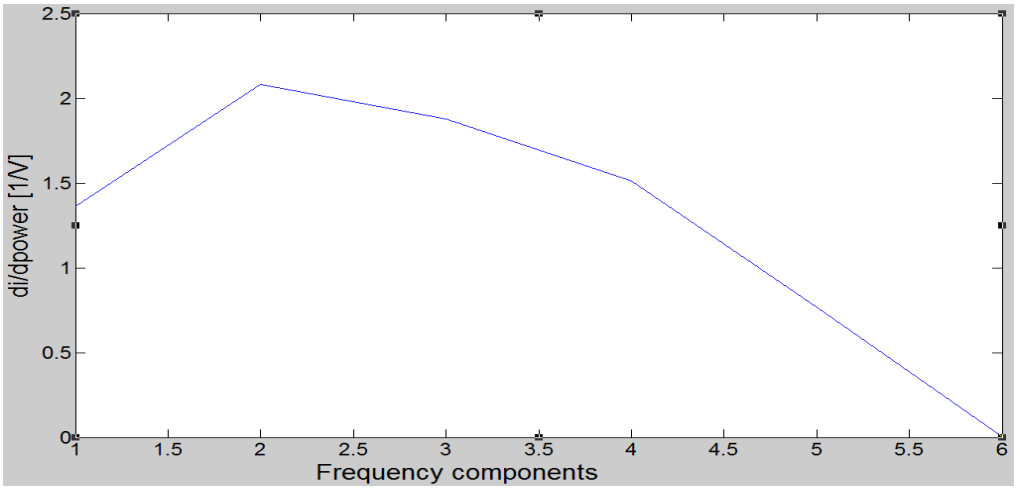


Figure 2.8 Plot of harmonic efficiency Δi/ΔP vs the component (harmonic) number.

2.4.1 Harvester design optimization

The objective is to maximize Q and R_{ant}, to maximize Vout and thus obtain higher harvester voltage while avoiding device breakdown. The maximum Q is constrained by the band width of the tuning circuit so R_{ant} and Q are used in concert to maximize V_{max}. Also in equation (2.26) in section 2.4 while calculating V_{out} the effect of the parasitic capacitances were not taken in to account. The schematic of the Nth stage of a N stage rectifier is shown in figure 2.9 with parasitic capacitor taken in to consideration. As indicated in figure 2.9 taking into account the parasitic capacitors of the rectifying devices equation 2.26 can be rewritten as

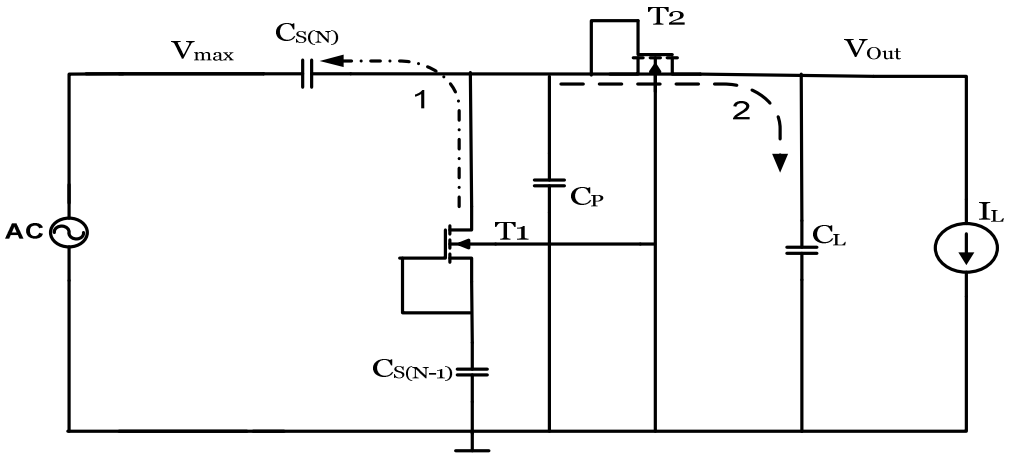


Figure 2.9 Nth stage of the rectifier where C_p is the sum of all the parasitic capacitor.

$$V_{out} = 2N\left[V_{\max}\left(\frac{C_S}{C_S + C_P}\right) - V_d\right] \tag{2.28}$$

The above equation indicates that the V_{out} decreases with the increase in parasitic capacitor so if C_P becomes comparable to C_S efficiency would be affected. Although $C_S >> C_P$ the size of the transistor must be optimize to achieve maximum efficiency.

Rectifiers are nonlinear even in the steady state condition. Therefore to optimize we need a current equation valid in all the regions of device operation. The EKV model [40] provides accurate current modeling in all regions, as a result the EKV model is used to estimate rectifier transistor $I_D - V_{GS}$ characteristic as follows:

$$I_D(V_{GS}) = I_S\left[\ln^2\left(1+e^{\frac{V_p - V_{GS}}{2U_T}}\right) - \ln^2\left(1+e^{\frac{V_p}{2U_T}}\right)\right]$$
$$\text{where } V_p = \frac{V_G - V_{th}}{n} \qquad (2.29)$$
$$\text{and } I_S = 2nK_p\frac{W}{L}U_T^2$$

In the above equations I_S is the specific current, U_T is the thermal voltage, Vth is the threshold voltage and V_p is the pinch off voltage.

From the efficiency equation 2.6 one can write

$$\eta = \frac{1}{\frac{P_{hav}}{P_{out}}+1} = \frac{1}{\frac{V_{GS}\, i_O(t)}{V_{out}\, I_{DC}}+1} \approx \frac{1}{\frac{V_{GSon}\, I_{DC}(T)}{V_{out}\, I_{DC}}+1} \qquad 2.30$$
$$\approx \frac{1}{\frac{\left(V_{GSon}(f_C) + nU_T \ln\left(\frac{mI_{on}}{Is}\right)\right) mI_{DC}}{V_{out}\, mI_{DC}}+1}$$
$$\approx \frac{1}{\frac{\left(V_{GSon}(f_C) + nU_T \ln\left(\frac{mI_{on}}{Is}\right)\right)}{V_{out}}+1}$$

where $V_{GSon}(f_C)$ is the minimum V_{GS} for NMOS turn on at the carrier frequency f_c and I_{on} is the average drain current at V_{GS} . Equation (2.30) shows that efficiency is maximized by having a greater harvest voltage, V_{out} and lower load current I_{out}, V_{out} is the output voltage which directly varies with Q. As the objective of optimization is to have higher harvested voltage with lower load current and achieving greater harvester efficiency so to perform the optimization we need to

calculate the R_{in} and Q for which we modeled the rectifier in MATLAB. The value of R_{in} is calculated from the rms voltage and current across the diode connected transistor. A plot of the R_{in} while varying the width W is presented in figure 2.10

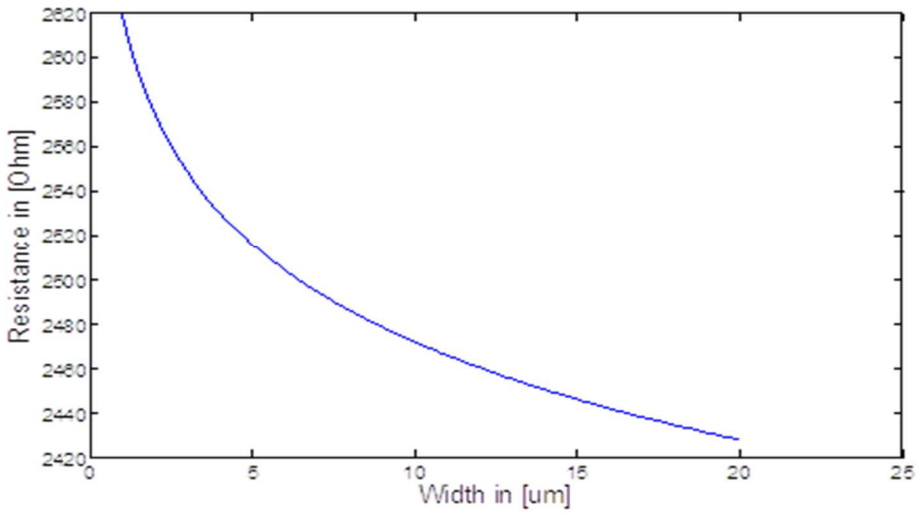


Figure 2.10 Rin versus transistor width.

From the above figure 2.10 it is observe that R_{in} decreases with increase in width of the transistor and it is nonlinear. After calculating the Rin, the Q values are also calculated using equation

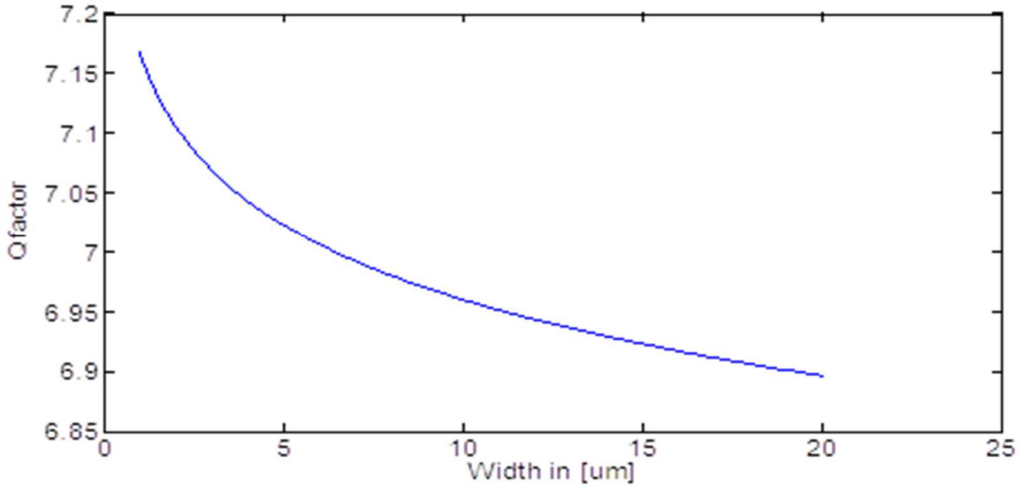


Figure 2.11 Q factor of the versus the transistor width.

(2.11) while calculating the value of Q, the R_{ant} is considered as 50Ω for convenience of RFID testing. Other values may be taken as required to maximize V_{max} while maintaining BW. A plot of Q with varying width is presented in figure 2.11. Figure 2.10 and 2.11 demonstrate that Rin and Q decrease with increases in width of the transistor. On the other hand V_{GS} or in this case V_d decreases with increase in width of transistor for constant drain current. Therefore considering (2.13), (2.16), (2.28) and (2.29), there exists a optimum width which would achieve maximum efficiency with maximum V_{out} and given load current. To find this optimal geometry harvester efficiency is simulated to find an estimate of the device geometry for maximum efficiency and V_{out} using a MATLAB program. The values of the matching network components are also determined from the Q values obtained in simulation. The efficiency plot from MATLAB is presented in figure 2.12. From figure 2.12 it is observed that maximum efficiency occurs in the range of 500 nm to 5 um of transistor width. The value of the inductor L_{match} is calculated to be 60 nH and the C_{match} value is 520 fF for a Q value of 6.5 To get an fabrication value for maximum efficiency a parametric sweep of device in the estimated width range is performed using Cadence Spectre with results presented in figure 2.12. In Cadence the resulting maximum efficiency device width is 1.75µm.

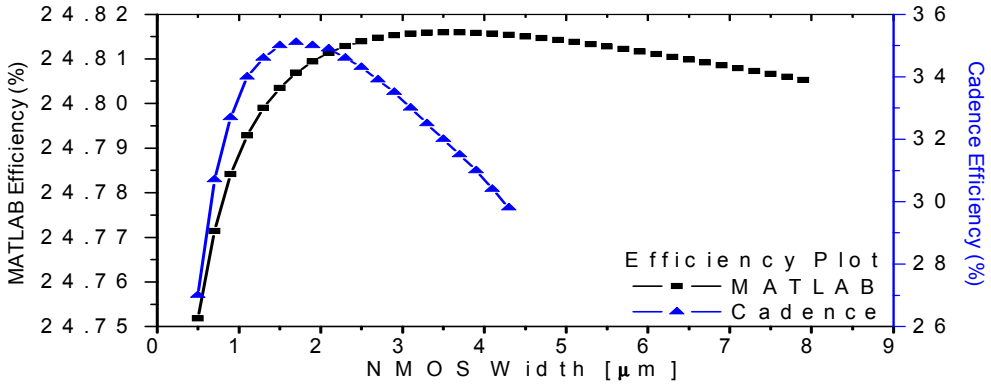


Figure 2.12 Efficiency η vs NMOS width from Matlab model and cadence simulation.

2.5 Results and discussion

In this case considering the resonance frequency as 900MHz the value of L_{match} comes to 60nH and the value of C_{match} is 521fF.With the above values of L and C a parametric sweep of the "diode" width is performed in Cadence where efficiency is plotted in Fig 2.11. This results in a maximum efficiency around a device width of 1.75µm, which supports our estimation with MATLAB of 2µm. Table 2.2 show the result of parasitic extracted simulation in cadence spectre for different width W with N equal to one at 900MHz, constant load power and a fixed input power of -6dbm in the 0.18µm IBM process. The desired power is maximum VDD i.e. 1V at 50µA. From the table one can see that the efficiency achieved are close to the plot in figure 2.12.

Table 2.2 Efficiency of the Harvester at different width of the rectifier device

Frquqency (MHz)	**MOS area**	**Pin (dbm)**	**L (nH)**	**C (fF)**	**Output voltage (V)**	**Load current range (µA)**	**Efficiency (%)**
900	2µm X .18µm	-6	74	422	1.16	74	34.3
900	3µm X .18µm	-6	74	422	1.08	74	31.9
900	3.5µm X .18µm	-6	74	422	1.02	74	30.2
900	4µm X .18µm	-6	74	422	0.970	74	28.7

Table 2.3 shows the comparison of our harvester to other similar harvesters. It is worth noting that all of the recently mentioned harvesters report a much lower load current than the proposed work. Also the output voltages are given as range and not as the voltage at the reported load current and as mention previously efficiency is highly dependent on both the load and output voltage. In comparison to the other harvester in our case the P_{in} minimum is higher by 4 to 16dBm

To show the dependence of total efficiency on the load current and the input power along with the harvester efficiency two plots figure 2.13 and figure 2.14 are presented. The plot presented in figure 2.13 is of the voltage V_{out} at the output of RF-DC converter versus the load current with constant input power of -6dBm. As the peak load current for the simulation was 73µA, the unregulated voltage developed is 1.18V which suggest that we can go below -6dBm as minimum V_{out} required is 900mV. Figure 2.14 is a plot of output voltage versus the input power for different load current. The plot clearly shows that the output voltage increases with the increase in input power and it also increases with the decrease in load current.

Table 2.3 Comparison of various RF_DC architectures

Author	**Frequency (MHz)**	**Process**	**Matching type**	**Switch type**	**No. of stages**	**Output voltage (V)**	**Load current range (µA)**	**Efficiency (%)**
Barnett [41]	900	0.18µm Bulk	Shunt	Schottky diode	16	0-3	1-8	4-8
Curty [42]	915	0.5µm SOI	Series	MOS diode	3	0-5	1	0-10
Sarpeshkar [37]	950	0.18µm Bulk	Shunt	MOS diode	2	0-5	4	16-23
Shameli [43]	920	0.18um Bulk	Series	MOS diode	4	0-1	2	5-10
Kotani [44]	953	0.18um Bulk	Series	MOS diode	1	0-2	31.5	67.5
Scorcini [45]	928	0.18um Bulk	Series	MOS diode	-	0-1.5	8.95	45
Triet [46]	915	0.18um Bulk	Series	MOS diode	-	0-1.5	1.26	30
Kuhn [47]	multiband	PCB	Series	Diode	-	0.9	18.25	52
This work	900	0.18µm Bulk	Series	MOS diode	1	0-1.2	74	34.3

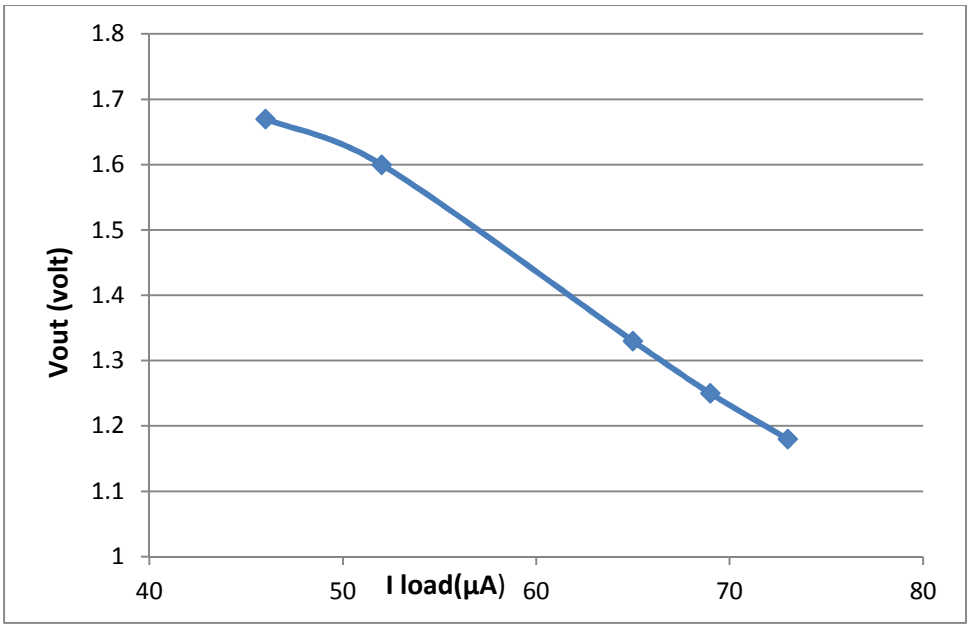


Figure 2.13 Vout vs I_L plot with P_{in}= -6dBm.

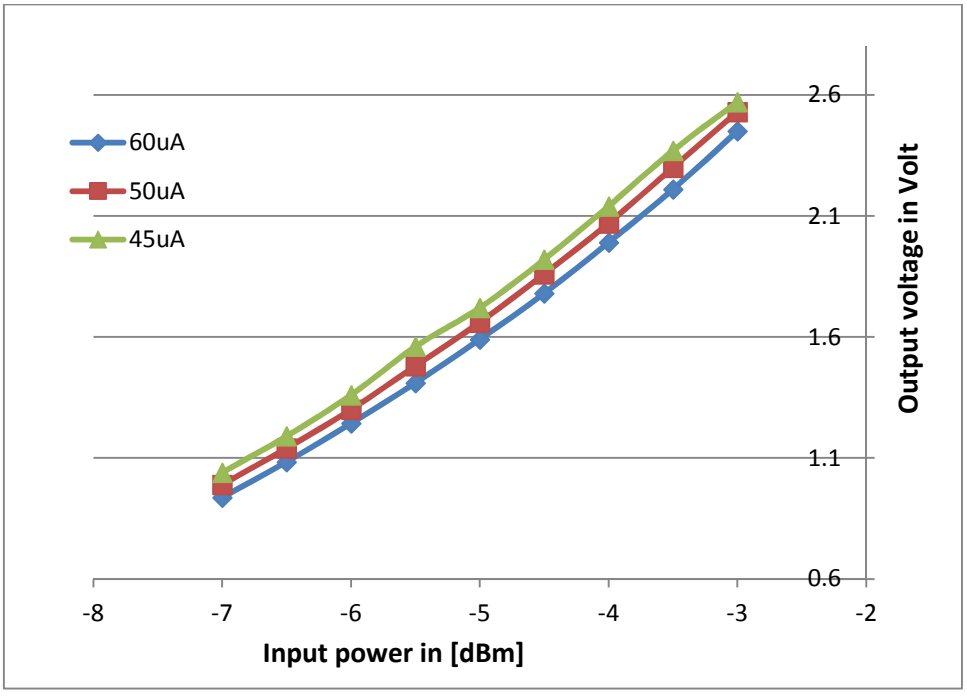


Figure 2.14 Vout vs Input power for different load current.

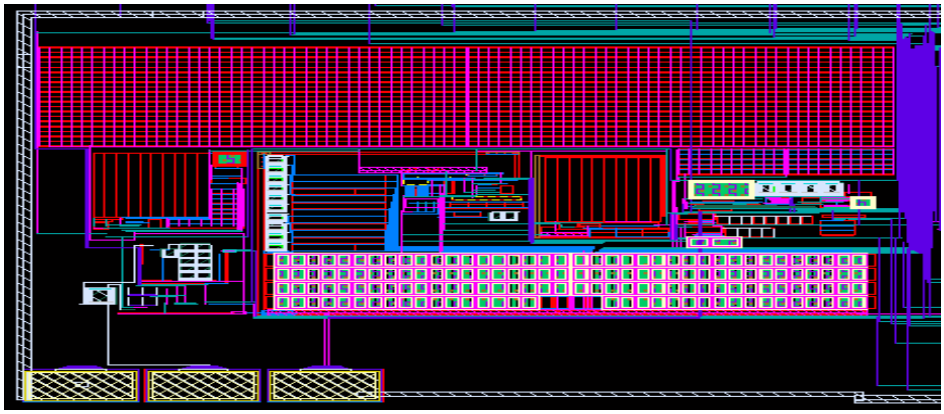


Figure 2.15 Layout of the harvester with matching cap and LDOs.

CHAPTER III

ADAPTIVE SWITCH CAPACITOR POWER REGULATOR

3.1 Introduction

The active power in a digital circuit varies quadratic with the supply voltage hence digital circuits uses supply voltage scaling to reduce power consumption [48-50], when this supply voltage is less than the threshold voltage of the transistor, the circuit is said to operate in subthreshold. Different leakage mechanism in a transistor are [51] a) subthreshold leakage, b) gate oxide tunneling, c) gate edge diode leakage and d) gate-induced diode leakage. In subthreshold the circuit consumes less energy for active operation due to supply reduction and the quadratic relation with the supply voltage. In addition static power is reduced due to DIBL effect on I_{off}, and the strong effect of supply voltage on gate oxide tunneling and gate oxide drain leakage [52]. In recent years with the rise in application of wireless network, and new process technology subthreshold circuit designing has gain much more favor. Circuits at subthreshold consumes less power and can now support bandwidth which is sufficient for RFID applications. In severely energy constrained systems such as passive smart RFIDs, where conserving energy is the primary objective subthreshold or near threshold circuits are ideal. In weak inversion the transistor channel is not inverted and current flow is by diffusion where the current maybe written

$$I_D = I_S \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nU_T}} (1 - e^{\frac{-V_{DS}}{U_T}}) \quad (3.1)$$

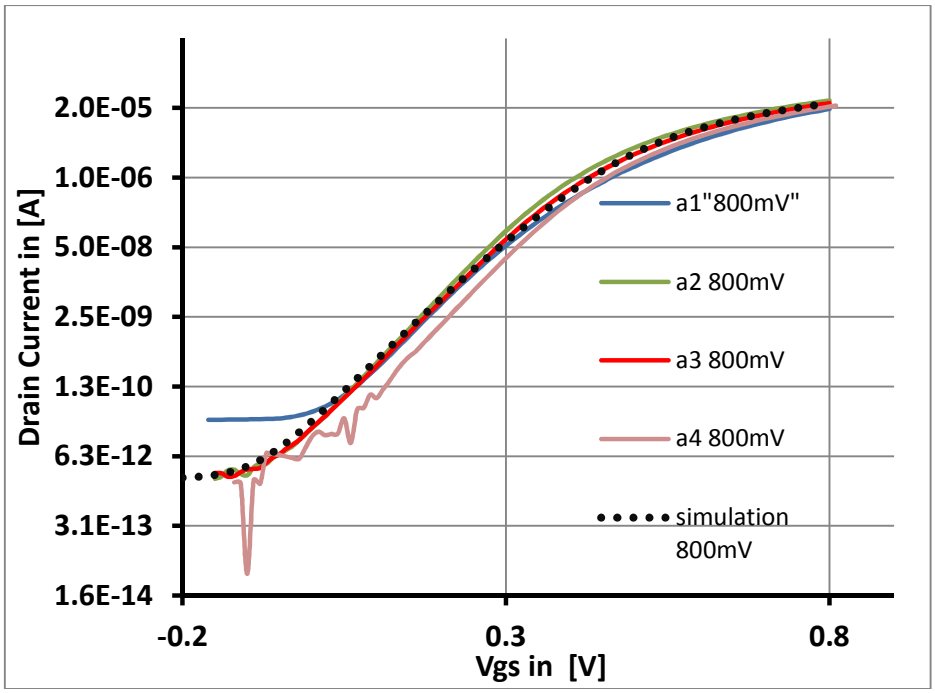


Figure 3.1 Plot of I_D vs V_{GS} at constant V_{DS}=800mV for NMOS of four different die, W/L=220nm/180nm at room temperature and V_{th}≈450mV.

So we observe from equation (3.1) and the plot in figure 3.1 I_D varies exponentially with the (V_{GS} – V_{TH}). To summarize in deep submicron processes operating in near threshold the issues that affects V_{TH} are

- short channel effect, reverse short channel effect [53].
- narrow channel effect and reverse narrow channel effect [54].
- DIBL effect.
- Variability and matching.
- V_{TH} variation with temperature.

All these cause variation in V_{TH}. This V_{TH} variation causes the variation of I_{ON} and I_{OFF} ratio, which affects the switching speed of a circuit. One can also observe from equation (3.1) the drain current I_D varies exponentially with V_{TH} in subthreshold so the effect of V_{TH} variation is more profound in subthreshold and near threshold. Put things in perspective, under classical logic operation we would expect compensation for

V_{TH} variation with temperature typically +/- 90mV +/- 120mV (Tempco equal 0.5 to 1.5mV/C), lot-to-lot and die-to-die

- Commercial -20C to 70C
- Industrial -40C to 85C,105C
- Military -55C to 125C
- Automotive -40°C to +150°C Soon to be 175C or 200C
- Oil field -40°C to +200°C OR -40°C to 225°C

$$\frac{I_D(T)}{I_D(T_0)} = \left(\frac{\mu n(T)}{\mu n(T_0)}\right)\left(\frac{T}{T_0}\right)^2 e^{1/U_T\left(V_{GS}(T_0) - e^{\left(-1/U_T\right)\left(\frac{V_{GS}(T)-V_T(T)}{T} - \frac{V_{GS}(T_0)-V_T(T_0)}{T_0}\right)}\right)} \tag{3.2}$$

$$V_{GS}(T) = \frac{T}{T_0}V_{GS}(T_0) + \left(1 - \frac{T}{T_0}\right)\left(V_T(T_0) + \alpha_{VT}(T_0) + nU_T \ln\left(\frac{I_D(T)T^{\alpha}}{I_D(T_0)T_0}\right)\right) \tag{3.3}$$

$$V_T(T) \approx V_T(T_0) + \alpha_{VT}(T - T_0) \tag{3.4}$$

where α_{VT} =-0.5mV/C t0 -4mV/C

- Supply voltage +/- 0.1VDD or higher as on LDOs readily afford requlation ro better than 2%.
- Mobiltity $\mu n(T) = \mu n(T_0)\,(T/T_0)^m$ where m = -1.5 OR -1.2 to 2

- Process +/- 70mV

- Threshold variability AvT/√2WL ≈2-3mV-um/√2WL 90 to 10nm.

In summary I_D variation can exceed +/- 25 fold excluding any VDD which is to be controlled to better than 2%. To mitigate this problem of V_{TH} variation due to process, temperature across technology we need to either overdesign our circuit which is not cost effective and most certainly consumes excess power. Alternate methods to compensate V_{TH} variation are 1) adaptive body biasing [55-57] 2) adaptive supply voltage [58, 59] scaling and 3) adaptive body biasing and supply voltage scaling in tandem[60]. In this chapter the application of adaptive supply voltage technique to compensate the impact of V_{TH} variation in subthreshold operation across process and temperature is presented. The concept of dynamic [61-63] supply voltage scaling is well documented as a tool for power reduction, product binning and testing. In this adaptive voltage regulator this concept is applied to compensate for the reduction in reliability of performance of the circuit in subthreshold operation. The idea is to dynamically determine in real time the supply value which ensures a systems reliable performance and yield at the target speed and then regulate the supply voltage at the determined reference value. In cases where the threshold voltage is higher (slow - slow process) the supply voltage is increased and additional power is consumed to ensure reliability. This can be explained more clearly by the block diagram presented in figure 3.2. This is a standard feedback control circuit where "system delay via critical path replica the plant replica" is compared to a reference clock and the error in the system timing is driven to zero by controlling VDD. The clock signal is applied to both the critical path replica and the phase comparator. The phase comparator compares the system clock with the delay in critical path replica and checks if system timing criteria is satisfied, if not the reference voltage is stepped up by one step and again the process of checking goes on until the timing criteria is satisfied, when timing criteria is satisfied the switch capacitor DC-DC converter clock switch is turned on. After this the SC DC-DC converter supply the Actual state machine

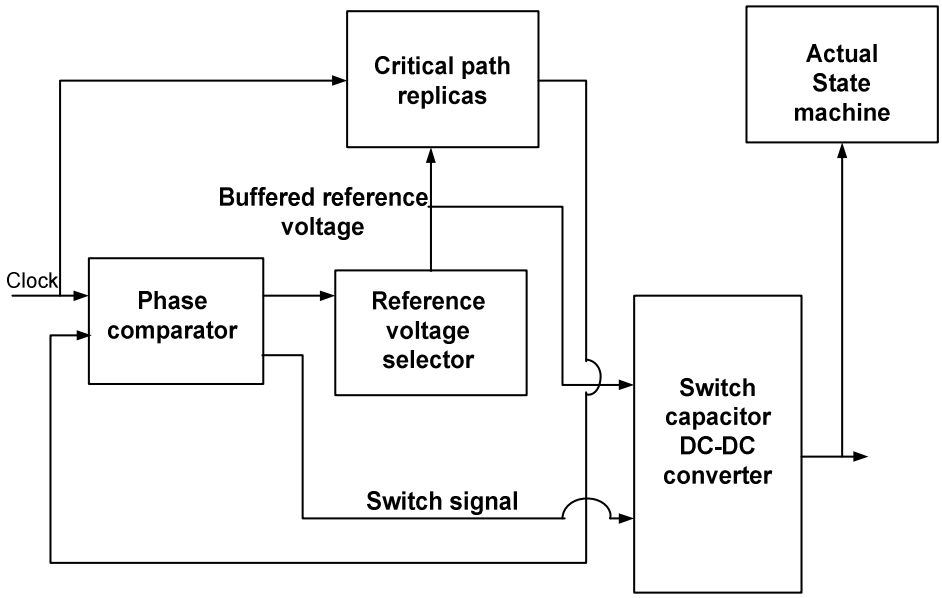


Figure 3.2 Block diagram of the adaptive voltage regulation process.

3.2 Critical path monitoring Circuit(CPM)

Timing closure of a circuit is determined based on its target yield, performance requirements, power dissipation, technology or the process used. Once cycle time is fixed and the design closure begins, a number of timing paths within the integrated circuit exceed the target cycle time. These critical paths then must be retimed to meet the cycle time. The critical paths are benchmarks of system timing as such critical path monitoring (CPM) can be used for real time adaptive supply voltage scaling(ASV). Based on the feedback signal provided by the CPM circuit the controller would control the supply voltage at or near its optimal value which would ensure proper functioning of the actual state machine. Keeping in mind the significance of CPMs, it needs to be located in the areas where the most severe variation is likely to occur. If CPM is inaccurate the feed back to the controller would also be in error resulting in system not being able to perform at the target speed and the reliability of the system is reduced [64]; so designing a accurate Critical path monitoring is critical. Various CPM systems that have been used for

dynamic voltage scaling [65-68]. The specific working of the system may vary but the basic blocks of a CPM system are functionally identical. A top level block diagram of the CPM is presented in figure 3.3

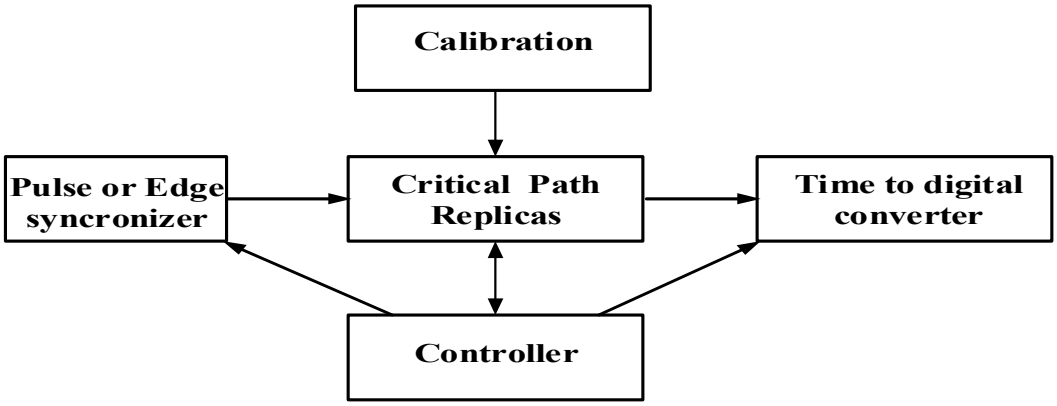


Figure 3.3 Block diagram of critical path monitoring system.

and include; a) Synchronizer, b) Critical path replicas c) Time to digital converter d) Controller with calibration paradigm.

3.2.1 Synchronizer

The function of the synchronizer is to generate the timing signal synchronized with the system clock. The critical paths in a state machine exist between latches so it would be advantageous if the timing signal is generated by a latch, thus able to capture the clock to data timing accurately. The synchronizer used in this work is a simple D flipflop.

3.2.2 Critical path replicas (CPR)

The most accurate approach is to use critical paths identical to the actual critical paths of the system state machine in CPM circuit. However typically critical path replicas are developed for the CPM that mimic the worst case behavior of actual critical paths. A representative of the actual critical path is constructed by using delay chains of NAND and NOR gate. These delay paths are

categorized in to two forms i) parallel delay paths and ii) serial delay paths. In a parallel path solution, multiple paths can be individually selected. As actual critical path can change with state of a state machine so selecting paths in parallel allows different paths to be synthesized which would otherwise be difficult to design by itself. The serial delay path use a multiplexing scheme to change the percentage of gate delay and wire delay in a delay path. The CPR for this adaptive regulator is represented by delay chains consisting of NAND and NOR gates. The delay chains are selected in parallel and then slowest path among these is selected by applying AND operation on all of them.

3.2.3 Time to digital converter

A time to digital converter converts the timing information from the delay path(s) to a control signal which is used to control the supply voltage selection, such that the delay error is corrected. The time to digital converter for this work is a simple circuit consisting of a D flipflop and an AND gate. This circuit ensures that the signal through the delay path arrives before one cycle of the system clock. A time to digital converter circuit is a simplified form of phase comparator.

3.2.4 Controller

The control block uses the signal from the time to digital converter to control the voltage reference selector and also the functioning of the CPM. The control block provides control signal for every three cycle. In the case explored here the control block does not have a calibration circuit, firstly for simplicity and secondly to reduce overhead power.

3.2.5 CPM role

The schematic of the CPM presented in this work is shown in figure 3.4. The Whole system works in three steps. The operation of the CPM is presented in the state diagram in figure 3.5 first the synchronizer consisting of a D flipflop generates a high signal synchronized with the system

clock which propagates through all the CPRs confirming the worst delay. In step two the time to digital converter generates outputs for the controller. The output of time to digital converter is “1” if the delay in the critical path is less than one clock period of the system clock so that the system timing is satisfied. On the other hand if critical path delays the signal by more than one clock period, then the system timing is violated and the output will be “0” . Observer “all” critical path delays must be meet.

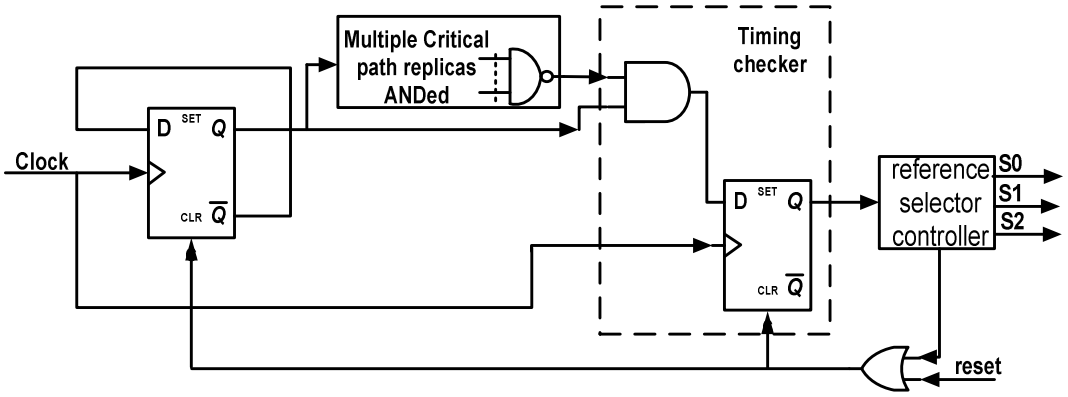


Figure 3.4 Schematic of critical path monitoring circuit.

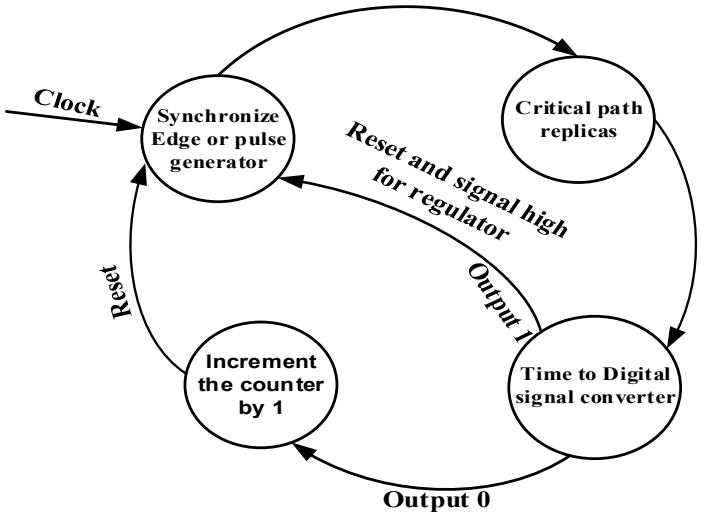


Figure 3.5 State diagram of the critical path monitoring circuit.

Finally in the third step depending on the output of the time to digital converter the controller which has a three bit counter, a “0” increments the count and while for a “1”, the count remains unchanged, the counter controls the reference voltage applied to regulator. For each CPM cycle the system timing closure is violated voltage selector counter is incremented by one and the regulator reference voltage is increased by 25mV which increasing the drain current by approximately 1.6 times. Table 3.1 presents the output of the counter and the reference voltage to explain it more clearly. In this last cycle after the counter operation the D flipflops are all reset except the counter to start a new cycle of the CPM. This cycle of increasing the reference voltage continues till the output of the time to digital converter is “1” and when the output is “1” a signal high is generated to start the operation of Switch capacitor voltage regulator.

3σ V_{TH} variation of minimum geometry NMOS due to process is +/-74.19mV at 450mV VDD and if we add another +/-90mV variation due to for temperature. Then

Total worst case variation is ≈164mV

Granularity = 164mv/8=20.5mV

We chose 25mV

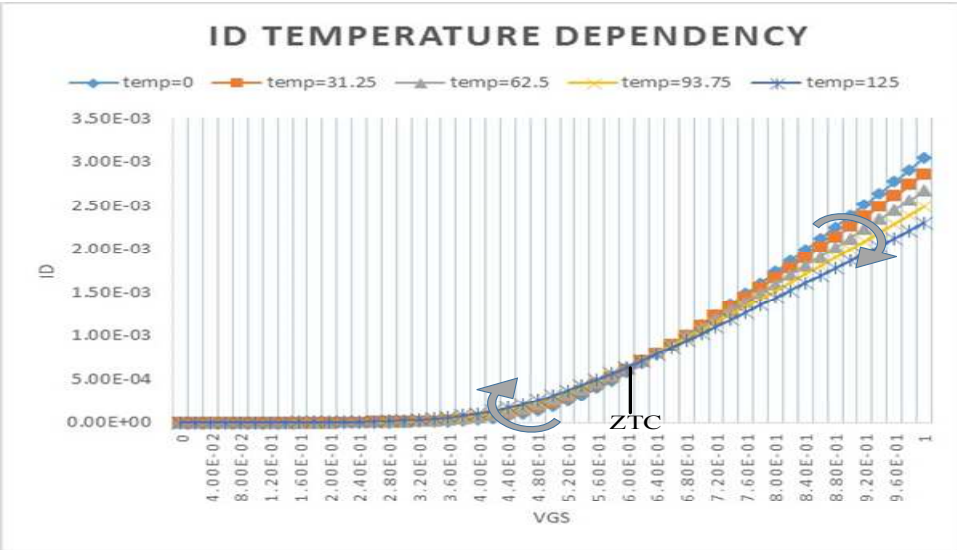


Figure 3.6 I_D dependency on temperature for subthreshold and velocity saturation.

Table3.1 Control output and V_{ref} selected			
S_0	**S_1**	**S_2**	**V_{ref}**
0	0	0	325mV
0	0	1	350mV
0	1	0	375mV
0	1	1	400mV
1	0	0	425mV
1	0	1	450mV
1	1	0	475mV
1	1	1	500mV

3.3 DC_DC Power Converter

The raw harvested voltage is unregulated as the incident RF energy is variable. This raw unregulated voltage needs to be regulated and limited before it can be used as supply voltage for different blocks in the system. The DC-DC converter performs this task of regulation in a system; it regulates the output voltage from raw input voltage with respect to some reference voltage by using a closed feedback loop. The DC to DC power converters can be broadly divided in to two category 1) Linear regulator 2) Switch mode regulator. Switch mode regulators can be further divided into a) inductor based b) capacitor based. Among the different regulators mentioned the linear regulator is capable of only supplying a lower regulated voltage than the raw supply voltage while switch mode regulators are capable of supplying either a higher or lower regulated supply voltage. In low power applications the DC-DC converter has become an essential part of system. They not only perform the task of power management but can also be used to supply multiple or variable supply voltages to optimize performance, power dissipation and speed. Some of the important parameters used to compare the merits of DC-DC converters as follow.

Efficiency-

$$\eta = \frac{P_{out}}{P_{in}} * 100 = \frac{P_{out}}{P_{loss} + P_{out}} * 100 \qquad (3.2)$$

Where P_{out} is the output power, P_{in} is the total input power and P_{loss} is the power loss of the converter itself.

Line regulation - The output voltage V_{out} changes with the input voltage V_{in} in a DC- DC converter so the line regulation is a measure of the ability of the converter to maintain the desired output voltage under varying supply voltage conditions.

$$Line\ regulation = \left(\frac{\Delta V_{out}}{\Delta V_{in}} \right)_{I_{out}=const} \tag{3.3}$$

Load regulation - Typically the output voltage V_{out} of the converter decreases as the load current increases due to the varying effective load. Thus the load regulation is the measure of the converter to maintain the output voltage under varying load conditions over a certain range of load.

$$Load\ regulation = \left(\frac{\Delta V_{out}}{\Delta I_{out}} \right)_{V_{in}const} \tag{3.4}$$

Noise - In case of low power application such as the one presented in this work or wireless sensors network one can have sensitive sensors or RF transmitter components which may be sensitive to switching noise in the output voltage or in case of inductor base switched converter the switching inductor may cause electromagnetic interference. For noise sensitive applications low noise regulated supplies are essential. Apart from the factors mentioned, some of the other factors for quantifying the converter are its footprint relative to area taken by it in the whole system. The output voltage is another quantifying characteristic, as in many applications along with variable input raw voltage the power demand also fluctuates. Hence to optimize the power management system a variable or multi output voltage converter is required instead of single fixed output voltage.

3.3.1 Linear Regulator

Linear regulators are active linear analog circuits that are used to convert a noisy raw unregulated DC power source in to well regulated power source. Linear regulators have simple design and are well suitable for analog noise sensitive applications, as they do not have any reactive (magnetic or capacitive exclusive of decoupling which is a must) components, also have the advantage of being completely on chip and having smaller footprint a representative architecture for linear regulators is the low dropout (LDO) regulator shown in figure 3.7. The dropout voltage refers to the minimum voltage drop between input and output voltages required to maintain the regulated output voltage $V_{out.}$ The LDO consist of an error amplifier and a pass-transistor which acts as a voltage controlled current source. The error amplifier continuously monitors the output voltage against a reference voltage. Based on output of the error amplifier regulation is performed

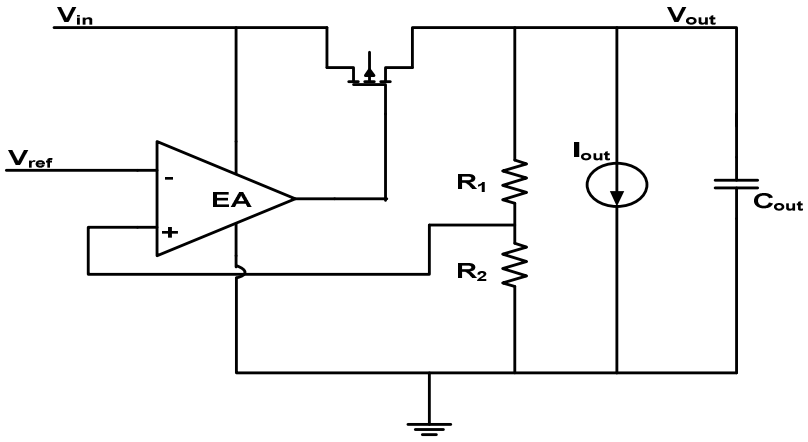


Figure 3.7 Low dropout Linear regulator.

by controlling the amount of current delivered to the load in order to maintain the output voltage at the desired value. The efficiency of the linear regulator is indirectly proportional to the dropout voltage given by

$$\eta = 1 - \frac{V_{drop}}{V_{in}} \tag{3.5}$$

Hence high efficiency is achieved for low drop out voltage and with increase in dropout value the efficiency drops drastically. There is also the problem of frequency compensation which may be sensitive to noise or process. As mentioned in chapter 2 our objective in self-powered system is to optimize power for which the digital blocks operated in moderate inversion as a result of which the drop out voltage would be approximately 450mV the efficiency performance of the LDO would be around or less than 50% for a unregulated voltage of 900mV-1.2V. Hence this type of regulator is not suitable for the voltage regulation in subthreshold range in the smart passive RFID.

3.3.2 Switch Mode Power Converter

From section 3.3 and 3.3.2 it is seen that switch mode power converters are the most suitable options available for the regulation of subthreshold supply voltage for the state machine in passive smart RFID. They can operate over a large dynamic range of input voltage without sacrificing efficiency. A switch mode converter consists of a power stage and a closed loop feedback controller to regulate the output voltage. The power stages consist of switches along with some reactive elements like inductors or capacitor to store energy temporarily from the input during the charging phase and then transfer it to the output during the discharge phase. Figures 3.8a and b illustrate the two typical types of step-down switch converters a) inductive converter, and b) switched-capacitor (SC) converter. The feedback controller controls the power stage to achieve desired output voltage, regardless of line, load or component variations. As the Q of the capacitors in this process is very high in the range of 1000 for the frequency we will be operating at, one can achieve more than 80% efficiency with switching regulator. The pros and cons of the

two types of converters are discussed in next section to determine the type of switch converter best suited for this application.

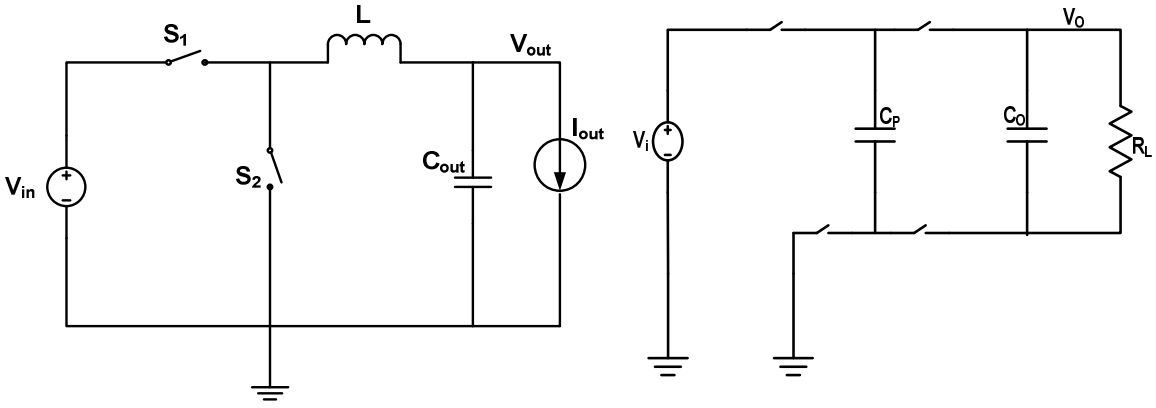


Figure 3.8 a)Power stage topology of Switch mode buck converter. b) Power stage topology of 2-to-1 switched capacitor converter.

3.3.2 a) Switched Inductor converter

The switched inductor converter presented in figure 3.8a is a buck converter. In a switched inductor converter charge is transferred from the input to the output in the form of magnetic field current in the inductor during in each cycle. To control the output voltage to the desired level the amount of energy is controlled by varying the duty cycle of current supply in the inductor. Ripple is controlled by having a sufficiently large decoupling capacitor at the output. In a switched inductor converter the inductor needs to have high Q or quality factor to reduce power loss and improve the overall efficiency [69, 70]. To meet the criterion of high Q the inductor typically needs to be off chip, although recently we have some CMOS process where small on-chip inductors are available. They are costly and have low Q-factors which severely affect the efficiency. This is the first drawback of inductor base converter for full on-chip integration. Achieving various conversion ratio is straight forward with switch inductor converter so greater granularity of the output voltage can be attained, but the capacitors have substantially higher energy and power density than the inductor [71]; resulting in the inductor having large footprint

which increases chip area hence cost. Beside the previous mentioned reasons one of the other dis-advantage of switched inductor converter on-chip integration is electromagnetic interference (EMI) to the surrounding devices. Due to these reason we need to consider the other alternative which is switch capacitor converter.

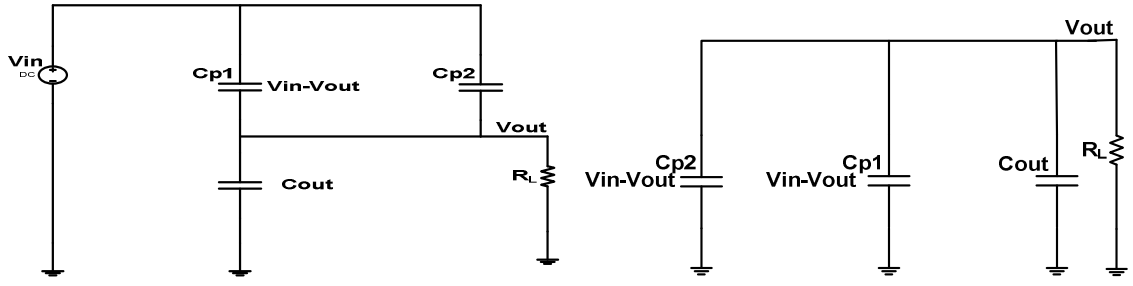
3.3.2 b) Switch capacitor converter

The second switch mode DC–DC converter is the switched-capacitor (SC) power converter represented in figure 3.8 b with conversion gain (CG) of 1/2, CG is the ratio of no load output voltage to the input voltage of the converter. Similar to the switch inductor converter, a SC converter also consists of two major components, the power stage consisting of arrays of capacitors which acts as energy storage, along with a closed loop feedback controller. In these converters the output voltage is maintained at a desired level by the use of switches and clock control signals to store sample charge on the capacitors during the charging phase and then transfer the charge to the output load and decoupling capacitor. The major advantage of SC power converters is; they employ capacitors as energy storage devices instead of inductors. Therefore we can achieve high efficiency with lower power loss in the converter and smaller foot print[71]. One major drawback of traditional SC DC–DC converters is their ability to provide only a single converter gain (CG). Due to charge redistribution if the output voltage deviates too much from ideal conversion ratio the power loss becomes excessively high hurting the efficiency of the converter[72]. In applications like dynamic voltage scaling where we need to accommodate a large range of output voltages conventional SC power converters with a fixed CG are not suitable. To overcome this drawback, SC power converter designs involving more switches and capacitors providing multiple CG is designed [73], capable of delivering output voltage of multiple discrete levels.

3.4 Design consideration for implementation of scalable switch capacitor converter

From the discussion in previous section in 3.2 it is conclude that scalable switch capacitor is the most suitable option for the adaptive voltage regulator, supplying voltage in the range of moderate inversion. In designing of the SC voltage regulator the main characteristic or the metrics that needed focus were discussed in section 3.3. To maximize the efficiency and power density one needs to choose the proper topology for the SC voltage regulator. The SC voltage regulator can commonly be categorized in to five different topologies which are; ladder, Dickson, Fibonacci, doubler and series-parallel. Each different topology has different advantage and thus may suit a different application. The Dickson and ladder topology provides regularity to the switches and their driver. Fibonacci and doubler are able to achieve high voltage gain for utilizing same number of switch and capacitor, the series-parallel topology maximize the utilization of capacitor hence they occupy smaller capacitor area. In this research work one of the objective is to minimize the footprint of the regulator so the series-parallel is chosen for the SC voltage regulator [74]. In this work we are only going to focus on the step-down voltage regulation as the SC regulator is going to be used to supply voltage to the digital core of the smart RFID working in subthreshold voltage.

To explain the basic operation and the important characteristic of the SC converter the 2:1 conversion ratio configuration for the series-parallel topology is chosen and is shown in figure 3.9



(a) (b)

Figure 3.9 Switch Capacitor of CG=1/2.

The reason for choosing this configuration is its easier to explain and the 2:1 conversion ratio configuration in all the topologies are nearly identical.

3.4.1 Output voltage

In a SC converter charge is stored in the pumping sampling capacitor and transferred to the load in the form of (charge/time) voltage. Hence the output voltage depends on the configuration of the SC. In figure 3.9 the pumping capacitors are first charged to V_{in}-V_{out} then during the discharge phase the pumping capacitors C_P are connected parallel with C_{out}. During the entire period of charging and discharging the load current I_L is provided to the load R_L by decoupling capacitor C_{out}. For simplicity the switch resistance and output ripple are considered to be negligible. As the ripple must negligible relative to V_{out} in a properly designed supply. Therefore applying the law of charge conservation

$$C_P(V_{in} - V_{out}) + C_{out}V_{out} = C_P V_{out} + C_{out}V_{out} + I_L T \tag{3.6}$$

Solving for V_{out} gives

$$V_{out} = \frac{V_{in}}{2} + \frac{I_L T}{C_P} = \frac{V_{in}}{2} + \frac{I_L}{C_P f} \tag{3.7}$$

Equation (3.7) shows that V_{out} in a SC converter depends on the capacitor configuration, load current, value of the pumping capacitor and the switching frequency. The intermediate voltage between the different discrete no load voltage is thus obtained by controlling these above mentioned aspects of a SC converter.

3.4.2 Efficiency

The efficiency of any voltage converter can be expressed as

$$\eta = \frac{P_{out}}{P_{in}} * 100\% \tag{3.8}$$

For SC converter equation (3.8) P_{in} can be broken into components and can be written as

$$\eta = \frac{V_{out}\ I_{out}}{CG\ V_{in}\ I_{in} + P_{cntrl} + P_{loss}} * 100 \tag{3.9}$$

Where the first term in (3.9) is the power extracted from the input purely for charge transferred to the load, P_{cntrl} is the average power required to operate the controller of the power stage and P_{loss} is the power loss in the power stage which includes conduction loss, switching loss, back plate parasitic loss redistribution loss and reversion loss. All the mentioned losses in power stage are next explained in detail next.

1) Conduction loss: In SC converters, the switches in power stage are implemented using MOSFET transistors. The transistor used as switches operate in triode region where current voltage relationship is given by

$$I_D = \mu C_{OX} \frac{W}{L} (V_{GS} - V_{th}) V_{DS} \tag{3.10}$$

Here μ is the mobility of the carriers, C_{OX} the oxide thickness, W the width of the transistor, L the length of the transistor, V_{th} the threshold voltage, $V_{GS,}$ the gate to source voltage and V_{DS}, thee gate to drain voltage of the transistor. This equation implies a linear relationship between V_{DS} and I_D which indicates the path from drain to source can be modeled by a resistor that is controlled by V_{GS}. The resistance is calculated to be

$$R_{on} = \frac{1}{\mu C_{OX} \frac{W}{L} (V_{GS} - V_{th})} \tag{3.11}$$

Therefore when current flows through the transistor resistance R_{on} causes conduction loss. As R_{on} is inversely proportional to width W conduction loss can be minimized by increasing W. While increasing W decreases R_{on}, parasitic capacitance associated with the transistor increases with increasing width, which in turn will increase the switching loss. The detail of switching loss is explained in the next section.

2) Switching loss: Switching loss is another contributor to the power loss in the power stage. This power loss is suffered due to the charging and discharging of the parasitic capacitance associated with the transistor during switching. Among the various parasitic capacitances associated with the transistor; gate to source capacitance C_{GS} dominates and contributes significantly to this power loss component.

$$\begin{aligned} P_{SW\,loss} &= f_S \sum_i C_{GS} V_{GS}^2 \\ &= f_S C_{OX} \sum W_i L_i V_{iGS}^2 \end{aligned} \qquad (3.12).$$

Where f_s is the switching frequency and C_{GSi} and V_{GSi} are the gate to source capacitance and voltage swing of the ith switching transistor. In section 3.4.2 (1) it was noted that to reduce the conduction loss R_{on} needs to be reduced but as the widths of the transistors is increased significant parasitic capacitance associated with the transistor's C_{GS} would increase, as will switching loss. Therefore from the switching loss perspective the switching transistor should not be too large. There will be an optimal solution as Cgs increases CV^2f goes infinite and I^2 R goes to zero and vice verse. Equation (3.12) presents that to reduce switching loss along with W and L the gate to source voltage and also the frequency need to be reduced. For switching transistor, minimum allowed L is used and the optimization of this W and f_s are discussed in detail in later section. Figure 3.9 present the plot power with respect to width and frequency for the switches.

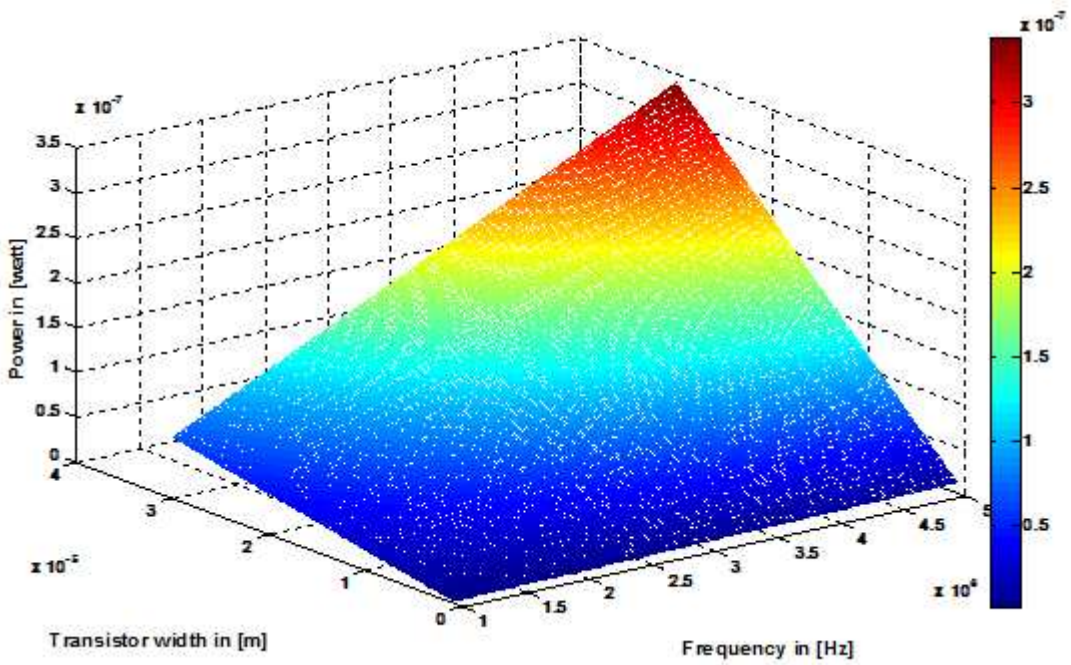


Figure 3.10 Power loss only due to switching loss for CG 1/2 configuration.

3) Redistribution loss: Redistribution loss occurs due to the fact that energy is lost when two capacitors with different voltage are connected together. To quantify the lost energy, we start with Kirchhoff's current law (KCL) that states "The principle of conservation of electric charge implies that: At any node (junction) in an electrical circuit, the sum of currents flowing into that node is equal to the sum of currents flowing out of that node." While applying this law to a system of capacitors connected to a single node it can be stated that in a system of capacitors, the sum of all charges leaving a node in any instance of charge transfer is equal to zero. To demonstrate this in simple form two capacitors (C_1 and C_2) are considered which are initially charged to voltage V_1 and V_2. These two capacitors are then connected together in parallel hence after charge distribution, the combined capacitor voltage becomes V_O. Where V_O can be written as

$$V_O = \frac{C_1 V_1 + C_2 V_2}{C_1 + C_2} \tag{3.13}$$

So the energy loss due to redistribution is

$$
\begin{aligned}
E_{loss} &= \frac{1}{2}(C_1 V_1^2 + C_2 V_2^2) - \frac{1}{2}(C_1 + C_2) V_o^2 \\
&= \frac{1}{2}(C_1 V_1^2 + C_2 V_2^2) - \frac{1}{2}(C_1 + C_2)\left(\frac{C_1 V_1 - C_2 V_2}{C_1 + C_2}\right) \\
&= \frac{1}{2}\left[\frac{C_1 C_2 (V_1 + V_2)^2}{C_1 + C_2}\right]
\end{aligned}
\tag{3.14}
$$

Figure 3.11 demonstrate redistribution loss calculations applied to SC voltage doubler. In a SC voltage doubler, C_P is charged to V_{in} during charge phase and at the beginning of discharge phase it is connected to the output node. Charge transfer occurs between C_P and C_{out}; therefore applying

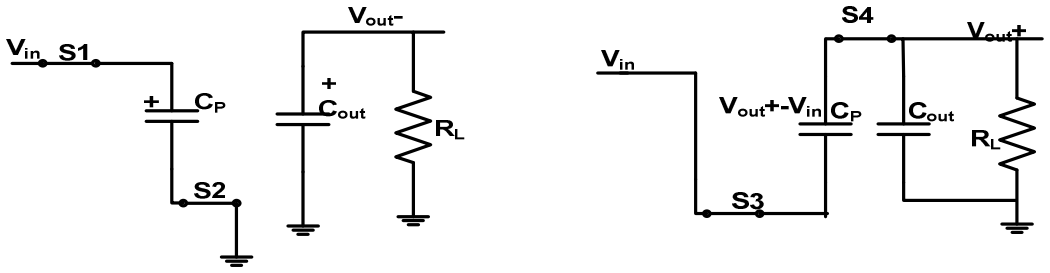


Figure 3.11 Charge states before and after the charge redistribution between C_P and C_{out} .

KCL for the capacitor node at the output gives.

$$
C_p V_{in} + C_{out} V_{out}^- = C_P (V_{out}^+ - V_{in}) + C_{out} V_{out}^+ \tag{3.15}
$$

Here V_{out}^- and V_{out}^+ are the voltage across C_{out} before and after the charge transfer. As $C_{out} >> C_P$ we can have

$$
C_{out} (V_{out}^+ - V_{out}^-) = I_L T \tag{3.16}
$$

Solving from equation (3.15) and (3.16) gives us

$$V_{out}^{+} = 2V_{in} - \frac{I_L}{C_P f_S} \tag{3.17}$$

$$V_{out}^{-} = 2V_{in} - \frac{I_L}{C_P f_S} - \frac{I_L}{C_{out} f_S} \tag{3.18}$$

Therefore, the distribution loss per cycle is

$$P_{loss} / f_S = \frac{1}{2}\left(C_P V_{in}^2 + C_{out} V_{out}^{-2} - C_P \left(V_{out}^{+} - V_{out}^{-}\right)^2 - C_{out} V_{out}^{+2}\right) \tag{3.19}$$

From (3.19) it can be concluded that the redistribution power loss depends on the switching frequency f_S, pumping capacitor C_P and decoupling capacitor C_{out}.

4) Reversion loss: Reversion loss is a form of redistribution loss where charge is transferred from the output capacitor C_{out} to power stage capacitors if proper attention is not paid to the timing of closing and opening operation of the switches. In order to avoid any reversion loss from taking place. A non overlapping clock is used to control the charge and discharge phase on, off operation of the switches.

5) Bottom-plate parasitic capacitors loss : The pumping capacitor C_P will always have parasitic capacitance associated with the top and bottom plate. For MIM capacitor as in this case the bottom plate parasitic capacitor are formed between the bottom plate and the substrate. While for N-well MOS capacitor this is due to the reverse bias diode junction capacitor formed between N-well and P substrate. The power loss due to the bottom plate capacitor arises as the bottom plate capacitors are being charged and discharged every cycle as shown in figure 3.12.

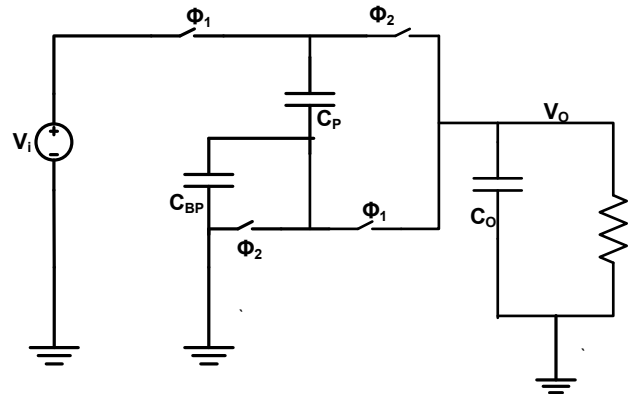


Figure 3.12 A 2:1 SC converter with bottom plate parasitic capacitor.

This component of power loss scales with the value of C_P and can be expressed as $C_{BP} = \alpha C_P$ where α is a technology dependent parameter and can be as high as 20% for on on-chip CMOS process, typical MOS cap behavior, for the IBM 180nm process it is 1%.

$$P_{BP\,loss} = \alpha C_P V_{out}^2 f_S \tag{3.20}$$

From (3.20) bottom plate power loss is dependent on output voltage $V_{out,}$ switching frequency f_S and process parameter α. For good converter efficiency bottom plate parasitic effect need to be reduced.

3.4.3 Output Voltage Ripple

From section 3.4.1 we know the SC power stages operate in two phases charge and discharge transfer phase. If the switch resistance is considered to be negligible compared to load impedance, then the charge transfer time from C_P to C_{OUT} during the discharge phase is much smaller than total discharge time, Also as $C_{out} >> C_P$, the voltage ripple at the output is given by

$$\Delta V = V_{out}^{+} - V_{out}^{-} = \frac{I_L}{f_S C_{out}} \tag{3.21}$$

From (3.21) we see output ripple voltage is dependent on the load current and can be reduced by increasing the C_{out} and the switching frequency. The negative effect of the above action are i) increasing C_{out} would increases area hence increase the converter foot print and cost. ii) increasing

f_s would increase the power loss due to switching and bottom plate loss as discussed in section 3.4.2 . Switching frequency will be determined by optimizing the frequency in conjunction with the width of the switches for minimum power loss in section 3.8. Then output capacitor C_{out} is chosen to ensure desired ripple for the specified load.

3.4.4 Number of capacitor

The SC converter power stage consists of switches and capacitors. Converting gain CG of the converter depends on configuration of the power stage during charge and discharge phase. Different CG requires different numbers of switches and capacitors; efficiency of input voltage range and the output ripple can be improved by having more CG configuration and having inter - leaving technique. But it would require more switches and capacitor so we need to trade of better performance with area and power. As there are multiple configurations by which one can achieve the same CG and from prior discussion in section 3.4.2 it is known the number of switches and capacitors directly contribute to the efficiency, converter area and cost. Hence careful attention needs to be paid to this issue and try to keep them at minimum.

3.5 Step-down voltage conversion using Switch capacitor DC-DC conversion.

In the step-down SC converter, the pumping capacitors C_P are placed between the input and the output during charge phase whereas for step-up SC converter, the pumping capacitors are placed between the input and the ground. During the discharge phase or transferring charge to the output decoupling capacitor, the pumping capacitors are placed in parallel with the output filtering capacitor C_{out} for step-down SC converters, whereas in case of step-up conversion the pumping capacitors are placed in series with the input node and the output filtering capacitor. The number of capacitor and switches in SC converter power stage determines the number of CGs it can provide[75] . Having higher number of capacitors provides more CGs which help to achieve greater efficiency and a larger input voltage range; however, this increases system complexity along with added area of the converter. In this work a reconfigurable topology which uses only two pumping capacitors is implemented. This topology can provide CGs of 1/3, 1/2 and 2/3; the

configuration of switches and capacitors for these CGs are discussed in detail in the next section. This topology is chosen as it has better current delivery performance, less bottom plate parasitic loss and also uses fewer capacitors. The present topology and the regular topology that is normally used are presented in figure 3.13 a and b

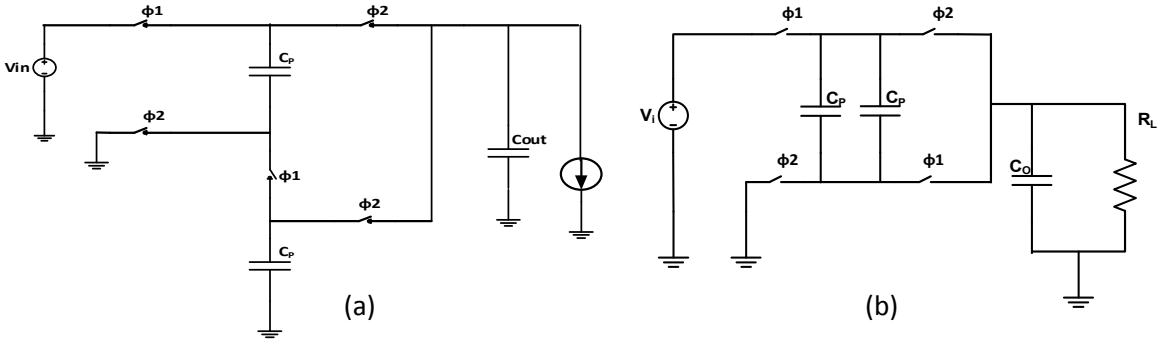


Figure 3.13a)regular series parallel topology for CG. 1/2 b)improved series parallel topology for CG 1/2.

Figure 3.13 a) and b) present two version of the CG 1/2 implementation, the first one is the regular implementation and the second is an improved version. In version a) lets consider CG 1/2 supply a load voltage of $V_{out} = V_{in}/2 - \Delta V$ where $V_{in}/2$ is the no load voltage and ΔV is the difference between no load and load voltage. In phase ϕ_1 the two pumping capacitor C_P both are charged to $V_{in}/2$. In phase ϕ_2 both the C_Ps discharge down to V_{out} by transferring charges to the load capacitor which is much larger than C_P. Therefore during charge when they are again connected in series the energy extracted from the V_{in} source is

$$E_{in} = C_P V_{in} \Delta V \tag{3.21}$$

During phase ϕ_2 the charge extracted from V_{in} is transferred to the load which is at a voltage V_{out}. Hence the energy delivered to load per cycle is a linear scaled version of the energy extracted during ϕ_1 and is given by

$$E_{out} = E_{in} \frac{V_{in}/2 - \Delta V}{V_{in}/2} = 2C_P V_{out} \Delta V \tag{3.22}$$

Therefore the power delivered to the load in each cycle is

$$P_{out} = E_{out} f_S = 2C_P V_{out} \Delta V f_S \tag{3.23}$$

In version b) of the CG 1/2 implementation during phase ϕ_2 the $2C_P$ pumping capacitor transfers charge to the load capacitor C_{out} and discharges to voltage V_{out}. During phase ϕ_1 the pumping capacitors are charged to $V_{in}/2+\Delta V$, thus the energy extracted from source V_{in} during ϕ_1 is given by

$$E_{in} = 4C_P V_{in} \Delta V \tag{3.24}$$

This excess charge extracted from V_{in} during ϕ_1 is transferred to the load capacitor V_{out} during ϕ_2. So the energy delivered to load is a linear scaled version of the energy extracted from V_{in} which is given by

$$E_{out} = E_{in} \frac{V_{in}/2 - \Delta V}{V_{in}/2} = 8C_P V_{out} \Delta V \tag{3.25}$$

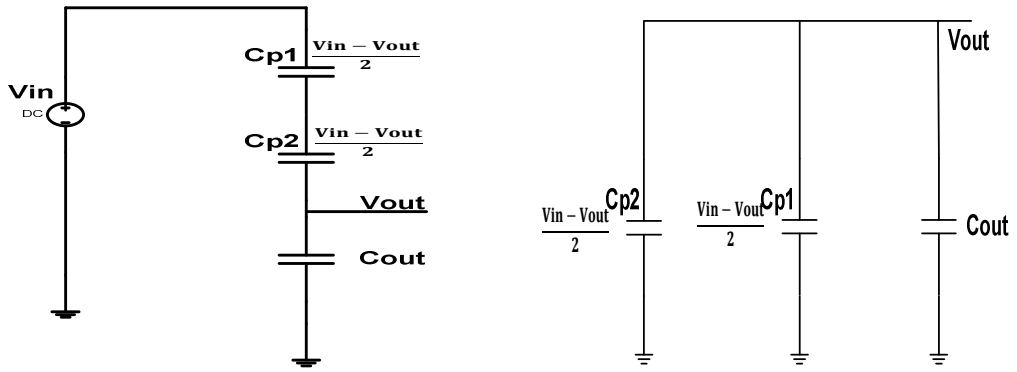
Hence the power delivered to load per cycle is given by

$$P_{out} = E_{out} f_S = 8C_P V_{out} \Delta V f_S \tag{3.26}$$

Comparing (3.23) and (3.26) we see version b) the topology of our choice has 4 times more power delivering capability than version a) for CG 1/2. The other benefit of version b) is the reduced effect of bottom plate capacitor loss. It is seen from (3.26) this topology has 4 times the power delivery capability than the former version but the increase in bottom plate capacitor loss is only twice that of the former. Hence it is concluded that effect of the bottom plate loss is only half than in version a). The most significant difference in implementation of version b) from version a) is inclusion of load capacitor C_{out} in charge transfer process; as a result fewer number of capacitor are required for implementation of a particular CG and also has the benefit of delivering more charge per cycle.

3.5.1 Implementation of different converter gain

Figure 3.13 shows the capacitor configuration for GR=1/3 during the charge phase, figure 3.13, both the pumping capacitor C_{P1} and C_{P2} are connected in series between the input and the output node. This connection charges pumping capacitors to $(V_{in}-V_{out})/2$. During discharge phase C_{P1} and C_{P2} are connected in parallel with C_{out} and V_{out} is calculated as

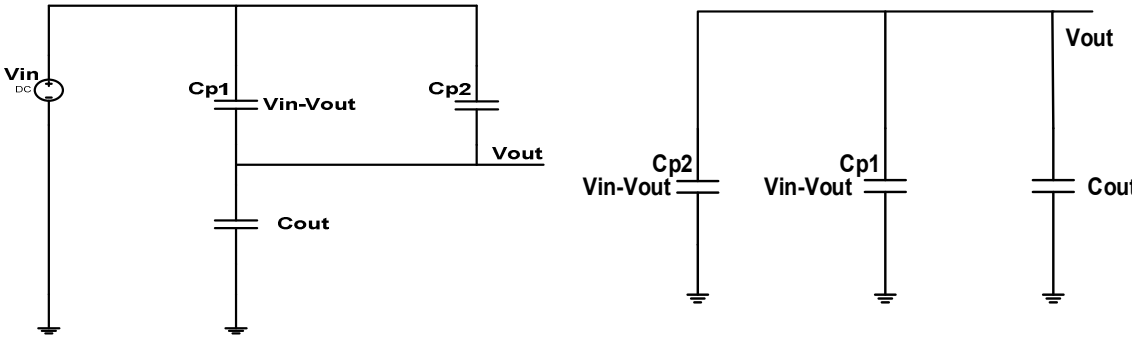


(a) (b)

Figure 3.14 (a) the charge phase(b) the discharge phase capacitor configuration of GR=1/3.

$$V_{out} = \frac{V_{in} - V_{out}}{2} \tag{3.27}$$

$$GR = \frac{V_{out}}{V_{in}} = \frac{1}{3} \tag{3.28}$$



(a) (b)

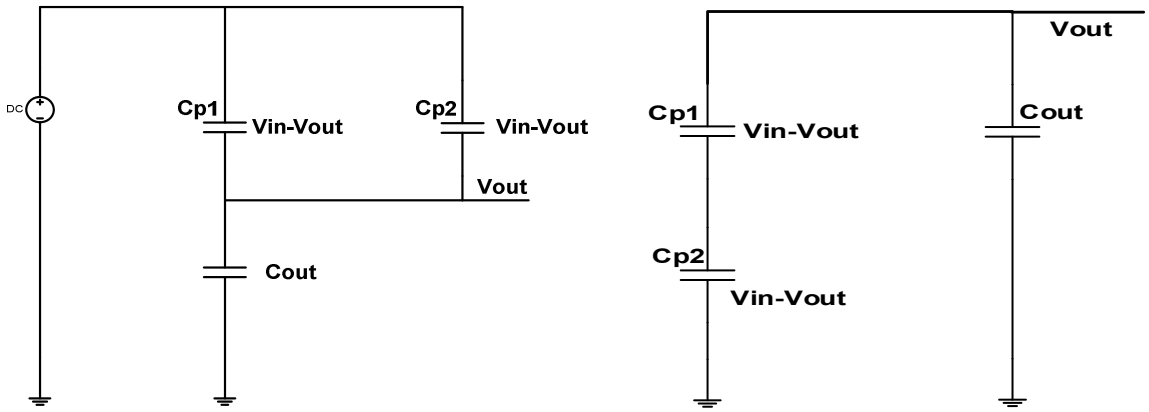
Figure 3.15 (a) the charge phase(b) the discharge phase capacitor configuration of GR=1/2.

Figure 3.14 shows capacitors configuration for GR=1/2. During the charge phase as shown, both pumping capacitors CP1 and CP2 are connected in parallel between the input and the output

node. This connection charges the capacitors to (V_{in}-V_{out}). During discharge phase when C_{P1} and C_{P2} are connected in parallel with C_{out} and then V_{out} is calculated as

$$V_{out} = V_{in} - V_{out} \tag{3.29}$$

$$GR = \frac{V_{out}}{V_{in}} = \frac{1}{2} \tag{3.30}$$



(a) (b)

Figure 3.16 (a) the charge phase(b) the discharge phase capacitor configuration of GR=2/3.

Figure 3.15 shows the capacitor configuration for GR=2/3 during charge phase as in figure both pumping capacitors C_{P1} and C_{P2} are connected in parallel between the input and the output node. This connection charges the capacitors to V_{in}-V_{out}. Then during the discharge phase C_{P1} and C_{P2} are connected in series with other and parallel with C_{out} as in figure 3.15(b) so the V_{out} is calculated as

$$V_{out} = 2 \times (V_{in} - V_{out}) \tag{3.30}$$

$$GR = \frac{V_{out}}{V_{in}} = \frac{2}{3} \tag{3.31}$$

The schematic of the whole reconfigurable power stage with CG of 1/3, 1/2 and 2/3 is presented in Figure 3.16. By systematically turning the switches on/off, all of the above mentioned capacitor configurations can be implemented. CG of 2/3 required seven switches, CG of 1/2 required eight switches and finally CG of 1/3 required seven switches. In the proposed power

stage design, all the CGs have been implemented with total nine switches, two pumping capacitors and a load capacitors C_L.

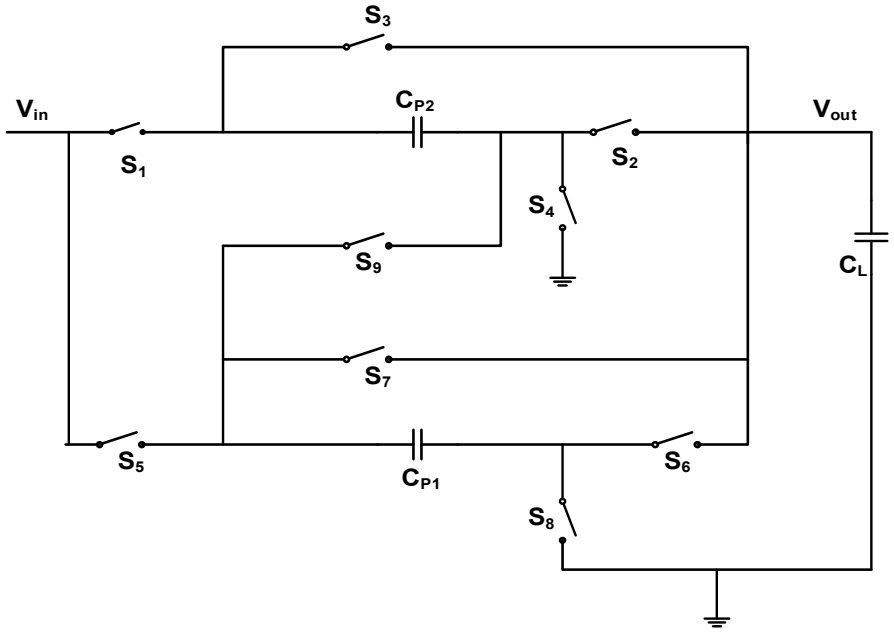
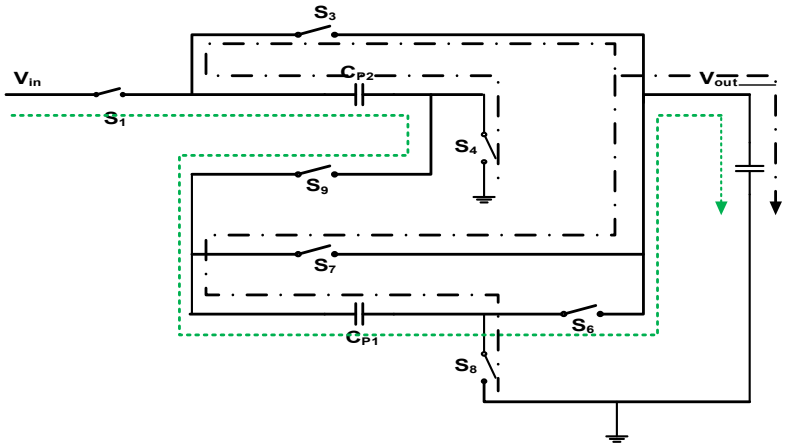
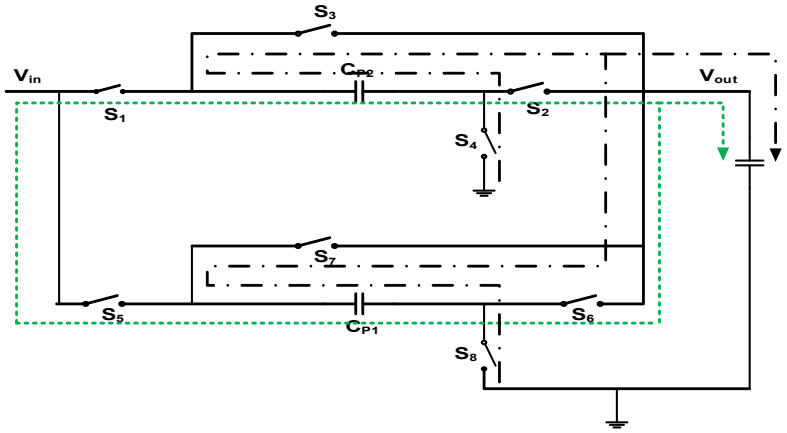


Figure 3.17 Switch capacitor power stage with reconfigurable multiple step-down GRs.

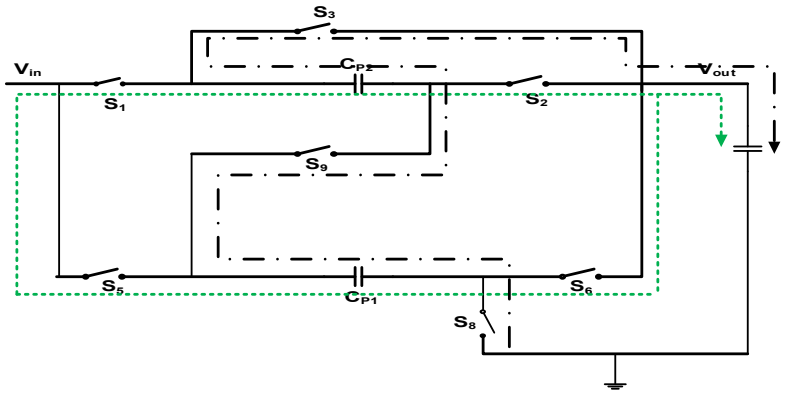
Detail circuit or the switch operations of all the CGs are presented in Figure 3.17. As each cycle is divided in to two phases, charging phase ϕ and discharging phase ϕ! The gate voltage signals to implement all the CGs where ϕ and ϕ! are non-overlapping clock signals is presented in table 3.2.



(a)Converter gain1/3.



(b) Converter gain 1/2.



(c) Converter gain 2/3.

Figure 3.18 Charge and discharge path of the multiple GR with the reconfigurable Sc power stage

Table 3.2 Switch control signal for all the CGs in figure 3.15									
GR	**S_1**	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**S_7**	**S_8**	**S_9**
1/3	ϕ	off	Φ!	ϕ	off	ϕ	Φ!	ϕ	Φ!
1/2	ϕ	ϕ	Φ!	ϕ	ϕ	ϕ	Φ!	ϕ	off
2/3	ϕ	ϕ	Φ!	off	ϕ	ϕ	off	ϕ	ϕ

3.6 Voltage Regulation techniques.

To provide intermediate output voltages different from the available discrete levels available in a SC converter; we can use four different technique

i) Pulse frequency modulation or pulse skipping

ii) Converter gain control

iii) Switch width modulation

iv) Pumping capacitor modulation

3.6.1 Pulse frequency modulation (PFM)

Pulse frequency modulation or pulse skipping is a technique used to regulate the unregulated voltage in a SC converter against the variation in load current or the input voltage. In this technique the pulse width or the frequency of switching the switching array is modulated to control the duration for charging and discharging or how frequently charge is being delivered to the output load. By employing this technique we can control the losses due to switching, bottom-plate and control circuitry loss as all these scale with frequency.

3.6.2 Converter gain control

Since in our case we are harvesting RF power the raw voltage can vary substantially. Hence to maintain good efficiency throughout the input range multiple gains are necessary. From(3.8) efficiency is dependent on CGs, V_{in} and V_{out}. To have good efficiency the CGs should be chosen such that no load output voltage is close as possible to the output voltage desired.

3.6.3. Switch width modulation

This is another way to control regulated voltage. To explain this technique let us consider the switching frequency and value of the pumping capacitor to be fixed. The amount of charge delivered to load in every cycle can be controlled by varying width of the switches. By increasing or decreasing width we are controlling R_{on} resistance and controlling the amount of current follow. But during large changes in load current and input voltage using only this technique, it is

difficult to regulate and also losses such as switching and bottom plate loss do not scale with load current.

3.6.4 Pumping capacitor modulation

Pumping capacitor modulation is another mode of control introduced in [76]. In this technique the regulation is performed by controlling the amount pumping capacitor that is being used to transfer energy per cycle. As the amount of energy transferred is proportional to the amount of pumping cap so it can be used to regulate V_{out} with varying load or input put voltage. The advantage of this technique is that size of the switches can be scaled with the amount of pumping capacitor so both bottom plate loss and switching loss can be scaled, but the disadvantage it would require a large array of switches increasing complexity to switching control.

3.7 Voltage Control circuit

The techniques that are used to regulate voltage in this present SC converter is a combination of gain and PFM. Different CGs have different charge transfer capability thus using the reconfigurable feature of the SC converter allow us to regulate and optimize the efficiency. However if only CGs are used to regulate then during the charge transfer phase if more charge is transferred we don't have any mechanism to fine tune this and result in high ripple at $V_{out.}$ In a step down SC converter the CGs is chosen such that minimum no load voltage is above the desired V_{out}. During light load condition, PFM circuit takes effect so pulses are skipped or when they are on their width is modulated to regulate V_{out}. On the other hand, during heavy load when PFM is not able to transfer sufficient energy, the gain control comes in to playand increases the gain by one-step to provide extra energy. This dual mechanism to regulate V_{out} is implemented using the controller circuit, which is explained in detail in the next paragraph.

The controller of the switch converter is a bang bang control or Hysteric control. The output voltage of the converter is maintained within the hysteric band centered about the reference

voltage. The hysteric controller is inexpensive, simple and an easy-to-use architecture. The benefits of hysteretic control are; it offers fast load transient response and eliminates the need for feedback-loop compensation and displays inherently stable performance [77, 78] . Figure 3.18 presents the control circuit block diagram. The reference voltage selected by CPM system acts as reference voltage for the hysteric comparator, which drives the switch that switch on/off the clock signal of the power stage to regulate the output voltage. The comparator has a Hysteresis of 15mV and works at 10.4 MHz that is four times the clocking frequency of the SC converter. If output voltage V_{out} is at or below (V_{ref} -V_{HYS}/2) the output of the hysteretic comparator goes high and Q turns on. This is the power stage on-state and it cause output voltage to increase. When output voltage V_{out} reaches or exceeds (V_{ref} + V_{HYS}/2), the output of hysteretic comparator turns low and then Q turns off. This is the power stage off-state and it causes the output capacitor to bleed and hence V_{out} decrease. This hysteretic method of control keeps output voltage within the hysteresis band around the reference voltage. Once there is voltage variation caused by a load transient, it recovers as quickly as the power filter allows which is determined by the output

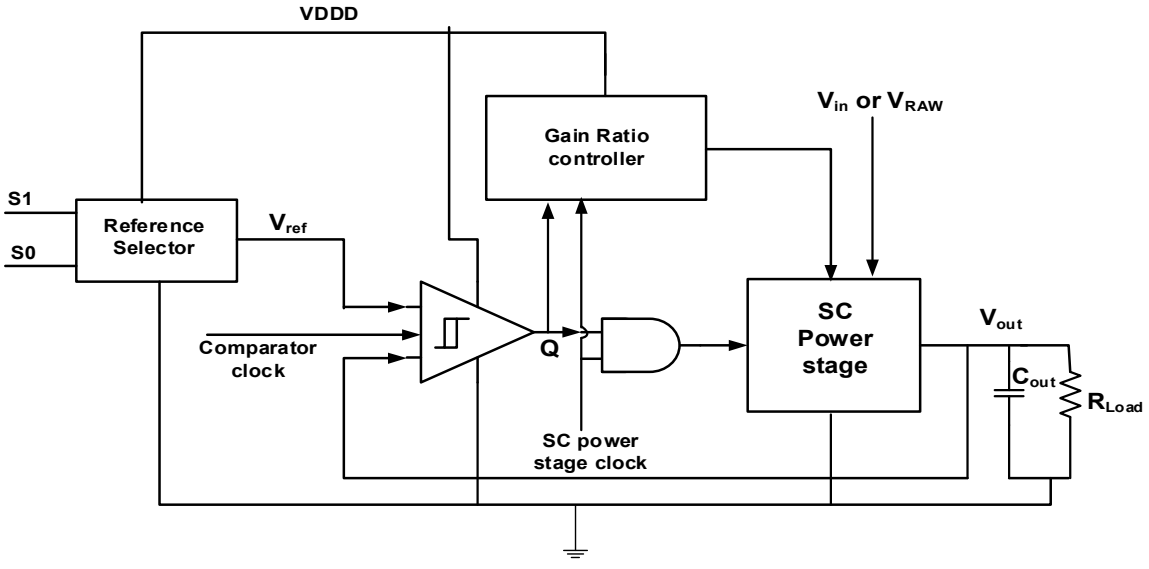


Figure 3.19 Block diagram of the control circuit.

capacitor $C_{out,}$ which has a large value to support large transient current and low output ripple. In addition to its fast transient response, this control scheme provides for simple design without any control loop stability concerns [79, 80].

3.7.1 Controller algorithm

As shown in Figure 3.19 the controller first takes the digital output from the CPM and selects the reference voltage. The SC power stage clock is on and the GR of the converter is 1/3, the output voltage starts rising. In the mean time the comparator continues to compare V_{out} to the V_{ref} as long as $V_{out} < V_{ref}$ the power stage clock is on when $V_{out} > V_{ref}$ the clock is switched off and the load is switched on. During comparison a counter checks the number of cycles taken to reach the steady state that is when the clock is switched off for the first time, if the counter is reaches seven then the GR is increased by one step otherwise as said before the GR is kept same and the clock is switched off and the load is switched on. After the steady state is reached for the first time the comparator checks V_{out}, when it reaches or exceeds ($V_{ref} + V_{HYS}$), the hysteretic comparator turns off the clock. The load current in the mean time bleeds the output capacitor and the V_{out} starts falling, when V_{out} is at or below ($V_{ref} - V_{HYS}$) the clock is again turned on. Once the load switch is turned on in case of $V_{out} < (V_{ref} - V_{HYS})$ for more than four clock cycle the CGs is again increased by one step from its present; if this condition remain an even higher CG is assigned along with maximum pulses. In this way by switching clock signal on/off and by controlling the CGs of the converter, output V_{out} is maintained within the hysteric band

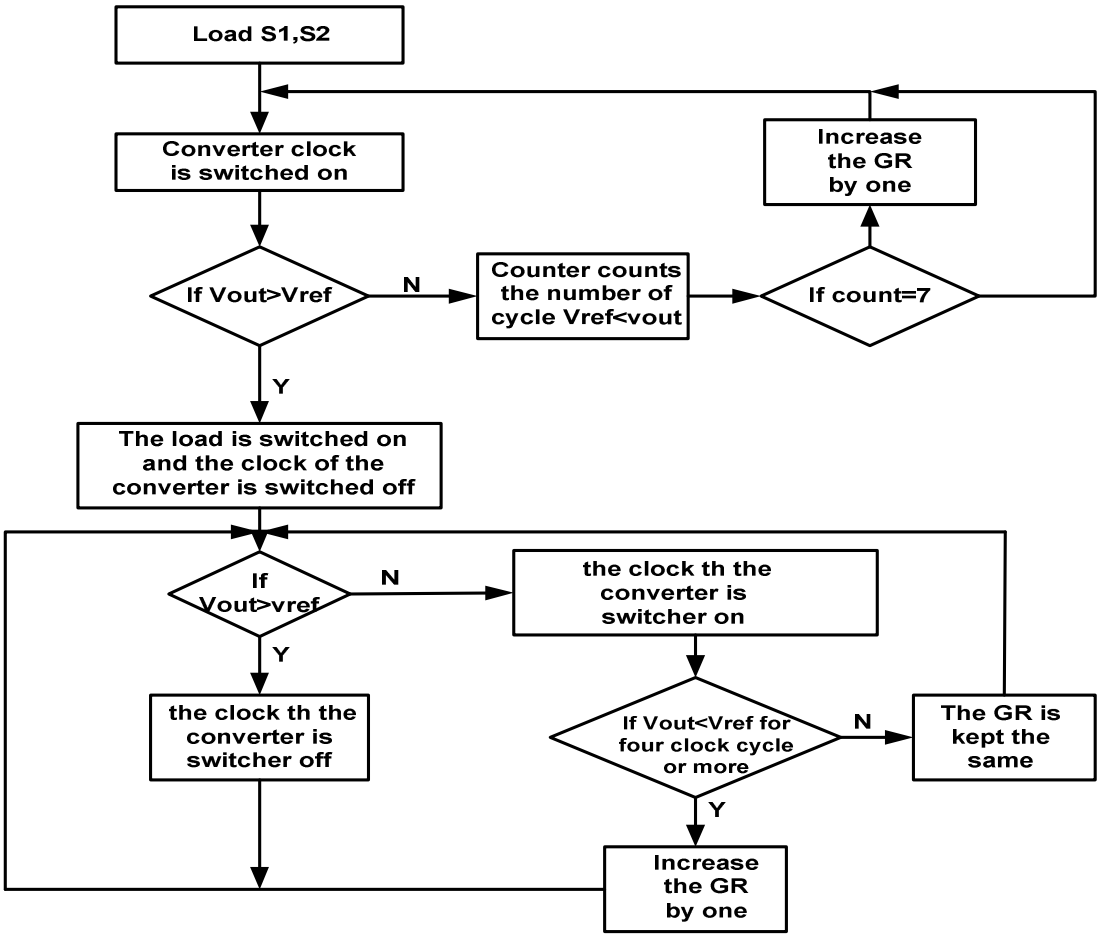


Figure 3.20 Control algorithm of the converter.

CHAPTER IV

POWER LOSS OPTIMIZATION OF A SWITCH CAPACITOR VOLTAGE CONVERTOR

4.1 Optimization of power loss

The Switch capacitor voltage regulator is built with the specification for supplying 6μA while maintaining a supply voltage between 350mV-500mV. The ripple should be less than 10% and the minimum unregulated voltage supply is 900mV. The power loss mechanisms had already been discussed in chapter 3 section 3.3.2. The power losses depends on resistance R_{on} of the switches, gate capacitance of the switches, frequency of switching and the bottom plate parasitic of the pumping capacitor. Maximum power loss is due to the switching loss and conduction loss [73]. To regulate the output voltage pulse frequency modulation and converter gain control technique are used in this SC converter. Therefore to minimize power loss the optimization variables used are switching frequency f_S and switch width W. To demonstrate the process of optimization let's consider the GR 1/2 configuration. This configuration uses eight of the nine switches as shown in figure 3.15(b). As depicted in figure 4.1, let's assume C_P is charged and discharged to V_H and V_L during the charge time t_c and the discharge time t_d, respectively during steady state. τ_c and τ_d are the respective charge and discharge time constant and α, β, γ, δ ,ζ are coefficient for different configuration. The net charge (ΔQ) thus transferred to load is thus given by (4.1) where I_L is the load current

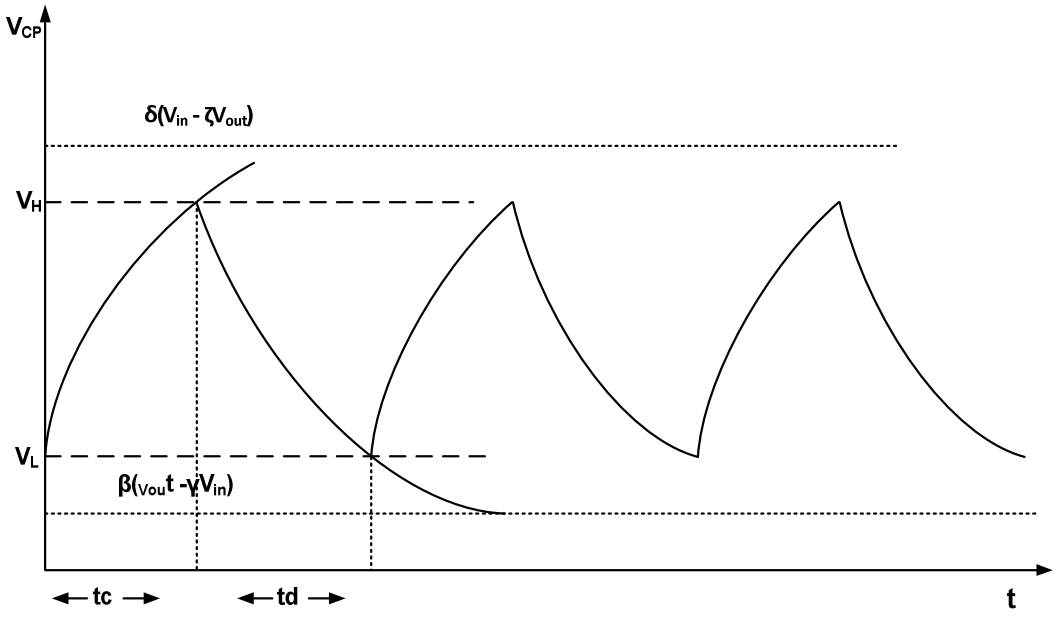


Figure 4.1 Typical voltage wave form observed across pumping capacitor C_P.

$$\Delta Q = C_P\left(V_H - V_L\right) = C_P \Delta V = \alpha I_L t_d \tag{4.1}$$

$$V_L = V_H - \left[V_H - \beta\left(V_{out} - \gamma V_{in}\right)\right]\left(1 - e^{\frac{-t_d}{\tau}}\right) \tag{4.2}$$

$$V_H = V_L + \left[\delta\left(V_{out} - \zeta V_{in}\right) - V_L\right]\left(1 - e^{\frac{-t_d}{\tau}}\right) \tag{4.3}$$

Now adding equation (4.2) from equation (4.3)

$$V_H - V_L\left(\frac{1}{1 - e^{\frac{-t_d}{\tau}}} + \frac{1}{1 - e^{\frac{-t_c}{\tau}}}\right) = \left(V_H - V_L\right) - V_{out}\left(\beta + \delta\zeta\right) + V_{in}\left(\delta + \beta\gamma\right) \tag{4.4}$$

Now replacing $(V_H - V_L)$ with ΔV in equation (4.4) and solving for V_{out} we get

$$V_{out} = V_{in}\left(\frac{\delta+\beta\gamma}{\beta+\delta\zeta}\right)+\frac{\Delta V}{\beta+\delta\zeta}\left(1-\frac{1}{1-e^{\frac{-t_d}{\tau}}}-\frac{1}{1-e^{\frac{-t_c}{\tau}}}\right) \tag{4.5}$$

Thus from equation (4.5) we see that the first term is a constant and the variation is represented by the second term which is.

$$\frac{\Delta V}{\beta+\delta\zeta}\left(1-\frac{1}{1-e^{\frac{-t_d}{\tau}}}-\frac{1}{1-e^{\frac{-t_c}{\tau}}}\right) \tag{4.6}$$

From equation (4.1) and equation (4.6) the variation of V_{out} is

$$\frac{\alpha I_L t_d}{(\beta+\delta\zeta)C_P}\left(1-\frac{1}{1-e^{\frac{-t_d}{\tau}}}-\frac{1}{1-e^{\frac{-t_c}{\tau}}}\right) \tag{4.7}$$

So power loss due to this variation is

$$P_{Vout} = \frac{\alpha I_L^2 t_d}{(\beta+\delta\zeta)C_P}\left(1-\frac{1}{1-e^{\frac{-t_d}{\tau}}}-\frac{1}{1-e^{\frac{-t_c}{\tau}}}\right) \tag{4.8}$$

Table 4.1 Coefficients value for different converter gains

CGs	**α**	**δ**	**ζ**	**β**	**γ**
1/3	1/2	1/2	1	1	0
1/2	1/2	1	1	1	0
2/3	2	1	1	1/2	0

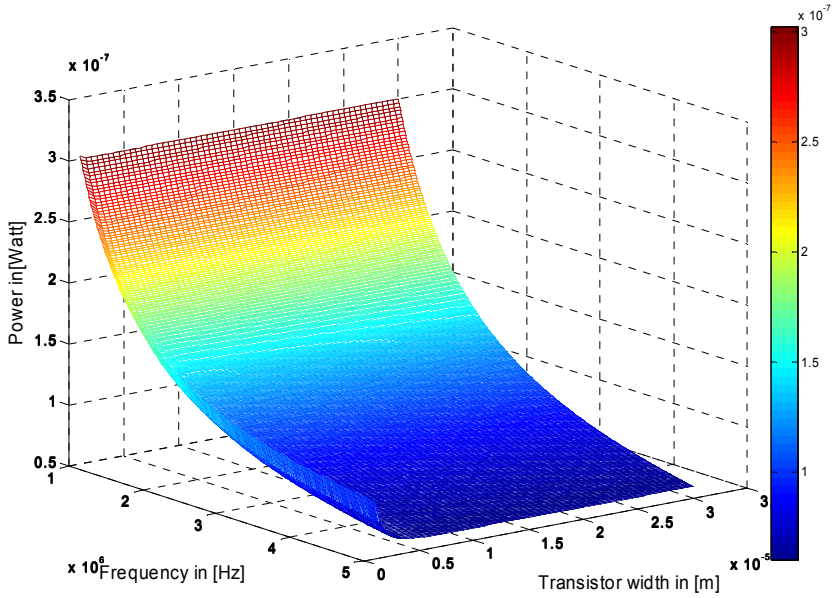


Figure 4.2 Plot for equation 4.13 for CGs ½.

Another major power loss is due to the switching loss as discussed in section 3.4.2 (2) it depend on the size of the switch and frequency thus the total power due to switching is

$$P_{SW} = \sigma f_s C_{OX} \sum_{i=1}^{9} L_i W_i V_{GS(i)}^2 \tag{4.9}$$

Where C_{ox} is the unit oxide capacitance, σ is fabrication process related coefficient and L_i, W_i are the length and width of the i_{th} switch. To reduce the switching power loss we have to reduce the parasitic capacitance so we choose the Length L to be minimum, so the total power loss

$$P_{loss} = \frac{I_L^2 t_d}{(\beta - \delta\zeta)C_P}\left(\frac{1}{1 - e^{\frac{td}{\tau}}} + \frac{1}{1 - e^{\frac{tc}{\tau}}}\right) + \sigma f_s C_{OX} \sum_{i=1}^{9} L_i W_i V_{GS(i)}^2 \tag{4.10}$$

The time constant τ_c and τ_d are dependent on the turn-on resistance in the charge and discharge path where total R_{on} is given by

$$R_{on} = \sum_{j=1}^{M} \frac{L_{min}}{\mu C_{OX} W_j (V_{GS} - V_{th})_j} \tag{4.11}$$

Where M and stands for the total number of power transistor in the charge and discharge path. Equation (4.10) shows that the total power loss is dependent on switching frequency f_s and W_j, therefore one needs to choose W_j and f_s such that least power loss occurs and high efficiency is achieved. Equation (4.10) is used to plot the P_{loss} with respect to W_j and f_s with the help of matlab programming for CG ½ which is shown in figure 4.3.

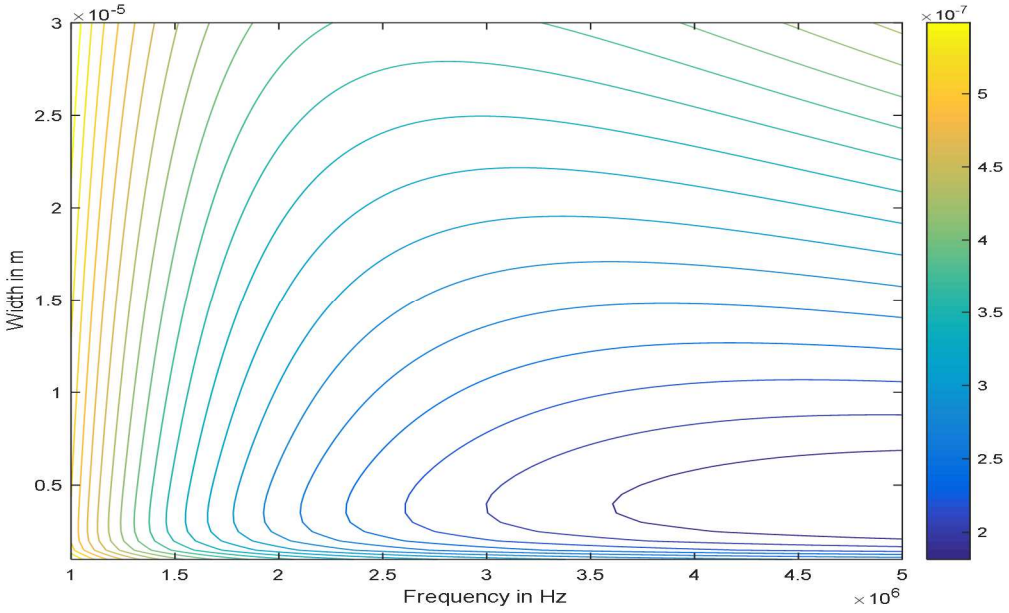


Figure 4.3 Countour plot of equation (4.15) which is total power loss with respect to f_S and width W.

From figure 3.20 f_S is chosen to be 2.56 MHz, as the state machine is operating at 640 KHz and this frequency is available from our PLL. The switch W for minimum power loss is 1.7um. The hysteresis comparator in the controller runs at 10.24MHz. The pumping capacitor is calculated from chapter 3 equation (3.7) for typical V_{in} of 1V and V_{out} equal to 450mV assuming it to be the

nominal V_{out} and I_L equal to 6µA, is 11.53pF but we choose it to be 12pF. The load capacitor or the decoupling capacitor C_L is calculated to be 160pF for ripple of 5% or less.

3.9 Simulation results.

The converter is implemented and simulated with IBM180nm process. All the simulation were completed in cadence spectre with the parasitic extracted netlist. The converter is implemented considering a fully integrated solution to power a state machine working with a near

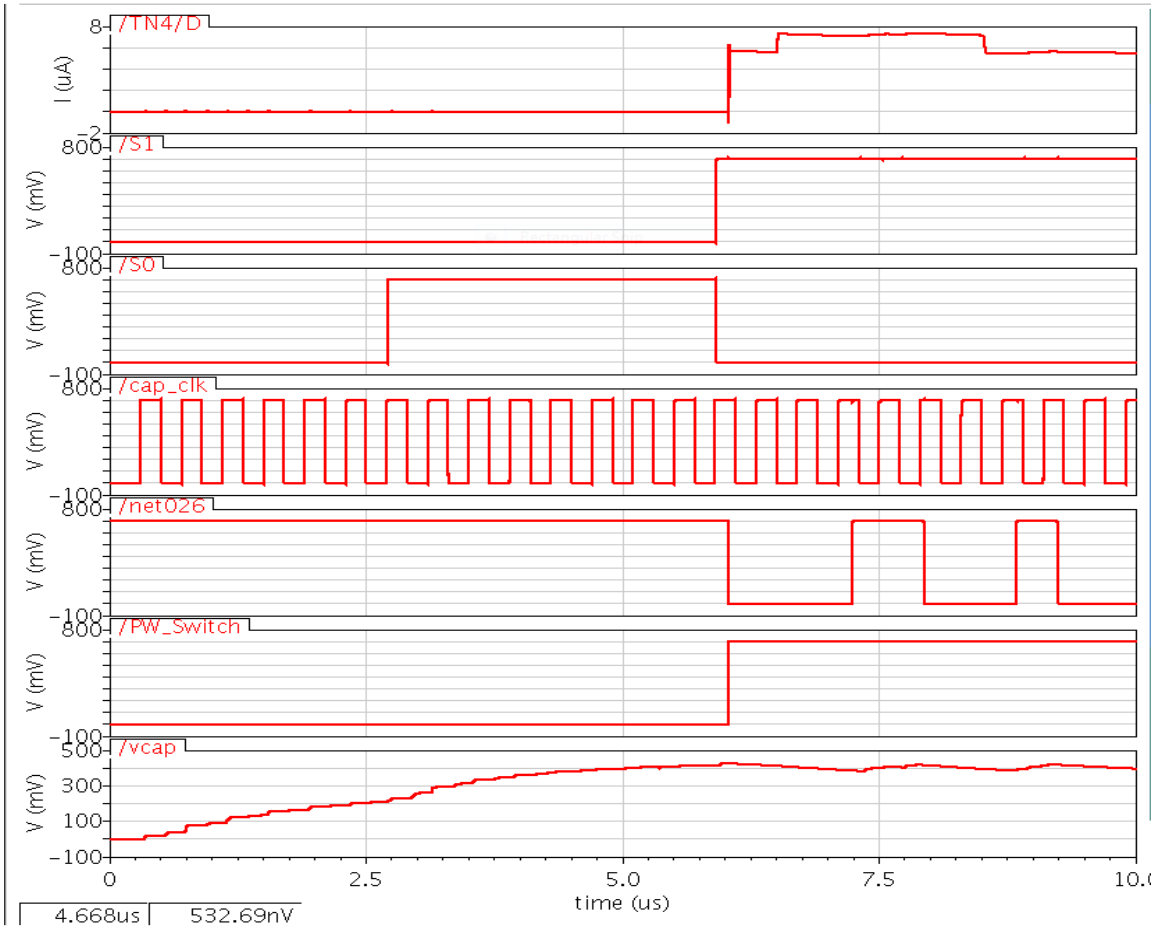
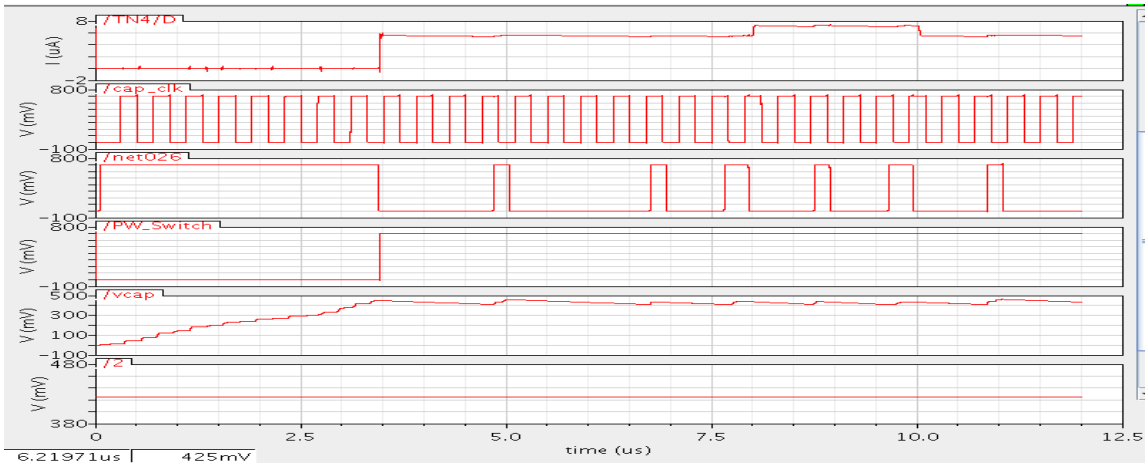


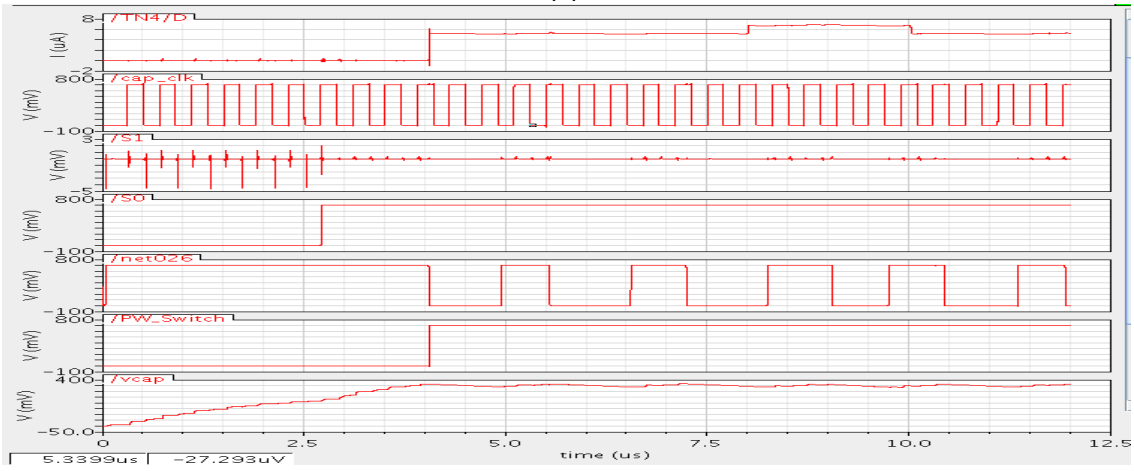
Figure 4.4 Simulation results of the load regulation of the converter.

subthreshold supply voltage with an average load current of 5µA. In this simulation we have constant V_{in} of 900 mV, V_{ref} of 400mVand the load current is first changed from

0µA to 6 µA then increased to 8 µA and then reduced to 6 µA. From the simulation plot in figure 4.4 we see first the gain ratio is changed from 1/3 to 1/2 before the load is switched on. After the load is switched the ripple is +/-10mV and the control is stable and load regulation is good. Figure 4.5a) and b) present the load regulation simulation results for the slow-slow and fast-fast corners respectively. For the slow-slow corner at -20°C the regulated voltage value is 425 mV and and the fast-fast corner at 70°C the regulated



(a)



(b)

Figure 4.5 Simulation results of the a)SS corner b)FF corner load regulation of the converter.

voltage is 350 mV. Simulation results for line regulation are presented in figure 4.6. In this simulation the load is kept constant at 6 µA and the reference voltage is kept the same at 400 mV and the V_{in} is changed from 1.2 V to 900 mV. In this case also first the CG is changed from 1/3 to 1/2 and after that V_{out} is maintained with a ripple of +/-12mV . The highest efficiency achieve is around 86%. Which is quite high compared to the LDO efficiency, which is less than 50%. A picture of the layout of the voltage regulator is presented in figure 4.7.

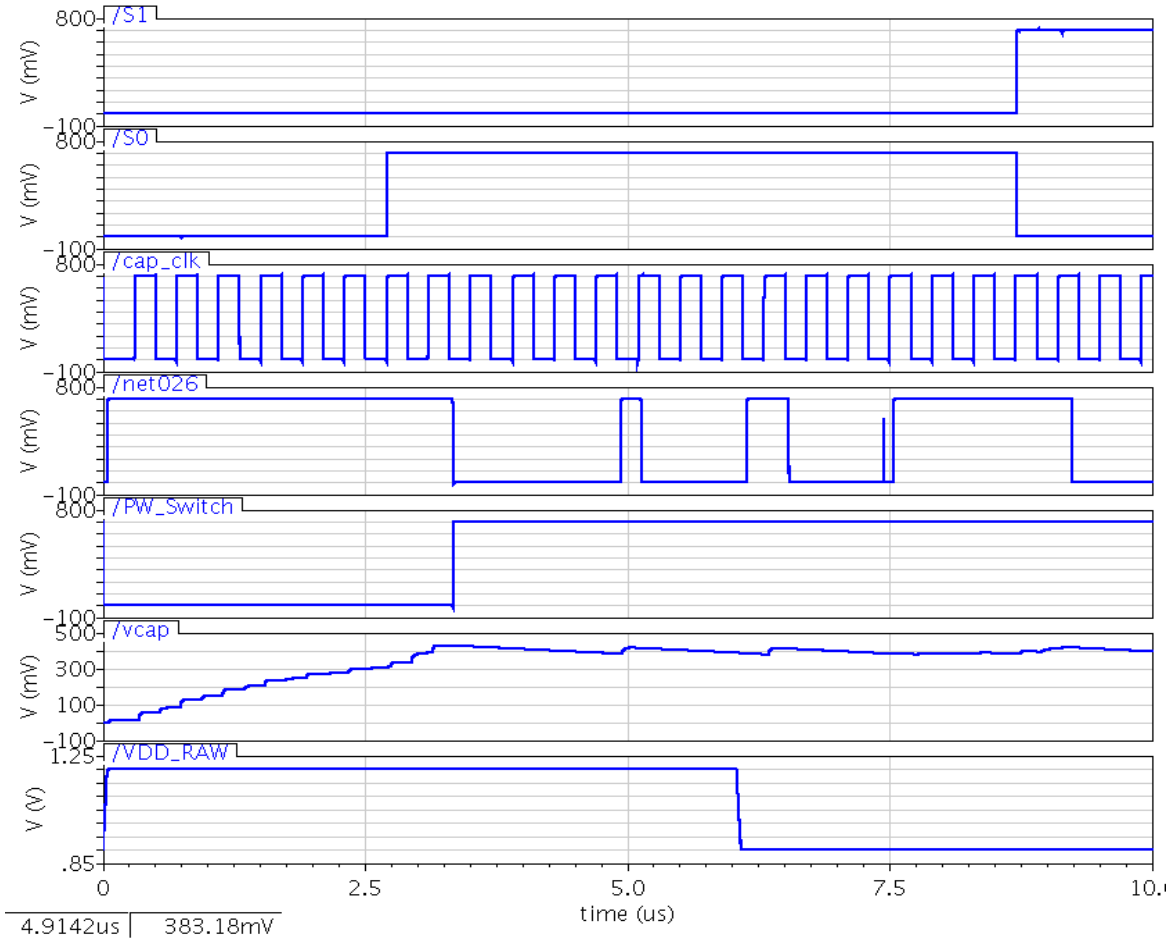


Figure 4.6 Simulation results of the load regulation of the converter.

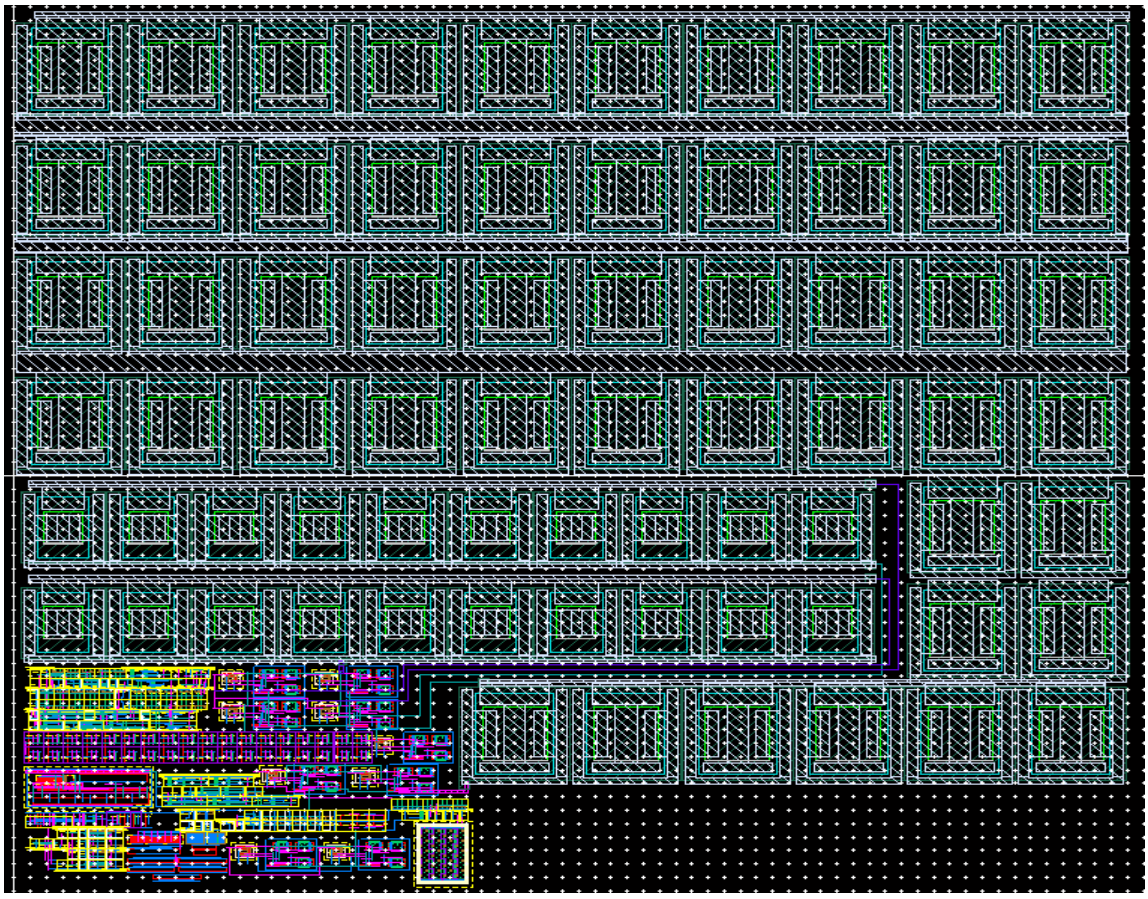


Figure 4.7 Layout of the Switch capacitor voltage regulator.

The layout area of the of the implemented voltage regulator is 350µm X 330µm

CHAPTER V

PHASE LOCK LOOP

5.1 Introduction

The PLL is an important block in most communication system. It is used to synthesize new frequencies from a known reference frequency, recover clock from digital data signal for communication and for performing frequency or phase modulation and demodulation. PLLs are also used to synchronize the input clock for different function blocks on chip to reduce clock skew and timing error. A phase lock loop (PLL) is a feed back control circuit where the phase of the output signal locks or tracks the phase of an input clock signal by the use of its negative feedback path. It responds to both frequency and phase change of input signal by varying the frequency of a controlled oscillator until the output signal matches the input reference in terms of both frequency and phase. The state at which PLL output frequency and input frequency match and both signals are in phase, is referred to as the locked state. After the PLL achieves lock state it continues to compare the two signals to keep them matched in phase and frequency. Note due to non-ideal loop errors or behavior the relative phase relationship is never perfect even though the average frequency can be exact. In its basic form a PLL consists of the following blocks 1) Phase detector or phase frequency detector (PFD) 2) charge pump (CP) 3) lowpass filter (LPF) 4) voltage controlled oscillator (VCO

and 5) an optional Divider/counter, as presented in figure 5.1. The phase detector compares the phase of input or reference signal to the phase of output signal and generates a error signal (phase error) proportional to the phase difference. The charge pump then depending on the error signal either increase or decrease the amount of charge on the low pass filter thereby controlling the input voltage of the VCO (voltage controlled oscillator) thus increasing or decreasing the output frequency respectively. The frequency divider is used in the feedback loop to synthesize a higher frequency from that of the reference frequency

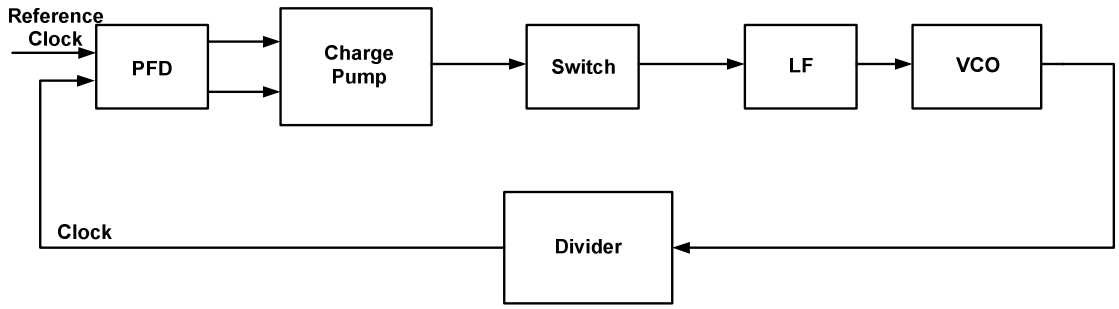


Figure 5.1 Basic PLL block diagram.

From basic feedback control theory the transfer function between the output phase φ_o and the input phase φ_i is given by

$$\frac{\phi_i(s)}{\phi_o(s)} = \frac{G(s)}{1+G(s)} \tag{5.1}$$

Where

$$G(s) = \frac{K_{PDF} K_{LP} K_{VCO}}{s} \tag{5.2}$$

In equation (5.2) K_{PDF} is the PFD gain, K_{LP} is the low pass filter gain and K_{VCO} is the VCO gain. Hence the closed loop equation of the PLL is

$$H(s) = \frac{K_{PDF} K_{LP} K_{VCO}}{s + \frac{K_{PDF} K_{LP} K_{VCO}}{N}} \tag{5.3}$$

Where N is the divide down factor of the VCO output that is fed back to the PFD.

5.2.1 Phase Frequency Detector

The Phase detector used in our case is a simple three state sequential architecture. Advantage of a sequential architecture is, it does not require the reference signal to have a 50% duty cycle and locking does not occur on harmonics resulting in a large hold in range[81]. If there is phase difference between the output and the reference frequency the PFD generates up or down signal, if there is a up signal the charge pump sinks current from the LP (low pass filter) and for down signal the charge pump source current to the LP . The schematic of the PFD is shown in the figure 5.2

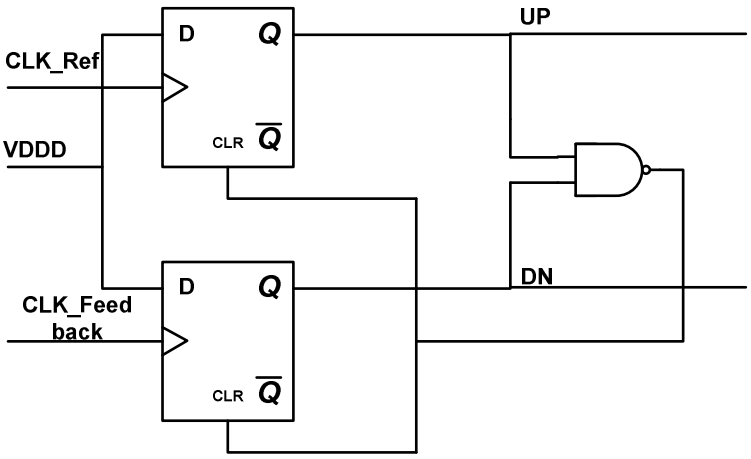


Figure 5.2 Phase frequency detector schematic.

The PFD uses two D flip flops one with the reference signal as the clock input and the other with the feedback signal as the clock input and a feedback NAND (ANDing function) gate to reset the

Dffs. The flip flop are positive edge triggered and the output of the PFD with two Dff are UP and DN signals. These UP and DN signal can have three valid state; the state UP=DN=1 occurs only for very small time, useful in minimizing the dead zone [82]. The three valid states for the two signal with respect to the reference signal and feedback signal are shown in the state diagram presented in figure 5.3. UP signal decrease and the DN signal increases the output frequency respectively . The gain K_{PFD} is given by

$$K_d = \frac{I_{CP}}{2\pi} \tag{5.4}$$

where I_{CP} is the charge pump current.

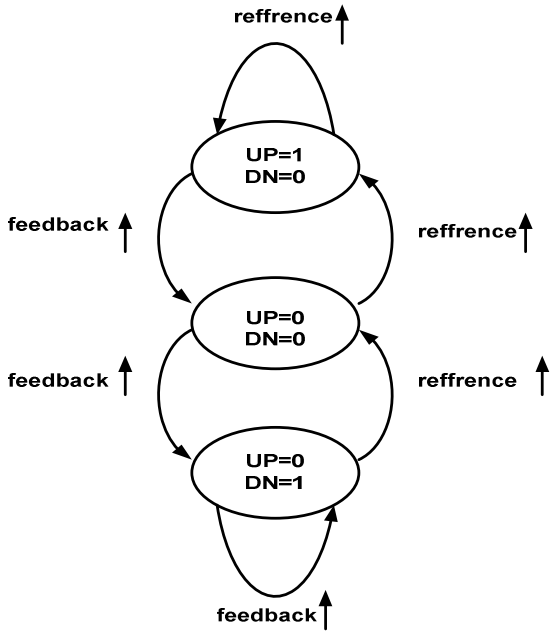


Figure 5.3 Phase frequency detector state diagram.

5.2.2Charge pump

The charge pump is second block of the PLL. The charge pump consist of two switchable current sources which are controlled by UP and DN signals from the PFD. For input UP high, the charge pump sinks current from the loop filter while for input DN high current is sourced to the loopfilter. The charge pump used in this PLL is a zero offset charge pump from Maneatis [83], The zero offset charge pump is essential because in the lock condition the PFD generates narrow UP and DN pulses simultaneously which are desirable to avoiding/minimizing the dead zone. If we do not have these narrow simultaneous UP and DN pulses then when we have a small phase difference where the PFD is unable to generate logical high UP or DN signal failing to switch the charge pump resulting in no corrective action. Because of no corrective action phase error accumulates and the PLL gets out of lock state, until a large enough phase error occurs to turn on the charge pump for corrective action.

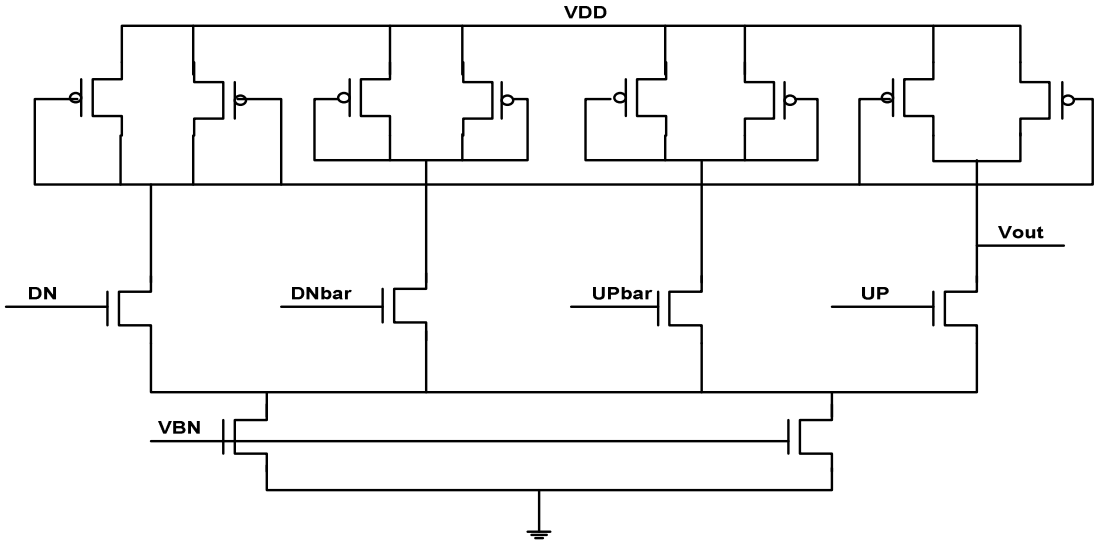


Figure 5.4 Charge Pump Schematic.

To have charge pump of zero static phase offset when in lock condition, the charge pump is constructed from two source coupled NMOS each with separate current source and is connected

with PMOS current mirror of symmetric load as shown in the figure 5.4. The symmetric load element used in the circuit provides a high dynamic supply rejection through a first order cancelation of noise coupling. This charge pump suffers from charge injection and charge sharing issues. An improved version of the charge pump is presented by Ingino [84] which deals with the issue of charge sharing and charge injection along with the balancing of charge. In this charge pump, in lock condition when both UP and DN signal are high the source coupled pair on the left will have the control voltage at the current mirror node while the PMOS in right coupled source will have the same voltage at the gate and drain which is connected to the loop filter through a switch. The PMOS thus sources equal amount of current that is sunk by the source coupled pair as a result the net charge transferred to or from the loop filter is zero so the static phase offset is zero.

5.2.3 Loop filter:

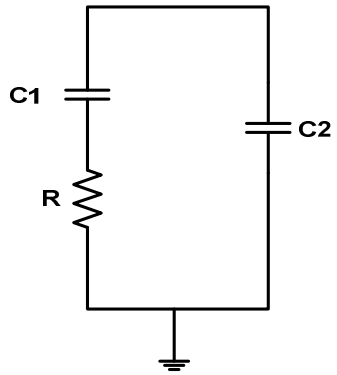


Figure 5.5 Loop filter Schematic.

The charge pump source or sinks current in-to /from the loop filter. The loop filter is a passive low pass filter with two capacitors and a resistor as in figure 5.5. The low pass filter together with the charge pump act as integrator that averages or attenuates the high frequency component of UP

and DN pulses and controls the voltage at the VCO input. The PLL circuit here is a type II PLL that is it has two poles at the origin one from the VCO and the other from the integrator capacitor C_1, which renders the loop to be unstable. To stabilize a resistance R is connected in series with C_1 to provide a stabilizing zero another capacitor C_2 which is one tenth of C_1 is connected in parallel to reduce the ripple of the control voltage V_{ctrl} at the VCO input [85, 86]. The transfer function of LP ignoring C_2 can be written as

$$LP(s) = \left(\frac{1}{C_1 s} (1 + RC_1 s) \right) \tag{5.5}$$

The low pass filter along with the stability and band width also determines the damping factor the detail of which is explained in later section.

5.2.4 Voltage controlled oscillatory VCO:

The voltage controlled oscillator is another important block of PLL, The VCO that we choose is current starved ring oscillator. The advantages with the ring oscillator is that it has a wide tuning range and amenability to integration, it also occupies less area. compared to the LC tank oscillator. The disadvantage of the ring oscillator is that it performance degrades as frequency increases because phase noise or jitter increases [87, 88], The LC tank oscillators have less jitter than ring oscillator for same power and oscillation frequency. The schematic of the current starved VCO is shown in figure 5.6. It operates in a similar manner as a ring oscillator, in this circuit M2 and M3 operate as a inverter while M1a-e and M4a-e act as current sources and control the current available to the inverter. As the M1a-e and M4a-e act as the current/sinks sources and are in saturation also to reduce the VCO 1/f noise contribution they are made of long channel devices. The current in M5 and M6 are equal and set by the control voltage, the current from M5 and M6 is then mirrored to each of the five inverter current source. The frequency of the

oscillator is adjusted with the V_{ctrl}. The slope of frequency versus the control signal plot gives us the voltage to frequency conversion gain K_{VCO}, the transfer function of the VCO is given by

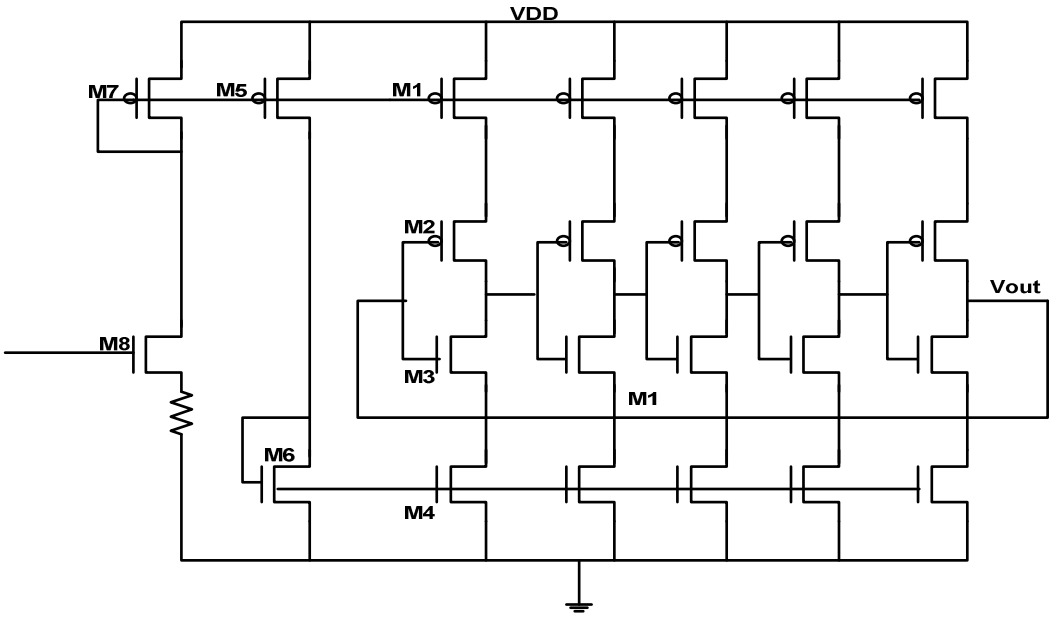


Figure 5.6 Voltage controlled oscillator schematic.

$$\frac{\Diamond_{VCO}}{V_{ctrl}}(s) = \frac{K_{VCO}}{s} \tag{5.6}$$

The design equation for the current starved VCO is as presented.

The total input output capacitance of M2 ,M3 inverter C_{tot} is

$$C_{tot} = \frac{5}{2} C_{ox}\left(W_p L_p + W_n L_n\right) \tag{5.7}$$

The time it takes to charge C_{tot} to V_{sp} from zero

$$t_1 = C_{tot}\frac{V_{sp}}{I_{D1}} \tag{5.8}$$

The time it takes to discharge C_{tot} from V_{dd} to V_{sp}

$$t_2 = C_{tot}\frac{V_{DD} - V_{sp}}{I_{D4}} \tag{5.9}$$

If we consider $I_{D1} = I_{D4} = I_D$ when $V_{DD} = V_{DD}/2$ then adding t_1 and t_2 we get

$$t_1 + t_2 = C_{tot}\frac{V_{DD}}{I_D} \tag{5.10}$$

The oscillatory frequency of the current starved VCO for N (here N = 5)stage is

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{I_D}{N\,C_{tot}V_{DD}} \tag{5.11}$$

Where f_{osc} is the center frequency when $V_{ctrl} = V_{DD}/2$ and current is I_D

If we apply the V_{ctrl} directly to the gate of M5 the current in M5, M6 will be nonlinear. Due to this nonlinearity we will have more jitter and the output of the phase-locked loop may take longer or not lock, because while solving for loop characteristics the K_{VCO} is considered to be constant . To achieve better current linear with respect to the VCO input voltage V_{ctrl} source degeneration is used. The width of M8 is made wide and a source degeneration resistance R is added to the source of M8, figure 5.7 shows the simulated transfer curve of the VCO with the linearization circuit.

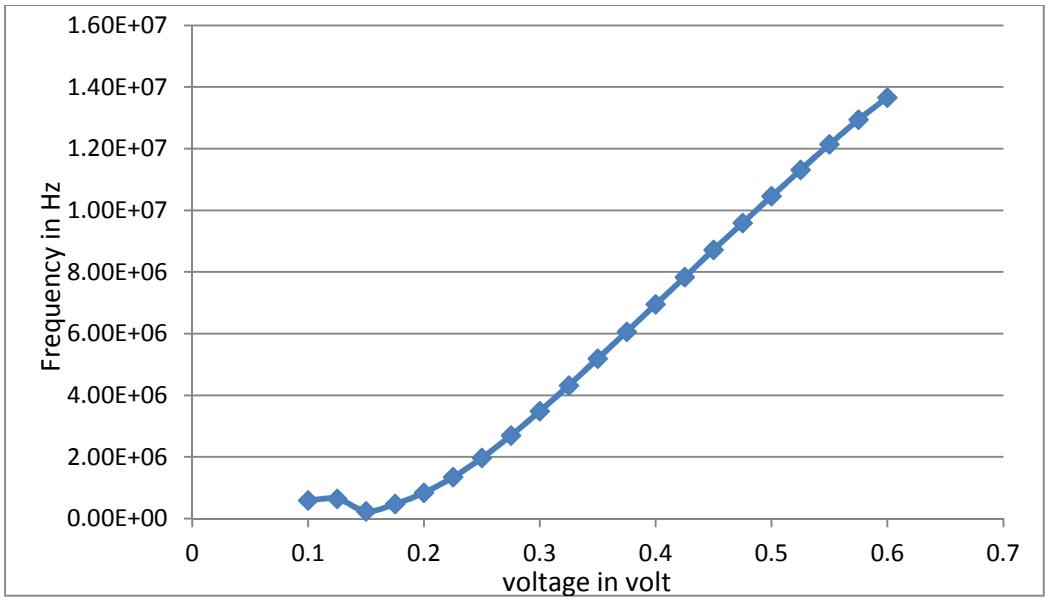


Figure 5.7 Simulated transfer curve of VCO.

The output of the VCO is applied to a frequency divider through a buffer to avoid loading. A 32 bit is applied to the output giving a final output of 160 KHz. our reference frequency.

5.3 Loop characteristics

In the previous section 5.2 we discussed about the different component of a PLL. In this section the dynamic behavior of the entire PLL will be described. The open-loop transfer function of a PLL can be written as

$$H_{open}(s) = K_{PFD} LP(s) \frac{K_{VCO}}{s}$$
$$= \frac{I_{CP}}{2\pi C_1}(1 + RC_1 s)\frac{K_{VCO}}{s^2} \qquad (5.12)$$

The transfer function described in (5.12) two poles at the origin and one compensating zero to stabilize the closed loop. The closed loop transfer function of the PLL is thus given by

$$\frac{\phi_{out}}{\phi_{in}}(s) = \frac{H_{open}(s)}{1 + H_{open}(s).1/N} \tag{5.13}$$

where N is due to the frequency divider at the output of the VCO, now replacing (5.12) in (5.13)

$$\frac{\phi_{out}}{\phi_{in}}(s) = \frac{\frac{I_{CP}K_{VCO}}{2\pi C_1}(RC_1 s + 1)}{s^2 + \frac{I_{CP}K_{VCO}}{2\pi N}Rs + \frac{I_{CP}K_{VCO}}{2\pi C_1 N}} \tag{5.14}$$

The transfer function given by (5.14) is a lowpass filter and hence it rejects input noise frequencies higher than the PLL band width. The natural frequency of the PLL can be written as

$$\omega n = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi C_1 M}} \tag{5.15}$$

and the damping factor of the PLL is given by

$$\zeta = \frac{R}{2}\sqrt{\frac{I_{CP}C_1 K_{VCO}}{2\pi N}} \tag{5.16}$$

Table 5.1 The value of the different parameter

Parameter	**Value**
Center frequency	5.12 MHz (2.012E7radian/s)
Natural frequency ω_n	16KHz
VCO gain K_{VCO}	35.3MHz/V
Charge pump current I_P	150nA
Damping factor ζ	0.9
C_1	16.3pF
R	975.46KΩ
C_2	1.63fF

5.4 Noise Analysis of PLL

As discussed in the introduction section the main objective of the PLL is to generate output clock with minimum timing uncertainty. There are two main factors that contribute to the timing uncertainty in a PLL, first is the mismatch in devices, the second is due to the device noise present in the system. The device mismatch causes static phase shift or skew. The skew is static in nature and is generally less of a problem. Skew in the output-clock can be minimized by having larger device size and using careful layout [89, 90]. The device electronic noise on the other hand causes random phase shift or jitter and is more critical. The device electronic noise of all the blocks in a PLL influence the output of the clock timing but among them VCO contribute the greatest jitter with the possible supply noise or substrate injection. A Different architecture for a VCO like the resonant circuit based exhibits improved noise performance but it consumes more power and is not easy to integrate. In this work we are using ring oscillator, the jitter per stage is

$$t_j = V_n \frac{C_{tot}}{I} = \sqrt{\frac{KT}{C_{tot}}} \frac{C_{tot}}{I} = \frac{1}{I}\sqrt{KTC_{tot}} \tag{5.17}$$

where I is the sourced current and C_{tot} is the total capacitance at input of a single stage. Hajimiri in [91] demonstrated that, jitter of a ring oscillator with a constant frequency decreases as the number of stages increases but again the power would increase. Hence we can see that the jitter due to device electronic noise has inverse an inverse dependence with power consumption. The other factor contributing to PLL jitter is power supply noise. So remedies for a clean PLL are as follows.

I. Larger than Minimum Geometry –↓skew

II. Greater W – Greater I/CoxWL - ↓ jitter

III. Reduced Supply Noise - dedicated supply- ↓ jitter

IV. Decoupling Reduced Droop - ↓ skew

V. Differential VCO

VI. Dedicated PLL supply

5.5 Clock data recovery circuit(CDR)

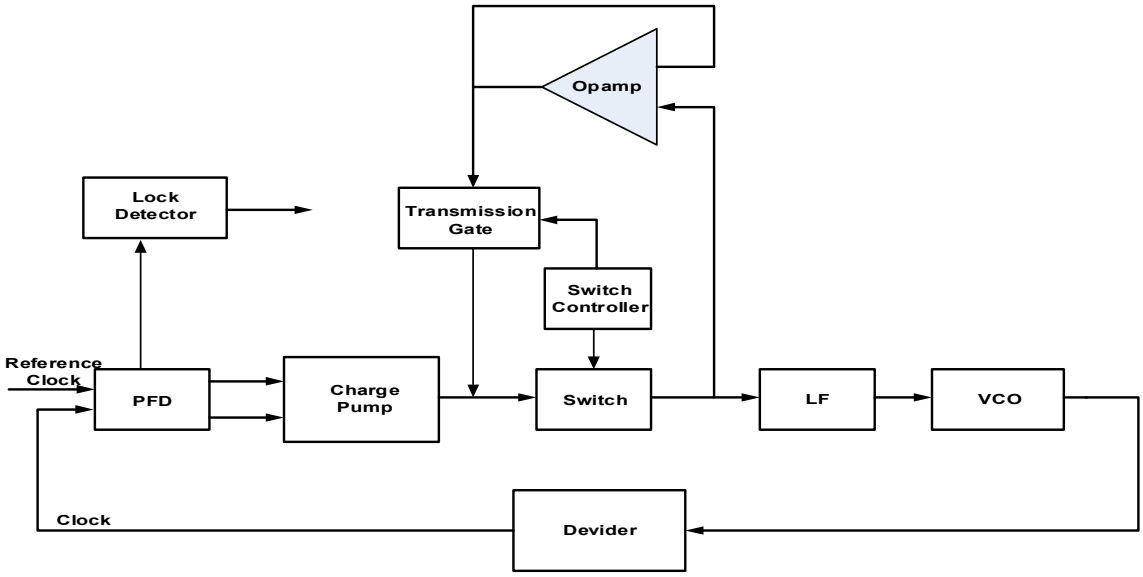


Figure 5.8 Block diagram of the total PLL circuit with the CDR.

The PLL presented in this work is capable of recovering clock form the EPC gen 2 protocol. The block diagram of the PLL of this work is presented in figure 5.8 and the clock data recovery system is being implemented by using switches, an opamp and a controller. The operation of the CDR circuit is explained in next section.

5.5.1 CDR operation

In this case the transmitted and received data follows the EPC gen 2 protocol, the data are pie encoded. At the beginning of each transmission a series of 0's are transmitted from the base station to synchronize the PLL with the reference frequency. Once the PLL achieves lock to the reference frequency; the PLL changes to what we may describe as switch mode to stop the PLL

output from drifting away by attempting to further recover the embedded clock from the data received, to do stop or halt the block transmission gate, Opamp, switch and the controller are used. In switch mode the controller turns the switch on only for rising edges of the data for phase comparison and turns off after half the reference clock period. As the transmission gate is controlled by complimentary signal, when the switch between the charge pump and the low pass filter is off the transmission gate turns on and maintain equal voltage across the switch with the unity gain feedback opamp. This is done to minimize leakage through the switch and maintain the voltage on the loop filter for the interval the switch is off, which prevents the PLL frequency from drifting by maintain a constant voltage at the VCO input. The VCO gain is high so any leakage of charge from or to the loop filter from the charge pump through the switch will force the VCO frequency to drift. In order to minimize the frequency drift we cut off switch between the charge pump and the loop filter we also use minimum geometry device for switch and control the switching device with bootstrap switch circuit [92]. Block diagram of the switch configuration is in figure 5.9.

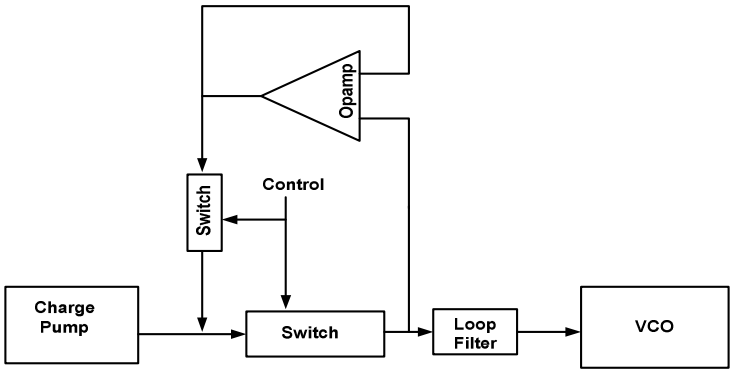


Figure 5.9 Block diagram of switch configuration.

5.6 Lock circuit

The schematic of the lock circuit is shown in figure 5.10. In the lock circuit we are detecting the delayed UP and DN signals with respect to feedback clock and the reference clock respectively with a D flip flop. The output of the flip flops are given as input to the NOR gate. when both the UP and DN signal are low at the rising edge of the feedback and reference frequency clock the out of the NOR gate is high and we start counting for eight reference clock pulses as long as the NOR output is high. After eight counts a lock signal is generated, an eight count is used to avoid a false lock signal.

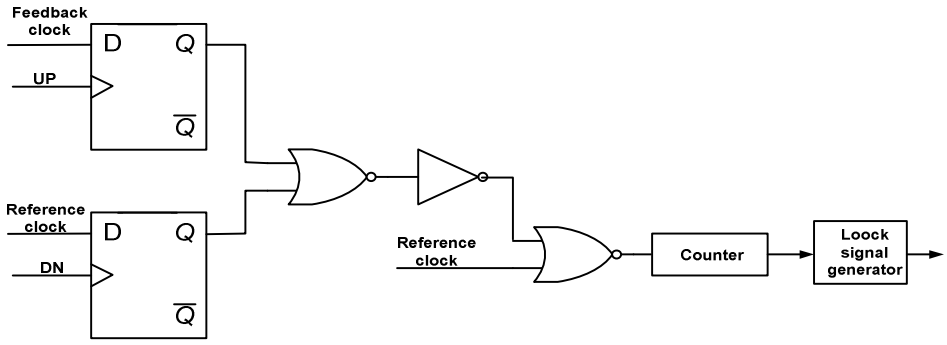


Figure 5.10 Block diagram of the Lock detection circuit.

5.7 Results

The PLL is implemented fabricated in the IBM 180 nm process. Simulation and measurement of the PLL is discussed below. The PLL is designed to have 160KHz as reference , recover clock from the data received and have a lock time of 160µs. Figure 5.11 is the montecarlo simulation of the lock time and frequency deviation of 25 samples. The number Monte Carlo runs were limited by the fact that it takes 5hr per run. The figure shows the mean lock time is 153.134uS which is very close to our design and the deviation is 16.926uS which can be tolerate.

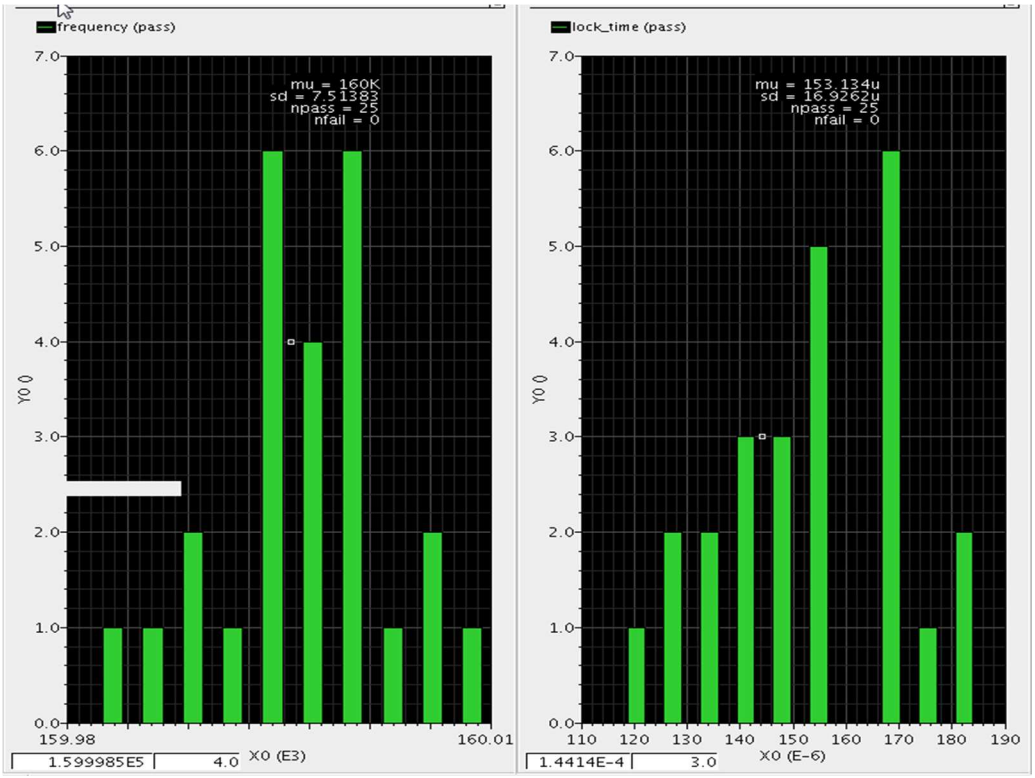


Figure 5.11 Monte Carlo simulation for the lock time and the frequency deviation.

Figure 5.12 show the simulation and measured results where the reference consist of a160KHz reference frequency and no data. This measurement was completed to get the data for the locking time and jitter under different supply voltage condition, with supply voltage of 680mV, 700mV and 720mV respectively, the jitter results are shown in table 5.1. In the second case the reference consist of regular reference frequency followed by the pie encoded data as can be seen in Figure 5.13; where the header consist 168.75µS of regular frequency followed by data consisting of seven "1" and three "0". While data is feed as the reference to the

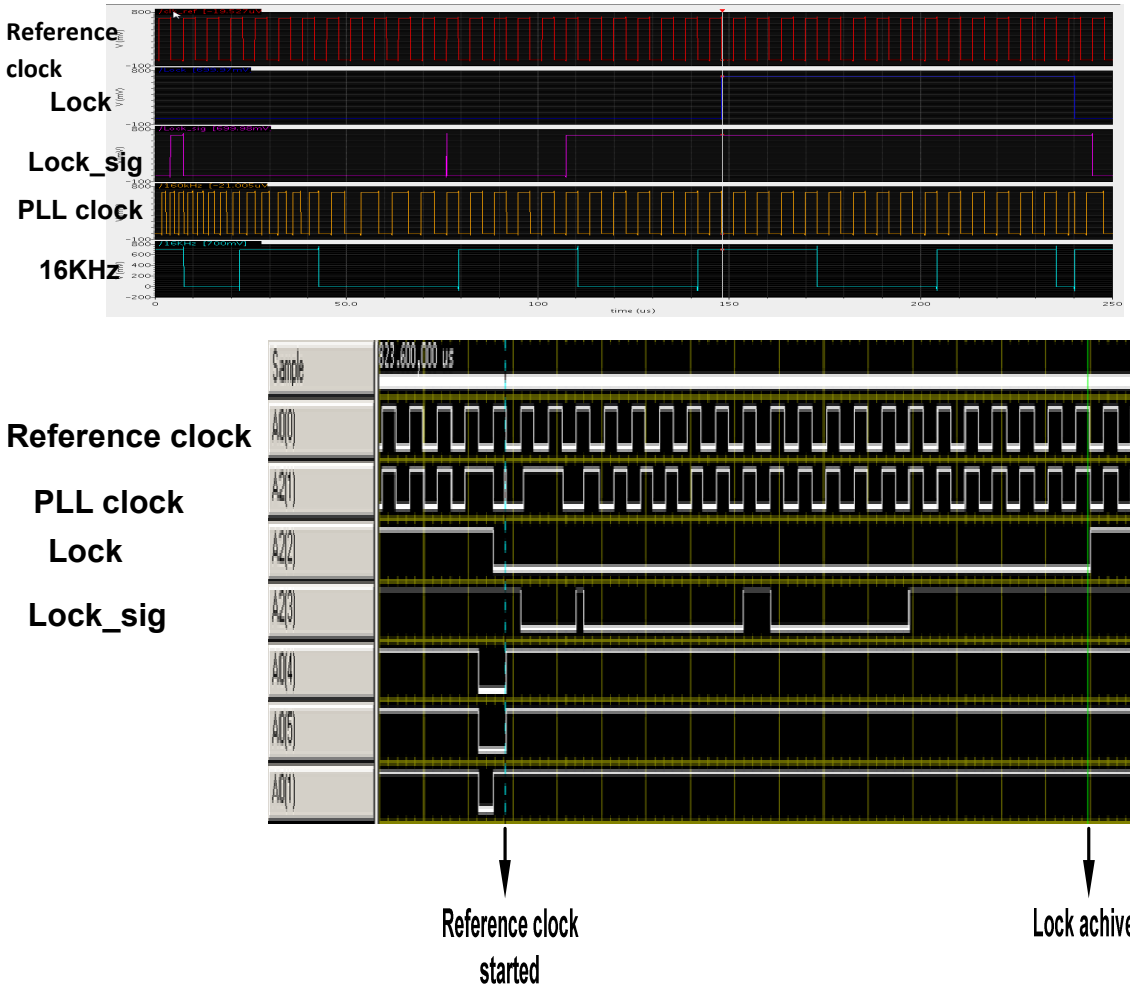


Figure 5.12 PLL transient simulation and measurement with reference clock only and no data.

the PFD from the simulation and measured plots we are able to recover the embedded clock from the received data and the PLL output remains stable or a 'drifting' free. The PLL recovers the clock from data.

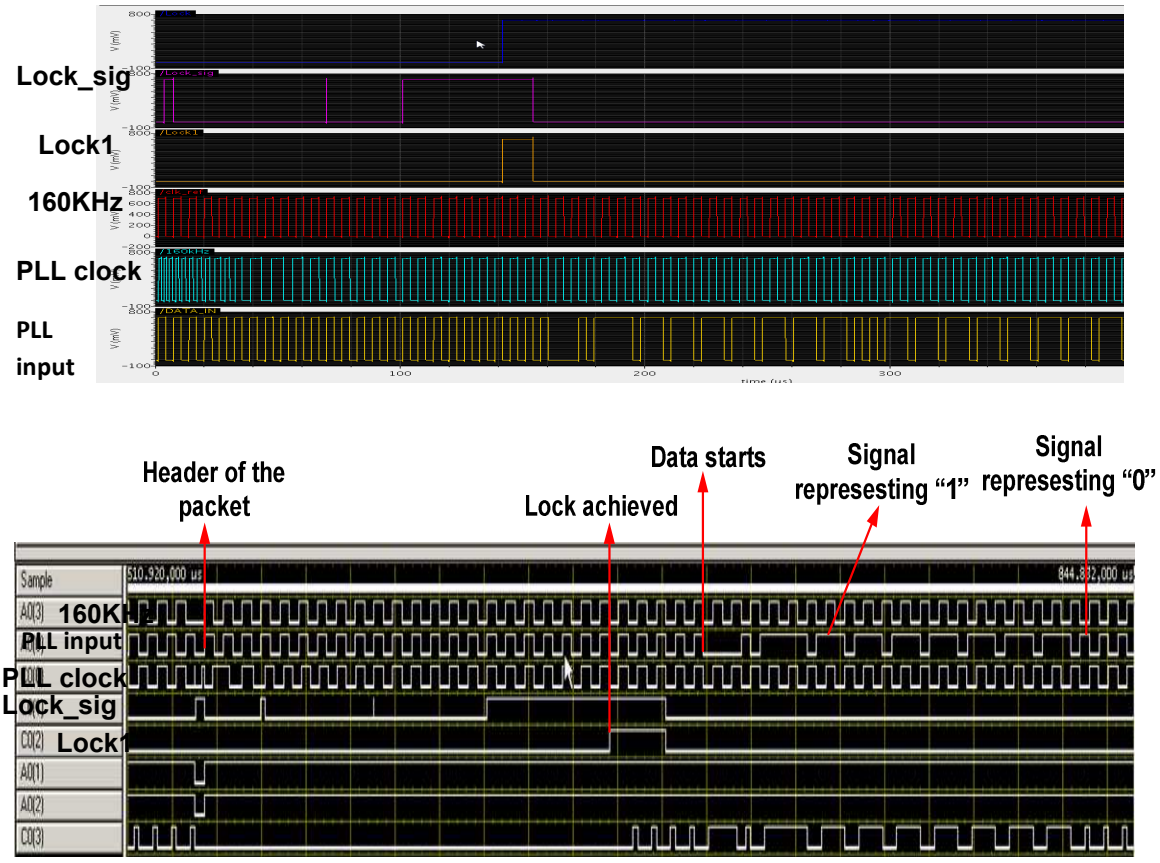


Figure 5.13 PLL transient simulation and measurement with reference clock header and then data.

The measurement of the Locking time was completed with supply voltages of 680mV, 700mV and 720mV respectively. First with the supply voltage continuously on while the reference frequency clock was stopped after 250µs and repeated again. For the second case the reference was clock was kept continuously on but the supply voltage was switched on and off at a interval of 250µs. During all of the above setting the measured lock time was within the 3σ simulation value. The jitter figures given in table 5.2 are all less than required by the digital controller to safely recover data by a factor of 36.

Table 5.2 MEASURED JITTER

Die No.	1	2	3	4	5	6	7	Average
Jitter(nsec)	20.84	19.29	20.35	21.66	36.3	22.45	21.1	23.14

Table 5.3 presents the measured power consumption of the PLL and the maximum power it consumes is 3.1µW which is less power compared to previous works [93, 94].

Table 5.3 MEASURED PLL POWER CONSUMPTION

Die No.	1	2	3	4	5	6	7	8	9	10	Average
Power (µW)	3	2.9	2.7	3.1	2.8	2.9	3.1	3	2.8	2.7	2.9

Measured lock time is presented in Table 5.4 and it is seen that the lock time of the PLL is smaller than the target lock time of 150µs.

Table 5.4 MEASURED PLL LOCK TIME

Die No.	1	2	3	4	5	6	7	8	9	10	Average
Lock time (µsec)	131	125	131	131	113	138	119	125	132	119	126.4

5.8 Conclusion

The PLL implemented for this present work is type II PLL with a output frequency of 5.12MHz. The PLL is implemented to operate at 700 mV supply voltage but it is observed during measurement to operate fine at 680 mV. While designing it was targeted to have a lock time of 150µs and the measured data is showing its performance is better. In simulation it was found to consume 2.7µW while measured data presents a little higher and the total area consumed by the PLL is 170µm x 95µm.

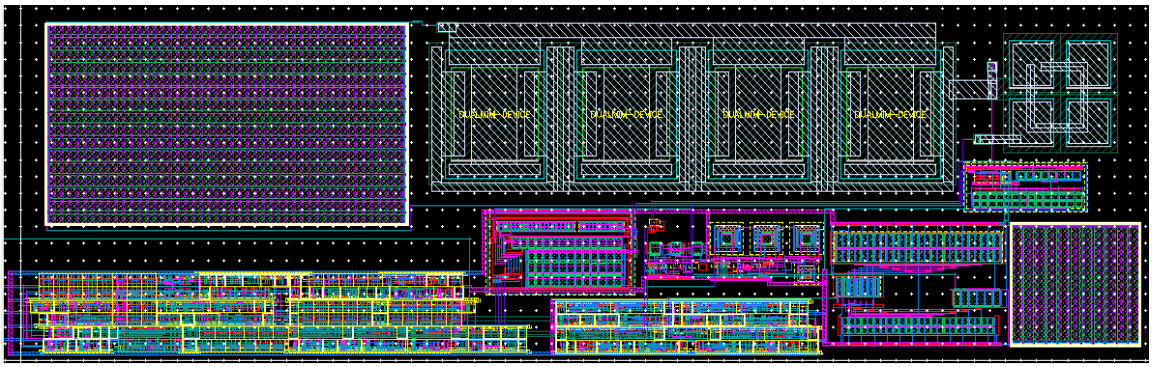


Figure 5.14 Picture of PLL layout.

CHAPTER VI

DEMODULATOR AND MODULATOR

6.1 Introduction

Demodulator and the modulator are the essential for communication between the RFID and the base station. Data needs to be modulated for transmission from the RFID to the base station through a wireless channel. In digital communication as is the case here modulation is performed by varying parameter such a amplitude ASK(amplitude shift keying), frequency (FSK) frequency shift keying or phase PSK (phase shift keying) of the sinusoid carrier relative to the bit stream to be transmitted. Given the limited power resource for a passive RFID, BPSK modulation or back scatter phase shift keying to varying phase is applied.

Demodulation is the process of extracting base band data from the modulated signal. In case of a ASK it is achieved by envelop detection the of "1''s"and "0's", in FSK is achieved by mixing with the synchronized carrier and band pass filtering to determine 1 and 0, and in case of PSK its uses a local oscillator synchronized with the transmitting station. The demodulator that we are using is a ASK or AM demodulator. Given the RFID is passive these circuits needs to be low power.

6.2 Demodulator

The demodulator schematic and the anticipated waveforms are shown in Figure 6.1. The demodulator extracts incoming ASK data and the reference clock for the PLL. The demodulator input is a double-sideband amplitude modulation (DSB-AM) signal centered at 900MHz and the modulating frequency is 160KHz. The demodulator consists of a peak detector circuit, diode D1, R1 and C1 and an inverter gain stage biased using back to back Schottky diodes followed by digital buffers, the RC time constant is 14.03ns. Power consumption is 0.1μW which when compared to power figures of other similar works presented in table 6.1; this new demodulator configuration offers dramatic improvement. The GEN-2 RFID standard defines the modulation index as equation (6.1)

$$m = \left(1 - \frac{B}{A}\right) \tag{6.1}$$

Where A and B are as notified in the waveform of figure 6.1. Typical value of the modulation index for GEN-2 standard range from 80 -100%. Fig. 11 shows the demodulator output level shifted to 1.2V from 700mV for modulation and carrier frequencies of 160 KHz and 900 MHz respectively with B/A = 0.5 which represents a modulation depth of 50%

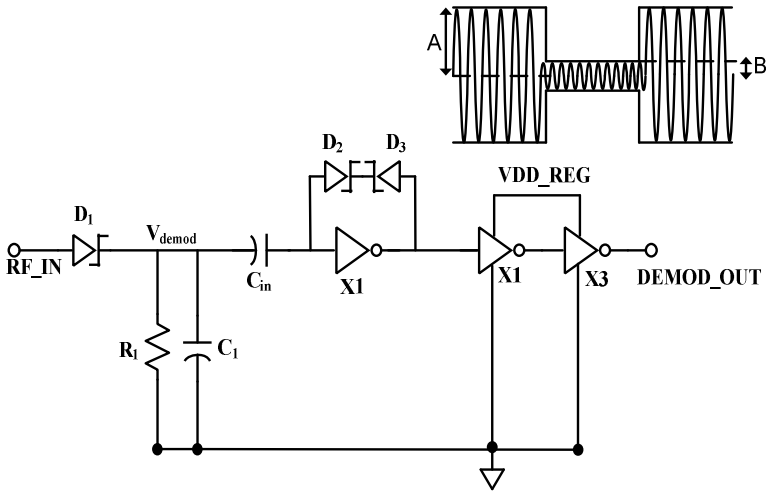


Figure 6.1Demodulator schematic

Demodulated signal

Modulated signal

Figure 6.2 Modulated signal is of -5dBm Power and 50% modulation from cadence simulations.

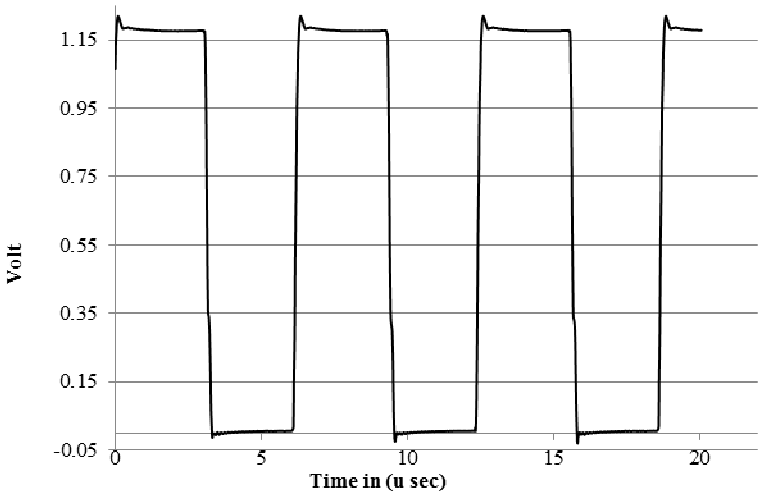


Figure 6.3 Measured result of the demodulator with a modulated signal of -5dBm and modulation index of 50%.

Simulation result and measured results of the demodulator are shown in Figure 6.2. and Figure 6.3 respectively. Measurements were completed with a 700mV supply voltage and Rohden-Schwartz rf generator at room temperature, with an AM modulation carrier frequency from 900MHz to 100MHz with power of -5dBm and a modulation index of 50%. This test configuration was to measure the lowest signal power and modulation index for which the demodulator is functional.

Table 6.1 Comparison of present demodulator with other similar works

Reference	Supply voltage	Modulation frequency	Power consumed	Input voltage	Process
Zong[95]	500mV	40KHz	105nW	300mV	90nm
Ganesh[96]	1.25V	160KHZ	200nW	44mV	180nm
Changming [97]	-	-	380nW	-	180nm
Maryam [98]	1.2V	160Hz	290nW	180mV	180nm
Mendizabal [99]	300mV	125kHz	15nW	-	90nm
Ashry [100]	1.2V	-	~20%of 1uW 200nW	-	130nm
This work	700mV	160KHz	100nW	125nV	180n

6.2 Modulator

The smart RFID sensor communicates outbound with the base station via back PSK scatter. Phase shift keying (PSK) is achieved by detuning the antenna impedance from harvester match resulting in PSK modulation of the reflected wave by x degrees plus or minus to represent a zero and one by +/- x degrees. The impedance mismatch or modulation is achieved by switching capacitors x and Y in and out to achieved phase advance and phase delay achieve 1 and zero effectively. In figure 6.4 C and C1 combined achieve the desired matching capacitor for resonance. The antenna impedance match is detuned by switching in C1 OR C2 to the matching network removing both making the mismatch inductive or switching both in (C1 and C2) make the matching network capacitive. This represents a digital 1 and 0 respectively. The simulated S11for “0” and “1” are shown in Figure 6.5 and Figure 6.6 respectively. Power must be harvest during out bound transmission thus 180 degree modulation angle is undesirable, but the bit error rate in the communication depends on a large angle between the modulation states. This makes angle selection a difficult task.

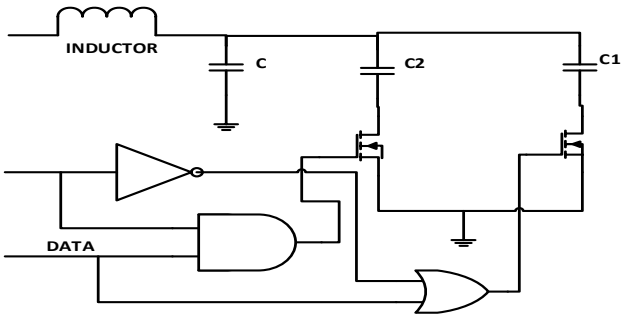


Figure 6.4 Modulator Schematic.

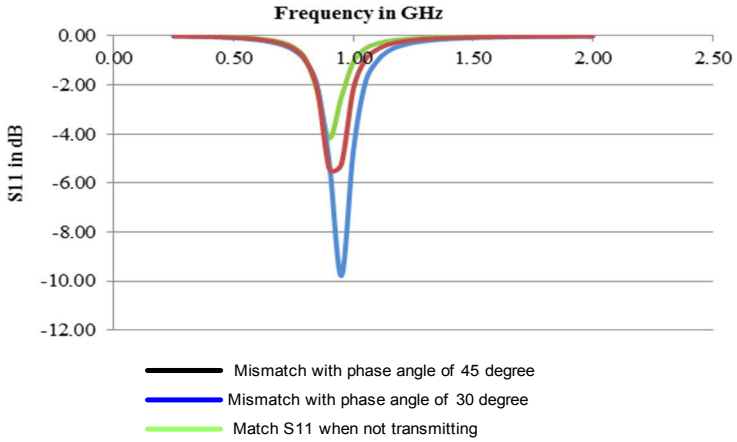


Figure 6.5 Simulated S11 When Transmitting a“0”.

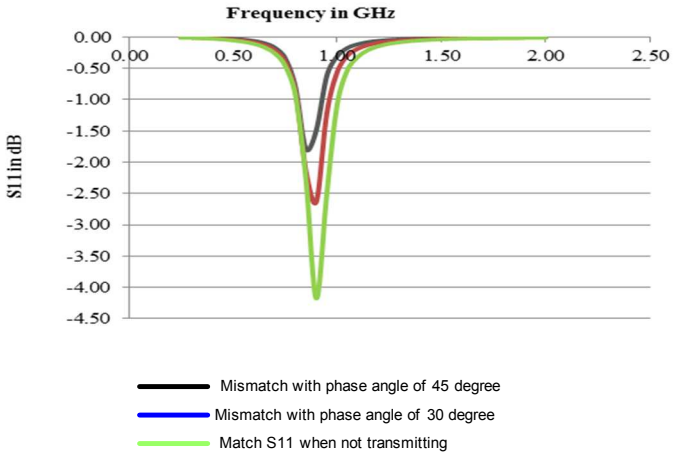


Figure 6.6 Simulated S11 When Transmitting a “1”.

CHAPTER VII

CONCLUSION

7.1 Summary of work

This dissertation presents the implementation detail of the front end of a 900MHz passive RFID for biological sensing. As the RFID is a passive one so it has to harvest its own power, Hence a efficient harvester is essential. In chapter 2 we present a optimal harvester designing process by which we can achieve both high ouput voltage and good efficiency. In this process a simple model of the harvester is presented and was simulated in matlab to get an estimation of the optimal design. After which the estimated values were used to do a parametric sweep in Cadence spectre to get the accurate device size and component value for maximum power conversion efficiency. The results were verified by doing a parasic extraction simulation on the layout of the design. The harvester had achieved a efficiency of 34% while supplying 74μA@1.2V.

In order to save power the digital core of the RFID is operated near subthreshold. Hence a voltage regulator to supply voltage in the range of near subthreshold or moderate inversion without much ripple is required. Again to have high conversion efficiency the switch capacitor voltage regulator is used for the purpose of voltage regulation. The implementation detail of which is presented in chapter 3. The DC-DC voltage regulator presented in this work is adaptive one, as we are going to apply the dynamic supply voltage scaling technique to compensate for the reduction in reliability of performance of the circuit due to variation of V_{TH}

across process due to random doping effects and temperature in subthreshold. The voltage regulator is capable of selecting the supply voltage adaptively at which the digital circuit would perform without any timing error. The line and load regulation results of the voltage converter is presented which shows that the converter has a power conversion efficiency of 86% and the ripple in the supply voltage is with +/- 12mV.

In chapter 5 the Phase lock loop (PLL) is presented. The PLL presented is a low power low jitter PLL. The reference clock of the PLL is 160 KHz and it can supply a maximum output frequency of 5.12MHz. The PLL is also capable of clock data recovery from a EPC gen 2 protocol data format. Both simulation and measured data of the PLL is presented in chapter 5 .

Finally in chapter 6 the Demodulator and the Modulator to be used for communication between the RFID and the base station is presented. The demodulator presented is a ultra low power AM (amplitude modulation) demodulator, which consumes only 100nW and is capable of demodulating a double-sideband amplitude modulated (DSB-AM) signal centered at 900MHz and the modulating frequency is 160KHz. The demodulator can demodulate signal having as low as -5dBm power and 50% modulation index. The modulation for transmitting signal is achieved by BPSK(back scatter phase shift keying) .

7.2 Future work

The adaptive voltage regulator implemented in this work can only step up the voltages it cannot step down the voltages once it has been stepped up. When not required this extra over drive would inefficiently consume extra power. Future works need to solve this problem by developing a continuous feed back solution which can both step up and step down voltage as required with changing die temperature. For a passive RFID harvester efficiency is a critical factor, much more work is needed to understand the factors affecting the efficiency and thus how to manipulate those factors to improve the efficiency. The harvester presented in this work was optimized for a

certain minimum output voltage and output current, other solution may be needed to operate the rectifier at highest efficiency point for a particular load current without any constraint on V_{out}. One possibility is post initial harvesting, adding a charge pump circuit like a doubler may be useful to attain a higher voltage. Finally, while reporting my harvester efficiency I find it difficult to compare my work with other works. As different harvesters were supplying different load currents at different supply voltages. A test standard is need in this case so that a fare comparison can be carried out between different reported works.

REFERENCES

[1] J. Landt, "The history of RFID," *Potentials, IEEE,* vol. 24, pp. 8-11, 2005.

[2] L. Steve, "A Basic Introduction to RFID Technology and Its Use In the Supply Chain."

[3] C. V. Trappey, A. J. C. Trappey, and C. S. Liu, "Develop patient monitoring and support system using mobile communication and intelligent reasoning," in *Systems, Man and Cybernetics, 2009. SMC 2009. IEEE International Conference on*, 2009, pp. 1195-1200.

[4] M. Merenda, C. Felini, and F. G. Della Corte, "Battery-less smart RFID tag with sensor capabilities," in *RFID-Technologies and Applications (RFID-TA), 2012 IEEE International Conference on*, 2012, pp. 160-164.

[5] W. B. Spillman, "Sensing and processing for smart structures," *Proceedings of the IEEE,* vol. 84, pp. 68-77, 1996.

[6] K. Finkenzeller, *RFID Handbook:Fundamentals and Applications in Contactless Smart Cards, Radio Frequency Identification and Near-Field Communication*, 3rd ed. New York, NY, USA: Wiley, 2010.

[7] Y. Lee. Antenna circuit design for RFID applications

[8] S. M. Rajesh, "Integration of Active RFID and WSN for real time low-cost data monitoring of patients in hospitals," in *Control, Automation, Robotics and Embedded Systems (CARE), 2013 International Conference on*, 2013, pp. 1-6.

[9] T. Volk, S. Gorbey, M. Bhattacharyya, W. Gruenwald, B. Lemmer, L. M. Reindl*, et al.*, "RFID Technology for Continuous Monitoring of Physiological Signals in Small Animals," *Biomedical Engineering, IEEE Transactions on,* vol. 62, pp. 618-626, 2015.

[10] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-μW minimum RF input power," *Solid-State Circuits, IEEE Journal of,* vol. 38, pp. 1602-1608, 2003.

[11] D. Yeager, Z. Fan, A. Zarrasvand, N. T. George, T. Daniel, and B. P. Otis, "A 9μA Addressable Gen2 Sensor Tag for Biosignal Acquisition," *Solid-State Circuits, IEEE Journal*

[12] C. Namjun, S. Seong-Jun, K. Sunyoung, K. Shiho, and Y. Hoi-Jun, "A 5.1-μW UHF RFID tag chip integrated with sensors for wireless environmental monitoring," in *Solid-State Circuits Conference, 2005. ESSCIRC 2005. Proceedings of the 31st European*, 2005, pp. 279-282.

[13] S. Hongwei, L. Lilan, and Z. Yumei, "Fully integrated passive UHF RFID tag with temperature sensor for environment monitoring," in *ASIC, 2007. ASICON '07. 7th International Conference on*, 2007, pp. 360-363.

[14] K. Shiho, C. Jung-Hyun, K. Hyun-Sik, K. Haksoo, K. Hee-Bok, and H. Suk-Kyung, "An EPC Gen 2 compatible passive/semi-active UHF RFID transponder with embedded FeRAM

and temperature sensor," in *Solid-State Circuits Conference, 2007. ASSCC '07. IEEE Asian*, 2007, pp. 135-138.
[15] R. Barnett, G. Balachandran, S. Lazar, B. Kramer, G. Konnail, S. Rajasekhar*, et al.*, "A Passive UHF RFID Transponder for EPC Gen 2 with -14dBm Sensitivity in 0.13μm CMOS," in *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, 2007, pp. 582-623.
[16] T. Lecklider. (October 2005) The World of the Near Field. *Evaluation Engineering*.
[17] A. Y. Chow, V. Y. Chow, K. H. Packo, J. S. Pollack, G. A. Peyman, and R. Schuchard, "The artificial silicon retina microchip for the treatment of vision loss from retinitis pigmentosa," *Arch Ophthalmol,* vol. 122, pp. 460-9, Apr 2004.
[18] M. F. Dorman, P. C. Loizou, and D. Rainey, "Simulating the effect of cochlear-implant electrode insertion depth on speech understanding," *J Acoust Soc Am,* vol. 102, pp. 2993-6, Nov 1997.
[19] W. Guoxing, L. Wentai, M. Sivaprakasam, M. S. Humayun, and J. D. Weiland, "Power supply topologies for biphasic stimulation in inductively powered implants," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, 2005, pp. 2743-2746 Vol. 3.
[20] R. K. M. Loy, and L. Williams. (2005) ISM band and short range device regulatory compliance overview Application report SERA048.
[21] "Human exposure to microwaves and radiofrequency electromagnetic fields," *Antennas and Propagation Society Newsletter, IEEE,* vol. 23, pp. 23-24, 1981.
[22] S. Mingui, M. Mickle, W. Liang, Q. Liu, and R. J. Sclabassi, "Data communication between brain implants and computer," *Neural Systems and Rehabilitation Engineering, IEEE Transactions on,* vol. 11, pp. 189-192, 2003.
[23] T. Ibrahim, D. Abraham, and R. Rennaker, "Electromagnetic Power Absorption and Temperature Changes due to Brain Machine Interface Operation," *Annals of Biomedical Engineering,* vol. 35, pp. 825-834, 2007.
[24] P. R. Kennedy and R. A. Bakay, "Restoration of neural output from a paralyzed patient by a direct brain connection," *Neuroreport,* vol. 9, pp. 1707-11, Jun 1 1998.
[25] J. F. Hetke, J. L. Lund, K. Najafi, K. D. Wise, and D. J. Anderson, "Silicon ribbon cables for chronically implantable microelectrode arrays," *IEEE Transactions on Biomedical Engineering,* vol. 41, pp. 314-321, 1994.
[26] R. J. Vetter, J. C. Williams, J. F. Hetke, E. A. Nunamaker, and D. R. Kipke, "Chronic neural recording using silicon-substrate microelectrode arrays implanted in cerebral cortex," *IEEE Transactions on Biomedical Engineering,* vol. 51, pp. 896-904, 2004.
[27] X. Lisheng, M. Q. H. Meng, R. Hongliang, and Y. Chan, "Radiation Characteristics of Ingestible Wireless Devices in Human Intestine Following Radio Frequency Exposure at 430, 800, 1200, and 2400 MHz," *Antennas and Propagation, IEEE Transactions on,* vol. 57, pp. 2418-2428, 2009.
[28] U. Kaiser and W. Steinhagen, "A low-power transponder IC for high-performance identification systems," *Solid-State Circuits, IEEE Journal of,* vol. 30, pp. 306-310, 1995.
[29] D. Friedman, H. Heinrich, and D. W. Duan, "A low-power CMOS integrated circuit for field-powered radio frequency identification tags," in *Solid-State Circuits Conference, 1997. Digest of Technical Papers. 43rd ISSCC., 1997 IEEE International*, 1997, pp. 294-295.
[30] V. Pillai, H. Heinrich, D. Dieska, P. V. Nikitin, R. Martinez, and K. V. S. Rao, "An Ultra-Low-Power Long Range Battery/Passive RFID Tag for UHF and Microwave Bands With a Current Consumption of 700 nA at 1.5 V," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 54, pp. 1500-1512, 2007.
[31] W. L. E. a. G. E. Anner, "Communication Engineering " vol. 3rd ed, 1956 1956

[32] C. Bowick, *RF Circuit Design*. London, UK: Newnes, 1997.
[33] H. Yehui and D. J. Perreault, "Analysis and Design of High Efficiency Matching Networks," *Power Electronics, IEEE Transactions on,* vol. 21, pp. 1484-1491, 2006.
[34] T. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits," pp. pp. 87– 107, 2004.
[35] Y. Chung-Ming and C. Ming-Hui, "A novel single-phase ac to high voltage dc converter based on Cockcroft-Walton cascade rectifier," in *Power Electronics and Drive Systems, 2009. PEDS 2009. International Conference on*, 2009, pp. 822-826.
[36] D. Michelon, E. Bergeret, A. Di Giacomo, and P. Pannier, "Optimization of integrated dickson voltage-multipliers for RF energy harvesting," in *New Circuits and Systems Conference (NEWCAS), 2014 IEEE 12th International*, 2014, pp. 448-451.
[37] S. Mandal and R. Sarpeshkar, "Low-Power CMOS Rectifier Design for RFID Applications," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 54, pp. 1177-1188, 2007.
[38] S. dela Cruz, M. G. de los Reyes, A. Alvarez, M. T. de Leon, and C. R. Roque, "Design and implementation of passive RF-DC converters for RF power harvesting systems," in *TENCON 2010 - 2010 IEEE Region 10 Conference*, 2010, pp. 1503-1508.
[39] W. Jeon, J. Rodgers, and J. Melngailis, "Design and fabrication of Schottky diode, on-chip RF power detector," in *Semiconductor Device Research Symposium, 2003 International*, 2003, pp. 294-295.
[40] C. C. K. Enz, F.; Vittoz, E. A, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low current applications," *Analog Integrated Circuits and Signal Processing,* pp. pp. 83-114, 1995.
[41] R. E. Barnett, L. Jin, and S. Lazar, "A RF to DC Voltage Conversion Model for Multi-Stage Rectifiers in UHF RFID Transponders," *IEEE Journal of Solid-State Circuits,* vol. 44, pp. 354-370, 2009.
[42] J. P. Curty, N. Joehl, F. Krummenacher, C. Dehollaini, and M. J. Declercq, "A model for μ-power rectifier analysis and design," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 52, pp. 2771-2779, 2005.
[43] A. Shameli, A. Safarian, A. Rofougaran, M. Rofougaran, and F. De Flaviis, "Power harvester design for passive UHF RFID tag using a voltage boosting technique," *IEEE Transactions on Microwave Theory and Techniques,* vol. 55, pp. 1089-1097, 2007.
[44] K. Kotani, A. Sasaki, and T. Ito, "High-Efficiency Differential-Drive CMOS Rectifier for UHF RFIDs," *Solid-State Circuits, IEEE Journal of,* vol. 44, pp. 3011-3018, 2009.
[45] S. Scorcioni, L. Larcher, and A. Bertacchini, "Optimized CMOS RF-DC converters for remote wireless powering of RFID applications," in *RFID (RFID), 2012 IEEE International Conference on*, 2012, pp. 47-53.
[46] T. Le, K. Mayaram, and T. Fiez, "Efficient Far-Field Radio Frequency Energy Harvesting for Passively Powered Sensor Networks," *Solid-State Circuits, IEEE Journal of,* vol. 43, pp. 1287-1302, 2008.
[47] V. Kuhn, C. Lahuec, F. Seguin, and C. Person, "A Multi-Band Stacked RF Energy Harvester With RF-to-DC Efficiency Up to 84%," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 63, pp. 1768-1778, 2015.
[48] (November 2000, AMD PowerNOW! Technology. Available: http://www.amd.com
[49] M. Fleischmann, "Longrun power management," 2001.
[50] e. a. S.Gochman, "The Intel Pentium M Processor: Microarchitecture and Performanc," *Intel Technology Journal,* vol. 7, pp. 22-36, May 2003.
[51] D. Scott, T. Shaoping, Z. Song, and M. Nandakumar, "Device physics impact on low leakage, high speed DSP design techniques," in *Quality Electronic Design, 2002. Proceedings. International Symposium on*, 2002, pp. 349-354.

[52] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE,* vol. 91, pp. 305-327, 2003.

[53] M. Suetake, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, N. Shigyo, S. Odanaka*, et al.*, "Precise physical modeling of the reverse-short-channel effect for circuit simulation," in *Simulation of Semiconductor Processes and Devices, 1999. SISPAD '99. 1999 International Conference on*, 1999, pp. 207-210.

[54] A. Ono, R. Ueno, and I. Sakai, "TED control technology for suppression of reverse narrow channel effect in 0.1 /spl mu/m MOS devices," in *Electron Devices Meeting, 1997. IEDM '97. Technical Digest., International*, 1997, pp. 227-230.

[55] T. Sakurai and A. R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," *Solid-State Circuits, IEEE Journal of,* vol. 25, pp. 584-594, 1990.

[56] T. Kobayashi and T. Sakurai, "Self-adjusting threshold-voltage scheme (SATS) for low-voltage high-speed operation," in *Custom Integrated Circuits Conference, 1994., Proceedings of the IEEE 1994*, 1994, pp. 271-274.

[57] Y. Yasuda, N. Kimizuka, Y. Akiyama, Y. Yamagata, Y. Goto, and K. Imai, "System LSI multi-vth transistors design methodology for maximizing efficiency of body-biasing control to reduce vth variation and power consumption," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, pp. 68-71.

[58] A. Sinha and A. Chandrakasan, "Dynamic power management in wireless sensor networks," *Design & Test of Computers, IEEE,* vol. 18, pp. 62-74, 2001.

[59] Z. Bo, L. Nazhandali, J. Olson, A. Reeves, M. Minuth, R. Helfand*, et al.*, "A 2.60pJ/Inst Subthreshold Sensor Processor for Optimal Energy Efficiency," in *VLSI Circuits, 2006. Digest of Technical Papers. 2006 Symposium on*, 2006, pp. 154-155.

[60] H. R. Pourshaghaghi and J. P. de Gyvez, "Power-performance optimization using fuzzy control of simultaneous supply voltage and body biasing scaling," in *Electronics, Circuits, and Systems (ICECS), 2010 17th IEEE International Conference on*, 2010, pp. 281-284.

[61] T. Miyake, T. Yamashita, N. Asari, H. Sekisaka, T. Sakai, K. Matsuura*, et al.*, "Design methodology of high performance microprocessor using ultra-low threshold voltage CMOS," in *Custom Integrated Circuits, 2001, IEEE Conference on.*, 2001, pp. 275-278.

[62] J. Tschanz, K. James, S. Narendra, R. Nair, D. Antoniadis, A. Chandrakasan*, et al.*, "Adaptive body bias for reducing impacts of die-to-die and within-die parameter variations on microprocessor frequency and leakage," in *Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International*, 2002, pp. 344-539.

[63] T. Chen and S. Naffziger, "Comparison of adaptive body bias (ABB) and adaptive supply voltage (ASV) for improving delay and leakage under the presence of process variation," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on,* vol. 11, pp. 888-899, 2003.

[64] P. Junyoung and J. A. Abraham, "A fast, accurate and simple critical path monitor for improving energy-delay product in DVS systems," in *Low Power Electronics and Design (ISLPED) 2011 International Symposium on*, 2011, pp. 391-396.

[65] T. Austin, D. Blaauw, T. Mudge, and K. Flautner, "Making typical silicon matter with Razor," *Computer,* vol. 37, pp. 57-65, 2004.

[66] A. Drake, R. Senger, H. Deogun, G. Carpenter, S. Ghiasi, T. Nguyen*, et al.*, "A Distributed Critical-Path Timing Monitor for a 65nm High-Performance Microprocessor," in *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, 2007, pp. 398-399.

[67] M. Elgebaly and M. Sachdev, "Variation-Aware Adaptive Voltage Scaling System," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on,* vol. 15, pp. 560-571, 2007.
[68] M. Nakai, S. Akui, K. Seno, T. Meguro, T. Seki, T. Kondo*, et al.*, "Dynamic voltage and frequency management for a low-power embedded microprocessor," *Solid-State Circuits, IEEE Journal of,* vol. 40, pp. 28-35, 2005.
[69] "3A, 2.2MHz, Synchronous Step-Down DC-DC Converter," June 2013.
[70] "Fully Integrated Power Management With Power Path and Battery Charger," Dec. 2011.
[71] M. D. Seeman, V. W. Ng, L. Hanh-Phuc, M. John, E. Alon, and S. R. Sanders, "A comparative analysis of Switched-Capacitor and inductor-based DC-DC conversion technologies," in *Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on*, 2010, pp. 1-7.
[72] Y. K. Ramadass, "Energy Processing Circuits for Low-Power Applications," Doctor of Philosophy, Electrical Engineering and ComputerScience, MASSACHUSETTS INSTITUTE OF TECHNOLOGY, June 2009.
[73] I. Chowdhury and M. Dongsheng, "On-chip reconfigurable SC power supply with adaptive gain/pulse control for self-powered energy-efficient devices," in *Industrial Electronics, 2008. ISIE 2008. IEEE International Symposium on*, 2008, pp. 1715-1720.
[74] V. W.-S. Ng, "Switched Capacitor DC-DC Converter: Superior where the Buck Converter has Dominated," Doctor of Philosophy, Electrical Engineering and Computer Sciences, University of California at Berkeley, August 17, 2011.
[75] M. S. Makowski and D. Maksimovic, "Performance limits of switched-capacitor DC-DC converters," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, 1995, pp. 1215-1221 vol.2.
[76] Y. K. Ramadass, A. A. Fayed, and A. P. Chandrakasan, "A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter With Digital Capacitance Modulation in 45 nm CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 45, pp. 2557-2565, 2010.
[77] N. Keskar and G. A. Rincon-Mora, "Self-stabilizing, integrated, hysteretic boost DC-DC converter," in *Industrial Electronics Society, 2004. IECON 2004. 30th Annual Conference of IEEE*, 2004, pp. 586-591 Vol. 1.
[78] Available: http://users.ece.gatech.edu/rincon-mora/research/hyst_ac.pdf
[79] T. Chung-Hsien and W. Jiin-Chuan, "A ripple control buck regulator with fixed output frequency," *Power Electronics Letters, IEEE,* vol. 1, pp. 61-63, 2003.
[80] O. A. Ursaru, C.; Lucanu, M, "Hysteretic-controlled Voltage Regulator using Integrated Circuit LM723," *Electronics & Electrical Engineering,* p. p45, September 2009.
[81] N. Nouri and S. Mirabbasi, "A900MHz-2GHz low-swing low-power 0.18/spl mu/m CMOS PLL," in *Electrical and Computer Engineering, 2005. Canadian Conference on*, 2005, pp. 1566-1569.
[82] M. Van Paemel, "Analysis of a charge-pump PLL: a new model," *Communications, IEEE Transactions on,* vol. 42, pp. 2490-2498, 1994.
[83] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *Solid-State Circuits, IEEE Journal of,* vol. 31, pp. 1723-1732, 1996.
[84] J. M. Ingino, "A 4 GHz 40 dB PSRR PLL for an SOC application," in *Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International*, 2001, pp. 392-393.
[85] F. M. Gardner, "Charge-Pump Phase-Lock Loops," *Communications, IEEE Transactions on,* vol. 28, pp. 1849-1858, 1980.
[86] B. Razavi, *Design of integrated circuits for optical communication*: McGraw Hill Higher Education, 2003.
[87] R. J. Baker, "CMOS CIRCUIT DESIGN, LAYOUT, AND SIMULATION," 2005.

[88] J.-F. D. Wu, "PHASE LOCKED LOOP FOR RADIATION HARDENED ENVIRONMENT," 2006.
[89] S. Sauter, D. Schmitt-Landsiedel, R. Thewes, and W. Weber, "Effect of parameter variations at chip and wafer level on clock skews," *Semiconductor Manufacturing, IEEE Transactions on,* vol. 13, pp. 395-400, 2000.
[90] P. Zarkesh-Ha, T. Mule, and J. D. Meindl, "Characterization and modeling of clock skew with process variations," in *Custom Integrated Circuits, 1999. Proceedings of the IEEE 1999*, 1999, pp. 441-444.
[91] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *Solid-State Circuits, IEEE Journal of,* vol. 33, pp. 179-194, 1998.
[92] C. J. B. Fayomi, G. W. Roberts, and M. Sawan, "Low-voltage CMOS analog bootstrapped switch for sample-and-hold circuit: design and chip characterization," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, 2005, pp. 2200-2203 Vol. 3.
[93] H. Nakamoto, D. Yamazaki, T. Yamamoto, H. Kurata, S. Yamada, K. Mukaida*, et al.*, "A Passive UHF RF Identification CMOS Tag IC Using Ferroelectric RAM in 0.35-μm Technology," *Solid-State Circuits, IEEE Journal of,* vol. 42, pp. 101-110, 2007.
[94] C. Chi-Fat, P. Kong-Pang, L. Ka-Nang, G. Jianping, L. K. L. Leung, and C. Chiu-Sing, "A Low-Power Continuously-Calibrated Clock Recovery Circuit for UHF RFID EPC Class-1 Generation-2 Transponders," *Solid-State Circuits, IEEE Journal of,* vol. 45, pp. 587-599, 2010.
[95] Z. Hongqiang, S. Jinpeng, L. Shan, J. Mei, B. Qingyuan, T. Ling*, et al.*, "An ultra low power ASK demodulator for passive UHF RFID tag," in *ASIC (ASICON), 2011 IEEE 9th International Conference on*, 2011, pp. 637-640.
[96] G. K. Balachandran and R. E. Barnett, "A Passive UHF RFID Demodulator With RF Overvoltage Protection and Automatic Weighted Threshold Adjustment," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 57, pp. 2291-2300, 2010.
[97] M. Changming, W. Xingjun, Z. Chun, and W. ZhiHua, "A low-power RF front-end of passive UHF RFID transponders," in *Circuits and Systems, 2008. APCCAS 2008. IEEE Asia Pacific Conference on*, 2008, pp. 73-76.
[98] M. G. Jomehei, S. Sheikhaei, and B. Forouzandeh, "A novel ultra low power ASK demodulator for a passive UHF RFID tag compatible with C1 G2 EPC standard protocol," *Analog Integr. Circuits Signal Process.,* vol. 75, pp. 21-29, 2013.
[99] M. Mendizabal, "Low Power Demodulator Design for RFID Applications," University of Windsor, 2012.
[100] K. Ahmed Ashry , MagdiIbrahim, "A compactlow-powerUHF RFID tag," *MicroelectronicsJournal,* 2009.

APPENDICES

Appendix A

```
clear
st=1.1;
sd=1;
Ql=50;
rant=50;
w = 1e-6:.25e-6:20e-6;%transistor width
l=180e-9;% transistor length
Vd1=1.38;%max voltage
Vd(1)=st-sd;% range of the diode drop
Voutx(1)=st;%dc level
kp=3.25e-4;
fre=900e6;% frequency
Lcap=20e-12;% load cap
Lcap1=20e-12;
fs=fre*2000;% fft sampling frequency
dt=1/fs;
ut=25e-3;% thermal voltage
ni=2;% ideality factor ni 1.2 & px 488
%px3=-490e-3;%Vp calculation
t = 0:1/fs:(150*(1/fre));% time
t1= 149*(1/fre):1/fs:(150*(1/fre));
an1=2*3.143*fre*t;%angle
w1=length(w);% length of the transistor width array
b=length(an1);
c=length(t1);
tx=(c-1);
cj=0;
cu1=Voutx(1)*Lcap1;
cu=sd*Lcap;
         for f1 = 1:w1
            c1=b+1;
            isx=2*ni*(w(f1)/l)*kp*(ut^2);%specific current
            ick=0;
            c2=0;
            c3=0;
            c4=0;
            c5=0;
            pw1=0;
```

```
            for p1 = 1:b
                vi2(p1)= Voutx(p1)+(Vd1*sin(an1(p1)));% input
voltage calculation
                A(p1) = (exp(Vd(p1)/ut)-1);
                B(p1)= exp(((vi2(p1)*(1-ni))-.425)/(ni*ut));
                C(p1) = A(p1)*B(p1);
                A1(p1)= exp(-0.425/(ni*ut));
                B1(p1)= exp(-vi2(p1)/ut)-1;
                C1(p1)= A1(p1)*B1(p1);
                idx1(p1)=C1(p1)*isx;
                %vi3(p1)= (vi2(p1)-.43);

%ifo=(log(1+exp((vi3(p1)+(ni*Vd(p1)))/(2*ni*ut))))^2;
                %ire=(log(1+exp((vi3(p1))/(2*ni*ut))))^2;
                idx(p1)= isx*C(p1);%(ifo-ire);% Id calculation
                cu1=cu1-((50e-6*dt)-(idx1(p1)*dt));
                cu=cu-((50e-6*dt)-(idx(p1)*dt));
                dvx(p1)=cu1/Lcap1;
                xy(p1)=cu;
                dv1(p1)=cu/Lcap;
                Vd(p1+1)=vi2(p1)-dv1(p1);
                de(p1)=Vd(p1+1);
                cj=cj+1;
               %D=(tx-cj);
                %if cj == tx
                   Voutx(p1+1)= dvx(p1);
                   %cj=0;

                %elseif cj==tx
                       %cj=0;
                       %Voutx(p1+1)=Voutx(p1);

                %else
                  % Voutx(p1+1)=Voutx(p1);

                %end
            end
      for p2 = c:-1:1
                c1=c1-1;
                ick=ick+(idx(c1)*dt);
                %pw(p2)=(idx(c1)*(Vd(c1))*dt);
                %pw1=pw1+pw(p2);
                vd2(p2)=(Vd(c1));
                idc(p2)=idx(c1);
                ty(p2)=t(c1);
                vd21(p2)=vi2(c1);
            end
            gr(f1) = vd2(1);
            gr1(f1)=vd21(1);
            for p3= 2:c
```

```
        if gr(f1) >vd2(p3)
        else
           gr(f1) =vd2(p3);
        end
    end
    for p4= 2:c
        if gr1(f1)<vd21(p4)
        else
           gr1(f1)=vd21(p4);
        end
    end
    %pw2(f1)=pw1/(1/fre);
    dv2(f1)=dv1(b);
    ic(f1)=ick/(1/fre);
    pwx(f1)=50e-6*dv2(f1);
 for j = 1:c
    if idc(j)>0
        ang=360*fre*ty(j);
        kx=j;
        break
    else
    end
end
for j1 = kx:c
     if idc(j1)<0
        ang1=360*fre*ty(j1);
        kx1=j1;
        break
    else
end
end
ang2(f1)=ang1-ang;
for j2 = kx:kx1
    c4= c4+((vd2(j2)^2)*dt);
    c5= c5+((idc(j2)^2)*dt);
    c2= c2+(vd2(j2)*dt);
    c3= c3+(idc(j2)*dt);
end
vrm(f1)=(c4/(t1(kx1)-t1(kx)))^0.5;
irm(f1)=(c5/(t1(kx1)-t1(kx)))^0.5;
pdi(f1)=(vrm(f1)*irm(f1));
res(f1) = vrm(f1)/irm(f1);
Q(f1)= ((res(f1)/rant)-1)^0.5;
nma(f1)=(1-(Q(f1)/Ql));
vmax(f1)= (dv2(f1)/2)+gr(f1);
pin(f1)=(vmax(f1)^2)/(2*res(f1)*nma(f1));
eff(f1)=(pwx(f1))/pin(f1);
effx(f1)=pwx(f1)/(pwx(f1)+pdi(f1));
vin(f1)= vmax(f1)/Q(f1);
PIN(f1)= (vin(f1)^2)/(2*rant);
effx1(f1)=pwx(f1)/PIN(f1);
```

```
        E(f1)=effx(f1)*Q(f1);
         end



%subplot(3,2,1);
%plot(w,gr);

%plot(w,pdi);

%subplot(2,2,2);
%plot(ty,vd21);
%plot(w,pw2);
%plot(fu,z2);
%subplot(2,2,1);
%plot(w,pdi);
%xlabel('Width in m')
%ylabel('Power dessipation')
%plot(w,nma);
%subplot(1,1,1);
%plot(w,res);
%plot(w,pw2);
plot(w,Q);
xlabel('Width in m')
ylabel('Q value')
%plot(t,de);
%plot(w,dv2);
%subplot(2,2,3)
%[X,Y,Z] = plotyy(w,effx,w,Q,'plot','plot');
%ylabel(X(1),'Efficiency')
%ylabel(X(2),'Q value')
%xlabel(X(2),'Width in m')
%hold on
%plot(w,effx);
%plot(w,effx2)
%hold off
%subplot(2,1,1);
%plot(w,res);
%xlabel('Width in m')
%ylabel('Resistance in ohm')
```

Appendix B

```
clear
fe = (1e6:10000:5e6);
wi = (1e-6:500e-9:30e-6);
n=length(fe)
m=length(wi)
[F,W] = meshgrid(fe,wi);
for i = 1:m;
    for j = 1:n;
       ff = F(i,j);
       ww = W(i,j);
       t = 1/(2*ff);
%beta value
be = .2;
%gama value
ga = 1;
%delta value
de = 1;
%load current
cox=8.95e-3;
kpn=3.13e-4;
kpp=1.11e-4;
ic = 6e-6;
% cap value
ca = 30e-12;
l = 180e-9;
        Ron = (ww*(2*l/(kpn*(.9-.4))))+(ww*(2*l/(kpn*(.6-.4))));
        a=ww*(kpn*(.6-.4));b=ww*(kpn*(.9-.3-.4));c=ww*(kpn*(.9-
.4));
        Rof =(l/a)+(l/b)+(l/c);
        % charging time constant
        tuc = Ron*ca;
        % discharging time constant
        tud = Rof*ca;
        % capacitir power loss
           capl = (t*ic^2/(ca*(be + ga*de)))*(1-(1/(1-
exp(t/tuc)))-(1/(1-exp(t/tud))));
        % switching power loss
        swpl = (ff*ww)*0.6*(l*cox*(.9^2 + .6^2 + .6^2 + .9^2));
        pow = capl+swpl;
Z(i,j)= pow;
    end
end
 % Z= Pcl+Psl;
       figure
mesh (F,W,Z)
%contour (F,W,Z,20)
```

VITA

Rehan Ahmed

Candidate for the Degree of

Doctor of Philosophy

Thesis: FRONT END OF A 900MHz RFID FOR BIOLOGICAL SENSING

Major Field: Electrical Engineering

Biographical: Kolkata, West Bengal, India

Education:

Completed the requirements for the Doctor of Philosophy in Electrical Engineering at Oklahoma State University, Stillwater, Oklahoma in December, 2015.

Completed Master of Science in Electrical Engineering at Oklahoma State University, Stillwater, Oklahoma in December, in 2009.

Completed Master of Science in Electronics at Sikkim Manipal University, India in December 2004.