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JAMES, DONALD WILLIAM

ENHANCED HIGH SPEED SERIAL DATA TEST SYSTEM

The University of Oklahoma

D. ENGR.

1979

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ENHANCED HIGH SPEED  
SERIAL DATA TEST SYSTEM

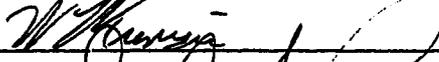
A DISSERTATION  
SUBMITTED TO THE GRADUATE FACULTY  
in partial fulfillment of the requirements for the  
degree of  
DOCTOR OF ENGINEERING

BY  
DONALD W. JAMES

1979

ENHANCED HIGH SPEED  
SERIAL DATA TEST SYSTEM

APPROVED BY

  
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DISSERTATION COMMITTEE

## ACKNOWLEDGMENT

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## ABSTRACT

This project was initiated as a United States Army contract, F41608-77-D-0065, which was awarded to Ra-Nav Laboratories. As a personal favor to John Perry, President of Ra-Nav Laboratories, I designed the logic for the Digital Data Analysis System. This is a high-speed serial data test system. This proposed design was presented and approved by my Doctoral Committee at the University of Oklahoma as partial fulfillment of the requirements for the degree of Doctor of Engineering in Electrical Engineering.

Before the design work started, there were preliminary meetings with the management of Ra-Nav Laboratories to discuss and define the interpretations of the design specifications. It was evident from the first meeting that the Army specifications were very vague. The management of Ra-Nav Laboratories felt that it was essential to begin the design work and would inform the Army Engineer of the problems at the monthly progress review meeting.

At the preliminary meetings between Ra-Nav and myself the structure of the design evolved. I proposed using either low-power Schottky TTL or CMOS logic to meet Ra-Nav requirements for no cooling fans. I also suggested using a

microprocessor which at the onset was rejected by Ra-Nav, but later was incorporated because of the changes in the specifications by the Army Engineer.

By the first monthly progress review meeting the Digital Message Generator logic was nearly completed. It was at this meeting that the Army Engineer was asked to clarify the specifications. Based on his suggestions, the following system was developed. One box would be the Digital Message Generator (DMG), while the second would be the Digital Signal Analyzer (DSA). The DSA was to include a PROM programmer. To meet the PROM programmer requirement, Ra-Nav planned to sell them a Data I/O PROM programmer.

This design was presented to and disapproved by the Army Engineer at the second monthly progress review meeting. The Army Engineer wanted the PROM programmer contained within the DSA. When Ra-Nav suggested repackaging the Data I/O programmer into the DSA, the Army Engineer again disapproved. He pointed out the following problems: The Data I/O was a word-structured PROM programmer, while he wanted a bit-structured programmer. He claimed that the hexadecimal addressing would cause problems for the testers and wanted a decimal address structure. It was at this time that Ra-Nav requested a change in the specifications to reflect the currently agreed upon changes in order that the design would have well defined goals.

The negotiations for the changes in the specifications

took over ten months due to 88 pages of changes to the original 33-page specifications. During these negotiations work was continued in order not to delay the project any longer than necessary. The building of the prototypes was completed, along with most of the debug of the logic design and the printed circuit card artwork.

At the final negotiating session a new Army engineer inserted additional requirements for the PROM programmer. At this point I assessed his requests to determine whether or not they could be included in the design and proposed the following plans to Ra-Nav. The first plan was for a quick-fix with minimum impact on schedule and projection, while the second would be the approach that would make the best possible system. The first method consisted of redesigning one printed wiring assembly by inserting a microprocessor. This method left all functions in the logic the same except for the programming function of the PROM programmer. The second method was to redesign three printed wiring assemblies into one or two, allowing the microprocessor to handle all the PROM programming features and some of the DSA operations.

Ra-Nav choose to use the first method, based on what they felt was the most economical solution from their position. They estimated that the cost to them to build one prototype printed wiring assembly was in the range of \$1200 to \$1500. They felt that the first method allowed them some return on their investment. It was agreed that, should

another order be placed for additional units, Ra-Nav would propose the second method as a cost reduction. In doing this they could negotiate a cost reduction program and would receive one half the cost saving to use in the development of the new printed wiring assemblies.

It may sound as though this project was an association of problems generated by the original specifications; however, it is very representative of a typical project in industry. Problems are generated because the person who writes the specification has his own ideas and interpretations which are often different from those of the designer. In most situations a third party checks the designer's system against the specifications bringing about a third interpretation. I have experienced similar problems in projects at Magnetic Peripherals Incorporated.

My last project at MPI would appear to have been an ideal situation. I personally wrote the specifications for the system; the customer reviewed the specifications and made changes. I then designed the system to the specifications, tested it, and presented it to the customer. When he tested the system, however, he found that it did not perform as he had envisioned it would. Therefore, he requested specification changes which resulted in major system changes. Thus, even the most ideal situations result in some specification changes.

It is not my intent to belabor the problems which

were encountered in designing this system, but rather to describe the Digital Message Generator (DMG), the Digital Signal Analyzer (DSA), and the PROM programmer (a unique part of the DSA), with emphasis on their enhancements, functions, and unique problems. The design principles used and problems encountered are discussed in the chapter on construction and testing.

The first article (first ten units of the contract) has been built and the first system has completed acceptance testing by the Army engineers. This first system exceeded all specification requirements during acceptance testing. The rest of the first article units are now in acceptance testing and are performing satisfactorily.

During the final presentation to my doctoral committee a demonstration of the system was given which consisted of a DMG connected to an ASR-33 teletypewriter. The demonstration featured some of the modes of operation using the stored message (the quick brown fox) and the selected character. These modes of operation used the message release feature which included a single message, single character, and continuous message. The DMG was demonstrated by intermittently adding a single error to the message while it was printing. The distortion feature was demonstrated by changing the percent of distortion until the teletype failed to print the correct character. The last feature demonstrated the use of the DMG to punch a paper tape of the stored message

by changing the parity select switch on the DMG. Three tapes of the stored message were punched using odd parity, even parity, and mark parity. The three tapes were then compared to show the difference in the parity bit positions.

## I. INTRODUCTION

### Scope and Purpose

This design was a test system for the United States Army under Contract No. F41608-77-D-0065 entitled Digital Data Analysis System. The contract had provisions for sixty units to be built. There were provisions for an additional fifty units for other branches of the services (Marines, Air Force, or Navy). The contract was based around the acceptance by the Army of ten qualification units. The first unit has now been built and is currently being tested for the first of ten qualification units.

The system will consist of two units: the Digital Message Generator (DMG) and the Digital Signal Analyzer (DSA). The equipment is to be used mainly in the test, repair, and evaluation of teletype machines, cryptograph equipment, and other terminal devices. The subsystems have evolved from previous test systems. They included features from their predecessors, enhancements, and new features. The DMG and DSA are related to the GGM-16 and GGM-21 test systems. The DSA and DMG contain most of the features from the GGM-16 and GGM-21, plus enhanced and new features, some

of which were beyond the state of the art when the GGM-16 and GGM-21 were designed.

### GGM-16 Features

The GGM-16 was designed in 1969 using mostly discrete transistors with some SSI circuits. The GGM-16 has the following features:

1. A 2047 bit ( $2^{11} - 1$ ) pseudo-random pattern generator.
2. One stored message in 5 bit Baudot code. The message is the "Quick Brown Fox" which is often used in typing drills.
3. A series of bit reversal patterns which are 1:1, 2:2, 6:1, 1:6.
4. A selected character generated by setting the bit levels on switches on the front panel. The character will be generated from 4 to 8 bits in start/stop mode while it will be 16 bits in the synchronous mode.
5. The GGM-16 baud rates are shown in Table I.
6. Telegraph distortion generation and measurement was from 0% to 49% in 1% increments. Telegraph distortion is defined as transition displacement as shown in Figure 1 (see page 3).
7. Generates and measures the following types of telegraph distortion (transition displacement): marking and spacing bias; marking and spacing end;

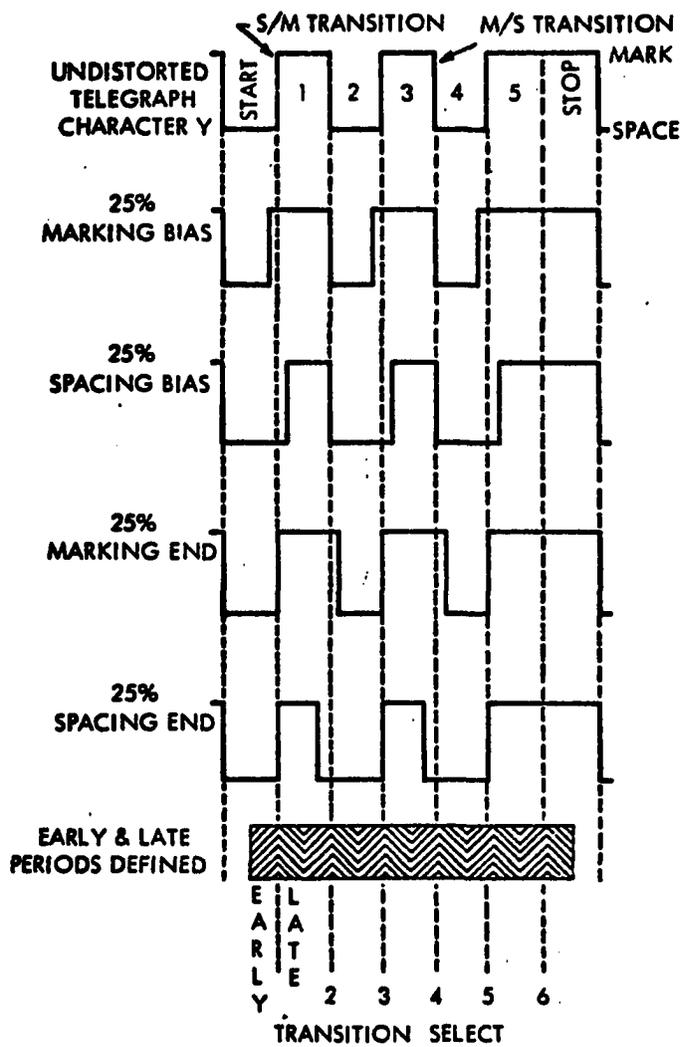


Figure 1. Types of Distortion

TABLE I

## AVAILABLE BAUD RATES FOR THE GGM-16

<u>Low</u>	<u>Medium</u>	<u>High</u>
37.5	150	1200
45.45	300	2400
50.0	600	4800
60.12		9600
74.2		
75.0		

total peak; early peak; late peak. These types of distortion are shown in Figure 1.

8. Two types of inputs and outputs. One is the polar/neutral isolated inputs and outputs. This is for operation at 300 volts polar or 150 volts neutral at 100 milliamperes maximum loop current. The second is low level MIL-STD 188B input and output for operation at +6 volts or +12 volts with 20 milliamperes loop current.
9. Front panel display is a Nixie tube readout.

### GGM-21 Features

The GGM-21 was designed in 1972 using SSI circuits with some functions built into LSI chips. These LSI special circuits were used for the 32k bit pseudo-random generators and ROM type memory. The GGM-21 has the following features:

1. A 32,768 bit pseudo-random pattern generator.

2. Two stored messages, one in 5 bit Baudot code and the second in 8 bit ASCII code. The messages are the "Quick Brown Fox".
3. The GGM-21 has a series of bit reversal patterns which are 1:1, 2:2, 6:1, and 1:6. It has a switch control for constant mark and constant space.
4. A selected character can be generated by setting the bit levels on switches on the front panel. The character can be generated either from 1 to 16 bits in start/stop mode, or 1 to 16 in synchronous mode.
5. The baud rates on the GGM-21 is from 30.0 in 1.0 increments to 9,999.0.
6. Telegraph distortion (Figure 1) generation, and measurement is from 0% to 49% in 1% increments.
7. Generates and measures the following types of telegraph distortion (transition displacement): marking and spacing bias; marking and spacing end; total peak; early peak; late peak. These types of distortion are shown in Figure 1.
8. Two types of inputs and outputs. One is the polar/neutral isolated inputs and outputs. This is for operation at 300 volts polar or 150 volts neutral at 100 milliamperes maximum loop current. The second is low level MIL-STD 188B inputs and outputs for operation at +6 volts or +12 volts

with 20 milliamperes loop current.

9. Seven-segment LED display on the front panel.

#### DMG and DSA Features and Enhancements

The DMG and DSA systems include the features of the GGM-16 and the GGM-21 with enhancements, additional memory, and a PROM programmer. The following are the features of the DMG and DSA:

1. Two pseudo-random pattern generators. One is 2047 bit like the GGM-16, but will be stored in EPROM memory. The second is 32,768 bit like the GGM-21, designed in digital logic.
2. Three stored messages:
  - (a) A 8 bit ASCII code - Quick Brown Box - like the GGM-21.
  - (b) A 5 bit Baudot code - Quick Brown Fox - like the GGM-16.
  - (c) A user definable message - anything that the user wishes to have.
3. A bit reversal pattern which is 1:1 (the other reversal patterns of the GGM-21 were deleted because they were never used), and either a constant mark or constant space.
4. A selected character generated by setting the bit levels on switches on the front panel. The character can be generated either as 4 to 16 bits in the start/stop mode or as 4 to 16 bits in the

synchronous mode.

5. The baud rate on the DMG and DSA is from 30.0 in increments of 0.1 baud to 9,999.0 and from 10,000 in increments of one baud to 99,990.
6. Telegraph distortion (Figure 1) generation, and measurement is from 0% to 49%. For baud rates from 30.0 to 9,999.0 the distortion is in 1% increments. For baud rates from 10,000 to 99,990 the distortion is in 5% increments.
7. Generates and measures the following type of telegraph distortion: marking and spacing bias; switch bias; total peak; early peak; late peak.
8. Two types of inputs and outputs. One is the polar/neutral isolated inputs and outputs. This is for operation at 300 volts polar or 150 volts neutral at 100 milliamperes maximum loop current. The second is low level MIL-STD 188B inputs and outputs for operation at  $\pm 6$  volts with 20 milliamperes loop current. There is a switch controllable 2 kHz low pass input filter. This filter can be switched in or out from 30.0 up to 199.9 baud. It is automatically switched out at 200 baud and above.
9. Seven-segment LED display on the front panel.
10. A PROM programmer is contained in the DSA capable of programming 2708 EPROMs. The programmer has

the following features:

- (a) A copy mode of operation where a previously programmed EPROM can be copied.
- (b) A manual mode of operation where any single bit or group of bits in memory can be changed by operation of a switch. There is a display for viewing contents of that bit.
- (c) An auto-in mode where a data stream can be programmed into bit locations defined by the start and stop address switches.
- (d) The memory is designed so that the unprogrammed area may be programmed without erasing and reprogramming the entire memory.

11. There are three additional features designed into the PROM programmer at the request of the Army engineer which are not currently shown in the design specifications:

- (a) A delete mode where any bit or bits can be deleted from memory and the programmed bits above moved downward leaving the unprogrammed area at the top.
- (b) An insert mode where any bit or bits can be inserted into memory and the previously programmed bits above moved upwards into unprogrammed area of memory.
- (c) A verify mode where the contents of an

EPROM can be verified against another EPROM or the EPROM that has just been reprogrammed.

12. The memory is accessible from any specified bit location to any other specified bit location. This area of memory is defined by the start/stop switches. An additional requirement is that no bits in memory will be unusable.

The most significant enhancement to the GGM-16 and GGM-21 is the PROM programmer and all its modes of operations as described in items 10, 11 and 12 above. This enhancement--itself a system--represents a large portion of the DSA and a full discussion is provided in Chapter IV. While the PROM programmer is the largest single enhancement, many of the other features of the GGM-16 and GGM-21 were enhanced in the DMG and DSA.

Item 1 which is the pseudo-random pattern generators from the GGM-16 and GGM-21 had minor enhancements; namely, the addition of a 2708 EPROM memory and the storage of the 2047 pseudo-random pattern in the EPROM.

Item 2(c) is an enhancement to the messages. This enhancement adds versatility to the test system by allowing the tester to use any message he desires up to 8k bits.

Items 5 and 6 represent another significant enhancement, that of increasing the speed of the data by a factor of 10 while keeping distortion measurements at the same percentage. The baud rate for the DMG and DSA are specified

as two ranges. The first range is the same as for the GGM-21 and includes those specific baud rates of the GGM-16 as shown in Table I; therefore, the second range is the enhancement.

The last enhancement is in item 8, that of the 2 kHz low pass input filter. The filter is controlled by a switch (in or out) up to 199.9 baud and is automatically switched out for any baud rate greater than 200 baud.

### Design Preparations

A large amount of the preparation for the design required reviewing several logic data books to optimize the logic design. Among these were the CMOS handbooks,<sup>1,2</sup> Low-Power Schottky data handbook,<sup>3</sup> and microprocessor handbook.<sup>4</sup> In addition to these I reviewed some text books on the design of phase-locked loops<sup>5,6</sup> and data transmission.<sup>7</sup> Other

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<sup>1</sup>Motorola Technical Information Center, Motorola CMOS Integrated Circuits, Series C (Phoenix: Motorola Incorporated, 1978), pp. 4-3 - 5-5.

<sup>2</sup>RCA COS/MOS Integrated Circuits (Somerville, N.J.: RCA Corporation, 1977), pp. 34-49.

<sup>3</sup>Motorola Technical Information Center, Motorola Low-Power Schottky TTL, Series B (Phoenix: Motorola Incorporated, 1977), pp. 1-2 - 2-8.

<sup>4</sup>Motorola Technical Information Center, The Complete Motorola Microcomputer Data Library, Series A (Phoenix: Motorola Incorporated, 1978), pp. 1-36 - 1-55.

<sup>5</sup>RCA COS/MOS Integrated Circuits, pp. 150-153.

<sup>6</sup>Motorola Technical Information Center, Motorola CMOS Integrated Circuits, pp. 7-124 - 7-128.

<sup>7</sup>William R. Bennett and James R. Davey, Data Transmissions (New York: McGraw-Hill, 1965), pp. 260-267.

reference sources included application notes.<sup>8,9</sup> This was my first design using CMOS logic. Since completing this design, I have used Low-Power Schottky in designs at MPI. I shall describe later in this chapter my reasons for choosing to use the CMOS logic.

The first step in the design required the selection of the logic family from which the system would be designed. The choice of logic family appeared to be one of three: one was T<sup>2</sup>L Low-Power Schottky circuits; the second was CMOS; the third was the LSI type of I<sup>2</sup>L (Ion Injection Logic) which would make the logic special purpose, similar to some of the circuits in the GGM-21. The I<sup>2</sup>L was dropped due to the cost per system and lead time requirements for this design. The contract was for 60 units; thus, cost effectiveness could not be met with the I<sup>2</sup>L.

A secondary consideration was a clause regarding heat inside the units. Should the logic consume too much power, the units would require a cooling fan. This would also increase the cost of the units. Figure 2 (page 12) is a graph of power dissipation comparing Low-Power Schottky to CMOS. The maximum frequency in the system will be 10<sup>6</sup> Hz. Only a small amount of the logic would be required to run at

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<sup>8</sup>Marvin K. Vander Kooi, ed., Linear Applications, Vol. 1 (Santa Clara, Calif.: National Semiconductor Corporation, 1973), pp. AN46-1 - AN46-12.

<sup>9</sup>Forest L. Sass, ed., Linear Applications, Vol. 2 (Santa Clara, Calif.: National Semiconductor Corporation, 1976), pp. LB30-1 - LB30-2.

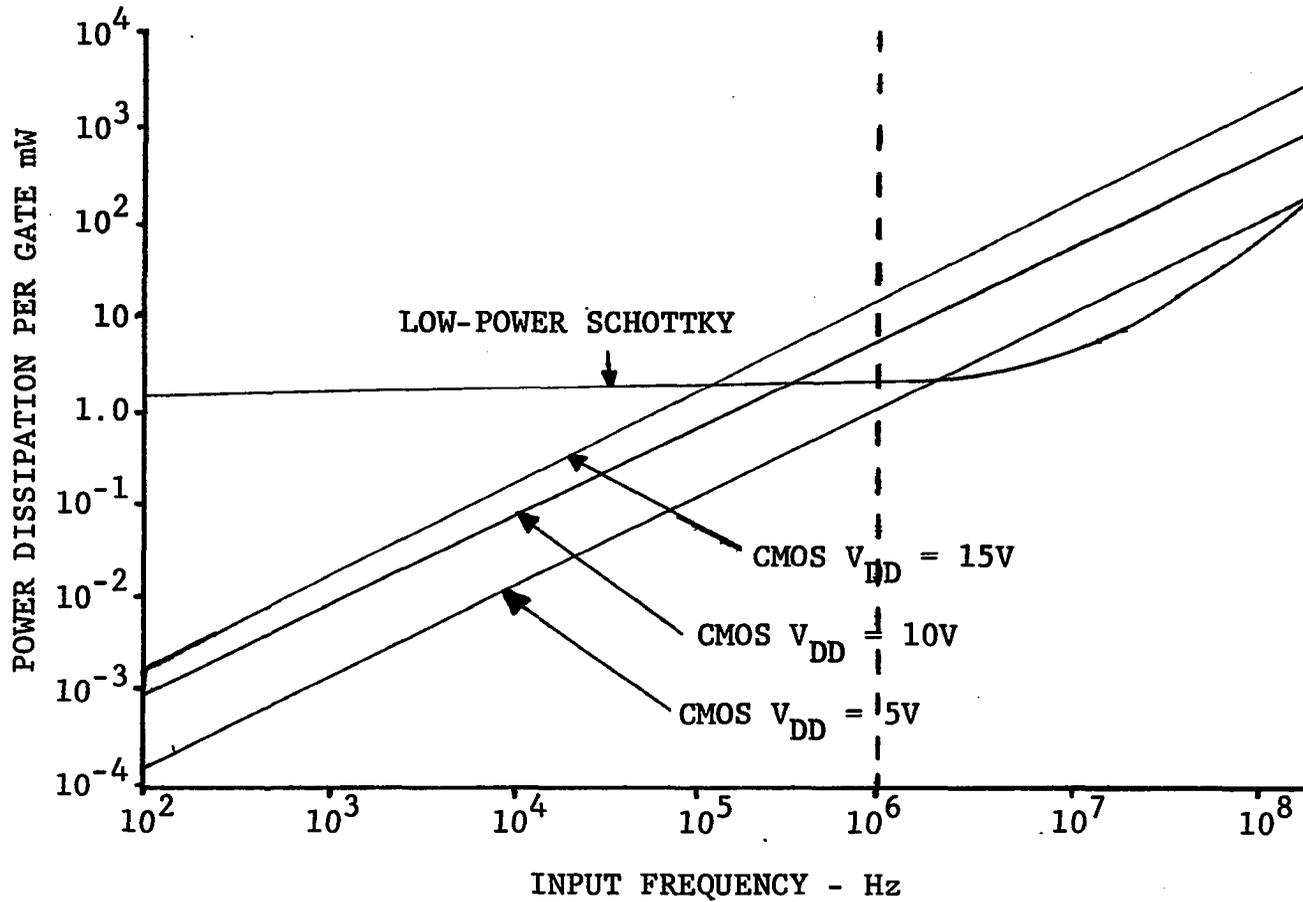


Figure 2. Low-Power Schottky vs CMOS Power Requirements

this frequency. Thus, assuming some Gaussian distribution of frequencies, the CMOS would require less power.

The CMOS has a disadvantage in regard to rise, fall, and propagation time. Figure 3 (shown below) is a graph of time delays for a typical gate of CMOS. From Figure 3 the operating voltage of +12 volts was chosen. In the +12 V range the rise, fall, and propagation times are near ideal values for CMOS. An advantage of CMOS is the larger scale of integration and larger selection of complex functions. This advantage allowed a reduction in number of chips, thus reducing the number of printed wiring assemblies (PWAs) needed in the units.

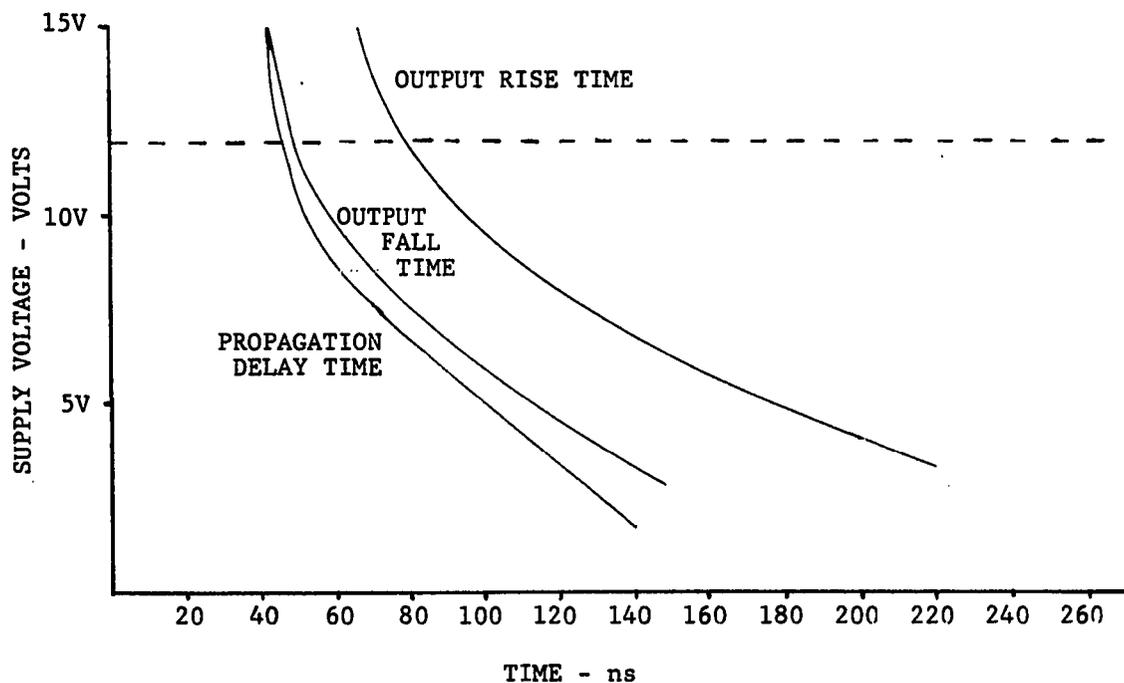


Figure 3. CMOS Rise, Fall, and Propagation Time

## II. DIGITAL MESSAGE GENERATOR

### Physical Description

The DMG has nine printed wiring assemblies (PWAs) inside the unit. These PWAs are five inches high and ten inches long with a 60 pin connector on one end. These PWAs can have a maximum of 34 integrated circuits. (The DSA has twelve of these PWAs.)

The PWAs were made this size in order that they could slide into a PWA rack inside the seven inch high unit. The front panel of the unit is hinged which enables it to drop forward in order that the PWAs can be replaced if necessary, or placed on an extender card for testing.

Figure 4 (page 15) is the front panel for the DMG. The switches on the panel are all mounted on printed wiring boards (PWBs). The PWAs are then mounted to the front panel. The PWAs have mass termination connectors in order that the ribbon cable can be routed to the logic. The thumbwheel switches are for the start memory location, stop memory location, and the distortion percent. The first four thumbwheel switches are the START ADDRESS. These are valid for decimal numbers from 0000 to 8191. Any setting beyond the 8191 is an invalid address. The STOP ADDRESS switches are

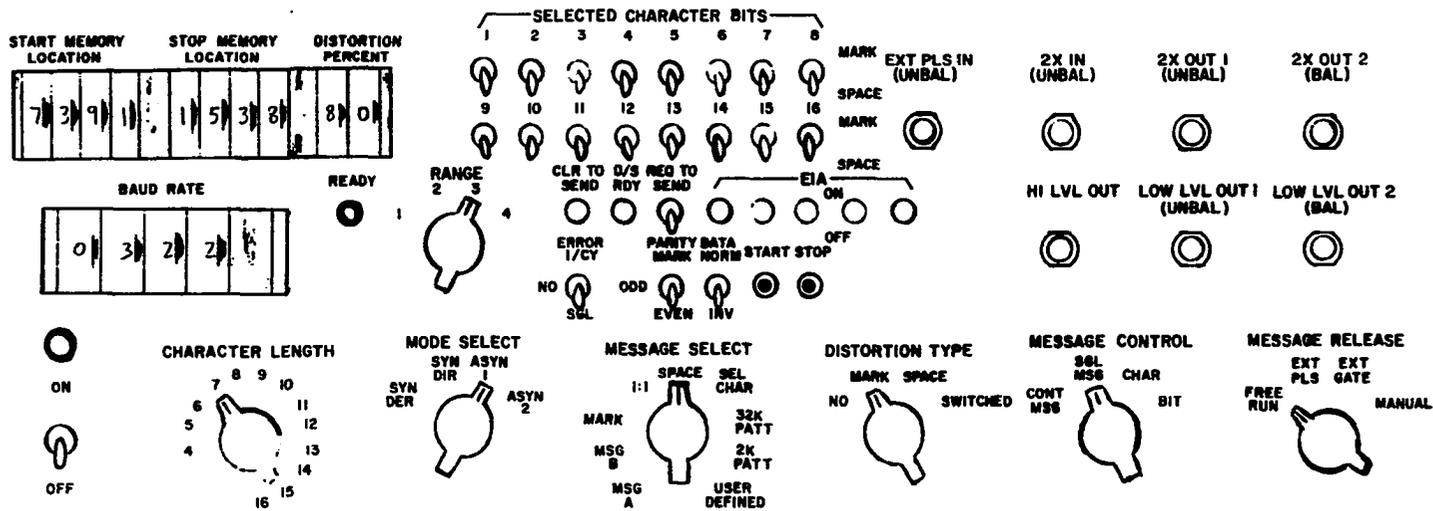


Figure 4. Front Panel of the DMG

the next four switches. Their function is similar to the start switches except they are the stop address. The start/-stop switches together define the portion of the memory which is to be used for generation of test data.

The next two thumbwheel switches are the DISTORTION PERCENT switches. These determine the percentage of distortion (from 0 to 49%) that the output signal has had added to the ideal output signal. The type of distortion is determined by the distortion type switch. There are four positions on this switch to select the following types:

1. NO - This selection will cause no distortion in the generated signal.
2. MARK - This will cause mark bias distortion (Figure 1) to be induced into the generator output signal to the percentage shown on the thumbwheel switches.
3. SPACE - This will cause space bias distortion (Figure 1) to be induced into the generator's output signal to the percentage shown on the thumbwheel switches.
4. SWITCHED - This will cause switched bias distortion to be induced into the generator signal to the percentage shown on the thumbwheel switches. Switched bias is first one character with mark bias then one character with space bias. Figure 5 (page 17) shows

Y CHARACTER BAUDOT CODE

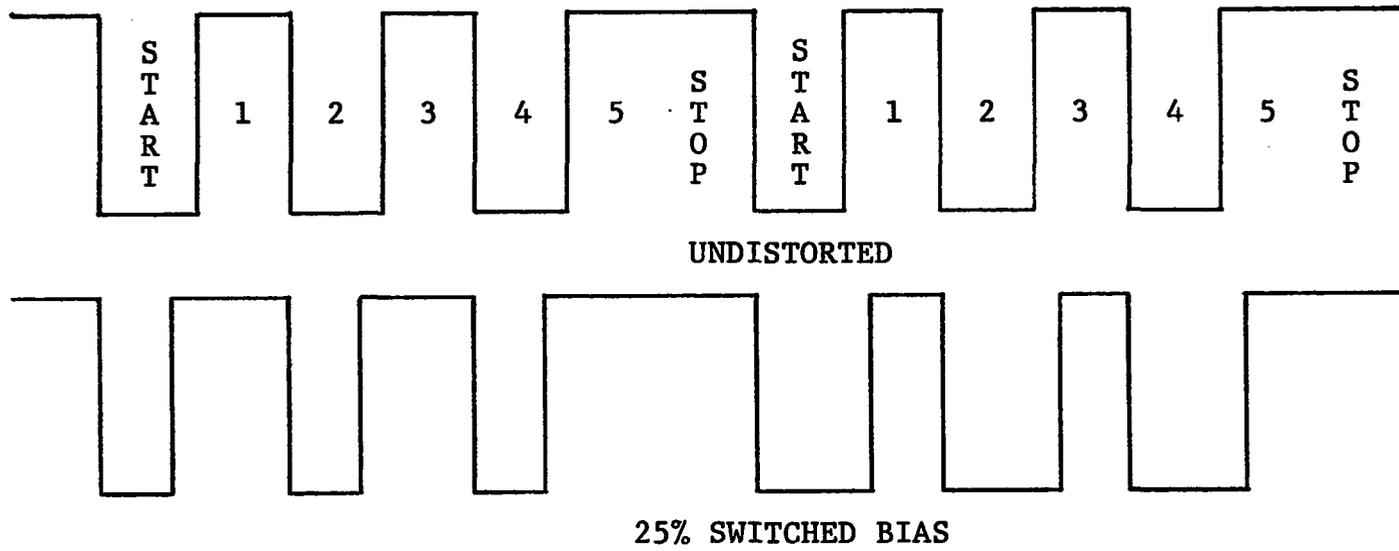


Figure 5. Switched Bias Distortion

how two characters would be affected by switched bias.

The last set of thumbwheel switches are the BAUD RATE switches. There are five switches which determine the baud rate of the master clock. In conjunction with the thumbwheel switches is the RANGE switch which is a multiplier for the thumbwheel switches. The baud rate is specified to operate between 30 and 99,990 baud; however, the logic will operate at any baud rate set on the switches. The lower baud rates below 30 baud are considered error conditions and are not required to meet clock jitter requirements. To aid the test technician LEDs are mounted inside and near the bottom of each thumbwheel switch. The RANGE switch logic illuminates the correct LED for a decimal point. Thus, the technician can take a direct reading of the baud rate selected by both the thumbwheel switches and the range rotary switch.

The LED between the BAUD RATE switches and the RANGE switch is the "Ready" indicator. This illuminates when the conditions on the front panel have been satisfied by the logic. If the "Ready" LED has not illuminated within 20 seconds, some setting on the panel is incorrect.

The sixteen toggle switches are the SELECTED CHARACTER BITS. These are set for the desired bit pattern for a character and when the MESSAGE SELECT switch is in "Sel Char" the bit pattern is transmitted. The character can be from

4 bits to 16 bits long depending on the setting on the CHARACTER LENGTH switch. These work either in the asynchronous (start/stop) mode or in the synchronous mode. The mode is determined by the setting on the MODE SELECT switch. The synchronous mode is a continuous stream of bits. There are two types of synchronous modes. One is a direct (external) 2X clock while the second is a derived (internal) 2X clock. These are indicated by "Syn Dir" for the external 2X clock and "Syn Der" for the internal 2X clock. The asynchronous (start/stop) mode has two choices. The first, "Asyn 1", has only one stop bit. The second, "Asyn 2", has two stop bits.

The message switches are the controls for the pattern that will be generated by the DMG. The message select switch defines the message to be generated into a data stream. The switch has nine positions and has the following names.

First, the "Msg A" position is a message used as a typing drill which uses all the characters in the alphabet. The message is called the "Quick Brown Fox." The message will print on the teletype or printer as follows:

(carriage return line feed)

TEST DE (7 "deletes" 5 "spaces")

(carriage return line feed)

THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG

(3 "spaces") 1234567890 TIMES END (20 "spaces")

Message A is an eight bit ASCII code as shown in Figure 6

## ASCII CODE

BIT 7			•	•					
BIT 6		•		•	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5
	NULL	SP	@						
	SOH	1	A	a	•				
	STX	"	B	b		•			
	ETX	#	C	c	•	•			
	EDT	\$	D	d			•		
	ENQ	%	E	e	•		•		
	ACK	8	F	f		•	•		
	BELL	'	G	g	•	•	•		
	BS	(	H	h				•	
	HT/SK	)	I	i	•			•	
	LF	*	J	j		•		•	
	VT	+	K	k	•	•		•	
	FF	'	L	l			•	•	
	CR	-	M	m	•		•	•	
	S0	.	N	n		•	•	•	
	S1	/	O	o	•	•	•	•	
	DLE	0	P	p					•
	DC1	1	Q	q	•				•
	DC2	2	R	r		•			•
	DC3	3	S	s	•	•			•
	DC4(STOP)	4	T	t			•		•
	NAK	5	U	u	•		•		•
	SYNC	6	V	v		•	•		•
	ETB	7	W	w	•	•	•		•
	CAN	8	X	x				•	•
	EM	9	Y	y	•			•	•
	SUB		Z	z		•		•	•
	ESC		[	{	•	•		•	•
	FS	<					•	•	•
	GS		]	}	•		•	•	•
	RS	>		~		•	•	•	•
	US	?		DEL	•	•	•	•	•

• is Mark or 1

Figure 6. ASCII Code Table

(page 20) and is stored in the PROM. The PROM addresses are selected by the selection of the "Msg A" position on the MESSAGE SELECT switch.

Message B is the same "quick brown fox" message; however, it is in five-bit Baudot code (see Figure 7, page 22). Again the message is stored in the PROM and the addresses are selected by the positioning of the MESSAGE SELECT switch to "Msg B". The next three positions are test signals. "Mark" is a continuous mark. The length of the mark is controlled by the CHARACTER LENGTH switch with start and stop bits in the asynchronous mode. "1:1" is a string of reversals; that, one mark followed by a single space followed by another mark. The length is determined by the CHARACTER LENGTH switch. The start and stop bits are inserted in the asynchronous mode. In the asynchronous mode the CHARACTER LENGTH switch will determine when the stop and start bits are generated. The third position is "Space" which is a continuous space just like the "Mark" described above.

The last three positions on the MESSAGE SELECT switch are patterns. The first, a 32k pseudo-random pattern ( $2^{15}$  bits), is generated by logic. The second, a 2k pseudo-random pattern ( $2^{11} - 1$  bits), is in the PROM and the addresses are selected by the logic. The last position is "User Defined". "User Defined" is the portion of the PROM addresses above the location of the message A, B, and 2k

## BAUDOT CODE

UPPER CASE	LOWER CASE	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5
-	A	•	•			
?	B	•			•	•
:	C		•	•	•	
\$	D	•			•	
3	E	•				
!	F	•		•	•	
8	G		•		•	•
STOP	H			•		•
^	I		•	•		
'	J	•	•		•	
(	K	•	•	•	•	
)	L		•			•
	M			•	•	•
/	N			•	•	
9	O				•	•
0	P		•	•		•
1	Q	•	•	•		•
4	R		•		•	
BELL	S	•		•		
5	T					•
7	U	•	•	•		
	V		•	•	•	•
2	W	•	•			•
/	X	•		•	•	•
6	Y	•		•		•
	Z	•				•
BLANK	BLANK					
C.R.	C.R.				•	
L.F.	L.F.		•			
SPACE	SPACE			•		
LTH SHIFT	LTH SHIFT	•	•	•	•	•
FIG SHIFT	FIG SHIFT	•	•		•	•

• is Mark or 1

Figure 7. Baudot Code Table

pattern. They are selected from the start/stop switches as described in Table II (shown below). "User Defined" can be any or all of the PROMS. This position allows special PROMS to be installed with special messages or test patterns which the test technician wishes to use for his tests. A detailed description of this function is included in the PROM programmer chapter.

TABLE II  
MEMORY ADDRESS FOR PROM

<u>Msg Sel Sw Positions</u>	<u>Start Byte Address</u>	<u>Stop Byte Address</u>	<u>Start Sw Setting</u>	<u>Stop Sw Setting</u>
Message A	0	127	0	1023
Message B	128	207	1024	1663
2k Pattern	208	719	1664	5759
User Defined	720	1023	5760	8191

The MESSAGE CONTROL switch is used to control the method by which the message will be generated. It also works in conjunction with the MESSAGE RELEASE switch. The MESSAGE CONTROL switch has four modes. The first is "Cont Msg" (continuous message) which causes a repeat of the message each time it has cycled through the programmed length. The second is "Sgl Msg" (single message). Only one complete message is generated each time the switch is pushed or one of the MESSAGE RELEASE switch options is used. The third position is "Char" (character). Only a

single character is generated for each operation. The fourth position is "Bit". This releases a single bit for each operation.

The MESSAGE RELEASE switch is used to determine the method by which the MESSAGE CONTROL is started. "Free Run" is the first position and causes the logic to run unrestricted. The "Ext Pls" (external pulse) position allows the message to start when an external pulse is applied. The "Ext Gate" (external gate) allows the message to run while the gate signal is high. The last position, "Manual", allows the start and stop buttons to be operated for a message to be generated.

There are some special function switches on the front panel used for different types of tests. The ERROR 1/CY (error one per cycle) switch is a three position switch which induces a single error, no error, or errors at the rate of one per each cycle. The down position will induce a single error in the message data stream. The up position causes an error to be induced with each cycle. The error is induced once for each message or once per character when the MESSAGE SELECT switch is in the "Sel Char" (selected character) position. The center position causes no errors to be induced in the data stream.

The second switch is also a three position switch used for parity. The center position is for "Odd" parity while the down position is for "Even" parity. The up

position is called "Mark" which causes a mark to be transmitted for the parity bit. The last special switch is the DATA switch. The up position is "Norm" (normal data); in the down position the data stream is "Inv" (inverted).

Figure 8 shows the back panel of the DMG. The switches at the top are for the system clocks. The bit rate clock is called the 2X clock while the master clock is 1 MHz (one Megahertz). The switch 2X OUT in either "Norm" or "Inv" position causes the 2X clock output signal on the front panel jack to be normal for "Norm" or inverted for "Inv". The second 2X OUT switch in the "Cont" position selects the bit rate clock or in the "Data" position selects the data stream to be the output. The 2X IN switch in "Norm" or "Inv" indicates which way the input 2X signal is used, either normal ("Norm") or inverted ("Inv"). The EXT PLSE switch in "Norm" or "Inv" indicates the normal ("Norm") or inverted ("Inv") pulse used to trigger events in the generator. The last switch, 1 MHz, selects the master clock either internal ("Int1") or external ("Ext").

The back panel is hinged for inserting a PWA inside the generator when the ultraviolet lamp is used to erase the EPROMs. The EPROMs are placed inside the DMG cabinet, the back panel is closed, and the UV lamp is turned on. After twenty minutes the EPROMs will have completed the erasure process and are ready for programming.

The power input is 115 VAC or 230 VAC from 50 to

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16. Other \_\_\_\_\_

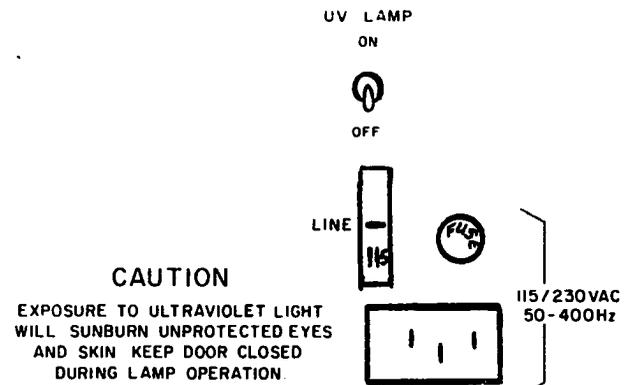
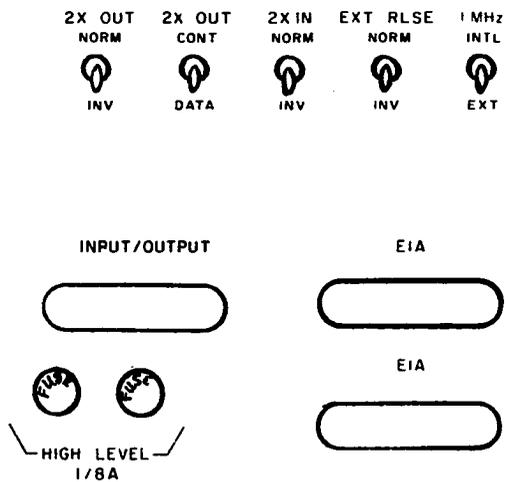
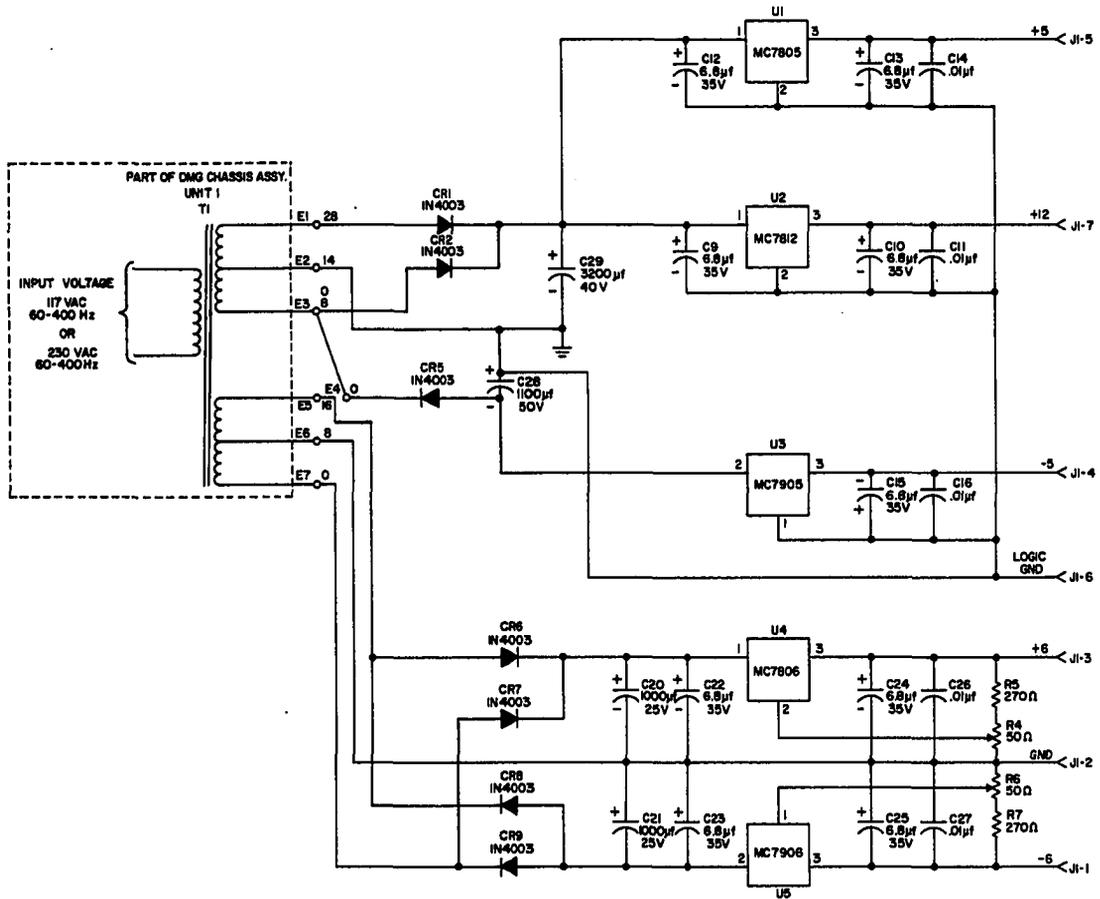


Figure 8. Back Panel of the DMG

400 Hertz. The input power is selectable on the switch; down is 115 VAC and up is 230 VAC. The switch has the numbers 115 or 230 visible for the position in which the switch is operated. The switch connects to the taps of the transformer, and when the AC is present, the proper transformer tap is selected. The power supply is similar for both the DMG and the DSA. The same transformer and power supply PWA is used in each unit, but the power supply PWA has the unused regulators left off when installed in the DMG.

Figure 9 is the schematic diagram of the DMG power supply. The power supply is a typical transformer, rectifier, filter and integrated circuit regulator. The +12 volt regulator and the +5 volt regulator are isolated from the frame of the generator or analyzer and mounted on a heat sink. The -5 volt supply is used only for the 2708 EPROMs, thus requires a very low current. The +6 volt and -6 volt supplies are used for the I/O and require a maximum of only 20 milliamps per output. The +5 volt supply in the DMG is used for the 2708 EPROMs and interface logic to the EPROMs. The +12 volt supply has two functions. One is to power the logic and the 2708 EPROM; the second is to power the LED indicators. The UV lamp switch is used to turn the UV lamp on or off. Above the AC input plug is the input power fuse, a 1 ampere slow-blow type fuse.

In the lower left corner are the I/O connectors. These connectors are wired directly to the front panel jacks



NOTE: PREFIX ALL REFERENCE DESIGNATIONS, EXCEPT T1, WITH 1A19.

Figure 9. Power Supply Schematic  
Diagram for the DMG

and use a twisted pair wire for the I/O signal. Telephone type tip and ring plugs are needed for the front panel. Below the connectors are 1/8 ampere fuses for the two high level outputs. These will be discussed in the I/O circuits later in this text.

### Logic Description

Figure 10 is the major block diagram for the DMG. The master clock in the system is a 1 MHz signal, derived from a 4 MHz oscillator. The clock for generating the baud rates is a phase-locked loop (PLL) which creates a 2X clock which is used as the baud rate clock, a 20X clock which is ten times the baud rate clock, and a 200X clock which is 100 times the baud rate. The value of the baud rate switches is used to preset the counters, which are used as a scaler in the PLL circuit. The circuit is a typical PLL circuit using a voltage controlled oscillator (VCO) and counters for the scaler. The reference frequency--the 100 Hertz reference frequency for the MC14046--is developed from the 4 MHz crystal oscillator using flip-flops and decade counters. The output of the VCO clocks the baud rate switch counters to produce a 200X clock. The VCO output is used also as a clock to a two stage decade counter to create a 20X clock. The RANGE switch is decoded as the select lines of a one-of-four multiplexer. The output of the counters is the input to the multiplexer. The RANGE switch selects the multiplexer inputs for either the 10 times or 100 times baud

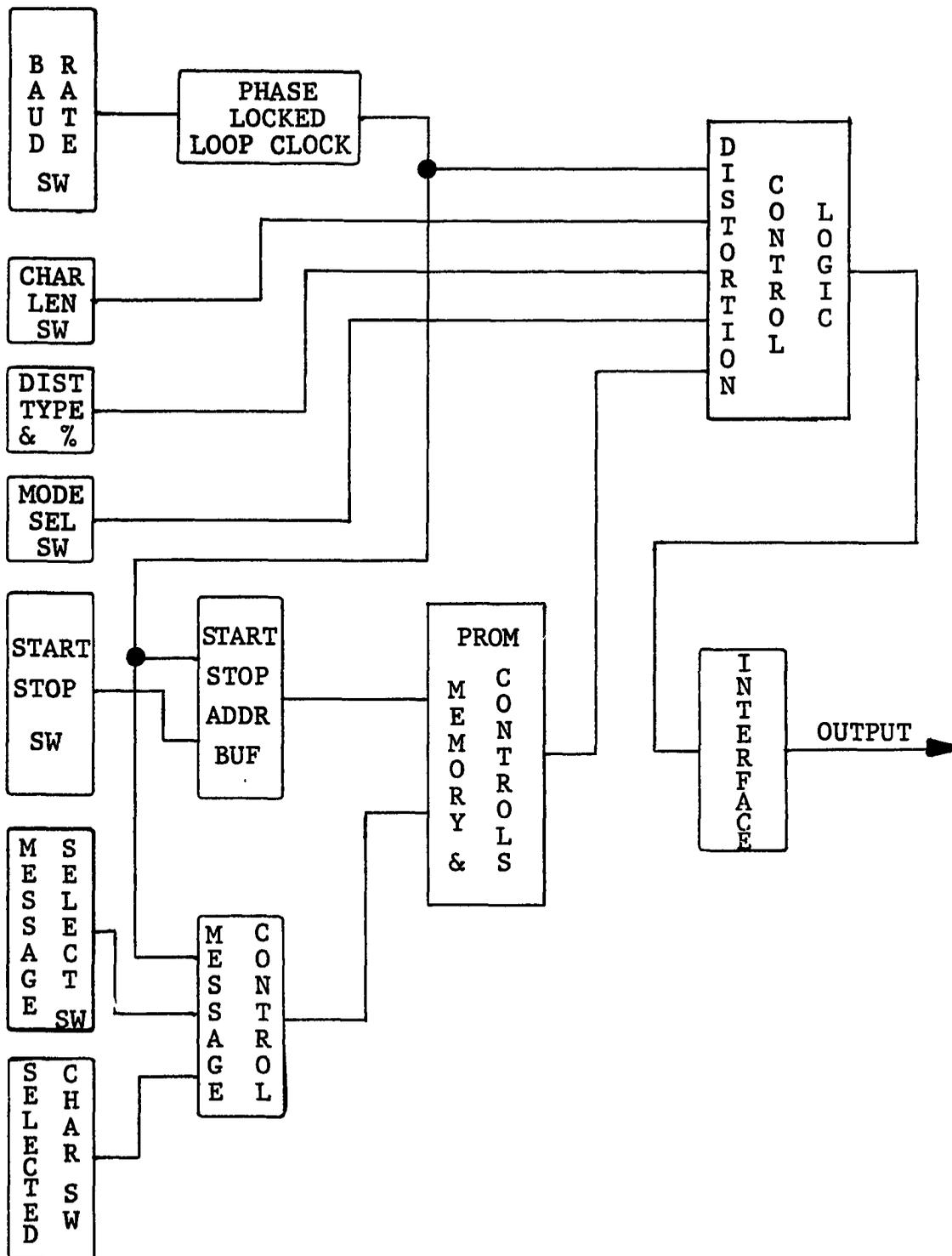


Figure 10. Digital Message Generator Block Diagram

rate clock. The 100 times baud rate clock (200X clock) is used for the three lower ranges 0 to 100, 100 to 1k and 1k to 10k. For the 10k to 100k range the 10 times baud rate clock (20X clock) is used. This meets the specifications and allows the logic to have a minimum of a 10 phase clock (ten 1 MHz cycles are generated for each of the highest baud rate clocks). The same clock circuit is also used in the DSA unit.

One of the features of the system is to be able to use an external clock. The external clock could be a 1 MHz standard clock used to test the jitter of the phase-lock loop oscillator and also to verify the logic response to an external master clock. The external 2X clock can be used from another unit in testing either distortion or transmission delays.

The three major clocks in the unit are the 1 MHz master clock, the 2X (baud rate) clock, and either the 200X or the 20X (depending on the selected range) clock. All signals are synchronized to the 1 MHz clock. The baud rate clocks can be derived from the phase-locked loop clock. The 2X clock is used as the bit rate clock and the 200X or 20X clock is used in generating the distortion measuring signals.

The distortion control logic, as shown in Figure 10, is the logic that pulls all the other blocks in Figure 10 together to create the output signal. In asynchronous mode (MODE SELECT switch in "Asyn 1" or "Asyn 2") the start and

stop bits are added by this logic. The distortion control needs inputs from the message control and memory control, from which it constructs the data signal. The input from the CHARACTER LENGTH switch is encoded from a 1 of 16 switch to four-bit binary code and loaded into a binary down counter. Each time the counter reaches zero a character length pulse is generated and the counter is reloaded for the next character cycle. The character length pulse is used in generating the stop and start bits in the asynchronous mode. The MODE SELECT switch determines if the mode is either synchronous or asynchronous with one or two stop bits.

The block called DIST TYPE and % SELECT are the inputs that select the type of distortion and the amount of distortion. Mark distortion is an early transition, while space distortion is a late transition. The switch distortion is a J-K type flip-flop with its output tied back to its input. This causes the distortion to be mark distortion for one cycle, then space distortion for the next. The clock to the switched distortion flip-flop is the character length pulse; thus, every other character has either an early or late transition. The inputs from the DISTORTION PERCENT switches are one set of inputs to two four-bit magnitude comparators cascaded in series. The other input to the comparators is the output from the distortion counter. Thus, the output of the comparators is active when the distortion in the counter is equal to the setting on the DISTORTION

PERCENT switches.

Figure 11 shows the 2X clock period with distortion types and percentages. The falling edge of the 2X clock starts the cycle. The next falling edge of the 2X clock completes this cycle and starts the next. The distortion counter is a two stage up-down decade counter. The counter is preloaded to fifty at the falling edge of the 2X clock. The 200X (or 20X) clock is used as the counter clock. The counter counts down until it reaches zero, which occurs at the rising edge of 2X clock. The counter control is changed to up count and the counter counts up to fifty. The distortion type control enables the comparators during the portion of the bit cycle either early or late as shown in Figure 11. When a compare results, the output signal is gated to allow a transition, if required.

When the 20X clock is selected, only the tens stage of the counter and comparators is active. The low order bit is used and converts the unit's digit output to either zero or five. The distortion is in 5% increments in this range. Figure 12 shows the relationship of the 2X clock to the 20X clock. If the RANGE switch is set from 1 to 3 the 200X clock would be used. For each pulse in Figure 12 there would be 10 pulses.

The next block in Figure 10 would be the PROM memory and controls. This includes the EPROM, the 32k pseudo-random pattern generator and the controls for both. The

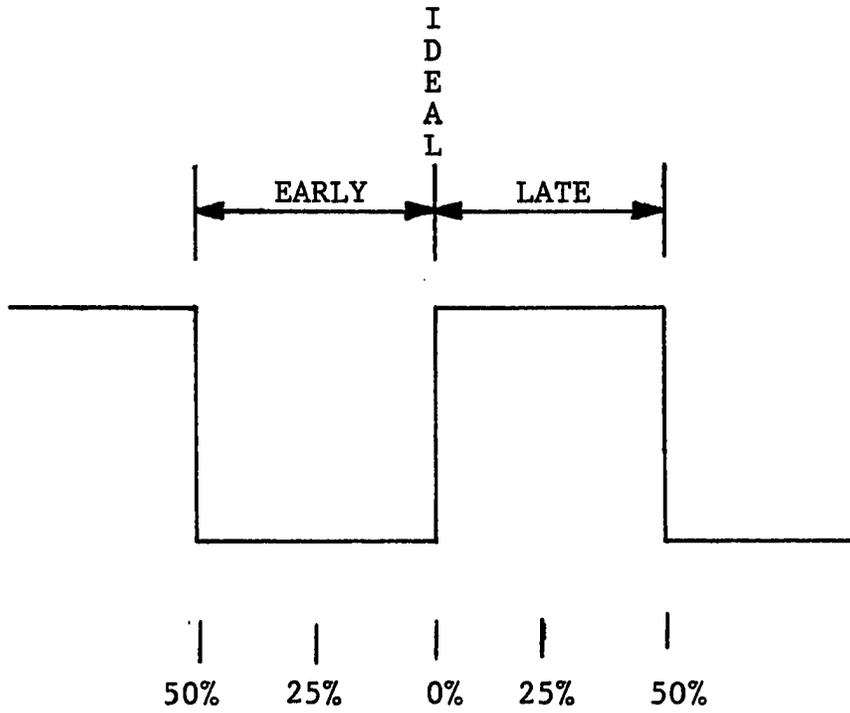


Figure 11. 2X Clock Period

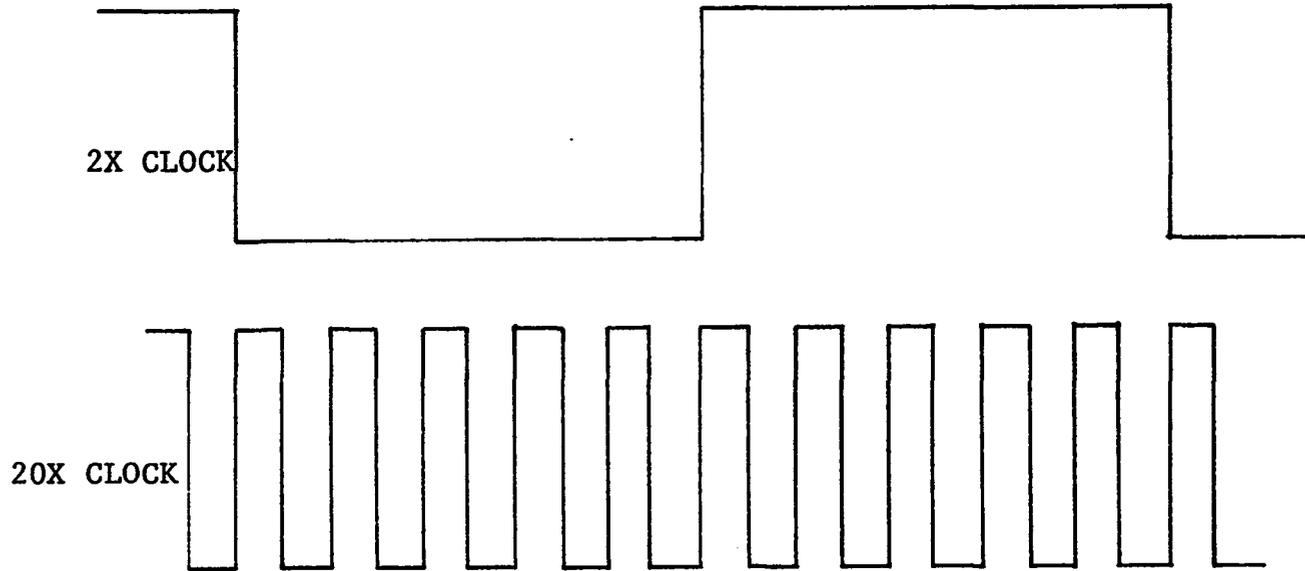


Figure 12. 2X Clock and 20X Clock

MESSAGE SELECT switch determines which of the following will be selected: the 32k pseudo-random pattern generator, the SELECTED CHARACTER BITS switches, or the START/STOP switches which control the EPROM addresses. The MESSAGE SELECT switch is decoded to the various start and stop addresses for the message A, ("Msg A"), message B ("Msg B"), 2047 pseudo-random pattern ("2k Patt"), and the "User Defined". The decode is performed as the select lines of a one-of-four multiplexer.

The SELECTED CHARACTER BITS switches, when selected by the MESSAGE SELECT switch, are transmitted per the conditions of the MESSAGE CONTROL switch. The 32k (15 bit) pseudo-random pattern was designed as a 15 bit shift register with exclusive-OR of the outputs as follows. The first 14 outputs are all ORed together so that when any of the outputs are ones, the result would be a one. Output 14 is exclusive-ORed with this result. The output of this logic is then exclusive-ORed with the output of bit 15. The output of this combination logic of 14 and 15 is inverted and fed back as the input to the shift register. The control to the shift register is a counter which counts to 16 then locks the feedback to the input. Before the circuit locks to the feedback signal, the SELECTED CHARACTER BITS switches are the input to the shift register. Figure 13 shows a representative block diagram of the 32k pseudo-random pattern generator.

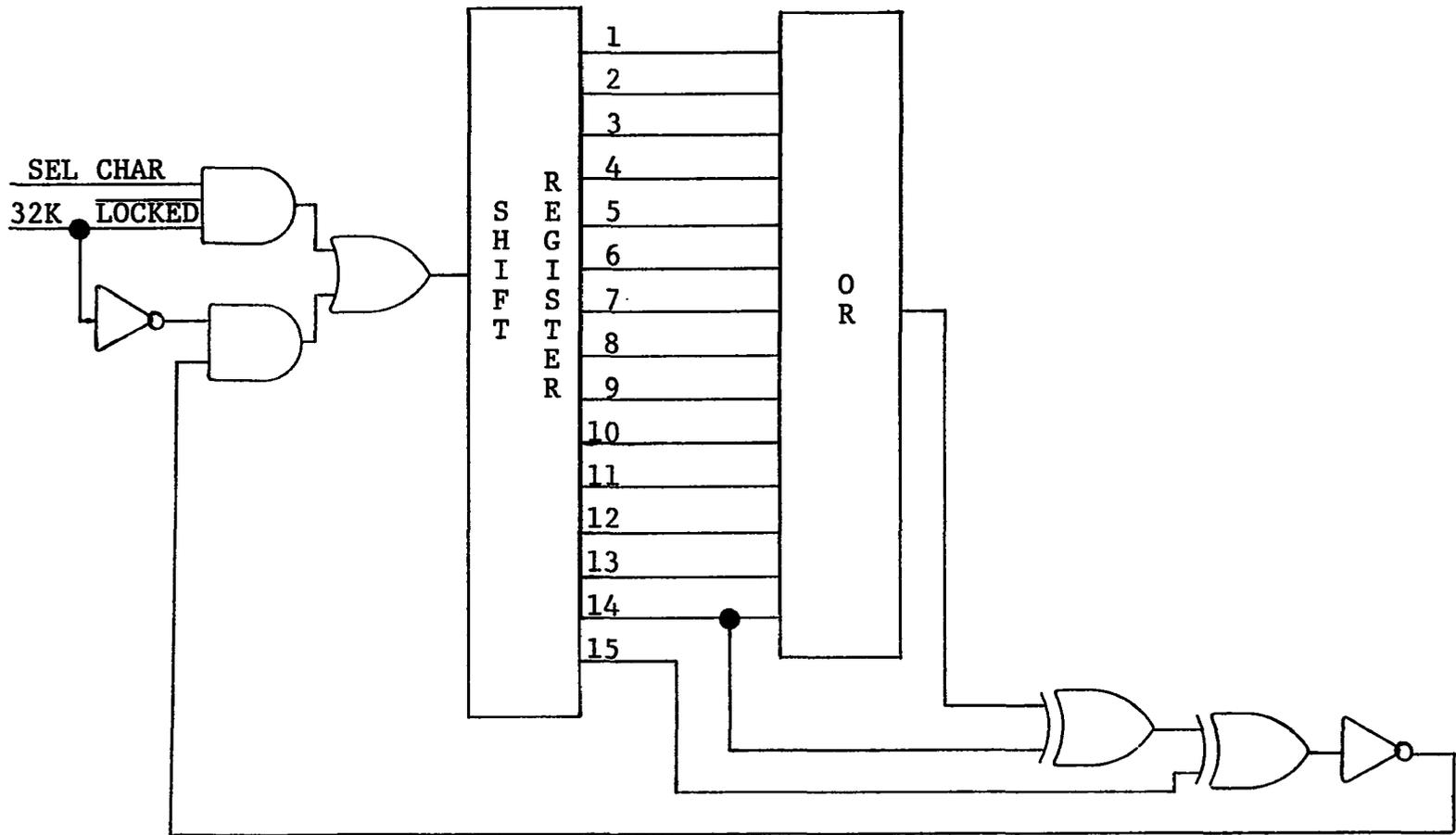


Figure 13. 32K Pseudo-Random Pattern Generator

A requirement for the START/STOP switches was for the logic to automatically follow the address on the switches whenever they are changed. An additional specification requirement was that every bit in the EPROM be addressable making every bit accessible to the test technician. The address display for each bit must be decimal, requiring a decimal-to-binary conversion and a counter stage which can be incremented by the logic.

The start and stop thumbwheel switch output is parallel loaded into a four stage decade down counter. Using the 1 MHz clock, it is down counted to zero. While the decade counter is counting down a stage of binary up counters is counting up. When the decimal down counter reaches zero the binary up counters are loaded into a buffer. The down counter is then parallel loaded to the value of the switches, the binary counter is reset to zero. This circuit is used for both the start and stop switches for the DMG and the DSA units. The difference in the start and stop is the buffer. The buffer in the start circuit is a binary up counter, while the buffer for the stop circuit is a register. Since the stop is always the value from the switches, these outputs are the input to a set of cascaded magnitude comparators.

The start buffer is a counter; therefore, the logic can control the sequencing of the addresses. The reset and preset are also controllable from the logic. The start address must be incremented when generating a message or

programming a PROM. The start control logic must be capable of preloading in order to loop through a set of addresses. The logic uses a compare of the stop switches for the trigger to start a new cycle if the MESSAGE CONTROL is in "Cont Msg".

The MESSAGE SELECT switch is encoded to the start and stop switch buffer. The message A starts at address 0000 and ends with address 0127. Message B starts at address 0128 and ends at address 0207. The 2047 bit pseudo-random pattern starts at address 0208 and ends at address 0463. The user definable area starts at address 0464 and ends at the top address of the EPROM of 1023. See Table II (page 23) for the bit address which the test technician must use.

The last part of the PROM memory and control is a register and an eight-to-one demultiplexer. The three low-order bits on the start address switch buffer constitute the bit position for the present bit of the EPROM word. The data from the EPROM is stored in a register. To get the selected bit out of the register a counter circuit develops the signals labeled S1, S2, S3, and S4. S1-S3 are the three low-order outputs of a binary counter. S4 is the last output and used to trigger another cycle of EPROM data. S1 to S3 are the controls of the demultiplexer. The data register is the input to the demultiplexer and the output becomes the selected bit. The timing is done at the rising edge of the 2X clock for counting; this allows the data bit to be ready

even if there is 49% distortion, which would be the next rising edge of the 200X clock pulse.

The logic timing to get the next EPROM data byte into the register is used to complete the address changes (either increment or reload the start address) during the last half of the 2X clock cycle when the counter is equal to seven. The address to the EPROM is either incremented, reset, or preset to the next address. This operation happens after the falling edge of the 2X clock, using the 200X or 20X clock. Thus, the address is settled and the EPROM data is presented to the register by the time the next rising edge of the 2X clock occurs. When the counter reaches S4 on the rising edge of the 2X clock, it is either asynchronously reset for the first bit of the next data byte, or preset to the start bit for restarting the message or pattern. There is a single flip-flop in the distortion controls that stores the data signal until the distortion control releases it. The data flip-flop is loaded by the falling edge of the 2X clock, using the falling edge of either the 200X or 20X clock pulse. No matter what the percentage of distortion, the data bit is always ready. Thus, on the next rising edge of either the 200X or the 20X clock, the data flip-flop can be loaded.

#### Input-Output Description

The data flip-flop is then put into the I/O circuits. Both the data and the 2X clock signals are fed into optical

couplers. These are used for the low level output and the RS-232-C<sup>10</sup> interface. The optical couplers drive the push-pull type circuits shown in Figure 14. The circuits in Figure 14 are the RS-422<sup>11</sup> and RS-423<sup>12</sup> type circuits which meet the MIL-STD-188-114. Figure 15 shows a typical circuit representation of the output. The RS-422 and RS-423 type output generators are available in integrated circuits; however, the MIL-STD-188-114 requirements for  $V_{OS}$  prevents the use of the RS-422 type integrated circuit drivers. Figure 16 illustrates the method of measuring  $V_{OS}$ . The RS-422 specification states that the magnitude of  $V_{OS}$  shall not be greater than 3.0 volts when measured between center point of test load and ground. MIL-STD-188-114 states that the magnitude of  $V_{OS}$  is less than or equal to 0.4 volts when measured between center point of test load and ground. Thus, the circuit meeting MIL-STD-188-114 also meets the RS-422, but RS-422 does not meet the MIL-STD-188-114.

The data signal and the 2X clock signal are also used as high level outputs. These are transformer coupled for isolation and are shown in Figure 17 as a typical circuit.

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<sup>10</sup>Electronic Industries Association, EIA Standard RS-232-C (Washington D. C.: Electronics Industries Association, 1969), pp. 4-18.

<sup>11</sup>Electronic Industries Association, EIA Standard RS-422 (Washington D. C.: Electronics Industries Association, 1975), pp. 3-12.

<sup>12</sup>Electronic Industries Association, EIA Standard RS-423 (Washington D. C.: Electronics Industries Association, 1975), pp. 4-15.

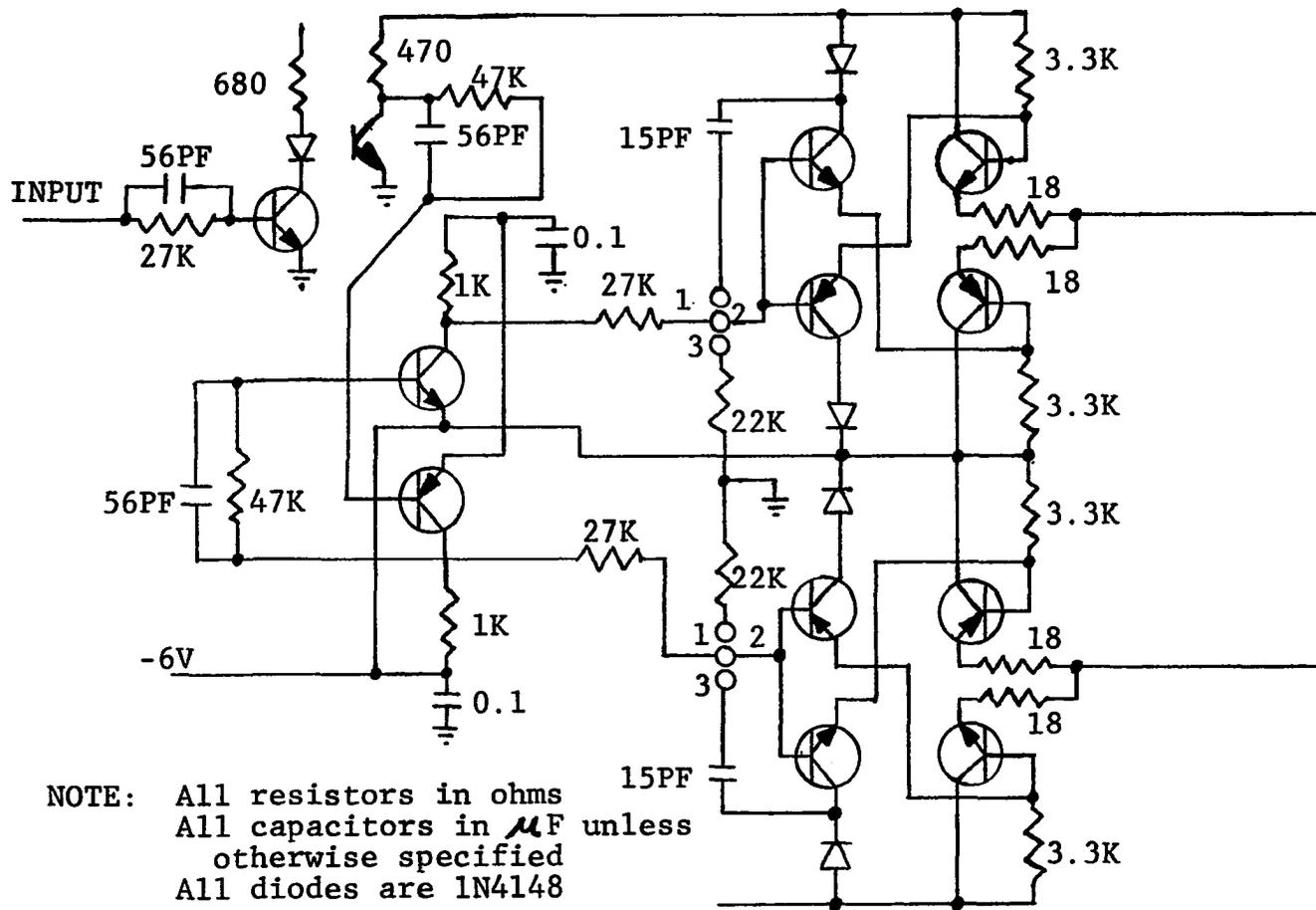


Figure 14. I/O Drivers

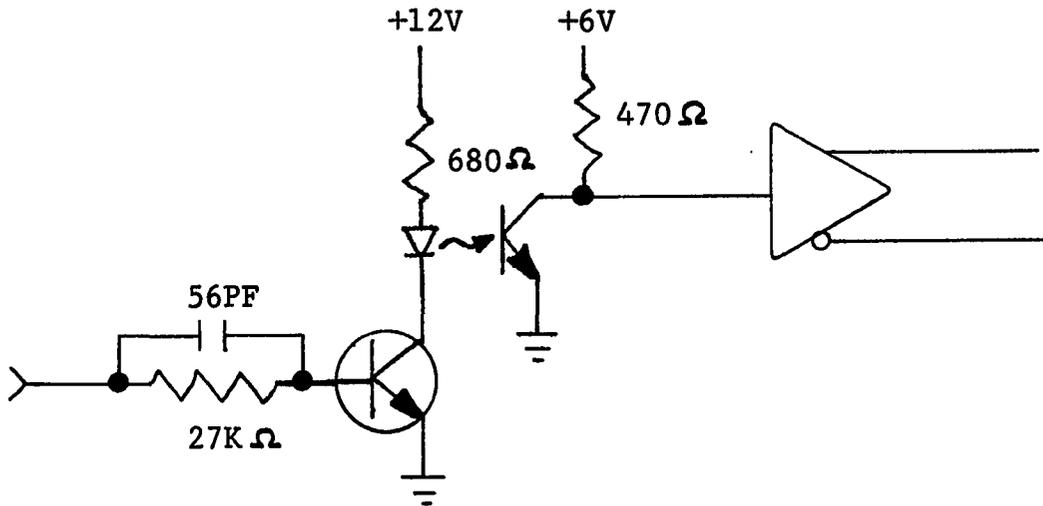


Figure 15. Typical Circuit for  
Input/Output

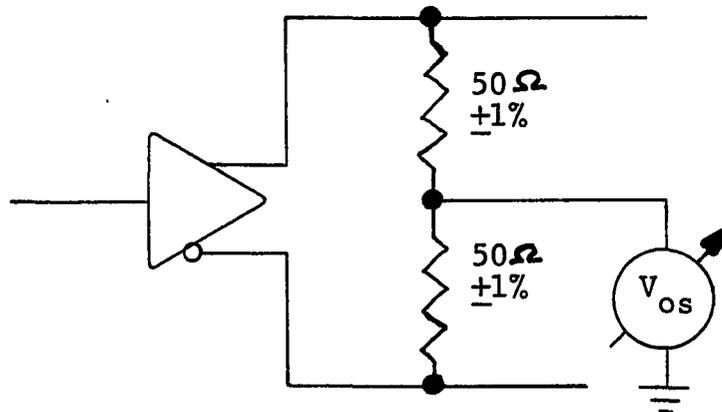


Figure 16. Generator Offset  
Voltage ( $V_{OS}$ ) Measurement

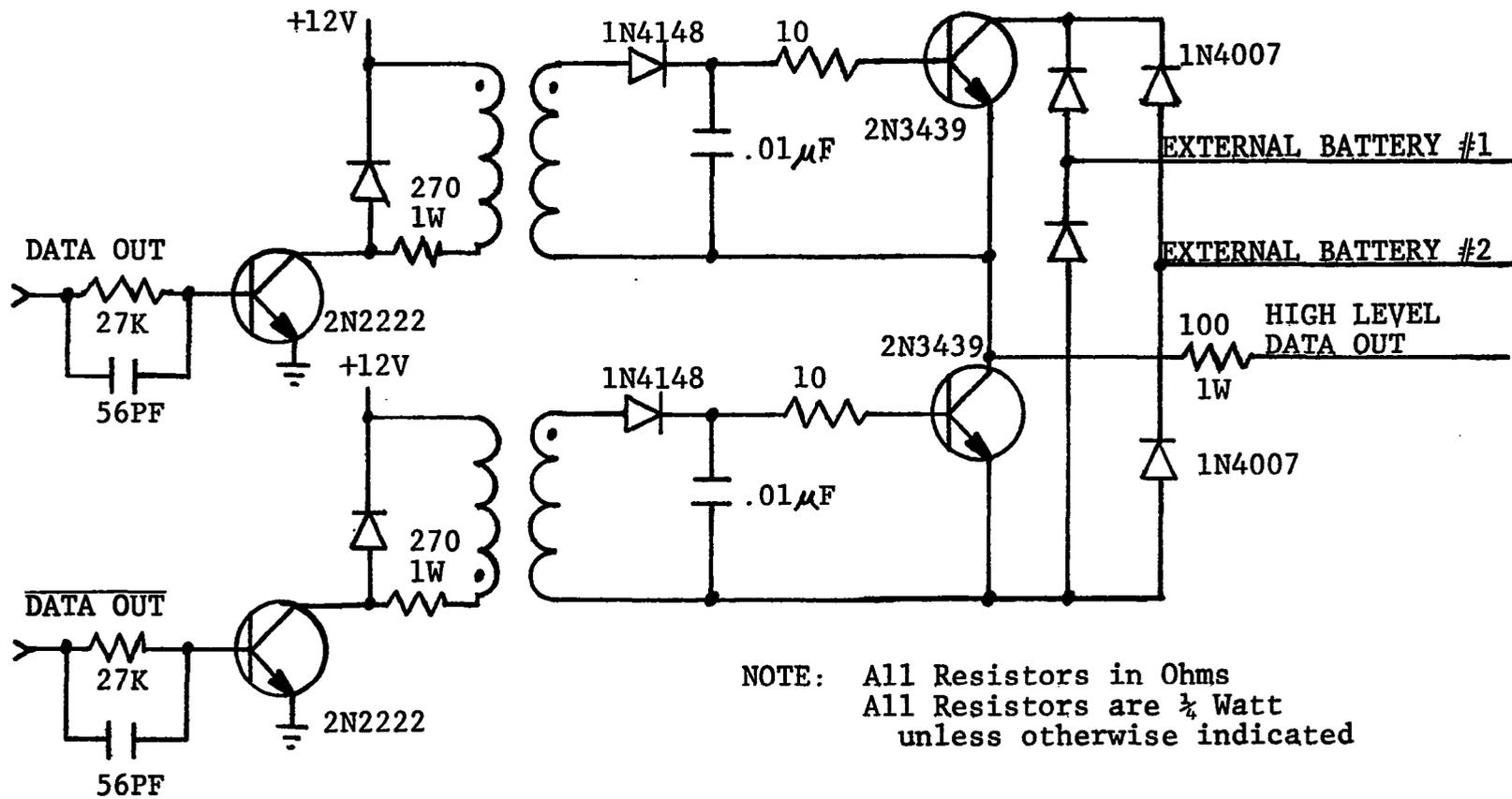


Figure 17. Transformer Coupled High Level Data Output

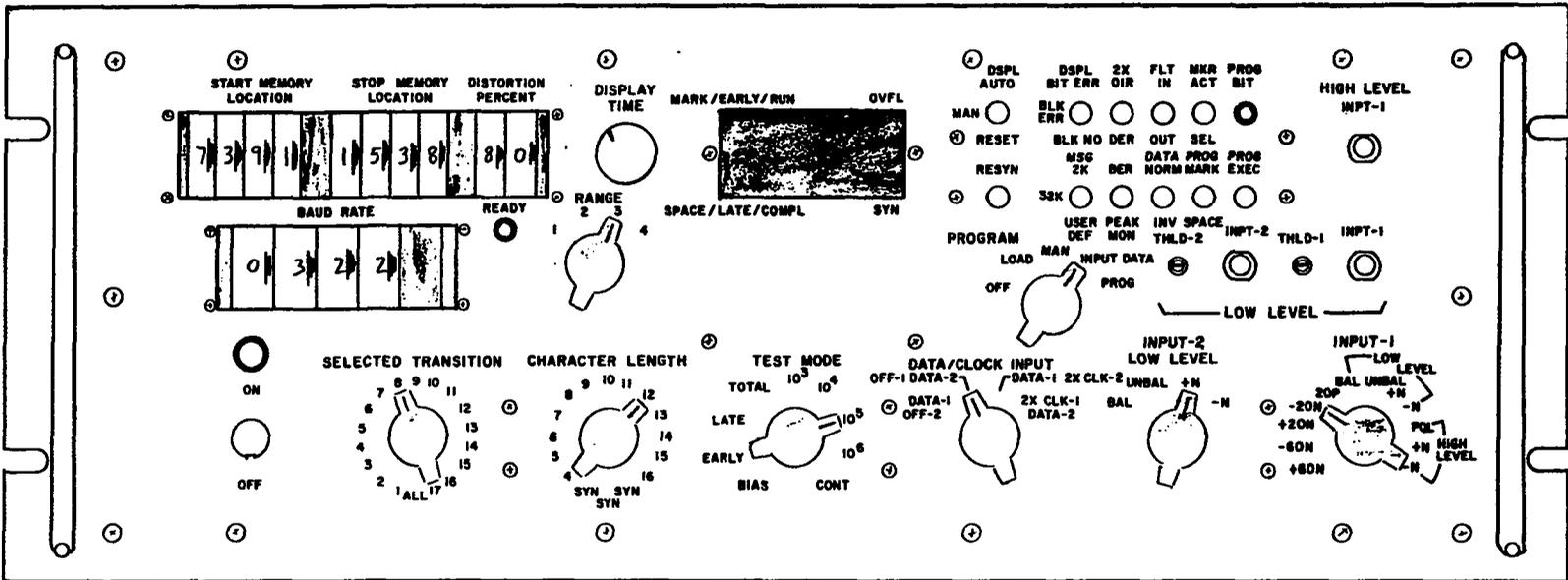
There are two inputs into the DMG on the front panel. They are the 2X IN (UNBAL) and the EXT PLS IN (UNBAL). These are both RS-423 type inputs. The receiver used for these is the MC3486 (Quad RS-422/423 Line Receiver). The 2X clock has another type of input, the EIA Standard RS-232-C type, on the back panel connector. The 2X IN and the CLR TO SEND are received by MC1489 (Quad RS-232-C Line Receivers).

### III. DIGITAL SIGNAL ANALYZER

#### Physical Description

The Digital Signal Analyzer (DSA) is different from the DMG. The DMG is used solely to generate a data signal. The DSA's function is to analyze the input signal and report any errors. Errors are indicated either when the input signal exceeds the setting on the front panel, or when the data polarity is wrong. The DSA also has a second function to perform, that of a PROM programmer.

Figure 18 shows the DSA front panel. Some of the switches perform the same functions as in the DMG. The BAUD RATE switches and the RANGE switch are the same in both the DSA and the DMG. The DSA START/STOP switches have some circuits similar to the DMG START/STOP switches. However, in the DSA there are more functions to be performed by the START/STOP switches, and they have no message select encoding (as in the DMG). The DISTORTION PERCENTAGE switches perform a different function than in the DMG. In the DMG the DISTORTION PERCENTAGE switches acted as the trigger to release the bit, while in the DSA any bit change occurring outside the limits of the distortion switches must be declared an error.



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Figure 18. Front Panel of the DSA

The CHARACTER LENGTH switch is another that is the same as in the DMG. However, the SELECTED TRANSITION is unique to the DSA. The SELECTED TRANSITION switch is used to generate a strobe for an oscilloscope trigger. The SELECTED TRANSITION switch has 18 positions, 17 for each possible transition of a 16 bit data stream and an "All" position. When a position from 1 to 17 is selected, on that specific transition a strobe is generated to the Z axis output. Figure 19 shows how each selection would cause a strobe. The "All" position will generate a strobe with each transition. It should be noted that the only way 17 transitions could be generated is for a sixteen bit data stream to alternate ones and zeros in asynchronous mode.

The rest of the switches and displays are different from the DMG. The DSA has a display of three digits. The digits are seven-segment LEDs and around the display are other individual LEDs to represent the following functions. On the top of the display is MARK which represents a bit whose level is a one. The next, EARLY, is the mark bias indicator for the distortion (Figure 1). The third is RUN which indicates that a test is in progress. The final LED on the top is OVFL which is the overflow indicator for the display. This represents a number larger than 999 which is the largest number that can be shown on the display. The bottom of the display has the following indicators. SPACE indicates a zero level bit in the data

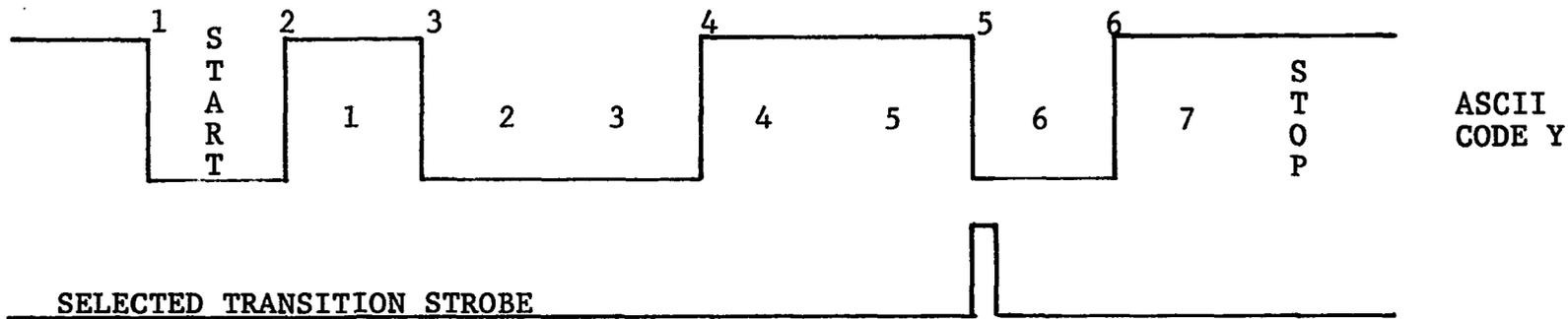
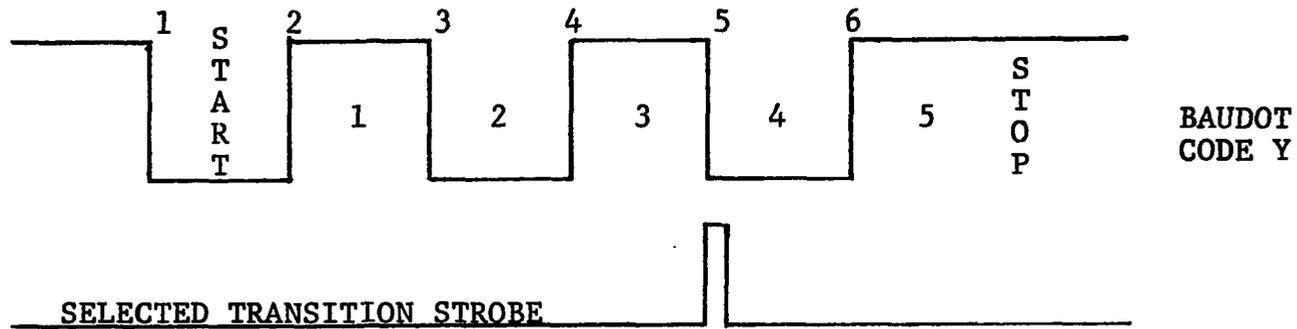


Figure 19. Selected Transition Strobe when Selected Transition Switch Set to 5

stream. LATE indicates space bias for distortion measurements (Figure 1). COMPL indicates that a test has been completed and no more data sampling will occur. The last one on the bottom is SYN which illuminates when the test mode selected is synchronous. The SYN LED will be off when using the start/stop mode (asynchronous mode).

The display has two control switches. The DISPLAY TIME is an adjustable switch which causes the time on the display reset signal to vary from two seconds to twenty seconds. The other switch controls the mode of the display. The DSPL AUTO is used with the DISPLAY TIME switch which allows the automatic resetting and loading of the display based on the adjustment of the switches. MAN is the center position and requires manual operation of the switch to reset the display. The manual reset is spring loaded and the switch returns to the center position when released.

The RESYN switch is used to restart the synchronizing logic, allowing the data pattern to be synchronized with the pattern generator data or the memory data. This switch is used when starting test or when preparing to start a new series of tests. During the resyn cycle the distortion is not measured until the READY light glows. The group of ten switches next to the MAN and RESYN switches are controls for the display and data stream. The last two are part of the PROM programmer, and they will be described with the PROM programmer.

The first switch is used with the display control for displaying bit and block errors or the block numbers. When the switch is up, the display is recording the bit error count. When the switch is in the center position, the display is recording the block error count. When the switch is placed in the down position, the block number is displayed.

The switch below this is the MESSAGE SELECT switch for the DSA. The up position is the 2k pseudo-random pattern that is stored in the EPROM. The center position is the 32k pseudo-random pattern generator that is in the logic. The down position is the user defined area of the EPROM. In this position the start/stop switches are used to address the EPROM. The DMG has "Msg A" and "Msg B" which can be used for testing errors and distortion by selecting the appropriate start and stop address on the start and stop switches of the DSA.

The next switch is for selecting the 2X clock for the DSA. The switch in the up position is for 2X "Dir" (2X clock direct from input). In the down position, the switch selects the 2X "Der" (2X clock derived from internal logic). The switch below the 2X is used for display selection. When the switch is in the "Ber"--bit error, block error, or block number position--the DSPL switch described earlier controls which one is displayed. The switch in the "Peak Mon" position causes the peak distortion to be displayed if the TEST MODE switch is in one of the following positions--"Early,

Late, Total". If the TEST MODE switch is in "Bias", the average distortion is displayed.

The next two switches are controls for the input data stream. The FLT IN or OUT is the 2 kHz low-pass filter used for Baud rates of 30 to 200. For Baud rates over 200, the filter is automatically switched out. The DATA "Norm" or "Inv" is the data input. The data is normal while the switch is up and inverted when the switch is down. This circuit, shown in Figure 20, is a switch which selects the data line through an exclusive OR. The circuit is used to obtain inversion through one gate as shown in Figure 21 (Truth Table for Two-Input, Exclusive OR Gate). When a low is applied to input A, the output follows input B. When input A is high, the output is the inversion of input B.

The PROG "Mark" or "Space" is used with the programmer in the manual operation mode. This switch is used to select whether a mark or a space is to be programmed at the bit address that is selected by the start switches. The PROG BIT is an LED that displays the bit selected by the start switches address. The LED is illuminated for a mark and off for a space. The push button switch PROG EXEC is the switch that causes execution of the program function selected by the PROGRAM switch.

The PROGRAM switch selects the different modes in which the programmer can be used. The positions are "Off, Load, Man, Input Data, and Prog". There are three more

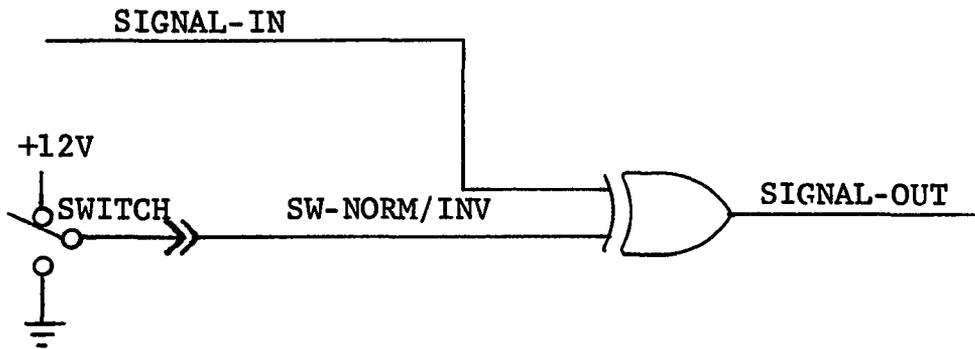


Figure 20. Normal or Inverted Controls



IN		OUT
A	B	C
L	L	L
L	H	H
H	L	H
H	H	L

Figure 21. Truth Table for Two Input Exclusive OR Gate

modes designed into the logic that currently do not show on the front panel. These modes are "Verify, Insert, and Delete". These three modes are controlled by the micro-processor. These will be discussed in the section on the PROM programmer.

The back panel switches and connectors, as shown in Figure 22, have the following functions. The switch 2X IN "Norm" or "Inv" is the 2X clock input to the DSA and can be normal or inverted. The logic is the same type as shown in Figures 20 and 21. The 2X OUT "Norm" or "Inv" is the 2X clock output and is the same style of circuit as shown in Figures 20 and 21. The 2X clock, when in the asynchronous mode, starts with the start bit and stops with the selected stop bit. The 2X clock is used in such a manner that the rising edge of the 2X clock is the ideal transition point while the falling edge is the ideal mid-bit point. (Ideal means that there is zero distortion.)

The 2X OUT "Stop 1" or "Stop 2" is used for the selection of the number of stop bits that is used in the asynchronous mode and also the point where the 2X clock output will remain low while no transmission is occurring. The requirement for the 2X clock output in asynchronous mode is to be on a character-to-character basis.

The next switch is the control for selecting the 1 MHz clock internal ("Int1") or external ("Ext"). The two jacks in the center are either the 1 MHz IN (the input for the

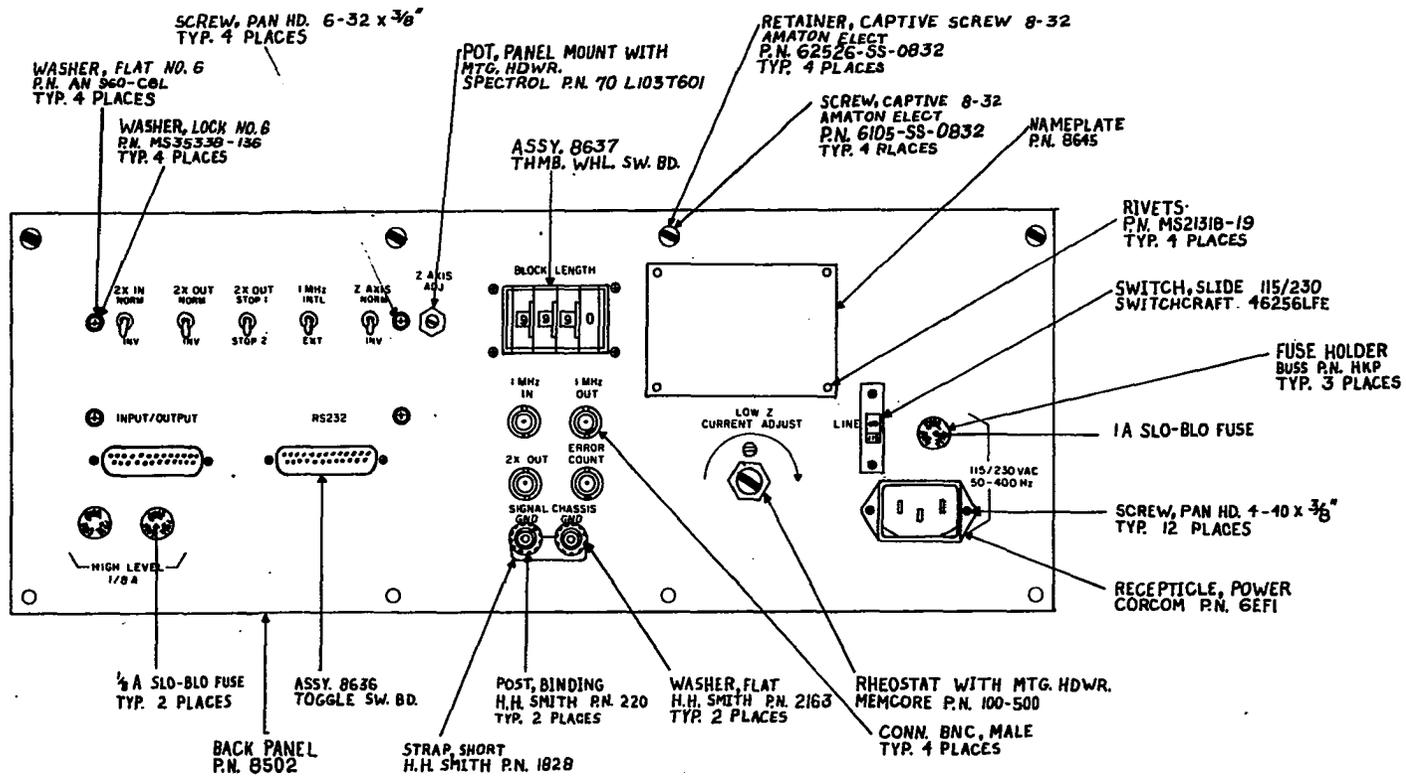


Figure 22. Back Panel of the DSA

external 1 MHz clock) or the 1 MHz OUT (the output for the 1 MHz clock either internal or external).

The next switch is used for the Z AXIS "Norm" or "Inv" which is used as intensity modulation for an oscilloscope. This circuit has the same inverter and switch as shown in Figures 20 and 21. The control next to the switch is a potentiometer to adjust the Z axis pulse magnitude from 1 volt D.C. to a maximum of 20 volts D.C. The pulse is the selected transition pulse. There is also an internal potentiometer which can adjust the pulse width from 1.0 microseconds to 10.0 microseconds. The pulse is generated using a 555 timer circuit with the potentiometer determining the pulse width.

The two connectors are back panel connections for the jacks on the front panel. These signals are wired from the front panel ports directly to the connectors. The LOW Z CURRENT ADJUST is a series rheostat that can be adjusted from 75 ohms to 5000 ohms and is fused by a 1/8 ampere slow fuse.

The BLOCK LENGTH switch is used for selecting a data block length from 10 to 9,990 bits. The rest of the switches and indicators are for the A.C. line inputs. The A.C. inputs are the same as described for the DMG.

The interface has high level and low level inputs which match the outputs of the DMG. In this case the coupling is accomplished for the input in order that the data

signals, once through the interface circuits, are at compatible CMOS levels. These input signals now activate the DSA logic which determines and displays any error conditions. A secondary function for the inputs provides input data for the PROM programmer which will be described later.

### Logic Description

The BAUD RATE switches and phase-locked loop clock are the same as in the DMG. The START/STOP switches are different only to the extent that message A and B addresses are not decoded. There was no specification requirement for distortion or error measurement of the messages. However, this can be accomplished by setting the MSG switch to "User Defined" and placing on the START/STOP switches the starting and ending address of the message which the tester wishes to analyze. There is a qualification in the specification that should this mode of testing be performed there exists the possibility that the signal may not sync correctly and the error indication could be erroneous. This test will not be held to the specification requirement for sync and errors. Our testing of data shows that the specifications are met by the DSA in this mode of testing.

The start/stop address buffer is very similar to the DMG (see Figure 23) except it has an additional function that is used with the PROM programmer. In addition to the decimal-to-binary conversion and the binary-to-hexadecimal conversion, the start/stop address buffer must allow

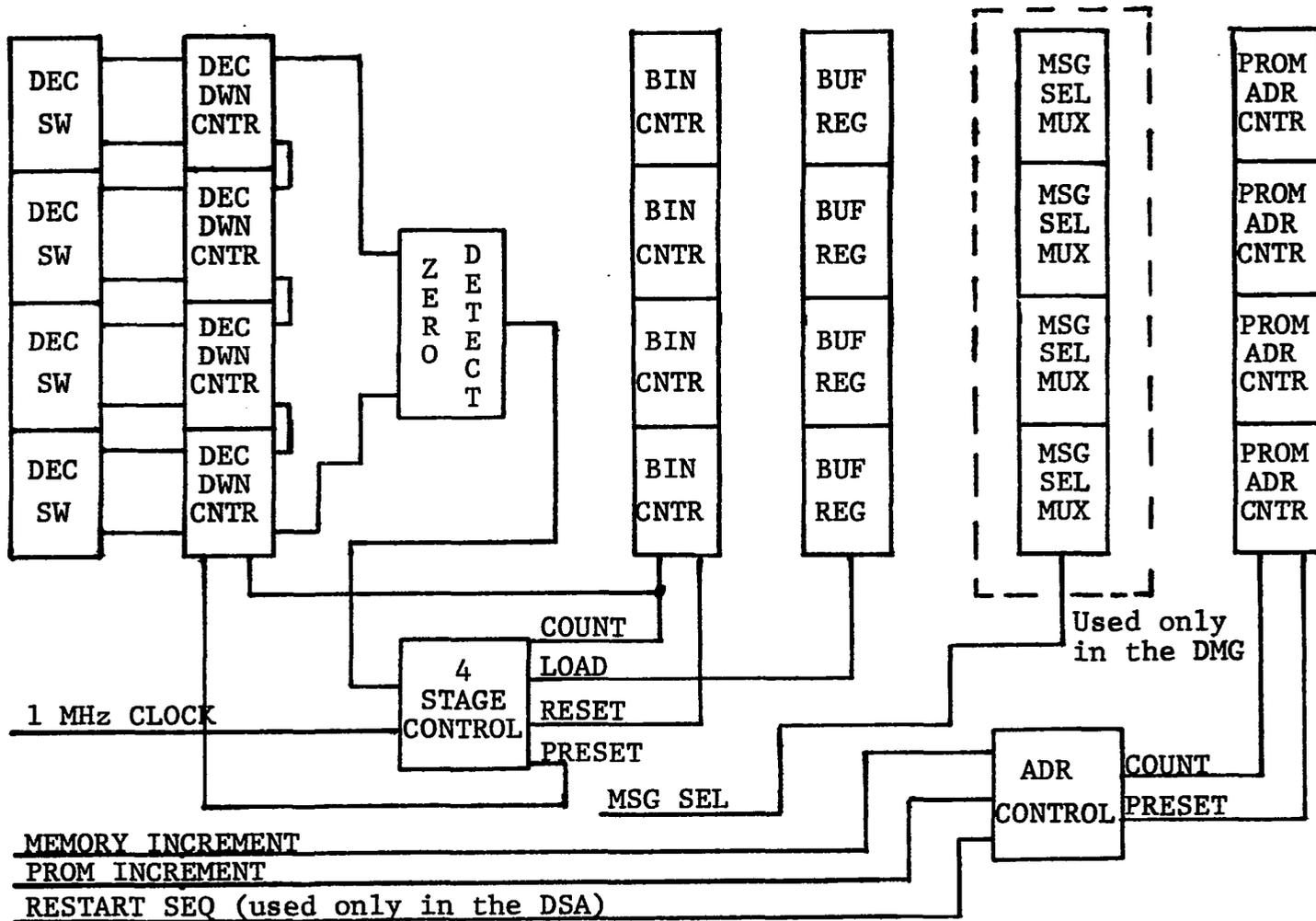


Figure 23. Start/Stop Switch Controls

incrementing of the address during the PROM programmer operations. The rest of the DSA is unique and has no similarity to the DMG.

The distortion monitor, Bit/Block error, and Peak/-Average logic all work together analyzing the input data. The distortion monitor has a different function in the DSA than in the DMG. In the DSA the distortion monitor value creates a window such that any value of distortion in the input data that is equal to or less than the value selected is considered good data. Any data that exceeds this value is considered an error. These errors are accumulated for display as either a bit error or a block error.

The circuit for distortion is a counter which pre-sets either to 50 or 5 (based on the baud rate) on the falling edge of the 2X clock and counts down to zero. The clock is either the 200X clock (50) or the 20X clock (5). On the rising edge of the 2X clock the counters are preset to zero and count up to either 50 or 5. A comparator reports when the count exceeds the distortion monitor switch setting, and if a transition is detected during this period, an error is recorded.

The errors are recorded in the following manner. The distortion error or a data level error can cause an increment of the error counter but the error counter cannot be incremented for both on the same bit. In a data level error the level (mark or space) does not compare to the level in

memory with which it is being compared. The number of bits on which the distortion is tested are selected on the front panel by the TEST MODE switch. The TEST MODE switch can be set to " $10^3$ ,  $10^4$ ,  $10^5$ ,  $10^6$ " or "Cont" (continuous running).

The distortion errors are then displayed either by bit errors or block errors. If the distortion errors are being reported as bit errors, the counters run for each bit transmitted to the DSA. If the distortion errors are being reported as block errors, the error counters are only incremented once for each block. The length of the blocks are determined by the BLOCK LENGTH switches on the back panel. These switches determine the number of bits that are to be in a block.

The test is performed with the TEST MODE switch which defines the number of bits to be measured for distortion. A set of counters count the bits until they compare to the BLOCK LENGTH switch and a block length strobe is issued. The block counters continue to increment until the number of bits received compares with the TEST MODE switch value. The block length is in bit multiples of ten, from 10 to 9,990 bits. When the TEST MODE switch is set for continuous running, the less than input of the comparator for the most significant decade is activated. Thus, the comparator can never get an active level on the equal output. When the comparator gets an active level on the equal output for any setting other than "Cont", the test stops.

In Figure 24 the counters keep track of the bits, bit errors, block numbers, and block errors. The bits are counted from 0 to  $10^6$  and the counters can roll over for continuous running. The bit error counter is incremented whenever an error occurs for the specific bit being tested. There is also another set of counters which keeps track of the block error count. The block error count increment is a flip-flop which holds only one error per block length pulse. When the block length pulse is issued, the block error count is incremented. Both the bit error count and the block error count can be selected for display by the tester. The block number counters value can be displayed by the tester. The display can only handle a number up to 999. If a number larger than 999 is to be displayed, the overflow LED is turned on.

The other test data that the tester can display involve the peak and average circuits. The peak is a display of the largest distortion in a stream of data bits. The TEST MODE switch selection of "Early, Late, or Total" is used with "Peak Mon" to display the largest distortion detected in a selected data stream. Early peak measures only the peak distortion that occurs before the ideal transition point. The late peak distortion measures the peak distortion after the ideal transition point. The total peak is a measurement of both early and late distortion. The peak value is stored for display until the test is restarted or a larger distortion

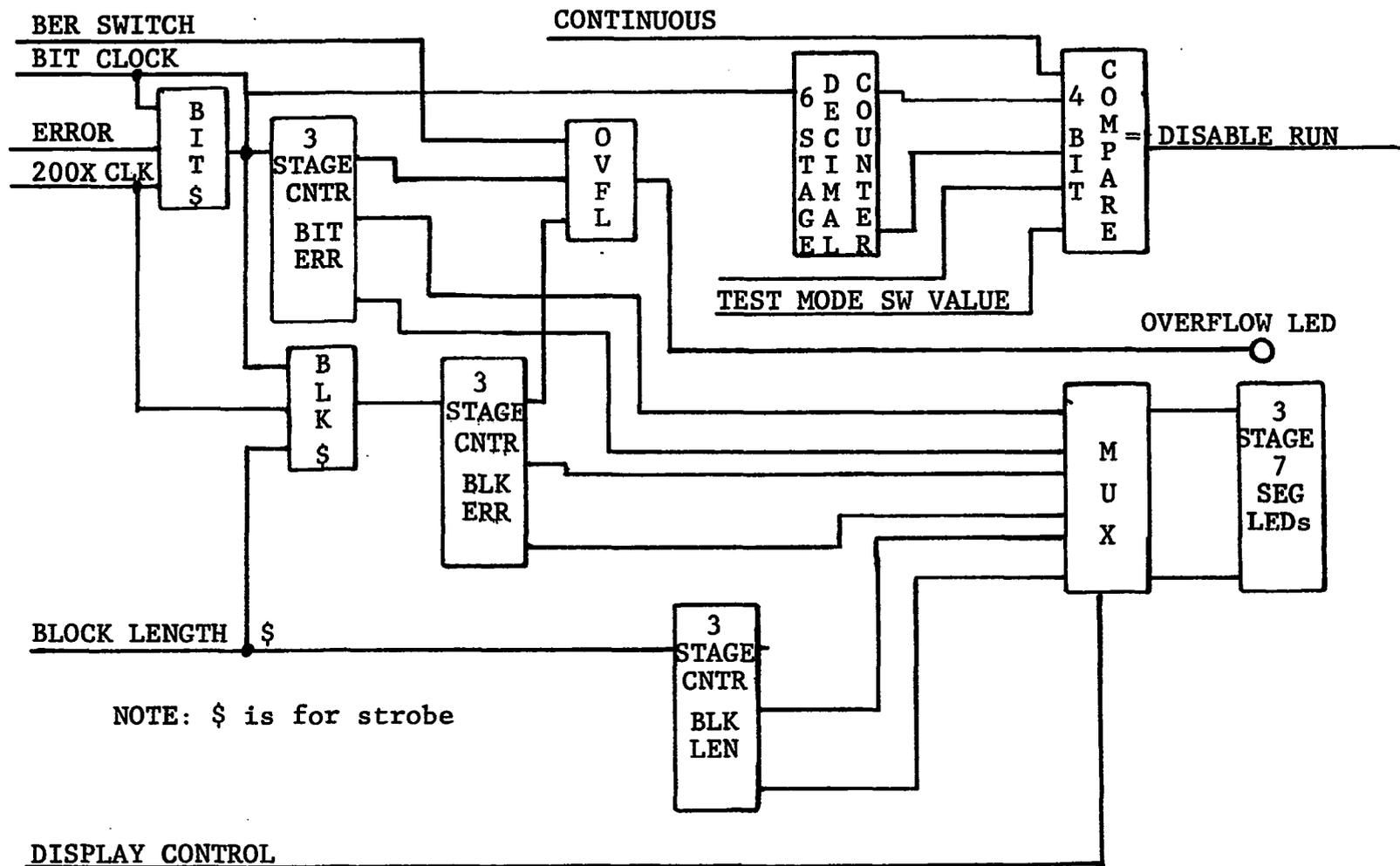


Figure 24. Bit, Bit Error, Block, Block Error Counters

value is measured.

The average distortion is a circuit of counters which accumulate the average distortion for the selected transition. This circuit requires the TEST MODE switch to be set on "Bias" and the SELECTED TRANSITION switch to be set on one of the eighteen positions. For the 1-17 positions the circuit averages the distortion of the selected transition for 100 characters. For the "All" position the circuit averages the distortion of all of the bits in each character until 100 bits have been measured.

The average circuit, Figure 25, consists of three sets of counters. The first two decade counters will divide the gated 200X clock by 100. The gated 200X clock is allowed to run from the start of the bit time until the transition occurs. Four examples of this timing are shown in Figures 26, 27, 28 and 29. The transition counter counts transitions to 100. The average counter stages are preset to 50 for each measurement cycle. The counter is down counted and will reach zero when 50 (0% distortion) selected transitions have occurred. The average counters will receive one count pulse for each one half bit of time that a transition has not occurred. Using Figure 26, which shows the timing for 25% early distortion, we can show how the average circuits function. Each time a transition window occurs, the circuit is to average the distortion. The divide-by-100 clock will run during the period from the rising edge of the 2X clock

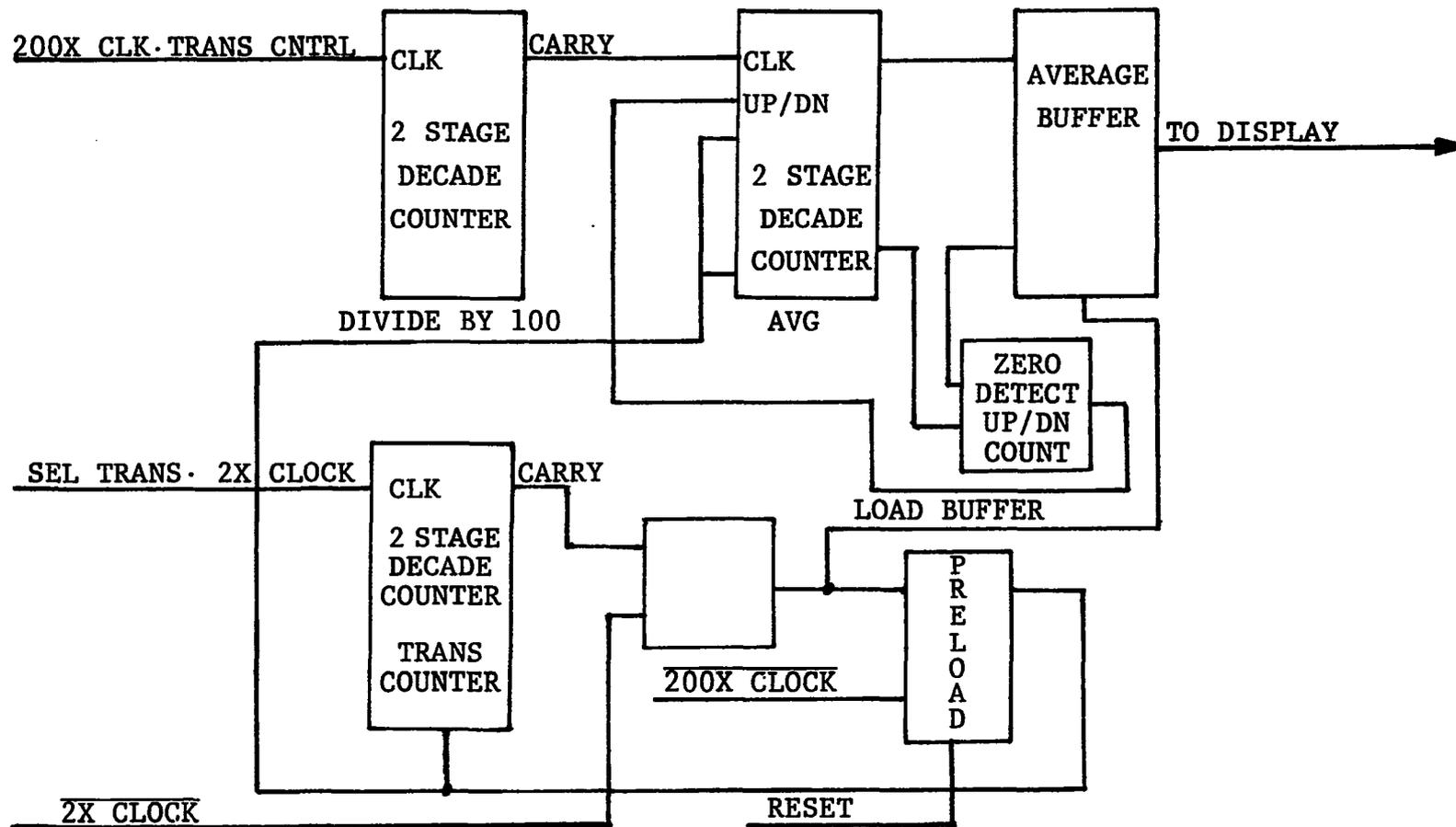


Figure 25. Block Diagram Average Distortion Circuit

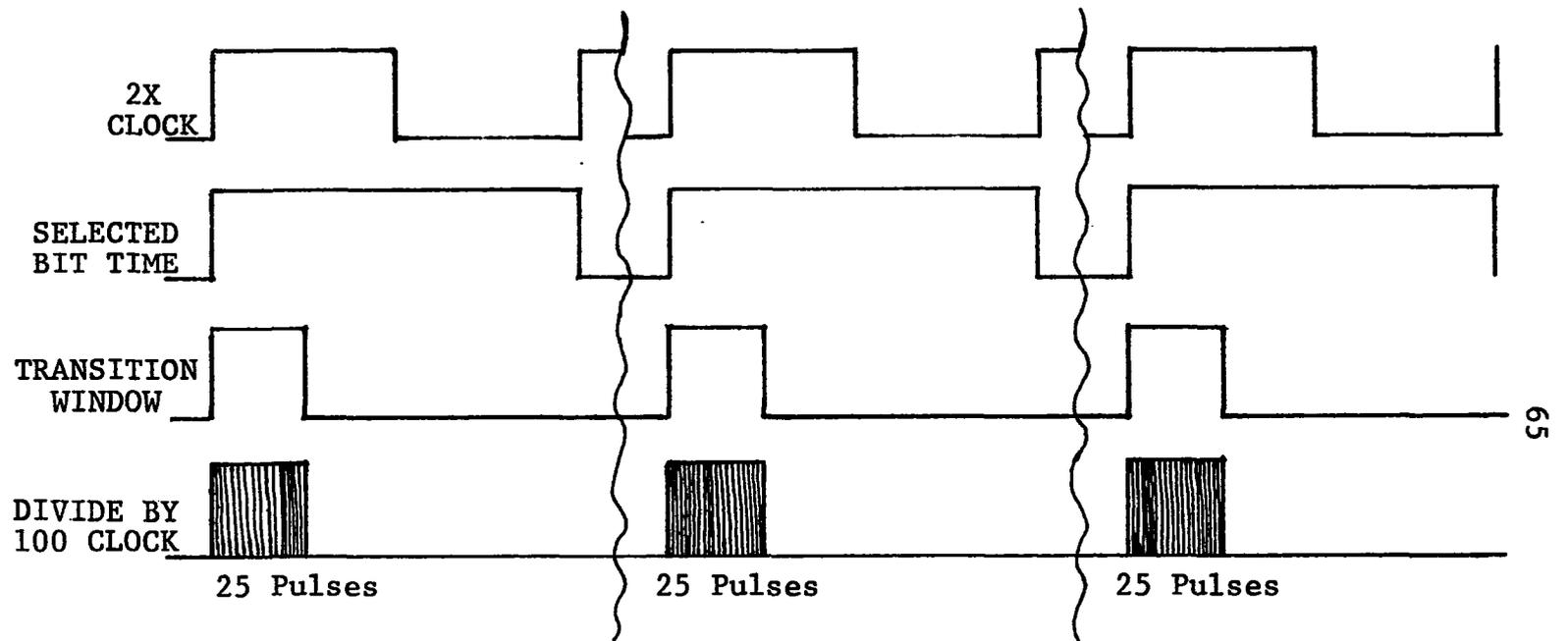
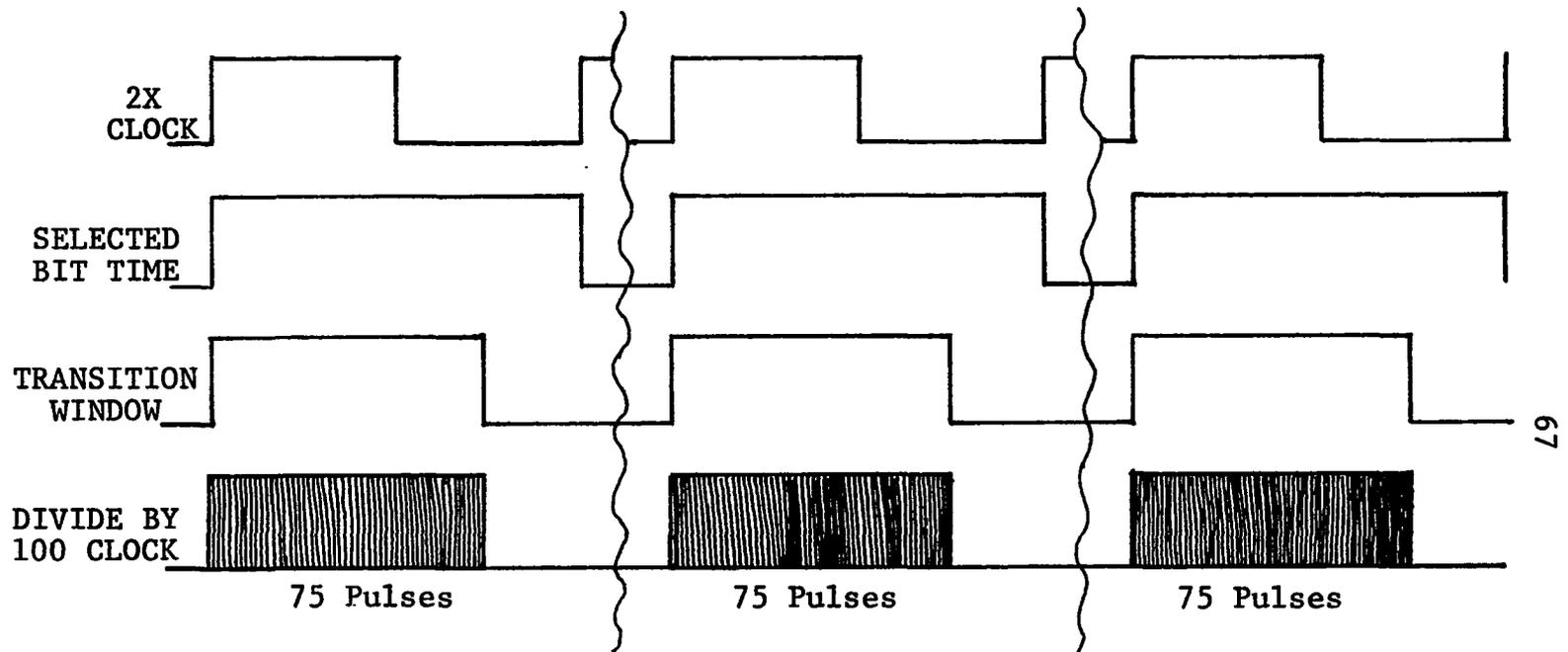


Figure 26. 25% Early Distortion

until the transition occurs. The divide-by-100 clock needs four transition windows to decrement the average counter by one. Thus, when the measurement period has ended, the average counter would be decremented to 25. This value would then be transferred to a buffer.

Using Figure 27 as an example of late transition distortion averaging, we would have the following sequences. For each transition window the average counters have received 75 clocks. This means that after 100 selected transitions the average counters will have received 75 clocks. The average counters upon reaching zero have the up-down control changed from decrementing to incrementing. Thus, upon completion of the measurement period, the average counters will have a value of 25.

Figure 28 is the timing for ideal distortion (0%), and we can see that this will result in 50 decrements of the average counters, leaving a value of zero. Figure 29 shows the timing for the last type of distortion--switched. The switched distortion will have early distortion on the first character, late distortion on the second character, and repeat this pattern for each additional pair of characters. The average counters would receive one decrement for every two transitions; thus, switched distortion will be averaged to the ideal distortion value of zero. Table III compares other distortion percentages and types of distortion to the value of the average counters. This table was used to verify



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Figure 27. 25% Late Distortion

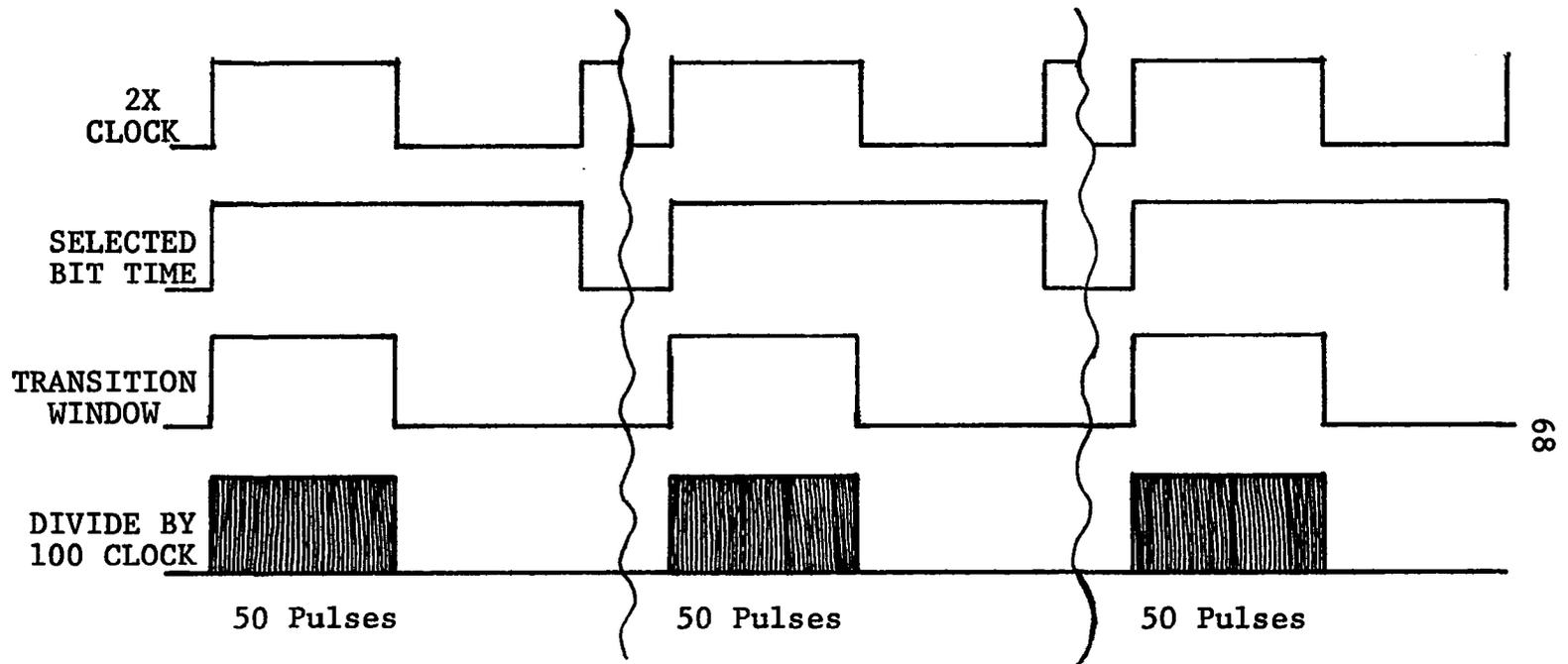


Figure 28. 0% Distortion

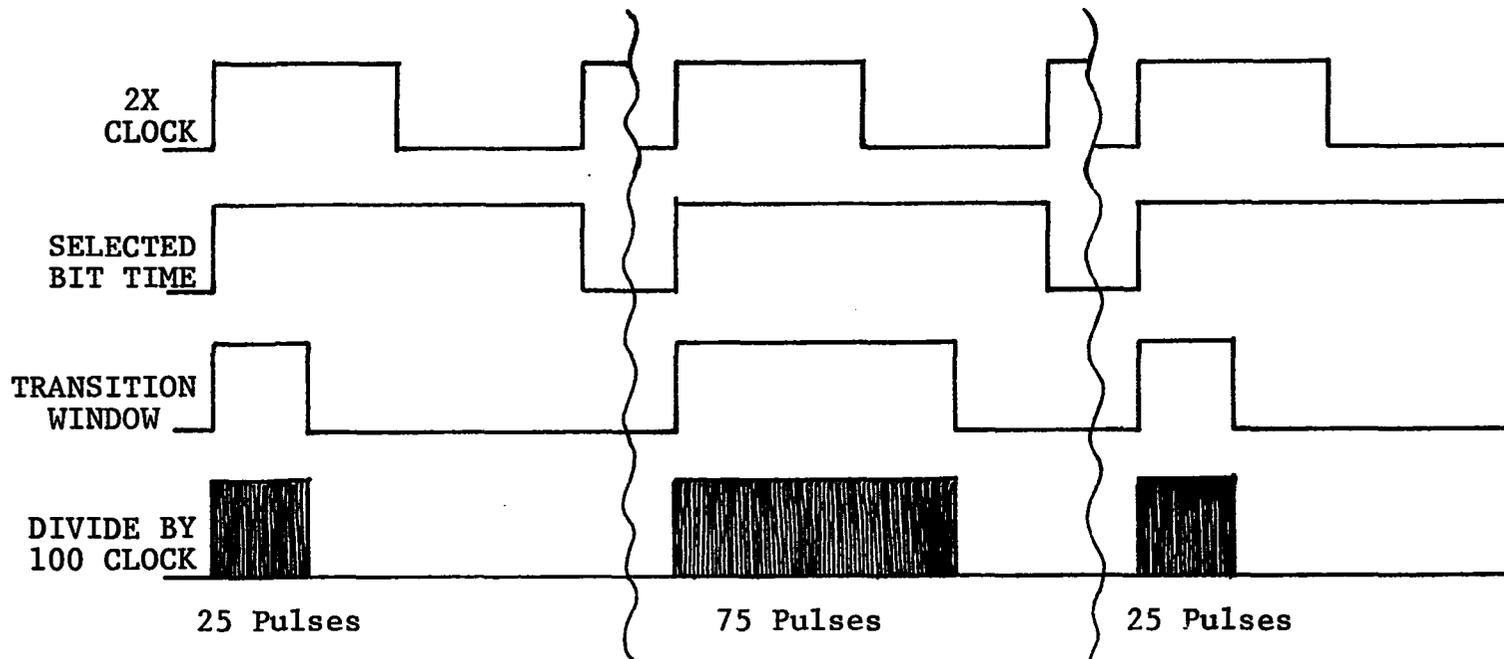


Figure 29. 25% Switched Distortion

TABLE III. AVG DISTORTION FOR VARIOUS TYPES & PERCENTAGES OF DISTORTION

DISTORTION TYPE	PERCENTAGE DISTORTION	PULSES PER TRANSITION WINDOW	AVG CNTR PULSES PER PERIOD	UP/DOWN CONTROL VALUE	AVERAGE COUNTERS VALUE
EARLY	49	1	1	Down	49
EARLY	32	18	18	Down	32
EARLY	17	33	33	Down	17
LATE	17	67	67	Up	17
LATE	32	82	82	Up	32
LATE	49	99	99	Up	49
SWITCHED	49	1 or 99	50	Up	0
SWITCHED	32	18 or 82	50	Up	0
SWITCHED	17	33 or 67	50	Up	0
SWITCHED	5	45 or 55	50	Up	0

that the average circuits would perform the intended functions. The tester displays the average distortion by placing the display switch in "Peak Mon".

The memory portion of the DSA is different than that in the DMG. While the START/STOP switches are the same, and the start/stop address buffer is similar, an additional control is needed for the DSA. This control is the memory sync and control. These signals are shown in Figure 23, used previously, when discussing the START/STOP switches. The logic in these circuits must control the selection of the PROM address and synchronize the data from the PROM to the input data. The 32k pseudo-random pattern generator (same as in the DMG) is used also in the memory sync circuitry. The 32k pseudo-random pattern (PRP) generator uses the first 16 bits of a data stream to sync. Additional controls were added to allow the input data stream to continue shifting through the 32k PRP shift registers. The 32k PRP shift register is also used when synchronizing the data stream to the PROM. A parallel 16 bit shift register carries the PROM data and the comparator compares the 32k PRP shift registers with that of the PROM shift registers for sync. The control logic for memory sync needs 16 characters to compare before it will indicate that the data is now in sync.

The clock for the shift registers is different until the sync has been declared. The 32k PRP shift register uses the 2X clock which the data follows. The memory sync

shift registers have two different rates. For all baud rates below 10k baud, the 1 MHz clock is used. At these baud rates the PROM data is chasing the input data, looking for a compare. Once a compare is found, the clock is switched to the 2X clock unless a non-compare is found before sync occurs. If a non-compare is found before sync, the clock is switched back to the 1 MHz and the PROM data is shifted through the shift register looking for the next compare. Once the two data patterns compare and sync are declared, the logic is locked to the 2X clock.

For baud rates of 10k baud and above the first two bytes of PROM data is loaded into the memory sync shift registers and no clock is used until a compare is found. In this case the PROM data waits for the input data to compare. When a compare is found, the 2X clock is used until a non-compare is found before sync. The PROM data waits for another sync. When sync is declared the 2X clock is again locked to the memory sync shift register.

Once the sync is declared, the sync LED is illuminated and the measurement of distortion or bit error is started. The test will continue until one of the following events occur. Either the test reaches completion based on the TEST MODE switch, or the test technician pushes the RESYN button on the DSA front panel. It should be noted that there is no start or stop switch on the DSA. The RESYN switch acts as the start switch. The RESYN switch action causes all

counters and registers to be cleared and the sync process starts over as described above until the DSA input data has been synchronized again.

Figure 30 is the block diagram of the DSA. This figure shows how each of the circuits discussed above are linked together. The interface was described in the last section of the chapter on the DMG and the first section of this chapter. The baud rate switches and phase-locked loop clock circuits are exactly the same as the ones used in the DMG. The START/STOP switches are the same as the DMG but the start stop address buffer has an additional control signal as described above. The peak and average circuitry was covered above in much detail. The bit error, block error and block number, along with the distortion monitor and memory sync, have been discussed. The blocks representing the test mode selection and the display were also covered previously. The analyzer controls, except for the PROM programmer, have been discussed. The only remaining blocks in Figure 30 to be covered are the memory and the PROM programmer. They are discussed in the next chapter.

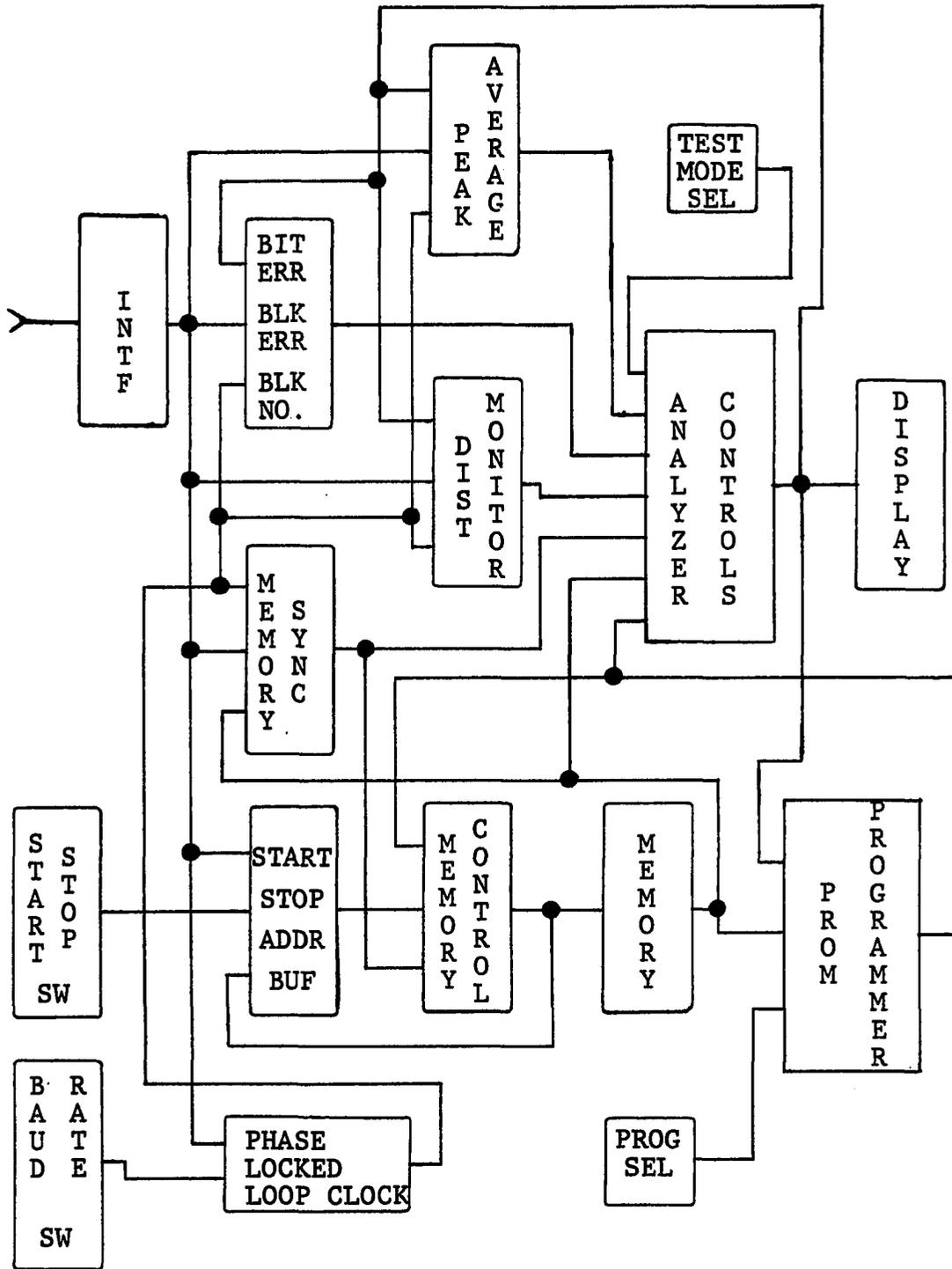


Figure 30. Digital Signal Analyzer Block Diagram

## IV. PROM PROGRAMMER

### Physical Description

The PROM programmer can be separated from the DSA in that its functions are performed in a non-test mode of the DSA. The memory is used for both the test mode and the program mode of the DSA. The memory and memory control relate more closely to the PROM programmer functions than to the DSA. The portion that relates to the test mode has already been described. The following discussion will relate to the PROM programmer.

The principal function of the PROM programmer is to program the 2708 EPROMs used in the DMG and the DSA. The features can best be described by the setting on the PROGRAM switch. These functions are "Off, Load, Manual, Input Data, Prog", and three positions not yet etched on the front panel. These three are "Insert, Delete, and Verify".

The "Off" position is used to place the DSA in the test mode of operation, and thus disable the PROM programmer. Likewise, the PROGRAM switch in any position other than "Off" disables the test mode of operation.

The "Load" function allows the copying of an existing EPROM into a RAM memory for temporary storage. The RAM

memory can be used to copy another EPROM or the memory can be modified by one of the other functions before programming a new EPROM.

The "Man" position is the manual function used to change the contents of the RAM memory. The bit location in memory is selected on the start address thumbwheel switch and the PROG switch is the data level for the bit (the switch is either in "Mark" or "Space"). To insert this bit into memory requires the operation of the PROG EXEC switch. The PROG BIT LED indicates the level of the select memory bit.

The "Input Data" function is to allow a message to be stored in the RAM memory. The start address and stop address thumbwheel switches define the bits that are to be used. The data stream must be sent to the DSA and the PROG EXEC switch pushed. The PROM programmer will start storing the bits at the start address then increment the address and store the next bit until the data bit is stored in the stop address. The programmer will stop at this point.

The "Prog" function is used to program the EPROM from the RAM memory.

The "Insert" is another edit mode by which a bit can be inserted at the location on the start address thumbwheel switch and all bits from that address to the top of the memory will be moved upward one address. This will cause the very top bit location to be lost.

The "Delete" function is the reverse of the "Insert".

The "Delete" function will delete the bit selected by the start address thumbwheel switch. The bits from the next address above to the top memory address are moved down one memory address. (The top address of memory is programmed as a mark.)

The "Verify" function is used to compare the RAM memory to the EPROM; if they do not compare, an error is indicated.

The logic was designed and the printed wiring boards (PWB) built before the addition of the "Insert, Delete, and Verify" functions. Due to the time involved in layout of the PWB and changes in the completed design, the microprocessor was added to handle these functions. Had these requirements been known before the design was started, the microprocessor would have controlled much more of the DSA system.

I proposed to the management of Ra-Nav Laboratories that the microprocessor could be incorporated in either of two ways in order to add the three new functions ("Insert, Delete, and Verify"). One method was to redesign one PWB incorporating the microprocessor to perform the "Program, Insert, Delete and Verify" functions. The second method would include the entire group of functions of the PROM programmer under microprocessor control. This would mean replacing four PWBs with one and a portion of a second (which possibly could be added to another PWB in the unit).

Ra-Nav chose the first alternative due to the economics and time required to implement this change. Since the load, manual, input data, and prog. logic was complete, the inclusion of the MPU for the additional functions could also handle the prog. function with no affect on the rest of the PWB artwork. The load, manual, and input data are controlled by logic which consists of a counter scheme and gating. I have shown this logic in a flow chart which also shows how the functions could have been added to the MPU if the second method had been incorporated. Figure 31 is a flow chart of how the counters function when the PROGRAM switch is in the "Off" position. By comparing the flow charts for the load function, Figure 32, the manual function, Figure 33, and the input data function, Figure 34, one can see the similarity and why the counter circuit was designed. To further emphasize the similarity, Table IV was prepared. Should any major changes or new system be required, the flow charts indicate that all these functions can be performed by the MPU with only additional firmware, saving two additional printed wiring assemblies.

### Logic Description

Figure 35 is the block diagram of the PROM programmer. The counter circuit described above is in the control block. The address buffer holds the present address of the data being used by the logic. The address buffer outputs, the RAM outputs and inputs, the PROM outputs, and the MPU data

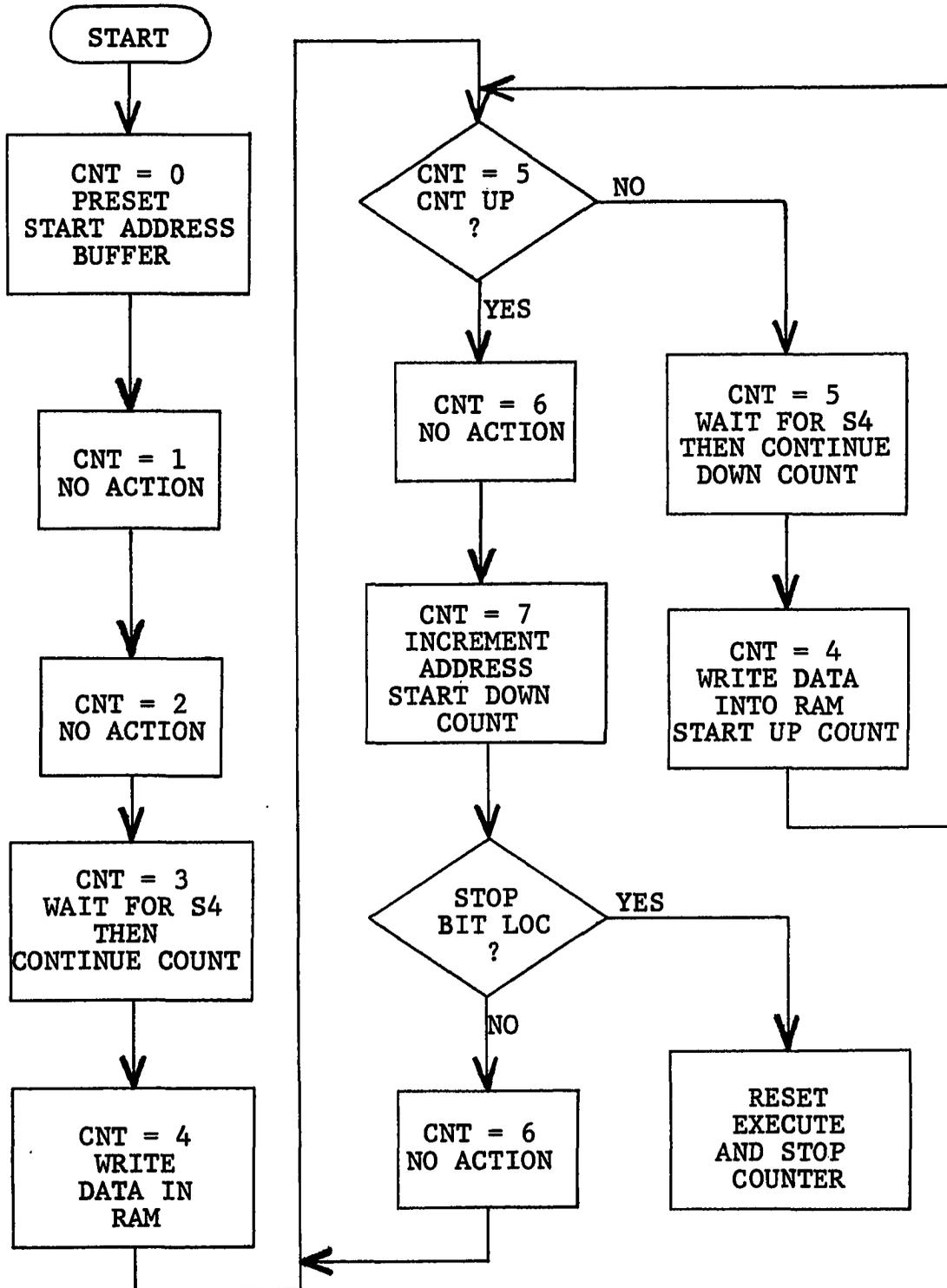


Figure 31. Flowchart of Counter Sequences for OFF

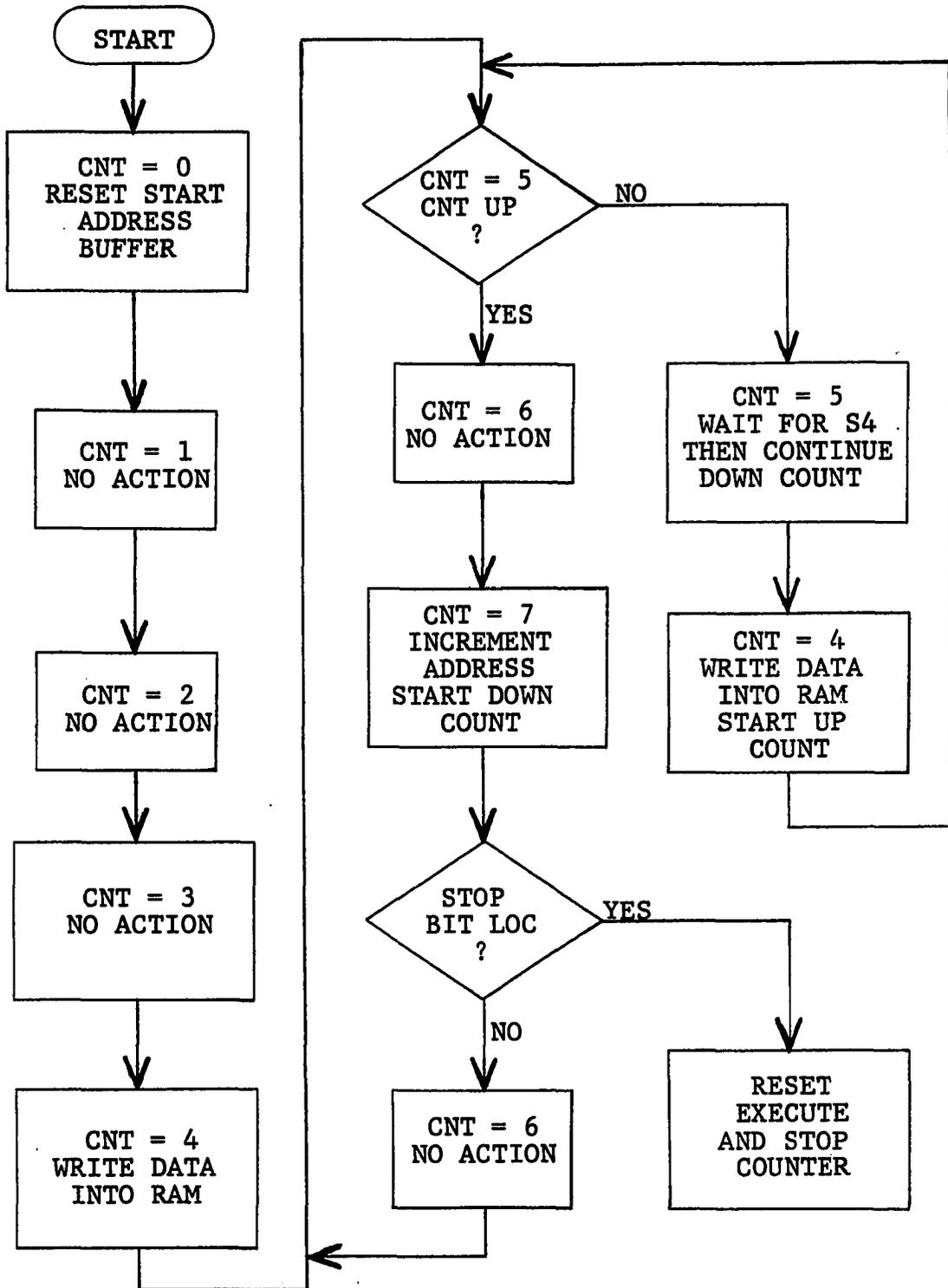


Figure 32. Flowchart of Counter Sequences for LOAD

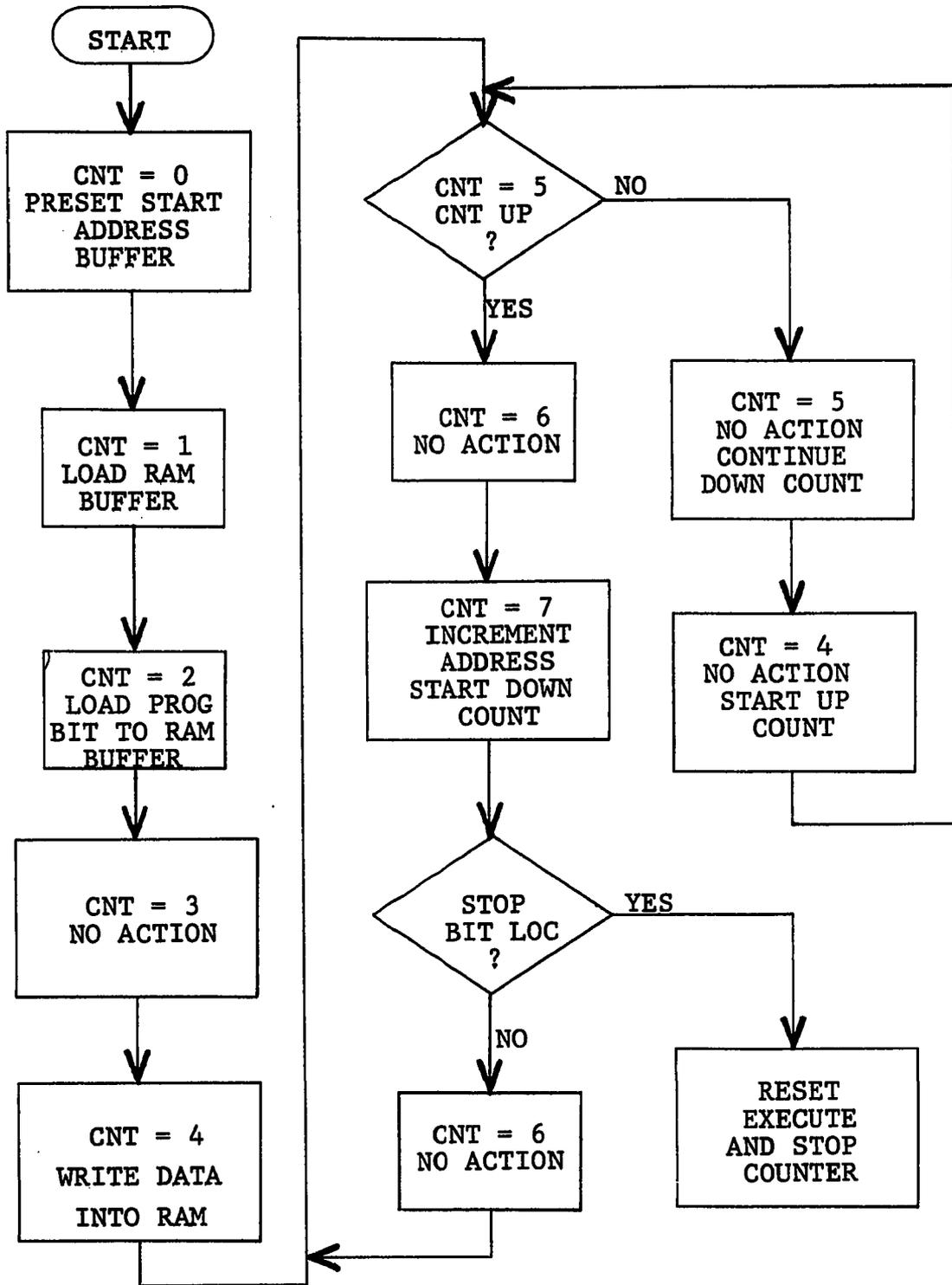


Figure 33. Flowchart of Counter Sequences for MANUAL

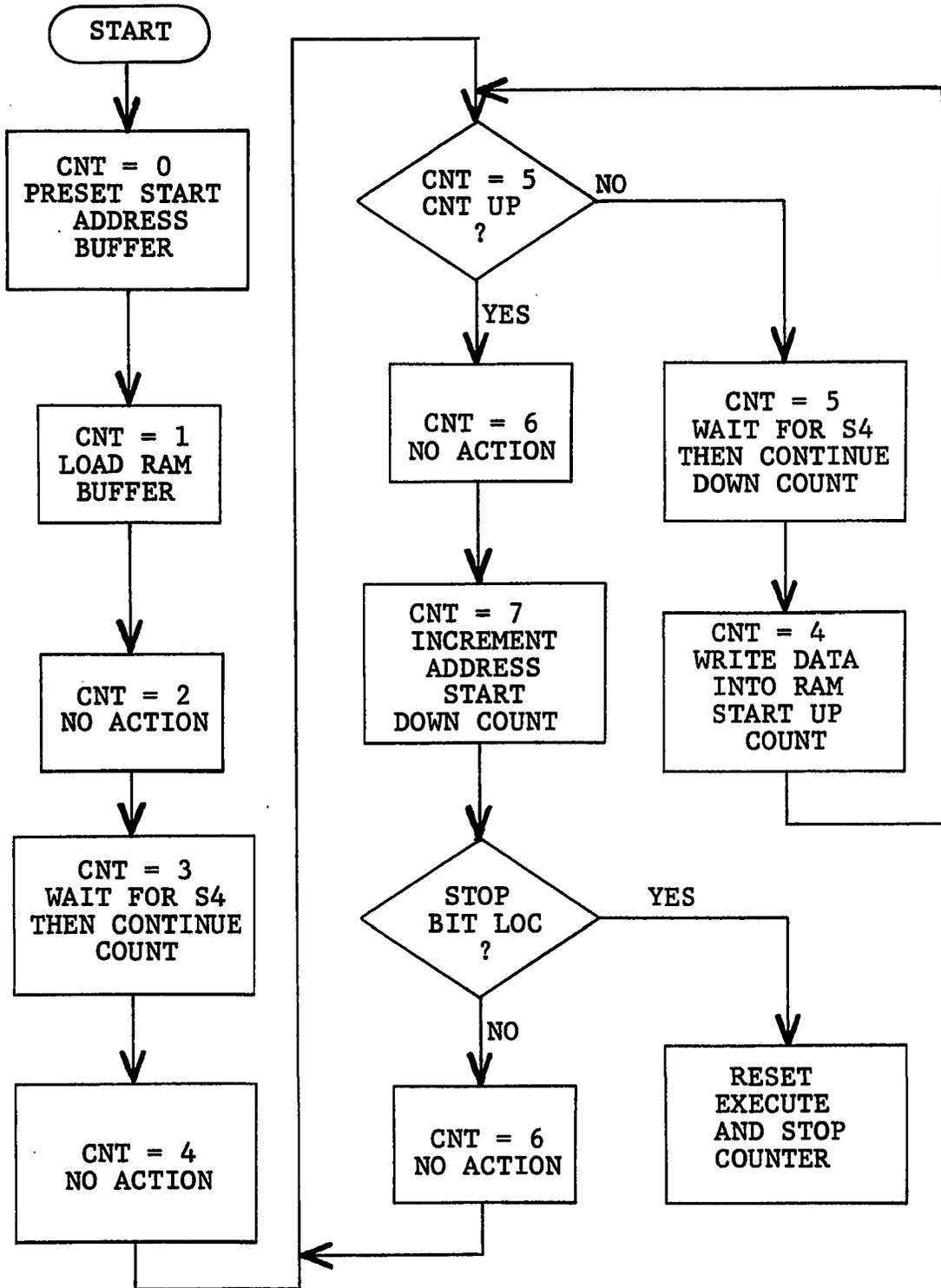


Figure 34. Flowchart of Counter Sequences for INPUT DATA

TABLE IV. STATE DIAGRAM FOR CONTROL COUNTER SEQUENCES

STATE	OFF FUNCTION	LOAD FUNCTION	MANUAL FUNCTION	INPUT DATA FUNCTION
COUNT = 0	Preset Start Address Buffers Continue Count	Reset Start Address Buffers Continue Count	Preset Start Address Buffers Continue Count	Preset Start Address Buffers Continue Count
COUNT = 1	No Action Continue Count	No Action Continue Count	Load RAM Buffer Continue Count	Load RAM Buffer Continue Count
COUNT = 2	No Action Continue Count	No Action Continue Count	Load Program Bit to RAM Buffer	No Action Continue Count
COUNT = 3	Wait for S4 Then Continue Count	No Action Continue Count	No Action Continue Count	Wait for S4 Then Continue Count
COUNT = 4	Write Data into RAM If Down Cnt, Start Up Count	Write Data into RAM If Down Cnt, Start Up Count	Write Data Into RAM Continue Count	Write Data into RAM If Down Cnt, Start Up Count
COUNT = 5	Cnt Up? Yes Cont No Wait for S4 Cont Down Cnt	No Action Continue Count	No Action Continue Count	Cnt Up? Yes Cont No Wait for S4 Cont Down Cnt
COUNT = 6	No Action Continue Count	No Action Continue Count	No Action Continue Count	No Action Continue Count
COUNT = 7	Incr Addr Stop Bit Loc? Yes Cont No Start Dwn Cnt	Incr Addr Addr=8192?Yes Cont No Start Dwn Cnt	No Action Continue Count	Incr Addr Stop Bit Loc? Yes Cont No Start Dwn Cnt
COUNT = 8	Reset Execute And Stop Counter	Reset Execute And Stop Counter	Reset Execute And Stop Counter	Reset Execute And Stop Counter

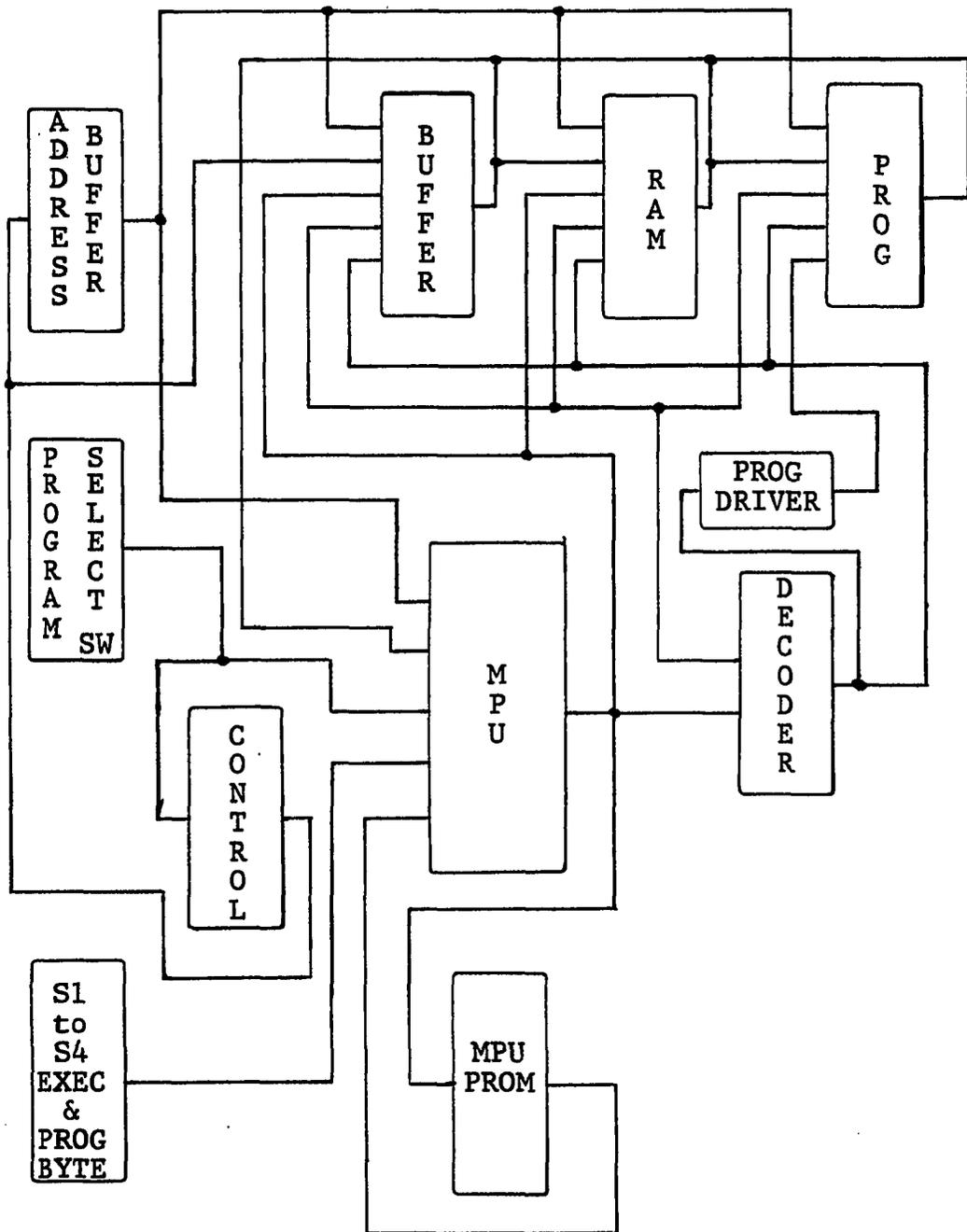


Figure 35. PROM Programmer  
Block Diagram

lines are all bussed together through transceivers. Also connected to the bus is the PROGRAM switch decoded outputs, execute program bit, and control bits S1, S2, S3, and S4. The S1 to S4 control bits are output of the counter which control the bit position of the data in the data byte. Here zero to seven indicates a bit position while S4 (eight) indicates that the present byte has been completed and preparation for the next byte must be made. The RAM buffers are flip-flops with tristate drivers on the output which can be enabled when the data is to be placed on the bus. The RAMs are 2114s which have tristate outputs for the bus. The decode and control logic is used to determine which select lines are to be enabled and where the write line is to be used. The PROM is a 2708 which is enabled via these control circuits. The MPU PROM is a 2708 and holds the firmware. The MPU is a 6802 microprocessor.

The PROGRAM switch functions that are done via firmware are the program, insert, delete, and verify. The actions (such as load RAM buffer, write RAM, preset or reset address, and increment address) are decoded from the MPU address bus. Table V gives all the decodes that are used by the MPU. The program pulse for the 2708 is a flip-flop with set and reset decodes. There are firmware routines for each of the functions: program, insert, delete, and verify. Figure 36 is the flow chart of the main program. Figure 37 to Figure 40 are the flow charts for the program, insert, delete and verify routines, respectively.

TABLE V. MICROPROCESSOR ADDRESS DECODES

<u>Microprocessor Address Lines Hexadecimal Code</u>	<u>Decode Functions</u>
FCXX	Firmware Addresses
E000	Read Address Buffer Bits 8 & 9
D000	Read Address Buffer Bits 0 - 7
C000	Read S1,S2,S3,S4, Prog. Bit & Execute Bit
B000	Read Program Switch
A000	Read RAM Buffer
9000	Read RAM Data
8000	Read PROM Data
7000	Reset Program Strobe
6800	Reset Execute
6000	Write RAM Data
5800	Decrement Memory Address
5000	Increment Memory Address
4000	Reset Memory Address
3000	Set Program Strobe
2000	Preset Memory Address
1000	Load RAM Buffers

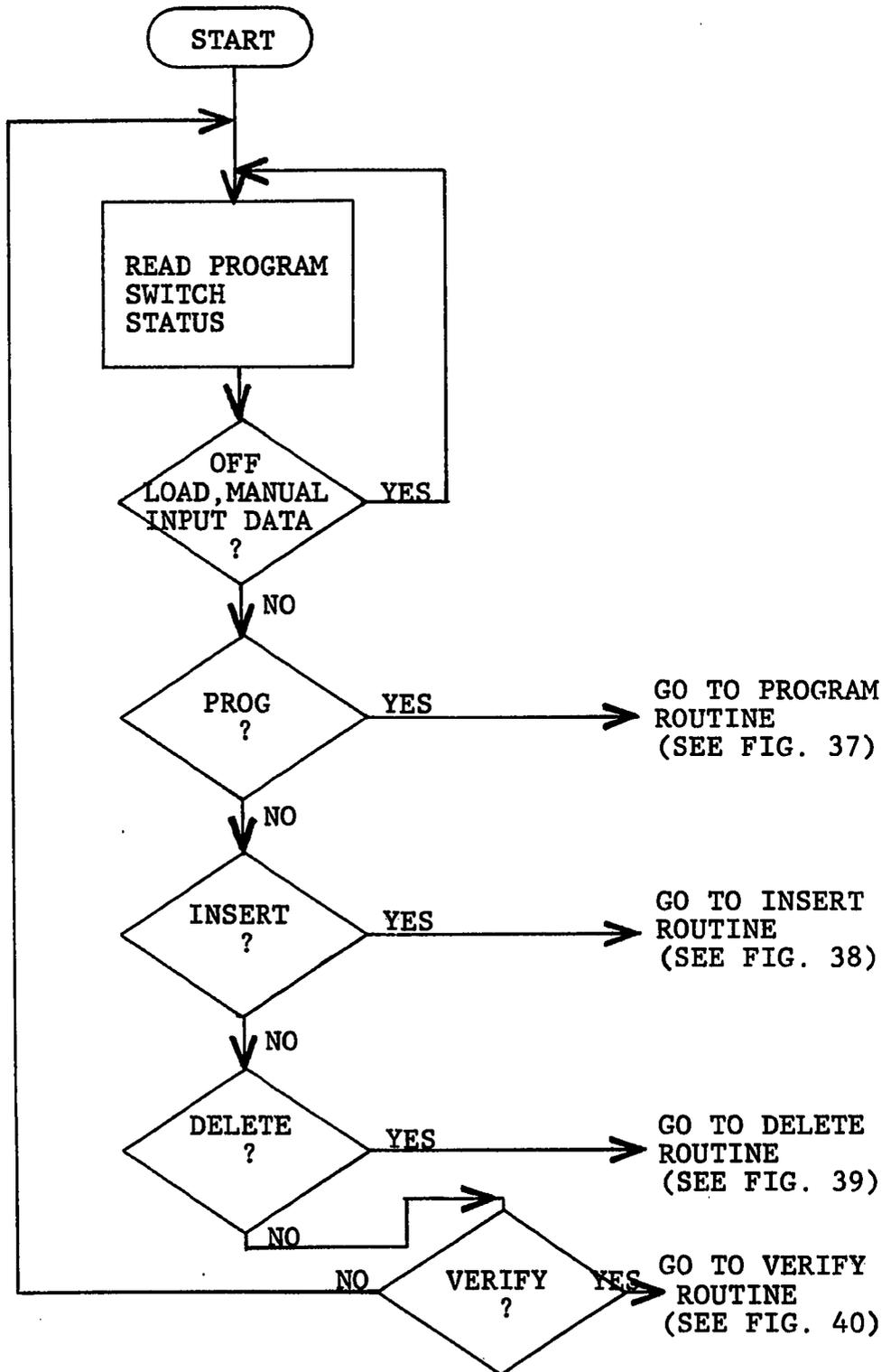


Figure 36. Main Program Routine

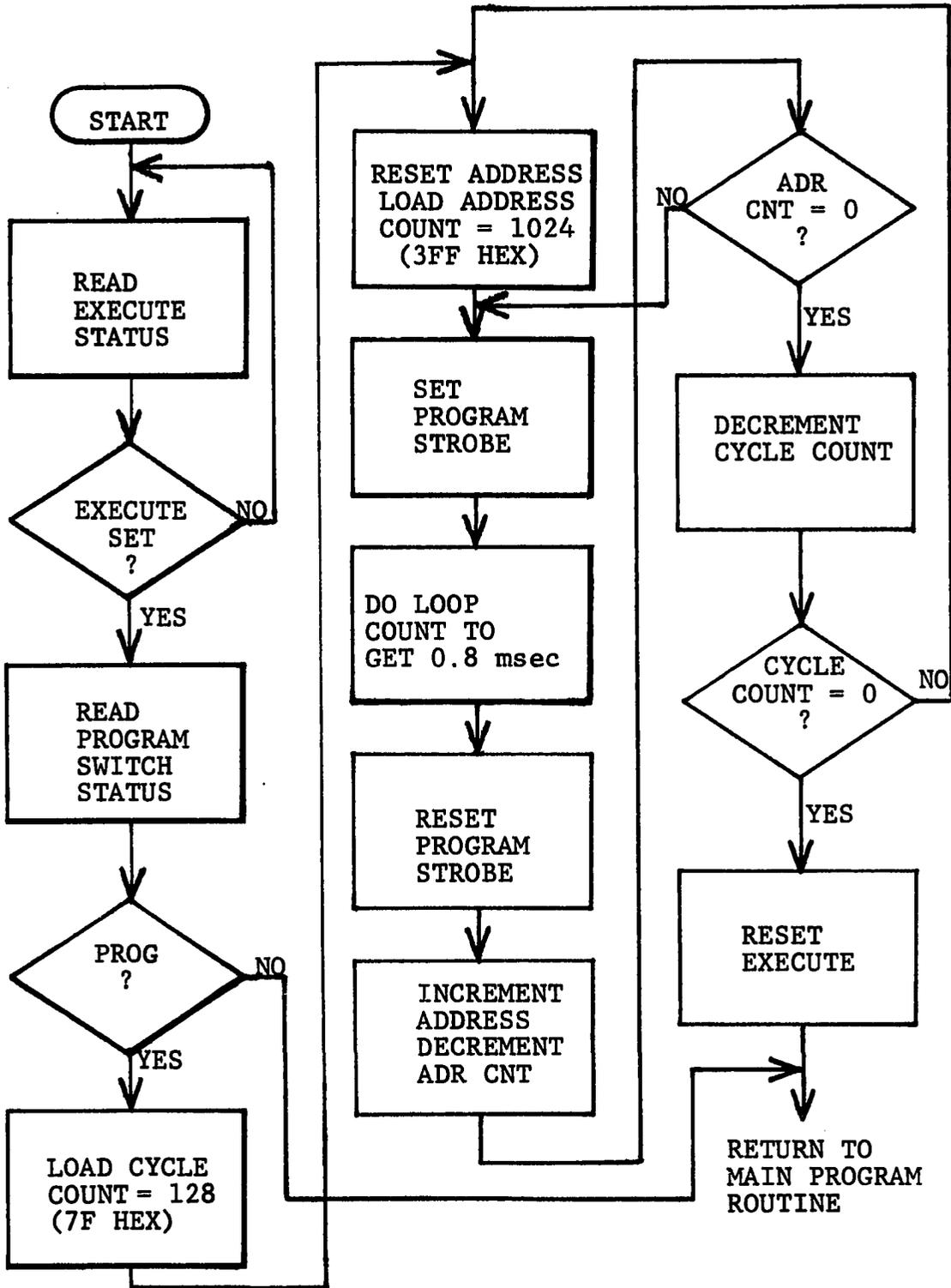


Figure 37. Flowchart for Program Routine

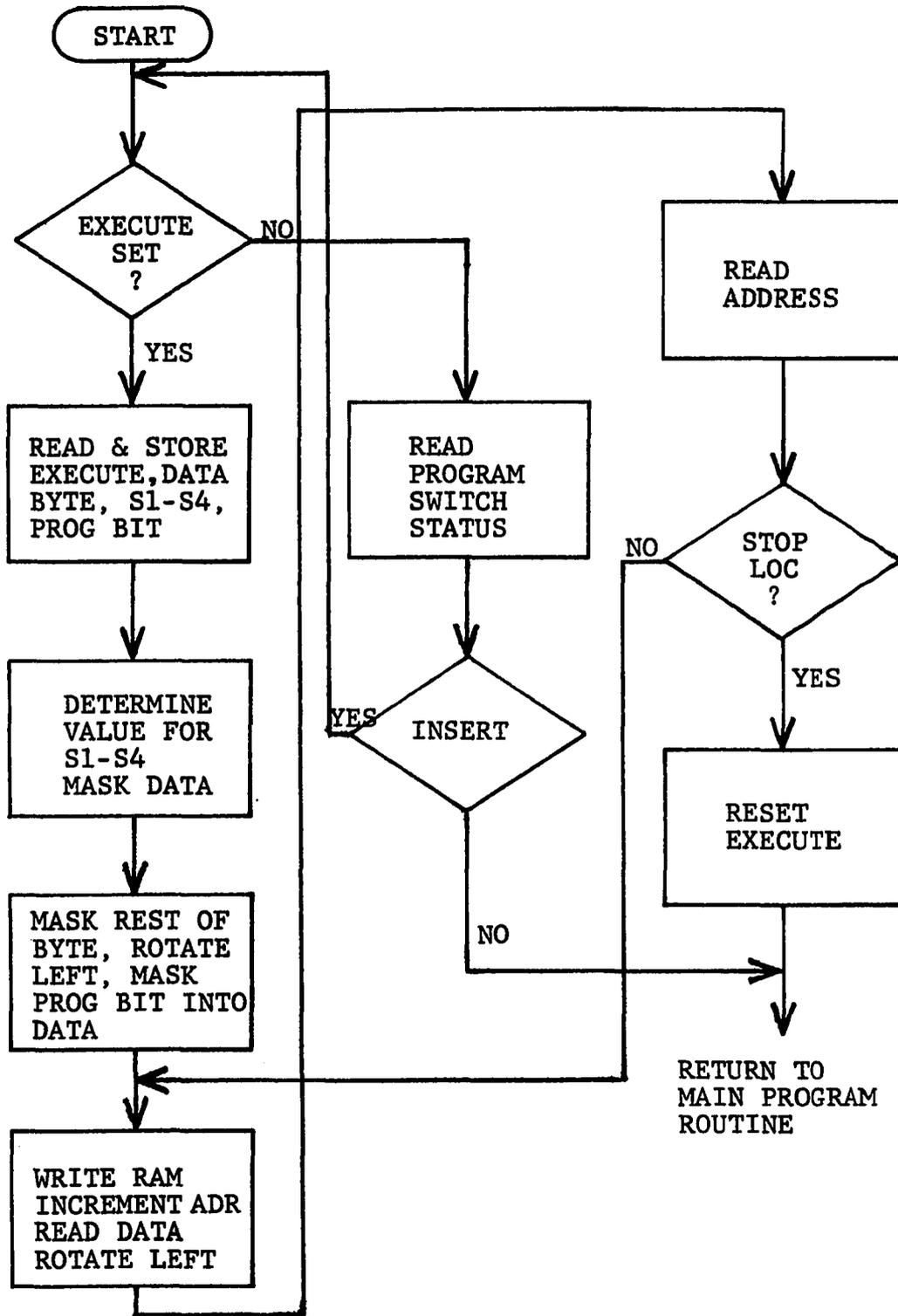


Figure 38. Flowchart for Insert Routine

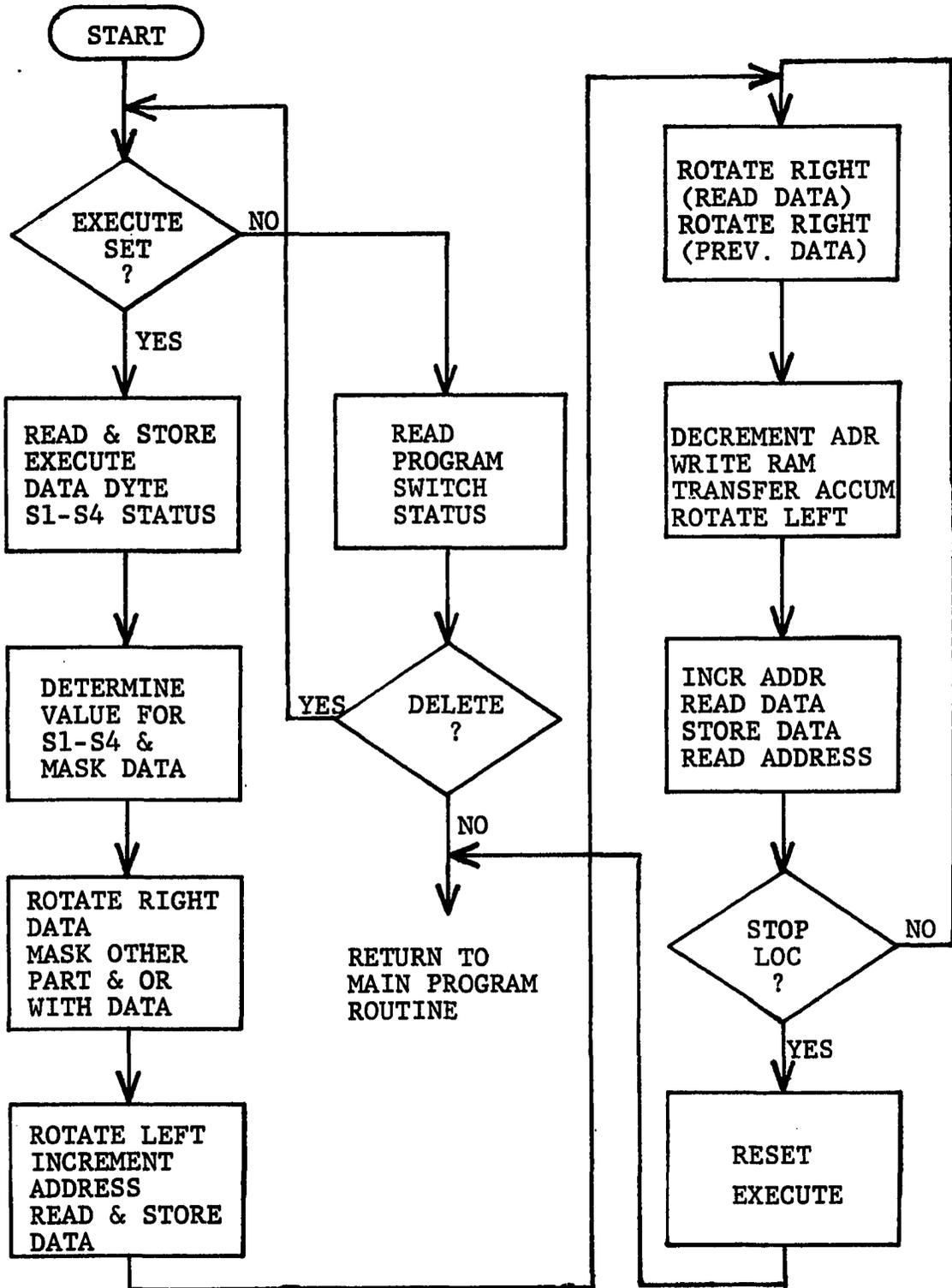


Figure 39. Flowchart for Delete Routine

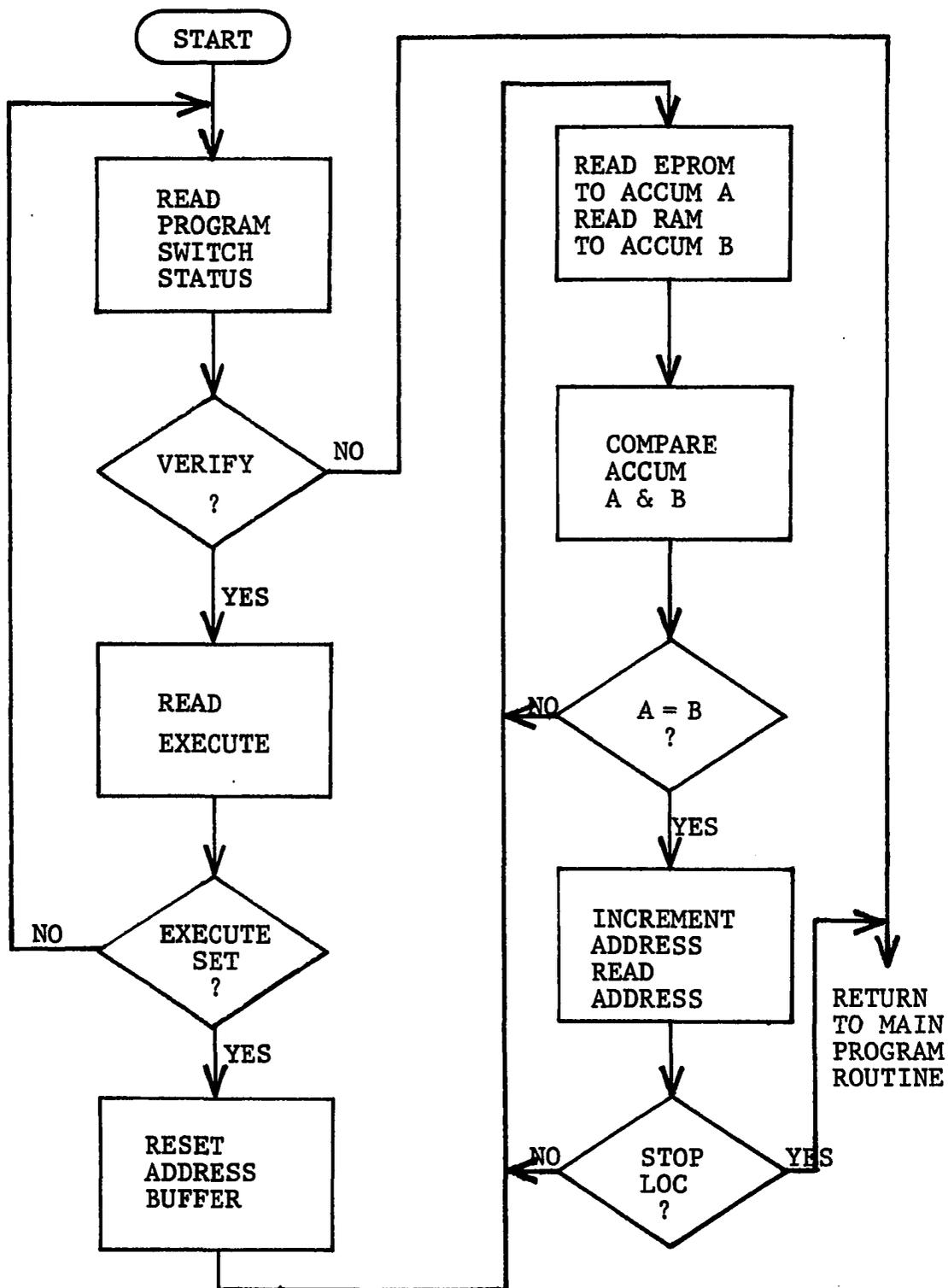


Figure 40. Flowchart for Verify Routine

## Firmware Description

The main operating program is very simple. Figure 36 shows the method used in developing the program. The function performed by the main operating program is to read the status of the PROGRAM switch. The switch is a BCD encoded switch and has a one-of-eight decoder which is presented to the MPU data bus and used as control lines to other logic circuits. The program reads this status byte into accumulator A; it does a series of rotate right and branches to one of the other routines if the carry bit is set. The first four bit functions are not under MPU control; therefore, the branch is back to the read status instructions for the off, load, manual, and input data.

The last four-bit functions are done by MPU control. The program flowchart is shown in Figure 37. Here the routine reads the execute bit status. If the execute switch is pushed, the routine verifies the PROGRAM switch status. If the PROGRAM switch has been changed, the MPU branches back to the main program and makes the appropriate branch based on the new status. The flowcharts for the routines contain enough detail to explain how the firmware functions.

## V. CONSTRUCTION AND TESTING

### Logic Design Principles

The rationale used in the logic design is the result of experience gained over the last nine years. Some of the design principles which served as guidelines in designing the DMG and DSA systems are as follows:

1. Never use one-shots in circuits except to blink lamps.
2. Avoid using the asynchronous inputs to flip-flops.
3. Never use gate delays as a means of re-setting signals.
4. Draw timing diagrams for all circuits that are clocked; add gate delay timing to these diagrams.
5. If possible, keep combination circuits to three or less levels of gate delays.
6. If possible, synchronize all inputs to clock signals.
7. Change data lines on the rising edge of clock signal and load registers on the falling edge of clock signal.

8. Use the inverted clock for testing and error detection.
9. Check all the circuit loads to verify that none exceed the recommended number of logic loads.
10. Use D type flip-flop followers to produce glitch-free timing pulses.

In applying principle number one to the design, only a single one-shot type circuit was used in the DSA and none in the DMG. The DSA has a 555 timer for resetting the display when the unit is in the auto display mode.

The second design principle is more flexible than some of the others. In some situations the asynchronous reset or set inputs could be used; for example, power on reset, restart, or resync conditions.

If the third design principle is followed, no logic race conditions will result. Using logic race conditions for timing can cause problems because all gates do not have uniform delay.

The next six principles are aids which minimize errors. Design principles 4, 7, and 8 are closely related. They are all timing of logic signals which provide a method of checking the timing before building the circuits. The checking of loading (principle 9) is needed to avoid having intermittent signal losses. The synchronizing of all input signals to the master clock (number 6) allows for a starting

reference of all measurements. The error induced will be less than one clock cycle which is significantly less than allowed for in the specification for measurements. The requirement to keep logic to three or less gates (number 5) is flexible. The reason for limiting the logic signals to three levels is because of the clock rate and the logic delays. The clock rate is 1 MHz; thus, there is 500 nanoseconds between clock edges. Using an allowance for clock skew of  $\pm 100$  nanoseconds leaves 400 nanoseconds for propagation time. By allowing one delay for set up time, the active time between clock edges is then only 300 nanoseconds. It should be noted that the flexibility in this case is when the signals are not needed until the next rising clock edge, then another four levels of gating can be allowed.

The last principle (10) is very helpful when developing timing for either counter circuits or sequences. The input to the two stages of D flip-flops is the signal used to activate either a counting sequence or some logic sequence to be measured. The sequence used from this circuit is four states; for example, the four states could be an enable, an idle state, a store value, and a clear, or other combinations of four states. A similar circuit for decoders uses the second half of the clock cycle as an enable to the decoders.

The interfacing between logic levels was accomplished using CMOS chips. The +5V logic was interfaced to the +12V CMOS logic by using MC14504. The design in the DMG used a

TTL 7406 chip because the MC14504 was not available when the logic design was completed and debug began; however, we were able to obtain the MC14504 to use in building the DSA.

The CMOS +12V was interfaced to the +5V using either the MC14049 or the MC14050. (The MC14049s are inverting gates while the MC14050s are non-inverting.) The +28V used 2N2222 transistors to interface to the logic circuits.

Other design elements to consider were the filtering on the artwork of the PWA and the power distribution in the cabling. These relate to possible design problems due to noise. In this case the signal cables have alternate wires as grounds and the +5V and +12V power uses multiple wires in the cable.

The PWBs were all designed using the following design principles: Each PWB that used CMOS circuits had one 6.8 microfarad capacitor and one 0.1 microfarad capacitor for every 10 ICs. The following principles were followed for the few TTL low-power Schottky circuits: One 6.8 microfarad capacitor for every 10 ICs; 0.1 microfarad capacitor, either one for every three SSI chips, or one for every MSI or LSI chip.

#### Problems Encountered

By carefully following the above principles, very few problems were encountered. A majority of the problems were due to the technician misinterpreting the schematics. Frequent errors occurred when he misunderstood the way the

flip-flops were drawn and missed inverters when the logic signals went from one page to other pages. I drew the J- $\bar{K}$  flip-flop as shown in the data books for high active input, but inverted the figure to represent low-active input; however, the technician failed to invert the flip-flop when wiring the breadboard; thus, when the DMG was wirewrapped on boards some flip-flops were wired wrong. Also a lot of wiring errors occurred when wires were put on the wrong pins or on the wrong chip positions.

One timing problem occurred due to an inverter being left off a clock signal which extended from one page of the schematic to another. The logic name was correct for the signal but the technician wired a non-inverted clock. In addition to the wiring error, the technician, trying to correct the problem, put other flip-flops in the circuit which only caused more trouble. After removing the technician's patch, I was able to determine that the clock phase was wired wrong to one of the flip-flops.

The major timing problem in the DMG was connected with the phase-locked loop clock circuit. Occasionally the jitter in the clock output would exceed the specifications. I finally determined that the problem was partially caused by the delay time of the CMOS flip-flops used to divide the crystal oscillator down to the phase-locked loop reference frequency. By replacing three CMOS flip-flops with TTL low-power Schottky flip-flops the jitter was reduced

enough to meet the specifications.

The problems encountered in the DSA were very similar to the those in the DMG; namely, wiring errors on the breadboarded model and missing inverters. To aid in the debug, I gave the technician a state-flow diagram or major timing diagrams before he started debugging each circuit. This helped to shorten the debug cycle. Other problems involved artwork errors as we went from the wirewrapped model to the hardboard model.

A major problem in the DSA which was discovered in the breadboard model, was the drooping of the +12V when the display was illuminated. To correct this problem a second set of +12V regulators were added to the DSA power supply to drive the LEDs and the display.

There were many minor problems common to constructing any device, such as the holes misdrilled in the front panel, ICs which did not arrive on time, an IC left off the artwork, runs left off the artwork, and other little but irritating problems.

#### Description of Unit Construction

The construction of the units was in modular form. The front and back panels are a group of PWAs with connectors in order to connect together all the modules with one strip of ribbon cable. The cable is a 60 conductor flat ribbon cable and is cut to fit as a PWA back panel and interconnecting cable.

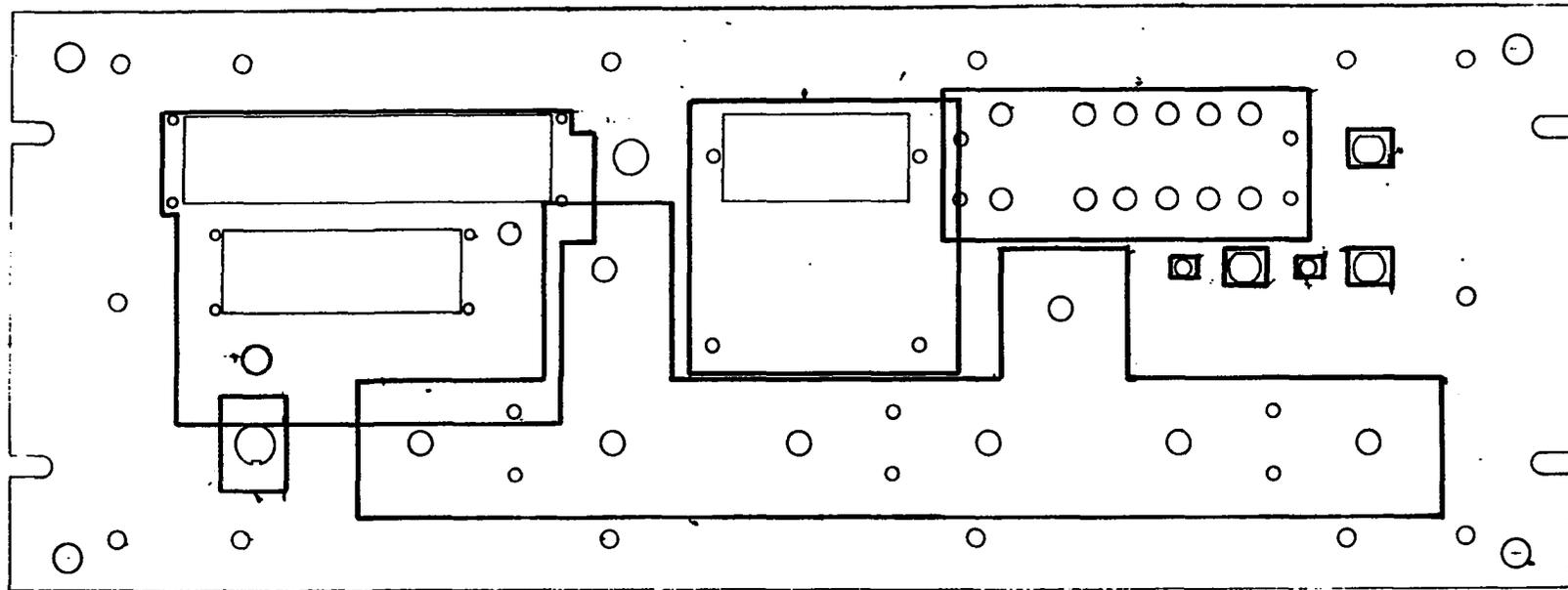
Figure 41 is a sketch of how the PWAs are mounted to the front panel of the DSA. The thumbwheel switch assembly is the same for both the DSA and the DMG. Figures 42 and 43 are the artworks for this assembly. Figure 44 shows the thumbwheel switch assembly. The ICs and connectors are mounted on the back side of the PWB. The thumbwheel switches are mounted on the front side of the PWB as shown in Figure 44 by dotted lines. Figures 45 and 46 show the thumbwheel switches and the way they mount to the PWB using the pins on the end of the switch. Figure 45 is the thumbwheel switch used for the start memory address, the stop memory address and the percentage of distortion. Figure 46 is the baud rate thumbwheel switch. The least significant digit on the baud rate thumbwheel switch is an engraved zero. The three LEDs between the switches are connected to the range switch. They illuminate for the proper value. The thumbwheel switch assembly schematic is Figure 47.

The modular construction of the unit can be shown by several examples of these assemblies. Figure 48 is the back panel assembly for the DSA. There are two PWAs shown here. One PWA is used for the toggle switches and the other PWA is used for the block length thumbwheel switches. There are many different sizes and shapes of PWAs used in the units. Figure 49 is the artwork for the rotary switch assemblies for the DSA. Figure 50 shows the rotary switch assembly for the DMG front panel. The E pins are standoffs used for

test points on the PWA. The switches were turned on the artwork to get the best fit. The switches are rotary switches with BCD outputs.

Another good example of the modular construction is represented by the toggle switch assembly for the DMG front panel. This assembly consists of the selected character bits switches with other toggle switches below them. Figure 51 shows the PWA. Here the toggle switches are mounted on the back side while the logic, components, and connectors are mounted on the front side. Figure 52 is the schematic for the toggle switch assembly. This represented an improvement over the GGM-16 and GGM-21 as the switches were individually mounted and hand wired. Thus, any failure would require the unit to be removed from the rack and repaired on the bench. The DSA and DMG could have a new assembly mounted while still in the rack.

The PWAs as panel assemblies have other purposes in addition to mounting the switches and indicators. The switch PWA on the back panel of the DMG is a good example. Figure 53 is the back panel switch assembly. On this assembly are the connections for the back panel used as the RS-232-C port, in addition to the connectors for cabling to the logic PWAs. An additional feature on this assembly is the terminal strips that are used to strap options. These straps were specified in the design specification. The terminal strips are wire-wrap posts and the options can be wired as desired. Figure 54



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Figure 41. Outline of Front Panel PWA on the DSA

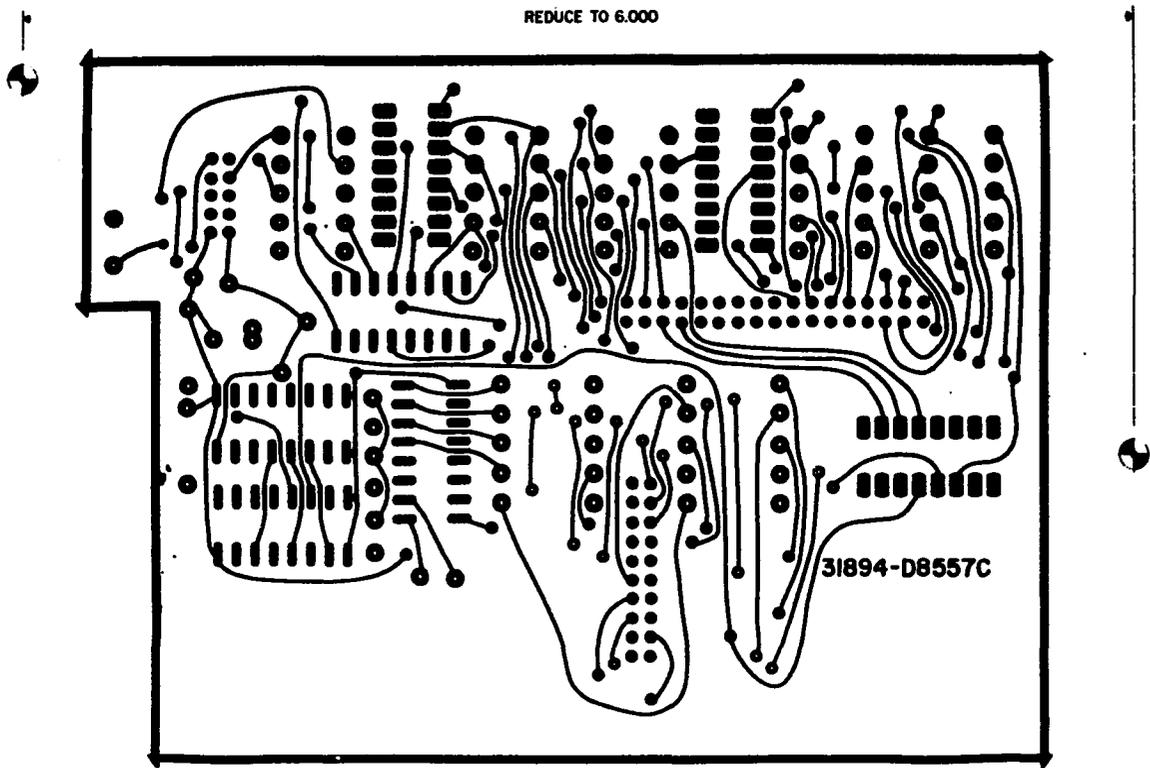


Figure 42. Front Side Artwork for the DMG  
Front Panel Thumbwheel Switch Assembly

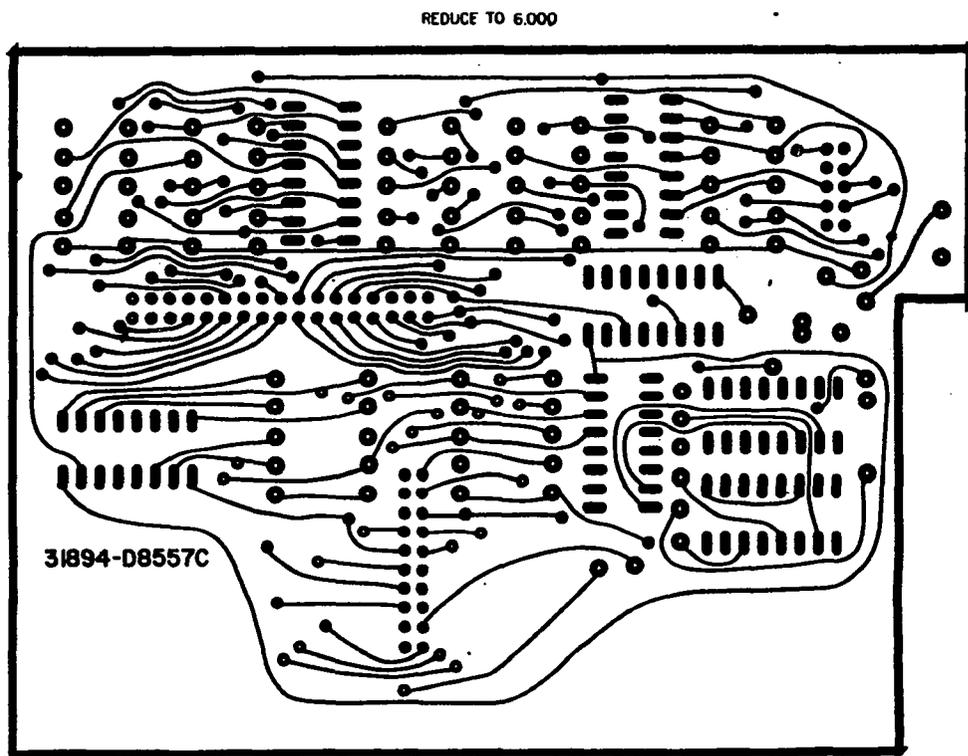
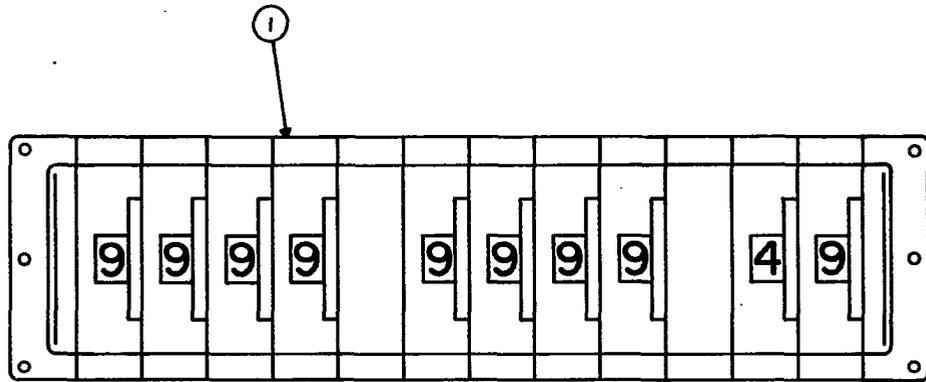
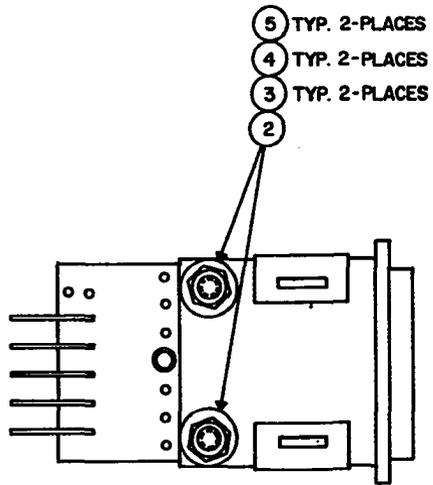


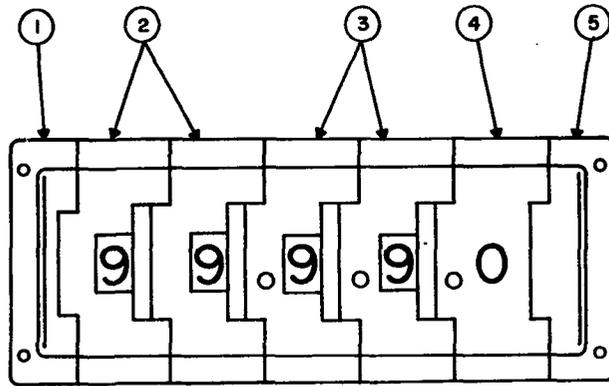
Figure 43. Back Side Artwork for the DMG  
Front Panel Thumbwheel Switch Assembly



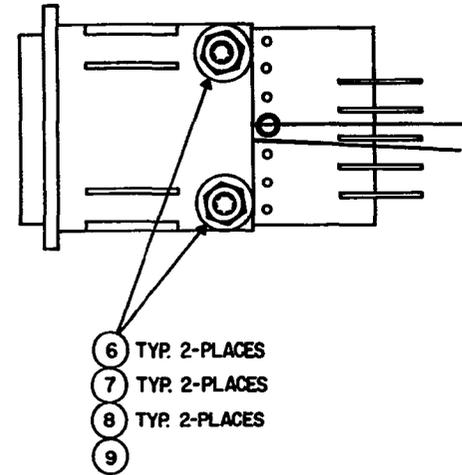


NOTE: FOR PARTS LIST, REFER TO RNL DRAWING NUMBER PL8612.

Figure 45. Memory Location and Distortion  
Thumbwheel Switch Assembly



NOTE: FOR PARTS LIST, REFER TO RNL DRAWING NUMBER PL8611.



- 6 TYP. 2-PLACES
- 7 TYP. 2-PLACES
- 8 TYP. 2-PLACES
- 9

Figure 46. Baud Rate Thumbwheel Switch Assembly

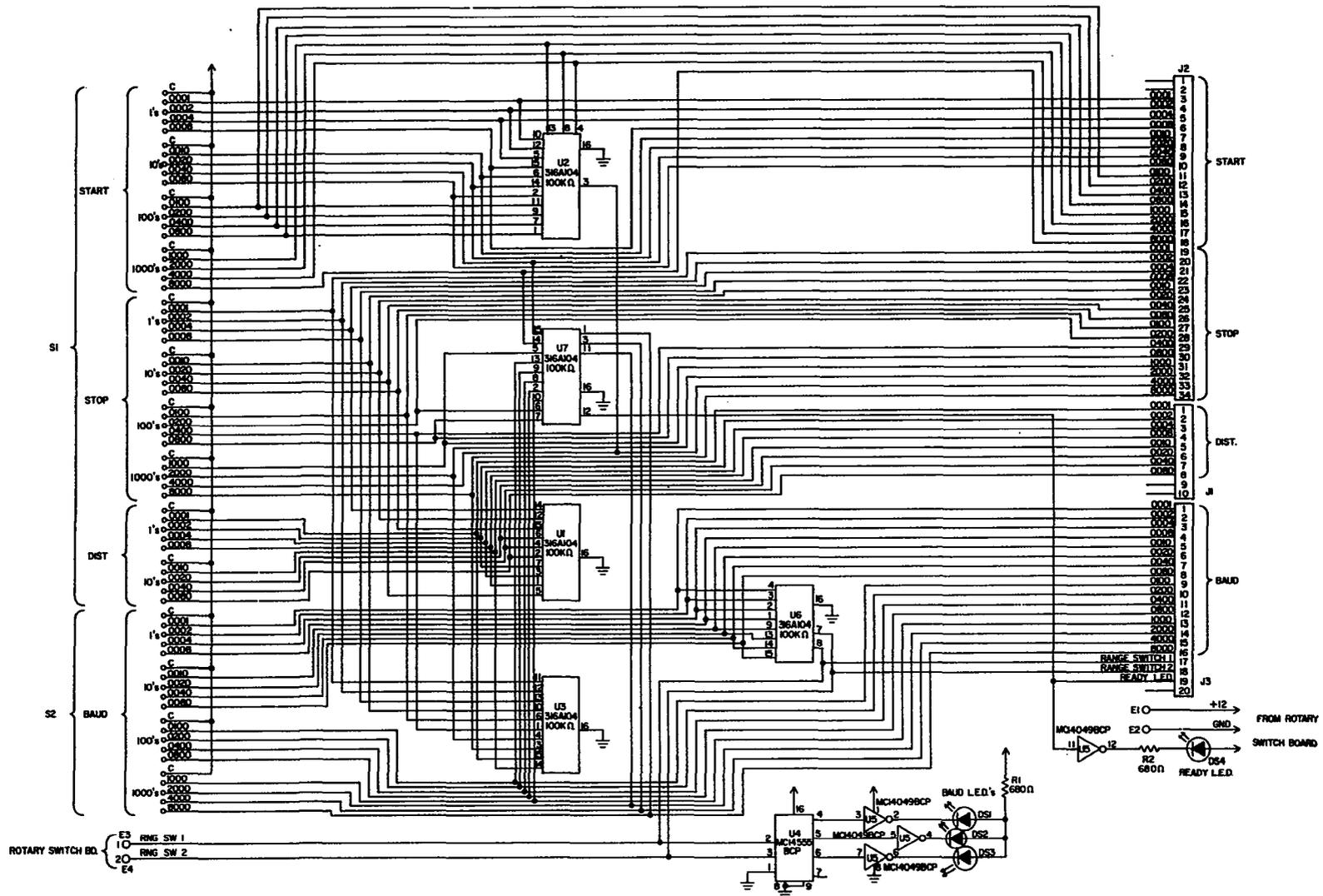
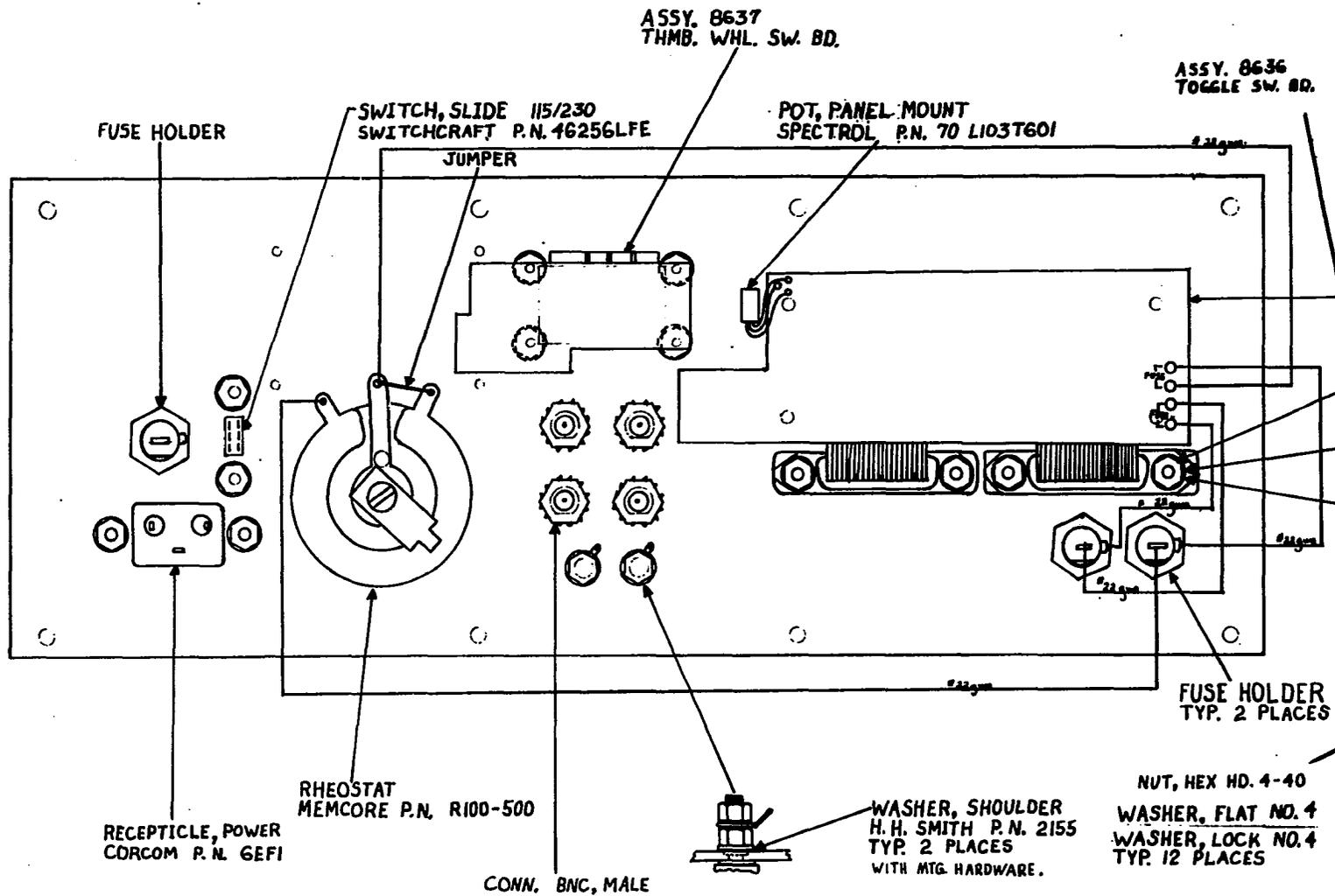


Figure 47. Schematic Diagram Front Panel Thumbwheel Switch Board



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Figure 48. Back Panel Assembly for the DSA

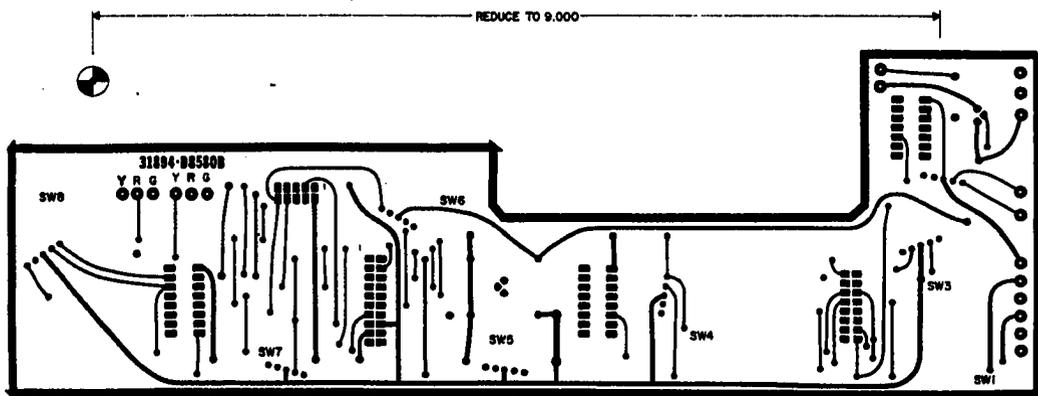
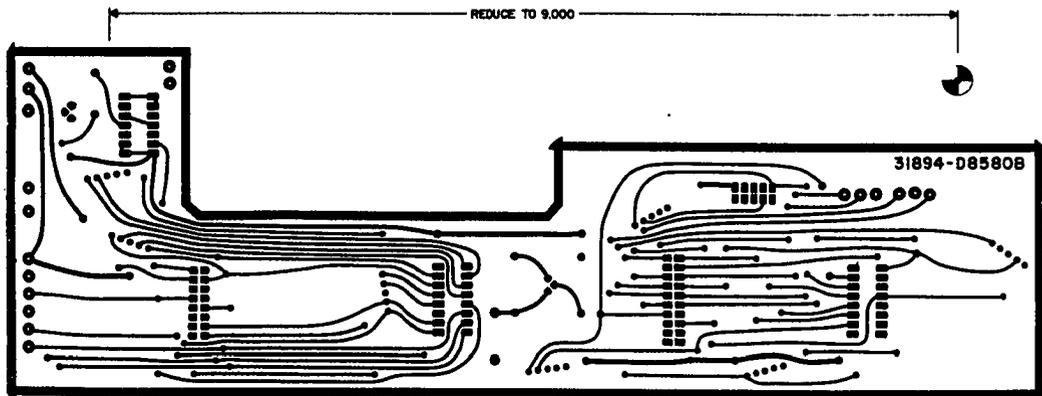
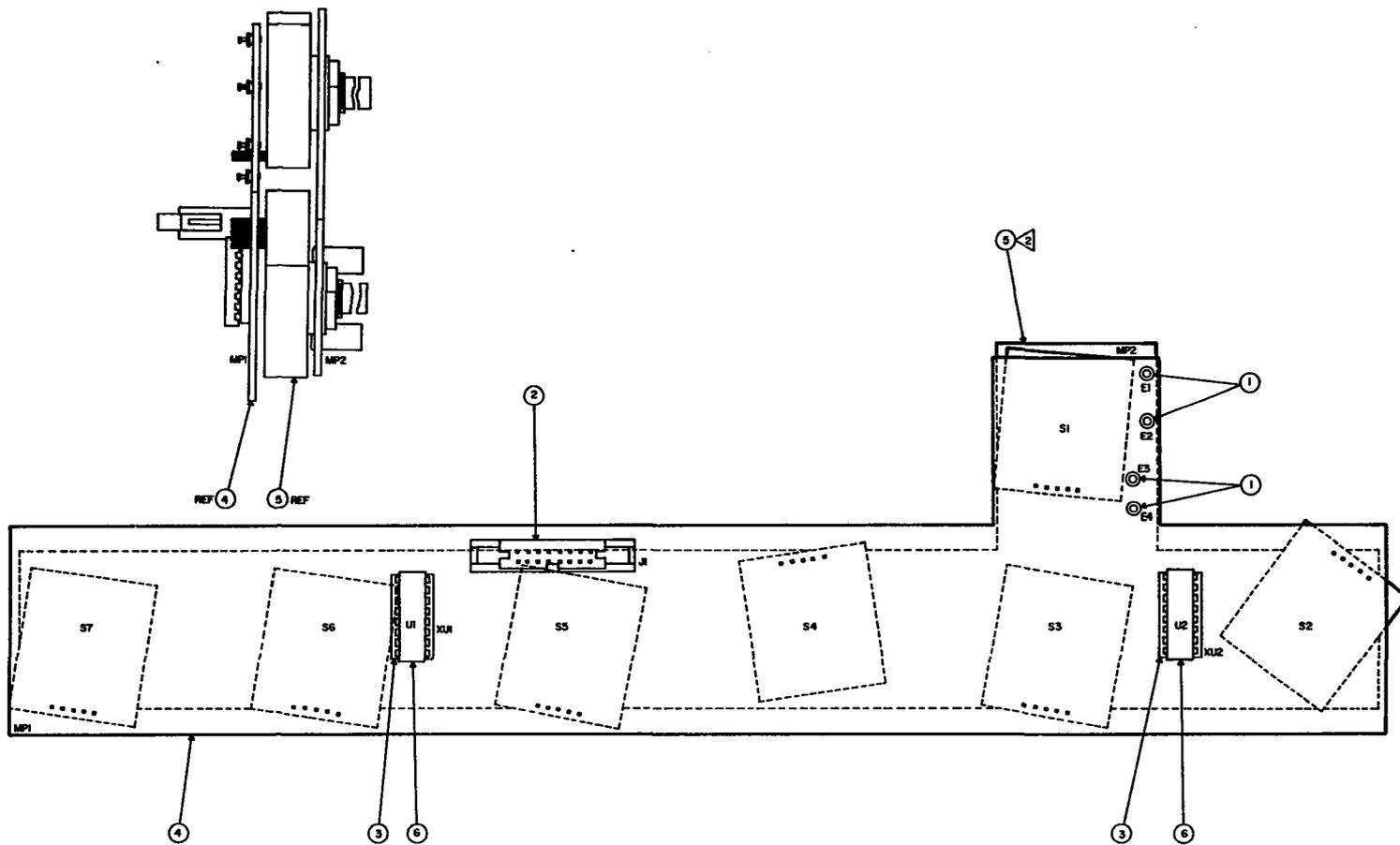


Figure 49. Front Side and Back Side Artworks for Rotary Switch Assembly

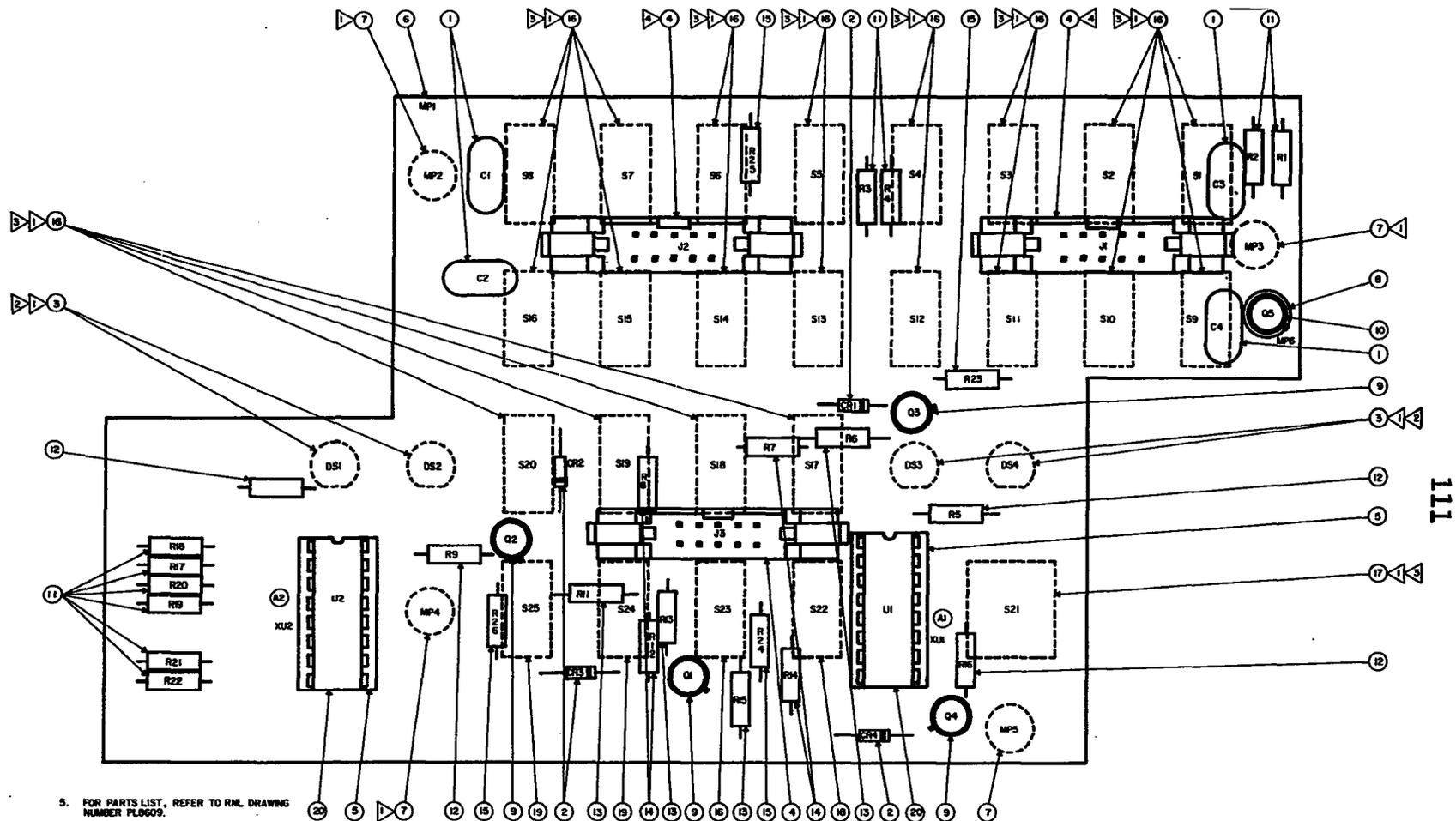


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ASSEMBLE PRINTED CIRCUIT BOARD BEFORE MOUNTING SUBASSEMBLY.

NOTES: 1. FOR PARTS LIST, REFER TO RNL DRAWING NUMBER PL6G15.

Figure 50. Front Panel Rotary Switch Assembly for the DMG



5. FOR PARTS LIST, REFER TO RML DRAWING NUMBER PL9609.

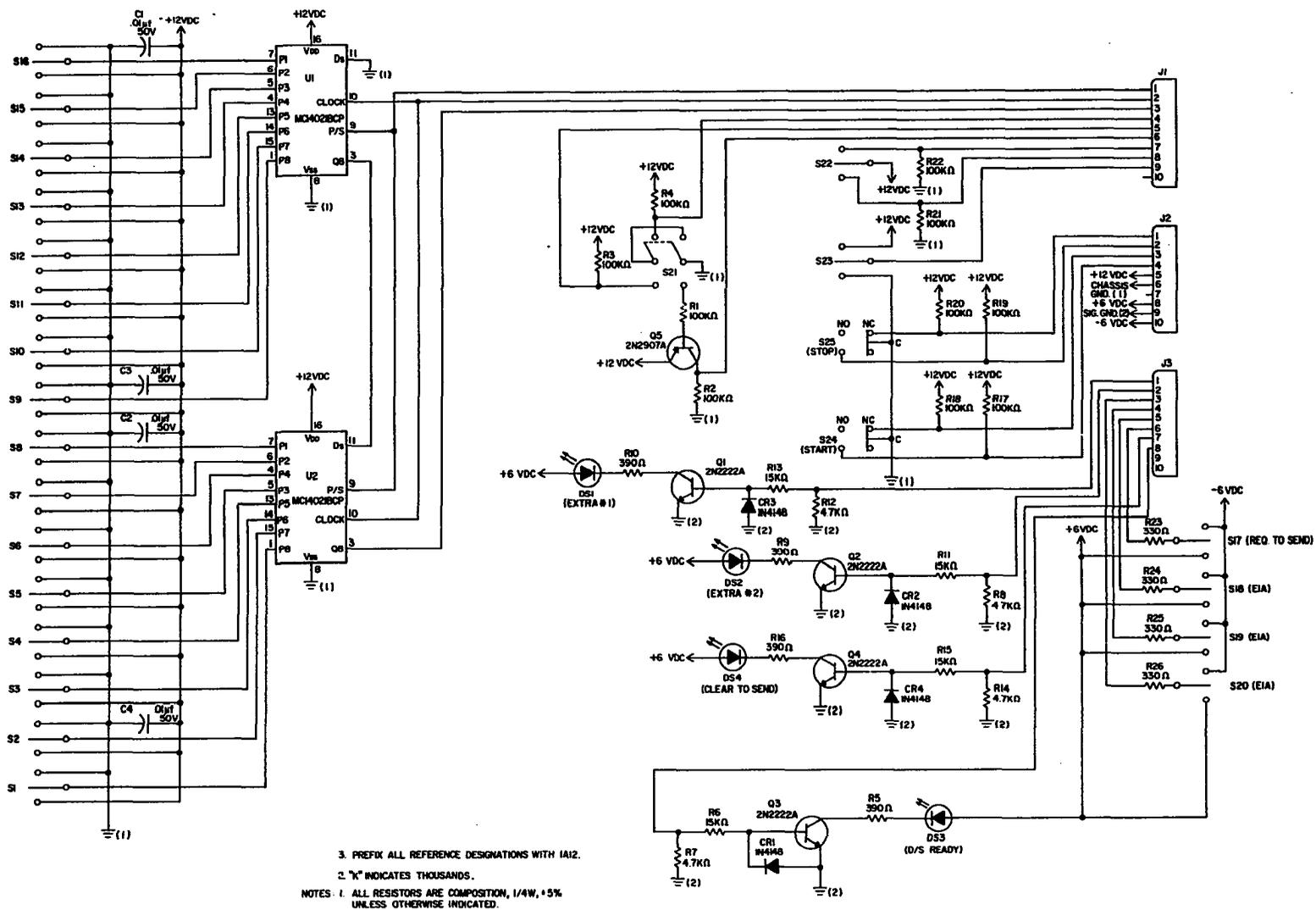
▲ MOUNT CONNECTORS LAST.

▲ MOUNT ALL SWITCHES PLACING THE KEYS ON SWITCHES S1-S23 SO THAT THEY FACE DOWN AND THE KEYS ON S24 AND S25 SO THAT THEY FACE UP WHEN MOUNTED TO THE FRONT PANEL. PUSH SWITCHES AS CLOSE TO THE BOARD AS POSSIBLE AND SOLDER INTO PLACE.

▲ MOUNT LEDS IN THEIR RESPECTIVE POSITIONS BEING SURE TO OBSERVE POLARITY. MOUNT THE PRINTED CIRCUIT BOARD ON THE FRONT PANEL. ALIGN THE LEDS AND SNAP THEM INTO THEIR RETAINERS WHICH ARE MOUNTED ON THE FRONT PANEL. SOLDER THE LEDS IN PLACE AND CLIP EXCESS LEADS. REMOVE THE PRINTED CIRCUIT BOARD.

NOTES: ▲ COMPONENTS IN DOTTED LINES INDICATE MOUNTING ON THE OPPOSITE SIDE OF THE PRINTED CIRCUIT BOARD.

Figure 51. Front Panel Toggle Switch Assembly for the DMG



3. PREFIX ALL REFERENCE DESIGNATIONS WITH IA12.  
 2. "K" INDICATES THOUSANDS.  
 NOTES: 1. ALL RESISTORS ARE COMPOSITION, 1/4W, ±5% UNLESS OTHERWISE INDICATED.

Figure 52. Schematic Diagram Toggle Switch Assembly

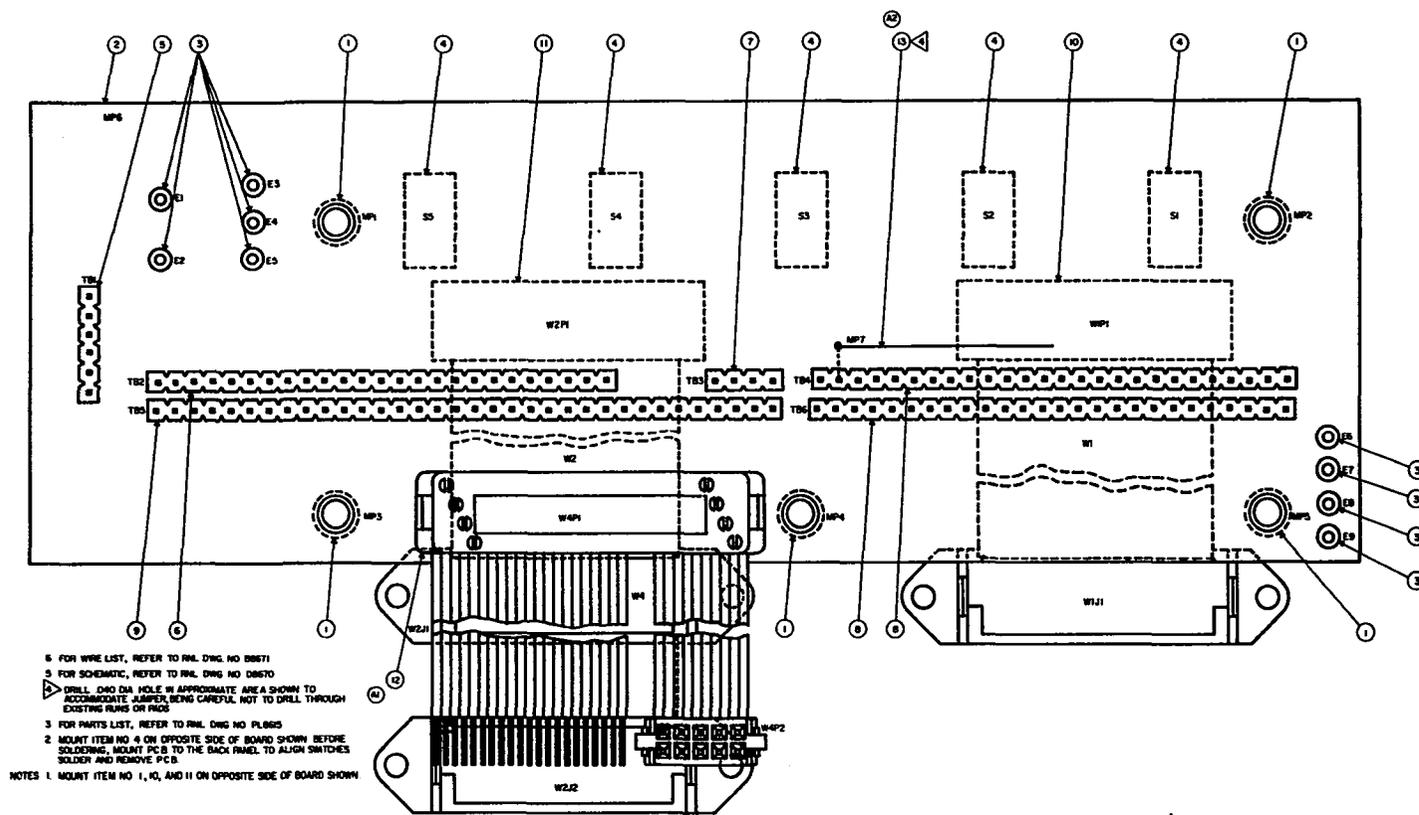


Figure 53. Back Panel Switches and Input/Output Assembly for the DMG

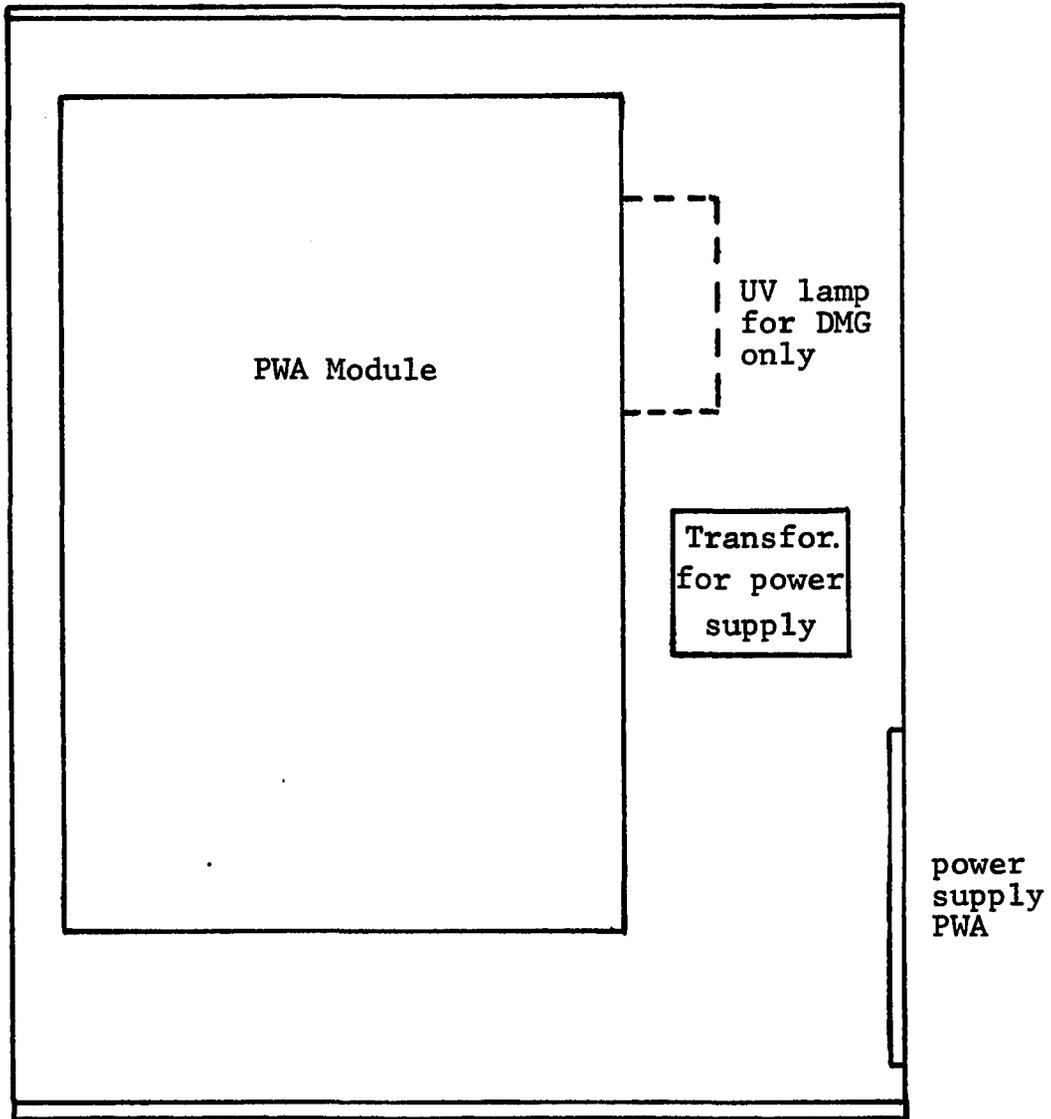


is the schematic for the back panel switch assembly. The design is modular for replacement at the PWA level. This method reduces the downtime of the equipment and provides for the sale of spare parts, the profit being in the spare parts.

Figure 55 is a sketch of the typical construction of the units. It shows the relationship of each modular unit. Figure 56 is the DMG PWA module, while Figure 57 is the DSA PWA module. Each PWA has been named by its function. The power supplies are on the side back corner. The DMG power supply is the same as the DSA, except the unused regulators and components are not on the assembly. Figure 58 shows the power supply assembly for the DMG. It should be noted that some components and regulators are not on this assembly. These are added when the assembly is used in the DSA. The regulators are mounted to a heatsink. They are detailed in Figure 59 which shows the heatsink assembly. The transformer for the power supply is mounted in the front of the unit.

The front and back panels are hinged so that either can be dropped forward to gain access to the interior of the unit. The plan is to rack mount these units; thus, these panels will be the only accessible entry to the interior of the unit. The tops are held in place with screws and the units can be removed from the rack, the top removed and repair performed on a bench. This was an improvement over the GGM-16 and GGM-21 as they were accessible only from the top. Therefore, repairs could only be made by removing the unit from the rack.

Front Panel



Back Panel

Figure 55. Typical Arrangement of Assemblies

Start/Stop
PROM Addr
MPU/MEM Sync
RAM MUX
Decode
Clock
AVE/MEM Sync
Distn Counter
Meas Counter
Error Meas
Control
I/O No. 1
I/O No. 2

Front Panel

Figure 57. PWA Arrangement in DSA

Clock
Start/Stop
PROM Addr
Memory
Msg Sel/Msg Distn
Control
Run Control
I/O No. 1
I/O No. 2
Spare for Extender
Spare for PROM Erase

Front Panel

Figure 56. PWA Arrangement in DMG

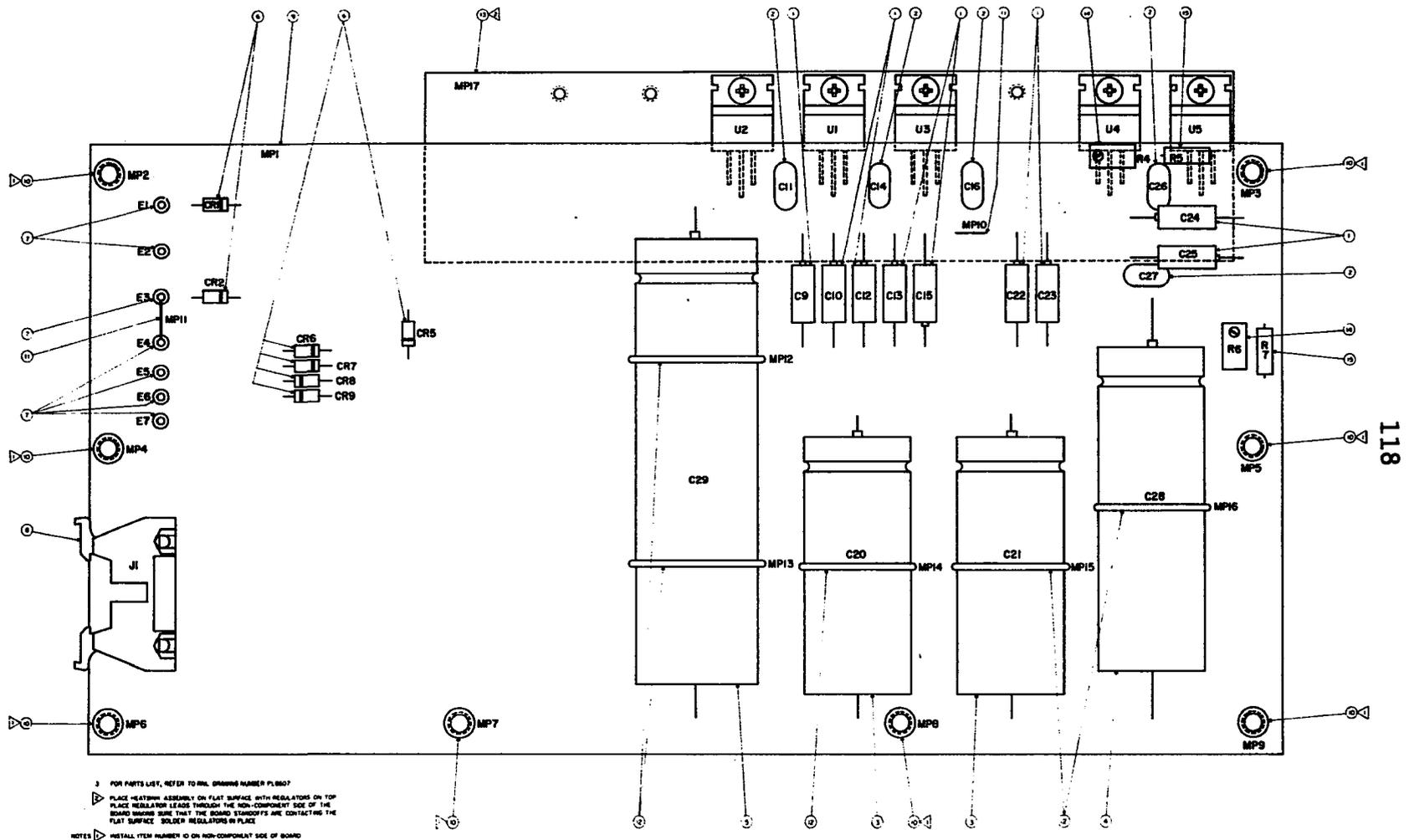
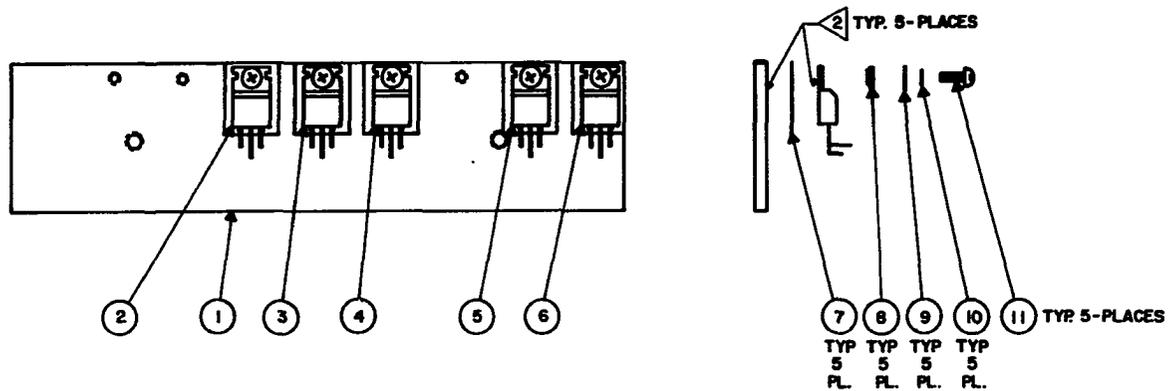


Figure 58. Power Supply Assembly for the DMG



3. FOR PARTS LIST, REFER TO RNL DRAWING NUMBER PL8655.

2 APPLY ITEM NUMBER 12 TO SURFACES INDICATED BEFORE ASSEMBLY.

NOTES: 1. FORM LEADS OF REGULATORS BEFORE ASSEMBLY USING THE FOLLOWING TOOLS:

- a. BENCH PRESS - T & B ANSLEY P/N 779-3100
- b. BASEPLATE - RNL P/N A8573.
- c. PUNCH - RNL P/N A8574

Figure 59. Heatsink Assembly Power Supply Board in the DMG

### Description of Printed Wiring Assemblies

The PWA can slide into the logic module from the back of the unit. The PWAs are five inches high and ten inches long with a 60 pin connector. Each PWA can hold up to 34 integrated circuits. Figures 60 and 61 are an example of a PWA artwork. Figure 60 shows the front side of the PWA and Figure 61 shows the back side. Examples of the PWAs are given in Figures 62 and 63. Figure 62 shows the start/-stop address PWA assembly; Figure 63 is the schematic. Further examples are Figures 64 through 67, which show the assemblies and schematics.

In order to be able to troubleshoot the PWAs an extender PWB was designed. Figure 68 shows the extender PWB. The PWB is fifteen inches long with test points for each connector pin. The extender allows the PWA to be placed outside the logic module for easy access to the chips.

### Description of Testing Procedures

The use of this equipment in the field will be two-fold. First, to test systems at a given location using both units. Secondly, to test lines between locations by sending and receiving from one location to a distant location. The test equipment at the other location may not be this system. Therefore, the unit is tested using the GGM-16 and the GGM-21. The Digital Data Analysis System (DDAS) which is composed of the DMG and the DSA must work with either the GGM-16 or the GGM-21.

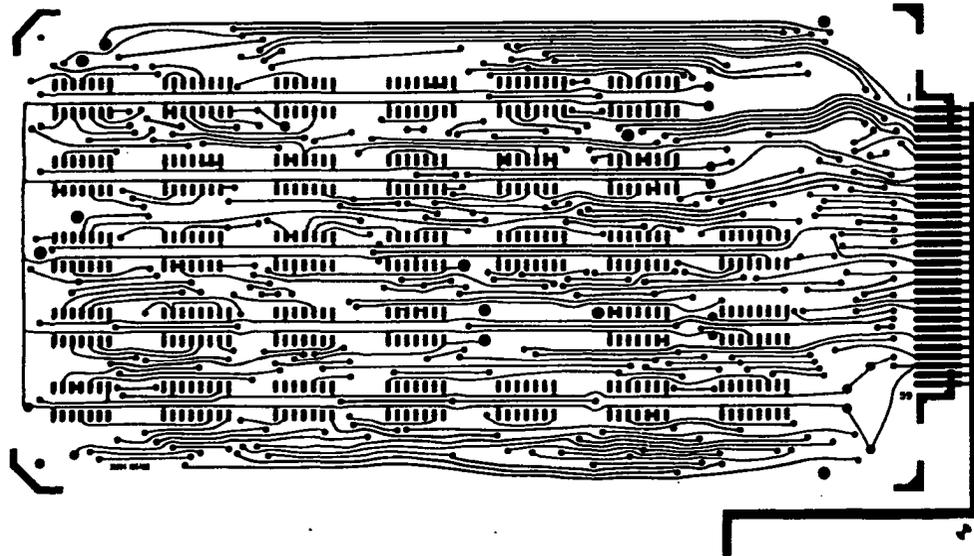


Figure 60. Typical PWA Artwork Front Side

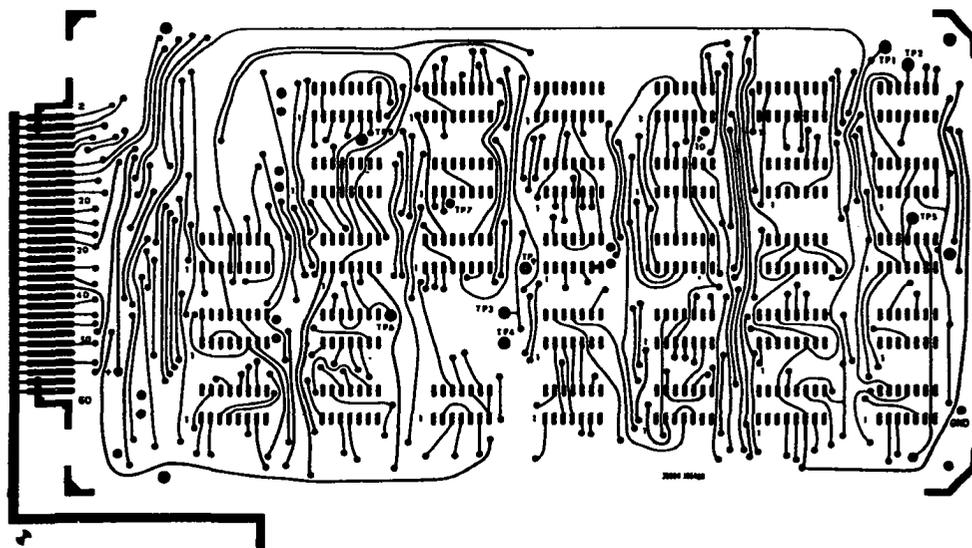


Figure 61. Typical PWA Artwork Back Side

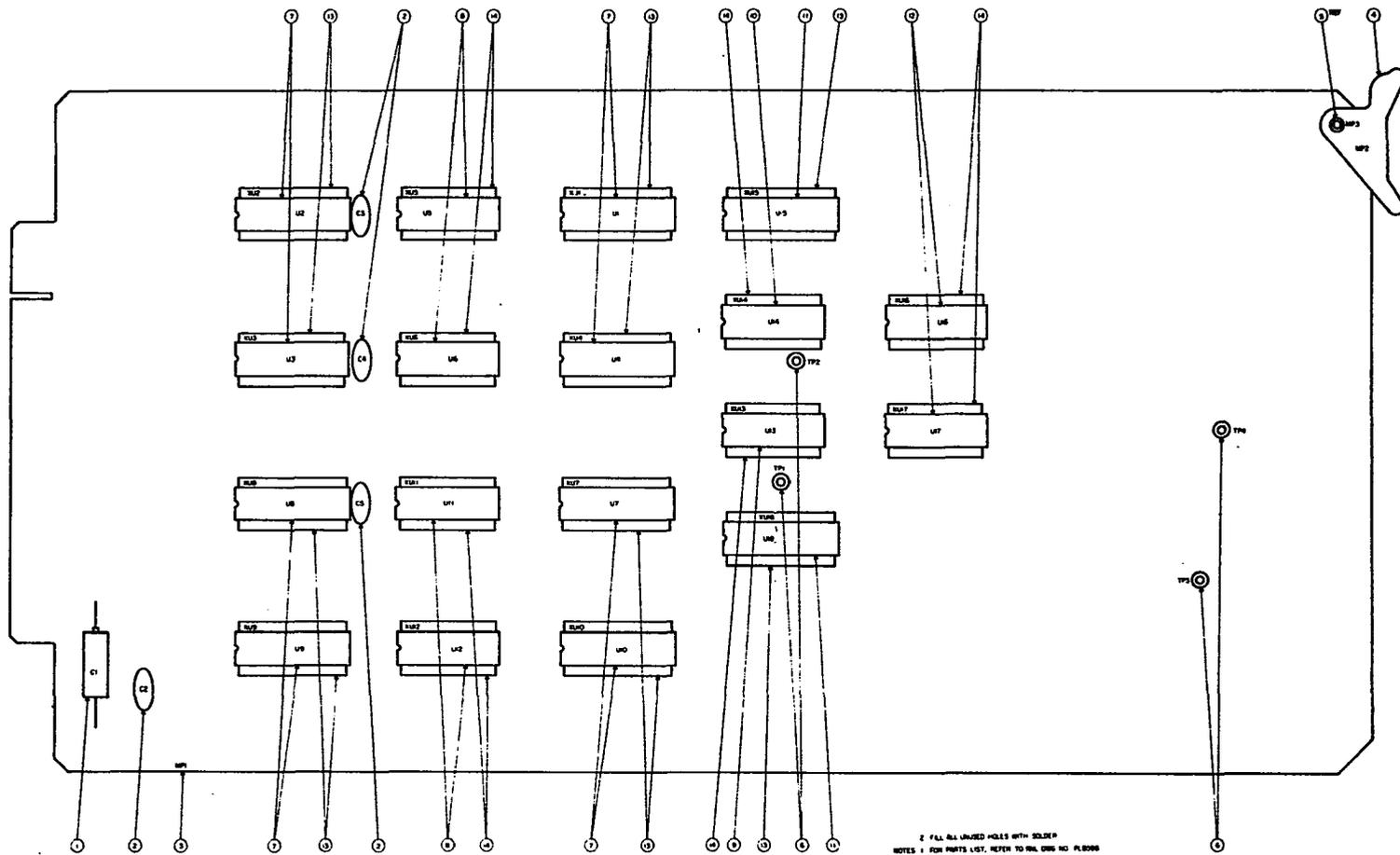


Figure 62. Start/Stop Address PWA Assembly

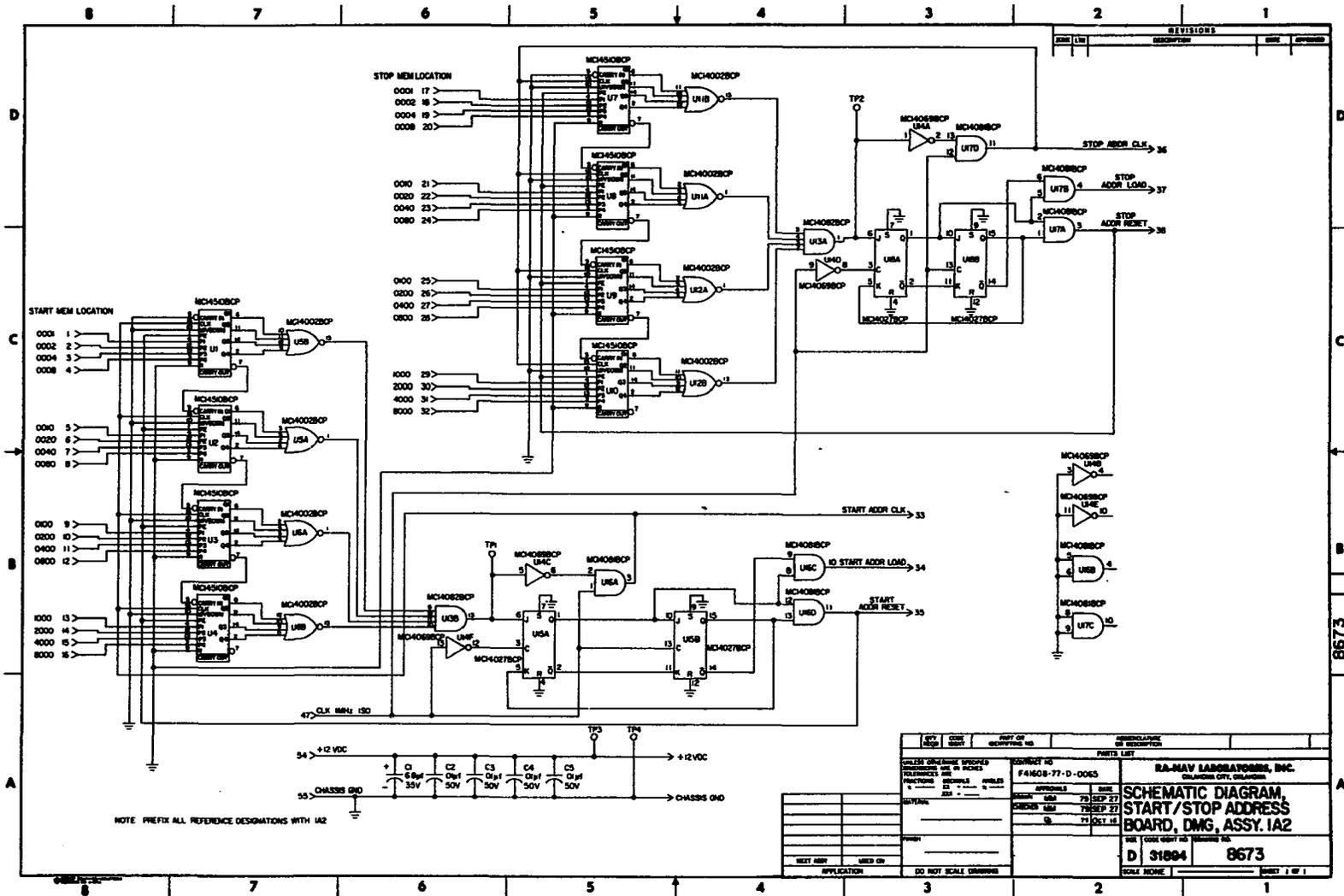


Figure 63. Schematic Diagram for Start/Stop Address PWA

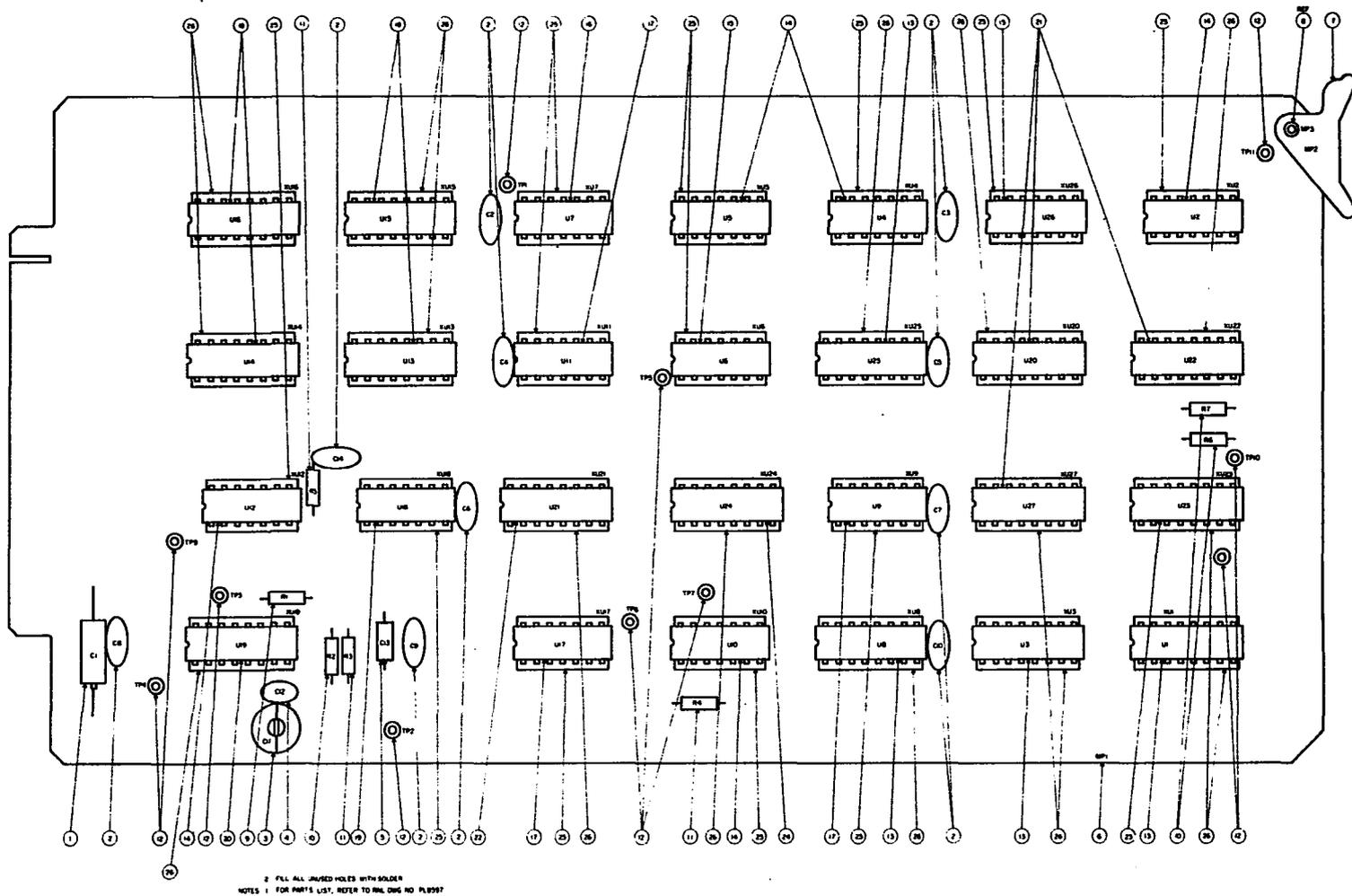
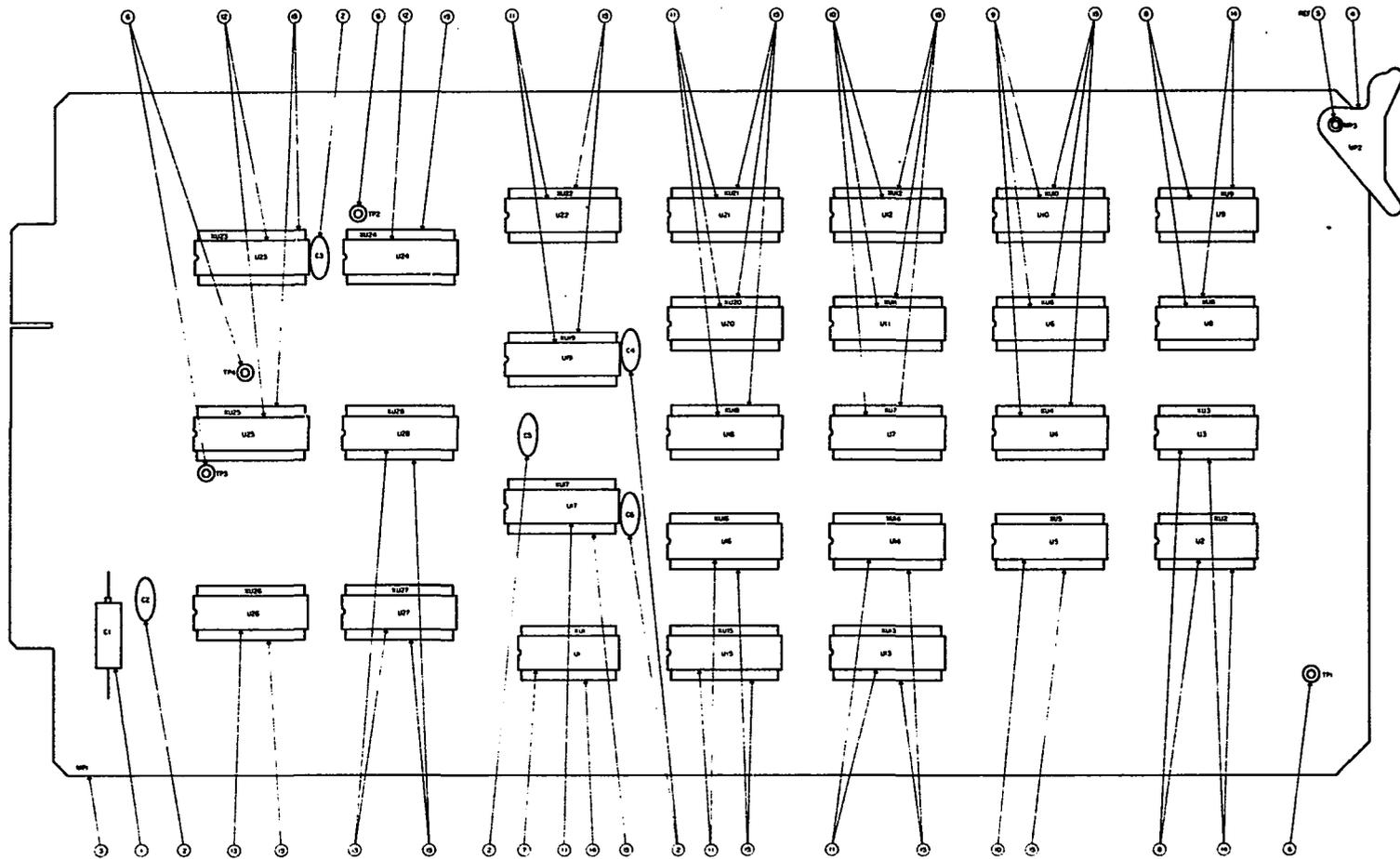


Figure 64. Clock PWA Assembly





2 FILL ALL UNUSED HOLES WITH 20.020  
 NOTES - FOR PARTS LIST, REFER TO THE DISC NO. 418999

Figure 66. PROM Address PWA

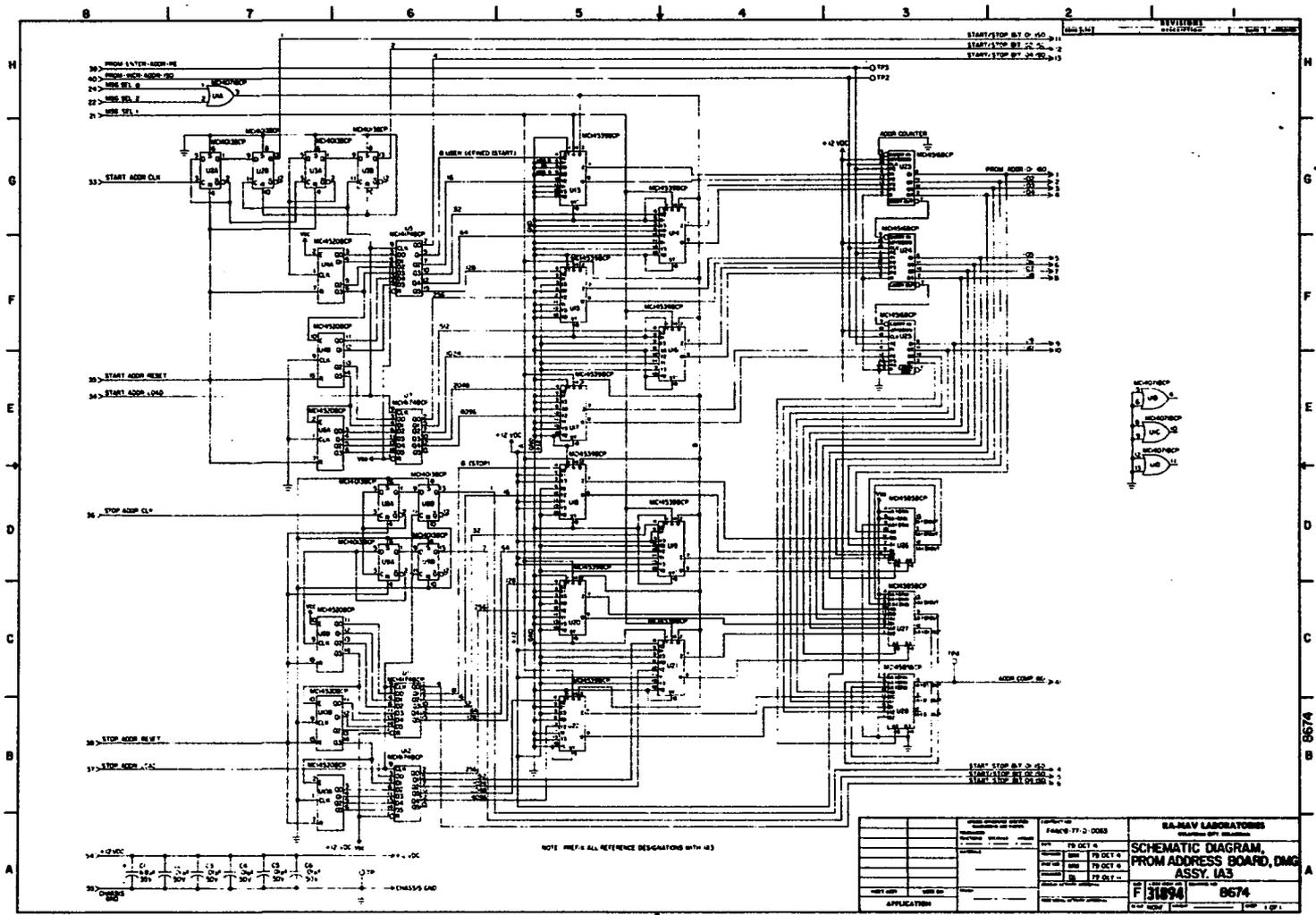
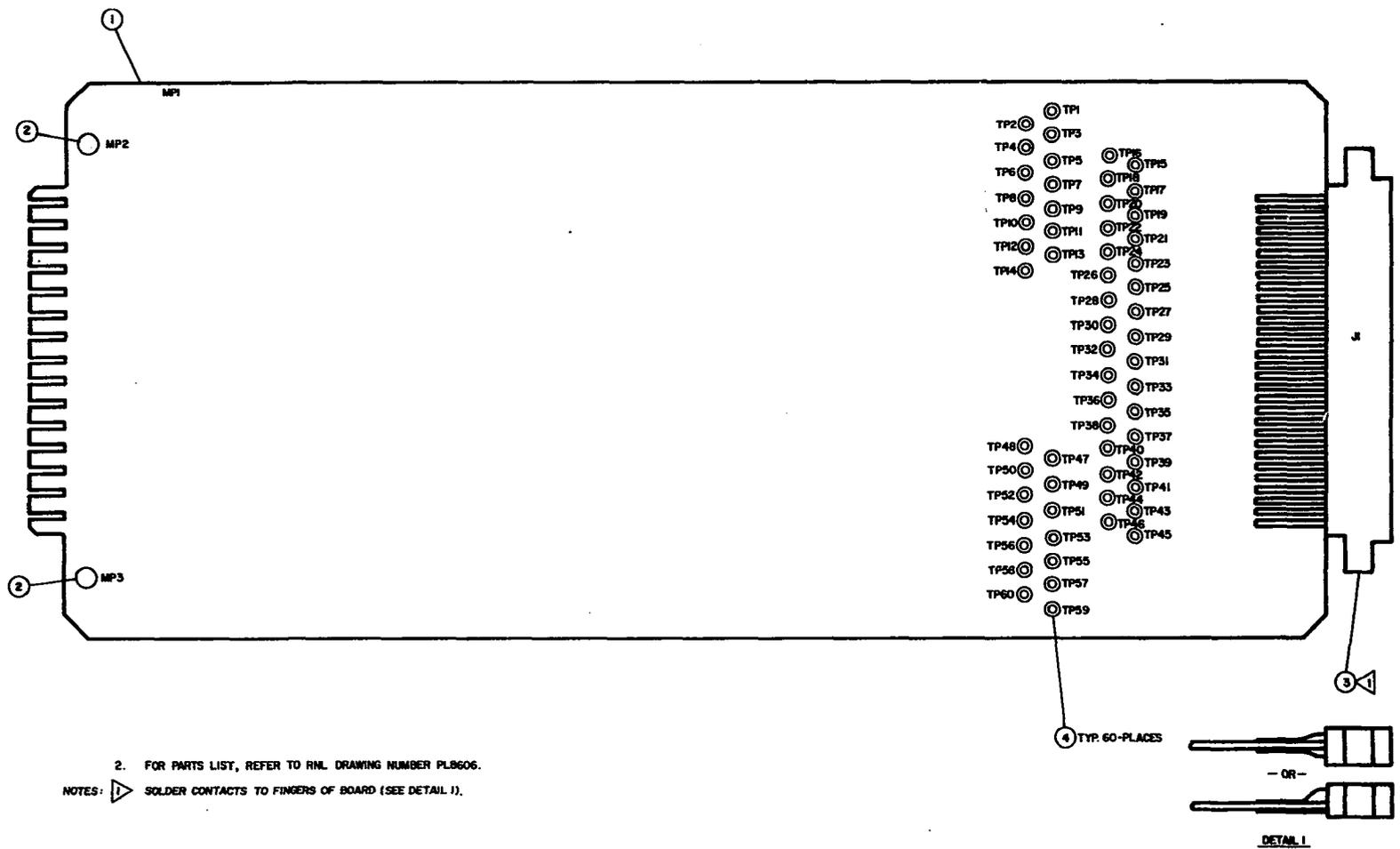


Figure 67. Schematic Diagram for PROM Address PWA



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Figure 68. Extender PWB

The procedure used to check the units is to test the newly constructed DMG first with a GGM-16 data analyzer and then with the GGM-21 data analyzer. Once the tests are satisfactory, the DMG is tested on a previous qualified DSA for final system tests. The DSA goes through the same test procedures. The next tests are the final audit testing. These are performed to a test specification written by Ra-Nav Laboratories. These test specifications are 188 pages long and are composed of three parts. The first part consists of tables of each test with a description of the test and a column to indicate if the test fails. The second part is a detailed description of each test that is to be performed. In the third part every possible measurement is taken to verify the performance of the DDAS. The test procedures begin as basic steps to verify grounds, switches, and output signals. After the inspection test, the detail testing of the functions are performed. Once all the tests are passed, the unit is ready to ship. The test procedures are kept as a record as to how the system performed.

## VI. CONCLUSIONS

At the time this dissertation was written the first ten units had been constructed. The ten DMG units had been tested completely and were ready to be sent to the Army for their acceptance testing. The DSA units had been built, but only one had been completely tested. The plan was to complete the testing of the rest of the DSA units and ship them as soon as possible after the end of the year.

The performance of the system exceeded the requirements of the specifications. During acceptance testing distortion measurements were recorded in the upper range (10,000 baud to 99,990 baud) with less than two percent error while the specifications allowed for five percent error. Another situation in which the system exceeded specifications was when using the messages for bit error measurement. The specifications indicated that this mode of testing would not be held to sync requirements because false syncs could occur; however, during acceptance testing the messages were used for bit error measurement and not one false sync occurred. In fact, the Army engineer spent a whole day trying to get a false sync but was unsuccessful.

During my oral defense a demonstration of a portion

of the system was given which consisted of a DMG connected to an ASR-33 teletype. The demonstration used the stored message in the DMG to show the different modes of operations. Sufficient distortion was added to the data to show that the teletype would print an incorrect character. Another feature demonstrated was the parity control switch on the DMG front panel enabling three tapes of the same message to be punched using different parity (odd, even, and mark).

Adhering to the logic design principles listed in Chapter V helped contribute to a successful design. Race conditions were eliminated by using timing diagrams and carefully checking propagation delays. Another factor which contributed to the elimination of race conditions was the use of the D flip-flop followers which allowed for four states and no glitch pulses.

Another factor which contributed to the success of this system was the use of CMOS for the logic family. The CMOS contributed to the avoidance of noise and also helped to meet the heat requirements. A test was performed to see if a heat problem existed. The ambient temperature was raised to 55° C and the DMG and DSA were run for 24 hours. At the end of 24 hours the covers were removed and all of the components were felt to see if any heat problems existed. None did. The one area where a heat problem was anticipated was in the power supplies; however, that did not occur because the CMOS did not require as much current. In addition

to the lower current requirements, the regulators were heat sunk to the cabinet.

The only disadvantage presented by using CMOS was in the interface with the microprocessor, RAMs, and EPROMs because additional gates were required to interface the +5 volt logic to the +12 volt logic. However, the CMOS more than compensated for these additional logic gates because of the larger scale of integration, ultimately resulting in a significant savings in the total number of gates needed to complete the design. This can be exemplified by the fact that the cabinet for the GGM-21 analyzer is two inches taller than the cabinet for the DSA and has no extra volume left inside. About one fourth of the volume in the DSA cabinet is unused even with the inclusion of the enhancement features and the PROM programmer.

Improvements derived from the mechanical design were as follows: (1) The hinged backpanel allows access to the PWAs for ease of servicing without removing the equipment from the rack. (2) The PWAs are all slotted at a different level so that they cannot be inserted in the wrong slot. (3) The modular design of the switch assemblies allow quick replacement if a problem occurs.

A new feature in the DMG is the UV lamp used for erasing the EPROMs. The UV lamp is next to the PWA rack with an access hole which enables a PWA with an EPROM to be erased when inserted backwards in the spare slot. Because

the three PWAs which have EPROMs (mounted in Textool sockets) are in the same location, any EPROM can be erased without removing it from the PWA.

The problems encountered in building the prototype units were due to the technician misinterpreting the schematics. This problem was solved once the technician was shown how to read the schematics. There were also some errors due to artwork mistakes.

As a follow-up to this design, I did a post design analysis. Often hindsight reveals improved design methods for future projects. While finishing this system I designed a microprocessor controller for a reader sorter at MPI. Using the experience gained from this design and the information obtained from the post design analysis, I was able to complete the new design much quicker and more efficiently than was anticipated. Two examples of direct benefits from the post design analysis were: (1) The use of tristate devices to connect directly to the microprocessor bus, whereas in the DSA PROM programmer extra tristate buffers were used to access the bus. (2) The use of the microprocessor address bus to perform functions based on an upper bit being active. The DSA used a single bit decode of the upper address bits to perform specific logic operations. This idea was extended in the controller design to use a single address bit to select a decoder and the lower address bits to provide the decoding for the logic

operations.

The final conclusion is that of a personal nature. A sense of satisfaction and accomplishment is always derived from a design that works.

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