MOGHADAM, HOSSEIN MOHAMAD

DATA DETECTION IN HIGH DENSITY DIGITAL MAGNETIC RECORDING

The University of Oklahoma PH.D. 1979

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DATA DETECTION IN HIGH DENSITY DIGITAL MAGNETIC RECORDING

A DISSERTATION

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in partial fulfillment of the requirements for the

degree of

DOCTOR OF PHILOSOPHY

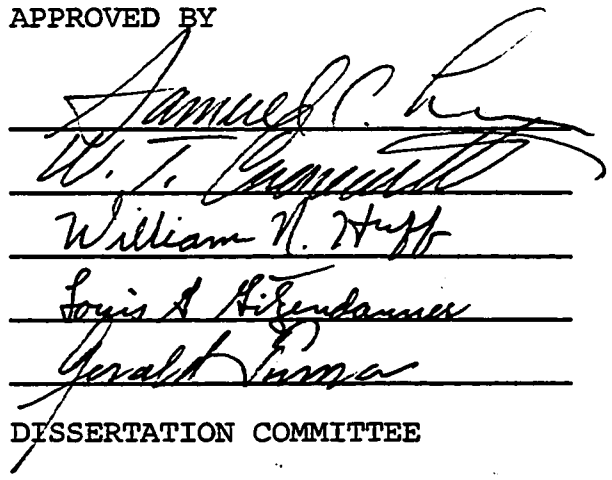
BY

HOSSEIN M. MOGHADAM

DATA DETECTION IN HIGH DENSITY DIGITAL

MAGNETIC RECORDING

APPROVED BY



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ABSTRACT

The specific application which is the subject of discussion and investigation is in the area of digital magnetic recording pertaining to high performance disk memory systems.

At high lineal and areal densities, the choice of read recovery electronics significantly influences error probabilities. In addition, the selection of a specific recording code which is used to achieve high bit densities, further complicates reliable detection.

This dissertation presents the necessary background theory and details the design of a generalized read system which combines several features in order to significantly increase probability of detection. Signal equalization in conjunction with a peak-follower qualifying channel, followed by a phase coherent matched filter are the key elements of the design. Additionally, for future investigation, the concept of a real-time majority decoder,in the block diagram form, is introduced and discussed. This concept, inspired by statistical detection theory, utilizes three differently processed channels resulting in a certain degree of uncorrelatedness among them. The outcome of the three channels are then voted on by a majority decode logic.

DATA DETECTION IN HIGH DENSITY DIGITAL MAGNETIC RECORDING

CHAPTER I

REVIEW OF CURRENT TECHNOLOGY

Introduction

The technique of magnetic recording was invented approximately seventy years ago (5), but only during the last two decades has it become extremely popular in a variety of applications in storage of information in audio, video, and digital recording. There are several reasons for the growing popularity of magnetic recording as an information storage medium. The medium is inexpensive and is available in large quantities. The recording process is relatively simple and is reversible, permitting a given record to be erased and recorded repeatably for an indefinite number of times.

There is a variety of disk memory systems currently being developed and manufactured by numerous computer peripherals manufacturers in the United States as well as other countries. These memories fall under two major categories - The "flexible" disk memory, and the "rigid"

disk memory. The flexible disk memory employs, as a recording medium, a pliable disk of approximately five inches or eight inches in diameter made of a material similar to the magnetic tape and operates within a protective paper sleeve. The flexible disk memories have historically been of significantly smaller size, lower cost, and reduced performance as compared to their rigid media counterparts.

The rigid disk memory, which is generally used as a random access memory, employs one or more structually rigid disk(s) of, most commonly, fourteen inches in diameter. The disks are enclosed in either a sealed or a filtered shroud, and rotate at speeds of 1500 RPM for the lower performance to 3600 RPM for the high performance units. Historically, the rigid disk memories have been technologically more advanced than the flexible disk memories in various areas in order to store and retrieve large quantities of digital information in a minimum amount of time. The more important of these areas which impact the internal design are in the specifics of disk and transducer (head) technologies, the track and flux densities, recording code, read signal processing, positioning servo, and the air filtration system. Some of the other design parameters which are user visible are in the number of disks, captive or operator removable storage capacity, average latency, average position time, total number of tracks, number of records per track, and data transfer rate.

The Recording Medium

In digital recording applications where high signal-to-noise ratio (S/N) and high signal resolution are highly desirable, only two types of media are currently being used; particulate dispersions, and thin metallic film commonly known as thin film or plated media. The thin film media usually employ the Fe-Co-Ni alloy in a thin (0.1 to 0.3μm) electroplate with a controlled coercivity of up to 800 oe. Due to high coercivity, the resultant signal level is higher as compared to that of the particulate dispersion media. The resultant S/N, however, suffers due to the magnetostatic coupling of the individual alloy grains resulting in a relatively high medium background noise.

The magnetic medium currently being used in the majority of disk memory systems is a particulate coating of from 0.6 to 3μm thick γ-Fe_2O_3[1] deposited on an aluminum substrate of 1.2 to 1.95mm thickness. In addition to the requirements of high remanent magnetization and high coercivity, the magnetic grains must be sufficiently small to form a tightly packed and homogenous dispersion of oriented particles. The surface finish is carefully controlled to an RMS surface roughness of typically within 0.2μm, necessitated by the close proximity requirement of medium to head interface.

---

[1] γ-Fe_2O_3 is a ferromagnetic meta stable phase of α-Fe_2O_3 with saturation magnetization ($4\pi M_s$)=4000 Gauss.

The Recording Transducer

Recording and retrieval (Write and Read) of information is accomplished by use of a transducer commonly referred to as the magnetic recording head. Although separate write and read transducers may be used in a variety of applications, in the case of disk memories however, the same transducer is generally used to accomplish both functions. Some low to medium performance memories use heads with an additional "erase" function.

The choice of design parameters of a head are influenced by factors such as maximum recording frequency, write and overwrite current requirements, read back signal amplitude, self resonance, signal spectral definition, in addition to aerodynamic and mechanical requirements. Two types of magnetic materials are most commonly used in fabrication of the head: Nickel-Zinc, and Manganese-Zinc ferrite; the latter results in somewhat higher signal amplitude and improved high frequency characteristics. The digital recording process currently being used in disk memories is saturation type recording which requires sufficiently high induced field in the recording head. This requirement may potentially result in pole tip saturation precluding optimum geometry designs for narrower track widths. This deficiency has lead to the development of the thin film head. The thin film head may be batch fabricated by electroplating, vacuum evaporation, or photolithographic methods.

Although single and multi turn thin film heads have been under investigations for several years, their appearance on the commercial scene has not as yet materialized.

Commonly Used Data Detection Techniques

The choice of detection technique depends on readback signal amplitude and resolution, flux density, recording code, and transfer rate. Signal resolution may be defined as,

$$\text{Signal Resolution}\Big|_{\text{(Single Frequency)}} = \frac{\text{Highest Frequency Voltage}}{\text{Lowest Frequency Voltage}}$$

In order to determine signal amplitude and resolution, a set of saturation curves are constructed by plotting the normalized head output voltage as a function of write current magnitude for each of several recording densities. The optimum operating point for each recording density is then determined by conducting "over-write" tests in order to minimize the residual low frequency content after it has been overwritten by the high frequency data. It is generally necessary to achieve a residual magnitude of -26db or less in order to preserve the spectral definition of the readback signal. A second curve is constructed by plotting the normalized head output voltage as a function of recording density, at a particular value of write current chosen from the first set of curves; this curve is referred to as the flux density curve. The flux density curve, which is

subdivided into four operating regions, as suggested by Graham (7), is used to determine signal resolution, amplitude, and operating region. This information in addition to the characteristics of the specific magnetic code, will help in deciding which method of signal detection should be used. Typical saturation and flux density curves are depicted in figures 1.1 and 1.2 respectively.

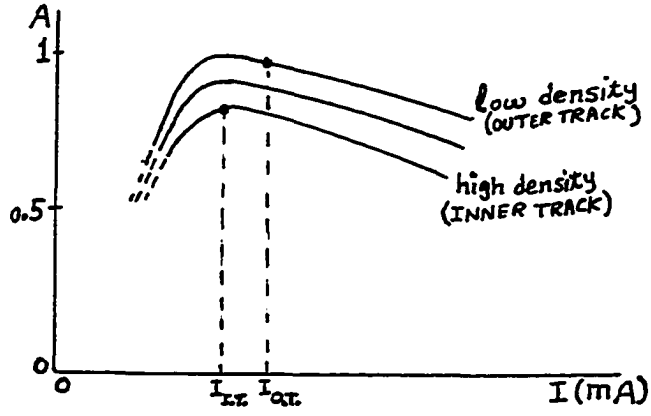


Figure 1.1 Saturation Curves for Various Densities

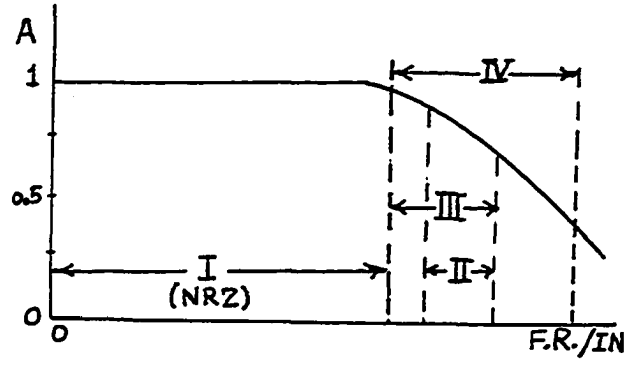


Figure 1.2 Flux Density Curve

The study of magnetic codes, a review of which is given in appendix A, is a complex and separate subject and will only be discussed to the extent necessary.

The more modern detection techniques employ Phase-Locked-Loops (PLL) in conjunction with single channel zero crossing or peak detection for region II, and an additional threshold qualifying channel for region III operation. In figures 1.3 and 1.4 a typical region II (35 - 140Kbits $/cm^2$) detector block diagram and its corresponding timing diagram are presented. The specific magnetic recording code used is the "Double Frequency" (DF) code which is generally used in low-to-medium performance disk memories. A brief description of the operation with reference to designated points on the block and the timing diagrams follows.

Signal A is an idealized encoded current waveform switched in the head during write operation. During the read operation, the mmf signal generated by the head is preamplified, filtered and its gain is dynamically adjusted with respect to a constant reference voltage. The resultant signal B, is then differentiated in order to produce signal C whose zero crossings correspond to the peaks of signal B. Signal D, a digitized signal, is subsequently converted to pulse-per-transition signal E and used as reference input to the PLL.

After sufficient synchronization time (10 to 50 micro-seconds), the Voltage Controlled Oscillator (VCO)

Signal F, through appropriate divide-by-N counter, provides reference detection clock signal G. Signal G in conjunction with pulse date signal E are used to generate the "detected" signal H. The "detected" or "recovered" signal H is then logically decoded from the DF coded sequence to produce the "Non Return to Zero" (NRZ) data J which is sent to the disk controller along with the "Read Clock" I.

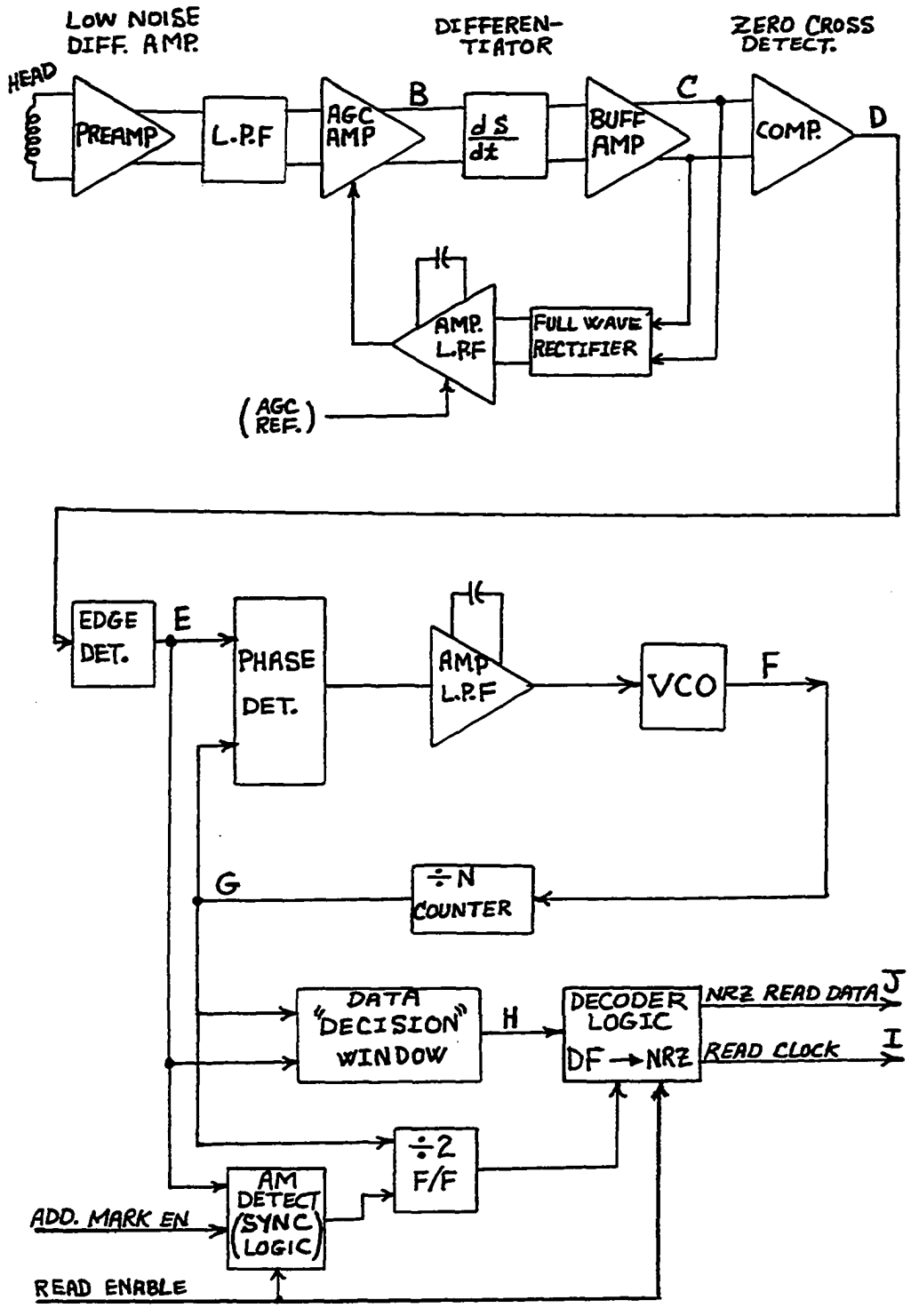


Figure 1.3 Typical Region II Detector

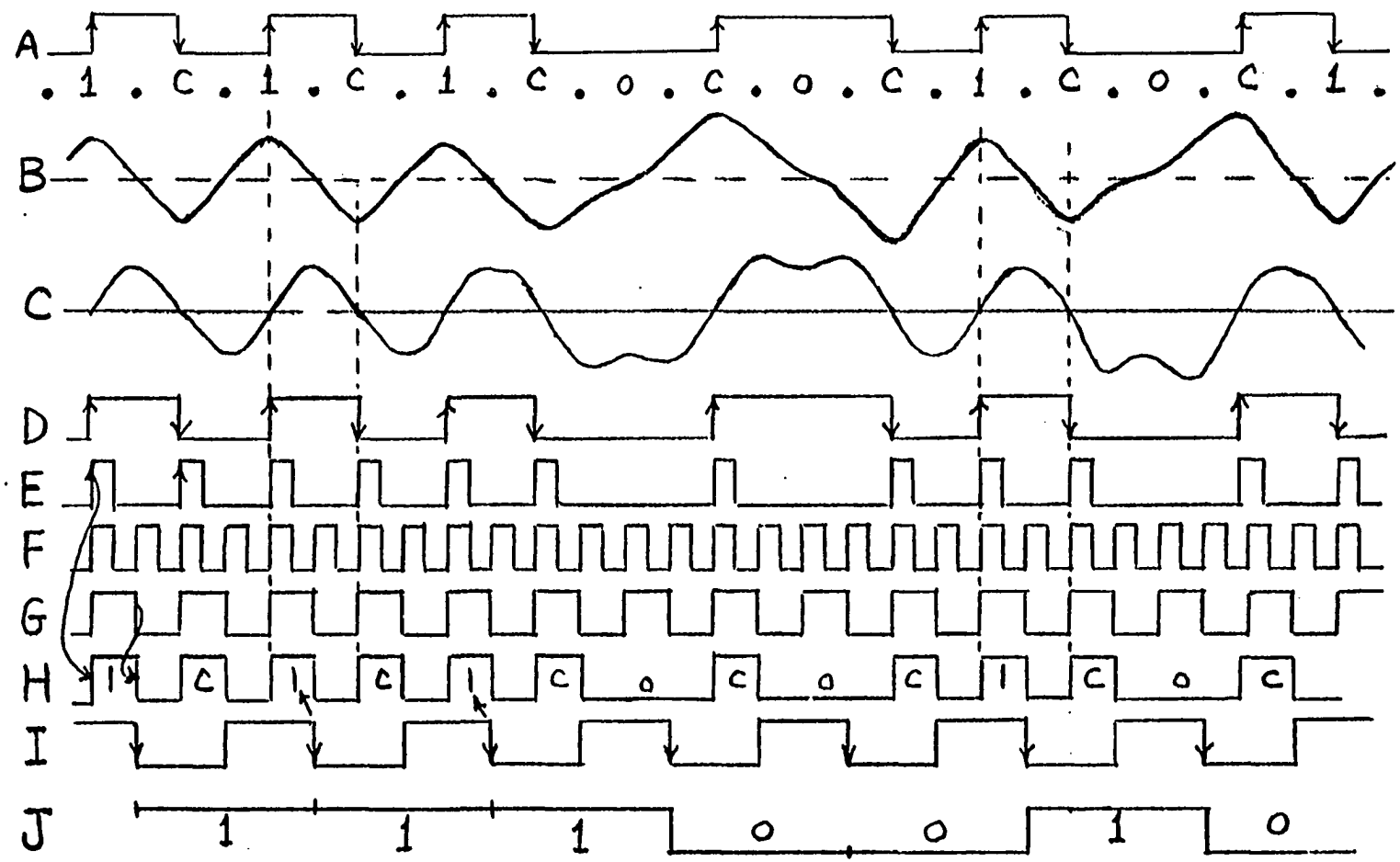


Figure 1.4 Timing Diagram for Region II Detector

The most recent high performance systems, which have the capability of storing from 300 to 500 K bits/cm^2, employ head and medium of higher performance and operate in region III of the flux density curve. The Modified Frequency Modulation (MFM) code is most often employed in this region in order to increase the data density by a factor of two over that of DF code. The flux density is also increased to the allowable limit of the recording channel. In order to achieve reliable operation at these densities, significant improvements have been achieved not only in the head and medium characteristics, but also in the design of the electronics. A typical detector capable of region III operation is depicted in figure 1.5 with the corresponding signal timing shown in figure 1.6. In this system the write data is usually precompensated using one of several different techniques available. The write pre-compensation is accomplished by purposely inducing a small amount of displacement in time to specific transitions in the direction opposite to the shift expected in the read mode. A brief description of the detector's operation with references to figures 1.5 and 1.6 follows.

A high resolution channel which is designed to enhance phase linearity in the passband and beyond, often produces undesirable extraneous crossings (signals C and D) for data sequences which have wide separation between flux transitions. A qualifying channel (signals E and F) with a

narrower band low-pass filter is employed in order to gate out the unwanted transitions. Signal D is appropriately delayed with respect to signal F and used as the timing reference in the qualifier logic to produce signals G and H. The leading transitions of signals G and H are used by the pulse-former logic which produces signal I. Signal I is then used as reference to the PLL which produces the phase coherent signal J necessary to produce the recovered signal K and the decoded signal M.

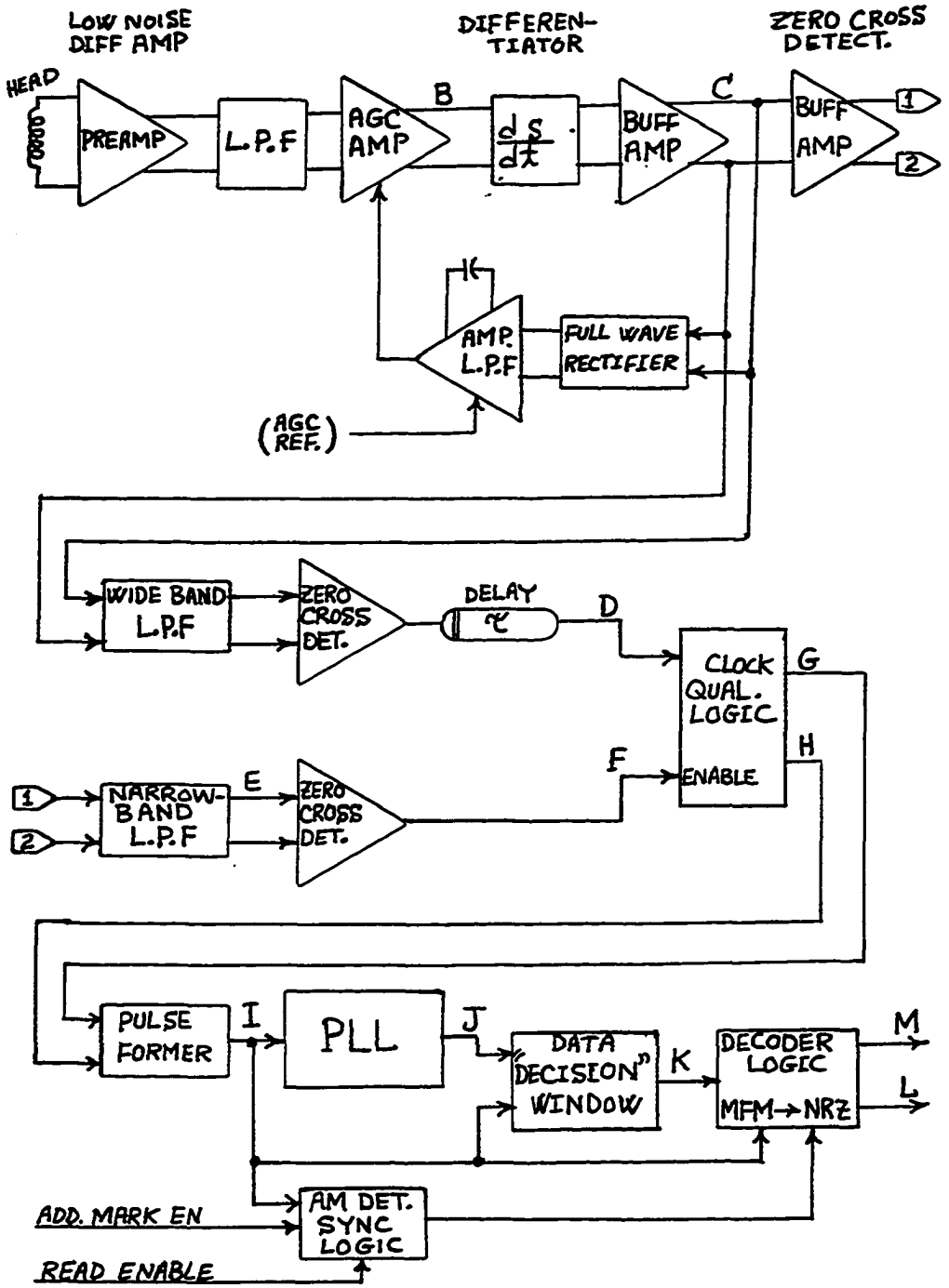


Figure 1.5 Typical Region III Detector

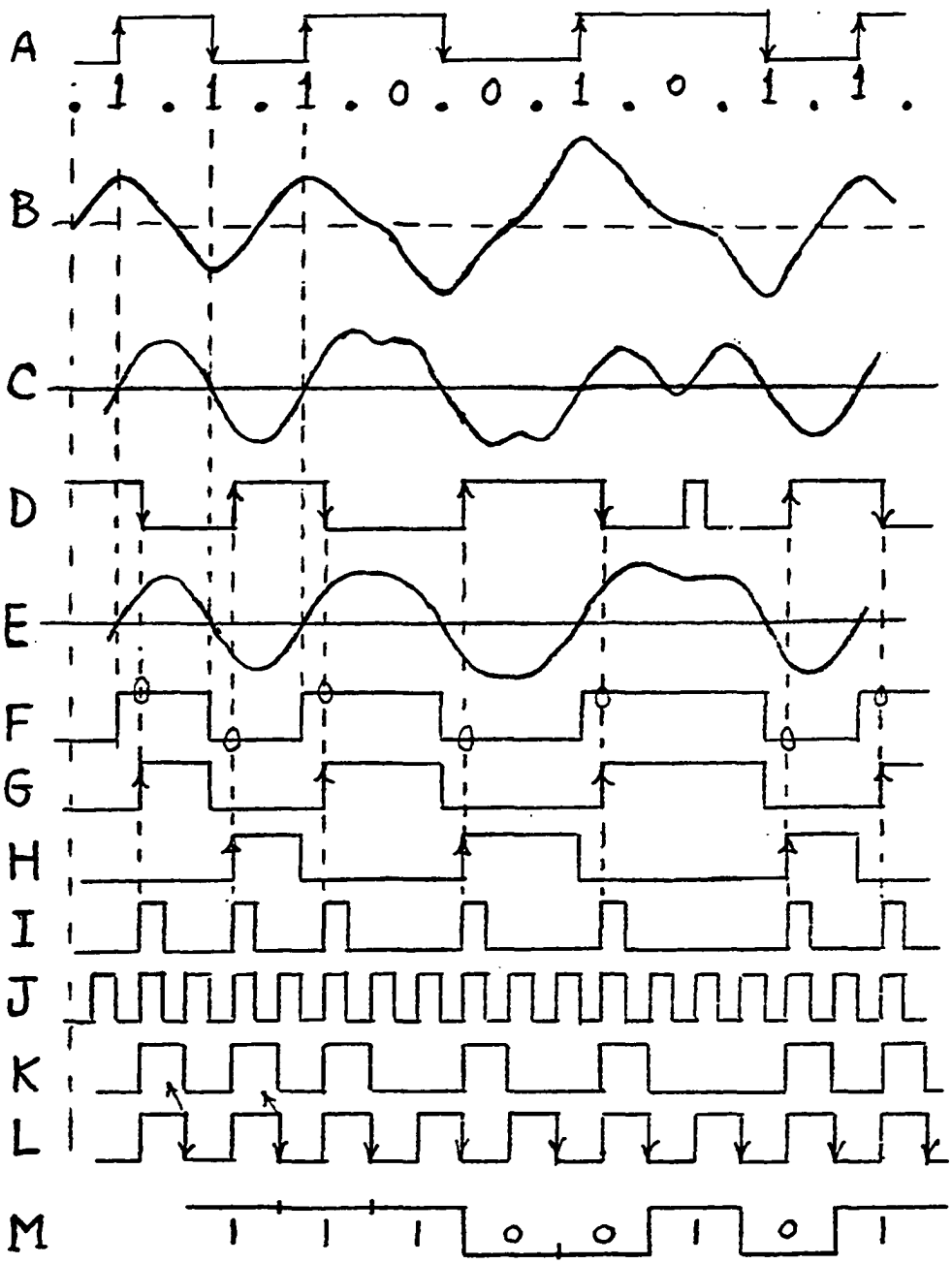


Figure 1.6 Timing Diagram for Region III Detector

CHAPTER II

BACKGROUND THEORY

Introduction

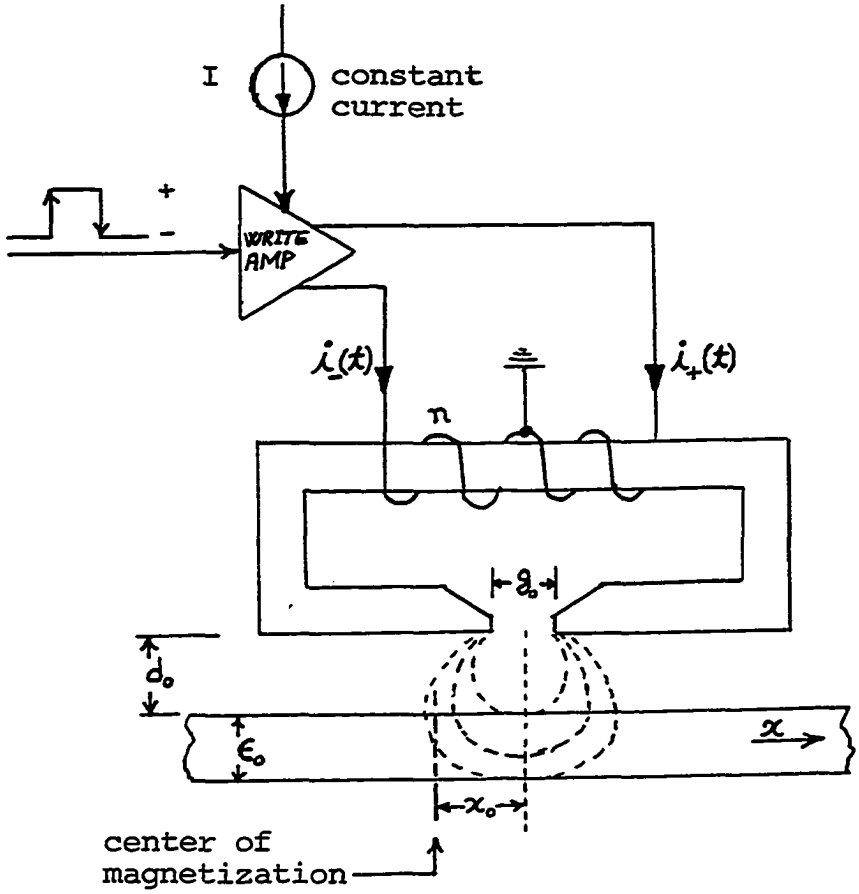
In this chapter the theory of recording and reproduction processes necessary to arrive at a better understanding of the required signal processing elements are first presented. The recording process, the magnetization transition, and the effect of self demagnetization are briefly discussed, and then the reproduction process, the "isolated pulse", and the concept of intersymbol interference are given. Specific examples of waveform simulations using linear superposition and harmonic series expansion lead the way in defining the necessary signal processing elements. Subsequently the signal processing elements such as the Cosine Equalizer, the Integrate and Dump matched filter, and the Peak-Follower autocorrelator are presented as the basic design elements used in the succeeding chapters.

The Recording Process and the Magnetic Transition

During the write process, the head is driven by a magnetomotive force proportional to ni ampere-turns which sets up leakage flux in the vicinity of the air gap penetrating the magnetizable layer of the medium. The model of the recording process is depicted in figure 2.1.

A narrow and definite transition region is highly desirable and requires a magnetizable medium with square hysteresis loop in addition to a sharp transition gradient at the trailing side of the head induced magnetic field. The widening of the transition region, as discussed by Sebestyen (23), is primarily attributed to the insufficient field penetrating the moving medium in the region just outside the saturation boundary of the head field. This process is referred to as the self demagnetization caused by the mmf generated by the medium, changing the permeance coefficient and hence the operating point on the hysteresis loop. The self demagnetization is proportional to length-to-diameter ratio of the magnetized region, and is thought to be one of the factors limiting the recording density.

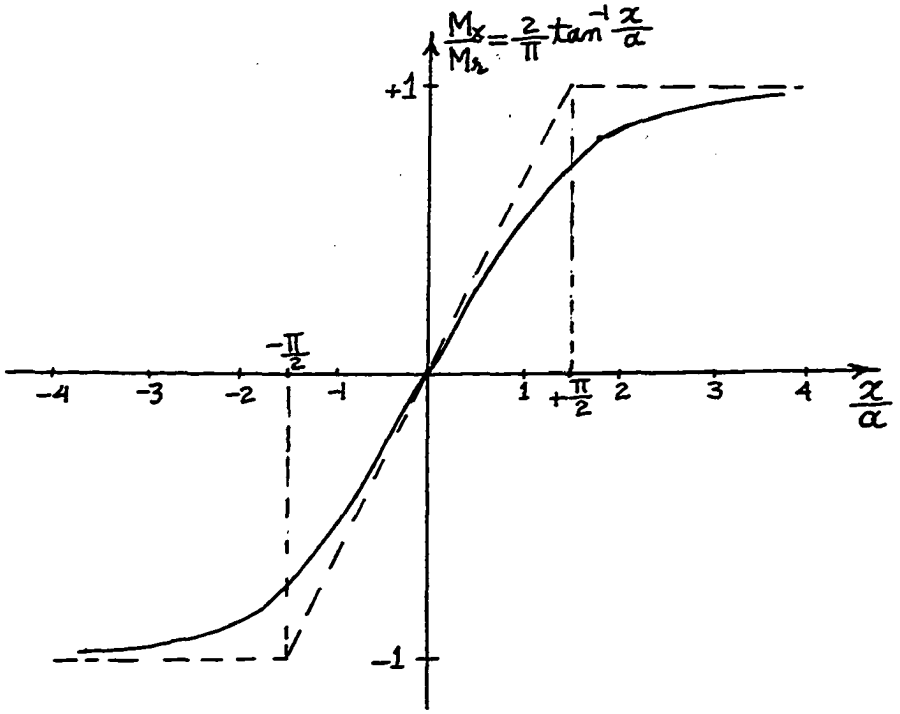
Due to head inductance and amplifier response limitations, the write transition is not instantaneous, and to a degree also influences the magnetic transition region.



ϵ_o =medium thickness
d_o =head to medium separation
g_o =head air gap
x =position of the medium
v =velocity of the medium
x_o =½ of magnetic transition region
n =head coil number of turns
$i_+(t)$ =positive transition current
$i_-(t)$ =negative transition current

Figure 2.1 Model of the Recording Process

The arctangent model of the magnetic transition depicted in figure 2.2 has been suggested by Speliotis - Morrison (31) and Middleton (35), and has been shown to be in close agreement with experimental data.



M_r: remanent magnetic moment per unit volume
M_x: longitudinal component of magnetization
a : magnetization parameter controlling sharpness of the transition

Figure 2.2 Arctangent Transition Model

Assuming only longitudinal magnetization, the effective demagnitizing has been shown (31) to be:

$$H_d = \frac{H_c}{M_r} = \frac{2}{\ell_o}\left[\epsilon_o \cdot \log\frac{D^2+\epsilon_o^2/4}{C^2+\epsilon_o^2/4} + 4\left(D\cdot\tan^{-1}\frac{\epsilon_o}{2D} - C\cdot\tan^{-1}\frac{\epsilon_o}{2C}\right)\right] \quad (2\text{-}1)$$

where: ℓ_o = written transition region

$C = x - \ell_o/2$

$D = x + \ell_o/2$

H_c = medium coercivity

An important parameter a, which controls the sharpness of the transition region, has been approximated (21, 23, 31, 32) and is given by:

$$a = b + \left[b^2 + \frac{\pi\cdot\epsilon_o\cdot B_r\cdot b}{2H_c}\right]^{\frac{1}{2}} \quad (2\text{-}2)$$

where: $b = \frac{2}{\pi}\left(1 - \frac{B_r}{B_m}\right)\cdot\left(d_o + \frac{\epsilon_o}{2}\right)$

B_r = residual induction

B_m = saturation induction

Equations (2-1) and (2-2) are plotted in figures 2.3 and 2.4 for two values of ℓ_o (50 μIN. and 100 μIN.), and two values of ϵ_o (30 μIN. and 50 μIN.). These values correspond to a typical high density particulate medium rotating at 3600 RPM resulting in inner and outer radii linear velocities of 1600 inches per second and 2400 inches per second respectively. It should be noted that, as the medium thickness ϵ_o is decreased, the surface demagnetization be-

comes the primary factor influencing the reproduce signal amplitude, hence limiting the recording density.

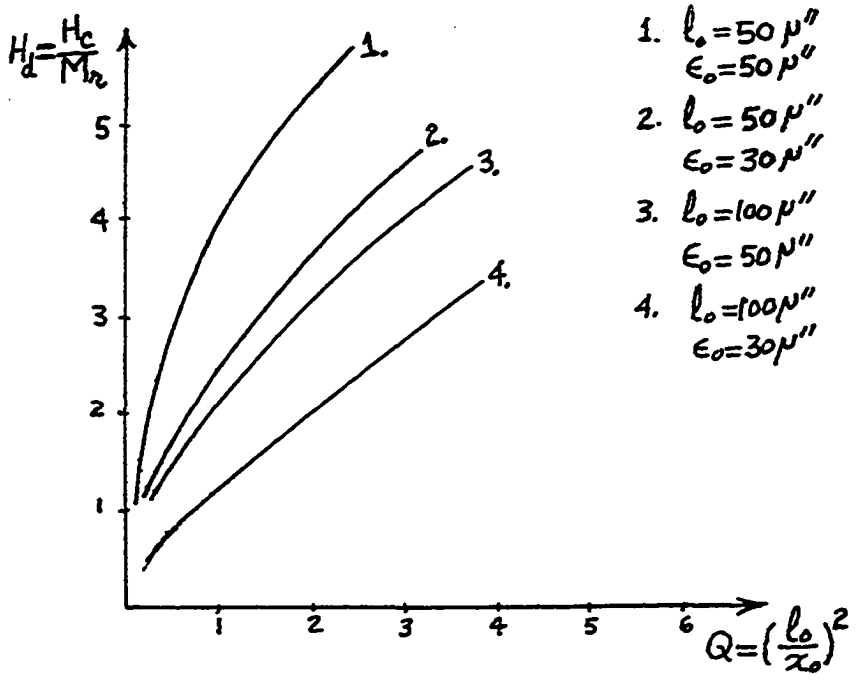


Figure 2.3 Demagnetization Fields for Various Medium Thicknesses and Speeds

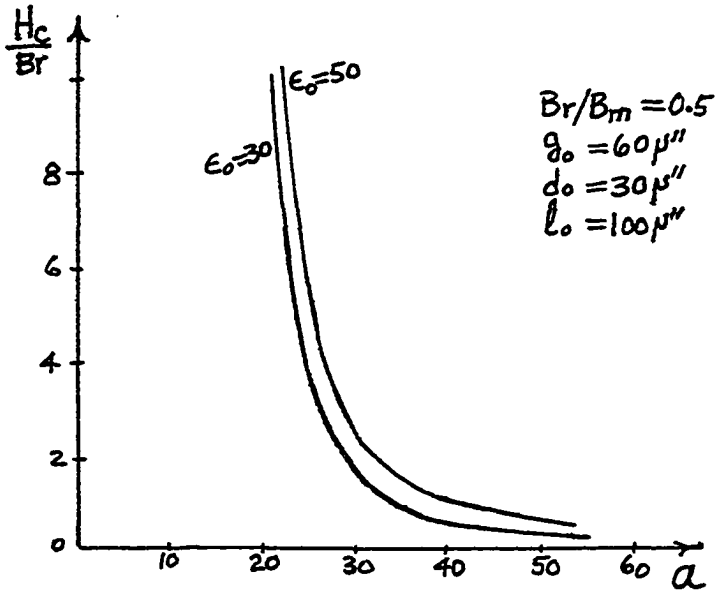


Figure 2.4 Transition Parameter a , as a Function of Medium Characteristics

The Reproduction Process and the Isolated Pulse

By passing the recording medium close to the head, an emf voltage at the terminals of the head is generated. This emf, which is expressed by equation (2-3), is proportional to the velocity of the medium and the rate of change of flux entering the high permeability head core material.

$$e = -n\frac{d\phi}{dt} = -nv\frac{d\phi}{dx} \qquad (2\text{-}3)$$

The isolated pulse response for the general case of finite gap length g_o, and an arctangent transition model has been derived (31) and may be approximated (21, 23) as

$$e(x) \simeq \frac{k}{g_o}\left(\tan^{-1}\frac{x+g_o}{a+d_o} - \tan^{-1}\frac{x-g_o}{a+d_o}\right) \qquad (2\text{-}4)$$

where: k = constant = $k_o \cdot (4vWM_r n \epsilon_o n_k)$

W = effective head core width

n_k = head core efficiency

k_o = numerical constant

The corresponding peak value of the isolated reproduce voltage occurs for $x=0$, and is given by

$$e_o = 2\frac{k}{g_o}\tan^{-1}\frac{g_o}{a+d_o} \qquad (2\text{-}5)$$

In figure 2.5, the normalized isolated pulse is plotted as a

function of x for specific values of d_o, g_o, and several values of the transition parameter a.

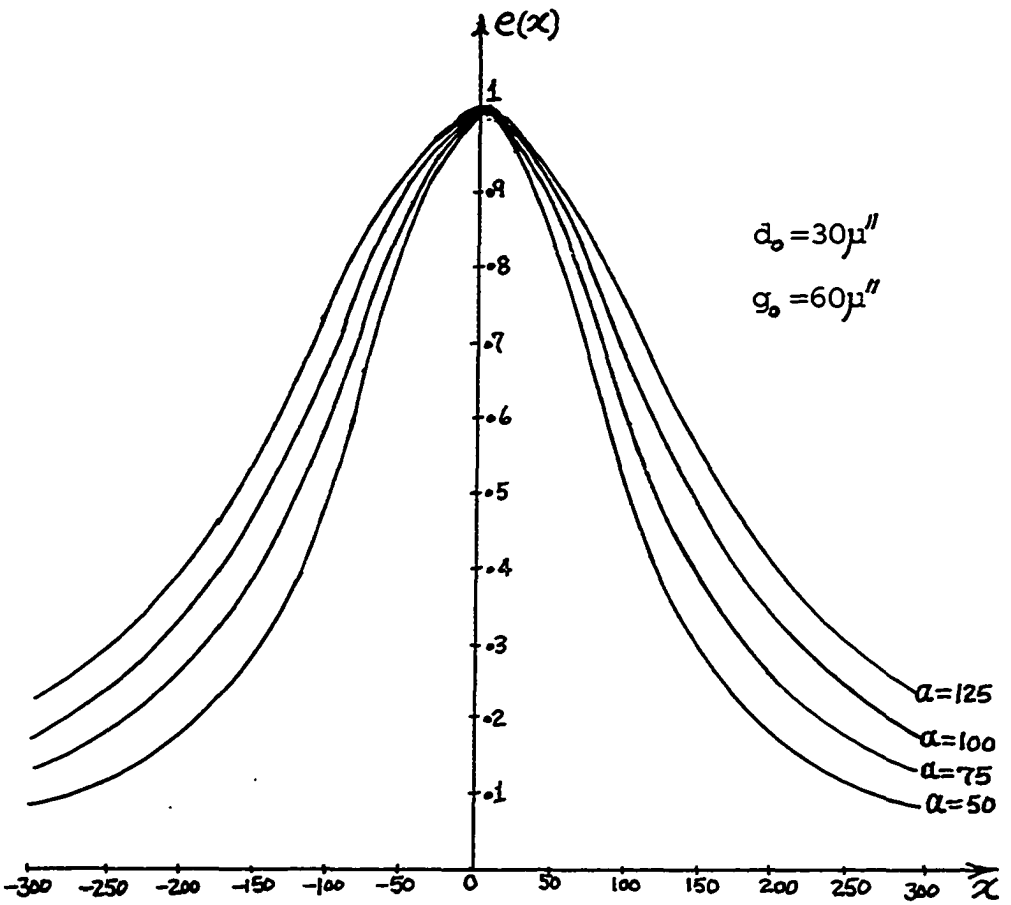


Figure 2.5 Normalized Isolated Pulse for Different values of a

Intersymbol Interference and Peak Shift

The half amplitude pulse width of equation (2-4) is of particular importance in determining composite signal characteristics. It is convenient to have an expression which describes the isolated pulse as a function of time t, given only the half amplitude pulse width PW_{50}. A good approximation to the Speliotis-Morrison equation (31) has been derived as a function of PW_{50} by Popa (33) and is given by

$$e(t) = G\left(\frac{1}{1+(Kt)^2}\right) \qquad (2\text{-}6)$$

where: $K = 2/PW_{50}$

G = gain constant

A preferred expression useful for spectral definition and channel frequency response determination, is the Fourier series expansion of equation (2-6) which may be represented as

$$e(t) = \frac{2\pi}{KT}\sum_{n=1}^{\infty} e^{\frac{-2\pi N}{KT}} \cdot \cos\left(\frac{2\pi N}{T}\right)t \qquad (2\text{-}7)$$

where: $K = 2/PW_{50}$

N = harmonic count

T = waveform period

The normalized spectrum of the isolated pulse as a function of frequency ω is plotted in figure 2.6 and the detailed results are tabulated in table 2.1.

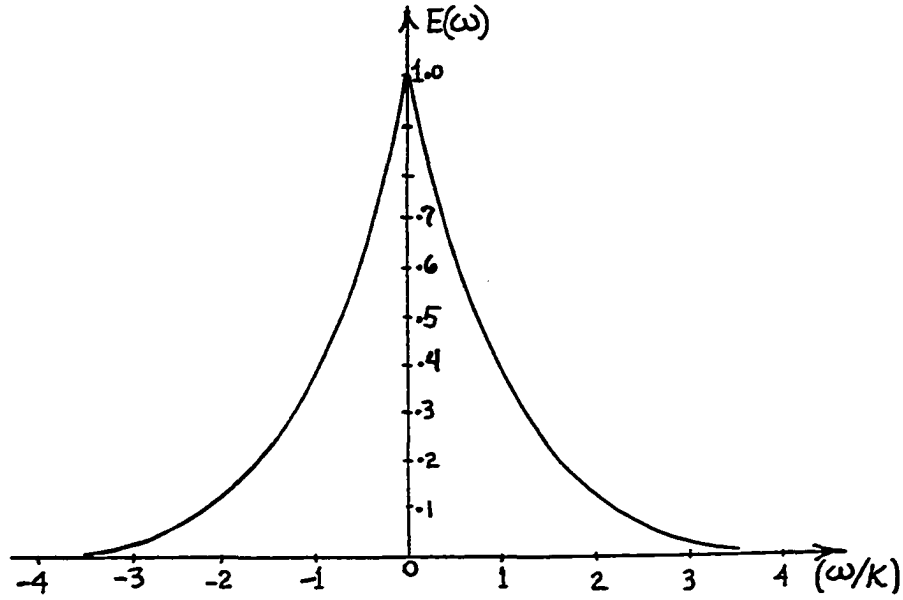


Figure 2.6 Normalized Frequency Spectrum of the Isolated Pulse

ω/K	E(ω)	ω/K	E(ω)
0.0	1.0	2.2	0.111
0.1	0.905	2.4	0.091
0.2	0.819	2.6	0.074
0.4	0.67	2.8	0.061
0.6	0.549	3.0	0.05
0.8	0.449	3.2	0.041
1.0	0.368	3.4	0.033
1.2	0.302	3.5	0.03
1.4	0.247	3.6	0.027
1.6	0.202	3.8	0.022
1.8	0.165	4.0	0.018
2.0	0.135	4.6	0.01

Table 2.1 Data Points for the Spectrum of the Isolated Pulse

The spectrum is useful in determining the channel bandwidth necessary for a certain degree of reconstruction accuracy. For example, for an isolated pulse width of 100×10^{-9} seconds, a bandwidth of approximately 10mHz provides a 95% reconstruction accuracy.

The simulation of the periodic equation (2-7) requires an upper limit for the harmonic count N. The upper limit for N also defines the simulated reconstruction accuracy, and is a function of the half amplitude pulse width PW_{50} and the waveform period T. The relationship between the frequency spectrum and the harmonic count may be expressed as

$$N = \frac{(\omega/K) \cdot T}{\pi \cdot PW_{50}} \qquad (2\text{-}8)$$

The reconstruction accuracy as a function of N, PW_{50}, and T for four different cases is plotted in figure 2.7.

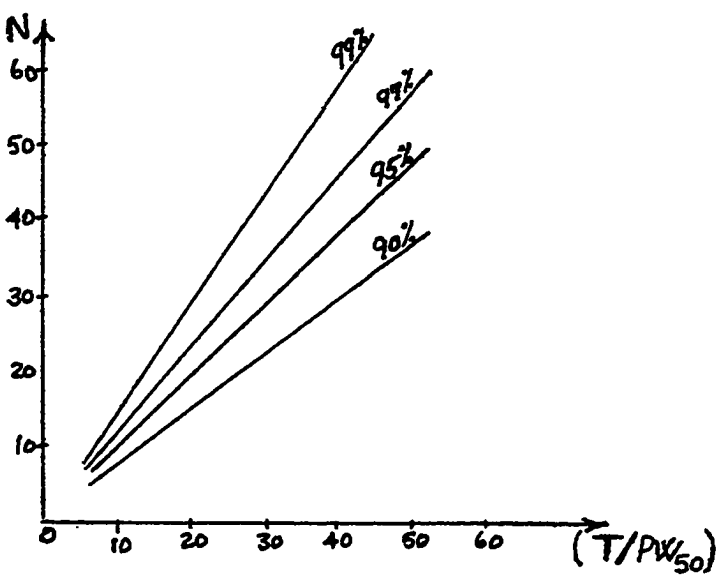


Figure 2.7 Waveform Reconstruction Accuracy

Equation (2-7) may be modified to describe a periodic waveform containing two or more pulses seperated by $T_1, \ldots, T_m$. Such a general expression which makes use of linear superposition of the individual reproduce pulses is represented by equation (2-9).

$$e(t) = \frac{P}{K} \sum_{N=1}^{U} e^{\frac{-NP}{K}} \cdot \left[\cos PNt \mp \cos PN(t-T_1) \right.$$

$$\left. \pm \cos PN(t-T_2) \mp, \ldots, \pm \cos PN(t-T_m) \right] \qquad (2\text{-}9)$$

where: $P = 2\pi/T$

U = upper limit of harmonic count

The case of two superimposed pulses positioned closely, demonstrates the principle of intersymbol interference (23), as in figure 2.8.

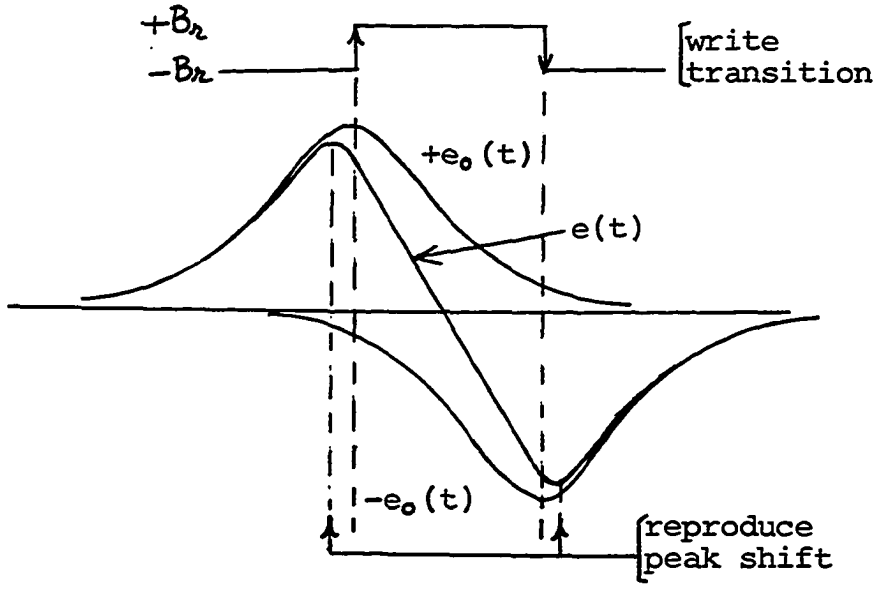
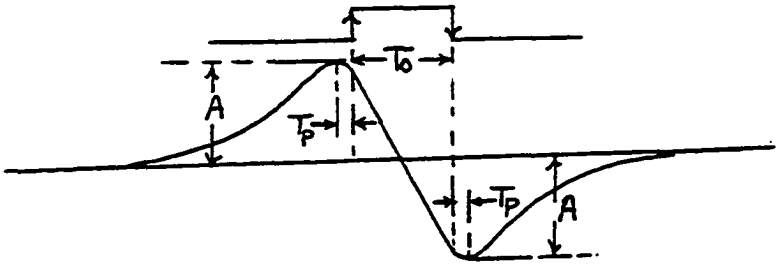
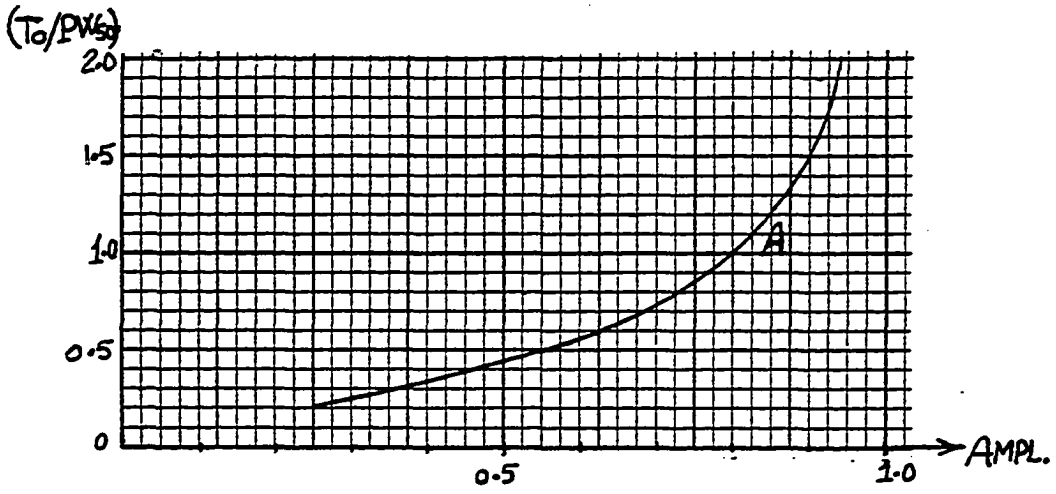


Figure 2.8 The Linear Superposition and Intersymbol Interference

In general, the intersymbol interference results in a reduction in pulse amplitude, a shift in the peak position, and for complex waveforms a low frequency baseline shift of an aperiodic nature.

The relationship between the half amplitude pulse width PW_{50} vs. peak shift and amplitude reduction for the cases of two (dibits) and three (tribits) closely positioned, but otherwise isolated, pulses have been simulated. The results are depicted in figures 2.9 and 2.10 and the computer program and data given in appendix B.





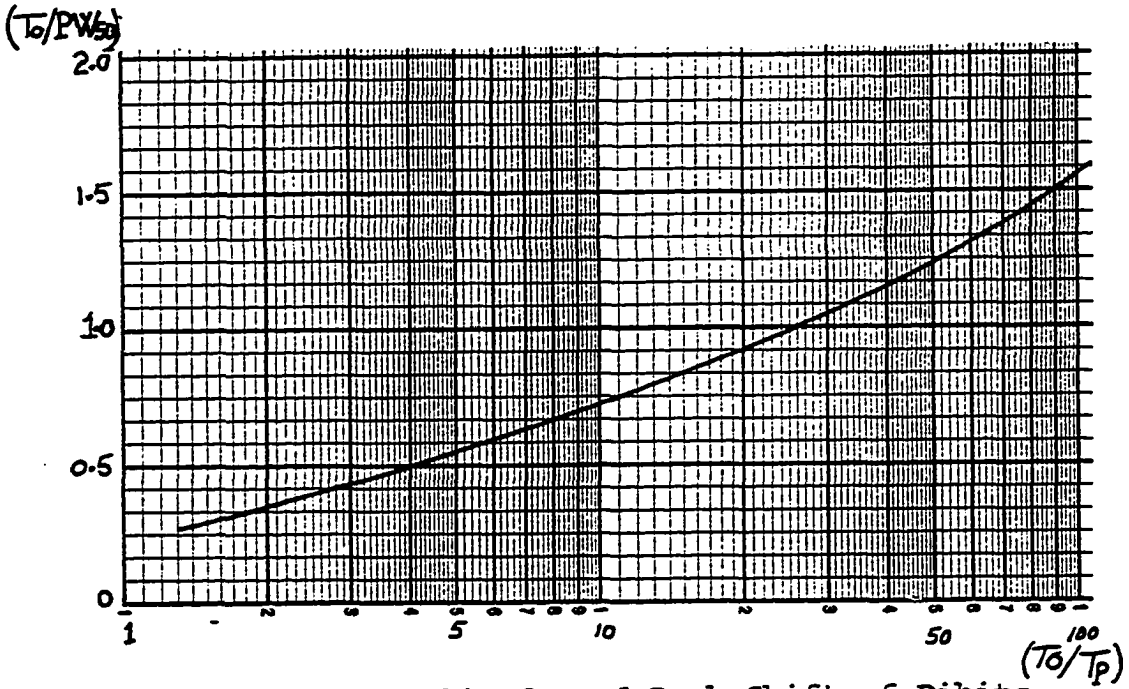
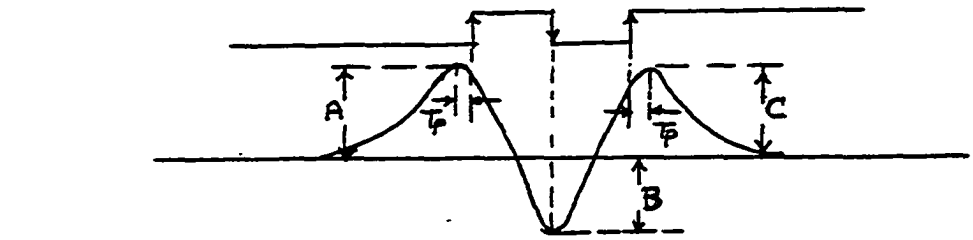
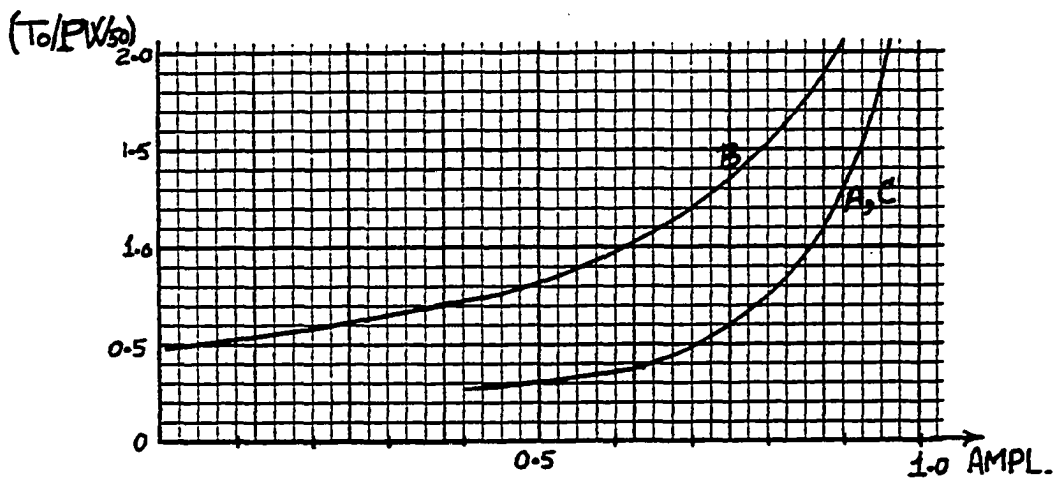


Figure 2.9 Amplitude and Peak Shift of Dibits





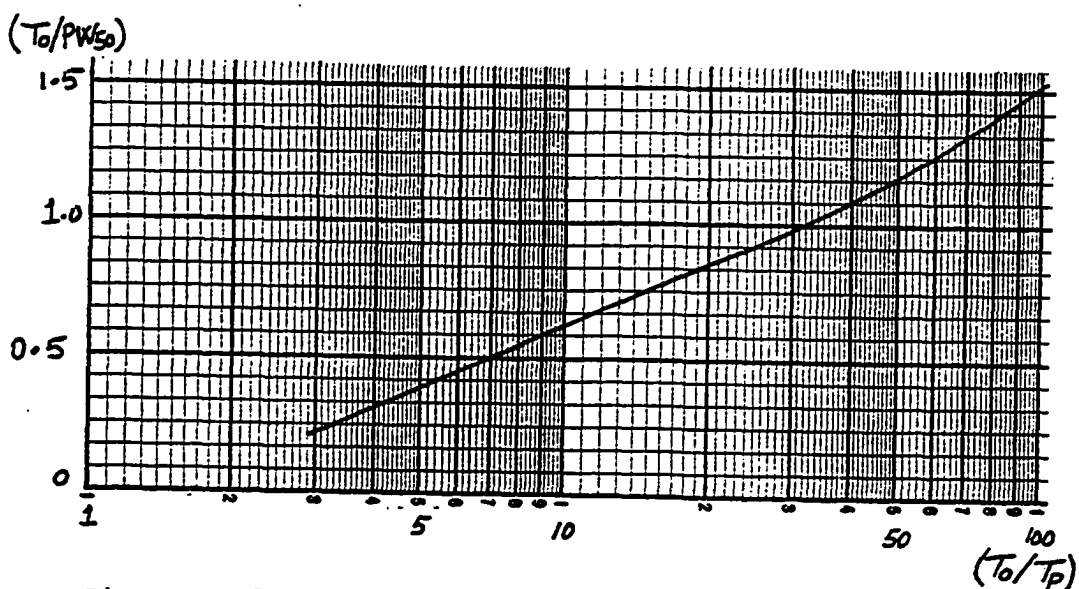


Figure 2.10 Amplitude and Peak Shift of Tribits

The linear superposition may again be used on the composite waveform in order to sense the peak positions through conversion of peaks to zero crossings. A realization of this principle employing a delay line of delay τ and a differential amplifier or a high gain comparator is shown in figure 2.11.

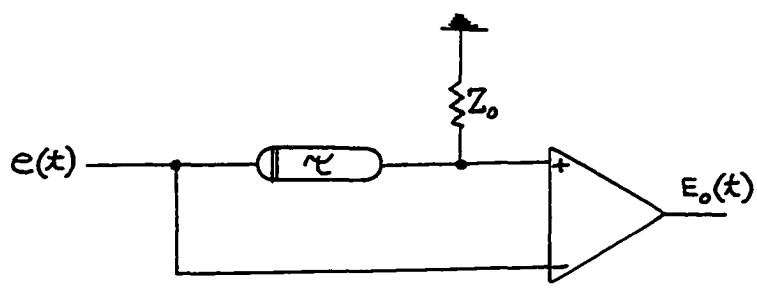


Figure 2.11 Realization of a Delay Line Differentiator

For a wide bandwidth delay line, the resultant output $E_o(t)$ is linear phase with respect to e(t), with a constant zero crossing delay of $T_o = \frac{1}{2}\tau$. For a unity gain differential amplifier, the amplitude of $E_o(t)$ as a function of the amplitude of e(t) and its period T, may be expressed as

$$A_{E_o(t)} = 2A_{e(t)} \ \mathrm{SIN}(\pi\tau/T)$$

The choice of τ is a compromise between signal amplitude and equalization of amplitudes of $E_o(t)$ for various frequencies of e(t).

An arbitrary MFM sequence of the reproduce waveform was simulated by programming equation (2-9) on a digital computer for values of $PW_{50} = 200\times10^{-9}$ seconds and $PW_{50} = 100\times10^{-9}$ seconds. For each case, both the peak waveform e(t) and the differentiated waveform $E_o(t)$ were calculated. The results of the simulation are plotted in figures 2.12 and 2.13, and the computer program and data are given in appendix C. As expected, for the case of $PW_{50} = 200\times10^{-9}$ seconds, a larger degree of intersymbol interference results in noticeable peak shift and amplitude variations of e(t).

The simulation results strongly suggest that irrespective of the system noise, the pulse crowding caused by by the finite width of the isolated pulse limits the channel bandwidth and hence the recording density.

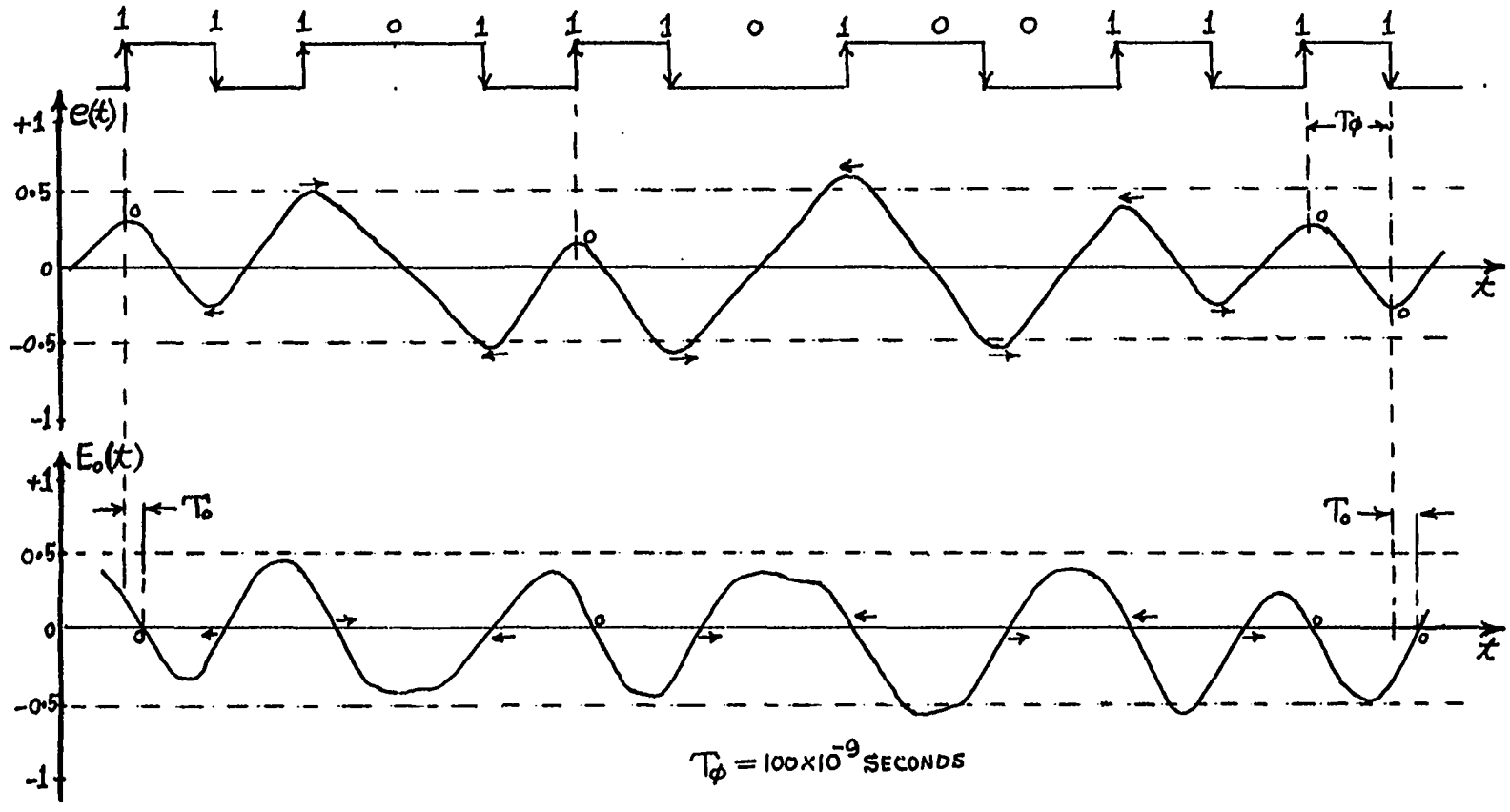


Figure 2.12 Simulated MFM Waveform for $PW_{50}=200 \times 10^{-9}$ Seconds

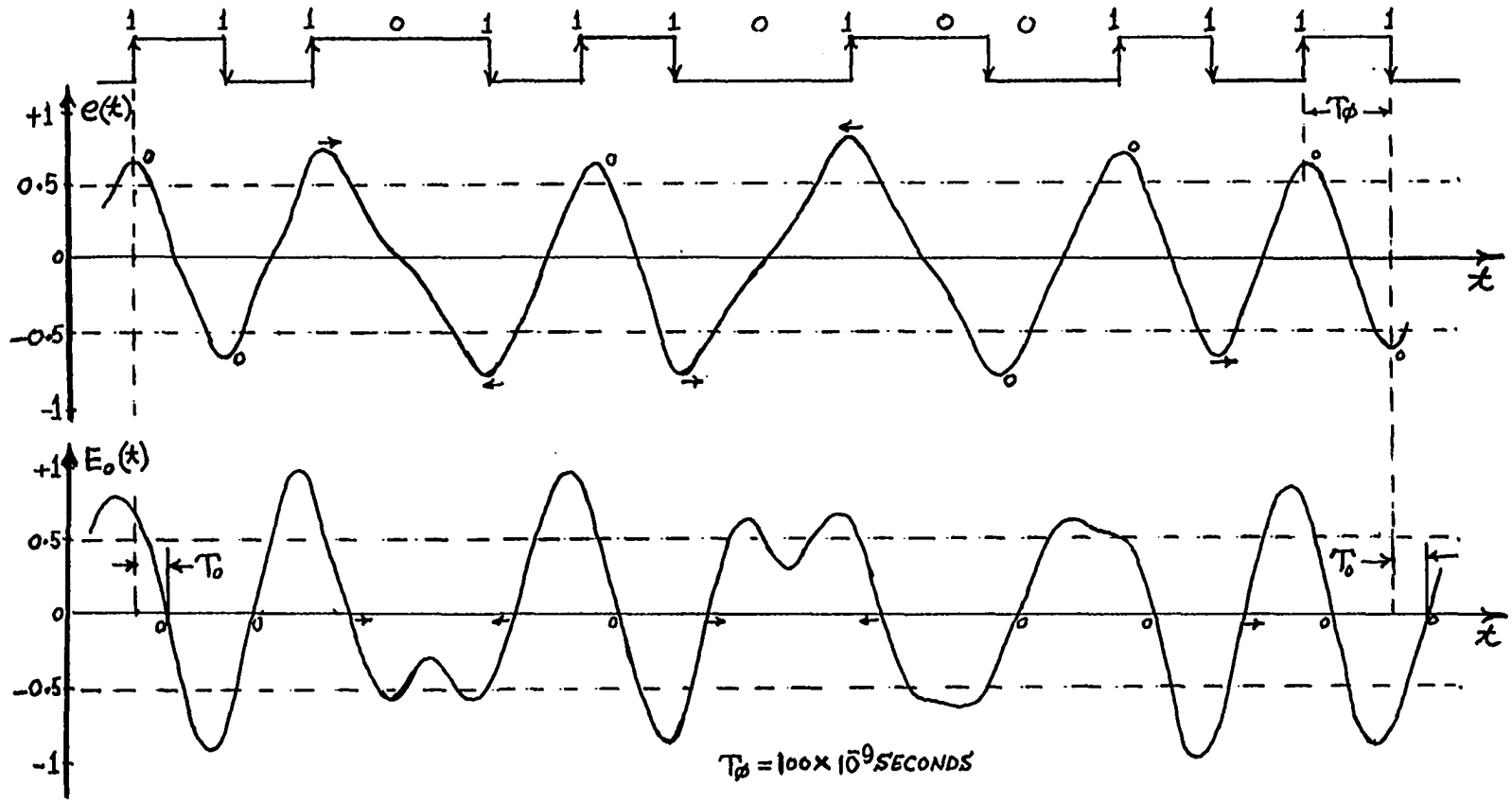


Figure 2.13 Simulated MFM Waveform for $PW_{50}=100x10^{-9}$ Seconds

Signal Equalization

For many years signal equalization techniques have been employed in a variety of applications in order to enhance signal definition and spectral purity.

Magnetic recording systems have been the more recent candidates for employing several methods of signal equalization. These methods have varied from passive filter realizations such as the Gaussian response filters, the bridged-T networks, and the phase equalizer (8,9), to the more effective transversal filter and the cosine equalizer (12,13,16, 17,20).

Waveform equalization by means of a transversal filter or a cosine equalizer may be inplemented in order to minimize peak shift, equalize amplitudes, and restore baseline. A realization of such an equalizer employing two delay lines and a differential amplifier is depicted in figure 2.14 with the corresponding signals given in figure 2.15.

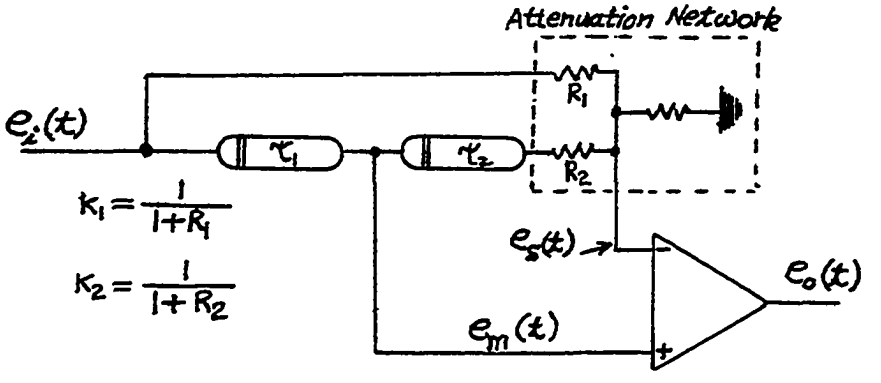


Figure 2.14 Realization of the Cosine Equalizer

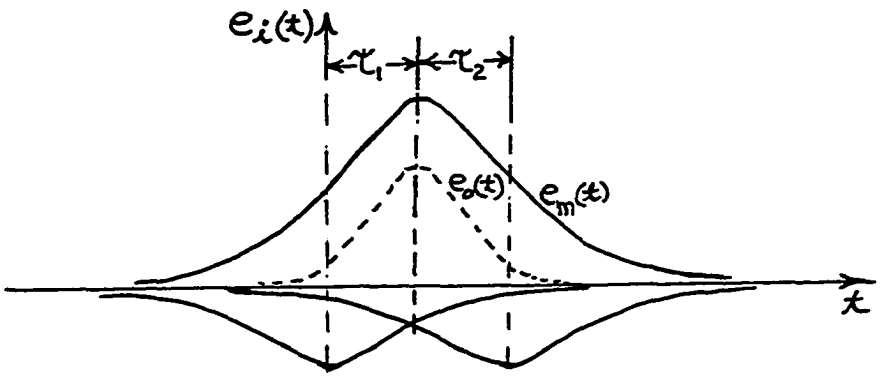


Figure 2.15 Typical Equalizer Waveform

The output waveform $e_o(t)$ in terms of the input waveform $e_i(t)$, the delays τ_1 and τ_2 and the attenuation factors K_1 and K_2 may be expressed as

$$e_o(t) = e_m(t) - e_s(t)$$
$$= e_i(t+\tau_1) - K_1 e_i(t) - K_2 e_i(t+\tau_1+\tau_2) \qquad (2\text{-}10)$$

In general, the two delay lines and the attenuation networks may be of unequal values in order to compensate for an asymmetry in the input waveform $e_i(t)$. The optimum values for the delays and the attenuation values are selected in order to provide minimum resultant pulse width with no appreciable undershoot, and an acceptable resultant signal amplitude. For a symmetrical input waveform $e_i(t)$, typical values of $K_1=K_2=0.35$ and $\tau_1=\tau_2=0.35(PW_{50})$ result in approximately 40 percent reduction in pulse width, with a corresponding amp-

litude reduction of approximately 5db. The reduction in pulse width minimizes the intersymbol interference, allowing an increase in the recording density. The amount by which the recording density may be increased however, is proportional to the reduction in pulse width only for sufficiently high S/N of input signal $e_i(t)$.

Waveforms of figures 2.9 and 2.10 have been simulated incorporating signal equalization of parameters K=0.35 and τ=0.35(PW_{50}). The results along with previous data, for ease of comparisons, have been plotted in figure 2.16. The computer program and data are given in appendix D. By examining figure 2.16 it is quite evident that significant restoration in peak positions and amplitudes have been achieved. It should be noted that the dibit of figure 2.9 is a good "worst case" peak shift simulation waveform, while the tribit of figure 2.10 accentuates the reduction in pulse amplitude.

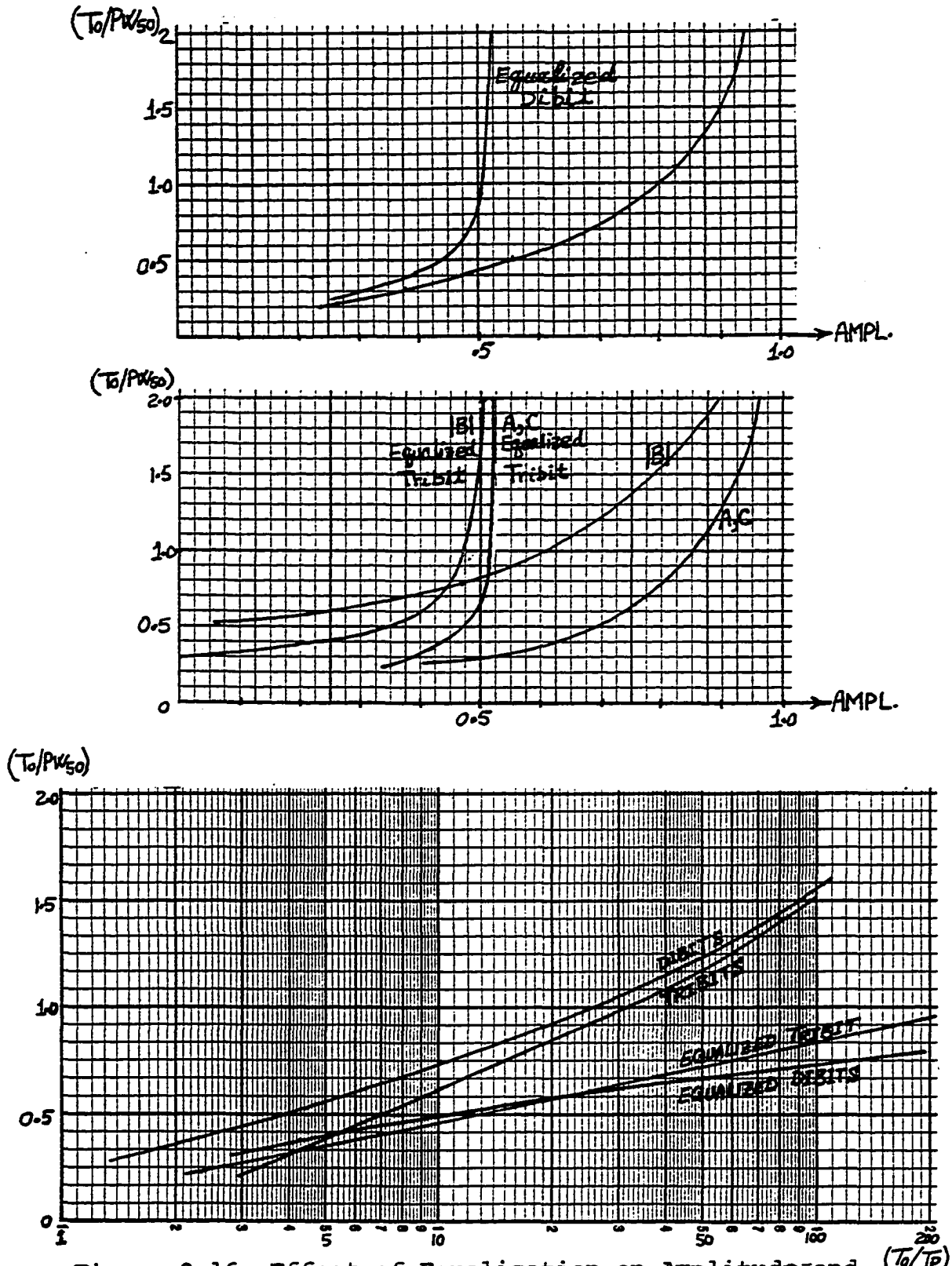


Figure 2.16 Effect of Equalization on Amplitude and Peak Shift of Dibits and Tribits

Significant improvements in amplitude equalization and peak shift reduction are possible by applying one or more levels of equalization at the expense of reduction in S/N. Generally, the equalization leads to an increase in the detection window, some of which may be allocated to counteract the increase in the predominantly random noise, resulting in a net gain. Another important benefit resulting from signal equalization is the decreased sensitivity to parameter variations in the head and the medium.

Integrate and Dump Matched Filter

The class of communication theory applicable to saturated magnetic recording is Digital Communications, involving specifically the detection of binary signals of known phase. From coherent detection theory, an optimum realizable detector is the correlation detector (2) which may be represented by

$$\int_0^{T_b} r(t)\left[s_1(t)-s_0(t)\right]dt \gtrless \frac{E_1-E_0}{2} + \frac{N_0}{2}\ln\left(\frac{\alpha}{\beta}\right) \qquad (2\text{-}11)$$

In equation (2-11), r(t) is the received signal corrupted by noise, E_1 and E_0 are the energies corresponding to the two possible signals $s_1(t)$ and $s_0(t)$, $N_0/2$ is the power density spectrum of the white noise, and α, β are the source probabilities. Equation (2-11) is schematically represented in figure 2.17. Assuming the received signal r(t) is of finite duration $0<t\leq T_b$, the above correlation detector may

be replaced by a linear filter having a unit impulse response that is "matched" to the transmitted signal such that $h_i(t)=s_i(T_b-t)$ $i=0,1$

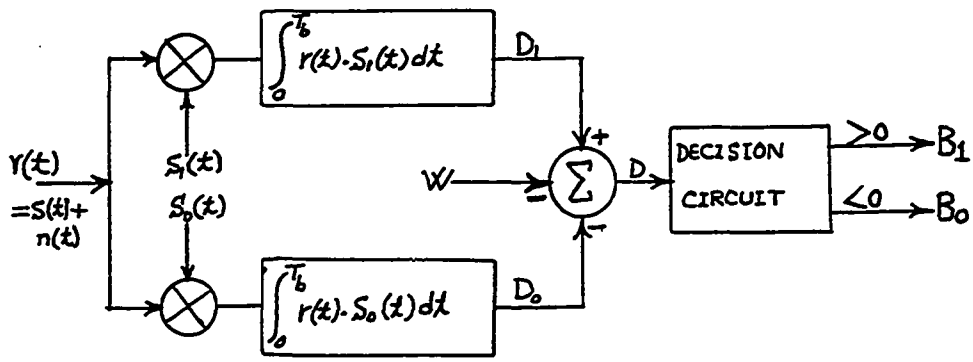


Figure 2.17 Schematic of the "Matched" Filter

A practical realization of the matched filter is the "Integrate and Dump" (I&D) filter which is represented by figure 2.18.

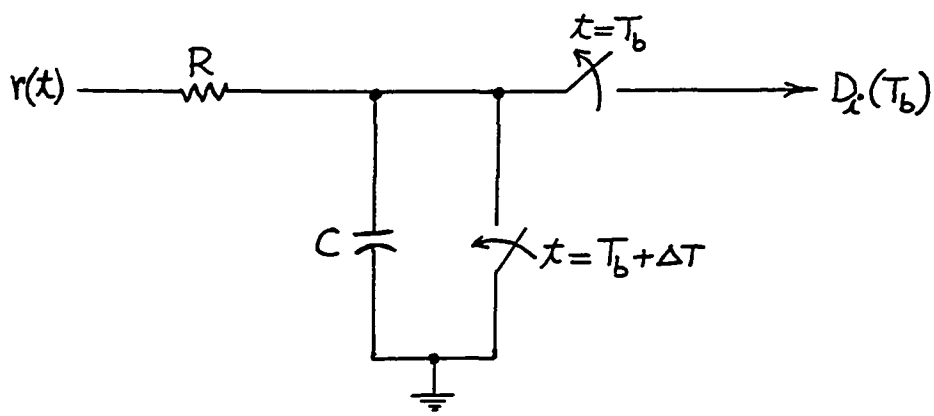


Figure 2.18 Realization of the I&D Filter

A more descriptive implementation represented by the block diagram of figure 2.19 and the associated timing diagram of figure 2.20, demonstrates the noise rejection capability of the I & D filter.

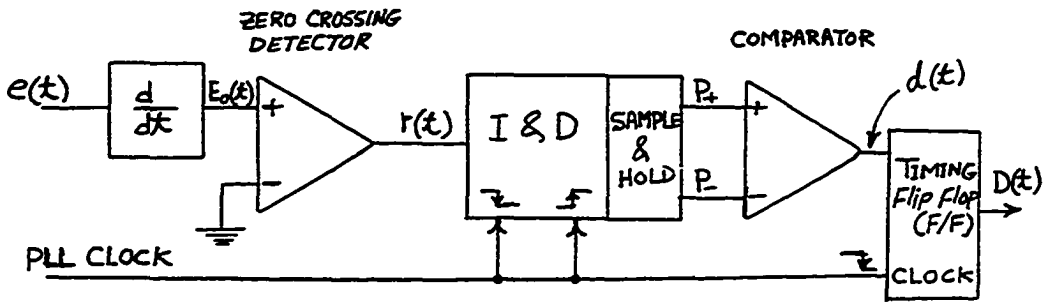


Figure 2.19 Block Diagram of the I&D Filter

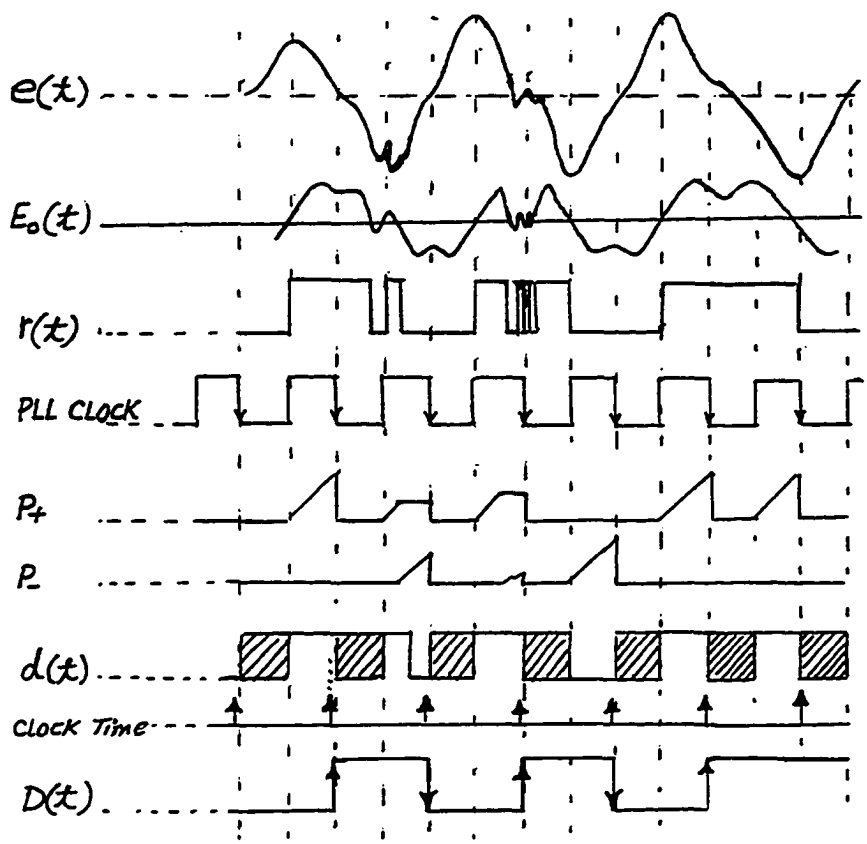


Figure 2.20 Timing Diagram of the I&D Filter

The signal e(t) corrupted by noise results in multiple zero crossings of $E_o(t)$ which in turn corrupt r(t) with unwanted spikes. The signal r(t) is then integrated over the interval 0 to T_b and the result is sampled in a bistable at the end of the integration time, to produce noise-free signal D(t).

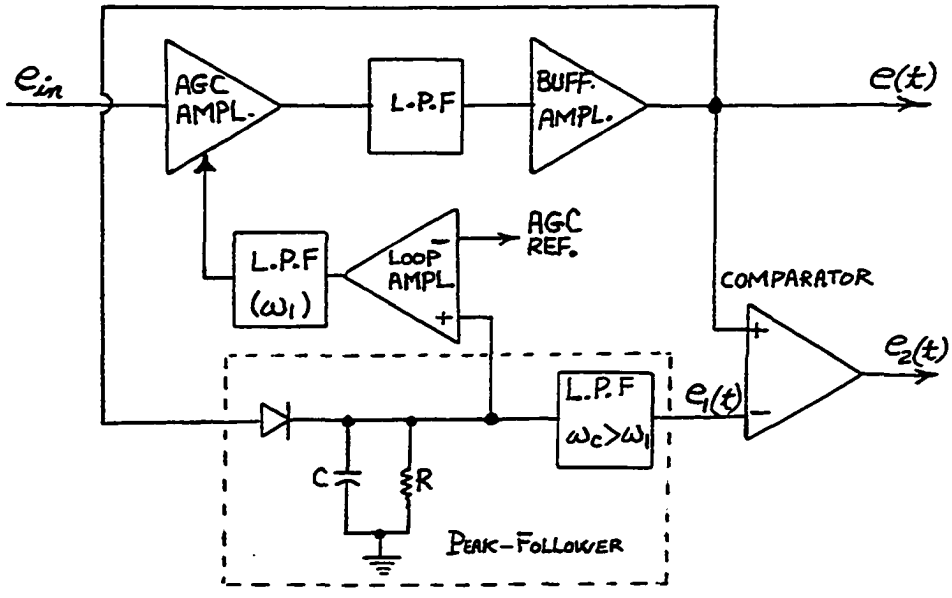
In designing high speed I & D circuits, extreme care in selecting matched circuit pairs, controlling "feedthrough" of the sampling clock, and minimizing effects of "dump time" are necessary in order to realize full advantage of the filter.

Peak-Follower Autocorrelator

Due to signal amplitude variations caused by parameter variations in heads, media and the different recording radii, an automatic gain control (AGC) circuit is desirable, and is generally used in the read electronics. The bandwidth of the AGC is carefully selected to accomodate steady state gain acquisition within a specified time. It is necessary to limit the AGC bandwidth in order to minimize harmonic distortion caused by feedback modulation. This constraint on the AGC limits its ability to follow relatively high frequency envelope modulations caused by imperfect overwrite, media defect, and runout due to media eccentricity.

The peak-follower autocorrelator complements the AGC

by providing a higher bandwidth feedforward envelope detection which is used as the reference threshold for the undifferentiated signal e(t). The realization of the peak-follower is similar to that of envelope demodulator and is depicted in figure 2.21



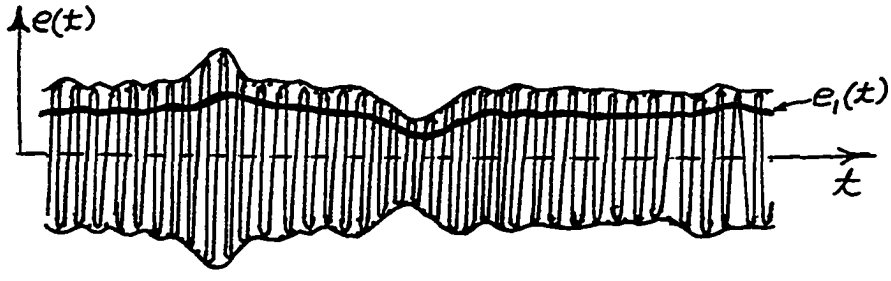


Figure 2.21 Block Diagram and Waveform of the Peak-Follower Autocorrelator

CHAPTER III

ENHANCED READ SYSTEM DESIGN

Introduction

In order to increase recording density, advancements in heads, media, and the electronics must be made. Once the parameters of the head and the medium (magnetic recording channel) have been determined, then the role of the detection system and the associated electronics may either deteriorate or significantly improve the performance. This claim has been proven time and time again during the last decade and deserves consistent follow up in the future. The read system, the design of which is presented in this chapter, is only moderately more complex than some current systems, but at the same time facilitates higher recording densities resulting in net savings. The improvement is achieved by employing signal equalization to minimize intersymbol interference, and by application of Integrate and Dump matched filters to minimize susceptibility to imperfections in the medium at high track densities. Furthermore, this system is claimed to be a generalized detector

which may be used in conjunction with any code to operate in regions II, III, or IV of the flux density curve.

In designing the system, both the architecture of the detection system and the specifics of the electronic design deserve careful attention. The system architecture and block diagram are extremely important and should be considered first in the design cycle. Some iterations and refinements of the architecture may be made while performing the detail design. Guidelines governing the architecture are: performance specifications, physical size and packaging restrictions, type of printed wire board layout, signal transmission, filtration, gain partitioning, and timing. Specifics of the electronics design require full familiarity with component specifications and their applications, in addition to expertise in analog and digital circuit design.

The design begins with the given assumptions, the key performance specifications, and system block diagram and timing. The iterations used to arrive at the block diagram and most of the trivial detail design have been omitted in order to give due attention to the main topics.

Assumption and Specifications

Since the design is concerned only with the detection system, certain assumptions must be made. It is assumed that all other functions of the disk file in which this detection system is to be used are designed in compliance

with their specifications. It is also assumed that a track following servo system which provides high degree of positioning accuracy (±100 μinches) and which provides a reference servo track driven "write clock" is employed. A tabulation of the assumptions and the specifications follows.

Assumptions:

1. PLL derived "write clock" locked to pre-recorded servo data.
   Write Clock Frequency 10mHz±5%
   Write PLL Bandwidth 3.5kHz

2. Zoned Current Write Amplifier and Head Select Electronics and Associated Fault Detection Circuits.

3. Low Noise, High CMRR Read Preamp Capable of Driving 75Ω Line.
   Preamp Gain - Differential 220±5%
   Preamp S/N - Minimum 34db

4. Preamp Frequency Response
   Flat Amplitude Response Through 10mHz
   Phase Linearity Through------ 15mHz

5. Head Output Voltage w.r.t Standard Reference Disk
   Maximum Volts - PP differential 0.00075
   Nominal Volts - PP differential 0.00051
   Minimum Volts - PP differential 0.00028

6. Head Output Voltage Variations as a Function of Different Media 2/1

7. Half Amplitude Isolated Pulse Width
   At 2400 IN/Sec 150ns
   At 1600 IN/Sec 200ns

8. Minimum System S/N At Preamp Output 24db

9. Power Supply Requirements:
   +12V±5%@.5A
   -12V±5%@.5A
   + 6V±5%@.2A
   - 6V±5%@.2A
   + 5V±5%@.3A
   - 5V±5%@.6A

Specifications:

1.	Recording Code	MFM
2.	Recording Density	900Kbits/cm^2
	Tracks/INCH (TPI)	900
	BITS/INCH (BPI)	6500
3.	Data Interface	NRZ
4.	Data Transfer Rate	10Mbits/Sec
5.	Error-Rate (Recoverable)	$1X10^{-10}$

System Block Diagram and Timing

The block diagram and its associated steady state timing, after phase lock, are depicted in figures 3.1 and 3.2. Prior to proceeding with the design of the individual functions, a description of the operation follows.

An arbitrary MFM encoded sequence (figure 3.2(A)) is assumed to have been pre-recorded. Prior to activating the read command (Read CMND), the Read PLL is locked to the reference Write Clock which is in turn locked to the speed of the rotating medium, thereby eliminating frequency lock up time requirements. To initiate detection, the Read CMND, under control of the host controller is activated in a field of "all zeros", allowing sufficient time for the PLL to acquire phase lock. During Read, the reproduce signal is preamplified and is differentially transmitted via a shielded twisted pair cable of known characteristic impedance. This signal is received by the data detection system and is further amplified and buffered (B) prior to equali-

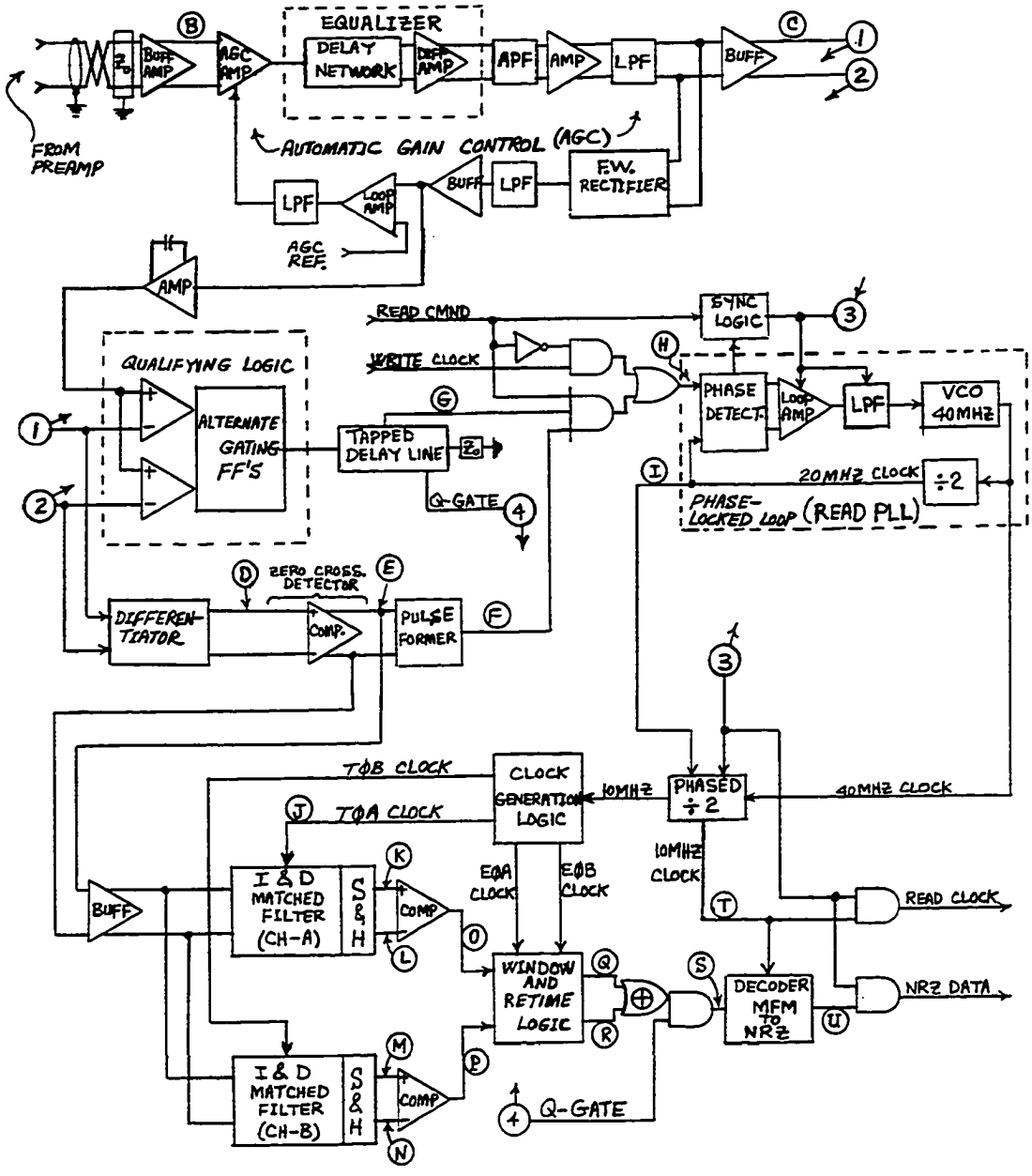


Figure 3.1 Block Diagram of the Enhanced Read System

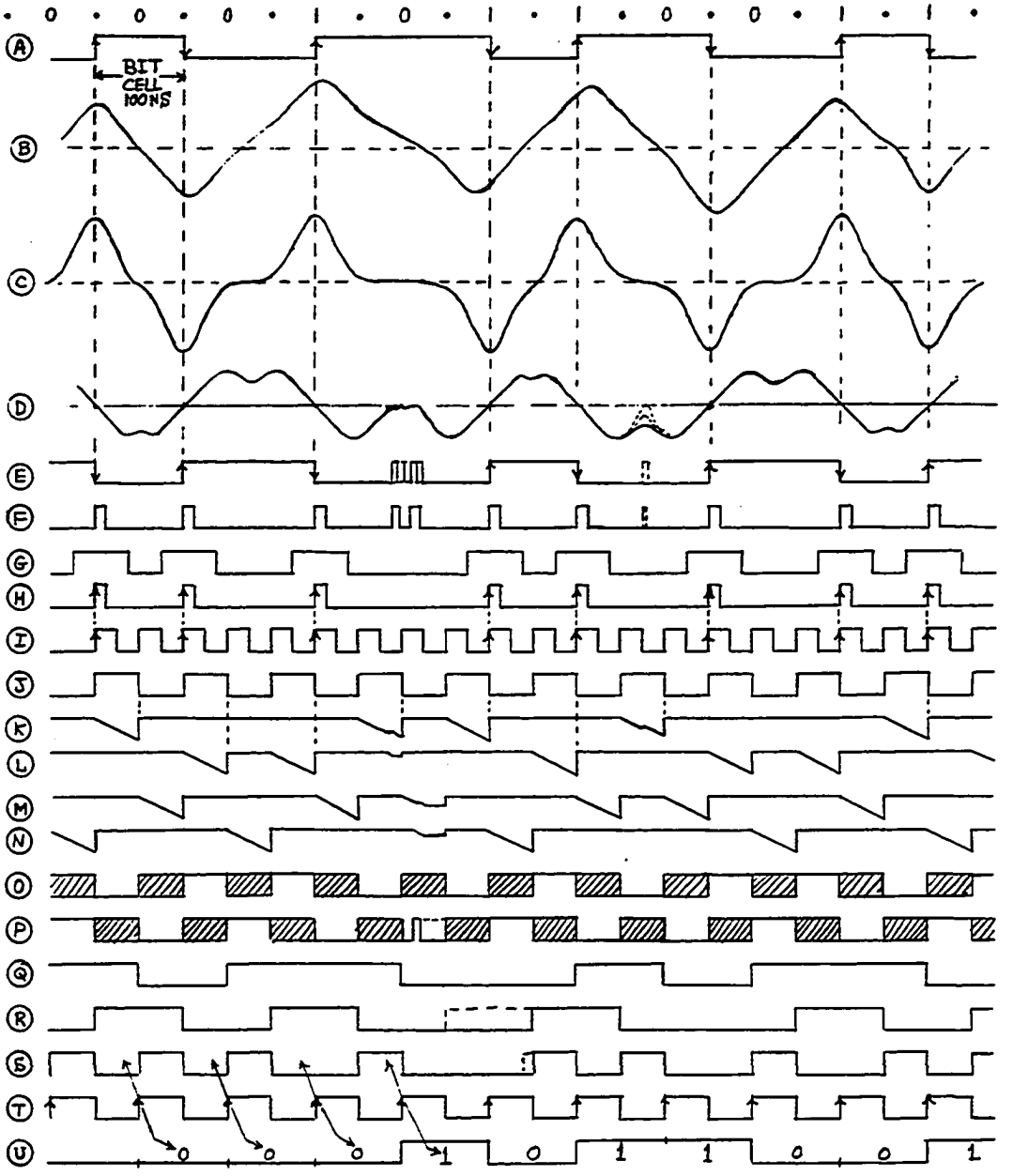


Figure 3.2 Timing Diagram of the Enhanced Read System

zation and automatic gain control. The equalized and gain controlled signal (C) is then differentiated (D) and is applied to the zero crossing detector to produce signal (E). Signal (C) is also used to generate signal (G) which is in turn used to qualify the pulse formed signal (F), removing majority of noise induced extraneous pulses and providing the reference signal (H) for the PLL. The PLL, through the Clock Generation Logic, provides appropriate clock phase (J) which is used to coherently "Integrate and Dump" signal (E), providing signals (K) and (L). In a parallel path, the alternate phases of the clock and data provide signals (M) and (N). These signals are subsequently level compared, resulting in signals (O) and (P), which are then sampled at appropriate times to produce signals (Q) and (R). Signals (Q) and (R) are "exclusive ORed" and are gated by the qualifying signal Q-Gate, producing signal (S) before being converted to the NRZ signal (U).

Equalizer and Filter Design

Signal Amplitude and Gain Scaling

The read signal received from the preamplifier is terminated in its characteristic impedance of 75 ohms in order to eliminate reflections and signal distortion. The amplitude of the read signal changes due to preamp gain tolerances of $\pm$5%, head signal variations from 0.28mV to 0.75mV, and media variations of 2/1. The maximum, minimum, and nominal peak-to-peak differential (ppd) amplitudes are:

A(max) = (220)(1.05)(0.75)(2)=347mV-ppd

A(min) = (220)(0.95)(0.28)(1) = 58mV-ppd

A(nom) = (220)(0.51) =112mV-ppd

The front-end gain scaling is achieved by the circuit of figure 3.3 prior to equalization. The received signal is differentially amplified by U1 which is configured for gain of 10, with gain variations from 9 to 11. Since the minimum gain for U1 is 9, an attenuation factor of 0.277 provided by R3, R4, R5, and R6 is necessary to properly scale the gain for a balanced AGC dynamic range. Emitter followers Q1 and Q2 provide bufferring for the attenuated signal and isolation for the AGC elements R10, R11, and Q3. The buffered signal is "AC Coupled" through capacitors C1, C2 and resistors R8, R9 in order to set signal DC reference to ground and to provide known bias for U2.

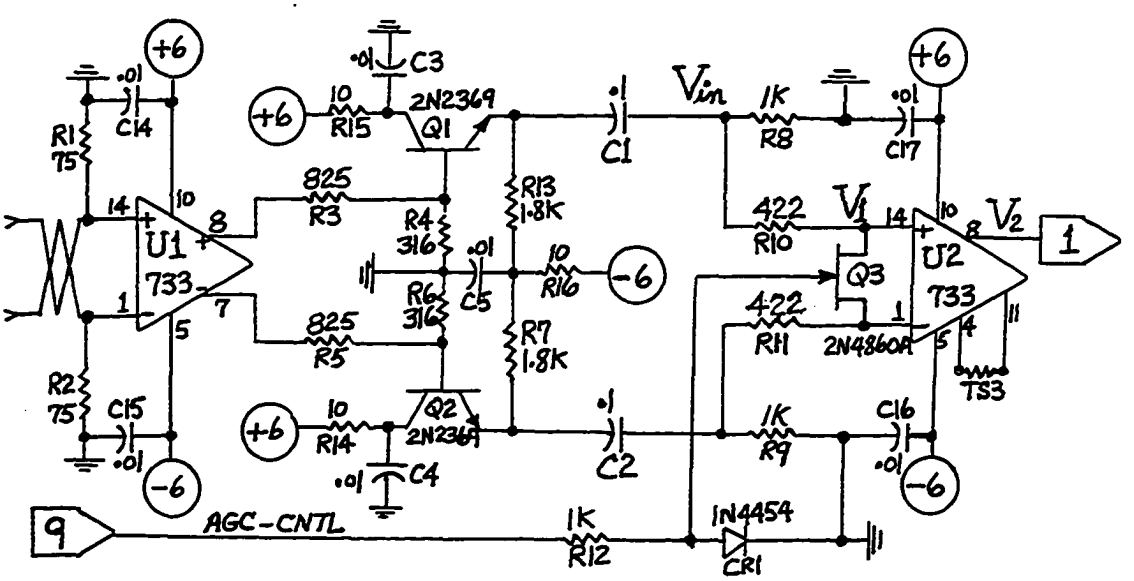


Figure 3.3 Front-End Gain Scaling

Q3, an N-channel field effect transistor, operates as a variable resistor controlled by the AGC loop, keeping the signal amplitude at V_1 constant. V_1 must be small or distortion due to FET nonlinearity will result. As it will be shown later, V_1=55mV-ppd, provides proper AGC dynamic range. Amplifier U2 which has a nominal differential gain of 16 set by "Test-Selected" resistor TS3, provides sufficient signal amplitude for the equalizer which follows. Ignoring small degree of signal attenuation due to Q1 and Q2, the signal amplitudes thus far are,

$V_{in}(max) = (0.28)(11)(0.347) = 1.07V\text{-ppd}$

$V_{in}(min) = (0.27)(9)(0.058) = 0.141V\text{-ppd}$

$V_{in}(nom) = (0.277)(10)(0.112) = 0.31V\text{-ppd}$

$V_1(nom) = 55mV\text{-ppd}$

$V_2(nom) = 0.88V\text{-ppd}$

Equalizer Design

The equalizer, the principle of which was presented in chapter II, has a circuit realization depicted in figure 3.4. Signal V_2, through emitter follower Q4 and AC coupling capacitor C6, drives a cascade of three 50ns, 100 ohm tapped delay lines terminated in R21. With reference to chapter II, the proper tap selections for the specified mean value of PW_{50}=175ns is, $\tau=\tau_1=\tau_2=0.35(175ns)=60ns$. Emitter followers Q5 and Q6 drive the attenuation network R28, R29, R30. This network attenuates the undelayed and the 2τ delayed signals by 65 percent. The summed attenuat-

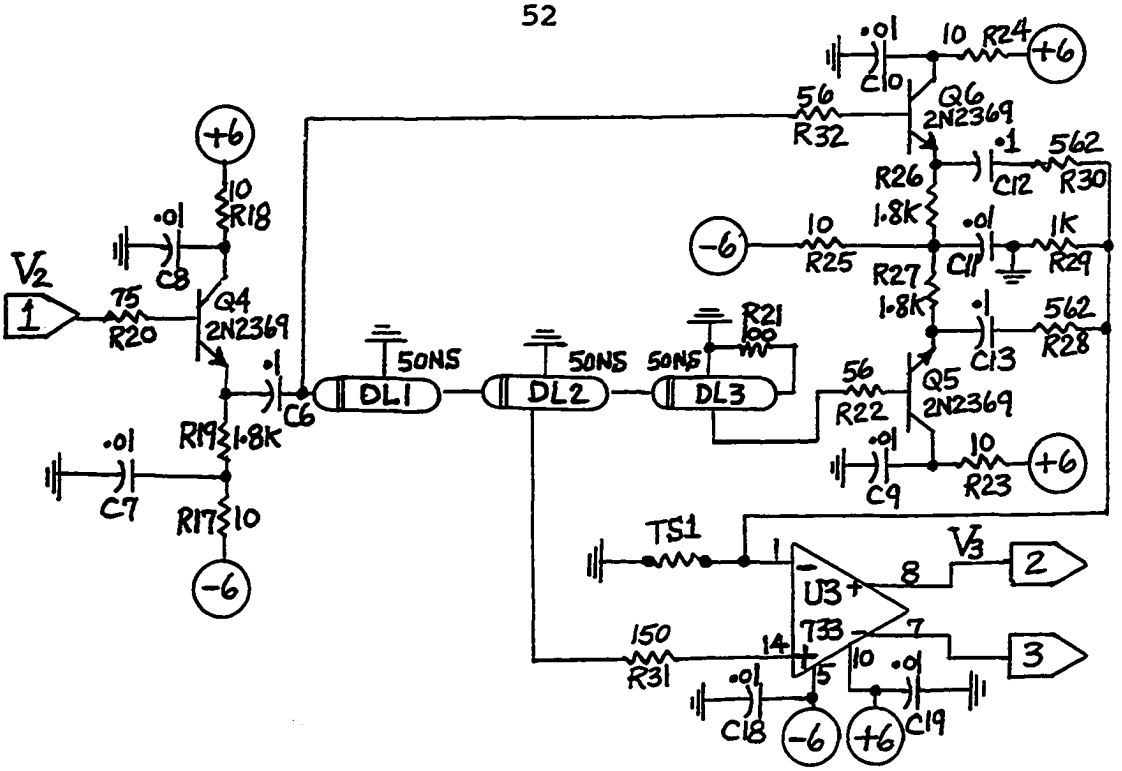


Figure 3.4 Circuit Realization of the Equalizer

ed signal and the τ delayed signal are differentially added and amplified by U3. Signal V_2 is delayed 60ns but is essentially unattenuated at the "+" input of U_3. The amplitude of the equalized signal for the given PW_{50}(max, min) =(200ns,175ns) is calculated with reference to figure 2.16, using the "worst case" amplitude tribit pattern:

		unequalized		equalized	
$\frac{T_o}{PW_{50}}$	$\frac{100ns}{150ns}=0.67\rightarrow$	A,C 0.75	B 0.35	A,C 0.5	B 0.42
$\frac{T_o}{PW_{50}}$	$\frac{100ns}{200ns}=0.5\rightarrow$	0.7	0.05	0.47	0.35

To determine the absolute instantaneous signal amplitudes, the equalized signal is first normalized with respect to

the unequalized signal, and then is multiplied by the gain of amplifier U3:

For PW_{50} = 150ns:

$$V_3(A,C)=\left(\frac{0.5}{0.75}\right)\frac{V_2}{2}(10)=(0.67)(0.44)(10)=2.95V\text{-ppd}$$

$$V_3(B)=\left(\frac{0.5}{0.75}\right)\frac{0.42}{0.5}(0.44)(10)=2.48V\text{-ppd}$$

For PW_{50} =200ns:

$$V_3(A,C)=\left(\frac{0.47}{0.7}\right)\frac{V_2}{2}(10)=(0.67)(0.44)(10)=2.95V\text{-ppd}$$

$$V_3(B)=\left(\frac{0.47}{0.7}\right)\frac{0.35}{0.47}(0.44)(10)=2.2V\text{-ppd}$$

The variations in V_3 calculated above are due only to intersymbol interference and are not compensated for by the AGC. They do however, to a small degree modulate the peak follower. The value of V_3 which is of interest for the AGC loop gain calculations is,

$$V_3(avg)=\frac{2.2V+2.95V}{2}=2.58V\text{-ppd}$$

Peak shift calculations are made by denormalizing values corresponding to the equalized dibit pattern of figure 2.16 as follows:

$$\frac{T_o}{PW_{50}}=\frac{100ns}{150ns}=0.67\longrightarrow Tp=\frac{100ns}{40}=\pm 2.5ns$$

$$\frac{T_o}{PW_{50}}=\frac{100ns}{200ns}=0.5\longrightarrow Tp=\frac{100ns}{11}=\pm 9ns$$

Both the amplitude and the peak shift thus calculated are indeed "worst case" since the MFM low frequency band falls within that of the simulated dibit and the tribit. The equalizer constants have been chosen such that there is a

crossover point between the peak shifts of the equalized dibits and the tribits at the point which corresponds to the mean value of PW_{50}=175ns. This is done to split peak shift evenly and minimize pattern sensitivity.

It should be noted that, special care in the printed wire board layout is required to insure minimum loss of common mode rejection due to the equalizer single ended circuits. To minimize ground loop currents and chance of high frequency oscillations, judiciously designed ground plane and signal routing is necessary. Filter-bypass networks such as R17, C7 and R18, C8 are used throughout to minimize probability of circuit oscillations.

Filter Design

So far, the signal has been properly amplified and equalized in order to enhance spectral definition and remove peak shift and amplitude variations to a great extent. No filter other than the wide band filter specified for the preamp has been used so far, in order to sufficiently preserve the harmonic content of the signal for proper equalization. Prior to zero crossing detection however, it becomes necessary to limit bandwidth as much as possible in order to reduce random noise and the effect of high frequency media noise. Phase linearity must be preserved up to and including 1.5 times the data frequency. This will insure inclusion of the third harmonic of the lowest MFM frequency within the linear region and hence minimizes the

degree of phase distortion. For the specified data transfer rate of 10Mbits/Sec, the highest MFM analog data frequency is 5mHz corresponding to an all "ones" or an all "zeros" sequence. The lowest analog waveform frequency is 2.5mHz and corresponds to an alternating ones and zeros sequence. It is therefore necessary to design the overall section, after the equalizer and before the zero crossing detector, to be phase linear up to at least 7.5mHz.

The circuit of figure 3.5 is comprised of the lattice "all pass" filter (R35, R36, C22, C23) at the input of a cascode amplifier (U4, Q7, Q8) which is in turn followed by a five pole linear phase filter and the emitter followers Q9 and Q10.

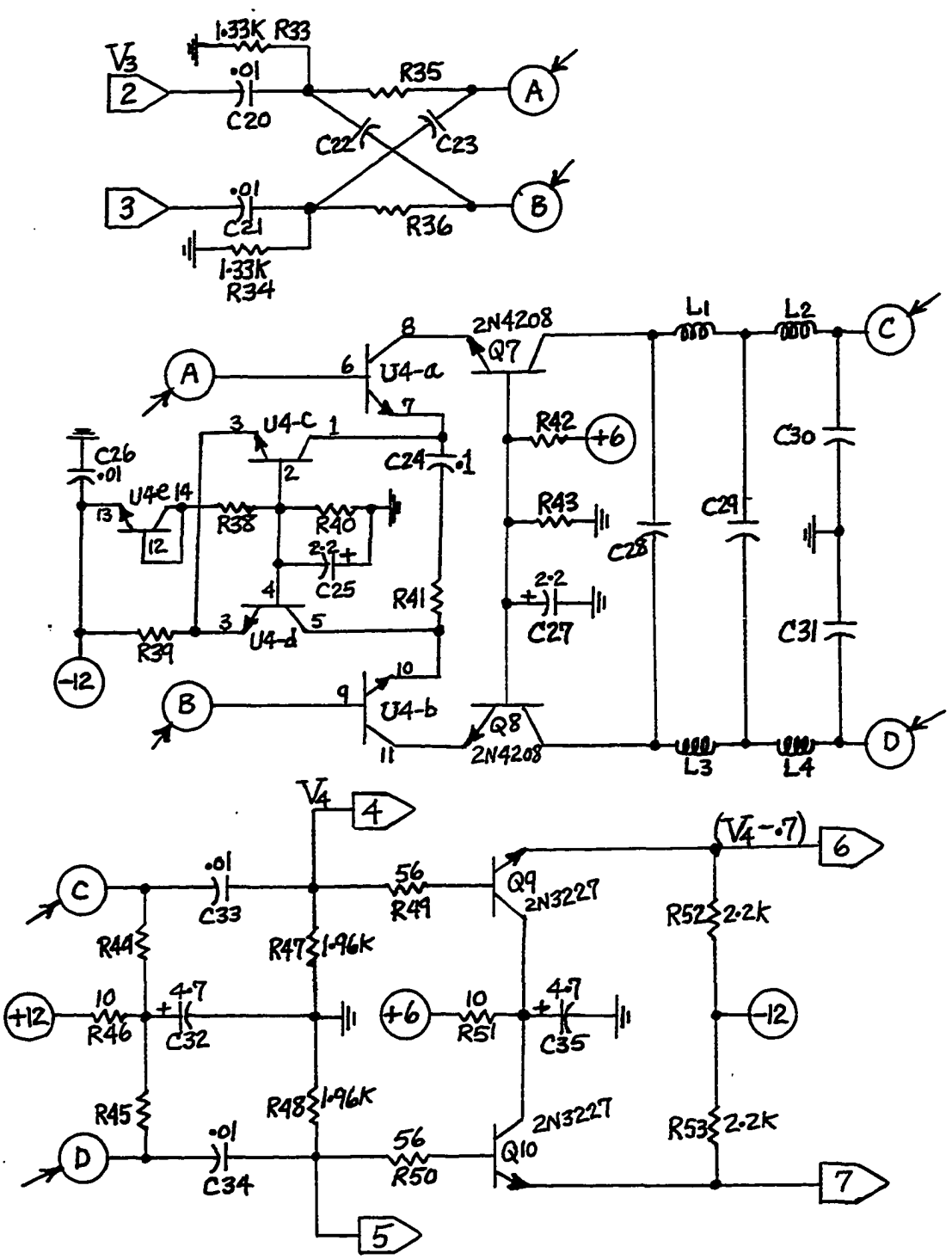


Figure 3.5 Schematic of Compensation Filters and the Cascode Amplifier

Lattice Phase Compensator

The lattice section has a flat amplitude response and is designed to compensate for minor phase nonlinearities due to the differentiator, the amplifiers, and the PWB stray capacitance. The equivalent circuit of figure 3.6 represents the filter being driven by a differential voltage source U3, and looking into high input impedance U4.

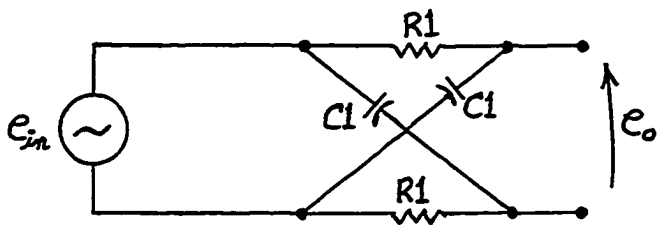


Figure 3.6 Equivalent Circuit of the Lattice

The transfer function of the lattice is,

$$\frac{E_o(s)}{E_{in}(s)} = \frac{1-R_1 C_1 s}{1+R_1 C_1 s}$$

By allowing $s \rightarrow j\omega$, and solving for the magnitude M_1 and the phase Φ_1, we get

$$M_1 = 1$$

$$\Phi_1 = \tan^{-1}\left\{\frac{-2a_1}{1-a_1^2}\right\} \qquad (3\text{-}1)$$

Where, $a_1 = \frac{\omega_1}{\omega_{o1}} = \frac{f_1}{f_{o1}}$, and $\omega_{o1} = \frac{1}{R_1 C_1}$

The plot of the phase angle as function of a_1, shown in figure 3.7, is useful in determining values of R_1 and C_1. These values may be fine tuned subsequent to final board

layout. As it will be shown later, R_1=511 ohms, and C_1= 27pF ($f_{o1} \simeq 11.5$mHz) provide proper phase compensation for the differentiator, throughout the passband.

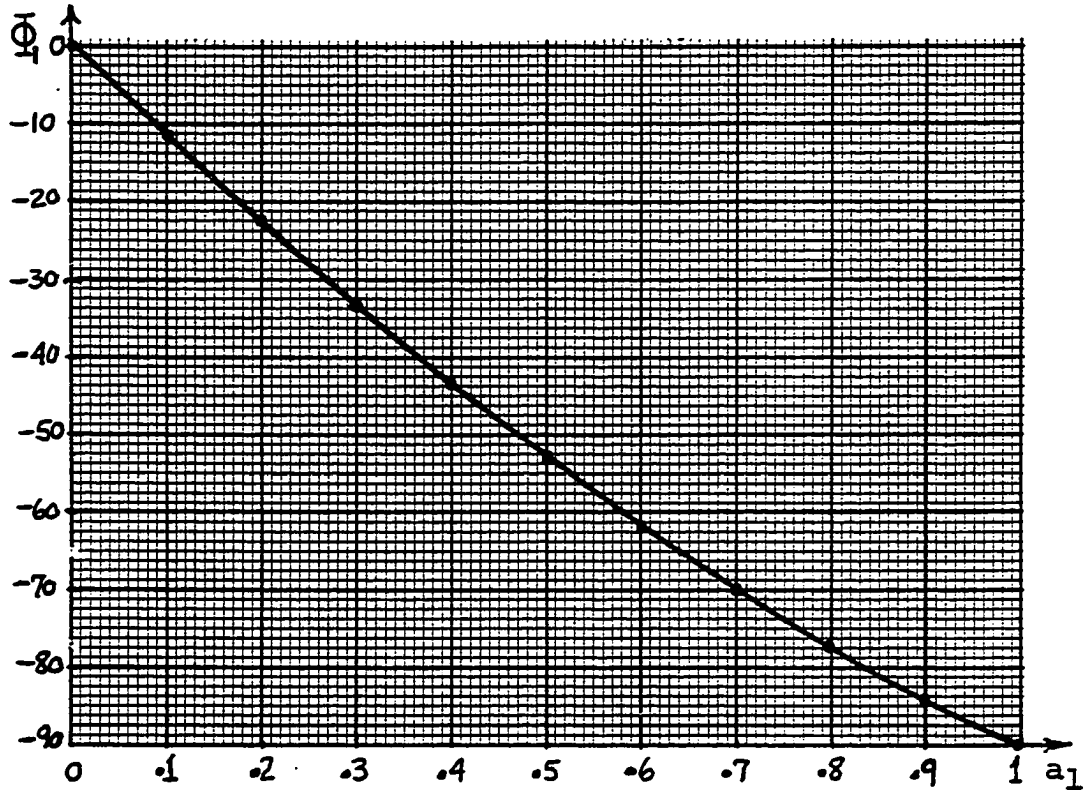


Figure 3.7 Phase Plot for the Lattice

Cascode Amplifier and Linear Phase L.P.F.

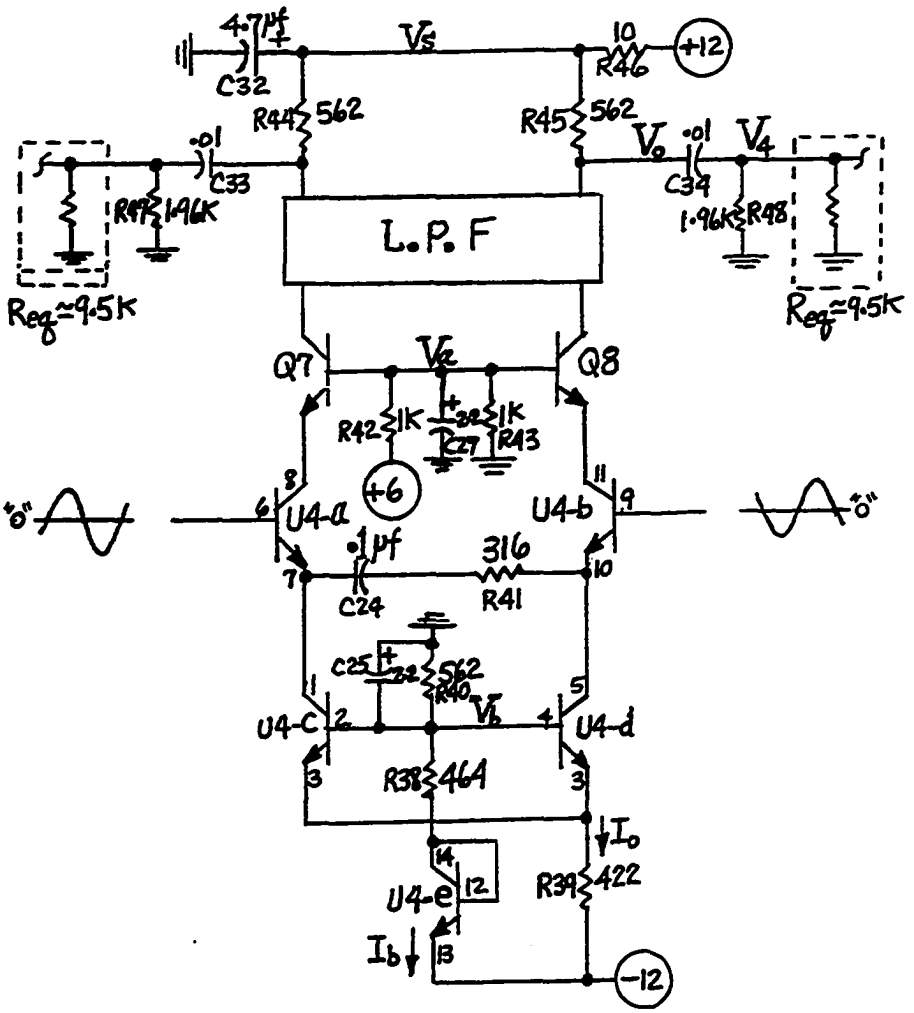
The cascode amplifier has been chosen to facilitate predictable low pass filter design by providing a very high output impedance to the filter, in addition to improving common mode rejection ratio (CMRR). The desired differential gain is 2.6. From the previous calculations, V_3(max) = 2.95V-ppd. To minimize chance of amplifier saturation, sufficient operating room in bias selection must be pro-

vided to allow a larger value of V_3 due to addition of media noise. V_3(max)=4V-ppd is a reasonable assumption. In figure 3.8, the schematic of the cascode differential amplifier and some selected calculations at nominal values are shown. The circuit values have been calculated for proper operation under worst case component tolerances. U4 is a transistor array with V_{BE} matching to within 5mV. This matching provides proper current splitting in the differential amplifier. With the assumed maximum input voltage of 2 volts peak-to-peak single ended (2V-pps), or 1 volt peak, the DC bias of V_b guarantees sufficient collector reverse bias working voltage for the differential current sources U4-c,d. Similarly, the DC bias value of V_a=+3V, does not allow emitters of Q7 and Q8 to drop below 2.2 volts, keeping collector-base junctions of U4-a,b in reverse bias operation. Total DC bias current of 13mA, set by R39, splits equally through the collector resistors R44 and R45 to provide the quiescent value of the output voltage allowing maximum signal amplitude at the output. The differential voltage gain A_d, for the amplifier may be approximated by

$$A_d = \frac{h_{fe} \cdot R_{ceq}}{(1+h_{fe})R_e + h_{ie}} = \frac{110(418)}{111(316/2)+440} = 2.56$$

$$\text{where, } h_{ie} = \frac{h_{fe} \cdot V_T}{|I_c|} = \frac{110(26\text{mV})}{6.5\text{mA}} = 440$$

$$R_{ceq} = 562 \| 1.96\text{k} \| 9.5\text{k} = 418\Omega$$



$$V_a=\frac{6(1k)}{2k}=+3V \quad , \quad V_b=\frac{-11.3(562)}{562+464}=-6.19V$$

$$I_b=\frac{12-0.7}{562+464}=11mA \quad , \quad \text{Let, } I_o=13mA$$

$$R39=\frac{6.19-0.7}{13mA}=422\Omega \quad , \quad R_o=562\|1.96k\|9.5k=418\Omega$$

$$V_s=12-10(13mA)=11.9V \quad , \quad V_o\,(DC)=11.9-6.5mA(562)=8.2V$$

Figure 3.8 The Cascode Amplifier

The CMRR calculates to be in excess of 80db and the unfiltered AGCed output voltage V_4' becomes,

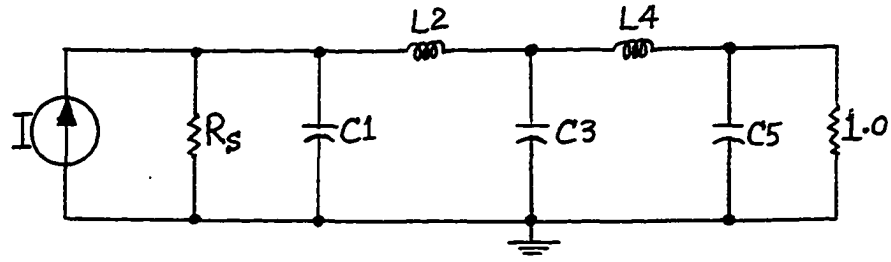
$$V_4'(avg)=V_3 \cdot A_d=(2.58)(2.56)=6.6V\text{-ppd}$$

The maximum and the minimum instantaneous voltages at V_4' before filtering are,

$$V_4'(max)=(2.95)(2.56)=7.55V\text{-ppd}$$

$$V_4'(min)=(2.2)(2.56)=5.63V\text{-ppd}$$

To provide good attenuation and phase linearity with minimum ripple, a 5 pole equiripple linear phase filter of 0.05° error is considered. The single sided equivalent circuit of the filter along with the normalized values are shown in figure 3.9.



$$L=\frac{R_r}{\omega_r}L' \qquad C=\frac{C'}{\omega_r \cdot R_r}$$

Normalized Values for $R_s=\infty$:

$C_1'=1.5144$ $\quad L_2'=1.0407$
$C_3'=0.8447$ $\quad L_4'=0.6177$
$C_5'=0.2456$

Figure 3.9 Five Pole Linear Phase L.P.F

Group delay of such a filter is flat up to 1.6 times the cutoff frequency. To provide phase linearity through 7.5mHz, it is sufficient to have $f_c \geq (7.5)/(1.6)=4.69$mHz. It is also desirable to minimize the attenuation of the signal. $f_c=5.8$mHz results in only 1.26db average attenuation and extends phase linearity up to 8.7mHz. The new V_4 value after applying filter attenuation becomes,

$$V_4(\text{avg})=(0.86)(6.6)=5.68\text{V-ppd}$$

Filter values are denormalized with respect to the equivalent load R_r and the cutoff frequency ω_c as follows,

$$C1 = \frac{1.5144}{3.64\text{x}10^7(418)} = 99\text{pF} \rightarrow (47\text{pFx}2)$$

$$C3 = \frac{0.8447}{1.52\text{x}10^{10}} = 55\text{pF} \rightarrow (27\text{pFx}2)$$

$$C5 = \frac{0.2456}{1.52\text{x}10^{10}} = 16\text{pF} \rightarrow (15\text{pFx}1)$$

$$L2 = \frac{418(1.0407)}{3.64\text{x}10^7} = 12\mu\text{H}$$

$$L4 = \frac{418(0.6177)}{3.64\text{x}10^7} \simeq 6.8\mu\text{H}$$

The differential equivalent filter is obtained by using only half the capacitance values calculated above, yielding half as many capacitors for the design. This option is usually exercised for the larger capacitance values, e.g. C1 and C3.

Design of the Automatic Gain Control Loop

The AGC is designed to provide a known constant amplitude by eliminating "low frequency" amplitude variations due to heads and media. The amplitude control is accomplished by peak detecting the full wave rectified signal and comparing it with a DC reference, to generate an amplitude difference error signal. The error signal is then amplified and filtered in the Loop Amp, and is fed back to the gain control element in order to drive the error signal to a minimum with a stable dynamic response.

Full Wave Rectifier and Loop Amp

The schematic of the F.W. Rectifier and Loop Amp is shown in figure 3.10. Q11 and Q12 provide full wave rectification at their emitters. Capacitor C38 is charged to the peak value of the rectified signal producing a "fast varying"voltage representing essentially the peak value of the signal. R58 provides averaging with some attenuation (G=0.71), while R57 provides a discharge rate of 0.22 volts /μSec, allowing proportional tracking of signal modulation caused by medium imperfections and insufficient over-write. The signal is buffered by the emitter follower U5-a, before being sensed by the Loop Amp and the Peak Follower circuits. The Loop Amp is comprised of the differential amplifier U5-b,c and constant current source U5-d. U5-c is referenced through the test selected resister TS2 to the temperature compensated zener CR2. TS2 is selected to provide

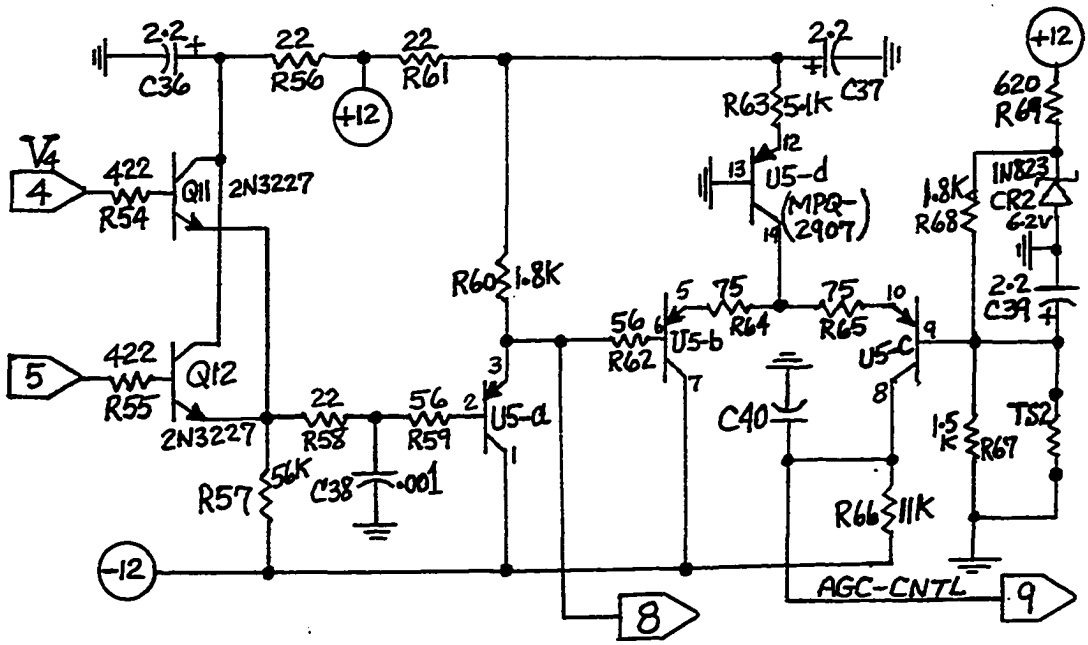


Figure 3.10 Schematic of F.W. Rectifier and the AGC Loop Amp

$(V_4/4)(0.71)$=1.0V-p reference, representing the desired peak signal value at the emitter of U5-a. When the signal at the base of U5-b becomes equal to the reference, approximately half the current (~1mA) is diverted to R66 to set up the appropriate AGC-CNTL voltage necessary to maintain the proper FET(Q3) resistance and hence the desired signal amplitude at V_1 of figure 3.3. When the signal at the base of U5-b becomes larger than the reference, more current is diverted through R66 making the AGC-CNTL signal more positive which in turn results in a smaller FET resistance needed to maintain V_1. Similarly for a smaller than reference signal at the base of U5-b, less current through R66 drives the AGC-CNTL more negative (towards "pinch-off")

allowing larger FET resistance and proportionally less signal attenuation necessary to still maintain V_1.

AGC Loop Design

The AGC Loop is designed by calculating the gain associated with each block, determining dynamic range requirements and FET operating points, and finally by synthesizing the gain and bandwidth requirements of the Loop Amp to meet the overall response. Block diagram of figure 3.11 represents the loop elements and the associated gains. The

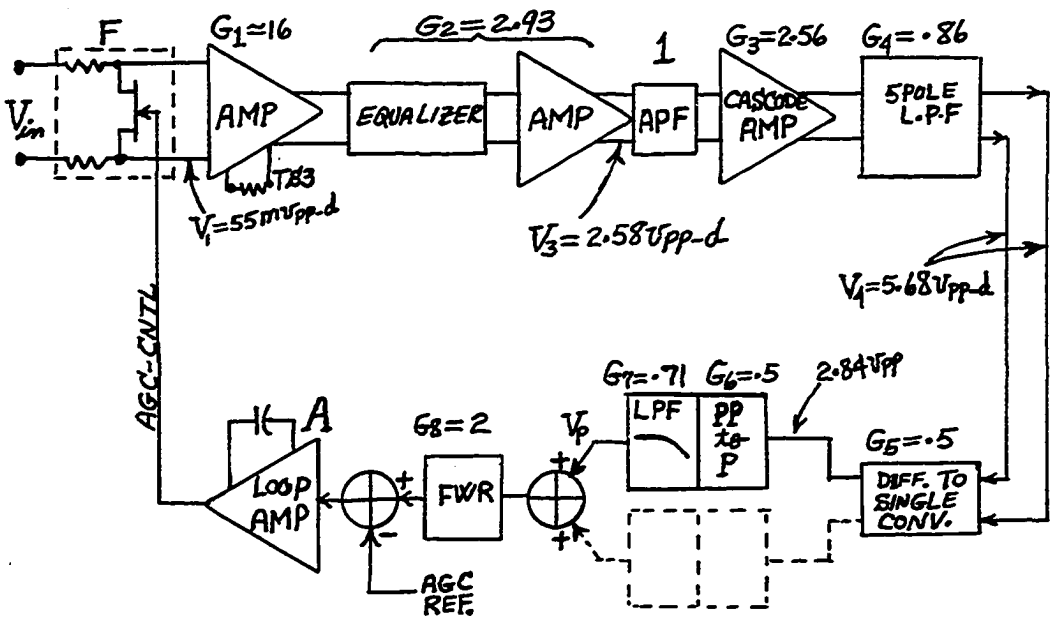


Figure 3.11 AGC Loop Block Diagram

overall loop gain designated by βG is,

$$\beta G=(G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot G_5 \cdot G_6 \cdot G_7 \cdot G_8) \cdot A \cdot F$$

where A is the gain of the Loop Amp, F is the FET gain, and G_i (i=1 to 8) correspond to the remaining blocks. To minimize bandwidth variations due to tolerances in the forward loop, the AGC loop is first opened and resistor TS3 of figure 3.3 is selected to get 1 volt peak rectified voltage at the emitter of U5-a. This will result in a known forward loop gain of

$$\beta G = (16)(2.93)(2.56)(.86)(.5)(.5)(.71)(2) A \cdot F$$

$$= (36.6) A \cdot F$$

D_o is the required dynamic range which is equivalent to the ratio of the maximum and the minimum input signals,

$$D_o = \frac{V_{in}(max)}{V_{in}(min)} = \frac{1.07}{0.141} = 7.6$$

The schematic for the FET (Q3) as a controlled variable resistor, and its single ended equivalent circuit are shown in figure 3.12. The output voltage V_1 may be represented in terms of V_{in} as follows,

$$V_1 = V_{in} \cdot \left[\frac{r_d}{r_d + R} \right] \qquad (3\text{-}2)$$

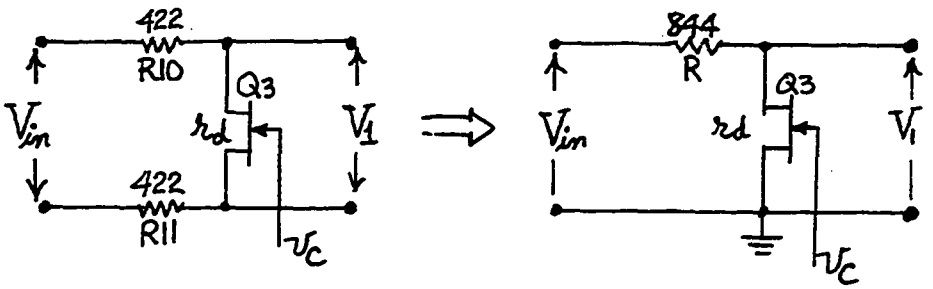
In equation (3-2), r_d is the FET source to drain resistance and is a function of the FET parameters as described below:

$$r_d = \frac{r_{d_o}}{1 - \frac{V_c}{V_p}} \qquad (3\text{-}3)$$

where, v_c = gate to source voltage

r_d = source to drain "on" resistance

v_p = pinch-off voltage



a-Differential b-Single Ended

Figure 3.12 The FET as a Controlled Variable Resistor

By substituting equation (3-3) into (3-2) and taking the derivative of V_1 with respect to v_c, the FET gain is derived to be,

$$\frac{dV_1}{dv_c} = \frac{r_{d_o} \cdot V_{in}}{R \cdot v_p \cdot (1 - v_c/v_p + r_{d_o}/R)^2} \qquad (3\text{-}4)$$

Using equations (3-3) and (3-4), three gain values (max, min, nom) for the FET with characteristics given below are calculated:

FET=2N4860A: $r_{d_o}(max)=40\Omega$, $v_p(min)=-6V$

$r_{d_o}(min)=20\Omega$, $v_p(max)=-2V$

$r_{d_o}(nom)=25\Omega$, $v_p(nom)=-3.5V$

$$r_d(max)=\frac{V_1 \cdot R(max)}{V_{in}(min)-V_1}=\frac{(0.055)(852)}{(0.141-0.055)}=545\Omega$$

$$r_d(min)=\frac{V_1 \cdot R(min)}{V_{in}(max)-V_1}=\frac{(0.055)(836)}{(1.07-0.055)}=45.3\Omega$$

$$r_d(nom)=\frac{V_1 \cdot R(nom)}{V_{in}(nom)-V_1}=\frac{(0.055)(844)}{(0.31-0.055)}=182\Omega$$

$$\left|\frac{v_c}{v_p}\right|_{max}=1-\frac{r_{d_o}}{r_d}=1-\frac{20}{545}=0.963$$

$$\left|\frac{v_c}{v_p}\right|_{min}=1-\frac{40}{45.3}=0.117$$

$$\left|\frac{v_c}{v_p}\right|_{nom}=1-\frac{25}{182}=0.863$$

$$F(max)=\left|\frac{dv_1}{dv_c}\right|_{(max)}=\frac{20(0.141)}{852(2)(1-0.963+20/852)^2}=0.453$$

$$F(min)=\frac{40(1.07)}{836(6)(1-0.117+40/862)^2}=0.00985$$

$$F(nom)=\frac{25(0.31)}{844(3.5)(1-0.863+25/844)^2}=0.0945$$

The new loop gains, taking FET gain variations into account are,

$$\beta G(max)=(36.6)(0.453)\cdot A=(16.6)\cdot A$$

$$\beta G(min)=(36.6)(0.00985)\cdot A=(0.361)\cdot A$$

$$\beta G(nom)=(36.6)(0.0945)\cdot A=(3.46)\cdot A$$

Two considerations influence the selection of the gain and frequency response of the Loop Amp. The first is the minimum DC loop gain necessary for an acceptable steady state error, and the second is the loop bandwidth necessary to have an acceptable AGC response time. For A=100, the minimum loop gain of $\beta G \approx 36.1 = 31.2db$, results in an acceptable steady state error which is well within 1 percent of the AGC reference. In figure 3.10, R66=11K provides the necessary DC gain for A. AGC response time of 10μSec maximum to reach to within 85% of the final value is usually specified and will be used here. The minimum required bandwidth to guarantee this is 200kHz which in turn results in a capacitor value of C40=2400pF. In figure 3.13 the open and the closed loop Bode plots for the different input signal amplitudes are shown. It is noted that the phase response is dependent only on the amplitude demodulator and any filtration thereafter. Figure 3.14 depicts the AGC envelope response for the maximum and the minimum input signal levels.

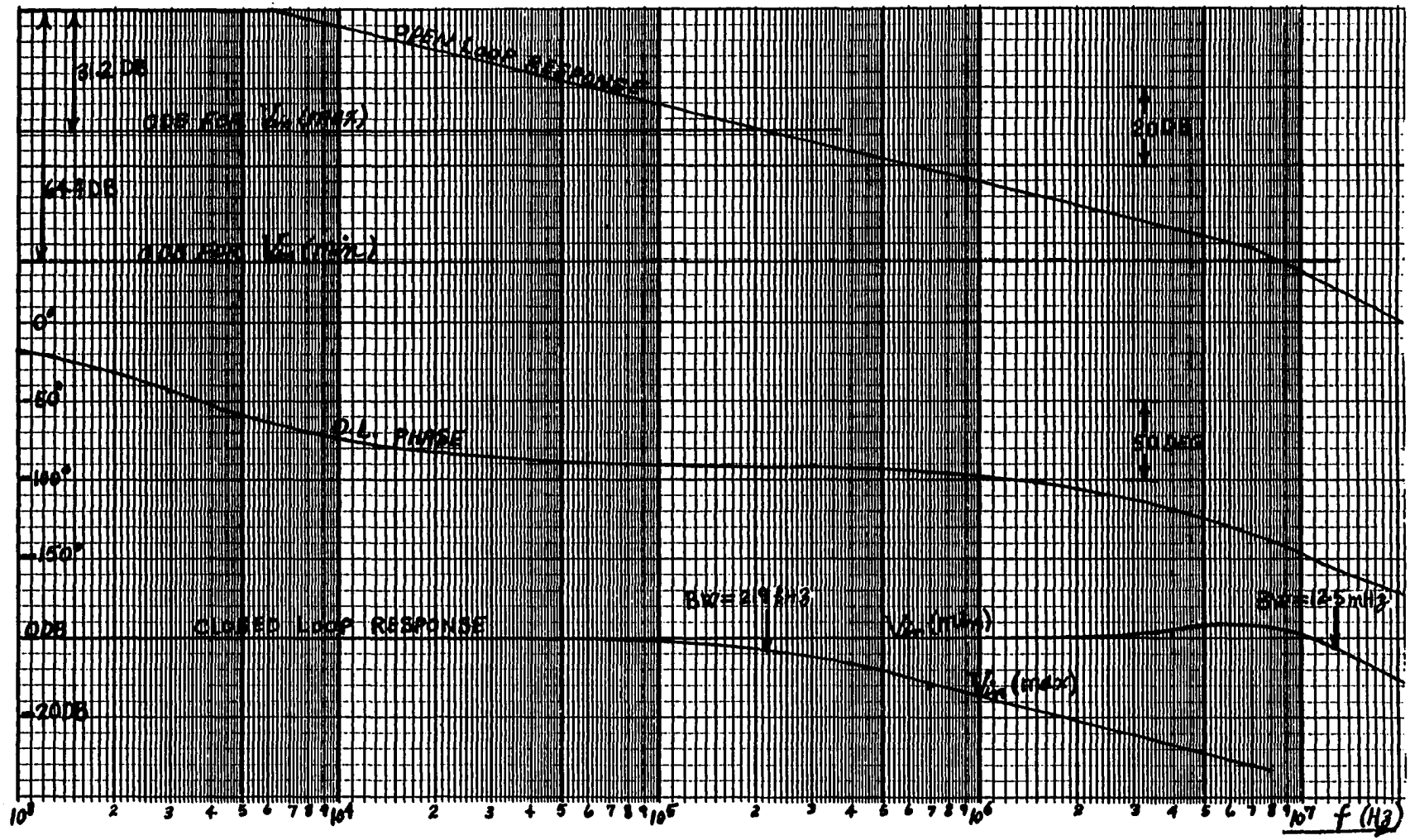
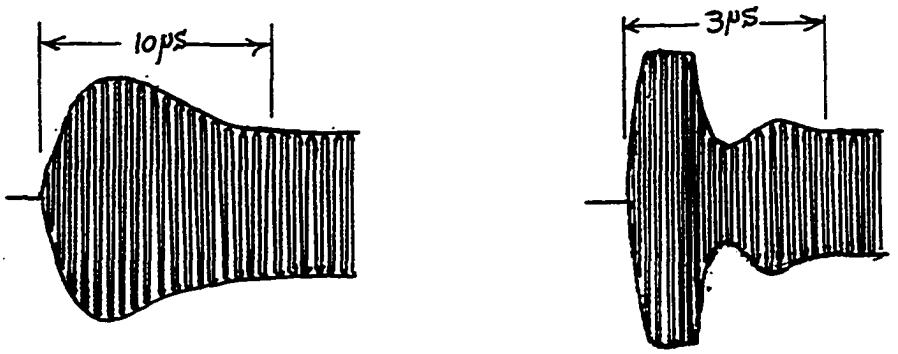


Figure 3.13 AGC Open and Closed Loop Response



a- V_{in}(max) b- V_{in}(min)

Figure 3.14 AGC Envelope Response

Design of the High Resolution Channel and the Zero Crossing Detector

The High Resolution Channel

The high resolution channel which is comprised of the entire signal path previousley discussed, in addition to the differentiator, must be designed to maintain phase linearity up to the zero crossing detector inputs. In figure 3.15, the schematic of the differentiator and the zero crossing detector are shown. The buffered and AGCed signal of figure 3.5 is differentiated by capacitors C41, C42, and resistors R70 and R71. The differentiator cutoff frequency ω_c is chosen such that both the magnitude and the phase response of the overall channel are satisfied. The equivalent circuit of the differentiator which is shown in figure 3.16 results in the transfer function,

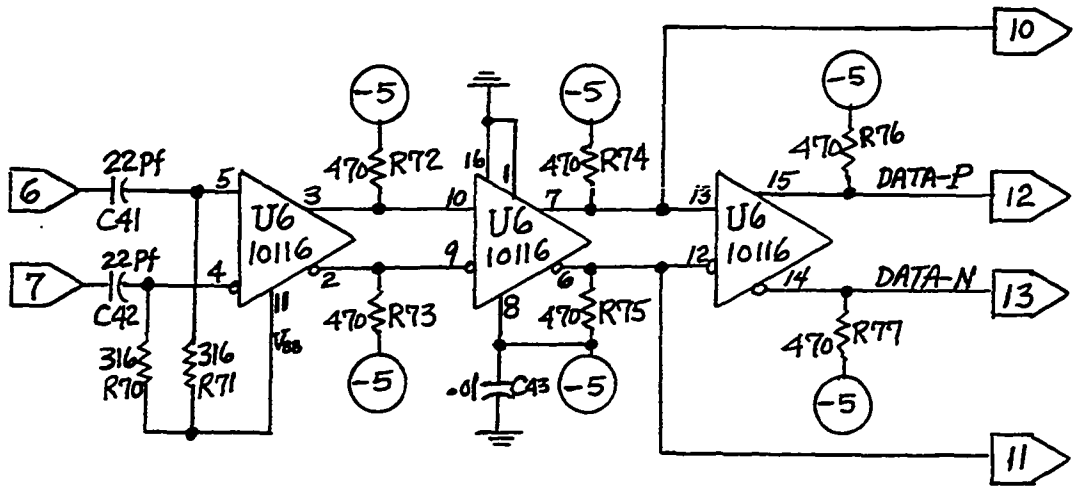


Figure 3.15 Differentiator and the Zero Crossing Detector

$$\frac{E_o(s)}{E_{in}(s)} = \frac{R_2C_2s}{1+R_2C_2s}$$

For $s \rightarrow j\omega$ and by rationalizing, the magnitude M_2 and the phase Φ_2 are derived to be,

$$M_2 = \left[\frac{a_2^2}{1+a_2^2}\right]^{\frac{1}{2}}$$

$$\Phi_2 = \tan^{-1}(1/a_2)$$

where, $a_2 = \frac{\omega_2}{\omega_{o2}} = \frac{f_2}{f_{o2}}$, and $\omega_{o2} = \frac{1}{R_2C_2}$

The normalized magnitude and phase response of the differentiator as a function of a_2 are plotted in figure 3.17. Plots of figures 3.7 and 3.17 are utilized to synthesize a linear phase, high resolution bandpass channel. By allowing f_{o2}=22.5mHz and $a_1=2a_2$ (i.e. f_{o1}=11.25mHz), good sig-

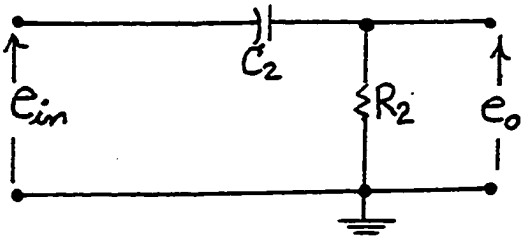


Figure 3.16 The Equivalent Circuit of the Differentiator

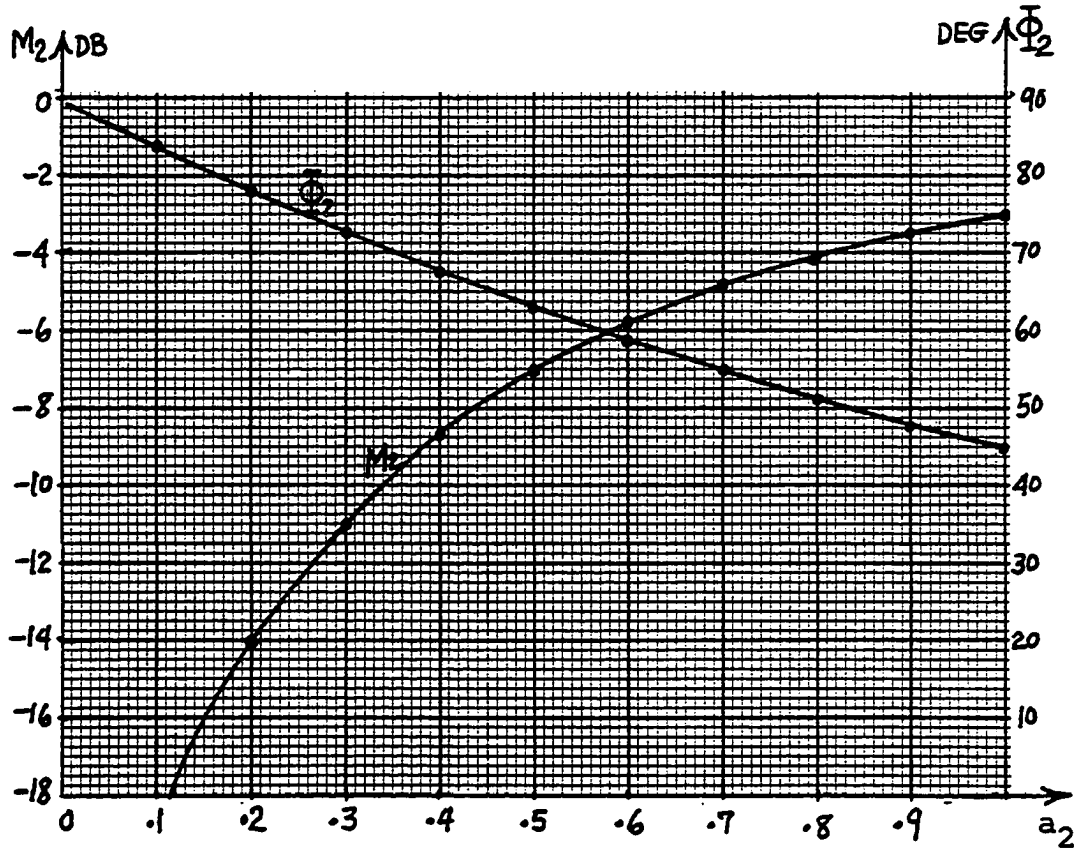


Figure 3.17 Phase and Magnitude Plots of the Differentiator

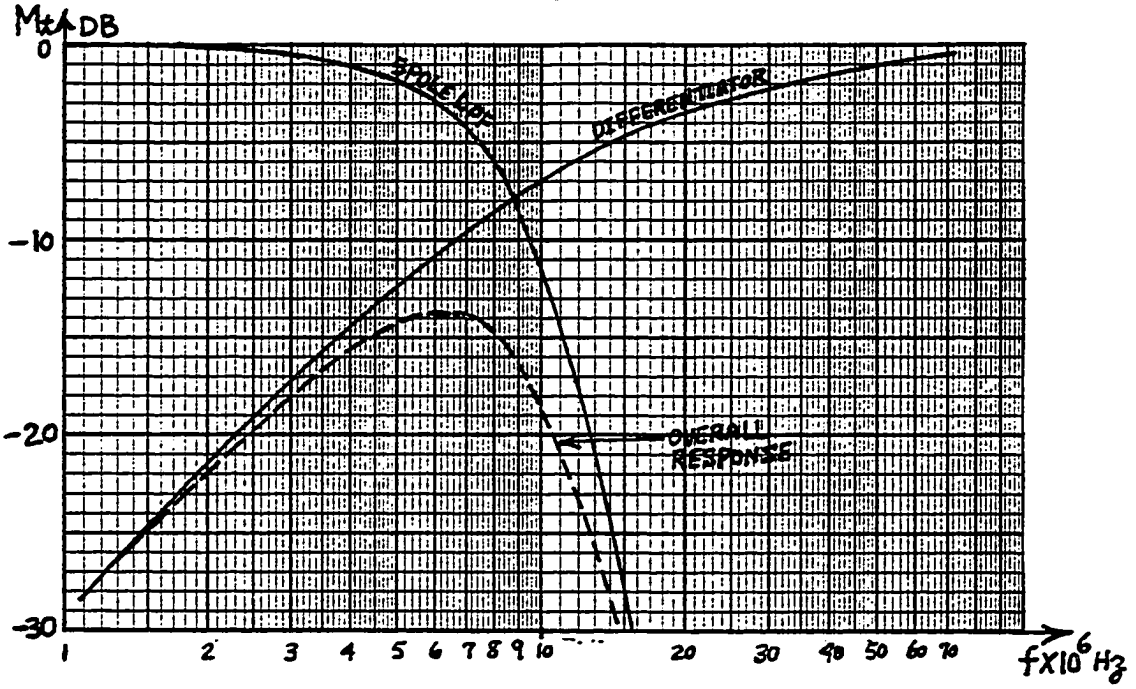
nal resolution, and phase nonlinearity of only 1 degree over the entire frequency range of interest are achieved. The magnitude and phase response up to the inputs of the zero crossing detector are plotted in figure 3.18. The attenuation of 15db at 5mHz and 20db at 2.5mHz tend to make the low frequency fundamental equal to or somewhat smaller than the high frequency fundamental, resulting in a high resolution differentiated signal. The cutoff frequencies of all AC coupling networks have been chosen low enough so that their impact on the magnitude and phase response in the region of interest is negligible.

The Zero Crossing Detector

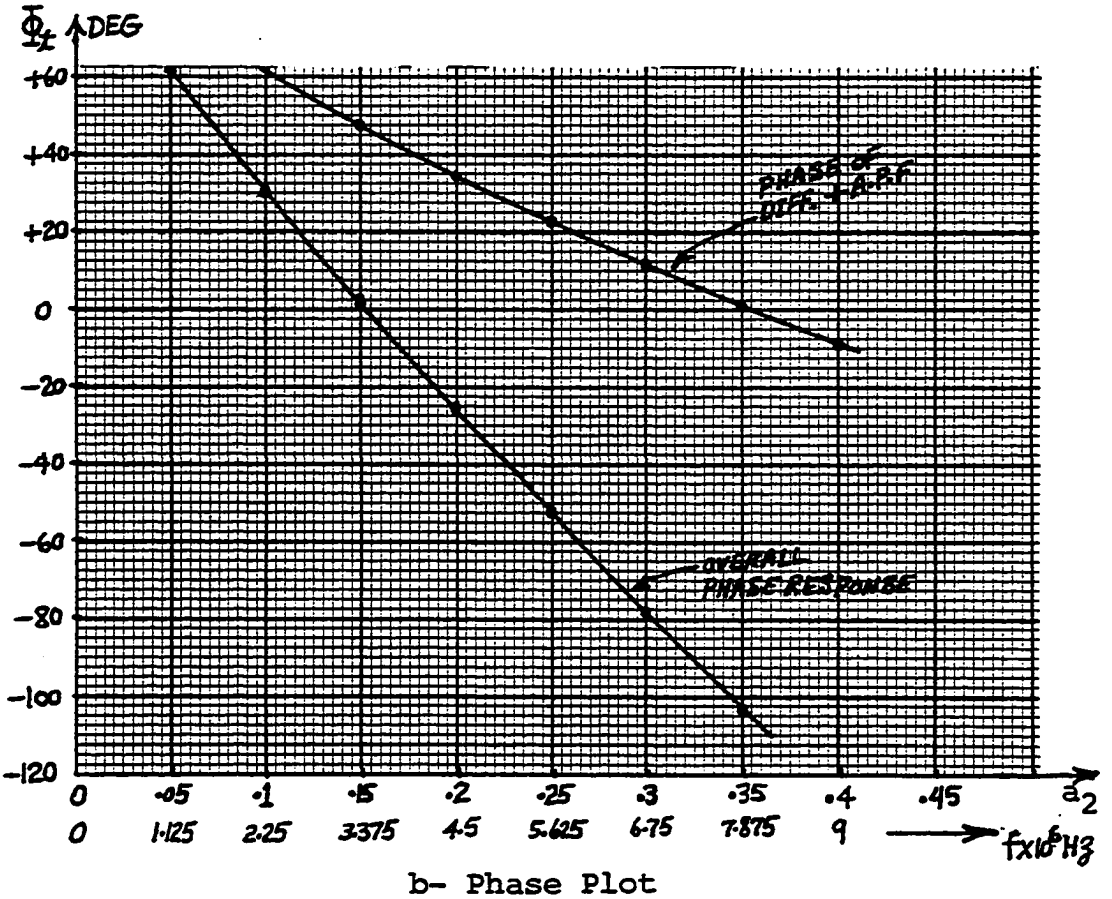
The zero crossing detector of figure 3.15 which is comprised of three cascaded ECL (Emitter Coupled Logic) differential receivers U6, requires ECL compatible maximum input voltage. Gain scaling of the previously discussed blocks provides this compatibility. Resistors R70 and R71 are tied to V_{BB} reference of U6 to provide appropriate DC bias for the inputs. A minimum of two stages of U6 provide the necessary gain for reliable ECL output levels. The signal amplitudes at the input of the first stage are calculated by applying -15db and -20db attenuation factors to the signal amplitudes previously calculated for V_4'.

$$V_5(max)=V_4'(max)\log^{-1}\left[\frac{-15}{20}\right]=7.55(0.178)=1.34V\text{-ppd}$$

$$V_5(min)=V_4'(min)\log^{-1}\left[\frac{-20}{20}\right]=5.63(0.1)=0.563V\text{-ppd}$$



a- Magnitude Plot



b- Phase Plot

Figure 3.18 Frequency Response of the High Resolution Channel

Values for R70, R71, and C41, C42 are then selected to reflect the desired differentiator cutoff frequency of f_o=22.5mHz which yields,

let: R70=R71=316Ω

then, C41=C42=22pF

Design of the Peak-Follower and the Qualifying Channel

The zero crossing detector circuit produces voltage equivalents of the flux transitions which are very well defined in time. The undesirable consequence of this high degree of time resolution is the extraneous crossings which must be gated out. In figure 3.19 the detailed schematic of the circuit which performs the gating function is shown. The output of the zero crossing detector is converted to pulse-per-transition by the pulse former circuit which is comprised of U7, C45, R78 and R79. U7-a and U7-b alternately, and with a very small delay, charge capacitor C45 which is alternately discharged with a longer delay through R79 and R78, producing overlapping delays at the inputs of U7-c,d. The outputs of U7-c,d are "wire ANDed" to produce pulses of approximately 10ns in duration for the values shown. The gating or qualifying of these pulses is accomplished by first thresholding the undifferentiated signal which is AC coupled through C47, C48, R82, and R83 to establish a "ground" DC reference at the inputs of comparator U9. The positive reference input for U9 is the peak-follower signal which has been produced from the full wave

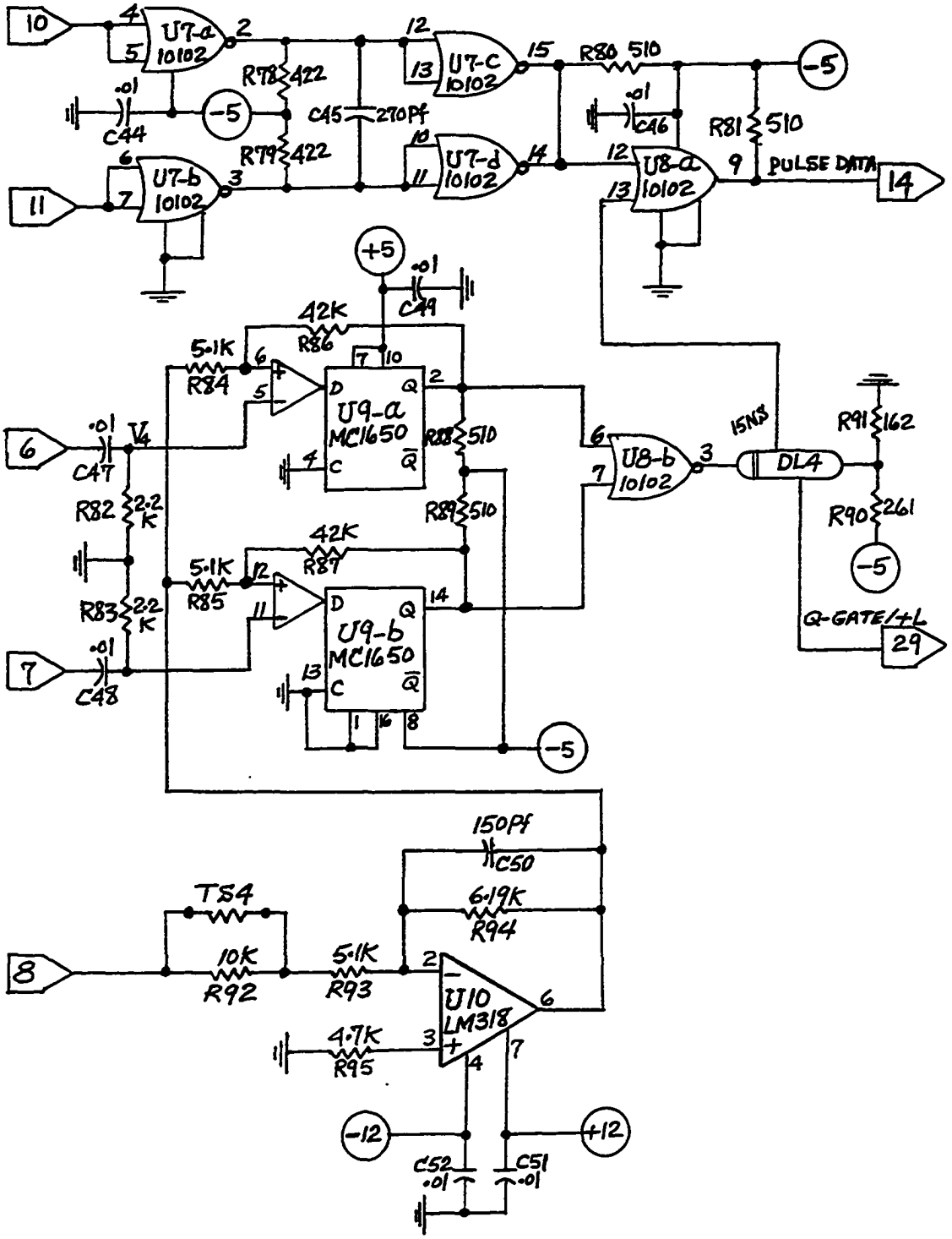


Figure 3.19 Schematic of the Peak-Follower and the Qualifying Channel

rectified AGC Loop Amp signal. Operational amplifier U10 provides additional filtering and threshold scaling to approximately 40% of the average signal peak amplitude. The clock inputs of U9 are grounded to allow continuous sampling of the comparator sections. Additionally, resistors R84, R86, R85, and R87 provide approximately 0.1 volts of hysteresis to minimize chance of multiple triggering. The outputs of U9 are subsequently "ORed" in U8-b and delayed appropriately in DL4 before qualifying the pulse formed signal in U8-a. The necessary delay for DL4 to line-up the paths is 15ns, half of which is due to the differentiator with the rest due to difference in the logic delays of the two paths. The delay of the zero crossing with respect to the signal peak due to the imperfect differentiation is calculated as follows,

at 5mHz: ns/Deg = 200/360 = 0.56

Differentiator Phase=76°

Delay w.r.t Peak=0.56(90-76)=7.78ns

The Phase-Locked-Loop Design

The Phase-Locked-Loop (PLL) is designed to provide an accurate reference clock which is phase locked to the input data. This clock is subsequently used by the "Integrate and Dump" filters, and the Decoder logic as a phase coherent reference. The PLL design presented is a high performance loop design which meets the specific performance requirements with ample margin. It is not however, intend-

ed to be an exhaustive treatment of the subject.

The PLL, a block diagram of which is given in figure 3.20, is comprised of the voltage controlled oscillator (VCO), the loop amplifier and filter, the phase detector, and the divide-by-N scaler.

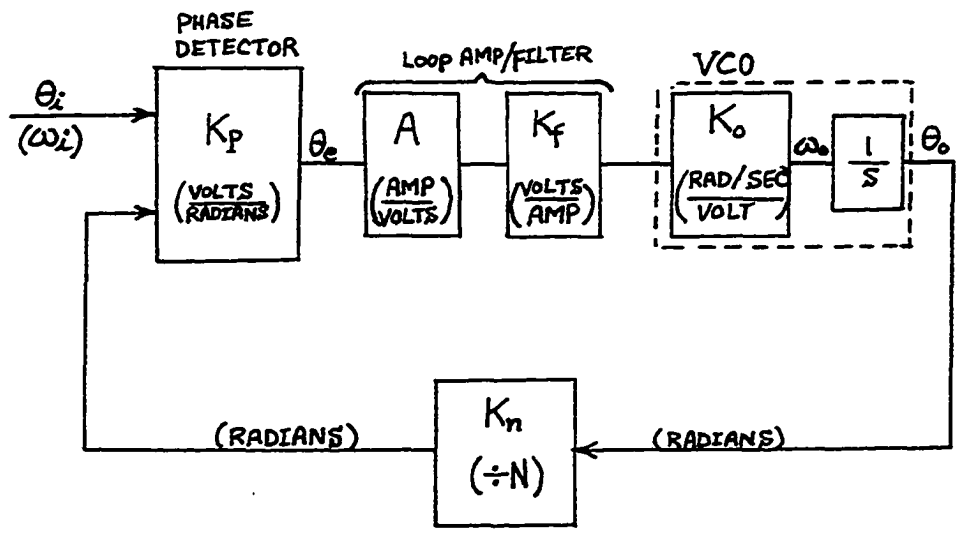


Figure 3.20 Block Diagram of the PLL

The pulse formed signal generated before is fed to the phase detector where it is phase compared with the VCO reference signal. The phase detector produces a proportional error signal which is amplified, filtered, and is fed to the VCO in order to modify its frequency; as a result its phase is forced to comply with that of the input data. The loop should be designed to have negligible steady

state errors for both step phase (position) and step frequency (velocity) inputs, in addition to having at least 50db of sideband rejection. Furthermore, a maximum "lock up" time of 5μSec to settle to within $\pm 1\%$ of the final value is specified. This will insure minimum amount of overhead sync data, and hence an efficient format.

Phase Detector and Clock Logic

Logic schematic and the steady state timing for the phase detector and clock logic are shown in figures 3.21 and 3.22. When the "Read CMND" is not active, a reference 10mHz write clock which is locked to the pre-recorded servo clock on the rotating medium, is passed through U8-c and U9 to the phase detector logic of U10-a, U11-a, and U12-a,b. This keeps the PLL in frequency lock at all times and minimizes the time required for phase lock upon activation of Read CMND. When the Read CMND is activated in a field of all zeros of at least 5μSec duration, the reference clock is disabled, and instead the Pulse Data is gated to the phase detector. The logic comprised of the uniquely configured T^2L single-shot of U15-a and the ECL flip flop of U16-a, generate the "WB-EN" signal. This signal synchronously enables the flip flop of U10-b, producing the "phased" 10mHz Read Clock which is used to generate the different clock phases for the I&D filters and the Decoder logic. The WB-EN signal is also used to increase the loop bandwidth during lock up. Feedback clock to the phase detector

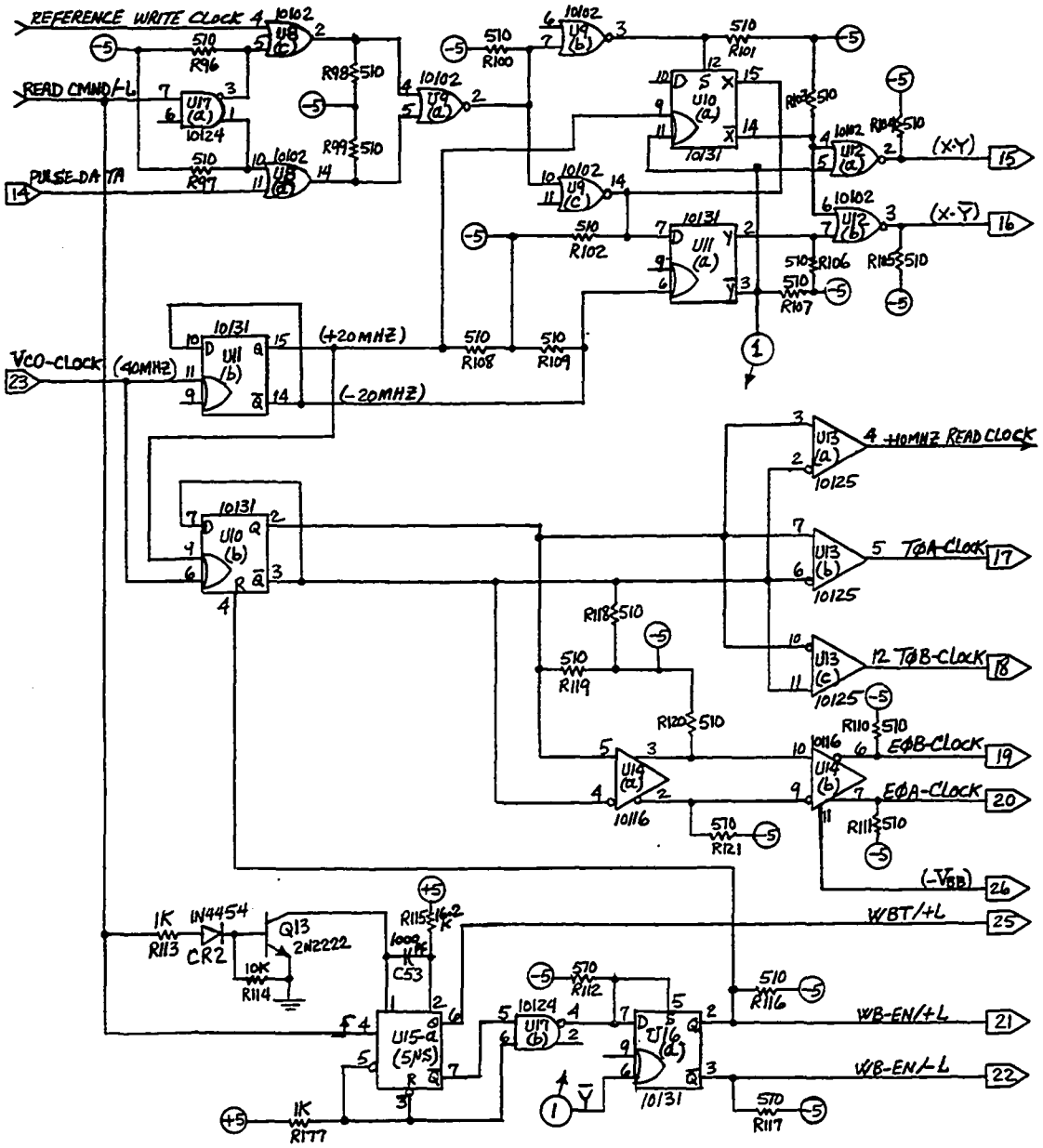


Figure 3.21 Schematic of the Phase Detector and the Clock Logic

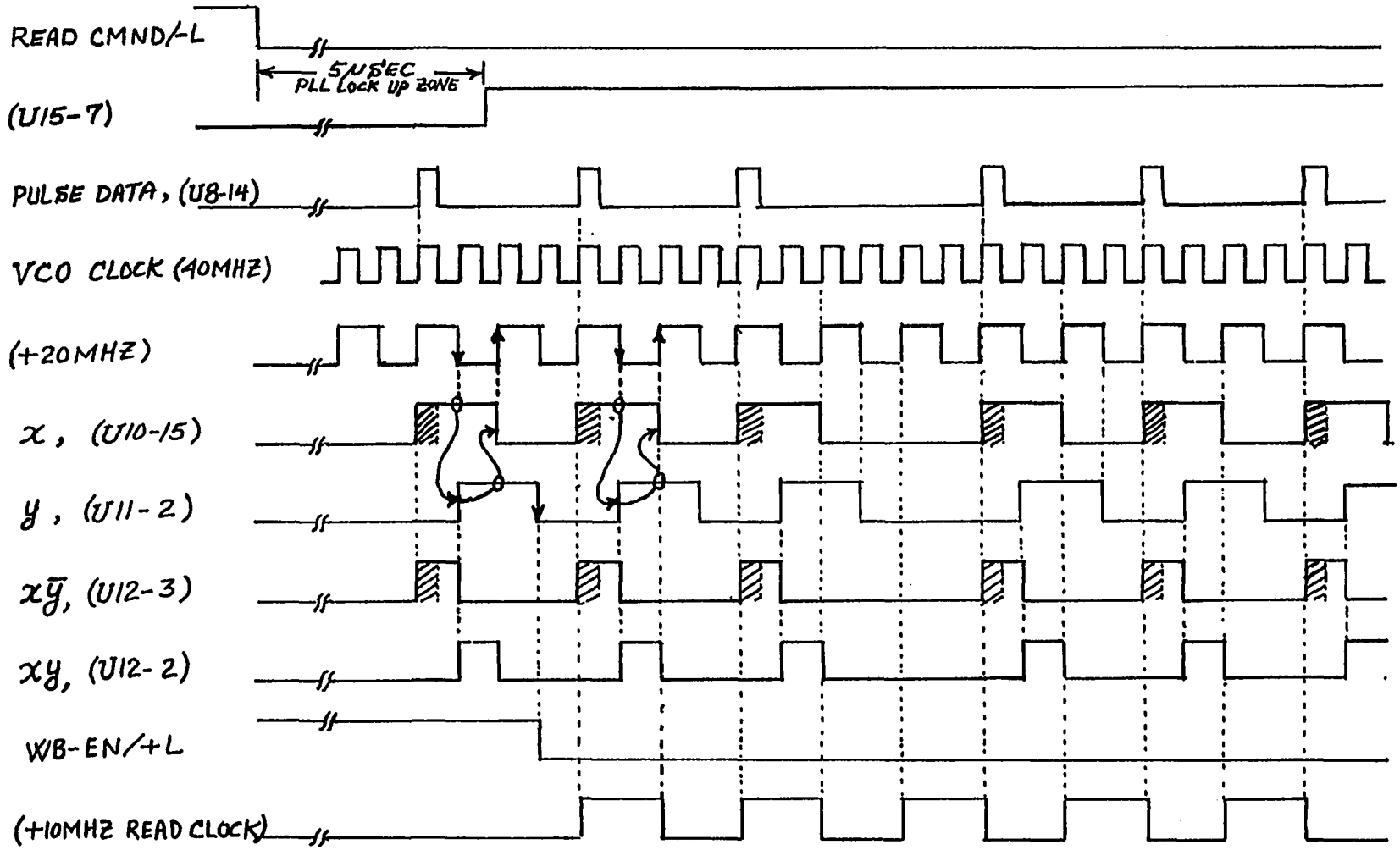


Figure 3.22 Steady State Timing Diagram for the Phase Detector and the Clock Logic

is derived by dividing the 40mHz VCO clock by two, in flip-flop 11-b. An additional phase detector inherent divide-by-two occurs in flip-flop U11-a resulting in $K_n=1/4$.

Phase Detector Gain

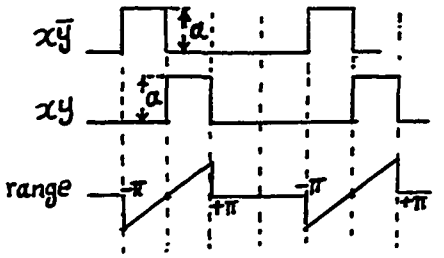
Phase detector gain K_p, is derived by calculating the equivalent DC average voltage per unit of phase error, as follows:

$$K_{p1}=\frac{a/2}{\pi}=0.16a \text{ V/Rad}$$

$$K_{p2}=\frac{a/4}{\pi}=0.08a \text{ V/Rad}$$

K_{p1}: all 0's or 1's

K_{p2}: 10101 pattern



K_{p1} and K_{p2} indicate a 6db gain variation as a function of data pattern. This gain variation will result in only minor changes in the loop response during tracking.

The Voltage Controlled Oscillator

The VCO is constructed by employing a high frequency ECL oscillator in MC1648, in conjunction with a voltage controlled capacitor (varactor diode), and an inductor as the tank circuit. Because of its inherent high Q and spectral purity, this type of VCO is generally superior to a miltivibrator type. The schematic of the VCO is depicted in figure 3.23. Resistors R123 and R124 set up the DC bias for the anodes of varactors VC1 and VC2 while the control voltage V_c, maintains a more positive bias on the cathodes keeping them in reverse bias condition at all times. The

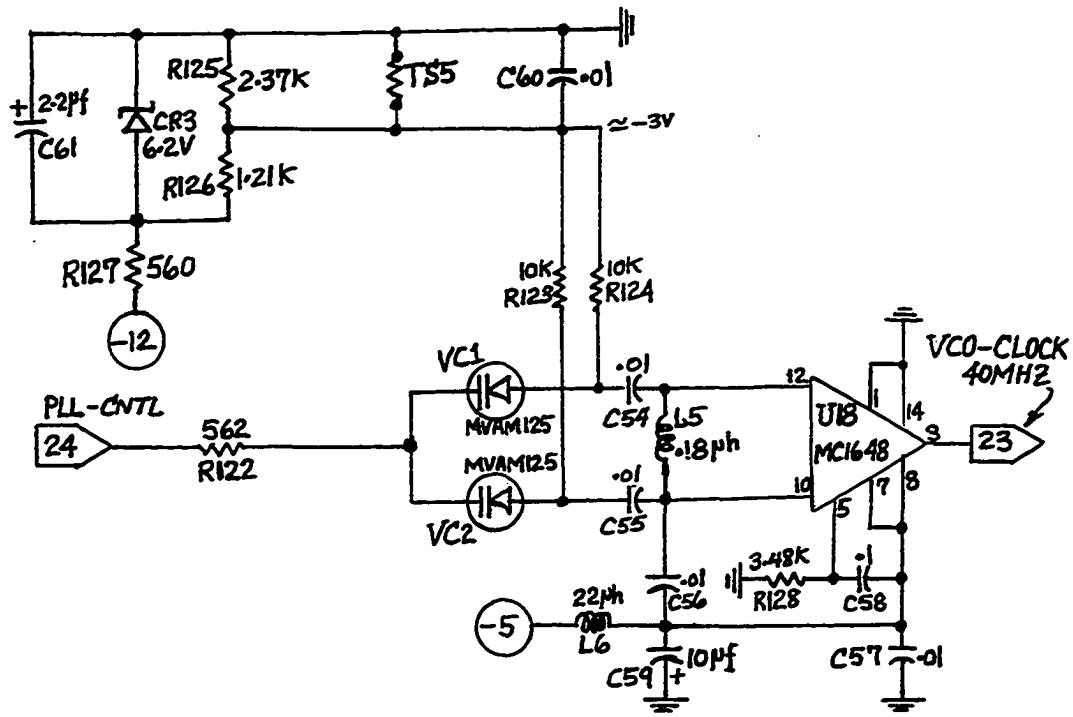


Figure 3.23 Schematic of the VCO

capacitance of the varactors which is a function of the reverse bias voltage, in conjunction with inductor L5 set-up the proper tank frequency for the oscillator U18. The resulting oscillator frequency is,

$$f=\frac{1}{2\pi\sqrt{L(C+C_s)}}$$

where, C_s=shunt capacitance, input and stray

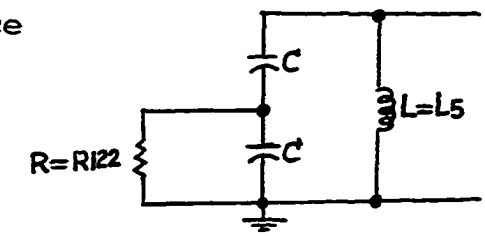
C =varactor capacitance

By observing that one side of the inductor L5 is "AC grounded" through C56 and that the control voltage V_c has negligible source impedance at the tank frequency, a tank equivalent circuit as viewed from the oscillator side may be drawn:

C=varactor capacitance

$$X_C=\frac{1}{\omega C}$$

$$X_{ceq}\cong\frac{RX_C}{R+X_C}$$



As viewed from the loop amplifier side, a single pole low pass filter comprised of R122 and C appears in the loop and is considered as part of the VCOs transfer function. With reference to the manufacturer's data for the varactor, the following values in the middle of the "linear range" are selected:

$$V_{R1}=-5V \longrightarrow C=195pF$$

$$V_{R_o}=-6V \longrightarrow C=160pF$$

$$V_{R2}=-7V \longrightarrow C=105pF$$

V_{R_o}=-6volts is the desired nominal reverse voltage selected to provide sufficient operating range for the varactors and the loop amplifier. The equivalent nominal varactor capacitance seen by the tank, at the desired tank frequency of 40mHz is calculated as follows:

$$X_C=\frac{1}{\omega C}=\frac{1}{2\pi(40x10^6)(160pF)}=25\Omega$$

$$X_{ceq}=\frac{RX_C}{R+X_C}=\frac{562(25)}{562+25}=23.9\Omega$$

$$X_{ct}=25+23.9=48.9\Omega$$

$$C_{eq}=\frac{1}{(48.9)(40x10^6)(2\pi)}=81.4pF$$

Assume C_s=6pF, Then $C_t=C_{eq}+C_s$=87.4pF

The value of the inductor L5 is calculated to be

$$L5=\frac{1}{C_t(2\pi f_o)^2}=\frac{1}{(87.4pF)(2\pi x40x10^6)^2}\simeq 0.18\mu H$$

Having calculated L5, the tank frequencies corresponding to V_{R1}, V_{R2}, and the VCO gain K_o are calculated:

V_{R1}=-5V C=195pF, X_c=20.4Ω

C_{eq}=99pF, C_t=105pF : f_1=36.6mHz

V_{R2}=-7V: C=105pF, X_c=37.9Ω

C_{eq}=54.5pF, C_t=60.5pF : f_2=48.2mHz

$$\frac{\Delta f}{\Delta V_R}=\frac{(48.8-37.1)mHz}{2V}=5.8mHz/V$$

$$K_o=2\pi\frac{\Delta f}{\Delta V_R}=3.66x10^7 \text{ Rad/V}$$

The VCO transfer function K_2 is,

$$K_2=\frac{K_o}{s}\left[\frac{1}{RCs+1}\right]=\frac{3.66x10^7}{s(4.46x10^{-8}s+1)}$$

Loop Amplifier and Filter

Loop amplifier and filter are required in order to sufficiently amplify the error signal and remove the undesirable sideband frequencies. In order to meet the requirement of negligible phase and frequency steady state errors, and maintain at least 50db of sideband rejection, a third order loop is considered. In conjunction with the third

order loop, a high speed and balanced loop amplifier is needed to minimize "dead-zone" and "feed-through". The schematic of figure 3.24 depicts the loop amplifier and filter.

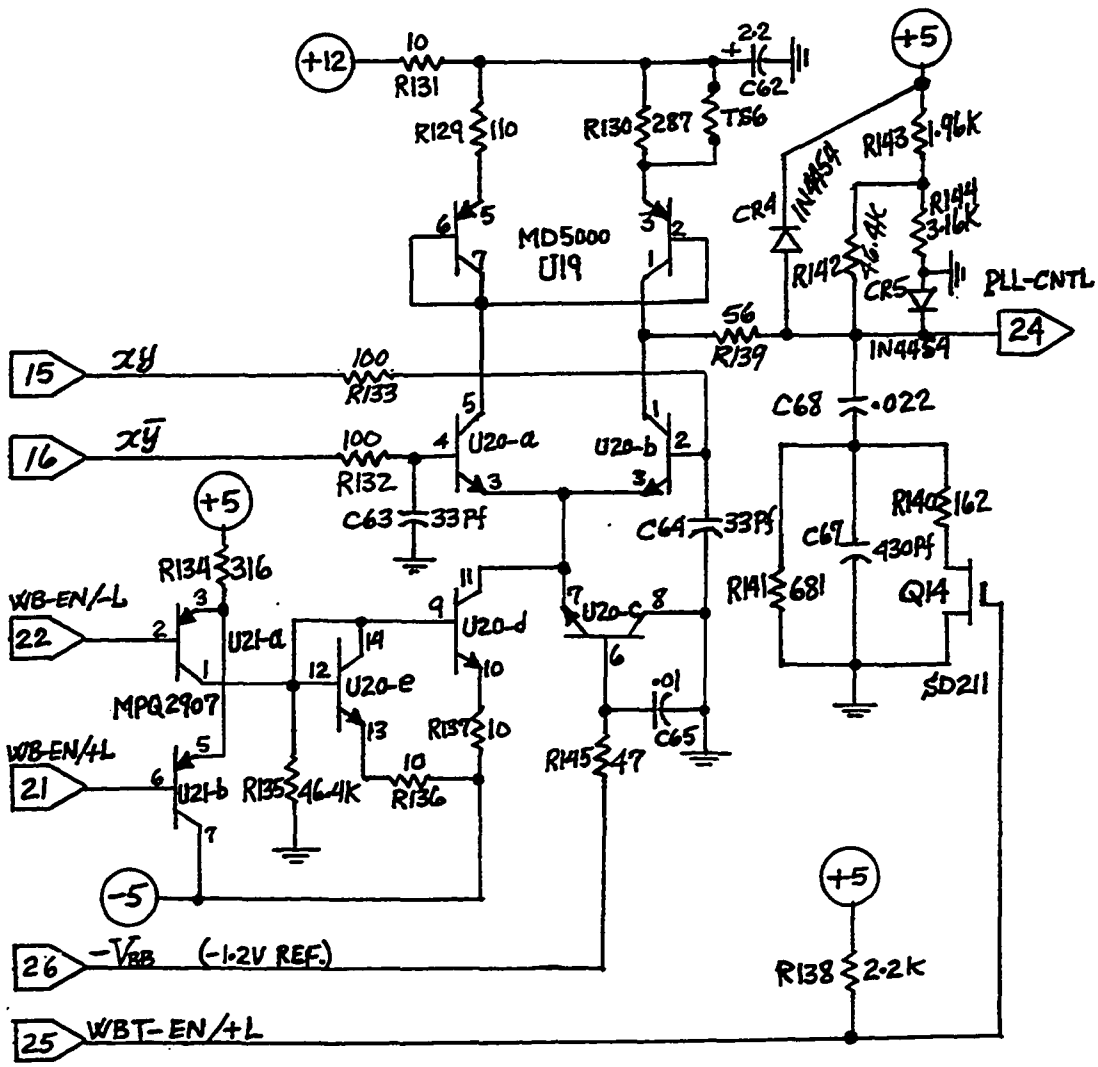


Figure 3.24 Schematic of the Loop Amplifier and Filter

The amplifier is a matched "current mirror" arrangement comprised of U19 and U20. When the loop is in lock, the phase detector outputs drive the bases of U20-a and b with alternating pulses which are in quadrature. Current I_o alternately charges and discharges the filter network which maintains the PLL-CNTL signal to a "DC" bias of approximately +3 volts. U20-c provides an ECL threshold for U20-a,b, while U20-e and R135 set up the quiescent current for U20-d. During lock up, U21-a increases the bias current in U20-d and at the same time Q14 and R140 modify the filter response, resulting in the "wideband" operation. R139 is provided to facilitate setting of the VCO's nominal frequency of 40mHz by disconnecting one side of it, and selecting TS5 of figure 3.23. Resistor TS6 is selected to split the detection window into two equal halves. This is accomplished by reading in a field of "all zeros" or "all ones" and selecting TS6 to yield a 25ns positive pulse at the phase detector output of U12-b.

PLL Loop Design

Linear techniques may be used to design the loop for predictable steady state and acceptable dynamic conditions. The loop is designed for both the wideband and the narrowband operating modes, using Bode plots and the Nichols chart. For a wideband mode, $t=10/\omega_n$ is used to insure settling to within ±1% of the final value during time t, where t is the settling time, and ω_n is the loop natural frequency.

Depending on the loop damping ζ, the loop natural frequency lies somewhere between the crossover frequency ω_{co} and the loop bandwidth ω_{-3db}. For Bode synthesis of higher order loops, it is more convenient to use ω_{co} instead of ω_n. Assuming $\omega_n \geq \omega_{co} = 3\text{x}10^6$, the maximum lock up time of 3.33 μSec provides sufficient margin for logic decoding time and circuit tolerances.

So far, the phase detector gain K_p, the scaler gain K_n, and the VCO transfer function K_2 have been determined. Loop synthesis begins as follows:

a. Draw the Bode plot for the combined transfer function $K_1 = K_2 \cdot K_n$

b. Superimpose on (a), the combined transfer function for the phase detector K_p, the loop amplifier A_I, and the filter K_f, which yields the desired overall response.

c. Determine DC gain for A_I, and calculate component values for K_f by equating like coefficients.

In figure 3.25 the magnitude and phase responses for the wideband mode are plotted. The phase response is calculated by superimposing all the "lead" and "lag" phase shifts in addition to the phase shift due to the Nyquist rate:

$$\Phi_{WB} = \left\{ -90 - \tan^{-1}\frac{\omega}{1.5\text{x}10^7} - \tan^{-1}\frac{\omega}{2.24\text{x}10^7} - \tan^{-1}\frac{\omega}{3.03\text{x}10^8} - \tan^{-1}\frac{\omega}{1\text{x}10^3} + \tan^{-1}\frac{\omega}{3\text{x}10^5} - 180\,\frac{\omega}{6.28\text{x}10^7} \right\}$$

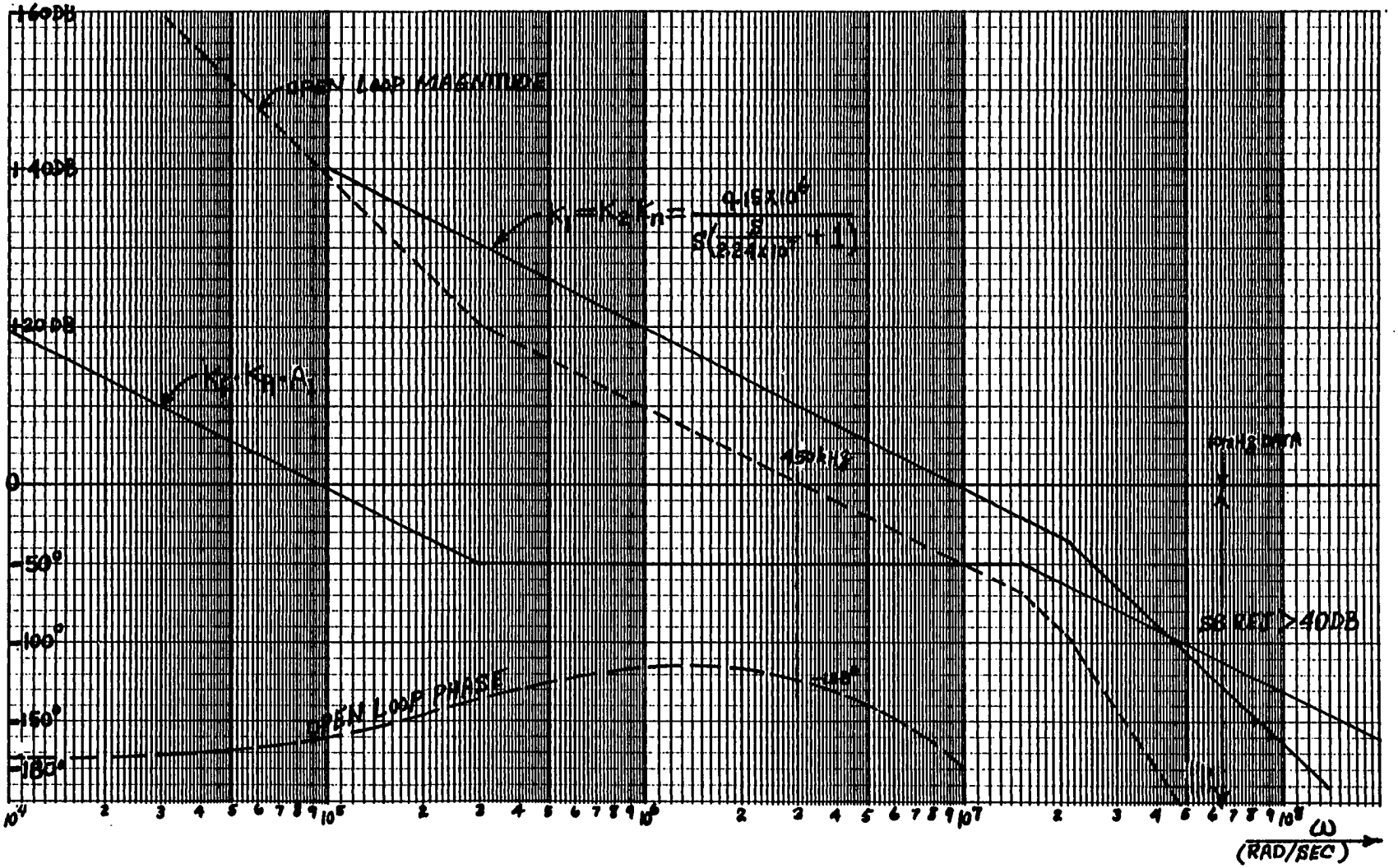
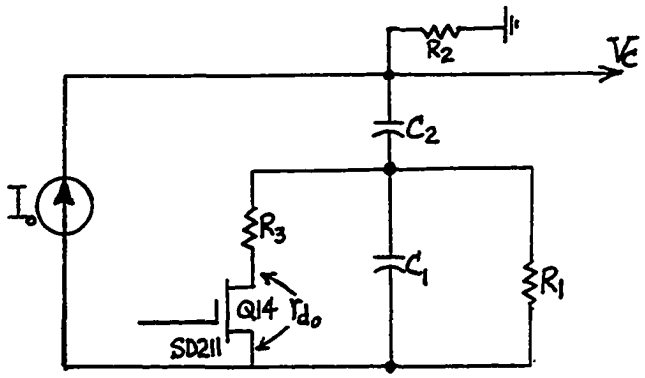


Figure 3.25 Magnitude and Phase Plots of the Wideband Loop

At $\omega_{co}=3x10^6$, $\Phi_{WB}=-123^o$ provides a stable phase margin, and less than 0.8db of peaking throughout the closed loop transfer function. The filter equivalent circuit and its transfer function K_f are shown in figure 3.26. From the magnitude plot, the required DC gain of 40db is used to determine the wideband current $I_o(WB)$ as follows:

$$40db \rightarrow 100=K_p \cdot A_I \cdot R_2=(0.16)I_o(WB)\cdot R_2$$

$$\text{let } R_2=46.4K \rightarrow I_o(WB)=13.5mA$$



$$K_f = \frac{R_2\left[1+R_x(C_1+C_2)s\right]}{1+s\left[R_x(C_1+C_2)+R_2C_2\right]+s^2R_xR_2C_1C_2}$$

$$R_x=\frac{R_1(R_3+r_{d_o})}{R_1+R_3+r_{d_o}} \quad , \; r_{d_o}=\text{FET "ON" Resistance} \simeq 32\Omega$$

Figure 3.26 Filter Equivalent Circuit and Transfer Function

All other filter component values are determined by equating like coefficients of K_f and that of the synthesized filter plot of figure 3.25 as shown below:

$$\left[\frac{K_f}{R_2}\right]_{WB} = \frac{1+R_x(C_1+C_2)s}{1+s\left[R_x(C_1+C_2)+R_2C_2\right]+s^2R_xR_2C_1C_2}$$

$$= \frac{1+3.33\times10^{-6}s}{(1+10^{-3}s)(1+6.67\times10^{-8}s)} = \frac{1+3.33\times10^{-6}s}{(1+1\times10^{-3}s+6.67\times10^{-11}s^2)}$$

$$\left.\begin{aligned} R_x(C_1+C_2)&=3.33\times10^{-6} \\ R_x(C_1+C_2)+R_2C_2&=10^{-3} \end{aligned}\right\} R_2C_2=10^{-3}-3.33\times10^{-6}=9.97\times10^{-4}$$

$$C_2=\frac{9.97\times10^{-4}}{46.4K}\simeq\underline{0.022uF}$$

$$\text{for } C_2\gg C_1, R_x\simeq\frac{3.33\times10^{-6}}{C_2}=\underline{151\Omega}$$

$$R_xR_2C_1C_2=6.67\times10^{-11}\rightarrow R_xC_1=6.53\times10^{-8}$$

$$C_1=\frac{6.53\times10^{-8}}{151}=\underline{430pF}$$

The narrow band loop is designed to provide sufficient rejection of the sideband and noise induced signal jitter, while providing sufficient signal tracking. A crossover frequency of 100kHz ($\omega_{co}=6.28\times10^5$) results in a good compromise. By following a similar procedure as described for the wideband mode, the magnitude and phase responses for the narrowband mode are plotted in figure 3.27. The DC gain of 13db is used to determine narrow-band value of I_o(NB):

$$I_o(NB)=\frac{4.47}{(0.16)(46.4K)}=96.3\mu A$$

Both I_o(WB) and I_o(NB) are used to calculate values of the current setting resistors R134 and R135 in figure 3.24. From figure 3.27, the narrow-band phase response may be

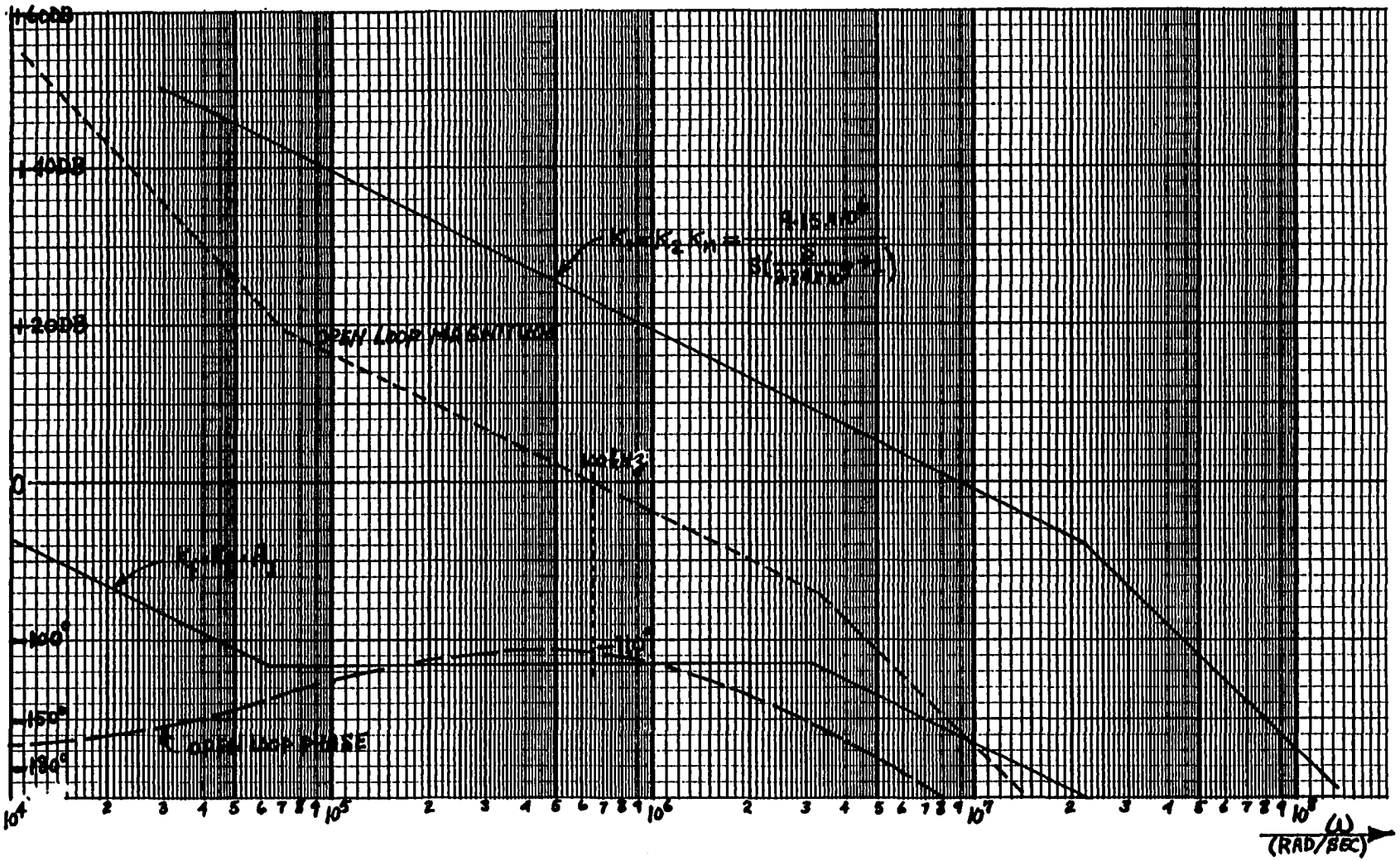


Figure 3.27 Magnitude and Phase Plots of the Narrow-Band Loop

written:

$$\Phi_{NB}=\left\{-90-\tan^{-1}\frac{\omega}{3.33\times10^{6}}-\tan^{-1}\frac{\omega}{2.24\times10^{7}}-\tan^{-1}\frac{\omega}{6.28\times10^{7}}\right.$$
$$\left.-\tan^{-1}\frac{\omega}{1\times10^{3}}+\tan^{-1}\frac{\omega}{6.67\times10^{4}}-180\,\frac{\omega}{6.28\times10^{7}}\right\}$$

At $\omega_{co}=6.28\times10^{5}$, $\Phi_{NB}=-110^{\circ}$ provides the damping needed for good signal tracking. By equating like coefficients, again the filter values are calculated, this time yielding the values for R1 and R3 of figure 3.26:

$$\left[\frac{K_f}{R_2}\right]_{NB}=\frac{1+1.5\times10^{-5}s}{(1+10^{-3}s)(1+3\times10^{-7}s)}=\frac{1+1.5\times10^{-5}s}{(1+10^{-3}s+3\times10^{-10}s^{2})}$$

$$\left.\begin{aligned}R_1(C_1+C_2)&=1.5\times10^{-5}\\ R_1(C_1+C_2)+R_2C_2&=10^{-3}\end{aligned}\right\}R_2C_2=10^{-3}-1.5\times10^{-5}=9.85\times10^{-4}$$

$$C_2\simeq0.022\mu F$$

$$\text{for } C_2\gg C_1,\ R_1\simeq1.5\times10^{-5}/C_2=669\Omega$$

$$\text{let } \underline{R_1=681\Omega}$$

$$R_3+r_{d_o}=\frac{R_x.R_1}{R_1-R_x}=\frac{151(681)}{681-151}=194\Omega$$

$$R_3=194-32=\underline{162\Omega}$$

Using the Nichols chart and the open loop magnitude and phase plots, the closed loop responses for the wideband and the narrow-band cases are plotted in figure 3.28.

Design of the Integrate and Dump Matched Filter

Having established a phase coherent reference for the data, the next step is to implement the I&D Matched Filter in such a way that timing accuracy is not compromised.

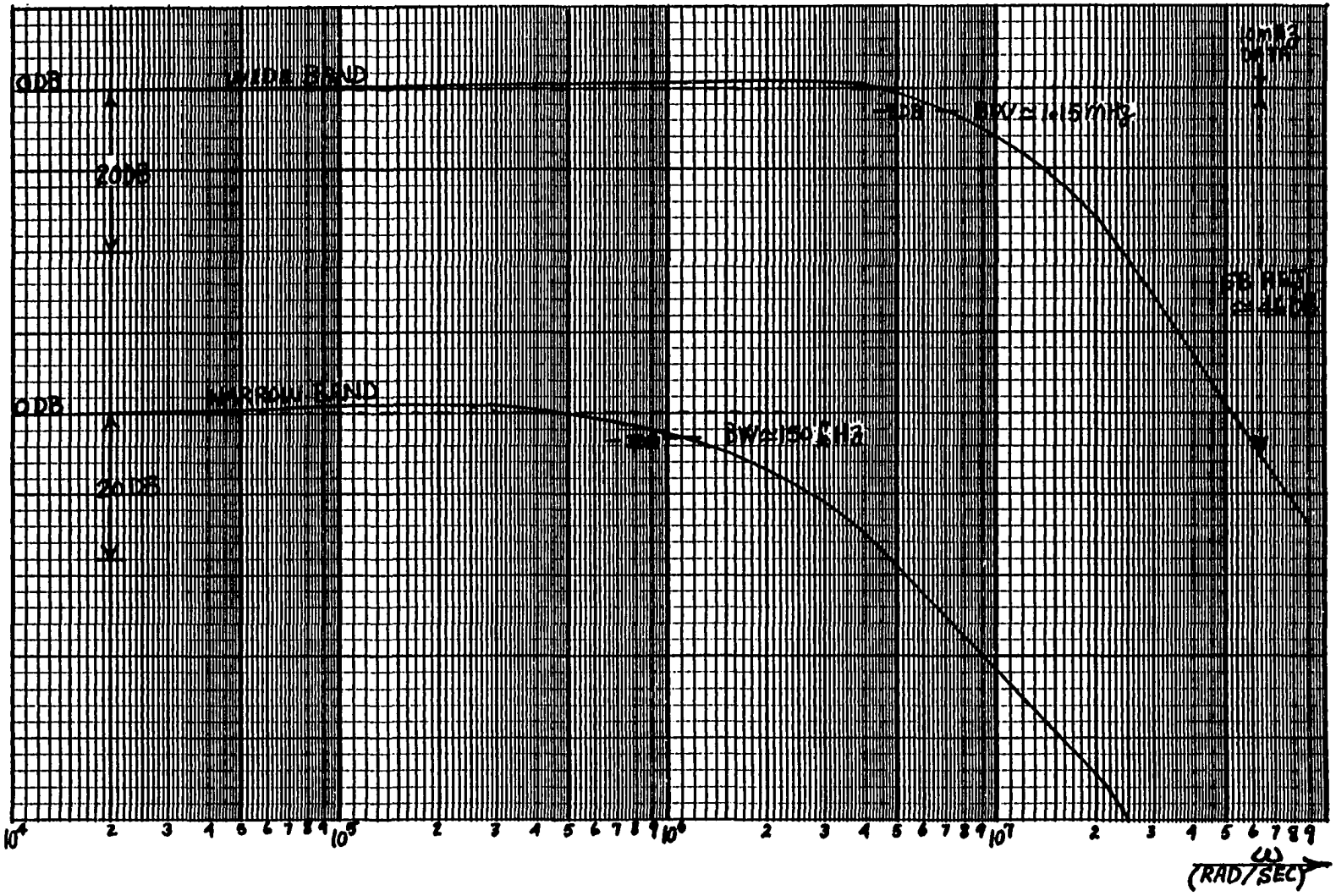


Figure 3.28 PLL Closed Loop Response

The circuit implementation is accomplished by utilizing the same types of high speed matched transistor arrays that were used for the PLL loop amplifier. Schematic representation of the I&D is shown in figure 3.29 and a representative signal timing is given in figure 3.30. The zero crossing detector of figure 3.15 drives two identical I&D circuits, each of which is used to process the data during the specific phase of the clock. Since the operation of the two circuits are similar, only one of them is discussed.

During the time that TΦA-Clock is "high", discharge (Dump) transistors U22 are in cutoff, and simultaneously the quiescent current of $I_o \simeq$ 2.9mA is established. The differential pair U22-a,b guided by the data polarity from the zero crossing detector, alternately steer the current I_o, charging capacitor C71 or C72. As soon as TΦA-Clock goes "low", the current source U22-c is disabled and simultaneously capacitors C71 and C72 are discharged to approximately the emitter voltage of U22 which is at +0.7 volts. The bases of U22-a,b are biased at -3.4 volts and swing from -2.9 volts to -3.9 volts in order to keep them out of saturation. The values for the integrating capacitors C71 and C72 are calculated by allowing sufficient reverse bias operating voltage for the base-collector junctions of the differential pair. Assuming the reverse bias voltage is 1.8 volts, the minimum allowable collector voltage for U22 is, -2.9V+1.8V=-1.1volts. The capacitance is then calculated as a function of the constant current I_o and the

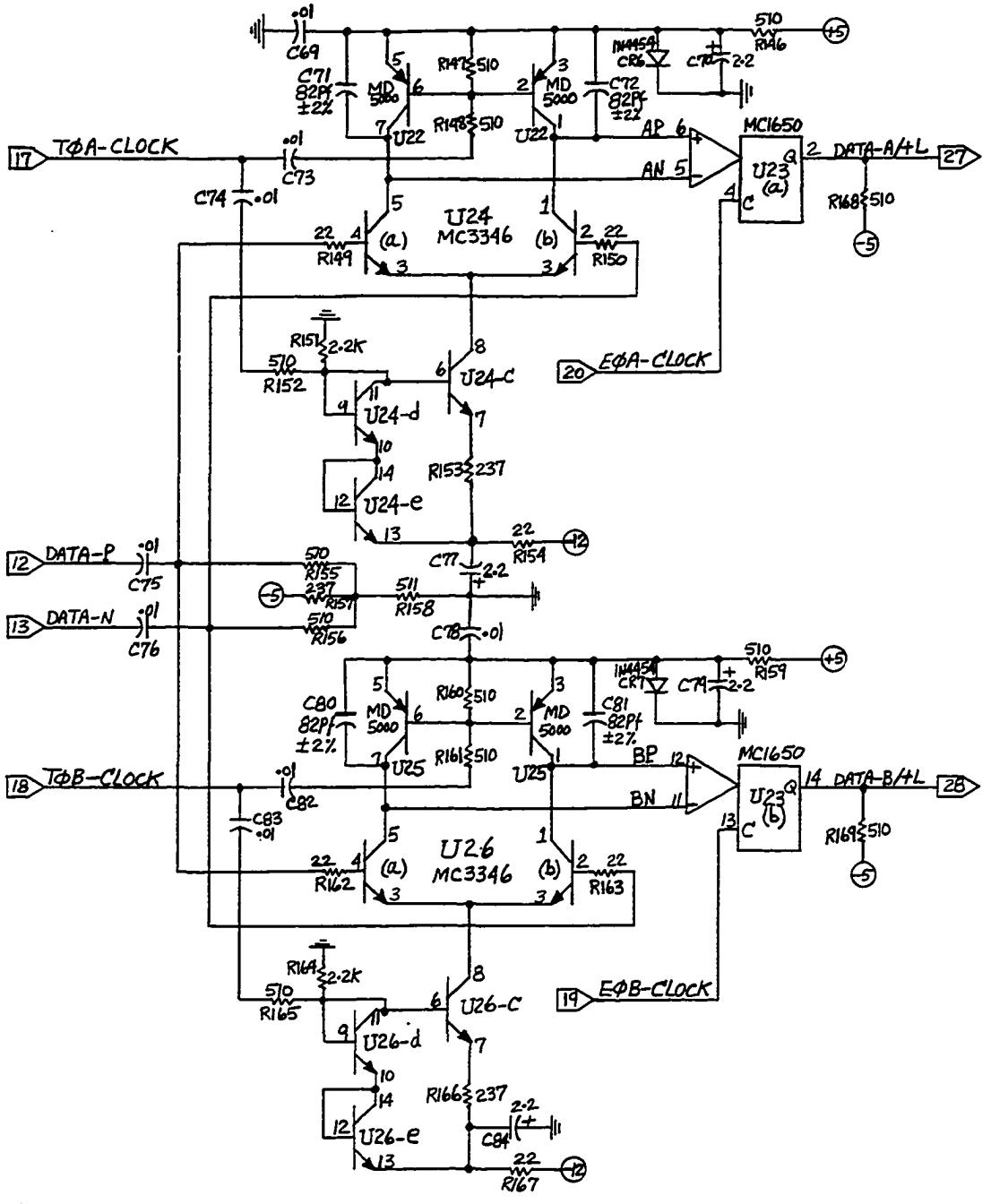


Figure 3.29 I&D Circuit Schematic

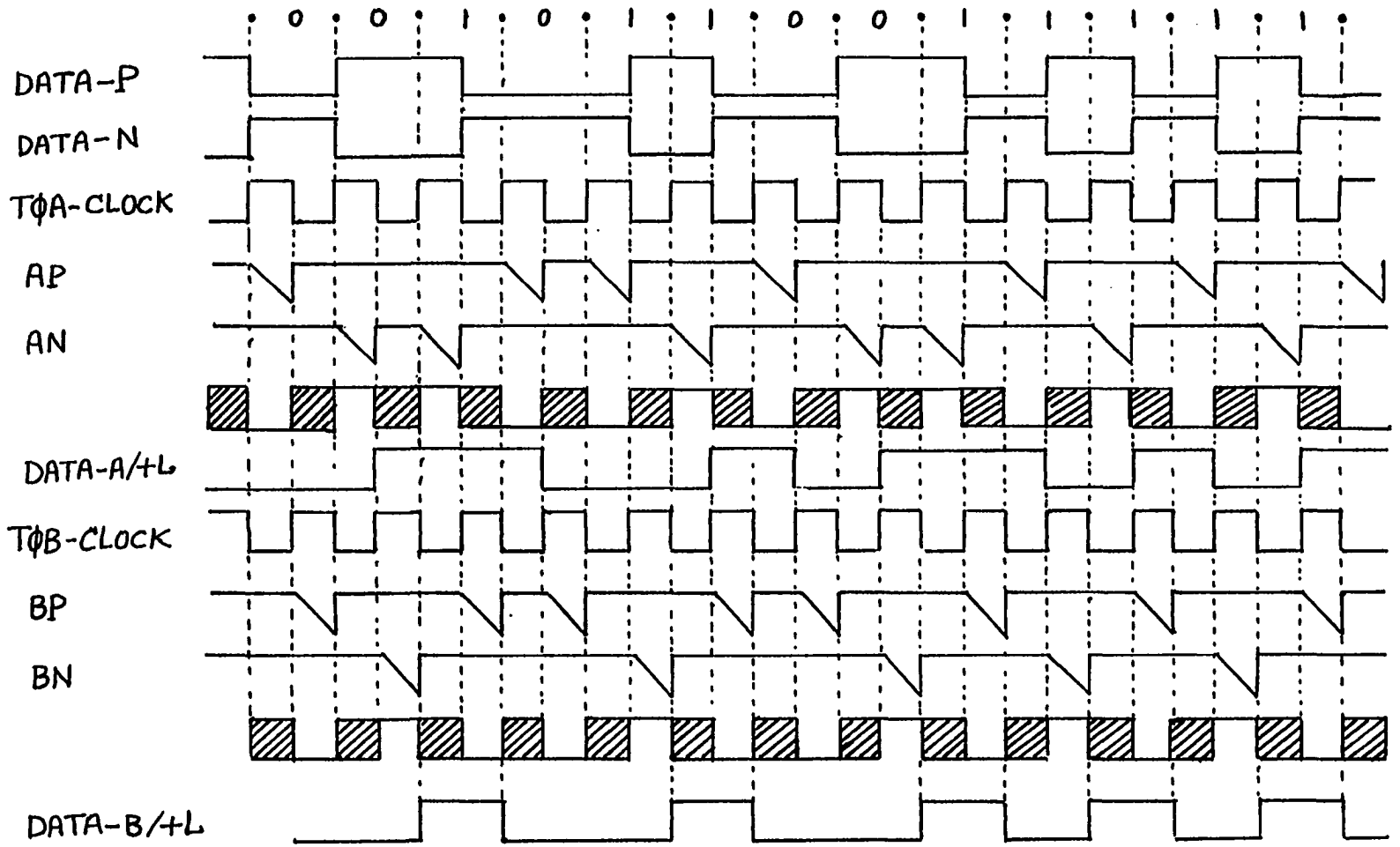


Figure 3.30 Timing Diagram for the I&D Filters

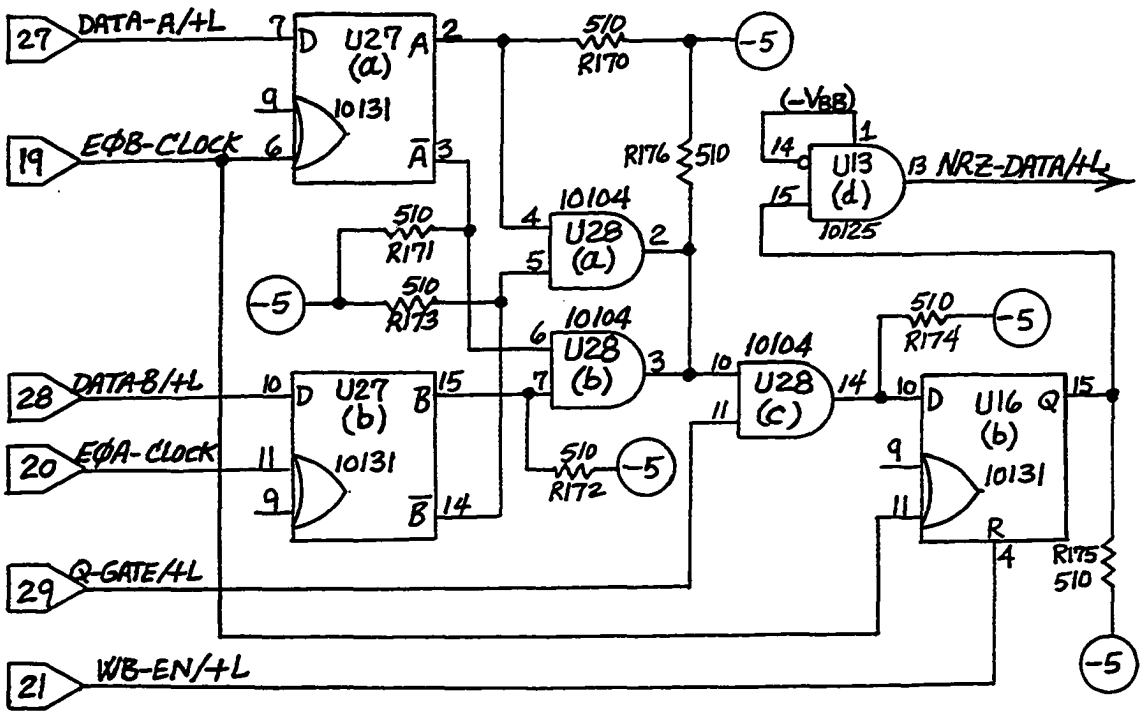
charge time of 50ns as follows:

$$C=\frac{I_o \cdot \Delta t}{\Delta V}=\frac{(2.9\text{x}10^{-3})(50\text{x}10^{-9})}{(1.1+0.7)}\simeq 82\text{pF}$$

An inherent property of this I&D circuit is its charge "hold" ability which occurs when the data changes polarity during the time that the TΦA-Clock is high. This property facilitates conversion to a representative digital signal DATA-A/+L, which is generated by comparing the two integrated signals "AP" and "AN" and sampling the result at the end of each clock interval. The alternate clock phase, TΦB-Clock, and the associated circuits generate DATA-B/+L signal in a similar manner.

The Decoder Design

Before attempting the MFM to NRZ decoding, the digitized outputs of the I&D filters must be converted to qualified flux reversal representations. This is accomplished by "re-timing" the signals with the appropriate clock phases, "exclusive ORing" the re-timed signals, and then by "ANDing" the result with the delayed qualifying signal of figure 3.19. The signal thus generated becomes a generalized "recovered" signal which may be decoded into NRZ data from any previously encoded data. The decoding for this design however, is from MFM to NRZ. The logic schematic of the Data Recovery and the Decoder, and a representative timing are given in figure 3.31. The MFM to NRZ decoding is simply accomplished by reclocking the recovered data in



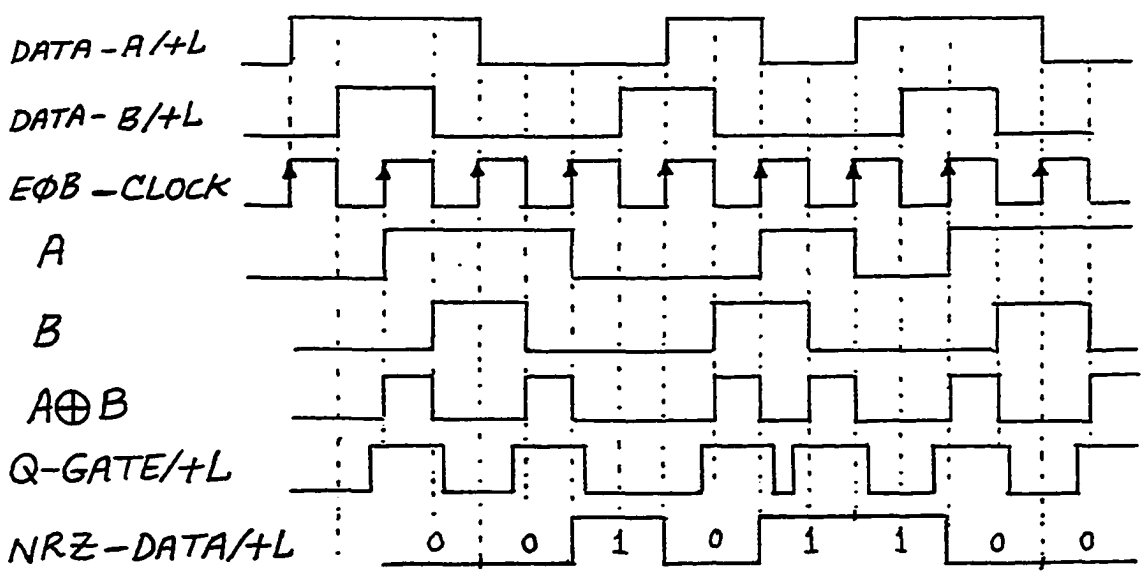


Figure 3.31 MFM to NRZ Decoder and Timing Diagram

flip-flop U16-b, using the rising edge of the EΦA-Clock which was appropriately phased in the field of all 0'S.

Summary

A rather detailed and systematic design procedure with emphesis on preservation of phase linearity and accurate timing has been presented. It was demonstrated that a straightforward circuit implementation of the equalizer minimizes signal parameter variations and reduces peak shift, for the general case, to within ±9ns, which is less than one half of the available detection window of ±25ns. A linear phase low-pass filter and lattice phase compensator were used to attenuate high frequency noise and maintain phase linearity in the "high resolution" channel. Additionally, a qualifying channel was designed to "gate out" the unwanted pulses generated by the high resolution channel, producing amplitude-qualified pulse-per-transition for the PLL. By employing linear techniques, the AGC and the PLL feedback loops were synthesized for stability and acceptable static and dynamic response. The"I&D Matched Filter" was implemented employing matched transistor arrays in order to minimize circuit tolerances and take full advantage of the filter's noise rejection capability. Finally, the design of the recovery logic for the generalized case, and the specific decoder logic for the MFM to NRZ case were presented.

CHAPTER IV

PARTIALLY UNCORRELATED CHANNELS

Introduction

Numerous theoretical formulations for determining error probabilities as a function of S/N may be found in the literature. In the first part of this chapter, a direct approach for allocation of error budgets and estimation of error rate performance as a function of the Effective Signal to Noise Ratio ES/N, the Theoretical Detection Window TDW, and the Available Detection Window ADW, is presented. The remainder of this chapter is dedicated to the introduction of a three-channel majority decode system, and the discussion of the channels' specific characteristics which make them partially uncorrelated.

The Detection Window and the Error Budgets

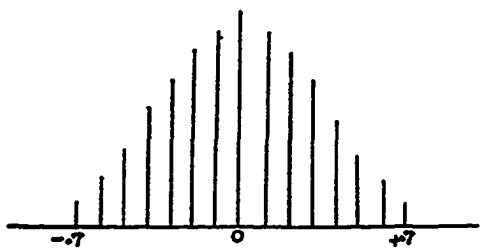
A sequence of previously recorded flux transitions reproduced from a rotating magnetic medium, may be decoded into a binary sequence by use of a phase coherent reference clock derived from a phase-locked-loop. The indexing in time, generated by the coherent decoding clock, may be viewed as the Theoretical Detection Window (TDW) during

which time the presence of a transition may be interpreted as a "1" and the absence of a transition as a "0". Two major factors which influence the position of a transition with respect to the center of the TDW are, the peak shift due to pulse crowding, and the ES/N. By specifying or measuring the magnetic response (PW_{50}), the degree of peak shift due to pulse crowding for various patterns may be accurately determined. A peak shift distribution is a histogram of the peak positions, with the abscissa representing the position in the TDW, and the ordinate representing the number of pulse peaks occuring at any given TDW position. It is generally sufficient to determine the maximum peak shift induced by the "worst case" pattern, however, knowledge of the histogram is beneficial and in some cases points out design anomalies such as phase distortion and improper write pre-compensation. Three typical histograms are shown in figure 4.1. The uncompensated histogram of figure 4.1-a spreads to ±70% of the TDW, with a Gaussian distributed pattern sensitivity. Both the write pre-compensated and the equalized cases however, modify the distribution and reduce the spread significantly, allowing more Available Detection Window (ADW) for the noise induced peak shifts.

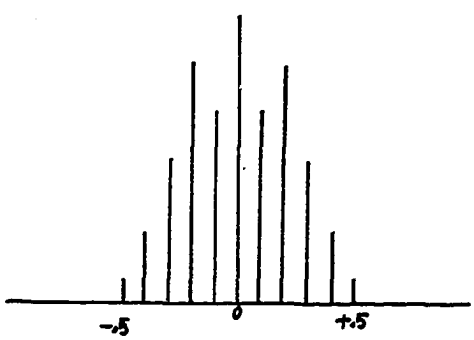
The peak shift induced due to noise (42) may be represented by

$$\frac{d}{dt}\left[s(t_o+\Delta t)+n(t)\right] \qquad (4\text{-}1)$$

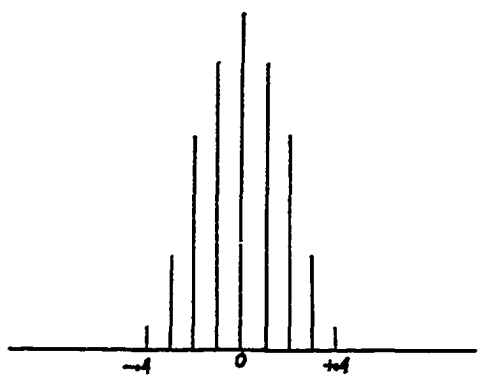
where s(t) is the signal waveform, t_o is the unperturbed peak position, Δt is the peak shift, and n(t) is the noise voltage as a function of time.



a- Without Pre-Compensation or Equalization



b- Pre-Compensated



c- Equalized

Figure 4.1 Typical Peak Shift Histograms

An expansion of s(t) in the Taylor series about t_o yields, to the first order, the peak shift which is $|\Delta t| = n'(t_o)/S''_i$, where $n'(t_o)$ is the rms noise voltage measured after differentiation and includes the net effect of all filters and signal processing elements. S''_i, is the second derivative

of the signal at the ith pulse. A plot of a large population of S_i'' 's yields the probability density function (p.d.f) of the peak shift in presence of noise. A typical overall p.d.f may be constructed by normalizing the noise p.d.f about the worst case peak shift as determined from the peak shift histogram. Figure 4.2 depicts a typical p.d.f for the case of the equalized histogram in presence of Gaussian noise.

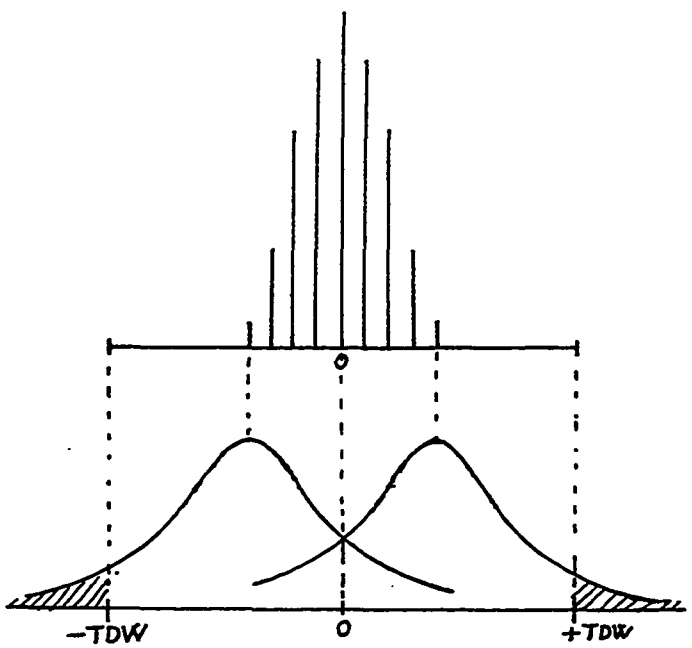


Figure 4.2 Typical p.d.f for the Equalized Histogram

The error probability is the area under the p.d.f curve that falls beyond the ±TDW as follows.

$$E=\int_{+TDW}^{+\infty} P(t)dt+\int_{-\infty}^{-TDW} P(t)dt \qquad (4-2)$$

For the case of the "worst case" peak shift pattern, it may

be shown that,

$$P(t)=\frac{1}{2}\left\{\exp\left[-(t-T_1)^2/2T_2^2\right]+\exp\left[-(t+T_1)^2/2T_2^2\right]\right\} \qquad (4\text{-}3)$$

where T_1 is the worst case peak shift due to pulse crowding, and T_2 is the rms value for the noise-induced peak shift. Assuming a Gaussian distributed noise as the special case, the integral of the p.d.f yields,

$$E=\text{Error-Rate}=\frac{1}{2}\left\{\operatorname{erf}\left[(TDW+T_1)/T_2\right]+\operatorname{erf}\left[(TDW-T_1)/T_2\right]\right\} \qquad (4\text{-}4)$$

A typical error-rate curve as a function of the TDW is shown in figure 4.3. The form of the error-rate curve for

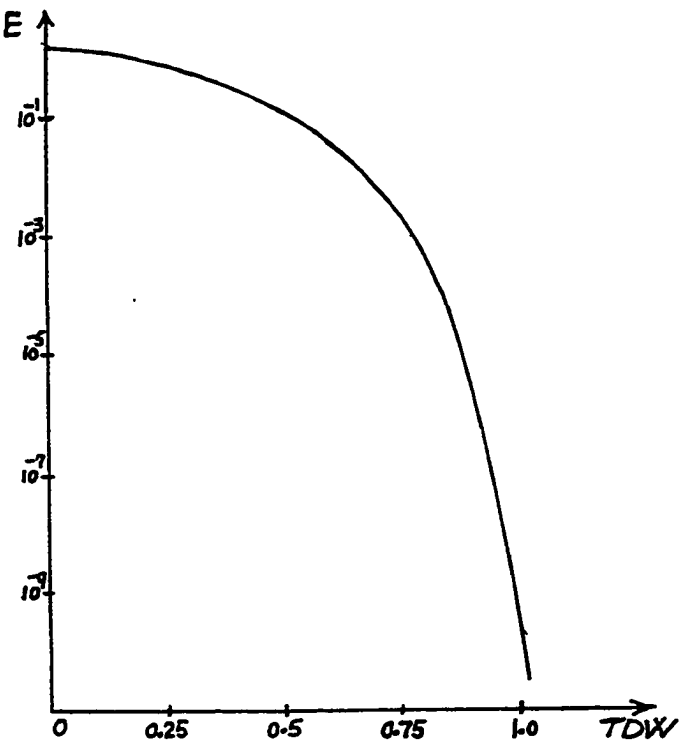


Figure 4.3 Error-Rate Curve for Specific Values of T_1 & T_2

a specific magnetic recording system may be determined by narrowing an adjustable detection window, and measuring T_1 and T_2 at several reduced positions of the TDW. The measured values for T_1, T_2, and the full TDW available for the code may be substituted into equation (4-4) to calculate the expected error-rate. In practice, additional margins must be allocated to account for volume production and parameter variations introduced due to the large quantities of heads and media. It is a generally accepted "rule of thumb" to achieve an error-rate of at least one order of magnitude better at the "spin-stand" level.

An alternative approach which complements the method just discussed is to formulate a direct approach based on the history of error tests and the statistics which have been accumulated on a variety of similar devices. In this case, the ES/N and the ADW are the two major factors in determining the expected error-rate. The ES/N includes the net effect of the magnetic channel, adjacent track interference, circuit, and signal processing elements prior to the zero crossing detector. Where a second qualifier channel is used, the rms value of the two channels is taken as the ES/N. The ADW is calculated by subtracting the total "error budget" from the TDW. The significant elements that deserve error budget allocation are as follows:

Peak Shift. Peak shift induced by intersymbol interference is by far the major factor which reduces the

ADW. As discussed earlier, the maximum peak shift for the system may be accurately determined, and may be reduced significantly through equalization, but at a loss in ES/N. The improvement in the ADW however, results in an improved error-rate only for a large (>15db) initial value of S/N.

Phase Distortion. The importance of phase linearity is well justified, since any delay distortion in the passband results in a corresponding degree of peak uncertainty and hence reduces the ADW.

Overwrite. Every time the pre-recorded data is overwritten, a certain amount of residual noise due to lack of perfect overwrite remains. This "signal like" noise is a function of the magnetic circuit loop which is comprised of the head and the recording medium.

Write Driver Asymmetry. A certain amount of switching time-asymmetry is generally induced by the Write Driver due to differences in the circuits' rise and fall times and the stray capacitance. Extreme care in the design is needed to control the asymmetry to within $\pm$0.5NS.

PLL Jitter. The PLL is always subject to some degree of jitter either due to signal induced noise, or due to environmental noise. By selecting proper circuit components and designing a stable and "narrow-band"

tracking loop, the noise induced jitter is minimized.

For the design given in chapter III, the loss in S/N predominantly due to the equalizer results in ES/N=24-5=19db. The total error budget (TEB) is ±12ns and is allocated as follows:

Peak Shift	= ±9ns
Phase Distortion	= ±1ns
Overwrite	= ±1ns
Write Driver	= ±0.5ns
PLL Jitter	= ±0.5ns

For the MFM code at a data transfer rate of 10Mbits/Sec, the ADW is calculated as follows:

$$ADW=TDW-TEB=\pm 25-(\pm 12NS)=\pm 13ns$$

Several error-rate graphs as a function of the ES/N and the normalized ADW, based on long term error-rate history on similar devices, have been gererated and are shown in figure 4.4. With reference to figure 4.4, the expected error-rate for ADW/TDW=0.52 and ES/N=19db is approximately 0.2×10^{-10}. Comparatively, the expected error-rate for ES/N=24db and ADW/TDW=0.3, without equalization or the I&D filters, would be about an order of magnitude more. It is cautioned that, usually the least known and the least controllable factor which may adversely affect error-rate performance is the impact of defects in the media. For this reason, it is more systematic to allocate reasonable but tight error budgets to all other significant factors, allocating the remaining

ADW for the "soft" media defects. Imperfections in the recording medium that cause the recoverable "drop-in" or "drop-out" errors, are considered "soft". The choice of a magnetic recording code and the specific detection channel may significantly improve the recoverable error-rate in the presence of media noise. The I&D matched filter, through its inherent averaging property, increases channel tolerance to media induced soft errors.

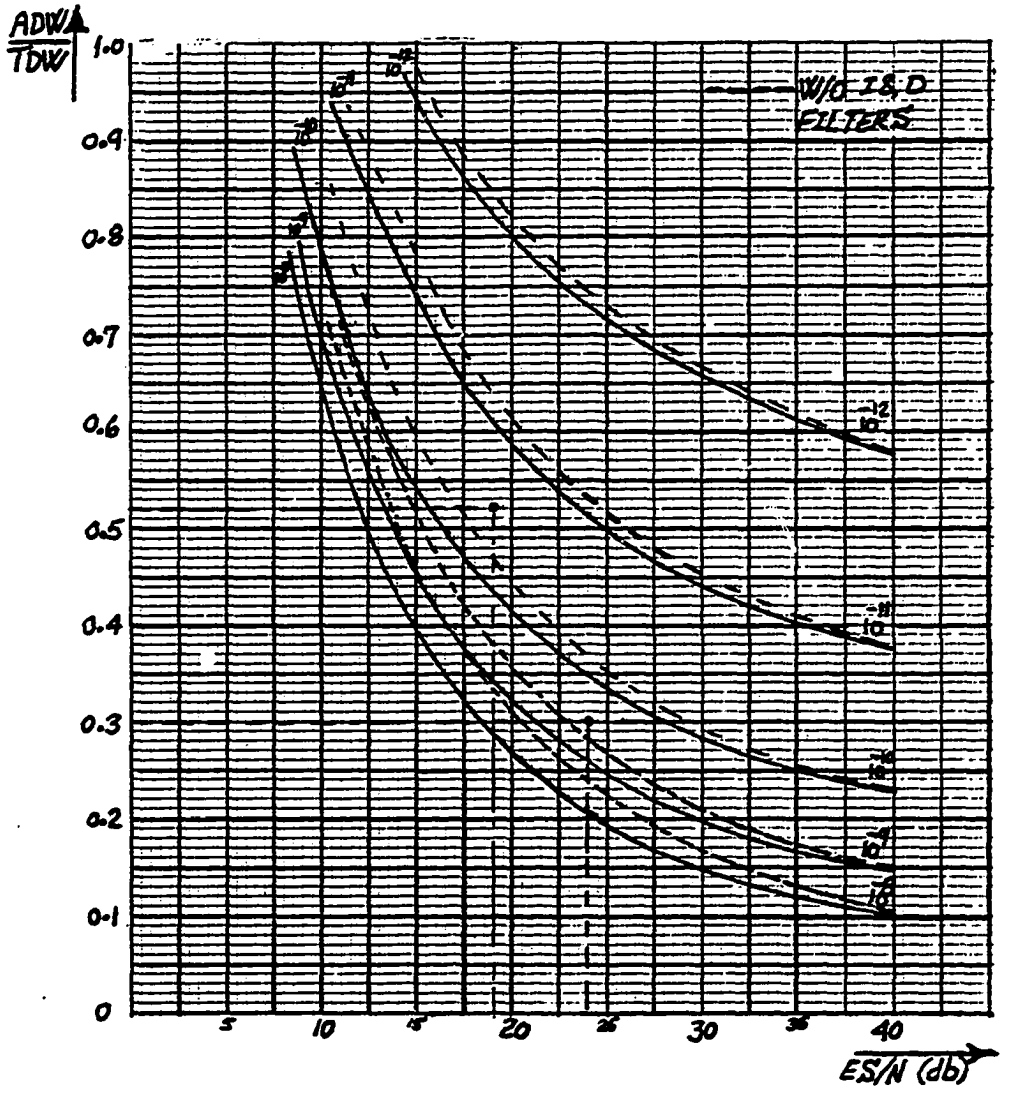


Figure 4.4 Error-Rate Curves Based on Long Term History

Comparisons of Channel Characteristics

For relatively high S/N(>15db), a single channel detection system may be designed to provide an acceptable error-rate. As the S/N is deteriorated significantly, due to large increases in the recording density, an alternative approach deserves consideration. In radar and space communications, the evolution of new techniques for improving performance with emphasis on increased data rate, at a fixed level of error performance, continues. Some of these techniques may be adapted to high density magnetic recording. One such technique is a multiple channel correlation detector.

In this section, a three-channel real time correlation detector which is adaptable to high density magnetic recording is introduced. Follow-up design and further investigations are recommended for future work. As depicted in the major block diagram of figure 4.5, the reproduce sig-

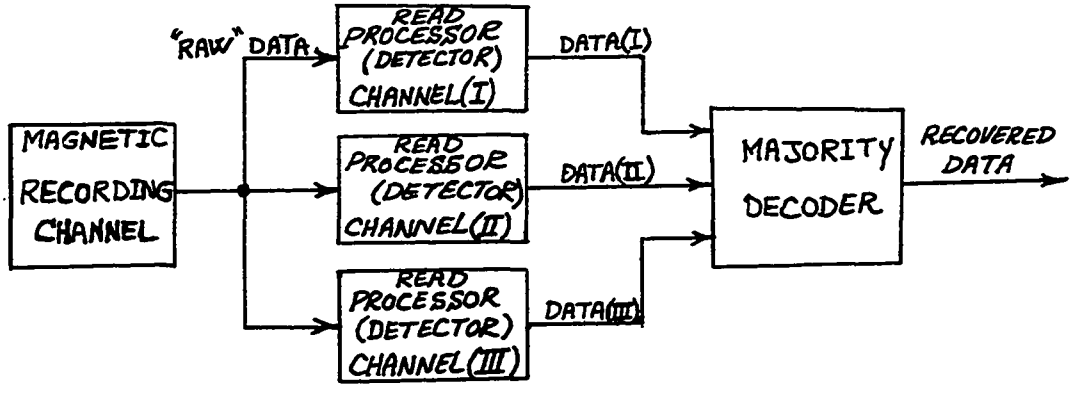


Figure 4.5 Major Block Diagram of a Three-Channel Correlation Detector

nal from the recording channel may be processed in parallel by three different channels, each of which has certain favorable characteristics. The three recovered signals are then majority decoded at each "window" interval. The degree of improvement expected from such a system, is directly a function of the degree of uncorrelatedness among the three channels. Needless to say, the uncorrelatedness should be achieved without the introduction of any significant detection deficiencies, or the resultant error-rate may deteriorate to even below that of an "optimum" single channel detector.

From a theroretical point of view, suppose that a signal from an ergodic and stationary random process having a power-density spectrum $S_x(f)$, is applied to two different filters as shown in figure 4.6. The input-output relation-

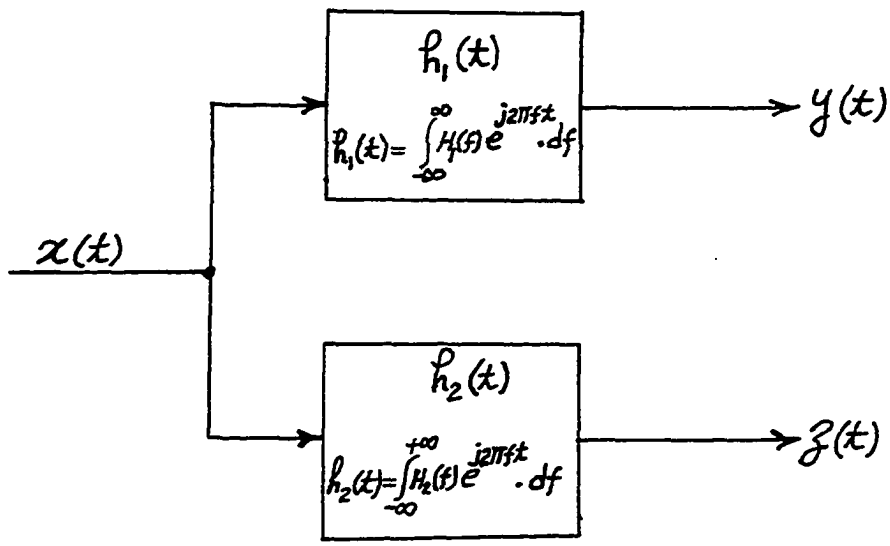


Figure 4.6 Two Signals Derived From a Common Source

ship for the two linear filters with transfer functions $H_1(f)$ and $H_2(f)$, and corresponding unit impulse response $h_1(t)$ and $h_2(t)$ are,

$$S_y(f)=\left|H_1(f)\right|^2.S_x(f)$$
$$S_z(f)=\left|H_2(f)\right|^2.S_x(f)$$

Assuming that y(t) and z(t) have zero means, we can write the cross covariance function as,

$$\rho_{yz}(\tau)=\frac{R_{yz}(\tau)}{\sigma_y.\sigma_z}$$
$$=\frac{1}{\sigma_y.\sigma_z}\int_{-\infty}^{+\infty}h_1(u)du\cdot\int_{-\infty}^{+\infty}h_2(v)dv\cdot R_x(\tau+u-v)$$

where $R_{yz}(\tau)$= cross-correlation function,

and $R_x(\tau)$ = input autocorrelation function

In terms of the input power density spectrum,

$$\rho_{yz}(\tau)=\frac{1}{\sigma_y\cdot\sigma_z}\int_{-\infty}^{+\infty}h_1(u)e^{j2\pi fu}du\cdot\int_{-\infty}^{+\infty}h_2(v)e^{-j2\pi fv}dv$$
$$\cdot S_x(f)e^{j2\pi f\tau}df$$

Since the first two integrals in the above expression are the transfer functions of the filters, it follows that,

$$\rho_{yz}(\tau)=\frac{1}{\sigma_y\sigma_z}\int_{-\infty}^{+\infty}H_1^*(f)\cdot H_2(f)\cdot S_x(f)e^{j2\pi f\tau}df$$

The output signals are uncorrelated for all values of τ only if $H_1(f)$ and $H_2(f)$ do not overlap. If there is overlap, the signals can still be uncorrelated for particular values of τ, depending upon the form of the function $\rho_{yz}(\tau)$. The foregoing may be extended to include a third channel

with its filter response as $h_3(t)$.

For three completely independent channels, each having an error-rate E, the resultant majority vote error-rate MVE, would be, $MVE=3P^2-2P^3$. It should be cautioned that complete independence among the channels may be viewed as a theoretical upper limit which is not realizable. In figure 4.7, the expected operating region for a three channel system is shown. To aid in the prediction of error-rates as a function of correlation coefficient and S/N, a Monte-Carlo Model (39,40) was constructed. The model in-

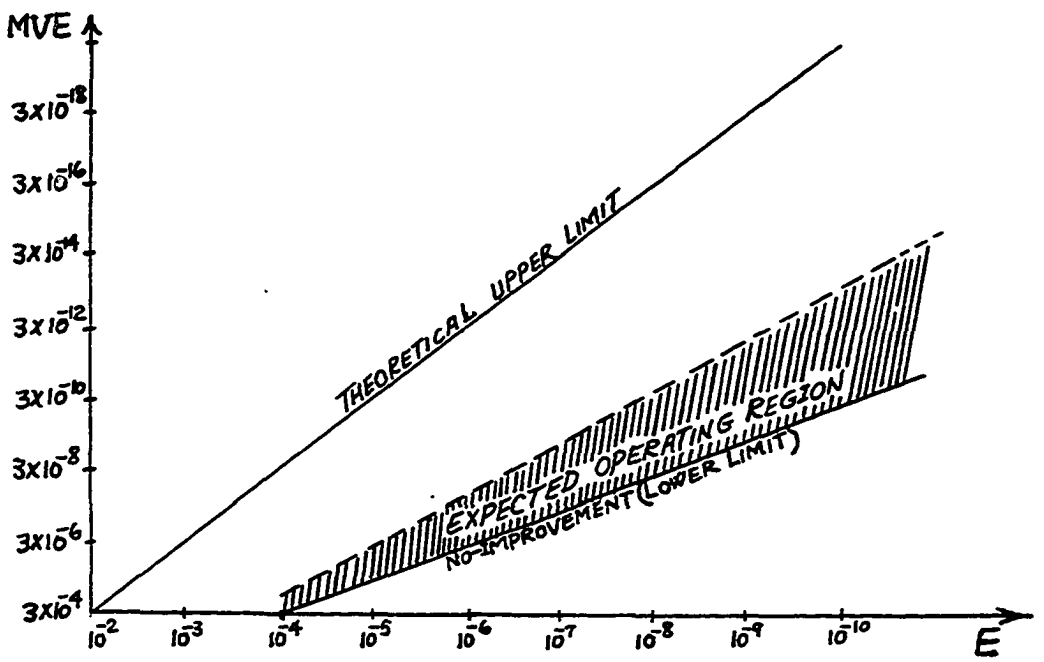


Figure 4.7 Expected Operating Region for a Three-Channel System

cluded a controllable amount of interaction among the detectors, and the means of setting a basic error-rate by means of a simulated Gaussian noise power. The results of

the simulation for S/N from 1 to 6 are given in figure 4.8.

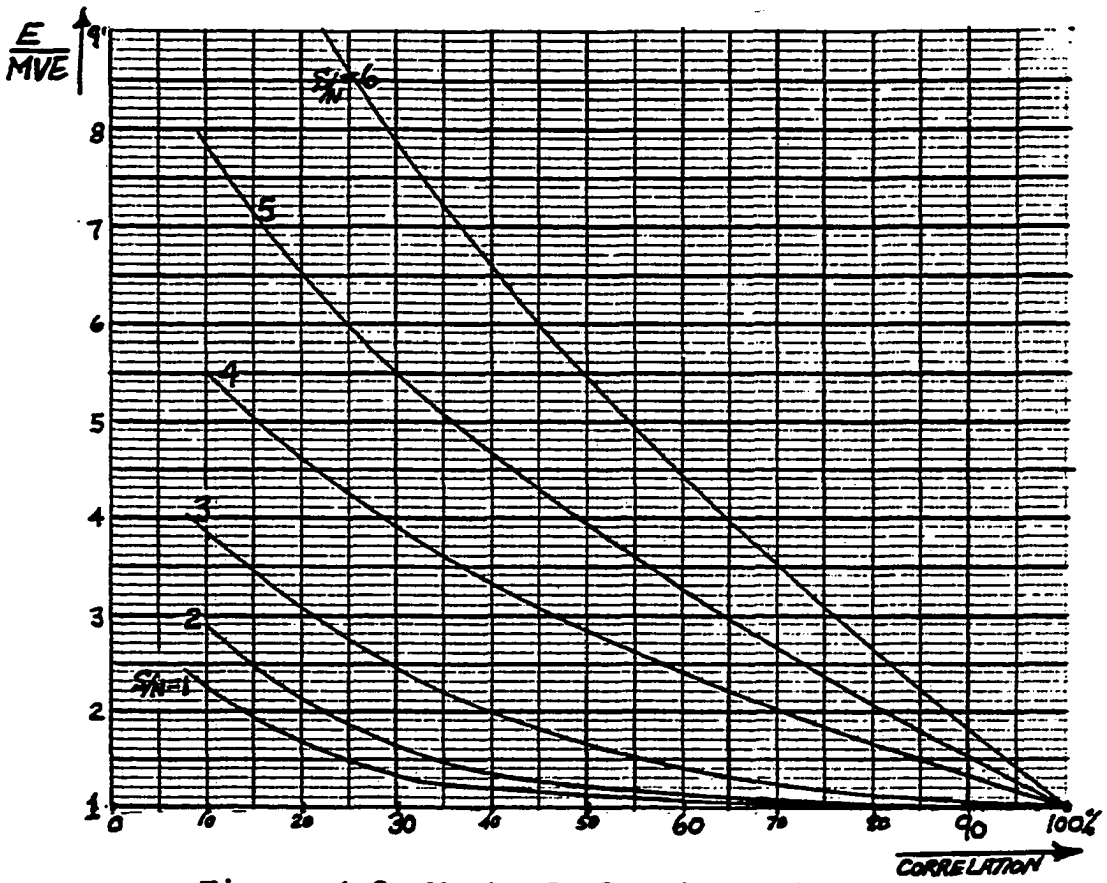


Figure 4.8 Monte Carlo Simulation of a Three-Channel System

As the basic S/N is increased and the error-rate is reduced, the excessive amount of computer time makes the exercise expensive and renders the model impractical.

The simplifying assumptions of linearity and ergodicity, although predominantly true, are not totally representative of a real life situation. The actual hardware and various complex signal and environmental conditions are extremely difficult, if not impossible, to represent mathematically. Hardware simulations may be the most reliable and representative tool which may be used to collect sta-

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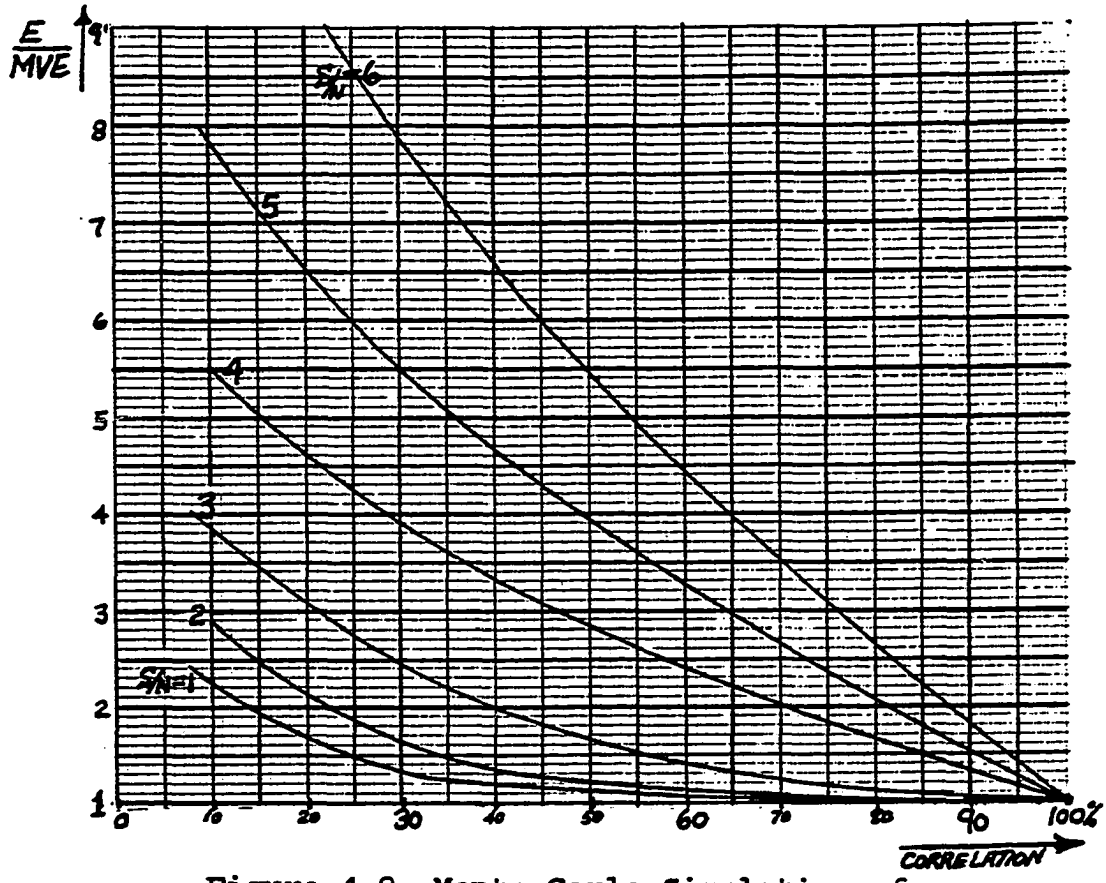

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tistics for model refinements, and for further extrapolations of long term error-rate performance.

A detailed block diagram of the proposed three-channel system is shown in figure 4.9. Channel I which employs I&D filters, is identical to the design presented in chapter III. Channel II is an extension pulse-data input to the PLL which utilizes a separate "window and re-time" logic block. A third channel which employs post equalization and base-line clipping in conjunction with a frequency domain hysteresis qualifier, has been introduced. The pre-equalizer, the AGC loop, and the PLL are common to the three channels. The following is the discussion of some of the inherent features of each channel.

Channel I has the major advantage over channels II and III in its tolerance to "dropins" which are predominantly caused by imperfections in the recording medium. Its inherent susceptibility to "drop-outs" has been reduced by use of the peak-following qualifier.

Channel II has major advantages in its simplicity and high resolution in timing resulting in optimum utilization of the available window, in addition to tolerance to amplitude variations as a result of the peak-following qualifier. This channel is inherently more susceptible to "drop-ins" than it is to "drop-outs".

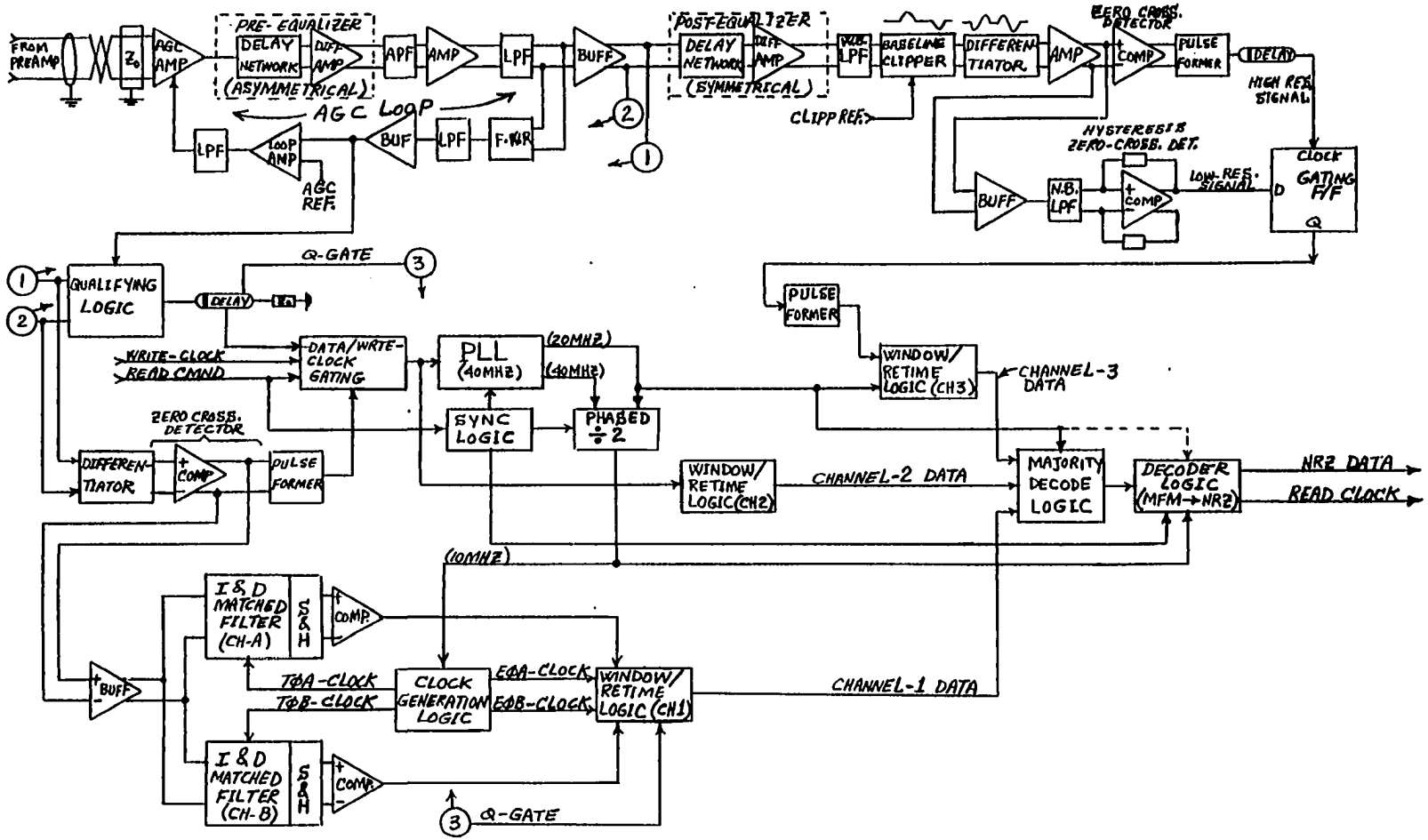

Figure 4.9 Detail Block Diagram of the Three-Channel System

Channel III employs post equalization to further enhance spectral definition and reduce peak shift. It employs a "baseline clipper", which introduces a well defined electronic baseline allowing a frequency domain qualifying channel for the general case. By differentiating after clipping the baseline, the differentiated sidelobes become well defined and independent of the baseline noise. Its major drawback is sensitivity to instantaneous peak amplitude variations. This sensitivity has been reduced by the introduction of the post equalizer which further reduces amplitude variations and peak shift at some loss in S/N. The net result is a uniform sensitivity to "drop-ins" and "drop-outs".

The Majority Decoder

The outputs of the three channels are first "retimed" with respect to the common PLL clock in order to align them in time prior to majority decoding. The logic of the majority decoder simply produces a pulse at each window interval, for any two or more input pulses as follows:

$$F=A\cdot B\cdot C+A\cdot B+A\cdot C+B\cdot C$$

$$=A\cdot B+A\cdot C+B\cdot C$$

Signal F may be viewed as a generalized "recovered" signal

which may be decoded into binary data from any previously encoded magnetic recording code.

Summary

Estimation of error-rate performance of a magnetic recording system is a non-trivial task which may lead to erroneous results if not approached properly. Two complimentary methods based on the allocation of error budgets, sample measurements, and long term statistics were presented.

Finally, the basic groundwork for a practical real-time three-channel correlation detector applicable to high density magnetic recording was given. By incorporating some modifications to the single channel detection system of chapter III, and by introducing a third channel with unique inherent properties, three channels with a certain degree of uncorrelatedness at the expense of a managable amount of hardware, were created. It is noted that, if designed properly, the three channel system has the capability of improving the performance. The degree of improvement would strongly depend on the magnetic system parameters such as the S/N ratio and the resolution. The detail design of the proposed three-channel system, its evaluation, and proof of attainable improvement in performance are recommended for future work.

APPENDIX A

A BRIEF DISCUSSION OF MAGNETIC RECORDING CODES

Magnetic disk storage systems use almost exclusively saturation type recording where either presence or absence, or the polarity and not the amplitude of the signal, carries the information.

The format of the recording most commonly used, is a phase coherent train of "encoded" pulses derived from the bit serial binary data. Some of the more important features used in classification (23) of codes are listed below:

1. Code Data Density. This parameter may be defined as the number of stored bits per flux reversal site.
2. Bandwidth. Usually, a code requiring narrow bandwidth is preferable to one requiring a wider bandwidth. In addition, codes requiring wide bandwidth generally can contain a high degree of DC component which increases amplifier settling time and low frequency baseline shift.
3. Self Clocking. In modern disk memories, a self

clocking code more commonly known as Run-Length-Limited (RLL) code, is a requirement for reliable detection.

4. Complexity of Encoding and Decoding. In recent years, with the proliferation of the high speed integrated circuits and high speed VLSI technology, the implementation of a new class of codes with favorable qualities and requiring relatively complex logic, is becoming very practicable and cost effective.
5. Noise Immunity. The sensitivity to "drop outs", "drop ins", and adjacent track interference varies from code to code, and should be considered when selecting a code.

The RLL codes are such that any two consecutive flux reversals are separated by at least d but not more than k missing reversals (27). Several RLL codes and their parameters (26) are depicted in figures A.1 and A.2 with respect to NRZI which is not a RLL code. A minimum bound on d is necessary in order to control pulse crowding which leads to excessive peak shift, while a maximum value on k is required to maintain self clocking property and to insure phase coherent detection. In constructing a RLL code, m bits of binary data are mapped into n possible flux reversal sites, resulting in a code which may be described by the parameters d,k,m,n, and r (28). Codes with r=1 are referred

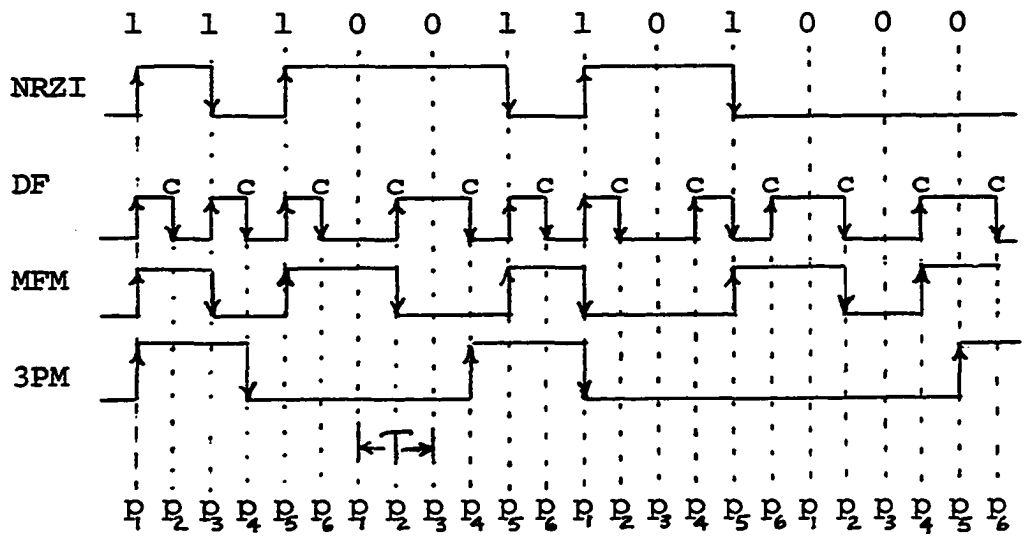

Figure A.1 Arbitrary Coded Sequence

code	m	n	m/n	d	k	r	T_w	T_{min}	T_{max}	η
NRZI	1	1	1	0	*	1	T	T	*	1
DF	1	2	.5	0	1	1	T/2	T/2	T	.5
MFM	1	2	.5	1	3	2	T/2	T	2T	1
3PM	3	6	.5	2	11	2	T/2	3T/2	6T	1.5

*Unlimited, T="Bit" Cell, η =Code Data Density

Figure A.2 Code Parameters

to as fixed length or freely concatenated codes, whereas codes with r>1 are called variable length or conditionally concatenated fixed-rate codes. For a binary sequence rate of 1/T seconds, the detection window T_w, the minimum time between flux transitions T_{min}, and the maximum time between flux transitions T_{max}, may be defined as,

$$T_w = (\frac{m}{n}) \cdot T$$

$$T_{min} = T_w \cdot (d+1)$$

$$T_{max} = T_w \cdot (k+1)$$

RLL codes with large T_w are less sensitive to timing jitters due to noise and peak shifts. For a specific magnetic recording channel, codes with large T_{min} result in high signal-to-noise ratio, whereas codes with large T_{max}/T_{min} ratio tend to have larger peak shift, contain larger spectral DC component, and suffer from loss in self clocking ability. It should be noted that, in general code parameters must be collectively considered when selecting a code which is to be used with a specific set of system parameters.

With reference to figure A.1, the encoding rules of each code is briefly discussed:

NRZI - (Non Return to Zero-Inverted). Not a RLL code; it may be encoded by providing a transition only at the flux reversal sites corresponding to each "1" bit. This code, as presented, is not used in high density recording due to absence of guaranteed synchro-

nization transitions. A variation of the NRZI which adds a synchronizing transition for each n data bits (n=2 to 10) may be used for relatively high density magnetic recording.

DF — (Double Frequency). As the name implies, two different frequencies are used to encode binary information into flux transitions and to provide self clocking capability. This code is generally used in low to medium density magnetic recording. To encode, a flux transition in the middle of the bit cell for each binary "1" in addition to a clock transition on every bit cell boundary are required.

MFM — (Modified Frequency Modulation). This code is commonly used in the medium to high density magnetic recording. At a given flux density, it provides twice the bit density as compared to the DF code. The encoding algorithm is somewhat more involved and may be stated as follows: Place a flux transition in the middle of the bit cell for every "1" bit, and a flux transition at the end of the bit cell for every "0" bit unless followed by a cell containing a "1" bit. The signal processing and

decoding electronics are more complex as compared to that of the DF code.

3PM - (3 Position Modulation). A relatively new code (26), provides 50 percent more bit density as compared to the MFM code at a given flux density. However, as it may be suspected, the encode/decode algorithms and the necessary signal processing electronics for reliable detection are significantly more complex when compared to the other codes under discussion. The 3PM code is a conditionally concatenated code whose encoding algorithm may be stated as follows, with reference to table A.1.

A sequence of binary bits containing an integral multiple of 3 bits may be encoded into flux transitions at each p_i (i=1,2,...,6) position containing a 1. In a sequence where a 1 occurs at p_5 of the present block (p_1,...,p_6) and also at p_1 of the following block (p_1,..., p_6), both p_1 and p_5 are merged into the present (center) block's p_6 position in order to preserve the d=2 condition. An example is illustrated by figure A.3.

Binary Sequence			Flux Transition Positions					
			p_1	p_2	p_3	p_4	p_5	p_6^*
0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	1	0	0
0	1	0	0	1	0	0	0	0
0	1	1	0	1	0	0	1	0
1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0
1	1	0	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0

*Reserved position to facilitate conditional concatenation

Table A.1 3PM Primary Conversions

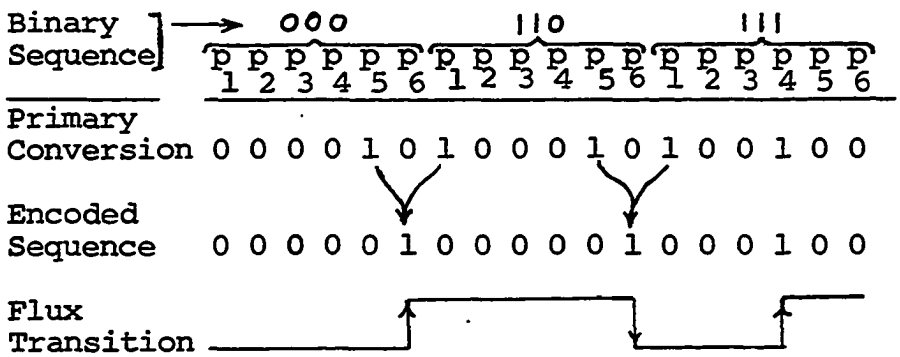

Figure A.3 Example of 3PM Encoding

APPENDIX B

AMPLITUDE AND PEAK SHIFT OF DIBITS AND TRIBITS

BASIC Program List and Data for the Dibit

```
10  T0=100E-9
20  TP=26*T0
30  P=2*3.14159/TP
40  PW=50E-9
50  K=2/PW
60  FOR T=-75E-9 TO TP STEP 1E-9
70  E=0
80  FOR N=1 TO 120
90  A0=COS(P*N*T)
100 A1=COS(P*N*(T-T0))
130 AA=A0-A1
140 AB=EXP(-N*P/K)
150 E=E+AA*AB
160 NEXT N
170 E=P*E/K
180 PRINT "T="T,"E="E
190 NEXT T
200 END
```

PW=50E-9		PW=100E-9	
TA= -.5E-9	EA=+.9405	TA= -3.8E-9	EA=+.806
TB=100.5E-9	EB=-.9405	TB=103.8E-9	EB=-.806

PW=133E-9		PW=165E-9	
TA= -8E-9	EA=+.711	TA=-14.5E-9	EA=+.6283
TB=108E-9	EB=-.711	TB=114.5E-9	EB=-.6283

PW=200E-9		PW=400E-9	
TA=-21.5E-9	EA=+.552	TA=-73E-9	EA=+.3103
TB=121.5E-9	EB=-.552	TB=173E-9	EB=-.3103

BASIC Program List and Data for the Tribit

```
10  T0=100E-9
20  TP=26*T0
30  P=2*3.14159/TP
40  PW=50E-9
50  K=2/PW
60  FOR T=-100E-9 TO TP STEP 1E-9
70  E=0
80  FOR N=1 TO 120
90  A0=COS(P*N*T)
100 A1=COS(P*N*(T-T0))
110 A2=COS(P*N*(T-2*T0))
120 A3=COS(P*N*(T-14*T0))
130 AA=A0-A1+A2-A3
140 AB=EXP(-N*P/K)
150 E=E+AA*AB
160 NEXT N
170 E=P*E/K
180 PRINT "T="T,"E="E
190 NEXT T
200 END
```

PW=50E-9		PW=66.66E-9	
TA=0	EA=+.956	TA=-1E-9	EA=+.926
TB=100E-9	EB=-.883	TB=100E-9	EB=-.801
TC=200E-9	EC=+.956	TC=201E-9	EC=+.926

PW=100E-9		PW=133E-9	
TA=-3.1E-9	EA=+.86	TA= -7E-9	EA=+.799
TB=100E-9	EB=-.602	TB=100E-9	EB=-.391
TC=103.1E-9	EC=-.86	TC=107E-9	EC=+.799

PW=165E-9		PW=200E-9	
TA=-10.8E-9	EA=+.753	TA=-15.5E-9	EA=+.715
TB=100E-9	EB=-.197	TB=100E-9	EB=-.009
TC=110.8E-9	EC=+.753	TC=115.5E-9	EC=-.715

PW=300E-9	
TA=-23.5E-9	EA=+.668
TB=100E-9	EB=+.363
TC=223.5E-9	EC=+.668

APPENCIX C

MFM WAVEFORM SIMULATION

BASIC Program and Selected Data for e(t)

```
10  T0=100E-9
20  TP=15*T0
30  P=2*3.14159/TP
40  PW=200E-9
50  K=2/PW
60  FOR T=0 TO TP STEP2.5E-9
70  E=0
80  FOR N=1 TO 15
90  A0=COS(P*N*T)
100 A1=COS(P*N*(T-T0))
110 A2=COS(P*N*(T-2*T0))
120 A3=COS(P*N*(T-4*T0))
130 A4=COS(P*N*(T-5*T0))
140 A5=COS(P*N*(T-6*T0))
150 A6=COS(P*N*(T-8*T0))
160 A7=COS(P*N*(T-9.5*T0))
162 A8=COS(P*N*(T-11*T0))
164 A9=COS(P*N*(T-12*T0))
166 B1=COS(P*N*(T-13*T0))
168 B2=COS(P*N*(T-14*T0))
170 AS=A0-A1+A2-A3+A4-A5
172 AA=AS+A6-A7+A8-A9+B1-B2
180 AB=EXP(-N*P/K)
190 E=E+AA*AB
192 NEXT N
200 E=P*E/K
202 E=E+.0005
204 E=INT(E*1000)/1000
210 PRINT"T="T,"E="E
220 NEXT T
230 END
```

PW_{50}=100E-9

t(E-9)	e(t)	t(E-9)	e(t)	t(E-9)	e(t)
2.5	+.669	460	+.143	980	-.586
5	+.662	470	+.336	1000	-.314
10	+.638	480	+.489	1020	-.061
30	+.395	490	+.586	1040	+.163
50	+.0057	497.5	+.616	1060	+.396
70	-.371	500	+.617	1080	+.622
80	-.509	515	+.535	1090	+.699
90	-.595	520	+.477	1095	+.721
97.5	-.622	530	+.324	1100	+.73
100	-.623	540	+.136	1105	+.723
105	-.614	560	-.273	1110	+.7
110	-.589	580	-.606	1120	+.605
120	-.496	590	-.71	1140	+.25
130	-.352	595	-.743	1160	-.189
140	-.167	600	-.763	1180	-.524
150	+.041	602.5	-.767	1190	-.611
160	+.254	605	-.769	1195	-.63
170	+.451	607.5	-.767	1197.5	-.634
180	+.612	610	-.761	1200	-.633
190	+.722	620	-.71	1210	-.595
195	+.755	640	-.5	1220	-.501
200	+.772	660	-.25	1240	-.189
202.5	+.775	680	-.12	1260	+.197
210	+.762	700	+.014	1280	+.526
215	+.737	720	+.091	1290	+.626
220	+.7	740	+.262	1295	+.654
240	+.479	760	+.53	1300	+.666
250	+.357	780	+.77	1305	+.66
260	+.247	790	+.83	1310	+.638
270	+.159	795	+.841	1320	+.545
280	+.094	800	+.837	1340	+.206
300	+.005	810	+.79	1360	-.207
320	-.095	820	+.699	1380	-.528
340	-.268	840	+.45	1390	-.614
360	-.498	860	+.197	1400	-.641
380	-.7	880	-.04	1410	-.606
390	-.755	900	-.299	1420	-.516
395	-.766	920	-.575	1440	-.199
397.5	-.767	940	-.768	1460	+.199
400	-.764	945	-.79	1480	+.534
410	-.72	950	-.798	1490	+.633
420	-.621	955	-.792	1500	+.669
440	-.282	960	-.773		

PW_{50}=200E-9

t(E-9)	e(t)	t(E-9)	e(t)	t(E-9)	e(t)
2.5	+.301	490	+.119	980	-.429
5	+.299	495	+.13	1000	-.275
10	+.29	497.5	+.133	1020	-.086
30	+.196	500	+.134	1040	+.106
50	+.043	502.5	+.133	1060	+.272
70	-.108	505	+.13	1080	+.381
80	-.162	510	+.119	1090	+.405
90	-.194	520	+.077	1092.5	+.408
95	-.201	540	-.07	1095	+.408
97.5	-.202	560	-.257	1100	+.405
100	-.201	580	-.422	1110	+.378
110	-.18	590	-.479	1120	+.328
120	-.132	600	-.515	1140	+.169
130	-.062	605	-.523	1160	-.018
140	+.025	607.5	-.525	1180	-.167
150	+.123	610	-.526	1190	-.211
160	+.222	612.5	-.525	1195	-.223
170	+.315	615	-.523	1200	-.228
180	+.396	620	-.514	1202.5	-.228
190	+.457	640	-.43	1205	-.226
200	+.495	660	-.294	1210	-.218
205	+.505	680	-.138	1220	-.183
210	+.508	700	+.022	1240	-.053
212.5	+.508	720	+.183	1260	+.109
215	+.506	740	+.345	1280	+.242
220	+.498	760	+.492	1290	+.28
240	+.419	780	+.592	1295	+.29
250	+.357	790	+.614	1300	+.293
260	+.29	792.5	+.616	1305	+.289
270	+.217	795	+.616	1310	+.279
280	+.142	797.5	+.615	1320	+.24
300	-.01	800	+.612	1340	+.102
320	-.164	820	+.541	1360	-.067
340	-.314	840	+.392	1380	-.202
360	-.445	860	+.194	1390	-.24
380	-.524	880	-.023	1395	-.25
385	-.533	900	-.233	1400	-.253
387.5	-.535	920	-.405	1405	-.249
390	-.535	930	-.466	1410	-.239
392.5	-.535	940	-.506	1420	-.2
395	-.532	945	-.518	1440	-.063
410	-.488	950	-.523	1460	+.106
420	-.43	952.5	-.523	1480	+.245
440	-.263	955	-.522	1490	+.286
460	-.073	960	-.514	1495	+.297
480	+.077	970	-.482	1500	+.301

BASIC Program and Selected Data for E(t)=de(t)/dt

```
10  T0=100E-9
15  TI=50E-9
20  TP=15*T0
30  P=2*3.14159/TP
40  PW=200E-9
50  K=2/PW
60  FOR T=0 TO TP STEP 2.5E-9
70  E=0
80  FOR N=1 TO 15
90  A0=COS(P*N*T) -COS(P*N*(T-T1))
100 A1=COS(P*N*(T-T0))-COS(P*N*(T-T0-T1))
110 A2=COS(P*N*(T-2*T0))-COS(P*N*(T-2*T0-T1))
120 A3=COS(P*N*(T-4*T0))-C)S(P*N*(T-4*T0-T1))
130 A4=COS(P*N*(T-5*T0))-COS(P*N*(T-5*T0-T1))
140 A5=COS(P*N*(T-6*T0))-COS(P*N*(T-6*T0-T1))
150 A6=COS(P*N*(T-8*T0))-COS(P*N*(T-8*T0-T1))
160 A7=COS(P*N*(T-9.5*T0))-COS(P*N*(T-9.5*T0-T1))
162 A8=COS(P*N*(T-11*T0))-COS(P*N*(T-11*T0-T1))
164 A9=COS(P*N*(T-12*T0))-COS(P*N*(T-12*T0-T1))
166 B1=COS(P*N*(T-13*T0))-COS(P*N*(T-13*T0-T1))
168 B2=COS(P*N*(T-14*T0))-COS(P*N*(T-14*T0-T1))
170 AS=A0-A1+A2-A3+A4-A5
172 AA=AS+A6-A7+A8-A9+B1-B2
180 AB=EXP(-N*P/K)
190 E=E+AA*AB
192 NEXT N
200 E=P*E/K
202 E=E+.0005
204 E=INT(E*1000)/1000
210 PRINT"T="T,"E="E
220 NEXT T
230 END
```

PW_{50}=100E-9, τ=50E-9

t(E-9)	E(t)	t(E-9)	E(t)	t(E-9)	E(t)
0	+.671	40	-.424	140	+.428
2.5	+.618	50	-.663	150	+.664
5	+.562	75	-.92	177.5	+.968
10	+.439	100	-.628	200	+.731
15	+.303	110	-.395	210	+.508
20	+.159	120	-.125	220	+.249
22.5	+.085	122.5	-.055	227.5	+.0508
25	+.009	125	+.0157	230	-.0129
27.5	-.065	127.5	+.0864	235	-.134
30	-.14	130	+.157	240	-.243

t(E-9)	E(t)	t(E-9)	E(t)	t(E-9)	E(t)
260	-.515	672.5	+.565	1125	-.037
270	-.541	680	+.547	1130	-.172
280	-.506	690	+.48	1140	-.449
290	-.434	725	+.228	1150	-.701
322.5	-.253	760	+.485	1175	-.993
350	-.385	770	+.574	1200	-.662
360	-.459	780	+.609	1210	-.406
370	-.514	790	+.568	1220	-.121
377.5	-.529	810	+.259	1222.5	-.049
400	-.385	820	+.0352	1225	+.022
410	-.223	822.5	-.0223	1230	+.162
420	-.117	830	-.189	1240	+.421
422.5	+.0464	840	-.38	1250	+.636
430	+.228	850	-.517	1275	+.894
440	+.473	875	-.623	1300	+.663
450	+.694	892.5	-.615	1310	+.441
475	+.971	910	-.637	1320	+.167
500	+.688	925	-.656	1325	+.0188
510	+.436	940	-.604	1327.5	-.0562
520	+.141	950	-.498	1330	-.131
522.5	+.064	960	-.333	1340	-.420
525	-.0127	970	-.123	1350	-.668
530	-.165	975	-.009	1375	-.94
540	-.45	980	+.104	1400	-.639
550	-.686	990	+.316	1410	-.399
575	-.943	1000	+.483	1422.5	-.0573
600	-.694	1010	+.591	1425	+.0129
610	-.489	1025	+.643	1430	+.152
620	-.254	1050	+.591	1440	+.415
630	-.0126	1070	+.575	1450	+.639
632.5	+.0457	1080	+.569	1475	+.916
640	+.21	1100	+.453	1500	+.671
660	+.511	1122.5	+.028		

PW_{50}=200E-9, τ=50E-9

t(E-9)	E(t)	t(E-9)	E(t)	t(E-9)	E(t)
0	+.28	50	-.258	177.5	+.459
2.5	+.258	75	-.365	200	+.372
5	+.235	100	-.244	210	+.286
10	+.184	110	-.143	220	+.183
15	+.129	120	-.024	227.5	+.099
20	+.071	122	0	230	+.072
22.5	+.041	125	+.038	236	-.006
25	+.011	127.5	+.069	240	-.037
26	-.001	130	+.1	260	-.218
30	-.049	140	+.22	270	-.281
40	-.162	150	+.323	280	-.325

t(E-9)	E(t)	t(E-9)	E(t)	t(E-9)	E(t)
290	-.353	690	+.372	1119	+.004
330	-.382	725	+.401	1130	-.126
350	-.373	760	+.39	1140	-.236
360	-.358	770	+.368	1150	-.33
370	-.329	780	+.328	1175	-.431
390	-.221	790	+.269	1200	-.303
400	-.14	810	+.095	1210	-.2
410	-.043	819	+.001	1220	-.081
415	+.009	825	-.064	1227	+.005
420	+.063	830	-.118	1230	+.042
430	+.172	840	-.222	1240	+.158
440	+.273	850	-.315	1250	+.256
450	+.357	875	-.478	1275	+.371
470	+.441	900	-.53	1300	+.265
490	+.382	910	-.52	1310	+.17
510	+.192	925	-.47	1320	+.057
520	+.066	940	-.376	1325	-.003
525	+.001	950	-.29	1327	-.027
530	-.065	960	-.189	1330	-.063
540	-.189	970	-.077	1340	-.178
550	-.296	977	+.003	1350	-.275
575	-.434	980	+.037	1375	-.386
600	-.352	990	+.148	1400	-.27
610	-.268	1000	+.248	1410	-.172
620	-.168	1010	+.332	1425	+.003
630	-.059	1025	+.421	1427	+.027
635	-.004	1050	+.469	1430	+.063
640	+.049	1070	+.422	1440	+.177
660	+.232	1080	+.37	1450	+.274
670	+.297	1100	+.211	1475	+.388
680	+.343	1115	+.05	1500	+.28

APPENDIX D

AMPLITUDE AND PEAK SHIFT OF EQUALIZED DIBITS AND TRIBITS

BASIC Program List and Data for the Equalized Dibit Pattern

```
10  T0=100-9
20  TP=15*T0
30  P=2*3.14159/TP
40  PW=50E-9
45  TI=.35*PW
50  K=2/PW
60  FOR T=-50E-9 TO TP STEP IE-9
70  E=0
90  A0=1/(1+(K*(T))↑2)
95  B0=-.35/(1+(K*(T+T1))↑2)-.35/(1+(K*(T-T1))↑2)
97  A0=A0+B0
100 A1=1/(1+K*(T-T0))↑2)
105 B1=-.35/(1+(K*(T-T0+T1))↑2)-.35/(1+(K*(T-T0-T1))↑2)
107 A1=A1+B1
170 AA=A0-A1
190 E=E+AA
202 E=E+.0005
204 E=INT(E*1000)/1000
210 PRINT "T="T, "E="E
220 NEXT T
230 END
```

PW=50E-9		PW=100E-9	
TA=0	EA=+.516	TA=.05E-9	EA=+.5025
TB=100E-9	EB=-.516	TB=100.05E-9	EB=-.5025

PW=133E-9		PW=165E-9	
TA= -.6E-9	EA=+.496	TA= -3.5E-9	EA=+.481
TB=100.6E-9	EB=-.496	TB=103.5E-9	EB=-.481

PW=200E-9		PW=400E-9	
TA= -8.5E-9	EA=+.451	TA= -49.5E-9	EA=+.288
TB=108.5E-9	EB=-.451	TB=1049.5E-9	EB=-.288

BASIC Program List and Data for the Equalized Tribit Pattern

```
10  T0=100E-9
20  TP=15*T0
30  P=2*3.14159/TP
40  PW=50E-9
45  TI=.35*PW
50  K=2/PW
60  FOR T=-50E-9 TO TP STEP 1E-9
70  E=0
90  A0=1/(1+(K*(T))↑2)
95  B0=-.35/(H(K*(T+T1))↑2)-.35/(1+(K*(T-T1))↑2)
97  A0=A0+B0
100 A1=1/(1+K*(T-T0))↑2)
105 B1=-.35/(1+(K*(T-T0+T1))↑2)-.35/(1+(K*(Y-T0-T1))↑2)
107 A1=A1+B1
110 A2=1/(H(K*(T-2*T0))↑2)
120 B2=-.35/(1+(K*(T-2*T0+T1))↑2)-.35/(1+(K*(T-2*T0-T1))↑2)
130 A2=A2+B2
170 AA=A0-A1+A2
190 E=E+AA
202 E=E+.0005
204 E=INT(E*1000)/1000
210 PRINT "T="T,"E="E
220 NEXT T
230 END
```

PW=50E-9		PW=66.66E-9	
TA=0	EA=+.52	TA=.06E-9	EA=+.517
TB=100E-9	EB=-.502	TB=100E-9	EB=-.489
TC=200E-9	EC=+.52	TC=200.06E-9	EC=+.517

PW=100E-9		PW=133E-9	
TA=-.4E-9	EA=+.517	TA=-.65E-9	EA=+.516
TB=100E-9	EB=-.475	TB=100E-9	EB=-.462
TC=200.4E-9	EC=+.517	TC=100.65E-9	EC=+.516

PW=165E-9

TA=-3.8E-9 EA=+.504
TB=100E-9 EB=-.425
TC=103.8E-9 EC=+.504

PW=200E-9

TA=-8E-9 EA=+.479
TB=100E-9 EB=-.352
TC=108E-9 EC=+.479

PW=300E-9

TA=-26.5E-9 EA=+.393
TB=100E-9 EB=-.089
TC=126.5E-9 EC=+.393

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