A BINARY ADDER USING TRANSISTORS

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CHAPTER I

INTRODUCTION

As the areas of application for electronic computers continue to expand, the need for larger computers increases. Since most of the digital computers now in operation employ vacuum-tube circuitry, they cannot be made larger without increasing the physical size, the power consumption, and the number of components, unless further advances in computer circuit technology is forthcoming. Since an enormous number of vacuum-tubes are used in a modern computer, the filament power requirement is very large--much larger, in fact, than the power required for the d-c plate supply. Because of this, external air conditioning is necessary to cool the vacuum-tubes.

With the invention and continued development of the transistor comes hope for resolving these problems of power and size. Transistors require neither filament power nor external cooling under normal operation. Computer circuits, using transistors for the active elements, can be made much smaller than corresponding computer circuits using vacuum-tubes. Furthermore, transistors afford new and more versatile computer circuits using complementary symmetry,[1] for which there is no vacuum-tube counterpart. However, transistors are not without limitations--the principal one being the maximum operating

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[1] Lo, Endres, Zawels, Waldhauer & Cheng, Transistor Electronics, Prentice-Hall, New Jersey, 1955, pp. 182-185, 217-221.

frequency commonly called the alpha cutoff frequency, f_α. The maximum switching speed is dependent upon f_α, decreasing as f_α decreases. This was a serious problem when transistors were first placed on the market, because f_α was much less than the maximum operating frequency of vacuum-tubes. At present, however, the art of manufacturing transistors has been improved to the extent that transistors are available in production quantities with f_α of 30 mc, and transistors with f_α of over 100 mc are in the development stage. Transistors with these and other present day qualities seem to be adequate for modern computer circuitry.

With transistors as a possible means to an end in solving the modern computer problems of size, power required, and heat dissipation, the purpose of this thesis is to develop some of the basic computer circuits using transistors instead of vacuum-tubes. Since the proper development of such computer circuits requires a method for testing these circuits as a system as well as individually, and adder was also chosen for development. Because an adder is merely a logical assembly of the basic computer circuits, these basic circuits can readily be integrated into an adder to determine their capabilities for operating as a part of a larger system.

CHAPTER II

LOGICAL DEVELOPMENT OF THE ADDER

Since there are many possible methods for performing the operation of addition, the first step in the development of an adder is to investigate these possible methods intelligently to arrive at a satisfactory and workable method for performing addition. Since there must be numbers before there can be addition, the first consideration is the choice of a radix for the number system. The radix of a number system is the numerical quantity of different digit symbols used in the number system. For example, the digits 0123456789 compose our most used number system of radix ten; whereas, the digits 0 and 1 compose the number system of radix two, which is referred to as the binary number system. It is possible to design a digital computer using any radix; but the quantity of equipment required, the resulting computer speed, and the required accuracy makes the choice of many radices impracticable. Richards states,[2] "So far as is known, radices two, three, eight, ten, twelve, and sixteen are the only ones which have ever received serious consideration for use in computing machinery."

Since a computer is unique in that it is able to store information, the electrical and mechanical equipment required for storage is a determining factor in the selection of the radix for the number system

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[2] R. K. Richards, Arithmetic Operations in Digital Computers, Van Nostrand, New Jersey, 1955, p. 5.

to be used. In general, it is true that the amount of equipment required to store a digit is proportional to the radix of the number system from which that digit was taken. For example, two stable states are required to store a digit of radix two; whereas, ten stable states are required to store a digit of radix ten. Four independent circuits, each with two stable states can exist in any one of $2^4 = 16$ stable states. Hence, less equipment is required to store a number in a number system of radix two than is required to store the same number in a system of radix ten. In general, the more equipment used in a computer system, the slower the system and the greater the probability of error. Each piece of equipment requires a certain fixed amount of time to operate; therefore, the more equipment used, the greater the required total operation time. Furthermore, since the accuracy of a computer system is determined by its simplicity and quantity of equipment, the least amount of equipment would again favor the binary number system for greatest accuracy in operation.

More materials and devices are capable of existing in two stable states than in any other number of stable states. This physical limitation is probably the greatest influence in favor of the choice of radix two for a number system in digital computers. For example, magnetic materials have two remnant flux states, making them capable of storing a binary digit. Simple mechanical contacts have two stable states, either open or closed. Furthermore, two triodes or transistors and a few passive components can be connected to form a circuit having two stable states, which is therefore capable of storing a binary digit. Many more than two, however, would be required to store any digit of a number system whose radix is greater than two. These are a portion of the facts which show why the binary number system

(radix two) has shown prominence over number systems of other radices for use in modern digital computers.

The next consideration is the method for performing addition. The discussion of addition will be more enlightening if it is introduced with the following definition and explanation. The order of a digit in a multi-digit number is a number n giving the digit a value equal to the radix R raised to the power n, R^n, where n is equal to the number of that digit counting from right to left beginning with n = 0. For example, in the number 10100 of radix two, the digit 1 to the right is of order 2 and, by itself, is equal to $1 \times 2^2 = 4_{10}$. Hence $100_2 = 4_{10}$, where numerical subscripts denote the radix of the number. Likewise, the digit 1 on the left of 10100_2 is of order 4 and has the value $1 \times 2^4 = 16_{10} = 10000_2$. Of course the zero, first, and third order digits are zero because $0 \times 2^n = 0$. Hence $10100_2 = 1 \times 2^4 + 1 \times 2^2 = 20_{10}$.[3]

The average person will perform the addition of several multi-digit decimal numbers by adding one column at a time beginning with the units digit column (order 0) on the right and progressing column by column toward the higher order digits to the left. Each time a column is added, that sum will indicate whether or not a carry must be added to the next higher order digit column. If the sum consists of two or more digits, the lowest order digit must be recorded and the remaining digits added to the next higher order column of digits according to their powers of the radix. If the sum for one column

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[3]Montgomery Phister, Jr., Logical Design of Digital Computers, Wiley, New York, 1958, Chapter 2.

consists of only one digit, that digit must be recorded and nothing added to the next higher order column of digits. This simple process is continued until each column has been added and its sum investigated for the presence of a carry and there is no higher order digit column. If a carry then exists, it is written with the sum of the higher order column of digits. For example, if the multi-digit numbers of radix ten to be added are

$$\begin{array}{r} 385 \\ 792 \\ \underline{108} \end{array}$$

then for addition they break down into

$$\begin{array}{r} 5 \\ 2 \\ \underline{8} \end{array}$$

carry ⟶ ⑮ ⟵ sum of units digit column (order 0)

$$\begin{array}{r} 8 \\ 9 \\ \underline{0} \end{array}$$

carry ⟶ ⑱ ⟵ sum of tens digit column (order 1)

$$\begin{array}{r} 3 \\ 7 \\ \underline{1} \end{array}$$

carry ⟶ ⑫ ⟵ sum of hundreds digit column (order 2)

where the last carry becomes part of the sum, or

⑫ ⟵ sum of hundreds digit column

Therefore, the total sum is equal to the sum of the partial sums of each order digit column, which is equal to 1285 of radix ten.

The preceding method of addition is obviously a satisfactory one; but it is not feasible to build a computer which adds by this method, because the quantity of equipment required would be greater than that required to perform addition by another method. Hence, for the problem at hand, another method of addition that requires a minimum

of equipment was chosen. It is developed in the discussion which follows.

A digital computer is unique in that it is able to store information. Since it must also be able to perform arithmetic operations, it must then have an arithmetic unit as well as a storage unit often called a memory unit. Since a computer must also be capable of transferring information back and forth between the arithmetic unit and the memory unit, the most feasible method of addition is to add multi-digit numbers one at a time as they are transferred from the memory unit to the arithmetic unit. Since present day electronic switching curcuits can have operation times in the order of tenths of a micro-second, addition by the one-at-a-time method is very rapid. For example, a computer adding the three multi-digit numbers previously shown would add the first two numbers by the method previously described and then add the third number to the sum of the first two by that same method. In short, this method of addition was selected because it is compatible with the requirements and inherent characteristics of present day electronic circuitry.

There are two basic methods by which two multi-digit numbers can be added. They are called serial and parallel addition. In serial addition, the two zero order digits are added first and recorded. Then the two first order digits plus the carry from the zero order digits are added and recorded. Then the second order digits plus the carry from the first order digits are added and recorded and so on until the highest order digits and carrys have been added and recorded. Since only one addition takes place at a time, only one adder circuit is needed to add all the digits in summing two multi-digit numbers.

In parallel addition, the two digits of every order are added simultaneously; then the carrys are added as they occur. Suppose the multi-digit numbers being added consisted of four digits each. Then four identical adder circuits would be required for parallel addition, one for each order of digits plus the circuitry necessary for the propagation of the carry digits. Therefore, parallel addition is much faster than serial addition, but less equipment is required for serial addition. The evaluation of these advantages is quite arbitrary, depending mostly upon the particular requirements of speed and equipment. The fact that speed is a problem with transistor circuitry motivated the writer to choose parallel addition for study.

To minimize the quantity of electronic equipment required, and to maximize the speed, accuracy, and transferability of the arithmetic operation, the arithmetic unit must be of the accumulator type. The name accumulator is given to a register[4] which accumulates and temporarily stores the sum of its contents plus the contents of another register. This simply means that the sum of two numbers placed in two different registers must accumulate in one of these two registers replacing the original number of that register. If this were not done, a third register would have to be added to the arithmetic unit to contain the sum. More registers would have to be used if more than two numbers were to be added at a time. Since no more than two registers are actually needed, only two will be used.

There are, however, additional requirements which influence the choice of circuitry for the adder. In short, these requirements are:

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[4]The term register is used to designate a group of identical electronic circuits, each of which is capable of temporarily storing a binary digit. They are arranged from right to left in ascending order of digits so as to be capable of displaying a multi-digit binary number.

1) The adder must be capable of storing the augend and the addend temporarily. 2) Addition must be controlled to begin at a predetermined instant of time. 3) The adder must be capable of storing the total sum. The first and third requirements are necessary to accommodate the transfer of information from the storage unit to the arithmetic unit and back, and to accomplish addition by adding one number at a time as previously described. The second requirement is necessary when addition is only one of a number of computer operations to be performed in sequence.

One of the most suitable electronic devices now available for generating and temporarily storing a binary digit at a predetermined time is the Eccles-Jordan bistable multivibrator commonly called the "flip-flop". Temporary storage is possible by virtue of the fact that the flip-flop has two stable states. It is capable of generating the binary digit, which it is to store, because of its transient response to an input trigger pulse. This trigger pulse is actually a timing signal from a pre-timed pulse generator. It allows the flip-flop to operate as a part of a larger sequence of operations. Conventional representation of the flip-flop is shown in Figure 1,

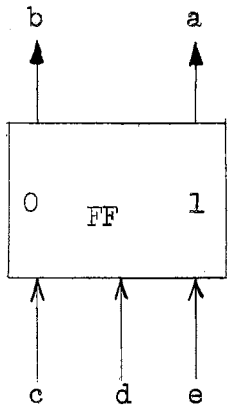

Figure 1. Standard Symbol for the Flip-Flop.

where a and b are the d-c output levels called "1" and "0" respectively, c and e are input pulses which set "0" and "1" output levels respectively, and d is an input pulse which complements[5] the d-c output level.

The discussion to this point has been spent in establishing the necessary requirements for a binary adder. An adder which will satisfy these requirements is shown in the block diagram of Figure 2.

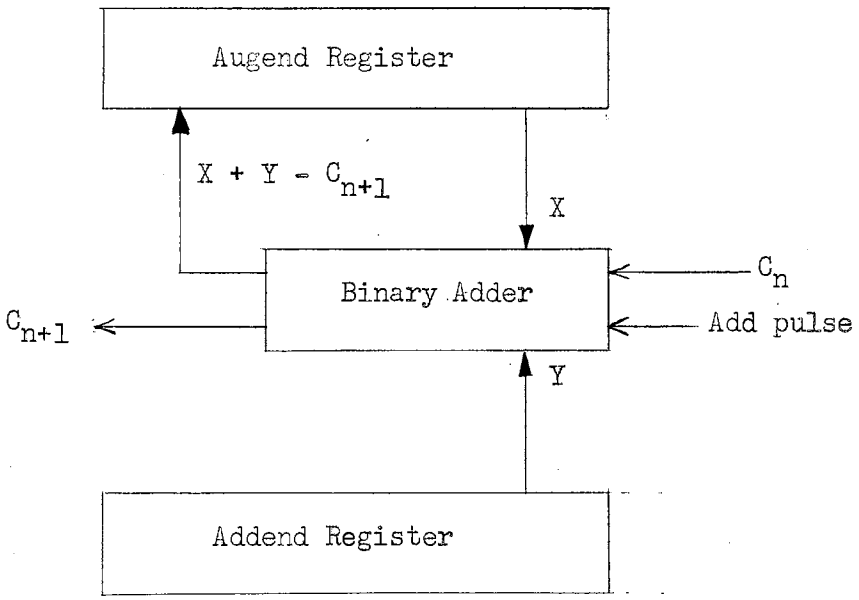

Figure 2. Required Binary Adder.

Referring to Figure 2, let X and Y be two binary digits of the same order to be added. By convention, X + Y means that Y is to be added to X. Thus, X is called the augend and Y the addend. Aside from adding X and Y, the binary adder must add in the carry digit from the next lower order, C_n, and generate a carry for the next higher

[5] A multi-digit binary number is complemented by changing its "1" digits to "0" and its "0" digits to "1".

order, C_{n+1}, when they occur. To avoid using a third register for storing the partial sum, $X + Y = C_{n+1}$, the partial sum is fed back to the augend register replacing the X that was there before addition occurred. This allows the augend register to be called an accumulator. The addition of Y to X has allowed the partial sum to accumulate in the same register that originally contained X. Furthermore, if the sum of X + Y + Z were required, Z would merely have to be placed into the addend register and added to the augend register which now contains the partial sum of X + Y. The carrys would also be taken care of by the binary adder as mentioned previously.

In order to arrive at a suitable electronic system which will best perform binary addition, it is necessary to consider the rules of binary addition. They are best expressed by the following truth table:

Augend Digit	0	0	1	1
Addend Digit	0	1	0	1
Sum Digit	0	1	1	0
Carry Digit	0	0	0	1

As explained previously, the augend digit is the digit to which the addend digit must be added. The sum digit is that part of the total sum which is of the same order as the corresponding augend and addend digits. The carry digit is that part of the total sum not included in the sum digit, which must be added to the next higher order digit.

From the truth table, the following Boolean algebra expressions can be deduced:[6]

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[6]Richards, op. cit., pp. 85-87.

$$\text{Sum} = \bar{X}Y + X\bar{Y}$$

$$\text{Carry} = XY$$

where:

X = Augend Digit

Y = Addend Digit

$\bar{X}$ = Complemented Augend Digit

$\bar{Y}$ = Complemented Addend Digit

Now, all that is required is an electronic circuit which will satisfy the above two equations. This could be any one of a number of possible circuits. To arrive at a specific circuit for binary addition, consider the preceding requirements along with the rules for binary addition. Such a circuit, which is capable of adding two 4-digit numbers, is shown in Figure 3. The notation used in Figure 3 is as follows:

A = "and" circuit

O = "or" circuit

D = pulse delay circuit

FF_n = flip-flop of order n in augend register

FF'_n = flop-flop of order n in addend register

$\longrightarrow$ = denotes d-c level

$\longrightarrow$ = denotes pulse

The add operation is begun with an add pulse applied to each order of digits. For every "1" digit in the addend register, the add pulse appears at the output of the corresponding "and" circuit. For every "0" digit in the addend register, the corresponding "and" circuit has no output. Furthermore, this output pulse from the "and" circuit will pass on through the "or" circuit to complement the corresponding flip-flop in the augend register. Hence a "1" has actually

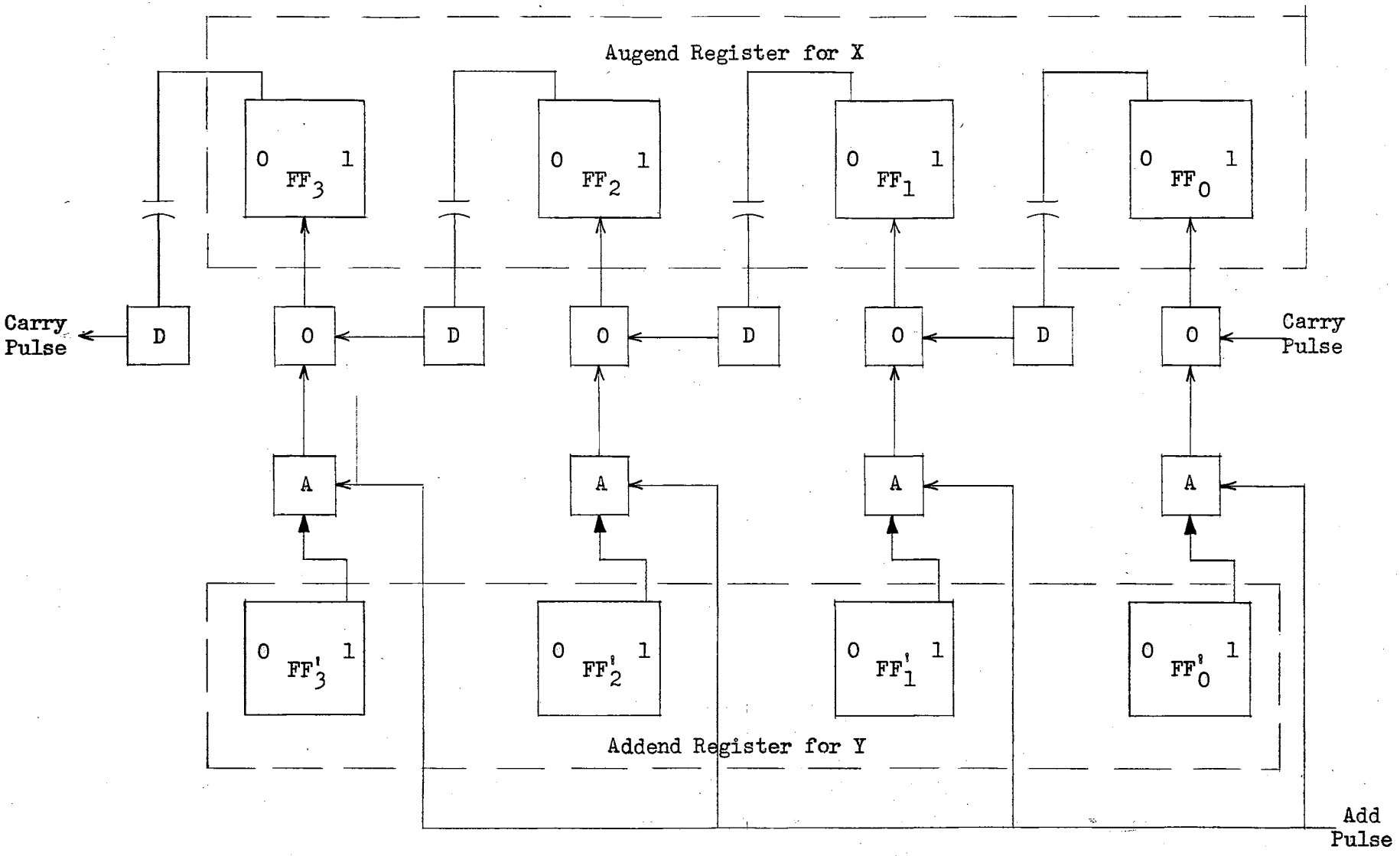

Figure 3. Four-Digit Binary Adder.

been added to each digit in the augend as designated by a corresponding "1" digit in the addend register. Complementing the augend flip-flops according to the contents of the addend flip-flops indeed satisfies the rules of binary addition. Since each augend flip-flop must switch to "0" and generate a carry for each addition of "1" + "1", the carry is taken as the positive pulse obtained from the differentiated output of the "0" side of each augend flip-flop. The carry pulse is then delayed to allow the addition to be completed before the carry is added into the partial sum by complementing the next higher order augend flip-flop. Again this is in accordance with the rules of binary addition. To accommodate the positive add and carry pulses, the accompanying circuitry is designed to operate on positive pulses only.

The remainder of this thesis consists of the analysis and synthesis of the flip-flop, the "and", and the "or" circuits as they were developed for general use in modern computer applications. Aside from affording the writer a study of computer logic design, the adder shown in Figure 3 was developed to obtain a system in which to employ and test these basic computer circuits.

CHAPTER III

THE BISTABLE MULTIVIBRATOR

Theory of Operation of the Bistable Multivibrator

The bistable multivibrator, commonly called the "flip-flop", is a regenerative circuit composed of two transistors (or vacuum tubes) which can exist indefinitely in either one of two stable states and can be made to change abruptly from one stable state to the other with an input trigger pulse. Its greatest attribute as a circuit device is its capability to be regenerative over the frequency range of approximately 0 to 10^6 c.p.s. It can be used as a binary storage unit, a binary switching circuit, or a combination of both. It is most commonly used as a switching circuit and a temporary storage unit. Since a shut-off in power will destroy the binary information stored in the flip-flop, it is seldom used for permanent storage. As a switching circuit, it has a square-wave output which is produced as a result of input trigger pulses.

The electrical circuit of the transistor flip-flop is normally symmetrical is shown in Figure 4. It is similar to the Eccles-Jordan vacuum-tube circuit. When referring to the flip-flop circuit the two transistors are called T_1 and T_2. When one of the transistors is cut off, it is said to be in the stable "off" state; likewise, when one of the transistors is conducting heavily, either into or near saturation, it is said to be in the stable "on" state.

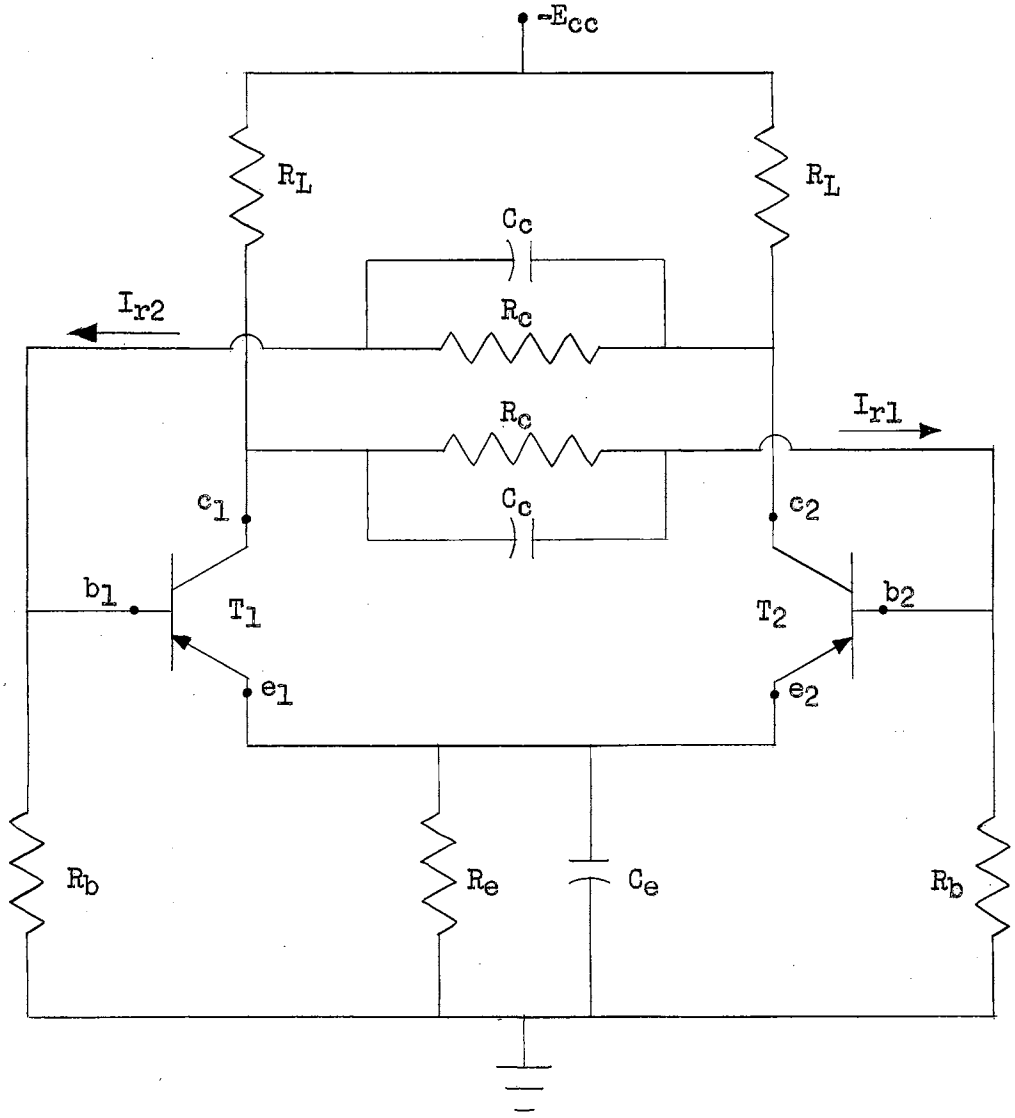

Figure 4. Basic Transistor Flip-Flop.

Two stable states exist such that one transistor is "off" when the other transistor is "on". This causes the collector voltage of the transistor which is "off", say T_1, to be higher than the collector voltage of T_2 which is "on". This is one stable state. The other stable state exists when T_1 is "on" and T_2 is "off". Because the flip-flop circuit is symmetrical the following correspondences exist. When T_1 is "on" and T_2 is "off", the corresponding values of V_{c1},

V_{b1}, V_{e1}, I_{b1}, and I_{r1} for T_1 are the same for T_2 when T_2 is "on" and T_1 is "off". For symmetrical operation T_1 and T_2 must have approximately the same value of β.

The nature of the two stable states is best presented by considering what happens when the flip-flop changes from one stable state to the other. Begin with T_1 "off" and T_2 "on". In this stable state, T_1 will have a higher collector potential than T_2; and because of circuit symmetry, the base of T_2 will be at a higher potential than the base of T_1. R_c and R_b are chosen such that the potential at the base of T_2 will cause T_2 to conduct heavily. This in turn causes the collector potential of T_2 to be low. Because the base of T_1 is electrically connected to the collector of T_2 by the resistor divider R_c and R_b, its potential is always lower than the collector potential of T_2. The base potential of T_1 is low enough, in fact, to cause T_1 to be cut off when T_2 is conducting heavily. This is one stable state.

A transition into the other stable state is achieved by letting a change in collector current, say I_{c1}, occur such as would be caused by an input trigger pulse. Since T_1 is off, I_{c1} is negligibly small and cannot respond to further decrease. I_{c1} must therefore be increased to accomplish the transition. As I_{c1} increases so does the voltage drop across R_L lowering the collector potential of T_1. This in turn lowers the base potential of T_2 allowing less collector current to flow in T_2. The decrease in collector current, I_{c2}, decreases the voltage drop across R_L allowing the collector potential of T_2 to rise. This in turn raises the base potential of T_1 which continues to increase I_{c1}. Thus a regenerative effect exists which continues until T_2 is cut off and T_1 is conducting heavily. Similarly, with

T_1 initially "on" and T_2 "off", a trigger pulse could be applied which would decrease I_{c1} causing T_2 to turn "on" through the same regenerative action.

Since the collector potential of either transistor is quite sensitive to changes in base voltage, the tolerance in components must be small to insure proper operation. In order to accommodate some variation in component values along with changes in transistor characteristics caused by deterioration, the flip-flop is adjusted so that one transistor is conducting heavily, almost into saturation, while the other is well below cutoff in one stable state. Saturation is avoided because of the longer transition time required to bring the transistor out of saturation and into the other stable state.

The speed with which this regenerative change in state takes place is limited by the junction capacitances of the transistor, which in turn determine the transistor cutoff frequency, f_α . The transition time from one state to another can be greatly improved by placing capacitors C_e and C_c in parallel with resistors R_e and R_c respectively for compensation.[7] For a present day transistor, the expected transition time is of the order of a microsecond.

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[7]Jacob Millman & Herbert Taub, Pulse and Digital Circuits, McGraw-Hill, New York, 1957, pp. 140-159.

Algebraic Analysis of the Bistable Operation

Before a more complete understanding of a bistable transistor multivibrator is possible, an algebraic analysis must be presented to better describe the bistable operation of the multivibrator. It was shown in the preceding section that two stable states exist--one when T_1 is "on" and T_2 is "off"; the other when T_2 is "on" and T_1 is "off". Because of this dual stability and the fact that the flip-flop circuit is symmetrical, it is acceptable to begin with T_2 "on" and T_1 "off" and write the circuit equations, knowing they will hold for T_2 "off" and T_1 "on".

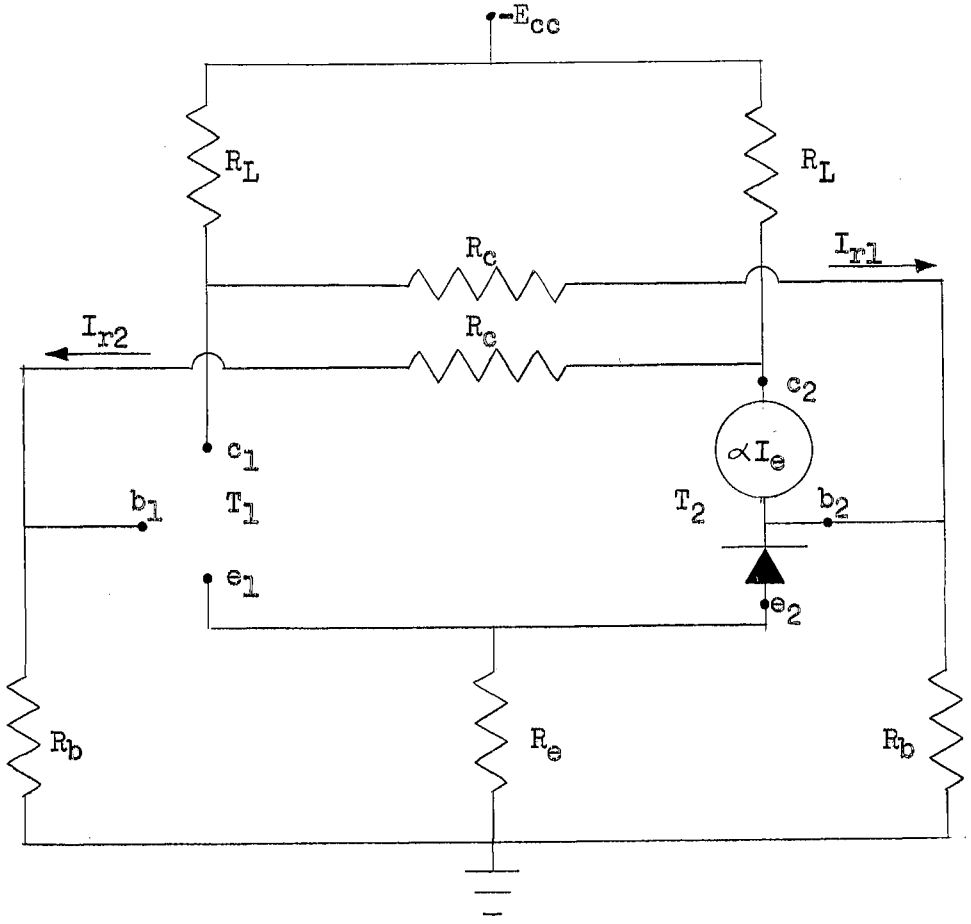

Figure 5. Low Frequency Flip-Flop Equivalent Circuit.

The equivalent circuit for Figure 4 with T_1 "off" and T_2 "on" is shown in Figure 5. By connecting the emitters together and using a single emitter resistor, R_e, an operating condition is established which permits one of the transistors to be cut off when the other is conducting. This would not be possible when using separate emitter resistors without additional d-c bias. Since this is a steady-state circuit analysis, the pulse-shaping capacitors C_c and C_e are considered non-applicable and are omitted from the equivalent circuit of Figure 5.

For T_1 to be "off" and T_2 to be "on", when using pnp transistors, the base voltage of T_1, V_{b1}, must be less negative than the emitter voltage, V_e; and for T_2 to be "on", its base voltage, V_{b2}, must be more negative than V_e. This means that the requirements for the existence of one stable state are $V_{b2} < V_e$ and $V_{b1} > V_e$. Note that V_e is the same for both transistors.

The use of Kirchhoff's voltage law to obtain the effect of the supply voltage, $-E_{cc}$, on V_{b2} and Kirchhoff's current law to determine the effect of the base current, I_{b2}, on V_{b2} gives:

$$V_{b2} = \frac{-E_{cc} R_b}{R_b + R_c + R_L} + \frac{I_b R_b (R_c + R_L)}{R_b + R_c + R_L}$$

Substituting $I_b = I_e(1 - \alpha)$ and rewriting

$$V_{b2} = \frac{-E_{cc} R_b}{R_b + R_c + R_L} + \frac{I_e(1 - \alpha) R_b(R_c + R_L)}{R_b + R_c + R_L} \qquad (1)$$

Obtaining V_{b1} in the same way,

$$V_{b1} = \frac{-E_{cc} R_b}{R_b + R_c + R_L} + \frac{I_c R_b R_L}{R_b + R_c + R_L},$$

substituting $I_c = \alpha I_e$ and rewriting

$$V_{b1} = \frac{-E_{cc} R_b}{R_b + R_c + R_L} + \frac{\alpha I_c R_b R_L}{R_b + R_c + R_L}. \qquad (2)$$

Combining equations (1) and (2) to obtain $V_{b2} < V_{b1}$,

$$\frac{-E_{cc} R_b}{R_b + R_c + R_L} + \frac{I_e(1 - \alpha) R_b(R_c + R_L)}{R_b + R_c + R_L}$$

$$< \frac{-E_{cc} R_b}{R_b + R_c + R_L} + \frac{\alpha I_e R_b R_L}{R_b + R_c + R_L},$$

subtracting equals from each side of the inequality sign leaves,

$$\frac{I_e(1 - \alpha) R_b(R_c + R_L)}{R_b + R_c + R_L} < \frac{\alpha I_e R_b R_L}{R_b + R_c + R_L}.$$

Dividing by $\frac{I_e R_b}{R_b + R_c + R_L}$ results in $(1 - \alpha)(R_c + R_L) < \alpha R_L$.

Rearranging $R_c(1 - \alpha) < \alpha R_L - R_L(1 - \alpha) = R_L(2\alpha - 1)$

$$\frac{R_c}{R_L} < \frac{2\alpha - 1}{1 - \alpha}. \qquad (3)$$

Thus the relationship between R_c and R_L has been established for a given α, where $\alpha = I_c/I_e$ for each transistor.

To assure that the flip-flop does not operate into the saturation region, it is required that $V_{b2} > V_{c2}$. Since $V_e > V_{b2}$, it follows that $V_e > V_{c2}$ or

$$-I_e R_e > \frac{-E_{cc}(R_b + R_c)}{R_b + R_c + R_L} + \frac{\alpha I_e R_L(R_b + R_c)}{R_b + R_c + R_L} . \qquad (4)$$

Changing signs in the above expression, it becomes

$$I_e R_e < \frac{-E_{cc}(R_b + R_c)}{R_b + R_c + R_L} - \frac{\alpha I_e R_L(R_b + R_c)}{R_b + R_c + R_L}$$

collecting terms and solving for I_e

$$I_e < \frac{\dfrac{E_{cc}(R_b + R_c)}{R_b + R_c + R_L}}{R_e + \dfrac{\alpha R_L(R_b + R_c)}{R_b + R_c + R_L}} . \qquad (5)$$

To assure that I_e is less than that indicated in equation (5), set

$$-I_e = \frac{V_{b2}}{R_e} = \frac{V_e}{R_e}$$

then $$-I_e R_e = V_{b2} = \frac{-E_{cc} R_b}{R_b + R_c + R_L} + \frac{I_e(1 - \alpha)R_b(R_c + R_L)}{R_b + R_c + R_L}$$

collecting terms and solving for I_e

$$I_e = \frac{\dfrac{E_{cc} R_b}{R_b + R_c + R_L}}{R_e + \dfrac{(1 - \alpha) R_b (R_c + R_L)}{R_b + R_c + R_L}} . \qquad (6)$$

The output voltage for the "on" transistor, T_2, is

$$V_{c2} = \frac{I_c R_L (R_b + R_c)}{R_b + R_c + R_L} - E_{cc} .$$

The output voltage for the "off" transistor, T_1, is

$$V_{c1} = \frac{I_b R_b R_L}{R_b + R_c + R_L} - E_{cc} .$$

The output voltage swing, ΔV_c, is then

$$\Delta V_c = V_{c2} - V_{c1} = \frac{I_c R_L (R_b + R_c)}{R_b + R_c + R_L} - E_{cc} - \left[\frac{I_b R_b R_L}{R_b + R_c + R_L} - E_{cc} \right]$$

$$\Delta V_c = I_e \left[\frac{\alpha R_L (R_b + R_c)}{R_b + R_c + R_L} - \frac{(1 - \alpha) R_b R_L}{R_b + R_c + R_L} \right] . \qquad (7)$$

Since I_e has been set at $-V_{b2}/R_e$,

$$R_e = \frac{-V_{b2}}{R_e} = \frac{E_{cc}}{I_e} \cdot \frac{R_b}{R_b + R_c + R_L} \quad .$$

Let: $\gamma = R_c/R_L$, $A = E_{cc}/I_e$

then, $$R_e = \frac{A\,R_b}{R_b + (\gamma + 1)R_L} \quad . \qquad (8)$$

Substituting equation (8) into (5)

$$I_e < \frac{\dfrac{E_{cc}(R_b + R_c)}{R_b + R_c + R_L}}{\dfrac{A\,R_b}{R_b + R_c + R_L} + \dfrac{\alpha R_L(R_b + R_c)}{R_b + R_c + R_L}}$$

then, $$\frac{I_e}{E_{cc}} < \frac{R_b + R_c}{A\,R_b + \alpha R_L(R_b + R_c)}$$

inverting, $$\frac{E_{cc}}{I_e} > \frac{A\,R_b + \alpha R_L(R_b + R_c)}{R_b + R_c} = \frac{A\,R_b}{R_b + R_c} + \alpha R_L \quad .$$

Solving for R_b, $$(R_b + R_c)\left(\frac{E_{cc}}{I_e} - \alpha R_L\right) > A\,R_b$$

$$\frac{E_{cc}}{I_e} R_c - \alpha R_c R_L > A\,R_b + \alpha R_L R_b - \frac{E_{cc} R_b}{I_e}$$

Substituting $A = E_{cc}/I_e$ and $\gamma = R_c/R_L$

$$R_b(A + \alpha R_L - A) < R_c(A - \alpha R_L)$$

$$R_b < \frac{A R_c}{\alpha R_L} - \frac{\alpha R_c R_L}{\alpha R_L} = \frac{A\gamma}{\alpha} - \gamma R_L \text{ .}$$

Since $\alpha < 1$ is always true for junction transistors, then $R_b < A\gamma/\alpha - \gamma R_L$ will hold as $\alpha = 1$ is set. Thus

$$R_b = A\gamma - \gamma R_L = \gamma(A - R_L) \text{ .} \qquad (9)$$

Substituting into equation (7) the following: $A = E_{cc}/I_e$, $R_c = \gamma R_L$, $R_b = \gamma(A - R_L)$, and $\rho = E_{cc}/\Delta V_c$;

$$\Delta V_c = I_e \left[\frac{\alpha R_L(R_b + R_c) - (1 - \alpha)R_b R_L}{R_b + R_c + R_L}\right]$$

$$\Delta V_c = \frac{E_{cc}}{A} \left[\frac{\alpha R_L \left[\gamma(A - R_L) + \gamma R_L\right] - (1 - \alpha)R_L \gamma(A - R_L)}{\gamma(A - R_L) + \gamma R_L + R_L}\right]$$

$$\frac{\Delta V_c}{E_{cc}} = \frac{1}{\rho} = \frac{1}{A} \left[\frac{\alpha R_L \gamma(A - R_L + R_L + A - R_L) - R_L \gamma(A - R_L)}{\gamma A - \gamma R_L + \gamma R_L + R_L}\right]$$

$$\rho = \frac{A^2\gamma + A R_L}{\gamma A R_L(2\alpha - 1) + R_L^2 \gamma(1 - \alpha)} \text{ .}$$

Rearranging as a quadratic equation in R_L

$$\gamma\rho(1 - \alpha)R_L^2 + \left[\gamma\rho A(2\alpha - 1) - A\right] R_L - \gamma A^2 = 0$$

Solving for R_L

$$R_L = \frac{-A\left[\delta\rho(2\alpha - 1) - 1\right] - A\left\{\left[\delta\rho(2\alpha - 1) - 1\right]^2 + 4\delta^2\rho(1 - \alpha)\right\}^{\frac{1}{2}}}{2\delta\rho(1 - \alpha)} \qquad (10)$$

These equations compose a set which expresses the unknown circuit component, R_b, R_c, R_e, and R_L, in terms of parameters which appear as specifications for the design of the flip-flop circuit.[8] The equations used are almost exact equations; i. e., few approximations have been made, the main one being that the circuit is linear. At the same time they are very lengthy and difficult to solve. While these equations provide a good mathematical presentation of bistable operation, their accuracy is, in fact, greater than the consistency of the parameters (namely α) for various transistors. Because of the amount by which α differs for each transistor, the accuracy of these equations is not necessary for circuit design. Hence, another method of analysis follows which is more general and more approximate.

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[8] Robert E. McMahon, "Designing Transistor Flip-Flops", Electronic Design, October 1955, pp. 24-27.

Algebraic Analysis of the Flip-Flop

While the preceding method of analysis provided a rather thorough mathematical representation of the bistable operation, it did not provide a simple and general method for flip-flop design. By taking a different approach to the analysis and making some intelligent assumptions, a more general and more applicable method of analysis results which will now be presented. Referring to the schematic diagram of Figure 4 and the corresponding equivalent circuit of Figure 5, consider the general analysis of the flip-flop.

There are certain operating conditions of the flip-flop, such as the two operating points, that must be selected with respect to the transistor characteristics used. They are; E_{cc}, I_e, ΔV_c, and β.[9] It is the purpose of this part of the thesis to derive equations for the unknowns R_b, R_c, R_e, and R_L in terms of E_{cc}, I_e, ΔV_c, and β, the latter group of which is either selected or otherwise specified for optimum operation. Since a negative power supply voltage is required for pnp transistors, it is designated $-E_{cc}$, where E_{cc} is positive.

To obtain maximum switching speed upon receiving an input trigger pulse, the bistable multivibrator must operate without saturating either transistor. Thus, with T_1 "off" and T_2 "on" in one of two stable states, the requirements are that $V_{b1} > V_e$ and $V_e - V_{c2} > 0.2$ volts[10] respectively.

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[9] $\beta = \dfrac{\alpha}{1-\alpha}$

[10] See Appendix A.

Consider the regenerative feedback circuitry consisting of R_b, R_c, and the input impedances of T_1 and T_2. With T_1 "off" and T_2 "on", the loading effect of the regenerative circuitry of T_2 on T_1 is an impedance $Z_2 \cong R_c + \beta R_b R_e/(R_b+\beta R_e)$, where βR_e is the input impedance[11] of T_2. Since T_1 is biased "off", the regenerative circuitry is actually not loading T_1, but merely drawing current from $-E_{cc}$, the effect of which is to make V_{c1} less negative. Thus the loading effect of Z_2 on T_1 is negligible. Since T_1 is "off", $I_{b1} \cong 0$. Thus, the loading effect of the regenerative circuitry for T_1 on T_2 is an impedance $Z_1 \cong R_c + R_b$. If R_c and R_b are made large enough, their loading effect will be negligible compared to R_L. For example, for $\beta \cong 32.3$ and $I_e \cong 3$ ma (minimum β and allowable emitter current of the transistors available) the current required to turn T_2 "on" is 3% of I_e or 0.09 ma. $\left[I_b \cong (1 - \alpha)I_e \cong (1 - 0.97)I_e \cong 0.03I_e \cong 0.09 \text{ ma}\right]$. Even with a slightly greater current required for regenerative feedback, this current, required for the feedback network of R_b in parallel with the input impedance of T_2, is negligible compared with $I_e \cong 3$ ma. As β increases, this feedback current decreases.

Neglecting the loading effect of the regenerative feedback circuitry, and keeping in mind that R_b and R_c are to be made as large as possible.

$$-E_{cc} \cong I_e(R_e + R_L) - 0.2$$

$$I_e \cong \frac{-E_{cc}}{R_e + R_L} .$$

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[11] See Appendix B.

Let $\Delta V_c = V_{c1} - V_{c2}$, which is the voltage swing of the collector of each transistor as operation changes from one stable state to the other. It is logical that ΔV_c must swing over the mid-range of the $-E_{cc}$-to-ground potential such that

$$V_{c2} = \frac{-E_{cc} + \Delta V_c}{2}$$

$$V_{c1} = V_{c2} - \Delta V_c = \frac{-E_{cc} - \Delta V_c}{2} .$$

For T_2 "on" to operate without saturating, $V_e - V_{c2} > 0.2$ volts is required. To obtain maximum voltage swing, operation must be as near saturation as possible, which is $V_e - V_{c2} \cong 0.2$ volts. Enough information is now available to begin solving for the unknown curcuit components:

$$R_e = \frac{V_e}{I_e} = \frac{V_{c2} + 0.2}{I_e} = \frac{1}{I_e}\left[\frac{-E_{cc} + \Delta V_c}{2} + 0.2\right]$$

$$R_e = \frac{-E_{cc} + \Delta V_c + 0.4}{2I_e} . \qquad (11)$$

To find R_L:

$$I_e R_L = -E_{cc} - V_{c2} = -E_{cc} - \frac{-E_{cc} + \Delta V_c}{2}$$

$$R_L = \frac{-E_{cc} - \Delta V_c}{2I_e} . \qquad (12)$$

With T_2 "on", $$V_{b2} \cong V_{c2} = \frac{-E_{cc} + \Delta V_c}{2}, \quad V_{c1} = \frac{-E_{cc} - \Delta V_c}{2}.$$

From the equivalent circuit of Figure 5,

$$V_{b2} = \frac{-E_{cc} \dfrac{R_b \beta R_e}{R_b + \beta R_e}}{R_L + R_c + \dfrac{R_b \beta R_e}{R_b + \beta R_e}}$$

$$= \frac{-V_{c1} \dfrac{R_b \beta R_e}{R_b + \beta R_e}}{R_c + \dfrac{R_b \beta R_e}{R_b + \beta R_e}}, \tag{13}$$

where βR_e is the input impedance of T_2 "on".

Let the current through R_c be I_{r1}. Then,

$$I_{r1} = \frac{V_{c2} - V_{c1}}{R_c} = \frac{\Delta V_c}{R_c} \tag{14}$$

But I_{r1} also flows into the impedance $\dfrac{R_b \beta R_e}{R_b + \beta R_e}$ such that

$$V_{b2} = I_{r1} \frac{R_b \beta R_e}{R_b + \beta R_e} = \frac{\Delta V_c R_b \beta R_e}{R_c (R_b + \beta R_e)}. \tag{15}$$

Solving equation (15) for R_c

$$R_c = \frac{\Delta V\, R_b\, \beta\, R_e}{V_{b2}(R_b + \beta R_e)} \quad . \tag{16}$$

Let $$B = \frac{R_b\, \beta\, R_e}{R_b + \beta R_e}$$

then $$R_c = \frac{\Delta V_c\, B}{V_{b2}} \quad . \tag{17}$$

Rewriting equation (13) in terms of B

$$V_{b2} = \frac{-E_{cc}\, B}{R_c + R_L + B} \quad , \tag{18}$$

substituting equation (17) into (18)

$$V_{b2} = \frac{-E_{cc}\, B}{\frac{\Delta V_c\, B}{V_{b2}} + R_L + B} = \frac{-E_{cc}}{\frac{\Delta V_c}{V_{b2}} + \frac{R_L}{B} + 1} \quad ,$$

substituting for B its original value

$$V_{b2} = \frac{-E_{cc}}{\frac{\Delta V_c}{V_{b2}} + \frac{R_L(R_b + \beta R_e)}{R_b\, \beta\, R_e} + 1} \quad ,$$

$$V_{b2} = \frac{-E_{cc}}{\frac{R_L}{\beta R_e} + \frac{R_L}{R_b} + \frac{\Delta V_c}{V_{b2}} + 1} \quad . \tag{19}$$

Rearranging and solving for R_b

$$\frac{V_{b2} R_L}{\beta R_e} + \frac{V_{b2} R_L}{R_b} + \Delta V_c + V_{b2} = -E_{cc}$$

$$\frac{V_{b2} R_L}{R_b} = -E_{cc} - \frac{V_{b2} R_L}{\beta R_e} - \Delta V_c - V_{b2}$$

$$R_b = \frac{V_{b2} R_L}{-E_{cc} - \frac{V_{b2} R_L}{\beta R_e} - \Delta V_c - V_{b2}} . \qquad (20)$$

Substituting R_b of equation (20) into equation (16) allows R_c to be determined. Thus the unknown components have been determined in terms of known parameters.

Numerical Systhesis of the Flip-Flop

While the unknown circuit components of the flip-flop have been derived in terms of the parameters E_{cc}, I_e, ΔV_c, and β, these parameters have not yet been given numerical values. It is the purpose of this section to show how these terms are given numerical meaning and to discuss their limitations and dependence upon the transistors selected. As this is done, these parameters are used according to the equations of the preceding section to obtain numerical values for the unknown circuit components. Reference is again made to the schematic diagram of Figure 4 and the corresponding equivalent circuit of Figure 5.

The transistors available for use were IBM Type 08. These pnp transistors had values of β ranging from 35 to 200, with a mean value near 100. Because of the limited quantity of transistors with nearly the same β, the transistors selected for use were those having β near 100. Hence, β is fixed by the transistors available.

The power supply voltage must now be determined. Using pnp transistors, it must be negative; so the power supply voltage will be designated $-E_{cc}$, where E_{cc} is positive. Since the transistors selected were rated for a minimum punch-through voltage of 15 volts, choose $E_{cc} = 15$ volts to insure that no more than 15 volts will ever appear from the collector to the emitter of either transistor. Because of R_L and R_e in series with the transistor, this voltage will always be less than 15 volts.

An operating current, I_e, for the transistor that is "on", must be chosen large enough so that a change in I_{co} with temperature will produce negligible change in I_e, but small enough so as not to exceed

the power rating of the transistor. For the transistors selected, the maximum $I_{co} = 50$ microamperes and the maximum $I_e = 7$ ma. Experimentally, $I_e = 3$ ma seemed to be the best choice.

To obtain maximum switching speed, the flip-flop must operate without saturating. For nonsaturating operation $V_e - V_{c2} > V_{eb} \cong 0.2$ volt.[12] But in order to gain maximum voltage swing, ΔV_c, operation must be as near saturation as possible. Hence, assume $V_e - V_{c2} \cong 0.2$ volt. Then for T_2 "on",

$$-E_{cc} = I_e(R_e + R_L) - 0.2.$$

The operating point for T_2 "on" is shown on the transistor characteristics of Figure 6 as the point $I_c = 0.3$ ma, $V_c = 0.2$ volt. This is very near the saturation region, which is to the left of the knee of the characteristic curves. The load resistance $R_e + R_L$ is represented by the d-c load line from which the value of $R_e + R_L$ is determined to be

$$\frac{\Delta V_c}{\Delta I_c} \cong \frac{15 \text{ volts}}{3.1 \text{ ma}} \cong 4.8 \text{ K}.$$

For maximum stability and minimum switching time, many flip-flop designs[13] use a collector voltage swing of approximately $\Delta V_c = |E_{cc}/2|$. However, in order to obtain maximum voltage swing without sacrificing stability or switching time, use $\Delta V_c > |E_{cc}/2|$; choose $\Delta V_c = 10$ volts.

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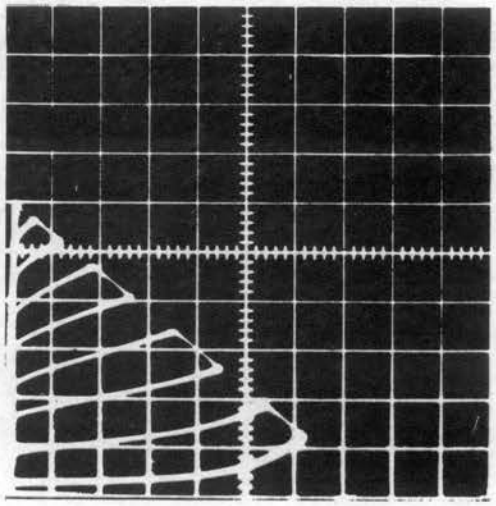
[12] See Appendix A.

[13] J. J. Suran and R. A. Reibert, "Two-Terminal Analysis and Synthesis of Junction Transistor Multivibrators", IRE Transactions, Vol. CT-3, March 1956, p. 37.



Horizontal: 2 volts/division

Vertical: 0.5 ma/division

Adjacent curves: 0.005 ma/step

Load line: R_L = 5 K

Figure 6. Transistor Characteristics for IBM Type 08.

Note that ΔV_c can always be decreased by increasing R_e; this in turn increases stability due to current feedback.

At this point it is desirable and only logical that ΔV_c must swing over the mid-range of the $-E_{cc}$-to-ground potential. This means that for T_2 "on" and T_1 "off";

$$V_{c2} = \frac{-E_{cc} + \Delta V_c}{2} = \frac{-15 + 10}{2} = -2.5 \text{ volts}$$

$$V_{c1} = V_{c2} - \Delta V_c = -2.5 - 10 = -12.5 \text{ volts}$$

$$R_e = \frac{V_{e2}}{I_e} = \frac{V_{c2} + 0.2}{3 \text{ ma}} = 766 \text{ ohms}$$

$$R_L = R_L + R_e - R_e = 4{,}800 - 766 \cong 4 \text{ K}$$

For T_1 to be "off" and T_2 to be "on" without saturating, it is required that $V_{b1} > V_{e1}$ and $V_{b2} > V_{c2}$ respectively. But to operate T_2 near saturation, set $V_{b2} \cong V_{c2} = -2.5$ volts. Since $\beta = 100$ for most of the transistors on hand and $I_e = 3$ ma as previously chosen, then

$$I_b = \frac{I_e}{\beta} = \frac{3 \text{ ma}}{100} = 0.03 \text{ ma.}$$

Now, let I_{r1} be sufficiently large to furnish enough base current, I_{b2}, to turn T_2 "on", plus sufficient additional current for bias stabilization through R_c and R_b. In order to make valid the previous assumption that the current drawn by the biasing resistors R_c and R_b and T_2 is negligible compared with $I_e = 3$ ma, I_{r1} must be kept small enough so as not to load the T_1 side of the flip-flop and draw excessive current. For $\beta = 100$, the base current, I_{b2}, required to turn T_2 "on" is approximately 1% of I_e. Furthermore, the current required to turn "on" and properly bias T_2 is taken from the T_1 side at a time when T_1 is "off"; hence, T_2 does not load T_1. Also, T_1 does not load T_2 when T_2 is "on" and T_1 is "off". For $I_b = 0.03$ ma, let $I_{r1} = 0.3$ ma. = 10% of I_e. Then

$$\frac{V_{c1}}{I_{r1}} = \frac{-12.5}{0.3 \text{ ma}} = 41.6 \text{ K} = R_c + \frac{R_b \beta R_e}{R_b + \beta R_e} \qquad (21)$$

but

$$R_c = \frac{\Delta V_c}{I_{r1}} = \frac{-10}{-0.3 \text{ ma}} = 33 \text{ K} . \qquad (22)$$

Substituting equation (22) into (21) and solving for R_b

$$\frac{R_b \beta R_e}{R_b + \beta R_e} = 41.6 \text{ K} - R_c = 41.6 \text{ K} - 33 \text{ K} = 8.6 \text{ K} \qquad (23)$$

but $\beta R_e = (100)(766) = 76.6 \text{ K}$

$$R_b(76.6 \text{ K}) = 8.6 \text{ K} (R_b + 76.6 \text{ K})$$

$$R_b(76.6 \text{ K} - 8.6 \text{ K}) = 660 \times 10^6$$

$$R_b = \frac{660 \times 10^6}{68 \times 10^3} = 9.7 \text{ K}$$

The loading effect of the regenerative feedback circuitry (R_e and R_c) is on the transistor which is turned "on", or T_2 in this case. It is equivalent to placing $R_c + R_b$ in parallel with R_L. But $R_c + R_b = 42.7$ K, or 9.35% of the 4 K load resistance, R_L. Compared with the variation in transistor parameters, the load of the regenerative feedback circuitry on T_1 and T_2 is negligible for purposes of design calculation. However, increasing R_L to compensate for this loading effect would be quite in order to make calculations more exact.

Experiment has shown that care must be taken not to make I_{r1} too small by choosing values of R_b and R_c which are too large. While R_b and R_c are bias resistors, they are also discharge paths for the junction capacitances of T_1 and T_2 and any other capacitances which might be inserted into the circuit for pulse shaping purposes. Consequently, R_b and R_c should be made as small as possible, without drawing excessive

current, in order to obtain maximum switching speed and stability of operating point. Therefore, optimum design calls for R_b and R_c to be large enough so as not to load the flip-flop circuit, but small enough to obtain maximum switching speed with minimum rise and fall times. These conclusions were verified by experiment.

It has previously been established that the flip-flop shall operate non-saturating; i. e., when T_2 is "on", the operating point is not in the saturation region of the transistor. However, with all the approximations and assumptions that have been made in calculating R_e, R_L, R_b, and R_c; the resulting flip-flop may or may not operate without saturating. This is especially true because the operating point for T_2 "on" was selected in the non-saturating region but as near to saturation as possible in order to gain maximum output voltage swing, ΔV_c. However, any adjustment of the operating point either toward saturation or away from saturation can easily be made experimentally by slightly changing the value of R_b until the proper operating point is obtained. For example, the calculated value of $R_b \cong 10$ K gave an operating point that was slightly in the saturation region. By reducing R_b to 8.2 K, the operating point was brought out of the saturation region for optimum operation. This experimental adjustment is possible and also necessary because R_b is dependent upon β, as shown in equation (23). This dependence is such that a change to transistors of higher β requires that R_b be decreased.

CHAPTER IV

THE "AND" AND "OR" CIRCUITS

Introduction

It is very necessary that the individual computer operations, such as addition, subtraction, multiplication, transfer, storage, etc., occur at the right instant of time. Otherwise, for example, addition might occur before the addend has been transferred to the addend register, or a storage operation might occur when the proper information is not available for storage. Failure is always the result when operations are not timed for proper sequence. In computer operation, time is measured in microseconds. Each operation normally requires only a few microseconds for its completion, and many operations occur simultaneously. As a result of such rapid operation, the timing of the individual operations must usually be controlled to within a microsecond.

At present, the most feasible means to accomplish precise timing is with pulses of electrical energy. Pulses with widths in the order of a few microseconds and with rise and fall times in the millimicrosecond range are now easily generated and are quite practical for timing electronic circuitry. The adder circuit presently under consideration must include the necessary circuitry for commanding the "add" operation at the right instant of time. It is the "and"

circuit which incorporates the timing pulses (called "add pulses") into the add operation. The "and" circuit allows the add pulse to pass through and complement the augend flip-flop when the addend register contains a "1" as depicted in Figure 3. This is the electronic method for adding the contents of the addend register to the augend register.

Theory of Operation of the "And" Circuit

Boolean algebra[14] lends itself to the mathematical expression of switching circuits because the digits "0" and "1", which are basic to the binary number system, can easily be represented by two different values of electrical potential. Furthermore, electrical circuits used for switching purposes readily perform the basic operations of Boolean algebra, namely "or", "and", and "not". A convenient means for representing a complex switching circuit and making obvious its operation without drawing the circuit is provided by Boolean algebra. It is the purpose of this section to explain the operation of the "and" circuit.

In Boolean algebra, the term "and" denotes the intersection of two or more sets or classes and normally conforms to the commutative and distributive laws in the same fashion as multiplication. In fact, the "and" operation is usually expressed by the multiplication symbol "." or "x". Since "0" and "1" are the only digits used to make up the complete binary number system to which Boolean algebra applies, the "and" operation applied to "0" and "1" can give only the following results:

$$0 \times 0 = 0$$
$$0 \times 1 = 0$$
$$1 \times 0 = 0$$
$$1 \times 1 = 1$$

The digits "0" and "1" can be represented electrically by two different values of d-c voltage or current. The values of voltage or current used depend upon the types of circuits selected to perform the "and" operation. These circuits could be composed of relays,

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[14] Montgomery Phister, Jr., op. cit., Chapters 3 and 4.

vacuum-tubes, transistors, or diodes. Because of the desire for miniaturization, power amplification, pulse type output from input pulses, and because of the components available, transistors were used in the "and" circuit.

In the design of a transistor "and" circuit, it is desirable that there be no shift in the operating point and that there be a maximum voltage swing at the output. This was suitably approached by choosing a signal voltage for "0" that cut off the transistor and a voltage for "1" that would drive the transistor into or very near saturation. Because maximum switching time was not a major consideration, the limitation being in the flip-flop, operation into saturation was selected as an easy means to achieve stability. In Figure 7, R_L was made large enough to prevent excessive emitter current when both transistors are turned "on". To satisfy the above requirements, "0" was represented by 0 volts and "1" by +10 volts. Experimental evidence showed this to be very satisfactory. Note that $\Delta V_c \cong 10$ volts for the flip-flop. The "and" circuit must operate satisfactorily with inputs of that magnitude.

The "and" operation can best be accomplished by connecting the transistors in series [15,16] for operation similar to the multi-grid gating vacuum-tubes, but there are two different circuit configurations which can be used. They are shown in Figures 7 and 8 where A

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[15] Lloyd P. Hunter, Handbook of Semiconductor Electronics, McGraw-Hill, New York, 1956, pp. 15-65 to 15-66.

[16] Richard F. Shea, Transistor Circuit Engineering, Wiley, New York, 1957, pp. 317-321.

and B are the two input voltages. This assembly of transistors-in-series may be connected either in grounded emitter form, as shown in Figure 7, for voltage amplification, or in the emitter follower connection, as shown in Figure 8, for current and power amplification. Since a logical circuit, such as the "and", is usually employed to drive many following stages of circuitry in modern computer usage, the emitter follower circuit of Figure 8 was chosen for development in order to supply the load power requirements.

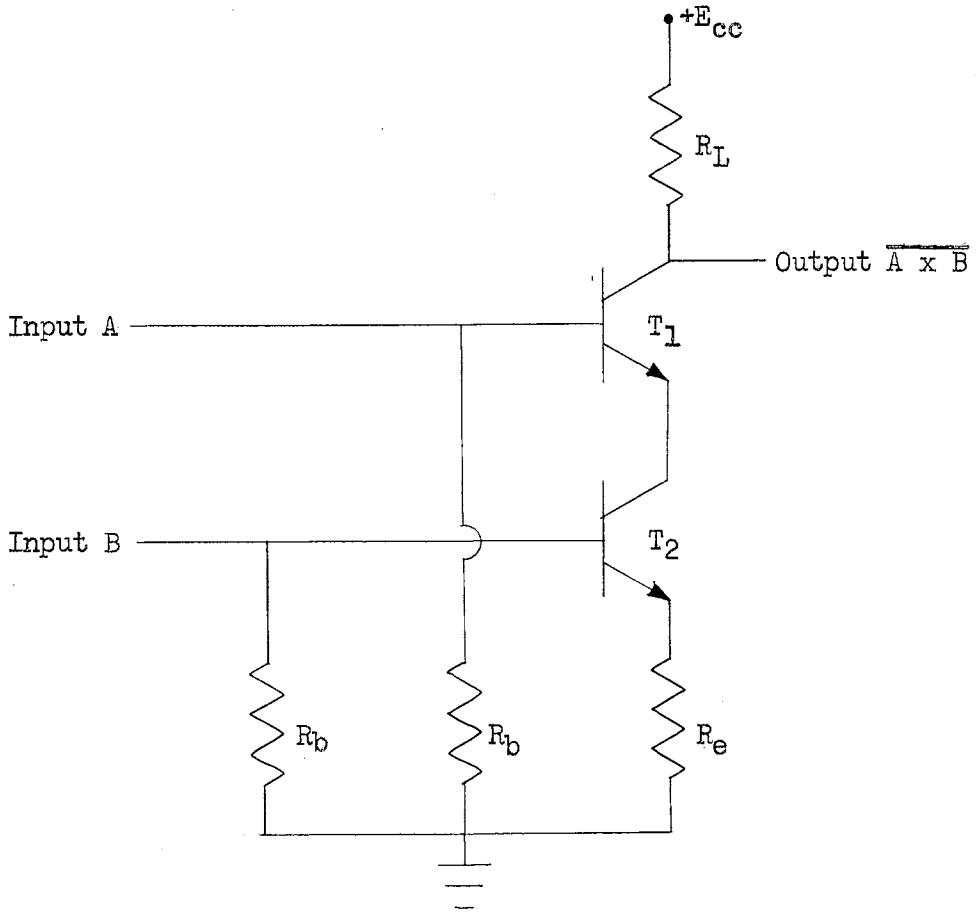

Figure 7. Grounded Emitter "And" Circuit.

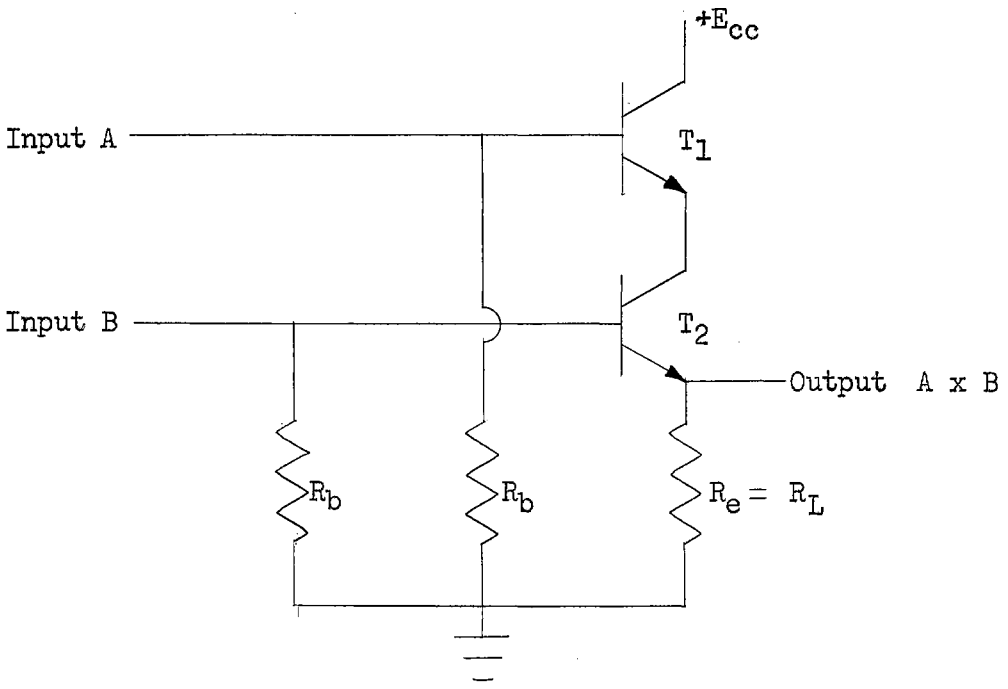

Figure 8. Emitter Follower "And" Circuit.

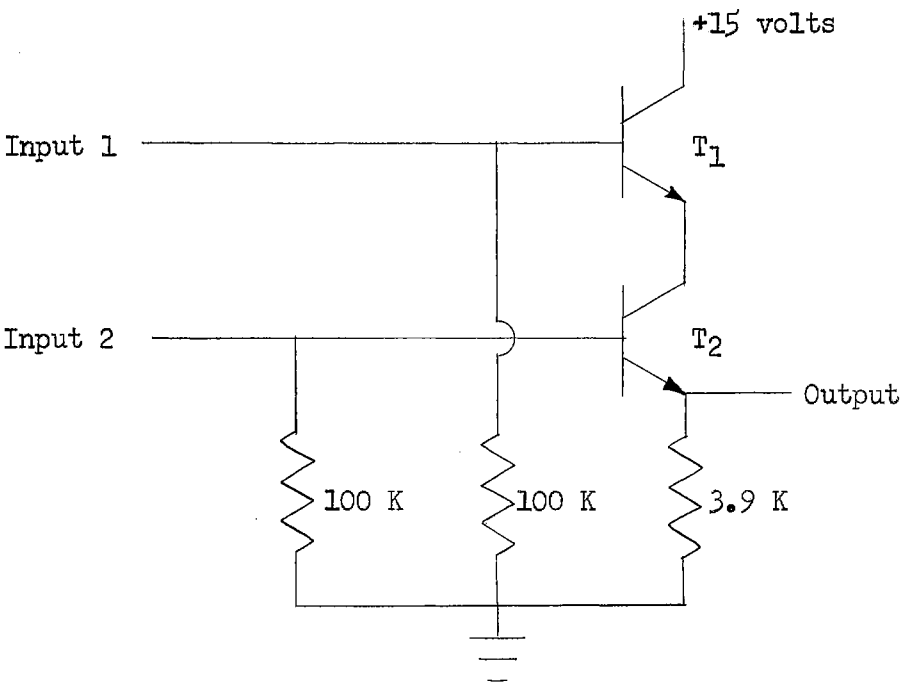

Figure 9. Typical Emitter Follower "And" Circuit.

Now, consider the curcuit operation when imputs A and B are applied in each of their possible combinations. First, let A = "0" and B = "0". This means that A = 0 volts and B = 0 volts which cause both T_1 and T_2 to be cut off. Hence, the output voltage is 0 volts satisfying the condition 0 x 0 = 0.

Let A = "0" and B = "1" which means A = 0 volts and B = 10 volts. T_2 is thus turned "on" such that $V_{c2} - V_{e2} = 0.2$ volts, but T_1 is turned "off" such that no emitter current, I_e, flows; hence, the output voltage is 0 volts satisfying the condition 0 x 1 = 0.

Let A = "1" and B = "0" which means A = 10 volts and B = 0 volts. This time T_2 is cut off and T_1 is turned "on", but no emitter current flows; hence, the output voltage is 0 volts satisfying the condition 1 x 0 = 0 as in the preceding paragraph. Note that when one transistor is "on" and the other "off", almost the entire potential of E_{cc} appears from collector to emitter of the transistor turned "off". Hence, E_{cc} must not exceed the punch-through voltage of the transistors used.

Finally, let A = "1" and B = "1" which means that both A and B equal 10 volts. Both T_1 and T_2 are turned "on" such that maximum emitter current flows; hence, maximum voltage appears across R_e equal to $I_e R_e$ making the output voltage approximately 10 volts. This satisfies the condition 1 x 1 = 1. Thus, all the possible combinations of "0" and "1" that can be applied to two inputs have been considered. This assembly of transistors-in-series is not, however, limited to two transistors. Three or more transistors can readily be connected in series to perform the "and" operation, the number required being one transistor for each input.

The preceding description of operation is true for the transistors-in-series connected in the grounded emitter configuration (Figure 7), and for small signal operation of the emitter follower connection (Figure 8). But the theory of operation fails to hold for large signal operation of the emitter follower connection of Figure 8. This was discovered experimentally when the typical "and" circuit of Figure 9 was tested. The two possible voltage levels for input 1 were selected as either 0 volts or 10 volts, making the collector voltage of T_2 approximately 0 volts or 10 volts respectively. Input 2 consisted of 2-volt pulses, 5 μsec wide, occurring at a rate of 2000 pps. The unpredicted result was that the pulses of input 2 appeared at the output with approximately the same amplitude as at input 2 regardless of whether input 1 was 0 volts or 10 volts.

The cause of this apparent feed-through from input to output illustrates the basic difference between the transistor and the vacuum tube. In normal Class A operation, the control grid of the vacuum tube is biased negatively to the extent that this grid never draws current even with maximum input signal. Conversely, the corresponding base of the npn transistor is cut off anytime the base is negative with respect to the emitter. Hence the base must normally operate in a region which is positive with respect to the emitter in which case the base draws current. As a result, when $V_{c2} = 0$, as it is when input 1 is 0 volts, the p-n junction of the base to emitter appears as a diode which passes the input signal on to the output as shown by the equivalent circuit of Figure 10, and transistor action does not exist. On the other hand, when the grid of a vacuum tube is biased negatively, this diode action cannot exist.

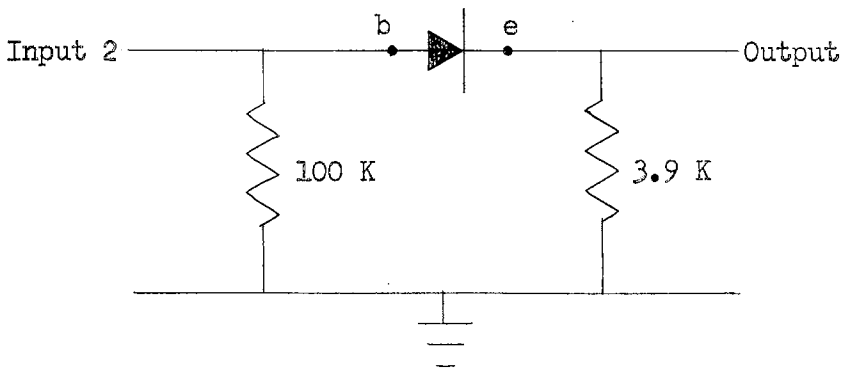

Figure 10. Diode Equivalent Circuit for T_2 "On".

When the collector potential, V_{c2}, of T_2 is approximately 10 volts, the diode action between the base and emitter of T_2 is modified to the extent that transistor action exists, and the input impedance into the base of T_2 is much greater than when V_{c2} is 0 volts. This is in agreement with transistor theory in that the diode equivalent circuit of Figure 10 is replaced by a transistor equivalent circuit which has an input impedance of βR_e, where β is the current gain for the grounded emitter configuration, and R_e is the emitter resistance external to the transistor. Since most of the transistors used in the experimental circuitry had $\beta > 50$, the input impedance was greater than 50 x 3.9 K $\cong$ 200 K. But as shown in Figure 9, this transistor input impedance is in parallel with a 100 K bias resistor making Z_i = (100 K)(200 K)/(300 K) = 67 K as shown in Figure 11. Conversely, Z_i for the diode equivalent circuit of Figure 10 is Z_i = 30 + 3.9 K $\cong$ 3.95 K, where 30 ohms is the forward resistance of the equivalent diode.

In view of the pulse feed-through problem previously discussed, the most logical thing to do would have been to discard the typical

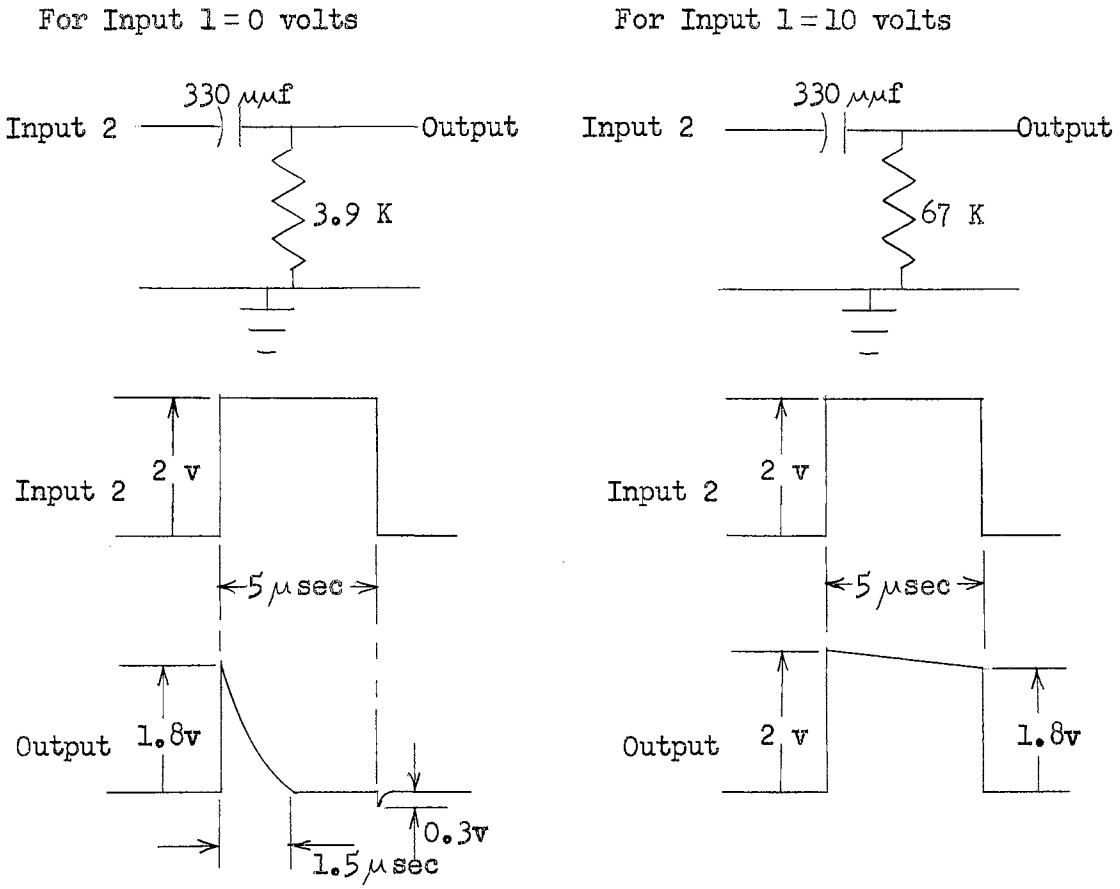

Figure 11

Equivalent Circuits and Waveforms for Capacitance Input.

circuit of Figure 8 and choose the grounded emitter configuration of Figure 7 for the "and" circuit to be used, because it was known to operate satisfactorily.[17,18] However, this would have left many problems yet unsolved concerning the emitter follower circuit. Furthermore, the output of the common emitter circuit is inverted with respect to the input, and an inverter is required to regain the "and" result. Also, the common emitter circuit provides voltage amplification, but it must be followed by an emitter follower stage if sufficient power is to be obtained to drive several following stages.

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[17] Shea, op. cit.

[18] Hunter, op. cit.

Hence, the idea of the emitter follower "and" circuit was not given up.

Experimentation revealed that it was possible to use the emitter follower "and" circuit. In fact, it was made to operate quite satisfactorily. Use was made of the fact that Z_i of input 2 is much greater when input 1 is 10 volts than when input 1 is 0 volts.

By connecting a capacitor in series with input 2, the output becomes the derivative of the input 2, but the difference in time constants is such that the output is greater when input 1 is 10 volts than when it is 0 volts. Equivalent circuits and waveforms are shown in Figure 11. It can be seen that much more pulse energy is available at the output when input 1 is 10 volts than when it is 0 volts. With the "and" circuit connected as shown in Figure 3 and with input 1 equal to 10 volts, the minimum pulse signal at input 2 required to trigger the augend flip-flop is 1.5 volts peak. Likewise, the maximum pulse signal at input 2 above which a change in input 1 from 0 volts to 10 volts has no control over triggering the augend flip-flop is 2.2 volts; i. e., when the 5 μsec pulses of input 2 are greater in peak value than 2.2 volts, the feed-through from input 2 to the output is great enough to trigger the augend flip-flop regardless of whether input 1 is 0 volts or 10 volts.

Satisfactory operation can also be obtained by inserting a resistor in series with input 2 instead of a capacitor. Pulses of 2-volt amplitudes and 5 μsec widths are again applied at input 2 as shown in Figure 11. Equivalent circuits and waveforms similar to Figure 11 are shown in Figure 12. As in Figure 11, it can be seen in Figure 12 that more pulse energy is available at the output when

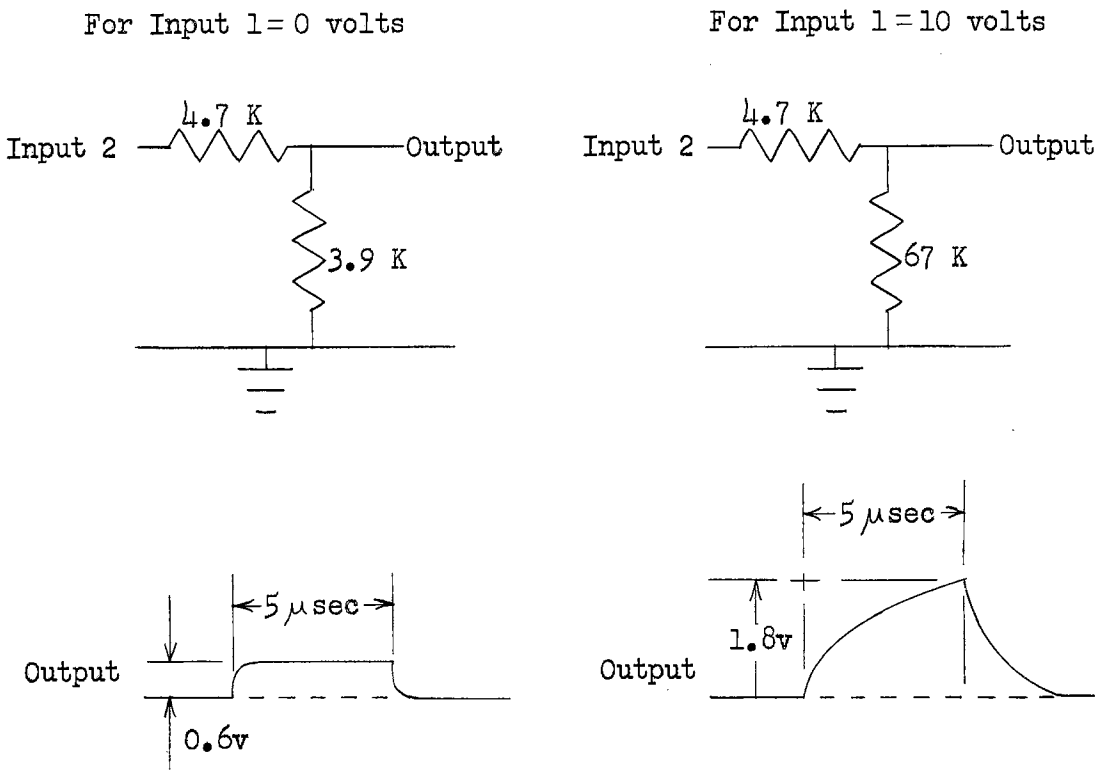

Figure 12

Equivalent Circuits and Waveforms for Resistance Input.

input 1 is 10 volts than when it is 0 volts. With the "and" circuit connected as shown in Figure 3 and with input 1 equal to 10 volts, the minimum pulse signal at input 2 required to trigger the augend flip-flop is 2.3 volts peak. Likewise, the maximum pulse signal at input 2, above which a change in input 1 from 0 volts to 10 volts has no control over triggering the augend flip-flop, is 5.8 volts. Note that the use of a series resistor allows a greater variation in the pulse amplitude of input 2 than a series capacitor. However, the rise and fall time of the output pulse for the series resistor circuit (Figure 12) is quite long; so long, in fact, that a circuit being triggered by it might receive a delay of a microsecond or two

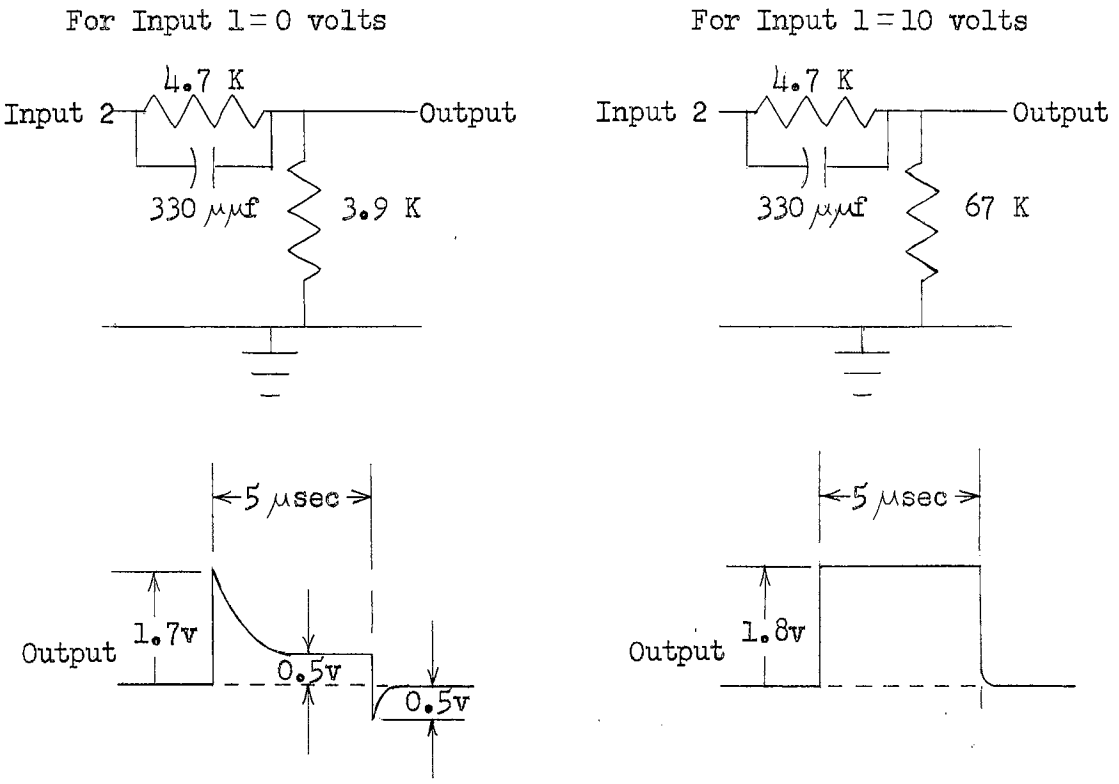

Figure 13

Equivalent Circuits and Waveforms for R-C Input.

until the amplitude of the output pulse becomes high enough to trigger the circuit. This would be unsatisfactory for miscrosecond timing.

Since the series capacitor of Figure 11 has a fast rise time but falls off rapidly as a differentiated pulse, and the series resistor of Figure 12 has a slow rise time but builds up to a maximum value within 5 μsec; a capacitor-resistor combination should be satisfactory. Equivalent circuits and waveforms of such a circuit are shown in Figure 13. Pulses of 2-volt amplitudes and 5 μsec widths are again applied at input 2 as shown in Figure 11. Note that the difference in pulse energy for input 1 = 0 volts and input 1 = 10 volts is much greater in Figure 13 than in either Figure 11 or Figure 12. With the "and" circuit connected as shown in Figure 2 and with input 1 equal to

10 volts, the minimum pulse signal at input 2 required to trigger the augend flip-flop is 1.5 volts peak. Likewise, the maximum pulse signal at input 2, above which a change in input 1 has no control over triggering the augend flip-flop, is 2.3 volts.

As a result of the above analysis and experimentation, the final "and" circuit that was selected is shown in Figure 14. Note that the effective feed-through can be further reduced by decreasing the emitter resistance, R_e, which in turn lowers the input impedance. This has a shunting effect upon the input pulses which reduces the output when either transistor is cut off. If it were deemed necessary to decrease R_e, the same analysis used in the preceding pages can be used to arrive at a new final circuit. For minimum feed-through, R_e must be as small as possible, yet large enough to prevent excessive emitter current through T_1 and T_2 and large enough to make the input impedance sufficiently high so as not to load the preceding circuitry excessively.

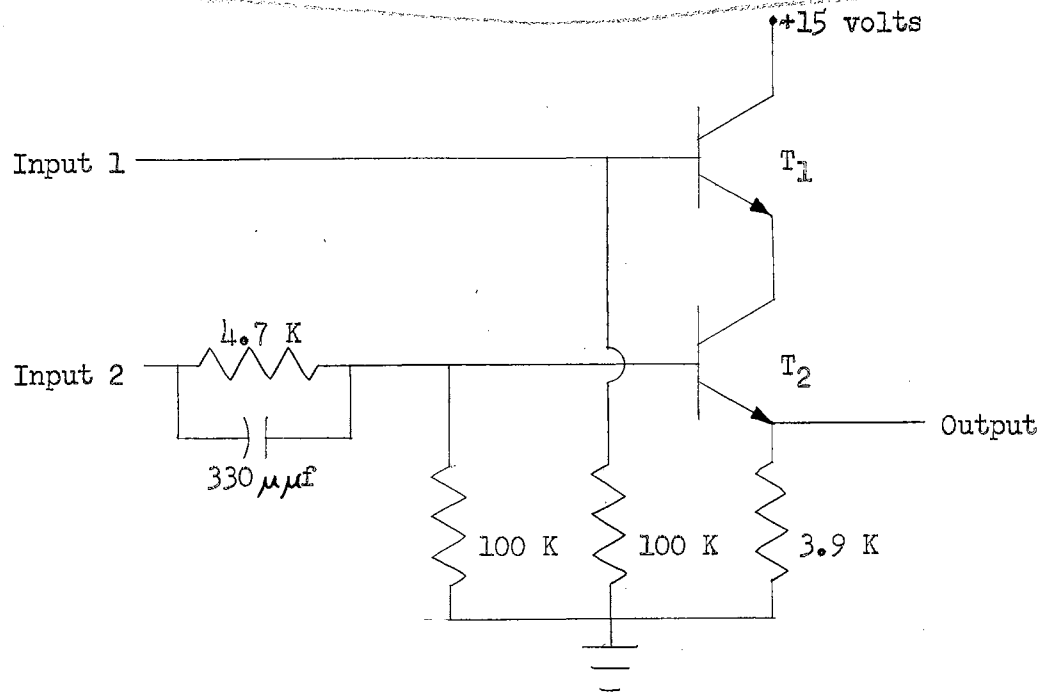

Figure 14. Final Emitter Follower "and" Circuit.

Theory of Operation of the "Or" Circuit

Whereas "and" is the Boolean algebra expression represented by the multiplication symbol "x", "or" is the boolean algebra expression represented by the addition symbol "+". Since "0" and "1" are the only digits used to make up the complete binary number system to which Boolean algebra applies, the "or" operation applied to "0" and "1" can give only the following results:

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 1$$

In general, the same circuit requirements which exist for the "and" circuit also exist for the "or" circuit; i. e., the requirements for power and switching speed of both the "and" and "or" circuits are essentially the same. Therefore, transistors were chosen to perform the "or" operation in order to obtain miniaturization, power amplification, pulse type output from input pulses, and because of the components available.

To assure no shift in operating point and to provide maximum voltage swing at the output, a voltage should be chosen for "0" that will cut off the transistor to which it is applied. Likewise, a voltage should be chosen for "1" that will drive the transistor, to which "1" is applied, either into or very near saturation. R_L must be made large enough to prevent excessive emitter current when either or both transistors are turned "on". To satisfy the above requirements, "0" was represented by 0 volts and "1" by 10 volts. (This was verified by experiment to be very satisfactory).

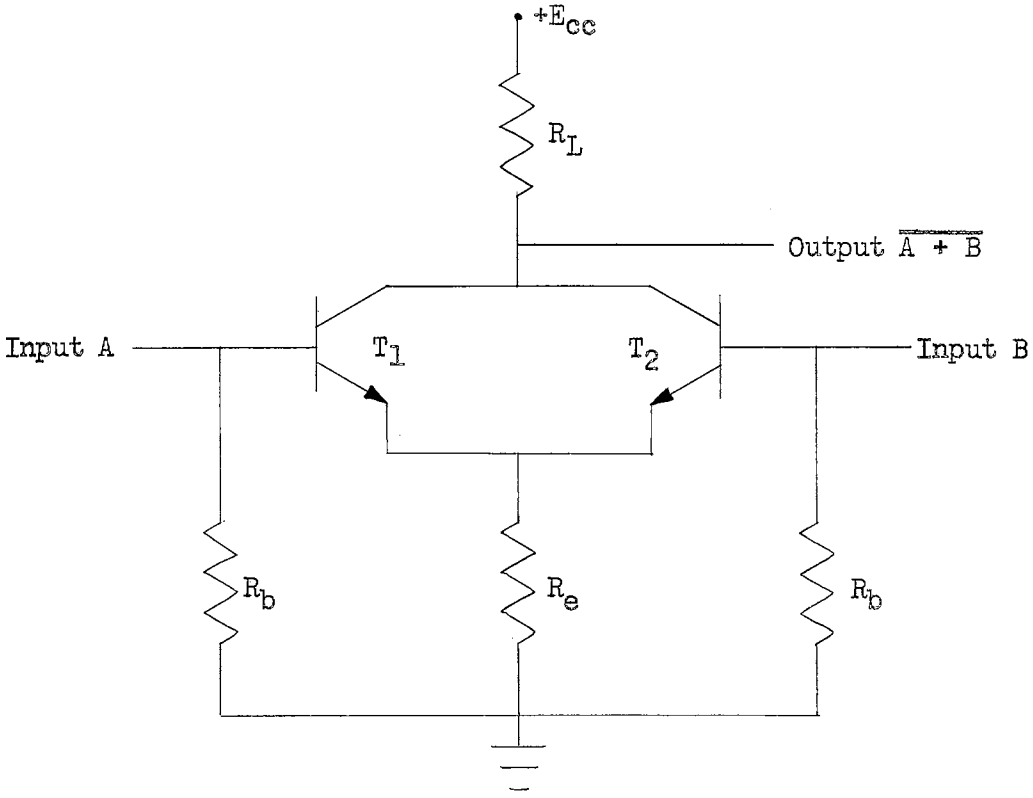

Figure 15. Grounded Emitter "Or" Circuit.

Whereas the "and" operation was accomplished by connecting transistors in series, the "or" operation is accomplished by connecting transistors in parallel.[19,20] Likewise, there are two different circuit configurations which can be used. They are shown in Figures 15 and 16, where A and B are the two input voltages. This assembly of transistors-in-parallel may be connected either as grounded emitter (Figure 15) for voltage amplification or as emitter follower (Figure 16) for current and power amplification. Since logical circuits such as the "and" and "or" are usually employed to drive many following

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[19] Hunter, op. cit.

[20] Shea, op. cit.

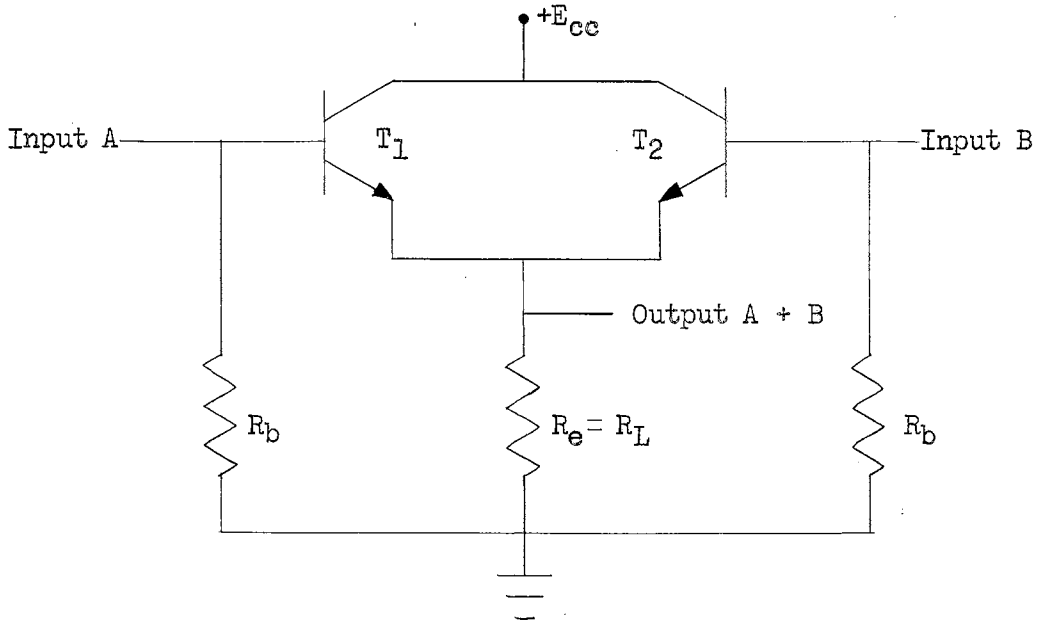

Figure 16. Emitter Follower "Or" Circuit.

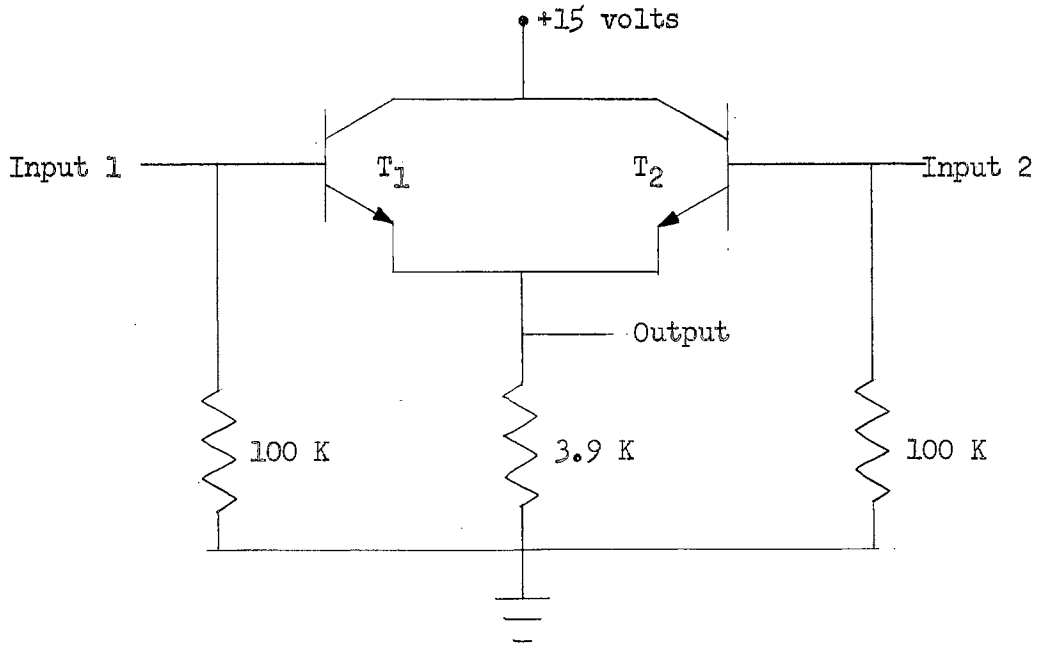

Figure 17. Typical Emitter Follower "Or" Circuit.

stages of circuitry in modern computer usage, the emitter follower circuit of Figure 16 was chosen for development in order to satisfy the load power requirements.

Now, consider the circuit operation when inputs A and B are applied in each of their possible combinations. First let A = "0" and B = "0". This means that A = 0 volts and B = 0 volts which cause both T_1 and T_2 to be cut off. Hence, the output voltage is 0 volts satisfying the condition 0 + 0 = 0.

Let A = "0" and B = "1" which means A = 0 volts and B = 10 volts. T_1 is thus turned "off", but T_2 is turned "on" such that $V_e = V_{b1}$ - 0.2 volts, making the output approximately 10 volts and satisfying the condition 0 + 1 = 1.

Let A = "1" and B = "0" which means A = 10 volts and B = 0 volts. T_2 is thus turned "off", but T_1 is turned "on" such that the output is V_{b2} - 0.2 volts, which is approximately 10 volts, satisfying the condition 1 + 0 = 1.

Finally, let A = "1" and B = "1" which means that both A and B equal 10 volts. Both T_1 and T_2 are thus turned "on" such that maximum emitter current, I_e, flows; hence, maximum voltage appears at the output across R_e equal to $I_e R_e$. But this output voltage can be no greater than (V_{b1} = V_{b2}) - 0.2 volts, which is approximately 10 volts. This satisfies the condition 1 + 1 = 1. Of course, this assembly of transistors-in-parallel is not limited to two transistors. Three or more transistors can readily be connected in parallel to perform the "or" operation, the number required being one transistor for each input.

Whereas the purpose of the "and" circuit is to keep a positive input signal out of the output unless both input signals are positive,

the purpose of the "or" circuit is to pass each positive input signal on to the output regardless of which input has the positive signal. The resulting difference in operation between the "and" and "or" circuits is enough to eliminate from the "or" circuit considerations one basic problem encountered in the "and" circuit; i. e., the problem of feed-through, which existed in the "and" circuit, does not exist in the "or" circuit. Since feed-through is the unwanted result of a positive signal feeding through from the base to the emitter of a transistor, it is no problem in the "or" circuit because each positive signal, which appears at either or both inputs, must also appear at the output in amplified form in order to perform the "or" operation.

The typical circuit of Figure 17 was connected into the adder circuit as shown in Figure 3 for testing. Input 1 handled the carry pulse from the next lower order digit flip-flop. The carry pulse has the characteristics shown in Figure 18. Input 2 carried the modified add pulse from the "and" circuit, the modified add pulse having the characteristics shown in Figure 19. The two input pulses, shown in Figures 18 and 19, are seen to be very different in amplitude; however, the "or" circuit passed both input pulses on to the output with power amplification and little or no distortion or attenuation. Neither of the input pulses interfered with the other in any way. This "or" circuit, simple as it is, was most satisfactory for this application.

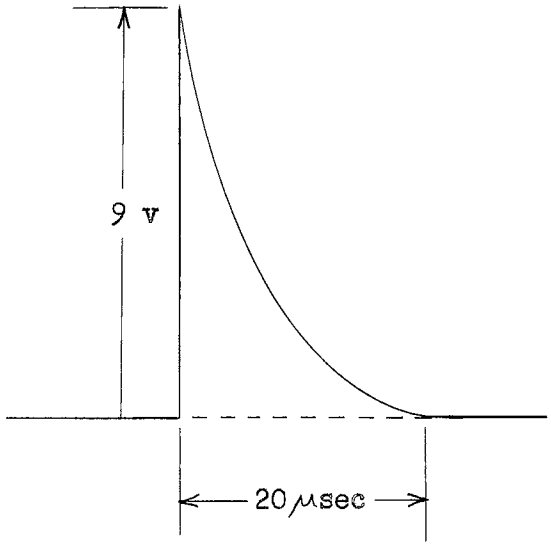

Figure 18. Carry Pulse from Lower Order Digit.

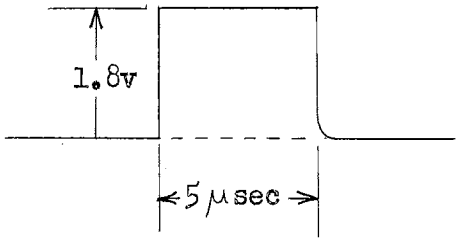

Figure 19. Add Pulse Input to the "Or" Circuit.

CHAPTER V

THE PERFORMANCE OF THE ADDER

The purpose of this chapter is to consider those problems which are peculiar to the system but were not obvious at the time the flip-flop, "and", and "or" circuits were synthesized. The first problem involves the synthesis of a pulse delay circuit.

Because of the feed-through problems in the "and" circuit (Chapter IV), the input trigger pulses must be kept small. Therefore, the flip-flop following the "and" circuit must be able to change states upon receiving this small trigger pulse. (The trigger pulse has an amplitude of approximately $0.2\,\Delta V_c$). Small input trigger pulses along with the desire for higher switching speed motivated the writer to develop some pulse steering techniques.

Because the base is the control element of the transistor, less input pulse energy is required to trigger the flip-flop at the base than at the emitter or collector. Since each input trigger pulse must switch the flip-flop to its other stable state, these pulses must be applied to both transistors in such a way that the "off" transistor will be turned "on" or the "on" transistor turned "off". This is accomplished by arranging the diodes D_1 and D_2 along with the capacitors C_3 and C_4 as shown in Figure 20.

It was found experimentally that the pnp transistors of the flip-flop can be triggered faster and with less pulse energy by positive

input trigger pulses, whereas npn transistors are better triggered by negative pulses. The positive trigger pulses cause the flip-flop to change its state by turning the "on" transistor "off". But this same trigger pulse is also applied to the other transistor, which is "off". Its effect is to turn the "off" transistor farther "off". Hence, the trigger pulses at the base of each transistor are essentially opposing each other. This makes triggering less efficient than if the input pulses were applied to only one transistor at a time. This difficulty is remedied, however, by the resistors R_8 and R_9, which serve to back bias the diodes according to the state of the flip-flop. For example, for T_1 "off" and T_2 "on", the potential at the anode of D_1 is negative with respect to ground. Hence, a positive input trigger pulse is blocked from entering the base of T_1. Because the anode potential of D_2 is near ground, the positive input trigger pulse can enter the base of T_2 to turn it "off". Experiment has shown that the resistors R_8 and R_9 of Figure 20 have actually increased the switching speed of the flip-flop and decreased the required amplitude of the input trigger pulses.

For Figure 20 the following values are used:

$R_1 = R_2 = R_{12} = R_{17} = R_{18} = 3.9$ K

$R_3 = R_4 = R_{19} = 33$ K

$R_5 = R_6 = R_{20} = R_{21} = 8.2$ K

$R_7 = R_{22} = 680$ ohms

$R_8 = R_9 = 22$ K

$R_{10} = R_{11} = R_{13} = R_{14} = 100$ K

$R_{15} = 1.8$ K

$R_{16} = 4.7$ K

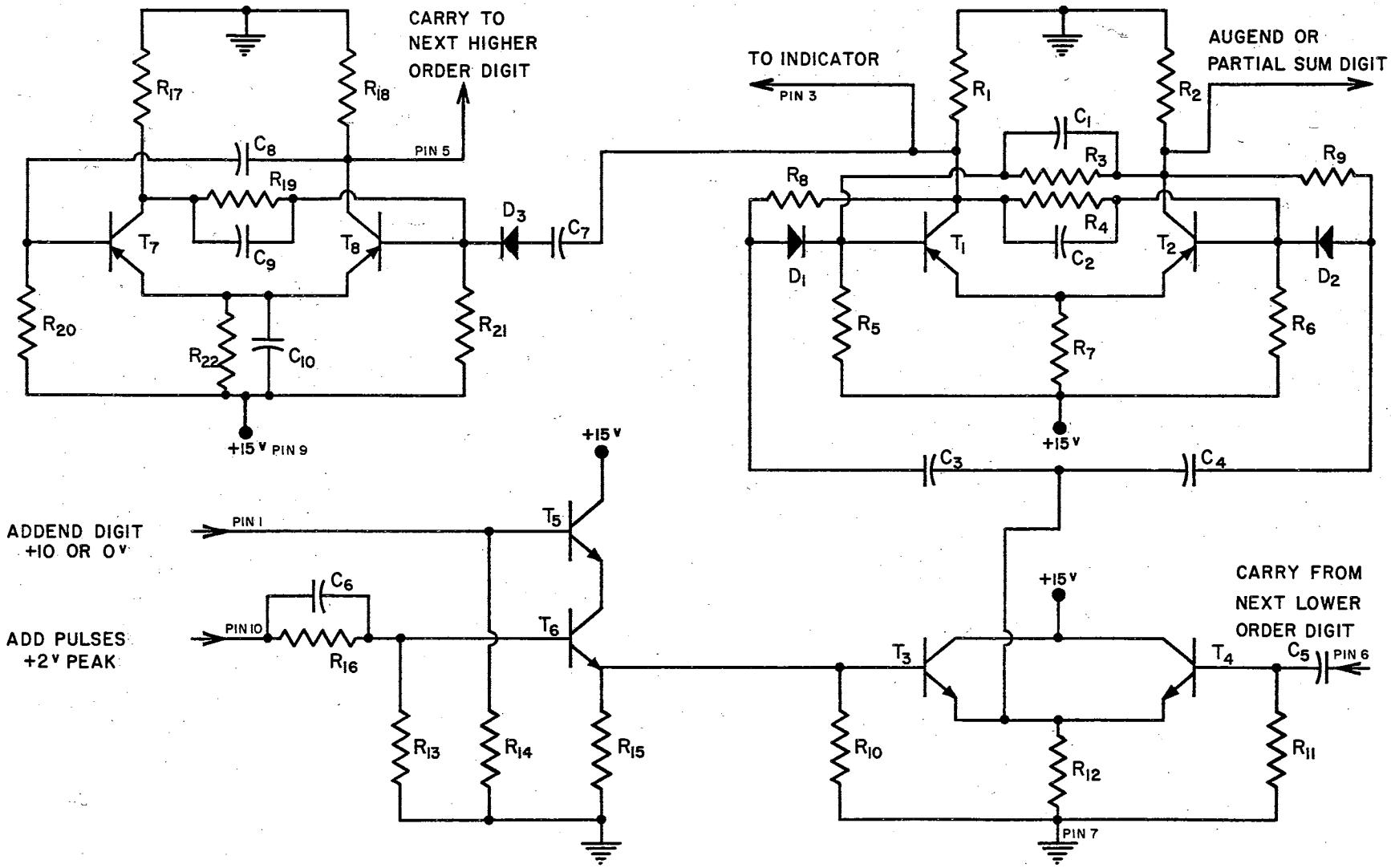

Figure 20. An Adder for One Binary Digit.

$C_1 = C_2 = C_9 = 500 \mu\mu f$

$C_3 = C_4 = 1000 \mu\mu f$

$C_5 = C_7 = 390 \mu\mu f$

$C_6 = 330 \mu\mu f$

$C_8 = 0.01 \mu f$

$C_{10} = 0.1 \mu f$

$D_1 = D_2 = D_3 = IN\ 48$

$T_1 = T_2 = T_7 = T_8 =$ IBM type 08 (pnp)

$T_3 = T_4 = T_5 = T_6 =$ IBM type 58 (npn)

In order to provide a delay for the carry pulse to the next order, a monostable multivibrator was incorporated. Whereas the bistable multivibrator (flip-flop) has two stable states, the monostable multivibrator has one stable state and one semi-stable state.[21] While the bistable multivibrator can be switched from one stable state to the other by an input trigger pulse, the monostable multivibrator can be switched only from its stable state to its semi-stable state by the same type of trigger pulse. Switching from the semi-stable state back to the stable state is accomplished automatically without an input trigger pulse after a predetermined lapse of time.

The monostable multivibrator is similar in construction to the flip-flop as shown in Figure 20. In fact, a bistable flip-flop can be made monostable by replacing one of the resistors, R_3 or R_4, by a capacitor,

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[21] Millman and Taub, op. cit., pp. 174-187.

C_8. While this is not a good design technique, it was done in this case because this conversion satisfied the circuit requirements.

As shown in the adder of Figure 3, a device is needed to delay the carry signal generated by each augend flip-flop for the period of time required to add the addend digits to the corresponding augend digits so that the partial sums appear in the augend register. Then the carrys can be added to the partial sums as they occur. Because of the transistors and components available, the monostable multivibrator was chosen as the device to delay the carry signal. All that is required of this delaying device is that its output be a pulse capable of triggering the augend flip-flop and that this output pulse be delayed with respect to the input pulse. This means that the waveforms of the monostable multivibrator are of no concern as long as the desired output pulse can be obtained at the required time.

The above requirements can be satisfied by merely replacing R_3 of the flip-flop with the capacitor C_8 whose value is determined by the approximate delaying time, $\beta R_{22} R_{20} C_8/(\beta R_{22} + R_{20})$. The delaying time must be greater than the switching time of the flip-flop. To assure ample switching time, a delay time of 100 μsec was chosen. The differentiated output of the monostable multivibrator, which is the delayed pulse shown in Figure 25, is the carry pulse.

Now that all of the circuits for the adder have been developed, the next step is to assemble these individual circuits according to the block diagram of Figure 3 to form the adder. According to Figure 3, the proper circuit assembly for adding one order of binary digits is the one shown in Figure 20. This assembly contains the necessary circuitry for adding in a carry from a lower order digit and generating

a carry for a higher order digit; hence, it is capable of performing as a part of a larger system and adding digits of any order in multi-digit numbers.

For testing, the circuit assembly of Figure 20 was fabricated on the circuit board as shown in Figure 21. For demonstrating the addition of two four-digit binary numbers, four of these circuit boards were fabricated.

Now consider the actual performance of the adder. Referring to Figure 20, the add pulses required to properly trigger the augend flip-flop were the 6 μsec, 2.2-volt pluses shown in Figure 22. The width of these add pulses could vary from 4 μsec to 100 μsec without affecting the add operation, but the tolerable variation in pulse amplitude was from 1.3 to 2.3 volts peak. Above 2.3 volts the pulses fed through the "and" circuit and triggered the flip-flop.

For the input trigger pulses shown in Figure 22, the output waveform of the flip-flop output is approximately 0.4 μsec while the fall time is 4 μsec. The maximum rate at which the input trigger pulses can occur, with each pulse switching the flip-flop, is 20,000 pps.

The differentiated output of the zero side of the augend flip-flop is the trigger pulse for the monostable multivibrator (delay circuit). The output of the monostable multivibrator is shown in Figure 24. Since a pulse must be used to trigger an augend flip-flop, the carry signal must be a pulse. Hence the output of the monostable multivibrator is differentiated producing a carry pulse, which is delayed with respect to the add pulses, as shown in Figure 25.

The primary limitation on the overall speed of addition is the augend flip-flop. The capacitors C_1 and C_2 of Figure 20 are in the

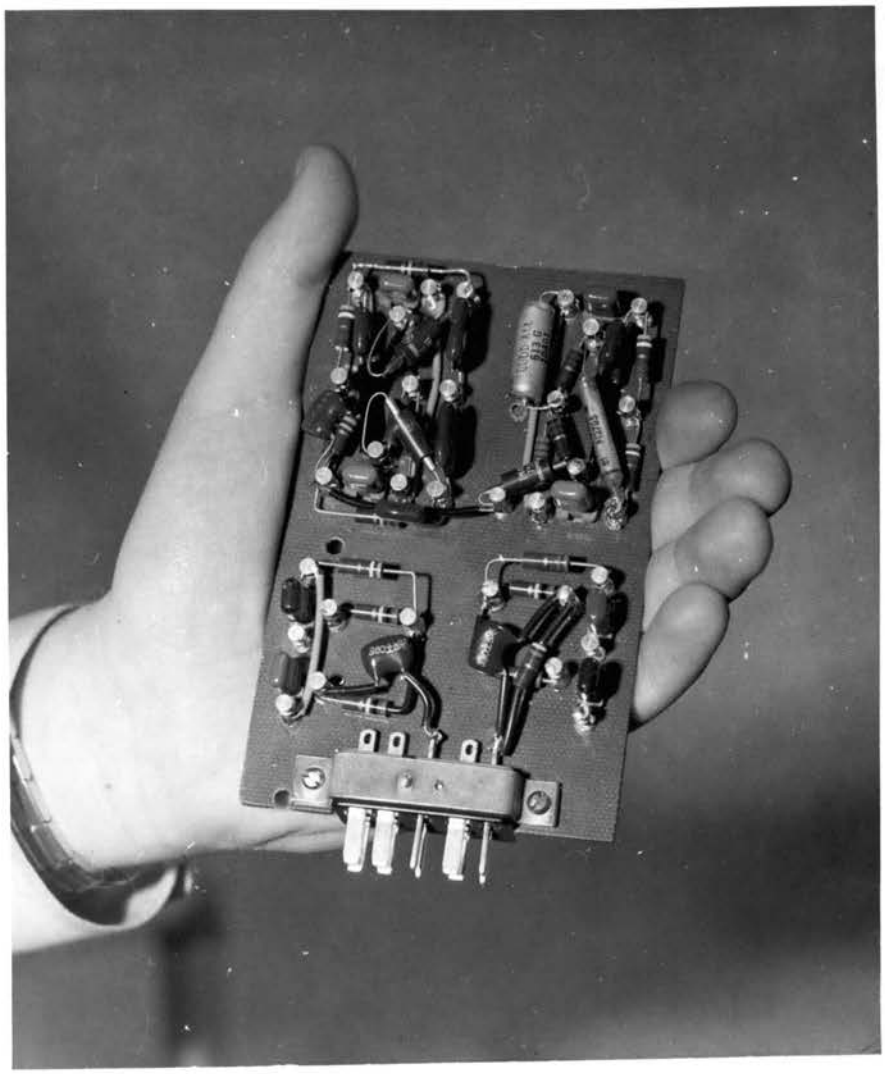

Figure 21

Fabricated Circuit Board for Adding One Binary Digit.

circuit to aid the switching of the flip-flop with their transient charge. While these capacitors enable the flip-flop to switch on a lower voltage input trigger pulse, their capacitance increases the rise and fall times of the flip-flop decreasing the maximum switching time. Removing these capacitors, however, requires that a larger input trigger pulse be used. The switching speed can also be increased by adding a 0.01 μf capacitor in parallel with R_7. As do C_1 and C_2, this capacitor produces a transient effect which aids in the switching of the flip-flop from one stable state to the other. Since the monostable delay circuit is essentially the same circuit as the flip-flop, the above discussion applies to it as well. As the switching speed of the flip-flop is increased, the delay time of the carry pulse can be decreased. This, of course, must be done to increase the overall speed of the add operation. If the necessary delay was small enough, it would be more economical to use a passive delay line rather than a monostable multivibrator.

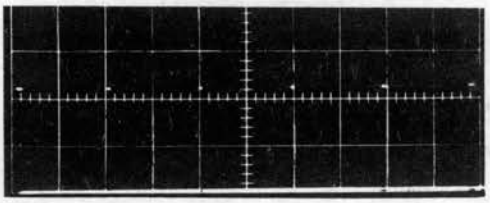

Figure 22. Input Trigger Pulses
Horizontal -
1 millisecond/division
Vertical -
1 volt/division

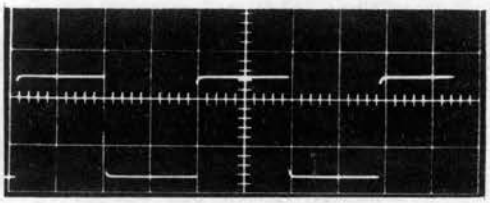

Figure 23. Output Waveform of Augend Flip-Flop
Horizontal -
1 millisecond/division
Vertical -
5 volts/division

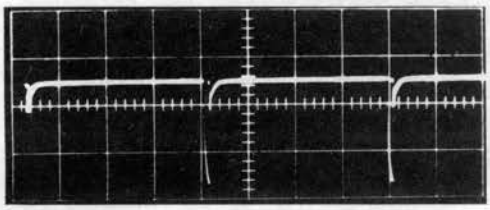

Figure 24. Output Waveform of Monostable Delay Circuit
Horizontal -
1 millisecond/division
Vertical-
5 volt/division

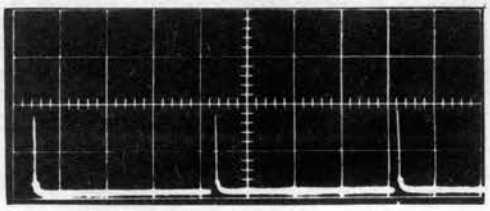

Figure 25. Delayed Carry Pulses
Horizontal -
1 millisecond/division
Vertical -
5 volts/division

CHAPTER VI

SUMMARY

The main problem for this thesis was the development of the basic digital computer circuits using transistors. These basic circuits are the flip-flop, the "and" circuit, and the "or" circuit. To facilitate the operation of these basic circuits together as a small system, a simple binary adder was developed.

The thesis was begun with a verbal, logical development of the binary adder. The result was a block diagram of a system for which the basic computer circuits were to be developed. Next the basic circuits, the flip-flop, the "and" circuit, and the "or" circuit, were developed individually and in that order.

Finally, these circuits were fabricated on circuit boards, according to the block diagram for the system, and tested. The system performed in accordance with the way it was designed to perform, i. e., the system will correctly add two multi-digit binary numbers. Hence, the results were satisfactory.

While the area of application of the completed adder was the addition of two multi-digit binary numbers, it is indeed not limited to this application. For example, the contents of the addend register (Figure 3) is added to the contents of the augend register each time an add pulse is applied. Hence, the contents of the addend register could be multiplied

by n by applying n add pulses to the adder. The resulting product would appear in the augend register. Also, the area of application could be extended to include subtraction by including an end-around-carry within the adder system.[22]

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[22] Richards, op. cit., pp. 119-126.

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APPENDIXES

APPENDIX A

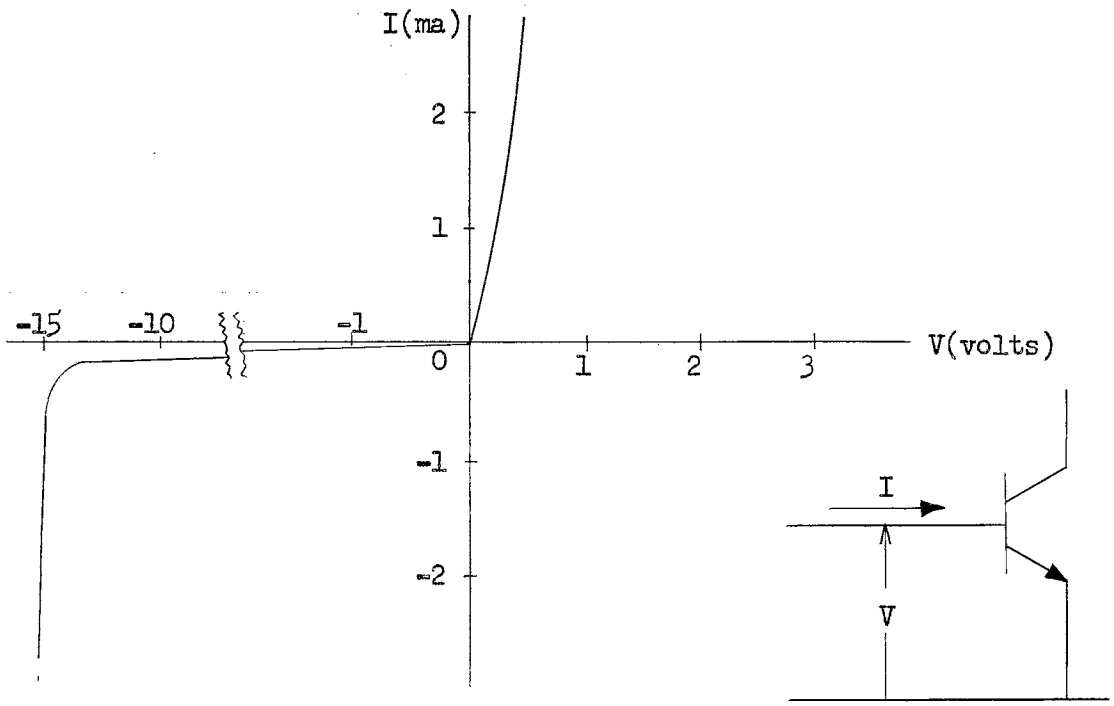

Figure 26. Characteristics of a p-n Junction.

The base-to-emitter junction[23] of an npn transistor has the characteristics shown in Figure 26. When the transistor is connected in the grounded emitter configuration, an increase in base voltage results in an increase in junction current. This V-I characteristic is the curve shown in the first quadrant of Figure 26. Note, however, that as I increases, V increases only slightly as shown by the shape of the V-I characteristic. This means that as I increases to its maximum value, V increases to a small value which is determined by the materials used in the transistor. For germanium transistors, $|V_{be}| \cong 0.2$ volt; for silicon transistors, $|V_{be}| \cong 0.5$ volt[24], where V_{be} is the base-to-emitter junction voltage.

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[23] Hunter, op. cit., p. 1-4.

[24] V_{be} was measured experimentally under large-signal operation.

That V_{be} is constant is expecially true in the flip-flop, because of its large-signal operation. Since the operating point of the "on" transistor is near saturation, the corresponding operating point on the V-I characteristic is at the higher extremity of the curve is the region where $\Delta V/\Delta I$ is very small. Therefore, since operating points are either near saturation or cutoff for the flip-flop, "or", and "and" circuits, $|V_{be}|$ can certainly be regarded as constant; and it can be measured.

APPENDIX B

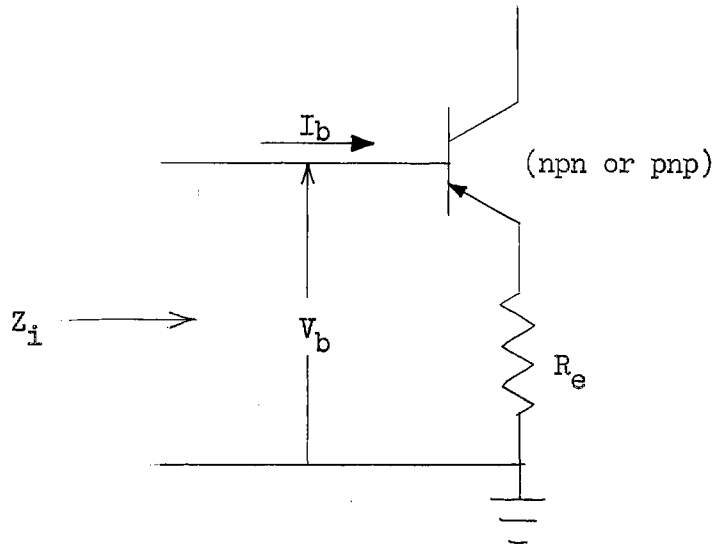

Figure 27. Typical Transistor with External Emitter Resistor, R_e.

Consider the input impedance, Z_i, into the base of the transistor shown in Figure 27. By definition,

$$Z_i = \frac{V_b}{I_b} .$$

But $$I_b = \frac{I_c}{\beta} \cong \frac{I_e}{\beta} \text{ , where } I_b << I_c .$$

For transistors which are conducting, Appendix A shows that

$$V_b = V_e + 0.2 \cong V_e .$$

But $$V_e = I_e R_e \cong \beta I_b R_e \cong V_b .$$

Therefore, $$Z_i = \frac{V_b}{I_b} \cong \frac{\beta I_b R_e}{I_b} \cong \beta R_e .$$

VITA

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