A VOLTAGE SPACE APPROACH TO DEVELOPING A SOFT-SWITCHED INVERTER TOPOLOGY WITH LOW DEVICE VOLTAGE STRESS

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PREFACE

The objective of this study was to expand the soft-switched inverter technology base to include a class of inverters that lack the high device voltage stress levels associated with resonant link topologies, which currently comprise the entirety of soft-switched inverter technology. The approach taken in this work is unique in that it examines the problem from the perspective of how an inverter's soft-switching mechanism restricts its output voltage trajectory in voltage space. A framework is established to describe the fundamental trajectories that a bridge-based soft-switched inverter can traverse. The resulting framework is used to describe a hypothetical soft-switched inverter topology with the same low device voltage stress level as a conventional hard-switched inverter, purely in terms of its voltage space trajectory characteristics. This description is then translated into a physical circuit design, the Parallel Auxiliary Link (PRAL) inverter, which approximates the voltage space characteristics of the hypothetical inverter. Next, simulation experiments are conducted to validate the electrical viability of the PRAL inverter concept and to compare its performance characteristics with those of a leading resonant link inverter design. The results confirm that the low voltage stress objective is fully satisfied and shows that the PRAL inverter has lower output waveform distortion and higher conversion efficiency than the resonant link design selected for the comparison.

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NOMENCLATURE

$\uparrow$	Phase leg transition from lower rail potential to upper rail potential
$\downarrow$	Phase leg transition from upper rail potential to lower rail potential
$\leftrightarrow$	Indicates no phase leg transition between upper and lower rail potentials
$\hat{\mathbf{a}}$	Unit vector used to represent Phase A in voltage and current space
A	Reference to Phase Leg A of a three-phase system
AC	Alternating Current
ACPRDL	Actively Clamped Parallel Resonant DC Link
$\alpha_i(t)$	Occupancy in state i at time t , $i \in \mathbf{S}^*$
AL	Auxiliary Link
$\hat{\mathbf{b}}$	Unit vector used to represent Phase B in voltage and current space
B	Reference to Phase Leg B of a three-phase system
β_i	Ratio of the least time spent in an active state to the minimum possible time spent in that state for a given spanning cycle in Ω_i, $i \in \mathbf{S}^{*-}$
$\hat{\mathbf{c}}$	Unit vector used to represent Phase C in voltage and current space
C	Reference to Phase Leg C of a three-phase system
C_C	Clamping capacitor used in the SPRDL resonant circuit
C_{DL}	Lower capacitor in the PRAL inverter's voltage divider
C_{DU}	Upper capacitor in the PRAL inverter's voltage divider
$CHD_X(k)$	Cumulative Harmonic Distortion in a periodic signal x(t), with period T, up through the k^{th} harmonic component X(k)
$\chi_{i,0}$	Primitive cycle in Ω_i traversing states S_0 and S_i, $i \in \mathbf{S}^{*-}$

$\chi_{i,0,i+}$	Primitive cycle traversing all three states defining Ω_i^-
$\chi_{i+,0}$	Primitive cycle in Ω_i traversing S_0 and S_{i+}, $i \in \mathbf{S}^{*-}$
$\chi_{i,i+}$	Primitive cycle in Ω_i traversing S_i and S_{i+}, $i \in \mathbf{S}^{*-}$
C_R	Capacitance of resonant circuit capacitor (Farads)
CRΔM	Current Regulated Delta Modulation
DC	Direct Current
D_{CL}	Lower power matrix rail clamping diode in a PRAL inverter
D_{Clamp}	Clamping diode
D_{CU}	Upper power matrix rail clamping diode in a PRAL inverter
$\Delta\mathbf{I}$	Estimated change in the vector load current over a prescribed time inverval
$\delta_{i,j}$	Kronecker delta function for integers i and j
$\Delta\mathbf{I}_{int}$	Intermediate vector used in cost-function based load current control
δ_{xL}	Threshold current used to trigger a L_L to T_U mode transition
δ_{xU}	Threshold current used to trigger a L_U to T_L mode transition
E_{Disp}	Dissipated energy
E_{Fixed}	Fixed component of the overall boost energy requirement of a PRAL inverter
$E_k(t)$	Back EMF voltage in Phase k of the load circuit model, $k \in \{A, B, C\}$
E_{LVD}	Boost energy required to offset the combination of load effects and voltage divider imbalance in a PRAL inverter
EMF	Elector-Motive Force
E_{Stored}	Energy stored in a reactive circuit element
E_{VD}	Boost energy required to offset the effects of voltage divider imbalance in a PRAL inverter
f	Frequency
Φ_{Error}	Integrated vector load current error

$\Phi(t)$	Net charge that has passed through the resonant circuit inductor of a PRAL inverter for all time up until time t
f_{Load}	Fundamental frequency of the synthesized sinusoidal voltage and current waveforms supplied to the load
f_{PC}	Primitive cycle frequency, Hz
f_{SC}	Spanning cycle frequency, Hz
FSM	Finite State Machine
γ	Coordinate of a point along the axis formed by $\hat{\psi}_{i+} - \hat{\psi}_i$ in the Hexagonal Coordinate System, where i corresponds to the sector Ω_i containing the point
$G\gamma$	Weighting factor used in cost-function load current control
Γ_i	Set of all four bridge inverter primitive cycles associated with Ω_i, $i \in \mathbf{S}^*$
GTO	Gate Turn-off Thyristor
h	Coordinate of a point along the $\hat{\psi}_i$ axis in the Hexagonal Coordinate System, where i corresponds to the sector Ω_i containing the point
$\mathbf{H}$	Hexagonal shaped region in voltage space containing all possible bridge inverter output voltages
$\mathbf{H}^\dagger$	Hexagonal shaped region containing all normalized bridge inverter output voltages
h_0	Fixed tolerance band limit
$\eta_i(t)$	Effective occupancy in state $\mathbf{S}_i$ at time t, $\mathbf{S}_i \in \mathbf{S}^*$
$\eta_{i+}(t)$	Effective occupancy in state $\mathbf{S}_{i+}$ at time t, $\mathbf{S}_{i+} \in \mathbf{S}^*$
h_{k+1}	Variable tolerance band limit at time step k
$\mathbf{h}(t)$	Generalized bridge inverter output voltage normalized with respect to $V_{Link}(t)$
i	General index variable
I_0	Peak current in the resonant circuit of a PRAL inverter when no boost current is applied and no phase leg transitions occur
I_{Boost}	Excess current used to overdrive resonant circuit oscillations in a PRDL or PRAL inverter
i_{Clamp}	Current in the "clamping" switch of an ACPRDL inverter

$i_{EL}(t)$	Equivalent load current used in the L mode circuit models
$\mathbf{I}_{Error}(t)$	Vector load current error
IGBT	Insulated Gate Bipolar Transistor
i_{iSU}	Current in the Phase i upper power matrix switch of an auxiliary link inverter, $i \in \{A, B, C\}$
i_j	Load phase current in Phase j, $j \in \{A, B, C\}$
I_L	Rated peak phase current of a three-phase load
$i_{LEL}(t)$	Total load phase current conducted by the lower power matrix rail during an auxiliary link inverter T mode
$i_{Link}(t)$	Link current
i_{Load}	Current associated with a generic load
$i_{LTO}(t)$	Total switch turn-off current of an auxiliary link inverter in the T_L mode
I_{LVD}	Boost current required for the combined effects of load interaction and voltage divider imbalance
$\mathbf{i}_P$	Vector current at an arbitrary point **P** in current-space
IPM	Integral Pulse Modulation
I_{Pump}	Maximum average current that a PRAL inverter can establish between the power matrix and the voltage divider node when no phase leg transitions are allowed to occur
i_{Ref}	Reference current used in load current control strategies
$i_R(t)$	Current in the resonant circuit inductor of a PRDL or PRAL inverter
$i_{SLoad-}(t)$	Sum of the load phase currents directed into the auxiliary link
$i_{SLoad-}^{T_L}(t)$	Same as $i_{SLoad-}(t)$ but denotes that the inverter is in the T_L mode
$i_{SLoad+}(t)$	Sum of the load phase currents directed out of the auxiliary link
$i_{SLoad+}^{T_L}(t)$	Same as $i_{SLoad+}(t)$ but denotes that the inverter is in the T_L mode
I_{Source}	DC source current
$i_S(t)$	Dependent current source

i_{Switch}	Current conducted between the terminals of a generic switch
$\mathbf{i}(t)$	Vector representing an inverter's output current
$i'_{TO}(t)$	Cumulative switch turn-off current
$i_{UEL}(t)$	Total load phase current conducted by the upper power matrix rail during an auxiliary link inverter T mode
$i_{uError}(t)$	Inverter output error current along the **u** axis
$i_{ULoad-}(t)$	Total load phase current directed into the upper power matrix rail
$i^{L_L}_{ULoad-}(t)$	Same as $i_{ULoad-}(t)$ but denotes that the inverter is in the L_L mode
$i_{ULoad+}(t)$	Total load phase current directed out of the upper power matrix rail
$i^{L_L}_{ULoad+}(t)$	Same as $i_{ULoad+}(t)$ but denotes that the inverter is in the L_L mode
$i_{URNet}(t)$	Net current passing from the upper power matrix rail into the auxiliary link without passing through the load
$i_{UTO}(t)$	Total switch turn-off current of an auxiliary link inverter T_U mode
I_{VD}	Boost current required to offset the effects of voltage divider imbalance
$i_{vError}(t)$	Inverter output error current along the **v** axis
I_X	Constant current representing the approximate value of $i_x(t)$ over a short time interval
$i_x(t)$	Net current passing from the resonant circuit to the auxiliary link in an auxiliary link inverter
j	General index variable
k	General index variable
k_0	Voltage clamping factor
kHz	Kilo-Hertz
kVA	Kilo-Volt-Ampere
kW	Kilo-Watt
L	"Latch" mode, either L_U or L_L, of an auxiliary link inverter
L_{eff}	Effective load inductance

L_{Eq}	Equivalent load inductance
λ_i	Ratio of the minimum possible effective occupancy time in state S_i to the minimum time required to transition between zero and full occupancy in state S_i
L_L	Lower rail "latch" mode in which the auxiliary link of an auxiliary link inverter is directly connected to the lower power matrix rail
L_P	Equivalent inductance of the equivalent load and resonant circuit inductances combined in parallel
L_R	Inductance of a resonant circuit inductor (Henries)
L_S	Load model series phase inductance
L_U	Upper rail "latch" mode in which the auxiliary link of an auxiliary link inverter is directly connected to the upper power matrix rail
M	General index variable
MCT	MOS Controlled Thyristor
MOS	Metal Oxide Semiconductor
MOS-FET	MOS Field Effect Transistor
MVA	Million Volt-Amperes
$NCHD_X(k)$	Normalized Cumulative Harmonic Distortion in a periodic signal x(t), of period T, up through the k^{th} harmonic component X(k)
PRAL	Parallel Resonant Auxiliary Link
PRDL	Parallel Resonant DC Link
PSPICE	An electronic circuit simulation software package based on SPICE
PWM	Pulse Width Modulation
n	General index variable
Q	Arbitrary point in $\Re^2$ with orthonormal basis set coordinates (q_U, q_V) and three-phase basis set coordinates (q_A, q_B, q_C)
q_A	Phase A coordinate in the three-phase basis set of an arbitrary point **Q** in $\Re^2$
q_B	Phase B coordinate in the three-phase basis set of an arbitrary point **Q** in $\Re^2$
q_C	Phase C coordinate in the three-phase basis set of an arbitrary point **Q** in $\Re^2$

Θ_i	Set of allowed primitive cycles in sector Ω_i, $i \in \mathbf{S}^{*-}$
Q_{Pump}	Maximum net charge transferred between the power matrix and the voltage divider node of a PRAL inverter when no phase leg transitions are allowed to occur
Q_R	Quality factor of a resonant circuit inductor, L_R
q_U	Coordinate of an arbitrary point **Q** in $\Re^2$ along the **u** axis
q_V	Coordinate of an arbitrary point **Q** in $\Re^2$ along the **v** axis
$\Re^2$	Two-dimensional real space
ρ_i	Minimum possible time required for $\alpha_i(t)$ to transition from zero to one and then back to zero divided by the minimum possible effective occupancy time in state S_i, $i \in \mathbf{S}^*$
ρ_L	Ratio of L_P to L_{Eq}
RMS	Root Mean Square
R_R	Effective series resistance associated with a resonant circuit inductor at a specified operating frequency
R_S	Load model series phase resistance
$\mathbf{S}^*$	Set of all seven distinct power matrix states $\{S_0, S_{001}, S_{010}, S_{011}, S_{100}, S_{101}, S_{110}\}$
$\mathbf{S}^{*-}$	Set of all six active power matrix states $\{S_{001}, S_{010}, S_{011}, S_{100}, S_{101}, S_{110}\}$
σ_0	Effective occupancy in state S_0
σ_A	Mean effective active state occupancy
SCR	Silicon Controlled Rectifier
$\Sigma\Delta M$	Sigma Delta Modulation
σ_i	Mean effective occupancy in state S_i, $i \in \mathbf{S}^*$
S_i	Power matrix state i, $i \in \{0, 001, 010, 011, 100, 101, 110\}$
S_{i-}	The power matrix state for which the static voltage vector is both adjacent to and clockwise of the static voltage vector associated with state S_i
σ_{i+}	Mean effective occupancy in state S_{i+}, $i \in \mathbf{S}^*$

S_{i+}	The power matrix state for which the static voltage vector is both adjacent to and counter-clockwise of the static voltage vector associated with state S_i
S_{iL}	Lower power matrix switch in Phase i, $i \in \{A, B, C\}$, of a bridge inverter
S_{iS}	Auxiliary link bilateral switch in Phase i, $i \in \{A, B, C\}$, of an auxiliary link inverter
S_{iU}	Upper power matrix switch in Phase i, $i \in \{A, B, C\}$ of a bridge inverter
SPICE	An industry standard electronic circuit simulation technology
SPRDL	Synchronized Parallel Resonant DC Link
T	"Transitional" mode, either T_U or T_L, of an auxiliary link inverter, or the period of given cycle
T_{AL}	Average frequency of the auxiliary link voltage of an auxiliary link inverter
T_{ci}	Minimum time required for $\alpha_i(t)$ to transition from 0 to 1 and back to 0, $i \in \mathbf{S}^*$
THD	Total Harmonic Distortion
t_i	General time variable, $i \in \{0, 1, 2, ...\}$
T_i	Effective time spent in state S_i during a spanning cycle, $i \in \mathbf{S}^*$
T_{i+}	Effective time spent in state S_{i+} during a spanning cycle, $i \in \mathbf{S}^*$
T_{i1}	Effective time spent in state S_i during the first occupancy of state S_i in a single spanning
T_{i2}	Effective time spent in state S_i during the second occupancy of state S_i in a single spanning cycle
T_{iL}	Lower power matrix bilateral switch in Phase i, $i \in \{A, B, C\}$, of a current-source bridge inverter
T_{iU}	Upper power matrix bilateral switch in Phase i, $i \in \{A, B, C\}$, of a current-source bridge inverter
T_L	Lower rail "transition" mode of an auxiliary link inverter in which the auxiliary link potential is approaching the lower power matrix rail potential and the auxiliary link is not directly connected to either power matrix rail
T_{Link}	Average resonant link period
T_{PC}	Period of an arbitrary primitive cycle

$T_{PC\ i,0}$	Period of a $\chi_{i,0}$ primitive cycle
$T_{PC\ i+,0}$	Period of a $\chi_{i+,0}$ primitive cycle
T_{pi}	Minimum possible effective occupancy time in state S_i, $i \in \mathbf{S}^*$
T_{Pump}	Average time over which a charge of Q_{Pump} Coulombs is transferred between the power matrix and the voltage divider node of a PRAL inverter
T_{SC}	Spanning cycle period, seconds
T_{ti}	Time required for $\alpha_i(t)$ to transition between 0 and 1, $i \in \mathbf{S}^{*-}$
T_U	Upper rail "transition" mode of an auxiliary link inverter in which the auxiliary link potential is approaching the upper power matrix rail potential and the auxiliary link is not directly connected to either power matrix rail
$\hat{\mathbf{u}}$	Unit vector representing the u axis in voltage-space or current-space
u_A	Inner-product of the three-phase basis set unit vector $\hat{\mathbf{u}}$ and the orthonormal basis set unit vector $\hat{\mathbf{a}}$
u_B	Inner-product of the three-phase basis set unit vector $\hat{\mathbf{u}}$ and the orthonormal basis set unit vector $\hat{\mathbf{b}}$
u_C	Inner-product of the three-phase basis set unit vector $\hat{\mathbf{u}}$ and the orthonormal basis set unit vector $\hat{\mathbf{c}}$
UPRDL	Unsynchronized Parallel Resonant DC Link
UPS	Uninterruptible Power Supply
$\hat{\mathbf{v}}$	Unit vector representing the v axis in voltage-space or current-space
$\mathbf{V}^*$	The set of all seven conventional bridge inverter static voltages
$\mathbf{V}^{*-}$	The set of all six conventional bridge inverter static active voltages
$\mathbf{V}^*(t)$	The set of all seven generalized bridge inverter static power matrix voltages, where static implies constant power matrix switch states rather than constant voltage
$\mathbf{V}^{*-}(t)$	The set of all six generalized bridge inverter static power matrix active voltages, where static implies constant power matrix switch states rather than constant voltage
$\mathbf{V}_0$	Bridge inverter output voltage in state S_0 as seen by the load

$V_0(t)$	Common-mode terminal voltage of a three-wire three-phase source relative to an arbitrarily chosen reference potential
v_A	Inner-product of the three-phase basis set unit vector $\hat{\mathbf{v}}$ and the orthonormal basis set unit vector $\hat{\mathbf{a}}$
$V_{ALink}(t)$	Voltage of the auxiliary link of an auxiliary link inverter referenced to the lower power matrix rail
$V_{ARP}(t)$	Instantaneous voltage associated with an arbitrary reference potential
$V_A(t)$	Voltage of Phase Leg A of a three-phase inverter, referenced to the lower power matrix rail
v_B	Inner-product of the three-phase basis set unit vector $\hat{\mathbf{v}}$ and the orthonormal basis set unit vector $\hat{\mathbf{b}}$
V_{BSW}	Voltage drop across a bilateral switch
$V_B(t)$	Voltage of Phase Leg B of a three-phase inverter, referenced to the lower power matrix rail
v_C	Inner-product of the three-phase basis set unit vector $\hat{\mathbf{v}}$ and the orthonormal basis set unit vector $\hat{\mathbf{c}}$
$V_C(t)$	Voltage of Phase Leg C of a three-phase inverter, referenced to the lower power matrix rail
V_D	Forward voltage across a diode
V_{DAT}	Threshold voltage above which corrective actions are taken to stabilize the voltage divider node potential of a PRAL inverter
V_{DBT}	Threshold voltage above which power matrix state transitions are blocked if they would increase the error in the voltage divider node potential of a PRAL inverter
$v_{DL}(t)$	Voltage across the lower voltage divider capacitor, C_{DL}, of a PRAL inverter
$v_{DU}(t)$	Voltage across the upper voltage divider capacitor, C_{DU}, of a PRAL inverter
$\mathbf{V}_{Error}$	Vector error voltage
$v_i(t)$	Instantaneous voltage of Phase Terminal i, $i \in \{A, B, C\}$, referenced to the phase terminal common-mode voltage $V_0(t)$
$V_i(t)$	Instantaneous voltage of Phase Terminal i, $i \in \{A, B, C\}$, referenced to an arbitrary reference potential, typically the lower power matrix rail of a bridge inverter

$V_{Link}(t)$	Upper power matrix rail voltage of a bridge inverter, referenced to the lower power matrix rail potential
V_{Lp}	Link voltage of a conventional voltage-source bridge inverter used as a reference for drawing comparisons with other inverters
$\mathbf{V}_{\mu}$	Mean primitive or spanning cycle voltage
$\mathbf{V}_{\mu k}$	Mean voltage of the k^{th} primitive cycle voltage in an ensemble of M primitive cycles, $k \in \{1, 2, ..., M\}$
$\mathbf{V}_P$	Arbitrary point in voltage-space
V_{P_γ}	Hexagonal coordinate of $\mathbf{V}_P$ along the axis formed by $\hat{\psi}_{i+} - \hat{\psi}_i$, where i is the index of the sector Ω_i containing $\mathbf{V}_P$
V_{Ph}	Hexagonal coordinate of $\mathbf{V}_P$ along the $\hat{\psi}_i$ axis, where i is the index of the sector Ω_i containing $\mathbf{V}_P$
V_{P_U}	Coordinate of $\mathbf{V}_P$ along the **u** axis in the orthonormal basis set
V_{P_V}	Coordinate of $\mathbf{V}_P$ along the **v** axis in the orthonormal basis set
$v_R(t)$	Voltage across the capacitor of a resonant circuit, such as those used in PRDL and PRAL inverters
V_{Ref}	Reference voltage used in load voltage control strategies
V_S	Constant DC source voltage
V_{Source}	DC source voltage
V_{SW}	Forward voltage drop across a unilateral switch
$\mathbf{V}(t)$	Vector representing the output voltage trajectory of an inverter in voltage-space
V_T	Threshold voltage
VVVF	Variable-Voltage Variable-Frequency
ω	Natural radian frequency
Ω_i	Sector in the Hexagonal Coordinate System defined by the triangular region in **H** with vertices $\frac{2}{3}V_{Lp}\hat{\psi}_i$, $\vec{0}$, and $\frac{2}{3}V_{Lp}\hat{\psi}_{i+}$, $i \in \mathbf{S}^{*-}$, $V_{LP} > 0$
$\Omega^{\dagger}_i$	Sector in the Hexagonal Coordinate System defined by the triangular region in $\mathbf{H}^{\dagger}$ with vertices $\hat{\psi}_i$, $\vec{0}$, and $\hat{\psi}_{i+}$, $i \in \mathbf{S}^{*-}$

ξ_k	Phase leg state of an auxiliary link inverter
Ψ	Set of all $\hat{\psi}_i$, $i \in \mathbf{S}^{*-}$
$\hat{\psi}_i$	Unit vector parallel to the static voltage associated with power matrix state S_i, $i \in \mathbf{S}^{*-}$
$\hat{\psi}_{i+}$	Unit vector parallel to the static voltage associated with power matrix state S_{i+}
Z_+	Set of all nonnegative integers
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

CHAPTER I

INTRODUCTION

1.1 Power Electronics: Background and Areas of Application

Power electronics is a specialized branch of electronics focusing on electronic manipulation of electrical energy at power levels greater than a few Watts. Light dimmers, variable speed power tools, computer and household appliance power supplies, and uninterruptible power supplies are a few examples of power electronics applications familiar to most residents of the developed world in the late twentieth century. Industrial applications of power electronics include machine drives [1-22], utility power conditioning systems [26-27], utility interfaces for renewable energy sources [28], etc. Each of these applications employs power electronics circuitry to form a conduit through which electrical energy is efficiently transferred between electrically dissimilar networks in a controlled manner.

The work presented in this document focuses on a specific class of devices called Variable-Voltage Variable-Frequency (VVVF) converters that penetrate nearly every segment of the power electronics industrial market. VVVF converters either partially or fully control the instantaneous voltage magnitude and phase at their tie point with each connected network. Despite the broad range of industrial applications, only the control strategy and ancillary circuitry differ appreciably amongst the various VVVF converter application areas. With a few exceptions, a given VVVF converter design is suitable for use in each of the industrial application areas listed above. Consequently, advances in VVVF converter technology geared toward a specific application are generally adaptable to other application areas.

Members of a special subclass of VVVF converters, known as machine drives, fully control the voltage magnitude and phase presented to the terminals of an electric motor. This allows an automatic control system, external to the VVVF converter, to control motor shaft speed, position, or torque via commands issued to the machine drive. Since machine drives dominate the industrial VVVF converter market, the work that follows is directed specifically at VVVF converters optimized for machine drive applications. However, the results of this study are germane to all application areas that require VVVF converters.

1.2 Evolution of Electronic Machine Drives

Electronics based machine drives began penetrating the industrial market in the late 1950's [1] following the development of the Silicon Controlled Rectifier (SCR) in 1957 [2]. The first generation of SCR-based machine drives employed three distinct approaches: inverters, cycloconverters, and slip power controllers [3-5]. Inverter-based drives are divided into two sub-categories, namely voltage-source and current-source. Voltage-source inverters synthesize AC voltage waveforms by switching the load terminals between the terminals of a DC voltage source. The resulting AC voltage presented to the load is the desired voltage combined with a noise component resulting from imperfections in the voltage synthesis process. Current-source inverters systematically inject current from a DC current source into selected load terminals to produce the desired load current, along with an extraneous noise current resulting from the switching process. For AC sources, the DC voltage or current feeding the inverter is typically obtained using a bridge rectifier. DC sources are normally connected directly to the inverter but may be connected through an intermediate DC-DC converter in some cases. More elaborate designs employ separate inverters connected to both the source and load networks. The DC links of both inverters are tied together, allowing electrical energy to flow in either direction. This allows mechanical energy from the driven machine to be converted to electrical energy and efficiently returned to the

electrical source feeding the machine drive. Such inverter-based designs are called dual converters and are typically used in applications requiring frequent dynamic braking.

Cycloconverters consist of a network in which a switched link exists between each AC load terminal and each AC source terminal. Systematic switching of the network links is employed to synthesize the desired load voltage or current waveforms. Cycloconverters have the advantage of innately providing bi-directional AC power flow and do not require large intermediate energy storage components, which are necessary in most inverter designs. High switch voltage and current stresses along with the need for a source to load frequency ratio of about 6:1 or higher for acceptable waveform quality limit the applicability and practicality of the cycloconverter method.

The slip power control method uses a doubly wound induction machine combined with an external mechanism for varying the effective rotor winding resistance. This provides a means for controlling rotor current, and thus torque. Before the power electronics era, wire-wound variable resistors were used to adjust the effective rotor resistance. Large heat sinks were required to dissipate the slip energy that was converted to heat in the resistors. Once the SCR became available, variable resistances were synthesized using a DC chopper, resulting in improved controllability. Later versions, such as the Static Kramer and Static Scherbius drives, eliminated the problems associated with disposition of the thermal energy generation in the resistor network [5]. This was achieved using a rectifier fed inverter or a cycloconverter connected between the rotor and stator terminals.

Despite decades of research and development devoted to the first generation of SCR-based machine drives, advances in self extinguishing devices rendered all but a few implementations obsolete by the early 1990's. The second generation of machine drives began with the commercial introduction of the power transistor in the 1960's [2]. The self extinguishing property of transistors eliminated the need for forced commutation circuits and removed the switching time restrictions associated with self-commutating and force-commutated SCR designs. Maximum

switching frequencies grew from the approximate 2.0 kHz limit achievable with SCRs to roughly 10-20 kHz, resulting in substantial improvements in waveform spectral quality. Initially, power transistors were not available at high power ratings, limiting the second generation of inverters to power levels of only a few kVA. Later, power transistor kVA ratings increased and new self-extinguishing devices were introduced with power ratings comparable to all but the largest SCRs. The Gate Turn-Off thyristor (GTO) was first reported in 1961 and by the early 1990's was available for use in a 50 MVA inverter [1]. The Insulated Gate Bipolar Transistor (IGBT) became commercially available in the early 1980's and is currently the dominant device for inverters below about 2 MVA. The advantages of the IGBT are low conduction drop, 1.7 - 3.0 volts, a MOS-FET control gate, and turn-off times in the range of 40-800ns. The MOS-Controlled Thyristor (MCT) became commercially available in 1992. It has terminal characteristics similar to the IGBT but has a conduction drop of about 1.0 volts. Accordingly, the MCT is expected to eventually replace the IGBT, due to reduced conduction losses.

The next major advancement in inverter technology began with the introduction of powerful and economical microprocessors in the late 1970's. Real-time algorithmic control capability made sophisticated switching schemes designed to minimize waveform distortion commercially viable. Throughout the early to middle 1980's, the literature was filled with advanced Pulse Width Modulation (PWM) and other sophisticated control techniques that exploited the new microprocessor technology. Techniques were developed to optimally select switching instants and inverter state transitions based on converter capability limitations [23]. The new control methods were applied to both first and second generation drives. By the early 1990's, microprocessor-based controllers were permanently ingrained in the commercial machine drive market.

Early concepts for a third generation of inverters began appearing in the literature in the middle of the 1980's. Two general approaches emerged with the common goal of reducing

waveform distortion through increased switching frequency. Both methods concentrated on new soft-switched designs that essentially eliminated switching losses. This allowed switching frequencies above 10-15 kHz without relinquishing valuable device kVA capacity to accommodate the excessive internal heat generation resulting from switching losses. High Frequency AC Link (HFAL) designs were proposed for high-power applications. Excessive voltage stress, a bilateral switch requirement, the need for auxiliary circuitry to limit unwanted link modulation, and other detracting factors squelched wide spread interest in the HFAL approach. The second approach, based on a collapsible DC link, has dominated soft-switched inverter research since its introduction in 1986 [6].

The original implementation of the collapsible DC link concept was the Parallel Resonant DC Link (PRDL) inverter. The original PRDL inverter introduced in [6] had the merit of switching at 20 kHz and was remarkably simple. Unfortunately, it suffered from device voltage stresses at least three times that of a conventional bridge inverter, rendering it commercially impractical. Improvements that reduced voltage stresses to workable levels and increased the switching frequency beyond 60 kHz were introduced during the late 1980's to early 1990's. A modified form of the PRDL that provided a mechanism for controlling the time at which the DC link collapses was first introduced in 1989 [8] in hopes of further reducing output waveform distortion. This new subclass of PRDL inverters became known as the Synchronized Parallel Resonant DC Link (SPRDL) inverter, due to the controllability of the link collapse time. Numerous SPRDL implementations were proposed throughout the early 1990's. By the mid 1990's, reports in the literature of significant enhancements to the PRDL and SPRDL designs diminished, signaling the apparent end of the first generation of soft-switched collapsible link inverters.

1.3 Switching Losses: The Motivation for Soft Switching

Electronic devices used in power conversion systems occupy one of three distinct operational states. An electronic device is said to be in the "on" state when it restricts the voltage across its terminals to a small value, known as the forward saturation voltage, which is typically about three volts or less. A device in the "on" state is often referred to as being in "saturation." In contrast, the voltage across the terminals of a device in the "off" state is determined by the network to which the device terminals are connected, rather than by the device itself. A third possible operational state, known as the "linear" state, exists for controlled switches. In the "linear" state, either the terminal voltage or current is controlled via the drive circuitry of the switch while the network determines the resulting terminal current or voltage, respectively. For power conversion applications, occupancy in the "linear" state is tolerable only during transitions between the "on" and "off" states. This is due to the excessive heat generation that occurs when the terminal voltage and current of a device are simultaneously greater than a few percent of their respective rated values.

The instantaneous heat generated inside electronic devices, such as transistors and diodes, is approximately equal to the instantaneous terminal voltage-current product. The approximation becomes an equality if control gate current, internal capacitance, and internal inductance are ignored. By convention, this type of heat generation is categorized as either conduction loss or switching loss. Conduction losses occur when a device is conducting current without appreciable changes in the voltage across its terminals. This condition can occur when a device is in either the "on" state or the "linear" state. However, for power conversion systems, sustained conduction is permitted only in the "on" state. Consequently, conduction losses in power conversion systems are associated only with the heat generated inside saturated devices. Switching losses occur when devices occupy the "linear" state during transitions between the "on" and "off" states. The time integral of a device's terminal voltage-current product during occupancy in this state is equal to

the switching energy, which is ultimately manifested as heat energy, associated with the transition between the "on" and "off" states.

Many modern power electronic devices demonstrate sub-microsecond turn-on and turn-off times, suggesting that inverter switching frequencies on the order of several hundred kHz are possible. In practice, conventional inverter designs larger than a few kVA are limited to about 10 kHz due to excessive internal heat generation resulting from switching losses. This limit is normally reached using auxiliary circuits, called snubbers, to divert some of the switching energy away from the main inverter switches. Absence of such auxiliary circuitry results in what is known as hard switching, which generally restricts operation to about 2-5 kHz.

Soft switching is a design paradigm in which the power converter topology is designed in such a way that all devices turn on and off while their terminal voltage or current is at near zero levels, essentially eliminating switching losses. Although inaccurate in the mathematical sense, restricting the terminal voltage of a device to a small fraction of its rated voltage during both the turn-on and turn-off processes, via circuitry external to the device, is commonly known as Zero-Voltage-Switching (ZVS). Zero-Current-Switching (ZCS) is a similar term used to describe the case where a device's terminal current is restricted to a small fraction of its rated value, again via external circuitry, during both the turn-on and turn-off processes.

The switching loss per-cycle for a particular device is a complex function of the internal structure of the device, other devices in the circuit, the terminal voltage and current existing at the onset of the switching event, etc. Accordingly, the circuit design determines the maximum switching frequency a device can tolerate before its effective current rating must be reduced to offset excessive switching losses. A rule-of-thumb switching frequency limit for full utilization of a device's current rating in a conventional bridge inverter is about 2-8 kHz for power transistors and about 5-12 kHz for IGBTs [1], [6]. The lower frequencies in each category reflect true hard-switched designs in which the devices form the only conduction paths between the load and

source networks. The higher frequencies correspond to designs that incorporate snubber circuits to direct some of the switching energy away from the switching devices. Snubbers vary from simple passive circuits consisting of a single diode, capacitor, and resistor to complex active circuits composed of transformers and auxiliary switches. Passive snubbers convert the diverted switching energy directly into heat, which is subsequently dissipated through heat sinks. Active snubbers transfer the diverted switching energy back into the power circuit in the form of electrical energy. This significantly reduces the heat energy generated in the inverter circuitry and improves conversion efficiency. For conventional inverter topologies, switching frequencies above those stated previously are generally attainable only by increasing component dissipation ratings. Practically, this means increasing component current ratings beyond those required at lower switching frequencies, a cost prohibitive solution in most cases.

Figure 1 illustrates the differences between hard switching, snubber assisted switching, and soft switching under ZVS conditions. The diagram shows the simultaneous terminal voltage and current trajectories for a switch transitioning between the "on" and "off" states. The trajectories in Figure 1 represent the most common case in which an inductance is present in the conduction path of the switch. Trajectories that deviate significantly from either the switch terminal voltage or current axes constitute switching trajectories with large terminal voltage-current products. For hard switching, a switch that is turning on must draw the full load current along with all applicable reverse recovery currents of any devices shunting its terminals before its terminal voltage will begin to drop. During turn-off, with series inductance in the conduction path, switch currents do not decrease until their current is transferred to another device, such as a clamping diode. Snubber assisted switching reduces the switching energy generated inside a device during transitions between the "on" and "off" states but comes far from eliminating it altogether. The Zero-Voltage-Switching (ZVS) trajectories shown in Figure 1 illustrate the advantage of soft switching over both hard switching and snubber assisted switching.

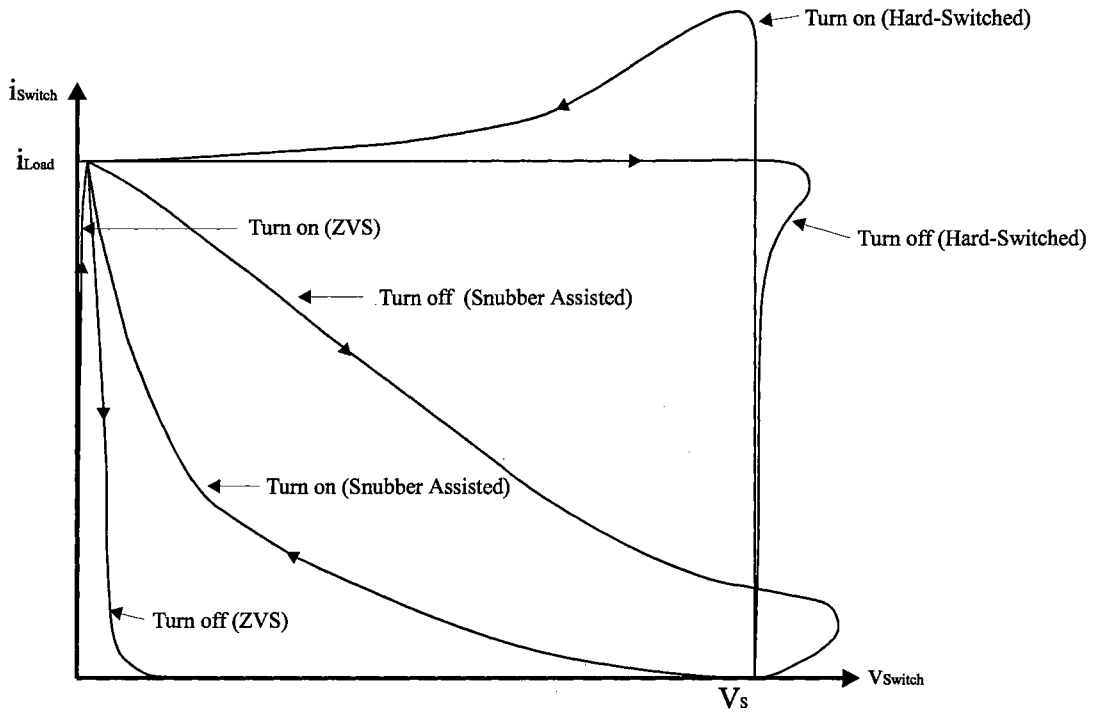


Figure 1. Typical hard-switched, snubber assisted, and ZVS soft-switched switching trajectories for a self-extinguishing device driving an inductive load with current i_{Load} from a DC voltage source of voltage V_S

1.4 Problem Statement

Soft-switched inverter topologies offer the greatest known hope of realizing switching frequencies above 20 kHz. All feasible proposals to date have been based on resonant link designs, which suffer from varying degrees of elevated voltage stress and appear to be limited to switching frequencies of approximately 80-100 kHz and power levels of approximately 100 kVA. The present availability of 800 kVA switching devices with sub-microsecond turn-on and turn-off times suggests that soft-switched inverters with switching frequencies of at least 100 kHz and three-phase power levels of up to 1300 kVA are possible. Unfortunately, resonant link inverters continue to underutilize switching device voltage ratings, despite a myriad of advances.

Interestingly, nearly all advances in resonant link inverter technology have been in response to specific deficiencies in earlier resonant link designs. Discussions of the fundamental underlying

problems afflicting the resonant link topology class are conspicuously absent from the literature. Consequently, it is reasonable to expect a formal investigation of the resonant link structure to yield insight into how existing limitations might be overcome. The potential results of such a study range from improvements to existing resonant link designs to the introduction of completely new topology classes.

1.5 Plan of Study

The premise of this study is that topologically imposed restrictions on an inverter's output voltage trajectory in voltage space influence both device voltage stress and output waveform quality. The initial phase of the study focuses on construction of an analytical framework for describing the behavior of bridge-based voltage-source inverter topologies in terms of their allowed vector output voltage trajectories in voltage space. The resulting framework is applied to both the conventional hard-switched voltage-source inverter and the resonant link topology. Comparisons drawn between the two are used to identify the restrictions on the resonant link inverter's output voltage trajectory responsible for elevating its device voltage stress above that of the conventional hard-switched bridge inverter. Additionally, the voltage trajectory restrictions are related to certain spectral properties of the distortion present in the inverter's output voltage waveforms.

The framework concepts are next used to synthesize a hypothetical soft-switched inverter with voltage stress levels lower than those attainable for any resonant link design. The resulting hypothetical inverter is described solely in terms of its allowed output voltage trajectories in voltage space. This is followed by synthesis of a physically viable topology that approximates the voltage trajectory characteristics of the hypothetical inverter. State-variable models for the resulting inverter topology are then developed for use in subsequent simulation investigations. Next, the control requirements unique to the newly proposed soft-switched inverter topology

class are explored in sufficient detail to permit meaningful modeling and simulation experiments to be conducted. Subsequently, SPICE is employed to demonstrate the electrical viability of the proposed physical circuit design in lieu of constructing and testing a physical prototype. Finally, state-variable simulation experiments are conducted to compare important performance aspects of the new topology, such as device stress, output waveform quality, and conversion efficiency to those of a leading SPRDL inverter design.

1.6 Organization of the Thesis

Chapter II summarizes the state-of-the-art of soft-switched inverter technology and presents background material for use in the following chapters. The analytical tools and definitions presented in Chapter II also establish the notational convention used throughout the remainder of the document.

Chapter III constitutes the beginning of the original work presented in the thesis by developing a framework for quantifying aspects of an inverter's output waveform characteristics in terms of topologically imposed restrictions on the behavior of its output voltage vector. The chapter includes a demonstration illustrating the application of the framework concepts. The chapter concludes with a set of design guidelines for soft-switched inverters based on the cumulative body of knowledge existing in the soft-switched inverter literature.

Chapter IV applies the concepts presented in Chapter III to the task of synthesizing a hypothetical soft-switched inverter with minimal device voltage stress and potentially superior spectral quality compared to resonant link designs.

Chapter V presents the synthesis process used to develop an electrically viable design that approximates the output voltage vector characteristics of the hypothetical inverter proposed in Chapter IV. Top-level control issues and potential shortcomings of the synthesized circuit are also included.

Chapter VI discusses detailed circuit design and control issues not covered in Chapter V that are essential to conducting meaningful simulation studies in chapters VII and VIII.

Chapter VII employs PSPICE to demonstrate the electrical viability of the inverter design proposed in chapter V. Unfortunately, the extreme complexity of the inverter's control circuitry prohibits waveform spectral analysis, due to numerical convergence limitations in the version of PSICE available for use in this study.

Chapter VIII employs state-variable simulation techniques to further demonstrate the viability of the proposed new topology and to investigate the spectral quality of its load current waveforms. Secondly, comparisons are drawn between the proposed new topology and a selected SPRDL inverter design in terms of device voltage stress, spectral quality of the load current waveforms, and conversion efficiency.

Chapter IX summarizes the work presented in the preceding chapters, reiterates essential assumptions underlying the conclusions reached in this work, and suggests related topics that may constitute fertile ground for future research.

CHAPTER II

BACKGROUND AND LITERATURE REVIEW

2.1 Introduction

The soft-switched inverter paradigm established over the past decade forms the basis for the work presented in the remaining chapters of this work. Accordingly, certain background material is needed to provide a clear understanding of the discussions and concepts that lie ahead. This chapter begins with a brief review of three-phase three-wire voltage and current representations and establishes notational conventions used throughout the remainder of the thesis. Next, a review of major soft-switched inverter categories is presented to summarize the state-of-the-art and to provide a convenient reference for ensuing discussions. Finally, a synopsis of soft-switched inverter control schemes is included for use in chapters dealing with simulation and control.

2.2 Representation of Three-Wire Three-Phase Voltages and Currents

Three-wire three-phase voltages and currents are vector quantities in two-dimensional real space, denoted by $\Re^2$, that are normally specified in terms of the scalar voltages or currents associated with each phase. This constitutes three basis vectors in $\Re^2$, one basis vector for each phase, and consequently results in an overdetermined basis set. Mapping the phase currents and terminal voltages to an orthonormal basis set in $\Re^2$ simplifies illustrative tasks and reduces the complexity of real-time control system implementation in some cases. Additionally, casting the

voltage and current representations into identical forms allows a single transformation to be used to relate coordinates in the phase basis set to coordinates in a single orthonormal basis set in $\Re^2$.

Phase terminal voltages are normally associated with four-wire three-phase systems for which a definitive measurable voltage exists between each phase terminal and the neutral terminal. It is also common to refer to the voltage between a phase terminal and the star-point of a Wye connected three-wire three-phase system as a "phase terminal voltage." However, the star-point of a Wye connected electrical machine is typically inaccessible and does not exist for Delta connected systems. Before proceeding further, it is necessary to develop an abstract definition of phase terminal voltages that is applicable to all three-wire three-phase systems.

One set of voltages that can always be measured in both Wye and Delta connected systems consists of the voltages between each of the phase terminals and a common arbitrary reference potential $V_{ARP}(t)$. Let $V_A(t)$, $V_B(t)$, and $V_C(t)$ be the voltages of phase terminals A, B, and C, respectively, referenced to $V_{ARP}(t)$. Next, define a new reference voltage $V_0(t)$, which is also referenced to $V_{ARP}(t)$.

$$V_0(t) = \frac{V_A(t) + V_B(t) + V_C(t)}{3} \qquad 2.2.1$$

The voltage $V_0(t)$ is the instantaneous average of the phase terminal voltages referenced to $V_{ARP}(t)$. Let the formal definition of the phase terminal voltages $v_j(t)$, $j \in \{A, B, C\}$, of a three-wire three-phase system, referenced to $V_0(t)$, be:

$$v_j(t) = V_j(t) - V_0(t) \quad j \in \{A, B, C\} \qquad 2.2.2$$

By referencing each phase terminal voltage to $V_0(t)$, the phase terminal voltages share an important property with the phase currents. Specifically, the sum of all three instantaneous phase terminal voltages, referenced to $V_0(t)$, is identically equal to zero for all values of t. Expressing $v_A(t)$, $v_B(t)$, and $v_C(t)$ in terms of $V_A(t)$, $V_B(t)$, $V_C(t)$, and $V_{ARP}(t)$ results in,

$$v_A(t) = \frac{2}{3}V_A(t) - \frac{1}{3}(V_B(t) + V_C(t)) \qquad 2.2.3$$

$$v_B(t) = \frac{2}{3}V_B(t) - \frac{1}{3}(V_A(t) + V_C(t)) \qquad 2.2.4$$

$$v_C(t) = \frac{2}{3}V_C(t) - \frac{1}{3}(V_A(t) + V_B(t)) \qquad 2.2.5$$

Summing 2.2.3, 2.2.4, and 2.2.5 results in 2.2.6 and thus confirms that the desired relationship exists between $v_A(t)$, $v_B(t)$, and $v_C(t)$.

$$v_A(t) + v_B(t) + v_C(t) = 0 \qquad 2.2.6$$

The reference voltage $V_0(t)$ is a common-mode voltage, associated with the voltage set $\{V_A(t), V_B(t), V_C(t)\}$, to which $v_A(t)$, $v_B(t)$, or $v_C(t)$ are added to yield the respective phase terminal voltages $V_A(t)$, $V_B(t)$, and $V_C(t)$, referenced to $V_{ARP}(t)$. The voltages between the phase terminal pairs, also known as the line-to-line voltages, are expressible entirely in terms of $v_A(t)$, $v_B(t)$, and $v_C(t)$. By definition, all conduction paths in a three-wire three-phase system terminate at the phase terminals. Consequently, the value of $V_0(t)$, as measured from the arbitrary reference $V_{ARP}(t)$, does not influence current conduction in any branch of a three-wire three-phase system. Since $V_0(t)$ has no effect on the phase currents, it is possible to locate $V_0(t)$ at the origin of $\Re^2$. In terms of voltage-current duality, the phase currents are also referenced to a common-mode current. However, the common-mode current of a three-wire three-phase system is identically equal to zero, as is evident from the well-known relationship between the phase currents of three-wire three-phase systems given in 2.2.7.

$$i_A(t) + i_B(t) + i_C(t) = 0 \qquad 2.2.7$$

Referencing the phase terminal voltages to the common-mode potential $V_0(t)$ has the effect of casting the three-wire three-phase system phase currents and terminal voltages into

mathematically identical forms. The forms of 2.2.6 and 2.2.7 clearly reveal that the phase terminal voltage and phase current vectors have two degrees of freedom and span $\Re^2$. However, when specified in terms of phase components, each is represented in an overdetermined basis set in $\Re^2$. Although specifying the phase terminal voltage and current vectors in terms of only two of the phase terminal basis vectors would eliminate this problem, the resulting basis vectors would not be orthogonal. The ability to represent the phase terminal voltage and current vectors in terms of an orthogonal, and for additional convenience an orthonormal, basis set significantly simplifies the analytical expressions in the following chapters.

The desired transformation between the overdetermined phase basis set and an arbitrary orthonormal basis set, both centered at the origin of $\Re^2$, can now be developed. Define an orthonormal basis in $\Re^2$ consisting of the unit basis vectors $\hat{\mathbf{u}}$ and $\hat{\mathbf{v}}$, where $\hat{\mathbf{u}} \times \hat{\mathbf{v}}$ is out of the page. Next, let the basis vectors for Phases A, B, and C in the phase basis be the unit vectors $\hat{\mathbf{a}}, \hat{\mathbf{b}}$, and $\hat{\mathbf{c}}$, respectively. Although experience suggests that the phase terminal basis vectors are oriented 120° apart, it is instructive to show that this is a mathematical characteristic of three-wire three-phase systems rather than an arbitrary choice made for convenience. Let **Q** be an arbitrary point in $\Re^2$ with coordinates (q_A, q_B, q_C) in the phase basis coordinate system and coordinates (q_U, q_V) in the orthonormal basis coordinate system. Let **Q** be formally expressed in terms of each basis set as,

$$\mathbf{Q}(q_A, q_B, q_C) = q_A\hat{\mathbf{a}} + q_B\hat{\mathbf{b}} + q_C\hat{\mathbf{c}} \qquad 2.2.8$$

$$\mathbf{Q}(q_U, q_V) = q_U\hat{\mathbf{u}} + q_V\hat{\mathbf{v}} \qquad 2.2.9$$

Since both the phase terminal and orthonormal basis sets share a common origin, any transformation between the two does not involve a translation. Consequently, the phase basis vectors can be written in terms of the orthonormal basis vectors as,

$$\hat{a} = u_A\hat{u} + v_A\hat{v} \qquad 2.2.10$$

$$\hat{b} = u_B\hat{u} + v_B\hat{v} \qquad 2.2.11$$

$$\hat{c} = u_C\hat{u} + v_C\hat{v} \qquad 2.2.12$$

Where u_j and v_j, $j \in \{A, B, C\}$, are real coefficients.

Since each basis vector is a unit vector, the following constraint is placed on coefficients u_j and v_j, $j \in \{A, B, C\}$.

$$u_j^2 + v_j^2 = 1 \quad \forall j \in \{A,B,C\} \qquad 2.2.13$$

The transformation from coordinates in the orthonormal basis to coordinates in the phase basis can be written as,

$$\begin{pmatrix} q_A \\ q_B \\ q_C \end{pmatrix} = \begin{pmatrix} u_A & v_A \\ u_B & v_B \\ u_C & v_C \end{pmatrix} \begin{pmatrix} q_U \\ q_V \end{pmatrix} \qquad 2.2.14$$

Writing the sum of the phase basis coordinates, q_A, q_B, and q_C, in terms of the orthonormal basis coordinates, q_U and q_V, yields,

$$q_A + q_B + q_C = q_U(u_A + u_B + u_C) + q_V(v_A + v_B + v_C) \qquad 2.2.15$$

Since the left-hand side of 2.2.15 is equal to zero for all points in $\Re^2$, per 2.2.6 and 2.2.7, the right-hand side of 2.2.15 must equal zero for all values of q_U and q_V. This can only be true if both 2.2.16 and 2.2.17 hold.

$$u_A + u_B + u_C = 0 \qquad 2.2.16$$

$$v_A + v_B + v_C = 0 \qquad 2.2.17$$

Summing 2.2.10, 2.2.11, and 2.2.12 and applying 2.2.16 and 2.2.17 shows that the sum of the phase basis unit vectors is identically equal to the zero vector.

$$\hat{a} + \hat{b} + \hat{c} = \vec{0} \qquad 2.2.18$$

Taking the inner product of 2.2.18 with $\hat{a}$, $\hat{b}$, and $\hat{c}$ produces 2.2.19, 2.2.20, and 2.2.21, respectively.

$$1 + \hat{a} \cdot \hat{b} + \hat{a} \cdot \hat{c} = 0 \qquad 2.2.19$$

$$\hat{a} \cdot \hat{b} + 1 + \hat{b} \cdot \hat{c} = 0 \qquad 2.2.20$$

$$\hat{a} \cdot \hat{c} + \hat{b} \cdot \hat{c} + 1 = 0 \qquad 2.2.21$$

Solving for the inner products of the phase basis vectors yields,

$$\hat{a} \cdot \hat{b} = \hat{b} \cdot \hat{c} = \hat{a} \cdot \hat{c} = -\frac{1}{2} \qquad 2.2.22$$

This condition can only exist in $\Re^2$ if the orientations of $\hat{a}$, $\hat{b}$, and $\hat{c}$ differ by exactly 120°. This result uniquely determines the coefficients of the transformation between the two coordinate systems up to a constant of rotation.

There are infinitely many valid transformations, each differing by a constant of rotation. The following definition, based on the generalized time-dependent phase terminal coordinates $q_A(t)$, $q_B(t)$, and $q_C(t)$ and the orthonormal basis coordinates $q_U(t)$ and $q_V(t)$ given in 2.2.23 and 2.2.24, is consistent with conventions adopted in [23]. This definition will be followed throughout the remainder of this work. Figure 2 graphically illustrates the resulting relationship between the orthonormal basis set unit vectors and the phase basis set unit vectors.

$$\begin{pmatrix} q_U \\ q_V \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ \frac{1}{\sqrt{3}} & \frac{2}{\sqrt{3}} & 0 \end{pmatrix} \begin{pmatrix} q_A \\ q_B \\ q_C \end{pmatrix} \qquad 2.2.23$$

$$\begin{pmatrix} q_A \\ q_B \\ q_C \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} q_U \\ q_V \end{pmatrix} \qquad 2.2.24$$

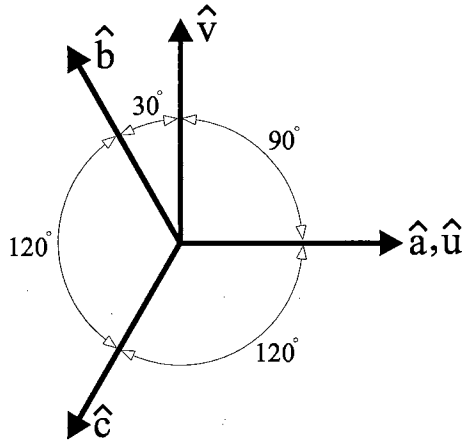


Figure 2. Phase basis set and orthonormal basis set unit vectors used to represent three-wire three-phase voltages and currents in $\Re^2$

2.3 Voltage and Current Space Diagrams

Voltage and current space diagrams are useful illustrative tools for representing three-wire three-phase voltage and current trajectories in $\Re^2$. In general, a voltage or current vector trajectory in $\Re^2$ forms a continuous curve with no specific pattern. However, the output voltage or current vector trajectory of a switched-mode power converter contains a definitive structure in voltage or current space, respectively. Switched-mode converters are finite state machines. A specific region of either voltage space or current space is ordinarily associated with each inverter state. During transitions between two specific inverter states, the output trajectory is typically

restricted to a specific corridor in $\Re^2$ connecting the voltage or current sets associated with the respective inverter states. Since this work focuses on inverter voltage stresses, the trajectory of the inverter output voltage vector in voltage space is of primary interest. The voltage space diagram of a voltage-source three-phase bridge inverter is referenced extensively in the next chapter. In order to provide adequate background for the upcoming chapters, the following definitions and discussions, loosely based on definitions found in [23], are presented for a voltage-source three-phase bridge inverter.

Consider the conventional voltage-source three-phase bridge inverter shown in Figure 3. When the inverter is not switching, one switch in each inverter phase leg is closed and the other is open. Each combination represents one static inverter state, where "static" indicates that the inverter is not in the process of changing states. Since each of the three inverter legs has exactly two static voltage levels, a three-phase bridge inverter has exactly 2^3, or eight, static states. Let **S** represent the set containing the eight static inverter states. Denote the individual states as S_{ABC}, where subscripts A, B, and C are one if the upper switch in the respective phase leg is closed and zero if the lower switch is closed. The inverter phase leg voltages $V_A(t)$, $V_B(t)$, and $V_C(t)$ shown in Figure 3 are references to the lower rail potential. Thus, the arbitrary reference potential $V_{ARP}(t)$ defined in Section 2.2 is equal to the lower rail potential. The corresponding common mode voltage $V_0(t)$ is,

$$V_0(t) = \frac{V_A(t) + V_B(t) + V_C(t)}{3} \qquad 2.3.1$$

The phase terminal voltages presented to the load are,

$$v_j(t) = V_j(t) - V_0(t) \quad j \in \{A, B, C\} \qquad 2.3.2$$

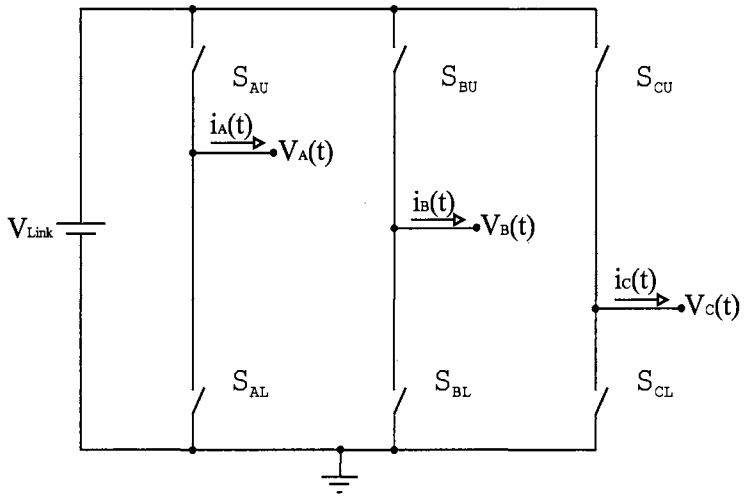


Figure 3. Schematic diagram of a conventional three-phase voltage-source bridge inverter

Using 2.3.1 in 2.3.2 results in,

$$\begin{pmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{pmatrix} = \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{pmatrix} \begin{pmatrix} V_A(t) \\ V_B(t) \\ V_C(t) \end{pmatrix} \qquad 2.3.3$$

Using 2.3.3 in 2.2.23 maps the inverter phase leg voltages to the phase terminal voltage representation defined in terms of the orthonormal **u-v** basis set.

$$\begin{pmatrix} v_U(t) \\ v_V(t) \end{pmatrix} = \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{pmatrix} \begin{pmatrix} V_A(t) \\ V_B(t) \\ V_C(t) \end{pmatrix} \qquad 2.3.4$$

The static inverter states along with the link voltage V_{Link} uniquely locate the inverter output voltage vector in voltage space when the inverter is not changing states. Applying 2.3.4 to the inverter leg voltages associated with each inverter state $S_{ABC} \in \mathbf{S}$, locates the corresponding

inverter output voltage $\mathbf{V}_{ABC}$ in voltage space. Figure 4 shows a voltage space diagram of the resulting eight static inverter voltages.

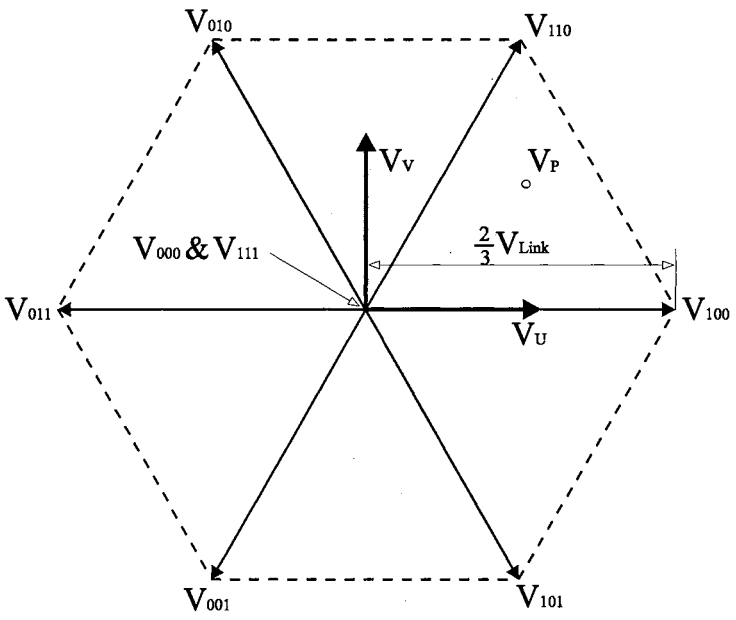


Figure 4. Voltage space diagram showing the eight static inverter output voltages of a three-phase bridge inverter. $\mathbf{V}_P$ is an arbitrary point in voltage space capable of being synthesized using the indicated link voltage

The eight static states of a three-phase bridge inverter consist of six active states and two passive states. The active state voltages $\mathbf{V}_{100}$, $\mathbf{V}_{110}$, $\mathbf{V}_{010}$, $\mathbf{V}_{011}$, $\mathbf{V}_{001}$, and $\mathbf{V}_{101}$, located at the vertices of the hexagonal region shown in Figure 4, correspond to the six inverter states for which energy can flow between the inverter and the load. The passive state voltages $\mathbf{V}_{000}$ and $\mathbf{V}_{111}$ corresponding to inverter states S_{000} and S_{111}, respectively, short circuit the load terminals and thus block energy transfer between the load and the inverter. Since the two passive states are degenerate in terms of energy flow and their associated voltages both lie at the origin of voltage space, they are collectively called the zero state and identified with the single symbol S_0. Let the associated zero state voltage, which is equal to both $\mathbf{V}_{000}$ and $\mathbf{V}_{111}$, be denoted as $\mathbf{V}_0$. To avoid confusion with $\mathbf{S}$, which contains all eight static inverter states, let $\mathbf{S}^*$ denote the set containing

the six active states and the zero state. Furthermore, let $\mathbf{V}^*$ denote the set containing the seven distinct voltages associated with the seven static inverter states contained in $\mathbf{S}^*$. Let $\mathbf{S}^{*-}$ represent the set of six active states and let $\mathbf{V}^{*-}$ be the set of active state voltages. Finally, notice that the orientation of the active voltages in Figure 4 is independent of the link voltage. The six unit vectors parallel to the voltage vectors in $\mathbf{V}^{*-}$ form an overdetermined basis set that is useful for describing the inverter output voltage vectors in terms of the power matrix state and the link voltage. Let Ψ represent the set of unit vectors parallel to the voltage vectors in $\mathbf{V}^{*-}$. The six elements of Ψ are given in 2.3.5 in terms of the **u-v** basis set.

$$\begin{pmatrix} \hat{\psi}_{100} \\ \hat{\psi}_{110} \\ \hat{\psi}_{010} \\ \hat{\psi}_{011} \\ \hat{\psi}_{001} \\ \hat{\psi}_{101} \end{pmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{pmatrix} \hat{u} \\ \hat{v} \end{pmatrix} \qquad 2.3.5$$

The one-to-one correspondence between the active states $S_{ABC} \in \mathbf{S}^{*-}$ and the unit vectors $\hat{\psi}_{ABC} \in \Psi$ tie each active state to a specific orientation in voltage space. It is often convenient to reference an active state in terms of another active state. For a given active state S_i, let S_{i+} denote the active state for which the static voltage unit vector $\hat{\psi}_{i+}$ is adjacent to and counter-clockwise of $\hat{\psi}_i$. Similarly, let S_{i-} denote the active state whose static voltage unit vector $\hat{\psi}_{i-}$ is adjacent to and clockwise of $\hat{\psi}_i$. For example, $S_{110} = S_{100+}$ and $S_{101} = S_{100-}$, as can be verified using either 2.3.5 or Figure 4.

A bridge inverter synthesizes the three-phase waveform presented to the load by switching between the seven states in $\mathbf{S}^*$. Consider the voltage $\mathbf{V}_P$ shown in Figure 4. In general, any

inverter output voltage trajectory $\mathbf{V}(t)$ in voltage space that satisfies conditions 2.3.6 and 2.3.7 is a valid trajectory for synthesizing $\mathbf{V_P}$.

$$V_{P_u} = \lim_{T\to\infty} \frac{1}{T} \int_0^T (\mathbf{V}(t) \cdot \hat{u}) dt \qquad 2.3.6$$

$$V_{P_v} = \lim_{T\to\infty} \frac{1}{T} \int_0^T (\mathbf{V}(t) \cdot \hat{v}) dt \qquad 2.3.7$$

Ideally, the control scheme is designed to synthesize $\mathbf{V_P}$ using only the zero state and the two active states that bound $\mathbf{V_P}$, $\mathbf{V_{100}}$ and $\mathbf{V_{110}}$ for the case shown in Figure 4. This is done to minimize the magnitude of the voltage error $\mathbf{V}(t)$ - $\mathbf{V_P}$. Consequently, only states S_0, S_i, and S_{i+}, for some i, are normally used to synthesize a given $\mathbf{V_P}$. The true significance of the preceding definitions will become apparent when the voltage synthesis process is formally addressed in Chapter III.

2.4 Soft-Switched Topologies

2.4.1 The PRDL Soft Switching Concept

The Parallel Resonant DC Link (PRDL) concept, first introduced by Divan in the middle 1980's, is the basis for most high-power soft-switched inverter designs proposed to date. Divan's work focused on augmenting a voltage source bridge inverter with various circuits that force the link voltage to periodically collapse, producing ZVS conditions for the power matrix switches [6]. This eliminates the need for snubbers and reduces switch drive requirements to simple on/off base or gate drive circuitry. The series inductance present in most machine and transformer loads provides adequate isolation between the link collapse circuit and the load back EMF. This is a significant advantage in terms of inverter cost, weight, and size. An additional advantage is low phase terminal dv/dt compared to both hard-switched and snubber assisted designs. This is

believed to reduce acoustic noise in driven machines and is thought to extend winding insulation life [6-7]. The original prototype successfully operated at 18 kHz while subsequent PRDL designs have operated at over 50 kHz, all with negligible switching losses and without the use of snubbers or special switch drive circuitry [7][18][20-22].

A diagram of the PRDL topology and an example link voltage waveform are shown in Figures 5 and 6, respectively. The six power matrix switches are allowed to change states only when the link voltage is zero. Turn-on is accomplished under true zero voltage conditions. All switch turn-off processes begin with the link voltage fully collapsed but do not complete before the link voltage begins to rise. However, the link collapse circuit prevents the link voltage from rising more than a few tens of volts within the turn-off time of the switch, t_{off}. This allows the power matrix switches to turn off under essentially ZVS conditions, virtually eliminating switching losses.

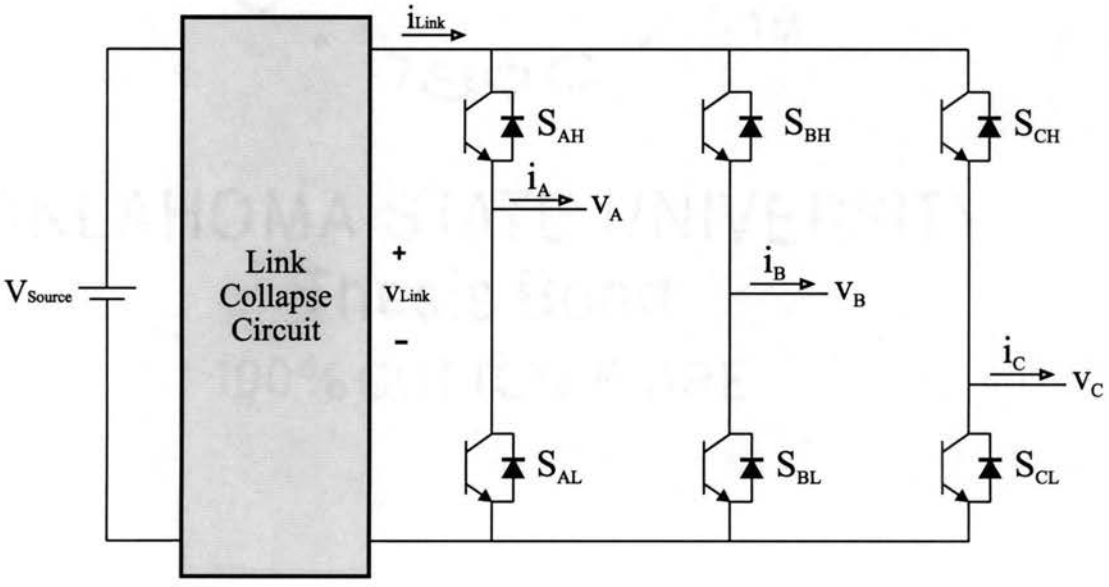


Figure 5. Schematic diagram of the three-phase PRDL topology consisting of a conventional six-switch bridge power matrix and a generalized link collapse circuit

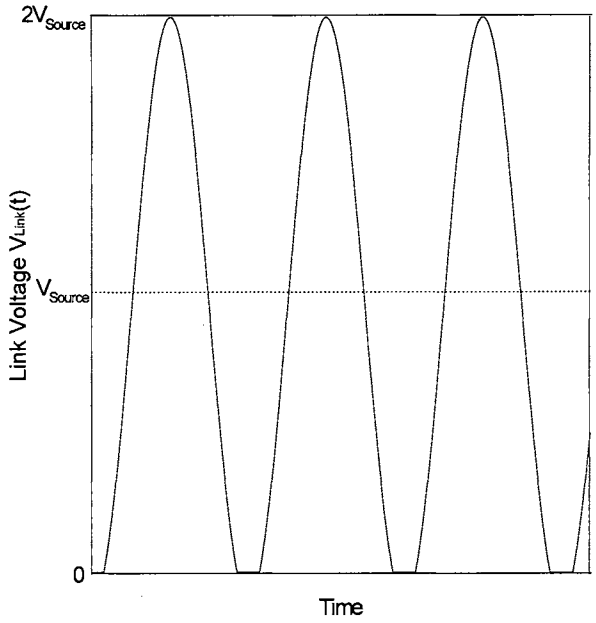


Figure 6. Generic voltage waveform of a PRDL inverter illustrating the cyclic link voltage collapse that provides near ZVS conditions

The link voltage waveform shown in Figure 6 is representative of the current initialization scheme proposed in [7] to maintain the peak link voltage constant from cycle to cycle. The link voltage pulse heights in the original PRDL prototype [6] fluctuated dramatically due to abrupt link current changes occurring in state S_0. More recent link collapse circuit designs include active elements that limit this effect by clamping the link voltage pulses at a fixed level or by adjusting the energy stored in the passive collapse circuit elements. The link dwell period at zero volts, shown in Figure 6, is characteristic of all resonant link topologies and is required to initialize the link collapse circuit for the next link cycle. The zero-voltage dwell time varies from cycle to cycle.

The PRDL topology is divided into two subclasses, synchronized and unsynchronized, based on the controllability of the link collapse circuit. The Unsynchronized Parallel Resonant DC Link (UPRDL) subclass has no explicit mechanism for controlling the timing of link collapse events. This precludes conventional Pulse Width Modulation (PWM) techniques for waveform synthesis and necessitates less precise Integral Pulse Modulation (IPM) methods. The Synchronized

Parallel Resonant DC Link (SPRDL) subclass includes a mechanism for controlling the link collapse time. In theory, this removes the IPM limitations of the UPRDL subclass but in practice provides only limited improvement due to precision limitations in the control circuitry and increased minimum pulse width.

2.4.2 UPRDL Topologies

2.4.2.1 UPRDL Voltage Synthesis The innate lack of control over the time of the link voltage collapse event relegates UPRDL inverters to IPM techniques for waveform synthesis. A conventional inverter, which has full control over its state transition events, can synthesize a static three-phase voltage $\mathbf{V_P}$ by cycling through a state sequence that satisfies both 2.3.6 and 2.3.7. A typical sequence might be: 200 μs in state S_{100}, 100 μs in state S_{110}, and 100 μs in state S_0, repeated every 400 μs. Due to IPM constraints, UPRDL inverters must approximate this particular sequence by interleaving cycles spent in states S_{100}, S_{110}, and S_0 so that on average, 50%, 25%, and 25% of the link voltage cycles are spent with the inverter in states S_{100}, S_{110}, and S_0, respectively. Figure 7 shows a typical time sequence of UPRDL inverter states illustrating the state interleaving necessitated by IPM constraints on the control system.

The inherent error in IPM arises from attempting to synthesize a single continuous pulse P_C of width T_C using a series of N consecutive pulses, each of width T_D. If N is chosen as the largest integer such that $NT_D < T_C$, the synthesized pulse may be short and produce an "undershoot" error. Similarly, if N is the smallest integer such that $NT_D > T_C$, an "overshoot" error may result. With proper selection of N, the synthesized pulse width error is limited to ½ T_D. The IPM undershoot and overshoot errors result is degraded spectral performance compared to a hypothetical conventional PWM inverter with the same switching frequency capability. The resulting UPRDL spectral performance using simple bang-bang control is comparable to a conventional PWM inverter switching at approximately 40% of the UPRDL frequency [24]. In

reality, the UPRDL switches at approximately ten times the rate of a conventional PWM inverter. Hence, spectral distortion comparable to a conventional PWM inverter operating at 2.5 times its practical switching frequency is attainable with UPRDL designs.

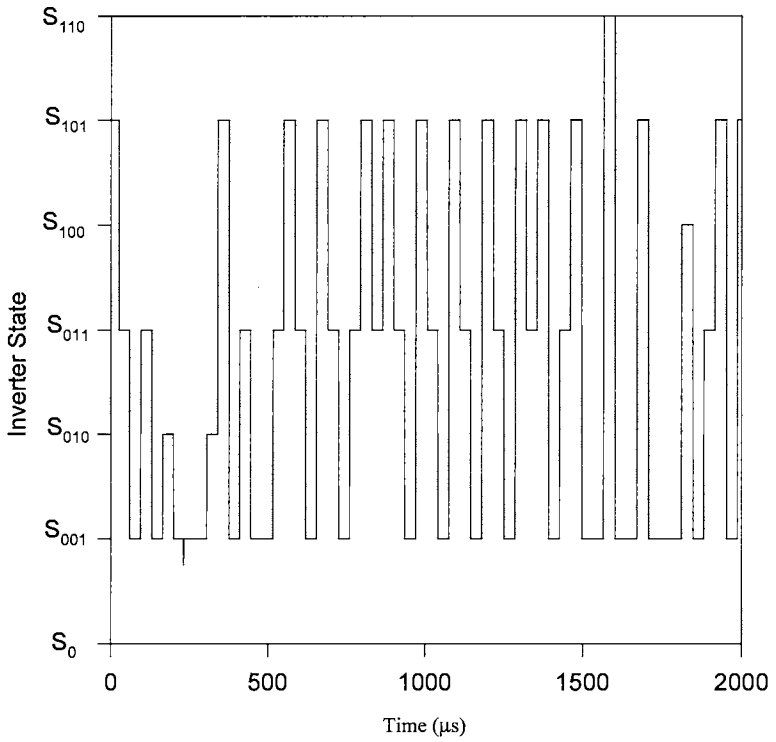


Figure 7. Example illustrating the time sequence of UPRDL inverter state visits used to synthesize a 60Hz three-phase voltage using IPM techniques

2.4.2.2 UPRDL Link Collapse Circuit Implementations The link collapse circuit in the original UPRDL inverter introduced in [6] consists of a single capacitor and inductor. The circuit's simplicity and lack of active elements are highly attractive features. Unfortunately, this configuration is particularly vulnerable to link voltage modulation resulting from abrupt link current changes during the occupancy of state S_0. This produces a peak voltage stress in the power matrix devices approximately three times that of a conventional inverter. Bose and Lai proposed a current initialization scheme to eliminated link voltage modulation through active control of the energy stored in the link collapse circuit [7]. This approach yields an unmodulated

link voltage waveform similar to that shown in Figure 6. Unfortunately, the initialization circuit requires an auxiliary voltage source and two switches operating under hard-switched conditions. Additionally, one of the switches is required to handle 2-3 times the peak load phase current. This unduly restricts the maximum inverter power rating that is achievable without resorting to switch paralleling. Although this approach reduces device voltage stress to about 2.3-2.5 times that of a comparable hard-switched conventional inverter, the elevated voltage stress combined with the complexity of the link collapse circuitry renders the design commercially unattractive.

The first practical UPRDL design was the Actively Clamped Parallel Resonant DC Link (ACPRDL), introduced by Divan in 1987 [22]. The ACPRDL link collapse circuit consists of the original UPRDL passive circuit augmented with the clamping capacitor and switch shown in Figure 8. The clamping switch inverse-parallel diode D_{Clamp} prevents the link voltage from exceeding $(1 + k)V_{source}$, where the nominal clamping coefficient k_o is typically chosen between 0.4 and unity. The active clamp switch S_{Clamp} is used to initialize L_R with sufficient current to ensure link collapse and to regulate the instantaneous clamping coefficient k about the nominal set point k_o. C_{clamp} is normally chosen so that k is controllable to within a few percent of k_o. Figure 9 shows a typical link voltage waveform for an ACPRDL inverter with $k_o = 0.58$.

The ACPRDL has the advantage of limiting voltage stresses in the power matrix devices to just under twice that of a conventional hard-switched bridge. However, the link voltage pulse widths are stretched for values of k_o less than unity. This decreases the link collapse frequency below the natural frequency of the resonant circuit. Since the resonant circuit frequency heavily influences the link dv/dt during switch turn-off, alleviating the pulse width increase by increasing the natural resonant frequency is not possible without increasing switching losses. Hence, the lower ACPRDL voltage stress comes at the cost of lower maximum achievable switching frequency [22].

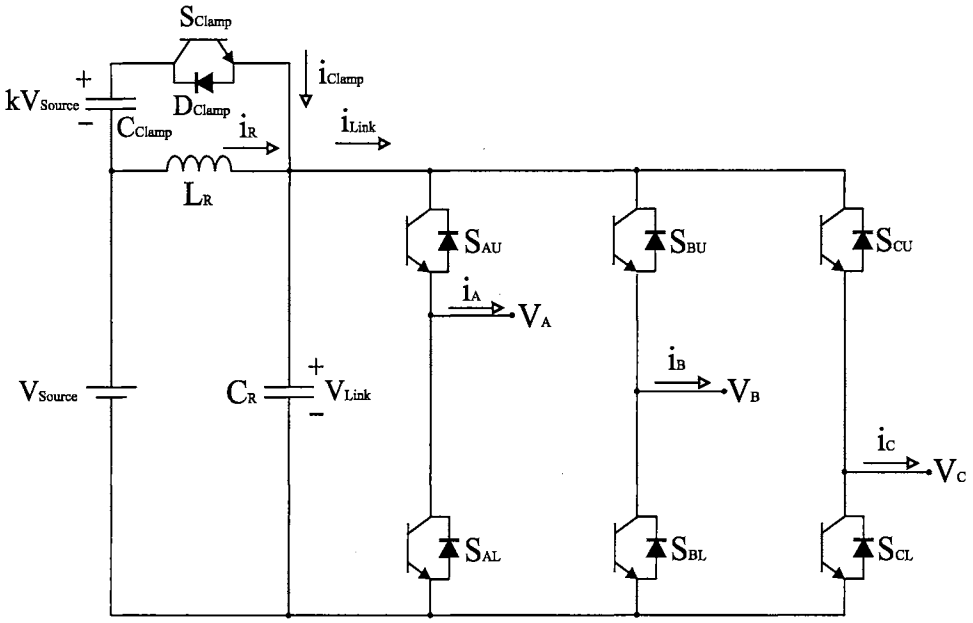


Figure 8. Schematic diagram of the three-phase ACPRDL inverter

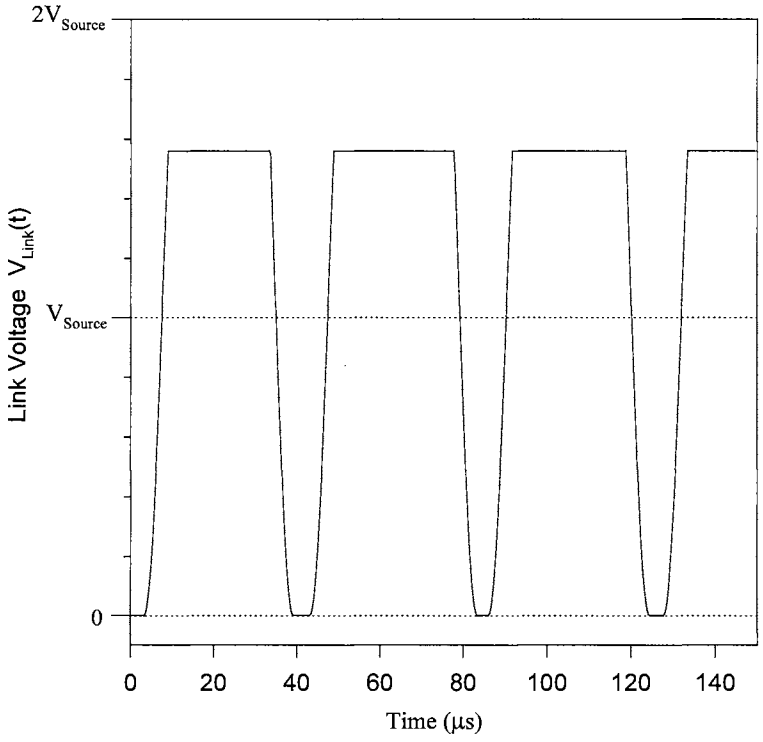


Figure 9. Typical link voltage, $V_{Link}(t)$, waveform for an ACPRDL inverter with clamping coefficient $k_0 = 0.58$

2.4.3 SPRDL Topologies

Soon after the PRDL topology was introduced, doubts arose about the waveform quality achievable using a discrete time switched source. Mohan, et. al. proposed a link collapse circuit modification to allow control of the collapse time in order to eliminate IPM quantization effects [8][9][16][20-21]. This new subclass of the PRDL topology became known as the Synchronous Parallel Resonant DC Link (SPRDL) or the quasi-resonant PRDL topology. The link collapse mechanism holds the link at the DC source voltage until it receives a command to collapse the link. Once the collapse command is received and the link voltage has collapsed to zero, the power matrix switches change states and the link returns to the supply voltage until the next link collapse command is issued. Theoretically, this removes the IPM undershoot and overshoot error innate to the UPRDL subclass. However, load current influence on the link collapse mechanism renders precise pulse width control virtually impossible without elaborate control mechanisms. The resulting pulse width error can easily reach 25% of a complete UPRDL inverter link cycle period.

An additional objective of precise pulse width control was to exploit the broad base of advanced PWM techniques developed for conventional bridge inverters over the past two decades [8]. Unfortunately, attempts to incorporate the effects of the link voltage collapse associated with each SPRDL state change into existing PWM strategies failed [16]. This precluded direct application of existing PWM methods. Secondly, all of the controllable link collapse mechanisms proposed to date require a substantial reset period following completion of each link collapse cycle before they are able to initiate a subsequent link collapse. The resulting delay typically extends the minimum pulse width achievable with a SPRDL inverter to about two to five times that of a UPRDL inverter with comparable link dv/dt characteristics. Finally, most of the SPRDL inverter proposals claim to have eliminated the voltage stress problem [8]. Unfortunately, this is only nearly true at low switching frequencies where the link collapse dwell time is negligible

compared to the time the link spends at the DC source voltage. Together, these factors detract from the perceived SPRDL advantage over the UPRDL.

A common factor in all synchronized implementations is the necessity for active devices in the link collapse circuit. The number of switches used in SPRDL collapse circuits ranges from one to three. Peak current ratings for the collapse circuit switches commonly range from 1.5 to 3.0 times the peak load phase current. Switch voltage stress is also higher for collapse circuit switches than for power matrix switches in some implementations. These factors further add to the cost of circumventing IPM.

The only comparison between the SPRDL and UPRDL subclasses based on experimental results is reported in [9]. Comparison of single-phase SPRDL and UPRDL inverters with similar minimum link pulse widths showed the SPRDL inverter RMS current distortion to be 66% of the value for a UPRDL inverter [9]. However, the comparison did not account for differences in control strategies. The SPRDL inverter used a control method that reportedly reduces low frequency distortion while the UPRDL inverter used simple bang-bang control, which is known for poor low frequency performance. Consequently, the reported 34% RMS current error reduction may be due in part to the more elaborate control scheme, detracting from the perceived SPRDL improvement. Moreover, three-phase switching requirements are more restrictive than those imposed on single-phase converters. A thorough study is needed before concluding that the SPRDL subclass is categorically superior to the unsynchronized scheme in terms of spectral performance [9].

2.4.4 The Series Resonant DC Link Inverter

Although Divan's work focused on voltage source designs, a current source dual exists and has been successfully implemented [13]. The Series Resonant DC Link (SRDL) inverter combines a conventional current-source bridge inverter with a series resonant circuit arrangement

that periodically forces the link current, $i_{Link}(t)$, to zero. A generic schematic diagram of the SRDL inverter is shown in Figure 10. The figure shows a generalized series resonant circuit driving a conventional current-source bridge inverter. Unlike the voltage-source case, which requires only unilaterally controllable switches, the current-source bridge configuration requires bilaterally controllable switches. The six power matrix bilateral switches shown in the figure are implemented using a popular configuration composed of a single unilaterally controllable switch and a simple bridge rectifier. This arrangement provides complete control of conduction through the bilateral switch, regardless of the polarity of the voltage applied across the terminals.

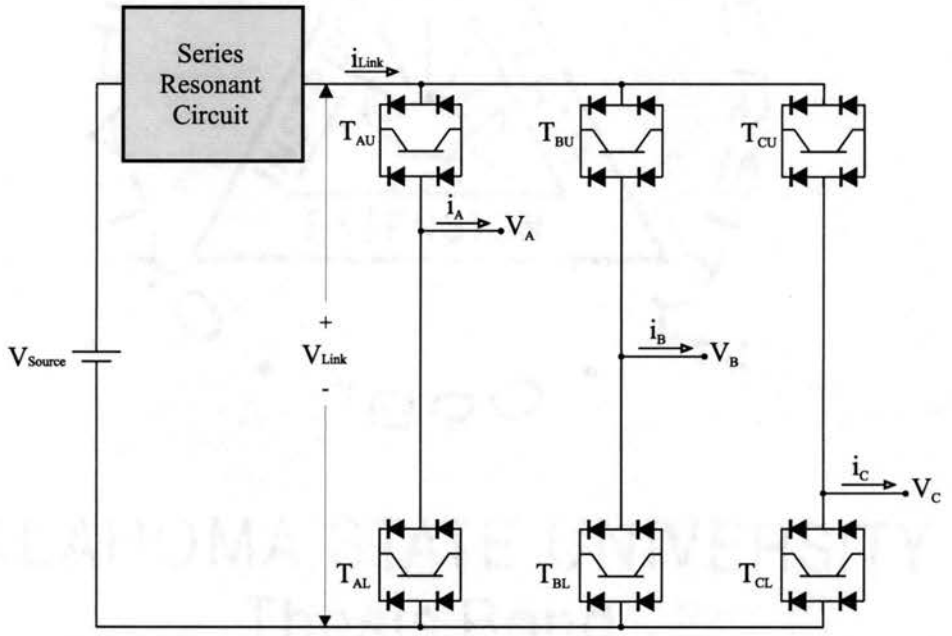


Figure 10. Schematic diagram of the SRDL topology consisting of a conventional three-phase current-source bridge inverter and a generic link current collapse circuit

Switching events are restricted to instants of zero link current, in contrast to instants of zero link voltage. The series resonant design requires shunt capacitors across the load, making it suitable for Uninterruptible Power Supply (UPS) applications but not for high performance machine drives where shunt capacitors hinder the fast torque response needed to counter abrupt load disturbances.

The term "current-source" is a misnomer when used to describe the SRDL topology. In order for the series resonant circuit to control $i_{Link}(t)$, the inverter must be fed from a voltage source. If V_{Source} in Figure 10 were replaced with a current source I_{Source}, as would be the case for a conventional current-source inverter, $i_{Link}(t)$ would always be equal to I_{Source}, rendering the series resonant circuit ineffective.

The SRDL topology has failed to receive the widespread attention given to the PRDL topology and has consequently retained many infantile flaws. Four-quadrant operation of the SRDL inverter requires bilateral switches in both the power matrix and the link current collapse circuit. Most proposed implementations use unilateral power matrix switches to reduce complexity and cost, at the price of two-quadrant capability. This presents little problem for UPS applications but prohibits dynamic braking in machine drive applications.

Like the PRDL topology, the complexity of the link current collapse circuit tends to increase as power matrix device stress and inverter performance limitations are reduced. The most recent synchronized SRDL design uses three auxiliary switches in the link current collapse circuit. The device voltage stresses in the power matrix and link current collapse circuits are 1.82 and 3.0 times the peak line-to-line voltage, respectively [13]. In summary, the SRDL topology is currently not a serious competitor to the PRDL approach.

2.5 Control Methods

2.5.1 PRDL Topology Controls

PRDL topology control techniques have received far less attention in the literature than the collapse mechanisms that distinguish the various PRDL designs. Control methods for the UPRDL subclass consist primarily of bang-bang style controllers that update the power matrix state once per link cycle. Optimal control methods that select the best inverter state for a given three-phase error current have been proposed for PRDL topology inverters [25]. Control methods for the

SPRDL subclass are surprisingly scarce considering the level of effort devoted in the early 1990's to circumventing the IPM limitations of the UPRDL subclass. Modified versions of simple PWM techniques and hysteresis band methods constitute the extent of present SPRDL control methodologies. A major obstacle to developing new PRDL control schemes is the inability to adequately model the output waveforms analytically. Load interaction with the link collapse circuit produces complex perturbations in the link voltage pulse shape, making analytical waveform analysis virtually impossible [24].

2.5.2 UPRDL Topology Controls

The bang-bang controllers used for both voltage and current control of UPRDL inverters are based on modified versions of the well known Sigma Delta Modulation (ΣΔM) method [11]. Normally, each inverter leg is separately controlled to track either a voltage or current reference signal. Figure 11 shows a block diagram of a modified ΣΔM voltage controller. The UPRDL inverter forms the sample and hold circuit shown in the figure. Unlike conventional ΣΔM, the sampling period is not constant and the pulses are non-rectangular and vary in shape slightly, hence the label "modified sample and hold." The modified sample and hold circuit updates only when a link collapse event occurs. If the integrated phase voltage error is positive, the upper inverter leg switch is left on for the following link cycle. Otherwise, the lower inverter leg switch

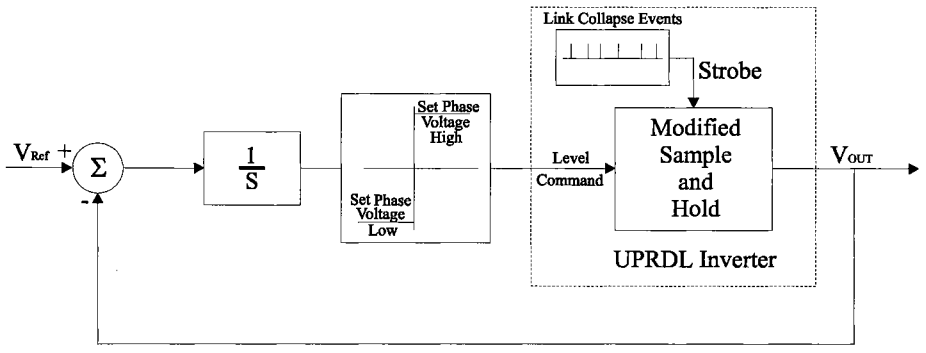


Figure 11. Block diagram of a modified ΣΔM voltage controller for one leg of a UPRDL inverter

is left on. Ideally, the integrator block nearly eliminates low frequency voltage offset. However, the integrator can "wind up" if the reference voltage V_{Ref} is near either the maximum or the minimum attainable average phase leg output voltage. If "wind up" occurs, severe voltage distortion or inverter instability can result.

Current control is generally preferred over voltage control due to superior torque response [1]. Secondly, the current transducers used in current control schemes provide a means of detecting destructive short circuit currents, adding built-in over-current protection at little extra cost. The Current Regulated Delta Modulation (CRΔM) scheme presented in [11] is the dominant current control method for UPRDL inverters. Figure 12 shows a block diagram of the CRΔM controller used for each load phase. The CRΔM method uses the series inductance of the load to integrate the phase voltage signal rather than employing a dedicated integrator block. Unlike the modified ΣΔM, the current error signal is not integrated. This leads to long run length bias and can result in significant low frequency error current.

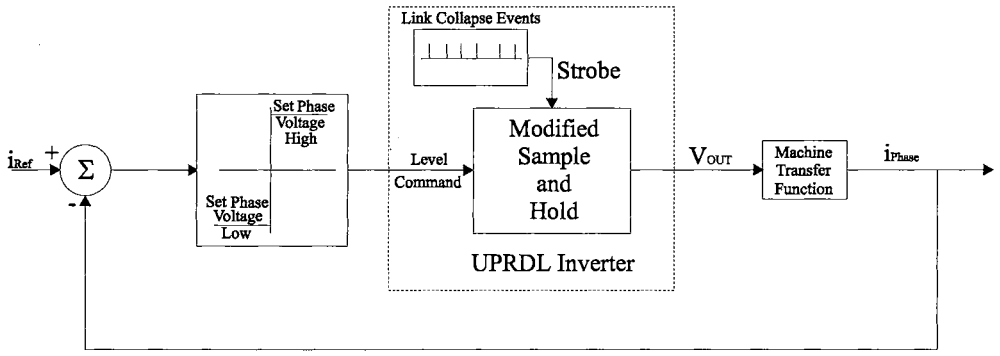


Figure 12. Block diagram of a CRΔM for one phase of a current controlled UPRDL inverter

2.5.3 SPRDL Topology Control

SPRDL voltage control methods must incorporate the effects of limited occupancy in the zero state prior to entering any of the six active states. PWM techniques that accommodate mandatory zero state occupancy exist and have been applied to SPRDL inverters [16]. However, emphasis is again placed on current control methods due to superior torque response. Unlike the UPRDL subclass, current controlled SPRDL inverters require an additional control signal to coordinate the link collapse event. All reported techniques to date use current error tolerance bands to generate the link collapse signal. The most direct approach issues a link collapse command whenever any of the load phase error currents fall outside a preset tolerance band [8]. Like the CRΔM, this method is susceptible to long run length bias and can produce significant low frequency load error currents. An alternative method, proposed for single-phase applications, uses variable tolerance band limits that are adjusted according to the error magnitude existing at the end of the previous link cycle [9].

To illustrate the variable tolerance band method, suppose the nominal phase error current tolerance band is the interval $[-h_o, h_o]$, where $h_o > 0$. Once the current error falls outside the band, the controller issues a link collapse command and the inverter changes states, forcing the error current back toward the tolerance band. Since the inverter is prevented from changing states again until the link collapse mechanism has reset, the current error may pass through the tolerance band before the link collapse mechanism is reset. This type of overshoot tends to bias the current error, resulting in significant low frequency current distortion. The method proposed in [9] adjusts the width of the tolerance band for the $k+1^{th}$ cycle following an overshoot in the k^{th} cycle such that the tolerance h_{k+1} in the $(k+1)^{th}$ cycle is equal to the magnitude of the peak current error in the k^{th} cycle. Cycles following cycles in which no overshoot occurs use the nominal tolerance band limit h_o. Unfortunately, this method has only been applied to a single-phase SPRDL inverter. Modification and evaluation of the scheme is needed for three-phase applications.

2.5.4 Optimal Inverter State Selection

Both voltage and current control schemes suffer from unmodeled system characteristics and erroneous parameter estimates. Current control of voltage source inverters is implemented through selection of inverter voltage states that drive the current error toward zero. The back EMF of the load alters the voltages that appear across the load impedance for a given static inverter voltage. This distorts the symmetry of the seven distinct static inverter voltages in voltage space, as viewed by the load impedance. This effect is nearly always ignored, resulting in the selection of sub-optimal inverter states. Cost-function methods, such as the one proposed in [23], select the best inverter state for producing a desired load current correction based on the load inductance and estimated load back EMF. This approach was developed for conventional inverters operating at a few kHz where optimal state selection is essential for good performance. Simulation of a UPRDL inverter using a simplified cost-function that considers only machine inductance and inverter voltage demonstrated improved spectral performance over the CRΔM method [25].

2.6 Summary

The chapter began with a review of three-wire three-phase voltages and currents in order to establish important nomenclature used throughout the remainder of the thesis. Next, the inverter states and static inverter voltages of a conventional three-phase voltage-source inverter were related to each other and then described in terms of a voltage space diagram. Finally, a brief history of the soft-switched inverter paradigm was reviewed. The primary focus of the review was the PRDL topology, which is summarized below.

The PRDL concept has both intrinsic advantages and liabilities that vary in degree according to the implementation of the link collapse circuit. The leading advantages of the PRDL approach, such as switching frequencies over 50kHz, complete absence of snubbers, and low acoustic noise

in driven machinery, have been experimentally verified [6-7][9][15-16]. The primary detractor of the PRDL topology as a whole is its elevated voltage stress compared to that of conventional hard-switched designs. Secondly, IPM restrictions in the UPRDL subclass along with imprecise control and significantly long minimal pulse widths in the SPRDC subclass reduce the spectral performance potential below that expected for an inverter capable of switching at such high frequencies. However, significant improvements may be possible through advanced control strategies that enhance the performance of existing PRDL topology implementations. Clearly, additional development effort is needed to enhance the control system knowledge base for both the UPRDL and SPRDL subclasses.

CHAPTER III

INVERTER SWITCHING TRAJECTORIES AND STATE OCCUPANCY

3.1 Introduction

Pulse width control and mitigation of excessive device stresses have dominated the soft-switched inverter research effort since the late 1980's [7-10][15-16][20]. Although the pulse width control problem is essentially solved, elimination of excessive device voltage stress remains unrealized. Without significant exception, all research effort has focused on voltage source resonant link topologies. Formal procedures for quantitatively relating device voltage stress levels to inverter topological characteristics are noticeably absent in the literature. Formal methods for relating fundamental spectral performance characteristics to topological properties are also lacking. Analytical tools for characterizing voltage stress and spectral characteristics as a function of topology classes are essential to identifying the underlying mechanisms limiting state-of-the-art designs. Once identified, topological modifications that circumvent these mechanisms may be apparent. The purpose of this chapter is to develop a formal framework for quantitatively characterizing voltage stress levels and certain spectral characteristics of bridge based voltage source inverters in terms of topological properties.

The trajectory that an inverter's output voltage vector follows in the course of synthesizing three-phase voltage waveforms depends on the inverter topology and control system. The discrete switching time and oscillating link voltage characteristics of resonant link voltage source topologies place strict restrictions on the output voltage trajectory that are not present in

conventional hard- switched bridge inverters. These restrictions are the root cause of high voltage stress in resonant link topologies and impose spectral performance limitations. The first sections of this chapter introduce the notions of primitive cycles, state occupancy, and minimal spanning cycles. These definitions are then used to unveil the underlying mechanisms that guide $\mathbf{V}(t)$ in voltage space for a generalized three-phase voltage-source bridge inverter. The final sections of the chapter apply the definitions to a generalized SPRDL inverter to illustrate analytic procedures and to obtain the relationship between voltage stress and spanning cycle frequency for the SPRDL topology.

3.2 Power Matrix and Link Decoupling

The definition given in Chapter II for the static inverter voltages contained in $\mathbf{V}^{*-}$ was developed for the conventional bridge inverter whose link voltage is constant. In the more general case where the link voltage is not constant, the magnitude of each voltage in $\mathbf{V}^{*-}$ is proportional to the link voltage. For the PRDL topology, the voltages in $\mathbf{V}^{*-}(t)$ converge to $\mathbf{V}_0 = \vec{\mathbf{0}}$ as $V_{Link}(t) \rightarrow 0$, leaving $\mathbf{V}^{*-}$ ill defined for $V_{Link}(t) = 0$. Consequently, the previous definition of $\mathbf{V}^{*-}$ breaks down for bridge topologies with time varying link voltages. In addition, $\mathbf{S}^*$ and $\mathbf{S}^{*-}$ are not well defined for $V_{Link}(t) = 0$. To resolve these difficulties, define the power matrix to be in S_0 whenever $V_{Link}(t) = 0$. Then, redefine $\mathbf{S}^*$, $\mathbf{S}^{*-}$, $\mathbf{V}^*$, and $\mathbf{V}^{*-}$ as given in 3.2.1 through 3.2.4 to accommodate a time dependent link voltage.

$$\mathbf{S}^{*-} = \begin{cases} \{S_{100}, S_{110}, S_{010}, S_{011}, S_{001}, S_{101}\} & V_{Link}(t) > 0 \\ \varnothing & \text{Otherwise} \end{cases} \qquad 3.2.1$$

$$\mathbf{S}^* = \mathbf{S}^{*-} \cup \{S_0\} \qquad 3.2.2$$

$$\mathbf{V}^{*-}(t)=\begin{cases}\left\{\frac{2}{3}V_{Link}(t)\hat{\psi}_i \mid i\in \mathbf{S}^{*-}\right\} & V_{Link}(t)>0\\ \varnothing & \text{Otherwise}\end{cases} \qquad 3.2.3$$

$$\mathbf{V}^{*}(t)=\mathbf{V}^{*-}(t)\cup\{\mathbf{V}_0\} \qquad 3.2.4$$

Based on the definition of $\mathbf{V}^{*}(t)$, all bridge inverter voltage trajectories are a series of finite length paths in voltage space whose endpoints are contained in $\mathbf{V}^{*}(t)$ for some t. The shape of the finite length paths depend on the inverter leg voltages $V_A(t)$, $V_B(t)$, and $V_C(t)$. In turn, each inverter leg voltage depends on the link voltage and the power Matrix State. During power matrix state transitions, a transitioning leg voltage could lie anywhere between the lower and upper link rail potentials. Normalizing the inverter leg voltages with respect to the link voltage provides a convenient mechanism for expressing the inverter output voltage as the product of the link voltage and a function of the power matrix state. Define $\mathbf{h}(t)$ to be the normalized inverter output voltage given by,

$$\mathbf{h}(t)=\begin{cases}\frac{3}{2}\frac{\mathbf{V}(t)}{V_{Link}(t)} & V_{Link}(t)>0\\ \mathbf{0} & V_{Link}(t)=0\end{cases} \qquad 3.2.5$$

The inverter output voltage, in terms of $\mathbf{h}(t)$ and $V_{Link}(t)$, is given by,

$$\mathbf{V}(t)=\tfrac{2}{3}V_{Link}(t)\,\mathbf{h}(t) \qquad 3.2.6$$

The preceding definitions provide the decoupling necessary to describe the power matrix switching characteristics and link voltage behavior separately. Let $\mathbf{H}^{\dagger}$ be the hexagonal compact set shown in Figure 13 whose vertices are the unit vectors in Ψ. Regardless of the inverter output voltage $\mathbf{V}(t)$, $\mathbf{h}(t)$ is an element of $\mathbf{H}^{\dagger}$ for all t. Figure 13 shows example mappings of $\mathbf{V}(t)$ into $\mathbf{H}^{\dagger}$

corresponding to inverter state transitions for conventional and resonant link topologies. The dotted line depicts one of many possible trajectories from S_{011} to S_{100} for a conventional hard-switched inverter with constant link voltage. In general, the path between $\hat{\psi}_{011}$ and $\hat{\psi}_{100}$ in $\mathbf{H}^{\dagger}$ could be any finite length path in $\mathbf{H}^{\dagger}$ resulting from simultaneous level changes in all three inverter legs. The dashed line shows another conventional inverter state transition, this time between S_{010} and S_{100}. Again, the path is curved due to simultaneous level changes in two of the three inverter legs. However, the path is restricted to the region in $\mathbf{H}^{\dagger}$ for which the non-transitioning leg voltage remains constant, the quadrilateral $\hat{\psi}_{100} - \hat{\psi}_{110} - \hat{\psi}_{010} - \vec{\mathbf{0}}$ in this case. The solid line shows a transition between S_{110} and S_{100}. Since only one leg changes levels, the path is a straight line.

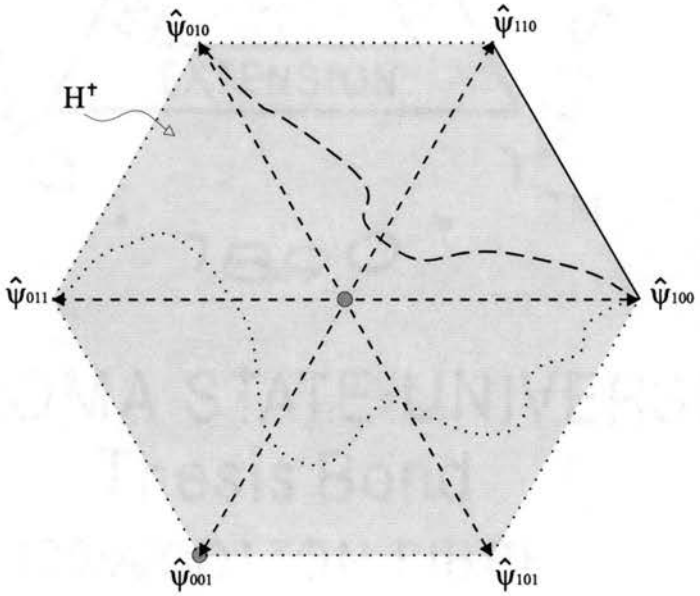


Figure 13. Normalized inverter output voltage diagram showing the continuous mapping of **V**(t) for conventional inverters and the discreet mapping of **V**(t) for resonant link topologies

True soft-switched resonant link topologies change states only when $V_{Link}(t) = 0$. Consequently, their state transitions are discontinuous in $\mathbf{H}^{\dagger}$. The circles located at the origin and the tip of $\hat{\psi}_{001}$ illustrate the discontinuous mapping of **V**(t) into $\mathbf{H}^{\dagger}$ for a transition between S_{001}

and S_0. It is important to note that the virtual absence of switching loss in resonant link topologies is due to zero link voltage during switching rather than the apparent instantaneous transition between states.

3.3 State Occupancy

The definition of **h**(t) provides an unambiguous method for specifying the state of the power matrix for any **V**(t). The power matrix is clearly in state k at time t if **h**(t) satisfies 3.3.1.

$$\mathbf{h}(t) \in \left\{ \hat{\psi}_k \mid k \in \mathbf{S}^{*-} \right\} \cup \left\{ \vec{0} \right\} \qquad 3.3.1$$

For resonant link topologies, no additional consideration is necessary since 3.3.1 holds for all t. However, 3.3.1 is insufficient for conventional topologies and non-resonant link alternatives that perform power matrix transitions while $V_{Link}(t) > 0$. Consequently, further definition is needed to handle the general case in which **h**(t) follows a continuous trajectory in $\mathbf{H}^{\dagger}$ between the elements of Ψ. In this case, the power matrix does not always fully occupy a single state in $\mathbf{S}^*$. Instead, two or more states in $\mathbf{S}^*$ are partially occupied. In order to describe the occupancy analytically, define $\alpha_k(t)$ as the power matrix state occupancy in state $k \in \mathbf{S}^*$ at time t and subject to the normalization constraints given in 3.3.2 and 3.3.3.

$$\alpha_i(t) \in [0,1] \quad \forall\, t \text{ and } \forall\, i \in \mathbf{S}^* \qquad 3.3.2$$

$$\sum_{i \in \mathbf{S}^*} \alpha_i(t) = 1 \quad \forall\, t \qquad 3.3.3$$

The one-to-one correspondence between the element of $\mathbf{S}^{*-}$ and the vertices of $\mathbf{H}^{\dagger}$ suggests the following relationship between **h**(t) and the $\alpha_i(t)$.

$$\mathbf{h}(t) = \sum_{i \in \mathbf{S}^{*-}} \alpha_i(t) \hat{\psi}_i \qquad 3.3.4$$

Equations 3.3.2 and 3.3.3 together provide three scalar equations for identifying the seven state occupancy coefficients associated with a given **h**(t). Setting all state occupancy coefficients to zero, except for $\alpha_0(t)$ and the coefficients corresponding to the two adjacent active states whose ψ_k form the equilateral triangle containing **h**(t), resolves the problem. If **h**(t) is directly between two states, only the occupancy coefficients for those two states need be considered. Solving for the $\alpha_i(t)$ and using 3.3.4 in 3.2.3 produces the decoupled output voltage expression given in 3.3.5.

$$\mathbf{V}(t) = \tfrac{2}{3} V_{Link}(t) \sum_{i \in \mathbf{S}^{*-}} \alpha_i(t) \hat{\psi}_i \qquad 3.3.5$$

Decoupling the power matrix state and link voltage is primarily geared toward providing a clear definition of the physical inverter state for use in circuit synthesis, modeling, and simulation. A slightly different occupancy definition is needed to effectively discuss voltage synthesis. For this purpose, it is convenient to express **V**(t) in terms of the static voltages corresponding to a conventional inverter with the same voltage stress level as the inverter under consideration. Let V_{Lp} be the link voltage of a reference conventional inverter, where V_{Lp} is the peak value of $V_{Link}(t)$ occurring for all values of t. This is expressed in 3.3.6 using the "limit superior" operator [32].

$$V_{Lp} = \limsup_{t \to \infty} V_{Link}(t) \qquad 3.3.6$$

Let **H** be the hexagonal compact set in voltage space with the vertices contained in $\left\{ \tfrac{2}{3} V_{Lp} \hat{\psi}_i \mid i \in \mathbf{S}^{*-} \right\}$. **H** then contains **V**(t) for all t and the vertices of **H** are the static inverter voltages of a conventional inverter with link voltage V_{Lp}.

The notion of effective state occupancy in the states corresponding to the vertices of **H** is convenient for voltage synthesis analysis. Next, employ a method similar to that used to represent

h(t) in terms of the elements of Ψ. **V**(t) can be written as a weighted sum of the vertex vectors of **H**. Let $\eta_i(t)$ be the effective state occupancy for $i \in \mathbf{S}^*$, as defined in 3.3.7

$$\eta_i(t) = \begin{cases} \frac{V_{Link}(t)}{V_{Lp}} \alpha_i(t) & i \in \mathbf{S}^{*-} \\ 1 - \frac{V_{Link}(t)}{V_{Lp}} \sum_{i \in \mathbf{S}^{*-}} \alpha_i(t) & i = 0 \end{cases} \qquad 3.3.7$$

V(t) is then given in terms of the effective state occupancies as,

$$\mathbf{V}(t) = \tfrac{2}{3} V_{Lp} \sum_{i \in \mathbf{S}^{*-}} \eta_i(t) \hat{\psi}_i \qquad 3.3.8$$

A second useful concept is the idea of mean effective state occupancy. The mean effective state occupancy coefficient σ_i, $i \in \mathbf{S}^*$, represents the total fraction of time the power matrix spends in state i and accounts for both periods of partial and full occupancy. The expression for σ_i, $i \in \mathbf{S}^{*-}$, is given in 3.3.9.

$$\sigma_i = \lim_{T \to \infty} \frac{1}{T} \int_0^T \eta_i(t) dt \quad i \in \mathbf{S}^{*-} \qquad 3.3.9$$

Using 3.3.7 and 3.3.9 along with the constraints on the $\alpha_i(t)$ yields the expression for the mean effective state occupancy in $\mathbf{S}_0$ given in 3.3.10.

$$\sigma_0 = 1 - \sum_{i \in \mathbf{S}^{*-}} \sigma_i \qquad 3.3.10$$

3.4 Hexagonal Coordinates

The symmetry of **H** suggests a coordinate system other than the orthonormal **u-v** system for locating $\mathbf{V}_P$ in **H**. Notice that for any $\mathbf{V}_P \in \mathbf{H}$ such that $|\mathbf{V}_P| > 0$, there is a $V_{Ph} > 0$ such that $\mathbf{V}_P$ lies on the hexagon whose vertices are $\{ V_{Ph}\hat{\psi}_i \mid i \in \mathbf{S}^{*-}\}$. In order to specify the region of **H** containing $\mathbf{V}_P$, let Ω_k, $k \in \mathbf{S}^{*-}$, be the triangular compact set in **H** with vertices $\frac{2}{3} V_{Lp}\hat{\psi}_k$, $\vec{\mathbf{0}}$, and $\frac{2}{3} V_{Lp}\hat{\psi}_{k+}$. Next, parameterize $\mathbf{V}_P$ along the hexagonal edge using the parameter $V_{P_\gamma} \in [0,1]$ as illustrated in Figure 14.

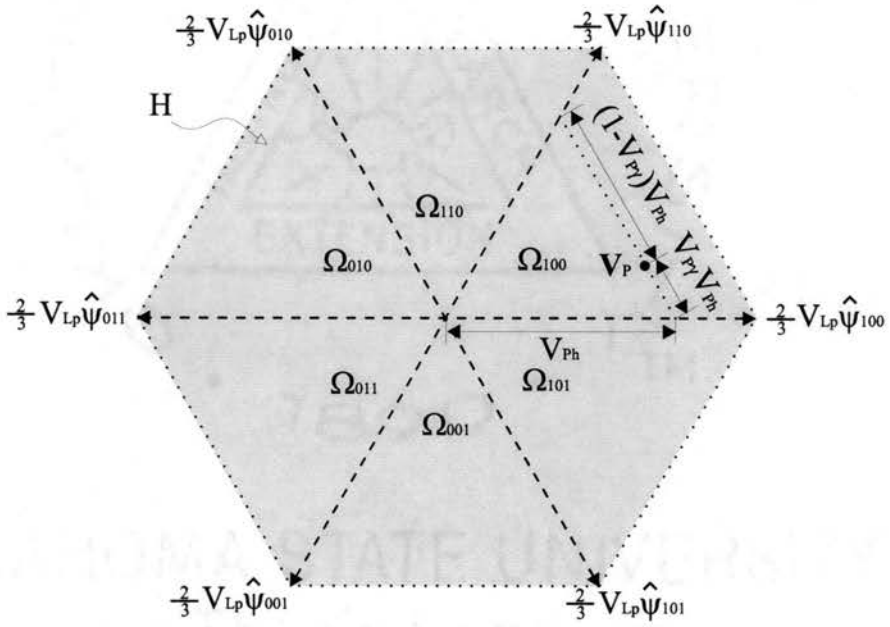


Figure 14. Voltage space diagram illustrating the hexagonal coordinate system for $\mathbf{V}_P \in \mathbf{H}$

If $\mathbf{V}_P \notin (\Omega_j \cap \Omega_{j+})$ for any $j \in \mathbf{S}^{*-}$ but $\mathbf{V}_P \in \Omega_i$ for some $k \in \mathbf{S}^{*-}$, $\mathbf{V}_P$ is given in hexagonal coordinates as $(V_{Ph}, V_{P\gamma}, k)$. If $|\mathbf{V}_P| > 0$ and $\mathbf{V}_P \in (\Omega_i \cup \Omega_{i+})$ for some $i \in \mathbf{S}^{*-}$, adopt the convention $\mathbf{V}_P = (V_{Ph}, 0, i^+)$. Finally, if $|\mathbf{V}_P| = 0$, denote $\mathbf{V}_P$ as $(0,0,S_0)$. With these definitions, $\mathbf{V}_P$

is uniquely defined in hexagonal coordinates for every $\mathbf{V}_P \in \mathbf{H}$. Transformations between orthonormal and hexagonal coordinates for $\mathbf{V}_P \in \Omega_{100}$ are given in 3.4.1 through 3.4.4.

$$V_{Ph} = V_{Pu} + \frac{V_{Pv}}{\sqrt{3}} \quad \mathbf{V}_p \in \Omega_{100} \tag{3.4.1}$$

$$V_{P\gamma} = \begin{cases} \dfrac{2V_{Pv}}{\sqrt{3}V_{Pu} + V_{Pv}} & V_{Pu} > 0, V_{Pv} > 0, \mathbf{V}_P \in \Omega_{100} \\ 0 & V_{Pu} = 0, V_{Pv} = 0, \mathbf{V}_P \in \Omega_{100} \end{cases} \tag{3.4.2}$$

$$V_{Pu} = V_{Ph} - \frac{V_{Ph}V_{P\gamma}}{2} \quad \mathbf{V}_P \in \Omega_{100} \tag{3.4.3}$$

$$V_{Pv} = \frac{\sqrt{3}}{2} V_{Ph}V_{P\gamma} \quad \mathbf{V}_P \in \Omega_{100} \tag{3.4.4}$$

Another useful expression is the vector magnitude of $\mathbf{V}_P$ in terms of the hexagonal coordinates V_{Ph} and $V_{P\gamma}$. It is easily show with the aid of Figure 14 that $|\mathbf{V}_P|$ is equal to,

$$|\mathbf{V}_P| = V_{Ph}\sqrt{V_{P\gamma}^2 - V_{P\gamma} + 1} \tag{3.4.5}$$

The definition of mean effective state occupancy given in 3.3.9 has special meaning when $\mathbf{V}_P$ is specified in hexagonal coordinates. Suppose $\mathbf{V}_P \in \Omega_i$ for some $i \in \mathbf{S}^{*-}$. The average voltage contribution from occupancy in states S_i and S_{i+} is $\frac{2}{3}\sigma_i V_{Lp}\hat{\psi}_i$ and $\frac{2}{3}\sigma_{i+} V_{Lp}\hat{\psi}_{i+}$, respectively. Equivalently, the effective fraction of time an inverter with static link voltage V_{Lp} spends in active states $\mathbf{S}_i$ and $\mathbf{S}_{i^+}$ is precisely σ_i and σ_{i+}, respectively. Consequently, the expression for a static synthesized voltage $\mathbf{V}_P$ in terms of σ_k and σ_{k+} is given by 3.4.6.

$$\mathbf{V}_P = \tfrac{2}{3}\sigma_i V_{Lp}\hat{\psi}_i + \tfrac{2}{3}\sigma_{i^+} V_{Lp}\hat{\psi}_{i^+} \text{ for some } i \in \mathbf{S}^{*-} \tag{3.4.6}$$

Using the fact that $\sigma_0 = 1 - \sigma_i - \sigma_{i+}$ in 3.4.6 yields,

$$\mathbf{V}_P = \tfrac{2}{3}(1-\sigma_0)V_{Lp}\left[\frac{\sigma_i}{1-\sigma_0}\hat{\psi}_i + \left(1-\frac{\sigma_i}{1-\sigma_0}\right)\hat{\psi}_{i^+}\right] \qquad 3.4.7$$

Since $\sigma_i \in [0, 1 - \sigma_0] \; \forall \; \mathbf{V}_P \in \Omega_i$,

$$0 \le \frac{\sigma_i}{1-\sigma_0} \le 1$$

Hence, 3.4.7 defines the point $\mathbf{V}_P$ lying in Sector Ω_i in terms of the hexagonal coordinates V_{Ph} and $V_{P\gamma}$ given by,

$$V_{Ph} = \tfrac{2}{3}(\sigma_i + \sigma_{i+})V_{Lp} \qquad 3.4.8$$

$$V_{P\gamma} = \frac{\sigma_{i^+}}{\sigma_i + \sigma_{i^+}} \qquad 3.4.9$$

Equation 3.4.8 indicates that the maximum effective link voltage is equal to the maximum sum of the mean effective active state occupancies multiplied by $\frac{2}{3}V_{Lp}$. As will be seen latter, the significance of the sum of the mean effective active state occupancies is sufficient to justify the special symbol σ_A defined in 3.4.10.

$$\sigma_A = \sigma_i + \sigma_{i^+} \qquad 3.4.10$$

Alternatively,

$$\sigma_A = 1 - \sigma_0 \qquad 3.4.11$$

Using 3.4.10 in 3.4.8 and 3.4.9 yields,

$$V_{Ph} = \frac{2}{3}\sigma_A V_{Lp} \qquad 3.4.12$$

$$V_{P\gamma} = \frac{\sigma_{i^+}}{\sigma_A} \quad \sigma_A > 0 \qquad 3.4.13$$

To achieve the same low voltage stress as a conventional bridge inverter, a given topology must be capable of synthesizing any voltage $\mathbf{V}_P$ lying in the largest circle contained in **H**. Specifically,

$$|\mathbf{V}_P| \leq \frac{V_{Lp}}{\sqrt{3}} \qquad 3.4.14$$

It is easily shown using 3.4.5 and 3.4.12 in 3.4.14 that an equivalent inequality expressing the minimum achievable σ_A as a function of $V_{P\gamma}$ is,

$$\sigma_A \geq \frac{\sqrt{3}}{2} \cdot \frac{1}{\sqrt{V_{P\gamma}^2 - V_{P\gamma} + 1}} \qquad 3.4.15$$

The significance of 3.4.15 is that any bridge-based topology that does not satisfy the inequality, due to either structural or control limitations, operates with higher peak power matrix voltage level than a conventional bridge inverter. It follows that the SPRDL subclass can only achieve near minimal voltage stress if the time spent in the active states is much larger than the time inadvertently spent in S_0 during commanded transitions between active states.

3.5 Primitive Cycles

Voltage trajectory characteristics are an important indicator of an inverter's waveform synthesis capabilities. The allowed trajectories, and equally importantly the forbidden trajectories, between elements of $\mathbf{V}^*(t)$ strongly influence device voltage stress and spectral performance of a given topology. Studying $\mathbf{V}(t)$ over one or more complete cycles of a synthesized three-phase output waveform involves arduous interaction with the control system and load. A more practical approach is to study the synthesis process for an arbitrary static three-phase voltage $\mathbf{V}_P$ in terms of power matrix switching events. This method leads to a trajectory characterization scheme that focuses on "microscopic" trajectory elements, making the analysis tractable.

In order to minimize output waveform distortion, high fidelity control systems limit power matrix state occupancy to the three states defining the Ω_i containing $\mathbf{V}_P$. If $\mathbf{V}_P$ lies in the interior of Ω_i, an example of the state sequence that could be used to synthesize $\mathbf{V}_P$ is: $\{S_i, S_{i+}, S_i, S_0, S_i, S_{i+}, S_i, S_0, \ldots\}$. The manner in which the inverter voltage trajectory $\mathbf{V}(t)$ passes through the corresponding elements of $\mathbf{V}^*(t)$ depends on $\eta_i(t)$ and $\eta_{i+}(t)$, which are themselves topology dependent. Analyzing the trajectory over a lengthy sequence of state visits is again not practical. Instead, recognize that the voltage trajectory in Ω_i can be partitioned into a sequence of closed loops such that the corresponding $\mathbf{h}(t)$ for each closed loop passes through either two or three of the vertices of $\Omega^\dagger_i$ exactly once. There are exactly four dissimilar closed loops in each $\Omega^\dagger_i$ of $\mathbf{H}^\dagger$ satisfying this condition. Each loop is unique in that no two loops visit exactly the same set of power matrix states. Since the loops are the most primitive cyclic elements in the overall trajectory, denoting them as "primitive cycle trajectories" seems appropriate. Additionally, let "primitive cycle" denote the sequence of states in Ω_i visited over the course of a particular primitive cycle trajectory. The state sets that uniquely identify the four distinct primitive cycles for a given $\Omega^\dagger_i$ are:

- $\chi_{i,0} = \{S_i, S_0\}$
- $\chi_{i+,0} = \{S_{i+}, S_0\}$
- $\chi_{i,i+} = \{S_i, S_{i+}\}$
- $\chi_{i,0,i+} = \{S_i, S_0, S_{i+}\}$

Definition: Let a segment of $\mathbf{V}(t)$ be a primitive cycle trajectory in Ω_i corresponding to primitive cycle state set χ_k, $k \in \{\{i, 0\}, \{i^+, 0\}, \{i, i^+\}, \{i, 0, i^+\}\}$, if and only if:

1) $\mathbf{V}(t_1) = \mathbf{V}(t_2)$ for some t_1 and t_2 where $t_2 > t_1$

2) $\mathbf{V}(t) \in \Omega_i \ \forall\ t \in [t_1, t_2]$

3) The power matrix enters each state in χ_k exactly once $\forall\ t \in [t_1, t_2]$

Let Γ_i denote the set of all possible primitive cycle state sets in Ω_i,

$$\Gamma_i = \{\chi_{i,0}, \chi_{i+,0}, \chi_{i,i+}, \chi_{i,0,i+}\}$$

The primitive cycle definition results in two subclasses of cycles involving either two or three states. Since the distinction is useful in latter discussions, denote $\chi_{i,0}$, $\chi_{i+,0}$, and $\chi_{i,0,i+}$ as two-state primitive cycles and $\chi_{i,0,i+}$ as a three state primitive cycle.

The sequence and duration of visits to the states in a given primitive cycle depends on the state occupancy coefficients. Let $\mathbf{V}_\mu$ be the mean voltage resulting from a particular primitive trajectory beginning at time t_1 and ending at time t_2. $\mathbf{V}_\mu$ is defined in terms of the state occupancy functions and the link voltage in 3.5.1.

$$\mathbf{V}_\mu = \frac{2}{3(t_2 - t_1)} \sum_{i \in S^*} \int_{t_1}^{t_2} V_{Link}(t)\alpha_i(t)\hat{\psi}_i dt \qquad 3.5.1$$

For convenience, $\mathbf{V}_\mu$ is redefined in terms of the effective state occupancy functions in 3.5.2.

$$\mathbf{V}_\mu = \frac{2V_{Lp}}{3(t_2 - t_1)} \sum_{i \in S^*} \int_{t_1}^{t_2} \eta_i(t) \hat{\psi}_i \, dt \qquad 3.5.2$$

For $\chi_{i,0}$ and $\chi_{i+,0}$, $\mathbf{V}_\mu$ lies along the vectors $\frac{2}{3} V_{Lp}\psi_i$ and $\frac{2}{3} V_{Lp}\psi_{i+}$, respectively. For $\chi_{i,i+}$, $\mathbf{V}_\mu$ lies between $\frac{2}{3} V_{Lp}\psi_i$ and $\frac{2}{3} V_{Lp}\psi_{i+}$ if the link voltage is constant but may dip into the interior of Ω_i if V_{Link} is time dependent. In contrast, $\chi_{i,0,i+}$ is the only primitive cycle whose $\mathbf{V}_\mu$ always lies in the interior of Ω_i. Figure 15 illustrates the four primitive cycle trajectories for Ω_{100} and depicts example locations of $\mathbf{V}_\mu$ for each state set in Γ_i. Note that for the case of $\chi_{i,0,i+}$, the trajectory is either clockwise or counter-clockwise.

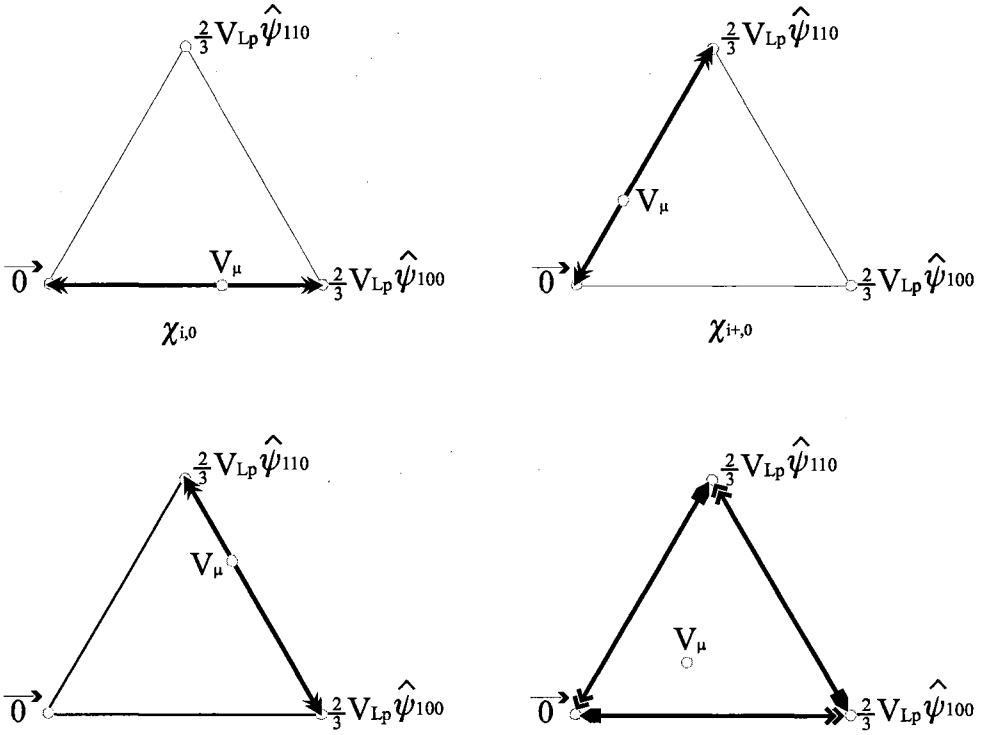


Figure 15. Illustration of possible primitive cycle trajectories and corresponding mean voltages $\mathbf{V}_\mu$ in Ω_{100} for the four primitive cycle state sets in Γ_{100}

3.6 Minimal Spanning Cycles

The previous section presented a method of decomposing the bridge inverter output voltage trajectory into a collection of basic elements. The next step is to discuss how an arbitrary static voltage $\mathbf{V}_P \in \mathbf{H}$ can be synthesized using the primitive trajectories available in a given bridge inverter topology. The obvious choice for synthesizing a voltage lying in the interior of some Ω_i is to use one cycle of $\chi_{i,0,i+}$. However, the set of all possible $\mathbf{V}_\mu$ for $\chi_{i,0,i+}$ may not cover the entire interior of Ω_i due to inverter topology or control limitations. In this case, it is necessary to use an ensemble of primitive trajectories for which the time weighted average equals $\mathbf{V}_P$. Additionally, it may be that one or more of the four primitive cycles are not available, as in the case of resonant link topologies where $\chi_{i,i+}$ and $\chi_{i,0,i+}$ are disallowed. In this case, at least two of the remaining primitive cycles must be combined to synthesize a voltage in the interior a given Ω_i. Voltages lying on the boundary of Ω_i can only be synthesized using the primitive trajectories on which they lie. Multiple cycles in the corresponding primitive cycle may be necessary if the set of all possible $\mathbf{V}_\mu$ for the cycle does not cover the entire boundary of Ω_i.

Primitive cycle trajectories were introduced to categorize fundamental cyclic state sequences. The next natural step is to identify the most elementary collections of primitive cycles that can synthesize voltages in the interior of **H**. In general, visits to all three states defining a given Ω_i are necessary to synthesize any voltage in the interior of Ω_i. Define a minimal spanning cycle for a given Ω_i as a sequence of complete primitive cycles such that two of the three states defining Ω_i are visited exactly once and the third state is visited at least once but no more than twice. There are four unique sets composed of one or more primitive cycles that satisfy this criterion:

- $\{\chi_{i,0,i+}\}$
- $\{\chi_{i,i+}, \chi_{i,0}\}$

- $\{\chi_{i,i+}, \chi_{i+,0}\}$
- $\{\chi_{i,0}, \chi_{i+,0}\}$

Let the duration of a given spanning cycle be T_{SC}. The contribution of each active state voltage over the duration of the spanning cycle can be represented in terms of the effective occupancy time spent in a particular active state, as defined in 3.6.1 and 3.6.2.

$$T_i = \int_{T_{SC}} \eta_i(t)dt \qquad 3.6.1$$

$$T_{i+} = \int_{T_{SC}} \eta_{i+}(t)dt \qquad 3.6.2$$

Using the definition of effective state occupancy, the effective time spent in S_0 during one cycle is simply $T_{SC} - T_i - T_{i+}$. A more useful parameter is the amount of time T_0 the inverter fully occupies S_0, as defined in 3.6.3.

$$T_0 = \int_{T_{SC}} a(t)dt \quad \text{where } a(t) = \begin{cases} 1 & \text{if } \alpha_0(t) = 1 \\ 0 & \text{Otherwise} \end{cases} \qquad 3.6.3$$

In the special case where $\eta_i(t)$ and $\eta_{i+}(t)$ are periodic with period T_{SC}, it is easily shown using 3.3.9, 3.6.1, and 3.6.2 that,

$$T_i = \sigma_i T_{SC} \qquad 3.6.4$$

$$T_{i+} = \sigma_{i+} T_{SC} \qquad 3.6.5$$

Using 3.6.4 and 3.6.5 in 3.4.8 and 3.4.9 produces:

$$V_{Ph} = \frac{2}{3} \frac{V_{Lp}(T_i + T_{i+})}{T_{SC}} \qquad 3.6.6$$

$$V_{P\gamma} = \frac{T_{i+}}{T_i + T_{i+}} \tag{3.6.7}$$

Using 3.6.6, 3.4.8, and 3.4.10 yields,

$$\sigma_A = \frac{T_i + T_{i+}}{T_{SC}} \tag{3.6.8}$$

Other useful parameter definitions are:

T_{ti} ≡ Time required for $\eta_i(t)$ to transition between 0 and 1, $i \in \mathbf{S}^*$. This is assumed to be the same for transitions from 0 to 1 and from 1 to 0.

T_{ci} ≡ The minimum state occupancy time defined as the minimum time in which $\eta_i(t)$, $i \in \mathbf{S}^*$, can transition from 0 to 1 and return to 0.

T_{pi} ≡ The minimum effective state occupancy time in state $i \in \mathbf{S}^*$ as defined by,

$$T_{p_i} = \int_{\tau=t_1}^{t_1+T_{c_i}} \eta_i(\tau) d\tau \tag{3.6.9}$$

where, t_1 is such that $\eta_i(t_1) = \eta_i(t_1+T_{ci}) = 0$ and $\eta_i(t_2) = 1$ for some $t_2 \in [t_1, t_1 + T_{ci}]$.

$$\beta_i \equiv \min\left(\frac{T_i}{T_{p_i}}, \frac{T_{i+}}{T_{p_{i+}}}\right) \tag{3.6.10}$$

$$\lambda_i \equiv \frac{T_{p_i}}{T_{t_i}} \tag{3.6.11}$$

Finally, let the spanning cycle frequency, f_{SC}, be defined as,

$$f_{SC} \equiv \frac{1}{T_{SC}} \tag{3.6.12}$$

The fundamental definitions now exist for comparing inverter topologies in terms of low level voltage synthesis characteristics. The spanning cycle frequency f_{SC} defines the lower frequency bound on the distortion signal for a given spanning cycle. The axial component $V_{\mu h}$ of the mean vector voltage $\mathbf{V}_{\mu}$ associated with a particular spanning cycle is often, at least in part, an inversely proportional function of f_{SC}. For example, the maximum achievable value of $V_{\mu h}$ for SPRDL topologies is only realized as $f_{SC} \rightarrow 0$.

3.7 The Spanning Cycle Frequency Metric

Ideally, closed form expressions for inverter output spectral power density would be used to compare candidate topologies and guide development of new structures and control strategies. In reality, such expressions, at least meaningful ones, are simply too difficult to obtain [24] . Without complete spectral information, incomplete, yet calculable, metrics become invaluable. A major premise of this work is that the spanning cycle frequency is such a metric. Knowing f_{SC} for a given voltage $\mathbf{V}_P$ establishes a lower frequency bound on the distortion spectrum. Since the winding inductance and inertial mass of most electrical machines tend to filter out the motion effects of high frequency distortion components, it follows that a lower bound on the distortion frequency has merit.

The application of f_{SC} as a spectral performance metric must be made in the proper context. Recall that the spanning cycle is based on synthesizing a static voltage in **H**. Voltages of practical interest generally progress along circular trajectories in **H** at frequencies far below that of most spanning cycles. Since the commanded voltage differs slightly from the beginning of one spanning cycles to the next, temporally adjacent spanning cycles are typically different. The adjacent cycles may be of the same class, say $\{\chi_{i,0}, \chi_{i+,0}\}$, but will have different effective occupancy times in at least one of the constituent states. The transition between two spanning cycles constitutes modulation that in general produces spectral power at frequencies below f_{SC}.

However, if f_{SC} is much larger than the frequency of the synthesized waveform voltage, the spectral power density below f_{SC} can likely be ignored. Voltages near the radial boundaries of the Ω_i, $V_{P\gamma} \cong 0$ or $V_{P\gamma} \cong 1$, are not good candidates for the f_{SC} metric because the control systems will typically synthesize these voltages using primitive cycle ensembles, discussed in the next section, consisting of primitive cycles from the two adjacent Ω_i nearest the commanded voltage.

The interpretation of the spanning cycle frequency metric requires further clarification. The metric is proposed for use on a point-by-point basis in regions of **H** where f_{SC} is much larger than the synthesized voltage frequency. This approach seems appropriate for comparing two topologies for which the commanded synthesized voltages progress along the same trajectories in **H**. Put another way, the idea is to compare the values of f_{SC} for two different topologies, **A** and **B,** over small segments of the synthesized voltage trajectory. If f_{SC} for **A** is consistently greater than or equal to that of **B** for a given synthesized voltage, the premise is that **A** has superior low frequency distortion performance in terms of the frequency gap between the synthesized voltage and the distortion spectra.

An extension of the preceding premise is that distortion spectra of spanning cycles scale upward as the spanning cycle frequency increases. This is at best a rough approximation intended only as a rule-of-thumb. However, it has some analytical basis. The number and sequence of state visits are similar for all spanning cycles. The trajectory of $\mathbf{V}(t)$ is similar between state transitions, owing to the resonant circuitry used to implement soft switching. The RMS distortion voltage is essentially the same for all topologies and spanning cycles given that the peak link voltage and transition trajectory shapes are similar. In summary, the spanning cycle frequency metric is of potential value but it is after all, only a metric, lacking axiomatic stature.

3.8 Cycle Ensembles

3.8.1 Voltage Resolution

The mean three-phase voltage $\mathbf{V}_\mu$ for a given spanning cycle depends on the behavior of $V_{Link}(t)$, $\alpha_i(t)$, and $\alpha_{i+}(t)$ during the cycle. Synchronized topologies such as the SPRDL inverter can theoretically control $\mathbf{V}(t)$ so that $\mathbf{V}_\mu$ exactly equals a target voltage, $\mathbf{V}_P$, at the end of a single spanning cycle. Unsynchronized topologies, such as the UPRDL, lack the necessary control over $\mathbf{V}(t)$ to precisely synthesize an arbitrary voltage $\mathbf{V}_P$ in a single spanning cycle. Using an ensemble of primitive cycles in lieu of a single minimal spanning cycle is usually necessary to achieve adequate voltage resolution.

Consider an ideal UPRDL inverter with resonant link period T_{Link}. The corresponding link voltage satisfies:

$$V_{Link}(t + (n + 1)T_{Link}) = V_{Link}(t + nT_{Link}) \text{ for all } t \text{ and all } n \in Z_+ \qquad 3.8.1.1$$

Since the link voltage collapses with period T_{Link}, all primitive cycle periods are integral multiples of T_{Link}. Under the definition of a primitive cycle, occupancy in an active state is limited to one link voltage cycle per UPRDL primitive cycle. The synthesized voltage for a given primitive cycle depends on the profile of $V_{Link}(t)$ over the link cycle and the number of cycles spent in S_0. Consequently, the synthesized voltages of UPRDL primitive cycles are discrete. Since spanning cycles are composed entirely of primitive cycles, it follows that the synthesized voltages of all UPRDL minimal spanning cycles are also discrete and that $\mathbf{V}_\mu$ lies along $V_{P\gamma} = ½$. The net effect is that unsynchronized topologies can not synthesize an arbitrary voltage in $\mathbf{H}$ using a single spanning cycle. Clearly, an ensemble of primitive cycles is needed to provide higher resolution, particularly in terms of $V_{P\gamma}$.

Theoretically, the magnitude of the voltage error converges to zero uniformly in **H** as the synthesis time approaches infinity. However, practical constraints limit the synthesis cycle time to a small fraction of the synthesized three-phase output waveform period. Unfortunately, only a finite number of voltages in **H** can be precisely synthesized using a finite ensemble of finite duration primitive cycles. Consequently, a small error voltage exists for most synthesized static voltages. The error voltage $\mathbf{V}_{Error}$ for an ensemble of $M \in Z_+$ primitive cycles of duration T_k and mean voltage $\mathbf{V}_{\mu k}$, $k \in [1,M]$ is given by,

$$\mathbf{V}_{Error} = \frac{\sum_{k=1}^{N} T_k \mathbf{V}_{\mu k}}{\sum_{k=1}^{N} T_k} - \mathbf{V}_P \qquad 3.8.1.2$$

For typical synthesized three-phase voltage waveforms, the change in the target $\mathbf{V}_P$ over a complete synthesis cycle is comparable to the ensemble error voltage magnitude $|\mathbf{V}_{Error}|$. This tends to obscure the finite precision effects resulting from integral pulse modulation.

3.8.2 Distortion Reduction

Although synchronized topologies generally do not require cycle ensembles to accurately synthesize an arbitrary voltage, the use of an ensemble can improve waveform quality in certain circumstances. Voltages near the edges of a given Ω_i constitute significant disparity in σ_i, σ_{i+}, and σ_0. In cases where two of the σ for a given $\mathbf{V}_P$ are considerably larger than the third, replacing a single spanning cycle with an ensemble consisting of a shorter duration spanning cycle and one or more two-state primitive cycles can reduce load current distortion.

To illustrate the potential advantage of cycle ensembles, consider a SPRDL inverter synthesizing a static voltage $\mathbf{V}_P$ with $\sigma_i = 0.5$, $\sigma_{i+} = 0.05$, and $\sigma_0 = 0.45$ using a single spanning cycle of period T_{SC}. Further assume that steady state conditions exist so that the target load

current $\mathbf{i}_P$ is also static. The resulting current error, $\mathbf{i}_{Error}(t) = \mathbf{i}(t) - \mathbf{i}_P$, has period T_{SC} and without loss of generality can be made to satisfy $\mathbf{i}_{Error}(nT_{SC}) = \mathbf{0}$ for all $n \in Z_+$. Recalling that the only spanning cycle available to SPRDL topologies is $\{\chi_{i,0}, \chi_{i+,0}\}$, the state sequence is of the form $\{S_0, S_{i+}, S_0, S_i, S_0, S_{i+}, \ldots\}$. Suppose the spanning cycle begins at $t = nT_{SC}$ with the onset of the S_0 to S_{i+} transition in the $\chi_{i+,0}$ primitive cycle. Since $\sigma_{i+} << \sigma_i$ and $\sigma_{i+} << \sigma_0$, only the minimum amount of time will be spent in S_{i+}. Following the transition from S_{i+} back to S_0, the time at which the $\chi_{i+,0}$ cycle ends is arbitrary up until the initiation of the transition from S_0 to S_i which is, by definition, part of the $\chi_{i,0}$ primitive cycle. Let the $\chi_{i+,0}$ primitive cycle end with the return to S_0 from S_{i+} and let the corresponding period of the $\chi_{i+,0}$ primitive cycle be $T_{PC\ i+,0}$. The remainder of the spanning cycle is spent in a single $\chi_{i,0}$ primitive cycle of period $T_{PC\ i,0} = T_{SC} - T_{PC\ i+,0}$.

For inductive loads, the instantaneous load current error for static voltage and current synthesis is approximately,

$$\mathbf{i}_{Error}(t) \cong \frac{1}{L_{eff}} \int_0^t \left(\mathbf{V}(\tau) - \mathbf{V}_P\right) d\tau \qquad 3.8.2.1$$

where the current error is given in **u-v** coordinates and is assumed to be zero at $t = 0$. L_{eff} is the effective load inductance along both the **u** and **v** axis. Without loss of generality, suppose $\mathbf{V}_P \in \Omega_{100}$. The error current expressed in terms of **u-v** coordinates and the effective state occupancies in Ω_{100} is approximately given by,

$$i_{u_{Error}}(t) \cong \frac{1}{L_{Eff}} \int_0^t \left(\tfrac{2}{3} V_{Lp}\left(\eta_{100}(\tau) + \tfrac{1}{2}\eta_{110}(\tau)\right) - V_{P_u}\right) d\tau \quad t \geq 0 \qquad 3.8.2.2$$

$$i_{v_{Error}}(t) \cong \frac{1}{L_{Eff}} \int_0^t \left(\tfrac{1}{\sqrt{3}} V_{Lp}\eta_{110}(\tau) - V_{P_v}\right) d\tau \quad t \geq 0 \qquad 3.8.2.3$$

Inspection of 3.8.2.3 shows that $\mathbf{i}_{VError}(t)$ is independent of occupancy in state S_{100} and is therefore influenced only by the $\chi_{110,0}$ primitive cycle in the $\{\chi_{100,0}, \chi_{110,0}\}$ spanning cycle. Given the $\mathbf{V}_P$ selected for this example, the period for which $\eta_{110}(t) > 0$ is assumed to be T_{C110}, the minimum possible value within the constraints of the inverter. Consequently, nothing can be done in the remainder of the spanning cycle to reduce $|\mathbf{i}_{VError}(t)|$. Also recognize that if the duration of the $\chi_{100,0}$ primitive cycle were changed, $\mathbf{i}_{VError}(nT_{SC})$ would not necessarily be zero for all $n \in Z_+$, violating the steady-state assumption.

For the given $\mathbf{V}_P$, the behavior of $\eta_{110}(t)$ in the $\chi_{110,0}$ primitive cycle is strictly topology dependent, given the definition of the beginning and ending times for the $\chi_{110,0}$ cycle. However, the nature of $\eta_{100}(t)$ in the $\chi_{100,0}$ primitive cycle is somewhat arbitrary with regard to the S_0 to S_{100} transition time. The S_0 to S_{100} transition must only occur sufficiently soon after the cycle begins so that there is time for the state to return to S_0 by the end of the spanning cycle. Steady-state conditions demand that the $\chi_{100,0}$ primitive cycle period and mean voltage remain constant. For illustrative purposes, suppose the controller initiates the S_0 to S_{100} transition in the $\chi_{100,0}$ primitive cycle for the smallest time $t_1 > 0$ such that $i_{uError}(nT_{SC} + T_{PC\ 110,0} + t_1) = 0$. Up to this point in the spanning cycle, both the **u** and **v** components of the current error are minimized subject to the physical constraints of the topology for every $t \in [nT_{SC} + T_{PC\ 110,0} + t_1]$, $n \in Z_+$. Given the example $\mathbf{V}_P$ ($\sigma_{100} = 0.5$, $\sigma_{110} = 0.05$), the respective primitive cycle periods satisfy,

$$T_{PC\ 110,0} + t_1 << T_{PC\ 100,0} - t_1 \qquad 3.8.2.4$$

If a single spanning cycle is used to synthesize $\mathbf{V}_P$, the integrand of 3.8.2.2 will change signs at most twice in the interval $[nT_{SC} + T_{PC\ 110,0} + t_1, (n+1)T_{SC}]$, depending on the state at $t = nT_{SC} + T_{PC\ 110,0} + t_1$. The values of $\alpha_{100}(t)$ and $\alpha_0(t)$ will be unity continuously over periods equal to several

times $T_{110,0}$ during the interval $[nT_{SC} + T_{PC\,110,0} + t_1, (n + 1)T_{SC}]$. Referring to 3.8.2.2, this could result in a substantial **u** component current error during certain segments of the interval.

Now suppose the single $\chi_{100,0}$ primitive cycle of period $T_{PC\,100,0}$ and mean voltage $\frac{2}{3}V_{Lp}\sigma_{100}\hat{\psi}_{100}$ is replaced by M $\chi_{100,0}$ primitive cycles, $M \in Z_+$, with combined period $T_{PC\,100,0}$ and time weighted mean voltage $\frac{2}{3}V_{Lp}\sigma_{100}\hat{\psi}_{100}$. Also suppose that $\mathbf{V}(t)$ remains the same for $t \in [nT_{SC} + T_{PC\,110,0}, nT_{SC} + T_{PC\,110,0} + t_1]$. Since $i_{uError}(nT_{SC} + T_{PC\,110,0} + t_1) = 0$, $i_{uError}((n+1)T_{SC}) = 0$ and the maximum amplitude of $V_u(t)$ is the same for both cases, it follows that the increased number of sign changes in the integrand of 3.8.2.2 resulting from the use of more than one $\chi_{100,0}$ cycle reduces the magnitude of $i_{uError}(t)$ for $t \in [nT_{SC} + T_{PC\,110,0} + t_1, (n+1)T_{SC}]$. In general, properly replacing a long duration two-state primitive cycle with two or more shorter duration versions of the same two-state primitive cycle can reduce load current distortion. This is not surprising since it effectively increases the inverter switching frequency, a long accepted method for reducing load current distortion.

The preceding example qualitatively illustrates the potential advantage of an ensemble over a single spanning cycle for a specific topology. The use of ensembles is applicable to all bridge based topologies. For topologies that support the $\{\chi_{i,0,i+}\}$ spanning cycle, a similar argument exists for inserting one or more two-state primitive cycles between the two highest occupancy states. Although many other examples exist, a general rule-of-thumb is that if one or more two-state primitive cycles can be inserted between the two highest occupancy states in a minimal spanning cycle sequence without increasing the total synthesis cycle period or producing a significantly different $\mathbf{V}_\mu$, waveform fidelity can be improved using a cycle ensemble.

3.9 SPRDL State Occupancy and Spanning Cycle Frequency Analysis

3.9.1 Section Objectives

This section employs the concepts and definitions introduced in the previous sections to identify the voltage stress and synthesis cycle period or frequency of a SPRDL inverter. The analysis is restricted to the case of static voltage synthesis using a single spanning cycle for voltages in the interior of a given Ω_i and a single primitive cycle for voltages lying on the common boundary of some Ω_i and Ω_{i+}. Computing the device voltage stress and spanning cycle period associated with each voltage in **H** provides an analytical basis for comparison with other topologies. Although cycle ensembles are not explicitly considered in the analysis, the results apply directly to the spanning cycles and primitive cycles embedded in every ensemble.

3.9.2 SPRDL Spanning Cycle Frequency and Voltage Stress

Consider a SPRDL inverter synthesizing a static three-phase voltage $\mathbf{V_P} = (V_{Ph}, V_{P\gamma}, i) \in \Omega_i$ for some $i \in \mathbf{S}^{*-}$. To simplify the analysis without serious loss of accuracy, sinusoidal link voltage collapse characteristics are assumed. Furthermore, it is assumed that parameters such as β_i, and λ_i are the same for all states. The symmetry of each Ω_i about $V_{P\gamma} = ½$ allows consideration of only the case where $V_{P\gamma} \in [0, ½]$. Since the case of $V_{P\gamma} = 0$ is achievable using only the primitive cycle $\chi_{i,0}$ and all the $\mathbf{V_P}$ for $V_{P\gamma} \in (0, ½]$ require the spanning cycle $\{\chi_{i,0}, \chi_{i+,0}\}$, it is necessary to treat the two cases separately.

Figure 16 shows active state occupancy and effective state occupancy plots for the most general case of the $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle in which the inverter spends at least one full minimum link cycle in the zero state. A second but equally valid case exists where the spanning cycle briefly passes through S_0 on the round trip between S_i and S_{i+}. For clarity, the former case is

denoted with the subscript S_0 to indicate that the inverter occupies S_0 for at least one full link cycle. In all cases considered, the amount of time spent in the least occupied state is minimized in order to minimize the spanning cycle period.

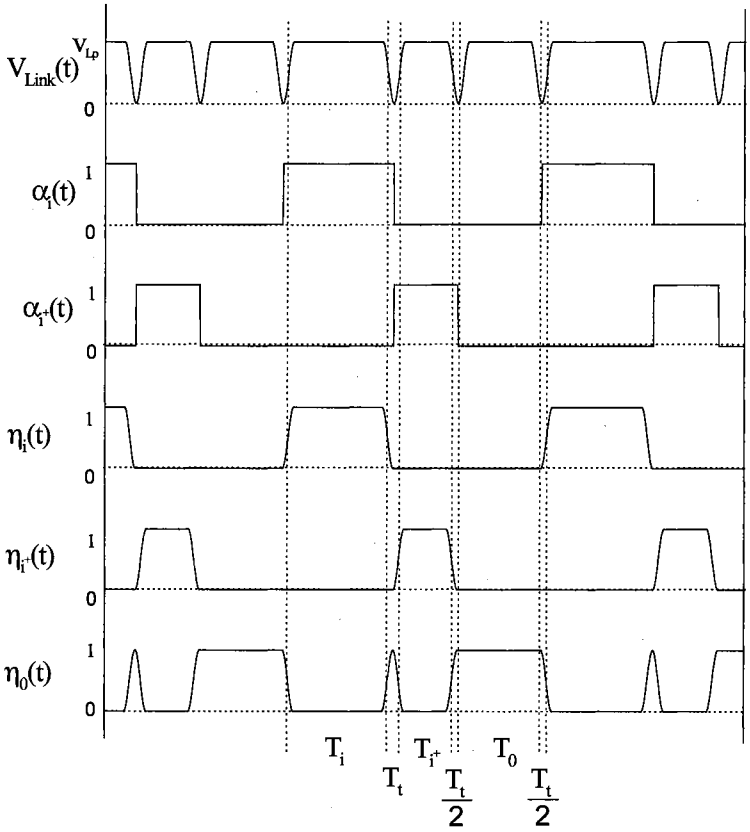


Figure 16. Representative link voltage, active state occupancy, and effective state occupancy plots for a SPRDL inverter $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle with the zero state fully occupied for at least one minimum link cycle period

First consider the case of $\{\chi_{i,0}, \chi_{i+,0}\}_{So}$ in which the time spent in S_0 is controllable.

Since only values of $\mathbf{V}_P$ with $0 < V_{P\gamma} \leq ½$ are being considered,

$$\min(T_i, T_{i+}) = T_{i+}$$

Hence,

$$\beta = \frac{T_{i^+}}{T_P}$$

From inspection of Figure 16, the spanning cycle period T_{SC} and mean effective active state occupancy σ_A are,

$$T_{SC} = T_i + T_{i+} + 2T_t + T_0 \qquad 3.9.2.1$$

$$\sigma_A = \frac{T_i + T_{i+}}{T_i + T_{i+} + 2T_t + T_0} \qquad 3.9.2.2$$

where T_i and T_{i+} are $\geq T_p$ and $T_0 \geq T_p + T_t$.

Using 3.6.7 along with the definitions of λ and β in 3.9.2.1 and 3.9.2.2 yields,

$$T_{SC} = \frac{\lambda\beta T_t}{V_{P\gamma}} + 2T_t + T_0 \qquad 3.9.2.3$$

$$\sigma_A = \frac{\frac{\lambda\beta T_t}{V_{P\gamma}}}{\frac{\lambda\beta T_t}{V_{P\gamma}} + 2T_t + T_0} \qquad 3.9.2.4$$

Which reduces to,

$$\sigma_A = \frac{1}{1 + \frac{V_{P\gamma}}{\lambda\beta}\left(2 + \frac{T_0}{T_t}\right)} \quad \beta \geq 1,\ T_0 \geq T_P + T_t \qquad 3.9.2.5$$

Combining 3.9.2.3 and 3.9.2.4, the spanning cycle period becomes,

$$T_{SC} = \frac{\lambda\beta T_t}{\sigma_A V_{P\gamma}} \qquad 3.9.2.6$$

The fundamental spanning cycle frequency f_{SC} is then,

$$f_{SC} = \frac{\sigma_A V_{P\gamma} f_t}{\lambda\beta} \qquad 3.9.2.7$$

Where $f_t = \frac{1}{T_t}$ and β is a function of σ_A and $V_{P\gamma}$.

For a given σ_A and $V_{P\gamma}$, T_0 and β are found using 3.9.2.5 and selecting the solution that maximizes the spanning cycle frequency. Examining 3.9.2.7 indicates that the later condition is satisfied by minimizing β for a given σ_A and $V_{P\gamma}$. Solving 3.9.2.5 for β yields,

$$\beta = \frac{V_{P\gamma}\left(2+\frac{T_0}{T_t}\right)}{\lambda\left(\frac{1}{\sigma_A}-1\right)} \qquad 3.9.2.8$$

Since $\beta \geq 1$, solving in terms of the inequality yields,

$$T_0 \geq \left(\frac{\lambda(1-\sigma_A)}{\sigma_A V_{P\gamma}}-2\right)T_t$$

But T_0 must also satisfy the constraint,

$$T_0 \geq T_P + T_t$$

Which can be written as,

$$T_0 \geq (1+\lambda)T_t$$

Hence,

$$T_0 = T_t \max\left(\frac{\lambda(1-\sigma_A)}{\sigma_A V_{P\gamma}}-2, 1+\lambda\right) \qquad 3.9.2.9$$

The boundary separating the two expressions in the maximum function is easily found by equating the expressions and solving for σ_A in terms of $V_{P\gamma}$. This yields,

$$\sigma_A = \frac{1}{1+V_{P\gamma}\left(1+\frac{3}{\lambda}\right)} \qquad 3.9.2.10$$

Finally, noting that T_0 must $\rightarrow \infty$ as $\sigma_A \rightarrow 0$ yields,

$$T_0 = \begin{cases} (1+\lambda)T_t, & \sigma_A \geq \dfrac{1}{1+V_{P\gamma}\left(1+\dfrac{3}{\lambda}\right)} \\ \left(\dfrac{\lambda(1-\sigma_A)}{\sigma_A V_{P\gamma}} - 2\right)T_t, & \sigma_A < \dfrac{1}{1+V_{P\gamma}\left(1+\dfrac{3}{\lambda}\right)} \end{cases} \qquad 3.9.2.11$$

Next, using 3.9.2.11 in 3.9.2.8 produces,

$$\beta = \begin{cases} \dfrac{\sigma_A V_{P\gamma}\left(1+\dfrac{3}{\lambda}\right)}{1-\sigma_A}, & \sigma_A \geq \dfrac{1}{1+V_{P\gamma}\left(1+\dfrac{3}{\lambda}\right)} \\ 1, & \sigma_A < \dfrac{1}{1+V_{P\gamma}\left(1+\dfrac{3}{\lambda}\right)} \end{cases} \qquad 3.9.2.12$$

Finally, using 3.9.2.12 in 3.9.2.7 gives the spanning cycle frequency for all $V_{P\gamma} \in (0,1/2]$ and $\sigma_A \in (0, 1)$.

$$f_{SC} = \begin{cases} \dfrac{1-\sigma_A}{3+\lambda} f_t, & \sigma_A \geq \dfrac{1}{1+V_{P\gamma}\left(1+\dfrac{3}{\lambda}\right)} \\ \dfrac{\sigma_A V_{P\gamma}}{\lambda} f_t, & \sigma_A < \dfrac{1}{1+V_{P\gamma}\left(1+\dfrac{3}{\lambda}\right)} \end{cases} \qquad 3.9.2.13$$

Now consider the second case in which the spanning cycle only briefly occupies S_0. Visually removing the T_0 interval in Figure 16 produces the following expressions for the spanning cycle period and effective active state occupancy.

$$T_{SC} = T_i + T_{i+} + 2T_t \qquad 3.9.2.14$$

$$\sigma_A = \frac{T_i + T_{i+}}{T_i + T_{i+} + 2T_t} \qquad 3.9.2.15$$

Writing both expressions in terms of λ, β, and γ yields,

$$T_{SC} = \frac{\lambda\beta T_t}{V_{P\gamma}} + 2T_t \qquad 3.9.2.16$$

$$\sigma_A = \frac{\frac{\lambda\beta T_t}{V_{P\gamma}}}{\frac{\lambda\beta T_t}{V_{P\gamma}} + 2T_t} \qquad 3.9.2.17$$

Which simplifies to,

$$\sigma_A = \frac{1}{1 + \frac{2V_{P\gamma}}{\lambda\beta}} \beta \geq 1 \qquad 3.9.2.18$$

Using 3.9.2.17 in 3.9.2.16 results in,

$$T_{SC} = \frac{\lambda\beta T_t}{\sigma_A V_{P\gamma}} \qquad 3.9.2.19$$

Letting $f_t = \frac{1}{T_t}$ as before, the spanning cycle frequency again becomes,

$$f_{SC} = \frac{\sigma_A V_{P\gamma}}{\lambda\beta} f_t \qquad 3.9.2.20$$

where β is again a function of σ_A and $V_{P\gamma}$.

Solving 3.9.2.18 for β yields,

$$\beta = \frac{2\sigma_A V_{P\gamma}}{\lambda(1 - \sigma_A)} \qquad 3.9.2.21$$

Applying the inequality $\beta \geq 1$ and solving for σ_A in terms of $V_{P\gamma}$ produces,

$$\sigma_A \geq \frac{1}{1+\frac{2V_{P\gamma}}{\lambda}}, \quad V_{P\gamma} \in \left(0, \tfrac{1}{2}\right] \qquad 3.9.2.22$$

Substituting 3.9.2.21 into 3.9.2.20 and applying the constraint of 3.9.2.22 yields,

$$f_{SC} = \frac{(1-\sigma_A)}{2} f_t, \quad \sigma_A \geq \frac{1}{1+\frac{2V_{P\gamma}}{\lambda}}, \; V_{P\gamma} \in \left(0, \tfrac{1}{2}\right] \qquad 3.9.2.23$$

Equations 3.9.2.13 and 3.9.2.23 reveal the three distinct spanning cycle regimes. Figure 17 shows σ_A as a function of $V_{P\gamma}$ for various values of β in the three regimes. The dashed line marks the boundary between the two versions of $\{\chi_{i,0}, \chi_{i+,0}\}$. The droop in σ_A as $V_{P\gamma} \rightarrow ½$ is the result of passing through S_0 each time the spanning cycle switches between states S_i and S_{i+}. The solid line denotes the $\{\chi_{i,0}, \chi_{i+,0}\}_{So}$ solution with minimal time, $(1 + \lambda)T_t$, continuously spent in S_0 and minimal β. Values of σ_A below the line correspond to increased time spent in S_0. Functionally, this is achieved by allowing the link to remain high longer than the minimal link cycle time, $(1 + \lambda)T_t$, while the inverter is in S_0. Since the occupancy in S_{i+} remains the minimum of the three state occupancies, $\beta = 1$. For voltages above the solid line, the $\{\chi_{i,0}, \chi_{i+,0}\}_{So}$ version of the spanning cycle spends the minimum time, $(1 + \lambda)T_t$, in S_0 but must spend more time in the active states to increase σ_A. Spending more time in the active states requires increasing β, and thus T_{SC}, in order to hold $V_{P\gamma}$ constant. The dashed line marks the lowest possible value of σ_A achievable without spending at least one full link cycle period in S_0. Comparison of 3.9.2.13 and 3.9.2.23 show that f_{SC} is lower when a full link cycle is spent in S_0, as expected. Hence, $\{\chi_{i,0}, \chi_{i+,0}\}_{So}$ should only be used for values of σ_A below the dashed line.

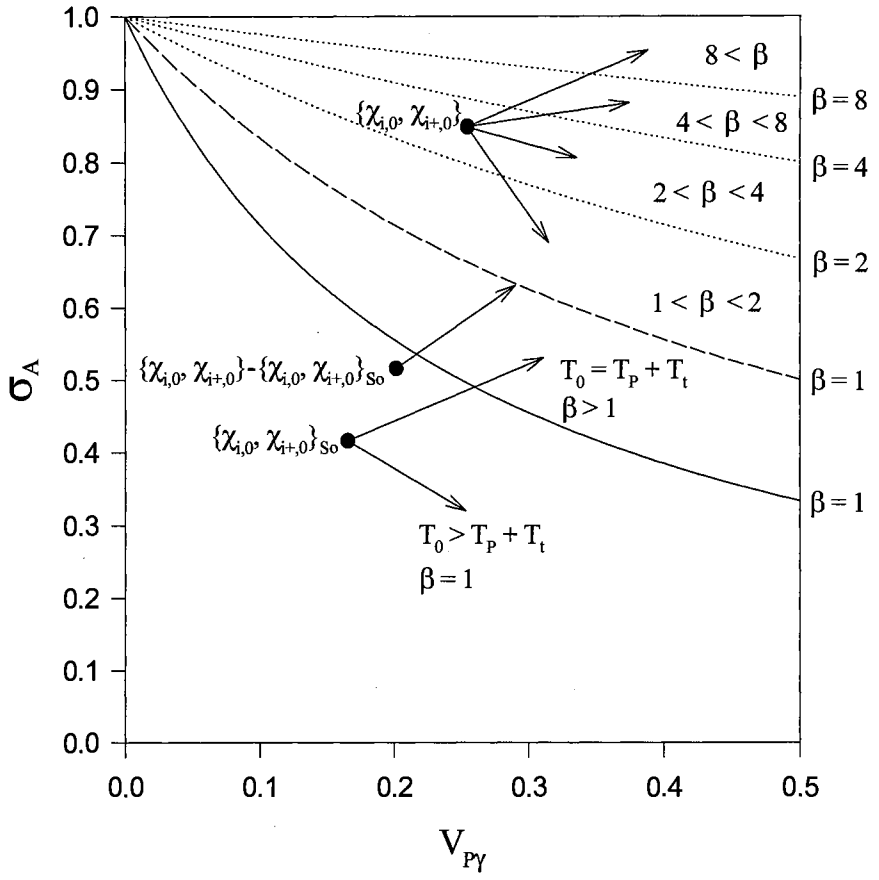


Figure 17. Plot of σ_A versus $V_{P\gamma}$ ($\lambda = 1$) showing the three spanning cycle regimes formed by $\{\chi_{i,0}, \chi_{i+,0}\}$ when at least one link cycle is spent in S_0 and when only the minimal time is spent in S_0

The spanning cycle frequency corresponding to the optimal spanning cycle regimes is given in 3.9.2.24. To reach values of σ_A above the dashed line, β must still be increased as before in order to counter the effects of passing through S_0.

$$f_{SC} = \begin{cases} \dfrac{1-\sigma_A}{2} f_t, & \sigma_A \geq \dfrac{1}{1+\dfrac{2V_{P\gamma}}{\lambda}} \\ \dfrac{1-\sigma_A}{3+\lambda} f_t, & \dfrac{1}{1+V_{P\gamma}\left(1+\dfrac{3}{\lambda}\right)} \leq \sigma_A < \dfrac{1}{1+\dfrac{2V_{P\gamma}}{\lambda}}, \quad V_{P\gamma} \in (0, \tfrac{1}{2}] \\ \dfrac{\sigma_A V_{P\gamma}}{\lambda} f_t, & \sigma_A < \dfrac{1}{1+V_{P\gamma}\left(1+\dfrac{3}{\lambda}\right)} \end{cases} \qquad 3.9.2.24$$

In order to synthesize voltages above the $\{\chi_{i,0}, \chi_{i+,0}\}$ - $\{\chi_{i,0}, \chi_{i+,0}\}_{So}$ boundary, either β must be raised above unity or V_{Lp} must be increased. Since the spanning cycle frequency is roughly inversely proportional to β for $\beta > 1$, significant spanning cycle frequency reduction results for σ_A above about 0.7 and $V_{P\gamma}$ greater than roughly 0.2 if β alone is raised. Increasing V_{Lp} would also increase the power matrix voltage stress. Consequently, SPRDL topologies can not simultaneously deliver their full spectral performance potential and maintain minimal voltage stress levels.

Figure 18 shows a three-dimensional plot of the spanning cycle frequency f_{SC} in the Ω_{100} sector of **H**. The abrupt jump near the center of the plot corresponds to the $\{\chi_{i,0}, \chi_{i+,0}\}$ - $\{\chi_{i,0}, \chi_{i+,0}\}_{So}$ boundary. For voltages above the boundary, the spanning cycle only passes though S_0 while for voltage below the boundary the spanning cycle spends at least one full link cycle in S_0.

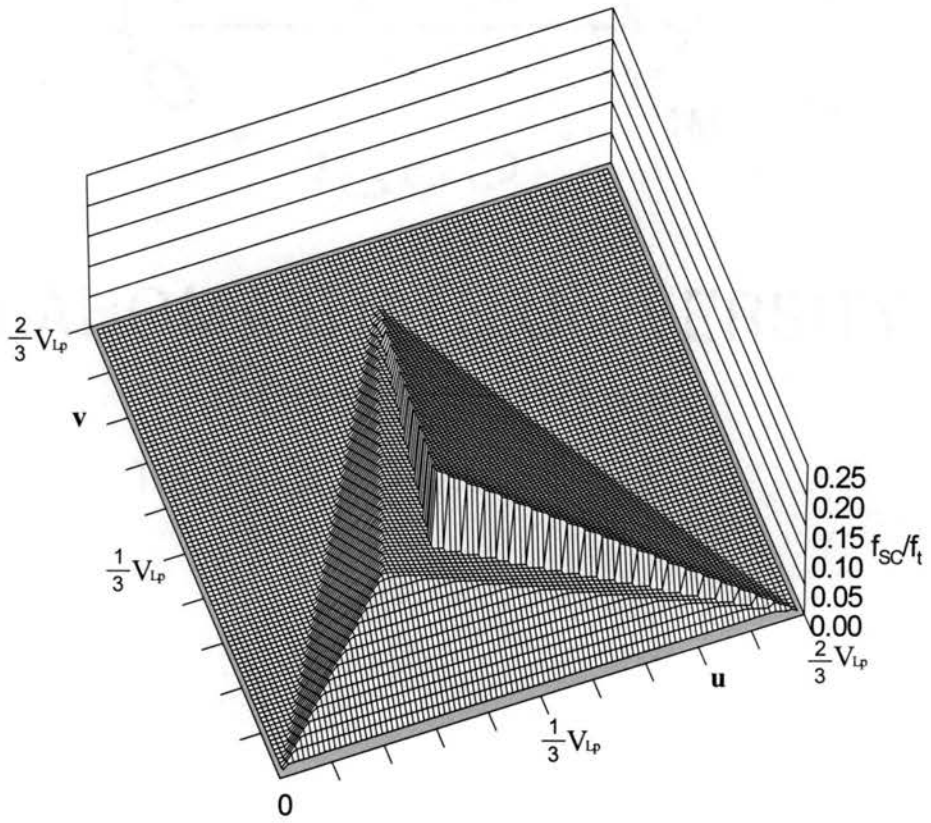


Figure 18. $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle frequency in the Ω_{100} sector of **H** for an SPRDL inverter

3.9.3 SPRDL Primitive Cycle Frequency

The use of cycle ensembles to replace single spanning cycles in certain circumstances warrants determining the relationship between the primitive cycle frequency and σ_A. For SPRDL topologies, only the $\chi_{i,0}$ primitive cycle need be considered. Three distinct cases exist for $\chi_{i,0}$. In the first case, the cycle passes through S_0 in minimal time and σ_A is controlled by the amount of time the power matrix is held in state S_i, $i \in \mathbf{S}^{*-}$. In the second case, the power matrix spends one minimum link cycle in S_0 and σ_A is again controlled by the amount of time the power matrix is held in S_i, $i \in \mathbf{S}^{*-}$. In the third case, the cycle passes through S_i, $i \in \mathbf{S}^{*-}$, in minimal time and σ_A is controlled by the amount of time the power matrix is held in S_0 beyond the minimal link cycle period.

Consider the first case in which the power matrix only passed through S_0. Examining Figure 16 and ignoring the segments involving S_{i+} shows the primitive cycle period to be,

$$T_{PC} = T_i + T_t \qquad 3.9.3.1$$

where $T_i \geq T_p$.

The mean effective active state occupancy is,

$$\sigma_A = \frac{T_i}{T_i + T_t} \qquad 3.9.3.2$$

Using the inequality $T_i \geq T_p$ in 3.9.3.2 places the following bound on σ_A,

$$\sigma_A \geq \frac{\lambda}{1+\lambda}$$

Solving 3.9.3.2 for T_i yields,

$$T_i = \frac{\sigma_A T_t}{1-\sigma_A}, \quad \sigma_A \geq \frac{\lambda}{1+\lambda} \qquad 3.9.3.3$$

Substituting 3.9.3.3 into 3.9.3.1 produces,

$$T_{PC} = \frac{T_t}{1-\sigma_A}, \quad \sigma_A \geq \frac{\lambda}{1+\lambda} \qquad 3.9.3.4$$

The primitive cycle frequency f_{PC} is,

$$f_{PC} = (1-\sigma_A) f_t, \quad \sigma_A \geq \frac{\lambda}{1+\lambda} \qquad 3.9.3.5$$

Next, consider the case where one minimum link cycle period is spent in S_0. Again referring to Figure 16 and ignoring the S_{i+} segment of the cycle yields,

$$T_{PC} = T_i + T_t + T_0 \qquad 3.9.3.6$$

Just as in the case of the $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle, $T_0 \geq T_p + T_t$. Using the minimum T_0, 3.9.3.6 becomes,

$$T_{PC} = T_i + (2+\lambda)T_t \qquad 3.9.3.7$$

The corresponding σ_A is given by,

$$\sigma_A = \frac{T_i}{T_i + (2+\lambda)T_t} \qquad 3.9.3.8$$

Since $T_i \geq T_p$,

$$\sigma_A \geq \frac{\lambda}{2(1+\lambda)} \qquad 3.9.3.9$$

Solving 3.9.3.8 for T_i yields,

$$T_i = \frac{\sigma_A T_t (2+\lambda)}{1-\sigma_A}, \quad \sigma_A \geq \frac{\lambda}{2(1+\lambda)} \qquad 3.9.3.10$$

Using 3.9.3.10 in 3.9.3.7 yields,

$$T_{PC} = \frac{(2+\lambda)T_t}{1-\sigma_A}, \quad \sigma_A \geq \frac{\lambda}{2(1+\lambda)} \qquad 3.9.3.11$$

The primitive cycle frequency is then,

$$f_{PC} = \frac{(1-\sigma_A)}{2+\lambda} f_t, \quad \sigma_A \geq \frac{\lambda}{2(1+\lambda)} \qquad 3.9.3.12$$

Finally, consider the case where the cycle only passes through S_i, $i \in \mathbf{S}^{*-}$, and fully occupies S_0 for at least the minimum link cycle period. Once more disregarding the S_{i+} segments of Figure 16, the corresponding primitive cycle period is,

$$T_{PC} = T_p + T_t + T_0 \qquad 3.9.3.13$$

The expression for σ_A becomes,

$$\sigma_A = \frac{\lambda T_t}{(1+\lambda)T_t + T_0} \qquad 3.9.3.14$$

Since $T_0 \geq (1+\lambda)T_t$,

$$\sigma_A \leq \frac{\lambda}{2(1+\lambda)} \qquad 3.9.3.15$$

Solving 3.9.3.14 for T_0 yields,

$$T_0 = T_t\left(\frac{\lambda}{\sigma_A} - (1+\lambda)\right), \quad \sigma_A \leq \frac{\lambda}{2(1+\lambda)} \qquad 3.9.3.16$$

Substituting 3.9.3.16 into 3.9.3.13 yields,

$$T_{PC} = \frac{\lambda T_t}{\sigma_A}, \quad \sigma_A \leq \frac{\lambda}{2(1+\lambda)} \qquad 3.9.3.17$$

The corresponding primitive cycle frequency is,

$$f_{PC} = \frac{\sigma_A f_t}{\lambda}, \quad \sigma_A \le \frac{\lambda}{2(1+\lambda)} \qquad 3.9.3.18$$

As in the $\{\chi_{i,0}, \chi_{i+0}\}$ spanning cycle case, the highest frequency solution is used whenever σ_A lies in more than one cycle regime. Consequently, the $\chi_{i,0}$ primitive cycle frequency is given by,

$$f_{PC} = \begin{cases} (1-\sigma_A) f_t & \sigma_A \ge \dfrac{\lambda}{1+\lambda} \\ \dfrac{(1-\sigma_A) f_t}{2+\lambda} & \dfrac{\lambda}{2(1+\lambda)} \le \sigma_A < \dfrac{\lambda}{1+\lambda} \\ \dfrac{\sigma_A f_t}{\lambda} & 0 < \sigma_A < \dfrac{\lambda}{2(1+\lambda)} \end{cases} \qquad 3.9.3.19$$

Figure 19 graphically illustrates the primitive cycle frequency as a function of σ_A. As in Figure 18, the three cycle regimes are clearly visible.

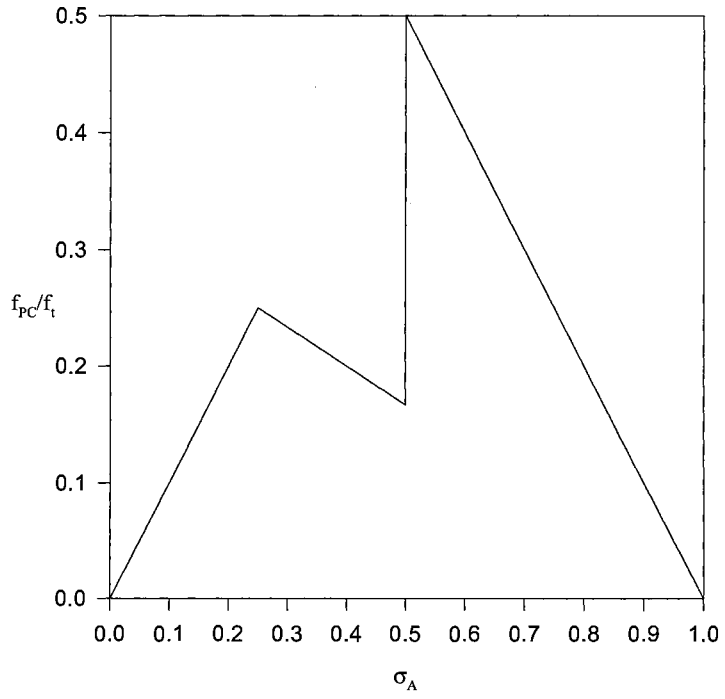


Figure 19. Primitive cycle frequency f_{PC} versus mean effective active state occupancy σ_A for the $\chi_{i,0}$ primitive cycle of a SPRDL inverter with $\lambda = 1$

3.10 Summary

The concepts and definitions introduced in this chapter provide the tools necessary for a structured description and comparison of alternative bridge based inverter topologies in terms of voltage space characteristics. It was seen that certain topologies, such as SPRDL, are not capable of using all of the primitive cycles available to the conventional bridge inverter. The chapter concluded with an example illustrating the analytical application of the definitions to the SPRDL topology. This revealed the relationship between the spanning cycle frequency and the inverter output voltage for a given power matrix voltage stress level, V_{Lp}.

CHAPTER IV

GUIDELINES FOR DEVELOPING SOFT-SWITCHED VOLTAGE-SOURCE BRIDGE TOPOLOGIES

4.1 Introduction

The purpose of this chapter is to establish guidelines for developing a soft-switched voltage-source bridge inverter that is superior to resonant link topologies in terms of both power matrix voltage stress and spanning cycle frequency. The techniques presented in the literature to reduce the voltage stress levels in UPRDL and SPRDL inverters are based on circuitry modifications that reduce the peak link voltage. The approach employed in this chapter is to identify voltage space characteristics that would permit a hypothetical soft-switched inverter with those characteristics to operate at the same low voltage stress level as a conventional bridge inverter while meeting or exceeding the spanning cycle frequency characteristics of the SPRDL topology. As will be seen, this can be accomplished by augmenting the SPRDL primitive cycle set such that all three states defining a given Ω_i, $i \in \mathbf{S}^{*}$, are represented equally in the corresponding spanning cycle set and the allowed state occupancy times are the same for all states in $\mathbf{S}^{*}$. The chapter closes with a set of circuit synthesis guidelines for soft-switched topologies. These guidelines are derived from a compilation of proposals found in the literature for enhancing resonant link topology performance along with inferences drawn from the preceding spanning cycle analysis.

4.2 A Voltage Space Approach to Developing Soft-Switched Voltage-Source Bridge Inverters with Low Voltage Stress and High Effective Switching Frequency

4.2.1 Primitive Cycle Set Symmetry Considerations

The root cause of the elevated voltage stress levels in resonant link topologies is the innate requirement for the link voltage to collapse prior to the power matrix entering an active state. This results in $\eta_0(t)$ being greater than zero during some portion of each primitive cycle. The only way to achieve full voltage utilization of the power matrix is to make primitive cycles available for which $\eta_0(t)$ remains zero during the entire primitive cycle. Of the four primitive cycles available to bridge inverters, only $\chi_{i,i+}$ satisfies this condition. Since $\chi_{i,i+}$ is forbidden to resonant link topologies, a new topology class is needed that can support $\chi_{i,i+}$ along with the primitive cycles available to resonant link topologies, namely $\chi_{i,0}$ and $\chi_{i+,0}$.

Consider a hypothetical soft-switched voltage-source bridge inverter whose primitive cycle set is that of the resonant link topology augmented with $\chi_{i,i+}$, $i \in S^{*-}$, as given in 4.2.1.1.

$$\Theta_i = \{\chi_{i,0}, \chi_{i+,0}, \chi_{i,i+}\} \quad i \in S^{*-} \qquad 4.2.1.1$$

The resulting primitive cycle set Θ_i in sector Ω_i, $i \in S^{*-}$, is fully symmetric with respect to state-to-state transitions in that direct transitions are allowed between any two of the three power matrix states defining Ω_i. Instead of the single spanning cycle $\{\chi_{i,0}, \chi_{i+,0}\}$ available to resonant link topologies, the augmented primitive cycle set results in the three element spanning cycle set: $\{\{\chi_{i,0}, \chi_{i+,0}\}, \{\chi_{i,0}, \chi_{i,i+}\}, \{\chi_{i+,0}, \chi_{i,i+}\}\}$. Moreover, the symmetry resulting from the augmentation is extended to the spanning cycle set. That is, the allowed spanning cycle set for Ω_i, $i \in S^{*-}$ is symmetric with respect to all three states defining Ω_i in terms of state-to-state transitions. The

resulting symmetry in both the primitive cycle and spanning cycle sets is in marked contrast to the asymmetry of resonant link topology spanning cycle sets in which direct active-state to active-state transitions are forbidden.

4.2.2 Spanning Cycle Frequency Considerations

The addition of $\chi_{i,i+}$ to the primitive cycle set of the hypothetical inverter potentially reduces the spanning cycle period for large values of σ_A. This results from reducing the fraction of time required in the active states to offset the effective time spent in S_0 during a $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle. However, further reductions in the spanning cycle period may be possible. Notice that all three spanning cycles formed from the elements of Θ_i, $i \in \mathbf{S}^{*-}$, require four state transitions per cycle. Given that the hypothetical topology is capable of supporting the state transitions necessary to implement Θ_i, $i \in \mathbf{S}^{*-}$, it is not unreasonable to assume that adding $\chi_{i,0,i+}$ to the allowed primitive cycle set could be accomplished without introducing additional infrastructure. The advantage of adding $\chi_{i,0,i+}$ is that in its dual role as a spanning cycle, $\{\chi_{i,0,i+}\}$, it requires only three state transitions to complete. Consequently, inclusion of the $\chi_{i,0,i+}$ primitive cycle has the potential of further decreasing the spanning cycle period in certain regions of **H**.

4.2.3 Symmetrical Allowed State Occupancy Time Considerations

UPRDL inverters either "pass through" a given state or remain in that state for an integer multiple of resonant link periods. This is true for both active and passive states, due to the symmetrical behavior of the resonant link with respect to the upper and lower power matrix rails. In contrast, all SPRDL designs proposed in the literature allow control of the time the link spends at the upper rail potential but not at the lower rail potential. This allows SPRDL inverters to simply pass through a given active state or remain there for any extended period, up to the maximum controllable link period. The allowed state occupancy time is not as flexible for the

zero state, S_0. As with active states, SPRDL inverters can pass through S_0 during an active state to active state transition. However, the smallest allowed state occupancy time, greater than that associated with a simple "pass through," is equal to the minimum link period. This is because once S_0 is selected, the link must cycle from the lower rail to the upper rail and then back to the lower rail before a transition to an active state can be initiated. This behavior constitutes an asymmetry with respect to active and passive states in terms of allowed state occupancy times. The consequence of this asymmetry is evident in the notch seen in the spanning cycle frequency plot shown in Figure 18. The notch is due to the inability of the SPRDL inverter to remain in S_0 for a time less than the minimum link period, except for the case of a simple pass through during active state to active state transitions. Although the notch occupies a relatively small portion of each sector in **H**, its presence degrades the average switching frequency for any commanded output voltage trajectory intersecting the notch. It follows that a link design capable of providing symmetrical state occupancy control to all states is potentially superior to those proposed for the SPRDL to date.

4.2.4 Proposed Voltage Space Characteristics for a New Soft-Switched Voltage-Source Bridge Topology

The preceding subsections described modifications to the voltage space characteristics of the SPRDL topology expected to yield a topology with the same low voltage stress levels as a conventional bridge inverter and potentially increase the effective switching frequency over that of existing SPRDL designs. The first of these enhancements consisted of adding $\chi_{i,i+}$ to the primitive cycle set of resonant link topologies to obtain the primitive cycle set of a new hypothetical topology with a voltage stress level equal to that of a conventional bridge inverter. The second enhancement called for further extending the primitive cycle set to include $\chi_{i,0,i+}$ in order to reduce the average spanning cycle period. The final proposed enhancement argued for

employing a link collapse circuit capable of controlling the time the link spends at both rail potentials rather than only at the upper rail potential so that the same degree of occupancy time control exists for both active and passive states. The following sections present an analytical analysis of the primitive and spanning cycles available to the proposed hypothetical topology.

4.3 Analysis of the Spanning Cycles Proposed for a New Hypothetical Soft-Switched Voltage-Source Bridge Topology

4.3.1 Analysis of the $\{\chi_{i,0}, \chi_{i+,0}\}$ Spanning Cycle Under Symmetrical Allowed State Occupancy Time Conditions

Before examining the voltage stress and spanning cycle frequency characteristics of the $\{\chi_{i,0}, \chi_{i,i+}\}$ and $\{\chi_{i,0,i+}\}$ spanning cycles, the $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle warrants reexamination in the context of symmetrical state occupancy time conditions. To begin, consider the generic $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle state occupancy and effective state occupancy plot shown in Figure 20. The state sequence depicted in the figure is $\{S_i, S_0, S_{i+}, S_0, S_i, S_0, \ldots\}$. The spanning cycle period T_{SC} is composed of four distinct segments, T_i, T_{01}, T_{i+}, and T_{02}. Recall that in the SPRDL analysis presented in Chapter III, T_0 was taken as the controlled time spent in S_0 rather than the effective occupancy time because S_0 was occupied as part of each entry into an active state. Since S_0 is now on an equal footing with the active states, it is both convenient and appropriate to redefine T_0 as the total effective occupancy time in S_0. Let T_0 be redefined as,

$$T_0 = T_{01} + T_{02} \qquad 4.3.1.1$$

Given that S_0 is entered twice in this cycle, there are two effective occupancy times for S_0, T_{01} and T_{02}. If the spectral content of a given spanning cycle were being computed, the individual occupancies times would have to be considered. For voltage stress and spanning cycle frequency

calculations however, only the total effective time spent in each state is relevant. Consequently,

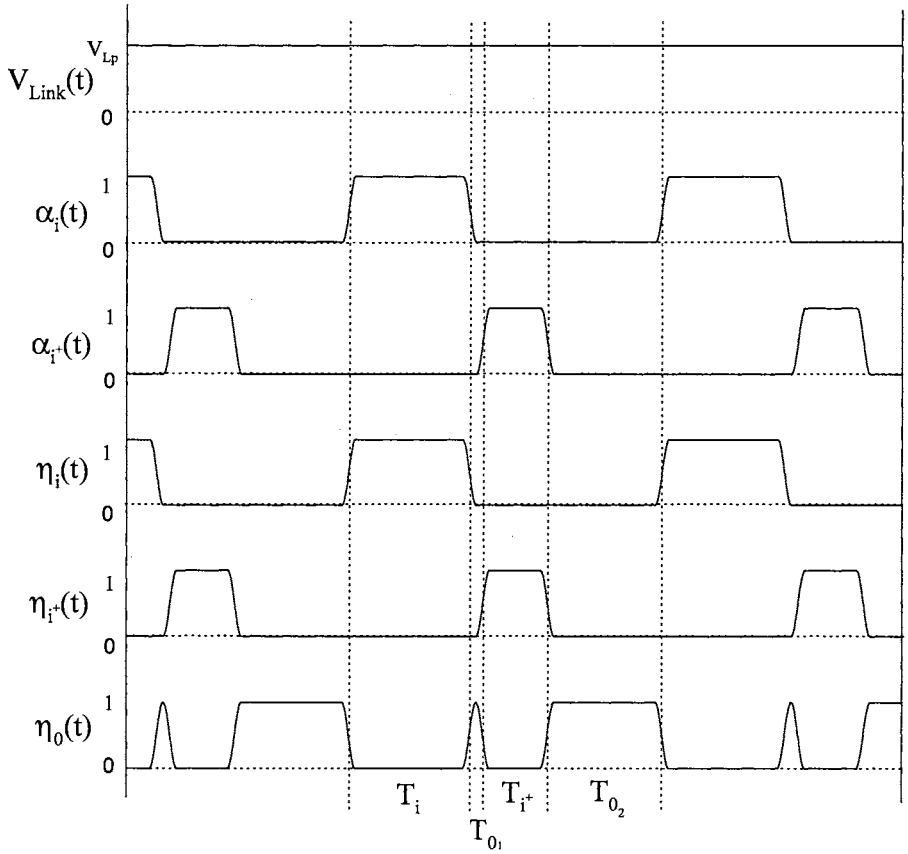


Figure 20. Generic state occupancy and effective state occupancy plots for the $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle of a hypothetical soft-switched inverter with symmetrical state occupancy time characteristics

only the total effective time T_0 spent in S_0 need be considered. Finally, for consistency with the premise that the topology should be symmetric with respect to transitions between any two states, state dependent parameters such as T_{pi} and T_{ci} are assumed to be the same for all $i \in \mathbf{S}^*$.

From Figure 20, the $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle period is,

$$T_{SC} = T_i + T_{i+} + T_0 \qquad 4.3.1.2$$

The restrictions on the terms of 4.3.1.2 are,

$$T_i \geq T_p \qquad 4.3.1.3$$

$$T_{i+} \geq T_p \qquad 4.3.1.4$$

$$T_0 \geq 2T_p \qquad 4.3.1.5$$

The elevated lower bound on T_0 results from the double occupancy of S_0 during the cycle.

For notational convenience, the γ coordinate of a given $\mathbf{V}_P$, $V_{P\gamma}$, is denoted as γ throughout the remainder of the document, except where clarification is required. As in the previous chapter, calculation of f_{SC} for all vectors $\mathbf{V}_P$ in a given sector Ω_i need only be performed for $\gamma \in (0, ½]$, due to the symmetry of f_{SC} about $\gamma = ½$. To begin the analysis, 3.6.7 is applied to 4.3.1.2 and the result normalized with respect to T_t to yield,

$$\frac{T_{SC}}{T_t} = \frac{\beta\lambda}{\gamma} + \frac{T_0}{T_t} \qquad 0 < \gamma \leq ½,\ T_0 \geq 2T_p,\ \beta \geq 1 \qquad 4.3.1.6$$

For $\gamma \in (0, ½]$, $T_i \geq T_{i+}$. Consequently, from 3.6.10,

$$\beta = \frac{T_{i+}}{T_p} \qquad 4.3.1.7$$

From 3.6.8, the effective active state occupancy is,

$$\sigma_A = \frac{T_i + T_{i+}}{T_{SC}} \qquad 4.3.1.8$$

Using 3.6.7 and 4.3.1.6, this can be expressed as,

$$\sigma_A = \frac{\lambda\beta}{\lambda\beta + \gamma\frac{T_0}{T_t}} \qquad 4.3.1.9$$

Solving 4.3.1.9 for T_0/T_t yields,

$$\frac{T_0}{T_t}=\frac{\lambda\beta(1-\sigma_A)}{\sigma_A\gamma} \quad \sigma_A>0,\ 0<\gamma\le ½,\ \beta\ge 1 \qquad 4.3.1.10$$

Applying condition 4.3.1.5 and selecting the smallest possible T_0 in order to minimize T_{SC} yields,

$$\frac{T_0}{T_t}=\max\left(\frac{\lambda\beta(1-\sigma_A)}{\sigma_A\gamma},2\lambda\right) \quad \sigma_A>1,\ 0<\gamma\le ½,\ \beta\ge 1 \qquad 4.3.1.11$$

Unlike the SPRDL, T_0 for the hypothetical inverter has no forbidden values above its minimum value. Hence, there is no need for both β and T_0 to simultaneously exceed their respective minimums. Consequently, there is a single boundary separating the terms of the maximum function in 4.3.1.11. Equation 4.3.1.11 can thus be written as,

$$\frac{T_0}{T_t}=\begin{cases}\dfrac{\lambda(1-\sigma_A)}{\gamma\sigma_A} & \sigma_A\le\dfrac{1}{1+2\gamma}\\[2ex] 2\lambda & \sigma_A>\dfrac{1}{1+2\gamma}\end{cases} \qquad 4.3.1.12$$

Next, solving 4.3.1.9 for β and using 4.3.1.12 leads to,

$$\beta=\begin{cases}1 & \sigma_A\le\dfrac{1}{1+2\gamma}\\[2ex] \dfrac{2\sigma_A\gamma}{1-\sigma_A} & \sigma_A>\dfrac{1}{1+2\gamma}\end{cases} \qquad 4.3.1.13$$

Substituting 4.3.1.12 and 4.3.1.13 into 4.3.1.6 yields,

$$\frac{T_{SC}}{T_t}=\begin{cases}\dfrac{\lambda}{\gamma\sigma_A} & \sigma_A\le\dfrac{1}{1+2\gamma}\\[2ex] \dfrac{2\lambda}{1-\sigma_A} & \sigma_A>\dfrac{1}{1+2\gamma}\end{cases} \qquad 4.3.1.14$$

The spanning cycle frequency is therefore,

$$\frac{f_{SC}}{f_t} = \begin{cases} \dfrac{\gamma\sigma_A}{\lambda} & \sigma_A \le \dfrac{1}{1+2\gamma} \\ \dfrac{1-\sigma_A}{2\lambda} & \sigma_A > \dfrac{1}{1+2\gamma} \end{cases} \qquad 4.3.1.14$$

The boundary separating the two spanning cycle regimes is shown in Figure 21. The boundary is identical to the boundary of the SPRDL $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle for $\beta = 1$, $T_0 = 0$, and $\lambda = 1$. However, as λ increases beyond unity, the SPRDL boundary moves toward increasing values of σ_A while the boundary of the hypothetical inverter remains stationary. Figure 22 shows a three-dimensional plot of the normalized $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle frequency in Ω_{100}. The existence of only two regimes as opposed to three for the SPRDL is evident in the absence of the notch seen for the SPRDL in Figure 18. Notice that from Figure 21, f_{SC} peaks at $(\sigma_A, \gamma) = (½, ½)$. The peak of the tetrahedron in Figure 22 is thus skewed toward S_0, making f_{SC} asymmetrical in Ω_i, for all i $\in \mathbf{S}^{*-}$.

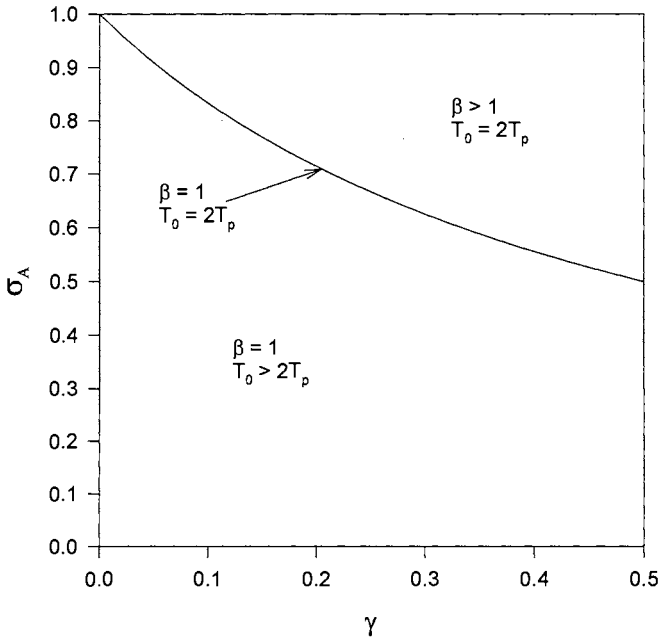


Figure 21. Regime boundary of the $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle for a hypothetical inverter with symmetrical state occupancy time characteristics

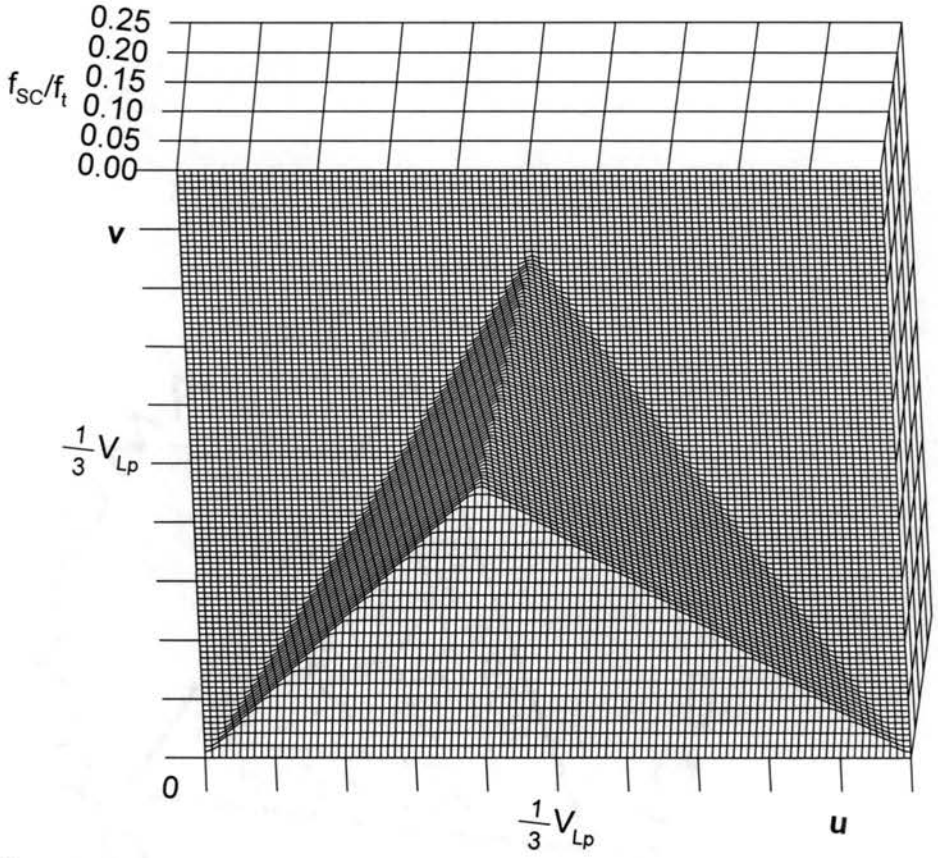


Figure 22. Three-dimensional plot of the normalized $\{\chi_{100,0}, \chi_{110,0}\}$ spanning cycle frequency of a hypothetical inverter with symmetrical state occupancy time characteristics

4.3.2 Analysis of the $\{\chi_{i,0}, \chi_{i,i+}\}$ Spanning Cycle

Section 4.3.1 addressed the impact of symmetrical allowed state occupancy times on the $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle. This section investigates the voltage stress and frequency characteristics of the $\{\chi_{i,0}, \chi_{i,i+}\}$ spanning cycle under the same symmetrical allowed state occupancy time conditions. Consider the $\{\chi_{i,0}, \chi_{i,i+}\}$ spanning cycle occupancy and effective occupancy plots shown in Figure 23. The state sequence is $\{S_i, S_{i+}, S_i, S_0, S_i, \ldots\}$. Owing to symmetry, the spanning cycle period is again composed of four distinct segments, T_{i1}, T_{i+}, T_{i2}, and T_0. As in the previous subsection, only the cumulative effective occupancy time spent in each state is needed to express f_{SC} as a function of σ_A and γ. Recall that in the $\{\chi_{i,0}, \chi_{i+,0}\}$ analysis, the two visits to S_0

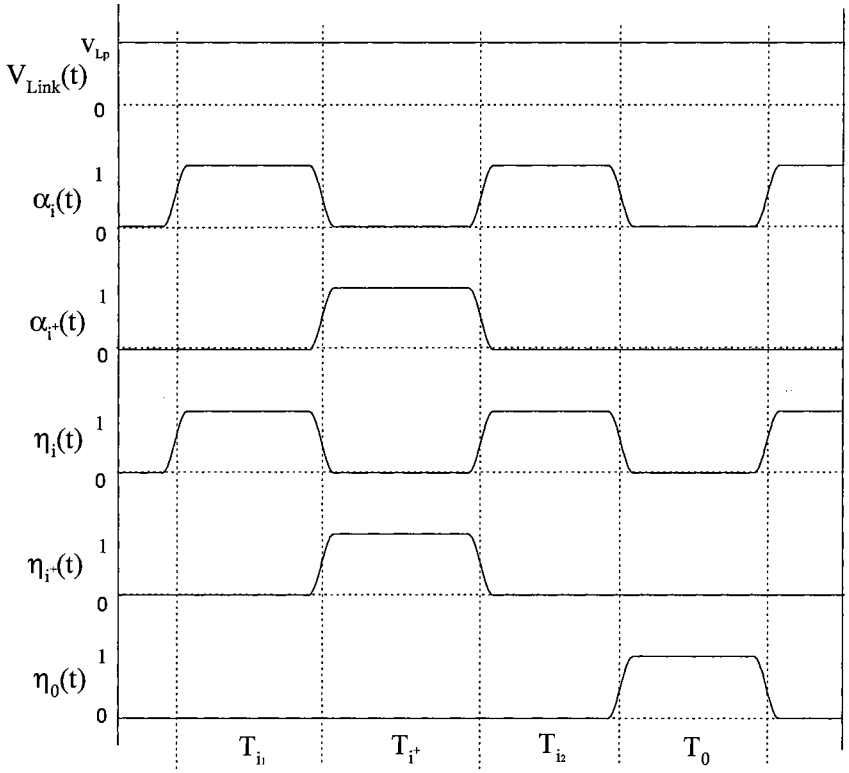


Figure 23. Representative link voltage, state occupancy, and effective state occupancy plots for the $\{\chi_{i,0}, \chi_{i,i+}\}$ spanning cycle of a hypothetical soft-switched inverter with symmetrical state occupancy time and state-to-state transition characteristics

resulted in two effective occupancy time components, T_{01} and T_{02}, which were combined into a single effective occupancy time for S_0. For the $\{\chi_{i,0}, \chi_{i,i+}\}$ spanning cycle, it is S_i that is visited twice, resulting in the two effective occupancy time components, T_{i1} and T_{i2}. The effective occupancy time in S_i is thus lumped into a single parameter, T_i, as defined below.

$$T_i = T_{i1} + T_{i2} \qquad 4.3.2.1$$

As before, state dependent parameters such as T_{pi} and T_{ci} are assumed to be the same for all $i \in \mathbf{S}^*$. From Figure 23, the spanning cycle period is,

$$T_{SC} = T_i + T_{i+} + T_0 \qquad 4.3.2.2$$

The restrictions on the individual terms in 4.3.2.2 are,

$$T_i \geq 2T_p \qquad 4.3.2.3$$

$$T_{i+} \geq T_p \qquad 4.3.2.4$$

$$T_0 \geq T_p \qquad 4.3.2.5$$

The restrictions on T_i and T_{i+} are now different than in the $\{\chi_{i,0}, \chi_{i+,0}\}$ case. For $\{\chi_{i,0}, \chi_{i,i+}\}$, T_{i+} can be maintained at T_p for values of γ near zero but T_i can only be reduced to $2T_p$ for values of γ near unity. Consequently, f_{SC} for $\{\chi_{i,0}, \chi_{i,i+}\}$ is not symmetric about $\gamma = ½$ in Ω_i, $i \in \mathbf{S}^{*-}$. However, since $T_{i+} > T_i$ for $\gamma > ½$, the $\{\chi_{i,0},\chi_{i,i+}\}$ spanning cycle period will necessarily be longer for $\gamma = ½ + \varepsilon$ than for $\gamma = ½ - \varepsilon$ for all $\varepsilon \in (0, ½)$. Given that f_{SC} for $\{\chi_{i,0}, \chi_{i,i+}\}$and f_{SC} for $\{\chi_{i+,0}, \chi_{i,i+}\}$ are mirror images in Ω_i about $\gamma = ½$, the $\{\chi_{i,0}, \chi_{i,i+}\}$ spanning cycle frequency will be greater than or equal to that of the $\{\chi_{i+,0}, \chi_{i,i+}\}$ spanning cycle for $\gamma \in (0, ½]$. Similarly, the values of f_{SC} for $\{\chi_{i+,0}, \chi_{i,i+}\}$ will be greater than or equal to those of $\{\chi_{i,0}, \chi_{i,i+}\}$ for $\gamma \in (½, 1)$. Hence, analysis of the $\{\chi_{i,0}, \chi_{i,i+}\}$ spanning cycle is only necessary for $\gamma \in (0, ½]$.

Applying 3.6.7 to 4.3.2.2 and normalizing with respect to T_t yields,

$$\frac{T_{SC}}{T_t} = \frac{\beta\lambda}{\gamma} + \frac{T_0}{T_t} \quad \gamma \in (0, ½] \qquad 4.3.2.6$$

However, $T_i \geq T_{i+}$ for $\gamma \in (0, ½]$. Consequently, from 3.6.10,

$$\beta = \frac{T_{i+}}{T_p} \qquad 4.3.2.7$$

The fact that T_i and T_{i+} must satisfy $T_i \geq 2T_p$ and $T_{i+} \geq T_p$ places a constraint on β that is not present in the case of the $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle. For values of γ approaching ½, T_i is free to decrease until it reaches $2T_p$. At this point, larger values of γ, up to ½, can only be realized by increasing β. It is easily shown using 4.3.2.3 in 3.6.7 that the resulting constraint on β is,

$$\beta \geq \frac{2\gamma}{1-\gamma} \qquad \gamma \in (0, \tfrac{1}{2}] \tag{4.3.2.8}$$

Since $\beta \geq 1$, the following inequality applies.

$$\beta \geq \max\left(\frac{2\gamma}{1-\gamma},\ 1\right) \tag{4.3.2.9}$$

The boundary separating the two cases in the maximum function occurs for $\gamma = \frac{1}{3}$, allowing the inequality to be written as,

$$\beta \geq \begin{cases} \dfrac{2\gamma}{1-\gamma} & \gamma \in (\tfrac{1}{3}, \tfrac{1}{2}] \\ 1 & \gamma \in (0, \tfrac{1}{3}] \end{cases} \tag{4.3.2.10}$$

Using 3.6.7, 3.6.8, and 4.3.2.6, σ_A can be expressed as,

$$\sigma_A = \frac{\lambda\beta}{\lambda\beta + \gamma\dfrac{T_0}{T_t}} \tag{4.3.2.11}$$

Solving 4.3.2.11 for T_0/T_t yields,

$$\frac{T_0}{T_t} = \frac{\lambda\beta(1-\sigma_A)}{\sigma_A\gamma} \quad 0 < \sigma_A < 1,\ 0 < \gamma \leq \tfrac{1}{2},\ \beta \geq 1 \tag{4.3.2.12}$$

However, combining 4.3.2.12 with condition 4.3.2.5 requires that,

$$\frac{T_0}{T_t} \geq \max\left(\frac{\lambda\beta(1-\sigma_A)}{\sigma_A\gamma}, \lambda\right) \quad 0<\sigma_A<1, 0<\gamma\leq\tfrac{1}{2},\ \beta\geq 1 \qquad 4.3.2.13$$

Applying 4.3.2.10 to 4.3.2.13 and selecting the smallest possible β, so that f_{SC} is maximized, produces,

$$\frac{T_0}{T_t} = \begin{cases} \max\left(\frac{\lambda(1-\sigma_A)}{\sigma_A\gamma}, \lambda\right), & \gamma\leq\frac{1}{3} \\ \max\left(\frac{2\lambda(1-\sigma_A)}{\sigma_A(1-\gamma)}, \lambda\right), & \gamma>\frac{1}{3} \end{cases} \qquad 4.3.2.14$$

Inspection of 4.3.2.14 shows that the boundary of the maximum function for the case of $\gamma\leq\frac{1}{3}$ is,

$$\sigma_A = \frac{1}{1+\gamma} \qquad 4.3.2.15$$

and that the boundary of the maximum function for the case $\gamma>\frac{1}{3}$ is,

$$\sigma_A = \frac{2}{3-\gamma} \qquad 4.3.2.16$$

The resulting expression for T_0/T_t is then,

$$\frac{T_0}{T_t} = \begin{cases} \frac{\lambda(1-\sigma_A)}{\sigma_A\gamma}, & \gamma\leq\frac{1}{3}, \sigma_A<\frac{1}{1+\gamma} \\ \frac{2\lambda(1-\sigma_A)}{\sigma_A(1-\gamma)}, & \gamma>\frac{1}{3}, \sigma_A<\frac{2}{3-\gamma} \\ \lambda & \text{Otherwise} \end{cases} \qquad 4.3.2.17$$

Solving 4.3.2.11 for β and using 4.3.2.17 yields,

$$\beta = \begin{cases} 1, & \gamma \le \frac{1}{3}, \sigma_A < \frac{1}{1+\gamma} \\ \frac{2\gamma}{1-\gamma}, & \gamma > \frac{1}{3}, \sigma_A < \frac{2}{3-\gamma} \\ \frac{\sigma_{A\gamma}}{1-\sigma_A}, & \text{Otherwise} \end{cases} \qquad 4.3.2.18$$

Using 4.3.2.18 and 4.3.2.17 in 4.3.2.6 produces,

$$\frac{T_{SC}}{T_t} = \begin{cases} \frac{\lambda}{\sigma_A \gamma}, & \gamma \le \frac{1}{3}, \sigma_A < \frac{1}{1+\gamma} \\ \frac{2\lambda}{\sigma_A(1-\gamma)}, & \gamma > \frac{1}{3}, \sigma_A < \frac{2}{3-\gamma} \\ \frac{\lambda}{1-\sigma_A}, & \text{Otherwise} \end{cases} \qquad 4.3.2.19$$

Finally, using 4.3.2.19 and again letting $f_t = \frac{1}{T_t}$ yields,

$$\frac{f_{SC}}{f_t} = \begin{cases} \frac{\sigma_A \gamma}{\lambda}, & \gamma \le \frac{1}{3}, \sigma_A < \frac{1}{1+\gamma} \\ \frac{\sigma_A(1-\gamma)}{2\lambda}, & \gamma > \frac{1}{3}, \sigma_A < \frac{2}{3-\gamma} \\ \frac{1-\sigma_A}{\lambda}, & \text{Otherwise} \end{cases} \qquad 4.3.2.20$$

The spanning cycle regime boundaries indicated in 4.4.20 are shown in Figure 24. Unlike the $\{\chi_{i,0}, \chi_{i,i+}\}$ spanning cycle who's regime boundaries divide Ω_i along the σ_A axis, the $\{\chi_{i,0}, \chi_{i,i+}\}$ spanning cycle is also divided along the γ axis, due to the asymmetrical constraint of 4.4.3.

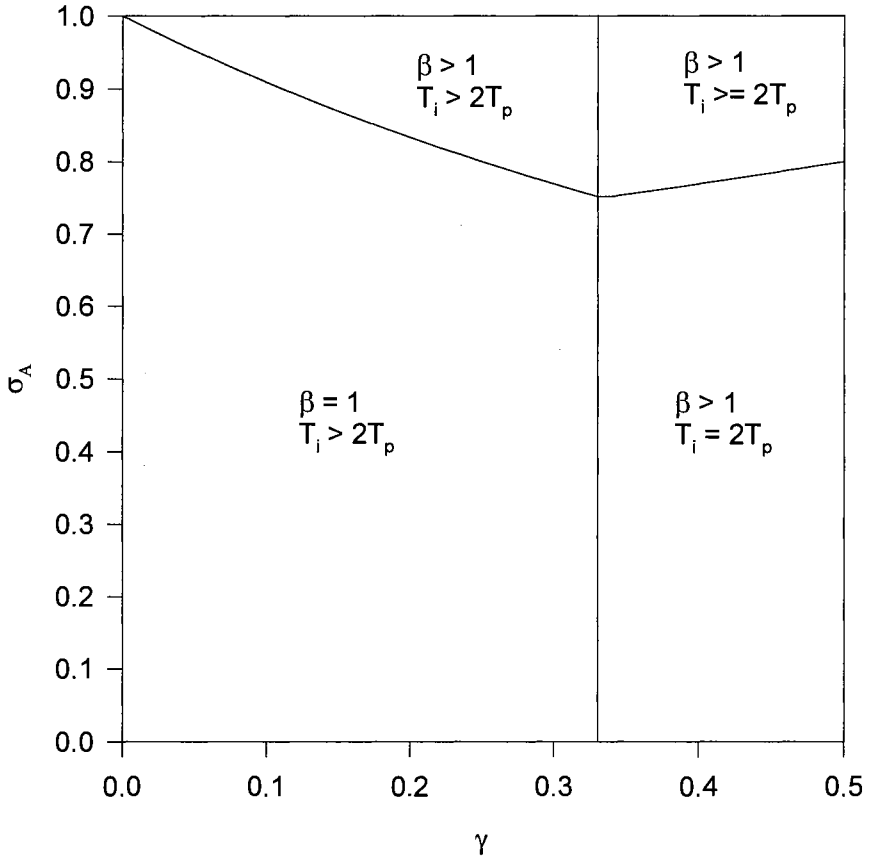


Figure 24. Regime boundaries of the $\{\chi_{i,0}, \chi_{i,i+}\}$ spanning cycle for a hypothetical inverter with symmetrical state occupancy time and state-to-state transition characteristics. Case shown is for $\lambda = 1$

Figure 25 shows the $\{\chi_{i,0}, \chi_{i,i+}\}$ spanning cycle frequency for $\gamma \in (0, \frac{1}{2}]$ in Ω_{100} along with f_{SC} for the $\{\chi_{i+,0}, \chi_{i,i+}\}$ spanning cycle for $\gamma \in (\frac{1}{2}, 1)$. The spanning cycle regime boundaries shown in Figure 24 are evident in Figure 25. Significant frequency degradation, resulting from double occupancy of either S_i or S_{i+}, clearly exists for values of γ near $\frac{1}{2}$. Examination of Figure 24 and Figure 25 shows that the peaks of f_{SC} are skewed away from the center of Ω_{100} toward the active states, in contrast to the $\{\chi_{i,0}, \chi_{i+,0}\}$ case.

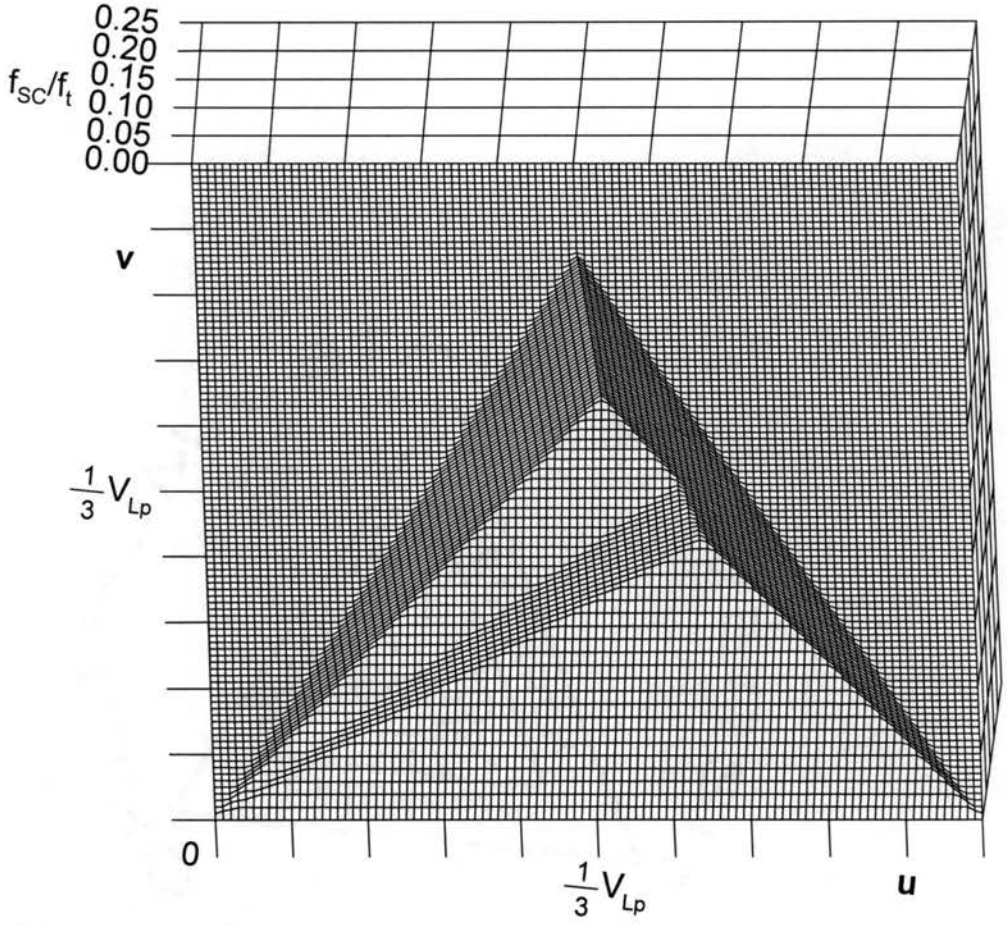


Figure 25. Three-dimensional plot of the $\{\chi_{i,0}, \chi_{i,i+}\}$ spanning cycle frequency for a hypothetical inverter with symmetrical state occupancy time and state-to-state transition characteristics

4.3.3 Analysis of the $\{\chi_{i,0,i+}\}$ Spanning Cycle

The final spanning cycle of the hypothetical topology to analyze is $\{\chi_{i,0,i+}\}$. Figure 26 shows representative occupancy and effective occupancy plots for $\{\chi_{i,0,i+}\}$. Again, identical transition and occupancy characteristics are assumed for S_i, S_{i+}, and S_0. The state sequence depicted in the figure is $\{S_0, S_i, S_{i+}, S_0, S_i, \ldots\}$. From inspection of the figure, the spanning cycle period is,

$$T_{SC} = T_i + T_{i+} + T_0$$

4.3.3.1

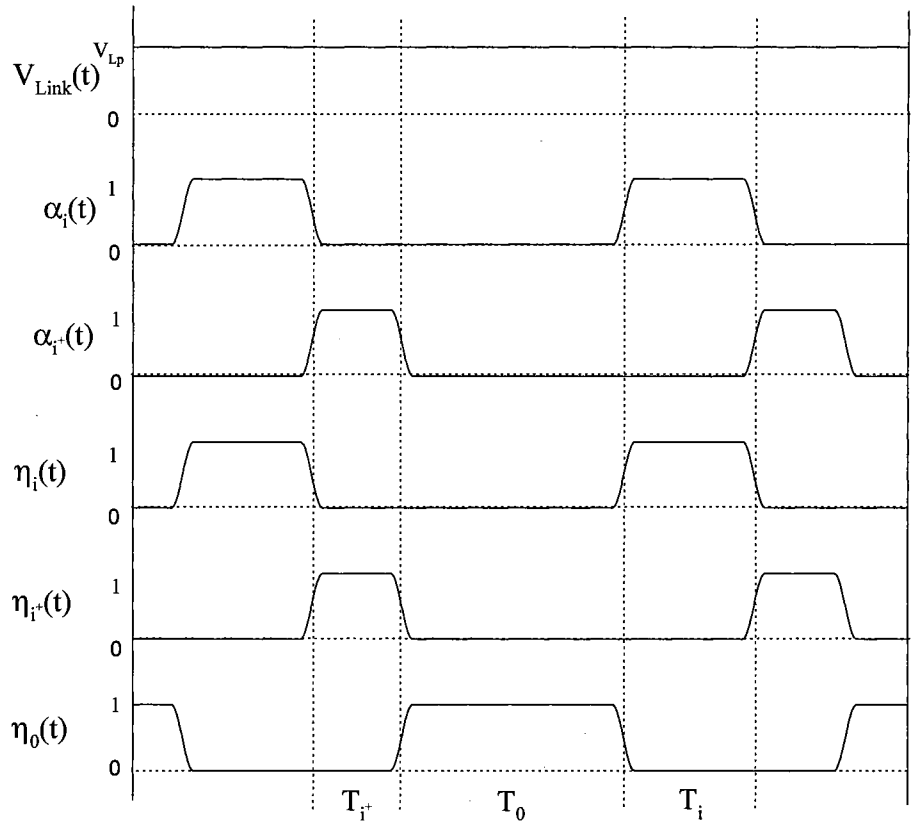


Figure 26. State occupancy and effective state occupancy for the $\{\chi_{i,0,i+}\}$ spanning cycle of a hypothetical inverter with symmetrical state occupancy times and state-to-state transition characteristics

For $\{\chi_{i,0,i+}\}$, S_i, S_{i+}, and S_0 are visited only once. Thus, the restrictions on T_i, T_{i+}, and T_0 are,

$$T_i \geq T_p \qquad 4.3.3.2$$

$$T_{i+} \geq T_p \qquad 4.3.3.3$$

$$T_0 \geq T_p \qquad 4.3.3.4$$

As for $\{\chi_{i,0}, \chi_{i+,0}\}$, symmetry allows for consideration of only the case $\gamma \in (0, ½]$, for which,

$$\beta = \frac{T_{i+}}{T_p} \qquad 4.3.3.5$$

Using 3.6.7, 3.6.11, and 4.3.3.5, 4.3.3.1 can be written as,

$$\frac{T_{SC}}{T_t} = \frac{\lambda\beta}{\gamma} + \frac{T_0}{T_t} \qquad 4.3.3.6$$

Using 4.3.3.6 in 3.6.8 produces the effective active state occupancy,

$$\sigma_A = \frac{\lambda\beta}{\lambda\beta + \gamma\left(\frac{T_0}{T_t}\right)} \qquad 4.3.3.7$$

Solving 4.3.3.7 for $\frac{T_0}{T_t}$ yields,

$$\frac{T_0}{T_t} = \frac{\lambda\beta}{\gamma\sigma_A}(1-\sigma_A) \qquad 4.3.3.8$$

But $\frac{T_0}{T_t} \geq \frac{T_p}{T_t} = \lambda$, Thus,

$$\frac{T_0}{T_t} = \max\left(\frac{\lambda\beta}{\gamma\sigma_A}(1-\sigma_A),\ \lambda\right) \qquad 4.3.3.9$$

Unlike the $\{\chi_{i,0}, \chi_{i,i+}\}$ case, the restrictions on T_i and T_{i+} do not force β to be greater than unity in order to achieve certain values of γ. Thus, there is no need to have both β and T_0 simultaneously greater than there respective minimal values. Since maximizing f_{SC} requires minimizing β and T_0, T_0 is greater than T_p only when $\beta = 1$. Consequently, the boundary in Ω_i, $i \in \mathbf{S}^{*-}$, separating the two terms in the maximum function of 4.3.3.9 also separates the cases of $\beta = 1$ and $\beta > 1$. Using this fact in 4.3.3.9 produces,

$$\frac{T_0}{T_t} = \begin{cases} \dfrac{\lambda(1-\sigma_A)}{\gamma\sigma_A} & \sigma_A \le \dfrac{1}{1+\gamma} \\ \lambda & \sigma_A > \dfrac{1}{1+\gamma} \end{cases} \qquad 4.3.3.10$$

Next, solving 4.3.3.7 for β and using 4.3.3.10 produces,

$$\beta = \begin{cases} 1 & \sigma_A \le \dfrac{1}{1+\gamma} \\ \dfrac{\gamma\sigma_A}{1-\sigma_A} & \sigma_A > \dfrac{1}{1+\gamma} \end{cases} \qquad 4.3.3.11$$

Using 4.3.3.10 and 4.3.3.11 in 4.3.3.6 yields,

$$\frac{T_{SC}}{T_t} = \begin{cases} \dfrac{\lambda}{\gamma\sigma_A} & \sigma_A \le \dfrac{1}{1+\gamma} \\ \dfrac{\lambda}{1-\sigma_A} & \sigma_A > \dfrac{1}{1+\gamma} \end{cases} \qquad 4.3.3.12$$

The $\{\chi_{i,0,i+}\}$ spanning cycle frequency is thus,

$$\frac{f_{SC}}{f_t} = \begin{cases} \dfrac{\gamma\sigma_A}{\lambda} & \sigma_A \le \dfrac{1}{1+\gamma} \\ \dfrac{1-\sigma_A}{\lambda} & \sigma_A > \dfrac{1}{1+\gamma} \end{cases} \qquad 4.3.3.13$$

Figure 27 shows the $\{\chi_{i,0,i+}\}$ spanning cycle boundary separating the cases of $\beta = 1$ and $\beta > 1$ while Figure 28 depicts f_{SC} in Ω_{100}. The values of f_{SC} peak at the geometric center of Ω_i, $\sigma_A = \frac{2}{3}$ and $\gamma = \frac{1}{2}$, and are fully symmetrical in Ω_i with respect to S_i, S_0, and S_{i+}. Finally, the peak value of f_{SC} is $\frac{1}{3} f_t$ in contrast to $\frac{1}{4} f_t$ or less for all previous cases examined.

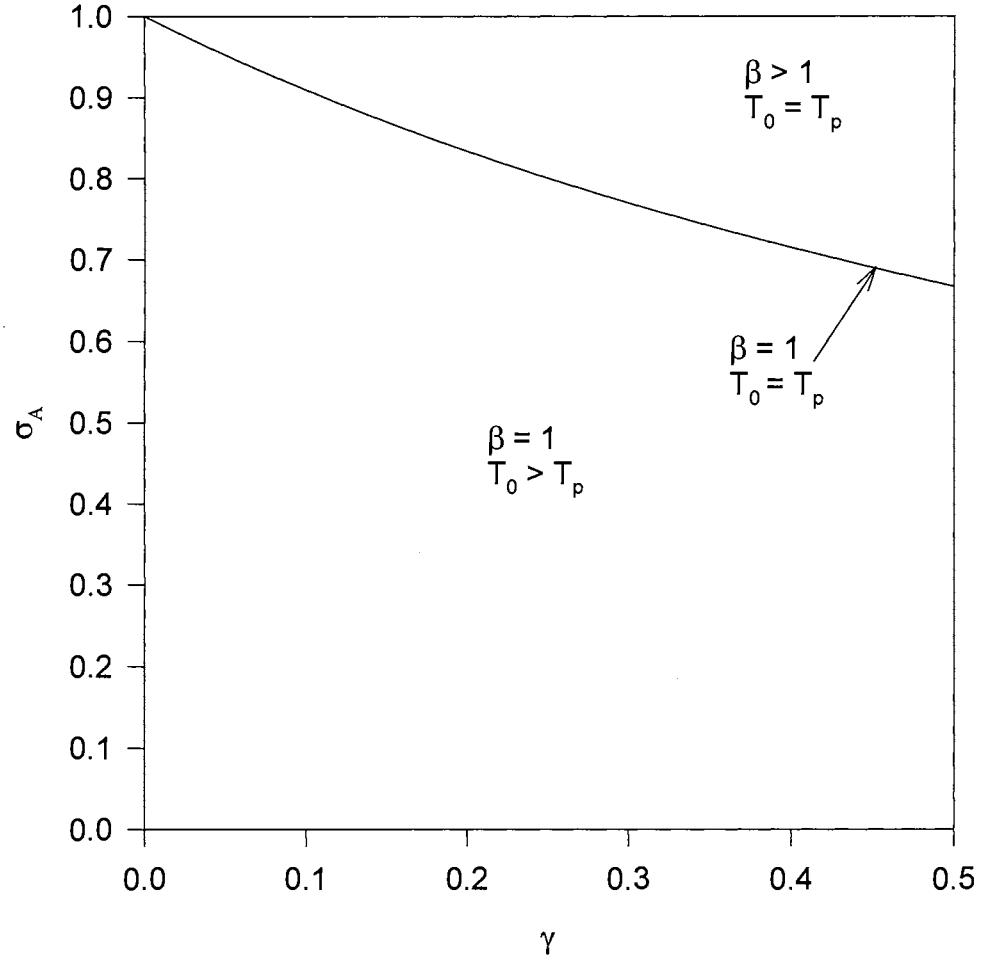


Figure 27. Regime boundary for the $\{\chi_{i,0,i+}\}$ spanning cycle of a hypothetical inverter with symmetrical state occupancy times and state-to-state transition characteristics

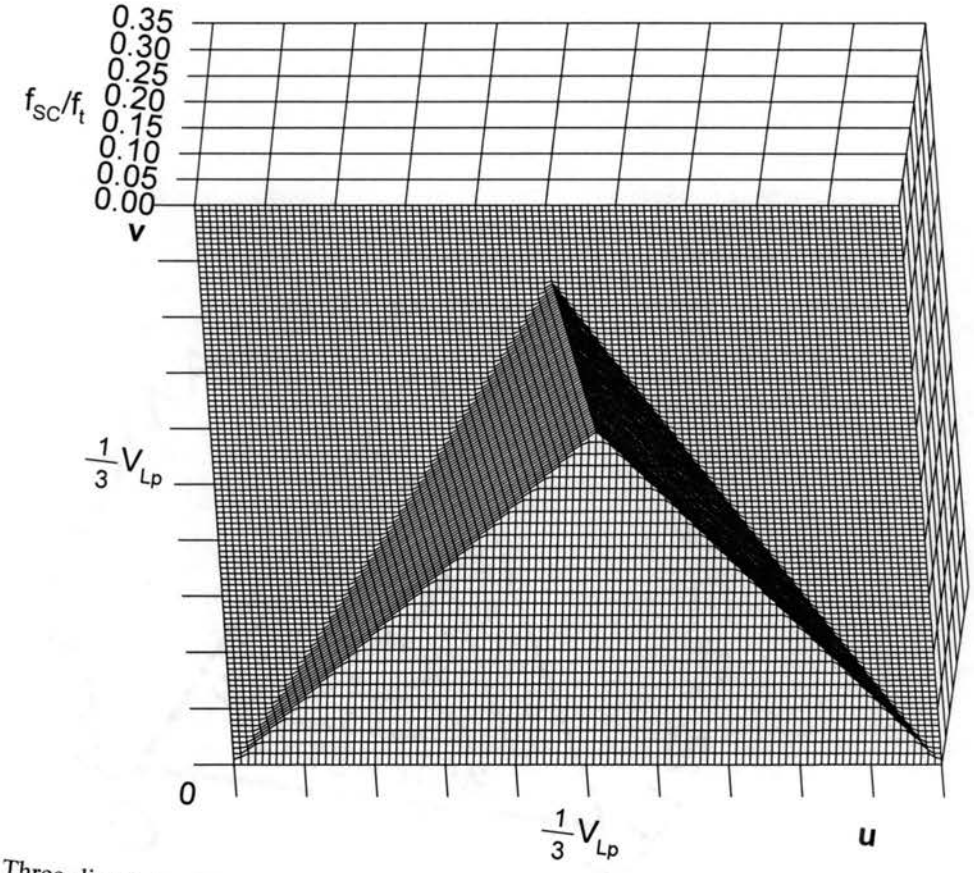


Figure 28. Three-dimensional plot of the $\{\chi_{i,0,i+}\}$ spanning cycle frequency of a hypothetical inverter with symmetrical state occupancy times and state-to-state transition characteristics

4.3.4 Analysis of the $\chi_{i,0}$ Primitive Cycle

The symmetrical state occupancy times and state-to-state transition characteristics assumed for the hypothetical topology produce different $\chi_{i,0}$ primitive cycle frequency characteristics than seen for the SPRDL topology. Since the state sequence for $\chi_{i,0}$ is simply $\{S_i, S_0, S_i, \ldots\}$, the primitive cycle period is,

$$T_{PC} = T_i + T_0$$

4.3.4.1

where T_i and T_0 are the effective times spent in S_i and S_0, respectively. Under the symmetrical allowed state occupancy time assumptions made earlier, the sole constraints on T_i and T_0 are,

$$T_i \geq T_p \qquad 4.3.4.2$$

$$T_0 \geq T_p \qquad 4.3.4.3$$

Since full symmetry exists between S_i and S_0, values of $\sigma_A < ½$ require the minimum amount of time spent in S_i while values of $\sigma_A \geq ½$ require the minimum amount of time spent in S_0. Consequently,

$$T_{PC} = T_i + T_p \quad \sigma_A \geq ½ \qquad 4.3.4.4$$

where $T_i \geq T_p$ and

$$T_{PC} = T_p + T_0 \quad \sigma_A < ½ \qquad 4.3.4.5$$

where $T_0 \geq T_p$.

Applying 3.6.8 and solving for T_i and T_0, respectively, produces,

$$\sigma_A = \begin{cases} \dfrac{T_i}{T_i + T_p} & \sigma_A \geq \frac{1}{2} \\ \dfrac{T_p}{T_p + T_0} & \sigma_A < \frac{1}{2} \end{cases} \qquad 4.3.4.6$$

Using 3.6.8 with $T_{i+} = 0$ along with 4.3.4.1 yields,

$$\frac{T_{PC}}{T_t} = \begin{cases} \dfrac{\lambda}{1-\sigma_A} & \sigma_A \geq \frac{1}{2} \\ \dfrac{\lambda}{\sigma_A} & \sigma_A < \frac{1}{2} \end{cases} \qquad 4.3.4.7$$

The $\chi_{i,0}$ primitive cycle frequency is then,

$$\frac{f_{PC}}{f_t} = \begin{cases} \frac{1-\sigma_A}{\lambda} & \sigma_A \geq \frac{1}{2} \\ \frac{\sigma_A}{\lambda} & \sigma_A < \frac{1}{2} \end{cases} \qquad 4.3.4.8$$

Figure 29 shows the $\chi_{i,0}$ primitive cycle frequency as a function of σ_A for $\lambda = 1$. Notice the simple symmetry about $\sigma_A = ½$. This is in contrast to the SPRDL case which exhibits a significant notch for $\sigma_A \in (0.25, 0.50)$ resulting from the asymmetry in the allowed state occupancy times for active and passive states.

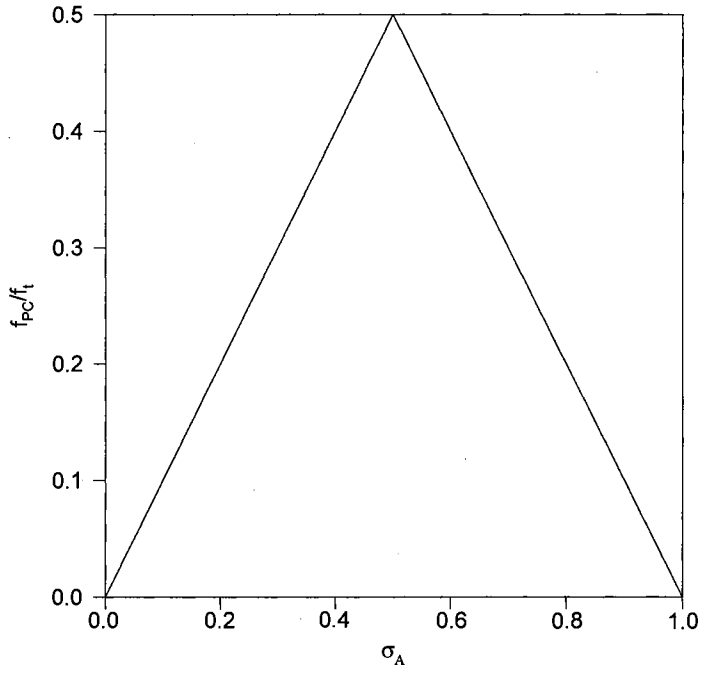


Figure 29. $\chi_{i,0}$ primitive cycle frequency for a hypothetical topology with symmetrical allowed state occupancy time and state-to-state transition characteristics

4.3.5 Analysis of the $\chi_{i,i+}$ Primitive Cycle

The state sequence for $\chi_{i,i+}$ is $\{S_i, S_{i+}, S_i, \ldots\}$. For $\gamma \leq ½$, State S_{i+} is occupied for the minimal length of time while for $\gamma \geq ½$, State S_i is occupied for the minimal amount of time. The primitive cycle period is,

$$T_{PC} = T_i + T_{i+} \tag{4.3.5.1}$$

and the constraints on T_i and T_{i+} are,

$$T_i \geq T_p \tag{4.3.5.2}$$

$$T_{i+} \geq T_p \tag{4.3.5.3}$$

Similar to the $\chi_{i,0}$ case,

$$T_{PC} = T_p + T_{i+}, \quad \gamma \geq ½ \tag{4.3.5.4}$$

where $T_{i+} \geq T_p$ and

$$T_{PC} = T_i + T_p, \quad \gamma < ½ \tag{4.3.5.5}$$

where $T_i > T_p$.

Using 3.6.7 yields,

$$\gamma = \begin{cases} \dfrac{T_{i+}}{T_{i+} + T_p}, & \gamma \geq \frac{1}{2} \\ \dfrac{T_i}{T_i + T_p}, & \gamma < \frac{1}{2} \end{cases} \tag{4.3.5.6}$$

Substituting 4.3.5.6 into 4.3.5.1 produces,

$$\frac{T_{PC}}{T_t} = \begin{cases} \dfrac{\lambda}{1-\gamma} & \gamma \in [\frac{1}{2},1) \\ \dfrac{\lambda}{\gamma} & \gamma \in (0,\frac{1}{2}) \end{cases} \qquad 4.3.5.7$$

$$\frac{f_{PC}}{f_t} = \begin{cases} \dfrac{1-\gamma}{\lambda} & \gamma \in [\frac{1}{2},1) \\ \dfrac{\gamma}{\lambda} & \gamma \in (0,\frac{1}{2}) \end{cases} \qquad 4.3.5.8$$

Under symmetrical allowed state occupancy time and state-to-state transition conditions, the $\chi_{i,i+}$ primitive cycle frequency should have the same distribution along the γ axis as the $\chi_{i,0}$ primitive cycle has along the σ_A axis. This is in fact the case, as shown in Figure 30.

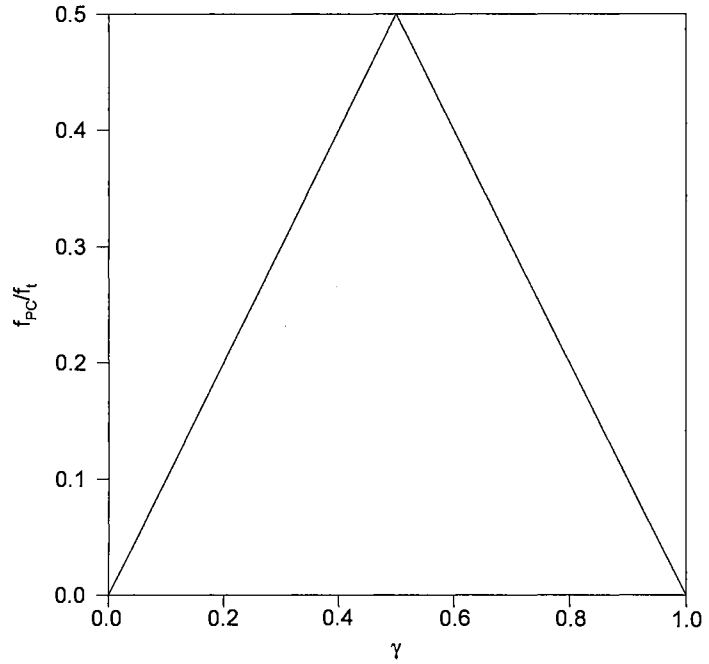


Figure 30. $\chi_{i,i+}$ primitive cycle frequency for a hypothetical topology with symmetrical allowed state occupancy time and state-to-state transition characteristics

4.3.6 Discussion and Conclusions Regarding Symmetrical Allowed State Occupancy Times and Symmetrical State-to-State Transition Characteristics

The analytical results are now in hand to ascertain the potential benefit of augmenting the SPRDL primitive cycle set with $\chi_{i,0}$ and $\chi_{i+,0}$ along with removing the asymmetry in the allowed state occupancy times. Contour maps of the SPRDL and hypothetical inverter spanning cycle frequencies, previously illustrated as three-dimensional surfaces in Figures 18, 22, 25, and 28, are provided below to foster the discussion. The contour maps are annotated to show voltage trajectories in the Ω_{100} sector of **H** for operation at rated and one-half rated voltage.

The effects of removing the state occupancy time constraint on S_0 are apparent from comparison of Figure 31, which shows the SPRDL $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle frequency, with Figure 32, which illustrates the $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle frequency for the hypothetical inverter. Note that the differences are due solely to relaxation of the allowed occupancy time constraint on S_0 and not the augmentation of the allowed spanning cycle set. Removing the occupancy time constraint has the net effect of eliminating the "V" shaped notch seen in Figure 31. For operation at voltages from about 70% to 100% of the rated inverter voltage, the notch has little impact. As the voltage decreases to 50% rated, approximately ½ of the trajectory lies in the degraded region. For $\sigma_A = 0.5$ and $\gamma = 0.5$, removing the occupancy time constraint on S_0 doubles the spanning cycle frequency from $0.125f_t$ to $0.25f_t$. Below about 33% of the rated inverter voltage, any potential benefit vanishes.

Figure 33 shows the $\{\chi_{i,0}, \chi_{i,i+}\}$-$\{\chi_{i+,0}, \chi_{i,i+}\}$ spanning cycle frequency of the hypothetical inverter. Comparison of Figure 33 with Figure 31 reveals that the spanning cycle frequency is essentially twice that of the SPRDL for voltages near 100% rated. The advantage begins to reverse as the voltage falls below 50% rated. The dip in the spanning cycle frequency near $\gamma = ½$, resulting from the second visit to one of the active states, is responsible for the degradation.

Notice, however, that the hypothetical inverter $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle frequency exceeds or matches that of the SPRDL in this region.

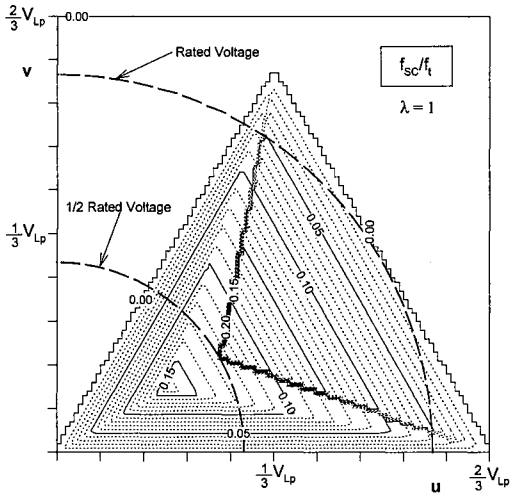


Figure 31. Contour map of the SPRDL $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle frequency in Ω_{100}

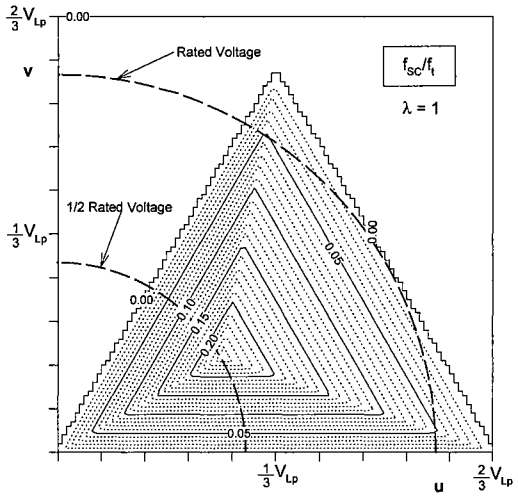


Figure 32. Contour map of the $\{\chi_{i,0}, \chi_{i+,0}\}$ spanning cycle frequency in Ω_{100} for a hypothetical inverter with symmetrical allowed state occupancy time characteristics for both active and inactive states

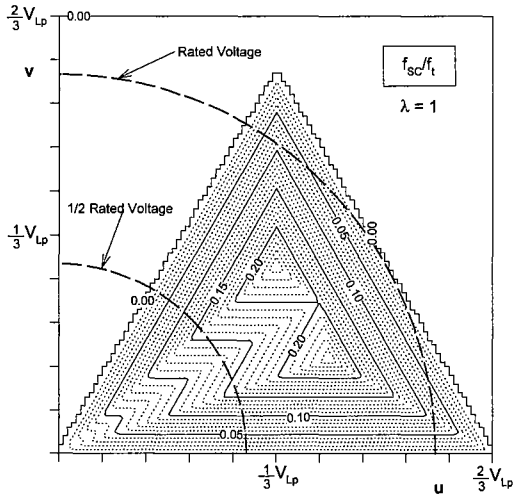


Figure 33. Contour map of the $\{\chi_{i,0}, \chi_{i,i+}\}$-$\{\chi_{i+,0}, \chi_{i,i+}\}$ spanning cycle frequency in Ω_{100} for a hypothetical inverter with symmetrical allowed state occupancy times and state-to-state transition characteristics

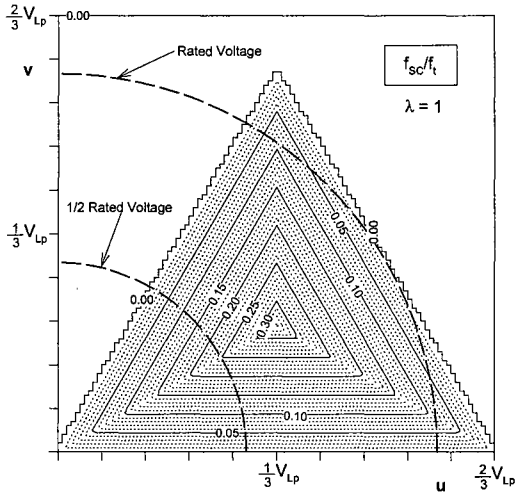


Figure 34. Contour map of the $\{\chi_{i,0,i+}\}$ spanning cycle frequency in Ω_{100} for a hypothetical inverter with symmetrical allowed state occupancy times and state-to-state transition characteristics

The most striking contour plot is that of the $\{\chi_{i,0,i+}\}$ spanning cycle frequency for the hypothetical inverter show in Figure 34. The $\{\chi_{i,0,i+}\}$ spanning cycle is clearly superior, in terms of spanning cycle frequency, to both the SPRDL and the other hypothetical inverter spanning cycles for all output voltages above one third of the rated value. Below one third of the rated voltage, the spanning cycle frequency is at least as high as that of the SPRDL.

Increasing the spanning cycle frequency through augmenting the allowed spanning cycle set is not the only mechanism for improvement made apparent by the developments presented in this and the preceding chapters. The above comparisons have been made with a key parameter, λ, equal to unity. In practical SPRDL designs, the minimum obtainable value of λ can easily exceed 2.0 [8-9]. Examination of 3.9.2.24 reveals that the spanning cycle regime boundaries move toward larger values of σ_A as λ increases and that the spanning cycle frequency is inversely proportional to λ for regimes below the upper boundary. For the hypothetical inverter, examination of 4.3.1.14, 4.3.2.20, and 4.3.3.13 show that the spanning cycle frequency is inversely proportional to λ throughout **H**. Developing a SPRDL topology variant with a value of λ approximately equal to one would likely be a of significant value. A more profound development, however, would be to develop a topology with the voltage space properties of the hypothetical inverter and a value of λ near unity. It will be seen in the next few chapters that this is in fact approximately achievable.

4.4 Soft-Switched Inverter Development Philosophy

4.4.1 Overview

The Results of the preceding spanning cycle frequency analysis along with a detailed review of the soft-switched topologies summarized in Chapter II suggest certain philosophical views that may serve as valuable guidelines for developing new soft-switched topologies. The remainder of

this section addresses six issues reflecting the leading fundamental questions encountered in devising new soft-switched topologies. The corresponding viewpoints and remarks are based on concepts presented in this work combined with an interpretation and evaluation of the strategies proposed in the soft-switched inverter literature that have lead to the maturing of the UPRDL and SPRDL topologies.

4.4.2 Voltage-Source Versus Current-Source Topologies

Fast and accurate torque response typify high performance machine drives. Stator and rotor current determine the instantaneous electromagnetic torque developed in a rotating machine. Rotor current is a slow changing state variable controlled by the machine drive control system, of which the inverter is a functional block. Sudden change in electromagnetic torque, such as that required to compensate for an abrupt load disturbance, is due almost exclusively to rapid changes in the machine stator currents. The rate of change in stator currents depends on the voltage applied across the stator terminals and the effective machine back EMF. The effective back EMF, which includes the voltage drop across the stator winding resistance, depends on the machine design and state. However, the voltage slew rate across the stator windings depends exclusively on the machine drive circuitry. Consequently, only machine drives with the ability to rapidly change their output voltage are suited for applications requiring fast torque response.

Current source inverters require shunt capacitors across the stator terminals to prevent damaging voltage spikes from occurring when inverter output currents are abruptly turned on and off during normal switching. Although the shunt capacitors help filter the line-to-line voltage seen at the stator terminals, they limit the maximum slew rate of the stator terminal voltages. Increased slew rate is obtainable only through increasing the peak inverter current rating well beyond that required for ordinary steady-state operation.

Voltage-source inverters use the machine stator inductance as an integral mechanism for limiting the line current slew rate to manageable levels. Voltage source topologies innately produce rapid changes in the stator terminal voltage, without incurring additional stresses. Consequently, voltage source topologies are natural structures for controlling inductive load currents. Under duality, current source topologies are natural choices for capacitive loads like capacitively filtered UPS systems where shunt capacitor line filters are an integral part of the UPS design. In summary, high performance machine drives should be based on a voltage-source topology.

4.4.3 Allowed State Occupancy Times

For three-wire three-phase loads, the conventional voltage-source bridge is believed to have the lowest achievable device voltage stress rating. The prime reason for this is the ability to maintain a given combination of line-to-line voltages for an indefinite period. In terms of Chapter III, the conventional bridge can maintain $\eta_0(t) = 0$ for an indefinite period. The major cause of high device voltage stresses in unsynchronized resonant link designs is the unavoidable occupancy of the zero state once every resonant cycle. Some SPRDL structures can remain in a given state indefinitely but all must pass through S_0 prior to entering any active state. Additionally, SPRDL designs do not permit the same control freedom for the zero state occupancy time as for active states. This forces active state occupancy times to be extended in certain cases in order to achieve the required synthesized voltage, degrading spectral performance. Removing this restriction so that the controllable occupancy time is the same for all states has potential value, as was seen in the previous section. In summary, the controllable occupancy time should be both unconstrained and uniform for all states in $\mathbf{S}^*$.

4.4.4 Direct Active-State to Active-State Transitions

The leg voltages of a conventional voltage source bridge inverter are free to transition between the upper and lower power matrix rail potentials independently, leaving state-to-state transitions totally unconstrained. The restricted primitive cycle set available to resonant link topologies forces them to always pass through the zero state when transitioning between active states, lowering the maximum attainable effective inverter line-to-line voltage. This necessitates increased inverter DC input voltage and consequently increased power matrix voltage stress. Synchronized designs reduce this effect by extending the allowable active state occupancy time. However, this can reduce the effective switching frequency, increasing line current distortion. The ability to transition directly between active states eliminates the need to elevate the DC input voltage or increase the active state occupancy time to compensate for time spent in the zero state. The preceding spanning cycle analysis clearly supports both notions.

4.4.5 Resonant Circuit Utilization

ZVS is only approximately achievable. In practice, the voltage across at least one conducting switch will begin to rise before turn-off is complete, regardless of the resonant circuit configuration employed. To minimize this effect, ZVS topologies should allow switching to occur only near the voltage crests of the resonant tank circuit where the dv/dt is minimal. By definition of ZVS, switch turn-on must occur only when the voltage across a switch is nearly zero, typically less than about three to five volts. Like the turn-off case, the resonant circuit must also maintain near zero-voltage conditions across all switches until they enter saturation. Again, this implies switch turn-on at tank voltage crests where the dv/dt is minimal. Although diodes are currently available with turn-on and turn-off times several times shorter than switches, similar care should be given to arranging the resonant circuit so that diodes are also switched under relatively low dv/dt conditions.

All resonant link topologies reported to date have the ability to switch only once per resonant cycle. If switching is limited to time intervals near the tank circuit voltage crests as recommended above, there are two potential switching instants per resonant cycle. If effectively exploited, the potential exists for producing a topology with ZVS conditions similar to the resonant link topology but with up to twice the switching frequency.

4.4.6 Resonant Circuit Configuration

The prevailing resonant link topologies all use dedicated auxiliary switches in the resonant circuit. In the ACPRDL described in Chapter II, the clamp switch S_{Clamp} must tolerate approximately 100% of the peak tank circuit current. All synchronized topologies use one or more switches in series with the tank inductance, resulting in the entire tank circuit current flowing through at least one auxiliary switch. The resonant components are typically chosen so that the peak tank current is 2-3 times the peak load current. This is done to prevent large tank current initialization delays during state transitions. Without paralleling the switches in the auxiliary circuit, this restricts the maximum inverter volt-ampere rating to about one third to one half that realizable if the rating were based solely on the power matrix switch current ratings.

The auxiliary switch involvement in the resonant circuit adds to the overall conversion losses through both conduction and switching losses. Auxiliary switch conduction losses can approach the total power matrix conduction losses. Switching losses in the auxiliary switches may be high if switching occurs far away from the resonant circuit voltage crests. The ACPRDL and the SPRL proposed in [9] are prime examples of designs with high auxiliary switch turn-off energies.

Ideally, the resonant tank should be free running with the only external interaction being that needed to replace energy dissipated in the reactive components and to provide voltage clamping across the power matrix switches during turn-on and turn-off. Developing alternatives to the

resonant link topology that employ resonant circuits operating under these conditions may lead to lower conversion losses and lower cumulative device volt-ampere ratings.

4.4.7 Switch Count

Although the attractiveness of the original resonant link inverter was low switch count, the cumulative volt-ampere rating of auxiliary circuit switches in most practical designs, especially synchronized topologies, is comparable to at least one half of the cumulative power matrix switch volt-ampere rating. Hence, there is no discernible basis for dismissing high switch count candidate topologies without first evaluating their required cumulative volt-ampere rating and performance potential.

4.5 Summary and Conclusions

This chapter has examined the shortcomings of the SPRDL topology resulting from its inability to directly transition between active states and to control the occupancy time in S_0 to the same degree for the active states. The concepts of Chapter III were employed to first suggest and then to analyze a hypothetical topology capable of executing all four primitive cycles available to bridge topologies. In addition, symmetrical allowed state occupancy time characteristics were assumed for the hypothetical inverter. Analysis of each spanning cycle available to the hypothetical inverter revealed a clear advantage over SPRDL topologies in terms of both voltage stress levels and spanning cycle frequency. The chapter concluded with a discussion of issues relevant to the synthesis of third generation soft-switched topologies, such as the one proposed in the next chapter.

CHAPTER V

THE PARALLEL RESONANT AUXILIARY LINK INVERTER

5.1 Introduction

The previous two chapters dealt with abstract notions that culminated in a hypothetical topology class ostensibly superior to the parallel resonant link topology. The obvious problem at this point is that the discussions have disregarded physical limitations and assumed that such a structure is realizable. The purpose of this chapter is to introduce a new soft-switched topology class and to propose the first inverter design belonging to that class. The term Auxiliary Link (AL) inverter class is coined here to denote this new topology class in which a special link is incorporated to implement the soft switching function. The name selected for the specific AL inverter design proposed in this work is the Parallel Resonant Auxiliary Link (PRAL) inverter. This name stems from the parallel resonant circuit used to drive the inverter's auxiliary link. The PRAL inverter, as well as other potential members of the AL inverter class, approximates the voltage-space characteristics of the hypothetical inverter described in the previous chapter. The development of the PRAL inverter is presented as a first attempt at synthesizing the hypothetical inverter and is purposely not required to precisely replicate its voltage-space characteristics. Put another way, the PRAL inverter is intended to be the first practical member of the AL inverter class, much like the ACPRDL was the first practical PRDL design. The PRAL inverter is thus offered as a new foundation upon which improved designs may be constructed in the future.

5.2 The Auxiliary Link Approach

The apparent simplicity of the special class of electronics known as "power electronics" is quickly dispelled once circuit synthesis begins. Synthesizing a physical circuit capable of emulating the voltage space properties of the hypothetical inverter proposed in Chapter IV is as much an art as a science. Although the previous chapter presented several guidelines pertaining to key issues that typically arise in the soft-switched inverter design process, insufficient clues exist to uniquely identify a structure that fully mimics the hypothetical inverter in voltage space. This is where the art of drawing an analogy with another physical system becomes an indispensable tool for filling the voids in, what is unfortunately, an incomplete theory.

The design guidelines of Chapter IV provide the only tangible clues at this point regarding the nature of the "consummate soft-switched inverter" and are thus the logical starting point for the synthesis process. To begin, the basic structure should somehow resemble a conventional bridge since the hypothetical inverter, as well as the spanning cycle concept, is based on a generalized bridge. Next, the inverter should be a voltage source rather than a current source design in order to satisfy the stated objectives of this work, i.e. development of a new machine drive. Using these two simple points, the general structure of the new topology is reduced from total obscurity to a structure resembling the conventional voltage source bridge inverter shown in Figure 35.

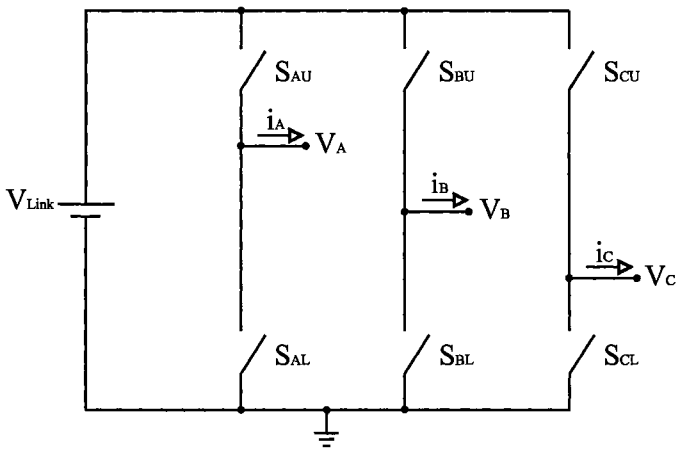


Figure 35. Schematic diagram of a conventional voltage-source bridge inverter

Recall that for the hypothetical inverter, the state occupancy functions are continuous and the link voltage is constant. This is in sharp contrast to the resonant link structure. The differences are a direct consequence of enabling direct transitions between active states. The constant voltage source, V_{Link}, shown between the upper and lower rails in Figure 35 is fully consistent with the hypothetical inverter characteristics. However, synthesis of the remaining circuitry needed to realize continuous state occupancy functions, not to mention soft switching, requires reexamination of the hypothetical inverter's voltage space behavior.

Recall that the states visited during a spanning cycle are exactly the states defining the particular Ω_i, $i \in \mathbf{S}^{*}$, containing the voltage being synthesized. Next, recall that the state transitions comprising a spanning cycle consist of level changes in either one or two phase leg voltages. Consider the case of a synthesized voltage $\mathbf{V}_P$ lying in Ω_{100}. The spanning cycle involves power matrix states S_{100}, S_{110}, and S_0, where S_0 actually consists of the two degenerate states S_{000} and S_{111}. Notice that S_{100} and S_{110} differ by exactly one phase leg level and that the states in the state pairs S_{100}-S_{000} and S_{110}-S_{111} also differ by exactly one phase leg level. From the perspective of the load, all three states defining Ω_{100} effectively differ by exactly one phase leg level. This is because transitions from a given active state to either S_{000} or S_{111} are identical in voltage space, as viewed by the load. Consequently, transitions between the active states and S_0 are degenerate in voltage space just as S_{000} and S_{111} are degenerate in the state space of the power matrix.

The changes occurring in the phase leg voltages during a hypothetical inverter spanning cycle provide valuable insight into the synthesis problem. Table 1 shows the phase leg level changes associated with the state transitions necessary to implement all of the hypothetical inverter spanning cycles in Ω_{100}. The symbol $\uparrow$ indicates a phase leg transition from the lower rail to the upper rail, $\downarrow$ indicates the opposite case, and $\leftrightarrow$ indicates no transition. The entries shown in brackets are degenerate transitions between the active states and one of the degenerate states of

S_0. The entries shown in braces represent transitions between the degenerate states of S_0, i.e. S_{000} and S_{111}. The latter transitions have the additional property of being unobservable from the load.

TABLE I

PHASE LEG LEVEL TRANSITIONS FOR ALL POSSIBLE STATE CHANGES IN Ω_{100} ASSOCIATED WITH THE HYPOTHETICAL INVERTER OF CHAPTER IV

	Next State			
Present State	S_{100}	S_{110}	S_{111}	S_{000}
S_{100}		$\leftrightarrow\uparrow\leftrightarrow$	$[\leftrightarrow\uparrow\uparrow]$	$[\downarrow\leftrightarrow\leftrightarrow]$
S_{110}	$\leftrightarrow\downarrow\leftrightarrow$		$[\leftrightarrow\leftrightarrow\uparrow]$	$[\downarrow\downarrow\leftrightarrow]$
S_{111}	$[\leftrightarrow\downarrow\downarrow]$	$[\leftrightarrow\leftrightarrow\downarrow]$		$\{\downarrow\downarrow\downarrow\}$
S_{000}	$[\uparrow\leftrightarrow\leftrightarrow]$	$[\uparrow\uparrow\leftrightarrow]$	$\{\uparrow\uparrow\uparrow\}$	

Symbol Legend:

$\uparrow$ - Phase leg transition from the lower rail to the upper rail

$\downarrow$ - Phase leg transition from the upper rail to the lower rail

$\leftrightarrow$ - No phase leg transition

[...] - Degenerate transition between an active state and S_0

{...} - Hidden transition between the internal states of S_0

Inspection of the Table I reveals a prominent pattern that begs for exploitation. For any given state transition in the table, all phase leg level changes are in the same direction, either all up or all down. This suggests that a mechanism capable of smoothly driving a selected set of phase leg voltages from one rail potential to the opposite rail potential would satisfy the state transition requirements necessary to synthesize the hypothetical inverter. Later, this property will be

recognized as a critical factor in the development of the PRAL inverter. For now, it provides additional insight into the synthesis problem. More importantly however, it provides the quintessential clue needed to continue the synthesis process. Namely, it suggests a simple physical system for use in an analogy.

It is often useful to first describe the behavior of a system under development in abstract terms and then search for an existing system with similar behavior. If a suitable analogous system is identified, implementation details of the existing system are often easily mapped to corresponding mechanisms within the system under development. However, the success of the mapping process depends upon the correlation between the two systems and the analyst's ability to correctly map behavioral and implementation details from one problem domain to the other.

Based on the nature of the synthesis problem established so far, a suitable analogous system for the hypothetical inverter is an elevator car that transports occupants of a two-story building between floors. In the analogy, the upper and lower rails of the power matrix correspond to the upper and lower floors of the building, respectively. The phase legs correspond to individual building occupants. The voltage of a given phase leg mimics the vertical coordinate of the corresponding building occupant. The transition of a phase leg voltage between the upper and lower rail potentials correspond to building occupants riding the elevator car between floors. Building occupants are allowed to exit a car only when its vertical position is equal to that of either the upper or the lower floor. Likewise, the voltage of a transitioning phase leg is free to remain at its present potential only when it is equal to either upper or lower rail potential. Occupants of the building may enter a car only when the car's vertical position is equal to that of the floor on which they are presently located. Similarly, a phase leg voltage is allowed to begin a transition between rail potentials only when the voltage of the inverter analog of the elevator car equals that of the rail to which the phase leg is initially connected. Finally, recall from Table I that for any state transition, all transitioning phase leg voltages begin and end at the same rail

potential. This suggests that a single "elevator" mechanism is sufficient for synthesizing the hypothetical inverter voltage space characteristics.

In power electronics terms, the elevator function is implemented by a snubber circuit that constrains the phase leg voltages to transition between the rail potentials in a controlled manner. This provides a mechanism for allowing ample time for devices to fully turn off before the voltage across their terminals rises significantly, thus implementing soft switching. The absence of a snubber circuit to protect against rapid phase leg voltage changes at the beginning of a transition is the elevator analogy equivalent of a passenger stepping into an open elevator shaft.

Two important questions remain regarding the translation of the elevator analogy to a physical realization of the hypothetical inverter. First, what is the electrical equivalent of an elevator car? Secondly, how do phase leg voltages "enter," "ride," and "exit" the inverter analog of the elevator car? To fully answer the second question and partially answer the first, consider the arrangement shown in Figure 36. The structure consists of a standard bridge inverter, such as the one shown in Figure 35, augmented with an auxiliary link. The auxiliary link is connected to each of the inverter phase legs through bilateral switches S_{AS}, S_{BS}, and S_{CS}. When both power matrix switches are open and the bilateral switch is closed in a given phase leg, the auxiliary link governs the respective phase leg voltage, just like an elevator car governs the vertical position of its occupants. Closing the bilateral switch between a given phase leg and the auxiliary link when the potentials of both are equal is comparable to opening the elevator car door to permit a building occupant to enter the car. Closing a power matrix switch when a transitioning phase leg voltage reaches that of a power matrix rail, via the auxiliary link, is equivalent to opening the elevator car door to allow a passenger to exit the car. Opening the bilateral switch in a given phase leg with one of the power matrix switches closed is equivalent to a building occupant being in a position to ride the elevator to the other floor but electing to remain on the present floor. Finally, opening a power matrix switch in a given phase leg with the corresponding bilateral

switch closed is equivalent to an elevator car passenger, who is in a position to either remain in the car or remain on the present floor, electing to travel to the other floor.

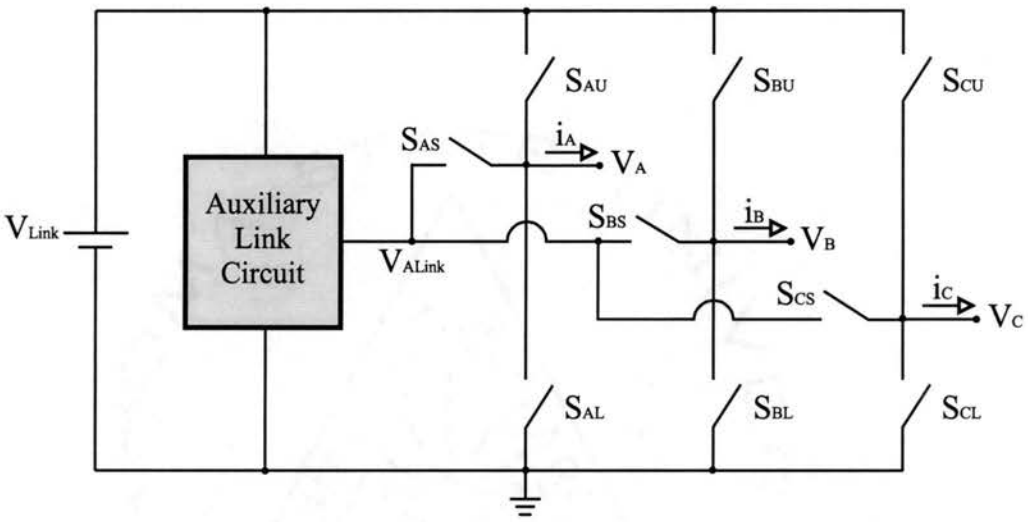


Figure 36. Generic implementation of the hypothetical inverter described in Chapter IV

Each phase leg is always connected to a power matrix rail, the auxiliary link, or both the auxiliary link and a power matrix rail when the auxiliary link potential equals that of a power matrix rail. The two power matrix switches and the auxiliary link bilateral switch in each phase leg are only opened and closed when the potential of the auxiliary link is within a few volts of a power matrix rail potential. Opening one of the bilateral switches when $V_{ALink}(t)$ differs significantly from one of the inverter rail potentials is comparable to a passenger stepping out of an elevator car while it is between floors. That is, the load current tied to the respective phase leg would rapidly drive the phase leg voltage toward one of the inverter rails, violating the requirement for soft switching.

To illustrate the auxiliary link concept in a purely electrical context, consider a transition of phase leg A between the upper and lower rail potentials. Suppose the inverter control system commands $V_A(t)$ to transition from the upper rail potential to the lower rail potential. Let the initial status of the three switches in phase leg A be: S_{AU} = ON, S_{AL} = OFF, S_{AS} = OFF. Using a

mechanism yet to be determined, $V_{Alink}(t)$ is raised to V_{Link}. When $V_{ALink}(t) = V_{Link}$, S_{AS} is turned on. S_{AU} is then turned off and $V_{ALink}(t)$ begins to decrease. The initial rate of decrease in $V_{ALink}(t)$, and thus $V_A(t)$, is sufficiently low to allow S_{AU} to turn off before $V_{Link} - V_{ALink}(t)$ exceeds a few tens of volts, thereby achieving soft switching of S_{AU}. Once $V_{ALink}(t)$ reaches the lower rail potential, S_{AL} is turned on and S_{AS} is turned off, freeing the auxiliary link for the next commanded transition. Since the number of phase legs that can transition together is unrestricted, the previous supposition that only one "elevator" mechanism is required to synthesize the hypothetical inverter is substantiated.

5.3 The Auxiliary Link Circuit

The unanswered question from the previous section is how to implement the auxiliary link drive circuit. A solution that eliminates significant switching losses in all inverter devices, allows full synthesis of the hypothetical inverter characteristics in voltage space, and is both efficient and economical to manufacture is desired. Unfortunately, the infancy of the new inverter class obscures the synthesis process to the point where finding only an approximate solution is of considerable value. This section discusses the relevant issues that preclude finding an exact solution based on the "elevator" analogy and describes the auxiliary link drive circuit used throughout the remainder of this work. It is intended that the knowledge gained from studying this approach will lead to future enhancements that more closely reflect the voltage space characteristics of the hypothetical inverter.

5.3.1 State Transition Delays

Consider again the case of transitions between the states comprising Ω_{100}. Suppose the inverter is in state S_0 (S_{000}) and the control system commands a transition from S_0 to S_{100}. Upon completion of the S_0 (S_{000}) to S_{100} state transition, $V_{ALink}(t) = V_{Link}$. Suppose the control system

then commands a subsequent transition from S_{100} to S_{110} while $V_{ALink}(t)$ is still at the upper rail potential, V_{Link}. In order to begin the S_{100} to S_{110} transition, $V_{ALink}(t)$ must first be lowered from the upper rail potential to the lower rail potential. Since this does not occur instantaneously, a delay is introduced. The delay is the rail-to-rail transition time of the auxiliary link voltage and is physically equivalent to the delay T_t defined in Chapter III.

Fortunately, the preceding characteristic is not manifested in all scenarios. This time suppose the inverter begins in state S_0 (S_{111}). The S_0 to S_{100} transition is accomplished by driving the voltages of phase legs B and C to the lower rail potential, leaving $V_{ALink}(t) = 0$ upon completion. The subsequent commanded transition from S_{100} to S_{110} is now free to begin immediately since $V_{ALink}(t)$ is at the proper potential to carry phase leg B to the upper rail potential. In general however, the auxiliary link voltage could be at either the upper or lower rail potential when the control system issues a transition command. Consequently, the delay between issuance of a transition command and the actual beginning of the transition may contain a latency of T_t seconds, depending on the state of the auxiliary link circuit.

Figure 37 shows the active state to active state transitions that are permitted to occur when the auxiliary link potential is equal to a specific inverter rail potential. The arrows labeled with either a U (Upper rail potential) or an L (Lower rail potential) indicate the required potential of $V_{ALink}(t)$ at the beginning of the state transition. For example, a transition from S_{100} to either S_{110} or S_{101} is possible if and only if $V_{ALink}(t)$ is equal to the lower rail potential (L). However, transitions between any active state and the zero state are allowed any time $V_{ALink}(t)$ is equal to either of the two rail potentials.

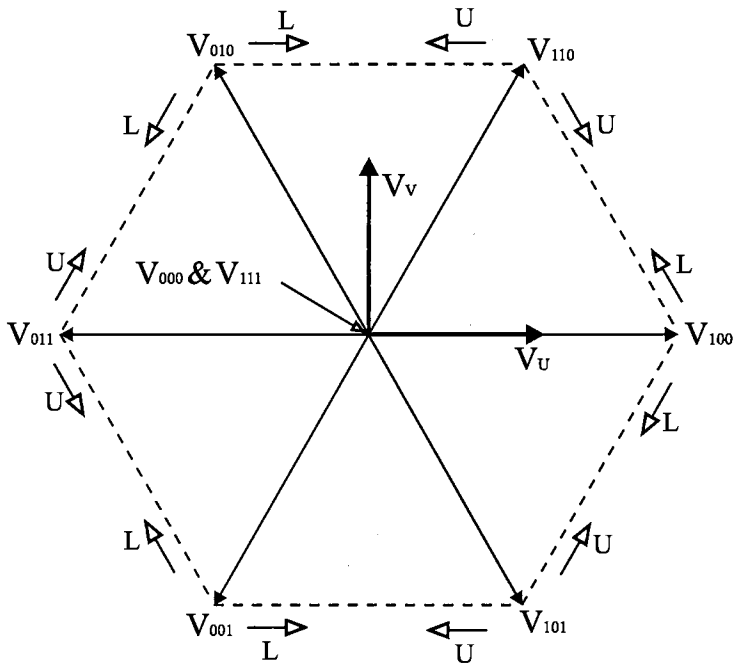


Figure 37. Voltage space diagram showing the auxiliary link potential required for transitions between neighboring active states

5.3.2 Discrete Spanning Cycle Mean Voltages

It is now necessary to consider tradeoffs between fully realizing the state transition characteristics of the hypothetical inverter and designing a practical drive circuit for the auxiliary link. The arguments toward the end of Chapter IV discouraged employing active devices directly inside tank circuit loops. However, all SPRDL designs reported in the literature employ this very practice, suggesting that synchronized control of the state transition time may only be achievable with active devices in the resonant circuit loop.

Recall from Chapter II that the evolution of the resonant link topology resulted from several significant advances that were all, to differing degrees, based on alleviating structural shortcomings of previous designs. Therefore, it is not unreasonable to develop the initial member of the auxiliary link inverter class using an unsynchronized design, thus allowing adherence to the resonant circuit configuration guidelines of Chapter IV. Careful study of a viable

unsynchronized auxiliary link inverter may provide the additional insight needed to develop a practical synchronized version. However, the possibility also exists, as was discussed in Chapter IV, that the spectral performance benefits of precisely controlling the switching events may not justify the potential economic, efficiency, and reliability costs.

Clearly, an unsynchronized design conceptually constitutes a significant departure from the voltage space properties of the hypothetical inverter. The net effect is discrete spanning cycle mean voltages in **H** as opposed to a continuum. It is worth noting, however, that the spanning cycle frequency corresponding to each discrete spanning cycle mean voltage is identical to that of the hypothetical inverter for the same mean voltage. Figure 38 shows the locations of the discrete spanning cycle mean voltages in Ω_{100}. The discrete voltages are dense near the boundaries of Ω_{100} but are sparse in the central region. For the case of rated voltage operation shown in the figure, the synthesized three-phase voltage trajectory lies largely within a high-density region of discrete

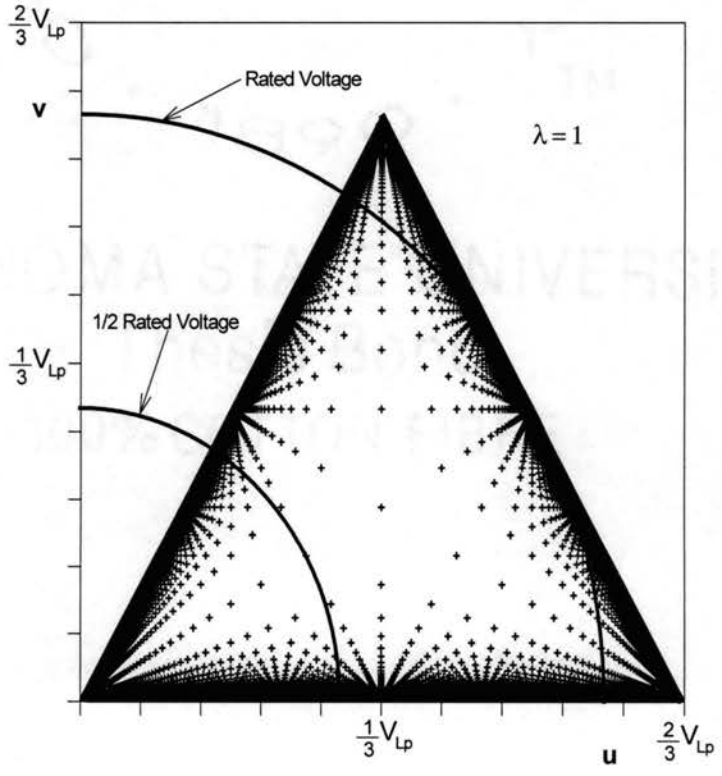


Figure 38. Discrete spanning cycle mean voltages in Ω_{100} resulting from utilization of an unsynchronized auxiliary link drive circuit

mean voltages. The ½ rated voltage trajectory traverses a region of Ω_{100} that is considerably less dense.

The potential detrimental effects of discrete spanning cycle mean voltages in **H**, particularly in the central regions of each Ω_i, $i \in \mathbf{S}^{*-}$, may be less serious than they may appear. The spanning cycles corresponding to the mean voltages lying near the boundaries of each Ω_i have a relatively long period compared to those corresponding to voltages lying near the center. Chapter IV described the potential low frequency spectral performance benefits of replacing a long period spanning cycle with an equivalent ensemble of shorter duration spanning and primitive cycles. This suggests that the long period spanning cycles whose mean voltages already lie in the high-density region could be replaced with cycle ensembles. The replacement has the potential of improving the spectral performance but more importantly, it increases the effective density of mean voltages near the boundaries of each Ω_i. Given that the spanning cycle mean voltages are already dense in these regions, the effects of discrete mean voltages may be negligible there.

The use of cycle ensembles to synthesize voltages in the central region of each Ω_i is clearly necessary due to the large distance between the available mean voltages. However, the spanning cycles associated with this region have much shorter periods than those corresponding to the regions near the boundaries of each Ω_i. For spanning cycles with mean voltages lying in the central regions of each Ω_i, the times spent in the three states defining a given Ω_i differ by a factor of about three or four, at most. Thus, there is no reason for a cycle ensemble to consecutively occupy a single state for more than three or four auxiliary link half-cycles. If two states are occupied for four half-cycles and the third is occupied for one half-cycle, the spanning cycle period will be less than five auxiliary link periods. It is conceivable then that most of the distortion in the synthesized waveform will occur at frequencies greater than approximately one fifth of the auxiliary link frequency. Consequently, the low density of discrete mean voltages in

the central regions of each Ω_i may not significantly affect the low frequency spectral quality of the synthesized waveform.

The true spectral performance penalty for using a design with discrete spanning cycle mean voltages is unclear. However, the preceding arguments suggest that the low frequency degradation may be modest. Conceptually, the general behavior of both the hypothetical and the auxiliary link inverters could be compared through simulation in order to study the effects of discrete spanning cycle mean voltages on the spectral performance characteristics. Unfortunately, the effects of the different control strategies required for synchronized and unsynchronized designs are not easily separated from the effects of continuous and discrete spanning cycle mean voltages. Any potential quantitative answer to this question is therefore deferred to future efforts that will likely have the benefit of an established knowledge base.

5.5.3 Implementation and Operation of the Auxiliary Link Drive Circuit

Despite the potential shortcomings identified in the previous two sections, the design selected for study throughout the remainder of this work is the unsynchronized auxiliary link inverter shown in Figure 39. The parallel resonant circuit in the figure suggests the name "Parallel Resonant Auxiliary Link" (PRAL) inverter. The structure is devoid of active devices directly in series with the main tank loop. In practice, the voltage divider used to anchor the left end of the tank would be implemented with capacitors in place of the voltage sources shown in the figure. Regulation of the voltage divider capacitor voltage is an integral part of the control system and is addressed in the next chapter.

The general PRAL inverter operating principle is illustrated with the following example. Suppose the power matrix is in state S_{010} and $V_{ALink}(t)$ is positive decreasing. Until $V_{ALink}(t)$ reaches the lower rail potential, switches S_{AL}, S_{BU}, and S_{CL} are on and all other power matrix and auxiliary link switches are off. Also, suppose that the control system has commanded a transition

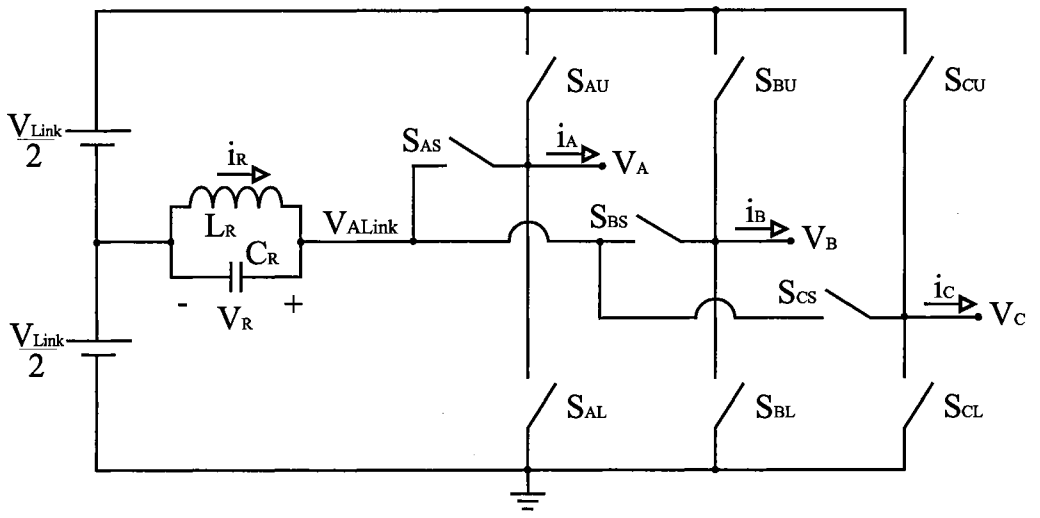


Figure 39. Schematic diagram of a PRAL inverter using a simple free running tank circuit to drive the auxiliary link

to S_{110}. Once $V_{ALink}(t)$ reaches zero, S_{AS} is turned on. Both S_{AS} and S_{AL} remain on until $i_R > i_A + I_{Boost}$, where I_{Boost} is a positive variable representing the "boost" current required to overcome potential load current changes and parasitic losses during transitions between the lower to upper rails. Once i_R satisfies the inequality, turn-off of S_{AL} is initiated. $V_{ALink}(t)$ then begins to rise slowly with $V_A(t)$ constrained to follow along to within the conduction voltage drop of S_{AS}. Since the switching action occurs at the voltage crest of the resonant circuit, as prescribed in Chapter IV, the voltage across S_{AL} is minimized throughout its turn-off period. When $V_{ALink}(t)$ reaches V_{Link}, S_{AU} is turned on, preventing any residual positive current in L_R from driving $V_{ALink}(t)$ above V_{Link}. If one or more subsequent phase leg transitions from the upper to the lower rail is required at this point, a similar scenario is exercised to drive the selected phase legs to the lower rail potential. If no power matrix state transition is commanded, S_{AS} is turned off when $i_R < - I_{Boost}$, allowing the auxiliary link to transition to the lower rail. The boost current, I_{Boost}, in this case is again positive but need only be sufficient to compensate for parasitic losses in the tank circuit.

A special case exists when the power matrix enters S_0 and is commanded to remain there for at least one half of an auxiliary link cycle. Suppose a transition from S_{100} to S_0 (S_{000}) has just

completed and $V_{ALink}(t) = 0$. Further, suppose the control system commands the power matrix to remain in S_0. The control system command is satisfied if all three phase legs remain connected to the lower rail and the auxiliary link is allowed to transition to the upper rail potential. There is no problem initializing L_R with adequate "boost" energy to ensure that $V_{ALink}(t)$ reaches V_{Link}. However, once $V_{ALink}(t)$ reaches V_{Link}, none of the upper power matrix or auxiliary link bilateral switches can be turned on to supply boost energy to L_R for the return journey to the lower rail potential. The problem is relatively minor since the quality factor, Q, typically quoted for the tank circuits used in PRDL designs is on the order of 100-150. Since the value of Q can be made so large, $V_{ALink}(t)$ should always return to within a few volts of the lower rail potential. Consequently, it would likely be acceptable to turn on the auxiliary link bilateral switches once $V_{ALink}(t)$ reached its minimum value. This would compensate for parasitic losses that may otherwise preclude a complete transition to the lower rail potential. However, the switch closure would occur across the drive circuit capacitor C_R and could thus result in substantial surge currents flowing in the auxiliary link and lower power matrix switches until $V_{ALink}(t)$ reached the lower rail potential. A similar condition exists when the roles of the upper and lower rails are reversed. An additional flaw in this strategy is that a potential delay is introduced for transitions between active states and S_0. The mechanism is identical to that described earlier for the case of transitions between active states and results in the same potential transition latency, T_t.

An alternative approach is to exploit the degeneracy of S_0. Under this strategy, the zero state presented to the load would result from all three auxiliary link switches being turned on to allow all of the load currents to circulate through the auxiliary link bus. From the perspective of the tank circuit, the auxiliary link would appear to be disconnected from the load. From the perspective of the load, the power matrix would be in state S_0 as the control system commanded. With this arrangement, the power matrix switches can be used to initialize L_R with the necessary boost energy each time the auxiliary link voltage reaches either rail potential. Additionally, this

approach poises the auxiliary link to execute a power matrix state transition to an active state every time V_{ALink} equals one of the rail potentials, eliminating the possible unnecessary latency associated with the former approach.

5.4 Auxiliary Link Inverter Control Logic

The previous section described the general operating principles of the PRAL inverter class. This section addresses the PRAL inverter control requirements in terms of the events and control actions that are common to all auxiliary link inverter designs, regardless of the auxiliary link drive circuitry and load control strategy employed. The inverter control system serves a dual role. First, it determines the appropriate state changes required under the given load control strategy. Second, it must respond to internal inverter events according to the logic structure innate to the auxiliary link inverter. Like resonant link inverters, the auxiliary link inverter is a state machine. The events that trigger control actions are derived from the auxiliary link voltage $V_{ALink}(t)$, the resonant circuit inductor current $i_R(t)$, the load phase currents $i_A(t)$, $i_B(t)$, and $i_C(t)$, and the commanded power matrix state. The closing and opening of the power matrix and auxiliary link switches constitute the resulting control actions.

Figure 40 shows the control flow diagram for phase leg j, $j \in \{A, B, C\}$, of an auxiliary link inverter. The control flow diagrams for all other phase legs of the inverter are identical. The events that trigger control actions in each phase leg are based on global inverter state variables and are therefore common to all phase legs. These events occur when the conditions in the shaded decision blocks are satisfied. The non-shaded blocks correspond to logical decisions or control actions taken by the inverter control system. The circles containing the three bit binary numbers are the states of the phase leg switches S_{jU}, S_{jS}, and S_{jL}. The state label is of the form $\boldsymbol{S}_{jU}\boldsymbol{S}_{jS}\boldsymbol{S}_{jL}$ where $\boldsymbol{S}_{jU}, \boldsymbol{S}_{jS}$, and $\boldsymbol{S}_{jL} \in \{0, 1\}$ with 0 and 1 indicating that the switch is off or on, respectively. For example, the phase leg state $\boldsymbol{S}_{jU}\boldsymbol{S}_{jS}\boldsymbol{S}_{jL} = 110$ corresponds to the conduction

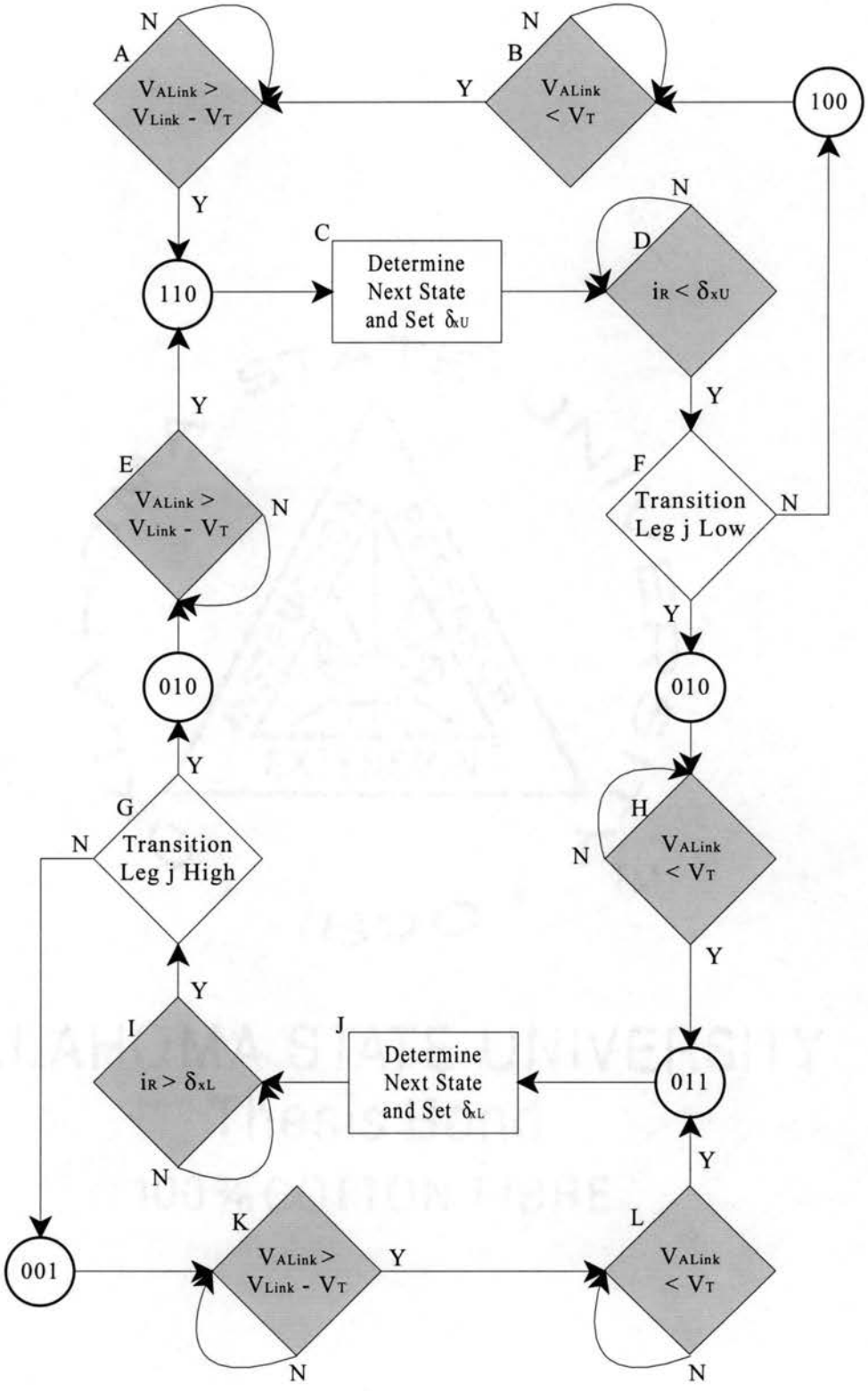


Figure 40. Control flow diagram for phase leg j of an auxiliary link inverter

status of the switches in phase leg j being: switch S_{jU} is on, switch S_{jS} is on, and switch S_{jL} is off. Blocks **C** and **J** represent the control system's role in determining the next state of the power matrix whenever the auxiliary link is at one of the rail potentials. The values of δ_{xU} and δ_{xL} depicted in these blocks depend on the load currents of the phase legs that are commanded to transition to the opposite rail. They also depend on the boost current, I_{Boost}, required to ensure that the auxiliary link completes the transition.

The shaded decision blocks inhibit phase leg state transitions until their respective conditions are satisfied. Since the conditions tested in the blocks are common to all phase legs, the phase leg state machines are synchronized. Although the specific blocks inhibiting phase leg transitions in an inverter are not necessarily at the same location in each phase leg control flow diagram, the condition they are testing is always the same. For example, a given inverter phase leg wait in either block **B**, **H**, or **L** for the condition $V_{ALink}(t) < V_T$ to be satisfied. Blocks **B**, **H**, and **L** mark the event of $V_{ALink}(t)$ falling below a small threshold voltage, V_T, as it approaches the lower rail. Reasonable values for V_T are in the range of 0-10 volts, depending on the resonant circuit frequency and the turn-on delay associated with the switches. If either S_{jL} or S_{jS} is on when $V_{ALink}(t)$ falls below V_T, the other is turned on. This ties the auxiliary link to the lower rail so that $i_R(t)$ can be initialized for the upcoming transition of $V_{ALink}(t)$ to the upper rail potential. However, if S_{jU} is turned on (phase leg state 100), no phase leg state transition occurs. Blocks **A**, **E**, and **K** serve a similar role in initializing $i_R(t)$ when $V_{ALink}(t)$ rises above $V_{Link} - V_T$. Blocks **D** and **I** cause the auxiliary link to remain connected to the upper and lower rails, respectively, until $i_R(t)$ is properly initialized for the auxiliary link transition to the opposite rail. Blocks **F** and **G** depend on the power matrix state transition decision made in blocks **C** and **J**, respectively, but are not directly event driven and are therefore shown without shading.

5.5 PRAL Inverter Modes and Governing Equations

5.5.1 Modeling Approach

5.5.1.1 Operational Modes The PRAL structural configuration takes on two fundamentally different forms over the course of an auxiliary link cycle. The first form exists when the auxiliary link is connected or "latched" to one of the power matrix rails. The second exists when the auxiliary link voltage is transitioning between the power matrix rail potentials. It is convenient to analyze the PRAL inverter circuit according to the structural configuration existing at a given instant, or more appropriately, the prevailing operational mode. The PRAL inverter operational modes fall into two distinct categories. Let "latched mode" or L mode denote the case in which the auxiliary link is connected to one of the power matrix rails through the power matrix and auxiliary link bilateral switches. Similarly, let "transitional mode" or T mode represent the case where the auxiliary link voltage is transitioning between the upper and lower rail potentials. It is useful to further subdivide the L mode based on the rail potential to which the auxiliary link is connected and the T mode based upon the rail to which it will next connect. Let the following symbols identify the four possible PRAL inverter operational modes.

L_U – Latched Mode (Upper Rail): $V_{ALink}(t) = V_{Link}$

L_L – Fixed Mode (Lower Rail): $V_{ALink}(t) = 0$

T_U – Transitional Mode (Upper Rail): $V_{ALink}(t) \in (0, V_{Link})$ and $V_{ALink}(t)$ increasing

T_L – Transitional Mode (Lower Rail): $V_{ALink}(t) \in (0, V_{Link})$ and $V_{ALink}(t)$ decreasing

5.5.1.2 Model Partitioning and Related Considerations The base circuit model used to develop the PRAL inverter governing equations is shown in Figure 41. Inspection of the figure shows that the source, inverter, and load can easily be partitioned into three separate entities. Both the source and load appear to the inverter as controlled current sources. This approach makes it possible to separate the state variable models that describe the source, inverter, and load. Partitioning permits different source and load configurations to be integrated into simulation models without modification of the inverter model.

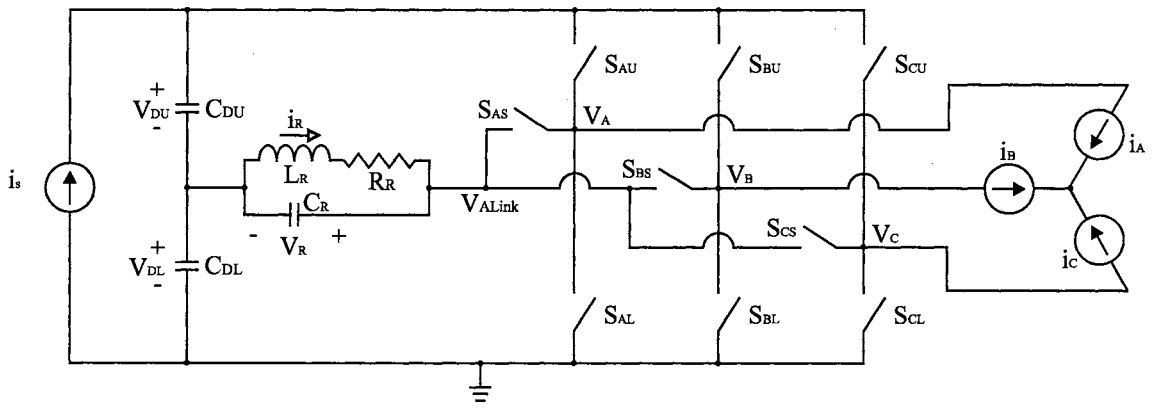


Figure 41. Schematic diagram of the circuit model used to develop the PRAL inverter governing differential equations

Figure 41 shows a realistic implementation of the voltage divider used to bias the auxiliary link resonant circuit. Capacitors C_{DU} and C_{DL} replace the constant voltage sources previously depicted. The inverter control system adjusts the boost current, I_{Boost}, to regulate the charge in C_{DU} and C_{DL} so that the potential of their common node remains approximately midway between the upper and lower rail potentials. Losses in the auxiliary link resonant circuit are assumed to occur primarily in the inductor, L_R, and are modeled using the series resistance, R_R, shown in the figure. The model incorporates a pseudo-ideal switch model to account for the effects of switch turn-off currents on the output waveforms and to estimate switching losses. This is accomplished by constructing the inverter circuit modeling based on "ideal" power matrix and auxiliary link

switches, as per the governing differential equations developed in Chapter V, and then adding controlled current sources to emulate the switch turn-off currents that would exist in a physical inverter. The resulting switch model is thus pseudo-ideal in that it has no forward or reverse voltage drop and turns on instantaneously but mimics a real switch in that its forward conduction current does not instantaneously fall to zero when it is commanded to turn off.

A second type of partitioning is applied to the PRAL inverter operational modes to simplify the state variable modeling process. A single model is developed for both the T_U and T_L modes while separate, but symmetrical, models are developed for the L_U and L_L modes. Since the load and source are modeled separately from the inverter, a single model for each is applicable to all four inverter operational modes. Finally, partitioning the model according to the operational modes has the additional advantage of limiting the consideration of switch turn-off currents to the transitional mode model.

5.5.2 Three-Wire Three-Phase Load Model

The partitioning scheme employed to separate the inverter and load models was designed to allow a single load model to be used for all four inverter modes. Just as the inverter model views the load as a set of controlled current sources, the load sees the inverter as a set of controlled voltage sources. This approach eliminates the need to develop separate models for each possible combination of load phase connections to the auxiliary link and power matrix rails. The arrangement is easily extended to accommodate multiple three-wire three-phase loads connected to a single auxiliary link and a single pair of power matrix rails. This is particularly convenient for studying three-phase to three-phase conversion applications in which one of the modeled loads is actually a three-phase source.

The general three-phase load model shown in Figure 42 is appropriate for both three-wire three-phase machines and transformers. The back EMF in each phase is modeled using an

independently controlled voltage source $E_k(t)$, $k \in \{A, B, C\}$. The voltage sources $V_k(t)$, $k \in \{A, B, C\}$, represent the inverter phase leg voltages presented to the load.

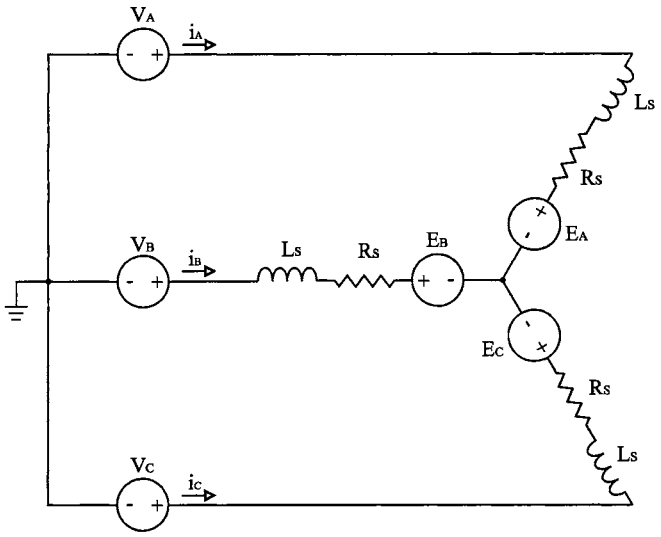


Figure 42. Schematic diagram of the three-wire three-phase load model

The governing differential equations for the load model are developed in the following analysis, which is initiated by writing the mesh equations for the circuit in Figure 42.

$$V_A - L_s\frac{di_A}{dt} - R_s i_A - E_A + E_B + R_s i_B + L_s\frac{di_B}{dt} - V_B = 0 \qquad 5.5.2.1$$

$$V_A - L_s\frac{di_A}{dt} - R_s i_A - E_A + E_C + R_s i_C + L_s\frac{di_C}{dt} - V_C = 0 \qquad 5.5.2.2$$

Since the phase currents must sum to zero, i_C can be factored out using,

$$i_C = -(i_A + i_B) \qquad 5.5.2.3$$

Next, use 5.5.2.3 in 5.5.2.1 and 5.5.2.2 to solve for $\frac{di_A}{dt}$ and $\frac{di_B}{dt}$.

$$\frac{di_A}{dt} = \frac{1}{3L_s}(2V_A - V_B - V_C - 2E_A + E_B + E_C - 3R_s i_A) \qquad 5.5.2.4$$

$$\frac{di_B}{dt} = \frac{1}{3L_s}(2V_B - V_A - V_C - 2E_B + E_A + E_C - 3R_s i_B) \qquad 5.5.2.5$$

In order to assign the proper value to the inverter phase leg voltages V_k, $k \in \{A, B, C\}$, adopt the following notation to represent the state of the inverter phase legs.

$$\xi_k = \begin{cases} U & \text{iff phase leg k is connected to the upper power matrix rail through switch } S_{kU} \\ L & \text{iff phase leg k is connected to the lower power matrix rail through switch } S_{kL} \\ S & \text{otherwise (phase leg k is connected to the auxiliary link and is transitioning between rails)} \end{cases}$$

Let $\delta_{i,j}$ be the Kronecker delta function given by,

$$\delta_{i,j} = \begin{cases} 1 & i = j \\ 0 & \text{otherwise} \end{cases}$$

Using the above notation, the voltages of the externally controlled voltage sources feeding the load model can be expressed in terms of the inverter phase leg switch states as,

$$V_k = (v_{DU}(t) + v_{DL}(t))\delta_{\xi_k,U} + (v_{DL}(t) + v_R(t))\delta_{\xi_k,S} \quad k \in \{A,B,C\} \qquad 5.5.2.6$$

5.5.3 Latched Modes: L_U and L_L

5.5.3.1 The L_U Mode Figure 43 shows an equivalent circuit for the L_U mode in which both switches S_{kU} and S_{kS} are turned on for at least one k, $k \in \{A, B, C\}$. Since the load is effectively connected to only the upper and lower power matrix rails in this mode, it is modeled using a single current source, $i_S(t)$, flowing from the upper rail to the lower rail. The equivalent load current, $i_{EL}(t)$, is modeled as a controlled current source that depends on the states of the power matrix switches and the load phase currents. Using the definitions of Subsection 5.5.2, the equivalent load current can be expressed as,

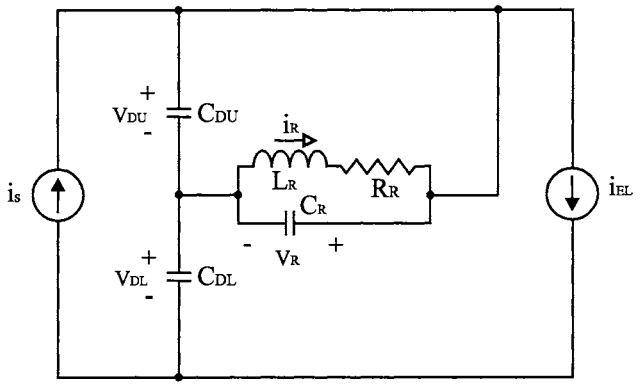


Figure 43. Equivalent PRAL inverter circuit model for the L_U mode

$$i_{EL} = \sum_{k\in\{A,B,C\}} i_k \delta_{\xi_k,U} \qquad 5.5.3.1.1$$

The circuit diagram can be further simplified by combining the upper auxiliary link voltage divider capacitor, C_{DU}, with the resonant circuit capacitor, C_R, and by combining the two current sources, $i_S(t)$ and $i_{EL}(t)$. The resulting simplified equivalent circuit is shown in Figure 44.

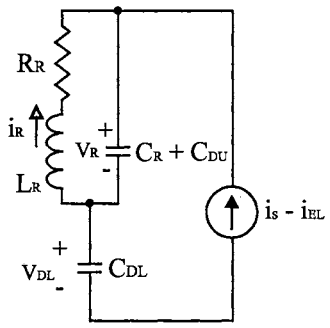


Figure 44. Schematic diagram of the simplified L_U mode equivalent circuit

The governing differential equations for the L_U mode model shown in Figure 44 are,

$$\frac{dV_{DL}}{dt} = \frac{1}{C_{DL}}(i_s - i_{EL}) \qquad 5.5.3.1.2$$

$$\frac{dV_R}{dt} = \frac{1}{C_{DU} + C_R}(i_R + i_s - i_{EL}) \qquad 5.5.3.1.3$$

$$\frac{di_R}{dt} = \frac{-1}{L_R}(i_R R_R + V_R) \qquad 5.5.3.1.4$$

The voltage across the upper auxiliary link voltage divider capacitor, C_{DU}, is the same as that of the resonant capacitor, C_R. Consequently, $v_{DU}(t) = v_R(t)$ in the L_U mode.

Next, consider the special, but important, case where the source holds the power matrix rail-to-rail voltage constant. Such a condition approximately exists in practice for applications with large filter capacitors shunting the source. This case is easily handled without developing an additional model by noting that for constant rail-to-rail voltage,

$$\frac{dv_{DL}}{dt} + \frac{dv_R}{dt} = 0 \qquad 5.5.3.1.5$$

Using 5.5.3.1.5 to eliminate $i_S(t)$ and $i_{EL}(t)$ from 5.5.3.1.2 and 5.5.3.1.3 yields,

$$\frac{dv_{DL}}{dt} = -\frac{i_R}{C_R + C_{DU} + C_{DL}} \qquad 5.5.3.1.6$$

$$\frac{dv_R}{dt} = \frac{i_R}{C_R + C_{DU} + C_{DL}} \qquad 5.5.3.1.7$$

The expression for $\frac{di_R(t)}{dt}$ remains the same as given in 5.5.3.1.4.

5.5.3.2 The L_L Mode By symmetry, the equivalent circuit for the L_L mode is sufficiently similar to that of the L_U mode that only the equivalent circuit and governing equations are presented. Figure 45 shows the simplified equivalent circuit in which the auxiliary link is connected to the lower rail. The model for the equivalent load current between the upper and lower rails is identical to that used for the L_U mode. The expression for $i_{EL}(t)$ remains the same as given in 5.5.3.1.1

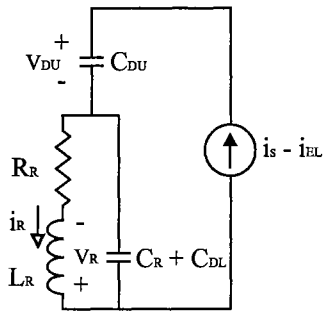


Figure 45. Schematic diagram of the L_L mode equivalent circuit

The governing differential equations for the most general case of the L_L mode are,

$$\frac{dv_{DU}}{dt} = \frac{1}{C_{DU}}(i_s - i_{EL}) \qquad 5.5.3.2.1$$

$$\frac{dv_R}{dt} = \frac{1}{C_R + C_{DL}}(i_R + i_{EL} - i_s) \qquad 5.5.3.2.2$$

$$\frac{di_R}{dt} = \frac{-1}{L_R}(i_R R_R + v_R) \qquad 5.5.3.2.3$$

As before, consider the special case where the source holds the power matrix rail-to-rail voltage constant. Noting that $v_{DL}(t) = -v_R(t)$ for the L_L mode leads to,

$$\frac{dv_{DU}}{dt} - \frac{dv_R}{dt} = 0 \qquad 5.5.3.2.4$$

Using 5.5.3.2.4 in 5.5.3.2.1 and 5.5.3.2.2 to eliminate $i_S(t)$ and $i_{EL}(t)$ yields,

$$\frac{dv_{DU}}{dt} = \frac{i_R}{C_R + C_{DU} + C_{DL}} \qquad 5.5.3.2.5$$

$$\frac{dv_R}{dt} = \frac{i_R}{C_R + C_{DU} + C_{DL}} \qquad 5.5.3.2.6$$

The expression for $\frac{di_R(t)}{dt}$ remains the same as given in 5.5.3.2.3.

5.5.4 Transition Modes

The PRAL inverter transitional modes are modeled using the single equivalent circuit shown in Figure 46. The left-hand section is identical to that of Figure 41 but the load and switches have been replaced by four controlled current sources. The two controlled current sources $i_{UEL}(t)$ and $i_{LEL}(t)$ represent the total load phase currents conducted through the upper and low power matrix rails, respectively. The sum of these two currents pass through the load and then into the auxiliary link, via one or more of the bilateral switches. T_U and T_L mode switch turn-off currents are represented by the controlled current sources $i_{UTO}(t)$ and $i_{LTO}(t)$, respectively. Including both $i_{UTO}(t)$ and $i_{LTO}(t)$ in the transitional mode circuit model results in a single set of governing differential equations for both the T_U and T_L modes.

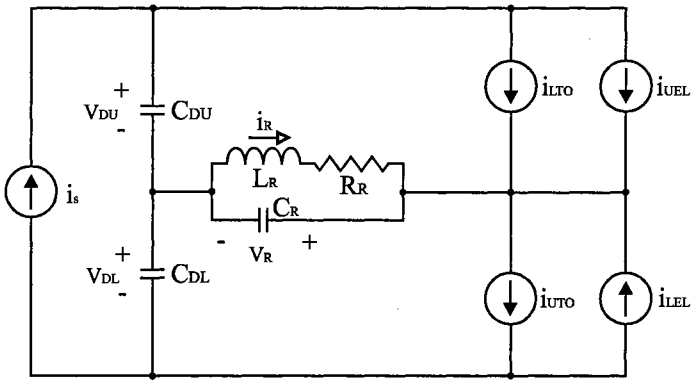


Figure 46. Schematic diagram of the equivalent circuit used to model both the T_U and T_L modes of the PRAL inverter

The objectives of including turn-off currents in the transitional mode circuit model are to incorporate the first order effects of the resulting auxiliary link transition delay on the inverter output waveforms and to establish a mechanism for estimating switching losses. The arrangement shown in Figure 46 lacks sufficient detail to estimate switching loss in individual devices but does provide a means of estimating the total instantaneous switching loss in the inverter. The orientation of both $i_{UTO}(t)$ and $i_{LTO}(t)$ is consistent with that of the turn-off currents associated

with the self-extinguishing devices forming the switches. Turn-off currents associated with the inverse-parallel diodes shunting the self-extinguishing devices are not considered. This substantially simplifies the circuit model and is justified by the fact that the turn-off time of a modern switching diode is roughly one order of magnitude less than that of a comparable self-extinguishing device, such a an IGBT.

Using the notation introduced in Subsection 5.5.2, the equivalent load currents leaving the upper and lower power matrix rails are,

$$i_{UEL} = \sum_{k\in\{A,B,C\}} i_k \delta_{\xi_k,U} \qquad 5.5.4.1$$

$$i_{LEL} = \sum_{k\in\{A,B,C\}} i_k \delta_{\xi_k,L} \qquad 5.5.4.2$$

The resulting governing differential equations for both the T_U and T_L modes are,

$$\frac{dv_{DU}}{dt} = \frac{1}{C_{DU}}(i_s - i_{LTO} - i_{UEL}) \qquad 5.5.4.3$$

$$\frac{dv_{DL}}{dt} = \frac{1}{C_{DL}}(i_{LEL} + i_s - i_{UTO}) \qquad 5.5.4.4$$

$$\frac{dv_R}{dt} = \frac{1}{C_R}(i_R + i_{LTO} + i_{UEL} + i_{LEL} - i_{UTO}) \qquad 5.5.4.5$$

$$\frac{di_R}{dt} = \frac{-1}{L_R}(i_R R_R + v_R) \qquad 5.5.4.6$$

As with the L_U and L_L modes, consider the case where $i_S(t)$ is controlled so that the power matrix rail-to-rail voltage is maintained constant. Clearly then,

$$\frac{dv_{DU}}{dt} + \frac{dv_{DL}}{dt} = 0 \qquad 5.5.4.7$$

Using 5.5.4.7 to eliminate $i_S(t)$ from 5.5.4.3 and 5.5.4.4 results in,

$$\frac{dv_{DU}}{dt} = \frac{1}{C_{DU} + C_{DL}}(i_{UTO} - i_{LTO} - i_{UEL} - i_{LEL}) \qquad 5.5.4.8$$

$$\frac{dv_{DL}}{dt} = \frac{1}{C_{DU} + C_{DL}}(i_{LEL} + i_{UEL} + i_{LTO} - i_{UTO}) \qquad 5.5.4.9$$

Equations 5.5.4.5 and 5.5.4.6 remain applicable for this special case, where $i_S(t)$ maintains the power matrix rail voltage at a constant potential.

5.6 PRAL Inverter Implementation Issues

5.6.1 Switch Implementation

The generalized schematic diagram shown in Figure 39 illustrates the basic topological structure of the PRAL inverter but does not provide the rudimentary design details necessary for physical implementation. The six power matrix switches S_{kU} and S_{kL}, $k \in \{A, B, C\}$, are only required to provide unidirectional current blocking capability. The three bilateral switches S_{kS}, $k \in \{A, B, C\}$, connecting the auxiliary link to the individual phase legs are required to block and conduct current in either direction. The requirements on the six power matrix switches can be satisfied using single BJT's, IGBT's, GTO's, etc, with inverse-parallel diodes placed in shunt to provide the conduction path in the uncontrolled current direction. However, the bilateral switches are not as straight forward in that several bilateral switch configurations are commonly used. The appropriate configuration depends on application specific constraints such as desired inverter efficiency, cost limitations, weight restrictions, availability of devices with the necessary voltage and current ratings, etc.

Figures 47 and 48 show two popular bilateral switch configurations. The bilateral switch in Figure 47 uses a single self-extinguishing device to short circuit the dc terminals of a standard full-wave bridge rectifier. The control gate, G_1, is used to "open" and "close" the path between the switch terminals T_1 and T_2. The configuration in Figure 48 employs two unilateral self-extinguishing devices in an inverse-parallel arrangement. The diode in series with each unilateral switch blocks reverse conduction through the inverse-parallel diode that exists naturally within most self-extinguishing devices. In this case, two control gates, G_1 and G_2, are used to enable or block current conduction between terminals T_1 to T_2.

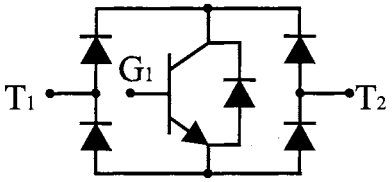


Figure 47. Schematic diagram of a bilateral switch implemented with a single self-extinguishing device

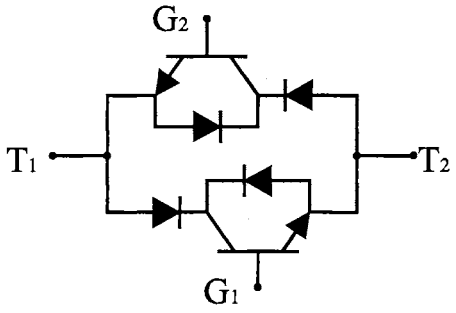


Figure 48. Schematic diagram of a bilateral switch implemented with two self-extinguishing devices

The configuration in Figure 47 requires one self-extinguishing device and four diodes while the configuration in Figure 48 requires two self-extinguishing devices and two diodes. Since self-extinguishing devices and the associated gate drive circuitry typically cost several times more than diodes with similar voltage and current ratings, the configuration shown in Figure 47 has the

advantages of lower cost and reduced circuit complexity. Conversely, the configuration shown in Figure 48 has the advantage of only one diode voltage drop in the conduction path compared to two diode voltage drops in the single switch configuration. For efficiency-critical applications, the elimination of one diode drop in the conduction path gives the dual switch implementation a distinct advantage. However, the single switch configuration is used throughout the remainder of this study in order to focus on the PRAL inverter configuration that is most economically competitive with PRDL inverter designs.

5.6.2 Auxiliary Link Clamping Diodes

Figure 49 shows the schematic diagram of the PRAL inverter implementation used throughout the remainder of this work. The figure is consistent with the previous PRAL inverter schematic diagram with the exception of diodes D_{CU} and D_{CL}. Diodes D_{CU} and D_{CL} prevent any boost current remaining in L_R at the end of an auxiliary link transition from driving $v_{ALink}(t)$ significantly above or below the upper and lower rail potentials, respectively. Allowing $v_{ALink}(t)$ to exceed the rail potentials would raise the voltage stress on the switches, thwarting the low

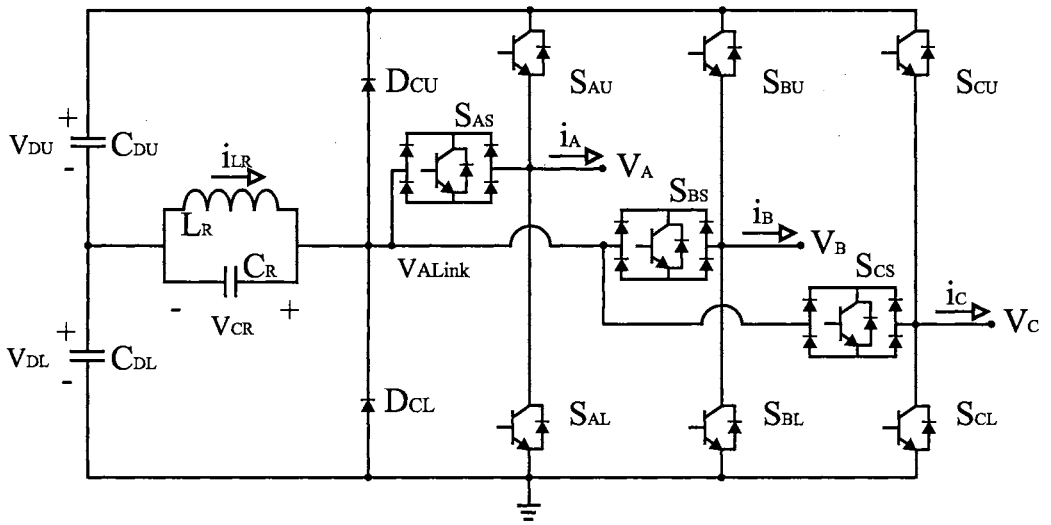


Figure 49. Schematic diagram of PRAL inverter implemented with single device bilateral switches composed of single self-extinguishing devices

voltage stress objective underlying the PRAL concept. Earlier discussions suggested that the power matrix and auxiliary link switches are precisely controlled to turn on at precisely the right time necessary achieve this function. Adding the two clamping diodes is a more practical approach that negates the need for ultra-high speed voltage sensors and precise gate drive circuitry. It also adds robustness to the design by providing a mechanism to prevent destructive over-voltage conditions in case of a control system fault.

5.6.3 Resonant Circuit Configuration

Most resonant link inverter designs place the resonant circuit capacitors between the free end of the resonant circuit inductor and either one or both terminals of the voltage source feeding the inverter. This places the voltage source inside the resonant circuit loop. Voltage sources used to feed inverters are normally formed from a high capacitance electrolytic capacitor fed from some form of current source. Electrolytic capacitors have substantial series resistance at frequencies in the range of those associated with the current circulating through PRDL resonant circuits. The result is reduced resonant circuit efficiency and added RMS current loading of the electrolytic capacitor. These effects are avoided in the PRAL inverter implementation shown in Figure 49 since the resonant capacitor is placed directly in shunt with the resonant circuit inductor. This eliminates the inverter voltage source from the resonant circuit loop.

5.7 Device Current Stress

5.7.1 General Approach and Definitions

The equivalence of the PRAL device voltage stress to that of a conventional hard-switched bridge inverter is well established at this point. However, the issue of device current stress remains unexplored. A precise study of this issue ultimately requires experimentation or highly detailed modeling and simulation, both of which are beyond the scope of the preliminary

development effort presented in this work. However, meaningful estimates of the device current stress are attainable by considering the forward voltage drop that occurs across conducting devices.

The addition of conduction voltage drops to the circuit model leaves the distinction between the inverter transitional and fixed modes fuzzy when $v_{ALink}(t)$ is near one of the power matrix rail potentials. To clarify the beginning and ending points of each mode, further definition is required. Define the T_U mode to end when $v_{ALink}(t)$ and all transitioning phase leg voltages have reached their peak potential above the lower power matrix rail. Define the L_U mode to end once turn-off is initiated in each upper power matrix and auxiliary link bilateral switch that would prevent $v_{ALink}(t)$ from transitioning to the lower rail potential if it were allowed to conduct current. Let similar definitions hold for T_L and L_L.

The analysis that follows uses a series of narratives to examine the various scenarios stemming from a T-L-T mode sequence. Since the PRAL inverter is symmetric with respect to the upper and lower power matrix rails, considering the mode sequence T_U-L_U-T_L is sufficient to fully address the objectives of this section. The following definitions, designed specifically for the case of a T_U-L_U-T_L mode sequence, are used throughout the narratives that follow. Let $i_{SLoad+}(t)$ be the sum of all load currents $i_k(t)$ such that $i_k(t) > 0$ and $\xi_k = S$, $k \in \{A, B, C\}$. Let $i_{SLoad-}(t)$ be the negative sum of all load currents $i_k(t)$ for which $i_k(t) < 0$ and $\xi_k = S$, $k \in \{A, B, C\}$. Currents $i_{SLoad+}(t)$ and $i_{SLoad-}(t)$ are thus the sum of the load phase currents that directed out of and into the auxiliary link, respectively. Similarly, let $i_{ULoad+}(t)$ be the sum of all load currents $i_k(t)$ for which $i_k(t) > 0$ and $\xi_k = U$, $k \in \{A, B, C\}$ and let $i_{ULoad-}(t)$ be the negative sum of all load currents $i_k(t)$ for which $i_k(t) < 0$ and $\xi_k = U$, $k \in \{A, B, C\}$. Currents $i_{ULoad+}(t)$ and $i_{ULoad-}(t)$ are the total load phase currents directed out of and into the upper power matrix rail, respectively. These specially defined currents are formally expressed below.

$$i_{SLoad+}(t) = \sum_{k\in(j|i_j>0)} i_k(t)\delta_{\xi_k,S} \qquad 5.7.1.1$$

$$i_{SLoad-}(t) = \sum_{k\in(j|i_j<0)} -i_k(t)\delta_{\xi_k,S} \qquad 5.7.1.2$$

$$i_{ULoad+}(t) = \sum_{k\in(j|i_j>0)} i_k(t)\delta_{\xi_k,U} \qquad 5.7.1.3$$

$$i_{ULoad-}(t) = \sum_{k\in(j|i_j<0)} -i_k(t)\delta_{\xi_k,U} \qquad 5.7.1.4$$

The devices considered in the remainder of this section are assumed to exhibit fixed forward conduction voltage drops. Let V_D be the voltage drop across a power matrix switch conducting in the non-blocking direction. Let V_{SW} be the voltage drop across a power matrix switch conducting in the blocking direction. Finally, let V_{BSW} be the voltage drop across an auxiliary link bilateral switch conducting current in either direction. V_D and V_{SW} are thus the forward voltage drops associated with the inverse-parallel diode and self-extinguishing devices composing the power matrix switches, respectively. V_{BSW} depends on the bilateral switch configuration employed as well as the conduction voltage drops of the constituent devices.

5.7.2 Device Current Stress at the End of the T_U Mode

To avoid overlap with the T_L mode analysis presented later, consider the phase of the T_U mode during which all device turn-off currents have subsided. The initial interaction between the auxiliary link and the upper rail serves to partition this portion of the T_U mode into two distinct segments. The term interaction, as used in this context, means that a current path, which does not pass through the load, exists directly between the auxiliary link and a power matrix rail. Before the interaction begins, exactly one switch, either a power matrix switch or an auxiliary link

bilateral switch, in each phase leg carries the entire load phase current while the remaining switches in the phase leg do not conduct. Consequently, the peak device current in the pre-interaction segment is limited to the peak load phase current.

The post-interaction segment of the T_U mode proceeds under one of two scenarios. In the first scenario, $i_{SLoad-}(t) = 0$. In this case, any transitioning phase leg voltages are forced toward V_{Link} solely by current directed from the auxiliary link to the respective load phase. Each transitioning phase leg voltage will thus equal $v_{ALink}(t) - V_{BSW}$ until the upper power matrix switch in the respective phase leg is turned on. Since $i_R(t) > 0$ for this scenario, residual current in L_R will normally drive $v_{ALink}(t)$ above V_{Link} until D_{CU} clamps it at $V_{Link} + V_D$. When $v_{ALink}(t)$ reaches V_{Link}, the upper power matrix switch in each transitioning phase leg is turned on. Since $v_{ALink}(t) \geq V_{Link} - V_{SW}$ at this point, the upper power matrix switches are not subjected to the resonant circuit capacitor impedance. Consequently, no conduction path exists directly between the upper rail and the auxiliary link through any of the power matrix or auxiliary link bilateral switches.

The upper power matrix switches present a potential of $V_{Link} - V_{SW}$ to the transitioning phase legs while the auxiliary link bilateral switches present at most $V_{Link} + V_D - V_{BSW}$. Since $V_{BSW} \cong V_{SW} + 2V_D$ for the bilateral switch implementation shown in Figure 49, the load phase current in each transitioning phase leg transfers from the bilateral switch to the corresponding upper power matrix switch. Since no further rise in either $v_{ALink}(t)$ or any of the phase leg voltages is possible, this marks the end of the T_U mode. The peak current in D_{CU} is limited to $i_{SLoad+}(t)$ plus the residual boost current at the time $v_{ALink}(t)$ first reaches $V_{Link} + V_D$. At the end of the T_U mode, exactly one power matrix switch in each phase leg carries the entire corresponding load phase current. None of the remaining power matrix or auxiliary link switches conduct. Consequently, the current stress in both the power matrix and auxiliary link switches never exceed the peak load phase current.

Now consider the second scenario in which $i_{SLoad-}(t) > 0$. Prior to any interaction between the auxiliary link and the upper rail, the voltage of each phase leg contributing to $i_{SLoad-}(t)$ is held at $v_{ALink}(t) + V_{BSW}$ by the auxiliary link bilateral switches. If $i_{SLoad+}(t) > 0$, the voltage of any transitioning phase leg whose load current contributes to $i_{SLoad+}(t)$ is held at $v_{ALink}(t) - V_{BSW}$. The voltages of the phase legs contributing to $i_{SLoad-}(t)$ are the largest of the transitioning phase legs. Consequently, they reach the upper rail potential first. Once they reach $V_{Link} + V_D$, they are clamped by the upper power matrix switch inverse-parallel diodes. When this occurs, $v_{ALink}(t) \cong V_{Link} + V_D - V_{BSW}$. The upper power matrix switch in each transitioning phase leg is then turned on and all phase currents contributing to $i_{SLoad+}(t)$ transfer from the bilateral switches to the upper power matrix switches. This raises the voltages of the phase legs contributing to $i_{SLoad+}(t)$ to $V_{Link} - V_{SW}$. If $i_R(t) > 0$ at this point, $v_{ALink}(t)$ continues to rise until it is clamped by D_{CU} at $V_{Link} + V_D$ or until $i_R(t)$ falls to zero, either way marking the end of the T_U mode. If $i_R(t) < 0$, $v_{ALink}(t)$ drops until it is clamped at $V_{Link} + V_D - V_{BSW}$ by the auxiliary link bilateral switches connected to the phase legs contributing to $i_{SLoad-}(t)$. However, in this case the decrease in $v_{ALink}(t)$ occurs in the L_U mode since all relevant voltages have already reached their respective peaks. In both cases, the maximum power matrix and auxiliary link switch currents are limited to the peak load phase currents. The peak current in the auxiliary link clamping diode, D_{CU}, is limited to the sum of the peak load phase current plus the peak residual boost current in L_R.

In conclusion, the device current stress levels experienced by both the power matrix switches and the auxiliary link bilateral switches in the phase of the T_U mode considered is limited to the peak load phase current. The only current stress level exceeding the peak load phase current is that of the auxiliary link clamping diode, D_{CU}. Fortunately, power diodes can typically safely withstand surge currents several times greater than their rated average current. Secondly, the average current in D_{CU} is a tiny fraction of the peak load current. This allows the rated average current for D_{CU} to be substantially smaller than that of the power matrix devices.

5.7.3 Device Current Stress in the L_U Mode

The duration of the L_U mode depends on the time needed to initialize L_R with the boost energy required for the following T_L mode. If $i_R(t)$ happens to satisfy this requirement at the end of the T_U mode, the L_U to be skipped entirely. Otherwise, the inverter occupies the L_U mode until $i_R(t)$ reaches the required level. This section addresses the latter case in which boost energy must be imparted to L_R before the T_L mode is allowed to begin.

The following facts and observations significantly simplify the process of estimating device current stress during the L_U mode. First, the load phase currents are essentially constant throughout the mode, which typically lasts less than 10μs for an inverter with a resonant circuit frequency of 25kHz or more. Second, the voltage change across C_{DU} and C_{DL} during the course of a single L_U mode is insignificant compared to the voltage across L_R. Thus, the only reactive element of consequence remaining in the circuit is L_R. Figure 50 shows a schematic diagram suitable for modeling the PRAL inverter in the L_U mode under these conditions. The power matrix voltage in the figure is modeled using a fixed voltage source. Since $v_{ALink}(t)$ will typically

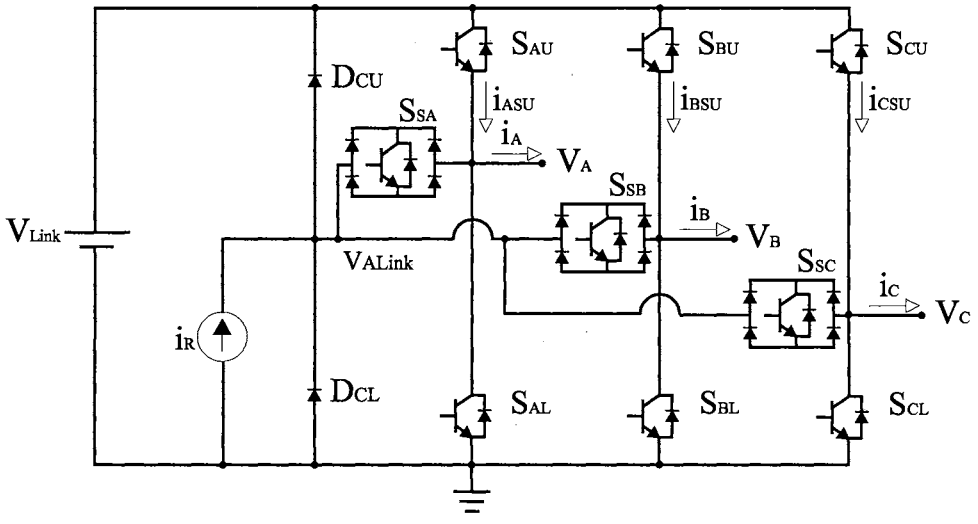


Figure 50. Schematic diagram of an approximate equivalent circuit model for the PRAL inverter operating in the L_U mode

change by at few hundredths of a Volt during the L_U, the limited influence of C_R is neglected to simplify the discussion. The current passing from the resonant circuit to the auxiliary link is thus approximately equal to $i_R(t)$ and is modeled as an independent current source.

The well-known intermediate value theorem provides a convenient means of finding the peak device current stress in the L_U mode. First, the voltage across L_R is such that $i_R(t)$ is monotonically decreasing throughout the entire L_U mode. Second, one or more power matrix or auxiliary link bilateral switches may be completing turn-on during the initial phase of the L_U mode but no switch turn-on commands are issued during the mode. The only switch turn-off commands issued during the mode are those at the very end that initiate the transition to the T_L mode. Third, current can not pass from the auxiliary link into the upper rail through the upper power matrix switch inverse-parallel diodes. Using these facts along with the assumption of constant load current, it follows that the currents $i_{ASU}(t)$, $i_{BSU}(t)$, and $i_{CSU}(t)$ shown in Figure 50 are monotonic non-decreasing. Since each $i_{kSU}(t)$ is monotonic and each $i_k(t)$ is constant for $k \in \{A, B, C\}$, the current in each auxiliary link bilateral switch is also monotonic non-decreasing. Any change in the bilateral switch currents must be directed toward the auxiliary link. Consequently, the current in each of the power matrix and auxiliary link switches is monotonic non-decreasing throughout the entire L_U mode.

Now that device current monotonicity has been established throughout the L_U mode, the intermediate value theorem can be applied to find the peak device current stresses in the L_U mode. Since a device current bound already exists for the end of the T_U mode and the device currents are continuous across the T_U-L_U mode boundary, a device current bound is already known for the beginning of the L_U mode. Thus, only a device current bound for the end of L_U remains to be found in order to establish a device current stress bound for the entire mode. To find such a bound, it is necessary to examine the conditions that trigger the L_U-T_L mode transition.

The conditions that exist at the end of the L_U mode depend upon the states of the phase legs in both the L_U mode and the following T_L mode. To aid the discussion, augment the definition of ξ_k with a mode designator. Let $\xi_k(j)$ be the k^{th} phase leg state, as defined in Subsection 5.5.2, when the inverter is in mode j, where $j \in \{T_U, L_U, T_L, L_L\}$. It is also useful to apply the mode designator to other quantities that depend on the various phase leg states when the specific inverter mode is not clear. For example, $\xi_k(T_U)$ is the state of phase leg k during the inverter T_U mode. Similarly, $i_{SLoad+}^{T_L}(t)$ is equal to $i_{SLoad+}(t)$ as defined in 5.7.1.1 but with the clear understanding that the inverter is in the T_L mode. Using this notation, it follows from Section 5.5.3 that the L_U mode ends when $i_R(t)$ satisfies,

$$i_R(t) \geq \sum_{k\in\{A,B,C\}} i_k \delta_{\xi_k(T_L),S} - I_{Boost} \qquad 5.7.3.1$$

For values of $i_R(t) \geq 0$ at the end of the L_U mode, D_{CU} conducts all of $i_R(t)$ while the bilateral switches carry no current. Since $i_R(t)$ is monotonic decreasing during the $L_U(t)$, the peak current in D_{CU} occurs at the beginning of the mode while the currents in all other devices remain constant throughout the mode. Consequently, the peak current in each device is equal to the value present at the beginning of the L_U mode. Thus, all device currents are less than or equal to those occurring in the latter segments of the T_U mode discussed previously.

Next, consider the case where $i_R(t) < 0$ at the end of the L_U mode. The condition that ends the L_U mode, given in 5.7.3.1, can be expressed in terms of $i_{SLoad+}^{T_L}(t)$ and $i_{SLoad-}^{T_L}(t)$ as,

$$i_R(t) + i_{SLoad-}^{T_L}(t) - i_{SLoad+}^{T_L}(t) + I_{Boost} \leq 0 \qquad 5.7.3.2$$

Rearranging 5.7.3.2 to obtain a lower bound on the value of $i_R(t)$ for which the L_U-T_L mode transition will occur results in,

$$i_R(t) \geq i_{SLoad+}^{T_L} - i_{SLoad-}^{T_L}(t) - I_{Boost} \qquad 5.7.3.3$$

Since only negative values of $i_R(t)$ cause current to flow in the auxiliary link bilateral switches, and thus potentially contribute to additional current flow in the upper power matrix switches, $i_{SLoad+}^{T_L}(t)$ can be dropped from 5.7.3.3. This leads to the following conservative lower bound on $i_R(t)$ at the end of the L_U mode.

$$i_R(t) \geq -(i_{SLoad-}^{T_L} + I_{Boost}) \qquad 5.7.3.4$$

Since $i_{SLoad-}^{T_L}(t) \leq I_L$, a more useful relation follows from 5.7.3.4,

$$i_R(t) \geq -(I_L + I_{Boost}) \qquad 5.7.3.5$$

This result indicates that the maximum current flowing through any bilateral switch at the end of the L_U mode is limited to the peak load phase current, I_L, plus the peak boost current used to initialize the resonant circuit.

Next, consider the current component in the upper power matrix switches resulting from the initialization of $i_R(t)$. If $i_R(t) + i_{ULoad-}^{L_L}(t) \geq 0$, the current passing from the load into the upper rail, via the upper power matrix inverse-parallel diodes, prevents any current from passing through the upper power matrix switches into L_R. In this case, the current stress in each upper power matrix switch is limited to the peak load phase current, I_L. If $i_R(t) + i_{ULoad-}^{L_L}(t) < 0$, any current over and above that of the phase leg currents contributing to $i_{ULoad+}^{L_L}(t)$ that passes through the power matrix switches is limited to the net current passing from the upper rail into L_R. For convenience, let $i_{URNet}(t)$ be the net current passing from the upper rail into the auxiliary link that does not pass through the load.

$$i_{URNet}(t)=\begin{cases}-(i_R(t)+i^{L_U}_{ULoad-}(t)) & i_R(t)\le -i^{L_U}_{ULoad-}(t)\\ 0 & \text{Otherwise}\end{cases} \qquad 5.7.3.6$$

From 5.7.3.4,

$$i_R(t)+i^{T_L}_{SLoad-}\ge -I_{Boost} \qquad 5.7.3.7$$

Since $i^{T_L}_{SLoad-}(t)\le i^{L_U}_{ULoad-}(t)$ at the L_U-T_L mode boundary, it follows from 5.7.3.7 that,

$$i_R(t)+i^{L_U}_{ULoad-}(t)\ge -I_{Boost} \qquad 5.7.3.8$$

Using 5.7.3.6 in 5.7.3.8, the following bound exists for $i_{URNet}(t)$,

$$0\le i_{URNet}(t)\le I_{Boost} \qquad 5.7.3.9$$

Therefore, the current in any upper power matrix switch resulting from the initialization of L_R is bounded by I_{Boost}. The only other current component in a given power matrix switch is the load current of the respective phase leg, which is bounded by I_L. Thus, the peak current stress in a power matrix switch at the end of the L_U mode is limited to $I_L + I_{Boost}$. Hence, the peak current stress in both the power matrix and auxiliary link bilateral switches throughout the entire L_U mode is limited to the peak load phase current plus the peak boost current.

5.7.4 Device Current Stress in the Initial Segment of the T_L Mode

5.7.4.1 The Case of $i_R(t) > 0$ in the T_L Mode Consider the case where $i_R(t) > 0$ at the beginning of the T_L mode. For $i_R(t) > 0$, the only conducting switches that are subject to a turn-off command are the upper power matrix switches in the phase legs contributing to $i^{T_L}_{SLoad+}(t)$. Once the affected switches begin to turn off, they come out of saturation. This causes the corresponding phase leg voltages to decrease until they reach $v_{ALink}(t) - V_{BSW}$, which is equal to $V_{Link} + V_D$ -

V_{BSW} for $i_R(t) > 0$. At this point, load phase current will begin to transfer from the upper power matrix switch to the auxiliary link bilateral switch in each affected phase leg. Since the turn-on time of most commonly used devices, including IGBT's, is several times shorter than their turn-off time, the bilateral switches will fully compensate for the reduction in upper power matrix switch currents as the switch turn-off currents decay. This prevents the voltages of the transitioning phase legs from exhibiting a large momentary voltage "droop" that would otherwise occur.

The transfer of $i_{SLoad+}^{T_L}(t)$ from the upper power matrix switches to the auxiliary link reduces the net positive current into the auxiliary link. Once the net current becomes negative, D_{CU} turns off and $v_{ALink}(t)$ begins to fall. If $i_{SLoad-}^{T_L}(t)$ is zero, no other switch turn-on or turn-off events occur and $v_{ALink}(t)$ continues to decrease until it reaches the lower rail potential. If $i_{SLoad-}^{T_L}(t) \geq 0$, $i_{SLoad-}^{T_L}(t)$ will transfer from the upper power matrix inverse-parallel diode to the corresponding auxiliary link bilateral switch in each phase leg contributing to $i_{SLoad-}^{T_L}(t)$ when $v_{ALink}(t)$ falls to $V_{Link} + V_D - V_{BSW}$. Although the inverse-parallel diode turn-off time is typically much shorter than that of a bilateral switch, the orientation of the load phase current is such that no phase leg voltage "droop" can occur. Thus, the zero-voltage switching requirements are not violated. Once the voltage across L_R has driven $i_R(t)$ sufficiently negative to offset the contribution of $i_{SLoad-}^{T_L}(t)$ to the net current leaving the auxiliary link, $v_{ALink}(t)$ will proceed toward the lower rail potential without further interruption.

5.7.4.2 The Case of $i_R(t) \leq 0$ in the T_L Mode Consider the case where $i_R(t) \leq 0$ at the beginning of the T_L mode. Since $v_{ALink}(t)$ could lie anywhere between $V_{Link} + V_D$ and $V_{Link} - V_{SW} - V_{BSW}$ for this condition, it is convenient to focus solely on the switch turn-off and turn-on events. As in the case of $i_R(t) > 0$, the only conducting upper power matrix switches that turn off are those in the phase legs contributing to $i_{SLoad+}^{T_L}(t)$. The auxiliary link bilateral switch in each

corresponding phase leg begins diverting its load phase current from the upper rail to the auxiliary link as soon as the respective phase leg voltage reaches $v_{ALink}(t) - V_{BSW}$. The bilateral switch carries the full load phase current once the upper power matrix switch tail current has fully decayed. As in the case of $i_R(t) > 0$, the bilateral switch prevents the phase leg voltage from "drooping" during the current path transition. If $i_{SLoad-}^{T_L}(t) > 0$, the load phase current in each phase leg contributing to $i_{SLoad-}^{T_L}(t)$ begins transferring from the corresponding upper power matrix inverse-parallel diode to the auxiliary link bilateral switch when $v_{ALink}(t)$ falls to $V_{Link} + V_D - V_{BSW}$. In the case of $i_R(t) < 0$, part or all of $i_R(t)$ may be routed through the bilateral switch of a non-transitioning phase leg. In this case, the respective bilateral switch current in each such phase leg will begin to decay shortly after the T_L mode begins. Consequently, the current in the corresponding upper power matrix switch is reduced, in-step, with the decay of the bilateral switch current.

For all cases of $i_R(t)$, no other switch turn-on or turn-off events, other than those described above, occur until the end of the T_L mode. The maximum current transferred to any newly conducting switch is limited to the peak load phase current. The current in each switch that turns off during the T_L mode only decreases from the level existing at the beginning of the mode. The current magnitude in all devices that do not change conduction states does not increase. Consequently, the maximum current stress in any of the inverter devices is limited to that existing at the beginning of the T_L mode, or equivalently, at the end of the L_U mode.

5.7.5 Summary and Conclusions Regarding PRAL Inverter Device Current Stresses

This section employed a series of qualitative arguments to establish a bound for the current stress levels that are likely to exist in PRAL inverter switching devices. This was accomplished through examination of a complete T-L-T mode sequence in which current bounds were established at relevant intermediate points in the time interval spanning the mode sequence. The

mean value theorem was then employed to establish that peak device current stress occurs at one of these intermediate points rather than between two of the points. Without loss of generality, only the T_U-L_U-T_L mode sequence was examined. The results revealed that the peak device current stress occurs during the L mode and is equal to the sum of the peak load phase current, I_L, and the peak commanded resonant circuit boost current, $\max(I_{Boost})$.

The resonant circuit initialization process typically consumes less than 15% of the entire resonant circuit period in UPRDL designs. Since the PRAL inverter L_U mode circuit configuration is similar to that of UPRDL inverters during initialization, it is reasonable to expect the L_U mode to occupy approximately the same fraction of the PRAL resonant circuit period. Consequently, the maximum fraction of time a switch might spend at stress levels above I_L is at most about 10%. Typically however, the total current in a given switch will rarely exceed I_L except in cases where the control system is attempting to correct for disturbances in the voltage divider node potential. This is discussed in detail in Chapter VI.

5.8 Summary

This chapter applied the voltage space concepts introduced in Chapters III and IV to the task of developing a new soft-switched inverter topology with significantly lower device voltage stress levels than is theoretically attainable for PRDL topologies. The proposed solution integrates an oscillating auxiliary link into a conventional bridge inverter to implement the required soft switching mechanism without compromising the bridge structure's low device voltage stress advantage. Current stress in all devices is essentially limited to the peak load phase current, with the exception of occasional brief intervals during which the resonant circuit boost current is also carried.

The pseudo-periodic nature of the auxiliary link imposes limitations on the time at which the inverter is permitted to change states. However, the number of state changes in a given time

interval that are achievable using the auxiliary link is roughly one order of magnitude greater than that achievable with the bridge structure alone. This is due entirely to the virtual elimination of switching losses stemming from soft switching. The potential performance penalty incurred over that of the hypothetical inverter is difficult to quantify, due to the difficulty of separating control system effects from topological characteristics. The need for one bilateral switch between each phase leg and the auxiliary link is an obvious detriment to the approach. However, the cumulative switch volt-ampere requirement for practical UPRDL and SPRDL designs typically equals or exceeds that of the proposed PRAL approach, due to the elevated voltage stress that typifies PRDL topologies.

CHAPTER VI

ADDITIONAL PRAL INVERTER DESIGN ISSUES

6.1 Introduction

Before proceeding to the simulation experiments presented in Chapters VII and VIII, several additional PRAL inverter design issues require attention. Adequate discussion of the boost current selection problem, regulation of the PRAL voltage divider node potential, selection of resonant circuit component values, and power matrix state selection strategies are noticeably absent in the preceding chapters. Thorough treatment of any one of these subjects could easily constitute a separate research effort. For brevity, only those aspects of each topic needed to meaningfully evaluate the PRAL inverter through simulation trials are considered in this chapter.

The problem of determining the boost current value that is required for proper operation of a given PRAL inverter design is similar to that for PRDL inverters. Unfortunately, the published PRDL inverter literature provides very little discussion on this subject. It is thus necessary to develop a strategy for selecting appropriate boost current values for the PRAL inverter without guidance from the soft-switched inverter literature.

The problem of regulating the voltage divider node potential so that it remains approximately halfway between the potentials of the upper and lower power matrix rails is unique to the PRAL topology. As suggested in Chapter V, the approach adopted in this work elevates the boost current under prescribed conditions in order to offset disturbance effects. Within this context, the objective of the chapter is to examine the implementation details associated with regulating the voltage divider potential using this approach.

Selection of resonant circuit component values is largely dependent upon the performance optimization objectives chosen for a specific inverter application. The pseudo-chaotic nature of PRAL inverter state transitions render analytical techniques for computing optimal values for C_R and L_R intractable. This leaves modeling and simulation as the only viable method for optimally selecting C_R and L_R, subject to a given optimization strategy. However, a few basic "first cut" design guidelines appear to yield reasonably good values of C_R and L_R that can be optimized through modeling and simulation if desired. These guidelines are presented later in the chapter along with relevant remarks concerning the selection of other PRAL inverter components.

The problem of selecting appropriate power matrix states for the PRAL inverter is similar to that of APRDL topologies except for the availability of active-state to active-state transitions. Moreover, existing load current control methodologies, which are superior to those described for the APRDL topologies proposed in the literature, are either directly applicable or are easily adaptable for use with the PRAL topology. The two techniques considered in this work include a simple Proportional-Integral (PI) current controller and a real-time cost-function controller that incorporates estimates of the load back EMF.

6.2 Resonant Circuit Boost Current

6.2.1 The Boost Current Problem

The PRDL inverter literature is devoid of explicit discussions regarding the resonant circuit boost current value required to ensure that the resonant link voltage collapses to zero at the end of each resonant cycle. The few references appearing in the literature suggest that a single fixed boost current value is used for all resonant cycles. This value is apparently determined through modeling and simulation or experimentation with prototype hardware for a given inverter-load configuration but is not included with the published evaluation results that typically accompany new PRDL design proposals.

The assumption that changes in the load current are negligible over the course of a resonant circuit cycle is well rooted in the PRDL literature and appears to be the premise justifying the use of fixed boost current values. Additionally, a fixed boost current value, as opposed to a variable value tailored to a given set of inverter state conditions, requires no dedicated real-time control logic to generate. However, the use of a boost current value greater than necessary tends to increase switching losses and thus reduces the effective switching frequency capability of the inverter. Furthermore, the proliferation of inexpensive high-performance microprocessors has substantially reduced the cost of real-time control logic, such as that needed to generate boost current values tailored to each L to T mode transition. It follows that at least a cursory analytical examination of boost current requirements is warranted for the newly proposed PRAL topology.

Five dominant factors determine the boost current value required for a given L to T mode transition. These include load impedance and load back EMF influences, imbalance in the voltage divider node potential, energy dissipation in the resonant circuit components, secondary influences such as measurement noise and modeling imperfections, and device turn-off current effects. Varying degrees of interdependence exists amongst the five factors. Unfortunately, combining their cumulative effects into a single analytical model with which the required boost current value could be determined appears to be analytically intractable. However, meaningful results are obtainable by considering the factors either separately or in small groups under the assumption that the remaining factors are not present.

The effects stemming from load impedance and load back EMF are easily modeled together with those arising from imbalance in the voltage divider node potential. Secondly, the boost current component associated with losses in the resonant circuit depends almost entirely on the value of i_R and i_X at the time of a given L to T mode transition. It is thus reasonable to consider the boost current component needed to compensate for resonant circuit losses separately from influences associated with the load and voltage divider potential. Furthermore, the boost current component needed to offset measurement noise and modeling errors requires no model. Instead,

this component is a fixed value determined through simulation, experimentation, or experience. The magnitude of this component is, by design, a small fraction of the combined boost current requirement of the two preceding cases. Finally, the principal result of device turn-off currents is an effective amplification of the boost current value existing at the time of a given L to T mode transition. Accordingly, the effects of device turn-off currents can be considered separately from the other factors with little consequence. The following subsections describe techniques for estimating the boost current requirements associated with each factor or group of factors along with a method for combining the results into a cumulative boost current requirement. The combination technique used to combine the boost current components relies on the associated energy stored in L_R. Thus, the boost current component estimates presented in the following subsections are accompanied by estimates of the corresponding boost energy components.

6.2.2 An Approximate Equivalent Load Circuit for Modeling Load Influences on the Resonant Circuit

To begin the analysis, consider the Thevenin equivalent circuit that the load presents to the auxiliary link during the T_U and T_L modes. Four possible arrangements exist in which none, one, two, or all three load phases are connected to the auxiliary link. The first and last cases result in no net current between the auxiliary link and the load and thus do not affect the boost current requirement. The second and third cases, however, are non-trivial. The second case, in which exactly one load phase terminal is connected to the auxiliary link during a state transition, is illustrated in Figure 51. The load back EMF and current associated with each load phase are labeled with subscripts 1, 2, or 3 instead of the conventional labels A, B, or C. This is done so that the results are applicable to all three possible cases where either Phase A, Phase B, or Phase C is connected to the auxiliary link. Voltage sources V_2 and V_3 represent the non-transitioning phase legs of the inverter and therefore have the same potential as either the upper or lower power matrix rails.

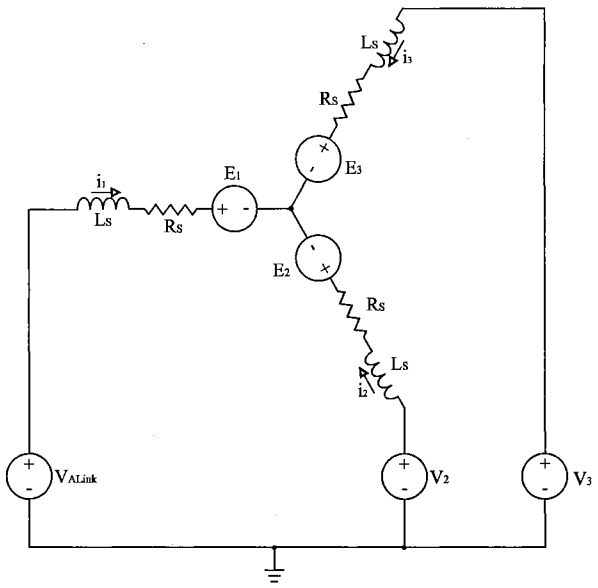


Figure 51. Equivalent load circuit model for the case where exactly one load phase is connected to the auxiliary link during a T_L or T_U mode

The inclusion of the load phase resistance in the model unduly complicates the expression for the boost current estimate. Fortunately, the voltage drop across a given load phase resistance is at most a small fraction of the voltage between the power matrix rails. Additionally, the current in a given load phase typically changes by at most a few percent of the rated inverter phase current during a given T mode. Consequently, the voltage drop across each phase resistance can be approximated as a constant voltage source. Using this simplification, the voltage appearing across each load phase resistance is assumed to be $R_S i_k(0)$, where $i_k(0)$ is the current flowing in phase k at the beginning of the T mode at time t = 0.

For practical load frequencies, the load back EMF voltages $E_1(t)$, $E_2(t)$, and $E_3(t)$ are slowly changing quantities and can be assumed constant over the short time span of a PRAL inverter T mode. For convenience, the values of these voltages during a T mode are also assumed to equal their respective values at the beginning of the mode at time t = 0. Applying these assumptions to

the circuit depicted in Figure 51 results in the approximate equivalent circuit shown in Figure 52. The associated approximate equivalent circuit parameters are given by 6.2.2.1 and 6.2.2.2

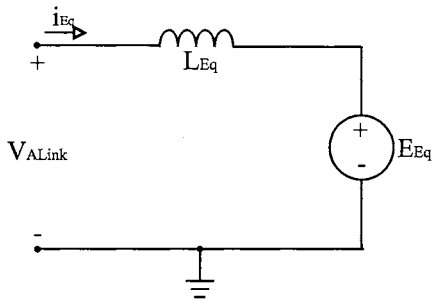


Figure 52. Approximate equivalent load presented to the auxiliary link for the case where one load phase is connected to the auxiliary link during a T_L or T_U mode

$$L_{Eq} = \tfrac{3}{2} L_S \qquad 6.2.2.1$$

$$E_{Eq} = E_1(0) + \tfrac{3}{2} i_1(0) R_S - \tfrac{1}{2}(E_2(0) + E_3(0)) + \tfrac{1}{2}(V_2(0) + V_3(0)) \qquad 6.2.2.2$$

Next, consider the case where two of the three load phase terminals are connected to the auxiliary link during either the T_U or T_L mode, as shown in Figure 53. As in the previous case, it is assumed that the voltage drop across each of the load phase resistances does not change significantly over the course of an inverter state transition. Using the resistance voltage drops present at the beginning of the state transition results in the same approximate equivalent circuit shown in Figure 52 with L_{Eq} again given by 6.2.2.1 but with the Thevenin equivalent voltage given by 6.2.2.3.

$$E_{Eq} = V_3(0) - E_3(0) - \tfrac{3}{2} i_3(0) R_S + \tfrac{1}{2}(E_1(0) + E_2(0)) \qquad 6.2.2.3$$

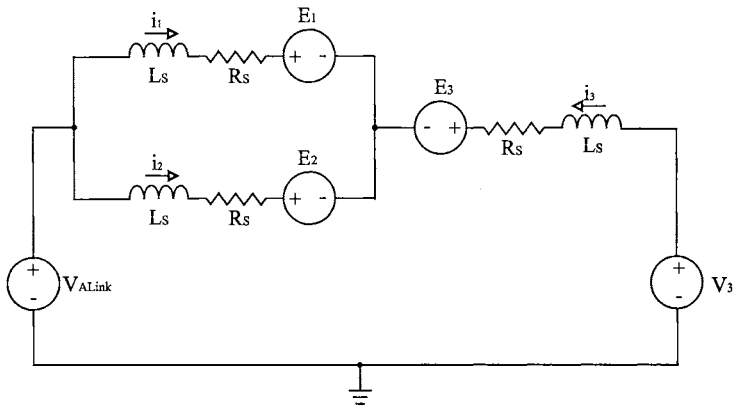


Figure 53. Approximate equivalent load circuit model for the case in which two load phase terminals are connected to the auxiliary link during a T_L or T_U mode

6.2.3 Boost Energy Associated with Voltage Divider Imbalance and Load Interaction

The next step in the analysis is to examine the behavior of the auxiliary link when it is connected to the approximate equivalent load circuit. The loss mechanism in the resonant circuit, R_R, is considered separately and is thus omitted from consideration here. Furthermore, it is assumed that the voltage divider capacitors, C_{DU} and C_{DL} are much larger than C_R, allowing any change in the voltage divider node potential to be negligible over the course of a given T mode. The resulting approximate equivalent circuit model shown in Figure 54 represents the combination of the auxiliary link resonant circuit with the approximate equivalent load circuit shown in Figure 52. The current $i_x(t)$ is the sum of the load phase currents associated with the transitioning phase legs, also referred to as the switched load current. The governing differential equations for the circuit are given in 6.2.3.1 through 6.2.3.3.

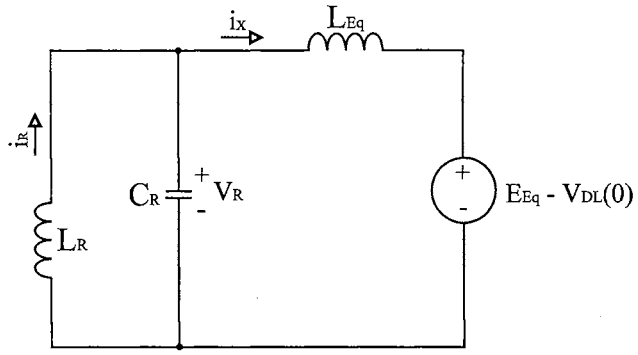


Figure 54. Approximate equivalent model of the combined auxiliary link resonant circuit and the approximate equivalent load circuit

$$\frac{dv_R}{dt} = \frac{1}{C_R}(i_R - i_X) \qquad 6.2.3.1$$

$$\frac{di_R}{dt} = -\frac{v_R}{L_R} \qquad 6.2.3.2$$

$$\frac{di_X}{dt} = \frac{1}{L_{Eq}}\left(v_R + v_{DL}(0) - E_{Eq}\right) \qquad 6.2.3.3$$

Differentiating 6.2.3.3 with respect to time and then employing 6.2.3.1 and 6.2.3.2 yields,

$$\frac{d^2v_R}{dt^2} + \frac{1}{C_R}\left(\frac{1}{L_R} + \frac{1}{L_{Eq}}\right)v_R = \frac{E_{Eq} - v_{DL}(0)}{C_R L_{Eq}} \qquad 6.2.3.4$$

Let L_P, ω, and ρ_L be defined as,

$$L_P = \frac{L_R L_{Eq}}{L_R + L_{Eq}} \qquad 6.2.3.5$$

$$\omega = \frac{1}{\sqrt{C_R L_P}} \qquad 6.2.3.6$$

$$\rho_L = \frac{L_P}{L_{Eq}} \qquad 6.2.3.7$$

Solving 6.2.3.4 for $v_R(t)$ using the initial conditions $v_R(0)$ and $i_R(0)$ yields,

$$v_R(t) = \left(v_R(0) + \left(v_{DL}(0) - E_{Eq}\right)\rho_L\right)\cos\omega t + \sqrt{\frac{L_P}{C_R}}\left(i_R(0) - i_X(0)\right)\sin\omega t + \left(E_{Eq} - v_{DL}(0)\right)\rho_L \qquad 6.2.3.8$$

where, $t \geq 0$.

The next step is to find the smallest $t_1 > 0$ such that $v_R(t_1)$ is a maximum or minimum. Taking the first derivative of 6.2.3.8 with respect to time and setting it equal to zero for $t = t_1$ results in,

$$t_1 = \frac{1}{\omega}\tan^{-1}\left(\sqrt{\frac{L_P}{C_R}} \cdot \frac{i_R(0) - i_X(0)}{v_R(0) - \rho_L\left(E_{Eq} - v_{DL}(0)\right)}\right) \qquad 6.2.3.9$$

Substituting 6.2.3.9 into 6.2.3.8 yields,

$$v_R(t_1) = \sqrt{\left(v_R(0) - \rho_L\left(E_{Eq} - v_{DL}(0)\right)\right)^2 + \frac{L_P}{C_R}\left(i_R(0) - i_X(0)\right)^2} + \rho_L\left(E_{Eq} - v_{DL}(0)\right) \qquad 6.2.3.10$$

Next, solving 6.2.3.10 for $i_R(0) - i_X(0)$ results in,

$$i_R(0) - i_X(0) = \pm\sqrt{\frac{C_R}{L_P}\left(v_R(t_1)^2 - v_R(0)^2 - 2\rho_L\left(E_{Eq} - v_{DL}(0)\right)\left(v_R(t_1) - v_R(0)\right)\right)} \qquad 6.2.3.11$$

The left-hand side of 6.2.3.11 is equal to the net current flowing into the auxiliary link at the beginning of either a T_U or T_L mode at time $t = 0$. The voltage $v_R(0)$ is the voltage across the resonant circuit capacitor, C_R, at the beginning of the PRAL state transition. The voltage $v_R(t_1)$ is the subsequent extreme, either maximum or minimum, voltage appearing across the resonant circuit capacitor approximately one-half resonant circuit cycle after the state transition begins.

Interpretation of the left-hand side of 6.2.3.11 depends on the inverter operating mode, T_U or T_L, and the sign of the argument on the right-hand side of the equation. First, consider the case of a T_L mode. The appropriate values of $v_R(0)$ and $v_R(t_1)$ are $v_{DU}(0)$ and $-v_{DL}(0)$, respectively. This assumes that $i_R(0) - i_X(0)$ is chosen so that there is just enough energy in L_R at $t = 0$ for $v_{ALink}(t)$ to reach $-v_{DL}(0)$ at $t = t_1$ and then immediately begin to rise if not constrained. For a T_L mode, it is physically impossible for the transition to begin unless the left-hand side of 6.2.3.11 is negative. When the argument under the radical is positive, the net current into the auxiliary link at the beginning of the T_L mode is found using 6.2.3.11 with the negative sign. The case where the argument under the radical is negative correspond to the case where no boost current is needed to drive $v_{ALink}(t)$ below the lower rail potential. The physical impossibility of increasing the left-hand side of 6.2.3.11 by holding the auxiliary link at the upper rail potential is consistent with the pure imaginary solution that results for 6.2.3.11 when a negative argument exists under the radical. For the case of the T_U mode, the values substituted into 6.2.3.11 for $v_R(0)$ and $v_R(t_1)$ are $--v_{DL}(0)$ and $v_{DU}(0)$, respectively. Since the left-hand side of 6.2.11 must be positive for a T_U mode transition to begin, the positive sign in 6.2.3.11 is taken when the argument under the radical is positive. It follows that the boost current component, I_{LVD}, required for a prescribed set of load and voltage divide node potential conditions is given by,

$$I_{LVD} = \begin{cases} \sqrt{\frac{C_R}{L_P}}\,\mathrm{Re}\left\{\left(v_{DL}(0)^2 - v_{DU}(0)^2 + 2\rho_L\left(E_{Eq} - v_{DL}(0)\right)\left(v_{DL}(t_1) + v_{DU}(0)\right)\right)^{1/2}\right\} & T_L \text{ Mode} \\ \sqrt{\frac{C_R}{L_P}}\,\mathrm{Re}\left\{\left(v_{DU}(0)^2 - v_{DL}(0)^2 - 2\rho_L\left(E_{Eq} - v_{DL}(0)\right)\left(v_{DU}(t_1) + v_{DL}(0)\right)\right)^{1/2}\right\} & T_U \text{ Mode} \end{cases} \qquad 6.2.3.12$$

The preceding analysis assumed the ideal case for which both the load back EMF and phase impedance were known. For most practical applications, the load phase impedance is sufficiently large to allow the influence of the load on the resonant circuit to be ignored. In such cases, only the voltage divider effects need to be considered. Let I_{VD} represent the boost current component

required for a given imbalance condition in the voltage divider node potential for the special case where load interaction with the resonant circuit is ignored. An expression for I_{VD} is easily obtained by letting L_{eq} approach infinity in 6.2.3.5 and 6.2.3.7 and then substituting the results into 6.2.3.12.

$$I_{VD} = \begin{cases} \sqrt{\frac{C_R}{L_P}}\,\mathrm{Re}\left\{\left(v_{DL}(0)^2 - v_{DU}(0)^2\right)^{1/2}\right\} & T_L \text{ Mode} \\ \sqrt{\frac{C_R}{L_P}}\,\mathrm{Re}\left\{\left(v_{DU}(0)^2 - v_{DL}(0)^2\right)^{1/2}\right\} & T_U \text{ Mode} \end{cases} \qquad 6.2.3.13$$

The final step in the analysis is to express the resulting boost current requirement obtained for the special case in which none of the other factors are considered to an equivalent boost energy component. Since 6.2.3.12 and thus 6.2.3.13 do not explicitly contain references to $i_X(t)$, an equivalent boost energy can be computed under the assumption that $i_X(t)$ is zero at the onset of the corresponding mode. The well-known expression for stored magnetic energy in a linear inductor is given in 6.2.3.14. Using 6.2.3.12 in 6.2.3.14 yields the boost energy required to compensate for both load interactions and imbalance in the voltage divider node potential.

$$E_{Stored} = \tfrac{1}{2} L_R I^2 \qquad 6.2.3.14$$

where, I is the total current in the inductor.

$$E_{LVD} = \begin{cases} \frac{C_R}{2L_{Eq}}\left(L_R + L_{Eq}\right)(Arg_1)^2 & T_L \text{ Mode} \\ \frac{C_R}{2L_{Eq}}\left(L_R + L_{Eq}\right)(Arg_2)^2 & T_U \text{ Mode} \end{cases} \qquad 6.2.3.15$$

where,

$$Arg_1 = \mathrm{Re}\left\{\left(v_{DL}(0)^2 - v_{DU}(0)^2 + 2\rho_L\left(E_{Eq} - v_{DL}(0)\right)\left(v_{DL}(t_1) + v_{DU}(0)\right)\right)^{1/2}\right\}$$

$$Arg_2 = \mathrm{Re}\left\{\left(v_{DU}(0)^2 - v_{DL}(0)^2 - 2\rho_L\left(E_{Eq} - v_{DL}(0)\right)\left(v_{DU}(t_1) + v_{DL}(0)\right)\right)^{1/2}\right\}$$

Similarly, 6.2.3.16 gives the estimated boost energy required to offset imbalance in the voltage divider node potential in the special case where load interactions with the resonant circuit are ignored.

$$E_{VD} = \begin{cases} \dfrac{C_R}{2L_{Eq}}\left(L_R + L_{Eq}\right)\left(\mathrm{Re}\left\{\left(v_{DL}(0)^2 - v_{DU}(0)^2\right)^{1/2}\right\}\right)^2 & T_L \text{ Mode} \\ \dfrac{C_R}{2L_{Eq}}\left(L_R + L_{Eq}\right)\left(\mathrm{Re}\left\{\left(v_{DU}(0)^2 - v_{DL}(0)^2\right)^{1/2}\right\}\right)^2 & T_U \text{ Mode} \end{cases} \qquad 6.2.3.16$$

6.2.4 Resonant Circuit Losses

The dominant loss mechanism in the resonant circuit is the series resistance R_R associated with the resonant circuit inductor L_R [7]. The high operating frequency of the resonant circuit results in R_R being frequency dependent. Given the quality factor Q of L_R, the effective series resistance at a specified frequency f is easily computed using 6.2.4.1.

$$R_R = \frac{fL_R}{Q} \qquad 6.2.4.1$$

The current in R_R is composed of the tank circuit natural resonant current and the switched load current $i_X(t)$. The switched load current is essentially static during a T mode, which is the only time interval of interest in estimating the boost energy requirement. Using the value of R_R computed at the resonant circuit natural frequency will result in overestimation of the resonant circuit losses, due to the inclusion of $i_X(t)$ in the overall current in R_R. However, modeling R_R as a frequency dependent component in the established PRAL and SPRDL circuit models introduces undue complexities. Consequently, the policy in estimating the boost energy requirement for

resonant circuit loss compensation shall be to use a fixed value of R_R computed at the resonant circuit natural frequency and thus err conservatively.

The objective of the following computation is to estimate the energy dissipated in R_R throughout a T mode. Since the quality factor for the resonant circuit can easily exceed 100 using Litz wire [6], the voltage drop across R_R is negligible compared to that across the inductance. For the purposes of computing the energy dissipated in the resonant circuit during a T mode, assume that the T mode begins at time t = 0 and that $i_R(t) = I_X$, where $I_X = i_X(0)$. The dissipated energy is estimated using the inductor current that would exist in the absence of any loss mechanisms. A suitable expression for $i_R(t)$ is given in 6.2.4.2.

$$i_R(t) = \begin{cases} I_0 \sin(\omega t) + I_X & T_U \text{ Mode} \\ -I_0 \sin(\omega t) + I_X & T_L \text{ Mode} \end{cases} \qquad 6.2.4.2$$

where I_0 is the peak resonant current in L_R given by,

$$I_0 = \frac{V_S}{2}\sqrt{\frac{C_R}{L_R}} \qquad 6.2.4.3$$

The energy dissipated during a given half-cycle of the resonant circuit is given by,

$$E_{Disp} = \int_0^{T/2} R_R i_R^2(t)dt \qquad 6.2.4.4$$

where T is the resonant circuit period and is related to resonant circuit angular frequency by,

$$T = \frac{2\pi}{\omega} \qquad 6.2.4.5$$

Using 6.2.4.2, 6.2.4.3, and 6.2.4.5 in 6.2.4.4 produces,

$$E_{Disp} = \begin{cases} \frac{L_R}{2Q}\left(I_X^2 + 4\frac{I_0 I_X}{\pi} + \frac{I_0^2}{2}\right) & T_U \text{ Mode} \\ \frac{L_R}{2Q}\left(I_X^2 - 4\frac{I_0 I_X}{\pi} + \frac{I_0^2}{2}\right) & T_L \text{ Mode} \end{cases} \qquad 6.2.4.6$$

The estimate given in 6.2.4.6 is applicable only to the case where $i_R(t)$ equals $i_X(t)$ at the initiation of a L to T mode transition. However, the only other cases that are physically possible are those in which excess energy exists in L_R. Since it is not necessary to compensate for the dissipation of excess energy in L_R, 6.2.4.6 is entirely suitable for use in estimating the dissipation component of the total resonant circuit boost energy requirement. It should be noted that the value given by 6.2.4.6 is the estimated energy dissipated in the absence of any applied boost current. The estimate given in 6.2.4.6 is thus approximately $\frac{Q}{Q+1}$ times the actual required value, which is approximately 0.99 for practical values of Q. To properly correct for this slight discrepancy, the other boost energy components must be included as well. Since this would introduce only a minor accuracy enhancement at the expense of considerable additional complexity, any error stemming from this approximation is relegated to the fixed boost energy component.

6.2.5 Estimation of the Total Boost Current Requirement

The final step in estimating the required boost current for a given L to T mode transition is to sum the boost energy components and compute a corresponding boost current in L_R. As with the computation of the boost energy components, the estimated total boost current estimate is predicated on the resonant circuit inductor current $i_R(t)$ equaling the switched load current $i_X(t)$ at the initiation of the L to T mode transition with no boost energy applied.

Recall that in Subsection 6.2.3 an expression was given for the combined boost energy requirements associated with both load interaction and voltage divider node potential imbalance. Additionally, an expression was provided for the simplified case where only the boost energy

associated with the voltage divider node imbalance was considered. This produces the need for two separate expressions for the total boost energy. For the complete case, in which both load interaction and voltage divider potential imbalance are considered, the total boost energy is given by,

$$E_{Boost} = E_{LVD} + E_{Disp} + E_{Fixed} \qquad 6.2.5.1$$

For the simplified case, which does not require a real-time estimate of the load back EMF, the total boost energy is given by,

$$E_{Boost} = E_{VD} + E_{Disp} + E_{Fixed} \qquad 6.2.5.2$$

The total instantaneous energy stored in L_R is proportional to the square of $i_R(t)$, suggesting that the total boost current depends on both the boost energy and the existing energy stored in L_R. However, for the purpose of computing a threshold value of $i_R(t) - i_X(t)$, for which the control system should initiate an L to T mode transition, it can be assumed that $i_R(t)$ equals $i_X(t)$ just prior to application of the boost energy to L_R and that $i_X(t)$ remains constant from the point at which boost energy infusion begins to the end of the corresponding T mode. Moreover, the voltage across R_R is negligible compared to that across L_R when the boost energy is transferred to L_R. Thus, the current responsible for driving the auxiliary link voltage between the power matrix rail potentials is $i_R(t) - i_X(t)$, rather than $i_R(t)$. Consequently, the total boost current is simply the current corresponding to a stored energy level in L_R equal to E_{Boost}. It follows that L to T mode transitions should be initiated when the appropriate relationship is given by either 6.2.5.3 or 6.2.5.4.

$$i_R(t) - i_X(t) \leq -\sqrt{\frac{2E_{Boost}}{L_R}} \quad L_U \rightarrow T_L \qquad 6.2.5.3$$

$$i_R(t) - i_X(t) \geq \sqrt{\frac{2E_{Boost}}{L_R}} \quad L_L \rightarrow T_T \qquad 6.2.5.4$$

The general expression for the boost current, I_{Boost}, which is defined as nonnegative for all L to T mode transitions, is thus,

$$I_{Boost} = \sqrt{\frac{2E_{Boost}}{L_R}} \qquad 6.2.5.5$$

6.2.6 Device Turn-Off Current Effects on Boost Current Requirements

This section addresses the impact of the switching device turn-off currents that exist for a short time after the initiation of each L to T mode transition. The net result of these currents is an effective amplification of the boost current. Consequently, the total boost current requirement estimated in the preceding subsection, which ignored device turn-off current effects, can be reduced, potentially lowering switching losses. Recognizing that the resonant circuit dynamics are identical for both the cases where turn-off currents do and do not exist, once the turn-off currents subside, suggests a procedure for determining the actual boost current requirement.

Consider the two simplified models of the PRAL resonant circuit shown in Figures 55 and 56. The model in Figure 55 corresponds to the case where turn-off currents do not exist, as was the case in the preceding subsections. In contrast, figure 56 depicts the case where turn-off currents exist with the cumulative net turn-off current between the auxiliary link and the power matrix modeled as a current source with current $i_{TO}(t)$. In both models, resonant circuit losses are ignored, a constant switched load current I_X is assumed, and the voltage divider node potential is assumed balanced. The state variables associated with the model shown in Figure 56 are designated with primes to distinguish them from those in Figure 55. In both cases, it is assumed

that an L_U to T_L mode transition occurs at time t = 0, $I_X = i_X(0)$, and both $v_R(t)$ and $v'_R(t)$ oscillate between $\pm\frac{1}{2}V_S$.

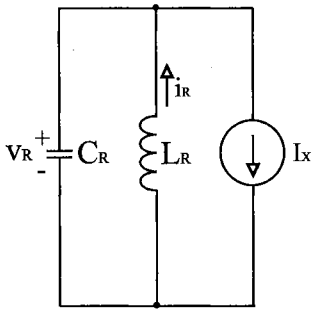


Figure 55. Simplified model of the PRAL resonant circuit without switching device turn-off currents

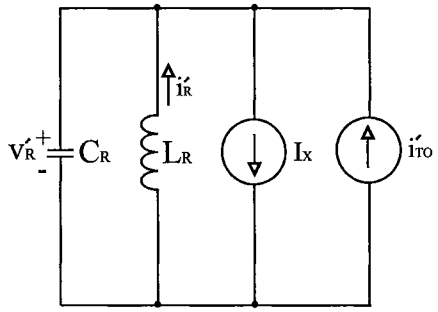


Figure 56. Simplified model of the PRAL resonant circuit with switching device turn-off currents

To begin the analysis, consider the circuit shown in Figure 56. Assume that the cumulative turn-off current $i'_{TO}(t)$ decays linearly to zero with time constant T_{TO} from an initial value equal to the net current between the auxiliary link and the power matrix existing at t = 0, as given in 6.2.6.1.

$$i'_{TO}(t) = \begin{cases} \left(I_X - i'_R(0)\right)\left(1 - \dfrac{t}{T_{TO}}\right) & t \in [0, T_{TO}] \\ 0 & \text{Otherwise} \end{cases} \qquad 6.2.6.1$$

The governing differential equations for the circuit model are:

$$\frac{di'_R}{dt} = \frac{-v'_R}{L_R} \qquad 6.2.6.2$$

$$\frac{dv'_R}{dt} = \frac{i'_R - I_X + i'_{TO}}{C_R} \qquad 6.2.6.3$$

For the L_U to T_L mode transition occurring at time t = 0, the initial conditions are:

$$v'_R(0) = \frac{V_S}{2}$$

$$i'_R(0) - I_X < 0$$

Differentiating 6.2.6.3 with respect to time and using 6.2.6.1 and 6.2.6.2 results in the following second order differential equation for $v'_R(t)$ in the interval [0, T_{TO}].

$$\frac{dv'^2_R}{dt^2} = \frac{1}{C_R}\left(\frac{i'_R(0) - i'_{TO}}{T_{TO}} - \frac{v'_R}{L_R}\right) \qquad 6.2.6.4$$

Solving 6.2.6.4 for $v'_R(t)$ subject to the initial conditions results in,

$$v'_R(t) = \left(\frac{V_s}{2} - \frac{L_R}{T_{TO}}\left(i'_R(0) - I_X\right)\right)\cos(\omega t) + \frac{L_R}{T_{TO}}\left(i'_R(0) - I_X\right) \quad t \in [0, T_{TO}] \qquad 6.2.6.5$$

where,

$$\omega = \frac{1}{\sqrt{C_R L_R}}$$

Using 6.2.6.5 in 6.2.6.3 solve for $i'_R(t)$ produces,

$$i'_R(t) = \left(1 - \frac{t}{T_{TO}}\right)\left(i'_R(0) - I_X\right) - \sqrt{\frac{C_R}{L_R}}\left(\frac{V_s}{2} - \frac{L_R}{T_{TO}}\left(i'_R(0) - I_X\right)\right)\sin(\omega t) + I_X \quad t \in [0, T_{TO}] \qquad 6.2.6.6$$

Now consider the case where there are no turn-off currents, as depicted in Figure 55 and for which 6.2.5.9 gives the conditions under which an L_U to T_L mode transition is allowed. The strategy to be employed is to find $i'_R(0)$ such that $v_R(t) = v'_R(T_{TO})$ and $i_R(t) = i'_R(T_{TO})$ for some $t \in (0, t_L)$, where t_L is the smallest value of $t > 0$ for which $v_R(t) = -\frac{1}{2}V_S$. This task is simplified if the cumulative energies stored in the resonant circuit elements of both Figures 55 and 56 are viewed as consisting of two distinct components when turn-off currents are not present.

In both models, the voltage and current associated with C_R are independent of the constant current I_X, which is conducted exclusively through L_R. Thus for Figure 55, the cumulative energy stored in the resonant circuit is composed of a constant component E_C plus a dynamic component $E_D(t)$ associated with the energy exchanged between L_R and the I_X current source. A similar situation exists for the case of Figure 56 once the device turn-off currents have decayed to zero. In this case, the constant and dynamic resonant circuit energy components are denoted as E'_C and $E'_D(t)$, respectively. It follows that E_C and E'_C can be calculated at any time t for which $v_R(t)$ and $i_R(t)$ are known and in the case of E'_C, when no turn-off currents are present. Thus, E_C can be evaluated at t = 0 and expressed as,

$$E_C = \frac{C_R V_S^2}{8} + \frac{L_R (i_R(t) - I_X)}{2} \qquad 6.2.6.7$$

Similarly, E'_C can be computed at $t = T_0$ using 6.2.6.5 and 6.2.6.6, and after simplification, expressed as,

$$E'_C = \frac{C_R L_R^2}{T_{TO}^2}(i'_R(0) - I_X)^2(1 + \cos\omega T_{TO}) + \frac{C_R V_S^2}{8} \qquad 6.2.6.8$$

The next step is to set E_C equal to E'_C and solve for $i'_R(0)$ in terms of $i_R(0)$. Equating 6.2.6.7 to 6.2.6.8 results in,

$$(i'_R(0)-I_X)^2-\frac{V_S T_0}{2L_R}(i'_R(0)-I_X)-\frac{T_0^2(i_R(0)-I_X)^2}{2C_R L_R(1-\cos(\omega T_0))}=0 \qquad 6.2.6.9$$

Solving for $i'_R(0)-I_X$ result in,

$$i'_R(0)-I_X=\frac{V_S T_0}{4L_R}\left(1-\sqrt{1+\frac{4L_R(i_R(0)-I_X)^2}{C_R V_S^2 \sin\frac{\omega T_0}{2}}}\right) \qquad 6.2.6.10$$

The preceding expression was computed for the case of an L_U to T_L mode transition. Moving I_X to the right side of the expression and employing symmetry to obtain a similar expression for the case of an L_L to T_U mode transition produces the desired result of this subsection given in 6.2.6.11.

$$i'_R(0)=\begin{cases} I_X+\frac{V_S T_0}{4L_R}\left(1-\sqrt{1+\frac{4L_R(i_R(0)-I_X)^2}{C_R V_S^2 \sin\frac{\omega T_0}{2}}}\right) & L_U \rightarrow T_L \\ I_X-\frac{V_S T_0}{4L_R}\left(1-\sqrt{1+\frac{4L_R(i_R(0)-I_X)^2}{C_R V_S^2 \sin\frac{\omega T_0}{2}}}\right) & L_L \rightarrow T_U \end{cases} \qquad 6.2.6.11$$

In either case described in 6.2.6.11, $i'_R(0)$ is the estimated actual inductor current required for a given L to T mode transition initiated at time t = 0 when turn-off current effects are present.

6.3 The PRAL Voltage Divider Regulation Problem

6.3.1 Introduction

Unlike conventional and PRDL inverter designs, the PRAL resonant circuit requires an auxiliary voltage source to bias the auxiliary voltage approximately half way between the power matrix rail potentials. The implementation proposed for this source in Chapter V replaces the traditional power matrix shunt capacitor with a center-tapped capacitor arrangement. The resulting voltage divider node potential is a state variable of the inverter circuit and is therefore subject to disturbance mechanisms. If the node voltage is allowed to deviate substantially from its nominal potential, the low switching device current stress levels predicted in the Chapter V may not be realized. For example, suppose the voltage divider becomes unbalanced to the point that $v_{DU} = 4v_{DL}$. In order for a T_U mode transition to complete under this condition, a boost current equal to 96.8% of the peak "free running" resonant circuit current, I_0, is required to drive $v_{Alink}(t)$ to the lower rail potential.

The functionality of the PRAL resonant circuit is very similar to that of PRDL designs, which are typically designed with I_0 equal to two to three times the inverter's rated instantaneous load current, I_L. Moreover, any inequality between v_{DU} and v_{DL} increases the effective resonant circuit period and thus decreases the inverter's effective switching frequency. Consequently, it is necessary to integrate stabilization mechanisms into the PRAL design so that the voltage divider node potential remains near the midpoint of the upper and lower rail potentials.

The objective of this section is to address the major disturbance mechanisms affecting the PRAL voltage divider node potential and to explore candidate stabilization techniques in sufficient detail to permit meaningful simulation experiments to be conducted in Chapter VIII. A more in-depth investigation, which from a practicality perspective requires data from hardware prototype experiments, is left to future efforts dedicated specifically to this topic.

6.3.2 Voltage Divider Node Disturbances and Candidate Stabilization Mechanisms

Like conventional and PRDL inverters, the PRAL inverter incorporates a large capacitance in shunt with the power matrix rails to squelch the rail-to-rail voltage transients that would otherwise result from power matrix state transitions. The shunt capacitance often serves a second role as a short-term energy reservoir in cases where the source energy is pulsed, such as when an AC source is feeding the inverter through a rectifier. The characteristics of the DC voltage source feeding the inverter and the commanded energy transfer between the inverter and the load primarily determine the instantaneous energy stored in the shunt capacitance. Consequently, the power matrix rail-to-rail voltage is a direct function of the energy stored in the shunt capacitance.

For the PRAL inverter, the stored energy is the cumulative energy stored in capacitors C_{DU} and C_{DL}, which form the center-tapped capacitance arrangement used to bias the PRAL resonant circuit. Unlike the cumulative energy, which primarily depends upon mechanisms that are external to the inverter, the distribution of the cumulative energy amongst C_{DU} and C_{DL} is inherently dependent upon mechanisms internal to the inverter. The difference in potential between the PRAL voltage divider node and the upper and lower power matrix rail potentials is a direct function of the difference in the energy stored in C_{DU} and C_{DL}. Consequently, the problem of regulating the voltage divider node potential can be attacked from the perspective of regulating the distribution of energy stored in C_{DU} and C_{DL}.

Any mechanism capable of producing charge flow out of the voltage divider node is, by definition, capable of disturbing the distribution of energy amongst C_{DU} and C_{DL}. Positive charge transfer out of the voltage divider node constitutes an increase in the ratio of energy in C_{DU} to that in C_{DL} while a negative charge transfer out of the voltage divider node decreases the same ratio. All charge transferred out of the voltage divider node must flow through either C_R or L_R. Since C_R is normally several orders of magnitude less than either C_{DU} or C_{DL} and does not constitute a DC path, the path through C_R can be ignored for the purposes of studying accumulating perturbations

in the voltage divider node potential. In contrast, L_R forms a DC path between the voltage divider node and the power matrix. Accordingly, the net accumulated charge passing through L_R is responsible for any significant imbalance in the voltage divider node potential. Let $\Phi(t)$ be the net cumulative charge that has from the voltage divider node through L_R up until time t, as defined in 6.3.1.

$$\Phi(t) = \int_{-\infty}^{t} i_R(\tau) d\tau \qquad 6.3.1$$

There are two dominant disturbance mechanisms for the PRAL voltage divider potential. One is closely associated with the PRAL inverter's L modes while the other is tied to the T modes. These mechanisms are denoted as L mode disturbances and T mode disturbances, respectively, and are qualitatively described next.

The sign of $\frac{di_R}{dt}$ is always negative when a PRAL inverter is in the L_U mode and always positive when it is in the L_L mode. The commanded boost current level for a given L mode affects the value of $\Phi(t)$ at the end of the L mode. $\Phi(t)$ becomes more positive at the end of a given L_L mode and more negative at the end of a given L_U mode if the boost current is increased beyond the value required for the subsequent T mode. Since $\Phi(t)$ is equal to the net charge removed from the voltage divider node, a candidate mechanism for affecting the voltage divider node potential is to selectively increase the boost current beyond the required level.

Net disturbances in the voltage divider node potential occur in the T mode when the power matrix is changing states and at least one of the states involved is an active state. When a PRAL inverter is executing such a transition, the net change in $\Phi(t)$ is equal to the integral of $i_x(t)$ over the course of the T mode. This assumption ignores the effects of device turn-off currents. As in previous discussions, assume that the load impedance and state transition time are such that $i_x(t)$ is constant with value I_X throughout a given T mode. The magnitude of change in $\Phi(t)$ over a T

mode is decreased if the mode duration is decreased and increased if the mode duration is increased. The magnitude of the disturbance affecting the voltage divider node potential for a given T mode is proportional to the change in $\Phi(t)$. Consequently, a controllable mechanism capable of changing the duration of a T mode is a candidate mechanism for regulating the voltage divider potential.

There are two readily apparent mechanisms capable of affecting the duration of a T mode. Additional circuitry could be added to the resonant circuit to alter its resonant frequency upon command. For example, a switched capacitor or inductor could be placed in shunt with the tank circuit to shift the natural resonant frequency as required. Unfortunately, this approach adds considerable complexity and cost to the PRAL design. An alternative approach is to increase the boost current beyond the value required to ensure the subsequent T to L mode transition. This would increase the unconstrained voltage swing of the tank circuit, effectively increasing the magnitude of the first time derivative of the auxiliary link potential throughout the T mode. Like the similar use of boost current described for the L modes, this method requires no additional circuitry. Unfortunately, there is no counterpart to this approach for extending the T mode duration since the boost current can not be reduced below the level required to complete the T mode transition.

Employing boost current control to regulate the PRAL voltage divider node potential is highly attractive due to the absence of additional required circuitry. Unfortunately, what has not been considered are the facts that the L mode boost current is, by definition, the boost current associated with subsequent T mode and that any excess boost current is carried into the subsequent L mode. Thus, opportunities to affect the voltage divider potential occur only once per resonant circuit half-cycle and influence the voltage divider potential throughout an L-T-L mode sequence rather than a single L or T mode. Furthermore, increasing the boost current associated with a given L to T mode transition may produce opposing results in the L and T modes. Table II

lists the net effects on the PRAL voltage divider node potential during an L-T-L mode sequence that will result from elevating the boost current under the conditions shown.

TABLE II

EFFECTS OF ADDITIONAL BOOST CURRENT ON THE PRAL VOLTAGE DIVIDER NODE

Mode Transition	$^*I_x$	L Mode Effect on $v_{DU} - v_{DL}$	T Mode Effect on $v_{DU} - v_{DL}$
$L_U \rightarrow T_L$	$I_x < 0$	< 0	> 0
$L_U \rightarrow T_L$	$I_x \geq 0$	< 0	< 0
$L_L \rightarrow T_U$	$I_x > 0$	> 0	> 0
$L_L \rightarrow T_U$	$I_x \geq 0$	> 0	< 0

Table II depicts the two cases in which elevating the boost current produces opposing disturbance effects in the associated L and T modes, specifically, the first and last rows in the table. The analysis needed to determine the net cumulative effect of increasing the boost current in each of these cases is complex and produces solutions in the form of transcendental equations. As a practical matter, any such solutions would have to be sampled and then stored in a look-up table for real-time control implementation. Simulation experiments conducted for a range of PRAL inverter designs clearly indicate that L mode effects dominate those of the T modes. However, further work, which is deferred to future efforts, is required to conclusively establish this tendency. The policy adopted in this work shall be to assume that L mode effects on $\Phi(t)$ always dominate those of the associated T mode. Table III lists the conditions under which the boost current may and may not be elevated under this policy. The entries enclosed in parentheses correspond to the cases in which the L mode and T mode effects differ in sign. These cases may

be exploited in future efforts to enhance the boost current control method. The entries without surrounding parentheses represent the cases in which the L and T mode produce disturbances with the same sign and for which the effect of boost current elevation is clearly defined. The decision whether or not to increase the boost current for each of these cases is clearly deducible from the decision variables indicated in the first three columns of the table.

TABLE III

DECISION TABLE FOR THE APPLICATION OF ADDITIONAL BOOST CURRENT FOR THE PURPOSE OF STABILIZING THE VOLTAGE DIVIDER NODE POTENTIAL

Mode Transition	$v_{DU} - v_{DL}$	i_x	Use Additional Boost Current
$L_U \rightarrow T_L$	< 0	< 0	*(No)
$L_U \rightarrow T_L$	< 0	≥ 0	No
$L_U \rightarrow T_L$	≥ 0	< 0	*(Yes)
$L_U \rightarrow T_L$	≥ 0	≥ 0	Yes
$L_L \rightarrow T_U$	< 0	< 0	Yes
$L_L \rightarrow T_U$	< 0	≥ 0	*(Yes)
$L_L \rightarrow T_U$	≥ 0	< 0	No
$L_L \rightarrow T_U$	≥ 0	≥ 0	*(No)

* Values in parenthesis indicate conditions under which L and T mode effects are in opposition

Three questions remain to be answered. First, under what conditions should corrective actions be taken to drive the voltage divider potential toward its nominal value? Second, how much should the boost current be elevated? Third, what should be done if the boost current elevation technique acting alone is incapable of stabilizing the voltage divider node potential? To begin, a

correction applied over the course of single L-T-L mode sequence should not be so great that the sign of the voltage divider potential error is changed, since this would promote "chattering." This requires that the result of a given correction be known prior to its initiation. The control logic needed for this capability is undesirable from a cost perspective. However, a simple alternative is to apply a correction only when the magnitude of the maximum attainable change in the voltage divider node potential error is less than the magnitude of the error. The conditions for this arrangement are easily computed using the PRAL inverter component parameters. To further reduce the possibility of instilling unnecessary "chattering" in the voltage divider node potential, a correction should be applied only if $|v_{DL}(t) - v_{DU}(t)| > V_{DAT}$, where V_{DAT} is a fixed threshold voltage that is sufficiently large to guarantee that several consecutive like-sign corrections are needed to drive $v_{DL}(t) - v_{DU}(t)$ to zero.

Arguments were made in Chapter V that the current stress in all of the PRAL inverter switching devices is limited to the peak load current, I_L, with the possible exception of the final moments of the L modes. As boost current is applied to L_R during the L modes, one or more power matrix switches may conduct its associated load current plus all or part of the applied boost current. Fortunately, this condition only occasionally results in device current stress levels greater than I_L and when it does, device surge current capacity can be exploited to negate any detrimental effects. First, the surge current ratings of most self-extinguishing devices are 2-4 times greater than their continuous current ratings. Secondly, the permitted device surge current duration is typically much greater than the 1-5 μs needed to apply boost current in most PRAL inverter designs. For a conservative PRAL inverter design, the continuous current rating of each switching device equals or exceeds the rated peak load current, I_L. Consequently, limiting the applied boost current to the specific device surge current rating minus I_L removes any potential device current stress penalties in most cases.

The preceding discussions were predicated on exclusively relying on the boost current elevation technique to stabilize the voltage divider node potential. If this method is incapable of

stabilizing the voltage divider node potential under certain conditions, a secondary stabilization mechanism will be needed to sustain the operational viability of the inverter. Suppose that whenever $|v_{DL}(t) - v_{DU}(t)|$ exceeds a prescribed threshold V_{DBT}, where $V_{DBT} > V_{DAT}$, state transitions are blocked if their associated switched load current, $i_X(t)$, would exacerbate the voltage divider node potential error. The proposed strategy is to block power matrix state transitions whenever $v_{DU}(t) - v_{DL}(t) > V_{DBT}$ and $i_X(t) > 0$ or whenever $v_{DL}(t) - v_{DU}(t) > V_{DBT}$ and $i_X(t) < 0$. Ideally, this arrangement guarantees that the auxiliary link will operate as a unidirectional "charge pump" for stabilizing the voltage divider node potential until the error returns to within acceptable limits, i.e. V_{DBT}. Unfortunately, blocking commanded state transitions would adversely affect the inverter's output waveform quality. Thus, it may be more appropriate to block only a fraction of all such offending state transitions. For example, the control logic could be configured to honor a larger fraction of blocking requests as $|v_{DU}(t) - v_{DL}(t)|$ increases beyond V_{DBT}.

Although a kaleidoscope of alternative techniques exist, the strategy employed to stabilize the voltage divider node potential throughout the remainder of this work is based on the preceding discussions. For the primary stabilization mechanism, the boost current value is elevated to the rated load current, I_L, for a given L to T mode transition whenever $|v_{DL}(t) - v_{DU}(t)| > V_{DAT}$ is satisfied and Table III indicates that elevating the boost current would tend to correct the imbalance condition. For the secondary stabilization mechanism, commanded state transitions are blocked according to the prescription given in Table IV. Although not indicated in the table, blocking is handled separately for the case where $v_{DU}(t) - v_{DL}(t) > V_{DBT}$ and for the case where $v_{DL}(t) - v_{DU}(t) > V_{DBT}$.

TABLE IV

STATE TRANSITION BLOCKING CRITERIA FOR STABILIZING THE VOLTAGE DIVIDER NODE POTENTIAL

Voltage Divider Potential Error	$i_X(t)$	Fraction of Blocked State Transitions
$\lvert v_{DU} - v_{DL} \rvert < V_{DBT}$	N/A	NONE
$V_{DBT} < v_{DU} - v_{DL} \leq 2V_{DBT}$	> 0	1 of 3
$2V_{DBT} < v_{DU} - v_{DL} \leq 3V_{DBT}$	> 0	2 of 3
$3V_{DBT} < v_{DU} - v_{DL}$	> 0	ALL
$V_{DBT} < v_{DL} - v_{DU} \leq 2V_{DBT}$	< 0	1 of 3
$2V_{DBT} < v_{DL} - v_{DU} \leq 3V_{DBT}$	< 0	2 of 3
$3V_{DBT} < v_{DL} - v_{DU}$	< 0	ALL

6.3.3 Maximum Average PRAL Charge Transfer Current

This subsection examines the influence of the resonant circuit component values L_R and C_R on the ability of the PRAL resonant circuit to function as a charge pump between the PRAL voltage divider node and the power matrix. More specifically, the objective is to obtain an expression for the maximum net average current, I_{Pump}, that can be induced when the PRAL is exclusively used as a charge pump for balancing the voltage divider potential. In order to remove extraneous factors, it is further assumed that the voltage divider node potential is balanced, the resonant circuit is loss free, and the switching devices are ideal.

Figure 57 shows a simplified PRAL circuit model stemming from the above simplifying assumptions. The case considered for the analysis attempts to produce the maximum attainable net current directed toward the voltage divider node without producing current levels in any of the switches that exceed the inverter's rated instantaneous load phase current, I_L. Since there are

no power matrix state transitions, this case corresponds to a boost current equal to I_L being applied to the L_U - T_L mode transitions and no boost current being applied to the L_L - T_U transitions. As discussed in Chapter V, this ensures that the switching device current is limited to I_L.

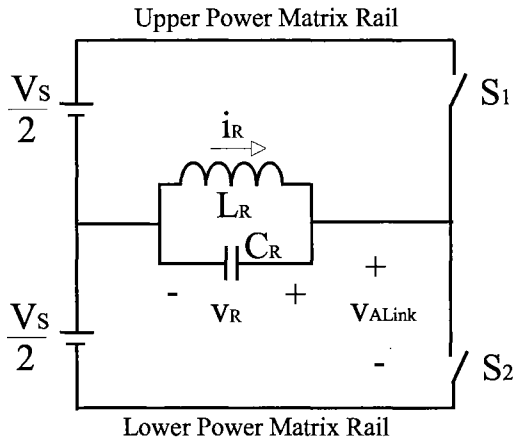


Figure 57. Simplified PRAL circuit model for computing I_{Pump}

Suppose that at time t_0 Switch S_1 is closed, Switch S_2 is open, and the values of v_R and i_R are $\frac{1}{2}V_S$ and zero, respectively. Figures 58 and 59 show plots of $v_R(t)$ and $i_R(t)$, respectively. Referring to Figure 58, at time t_1 i_R falls to $-I_L$ and Switch S_1 opens, initiating the T_L mode. Figure 59 shows the voltage across the resonant circuit falling to zero at t_2 and subsequently to $-\frac{1}{2}V_S$ at t_3, at which time Switch S_2 is closed, ending the T_L mode. Since the resonant circuit is ideal and the objective is to produce a net current directed toward the voltage divider node, no boost current is applied in the L_L mode. Once i_R reaches zero, S_2 is opened, marking the L_L to T_U mode transition. Both the T_U mode and the resonant cycle conclude at time t_5 with $v_R(t)$ and $i_R(t)$ equaling $\frac{1}{2}V_S$ and zero, respectively.

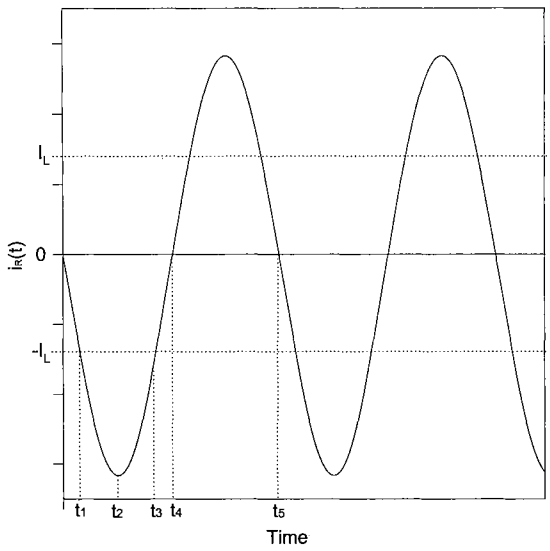


Figure 58. Resonant circuit voltage for the PRAL circuit being operated as a charge pump

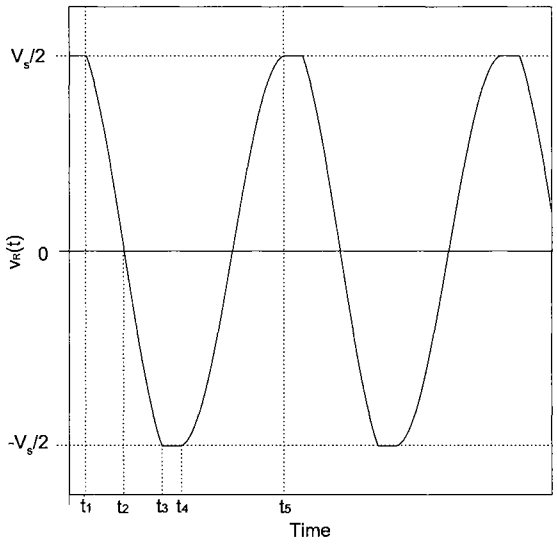


Figure 59. Resonant circuit current for the PRAL circuit being operated as a charge pump

The computation of I_{Pump} requires the calculation of the PRAL cycle period and the net charge transferred between the voltage divider node and the power matrix over the course of a single PRAL cycle. Since the switching devices are assumed ideal, charge transfer between the voltage divider node and the power matrix occurs only during the L_U and L_L modes, or more specifically,

during time intervals $[t_0, t_1]$ and $[t_3, t_4]$. Furthermore, the charge transferred during time interval $[t_3, t_4]$ is equal to that during time interval $[t_0, t_1]$ since the resonant circuit is loss free and the voltage divider potential is balanced.

Consider the first time interval, $[t_0, t_1]$. The boundary conditions for $i_R(t)$ and $v_R(t)$ are given by,

$$i_R(t_0) = 0 \qquad 6.3.3.1$$

$$i_R(t_1) = - I_L \qquad 6.3.3.2$$

$$v_R(t) = \frac{V_S}{2}, t \in [t_0, t_1] \qquad 6.3.3.3$$

From inspection of Figure 55, $i_R(t)$ is given by,

$$i_R(t) = -\frac{V_S}{2L_R}(t - t_0) \quad t \in [t_0, t_1] \qquad 6.3.3.4$$

For convenience and without loss of generality, let $t_0 = 0$ and solve for t_1.

$$t_1 = \frac{2I_L L_R}{V_S} \qquad 6.3.3.5$$

Now consider the second time interval, $[t_1, t_2]$. The boundary conditions on $v_R(t)$ and the initial condition for $i_R(t)$ are given by,

$$v_R(t_1) = \frac{V_S}{2} \qquad 6.3.3.6$$

$$v_R(t_2) = 0 \qquad 6.3.3.7$$

$$i_R(t_1) = -I_L \qquad 6.3.3.8$$

From inspection of Figure 55, the differential equations applicable to this interval are:

$$\frac{dv_R}{dt} = \frac{i_R}{C_R} \qquad 6.3.3.9$$

$$\frac{di_R}{dt} = -\frac{v_R}{L_R} \qquad 6.3.3.10$$

Solving 6.3.3.9 and 6.3.3.10 and then isolating $t_2 - t_1$ results in,

$$t_2 - t_1 = \frac{1}{\omega}\tan^{-1}\left(\frac{V_S}{2I_L Z_0}\right) \qquad 6.3.3.11$$

where,

$$\omega = \frac{1}{\sqrt{L_R C_R}} \qquad 6.3.3.12$$

$$Z_0 = \sqrt{\frac{L_R}{C_R}} \qquad 6.3.3.13$$

By symmetry $t_3 - t_2 = t_2 - t_1$, resulting in $t_3 - t_1$ being given by,

$$t_3 - t_1 = \frac{2}{\omega}\tan^{-1}\left(\frac{V_S}{2I_L Z_0}\right) \qquad 6.3.3.14$$

The symmetry stemming from the loss-free resonant circuit and balanced voltage divider node assumptions leads to $t_4 - t_3 = t_1 - t_0$, and thus,

$$t_4 - t_3 = \frac{2I_L L_R}{V_S} \qquad 6.3.3.15$$

Finally, since the resonant circuit is unrestricted and is undamped for all $t \in [t_4, t_5]$,

$$t_5 - t_4 = \frac{\pi}{\omega} \qquad 6.3.3.16$$

The period of a complete PRAL pumping cycle, T_{Pump}, is equal to $t_5 - t_0$ and is given by,

$$T_{Pump} = \frac{4I_L L_R}{V_S} + \frac{1}{\omega}\left(\pi + 2\tan^{-1}\left(\frac{V_S}{2I_L Z_0}\right)\right) \qquad 6.3.4.17$$

The average pumped charge per PRAL cycle is equal to the charge transferred between the voltage divider node and the power matrix during intervals $[t_0, t_1]$ and $[t_3, t_4]$ divided by T_{Pump}. Integrating $i_R(t)$ over these two intervals and then summing produces the net charge pumped per cycle, Q_{Pump}.

$$Q_{Pump} = -\frac{2I_L^2 L_R}{V_S} \qquad 6.3.3.18$$

Dividing 6.3.4.18 by 6.3.4.17 yields the magnitude of the maximum average current, I_{Pump}, that can be established between the voltage divider node and the power matrix using the boost current elevation technique.

$$I_{Pump} = \frac{I_L}{2 + \frac{I_0}{I_L}\left(\pi + 2\tan^{-1}\left(\frac{I_0}{I_L}\right)\right)} \qquad 6.3.3.19$$

Where, I_0 is the peak unrestricted resonant circuit current given by,

$$I_0 = \frac{V_S}{2}\sqrt{\frac{C_R}{L_R}} \qquad 6.3.3.20$$

Figure 62 illustrates the relationship between I_{Pump} and I_0 for a given value of I_L, as described in 6.3.3.19. The figure shows that as the ratio of I_0 to I_L approaches infinity, the ability to use the elevated boost current technique to transfer charge between the voltage divider node and the power matrix vanishes. This is consistent with the fact that as I_L approaches zero for a given I_0, so

does the maximum boost current that can be applied. For the opposite extreme, in which the ratio of I_0 to I_L approaches zero, I_{Pump} approaches $\frac{1}{2} I_L$ from below. In this case, the fraction of each PRAL cycle spent in an L mode approaches unity. Since the magnitude of i_R varies linearly between zero and I_L during each L mode, the average magnitude of $i_R(t)$ during both the L_U and L_L modes is $\frac{1}{2} I_L$. Hence, the limiting value of $\frac{1}{2} I_L$ for I_{Pump}. The practical significance of 6.3.3.19 is that it suggests how L_R and C_R might be modified to increase the ability of a given PRAL inverter design to better stabilize its voltage divider node potential via the boost current elevation technique.

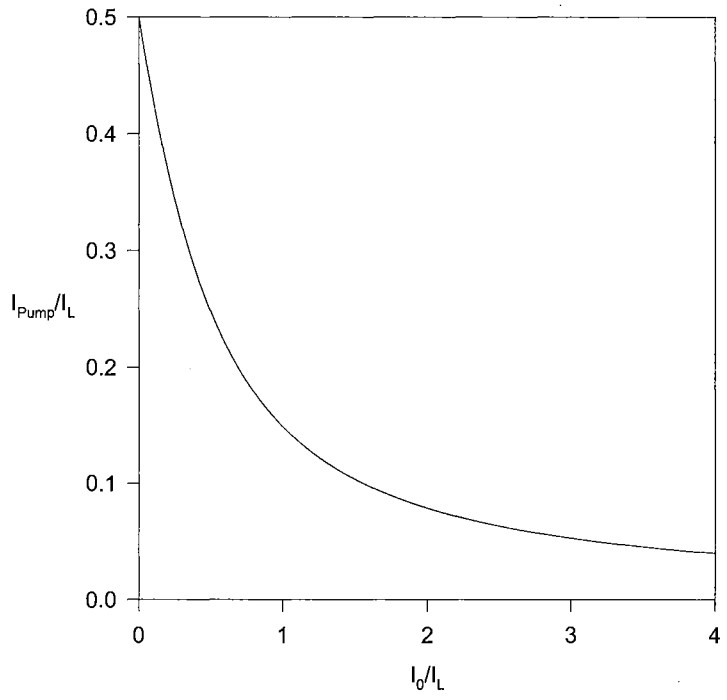


Figure 60. Dependency of I_{Pump} on the unrestricted peak resonant circuit current I_0 in relation to the rated peak load phase current I_L

6.4 The Component Selection Problem

6.4.1 Introduction

Like conventional and PRDL inverters, the problem of selecting appropriate component parameter values for the PRAL inverter is subject to several application specific requirements. Application requirements uniquely determine some component parameter values while others are free to be selected within the context of some optimization strategy. The major PRAL inverter component parameters are the voltage and current ratings of the switching devices, the resonant circuit inductor and capacitor value, the value of the voltage divider capacitors, and the turn-off times of the switching devices. The dominant application requirements driving the component parameter selection process are the DC source voltage, the required output waveform quality, the rated load voltage, and the maximum load KVA rating. Since the PRAL inverter fully utilizes both the voltage and current ratings of its switching devices, the load voltage, load KVA rating, and DC source voltage uniquely determine the required voltage and current rating of all switching devices. In contrast, the required output waveform quality can be satisfied using a variety of load control strategies, and thus a variety of auxiliary link frequencies. Once a control strategy is chosen and the minimal effective frequency for the auxiliary link is established, a considerable degree of flexibility remains in the selection of the remaining component parameter values.

The component parameters that are not uniquely determined by the application requirements are the voltage divider capacitor values C_{DU} and C_{DL}, the turn-off time of the switching devices, and interestingly, the resonant circuit characteristic impedance, $\sqrt{\frac{L_R}{C_R}}$. The complexity of the power matrix state trajectories place the development of any closed form analytical expressions for these parameters outside the scope of this preliminary work. This necessitates the use of modeling and simulation to determine optimal component parameter values.

Some form of optimization strategy is required to guide component parameter value adjustment during the simulation based design process. For example, one solution is to choose the component parameter values so that the overall conversion efficiency is maximized. Another strategy might be to minimize the inverter's weight or volume. Finally, the component parameter values could be optimized to allow the use of relatively inexpensive switching devices, which characteristically have substantially larger turn-off times than more expensive devices with comparable voltage and current ratings.

The remainder of this section examines previously described PRAL inverter characteristics that provide insight into how the resonant circuit inductor and capacitor values should be adjusted to satisfy the fundamental operating requirements of the PRAL topology. Additionally, a discussion of the voltage divider capacitance and switching device turn-off time selection problem is included along with a suggested method for finding suitable "first cut" values for these parameters.

6.4.2 Resonant Circuit Component Selection and Adjustment

The task of selecting appropriate values for L_R and C_R ultimately results in finding values that satisfy the selected output waveform quality criteria and reasonably support the selected optimization strategy. In essence, this means initially selecting an average auxiliary link frequency that satisfies the output waveform quality requirement and then finding values of L_R and C_R that yield the target auxiliary link frequency. This procedure is straightforward except for one major problem, the average auxiliary link frequency is not a valid metric for guaranteeing equivalent output waveform quality from two different sets of L_R and C_R values. Different sets of L_R and C_R values can produce the same average auxiliary link frequency but interact with the control system in such a way that the output waveform quality is substantially different. Unfortunately, there is no readily apparent alternative to using the average auxiliary link frequency as a reference point when adjusting L_R and C_R during attempts to reduce switching

losses. However, it is worth noting that there is no procedure in the extensive PRAL inverter literature for determining the required resonant link frequency needed to produce an output waveform of a specified quality. To this end, specifying the average frequency of the auxiliary link is only a means of selecting initial "first cut" values for L_R and C_R.

The values of L_R and C_R determine far more than the average frequency of the auxiliary link. The ratio of L_R to C_R determines the variability in the duration of the auxiliary link half-cycle that results from changes in the power matrix state. Moreover, the previous section argued that the ability of the PRAL circuit to offset disturbances in the voltage divider node potential increases as $\frac{L_R}{C_R}$ increases. Since the design proposed in this work relies on the ability of the PRAL circuit acting alone to regulate the voltage divider potential, this imposes a lower bound on $\frac{L_R}{C_R}$. Finally, 6.2.3.12 shows that boost current requirements decrease as $\frac{L_R}{C_R}$ increases. In contrast, it was previously argued that switching losses increase as $\frac{L_R}{C_R}$ increases, due to the fact that the value of $\left|\frac{dv_{ALink}}{dt}\right|$ during the T modes increases with increasing $\frac{L_R}{C_R}$.

The process of initially selecting and then adjusting L_R and C_R to satisfy a given optimization strategy is relatively straightforward. Accumulated experience with the PRAL inverter will most likely provide guidance in selecting a candidate average frequency for the auxiliary link that satisfies the output waveform quality requirements. Given that the auxiliary link voltage waveform must be approximately sinusoidal, per the soft-switched inverter design guidelines presented in Chapter IV, a reasonable "first cut" value for L_RC_R is that corresponding to a loss-free tank circuit oscillating at the selected average auxiliary link frequency. A second guideline for selecting initial values of L_R and C_R comes from preliminary simulation results that suggest using a value of $\frac{L_R}{C_R}$ that produces a peak current in L_R equal to $2I_L$ when the resonant circuit is

oscillating freely and is unperturbed by load interactions. These two conditions taken together readily yield "first-cut" values for L_R and C_R.

Although the auxiliary link behavior primarily depends on L_R and C_R, the voltage divider capacitors become functionally relevant if their capacitance values are less than about two orders of magnitude larger than C_R. The next subsection describes a simple procedure for determining appropriate capacitance values for the voltage divider capacitors. For the remainder of this section, however, it is necessary to obscure the effects of these capacitors on the operation of the auxiliary link negligible. The voltage divider capacitors used in this phase of the simulation based design process should be sized such that applying a DC current of magnitude I_L for a time equal to the inverter output waveform period produces no more than a 0.01% change in the nominal voltages across C_{DU} and C_{DL}.

The next step in determining suitable values for L_R and C_R is to repeatedly simulate the inverter for at least one output waveform period and adjust C_R and L_R to obtain satisfactory performance. However, the selected component values must result in viable inverter operation throughout the simulation interval. The critical requirement for operational viability in this phase of the design process is that the auxiliary link voltage must reach both power matrix rail potentials during each cycle.

The following iterative procedure is proposed for adjusting L_R and C_R. It assumes that the initial values of L_R, C_R, C_{DU}, and C_{DL} are computed as described above. Using the preceding definition of operational viability, repeatedly simulate the inverter and adjust $\frac{L_R}{C_R}$, while holding L_RC_R constant, until the inverter is operationally viable, but on the verge of being nonviable. Next, compute the required waveform quality metric(s), such as voltage or current THD, RMS voltage or current error, etc. If the resulting output waveform quality is too low, decrease L_RC_R while holding $\frac{L_R}{C_R}$ constant. If it is too high and there is a reason for reducing it, such as to use

less expensive switching devices with larger turn-off times, increase $L_R C_R$, again holding $\frac{L_R}{C_R}$ constant. Repeat these steps as appropriate until the quality metric(s) for the simulated output waveform are acceptable.

6.4.3 Voltage Divider Capacitance and Switching Device Turn-off Time Selection

The proposed procedure for finding suitable value for C_{DU} and C_{DL} is as follows. For notational simplicity, let both voltage divider capacitors have capacitance C_D. First, set C_D equal to the maximum value feasible for the given application. Next, run the simulation model. If the inverter is operationally nonviable, either C_D or $\frac{L_R}{C_R}$ must be increased until viability is restored. In either case, it may be necessary to make slight adjustments to both L_R and C_R in order to meet the required output waveform quality. If this is the case, follow the procedure outlined in the preceding subsection for adjusting L_R and C_R. However, in this case select a value of $\frac{L_R}{C_R}$ that is slightly larger than the minimum value for which the inverter is operationally viable. The appropriate safety margin is at the discretion of the designer and is application dependent. Repeat this procedure as appropriate, further reducing C_D until values for L_R, C_R, C_{DU}, and C_{DL} are found that are acceptable for the given application.

The problem of selecting the switching device turn-off time constitutes the third tier in the design approach. Normally, the preceding design oriented simulations will be conducted using the turn-off time of some preferred device(s). Typically, this will be the least expensive, and thus largest turn-off time, device available. If the estimated losses in the switching devices exceed the rated power dissipation limit, devices with a shorter turn-off time must be employed. Using the turn-off time of the new devices, run the simulation model and compare the losses to the new device's rated power dissipation limit. It may be necessary to increase $\frac{L_R}{C_R}$ slightly if excursions

in the voltage divider node potential cause the inverter to become operationally nonviable. This can result from shortening the duration of the device turn-off currents, which affect the ability of the PRAL circuit to regulate the voltage divider node potential. As in the previous tiers of this simulation based design process, this step is repeated as necessary until all of the achievable design goals are satisfied.

6.5 Load Back EMF Consideration in the Power Matrix State Selection Process

The simple bang-bang load current control strategy employed in the majority of PRDL inverters described in the literature does not include the effects of the load back EMF in the selection of power matrix states. The load current control technique described in this section for the PRAL inverter is an extension of a load back EMF aware control method proposed in [23] for a single-phase controlled rectifier. Like the single-phase case, it is assumed that real-time estimates of the load back EMF are available and that the load phase inductance is known. This is generally the case in machine drive applications where these quantities are typically needed to generate the load current reference values sent to the inverter.

The voltage applied across the load phase inductance effectively determines the change in the load current. For the Thevenin equivalent load model shown in Figure 51, the voltage applied to each phase inductance is a linear combination of the inverter output voltage, the load back EMF, and the voltage drop across the load phase resistances. Of these, the phase resistance voltage drops are comparatively inconsequential and can be ignored, as in [23].

Figure 61 shows a voltage space diagram depicting a typical load back EMF voltage along with the static voltages of a bridge-based inverter, such as the PRAL inverter. Most control strategies employed in the PRDL literature, such as the various bang-bang schemes, assume that the voltages available for presentation to the three-phase load inductance are symmetrical in voltage space, as shown in Figure 61. Although this assumption normally leads to stable control of the load current, it does not necessarily produce the best possible output waveform quality.

Figure 62 illustrates the effective static voltages that are actually available for presentation to the three-phase load inductance as a result of the load back EMF shown in Figure 61. The asymmetry in the effective static voltages is dramatic and suggests that substantial improvements in the inverter output waveform quality may be possible if the load back EMF is considered in the power matrix state selection process.

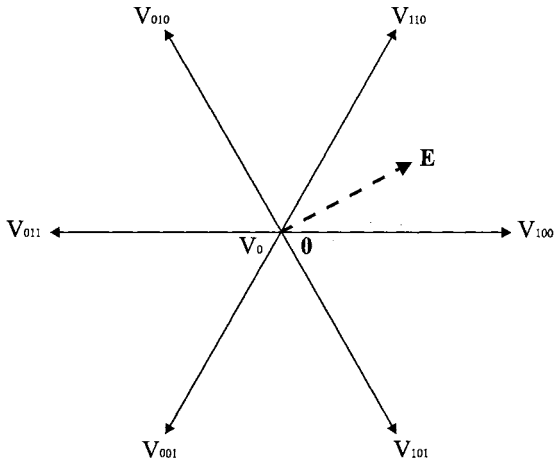


Figure 61. Voltage space diagram showing the PRAL inverter static voltages (solid) and a representative load back EMF voltage **E** (dashed)

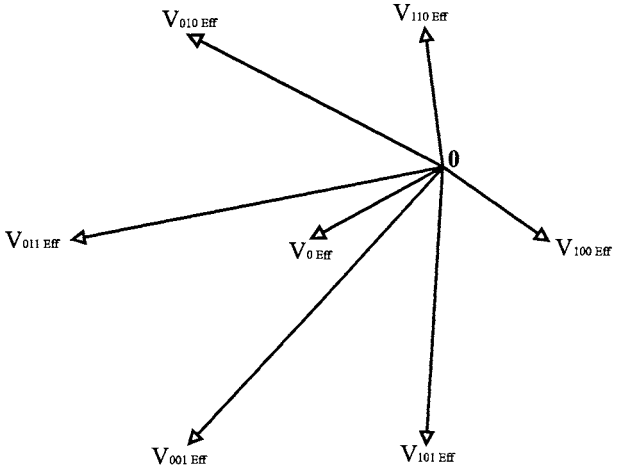


Figure 62. Voltage space diagram showing the effective inverter static voltages presented to the three-phase inductance for the example load back EMF shown in Figure 61

Like the state selection method proposed in [23], the approach adopted for the PRAL inverter employs a cost-function that penalizes candidate power matrix states according to the predicted current error existing at a specific time in the future. In the case of the three-phase PRAL inverter, the current error is a two-dimensional quantity instead of the simple scalar quantity discussed in [23]. Secondly, the candidate next states for the PRAL inverter are in many cases limited to only three of the seven non-degenerate states, a restriction not present in the conventional bridge rectifier considered in [23]. Finally, switching opportunities occur for the PRAL inverter on average every $\frac{T_{AL}}{2}$ seconds, where T_{AL} is the average auxiliary link period. Consequently, the cost-function is formulated to favor candidate next states that produce near zero load current error at a time $\frac{T_{AL}}{2}$ in the future.

The cost-function incorporates real-time estimates of the load back EMF **E**, the load current error $\mathbf{I_{Error}}$, and the integrated load current error $\mathbf{\Phi_{Error}}$, each given in **u-v** coordinates. The latter is included to reduce low frequency distortion. A penalty is assigned to each state the PRAL inverter could occupy at the conclusion of the next T mode. The penalty computation is conducted as follows. Suppose the inverter is in State $\mathbf{S}_k$ when the cost-function is evaluated and that State $\mathbf{S}_j$ is a candidate state that the inverter could occupy at the end of the upcoming T mode. First, the estimated change in the load current over the course of the next $\frac{T_{AL}}{2}$ time interval is computed. To a first approximation, the effective voltage applied to the load phase inductance is equal to the average of the voltages applied at either end of the time interval, specifically $\mathbf{V}_k$ and $\mathbf{V}_j$, respectively. This approximation yields an expression for the estimated change in the load current, $\Delta\mathbf{I}$, over the next one-half auxiliary link period.

$$\Delta\mathbf{I} = \left(\frac{\mathbf{V}_k + \mathbf{V}_j}{2} - \mathbf{E}\right)\frac{T_{AL}}{3L_s} \qquad 6.5.1$$

The next step is to compute the intermediate vector quantity $\Delta\mathbf{I}_{int}$ defined in 6.5.2.

$$\Delta\mathbf{I}_{int} = \mathbf{I}_{Error} + G_{\gamma}\Phi_{Error} - \Delta\mathbf{I} \qquad 6.5.2$$

Equation 6.5.2 combines the present current error with the expected change in the load current over the next $\frac{T_{AL}}{2}$ time interval. The inclusion of the integrated current error, Φ_{Error}, provides a mechanism for penalizing candidate states that perpetuate accumulation of DC bias in the error current. The weighting factor, G_{γ}, is normally taken to be quite small. A value of 0.05 proved adequate in preliminary simulation experiments. If G_{γ} is set to zero, 6.5.2 becomes zero whenever the predicted load current change would exactly cancel the existing current error at the end of the next T mode.

The final step in computing the penalty associated with a given candidate state is to construct a scalar function of $\Delta\mathbf{I}_{int}$ suitable for use as a cost-function. A natural candidate cost-function is $|\Delta\mathbf{I}_{int}|$. However, preliminary simulation results suggest that $|\Delta\mathbf{I}_{int}|^4$ produces superior performance results over $|\Delta\mathbf{I}_{int}|$, $|\Delta\mathbf{I}_{int}|^2$, and $|\Delta\mathbf{I}_{int}|^3$. Simply using the vector length leads to selection of states that concentrate the current error along one axis. Using the fourth power forces selection of states that more vigorously balance the error equally amongst the **u** and **v** axes, which tends to produce lower total load current distortion over the course of an entire output waveform period.

6.6 Summary

This chapter addressed four important design issues not covered in earlier chapters that are necessary for conducting the PRAL inverter modeling and simulation experiments presented in the next two chapters. Analytical expressions were developed for the boost current required to ensure inverter viability. The problem of regulating the voltage divider node potential was addressed and a "control based" solution proposed. Moreover, an outline was presented for

determining suitable values for the major PRAL inverter component parameters. Finally, a simple load current control method was outlined for selecting power matrix states based on knowledge of the load back EMF and the load phase inductance.

CHAPTER VII

DEMONSTRATION OF PRAL INVERTER ELECTRICAL VIABILITY AND DEVICE STRESS LEVELS THROUGH CIRCUIT SIMULATION

7.1 Introduction

SPICE is a widely used digital computer based circuit analysis tool. Several software packages based on SPICE are available from various manufactures and are typically supplied with models for a variety of electronic devices. The predefined component models turn a common personal computer into a virtual prototyping board into which a designer inserts components from device model libraries and connects them using virtual wires. All implementations of SPICE have built-in support for fundamental circuit elements such as independent sources, dependent sources, and passive elements like resistors, inductors, and capacitors. Convenient mechanisms exist for constructing custom device models using fundamental circuit elements. However, modeling complex devices, such as IGBTs, FETs, and SCRs, using vendor supplied device models lends credibility to simulation results by eliminating the possibility of an analysts biasing device models to perform in a desirable, but unrealistic, manner.

Unfortunately, the device models found in many component libraries do not accurately model one or more important device characteristics. It is not uncommon to find a transistor in a device library that will withstand millions of volts between its collector and emitter without breaking down or a diode with a zero reverse recovery time. To avoid serious discrepancies between

simulated results and physical prototype behavior, it is important to construct simple SPICE test beds to verify that key circuit component models perform realistically when subjected to conditions similar to those existing in the circuit under investigation. Although SPICE device models do not perfectly characterize real devices, SPICE simulation results are typically more accurate than alternative approaches, such as state variable methods.

This chapter employs SPICE to substantiate the electrical viability of the PRAL inverter and to support the device stress predictions stated in previous chapters. The chapter begins with a discussion of the applicability of SPICE to power electronic circuits. Next, an approach for modeling the PRAL inverter within the limitations of SPICE is presented. Simulated internal and output waveforms are then generated to illustrate the electrical characteristics of the PRAL inverter and to support device stress predictions.

7.2 PRAL Inverter Modeling and Simulation with SPICE

7.2.1 Applicability of SPICE to Power Electronics Circuit Simulation

SPICE based digital computer simulation packages provide a valuable tool for assessing the performance of power electronic circuitry early in the development cycle. A SPICE circuit model is easily altered to correct design flaws or to investigate alternative configurations. This allows designers to identify fundamental design errors and identify weaknesses prior to committing resources to fabricating and testing physical prototypes. SPICE has the added advantage of allowing unrestricted access to all node voltages and branch currents without perturbing the circuit behavior.

Despite the attractive features of SPICE, available implementations are oriented toward signal electronics applications and have severe shortcomings when applied to modern power electronics based energy conversion systems. The predominant obstacle to analyzing electronic power converters with SPICE is the inability to model algorithmic control mechanisms. Modern

electronic power converters rely heavily on control algorithms executing on microprocessors to instigate power matrix state changes. Complex algorithms that estimate present and near-term load characteristics offer substantial performance improvements over the simple "bang-bang" type analog controllers found in older converter designs. Since SPICE is fully capable of modeling logic gates and any algorithm can theoretically be implemented using logic gates, a potential solution is to synthesize control algorithms using logic gates and then implement a SPICE model of the resulting logic circuitry. Unfortunately, such an approach is tedious to implement and computational limitations in SPICE restrict the complexity of circuits that can be simulated using this technique. The computational limitations are due primarily to the floating point word size available on most computing platforms.

The SPICE implementation used in this work, "PSPICE 6.1" by MICROSIM, is limited to a minimum integration time step size of approximately $3e^{-18}$ seconds for a 4 ms simulation window. The minimum integration time step size increases proportionally with the simulation window size. Simulation of complex circuit models, particularly those with strong nonlinear behavior, typically require small integration time steps in order to obtain convergent numerical solutions. Thus, the maximum simulation time interval achievable with PSPICE can be seriously limited for complex circuit models. Bang-bang controllers using feedback through a modest logic network can easily require integration time steps smaller than $3e^{-18}$ in order to obtain a convergent numerical solution. Consequently, this eliminates SPICE as a single source simulation tool for investigating new complex power conversion techniques.

Despite the inability of SPICE to simulate algorithmic control signals in advanced power conversion systems, it remains a useful tool for validating expected power matrix behavior. Analyzing a new power matrix configuration using a simplified control algorithm that fits within the confines of SPICE's limitations can provide important information about new candidate topologies. The voltages and currents existing in the power matrix during each mode, and

particularly during mode transitions, expose the topological merits or drawbacks of a given design in terms of power matrix operation and device stress. Advanced control algorithms typically merely enhance performance through optimal sequencing of power matrix modes. A simple bang-bang controller will typically excite the general circuit behavior as an advanced control algorithm, only in a sub-optimal manner.

7.2.2 SPICE Modeling Approach and Convergence Issues for the PRAL Inverter

The PRAL inverter requires significant algorithmic control mechanisms to operate in the soft-switched mode. This is due to the stringent restrictions placed on power matrix state transitions and the need to delay state transitions until the resonant circuit inductor current is properly initialized. Additionally, the initialization current for the resonant circuit inductor must be computed in real-time prior to each state transition. Simulating the logic circuitry that implements these basic PRAL inverter control functions heavily stresses the numerical convergence limitations of the SPICE implementation used in this work. Consequently, the inclusion of logic circuitry to regulate the voltage divider node potential and optimize the boost current level is omitted. Instead, the model contains balanced ideal voltage sources to represent the voltage divider capacitors and employs a fixed boost current with sufficient magnitude to ensure inverter operability.

The PRAL inverter model shown in Figure 63 is composed of the PRAL inverter circuit described in preceding chapters, ancillary sub-circuits to drive the switching device gates and measure key state variables, control logic circuitry, and a simple inductive load model, complete with back EMF. Expanded views of Figure 63 are provided in Appendix A. With the exception of the control logic circuitry, all of these sub-circuits are self-explanatory, based on discussions presented in earlier chapters.

The control logic circuitry is broken into four functional groups: Event Generation, Phase Leg Control, State Transition Control, and Initialization Current Generation. Event Generation blocks detect the occurrence of critical events, such as the resonant circuit inductor current reaching the value needed to begin an L to T mode transition, and notify other control block(s) that a particular event has occurred. Phase Leg Control blocks control the three switching devices contained in each phase leg. These blocks accept "Transition" commands from the State Transition Control block and turn the respective phase leg switches on or off in a manner consistent with Figure 40 of Chapter V. The State Transition Control block determines the appropriate voltage level (phase leg state) for each phase leg based on a simple bang-bang current control scheme, implemented in the right-hand side of Figure 63, and signals each Phase Leg Control block when a voltage level transition is required.

The control logic circuitry used in the PRAL inverter model is composed of simple logic gates, such as "AND," "NAND," "OR," and "NOR" gates. The models for these devices are specified in terms of intrinsic SPICE circuit elements, namely resistors, capacitors, dependent sources, etc. More complex logic devices, such as "Flip-Flops" and "One-Shots," are constructed from these simple logic gate building blocks using the graphical sub-circuit editing tool provided with the SPICE implementation used in this work. The four control logic blocks described earlier were also constructed using the SPICE graphical sub-circuit editor. With the exception of voltage sources replacing the voltage divider capacitors and the use of a constant boost current, the control mechanisms for the PRAL inverter SPICE model are as described in Chapter V. SPICE source code or sub-circuit schematic diagrams are provided in Appendix A for all relevant control logic circuitry along with a complete SPICE generated circuit model listing for the entire PRAL inverter model.

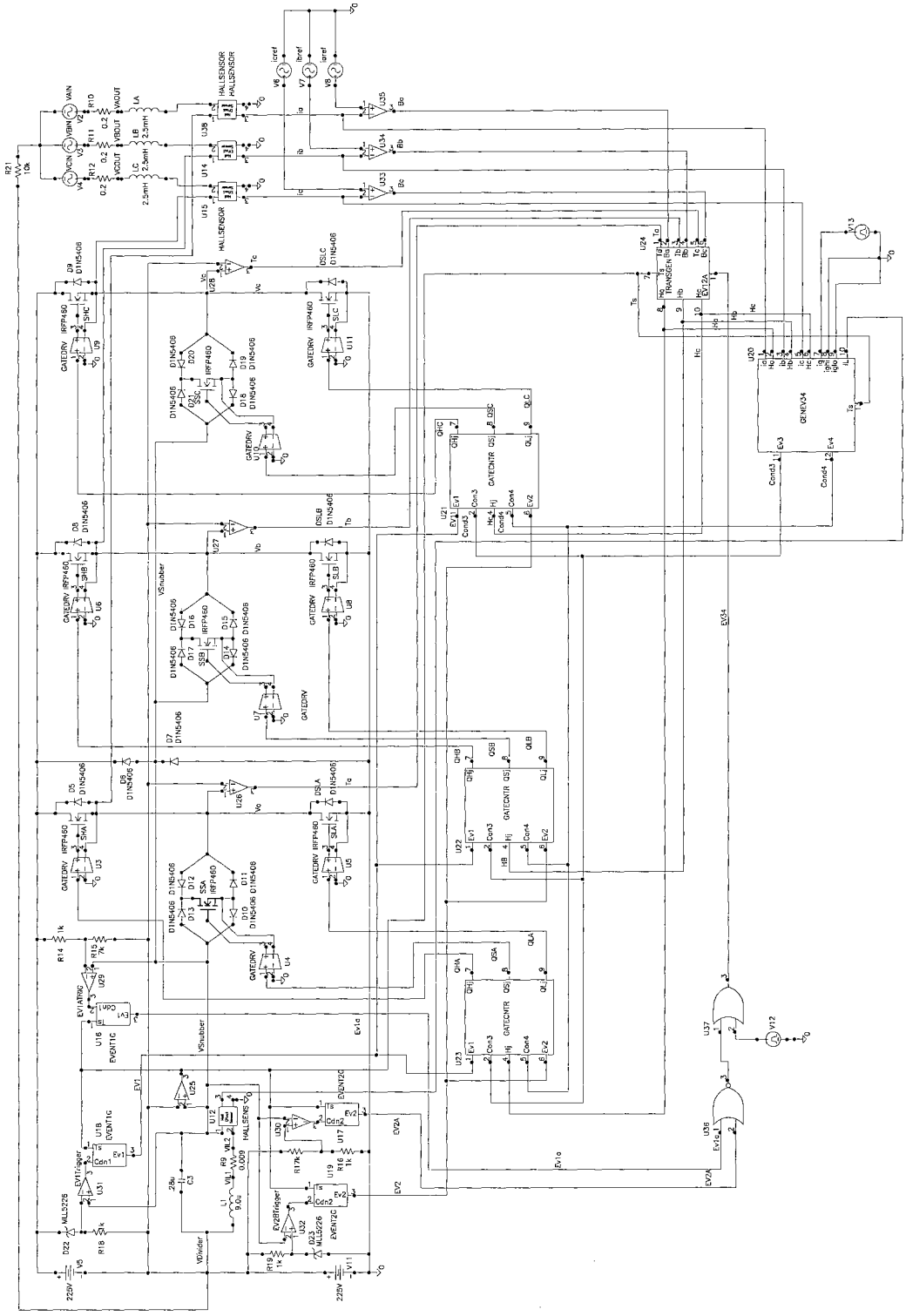


Figure 63. Top level SPICE model circuit diagram of a PRAL inverter feeding an inductive load with back EMF

Examination of Figure 63 and expanded views of its constituent sub-circuits, located in Appendix A, reveals a number of transient voltage sources, logic gates, small capacitors, and large resistors that are extraneous to the PRAL inverter model. These circuit elements were inserted to force the SPICE bias point and transient analysis algorithms to converge. All active sources are turned off within a few microseconds of simulation initiation and the effects of the added resistors and capacitors are negligible in terms of the inverter state variables of interest. Additionally, the convenient analytical tools that accompany SPICE, such as Fourier Analysis, could not be enabled without causing the SPICE transient analysis algorithm to diverge. Several control logic circuit implementations were constructed in an attempt to alleviate this problem. However, all attempts failed, suggesting that the problem stems from the number of nodes and feedback loops existing in the PRAL inverter model rather than the model implementation. Finally, convergence in both the bias point and transient algorithms was attainable using FET device models but not with available IGBT device models. This is believed to be due to the presence of more pronounced non-linearities in the behavior of IGBTs than in FET devices.

7.3 Simulation Model Parameters, Simulation Results, and Conclusions

7.3.1 Model Parameters

The component parameters used in the SPICE simulation model of the PRAL inverter were selected using the "first-cut" component selection guidelines described in Chapter VI. Normally, the design process would involve iterative refinement of the component parameters to improve selected performance aspects of interest. However, optimization efforts have questionable value in the present case since the voltage divider voltages and the boost current are constant. Additionally, the results obtained prior to any parameter refinements have the advantage of demonstrating the merits of the "first-cut" component selection guidelines. Consequently, design refinements were omitted in this exercise.

The requirements selected for the PRAL inverter example presented in this chapter are that it have a volt-ampere rating of 5.9kVA, a line voltage ratting of $240V_{RMS}$, and a DC input voltage of 450V. The $240V_{RMS}$ voltage was selected due to its widespread commercial use. The 5.9kVA rating is based on the voltage and current ratings of the switching devices selected for the SPICE simulation experiments. Normally, some form of output waveform quality metric would be included in the inverter requirements. Unfortunately, computational limitations in the available SPICE implementation for this effort precluded the generation of data over a sufficient time interval to compute meaningful output waveform quality metrics, such as load current Total Harmonic Distortion (THD). Consequently, a free-running auxiliary link frequency of 100kHz was selected in lieu of a waveform quality metric.

The component values, principal operating parameters, and other parameters of interest for the PRAL inverter model are given in Table V. The switching device selection is based on available FET data sheets. A quality factor of 100 was assumed for the resonant circuit inductor. Diode selection was based on devices available in the SPICE model library that demonstrated transient characteristics similar to those of a desired device that was not present in the libraries. The resonant circuit component selection is based on the "first-cut" design rules given in Chapter VI. The specified volt-ampere and voltage ratings translate to a peak load current of approximately 20A.

TABLE V

PRAL INVERTER SPICE MODEL COMPONENT PARAMETERS AND OPERATING VALUES

PARAMETER/DEVICE	VALUE/PART NUMBER
L_R	9.0μH
R_R	0.009Ω (@ 100 kHz)
C_R	0.28μF
L_S	2.5mH
R_S	0.20Ω
$\lvert \mathbf{E}_{Phase} \rvert$	85V (RMS)
I_{Ref}	20A
f_{Load}	60Hz
FET Part Number	IRFP460
FET Forward Current (Continuous)	20A
FET Forward Current (Surge)	80A
FET Power Dissipation (Max)	280W
Diode Part Number	D1N5406

7.3.2 Simulation Results: Electrical Viability of the PRAL Inverter

The SPICE simulation was conducted for a 500 μs interval. The resulting auxiliary link voltage and the resonant circuit inductor current waveforms are shown in Figure 64. To enhance clarity, Figure 65 shows a 50 μs interval of the same waveforms. The L modes are easily discernable from the auxiliary link voltage waveforms in each figure. The T modes begin and end where the slope of the auxiliary link voltage waveform abruptly changes near 0V and 450V. The modulation in the resonant circuit inductor current is due to changes in the auxiliary link current

resulting from different load phases being connected to the auxiliary link. The same form of modulation is seen throughout the PRDL literature.

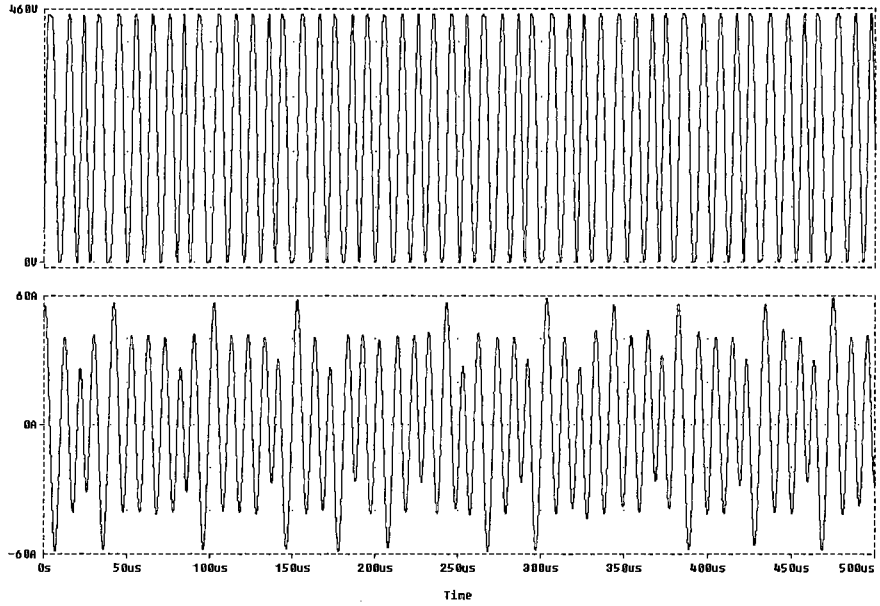


Figure 64. Simulated auxiliary link voltage waveform $v_R(t)$ (upper) and resonant circuit inductor current waveform $i_R(t)$ (lower)

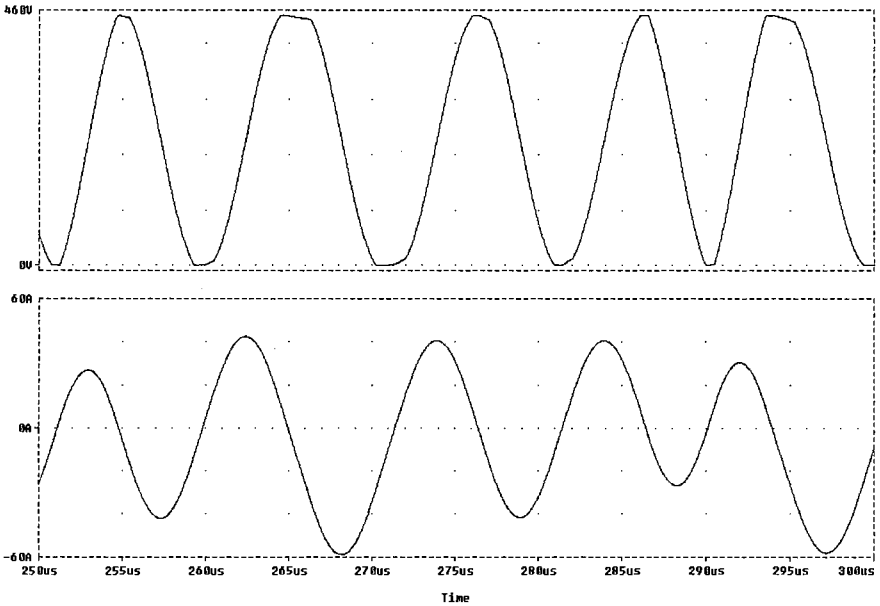


Figure 65. Expanded view of the simulated auxiliary link voltage waveform $v_R(t)$ (upper) and resonant circuit inductor current waveform $i_R(t)$ (lower)

Figure 66 shows the auxiliary link voltage along with the phase leg voltages, all referenced to the lower power matrix rail. Figure 67 provides a 50 μs expanded view of the same waveforms shown in Figure 66. Figure 68 shows the line-to-line voltages presented to the load.

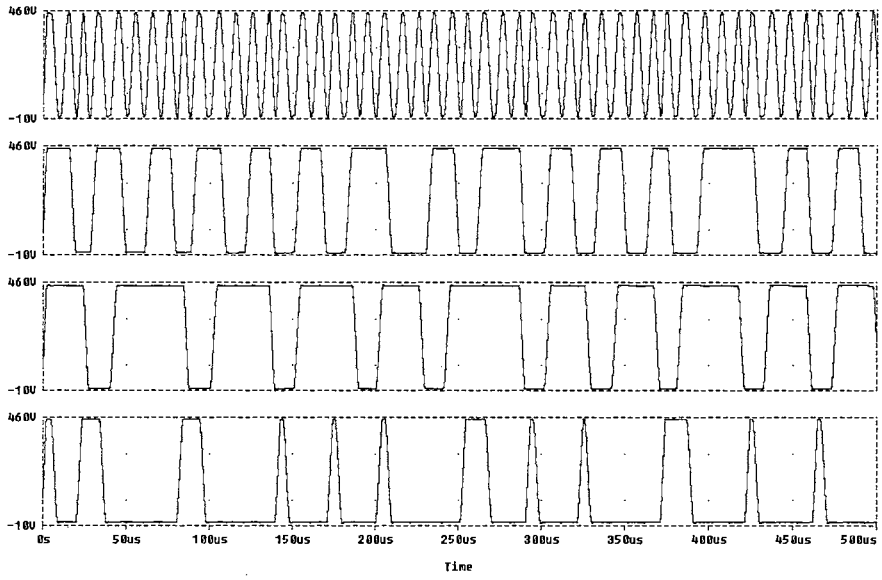


Figure 66. SPICE generated auxiliary link voltage $v_R(t)$ (upper), Phase Leg A voltage (second from top), Phase Leg B voltage (second from bottom), and Phase Leg C voltage (bottom) waveforms

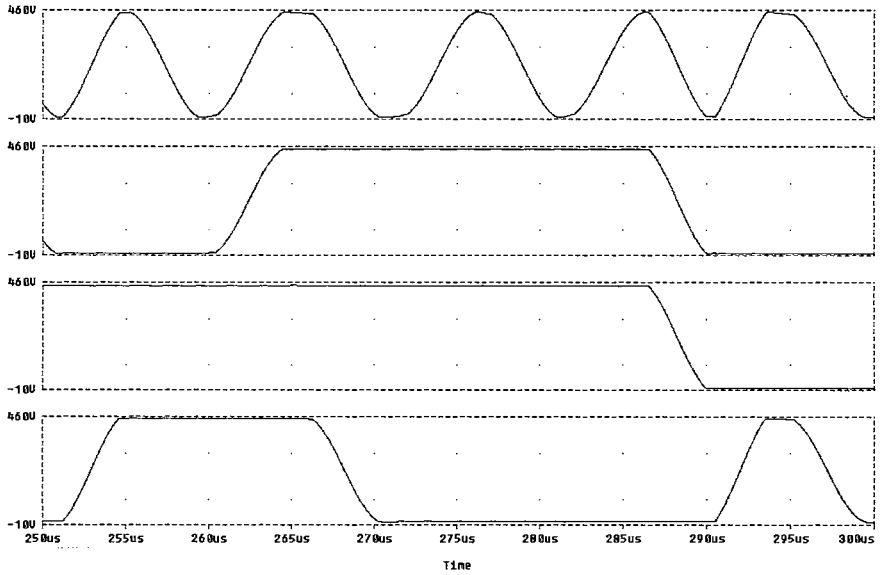


Figure 67. Expanded view of SPICE generated auxiliary link voltage $v_R(t)$ (upper), Phase Leg A voltage (second from top), Phase Leg B voltage (second from bottom), and Phase Leg C voltage (bottom) waveforms

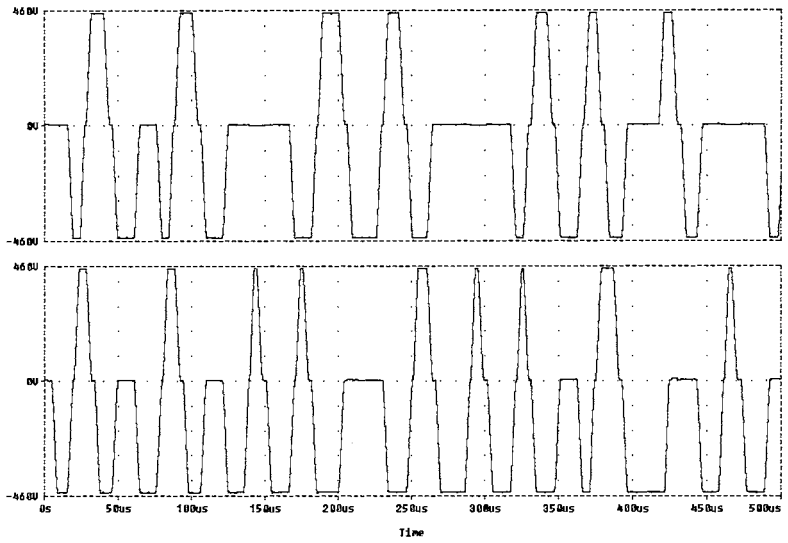


Figure 68. Plot showing a 500μs interval of the SPICE generated PRAL inverter output line-to-line voltages, $v_{ab}(t)$ (upper) and $v_{ca}(t)$ (lower), presented to the load during synthesis of a 60Hz (16.67ms period) sinusoidal three-phase voltage waveform

Figure 69 shows approximately 3% of a complete period of the 60Hz load current waveforms. The simple bang-bang current control scheme employed in this exercise does not contain a mechanism for mitigating DC bias in the load error current. This is evident from the load phase currents shown in the figure "riding" toward one side of their respective reference current waveforms. Despite this shortcoming, the RMS load error current in all three phases do not exceed 3.5% of the rated RMS load current, as can be seen in Table VI.

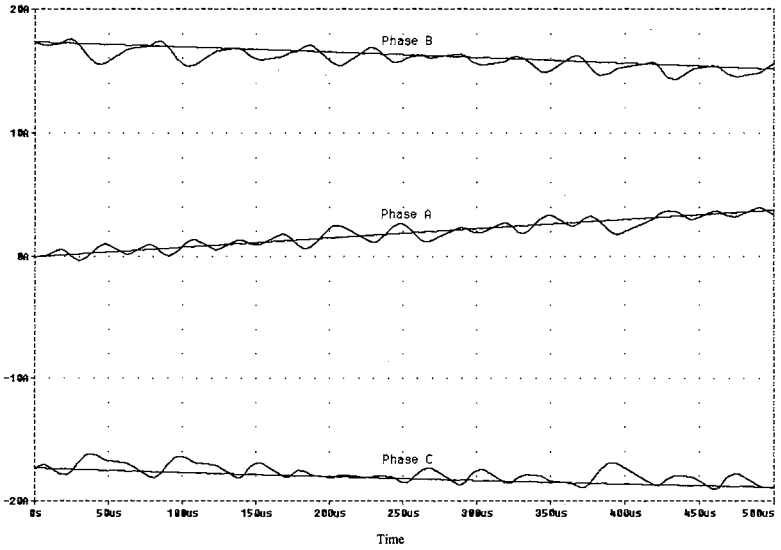


Figure 69. SPICE generated load phase current and associated reference current waveforms

TABLE VI

LOAD RMS ERROR CURRENTS FOR THE PRAL INVERTER

Load Phase	RMS Error Current	Percent of Rated Current
A	0.48A	3.4%
B	0.43A	3.0%
C	0.49A	3.5%

The waveforms shown to this point support the claim that the PRAL inverter topology is electrically viable. The auxiliary link voltage smoothly transitions between the upper and lower power matrix rails in a manner consistent with the PRAL inverter concept. Moreover, the "first-cut" resonant circuit component values resulted in an operable design with reasonably low auxiliary link voltage slew rates during the initial phase of each T mode, a necessity for soft-switched operation.

7.3.3 Device Stress Levels

7.3.3.1 Inferring Device Stress Levels from the SPICE Simulation Results Aside from demonstrating the electrical viability of the PRAL inverter topology, the SPICE simulation exercise provides a means of assessing the voltage, current, and thermal stresses placed on the switching devices. The voltage and current stresses are directly discernable from the node voltages and branch currents generated using the SPICE circuit model. The thermal stresses are somewhat elusive in that the heat sink used in a given physical implementation significantly affects the device temperature, and thus the ability of a device to function without damage. To generalize the thermal stress assessment, only the average thermal power generated within the switching devices is considered in the following discussions.

Although the PRAL inverter switches contain at least one diode, it is the controllable devices that are of interest when considering thermal stress levels. This is because the turn-off time for controllable devices, such as the FETs used in this exercise, are roughly one order of magnitude larger than those for available diodes with similar voltage and current ratings. Secondly, unlike diodes, controllable devices can be turned on under non-zero voltage conditions, exposing them to a switching loss regime that does not exist for diodes. Moreover, diodes are typically far more robust in terms of the surge current that they can endure without damage. For these reasons, only the voltage stress placed on the diodes contained in the PRAL inverter switches is examined in the following device stress assessment. A similar omission of diode stress considerations exists in the PRDL literature.

The FET terminal voltage, current, and internal power are all associated with the FET drain and source terminals. The FET gate current is, by nature of the device, insignificant compared to the drain and source terminal currents. Additionally, the FET gate terminal voltage is always maintained to within approximately 10V of the FET source terminal voltage in the circuit configuration used in this exercise. Consequently, undue voltage stress involving the FET gate terminal is not present, by design.

For convenience in the following discussions of the SPICE simulation results, the following terms are adopted. Define the FET terminal voltage to be that of the drain terminal referenced to the source terminal. Similarly, define the FET terminal current as the net current flowing through the device from the drain terminal to the source terminal. Let the FET terminal power be defined to be the product of the FET terminal voltage and current. Finally, let the FET cumulative terminal energy at time t be defined as the time integral of the FET terminal power computed over the interval $(-\infty, t)$.

The interpretive method employed in the following subsections to ascertain the FET thermal stress exposure is based on plots of the terminal power and cumulative terminal energy. This

method is complicated by the fact that FETs, like other controllable switching devices, contain a significant internal capacitance between the drain and source terminals. Plots of the FET terminal power capture both the thermal power generated within the device and the reactive power associated with the terminal capacitance. Similarly, plots of the FET cumulative terminal energy show both positive and negative fluctuations due to the presence of the terminal capacitance. This results in the FET appearing to produce a small amount of power when the auxiliary link drives its terminal voltage toward zero. On average, however, switching devices are always electrical power sinks rather than electrical power sources. The effects of the internal terminal capacitance is most pronounced in the plots for the Phase A FETs where the conduction current associated with the load is nearly zero for the simulation window shown.

Stress level plots for each FET in the PRAL inverter are shown in the following subsections in nine separate plots, one plot for each device. The FET terminal voltage and current are shown as the upper and second most upper plot in each figure, respectively. The third plot from the top of each figure represents the instantaneous FET terminal power appearing across the drain and source terminals while the lower most plot represents the instantaneous FET cumulative terminal energy. The nine FET stress plots are presented and discussed on a per phase basis in the following subsections.

7.3.3.2 Device Stresses in Phase Leg A Figures 70, 71, and 72 show switching device stress plots for the FETs in Switches SHA, SLA, and SSA, respectively. Examination of all three figures reveals that the maximum FET terminal voltage is below 460V, less than 10V above the 450V DC inverter input voltage. Additionally, the diode configuration in each of the three phase leg switches is such that the applied reverse voltage across any given diode is never greater than the forward voltage applied to the FET in the same switch. Consequently, the voltage stress placed on any given component in any of the switches in Phase Leg A is effectively limited to the inverter DC input voltage, as expected.

The FET terminal currents are all below the inverter rated peak load current of 20A. The spikes seen in the FET terminal current and terminal power plots of each figure are a consequence of the respective switches participating in the initialization of the resonant circuit inductor current. The low average terminal currents seen for all three FETs are due to the low reference current for Phase A in the simulation time interval, as previously shown in Figure 69.

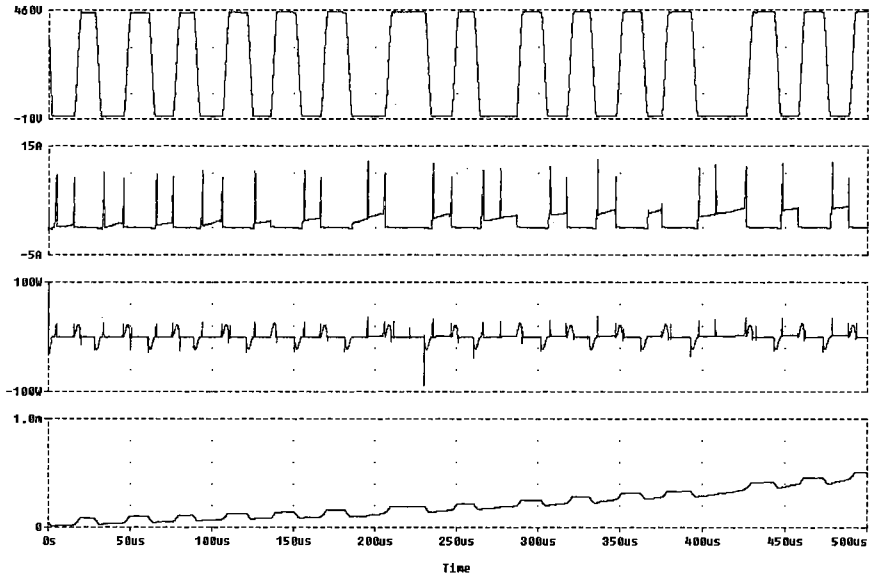


Figure 70. Stress waveforms for the FET in Switch SHA: (Top) FET terminal (drain to source) voltage (Volts), (Second from top) FET terminal current (Amps), (Second from bottom) FET terminal power (Watts), (Bottom) cumulative FET terminal energy (milli-Joules)

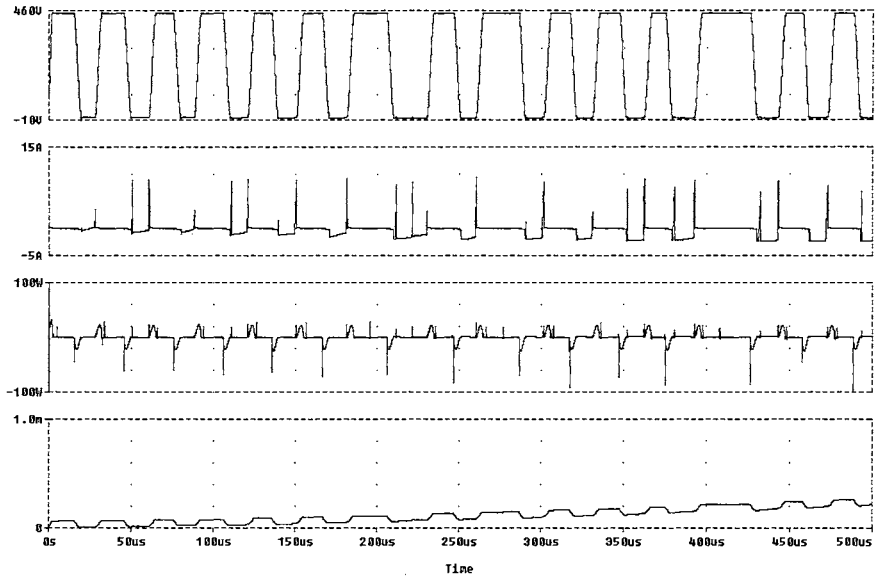


Figure 71. Stress waveforms for the FET in Switch SLA: (Top) FET terminal (drain to source) voltage (Volts), (Second from top) FET terminal current (Amps), (Second from bottom) FET terminal power (Watts), (Bottom) cumulative FET terminal energy (milli-Joules)

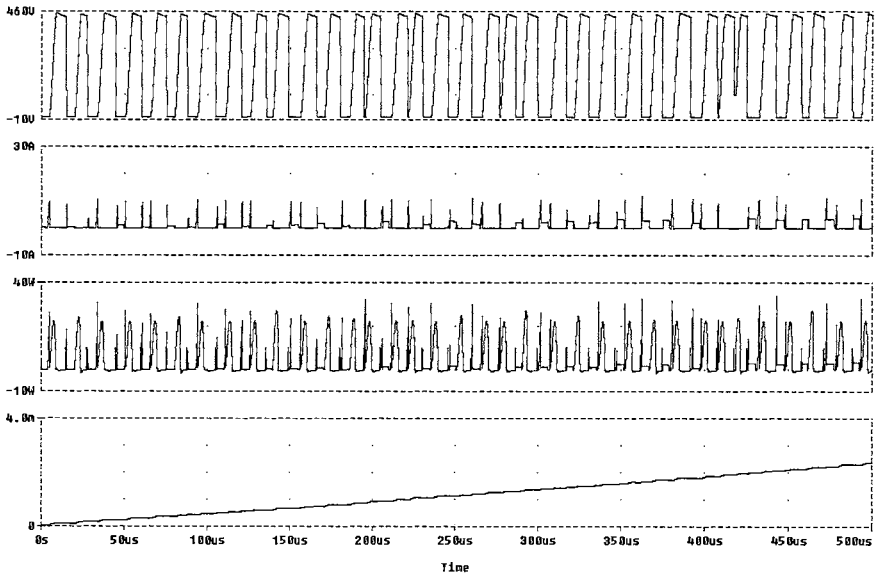


Figure 72. Stress waveforms for the FET in Switch SSA: (Top) FET terminal (drain to source) voltage (Volts), (Second from top) FET terminal current (Amps), (Second from bottom) FET terminal power (Watts), (Bottom) cumulative FET terminal energy (milli-Joules)

The presence of the FET terminal capacitance is clearly manifested in the piecewise sinusoidal ripple seen in the terminal power plots in all three figures. For the FETs in Switches SHA and SLA, the sign of the terminal power ripple is positive for increasing terminal voltage and negative for decreasing terminal voltage. This is as expected since the FET terminals are directly connected between the phase leg and one of the power matrix rails. In contrast, the ripple seen in the terminal power for the FET in Switch SSA is always positive and occurs only when the terminal voltage is rising. This behavior is a result of the bridge rectifier used to implement the bilateral switch. When the voltage across the bilateral switch terminals diverges from zero, becoming either more negative or more positive, the FET terminal voltage becomes more positive, due to the rectifying action of the bridge diodes. When the auxiliary link resonant circuit drives the voltage across the bilateral switch terminals toward zero, the FET terminal capacitance acts as a voltage source, reverse biasing the bridge diodes and preventing discharge of the FET terminal capacitance through the bilateral switch terminals. When the bilateral switch FET is turned on, the energy stored in the FET terminal capacitance is converted to heat energy. Since the capacitance is internal to the FET, there is no observable effect on the FET's terminal current, and thus no evidence in the terminal power plot that the stored energy in the terminal capacitance is being converted to heat energy. Consequently, terminal power ripple resulting from the FET's terminal capacitance is only observed when the auxiliary link is driving the bilateral switch terminal voltage away from zero.

The FET terminal capacitance produces a second interesting effect in the bilateral switch implementation employed in this exercise. The terminal voltage plot for Switch SSA seen in Figure 72 reveals that the FET terminal voltage decreases to approximately 100V near 420μs and then returns to the upper rail potential. Inspection of Figure 66 shows that Phase Leg A is held at the upper rail potential during the corresponding inverter T_L mode. Consequently, no load current flows in Switch SSA during the T_L mode. The underlying condition enabling this seemingly

erroneous behavior is that the resonant circuit inductor current is adequate upon the inverter entering the L_U mode for the T_L mode to begin immediately.

The peculiar terminal voltage behavior seen for the SSA FET results from the following sequence of events. The control logic turns the FET on when the auxiliary link potential nears that of the upper rail and turns it off a few hundred nanoseconds later when the inverter enters the T_L mode. The resulting commanded "on time" for the FET, resulting from the infinitesimal L_U mode duration, is insufficient to fully discharge the terminal capacitance. During the T_L mode, the voltage across the bilateral switch terminals eventually exceeded that of the residual FET terminal voltage. When this occurs, the diodes in the bilateral switch bridge become forward biased, forcing the FET terminal voltage to increase along with the voltage across the bilateral switch terminals. Since the bilateral switch does not conduct load current when this scenario occurs, there are no operationally detrimental consequences.

7.3.3.3 Device Stresses in Phase Leg B Figures 73, 74, and 75 show stress plots for the FETs contained in Switches SHB, SLB, and SSB, respectively. As with the FETS in the Phase Leg A switches, the peak terminal voltages for all three FETs are within less than 10V of the 450V DC inverter input voltage. The peak FET terminal current in all three FETs is below the 20A rated load current with the exception of a few current spikes resulting from initialization of the resonant circuit inductor current. The amplitudes of these spikes, the largest reaching approximately 27A, are consistent with the 5A fixed boost current and the control logic circuitry delays present in the SPICE PRAL inverter circuit model. Recall that a fixed boost current was used in lieu of a value tailored to each L-T mode transition in order to alleviate numerical convergence difficulties arising from excessive circuit model complexity. The actual required boost current was less than 2A for most L-T mode transitions. Secondly, the propagation delays associated with the control logic circuitry in the SPICE model were made significantly larger than would normally be seen in practice in order to overcome numerical convergence problems during

the first few nano-seconds of the simulation. This resulted in turn-off being initiated in the power matrix switches approximately 400ns after the boost current reached the 5A threshold, artificially raising the peak switch current. These two factors stem from limitations in SPICE rather than the PRAL topology, suggesting that the magnitudes of the current spikes in the SPICE simulation are likely larger than would be seen in a physical prototype of the PRAL inverter.

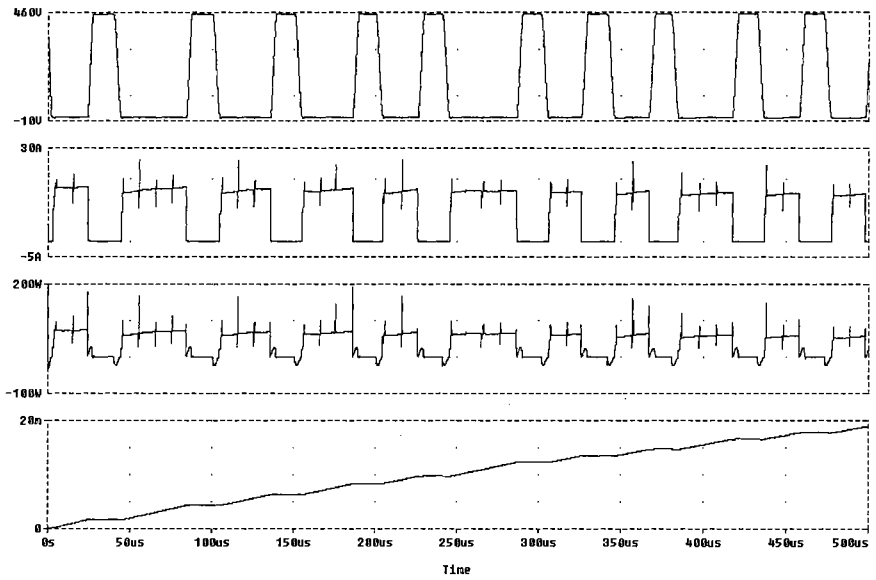


Figure 73. Stress waveforms for the FET in Switch SHB: (Top) FET terminal (drain to source) voltage (Volts), (Second from top) FET terminal current (Amps), (Second from bottom) FET terminal power (Watts), (Bottom) cumulative FET terminal energy (milli-Joules)

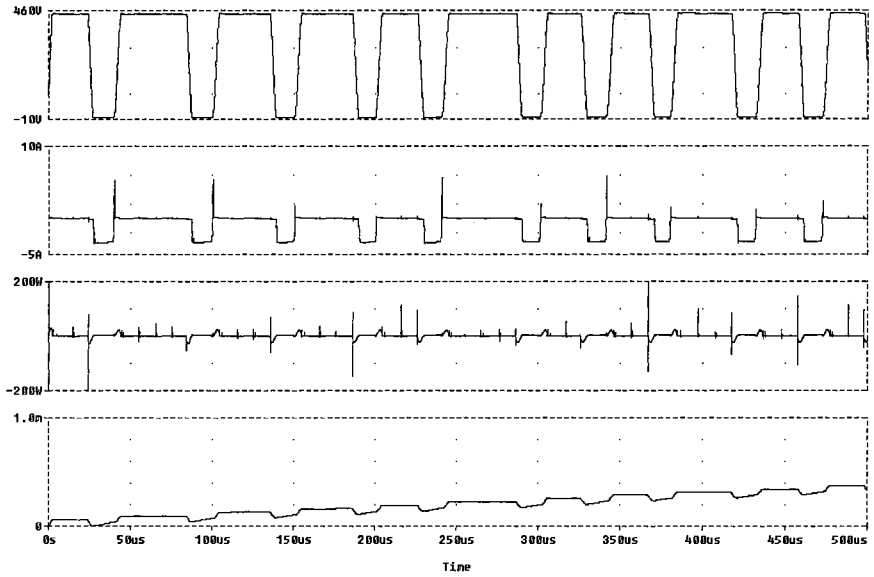


Figure 74. Stress waveforms for the FET in Switch SLB: (Top) FET terminal (drain to source) voltage (Volts), (Second from top) FET terminal current (Amps), (Second from bottom) FET terminal power (Watts), (Bottom) cumulative FET terminal energy (milli-Joules)

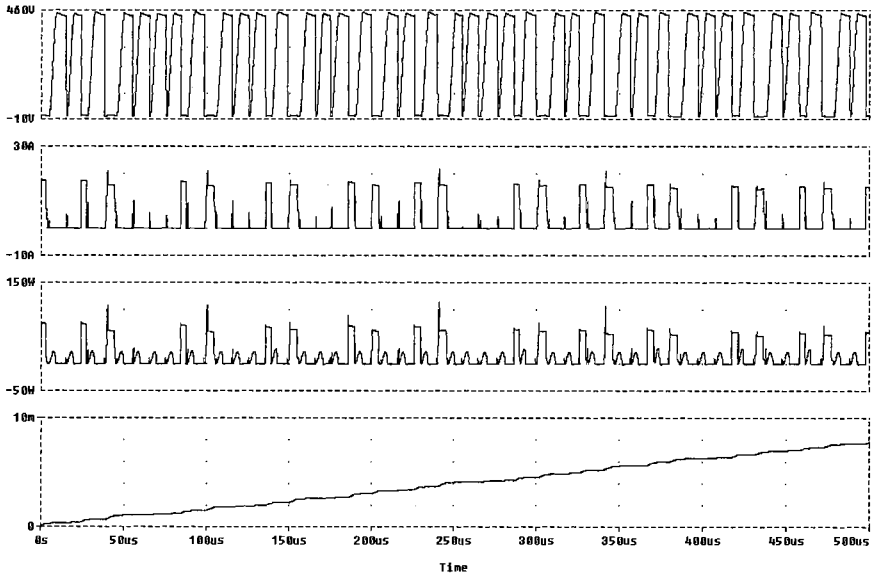


Figure 75. Stress waveforms for the FET in Switch SSB: (Top) FET terminal (drain to source) voltage (Volts), (Second from top) FET terminal current (Amps), (Second from bottom) FET terminal power (Watts), (Bottom) cumulative FET terminal energy (milli-Joules)

Unlike the Phase A load current, which has a near zero reference load current in the simulation time interval, the Phase B load reference current is approximately 17A, directed toward the load. Consequently, significant load current conduction losses are seen in some of the figures. Figure 74 shows the FET in SLB occasionally conducting a negative current. Although most of the conduction current in SLB flows through the inverse-parallel diode, approximately 3A flows through the reverse biased FET. This produces a small conduction loss in the SLB FET, as can be seen from the terminal power and integrated terminal power plots in Figure 73.

Examination of the terminal power and integrated terminal power plots for the FETs in all three figures shows that the thermal energy generated from load current conduction far exceeds that resulting from switching and initialization of the resonant circuit inductor current. Moreover, the load current conduction loss in the SSB FET over a given auxiliary link half-cycle exceeds the loss resulting from converting the FET terminal capacitance energy to heat energy each time SSB is turned on. This energy is stored in the FET terminal capacitance during an auxiliary link half-cycle in which SSB is not conducting any load current. It follows that the "worst case" thermal stress condition for the bilateral switch FET occurs when the bilateral switch conducts continuously over a long series of resonant circuit half-cycles.

7.3.3.4 Device Stresses in Phase Leg C The device stress plots shown in Figures 76 through 78 for the Phase Leg C FETs are similar to those shown for the Phase Leg B FETs. The voltage stress on all of the Phase Leg C FETs is within a few volts of the inverter input DC voltage. Current spikes resulting from initialization of the resonant circuit inductor current are present in all three figures. The FETS in Switches SLC and SSC experience current spikes of up to 29A while the spikes seen for the FET contained in the SHC FET are below 10A. The largest of these current spikes, 29A, are well below the surge current rating of 80A allowed for the RFP460 FETs used in the SPICE circuit model.

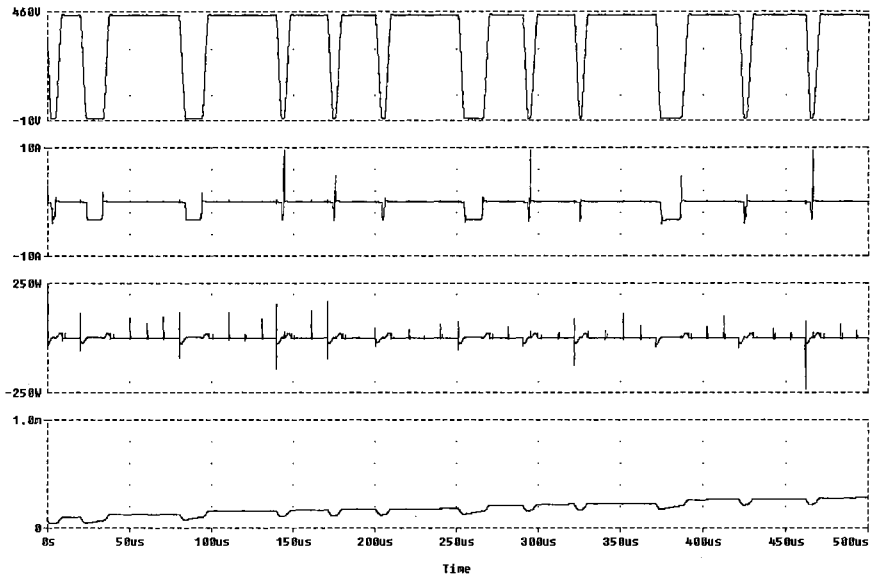


Figure 76. Stress waveforms for the FET in Switch SHC: (Top) FET terminal (drain to source) voltage (Volts), (Second from top) FET terminal current (Amps), (Second from bottom) FET terminal power (Watts), (Bottom) cumulative FET terminal energy (milli-Joules)

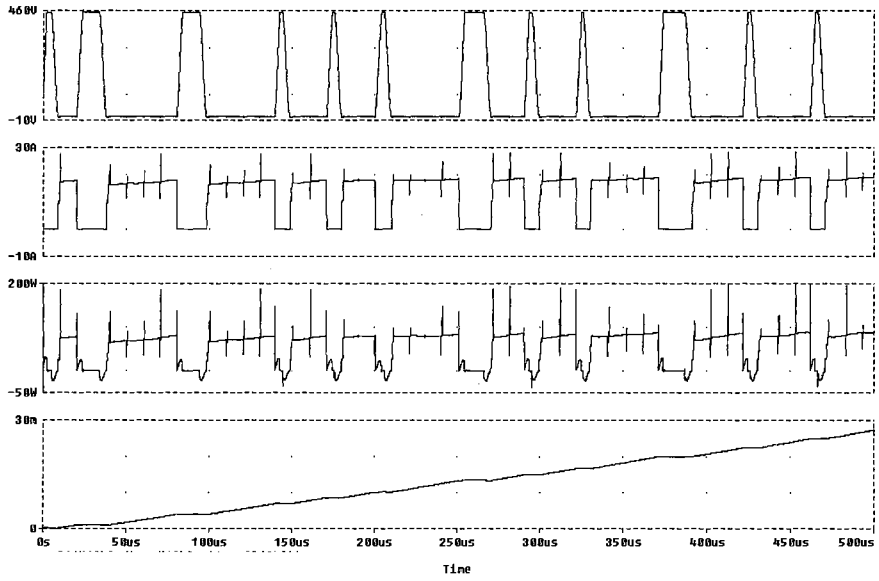


Figure 77. Stress waveforms for the FET in Switch SLC: (Top) FET terminal (drain to source) voltage (Volts), (Second from top) FET terminal current (Amps), (Second from bottom) FET terminal power (Watts), (Bottom) cumulative FET terminal energy (milli-Joules)

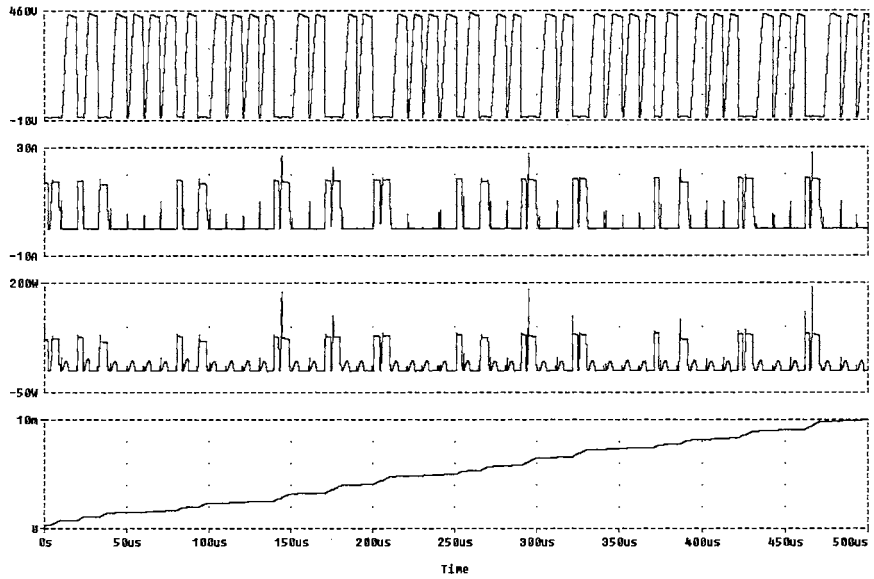


Figure 78. Stress waveforms for the FET in Switch SSC: (Top) FET terminal (drain to source) voltage (Volts), (Second from top) FET terminal current (Amps), (Second from bottom) FET terminal power (Watts), (Bottom) cumulative FET terminal energy (milli-Joules)

The Phase C load current flows toward the inverter for the simulation time interval shown in the figures. Consequently, the load current is not manifested as forward conduction current in the SHC FET. As with Switch SLB in Phase Leg B, when Switch SHC is conducting load current, the FET is reversed biased and shares a few Amperes of the total conduction current with the inverse-parallel diode. This is the dominant contributor to thermal energy generation in SHC.

7.3.4. Conclusions Regarding Switching Device Stresses

The preceding voltage and current stress plots for the FETs contained in the PRAL switches were fully consistent with predictions made in Chapter V. The voltage stress placed on each of the FETs and diodes forming the PRAL switches was demonstrated to be limited to within 10V of the inverter DC input voltage. The FET terminal currents did not exceed the load current in the respective phase leg except for a few sub-microsecond current spikes that resulted from initialization of the resonant circuit inductor current. In all cases, the magnitudes of the current spikes were well below the 80A limit for the IRP460 FET used in the SPICE simulation model.

The thermal energy generation characteristics were fully consistent with the soft switching paradigm. All nine switches in the PRAL inverter demonstrated substantially lower internal thermal energy generation from switching related losses than from load current conduction losses. The average thermal power generated in each FET in the PRAL inverter computed over the simulation time interval is shown in Table VII below. The table entries are all well below the 280 rated thermal power of the IRP460 FET. The largest generated thermal power entry in Table VII is only 19.7% of the rated thermal power dissipation limit for the FETs. It is apparent from an examination of the preceding nine figures that the "worst case" scenario for thermal energy generation within a given FET is for it to continuously conduct the rated load current. In conclusion, SPICE simulation exercise fully supports the switching device stress levels predicted for the PRAL inverter in the preceding chapters.

TABLE VII

AVERAGE THERMAL POWER GENERATED IN THE PRAL INVERTER FETS

SWITCH	AVERAGE THERMAL POWER (WATTS)
SUA	1.0
SLA	0.4
SSA	4.6
SUB	38.2
SLB	0.8
SSB	15.8
SUC	4.1
SLC	55.4
SSC	20.3

7.4 Summary

This chapter presented a rationale for employing digital computer based circuit simulation tools to evaluate power electronics based systems in the early phases of development and discussed their implementation limits. An approach was described for employing an available implementation of SPICE to examine the electrical viability of the PRAL inverter and to examine the stresses placed on its switching devices. A suitable power matrix model was constructed along with the minimal control logic circuitry needed to implement a representative PRAL inverter. FETs were used in the power matrix in place of more appropriate IGBTs in order to overcome numerical convergence limitations in SPICE resulting from undue complexity of the accompanying control logic circuitry. Logic circuitry needed to generate the variable boost current commands required to regulate the voltage divider potential could not be included due to convergence limitations in SPICE, forcing a fixed voltage divider potential to be used in the simulation.

The results of the SPICE simulation established proof-of-concept for all functional aspects of the PRAL inverter except for regulation of the voltage divider potential. The voltage stress and current stress predictions of Chapter V were validated. The thermal stress placed on the switching devices resulted almost exclusively from load current conduction losses with relatively minor heat generation from switching related losses.

CHAPTER VIII

STATE VARIABLE SIMULATION AND ANALYSIS

8.1 Introduction

This chapter employs state-variable modeling and simulation to examine the internal behavior and output performance of the PRAL inverter and to compare the output performance of a prominent SPRDL design with that of a comparable PRAL inverter. The chapter begins with a brief discussion of the relevant limitations and assumptions associated with the state-variable modeling process that potentially affect the accuracy of the simulation results. The simulation experiments are initially directed at validating the boost current computation and voltage divider node stabilization strategies proposed in Chapter VI. Next, simulation experiments are conducted to compare the PRAL inverter with a selected SPRDL design in terms of output waveform spectral quality, device stresses, and conversion efficiency. Finally, the performance characteristics of a PRAL inverter configured with load back EMF based cost-function current control is compared to the selected SPRDL inverter.

8.2 State-Variable Simulation Issues and Tools

Modern digital computer based state-variable simulation and analysis tools do not present the barriers to inverter control logic modeling encountered with the SPICE circuit model in the previous chapter. The disadvantage of the state-variable approach is that detailed switching device behavior during turn-on and turn-off is not easily incorporated into the model. Fortunately, soft-switched voltage-source inverters are relatively insensitive to most non-ideal device

characteristics. This is because the inverter soft switching circuitry, rather than the terminal characteristics of the device, predominately determine the terminal voltage of all switching devices during turn-on and turn-off. The only non-ideal switching device characteristic significantly affecting soft-switched inverter behavior is the device turn-off current. Fortuitously, the net influence of this particular device characteristic on the internal voltages and currents of each inverter type considered in this study is easily incorporated into the respective state-variable models.

Several simplifying assumptions are made in the modeling process to minimize extraneous influences that could erroneously bias the simulation results in favor of a particular inverter topology and to efficiently conduct the simulation experiments using the available simulation tools. First, the DC voltage source feeding the inverters is assumed to be constant with zero series impedance. This practice is commonly seen in the literature. The governing differential equations for each inverter model are based on the assumption of pseudo-ideal switches that are non-ideal only in the sense that a linearly decaying turn-off current is integrated into the inverter circuit model. This practice is commonly used in the literature when device turn-off effects are considered. The pseudo-ideal switch model does not possess the infrastructure necessary to determine the current distribution between parallel conducting devices. It is thus necessary in many situations to estimate cumulative conduction and switching losses for a group of switches rather than for each individual device in a given inverter. This presents little difficulty for the cases considered in this study since the cumulative inverter switching losses typically fall below the maximum value allowed for a single device. Additionally, the distribution of conduction losses amongst switches in a given group is easily inferred in most cases.

The State-Variable based digital simulation tools, MATLAB, SIMULINK, and STATEFLOW, used in this investigation are all part of a popular digital simulation suite. MATLAB is a high-level language geared for simulation of dynamic systems that are described in terms of a state-variable model. SIMULINK is a graphical design tool for constructing

dynamic system models from a set of standard and user-definable graphical building blocks. Standard blocks include integrators, summations, gains, controlled switches, etc. User-defined blocks are implemented using subroutines written in the MATLAB language. STATEFLOW is an extension of SIMULINK that provides for graphical modeling of a Finite State Machine (FSM), such as a PRDL or PRAL inverter. More information on MATLAB, SIMULINK, and STATEFLOW is available in [29], [30], and [31], respectively.

8.3 Inverter State-Variable Simulation Models

8.3.1 The PRAL Inverter State-Variable Simulation Model

The graphical SIMULINK state-variable simulation model for the PRAL inverter is shown in Figure 79. An expanded view of each functional block is provided in Appendix B along with the MATLAB source code that implements the user defined functional blocks.

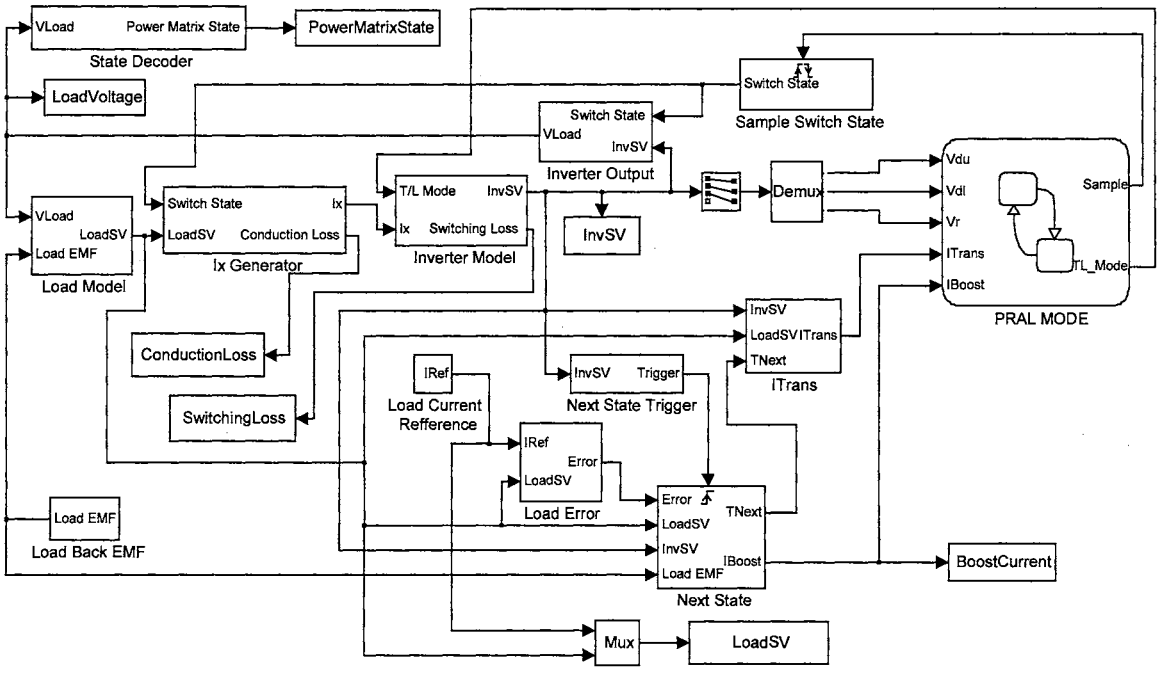


Figure 79. Block diagram of the SIMULINK state-variable model of the PRAL inverter with PI load current control

The blocks shown in Figure 79 fall into one of three categories. The blocks without outputs are data sinks used to record the state-variables associated with their inputs. The blocks labeled "Inverter Model" and "Load Model" employ the differential equations developed in Chapter V to model the PRAL inverter and its associated three-phase load, respectively. The "Inverter Model" block contains additional logic used to estimate switching losses. The remaining blocks model the PRAL control system. The "PRAL Mode" block is a STATEFLOW block used to emulate the state-machine aspects of the PRAL inverter control system. The "Next State Generator" control block is activated near the end of each T mode to determine the appropriate power matrix state at the end of the next T mode. Different implementations of the "Next State Generator" and "Load Error" blocks are used to explore the various control strategies considered in this chapter. The remaining blocks are independent of the control strategy. Their functionality and arrangement are primarily a result of SIMULINK and STATEFLOW modeling requirements rather than the PRAL inverter control system design. Consequently, they can not be described in a narrative fashion without an accompanying detailed discussion of SIMULINK and STATEFLOW, which is outside the scope of this work.

8.3.2 The SPRDL State-Variable Simulation Model

Figure 80 shows a circuit diagram of the three-phase SPRDL inverter proposed in [9]. Figure 81 shows the corresponding SIMULINK model used throughout the remainder of this work. Like the SIMULINK model of the PRAL inverter, Figure 81 contains an "Inverter Model" block, a "Load Model" block, several control system blocks, and various data sink blocks. Again, there is a single STATEFLOW block, labeled "SPRDL MODE" in this case, that implements the state-machine aspects of the inverter. Appendix C contains expanded views of each block along with source code listings for all associated user-defined procedures. As with the PRAL inverter, detailed explanation of the SIMULINK model is not possible without providing extensive details of MATLAB, SIMULINK, and STATEFLOW, and is thus omitted.

Although the inverter described in [9] is a three-phase design, the load current control strategy proposed in [9] is for a single-phase version of the inverter. The extrapolation of this control strategy to the three-phase version used throughout the remainder of this study was accomplished as follows. The variable hysteresis band control technique described in [9] was implemented in all three inverter phase legs. In the single-phase SPRDL inverter, collapse events occurred whenever the single-phase current exceeded the hysteresis band limits. In the three-phase version developed here, link collapse events occur whenever one or more of the load phase currents exceed its respective hysteresis band limits. Additionally, the practice of adjusting the current error tolerance band to match the load current error that exists when a link collapse event occurs is preserved and is independently applied to each phase. With these exceptions, the three-phase SPRDL inverter considered throughout the remainder of this document is identical to that proposed in [9].

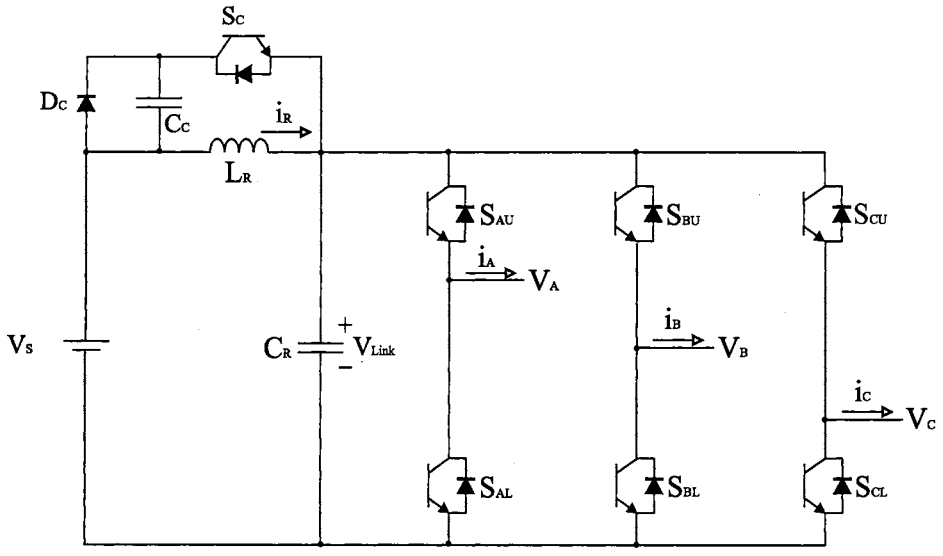


Figure 80. Circuit diagram of the SPRDL inverter proposed in [9]

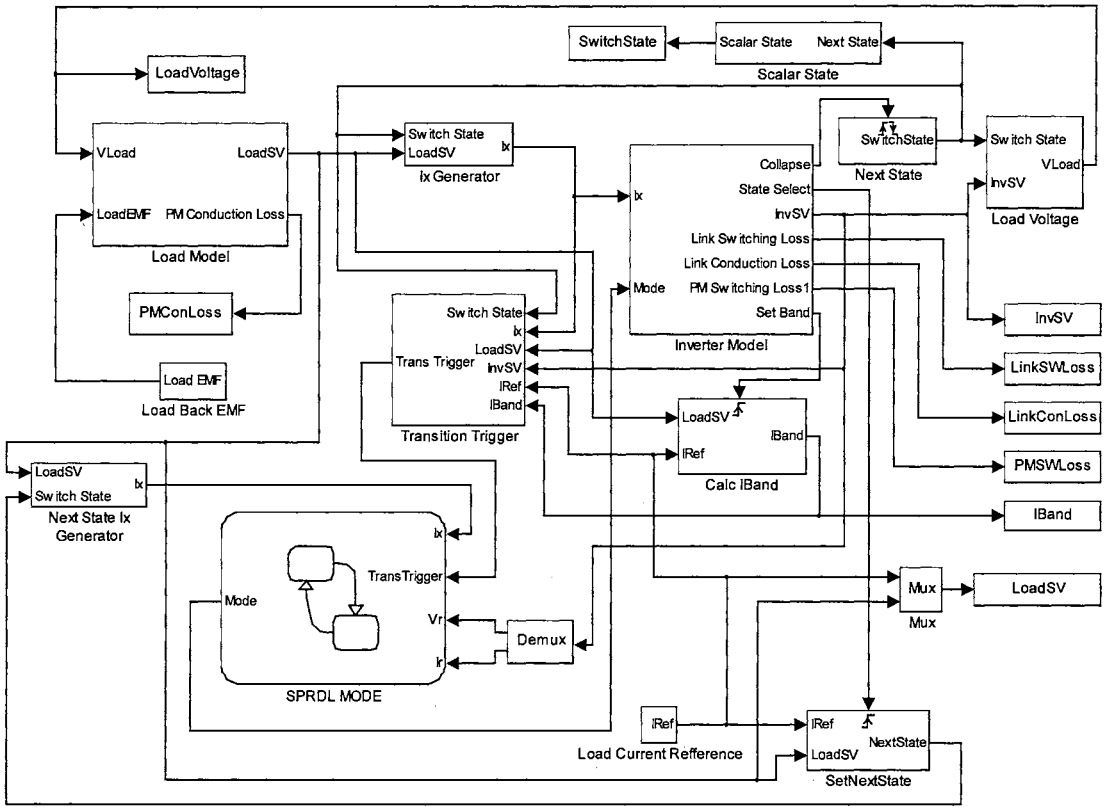


Figure 81. SIMULINK Block diagram of the three-phase SPRDL inverter model

8.4 Validation of the Boost Current Computation and Voltage Divider Node Potential Stabilization Strategies

8.4.1 Objectives and Experimental Model Parameters

This section uses state-variable simulation to demonstrate important aspects of the PRAL inverter's internal behavior that eluded validation in the SPICE analysis presented in Chapter VII. The two issues examined in this section are the boost current computation and voltage divider node potential stabilization strategies that were described in Chapter VI. The results of four simulation experiments are presented to demonstrate the effectiveness of both schemes. The first two experiments use the version of the boost current computation procedure that incorporates

real-time estimates of the load back EMF to compensate for load effects on the resonant circuit. The first of these two experiments uses relatively small voltage divider capacitors, 500 μF, while the second uses larger capacitors, 1500μF. This is done to demonstrate the impact of voltage divider capacitor size on the fraction of T modes in which the control system elevates the boost current to adjust the voltage divider node potential. The third and fourth experiments demonstrate the version of the boost current computation procedure that does not use real-time estimates of the load back EMF. For these experiments, the fixed boost current component, I_{Fixed}, is augmented to accommodate load effects under the worst possible conditions. Again, the first and last of these experiments are conducted using 500 μF and 1500μF voltage divider capacitors, respectively.

The PRAL inverter configuration selected for this exercise is designed to drive a 240 Volt (RMS) three-phase load with a rated peak current of 100 Amps (70.7Amps RMS). To avoid voltage saturation effects, a power matrix voltage of 400 Volts is used in lieu of the minimum theoretically required 391.9 Volts. This is a common practice and constitutes a power matrix voltage reserve of approximately 2%. The load back EMF and phase inductance are based on a load power factor of 0.8 and a load phase resistance of 0.2 Ohms. The resonant circuit component values are based on the "first-cut" component selection guidelines provided in Chapter VI. The value of T_{TO} used for the switching devices is typical of lower cost IGBT devices with the voltage and current ratings required for this configuration. The PRAL inverter and load model parameters are listed in Table VIII. Finally, conventional PI load current control was used in all four simulation experiments.

TABLE VIII

COMMON MODEL PARAMETERS USED TO VALIDATE THE BOOST CURRENT COMPUTATION AND VOLTAGE DIVIDER NODE STABILIZATION STRATEGIES

PARAMETER	VALUE
C_{DL}, C_{DU}	*500 μF
C_R	2.0 μF
f_{Load}	60 Hz
I_{Fixed}	5.0 A
I_{Ref}	100.0 A
L_R	2.0 μH
L_S	1.59 mH
$\|\mathbf{E}\|$	173.9 V (RMS)
Q_R	100
R_S	0.20 Ω
V_{DAT}	1.0 V
V_{DBT}	1.5 V
T_{TO}	750 ns
V_D	1.7 V
V_S	400 V
V_{SW}	2.3 V
V_{BSW}	5.7 V

* Value differs where indicated

8.4.2 Boost Current Control Incorporating Real-Time Load Back EMF Estimates

The boost current computation method examined in this subsection incorporates the projected load influence on the resonant circuit via real-time estimates of the load back EMF. This is accomplished using the load back EMF dependent boost energy component, E_{LVD}, given in 6.2.3.15. Two simulation experiments were conducted to illustrate the influence of voltage divider capacitor size on the boost current and the voltage divider node potential error. Figures 82 and 83 show plots of the voltage divider node potential error and boost current obtained using 500μF and 1500μF voltage divider capacitors, respectively. For enhance clarity, the time interval shown in the figures corresponds to the 2.77 ms that the commanded load current occupied Sector Ω_{100}. In each case, the simulation was conducted over two complete output waveform periods, or approximately 33.4ms. This was done to expose "worst case" conditions for which the boost current computation or voltage divider node potential stabilization strategies might prove ill suited. In each case, both the auxiliary link and the voltage divider node potential behaved properly throughout the simulation time interval using the modest value of I_{Fixed} given in Table VIII.

The Boost current plots in Figures 82 and 83 show that the commanded boost current remains low, less than about 15 Amps, except when it is elevated to I_L to adjust the voltage divider potential. The total fraction of T modes used to correct the voltage divider potential is significantly higher for 500μF voltage divider capacitors than for 1500 μF capacitors, 18.1% and 11.0% respectively.

The boost current plots in both figures show several sizable time intervals during which every available T mode was used to adjust the voltage divider potential. The most pronounced clusters lie between 1.4 ms and 2.0 ms in Figure 82. Similar clusters occurred throughout the 34.4 ms simulation interval. Interestingly, there was no apparent correlation between the location of the clusters and the phase of the commanded load current throughout the simulation interval.

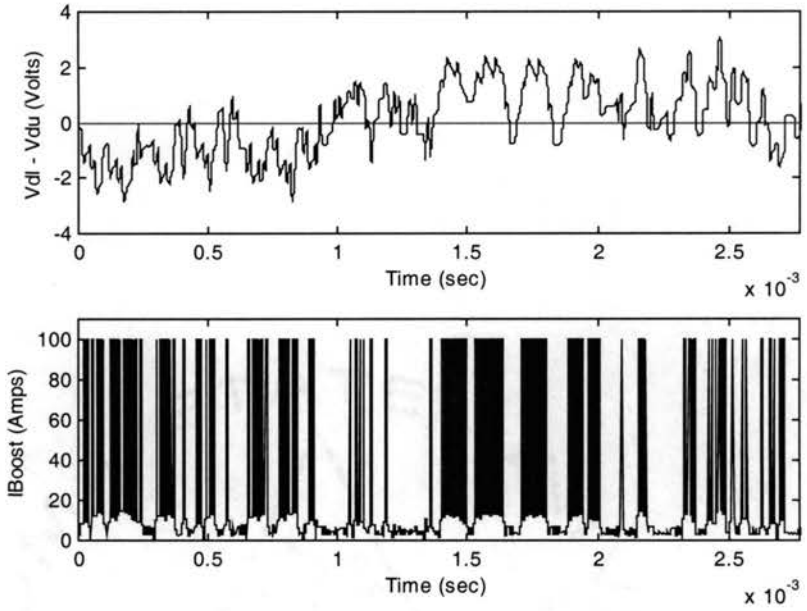


Figure 82. Plot of voltage divider node potential error (upper) and boost current (lower) using 500μF voltage divider capacitors and real-time load back EMF estimates

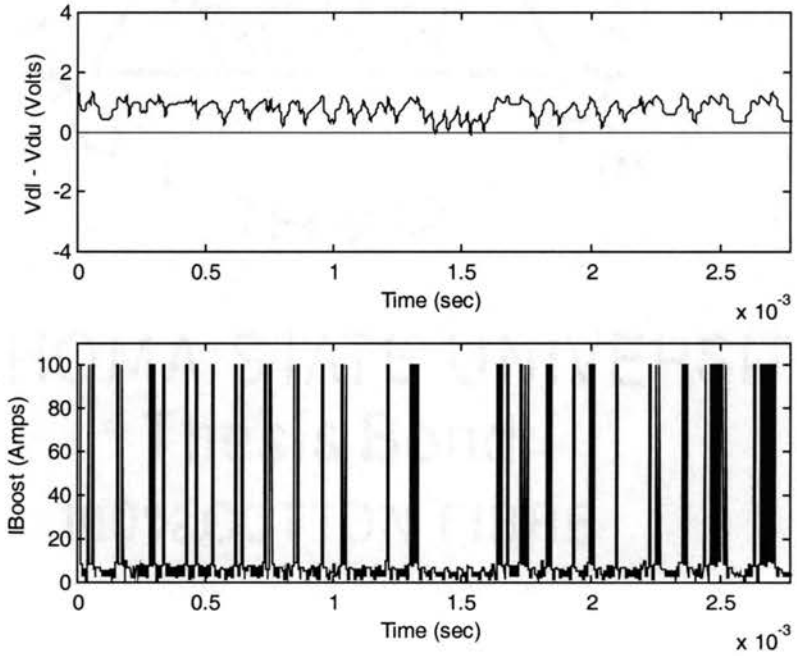


Figure 83. Plot of voltage divider node potential error (upper) and boost current (lower) using 1500μF voltage divider capacitors and real-time load back EMF estimates

Two principal mechanisms are responsible for the pseudo-random clustering effect seen in Figures 82 and 83. First, the boost current elevation technique becomes less effective at transferring net charge between the voltage divider node and the power matrix as $|v_{DU}(t) - v_{DL}(t)|$ increases. In the case of the 500 μF voltage divider capacitors shown in Figure 82, the deflection in $v_{DU}(t) - v_{DL}(t)$ will be approximately three times larger for a given disturbance than for the case shown in Figure 83 where 1500 μF capacitors are used. Consequently, the boost current must be elevated over a larger number of consecutive T modes to compensate for a given disturbance as the size of the voltage divider capacitors decreases. This assertion is fully consistent with the plots shown in Figures 82and 83. Second, the load current control strategies used in this work produce chaotic power matrix state patterns. This causes the switched load current, $i_X(t)$, to be chaotic as well. Since $i_X(t)$ is responsible for destabilizing the voltage divider node potential, it follows that the T modes dedicated to stabilizing the node potential form a chaotic pattern in the simulation time interval, as seen in Figures 82 and 83. This is consistent with the apparent lack of correlation between the observed voltage divider node potential adjustments and the phase of the commanded load current.

The preceding experiments were repeated with the boost energy component associated with load interactions and voltage divider node potential imbalance given in 6.2.3.15 replaced with the expression given in 6.2.3.16, which considers only voltage divider node potential imbalance. This removes the need for real-time load back EMF estimates and thus yields an implementation that is more competitive with PRDL designs, which have historically ignored load interaction effects. To ensure proper operation of the auxiliary link, 6.2.3.15 was used to estimate the "worst case" boost energy component needed to compensate for load interaction under balanced voltage divider conditions. Based on the values given in Table VIII and using 6.2.3.15, a situation could develop requiring 17.3 Amps of boost current to compensate for load influences on the resonant circuit. Combining this current with the value of I_{Fixed} given in Table VIII results in a modified

fixed boost current of 18.0 Amps. Results of simulations conducted using 500 μF and 1500μF voltage divider capacitors along with this boost current computation method are shown in Figures 84 and 85, respectively.

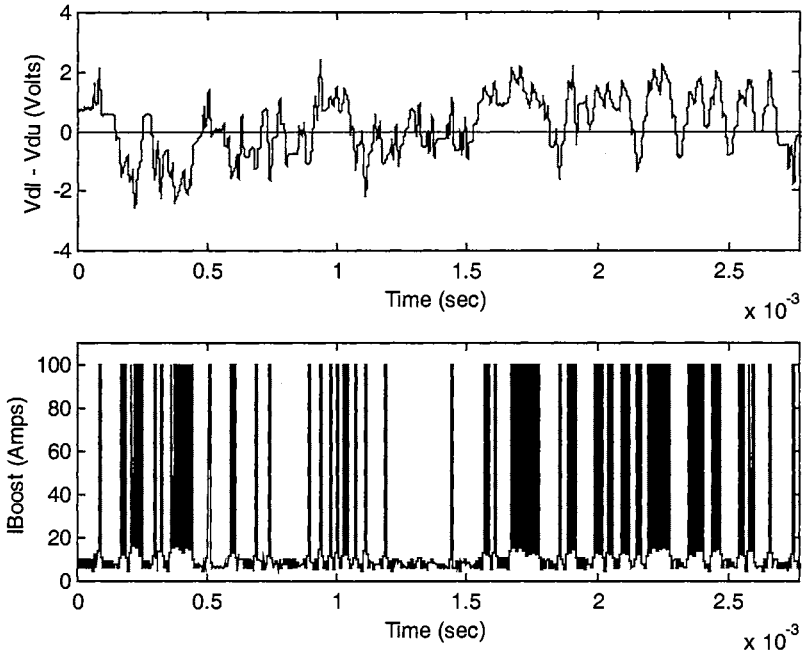


Figure 84. Plot of voltage divider node potential error (upper) and boost current (lower) shown in Sector Ω_{100} for a PRAL inverter using 500 μF voltage divider capacitors and fixed "worst case" load effect estimates

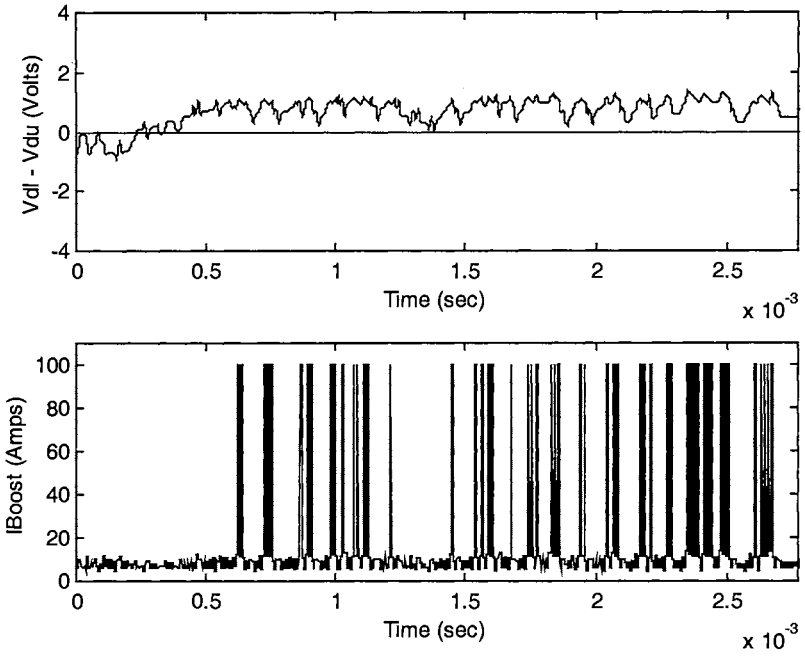


Figure 85. Plot of voltage divider node potential error (upper) and boost current (lower) shown in Sector Ω_{100} for a PRAL inverter using 500 μF voltage divider capacitors and fixed "worst case" load effect estimates

The Fraction of T modes used to adjust the voltage divider potential, the switching losses, and the total conversion losses for each of the four preceding simulation experiments are summarized in Table IX. Inspection of the table indicates that excluding the real-time load back EMF estimate from the boost current computation had no significant effect on the fraction of T modes used to adjust the voltage divider node potential. Perhaps more importantly, replacing the real-time back EMF estimate with a fixed "worst case" value did not increase the overall conversion losses and did not significantly affect the total switching losses. In all four cases, the combined switching loss in all nine PRAL inverter switching devices was less than 10 Watts, which is approximately 0.035% of the 29.4 kVA complex power provided to the load. Moreover, the total conversion losses, including copper losses in the resonant circuit, were less than 2.0% of the inverter's rated complex output power. The only significant distinction between the results obtained for the four cases was due to the use of different voltage divider capacitor sizes. The use of 1500 μF capacitors in lieu of the smaller 500 μF components produced an approximate 38% reduction in

the number of T modes needed to adjust the voltage divider node potential. However, this had no significant effect on overall conversion efficiency.

The power matrix filter capacitor, which the voltage divider capacitors emulate, constitutes a substantial portion of the bulk and weight of the overall power conversion circuitry in both conventional and soft-switched bridge inverters. Unless there is some necessity to use large capacitors, the smallest voltage divider capacitors that permit the PRAL inverter to operate properly should be used. Additional experiments conducted for this PRAL inverter design revealed that the minimum viable voltage divider capacitor size is approximately 325 μF. Assuming a 50% safety factor, the lowest acceptable voltage divider capacitor size is approximately 500 μF. It is worth noting that the power matrix filter capacitor of a conventional bridge inverter of similar power rating would typically be rated at several thousand micro-Farads.

TABLE IX

SUMMARY OF CONVERSION LOSSES AND VOLTAGE DIVIDER STABILIZATION ACTIONS RESULTING FROM VARIABLE AND FIXED ESTIMATES OF LOAD INTERACTION BOOST ENERGY REQUIREMENTS

Load Interaction Boost Energy Estimate	C_{DU}, C_{DL} (μF)	Switching Losses (Watts)	Total Conversion Losses (Watts)	Fraction of T Modes used to Correct Voltage Divider Potential
Variable	500	9.71 {0.033}	576.4 {1.96}	18.1%
Variable	1500	7.62 {0.026}	566.4 {1.93}	11.0%
Fixed	500	9.96 {0.034}	566.1 {1.93}	18.7%
Fixed	1500	7.78 {0.026}	564.7 {1.92}	10.5%

* Values in brackets indicate the corresponding percentage of the 29.4 kVA supplied to the load

8.5 Selected Waveforms Generated Using the SIMULINK PRAL Inverter Model

This section contains selected waveforms obtained using the SIMULINK model parameters given in Table VIII. The plots demonstrate some of the PRAL inverter's internal characteristics predicted in preceding chapters. The boost current is computed using a fixed "worst case" load effect estimate and a simple PI load current control scheme is used to select power matrix states. Figure 86 shows plots of the auxiliary link voltage, resonant circuit inductor current, and the boost current. The auxiliary link voltage plot illustrates the variability in the duration of both the L and T modes that result from discontinuities in the switched load current, $i_X(t)$, and the occasionally high boost current levels used to adjust the voltage divider potential.

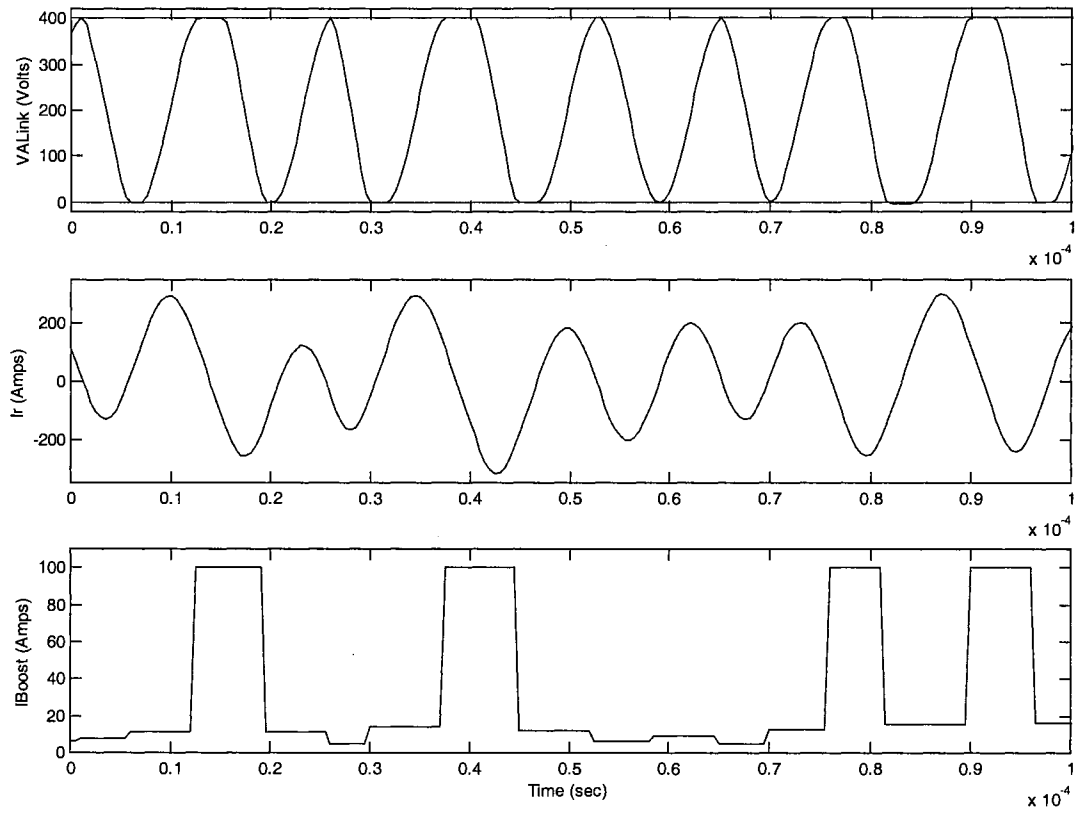


Figure 86. Plots of the auxiliary link voltage (upper), resonant circuit inductor current (middle), and boost current (lower) for the PRAL inverter design specified in Table VIII

Figure 87 shows a normalized plot of the auxiliary link voltage spectrum. The peak occurs at 78.67 kHz, less than 1.7% below the designed 80 kHz free-running frequency. The broad secondary peaks centered at roughly 66 kHz and 92 kHz are due to modulation resulting from elevating the boost current to adjust the voltage divider potential and from occasional large discontinuities in the switched load current, $i_X(t)$. Peaks corresponding to the second and third harmonics of the fundamental auxiliary link voltage frequency are discernable at approximately 157 kHz and 236 kHz, respectively.

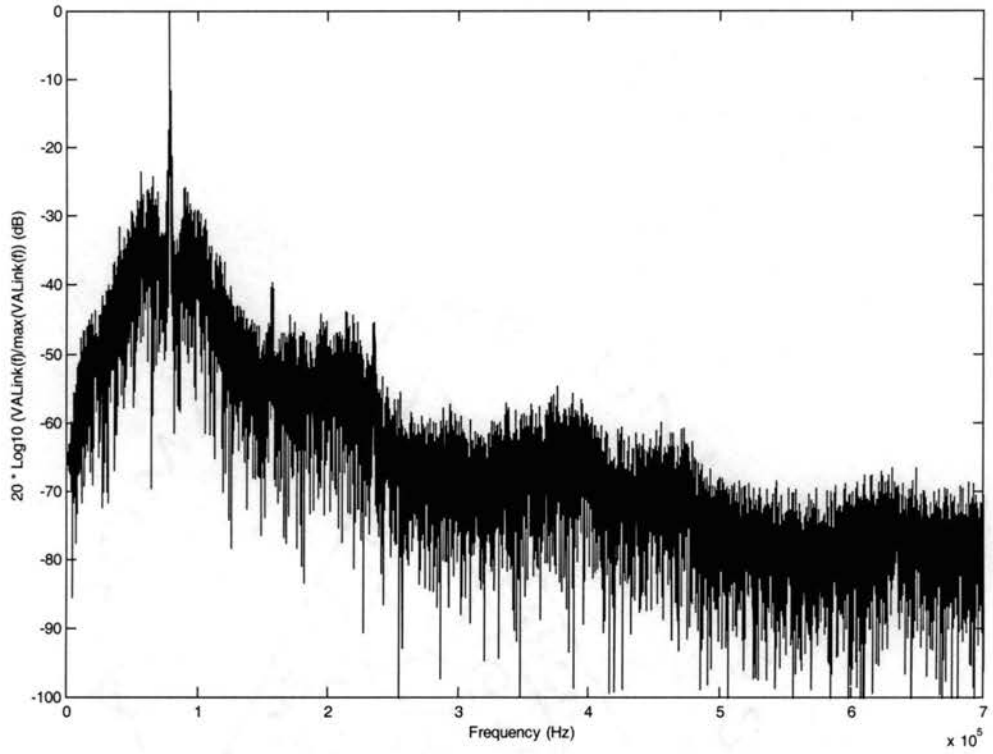


Figure 87. Normalized spectrum of the auxiliary link voltage, $V_{ALink}(f)$, for the PRAL inverter model specified in Table VII

Figure 88 shows the line-to-line voltage presented to the load between phase terminals A and B along with auxiliary link voltage. Comparison of the two plots shown in the figure reveals that the frequency of switching opportunities, which occur at each crest of the auxiliary link voltage waveform, significantly exceeds the frequency of commanded switching events

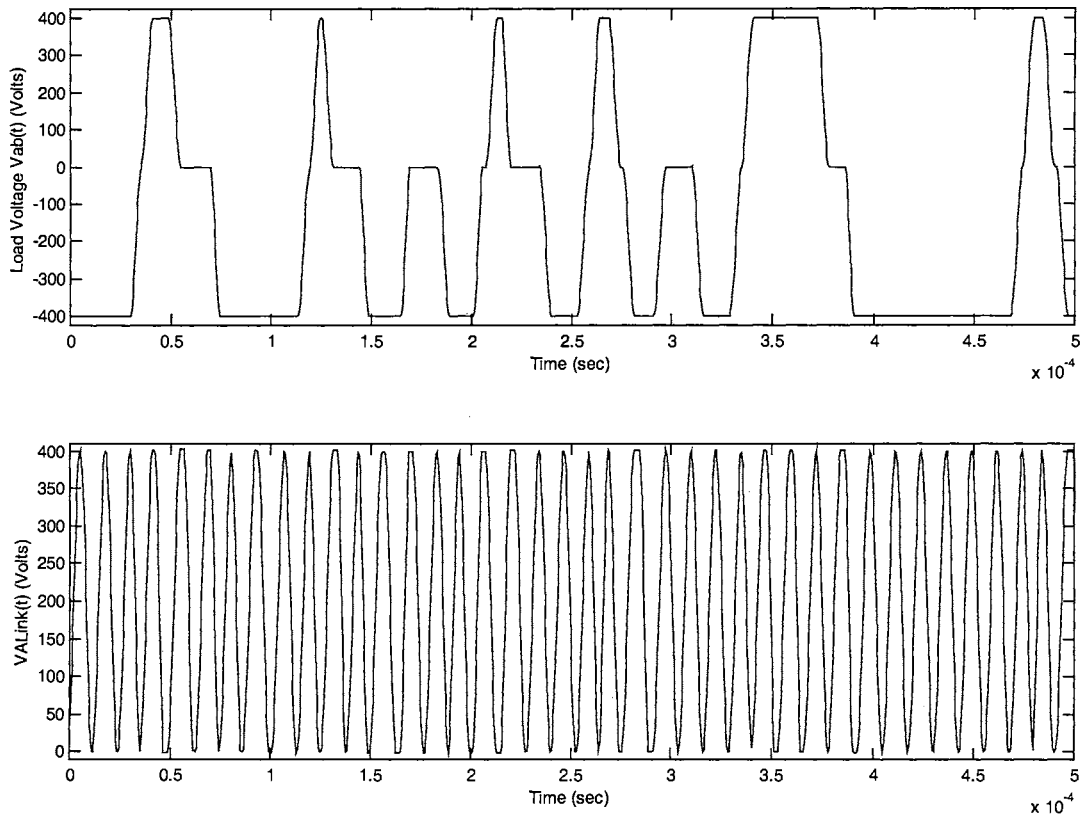
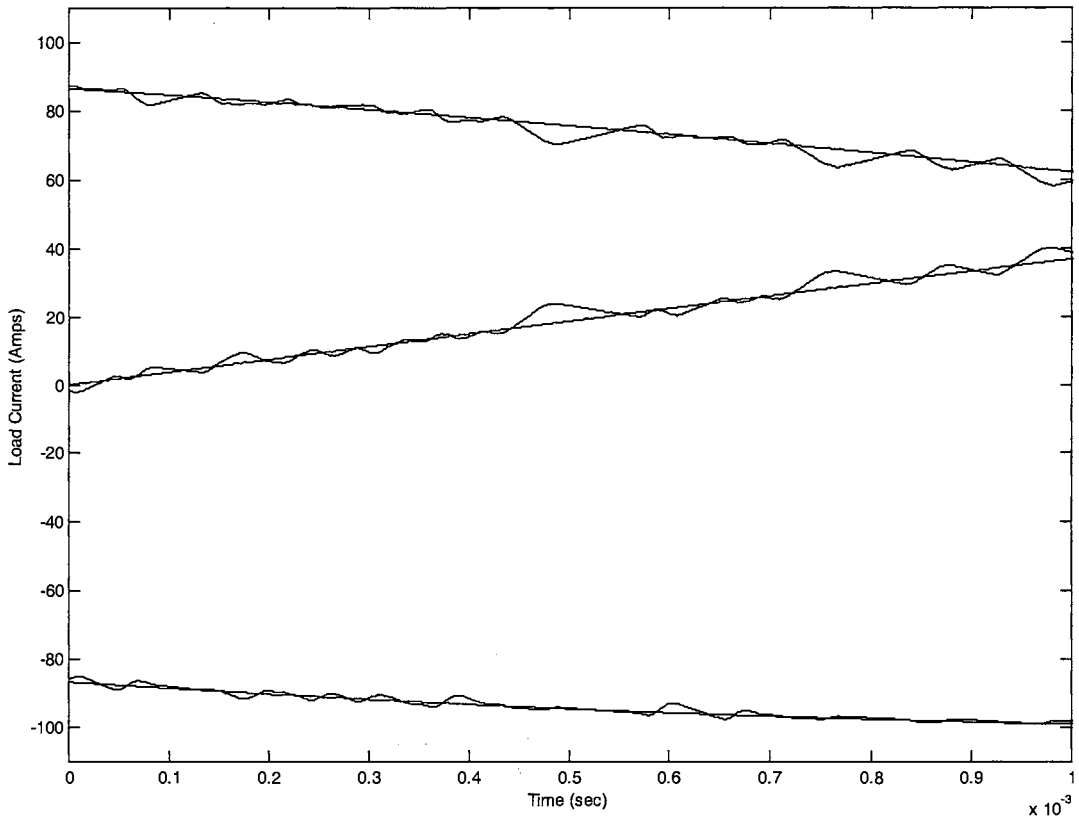


Figure 88. Plots of the PRAL inverter output line-to-line voltage $V_{AB}(t)$ applied between load phases A and B (upper) and the auxiliary link voltage $v_{ALink}(t)$ (lower)

Figure 89 shows a plot of the load phase currents along with the respective commanded phase currents. The phase currents are continuous, due to the load phase inductance, and track the reference currents reasonably well. The larger excursions seen in the figure are due to the low value of V_S selected for the power matrix voltage. When the inverter operates at rated output voltage, as in this case, voltage saturation effects can degrade the output waveform quality by severely limiting the voltage that the inverter can place across the load phase inductances. If the load back EMF is reduced, as in the case of operation at reduced output frequencies, or the value of V_S is increased sufficiently, this effect essentially vanishes. It should be noted that the same phenomena is seen in both conventional and PRDL inverters.



Upper = Phase B Middle = Phase A Lower = Phase C

Figure 89. PRAL inverter load phase currents shown with their corresponding commanded currents

8.6 Selected Waveforms Generated Using the SIMULINK SPRDL Inverter Model

This section contains a compilation of selected SPRDL inverter waveforms that are intended to demonstrate the SIMULINK SPRDL inverter model and to reinforce discussions from previous chapters. Unlike the PRAL inverter, the SPRDL boost current used for the SPRDL model is fixed at 100 Amps. This is due to the design of the resonant link circuit described in [9]. The link collapse event can be initiated at any commanded time, provided there is sufficient energy available to fully collapse the link. Losses in the resonant circuit inductor and voltage drops across the switching devices embedded in the resonant circuit dissipate the energy stored in the

resonant circuit inductor. This places an upper limit on the time allowed between link collapse events. The 100 Amp boost current level was selected to maximize the controllability of the inverter's collapse events while ensuring that device current stress levels do not exceed those occurring in the PRAL inverter. The parameters used in the SIMULINK SPRDL inverter model were extracted from [9], where possible, and are listed in Table X.

TABLE X

SIMULINK SPRDL INVERTER MODEL PARAMETERS

PARAMETER	VALUE
C_C	8 μF
C_R	0.44 μF
f_{Load}	60 Hz
I_{Ref}	100.0 A
L_R	9.0 μH
L_S	1.59 mH
$\|\mathbf{E}\|$	173.9 V (RMS)
Q_R	100
R_S	0.20 Ω
T_{TO}	750 ns
V_D	1.7 V
V_S	400 V
V_{SW}	2.3 V

Figure 90 shows plots of the SPRDL inverter link voltage and resonant circuit inductor current. The link voltage normally peaks at approximately 550 Volts but reaches 604 Volts in one instance due to modulation resulting from the switched load current. Unlike the PRAL inverter, which employs the large power matrix filter capacitance to squelch such voltage transients, the SPRDL is protected only by the relatively small clamping capacitor C_C.

Inspection of the resonant circuit inductor current shows several cases where $i_R(t)$ nearly decays to zero before the link collapses, and yet the inverter functions properly. In these cases, the energy needed to collapse the link comes largely, or entirely in a few cases, from the switched load current rather than from energy stored in the resonant circuit inductor. This behavior is consistent with the results reported in [9].

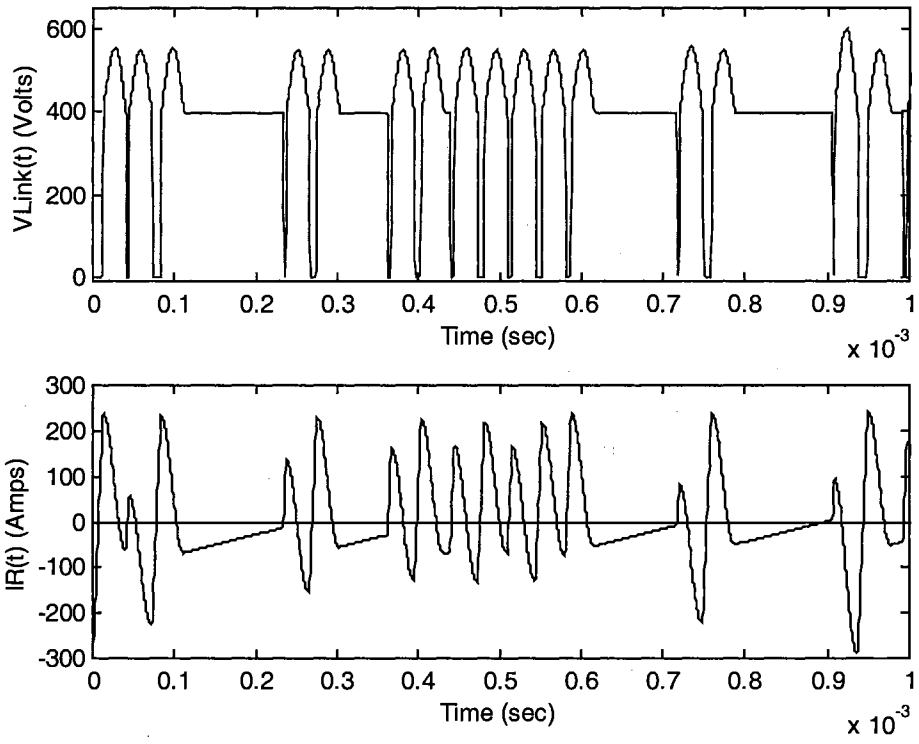


Figure 90. Plot of the link voltage, $v_{Link}(t)$ (upper), and resonant circuit inductor current, $i_R(t)$ (lower), for the SPRDL inverter design specified in Table X

Figure 91 shows the normalized link voltage spectrum $V_{Link}(f)$ for the SPRDL inverter. The average link frequency is approximately 25 kHz, with both even and odd harmonics clearly visible. The variable collapse delay characteristic of the SPRDL design produces a broad distribution around the average link frequency, as expected.

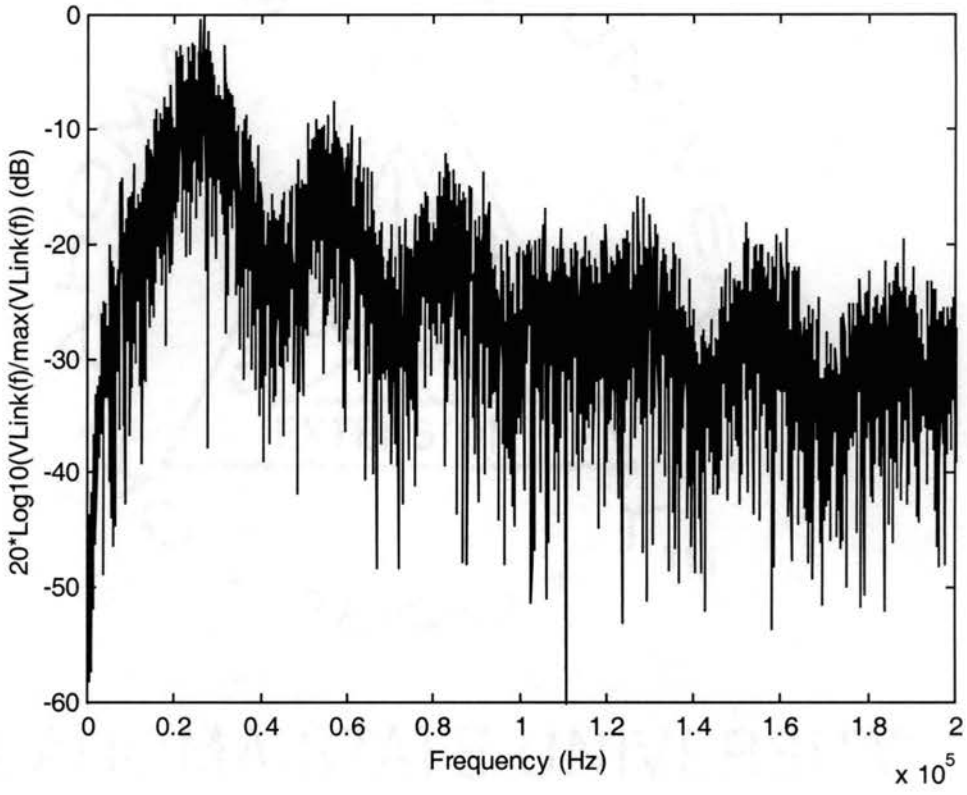


Figure 91. Normalized spectrum of the link voltage, $V_{Link}(f)$, for the SPRDL inverter specified in Table IX

Figure 92 shows one of the line-to-line voltages, $v_{AB}(t)$, presented to the load along with the link voltage, $v_{Link}(t)$. The plots shown are fully consistent with those shown in [9], which were generated for a single-phase implementation of the SPRDL inverter.

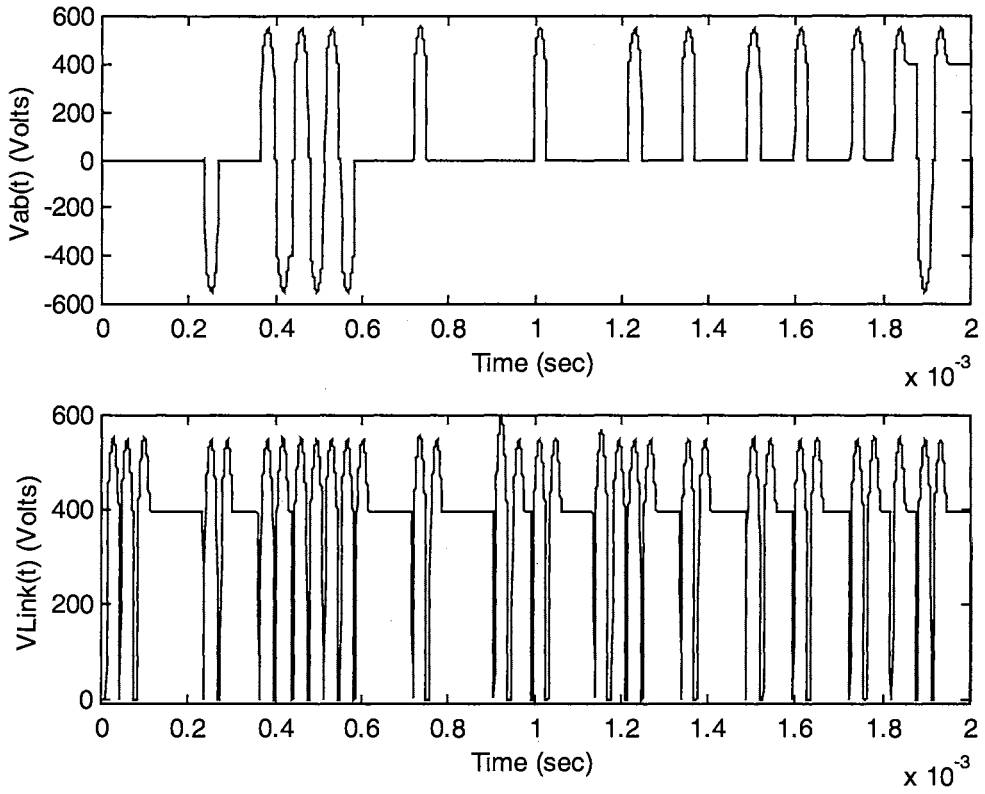
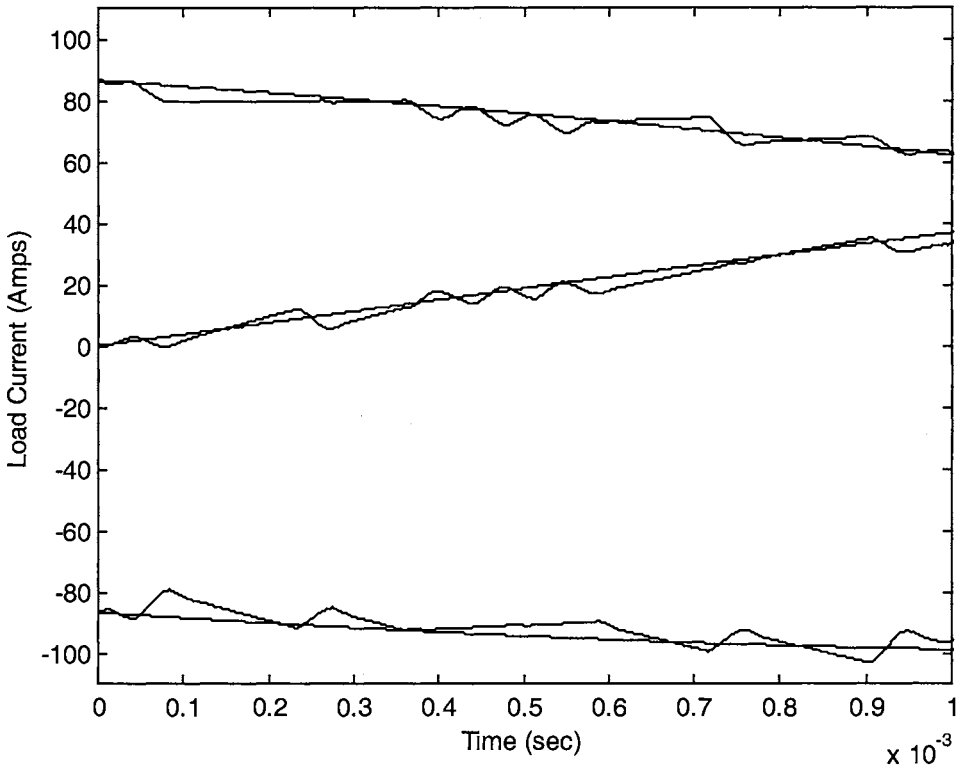


Figure 92. SPRDL inverter output line-to-line voltage $V_{AB}(t)$ (upper) applied between load phases A and B and the link voltage, $v_{Link}(t)$ (lower)

Figure 93 shows load phase currents and the corresponding commanded phase currents generated using the SPRDL model. The load currents track their commanded values reasonably well, suggesting that the three-phase extrapolations made to the variable tolerance band control scheme proposed in [9] were at least moderately successful.



Upper = Phase B Middle = Phase A Lower = Phase C

Figure 93. SPRDL inverter load phase currents shown with their corresponding commanded currents

8.7 Comparison of the PRAL and SPRDL Inverters

This section compares the PRAL inverter to the three-phase implementation of the SPRDL inverter described in [9]. The comparison is made in terms of output waveform quality, device losses, and overall conversion efficiency. The major differences in the inverter designs complicate this task in that there are no clear criteria for designing "similar" inverters for comparison. The current control technique, resonant circuit frequency, and parameter optimization strategy are just a few of the design issues that differ substantially between the two topologies. However, there is one aspect of the resonant circuit frequency that is common to both designs. Both topologies rely heavily on real-time measurements of the resonant circuit inductor current. The Hall-Effect sensors needed to measure this current have a cut-off frequency of approximately 150-200 kHz. It follows that the scalability of both topologies, in terms of resonant circuit frequency, is limited by a common impediment. By comparing the two topologies based on a common free-running resonant circuit frequency, each design has approximately the same potential for performance growth as advances in current measurement devices occur.

The SPRDL inverter proposed in [9] has been physically prototyped and successfully operated in its single-phase form. It is thus a logical basis for the comparison. The SPRDL inverter parameters in Table IX are based on the single-phase prototype described in [9]. The PRAL inverter specified in Table VII was intentionally designed for comparison with this specific SPRDL inverter. The 80 kHz free-running resonant circuit frequency, the 400 Volt DC input voltage, and the load are the same for both inverter designs. As a point of interest, the average link voltage of the SPRDL inverter is within one volt of the DC input voltage, due to the action of the clamping capacitor, C_C. Thus, the use of equal DC input voltages for both topologies is entirely appropriate.

The PRAL inverter considered in this section was designed to demonstrate the performance characteristics of a "low end" configuration against those of a leading SPRDL inverter.

Conventional PI control is used to regulate the load current instead of the more complex cost-function method described in Chapter VI. The control circuitry needed to implement this type of control is no more complex than that required for the variable tolerance band method used in the SPRDL design. The PRAL inverter's boost current is computed using "worst case" load effect estimates in lieu of computations based on real-time load back EMF estimates. Again, this is done to eliminate the need for load back EMF estimates, which are not used in the SPRDL design. Finally, the smallest practical capacitance value, 500 μF, is used for the voltage divider capacitors. Since the voltage divider capacitance contributes to the DC source shunt capacitance, which would normally be several thousand micro-Farads for inverters of this power rating, the inclusion of the split capacitor voltage divider adds negligible net economic cost when compared to the SPRDL design. The net result of the design choices made for the PRAL inverter used in the following comparison with the SPRDL inverter is that there is considerable potential for improvement to both output waveform quality and conversion efficiency through control system enhancements and component value selection.

The following figures and tables illustrate the performance differences between the two inverters operating at output frequencies of 60 Hz, 50 Hz, 40 Hz, 30 Hz, and 20 Hz. In each case, the load back EMF is adjusted to maintain a constant Volts-to-Hertz ratio. The corresponding data are grouped according the output frequency. Each data set consists of load phase current plots, a plot of the Phase A load current spectrum, and Normalized Cumulative Harmonic Distortion (NCHD) plots for each inverter's Phase A load current. A table listing switching device conduction and switching losses, copper losses in the resonant circuit inductor, and total conversion losses is provided at the end of each data set.

The NCHD plots in each of the cases shown below are included to graphically emphasize the spectral distribution of the harmonic distortion components in the load phase current. The definition of NCHD used in the plots is as follows. Let x(t) be a time domain signal defined on the interval [0, T], where $T > 0$. Let $X(k)$, $k \in \{0, 1, 2, \ldots\}$, be the Fourier Series associated with

x(t) in the interval [0, T]. Define the Cumulative Harmonic Distortion (CHD) in x(t) at frequency $\frac{k}{T}$ as,

$$CHD_X(k) = \sqrt{\sum_{j=2}^{k} |X(j)|^2} \qquad 8.7.1$$

Normalizing with respect to the fundamental frequency component in the Fourier Series yields the following expression for the NCHD corresponding to x(t) in [0, T].

$$NCHD_X(k) = \frac{1}{|X(1)|}\sqrt{\sum_{j=2}^{k} |X(j)|^2} \qquad 8.7.2$$

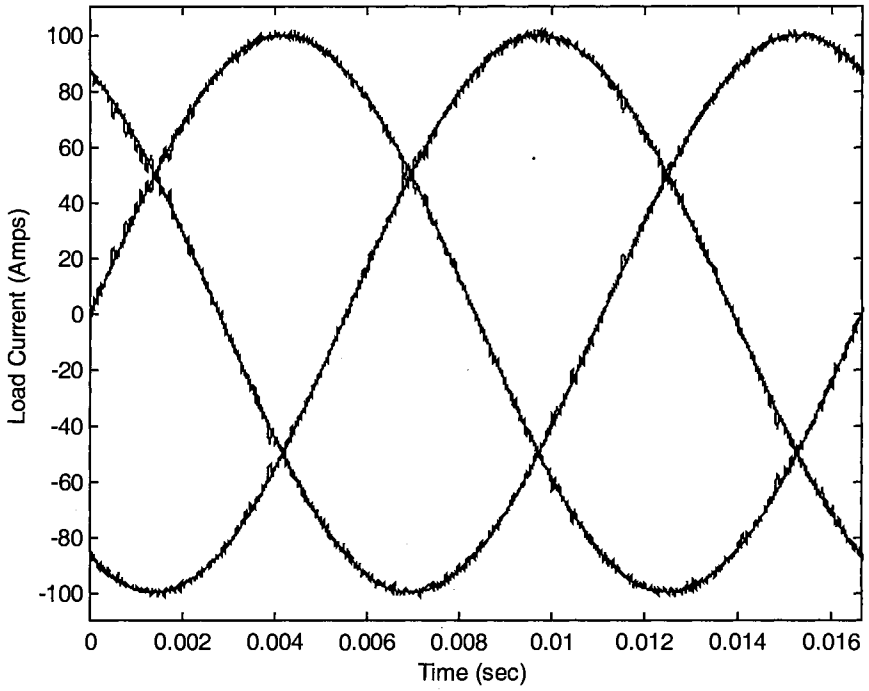


Figure 94. Load and reference currents for the PRAL inverter with PI current control driving the load at 60 Hz

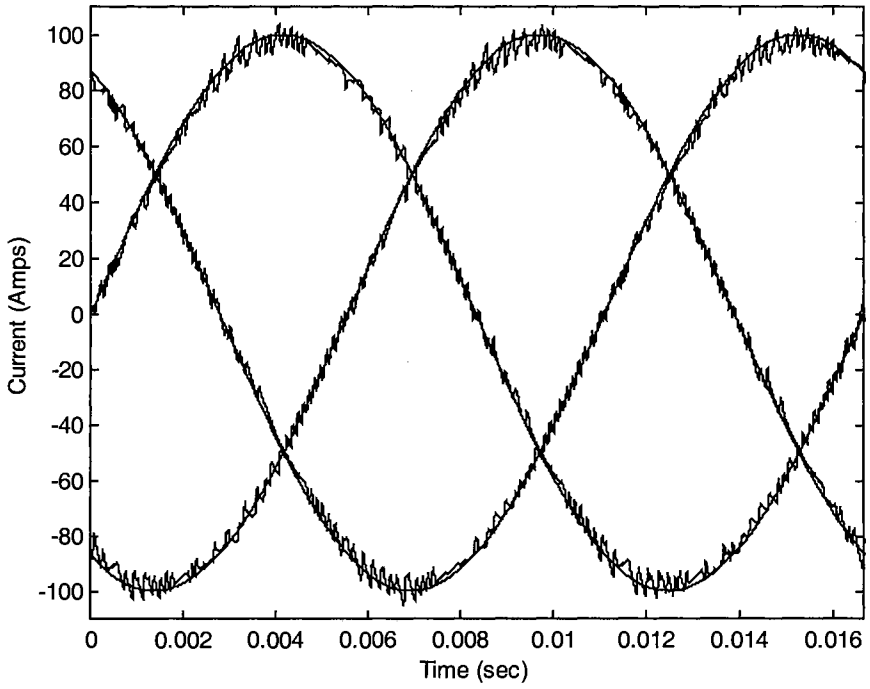


Figure 95. Load and reference currents for the SPRDL inverter driving the load at 60 Hz

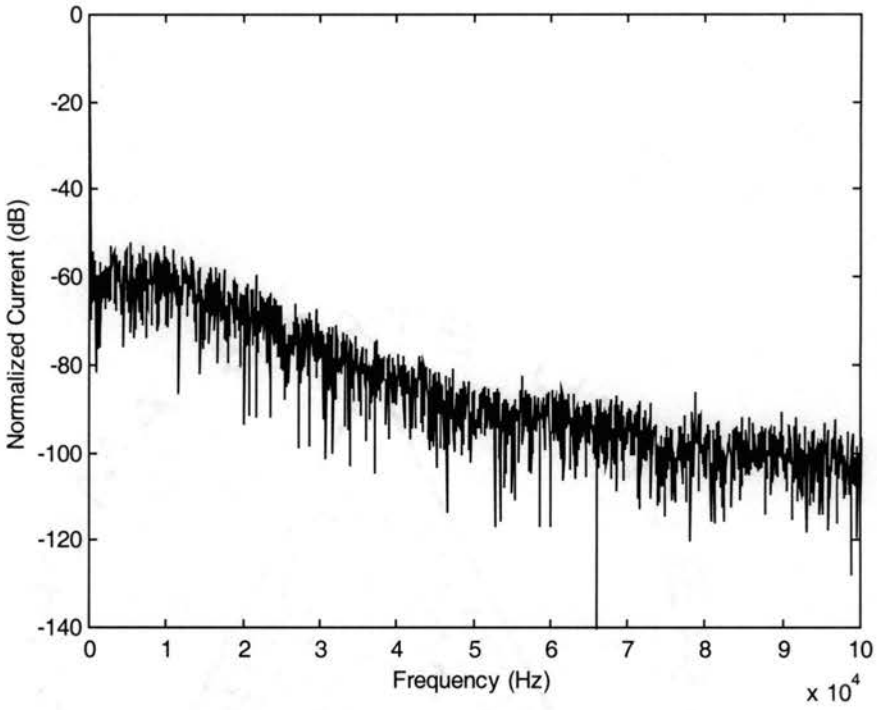


Figure 96. Normalized load current spectrum for the PRAL inverter driving the load at 60 Hz

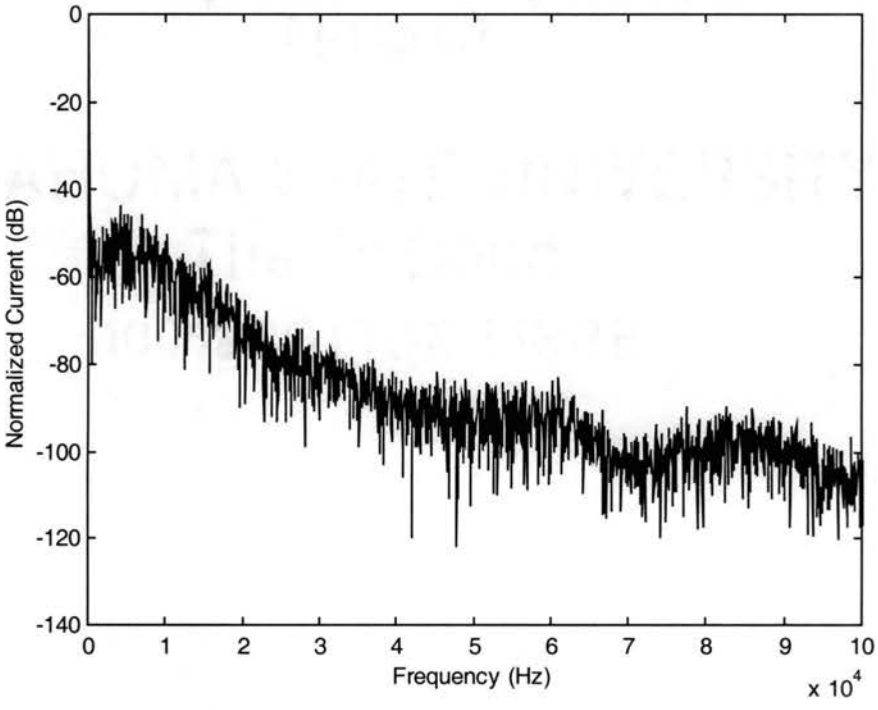


Figure 97. Normalized load current spectrum for the SPRDL inverter driving the load at 60 Hz

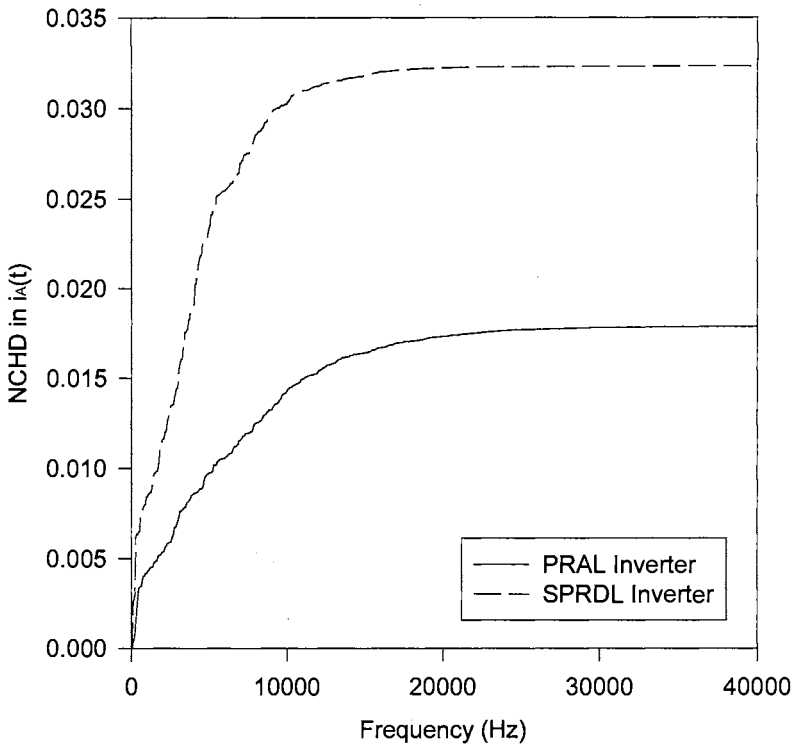


Figure 98. Normalized cumulative harmonic distortion in the Phase A load current produced by the PRAL inverter with PI current control and the SPRDL inverter driving the load at 60 Hz

TABLE XI

SUMMARY OF CONVERSION LOSSES FOR THE PRAL INVERTER WITH PI CURRENT CONTROL AND THE SPRDL INVERTER BOTH DRIVING THE LOAD AT 60 HZ

Inverter Type	Phase Leg Losses (Watts)		Resonant Circuit Losses (Watts)			Total Losses (Watts)
	Device Conduction	Device Switching	Device Conduction	Device Switching	Copper (R_R)	
PRAL	517.27 {1.759}	9.97 {0.034}	NA	NA	38.86 {0.132}	566.09 {1.926}
SPRDL	409.18 {1.392}	12.43 {0.042}	184.02 {0.625}	19.08 {0.065}	68.42 {0.233}	693.1 {2.358}

* Values in brackets indicate the corresponding percentage of the 29.4 kVA supplied to the load

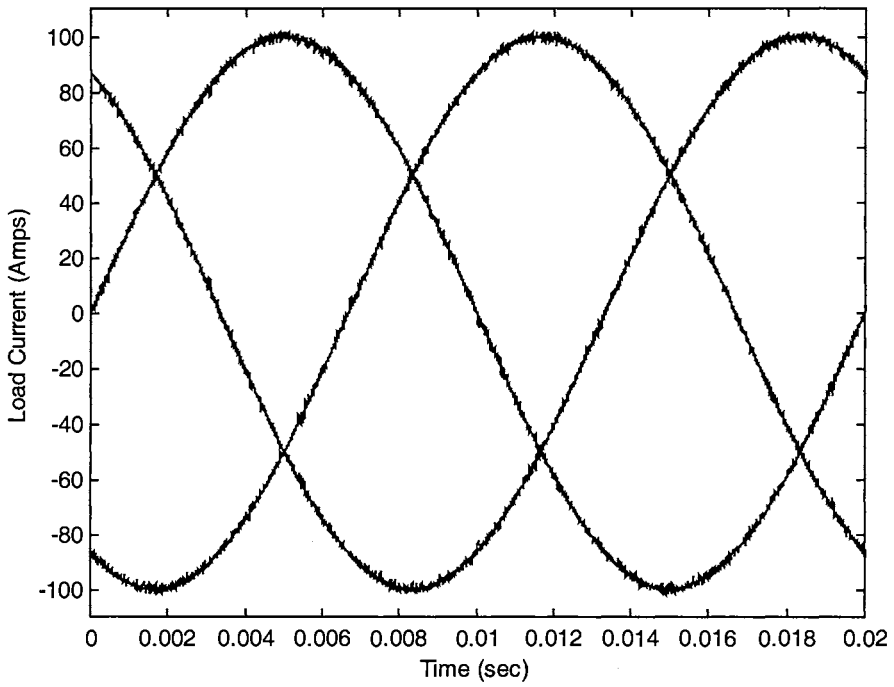


Figure 99. Load and reference currents for the PRAL inverter with PI current control driving the load at 50 Hz

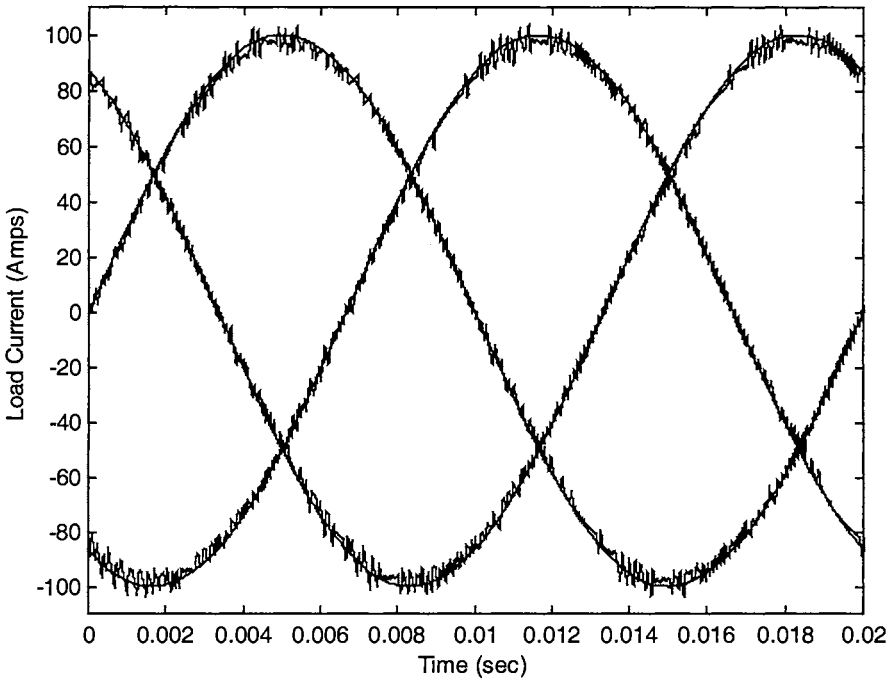


Figure 100. Load and reference currents for the SPRDL inverter driving the load at 50 Hz

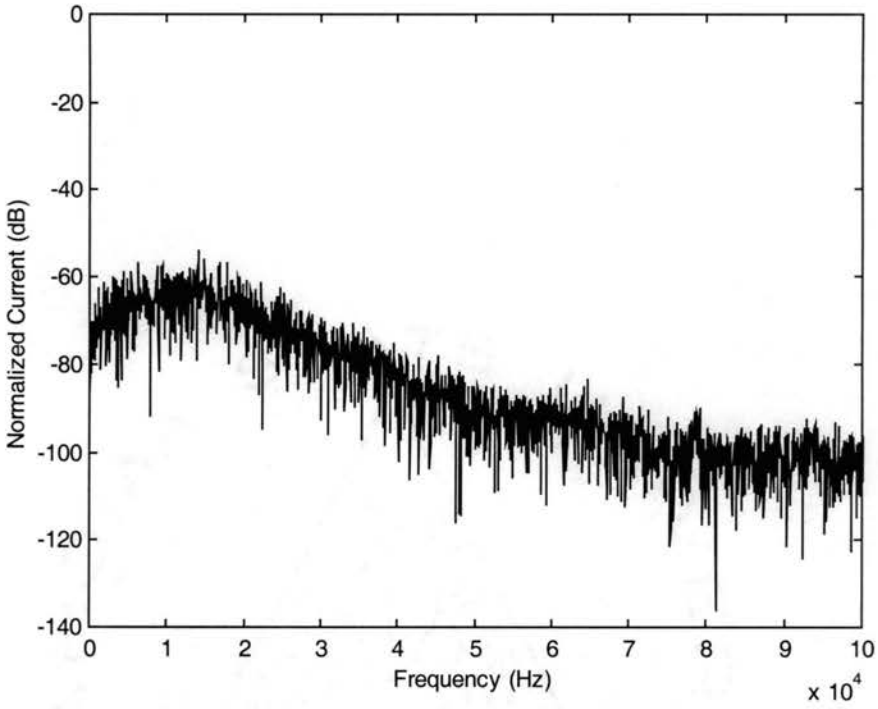


Figure 101. Normalized load current spectrum for the PRAL inverter driving the load at 50 Hz

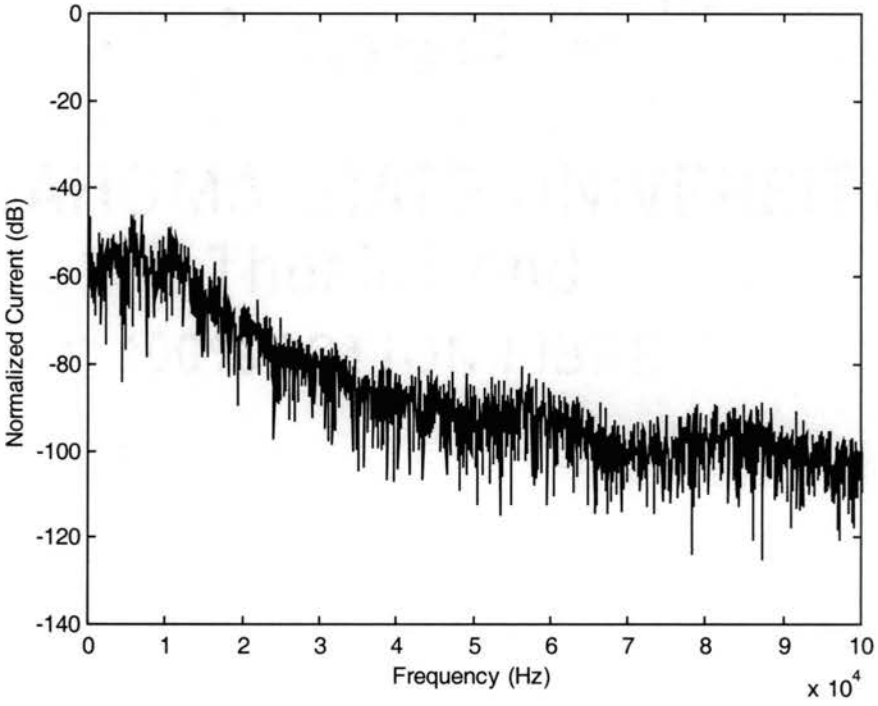


Figure 102. Normalized load current spectrum for the SPRDL inverter driving the load at 50 Hz

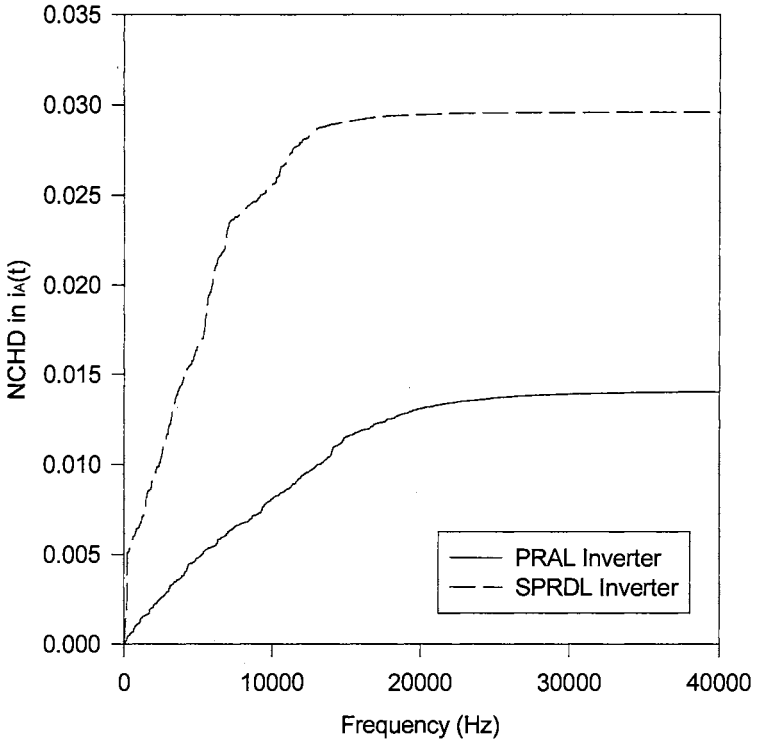


Figure 103. Normalized cumulative harmonic distortion in the Phase A load current produced by the PRAL inverter with PI current control and the SPRDL inverter driving the load at 50 Hz

TABLE XII

SUMMARY OF CONVERSION LOSSES FOR THE PRAL INVERTER WITH PI CURRENT CONTROL AND THE SPRDL INVERTER BOTH DRIVING THE LOAD AT 50 HZ

Inverter Type	Phase Leg Losses (Watts)		Resonant Circuit Losses (Watts)			Total Losses (Watts)
	Device Conduction	Device Switching	Device Conduction	Device Switching	Copper (R_R)	
PRAL	535.04 {1.820}	9.22 {0.031}	NA	NA	39.41 {0.134}	583.67 {1.985}
SPRDL	404.71 {1.377}	15.19 {0.052}	197.97 {0.673}	25.08 {0.085}	84.24 {0.287}	727.2 {2.473}

* Values in brackets indicate the corresponding percentage of the 29.4 kVA supplied to the load

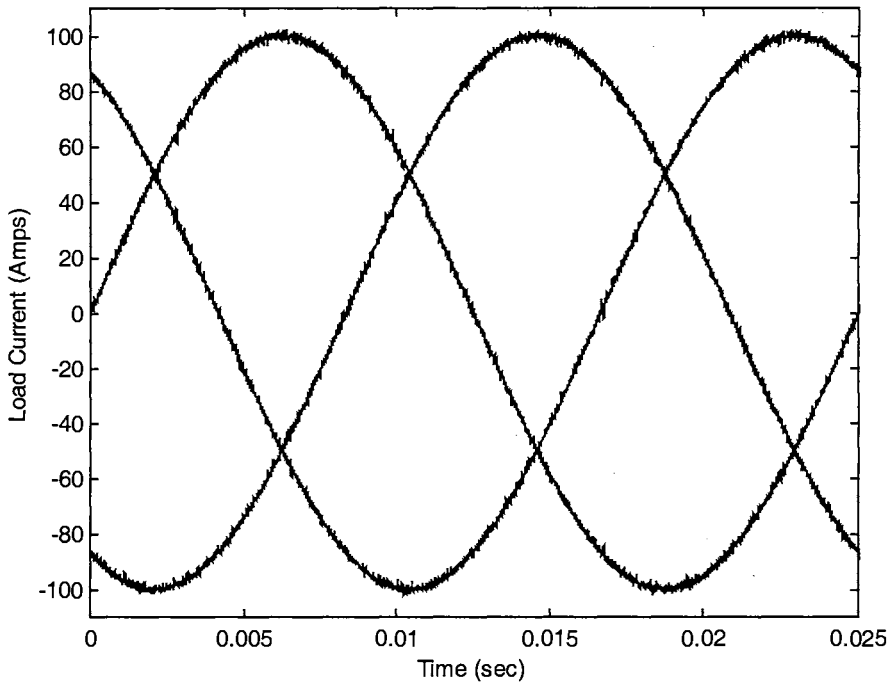


Figure 104. Load and reference currents for the PRAL inverter with PI current control driving the load at 40 Hz

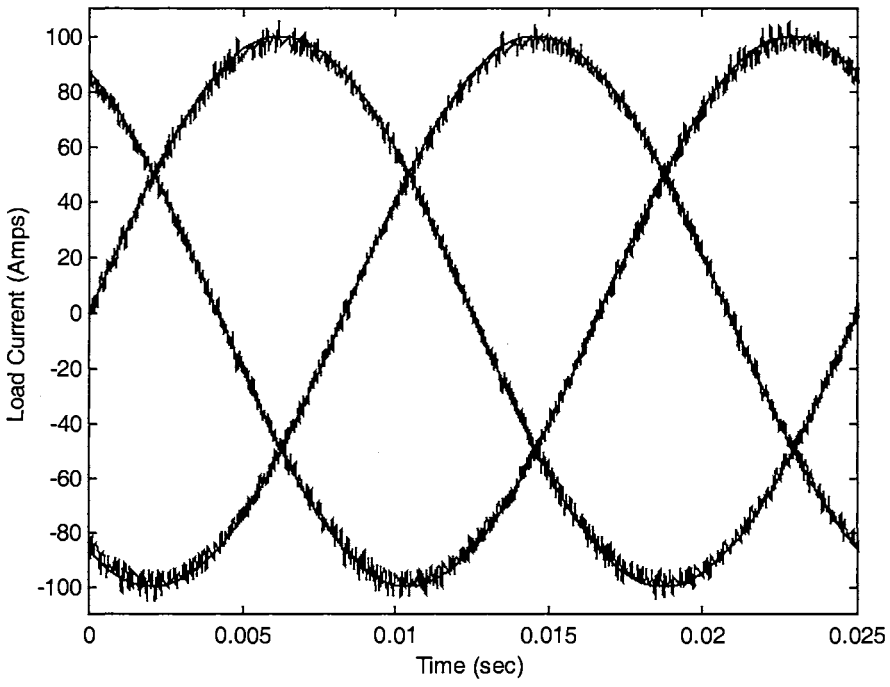


Figure 105. Load and reference currents for the SPRDL inverter driving the load at 40 Hz

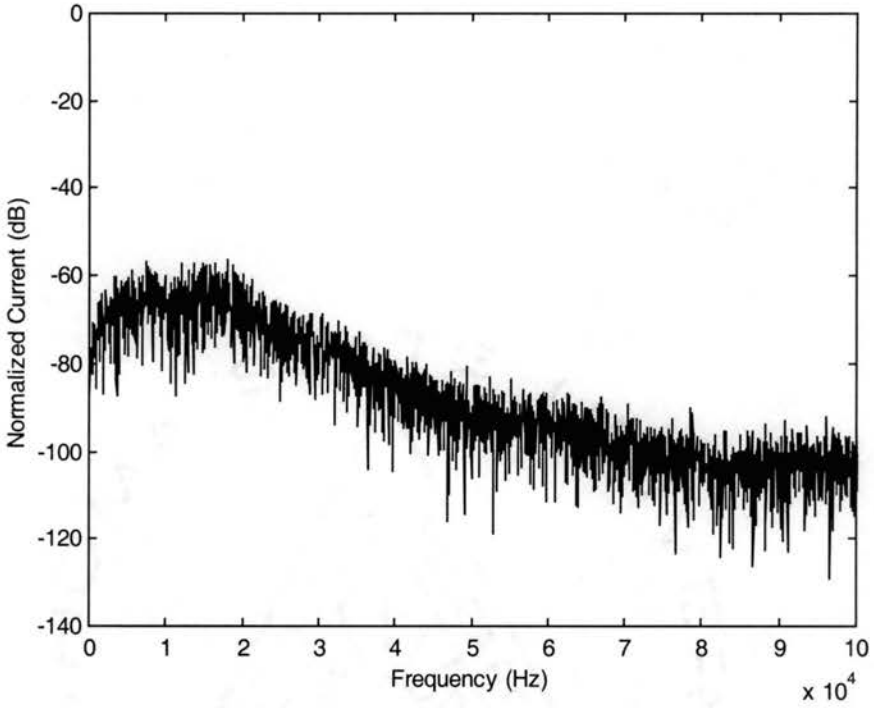


Figure 106. Normalized load current spectrum for the PRAL inverter driving the load at 40 Hz

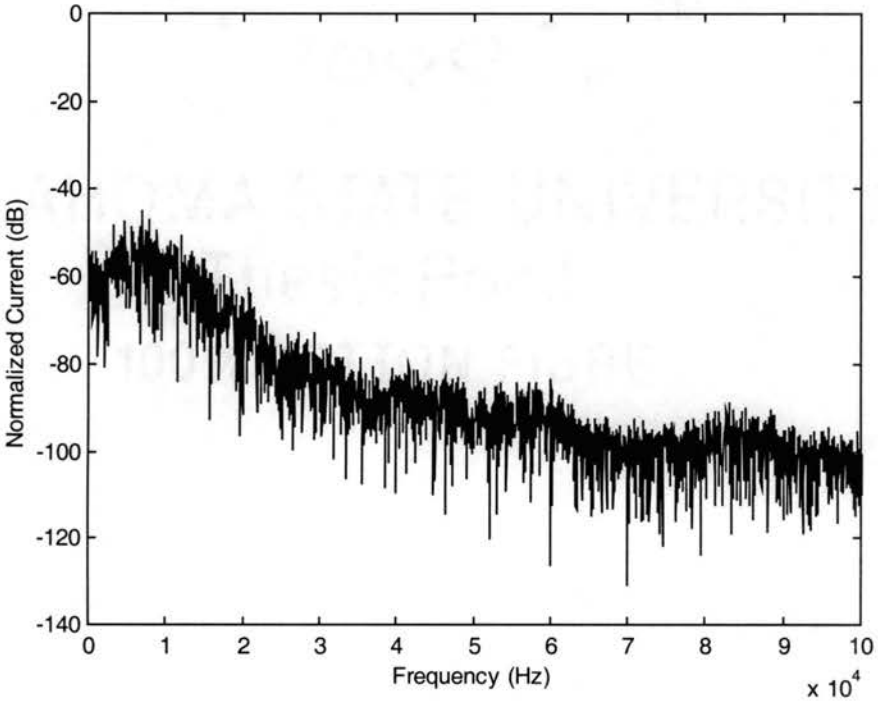


Figure 107. Normalized load current spectrum for the SPRDL inverter driving the load at 40 Hz

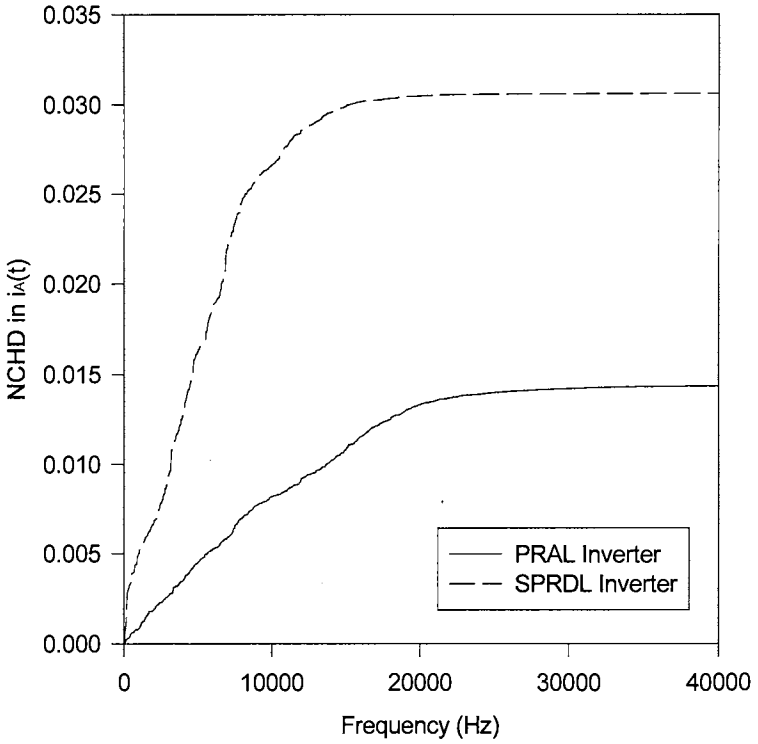


Figure 108. Normalized cumulative harmonic distortion in the Phase A load current produced by the PRAL inverter with PI current control and the SPRDL inverter driving the load at 40 Hz

TABLE XIII

SUMMARY OF CONVERSION LOSSES FOR THE PRAL INVERTER WITH PI CURRENT CONTROL AND THE SPRDL INVERTER BOTH DRIVING THE LOAD AT 40 HZ

Inverter Type	Phase Leg Losses (Watts)		Resonant Circuit Losses (Watts)			Total Losses (Watts)
	Device Conduction	Device Switching	Device Conduction	Device Switching	Copper (R_R)	
PRAL	537.25 {1.827}	9.64 {0.033}	NA	NA	40.00 {0.136}	586.88 {1.996}
SPRDL	400.09 {1.361}	16.07 {0.055}	209.96 {0.704}	27.23 {0.099}	87.96 {0.299}	738.3 {2.511}

* Values in brackets indicate the corresponding percentage of the 29.4 kVA supplied to the load

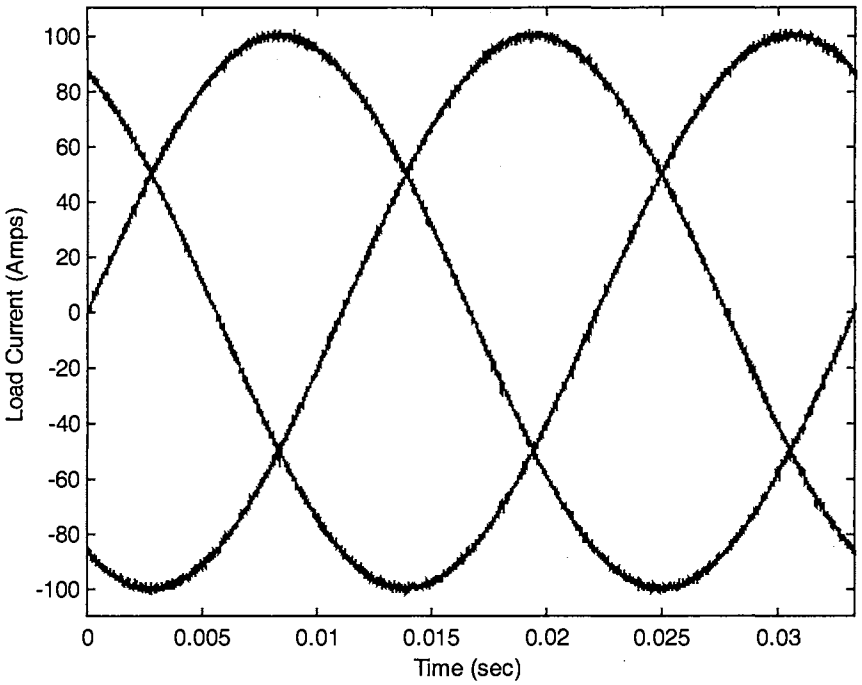


Figure 109. Load and reference currents for the PRAL inverter with PI current control driving the load at 30 Hz

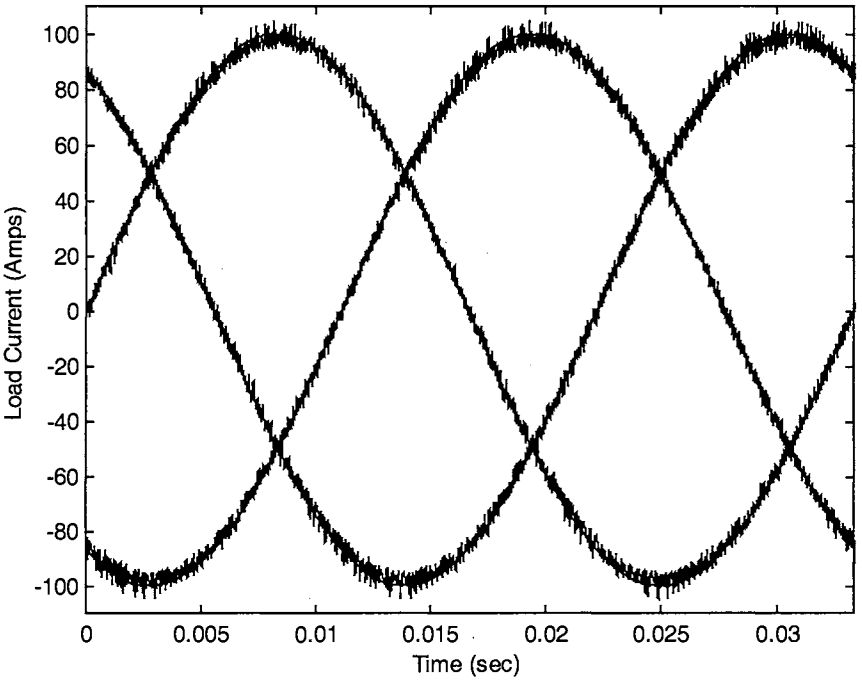


Figure 110. Load and reference currents for the SPRDL inverter driving the load at 30 Hz

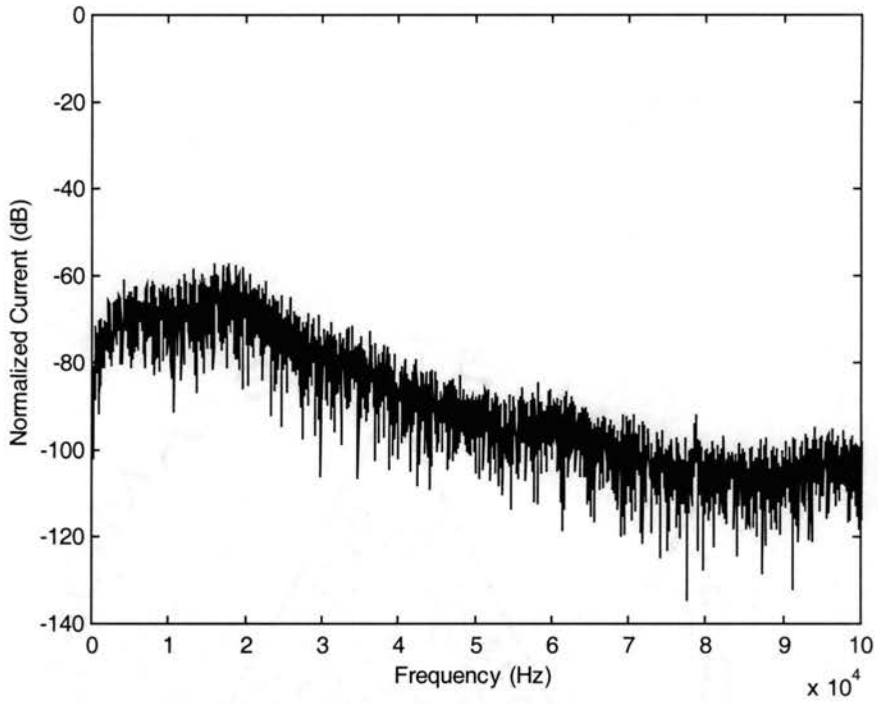


Figure 111. Normalized load current spectrum for the PRAL inverter driving the load at 30 Hz

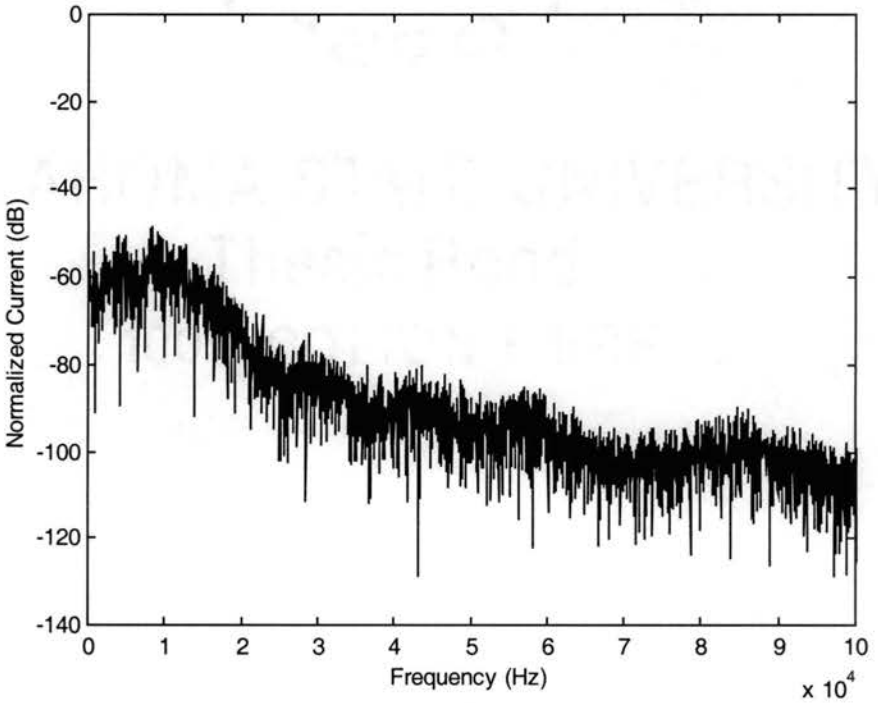


Figure 112. Normalized load current spectrum for the SPRDL inverter driving the load at 30 Hz

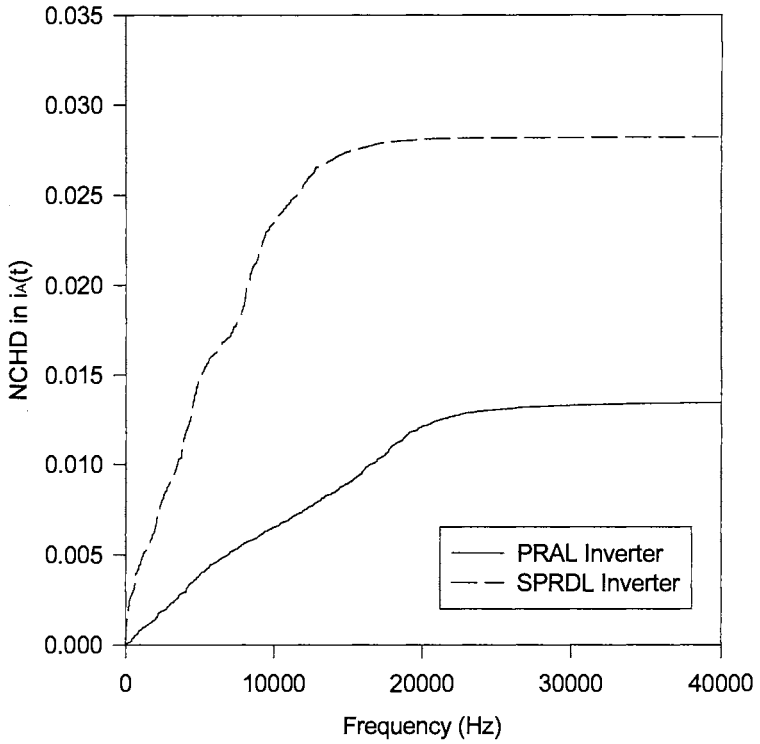


Figure 113. Normalized cumulative harmonic distortion in the Phase A load current produced by the PRAL inverter with PI current control and the SPRDL inverter driving the load at 30 Hz

TABLE XIV

SUMMARY OF CONVERSION LOSSES FOR THE PRAL INVERTER WITH PI CURRENT CONTROL AND THE SPRDL INVERTER BOTH DRIVING THE LOAD AT 30 HZ

Inverter Type	Phase Leg Losses (Watts)		Resonant Circuit Losses (Watts)			Total Losses (Watts)
	Device Conduction	Device Switching	Device Conduction	Device Switching	Copper (R_R)	
PRAL	541.54 {1.842}	9.44 {0.032}	NA	NA	40.11 {0.136}	591.09 {2.011}
SPRDL	395.19 {1.344}	17.59 {0.060}	213.59 {0.727}	30.46 {0.104}	97.17 {0.331}	754.0 {2.565}

* Values in brackets indicate the corresponding percentage of the 29.4 kVA supplied to the load

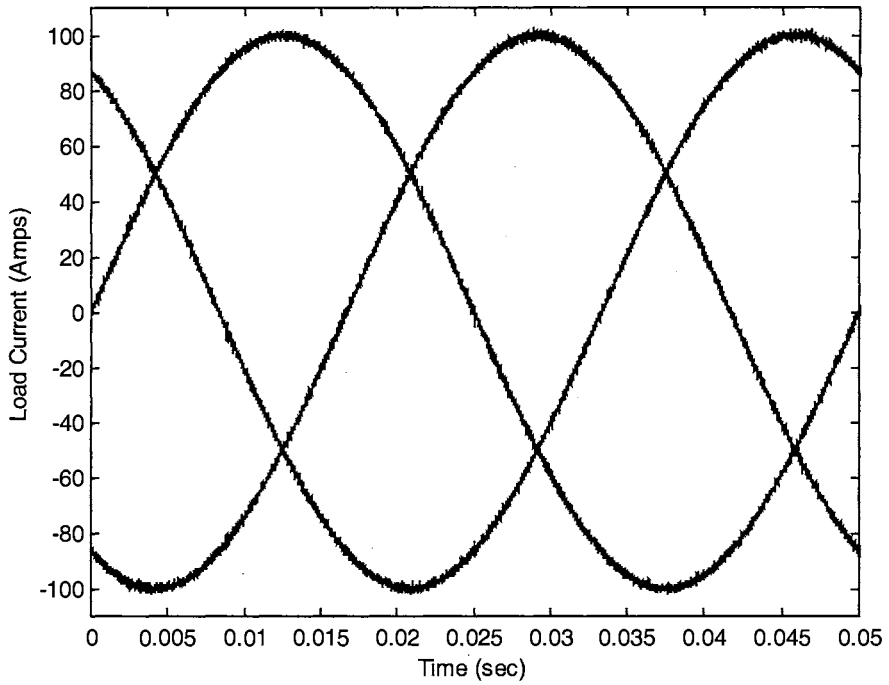


Figure 114. Load and reference currents for the PRAL inverter with PI current control driving the load at 20 Hz

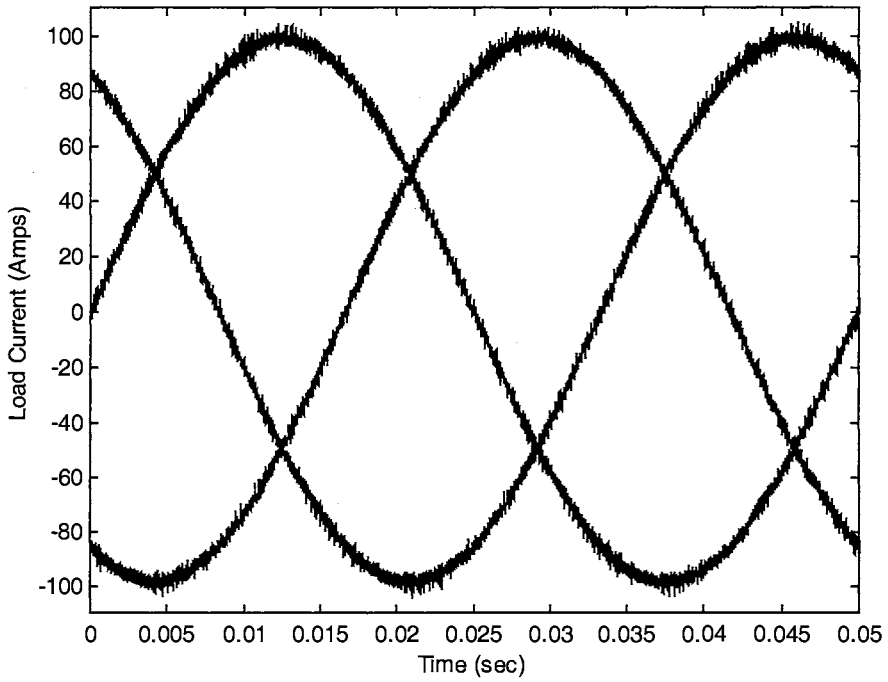


Figure 115. Load and reference currents for the SPRDL inverter driving the load at 20 Hz

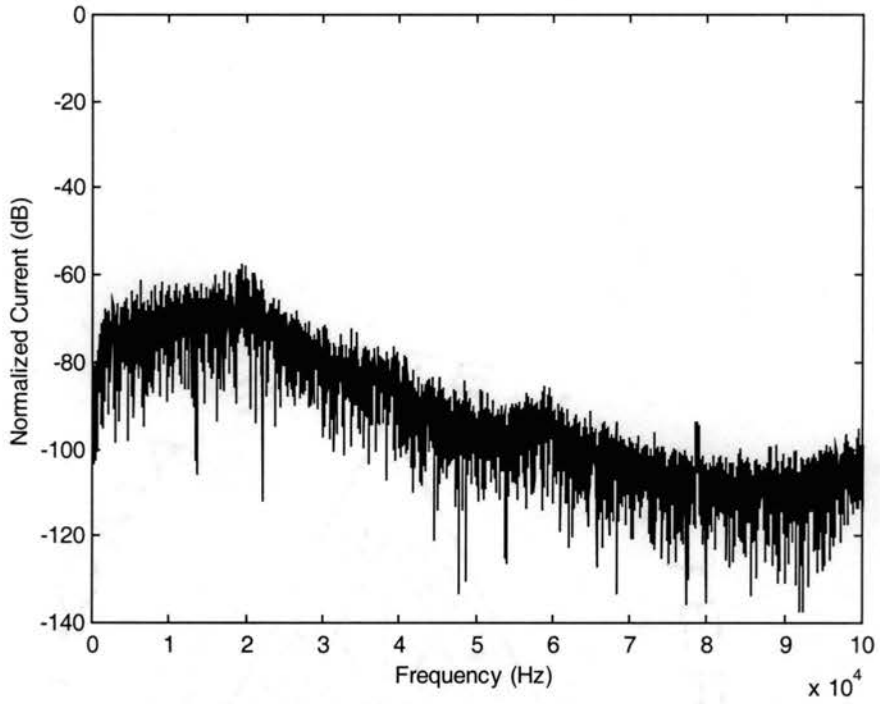


Figure 116. Normalized load current spectrum for the PRAL inverter driving the load at 20 Hz

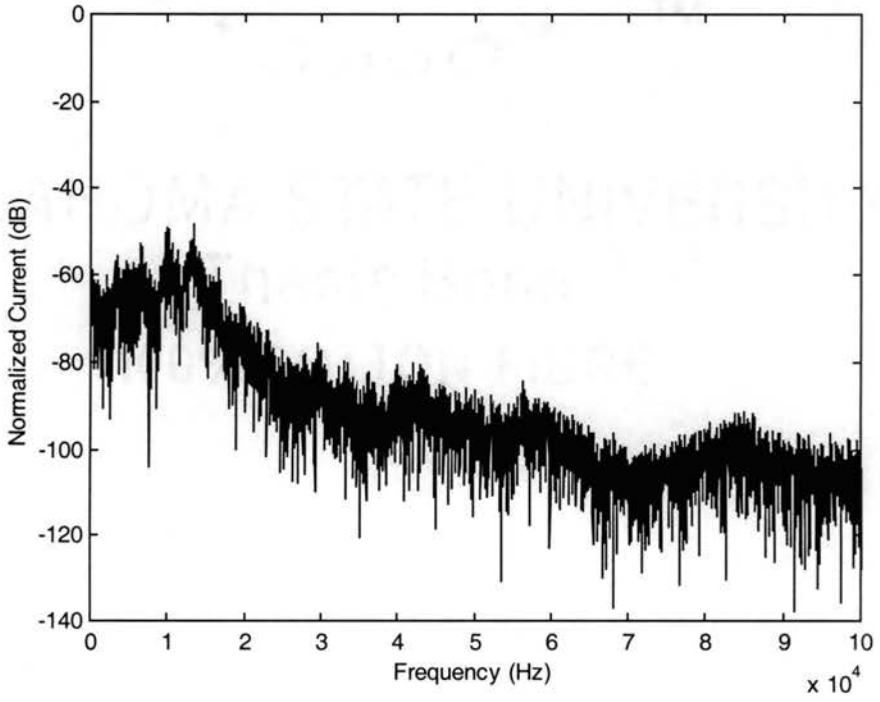


Figure 117. Normalized load current spectrum for the SPRDL inverter driving the load at 20 Hz

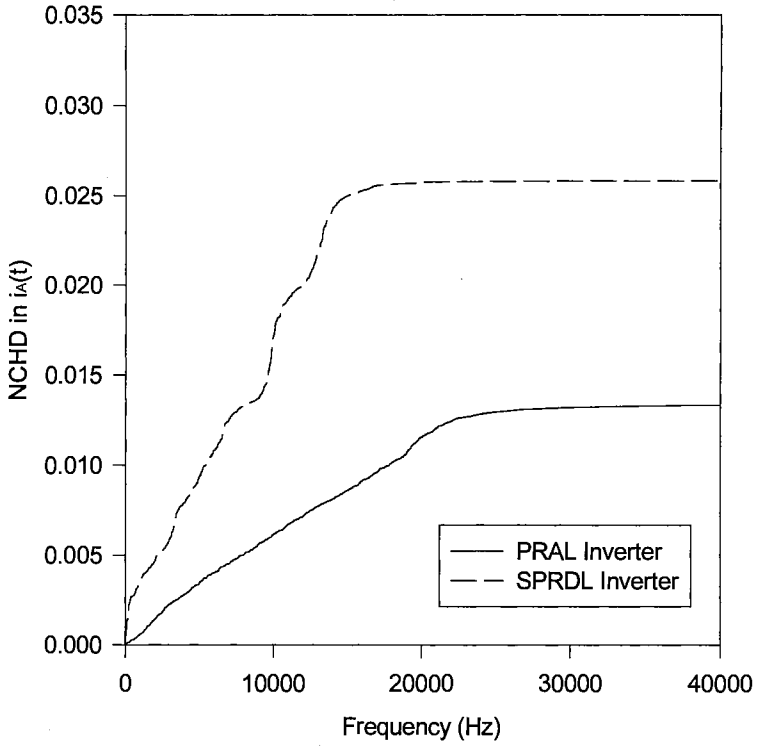


Figure 118. Normalized cumulative harmonic distortion in the Phase A load current produced by the PRAL inverter with PI current control and the SPRDL inverter driving the load at 20 Hz

TABLE XV

SUMMARY OF CONVERSION LOSSES FOR THE PRAL INVERTER WITH PI CURRENT CONTROL AND THE SPRDL INVERTER BOTH DRIVING THE LOAD AT 20 HZ

Inverter Type	Phase Leg Losses (Watts)		Resonant Circuit Losses (Watts)			Total Losses (Watts)
	Device Conduction	Device Switching	Device Conduction	Device Switching	Copper (R_R)	
PRAL	545.51 {1.855}	9.33 {0.032}	NA	NA	40.17 {0.137}	595.0 {2.024}
SPRDL	390.76 {1.329}	19.33 {0.066}	212.51 {0.723}	34.10 {0.116}	97.87 {0.333}	754.6 {2.566}

* Values in brackets indicate the corresponding percentage of the 29.4 kVA supplied to the load

Based on the preceding five data sets, the PRAL inverter offers significant advantages over the SPRDL inverter in terms of both output waveform quality and conversion efficiency. The Total Harmonic Distortion (THD) in the PRAL load current is at least 44.5% lower than for the SPRDL inverter in all five cases examined. The total switching device conduction and switching losses are at least 15.3% lower in the PRAL inverter than in the SPRDL inverter. Moreover, the estimated copper loss in the PRAL resonant circuit is at least 43% lower than the value estimated for the SPRDL inverter. However, the calculated copper losses in both inverters are most likely exaggerated due to the fact that R_R was computed at the 80 kHz free-running frequency of the resonant circuits. In fact, most of the spectral power content of the resonant circuit inductor current lies below 80 kHz for both inverters. This is particularly true for the SPRDL inverter since its average link frequency is substantially lower than the average frequency of the PRAL inverter's auxiliary link. Consequently, the estimates obtained for the resonant circuit copper losses in each inverter model must be used with care.

Figure 119 shows plots of the load current Total Harmonic Distortion (THD) obtained for each inverter. The distortion is most severe at 60 Hz for both inverters. For lower frequencies, the load current THD for the PRAL inverter ranges between about 1.4-1.5% and exhibits a slight decrease with decreasing inverter output frequency. The load current THD for the SPRDL inverter is nearly twice that of the PRAL inverter at all five output frequencies investigated.

The markedly higher load current TDH seen at 60 Hz is a result of voltage saturation hindering the ability of both inverters to synthesize output voltages near rated voltage, 240 Volts (RMS) in this case. Recall that V_S is only about 2% larger than the peak line-to-line voltage required at rated voltage. Normally, a larger margin would be selected, as was the case in [9] where the load voltage was significantly lower. However, the rated output voltage used in this exercise was deliberately selected to demonstrate the ability of the PRAL inverter to function reasonably well under near voltage saturation conditions.

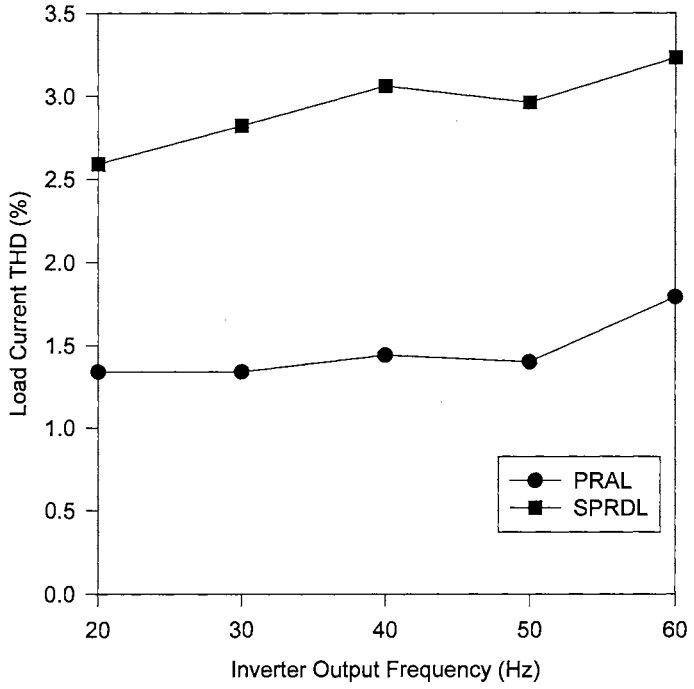


Figure 119. Load current THD for the PRAL and SPRDL inverters

Examination of the load current NCHD plots presented for each of the five output frequencies clearly shows that the magnitude of the first few harmonic components are substantially lower for the PRAL inverter than for the SPRDL inverter. This is particularly important in machine drive applications where the torque produced by low-order harmonic components of the load current can seriously damage mechanical equipment.

Figures 120 show plots of the combined device conduction losses for both inverters. Although the plots have a definitive pattern, the total deflection in each is insignificant compared to their respective magnitude. The most relevant aspect of this figure is that the total conduction losses for the SPRDL inverter are greater than for the PRDL inverter, despite the use of the "low end" bilateral switch configuration with its 5.4V forward voltage drop. Secondly, the same forward voltage drops were used in both the PRAL and SPRDL inverter simulation models. It is well known that the forward voltage drop across self-extinguishing devices and diodes increases with reverse voltage rating. The switching devices in the SPRDL inverter must withstand voltage

stress levels at least 50% greater than the switching devices in the PRAL inverter. Thus, the device forward voltage drops for the SPRDL inverter will realistically exceed those of the PRAL inverter. Consequently, the device conduction loss aspects of the PRAL inverter should compare even more favorably to the SPRDL inverter in practice.

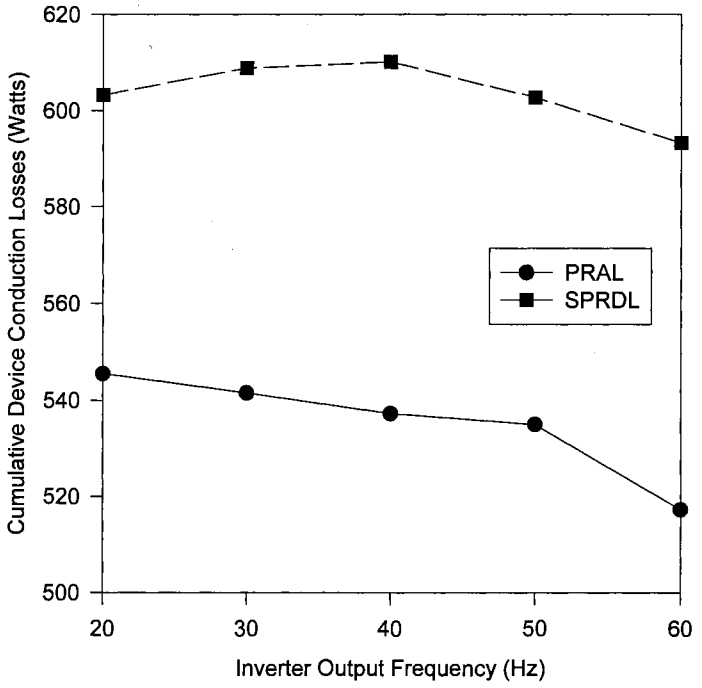


Figure 120. Cumulative device conduction losses in the PRAL and SPRDL inverters

Figure 121 shows plots of the cumulative device switching losses obtained for both inverters. The switching losses in both inverters are effectively negligible compared to hard-switched designs in which switching losses are often comparable to conduction losses. However, the switching losses in the PRAL inverter are essentially constant with respect to output frequency and are 3-5 times lower than the SPRDL inverter switching losses.

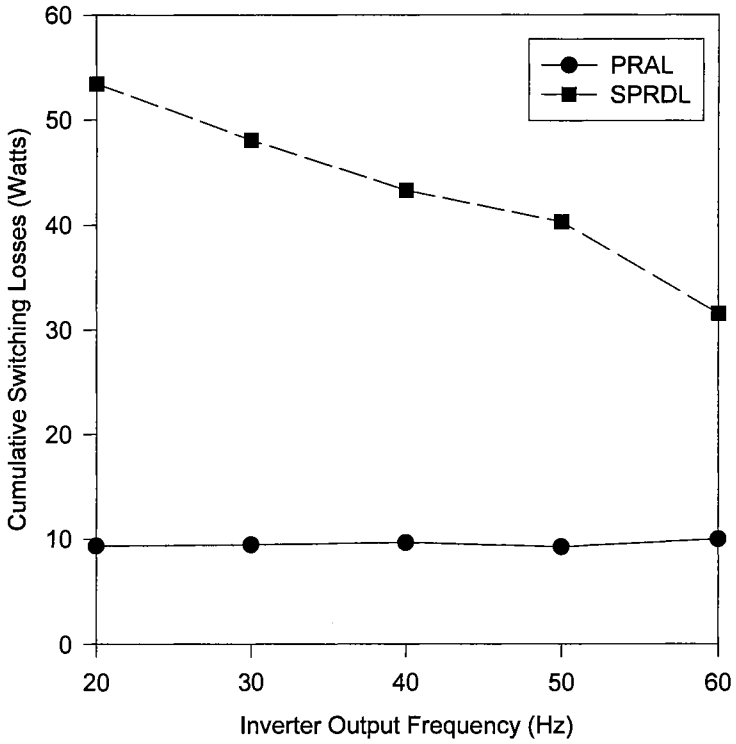


Figure 121. Cumulative device switching losses in the PRAL and SPRDL inverters

Figures 122 and 123 show plots of the total conversion losses and the overall conversion efficiency, respectively, obtained for the PRAL and SPRDL inverters. The total conversion loss plots include the conduction and switching losses associated with each device in the respective inverter along with the estimated copper losses in the resonant circuit inductor. The overall conversion efficiency plots are based on the total conversion losses and are referenced to the 24.3 kW of real power delivered to the load.

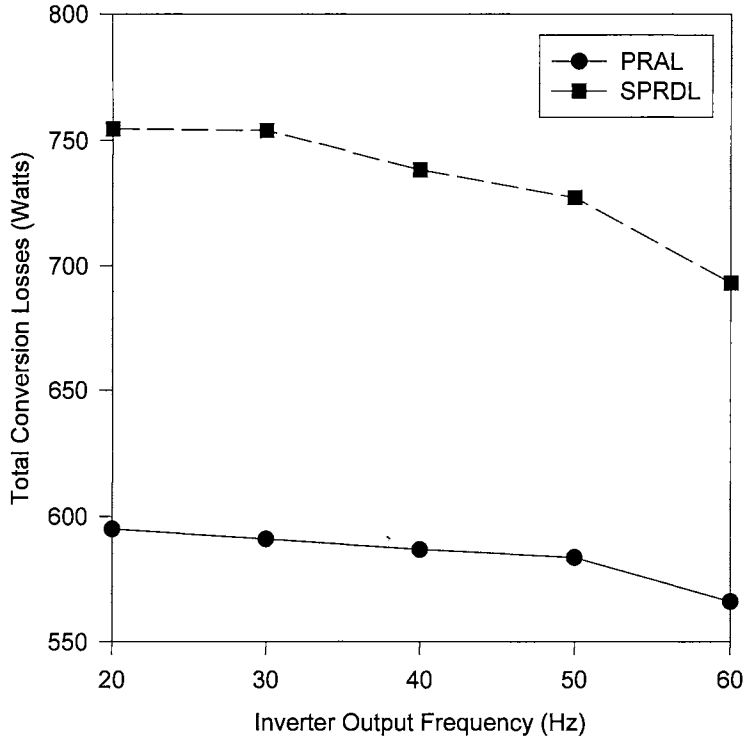


Figure 122. Total inverter conversion losses for the PRAL and SPRDL inverters

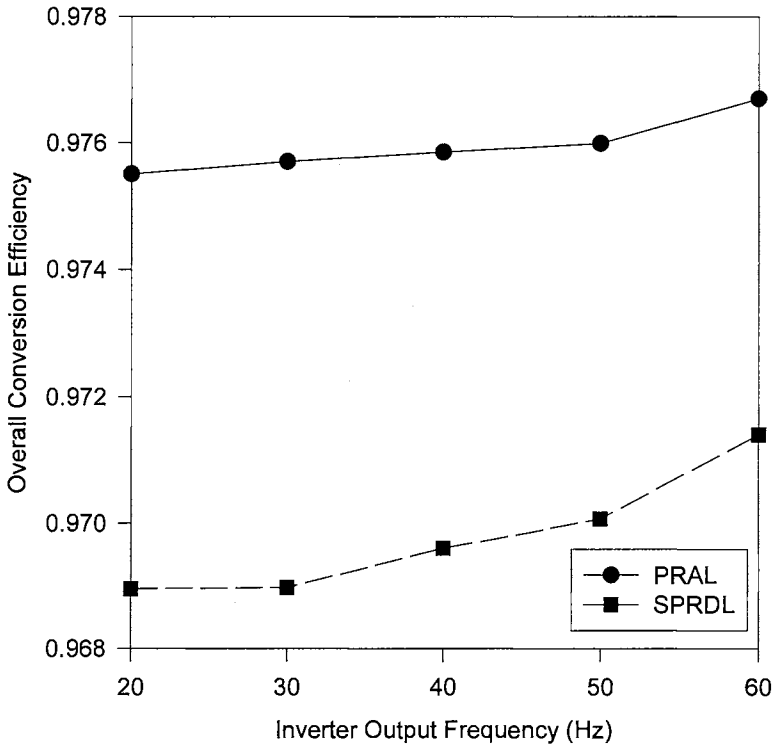


Figure 123. Overall conversion efficiency of the PRAL and SPRDL inverters, based on the 24.3 kW of real power supplied to the load

8.8 Cost-Function Load Current Control

This section examines the merits of the cost-function based load current control strategy described in Chapter VI. The PRAL inverter model used in this section is identical to that used in the previous section with the exception of the "Load Error" and "Next State" blocks shown in Figure 79. Expanded views of these blocks are provided in Appendix B. Simulation experiments were conducted at inverter output frequencies of 60 Hz, 40 Hz, and 20 Hz for this configuration. The results of each simulation trial are presented below along with relevant results from the preceding section that aid in comparing the cost-function approach to the traditional PI current control method.

Inspection of the load current plots shows that the cost-function control method yields substantially smoother current waveforms than were obtained using PI current control. Moreover, examination of the load current spectrum plots reveals that the "hump" that occurred near 10 kHz for the PI controlled PRAL inverter is essentially absent in the spectrum of the cost-function controlled PRAL inverter. Additionally, all three load current NCHD plots show that the cost-function control method is substantially superior to the PI control method in attenuating low-order harmonic current components, especially at lower inverter output frequencies. The cost-function approach reduces the THD in the load current by at least 33% compared to the PI controlled PRAL inverter and by at least 57% compared to the SPRDL inverter for all three inverter output frequencies. The most significant improvement is seen for the 20 Hz case in which the load current THD is less than approximately 0.65%. Unfortunately, these improvements come at the cost of real-time load back EMF estimates. If only rough estimates are available or the available estimates contain substantial noise, the potential advantages of this approach will be correspondingly eroded.

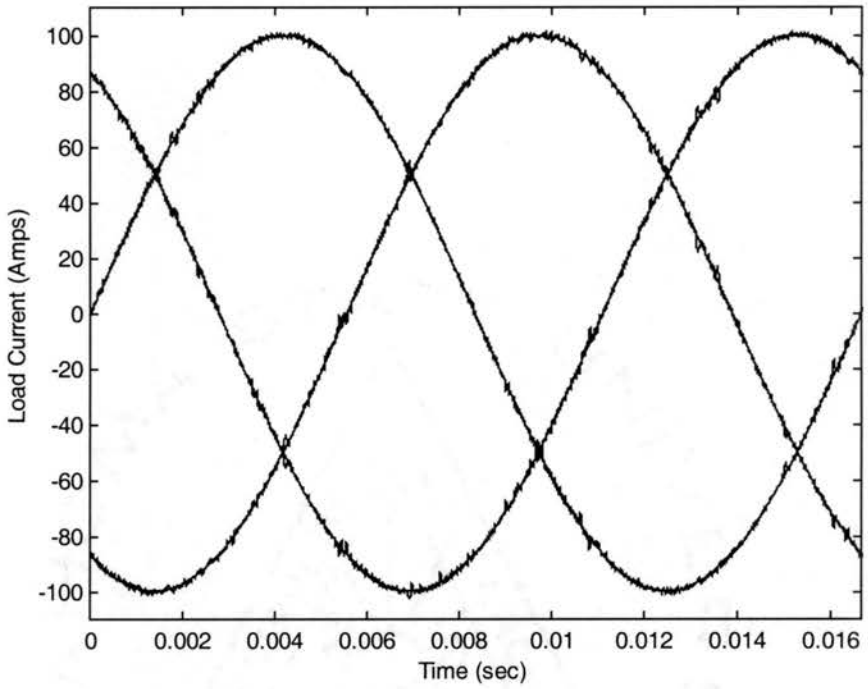


Figure 124. Load and reference currents for the PRAL inverter with cost-function current control driving the load at 60 Hz

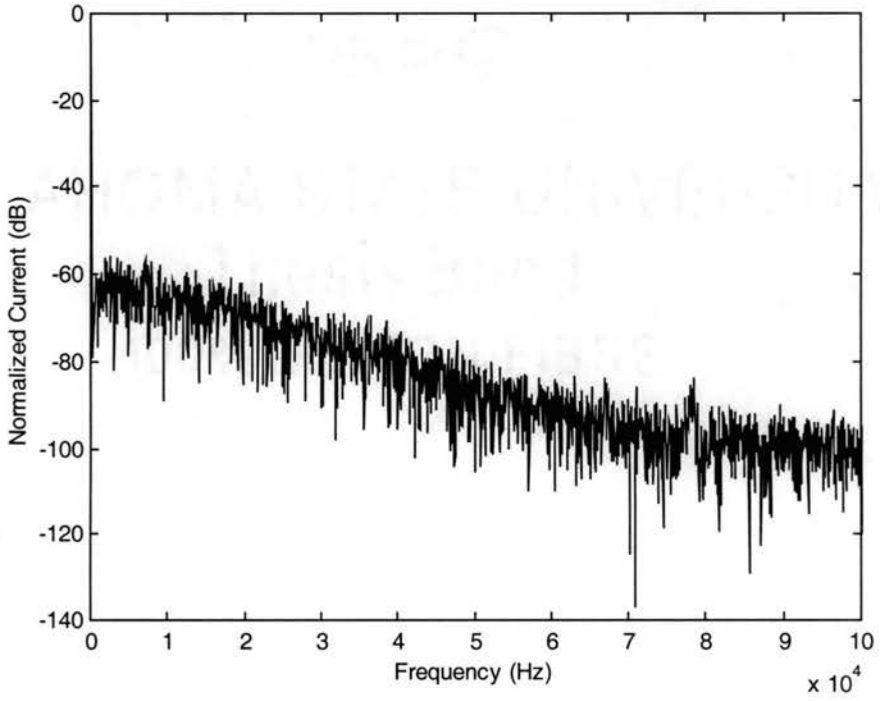


Figure 125. Normalized load current spectrum for the PRAL inverter with cost-function current control driving the load at 60 Hz

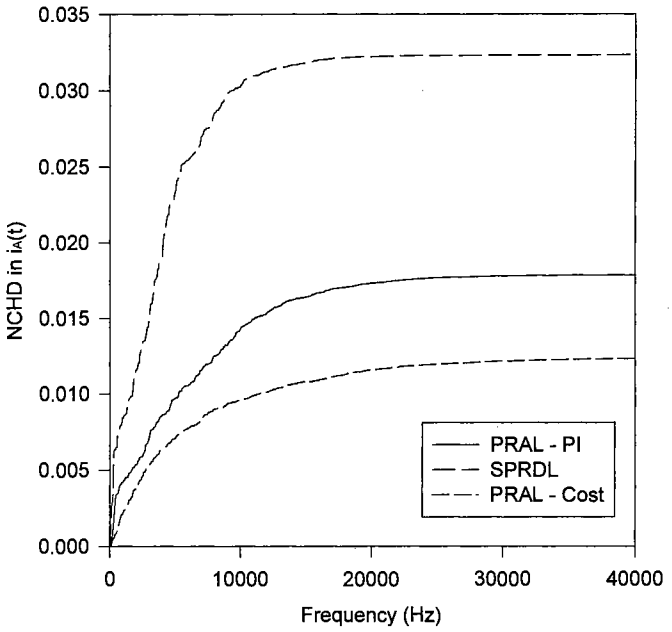


Figure 126. Normalized cumulative harmonic distortion in the Phase A load current produced by the PRAL inverter with PI current control, the PRAL inverter with cost-function current control, and the SPRDL inverter driving the load at 60 Hz

TABLE XVI

SUMMARY OF CONVERSION LOSSES FOR THE PRAL INVERTER WITH PI CURRENT CONTROL, THE PRAL INVERTER WITH COST-FUNCTION CURENT CONTROL, AND THE SPRDL INVERTER ALL DRIVING THE LOAD AT 60 HZ

Inverter Type	Phase Leg Losses (Watts)		Resonant Circuit Losses (Watts)			Total Losses (Watts)
	Device Conduction	Device Switching	Device Conduction	Device Switching	Copper (R_R)	
PRAL (PI)	517.27 {1.759}	9.97 {0.034}	NA	NA	38.86 {0.132}	566.09 {1.926}
PRAL (Cost)	581.70 {1.978}	11.94 {0.041}	NA	NA	40.00 {0.139}	634.60 {2.158}
SPRDL	409.18 {1.392}	12.43 {0.042}	184.02 {0.625}	19.08 {0.065}	68.42 {0.233}	693.1 {2.358}

* Values in brackets indicate the corresponding percentage of the 29.4 kVA supplied to the load

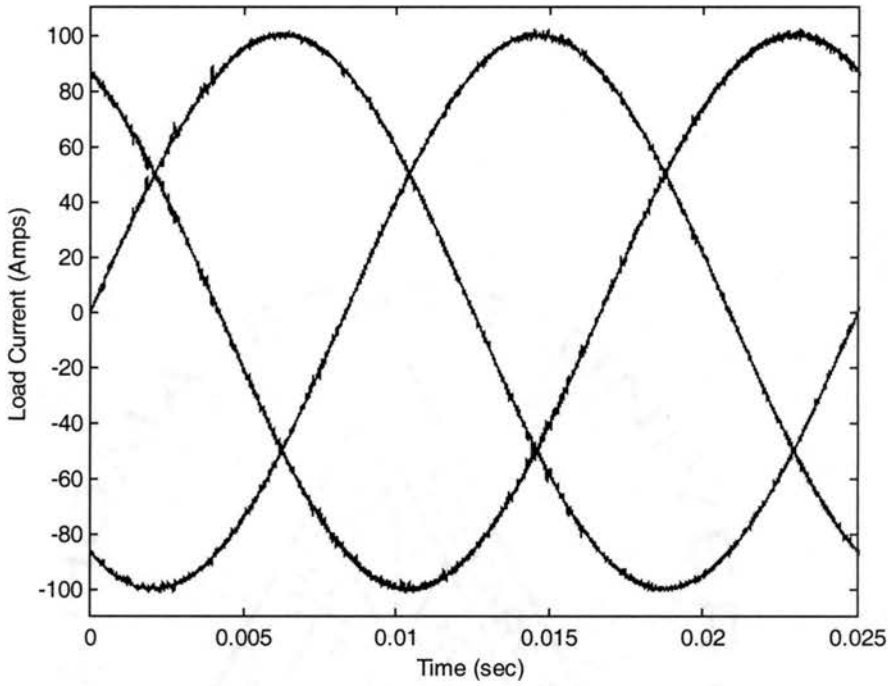


Figure 127. Load and reference currents for the PRAL inverter with cost-function current control driving the load at 40 Hz

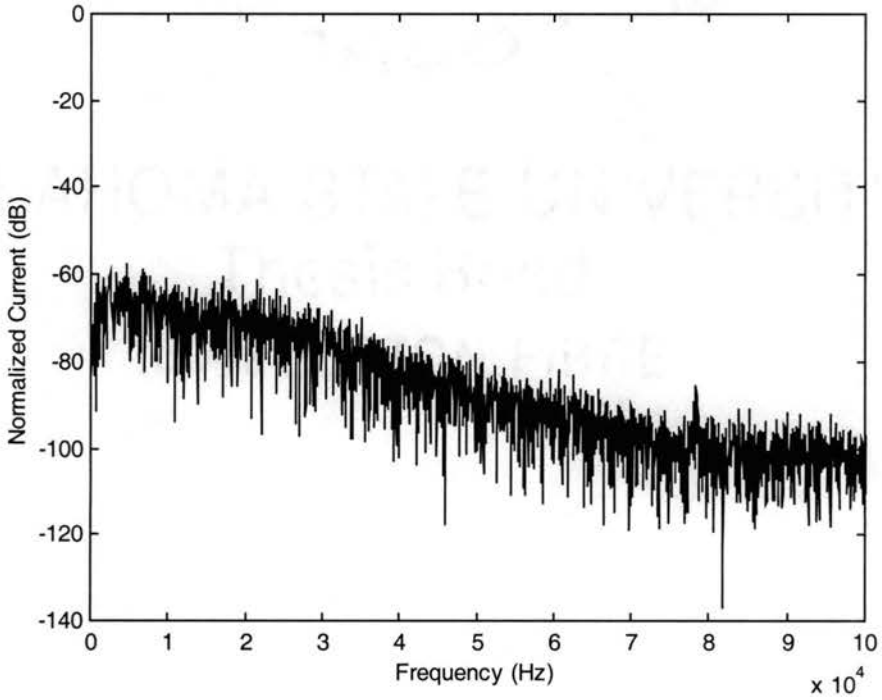


Figure 128. Normalized load current spectrum for the PRAL inverter with cost-function current control driving the load at 40 Hz

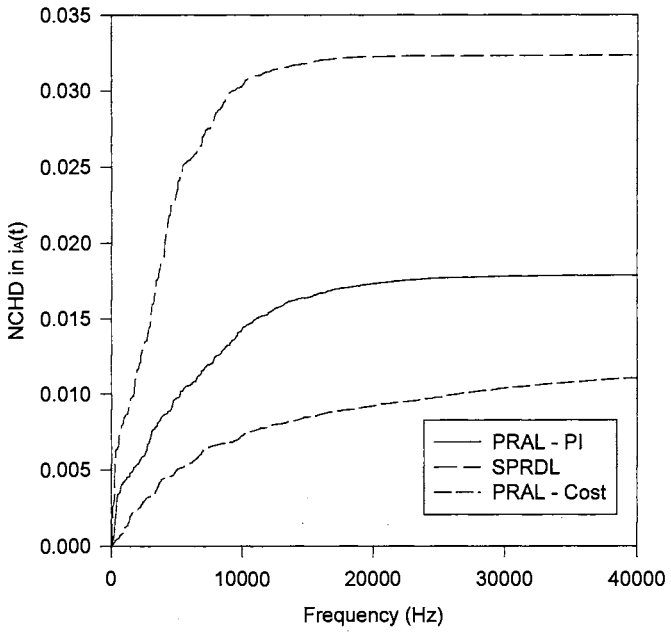


Figure 129. Normalized cumulative harmonic distortion in the Phase A load current produced by the PRAL inverter with PI current control, the PRAL inverter with cost-function current control, and the SPRDL inverter driving the load at 40 Hz

TABLE XVII

SUMMARY OF CONVERSION LOSSES FOR THE PRAL INVERTER WITH PI CURRENT CONTROL, THE PRAL INVERTER WITH COST-FUNCTION CURENT CONTROL, AND THE SPRDL INVERTER ALL DRIVING THE LOAD AT 40 HZ

Inverter Type	Phase Leg Losses (Watts)		Resonant Circuit Losses (Watts)			Total Losses (Watts)
	Device Conduction	Device Switching	Device Conduction	Device Switching	Copper (R_R)	
PRAL (PI)	537.25 {1.827}	9.64 {0.033}	NA	NA	40.00 {0.136}	586.88 {1.996}
PRAL (Cost)	599.09 {2.038}	12.03 {0.041}	NA	NA	42.01 {0.143}	653.09 {2.221}
SPRDL	400.09 {1.361}	16.07 {0.055}	209.96 {0.704}	27.23 {0.099}	87.96 {0.299}	738.3 {2.511}

* Values in brackets indicate the corresponding percentage of the 29.4 kVA supplied to the load

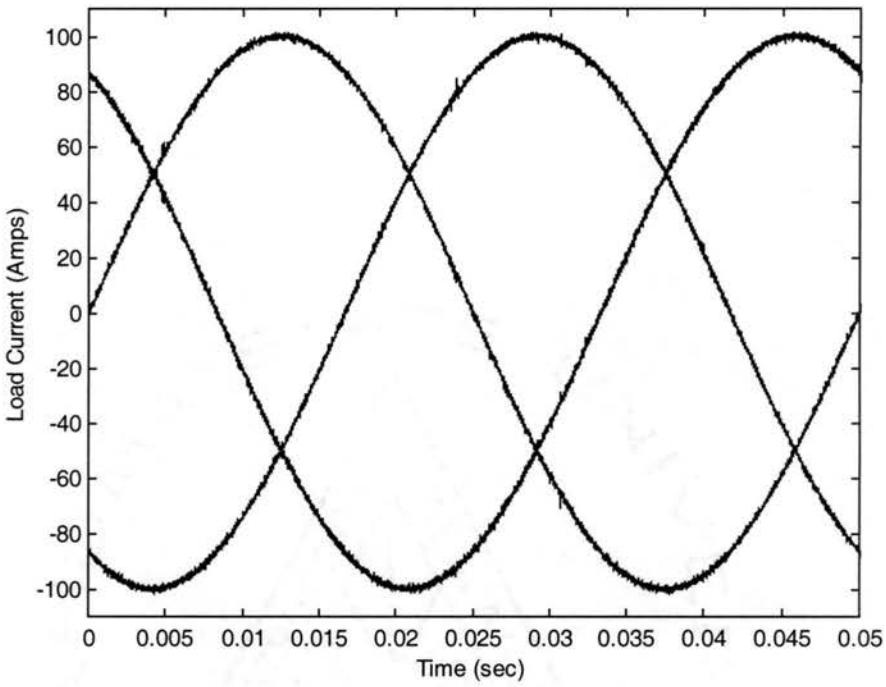


Figure 130. Load and reference currents for the PRAL inverter with cost-function current control driving the load at 20 Hz

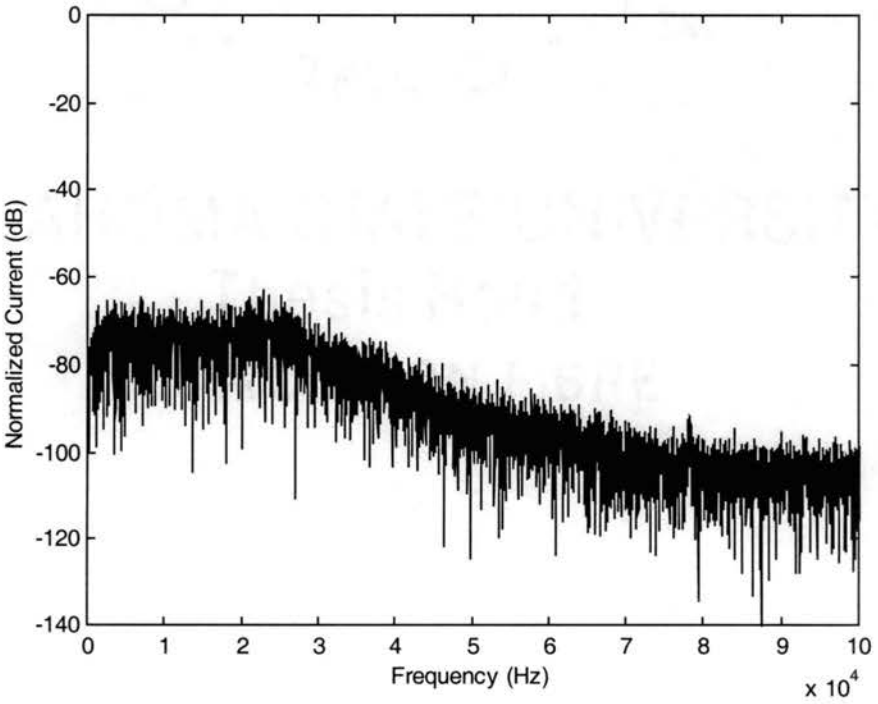


Figure 131. Normalized load current spectrum for the PRAL inverter with cost-function current control driving the load at 20 Hz

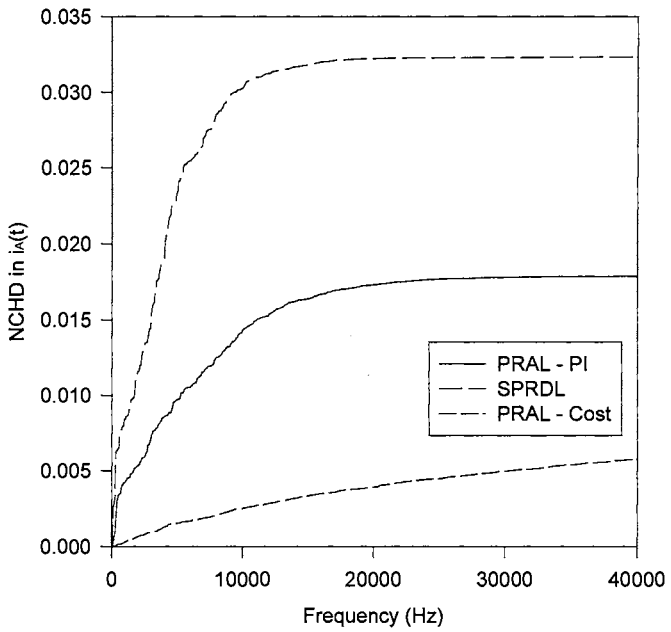


Figure 132. Normalized cumulative harmonic distortion in the Phase A load current produced by the PRAL inverter with PI current control, the PRAL inverter with cost-function current control, and the SPRDL inverter driving the load at 20 Hz

TABLE XVIII

SUMMARY OF CONVERSION LOSSES FOR THE PRAL INVERTER WITH PI CURRENT CONTROL, THE PRAL INVERTER WITH COST-FUNCTION CURENT CONTROL, AND THE SPRDL INVERTER ALL DRIVING THE LOAD AT 20 HZ

Inverter Type	Phase Leg Losses (Watts)		Resonant Circuit Losses (Watts)			Total Losses (Watts)
	Device Conduction	Device Switching	Device Conduction	Device Switching	Copper (R_R)	
PRAL (PI)	545.51 {1.855}	9.33 {0.032}	NA	NA	40.17 {0.137}	595.0 {2.024}
PRAL (Cost)	604.28 {2.055}	12.06 {0.041}	NA	NA	42.41 {0.144}	658.75 {2.241}
SPRDL	390.76 {1.329}	19.33 {0.066}	212.51 {0.723}	34.10 {0.116}	97.87 {0.333}	754.6 {2.566}

* Values in brackets indicate the corresponding percentage of the 29.4 kVA supplied to the load

8.9 Summary

This section demonstrated the performance characteristics of the PRAL inverter within the context of performing a simulation-based comparison with a premiere SPRDL design. The models were constructed using a popular graphically-oriented modeling and simulation suite. A PRAL inverter was specifically designed for comparison with a three-phase version of the SPRDL inverter described in [9]. The associated PRAL inverter model was used to demonstrate the viability of the strategies proposed in Chapter VI for calculating the required boost current and regulating the voltage divider potential. Both strategies proved suitable and it was shown that relatively small capacitors, 500 μF, could be used in the voltage divider circuit without adversely impacting operational viability or conversion efficiency.

Comparisons were conducted between the PRAL and SPRDL inverters at various output frequencies in order to evaluate the performance of both topologies synthesizing a variety of circular voltage trajectories **H**. In all cases, the PRAL inverter outperformed the SPRDL in terms output waveform quality and conversion losses. Most importantly however, the voltage stress placed on the PRAL switching devices never exceeded 400V, which was the voltage of the DC source feeding both inverters. This is in marked contrast to the SPRDL inverter, which demonstrated device voltage stress levels above 600V, as was shown in Figure 90. Finally, the load back EMF based cost-function control strategy proposed for the PRAL inverter in Chapter VI was evaluated and produced substantial improvements in output waveform quality compared to the more simplistic PI control approach.

CHAPTER IX

THESIS SUMMARY AND CONCLUDING REMARKS

9.1 Thesis Summary

The objective of this thesis was to extend the soft-switched inverter technology base to include a topology class devoid of the high voltage stress levels presently associated with soft-switched inverter topologies. Soft switching is an elegant approach to suppressing the high thermal power levels that can occur inside an inverter's switching devices when they transition between the conducting and blocking states. Switching losses limit the switching frequency of conventional hard-switched and snubber protected inverter designs to approximately 3-5 kHz and 5-10 kHz, respectively, due to practical limitations on the average thermal power that can be extracted from a given switching device. By effectively eliminating switching losses, soft-switched topologies provide the first practical avenue to realizing high-power inverter systems with average switching frequencies significantly above 10 kHz.

Soft-switched inverter topologies are structured and controlled so that switching devices are always turned on and off while the inverter holds either their terminal voltage or current near zero, effectively preempting generation of switching energy. This innate property of soft-switched topologies distinguishes them from conventional hard-switched and snubber protected designs and has resulted in experimental prototypes with power ratings of more than 50 kVA operating at switching frequencies above 120 kHz.

Since the middle 1980s when the first successful high-power soft-switched inverter was introduced [6], two principal objectives have dominated the research effort that followed. The

first of these has been a quest to reduce device voltage stress to a level comparable to that of a conventional bridge inverter. The second objective has been to precisely control the time at which power matrix state transitions occur in an effort to improve output waveform quality. The first objective has been partially achieved. Practical designs have been reported in the literature with voltage stress levels approximately 1.5 times that of comparable conventional bridge inverters. This constitutes an improvement of nearly a factor of two over the original UPRDL inverter reported in [6], which suffered from a voltage stress level 2.5-3 times that of a conventional bridge design. The second objective was achieved in the late 1980s. Unfortunately, the ability to control the time at which state transitions occur did not yield the anticipated waveform quality improvements envisioned for three-phase applications. This was due, at least in part, to the substantial time required to reset the link collapse circuit following a link collapse event. Ironically, the lengthy reset time, which is typically greater than two free-running resonant circuit periods, is a direct consequence of mechanisms employed to limit voltage stress to practical levels.

The inspiration for this thesis resulted from the observation that all soft-switched inverter research reported in the literature has been directed toward resonant link topologies. This suggested that non-resonant link soft-switched topologies, if they exist, have not been investigated. The fundamental premise underlying this work is that resonant link topologies, which in the present literature are synonymous with soft-switched inverters, constitute a distinct topological class of soft-switched inverters rather than the entirety of all soft-switched inverter topologies. A corollary to this supposition is that one or more undesirable attributes of resonant link topologies, such as high voltage stress, may be absent in certain non-resonant link soft-switched inverter classes.

Unfortunately, analytical techniques for describing the performance characteristics of resonant link designs are effectively nonexistent in the literature. Consequently, no obvious preexisting starting point from which to initiate a search for viable non-resonant link topologies was available

at the outset of this effort. This void precipitated formulation of the concepts and definitions introduced in Chapter III that delineate the search for the consummate soft-switched inverter pursued in Chapter IV and constitute the beginning of the original work presented in this thesis.

The premise behind Chapter III is that the trajectories a given inverter's output voltage is capable of traversing in voltage space constitute a "fingerprint" that uniquely maps the inverter into a unique topological class. For example, the voltage space trajectories of all resonant link inverters form a distinct and finite set of line segments in voltage space. In contrast, the voltage space trajectories of a conventional bridge inverter form an infinite continuum that completely covers a specific region of voltage space. Moreover, each topological class possess certain performance attributes, such as power matrix voltage stress, that are a direct result of the particular "fingerprint" their member inverters form in voltage space.

Analytical techniques were developed in Chapter III to express two important performance metrics of a given topological class in terms of the output voltage trajectories forming its "fingerprint" in voltage space. The first of these was the voltage stress placed on a member inverter's power matrix switching devices. The second was the spanning cycle frequency. The spanning cycle frequency constitutes a lower frequency bound on the waveform distortion associated with an inverter synthesizing a fixed voltage vector in voltage space. Although this metric lacks information about the strength and distribution of the distortion energy above the frequency bound, it has merit as a means of comparing different topological classes in terms of low frequency distortion. This is of particular value in machine drive applications where low frequency distortion components can seriously damage driven mechanical equipment. Finally, the concepts and analytical techniques developed in the chapter were applied to the SPRDL inverter.

Chapter IV employed the voltage space concepts developed in Chapter III to synthesize the voltage space characteristics of a "hypothetical" soft-switched inverter topology with the same power matrix voltage stress as a conventional bridge inverter. The principal difference between the resulting hypothetical inverter and resonant link topologies is that the hypothetical inverter's

allowed voltage space trajectories include direct paths between adjacent active state voltages while those of resonant link topologies do not. The addition of these trajectories was shown to have the added benefit of increasing the lower frequency bound on the output voltage distortion by as much as a factor of two in certain regions of voltage space. Finally, the chapter included a series of circuit synthesis guidelines for developing soft-switched inverters. These guidelines were based on a distillation of the myriad of resonant link inverter designs proposed in the literature during the past decade.

Chapter V described the circuit synthesis process used to develop an electrically viable soft-switched inverter that approximates the voltage space characteristics of the abstract hypothetical inverter proposed in Chapter IV. The discussions described various tradeoffs made during the synthesis process in order to adhere to the soft-switched inverter design guidelines proposed at the end of Chapter IV. The net result was a new soft-switched inverter topology consisting of a conventional hard-switched bridge inverter augmented with an oscillating auxiliary link arrangement that allows all switching devices to turn on and off under near zero voltage conditions. This particular inverter design was assigned the name "Parallel Resonant Auxiliary Link" or PRAL due to the resonant circuit configuration used to drive the auxiliary link. The name assigned to the topological class containing the PRAL inverter is aptly labeled "Resonant Auxiliary Link" to distinguish it from the "Resonant Link" class that essentially encompasses all soft-switched inverter topologies reported in the literature to date. Unlike the hypothetical inverter described in Chapter IV, the PRAL inverter is unsynchronized and has minor restrictions on its ability to directly transition between adjacent active states. None the less, it has exactly the same voltage stress level as a conventional hard-switched bridge inverter and is a reasonable "first cut" approximation to the idealistic hypothetical inverter described in Chapter IV.

Chapter VI discussed control and design issues specifically related to the PRAL inverter. The chapter began with the description of a real-time method for computing the boost current required for the auxiliary link resonant circuit. A strategy was then proposed for selectively elevating the

boost current in order to regulate the potential of the voltage divider node used to bias the auxiliary link resonant circuit. Next, a set of "first cut" guidelines were proposed for selecting circuit component parameter values. This was followed by a suggested iterative procedure for adjusting component parameter values based on the results of simulation trials. Finally, a load back EMF based cost-function approach to selecting "optimal" PRAL inverter power matrix states was described in sufficient detail to permit meaningful simulation experiments to be conducted in Chapter VIII.

Chapter VII marked the beginning of the validation phase of the PRAL inverter development. The inverter was modeled and simulated to demonstrate its electrical viability and to substantiate voltage stress and output waveform quality predictions. Adherence to soft-switched operating principles was validated using an electronic circuit simulation package (SPICE) that incorporated the complex terminal behavior of the switching devices into the overall inverter model. The results clearly demonstrated the ability of the auxiliary link arrangement to suppress the generation of switching energy. Additionally, the observed device voltage stress levels were effectively equal to the DC input voltage feeding the inverter, as predicted in Chapter V. Finally, the device current stresses did not exceed the peak load current, except as predicted in Chapter VI. In these isolated instances, both the magnitude and duration of the device currents were well within the surge current ratings of the switching devices, again as predicted in Chapter VI.

Chapter VIII employed state-variable modeling and simulation techniques to evaluate performance aspects of the PRAL inverter that eluded examination in Chapter VII due to limitations in the available electronic circuit simulation package. Additionally, a state-variable model of the SPRDL inverter proposed in [9] was included and evaluated against a comparable PRAL inverter design. The chapter began with a demonstration of the boost current computation and voltage divider potential stabilization strategies proposed in Chapter VI. Both control strategies were shown to work satisfactorily. Next, internal and external waveforms were presented for a three-phase version of the SPRDL inverter described in [9] and a PRAL inverter

with identical resonant circuit frequency and output ratings. Simulation trials were conducted with both inverters driving an inductive load with back EMF at various output frequencies. The PRAL inverter design used in these trials employed a simple PI controller to select power matrix states. The SPRDL inverter used a three-phase extrapolation of the single-phase current control scheme proposed in [9]. In all cases, the PRAL inverter demonstrated significantly less output waveform distortion than the SPRDL inverter. The load current THD was at least 30% lower for the PRAL inverter than for the SPRDL inverter at each examined output frequency, which ranged from 20 Hz to 60 Hz. Additionally, the cumulative device conduction, cumulative device switching, and resonant circuit losses were significantly lower for the PRAL inverter than for the SPRDL design in all trials. The total conversion losses in the PRAL inverter were below 85% of the corresponding SPRDL inverter losses in all cases. Finally, selected trials were repeated with the PRAL inverter model configured with the cost-function based load current controller described in Chapter VI. The resulting load current THD was less than 67% of the value seen for the PI load current controller and less than 43% of the value seen for the SPRDL inverter. The total conversion losses were slightly higher for the PRAL inverter with cost-function control than with PI control. However, the PRAL inverter demonstrated significantly lower losses than the SPRDL inverter in all cases examined, regardless of the strategy employed to control the load current.

9.2 Conclusions

The PRAL inverter fully satisfies the fundamental objective of this work, which was to develop a soft-switched inverter with the same low device voltage stress as a conventional hard-switched inverter. Although the voltage space approach to soft-switched inverter design lacks the virtues of strict analytical rigor and completeness, it has the merit of providing insight into a problem domain for which there are few other sources of illumination. Despite the shortcomings of this approach, the PRAL topology that resulted proved ostensibly superior to a comparable

leading SPRDL design not only in terms of voltage stress but also in terms of waveform quality and conversion efficiency.

The requirement for the three bilateral switches used in conjunction with the auxiliary link and the lack of control over state transition timing constitute the PRAL inverter's only apparent disadvantages compared to resonant link designs. The first of these is due to the absence of commercially available pre-packaged bilateral switch modules and the potential perception that the inverter's nine switching devices constitute an excessive switch count. However, recall that the voltage stress on the power matrix switches in the SPRDL inverter examined in Chapter VIII was 50% greater than for the PRAL inverter and that the current stress was essentially equal in both designs. Thus, the combined Volt-Ampere rating of the three self-extinguishing devices required in a single PRAL inverter leg is equivalent to that of the two self-extinguishing devices contained in a single SPRDL inverter leg. Moreover, the SPRDL inverter design requires an additional self-extinguishing device in its link drive circuit, with a required current rating approximately twice that of its power matrix devices and a voltage rating comparable to the PRAL inverter devices. Consequently, the PRAL inverter has a distinct net advantage in terms of cumulative self-extinguishing device Volt-Amperer requirements, despite its slightly larger switching device count.

If the PRAL topology were adopted as a staple inverter design, sufficient demand may be created to spur mass production of pre-packaged bilateral switches. Moreover, entire phase leg modules consisting of two unilateral switches and one bilateral switch may prove economically feasible to produce on a mass scale. An example of a similar arrangement that is currently commercially available is the family of dual unilateral switch packages designed to modularly implement an entire leg of a conventional hard-switched inverter.

The second potential disadvantage stems from adherence to the soft-switched inverter design guidelines proposed in Chapter VI that essentially precluded inclusion of circuitry to control the time at which state transitions occur. Had such circuitry been incorporated into the design, the

switching device count would have likely risen to truly undesirable levels. However, the results of Chapter VIII are compelling evidence that the lack of control over state transition times is secondary compared to the fundamental advantages of PRAL inverter's voltage space properties. In conclusion, the analytical predictions and simulation results presented in this work clearly warrant continued investigation of the PRAL inverter concept through laboratory evaluation of hardware prototypes.

9.3 Recommendations for Further Investigation

A kaleidoscope of issues related to the concepts and techniques described in this thesis warrant further investigation. The topics recommended for further study fall into two broad categories. The first of these is the analysis and synthesis of generalized electronic power conditioning systems from the perspective of their behavior in voltage space. This includes studying the voltage space trajectory restrictions that fundamentally limit a given topology's performance capabilities and the control strategies that "optimally" select inverter states, and state transition times in the case of synchronized designs. The second category consists of issues relating to the refinement of the PRAL inverter design outlined in Chapters V and VI. Issues in this category range from developing robust analytical methods for selecting component values to fault tolerant control strategies for safely handling the potentially catastrophic case where a T mode fails to transition to the proper L mode.

The voltage space concepts described in Chapter III were based on the bridge inverter structure. It may be valuable to expand these concepts to non-bridge structures, such as cycloconverters. Furthermore, extending this to a generalized approach encompassing all topological classes is admittedly an idealistic but potentially rewarding goal that may yield new topological structures or may show the bridge arrangement to be superior to all other structures. Secondly, analytical effort developed for the voltage space concepts presented in this work were

essentially limited to the computing of the lowest frequency at which output waveform distortion occurs for a given inverter operating under idealistic state selection and state transition time conditions. Significant benefits may be realized from expanding the analysis to include analytical methods for computing the power spectral density of the output waveform distortion associated with a given synthesized static voltage.

The next logical step in the evolution of the PRAL inverter, beyond the work presented in this thesis, is experimentation with hardware prototypes. This will undoubtedly result in the identification of design issues that were not considered in the modeling and simulation phase of this work. Although no significant problematic issues are anticipated, it is recommended that extension and refinement of the "first cut" analytical PRAL inverter design tools presented in Chapters V and VI be made after evaluation of a hardware prototype inverter. This will allow any newly discovered behavior affecting the component parameter selection process to be integrated into a final set of design procedures.

The finite state machine model developed in Chapter V to describe the PRAL inverter's control system requirements did not address practical implementation issues, such as how oscillation is initially established in the auxiliary link. Numerous solutions exist for this and other related prototype implementation issues. Additionally, a strategy is needed to handle incidents in which the auxiliary link voltage fails to complete its transition to the target rail potential. Although such occurrences are expected to be rare, sensor noise, subtle errors in component parameter estimates, etc. can occasionally produce inadequate boost current values. In such cases, some form of override mechanism is needed in the inverter's control system to restore proper operation.

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APPENDIX A

SPICE SIMULATION MODEL FOR THE PRAL INVERTER

A.1 Expanded Top Level Views of the SPICE PRAL Inverter Model

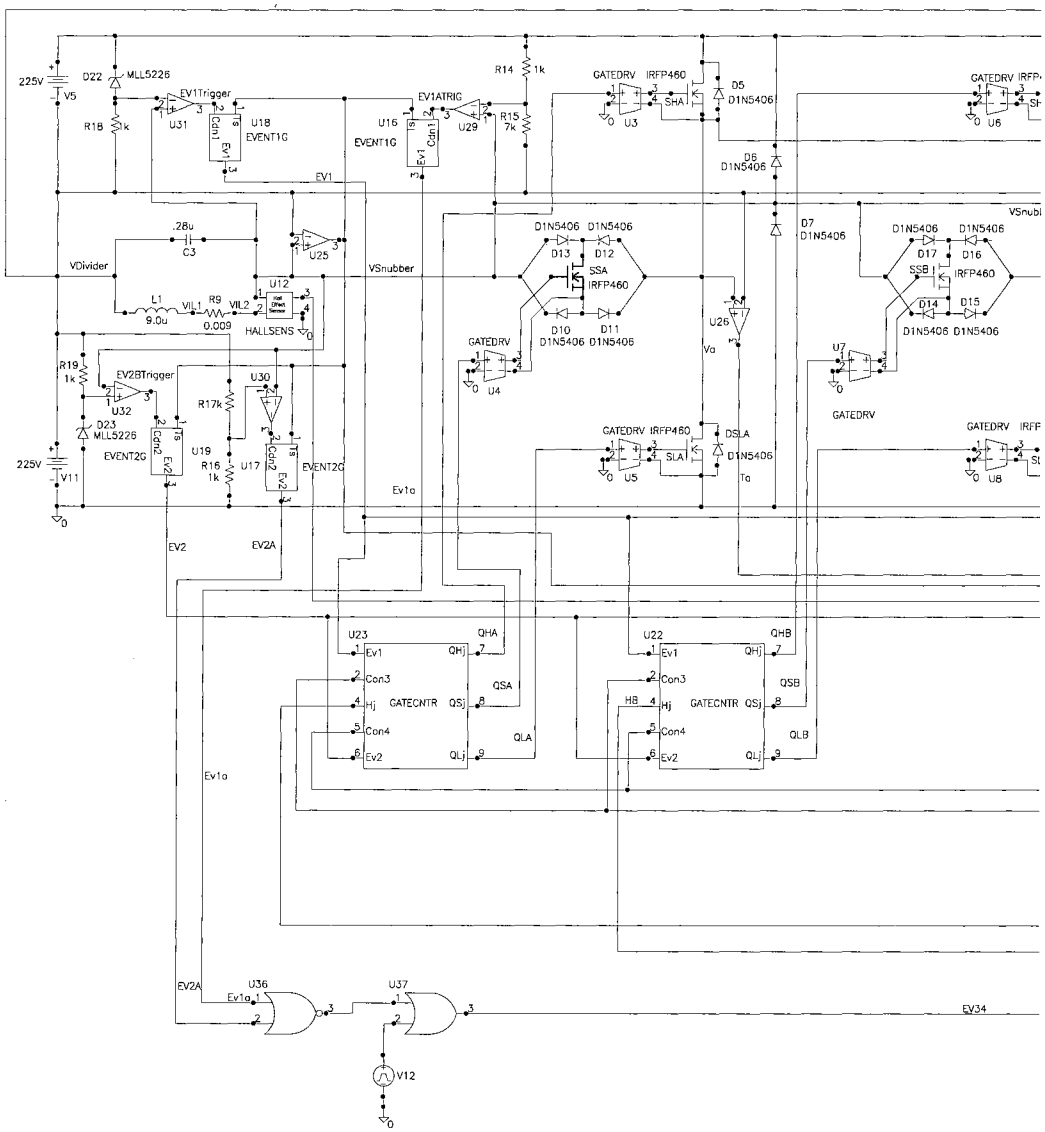

Figure A1. Left half of the PRAL inverter SPICE model schematic diagram

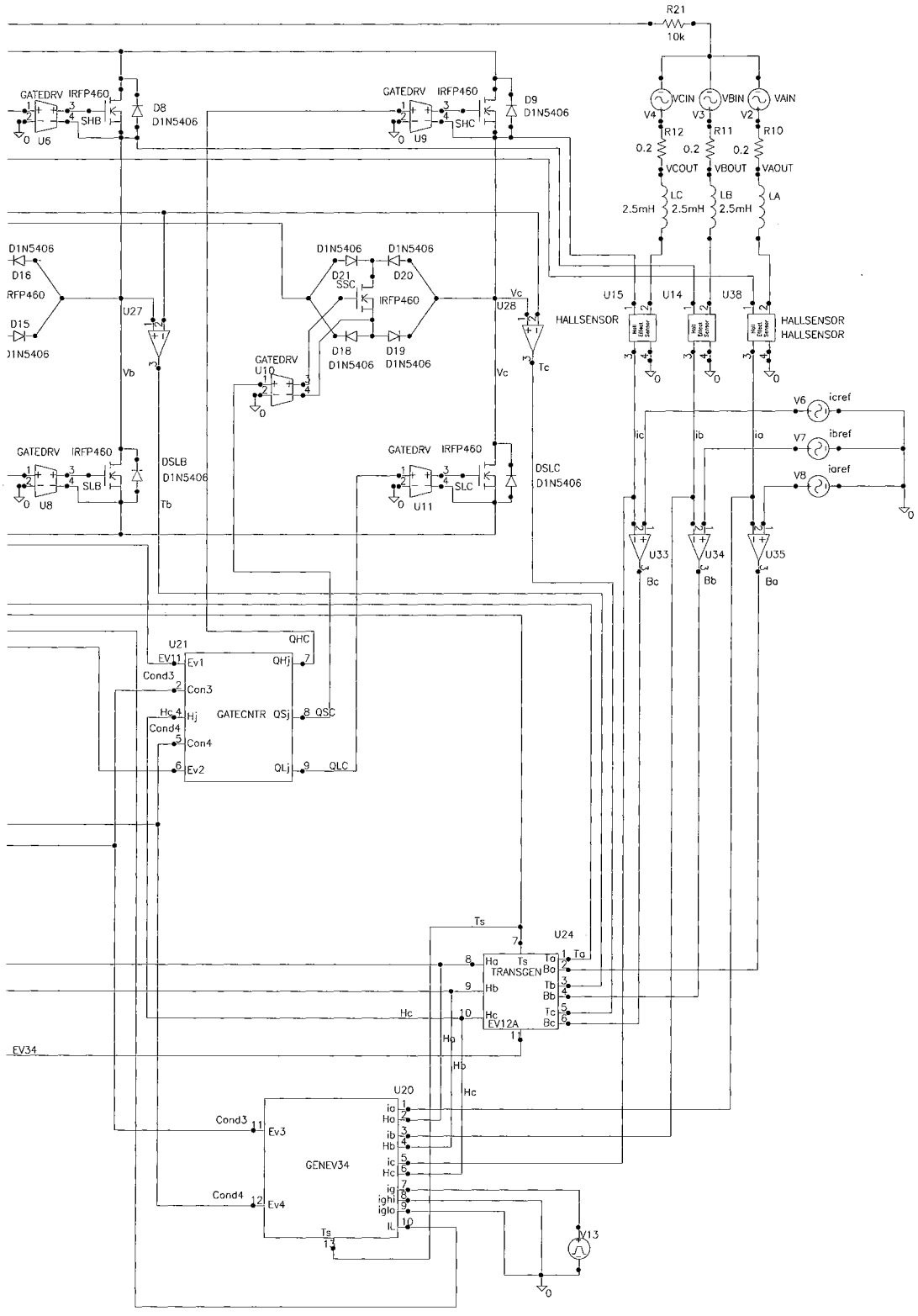

Figure A2. Right half of the PRAL inverter SPICE model schematic diagram

A2. Internal Views of SPICE User-Defined Blocks

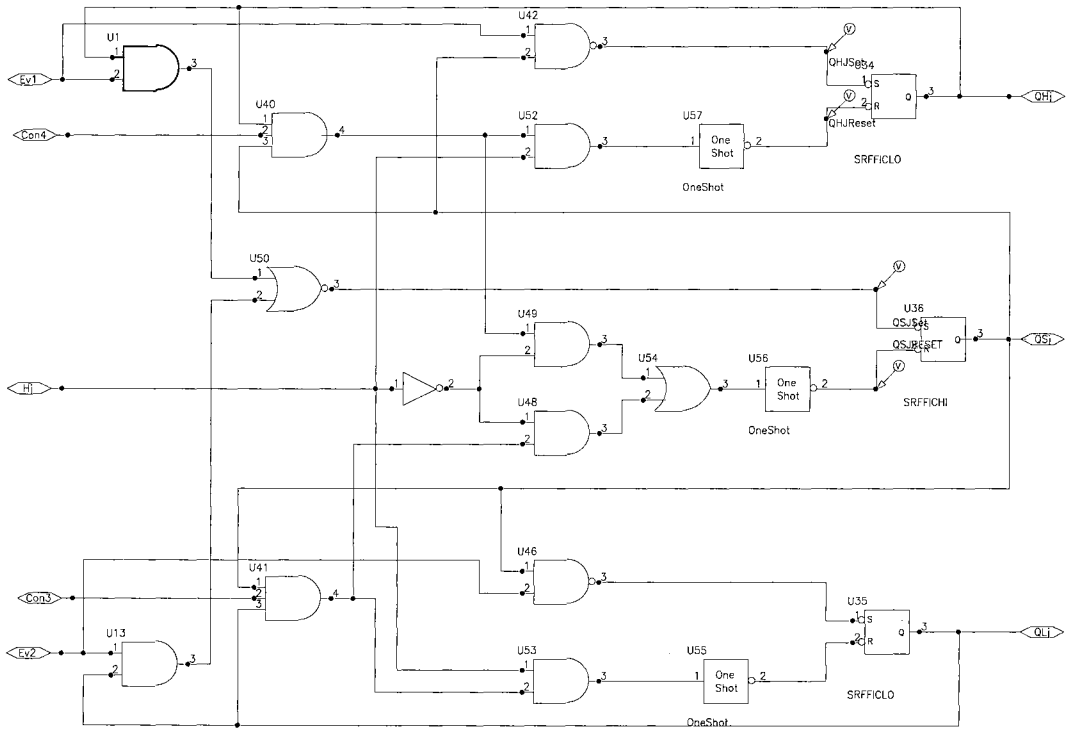

Figure A3. Expanded schematic diagram of the phase leg switch gate control block (GATECNTR)

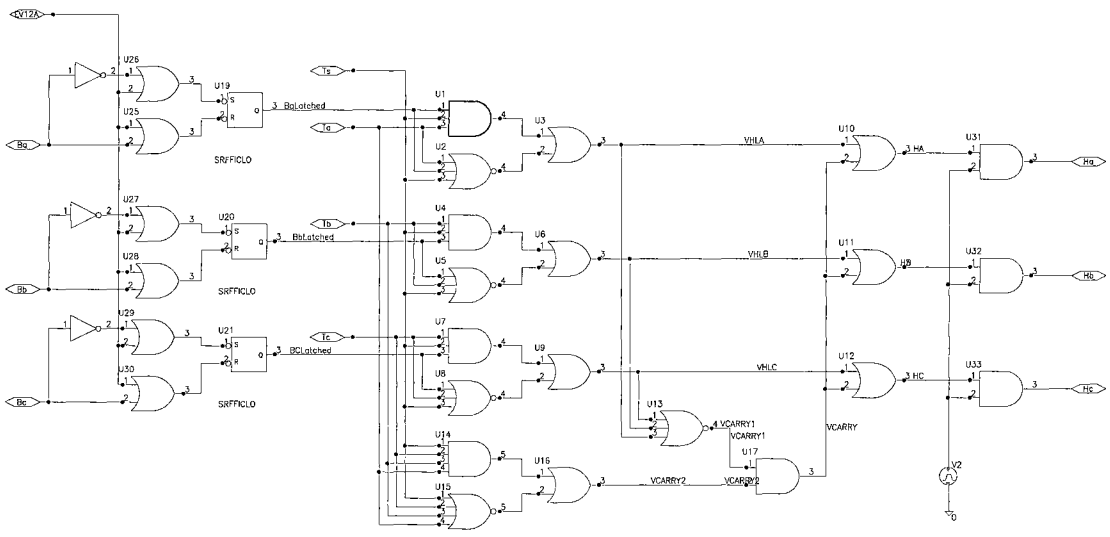

Figure A4. Expanded schematic diagram of the state transition generator control block (TRANSGEN)

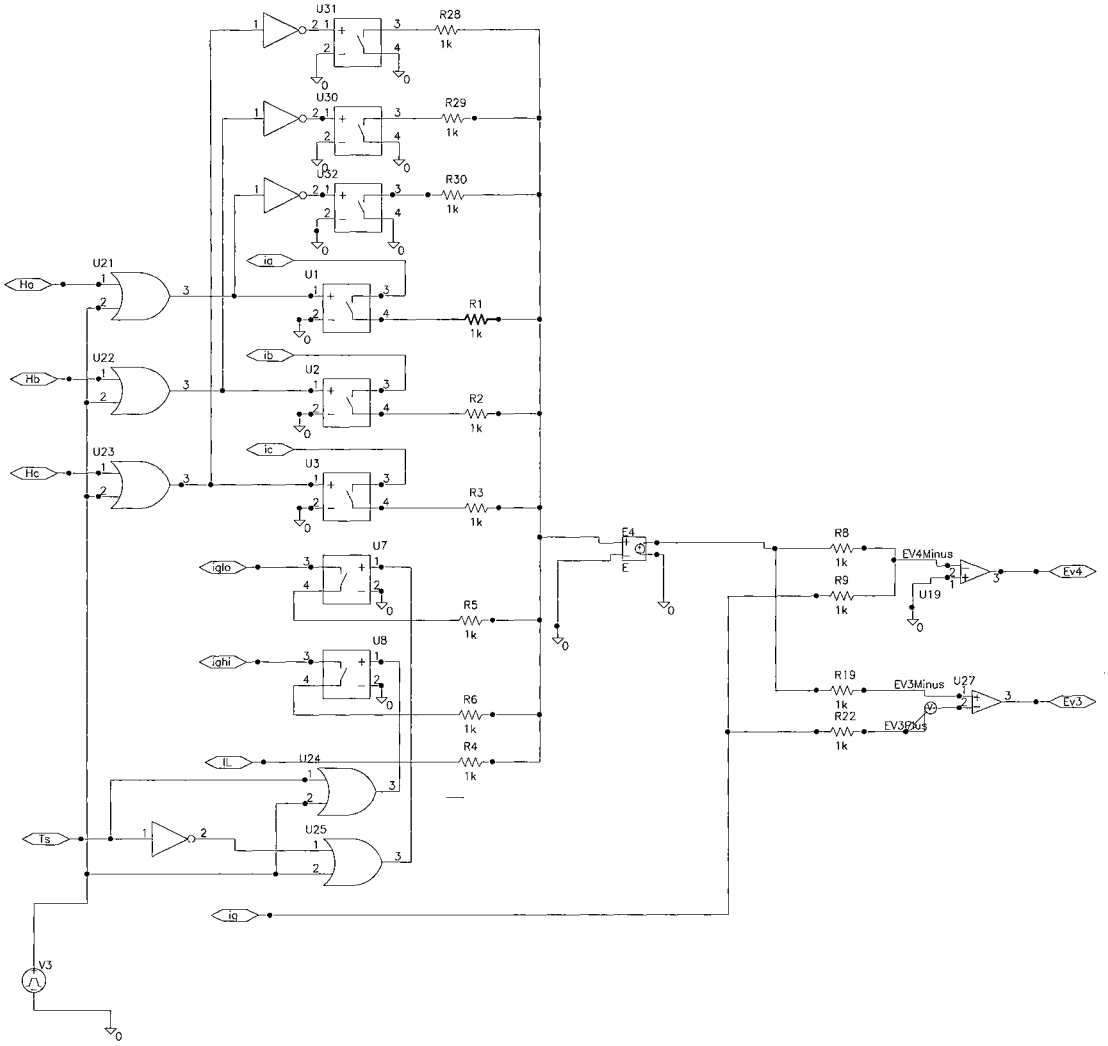

Figure A5. Expanded schematic diagram of the Event 3 and 4 generator block (GENEV34) used to initiate L_U to T_L mode transitions (Event 3) and L_L to T_U mode transitions (Event 4)

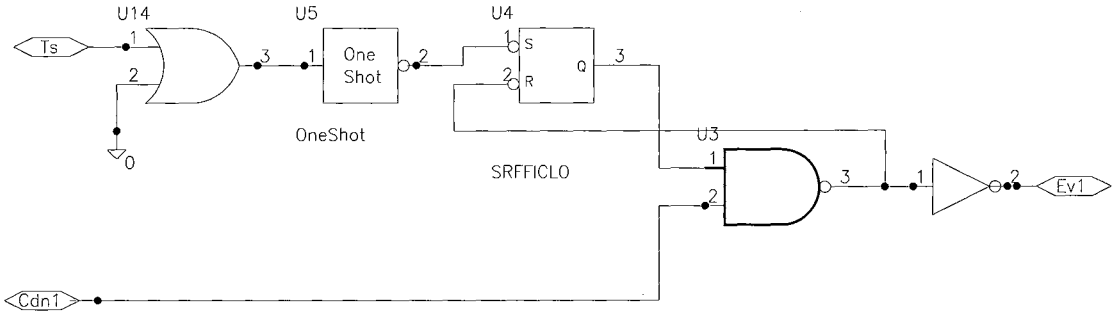

Figure A6. Expanded schematic diagram of the Event Type 1 generator block (EVENT1G) used to generate state transitions in the control logic state machine as the auxiliary link voltage rises toward the upper rail potential

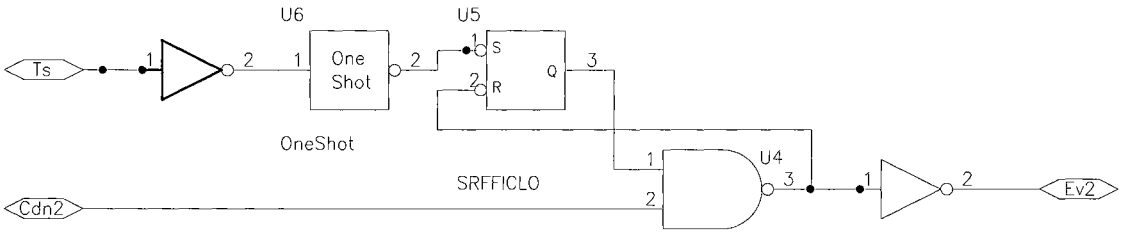

Figure A7. Expanded schematic diagram of the Event Type 2 generator block (EVENT2G) used to generate state transitions in the control logic state machine as the auxiliary link voltage falls toward the lower rail potential

A.3 SPICE Sub-Circuit Definition File for Analog Circuit Blocks Used in the SPICE PRAL Inverter Model

```
*********************************************************************
** Current Sensor
*********************************************************************
.subckt HALLSENSOR 1 2 3 4 params: gainp=1 R_1=1 R_2=1 C=1UF
R1 5 6 {R_1}
R2 6 3 {R_2}
C1 6 4 {C}
V1 2 1 0
H1 5 4 V1 0.1
.ends
*********************************************************************
** Ideal Amplifier
*********************************************************************
.subckt IDEALAMP 1 2 3 params: my_gain=1000
R1 1 2 500k
R2 3 4 1
E1 4 0 1 2 {my_gain}
.ends
*********************************************************************
** Gate Drive
*********************************************************************
.subckt GATEDRV 1 2 3 4 params: VINIT_IN=0 VINIT_OUT=0
R1 1 7 1k
R3 7 2 10k
R2 5 3 5
C1 7 2 0.1n IC={VINIT_IN}
C2 3 4 10n IC={VINIT_OUT}
E1 5 4 7 2 1.7
.ends
*********************************************************************
** Ideal Switch
*********************************************************************
.subckt IDEALSW 1 2 3 4
R1 1 5 10k
R2 2 5 10k
C1 1 5 0.01n IC=0
S1 3 4 1 5 SW1
.model SW1 VSWITCH ron=0.1 roff=1.0e6 von= 1.75 voff=0.75
.ends
```

A.4 SPICE Sub-Circuit Definition File for Digital Logic Circuit

Blocks used in the SPICE PRAL Inverter Model

```
*****************************************************************
** Two input NAND gate
*****************************************************************
.subckt NAND2 1 2 3 params: VINIT=0
R1 1 4 1k
R2 2 5 1k
R3 4 0 1k
R4 5 0 1k
C1 4 0 0.1n IC={VINIT}
C2 5 0 0.1n IC={VINIT}
V1 6 0 5
R5 6 3 5
S1 3 7 4 0 SW1
S2 7 0 5 0 SW1
.model SW1 VSWITCH ron=0.1 roff=1.0e4 von=1.75 voff=0.75
.ends
*****************************************************************
** Two input AND gate
*****************************************************************
.subckt AND2 1 2 3
R1 1 4 1k
R2 2 5 1k
R3 4 0 1k
R4 5 0 1k
C1 4 0 0.1n IC=0
C2 5 0 0.1n IC=0
V1 10 0 5
R5 3 0 5
S1 10 11 4 0 SW1
S2 11 3  5 0 SW1
.model SW1 VSWITCH ron=0.1 roff=1.0e4 von=1.75 voff=0.75
.ends
*****************************************************************
** Three input NAND gate
*****************************************************************
.subckt NAND3 1 2 3 4
R1 1 5 1k
R2 2 6 1k
R3 3 7 1k
R4 5 0 1k
R5 6 0 1k
R6 7 0 1k
C1 5 0 0.1n IC=0
C2 6 0 0.1n IC=0
C3 7 0 0.1n IC=0
V1 10 0 5
R7 10 4 5
S1 4 12 5 0 SW1
S2 12 13 6 0 SW1
S3 13 0 7 0 SW1
.model SW1 VSWITCH ron=0.1 roff=1.0e4 von=1.75 voff=0.75
```

```
.ends
*****************************************************************
** Four input AND gate
*****************************************************************
.subckt AND4 1 2 3 4 5
R1 1 6 1k
R2 2 7 1k
R3 3 8 1k
R4 4 9 1k
R5 6 0 1k
R6 7 0 1k
R7 8 0 1k
R8 9 0 1k
C1 6 0 0.1n IC=0
C2 7 0 0.1n IC=0
C3 8 0 0.1n IC=0
C4 9 0 0.1n IC=0
V1 10 0 5
R9 5 0 5
s1 10 20 6 0 SW1
s2 20 21 7 0 SW1
s3 21 22 8 0 SW1
s4 22 5  9 0 SW1
*C5 20 0 0.1n IC=0
*C6 21 0 0.1n IC=0
*C7 22 0 0.1n IC=0
*C8 5 0 0.1n  IC=0
.model SW1 VSWITCH ron=0.1 roff=1.0e3 von=1.75 voff=0.75
.ends
*****************************************************************
** Three input AND gate
*****************************************************************
.subckt AND3 1 2 3 4
R1 1 5 1k
R2 2 6 1k
R3 3 7 1k
R4 5 0 1k
R5 6 0 1k
R6 7 0 1k
C1 5 0 0.1n IC=0
C2 6 0 0.1n IC=0
C3 7 0 0.1n IC=0
V1 10 0 5
R7 4 0 5
S1 10 11 5 0 SW1
S2 11 12 6 0 SW1
S3 12 4  7 0 SW1
*C4 4 0 0.1n  IC=0
*C5 12 0 0.1n IC=0
*C6 11 0 0.1n IC=0
.model SW1 VSWITCH ron=0.1 roff=1.0e4 von=1.75 voff=0.75
.ends
*****************************************************************
** Inverter
*****************************************************************
.subckt INVERTER 1 2 params: VINIT=0
R1 1 3 1k
```

```
R2 3 0 1k
C1 3 0 0.1n IC={VINIT}
V1 4 0 5
R3 4 2 5
S1 2 0 3 0 SW1
.model SW1 VSWITCH ron=0.1 roff=1.0e4 von=1.75 voff=0.75
.ends
*****************************************************************
** Two input NOR
*****************************************************************
.subckt NOR2 1 2 3 params: VINIT=0
R1 1 4 1k
R2 2 5 1k
R3 4 0 1k
R4 5 0 1k
C1 4 0 0.1n IC={VINIT}
C2 5 0 0.1n IC={VINIT}
V1 6 0 5
R5 6 3 5
S1 3 0 4 0 SW1
S2 3 0 5 0 SW1
.model SW1 VSWITCH ron=0.1 roff=1.0e4 von=1.75 voff=0.75
.ends
*****************************************************************
** Two input OR
*****************************************************************
.subckt OR2 1 2 3 params: VINIT=0
R1 1 4 1k
R2 2 5 1k
R3 4 0 1k
R4 5 0 1k
C1 4 0 0.1n IC={VINIT}
C2 5 0 0.1n IC={VINIT}
V1 10 0 5
R5 3 0 1
S1 10 3 4 0 SW1
S2 10 3 5 0 SW1
.model SW1 VSWITCH ron=0.1 roff=1.0e4 von=1.75 voff=0.75
.ends
*****************************************************************
** Three input NOR
*****************************************************************
.subckt NOR3 1 2 3 4
R1 1 5 1k
R2 2 6 1k
R3 3 7 1k
R4 5 0 1k
R5 6 0 1k
R6 7 0 1k
C1 5 0 0.1n IC=0
C2 6 0 0.1n IC=0
C3 7 0 0.1n IC=0
V1 10 0 5
R7 10 4 1
S1 4 0 5 0 SW1
S2 4 0 6 0 SW1
S3 4 0 7 0 SW1
```

```
.model SW1 VSWITCH ron=0.1 roff=1.0e4 von=1.75 voff=0.75
.ends
*********************************************************************
** Four input NOR
*********************************************************************
.subckt NOR4 1 2 3 4 5
R1 1 6 1k
R2 2 7 1k
R3 3 8 1k
R4 4 9 1k
R5 6 0 1k
R6 7 0 1k
R7 8 0 1k
R8 9 0 1k
C1 6 0 0.1n IC=0
C2 7 0 0.1n IC=0
C3 8 0 0.1n IC=0
C4 9 0 0.1n IC=0
V1 10 0 5
R9 10 5 5
S1 5 0 6 0 SW1
S2 5 0 7 0 SW1
S3 5 0 8 0 SW1
S4 5 0 9 0 SW1
.model SW1 VSWITCH ron=0.1 roff=1.0e4 von=1.75 voff=0.75
.ends
*********************************************************************
** Three input OR
*********************************************************************
.subckt OR3 1 2 3 4
R1 1 5 1k
R2 2 6 1k
R3 3 7 1k
R4 5 0 1k
R5 6 0 1k
R6 7 0 1k
C1 5 0 0.1n IC=0
C2 6 0 0.1n IC=0
C3 7 0 0.1n IC=0
V1 10 0 5
R7 4 0 5
S1 10 4 5 0 SW1
S2 10 4 6 0 SW1
S3 10 4 7 0 SW1
.model SW1 VSWITCH ron=0.1 roff=1.0e4 von=1.75 voff=0.75
.ends
*********************************************************************
** Pulse Generator
*********************************************************************
.subckt PulseGen 1 2
C1 1 3 0.02nf IC=0
R1 1 3 10Meg
R2 3 0 10k
R3 4 2 5
V1 4 0 5
S1 2 0 3 0 SW1
.model SW1 VSWITCH ron=0.1 roff=1.0e4 von=2.525 voff=2.475
```

```
.ends
************************************************************
** Voltage Comparator
************************************************************
.subckt VCOMP 1 2 3 params: V_ON=0.0025 V_OFF=-0.0025
R1 1 10 50k
R2 2 20 50k
R3 3 4 1
R4 10 0 50k
R5 20 0 50k
c1 10 0 0.01p IC=0
c2 20 0 0.01p IC=0
D1 10 20 DIODE
D2 20 10 DIODE
V1 4 0 5
S1 3 0 20 10 SW1
.model DIODE D( BV = 1E5 )
.model SW1 VSWITCH ron=0.1 roff=1.0e4 von={V_ON} voff={V_OFF}
.ends
```

A.5 SPICE Circuit Simulation Definition File Generated for the PRAL Inverter Model

```
.tran 20ns 500us 0 20ns UIC
.OP
.lib D:msimlib\ilogic.lib
.lib D:msimlib\ianalog.lib
.lib nom.lib

M_SSA          $N_0003 $N_0002 $N_0001 $N_0001 IRFP460
M_SHA          $N_0005 $N_0004 Va Va IRFP460
M_SLA          Va $N_0006 0 0 IRFP460
M_SSB          $N_0009 $N_0008 $N_0007 $N_0007 IRFP460
M_SHB          $N_0005 $N_0010 Vb Vb IRFP460
M_SLB          Vb $N_0011 0 0 IRFP460
M_SSC          $N_0014 $N_0013 $N_0012 $N_0012 IRFP460
M_SHC          $N_0005 $N_0015 Vc Vc IRFP460
M_SLC          Vc $N_0016 0 0 IRFP460
L_L1          VDivider VIL1 9.0u IC=50
R_R9          VIL1 VIL2 0.009
C_C3          VDivider VSnubber .28u IC=170
V_V2          VAIN $N_0017
+SIN 0 120V 60 4us 0 0
V_V3          VBIN $N_0017
+SIN 0 120V 60 4us 0 120
V_V4          VCIN $N_0017
+SIN 0 120V 60 4us 0 240
R_R10          VAIN VAOUT 0.2
R_R11          VBIN VBOUT 0.2
R_R12          VCIN VCOUT 0.2
L_LB          VBOUT $N_0018 2.5mH IC=-17.32
L_LC          VCOUT $N_0019 2.5mH IC=17.32
L_LA          VAOUT $N_0020 2.5mH IC=0
V_V5          $N_0005 VDivider 225V
D_D5          Va $N_0005 D1N5406
D_D6          VSnubber $N_0005 D1N5406
D_D7          0 VSnubber D1N5406
D_DSLB          0 Vb D1N5406
D_DSLA          0 Va D1N5406
D_D8          Vb $N_0005 D1N5406
D_D9          Vc $N_0005 D1N5406
D_DSLC          0 Vc D1N5406
D_D10          $N_0001 VSnubber D1N5406
D_D11          $N_0001 Va D1N5406
D_D12          Va $N_0003 D1N5406
D_D13          VSnubber $N_0003 D1N5406
D_D14          $N_0007 VSnubber D1N5406
D_D15          $N_0007 Vb D1N5406
D_D16          Vb $N_0009 D1N5406
D_D17          VSnubber $N_0009 D1N5406
D_D18          $N_0012 VSnubber D1N5406
D_D19          $N_0012 Vc D1N5406
D_D20          Vc $N_0014 D1N5406
D_D21          VSnubber $N_0014 D1N5406
```

```
R_R14          $N_0021 $N_0005 1k
R_R15          VDivider $N_0021 7k
R_R16          0 $N_0022 1k
R_R17          $N_0022 VDivider 7k
D_D22          $N_0023 $N_0005 MLL5226
R_R18          VDivider $N_0023 1k
D_D23          0 $N_0024 MLL5226
R_R19          $N_0024 VDivider 1k
V_V6          icref 0
+SIN 0 2 60 0 0 60
V_V7          ibref 0
+SIN 0 2 60 0 0 -60
V_V8          iaref 0
+SIN 0 2 60 0 0 180
V_V11          VDivider 0 225V
X_U3          QHA 0 $N_0004 Va GATEDRV
+ PARAMS: VINIT_IN=0 VINIT_OUT=0
X_U4          QSA 0 $N_0002 $N_0001 GATEDRV
+ PARAMS: VINIT_IN=15 VINIT_OUT=15
X_U5          QLA 0 $N_0006 0 GATEDRV
+ PARAMS: VINIT_IN=0 VINIT_OUT=0
X_U6          QHB 0 $N_0010 Vb GATEDRV
+ PARAMS: VINIT_IN=0 VINIT_OUT=0
X_U7          QSB 0 $N_0008 $N_0007 GATEDRV
+ PARAMS: VINIT_IN=15 VINIT_OUT=15
X_U8          QLB 0 $N_0011 0 GATEDRV
+ PARAMS: VINIT_IN=0 VINIT_OUT=0
X_U9          QHC 0 $N_0015 Vc GATEDRV
+ PARAMS: VINIT_IN=0 VINIT_OUT=0
X_U10          QSC 0 $N_0013 $N_0012 GATEDRV
+ PARAMS: VINIT_IN=5 VINIT_OUT=15
X_U11          QLC 0 $N_0016 0 GATEDRV
+ PARAMS: VINIT_IN=0 VINIT_OUT=0
X_U12          VSnubber VIL2 $N_0072 0 HALLSENSOR
+ PARAMS: GAINP=1 R_1=2 R_2=2 C=.0001UF
X_U14          Vb $N_0018 ib 0 HALLSENSOR
+ PARAMS: GAINP=1 R_1=2 R_2=2 C=.0001UF
X_U16_U3          $N_0028 EV1ATRIG $N_0032 NAND2
+ PARAMS: VINIT=0
X_U16_U4_U8          $N_0027 $N_0029 $N_0028 NAND2
+ PARAMS: VINIT=5
V_U16_U4_V4          $N_0030 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U16_U4_V5          $N_0031 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U16_U4_U9          $N_0032 $N_0031 $N_0033 AND2
X_U16_U4_U10          $N_0036 $N_0030 $N_0029 OR2
+ PARAMS: VINIT=5
X_U16_U4_U11          $N_0033 $N_0028 $N_0027 NAND2
+ PARAMS: VINIT=0
C_U16_U5_C4          $N_0034 $N_0035 15n IC=0
R_U16_U5_R6          0 $N_0035 300
X_U16_U5_U10          $N_0035 $N_0036 INVERTER
+ PARAMS: VINIT=0
X_U16_U12          $N_0032 Ev1a INVERTER
+ PARAMS: VINIT=5
X_U16_U14          Ts 0 $N_0034 OR2
```

```
+ PARAMS: VINIT=0
X_U17_U1          Ts $N_0045 INVERTER
+ PARAMS: VINIT=0
X_U17_U4          $N_0039 $N_0037 $N_0043 NAND2
+ PARAMS: VINIT=0
X_U17_U5_U8          $N_0038 $N_0040 $N_0039 NAND2
+ PARAMS: VINIT=5
V_U17_U5_V4          $N_0041 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U17_U5_V5          $N_0042 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U17_U5_U9          $N_0043 $N_0042 $N_0044 AND2
X_U17_U5_U10          $N_0047 $N_0041 $N_0040 OR2
+ PARAMS: VINIT=5
X_U17_U5_U11          $N_0044 $N_0039 $N_0038 NAND2
+ PARAMS: VINIT=0
C_U17_U6_C4          $N_0045 $N_0046 15n IC=0
R_U17_U6_R6          0 $N_0046 300
X_U17_U6_U10          $N_0046 $N_0047 INVERTER
+ PARAMS: VINIT=0
X_U17_U9          $N_0043 EV2A INVERTER
+ PARAMS: VINIT=5
X_U18_U3          $N_0049 EV1Trigger $N_0053 NAND2
+ PARAMS: VINIT=0
X_U18_U4_U8          $N_0048 $N_0050 $N_0049 NAND2
+ PARAMS: VINIT=5
V_U18_U4_V4          $N_0051 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U18_U4_V5          $N_0052 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U18_U4_U9          $N_0053 $N_0052 $N_0054 AND2
X_U18_U4_U10          $N_0057 $N_0051 $N_0050 OR2
+ PARAMS: VINIT=5
X_U18_U4_U11          $N_0054 $N_0049 $N_0048 NAND2
+ PARAMS: VINIT=0
C_U18_U5_C4          $N_0055 $N_0056 15n IC=0
R_U18_U5_R6          0 $N_0056 300
X_U18_U5_U10          $N_0056 $N_0057 INVERTER
+ PARAMS: VINIT=0
X_U18_U12          $N_0053 EV1 INVERTER
+ PARAMS: VINIT=5
X_U18_U14          Ts 0 $N_0055 OR2
+ PARAMS: VINIT=0
X_U19_U1          Ts $N_0065 INVERTER
+ PARAMS: VINIT=0
X_U19_U4          $N_0059 EV2BTrigger $N_0063 NAND2
+ PARAMS: VINIT=0
X_U19_U5_U8          $N_0058 $N_0060 $N_0059 NAND2
+ PARAMS: VINIT=5
V_U19_U5_V4          $N_0061 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U19_U5_V5          $N_0062 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U19_U5_U9          $N_0063 $N_0062 $N_0064 AND2
X_U19_U5_U10          $N_0067 $N_0061 $N_0060 OR2
+ PARAMS: VINIT=5
X_U19_U5_U11          $N_0064 $N_0059 $N_0058 NAND2
```

```
+ PARAMS: VINIT=0
C_U19_U6_C4          $N_0065 $N_0066 15n IC=0
R_U19_U6_R6          0 $N_0066 300
X_U19_U6_U10          $N_0066 $N_0067 INVERTER
+ PARAMS: VINIT=0
X_U19_U9          $N_0063 EV2 INVERTER
+ PARAMS: VINIT=5
R_U20_R1          $N_0069 $N_0068 1k
R_U20_R2          $N_0070 $N_0068 1k
R_U20_R3          $N_0071 $N_0068 1k
R_U20_R4          $N_0072 $N_0068 1k
R_U20_R5          $N_0073 $N_0068 1k
R_U20_R6          $N_0074 $N_0068 1k
R_U20_R8          $N_0075 U20_EV4Minus 1k
R_U20_R9          $N_0076 U20_EV4Minus 1k
V_U20_V3          $N_0077 0
+PULSE 5 0 400ns 500ns 500ns 10000 200000
X_U20_U17          Ts $N_0078 INVERTER
+ PARAMS: VINIT=0
X_U20_U19          0 U20_EV4Minus Cond4 VCOMP
+ PARAMS: V_ON=0.0025 V_OFF=-0.0025
R_U20_R19          $N_0075 U20_EV3Minus 1k
X_U20_U21          Ha $N_0077 $N_0079 OR2
+ PARAMS: VINIT=0
X_U20_U22          Hb $N_0077 $N_0080 OR2
+ PARAMS: VINIT=0
X_U20_U23          Hc $N_0077 $N_0081 OR2
+ PARAMS: VINIT=0
X_U20_U24          Ts $N_0077 $N_0082 OR2
+ PARAMS: VINIT=0
X_U20_U25          $N_0078 $N_0077 $N_0083 OR2
+ PARAMS: VINIT=0
X_U20_U27          U20_EV3Minus U20_EV3Plus Cond3 VCOMP
+ PARAMS: V_ON=0.0025 V_OFF=-0.0025
R_U20_R22          $N_0076 U20_EV3Plus 1k
X_U20_U1          $N_0079 0 ia $N_0069 IDEALSW
X_U20_U2          $N_0080 0 ib $N_0070 IDEALSW
X_U20_U3          $N_0081 0 ic $N_0071 IDEALSW
X_U20_U7          $N_0083 0 0 $N_0073 IDEALSW
X_U20_U8          $N_0082 0 0 $N_0074 IDEALSW
E_U20_E4          $N_0075 0 $N_0068 0 5
X_U20_U30          $N_0084 0 $N_0085 0 IDEALSW
X_U20_U31          $N_0086 0 $N_0087 0 IDEALSW
X_U20_U32          $N_0088 0 $N_0089 0 IDEALSW
X_U20_U33          $N_0081 $N_0086 INVERTER
+ PARAMS: VINIT=0
X_U20_U34          $N_0080 $N_0084 INVERTER
+ PARAMS: VINIT=0
X_U20_U35          $N_0079 $N_0088 INVERTER
+ PARAMS: VINIT=0
R_U20_R28          $N_0087 $N_0068 1k
R_U20_R29          $N_0085 $N_0068 1k
R_U20_R30          $N_0089 $N_0068 1k
X_U21_U1          QHC EV1 $N_0090 AND2
X_U21_U13          EV2 QLC $N_0091 AND2
X_U21_U15          Hc $N_0092 INVERTER
+ PARAMS: VINIT=0
```

```
X_U21_U35_U8          $N_0097 $N_0098 QLC NAND2
+ PARAMS: VINIT=5
V_U21_U35_V4          $N_0099 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U21_U35_V5          $N_0100 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U21_U35_U9          $N_0113 $N_0100 $N_0101 AND2
X_U21_U35_U10          $N_0102 $N_0099 $N_0098 OR2
+ PARAMS: VINIT=5
X_U21_U35_U11          $N_0101 QLC $N_0097 NAND2
+ PARAMS: VINIT=0
X_U21_U34_U8          $N_0103 $N_0104 QHC NAND2
+ PARAMS: VINIT=5
V_U21_U34_V4          $N_0105 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U21_U34_V5          $N_0106 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U21_U34_U9          U21_QHJReset $N_0106 $N_0107 AND2
X_U21_U34_U10          U21_QHJSet $N_0105 $N_0104 OR2
+ PARAMS: VINIT=5
X_U21_U34_U11          $N_0107 QHC $N_0103 NAND2
+ PARAMS: VINIT=0
X_U21_U36_U3          $N_0108 U21_U36_VReset1 U21_U36_VOutBar NAND2
+ PARAMS: VINIT=5
V_U21_U36_V2          $N_0109 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U21_U36_V3          $N_0110 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U21_U36_U4          U21_QSJSet $N_0110 U21_U36_VSet1 AND2
X_U21_U36_U5          U21_QSJRESET $N_0109 U21_U36_VReset1 OR2
+ PARAMS: VINIT=5
X_U21_U36_U6          U21_U36_VSet1 U21_U36_VOutBar $N_0108 NAND2
+ PARAMS: VINIT=0
R_U21_U36_R2          $N_0108 QSC 5
X_U21_U40           QHC Cond4 QSC $N_0093 AND3
X_U21_U41           QSC Cond3 QLC $N_0094 AND3
X_U21_U42           EV1 QSC U21_QHJSet NAND2
+ PARAMS: VINIT=0
X_U21_U48           $N_0092 $N_0094 $N_0095 AND2
X_U21_U49           $N_0093 $N_0092 $N_0096 AND2
X_U21_U50           $N_0090 $N_0091 U21_QSJSet NOR2
+ PARAMS: VINIT=5
X_U21_U52           $N_0093 Hc $N_0116 AND2
X_U21_U53           Hc $N_0094 $N_0111 AND2
X_U21_U46           QSC EV2 $N_0102 NAND2
+ PARAMS: VINIT=0
X_U21_U54           $N_0096 $N_0095 $N_0114 OR2
+ PARAMS: VINIT=0
C_U21_U55_C4          $N_0111 $N_0112 15n IC=0
R_U21_U55_R6          0 $N_0112 300
X_U21_U55_U10          $N_0112 $N_0113 INVERTER
+ PARAMS: VINIT=0
C_U21_U56_C4          $N_0114 $N_0115 15n IC=0
R_U21_U56_R6          0 $N_0115 300
X_U21_U56_U10          $N_0115 U21_QSJRESET INVERTER
+ PARAMS: VINIT=0
C_U21_U57_C4          $N_0116 $N_0117 15n IC=0
```

```
R_U21_U57_R6          0 $N_0117 300
X_U21_U57_U10          $N_0117 U21_QHJReset INVERTER
+ PARAMS: VINIT=0
X_U22_U1          QHB EV1 $N_0118 AND2
X_U22_U13          EV2 QLB $N_0119 AND2
X_U22_U15          Hb $N_0120 INVERTER
+ PARAMS: VINIT=0
X_U22_U35_U8          $N_0125 $N_0126 QLB NAND2
+ PARAMS: VINIT=5
V_U22_U35_V4          $N_0127 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U22_U35_V5          $N_0128 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U22_U35_U9          $N_0141 $N_0128 $N_0129 AND2
X_U22_U35_U10          $N_0130 $N_0127 $N_0126 OR2
+ PARAMS: VINIT=5
X_U22_U35_U11          $N_0129 QLB $N_0125 NAND2
+ PARAMS: VINIT=0
X_U22_U34_U8          $N_0131 $N_0132 QHB NAND2
+ PARAMS: VINIT=5
V_U22_U34_V4          $N_0133 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U22_U34_V5          $N_0134 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U22_U34_U9          U22_QHJReset $N_0134 $N_0135 AND2
X_U22_U34_U10          U22_QHJSet $N_0133 $N_0132 OR2
+ PARAMS: VINIT=5
X_U22_U34_U11          $N_0135 QHB $N_0131 NAND2
+ PARAMS: VINIT=0
X_U22_U36_U3          $N_0136 U22_U36_VReset1 U22_U36_VOutBar NAND2
+ PARAMS: VINIT=5
V_U22_U36_V2          $N_0137 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U22_U36_V3          $N_0138 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U22_U36_U4          U22_QSJSet $N_0138 U22_U36_VSet1 AND2
X_U22_U36_U5          U22_QSJRESET $N_0137 U22_U36_VReset1 OR2
+ PARAMS: VINIT=5
X_U22_U36_U6          U22_U36_VSet1 U22_U36_VOutBar $N_0136 NAND2
+ PARAMS: VINIT=0
R_U22_U36_R2          $N_0136 QSB 5
X_U22_U40          QHB Cond4 QSB $N_0121 AND3
X_U22_U41          QSB Cond3 QLB $N_0122 AND3
X_U22_U42          EV1 QSB U22_QHJSet NAND2
+ PARAMS: VINIT=0
X_U22_U48          $N_0120 $N_0122 $N_0123 AND2
X_U22_U49          $N_0121 $N_0120 $N_0124 AND2
X_U22_U50          $N_0118 $N_0119 U22_QSJSet NOR2
+ PARAMS: VINIT=5
X_U22_U52          $N_0121 Hb $N_0144 AND2
X_U22_U53          Hb $N_0122 $N_0139 AND2
X_U22_U46          QSB EV2 $N_0130 NAND2
+ PARAMS: VINIT=0
X_U22_U54          $N_0124 $N_0123 $N_0142 OR2
+ PARAMS: VINIT=0
C_U22_U55_C4          $N_0139 $N_0140 15n IC=0
R_U22_U55_R6          0 $N_0140 300
```

```
X_U22_U55_U10          $N_0140 $N_0141 INVERTER
+ PARAMS: VINIT=0
C_U22_U56_C4           $N_0142 $N_0143 15n IC=0
R_U22_U56_R6           0 $N_0143 300
X_U22_U56_U10          $N_0143 U22_QSJRESET INVERTER
+ PARAMS: VINIT=0
C_U22_U57_C4           $N_0144 $N_0145 15n IC=0
R_U22_U57_R6           0 $N_0145 300
X_U22_U57_U10          $N_0145 U22_QHJReset INVERTER
+ PARAMS: VINIT=0
X_U23_U1          QHA EV1 $N_0146 AND2
X_U23_U13          EV2 QLA $N_0147 AND2
X_U23_U15          Ha $N_0148 INVERTER
+ PARAMS: VINIT=0
X_U23_U35_U8           $N_0153 $N_0154 QLA NAND2
+ PARAMS: VINIT=5
V_U23_U35_V4           $N_0155 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U23_U35_V5           $N_0156 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U23_U35_U9           $N_0169 $N_0156 $N_0157 AND2
X_U23_U35_U10          $N_0158 $N_0155 $N_0154 OR2
+ PARAMS: VINIT=5
X_U23_U35_U11          $N_0157 QLA $N_0153 NAND2
+ PARAMS: VINIT=0
X_U23_U34_U8           $N_0159 $N_0160 QHA NAND2
+ PARAMS: VINIT=5
V_U23_U34_V4           $N_0161 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U23_U34_V5           $N_0162 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U23_U34_U9           U23_QHJReset $N_0162 $N_0163 AND2
X_U23_U34_U10          U23_QHJSet $N_0161 $N_0160 OR2
+ PARAMS: VINIT=5
X_U23_U34_U11          $N_0163 QHA $N_0159 NAND2
+ PARAMS: VINIT=0
X_U23_U36_U3           $N_0164 U23_U36_VReset1 U23_U36_VOutBar NAND2
+ PARAMS: VINIT=5
V_U23_U36_V2           $N_0165 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U23_U36_V3           $N_0166 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U23_U36_U4           U23_QSJSet $N_0166 U23_U36_VSet1 AND2
X_U23_U36_U5           U23_QSJRESET $N_0165 U23_U36_VReset1 OR2
+ PARAMS: VINIT=5
X_U23_U36_U6           U23_U36_VSet1 U23_U36_VOutBar $N_0164 NAND2
+ PARAMS: VINIT=0
R_U23_U36_R2           $N_0164 QSA 5
X_U23_U40          QHA Cond4 QSA $N_0149 AND3
X_U23_U41          QSA Cond3 QLA $N_0150 AND3
X_U23_U42          EV1 QSA U23_QHJSet NAND2
+ PARAMS: VINIT=0
X_U23_U48          $N_0148 $N_0150 $N_0151 AND2
X_U23_U49          $N_0149 $N_0148 $N_0152 AND2
X_U23_U50          $N_0146 $N_0147 U23_QSJSet NOR2
+ PARAMS: VINIT=5
X_U23_U52          $N_0149 Ha $N_0172 AND2
```

```
X_U23_U53          Ha $N_0150 $N_0167 AND2
X_U23_U46          QSA EV2 $N_0158 NAND2
+ PARAMS: VINIT=0
X_U23_U54          $N_0152 $N_0151 $N_0170 OR2
+ PARAMS: VINIT=0
C_U23_U55_C4          $N_0167 $N_0168 15n IC=0
R_U23_U55_R6          0 $N_0168 300
X_U23_U55_U10          $N_0168 $N_0169 INVERTER
+ PARAMS: VINIT=0
C_U23_U56_C4          $N_0170 $N_0171 15n IC=0
R_U23_U56_R6          0 $N_0171 300
X_U23_U56_U10          $N_0171 U23_QSJRESET INVERTER
+ PARAMS: VINIT=0
C_U23_U57_C4          $N_0172 $N_0173 15n IC=0
R_U23_U57_R6          0 $N_0173 300
X_U23_U57_U10          $N_0173 U23_QHJReset INVERTER
+ PARAMS: VINIT=0
X_U24_U1          U24_BaLatched Ts Ta $N_0174 AND3
X_U24_U2          Ta U24_BaLatched Ts $N_0175 NOR3
X_U24_U3          $N_0174 $N_0175 U24_VHLA OR2
+ PARAMS: VINIT=0
X_U24_U4          Tb Ts U24_BbLatched $N_0176 AND3
X_U24_U5          U24_BbLatched Tb Ts $N_0177 NOR3
X_U24_U6          $N_0176 $N_0177 U24_VHLB OR2
+ PARAMS: VINIT=0
X_U24_U7          Tc Ts U24_BCLatched $N_0178 AND3
X_U24_U8          U24_BCLatched Tc Ts $N_0179 NOR3
X_U24_U9          $N_0178 $N_0179 U24_VHLC OR2
+ PARAMS: VINIT=0
X_U24_U10          U24_VHLA U24_VCARRY U24_HA OR2
+ PARAMS: VINIT=0
X_U24_U11          U24_VHLB U24_VCARRY U24_HB OR2
+ PARAMS: VINIT=0
X_U24_U12          U24_VHLC U24_VCARRY U24_HC OR2
+ PARAMS: VINIT=0
X_U24_U13          U24_VHLC U24_VHLB U24_VHLA U24_VCARRY1 NOR3
X_U24_U14          Ts Tc Tb Ta $N_0180 AND4
X_U24_U15          Ts Tc Tb Ta $N_0181 NOR4
X_U24_U16          $N_0180 $N_0181 U24_VCARRY2 OR2
+ PARAMS: VINIT=0
X_U24_U17          U24_VCARRY1 U24_VCARRY2 U24_VCARRY AND2
X_U24_U19_U8          $N_0186 $N_0187 U24_BaLatched NAND2
+ PARAMS: VINIT=5
V_U24_U19_V4          $N_0188 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U24_U19_V5          $N_0189 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U24_U19_U9          $N_0190 $N_0189 $N_0191 AND2
X_U24_U19_U10          $N_0192 $N_0188 $N_0187 OR2
+ PARAMS: VINIT=5
X_U24_U19_U11          $N_0191 U24_BaLatched $N_0186 NAND2
+ PARAMS: VINIT=0
X_U24_U20_U8          $N_0193 $N_0194 U24_BbLatched NAND2
+ PARAMS: VINIT=5
V_U24_U20_V4          $N_0195 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U24_U20_V5          $N_0196 0
```

```
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U24_U20_U9          $N_0197 $N_0196 $N_0198 AND2
X_U24_U20_U10          $N_0199 $N_0195 $N_0194 OR2
+ PARAMS: VINIT=5
X_U24_U20_U11          $N_0198 U24_BbLatched $N_0193 NAND2
+ PARAMS: VINIT=0
X_U24_U21_U8          $N_0200 $N_0201 U24_BCLatched NAND2
+ PARAMS: VINIT=5
V_U24_U21_V4          $N_0202 0
+PULSE 5 0 2500ns 10n 10n 100000 200000
V_U24_U21_V5          $N_0203 0
+PULSE 0 5 2000ns 10n 10n 100000 200000
X_U24_U21_U9          $N_0204 $N_0203 $N_0205 AND2
X_U24_U21_U10          $N_0206 $N_0202 $N_0201 OR2
+ PARAMS: VINIT=5
X_U24_U21_U11          $N_0205 U24_BCLatched $N_0200 NAND2
+ PARAMS: VINIT=0
X_U24_U22          Ba $N_0182 INVERTER
+ PARAMS: VINIT=0
X_U24_U23          Bb $N_0183 INVERTER
+ PARAMS: VINIT=0
X_U24_U24          Bc $N_0184 INVERTER
+ PARAMS: VINIT=0
X_U24_U25          EV34 Ba $N_0190 OR2
+ PARAMS: VINIT=0
X_U24_U26          $N_0182 EV34 $N_0192 OR2
+ PARAMS: VINIT=0
X_U24_U27          $N_0183 EV34 $N_0199 OR2
+ PARAMS: VINIT=0
X_U24_U28          EV34 Bb $N_0197 OR2
+ PARAMS: VINIT=0
X_U24_U29          $N_0184 EV34 $N_0206 OR2
+ PARAMS: VINIT=0
X_U24_U30          EV34 Bc $N_0204 OR2
+ PARAMS: VINIT=0
X_U24_U31          U24_HA $N_0185 Ha AND2
X_U24_U32          U24_HB $N_0185 Hb AND2
X_U24_U33          U24_HC $N_0185 Hc AND2
V_U24_V2          $N_0185 0
+PULSE 0 5 1.6us 60ns 60ns 1000 2000
V_V12          $N_0025 0
+PULSE 5 0 1.1us 40ns 40ns 1000 2000
X_U25          VSnubber VDivider Ts VCOMP
+ PARAMS: V_ON=0.025 V_OFF=-0.025
X_U26          Va VDivider Ta VCOMP
+ PARAMS: V_ON=0.025 V_OFF=-0.025
X_U27          Vb VDivider Tb VCOMP
+ PARAMS: V_ON=0.025 V_OFF=-0.025
X_U28          Vc VDivider Tc VCOMP
+ PARAMS: V_ON=0.025 V_OFF=-0.025
X_U29          VSnubber $N_0021 EV1ATRIG VCOMP
+ PARAMS: V_ON=0.025 V_OFF=-0.025
X_U30          $N_0022 VSnubber $N_0037 VCOMP
+ PARAMS: V_ON=0.025 V_OFF=-0.025
X_U31          VSnubber $N_0023 EV1Trigger VCOMP
+ PARAMS: V_ON=0.025 V_OFF=-0.025
X_U32          $N_0024 VSnubber EV2BTrigger VCOMP
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```
+ PARAMS: V_ON=0.025 V_OFF=-0.025
X_U33          icref ic Bc VCOMP
+ PARAMS: V_ON=0.0025 V_OFF=-0.0025
X_U34          ibref ib Bb VCOMP
+ PARAMS: V_ON=0.0025 V_OFF=-0.0025
X_U35          iaref ia Ba VCOMP
+ PARAMS: V_ON=0.0025 V_OFF=-0.0025
X_U36          Ev1a EV2A $N_0026 NOR2
+ PARAMS: VINIT=0
X_U37          $N_0026 $N_0025 EV34 OR2
+ PARAMS: VINIT=5
V_V13          $N_0076 0
+PULSE 2 .5 3us 30ns 30ns 1000 2000
R_R21          VDivider $N_0017 10k
X_U15          Vc $N_0019 ic 0 HALLSENSOR
+ PARAMS: GAINP=1 R_1=2 R_2=2 C=.0001UF
X_U38          Va $N_0020 ia 0 HALLSENSOR
+ PARAMS: GAINP=1 R_1=1 R_2=2 C=1UF

* Schematics Aliases *

.ALIASES
M_SSA            SSA(d=$N_0003 g=$N_0002 s=$N_0001 s=$N_0001 )
M_SHA            SHA(d=$N_0005 g=$N_0004 s=Va s=Va )
M_SLA            SLA(d=Va g=$N_0006 s=0 s=0 )
M_SSB            SSB(d=$N_0009 g=$N_0008 s=$N_0007 s=$N_0007 )
M_SHB            SHB(d=$N_0005 g=$N_0010 s=Vb s=Vb )
M_SLB            SLB(d=Vb g=$N_0011 s=0 s=0 )
M_SSC            SSC(d=$N_0014 g=$N_0013 s=$N_0012 s=$N_0012 )
M_SHC            SHC(d=$N_0005 g=$N_0015 s=Vc s=Vc )
M_SLC            SLC(d=Vc g=$N_0016 s=0 s=0 )
L_L1             L1(1=VDivider 2=VIL1 )
R_R9             R9(1=VIL1 2=VIL2 )
C_C3             C3(1=VDivider 2=VSnubber )
V_V2             V2(+=VAIN -=$N_0017 )
V_V3             V3(+=VBIN -=$N_0017 )
V_V4             V4(+=VCIN -=$N_0017 )
R_R10            R10(1=VAIN 2=VAOUT )
R_R11            R11(1=VBIN 2=VBOUT )
R_R12            R12(1=VCIN 2=VCOUT )
L_LB             LB(1=VBOUT 2=$N_0018 )
L_LC             LC(1=VCOUT 2=$N_0019 )
L_LA             LA(1=VAOUT 2=$N_0020 )
V_V5             V5(+=$N_0005 -=VDivider )
D_D5             D5(1=Va 2=$N_0005 )
D_D6             D6(1=VSnubber 2=$N_0005 )
D_D7             D7(1=0 2=VSnubber )
D_DSLB           DSLB(1=0 2=Vb )
D_DSLA           DSLA(1=0 2=Va )
D_D8             D8(1=Vb 2=$N_0005 )
D_D9             D9(1=Vc 2=$N_0005 )
D_DSLC           DSLC(1=0 2=Vc )
D_D10            D10(1=$N_0001 2=VSnubber )
D_D11            D11(1=$N_0001 2=Va )
D_D12            D12(1=Va 2=$N_0003 )
D_D13            D13(1=VSnubber 2=$N_0003 )
D_D14            D14(1=$N_0007 2=VSnubber )
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```
D_D15           D15(1=$N_0007 2=Vb )
D_D16           D16(1=Vb 2=$N_0009 )
D_D17           D17(1=VSnubber 2=$N_0009 )
D_D18           D18(1=$N_0012 2=VSnubber )
D_D19           D19(1=$N_0012 2=Vc )
D_D20           D20(1=Vc 2=$N_0014 )
D_D21           D21(1=VSnubber 2=$N_0014 )
R_R14           R14(1=$N_0021 2=$N_0005 )
R_R15           R15(1=VDivider 2=$N_0021 )
R_R16           R16(1=0 2=$N_0022 )
R_R17           R17(1=$N_0022 2=VDivider )
D_D22           D22(1=$N_0023 2=$N_0005 )
R_R18           R18(1=VDivider 2=$N_0023 )
D_D23           D23(1=0 2=$N_0024 )
R_R19           R19(1=$N_0024 2=VDivider )
V_V6            V6(+=icref -=0 )
V_V7            V7(+=ibref -=0 )
V_V8            V8(+=iaref -=0 )
V_V11           V11(+=VDivider -=0 )
X_U3            U3(1=QHA 2=0 3=$N_0004 4=Va )
X_U4            U4(1=QSA 2=0 3=$N_0002 4=$N_0001 )
X_U5            U5(1=QLA 2=0 3=$N_0006 4=0 )
X_U6            U6(1=QHB 2=0 3=$N_0010 4=Vb )
X_U7            U7(1=QSB 2=0 3=$N_0008 4=$N_0007 )
X_U8            U8(1=QLB 2=0 3=$N_0011 4=0 )
X_U9            U9(1=QHC 2=0 3=$N_0015 4=Vc )
X_U10           U10(1=QSC 2=0 3=$N_0013 4=$N_0012 )
X_U11           U11(1=QLC 2=0 3=$N_0016 4=0 )
X_U12           U12(1=VSnubber 2=VIL2 3=$N_0072 4=0 )
X_U14           U14(1=Vb 2=$N_0018 3=ib 4=0 )
_    U16(Ts=Ts Cdn1=EV1ATRIG Ev1=Ev1a )
X_U16_U3          U16.U3(1=$N_0028 2=EV1ATRIG 3=$N_0032 )
_    U16.U4(Set=$N_0036 Reset=$N_0032 Output=$N_0028 )
X_U16_U4_U8          U16.U4.U8(1=$N_0027 2=$N_0029 3=$N_0028 )
V_U16_U4_V4          U16.U4.V4(+=$N_0030 -=0 )
V_U16_U4_V5          U16.U4.V5(+=$N_0031 -=0 )
X_U16_U4_U9          U16.U4.U9(1=$N_0032 2=$N_0031 3=$N_0033 )
X_U16_U4_U10          U16.U4.U10(1=$N_0036 2=$N_0030 3=$N_0029 )
X_U16_U4_U11          U16.U4.U11(1=$N_0033 2=$N_0028 3=$N_0027 )
_    U16.U5(1=$N_0034 2=$N_0036 )
C_U16_U5_C4          U16.U5.C4(1=$N_0034 2=$N_0035 )
R_U16_U5_R6          U16.U5.R6(1=0 2=$N_0035 )
X_U16_U5_U10          U16.U5.U10(1=$N_0035 2=$N_0036 )
X_U16_U12           U16.U12(1=$N_0032 2=Ev1a )
X_U16_U14           U16.U14(1=Ts 2=0 3=$N_0034 )
_    U17(Ts=Ts Cdn2=$N_0037 Ev2=EV2A )
X_U17_U1          U17.U1(1=Ts 2=$N_0045 )
X_U17_U4          U17.U4(1=$N_0039 2=$N_0037 3=$N_0043 )
_    U17.U5(Set=$N_0047 Reset=$N_0043 Output=$N_0039 )
X_U17_U5_U8          U17.U5.U8(1=$N_0038 2=$N_0040 3=$N_0039 )
V_U17_U5_V4          U17.U5.V4(+=$N_0041 -=0 )
V_U17_U5_V5          U17.U5.V5(+=$N_0042 -=0 )
X_U17_U5_U9          U17.U5.U9(1=$N_0043 2=$N_0042 3=$N_0044 )
X_U17_U5_U10          U17.U5.U10(1=$N_0047 2=$N_0041 3=$N_0040 )
X_U17_U5_U11          U17.U5.U11(1=$N_0044 2=$N_0039 3=$N_0038 )
_    U17.U6(1=$N_0045 2=$N_0047 )
C_U17_U6_C4          U17.U6.C4(1=$N_0045 2=$N_0046 )
```

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R_U17_U6_R6          U17.U6.R6(1=0 2=$N_0046 )
X_U17_U6_U10          U17.U6.U10(1=$N_0046 2=$N_0047 )
X_U17_U9          U17.U9(1=$N_0043 2=EV2A )
_    U18(Ts=Ts Cdn1=EV1Trigger Ev1=EV1 )
X_U18_U3          U18.U3(1=$N_0049 2=EV1Trigger 3=$N_0053 )
_    U18.U4(Set=$N_0057 Reset=$N_0053 Output=$N_0049 )
X_U18_U4_U8          U18.U4.U8(1=$N_0048 2=$N_0050 3=$N_0049 )
V_U18_U4_V4          U18.U4.V4(+=$N_0051 -=0 )
V_U18_U4_V5          U18.U4.V5(+=$N_0052 -=0 )
X_U18_U4_U9          U18.U4.U9(1=$N_0053 2=$N_0052 3=$N_0054 )
X_U18_U4_U10          U18.U4.U10(1=$N_0057 2=$N_0051 3=$N_0050 )
X_U18_U4_U11          U18.U4.U11(1=$N_0054 2=$N_0049 3=$N_0048 )
_    U18.U5(1=$N_0055 2=$N_0057 )
C_U18_U5_C4          U18.U5.C4(1=$N_0055 2=$N_0056 )
R_U18_U5_R6          U18.U5.R6(1=0 2=$N_0056 )
X_U18_U5_U10          U18.U5.U10(1=$N_0056 2=$N_0057 )
X_U18_U12          U18.U12(1=$N_0053 2=EV1 )
X_U18_U14          U18.U14(1=Ts 2=0 3=$N_0055 )
_    U19(Ts=Ts Cdn2=EV2BTrigger Ev2=EV2 )
X_U19_U1          U19.U1(1=Ts 2=$N_0065 )
X_U19_U4          U19.U4(1=$N_0059 2=EV2BTrigger 3=$N_0063 )
_    U19.U5(Set=$N_0067 Reset=$N_0063 Output=$N_0059 )
X_U19_U5_U8          U19.U5.U8(1=$N_0058 2=$N_0060 3=$N_0059 )
V_U19_U5_V4          U19.U5.V4(+=$N_0061 -=0 )
V_U19_U5_V5          U19.U5.V5(+=$N_0062 -=0 )
X_U19_U5_U9          U19.U5.U9(1=$N_0063 2=$N_0062 3=$N_0064 )
X_U19_U5_U10          U19.U5.U10(1=$N_0067 2=$N_0061 3=$N_0060 )
X_U19_U5_U11          U19.U5.U11(1=$N_0064 2=$N_0059 3=$N_0058 )
_    U19.U6(1=$N_0065 2=$N_0067 )
C_U19_U6_C4          U19.U6.C4(1=$N_0065 2=$N_0066 )
R_U19_U6_R6          U19.U6.R6(1=0 2=$N_0066 )
X_U19_U6_U10          U19.U6.U10(1=$N_0066 2=$N_0067 )
X_U19_U9          U19.U9(1=$N_0063 2=EV2 )
_    U20(ia=ia Ha=Ha ib=ib Hb=Hb ic=ic Hc=Hc ig=$N_0076 ighi=0 iglo=0
IL=$N_0072
+  Ev3=Cond3 Ev4=Cond4 Ts=Ts )
R_U20_R1          U20.R1(1=$N_0069 2=$N_0068 )
R_U20_R2          U20.R2(1=$N_0070 2=$N_0068 )
R_U20_R3          U20.R3(1=$N_0071 2=$N_0068 )
R_U20_R4          U20.R4(1=$N_0072 2=$N_0068 )
R_U20_R5          U20.R5(1=$N_0073 2=$N_0068 )
R_U20_R6          U20.R6(1=$N_0074 2=$N_0068 )
R_U20_R8          U20.R8(1=$N_0075 2=U20_EV4Minus )
R_U20_R9          U20.R9(1=$N_0076 2=U20_EV4Minus )
V_U20_V3          U20.V3(+=$N_0077 -=0 )
X_U20_U17          U20.U17(1=Ts 2=$N_0078 )
X_U20_U19          U20.U19(1=0 2=U20_EV4Minus 3=Cond4 )
R_U20_R19          U20.R19(1=$N_0075 2=U20_EV3Minus )
X_U20_U21          U20.U21(1=Ha 2=$N_0077 3=$N_0079 )
X_U20_U22          U20.U22(1=Hb 2=$N_0077 3=$N_0080 )
X_U20_U23          U20.U23(1=Hc 2=$N_0077 3=$N_0081 )
X_U20_U24          U20.U24(1=Ts 2=$N_0077 3=$N_0082 )
X_U20_U25          U20.U25(1=$N_0078 2=$N_0077 3=$N_0083 )
X_U20_U27          U20.U27(1=U20_EV3Minus 2=U20_EV3Plus 3=Cond3 )
R_U20_R22          U20.R22(1=$N_0076 2=U20_EV3Plus )
X_U20_U1          U20.U1(1=$N_0079 2=0 3=ia 4=$N_0069 )
X_U20_U2          U20.U2(1=$N_0080 2=0 3=ib 4=$N_0070 )
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X_U20_U3          U20.U3(1=$N_0081 2=0 3=ic 4=$N_0071 )
X_U20_U7          U20.U7(1=$N_0083 2=0 3=0 4=$N_0073 )
X_U20_U8          U20.U8(1=$N_0082 2=0 3=0 4=$N_0074 )
E_U20_E4          U20.E4(3=$N_0075 4=0 1=$N_0068 2=0 )
X_U20_U30          U20.U30(1=$N_0084 2=0 3=$N_0085 4=0 )
X_U20_U31          U20.U31(1=$N_0086 2=0 3=$N_0087 4=0 )
X_U20_U32          U20.U32(1=$N_0088 2=0 3=$N_0089 4=0 )
X_U20_U33          U20.U33(1=$N_0081 2=$N_0086 )
X_U20_U34          U20.U34(1=$N_0080 2=$N_0084 )
X_U20_U35          U20.U35(1=$N_0079 2=$N_0088 )
R_U20_R28          U20.R28(1=$N_0087 2=$N_0068 )
R_U20_R29          U20.R29(1=$N_0085 2=$N_0068 )
R_U20_R30          U20.R30(1=$N_0089 2=$N_0068 )
*    U21(Ev1=EV1 Con3=Cond3 Hj=Hc Con4=Cond4 Ev2=EV2 QHj=QHC QSj=QSC
QLj=QLC )
X_U21_U1          U21.U1(1=QHC 2=EV1 3=$N_0090 )
X_U21_U13          U21.U13(1=EV2 2=QLC 3=$N_0091 )
X_U21_U15          U21.U15(1=Hc 2=$N_0092 )
*    U21.U35(Set=$N_0102 Reset=$N_0113 Output=QLC )
X_U21_U35_U8          U21.U35.U8(1=$N_0097 2=$N_0098 3=QLC )
V_U21_U35_V4          U21.U35.V4(+=$N_0099 -=0 )
V_U21_U35_V5          U21.U35.V5(+=$N_0100 -=0 )
X_U21_U35_U9          U21.U35.U9(1=$N_0113 2=$N_0100 3=$N_0101 )
X_U21_U35_U10          U21.U35.U10(1=$N_0102 2=$N_0099 3=$N_0098 )
X_U21_U35_U11          U21.U35.U11(1=$N_0101 2=QLC 3=$N_0097 )
*    U21.U34(Set=U21_QHJSet Reset=U21_QHJReset Output=QHC )
X_U21_U34_U8          U21.U34.U8(1=$N_0103 2=$N_0104 3=QHC )
V_U21_U34_V4          U21.U34.V4(+=$N_0105 -=0 )
V_U21_U34_V5          U21.U34.V5(+=$N_0106 -=0 )
X_U21_U34_U9          U21.U34.U9(1=U21_QHJReset 2=$N_0106 3=$N_0107 )
X_U21_U34_U10          U21.U34.U10(1=U21_QHJSet 2=$N_0105 3=$N_0104 )
X_U21_U34_U11          U21.U34.U11(1=$N_0107 2=QHC 3=$N_0103 )
*    U21.U36(Set=U21_QSJSet Reset=U21_QSJRESET Output=QSC )
X_U21_U36_U3          U21.U36.U3(1=$N_0108 2=U21_U36_VReset1
3=U21_U36_VOutBar
+  )
V_U21_U36_V2          U21.U36.V2(+=$N_0109 -=0 )
V_U21_U36_V3          U21.U36.V3(+=$N_0110 -=0 )
X_U21_U36_U4          U21.U36.U4(1=U21_QSJSet 2=$N_0110 3=U21_U36_VSet1
)
X_U21_U36_U5          U21.U36.U5(1=U21_QSJRESET 2=$N_0109
3=U21_U36_VReset1 )
X_U21_U36_U6          U21.U36.U6(1=U21_U36_VSet1 2=U21_U36_VOutBar
3=$N_0108 )
R_U21_U36_R2          U21.U36.R2(1=$N_0108 2=QSC )
X_U21_U40          U21.U40(1=QHC 2=Cond4 3=QSC 4=$N_0093 )
X_U21_U41          U21.U41(1=QSC 2=Cond3 3=QLC 4=$N_0094 )
X_U21_U42          U21.U42(1=EV1 2=QSC 3=U21_QHJSet )
X_U21_U48          U21.U48(1=$N_0092 2=$N_0094 3=$N_0095 )
X_U21_U49          U21.U49(1=$N_0093 2=$N_0092 3=$N_0096 )
X_U21_U50          U21.U50(1=$N_0090 2=$N_0091 3=U21_QSJSet )
X_U21_U52          U21.U52(1=$N_0093 2=Hc 3=$N_0116 )
X_U21_U53          U21.U53(1=Hc 2=$N_0094 3=$N_0111 )
X_U21_U46          U21.U46(1=QSC 2=EV2 3=$N_0102 )
X_U21_U54          U21.U54(1=$N_0096 2=$N_0095 3=$N_0114 )
*    U21.U55(1=$N_0111 2=$N_0113 )
C_U21_U55_C4          U21.U55.C4(1=$N_0111 2=$N_0112 )
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R_U21_U55_R6          U21.U55.R6(1=0 2=$N_0112 )
X_U21_U55_U10          U21.U55.U10(1=$N_0112 2=$N_0113 )
_    U21.U56(1=$N_0114 2=U21_QSJRESET )
C_U21_U56_C4          U21.U56.C4(1=$N_0114 2=$N_0115 )
R_U21_U56_R6          U21.U56.R6(1=0 2=$N_0115 )
X_U21_U56_U10          U21.U56.U10(1=$N_0115 2=U21_QSJRESET )
_    U21.U57(1=$N_0116 2=U21_QHJReset )
C_U21_U57_C4          U21.U57.C4(1=$N_0116 2=$N_0117 )
R_U21_U57_R6          U21.U57.R6(1=0 2=$N_0117 )
X_U21_U57_U10          U21.U57.U10(1=$N_0117 2=U21_QHJReset )
_    U22(Ev1=EV1 Con3=Cond3 Hj=Hb Con4=Cond4 Ev2=EV2 QHj=QHB QSj=QSB
QLj=QLB )
X_U22_U1          U22.U1(1=QHB 2=EV1 3=$N_0118 )
X_U22_U13          U22.U13(1=EV2 2=QLB 3=$N_0119 )
X_U22_U15          U22.U15(1=Hb 2=$N_0120 )
_    U22.U35(Set=$N_0130 Reset=$N_0141 Output=QLB )
X_U22_U35_U8          U22.U35.U8(1=$N_0125 2=$N_0126 3=QLB )
V_U22_U35_V4          U22.U35.V4(+=$N_0127 -=0 )
V_U22_U35_V5          U22.U35.V5(+=$N_0128 -=0 )
X_U22_U35_U9          U22.U35.U9(1=$N_0141 2=$N_0128 3=$N_0129 )
X_U22_U35_U10          U22.U35.U10(1=$N_0130 2=$N_0127 3=$N_0126 )
X_U22_U35_U11          U22.U35.U11(1=$N_0129 2=QLB 3=$N_0125 )
_    U22.U34(Set=U22_QHJSet Reset=U22_QHJReset Output=QHB )
X_U22_U34_U8          U22.U34.U8(1=$N_0131 2=$N_0132 3=QHB )
V_U22_U34_V4          U22.U34.V4(+=$N_0133 -=0 )
V_U22_U34_V5          U22.U34.V5(+=$N_0134 -=0 )
X_U22_U34_U9          U22.U34.U9(1=U22_QHJReset 2=$N_0134 3=$N_0135 )
X_U22_U34_U10          U22.U34.U10(1=U22_QHJSet 2=$N_0133 3=$N_0132 )
X_U22_U34_U11          U22.U34.U11(1=$N_0135 2=QHB 3=$N_0131 )
_    U22.U36(Set=U22_QSJSet Reset=U22_QSJRESET Output=QSB )
X_U22_U36_U3          U22.U36.U3(1=$N_0136 2=U22_U36_VReset1
3=U22_U36_VOutBar
+  )
V_U22_U36_V2          U22.U36.V2(+=$N_0137 -=0 )
V_U22_U36_V3          U22.U36.V3(+=$N_0138 -=0 )
X_U22_U36_U4          U22.U36.U4(1=U22_QSJSet 2=$N_0138 3=U22_U36_VSet1
)
X_U22_U36_U5          U22.U36.U5(1=U22_QSJRESET 2=$N_0137
3=U22_U36_VReset1 )
X_U22_U36_U6          U22.U36.U6(1=U22_U36_VSet1 2=U22_U36_VOutBar
3=$N_0136 )
R_U22_U36_R2          U22.U36.R2(1=$N_0136 2=QSB )
X_U22_U40          U22.U40(1=QHB 2=Cond4 3=QSB 4=$N_0121 )
X_U22_U41          U22.U41(1=QSB 2=Cond3 3=QLB 4=$N_0122 )
X_U22_U42          U22.U42(1=EV1 2=QSB 3=U22_QHJSet )
X_U22_U48          U22.U48(1=$N_0120 2=$N_0122 3=$N_0123 )
X_U22_U49          U22.U49(1=$N_0121 2=$N_0120 3=$N_0124 )
X_U22_U50          U22.U50(1=$N_0118 2=$N_0119 3=U22_QSJSet )
X_U22_U52          U22.U52(1=$N_0121 2=Hb 3=$N_0144 )
X_U22_U53          U22.U53(1=Hb 2=$N_0122 3=$N_0139 )
X_U22_U46          U22.U46(1=QSB 2=EV2 3=$N_0130 )
X_U22_U54          U22.U54(1=$N_0124 2=$N_0123 3=$N_0142 )
_    U22.U55(1=$N_0139 2=$N_0141 )
C_U22_U55_C4          U22.U55.C4(1=$N_0139 2=$N_0140 )
R_U22_U55_R6          U22.U55.R6(1=0 2=$N_0140 )
X_U22_U55_U10          U22.U55.U10(1=$N_0140 2=$N_0141 )
_    U22.U56(1=$N_0142 2=U22_QSJRESET )
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```
C_U22_U56_C4          U22.U56.C4(1=$N_0142 2=$N_0143 )
R_U22_U56_R6          U22.U56.R6(1=0 2=$N_0143 )
X_U22_U56_U10          U22.U56.U10(1=$N_0143 2=U22_QSJRESET )
_    U22.U57(1=$N_0144 2=U22_QHJReset )
C_U22_U57_C4          U22.U57.C4(1=$N_0144 2=$N_0145 )
R_U22_U57_R6          U22.U57.R6(1=0 2=$N_0145 )
X_U22_U57_U10          U22.U57.U10(1=$N_0145 2=U22_QHJReset )
_    U23(Ev1=EV1 Con3=Cond3 Hj=Ha Con4=Cond4 Ev2=EV2 QHj=QHA QSj=QSA
QLj=QLA )
X_U23_U1          U23.U1(1=QHA 2=EV1 3=$N_0146 )
X_U23_U13          U23.U13(1=EV2 2=QLA 3=$N_0147 )
X_U23_U15          U23.U15(1=Ha 2=$N_0148 )
_    U23.U35(Set=$N_0158 Reset=$N_0169 Output=QLA )
X_U23_U35_U8          U23.U35.U8(1=$N_0153 2=$N_0154 3=QLA )
V_U23_U35_V4          U23.U35.V4(+=$N_0155 -=0 )
V_U23_U35_V5          U23.U35.V5(+=$N_0156 -=0 )
X_U23_U35_U9          U23.U35.U9(1=$N_0169 2=$N_0156 3=$N_0157 )
X_U23_U35_U10          U23.U35.U10(1=$N_0158 2=$N_0155 3=$N_0154 )
X_U23_U35_U11          U23.U35.U11(1=$N_0157 2=QLA 3=$N_0153 )
_    U23.U34(Set=U23_QHJSet Reset=U23_QHJReset Output=QHA )
X_U23_U34_U8          U23.U34.U8(1=$N_0159 2=$N_0160 3=QHA )
V_U23_U34_V4          U23.U34.V4(+=$N_0161 -=0 )
V_U23_U34_V5          U23.U34.V5(+=$N_0162 -=0 )
X_U23_U34_U9          U23.U34.U9(1=U23_QHJReset 2=$N_0162 3=$N_0163 )
X_U23_U34_U10          U23.U34.U10(1=U23_QHJSet 2=$N_0161 3=$N_0160 )
X_U23_U34_U11          U23.U34.U11(1=$N_0163 2=QHA 3=$N_0159 )
_    U23.U36(Set=U23_QSJSet Reset=U23_QSJRESET Output=QSA )
X_U23_U36_U3          U23.U36.U3(1=$N_0164 2=U23_U36_VReset1
3=U23_U36_VOutBar
+  )
V_U23_U36_V2          U23.U36.V2(+=$N_0165 -=0 )
V_U23_U36_V3          U23.U36.V3(+=$N_0166 -=0 )
X_U23_U36_U4          U23.U36.U4(1=U23_QSJSet 2=$N_0166 3=U23_U36_VSet1
)
X_U23_U36_U5          U23.U36.U5(1=U23_QSJRESET 2=$N_0165
3=U23_U36_VReset1 )
X_U23_U36_U6          U23.U36.U6(1=U23_U36_VSet1 2=U23_U36_VOutBar
3=$N_0164 )
R_U23_U36_R2          U23.U36.R2(1=$N_0164 2=QSA )
X_U23_U40          U23.U40(1=QHA 2=Cond4 3=QSA 4=$N_0149 )
X_U23_U41          U23.U41(1=QSA 2=Cond3 3=QLA 4=$N_0150 )
X_U23_U42          U23.U42(1=EV1 2=QSA 3=U23_QHJSet )
X_U23_U48          U23.U48(1=$N_0148 2=$N_0150 3=$N_0151 )
X_U23_U49          U23.U49(1=$N_0149 2=$N_0148 3=$N_0152 )
X_U23_U50          U23.U50(1=$N_0146 2=$N_0147 3=U23_QSJSet )
X_U23_U52          U23.U52(1=$N_0149 2=Ha 3=$N_0172 )
X_U23_U53          U23.U53(1=Ha 2=$N_0150 3=$N_0167 )
X_U23_U46          U23.U46(1=QSA 2=EV2 3=$N_0158 )
X_U23_U54          U23.U54(1=$N_0152 2=$N_0151 3=$N_0170 )
_    U23.U55(1=$N_0167 2=$N_0169 )
C_U23_U55_C4          U23.U55.C4(1=$N_0167 2=$N_0168 )
R_U23_U55_R6          U23.U55.R6(1=0 2=$N_0168 )
X_U23_U55_U10          U23.U55.U10(1=$N_0168 2=$N_0169 )
_    U23.U56(1=$N_0170 2=U23_QSJRESET )
C_U23_U56_C4          U23.U56.C4(1=$N_0170 2=$N_0171 )
R_U23_U56_R6          U23.U56.R6(1=0 2=$N_0171 )
X_U23_U56_U10          U23.U56.U10(1=$N_0171 2=U23_QSJRESET )
```

```
_    U23.U57(1=$N_0172 2=U23_QHJReset )
C_U23_U57_C4          U23.U57.C4(1=$N_0172 2=$N_0173 )
R_U23_U57_R6          U23.U57.R6(1=0 2=$N_0173 )
X_U23_U57_U10          U23.U57.U10(1=$N_0173 2=U23_QHJReset )
_    U24(Ta=Ta Ba=Ba Tb=Tb Bb=Bb Tc=Tc Bc=Bc Ts=Ts Ha=Ha Hb=Hb Hc=Hc
EV12A=EV34
+  )
X_U24_U1          U24.U1(1=U24_BaLatched 2=Ts 3=Ta 4=$N_0174 )
X_U24_U2          U24.U2(1=Ta 2=U24_BaLatched 3=Ts 4=$N_0175 )
X_U24_U3          U24.U3(1=$N_0174 2=$N_0175 3=U24_VHLA )
X_U24_U4          U24.U4(1=Tb 2=Ts 3=U24_BbLatched 4=$N_0176 )
X_U24_U5          U24.U5(1=U24_BbLatched 2=Tb 3=Ts 4=$N_0177 )
X_U24_U6          U24.U6(1=$N_0176 2=$N_0177 3=U24_VHLB )
X_U24_U7          U24.U7(1=Tc 2=Ts 3=U24_BCLatched 4=$N_0178 )
X_U24_U8          U24.U8(1=U24_BCLatched 2=Tc 3=Ts 4=$N_0179 )
X_U24_U9          U24.U9(1=$N_0178 2=$N_0179 3=U24_VHLC )
X_U24_U10          U24.U10(1=U24_VHLA 2=U24_VCARRY 3=U24_HA )
X_U24_U11          U24.U11(1=U24_VHLB 2=U24_VCARRY 3=U24_HB )
X_U24_U12          U24.U12(1=U24_VHLC 2=U24_VCARRY 3=U24_HC )
X_U24_U13          U24.U13(1=U24_VHLC 2=U24_VHLB 3=U24_VHLA
4=U24_VCARRY1 )
X_U24_U14          U24.U14(1=Ts 2=Tc 3=Tb 4=Ta 5=$N_0180 )
X_U24_U15          U24.U15(1=Ts 2=Tc 3=Tb 4=Ta 5=$N_0181 )
X_U24_U16          U24.U16(1=$N_0180 2=$N_0181 3=U24_VCARRY2 )
X_U24_U17          U24.U17(1=U24_VCARRY1 2=U24_VCARRY2 3=U24_VCARRY )
_    U24.U19(Set=$N_0192 Reset=$N_0190 Output=U24_BaLatched )
X_U24_U19_U8          U24.U19.U8(1=$N_0186 2=$N_0187 3=U24_BaLatched )
V_U24_U19_V4          U24.U19.V4(+=$N_0188 -=0 )
V_U24_U19_V5          U24.U19.V5(+=$N_0189 -=0 )
X_U24_U19_U9          U24.U19.U9(1=$N_0190 2=$N_0189 3=$N_0191 )
X_U24_U19_U10          U24.U19.U10(1=$N_0192 2=$N_0188 3=$N_0187 )
X_U24_U19_U11          U24.U19.U11(1=$N_0191 2=U24_BaLatched 3=$N_0186
)
_    U24.U20(Set=$N_0199 Reset=$N_0197 Output=U24_BbLatched )
X_U24_U20_U8          U24.U20.U8(1=$N_0193 2=$N_0194 3=U24_BbLatched )
V_U24_U20_V4          U24.U20.V4(+=$N_0195 -=0 )
V_U24_U20_V5          U24.U20.V5(+=$N_0196 -=0 )
X_U24_U20_U9          U24.U20.U9(1=$N_0197 2=$N_0196 3=$N_0198 )
X_U24_U20_U10          U24.U20.U10(1=$N_0199 2=$N_0195 3=$N_0194 )
X_U24_U20_U11          U24.U20.U11(1=$N_0198 2=U24_BbLatched 3=$N_0193
)
_    U24.U21(Set=$N_0206 Reset=$N_0204 Output=U24_BCLatched )
X_U24_U21_U8          U24.U21.U8(1=$N_0200 2=$N_0201 3=U24_BCLatched )
V_U24_U21_V4          U24.U21.V4(+=$N_0202 -=0 )
V_U24_U21_V5          U24.U21.V5(+=$N_0203 -=0 )
X_U24_U21_U9          U24.U21.U9(1=$N_0204 2=$N_0203 3=$N_0205 )
X_U24_U21_U10          U24.U21.U10(1=$N_0206 2=$N_0202 3=$N_0201 )
X_U24_U21_U11          U24.U21.U11(1=$N_0205 2=U24_BCLatched 3=$N_0200
)
X_U24_U22          U24.U22(1=Ba 2=$N_0182 )
X_U24_U23          U24.U23(1=Bb 2=$N_0183 )
X_U24_U24          U24.U24(1=Bc 2=$N_0184 )
X_U24_U25          U24.U25(1=EV34 2=Ba 3=$N_0190 )
X_U24_U26          U24.U26(1=$N_0182 2=EV34 3=$N_0192 )
X_U24_U27          U24.U27(1=$N_0183 2=EV34 3=$N_0199 )
X_U24_U28          U24.U28(1=EV34 2=Bb 3=$N_0197 )
X_U24_U29          U24.U29(1=$N_0184 2=EV34 3=$N_0206 )
```

```
X_U24_U30          U24.U30(1=EV34 2=Bc 3=$N_0204 )
X_U24_U31          U24.U31(1=U24_HA 2=$N_0185 3=Ha )
X_U24_U32          U24.U32(1=U24_HB 2=$N_0185 3=Hb )
X_U24_U33          U24.U33(1=U24_HC 2=$N_0185 3=Hc )
V_U24_V2         U24.V2(+=$N_0185 -=0 )
V_V12          V12(+=$N_0025 -=0 )
X_U25          U25(1=VSnubber 2=VDivider 3=Ts )
X_U26          U26(1=Va 2=VDivider 3=Ta )
X_U27          U27(1=Vb 2=VDivider 3=Tb )
X_U28          U28(1=Vc 2=VDivider 3=Tc )
X_U29          U29(1=VSnubber 2=$N_0021 3=EV1ATRIG )
X_U30          U30(1=$N_0022 2=VSnubber 3=$N_0037 )
X_U31          U31(1=VSnubber 2=$N_0023 3=EV1Trigger )
X_U32          U32(1=$N_0024 2=VSnubber 3=EV2BTrigger )
X_U33          U33(1=icref 2=ic 3=Bc )
X_U34          U34(1=ibref 2=ib 3=Bb )
X_U35          U35(1=iaref 2=ia 3=Ba )
X_U36          U36(1=Ev1a 2=EV2A 3=$N_0026 )
X_U37          U37(1=$N_0026 2=$N_0025 3=EV34 )
V_V13          V13(+=$N_0076 -=0 )
R_R21          R21(1=VDivider 2=$N_0017 )
X_U15          U15(1=Vc 2=$N_0019 3=ic 4=0 )
X_U38          U38(1=Va 2=$N_0020 3=ia 4=0 )
```

APPENDIX B

PRAL INVERTER STATE-VARIABLE SIMULATION MODELS

B.1 Top Level SIMULINK Block Diagrams Used to Simulate the PRAL Inverter

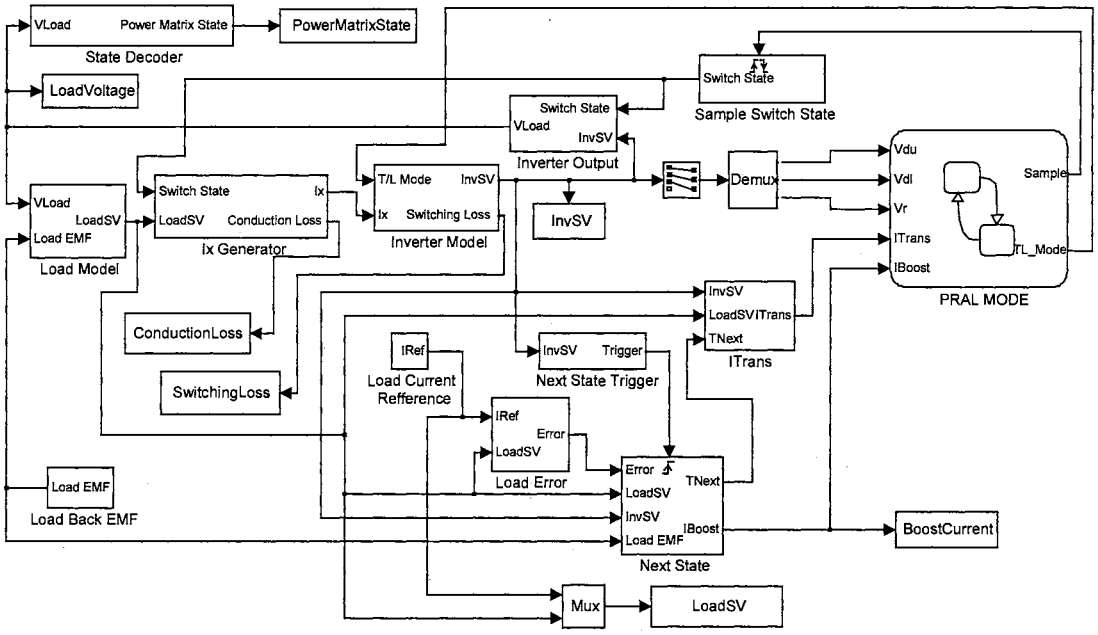

Figure B1. Top level block diagram of the PRAL inverter state-variable simulation model using PI current control

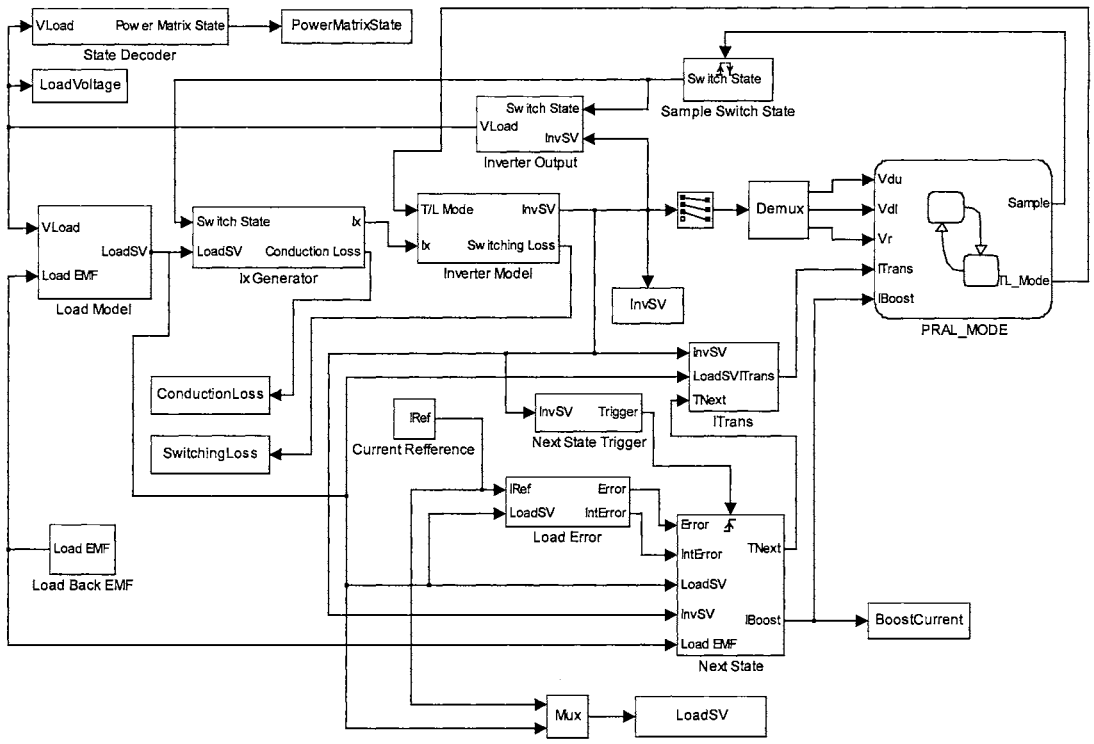

Figure B2. Top level block diagram of the PRAL inverter state-variable simulation model using cost function current control

B.2 STATEFLOW Block Diagram

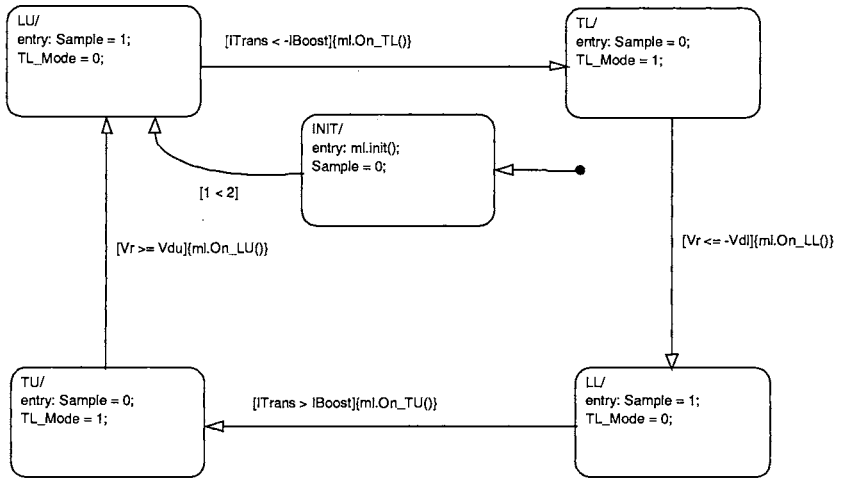

Figure B3. Internal view of the "PRAL Mode" block constructed using STATEFLOW

B.3 SIMULINK Block Diagrams of the PRAL Inverter and Load Models

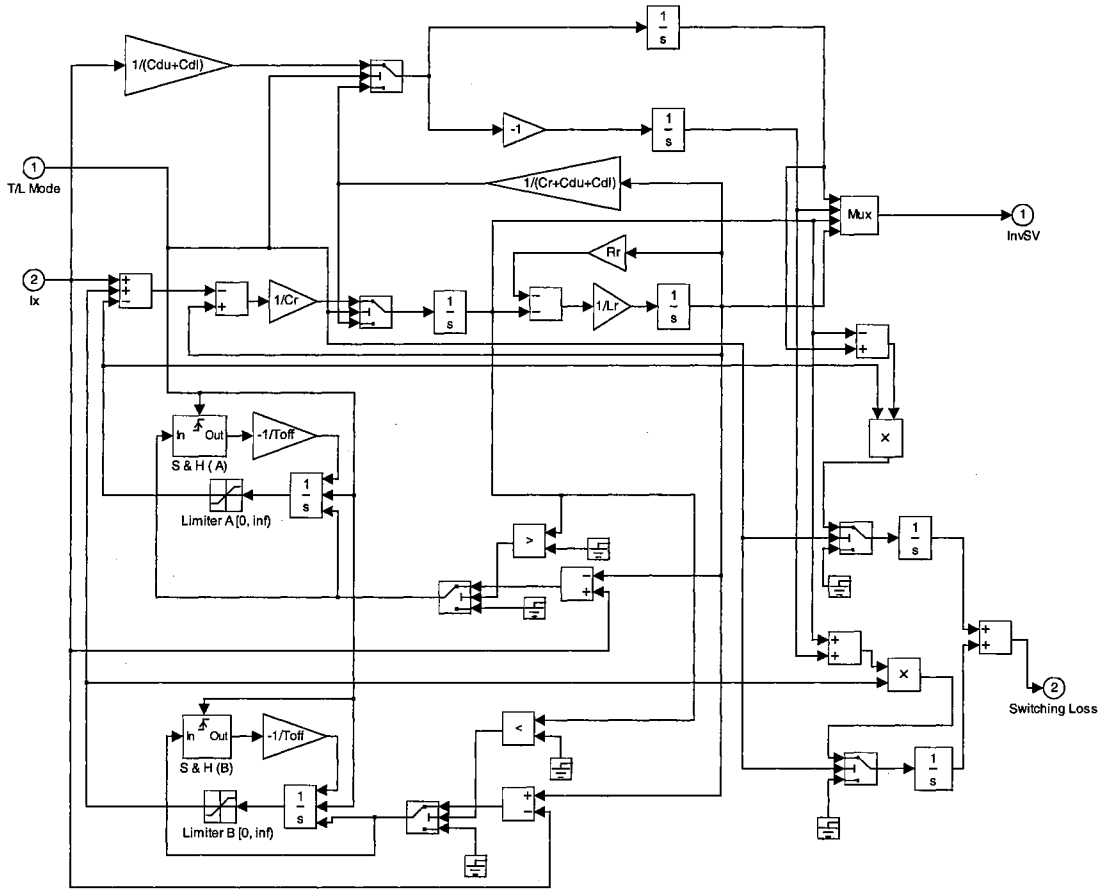

Figure B4. Internal view of the SIMULINK "Inverter Model" block

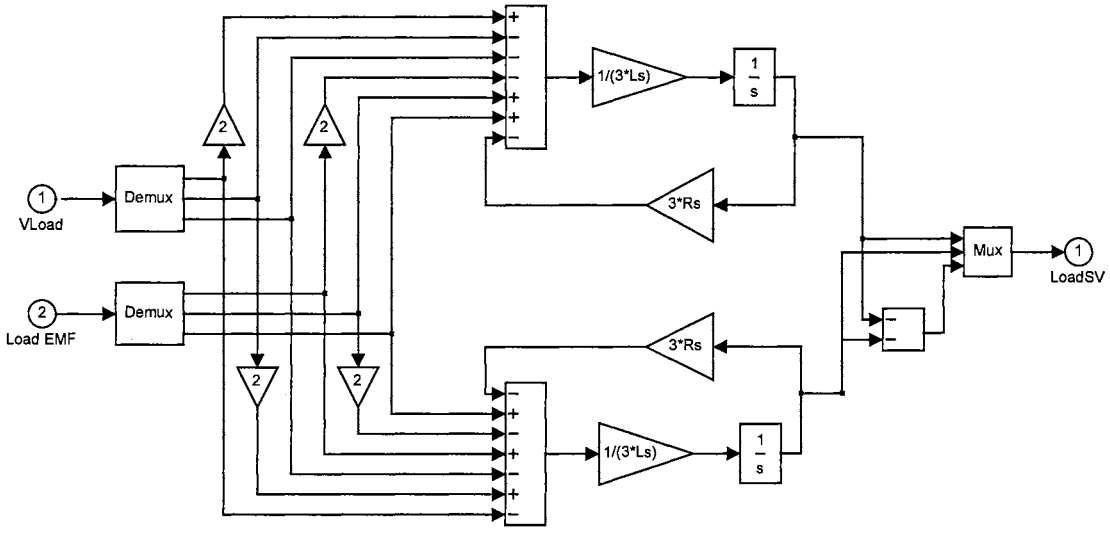

Figure B5. Internal view of the "Load Model" block

B.4 SIMULINK Block Diagrams of Control Blocks Common to Both PI and Cost Function Current Control Configurations

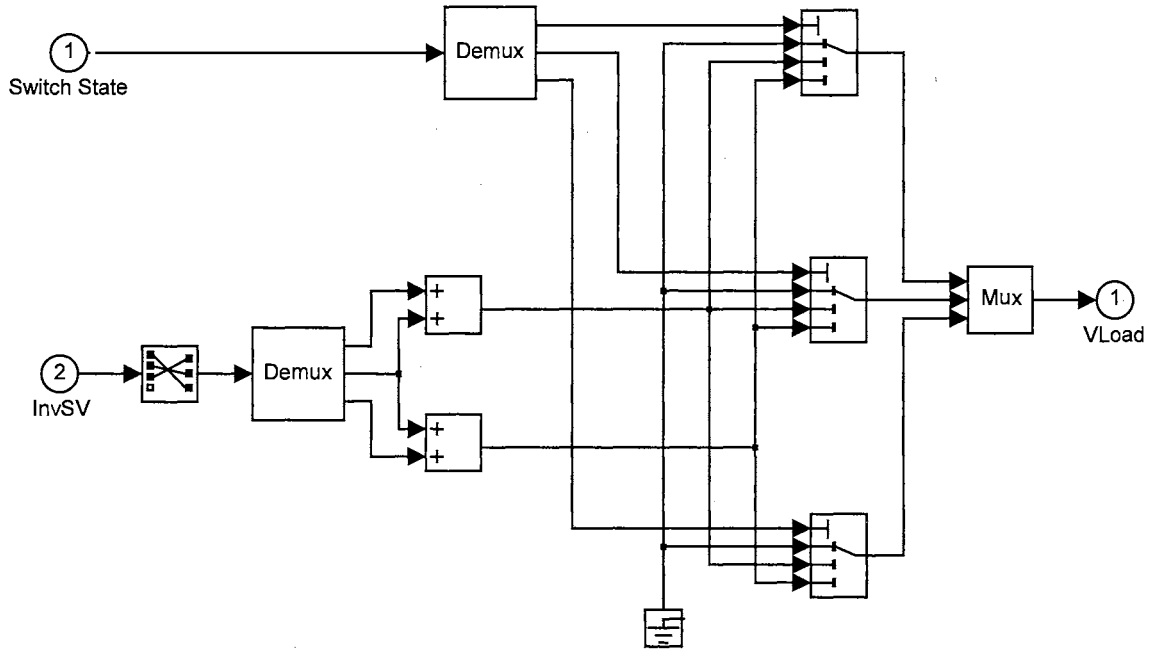

Figure B6. Internal view of the "Inverter Output" block

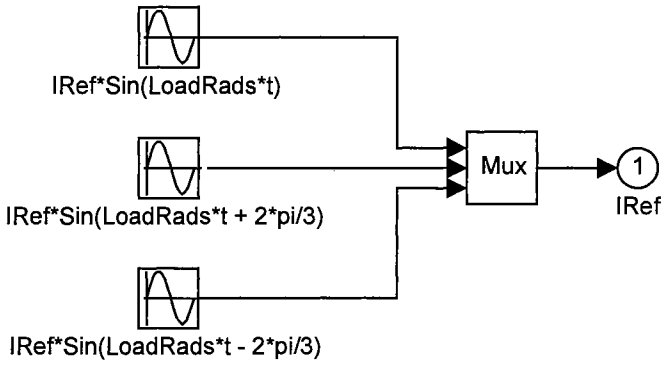

Figure B7. Internal view of the "Current Reference" block

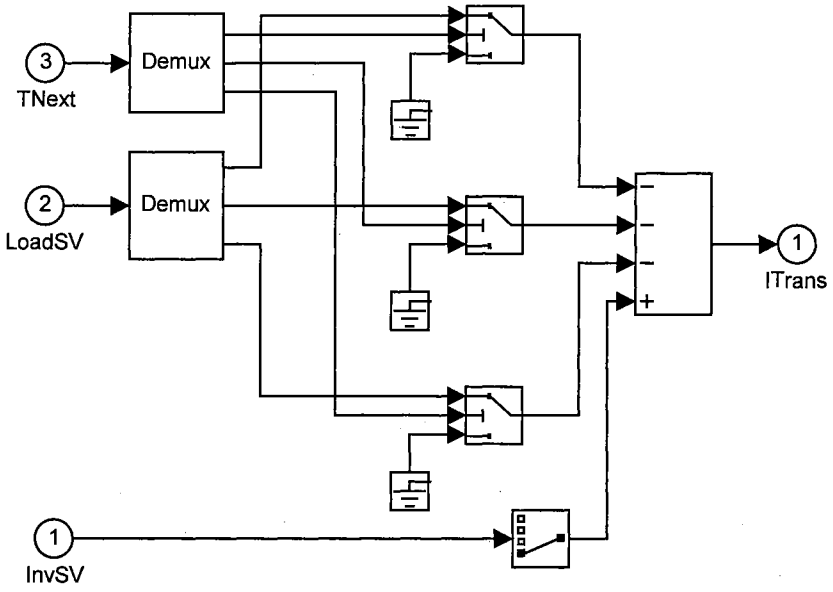

Figure B8. Internal view of the "ITrans" block

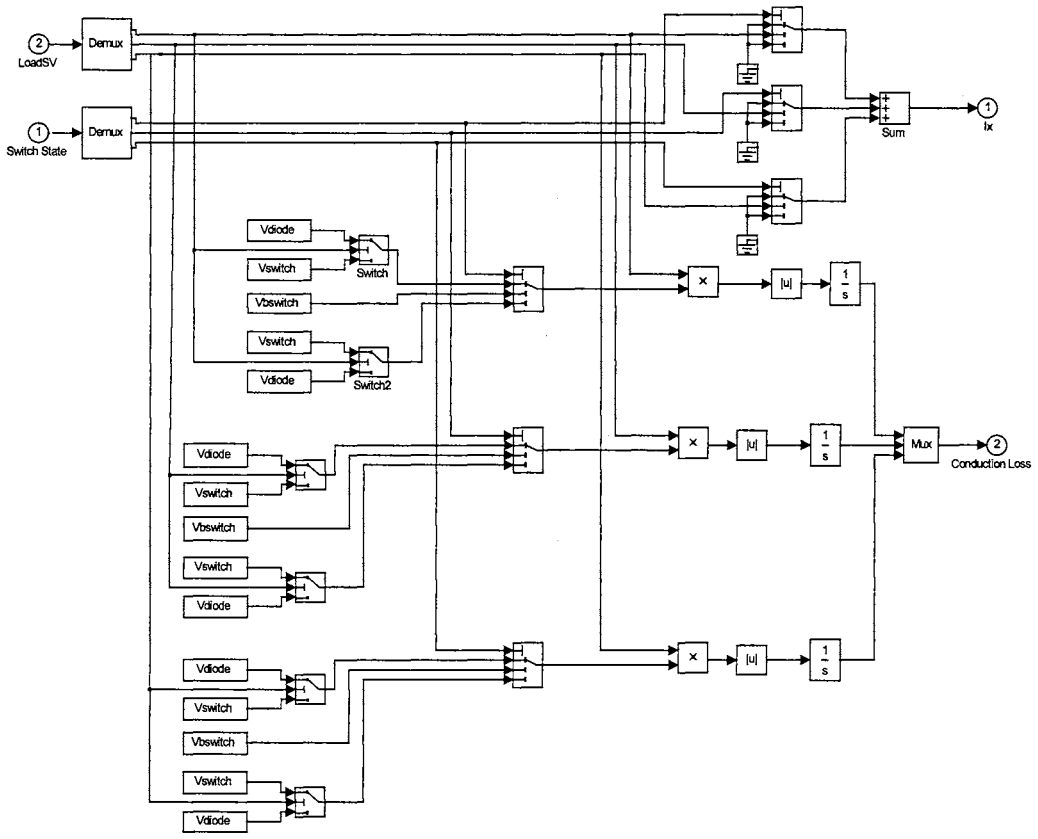

Figure B9. Internal view of the "Ix Generator" block

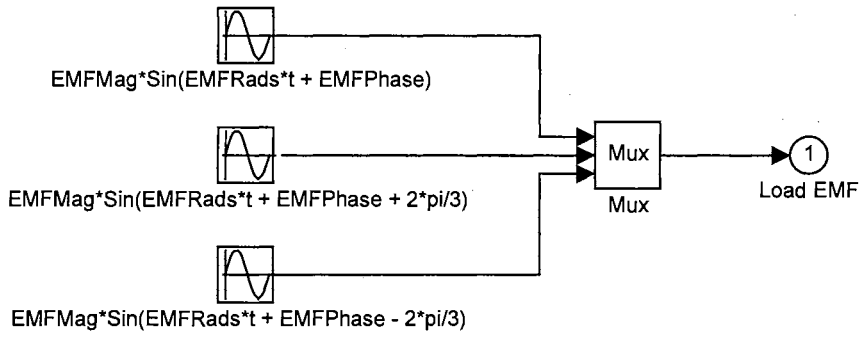

Figure B10. Internal view of the "Load Back EMF" block

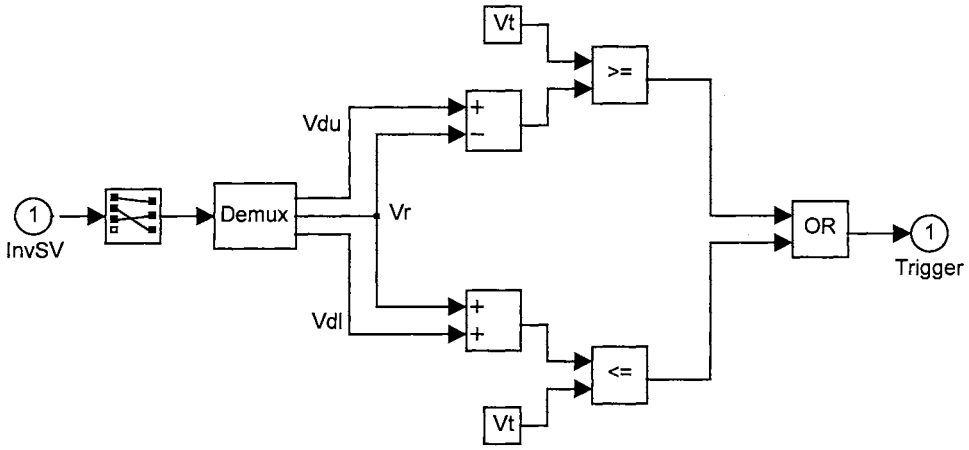

Figure B11. Internal view of the "Next State Trigger" block

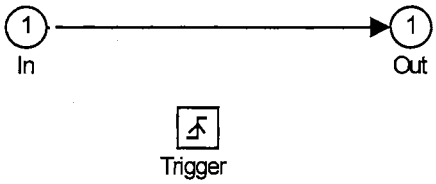

Figure B12. Internal view of "S & H" block

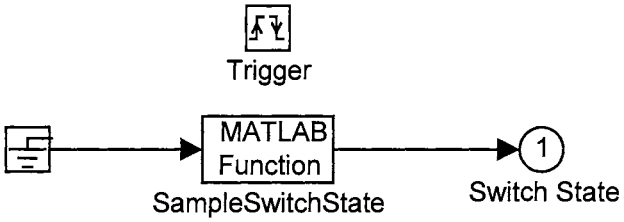

Figure B13. Internal view of the "Sample Switch State" block

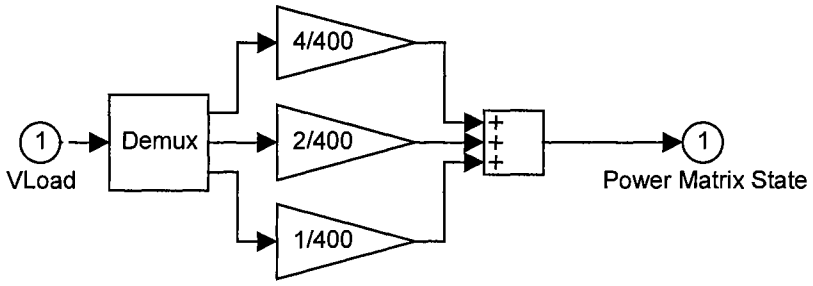

Figure B14. Internal view of the "State Decode" block

B.5 SIMULINK Block Diagrams Unique to the PI Current Control Configuration

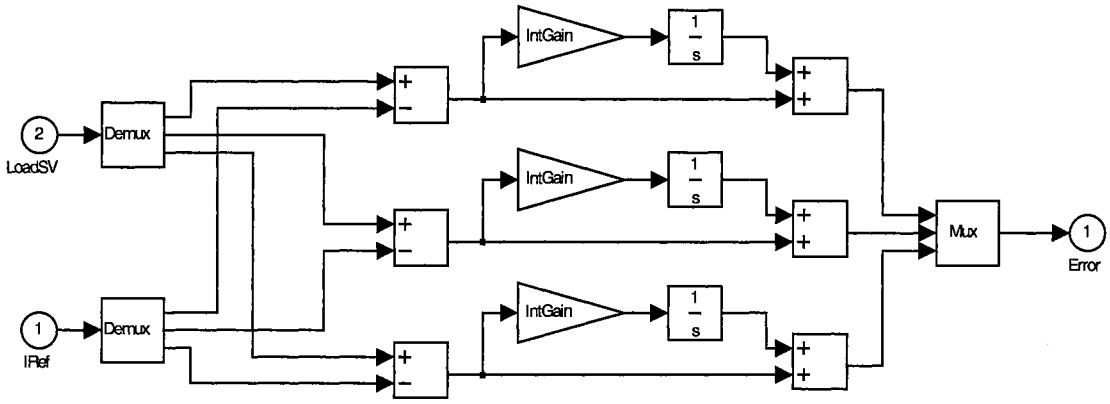

Figure B15. Internal view of the "Load Error" block used in the PI current control implementation

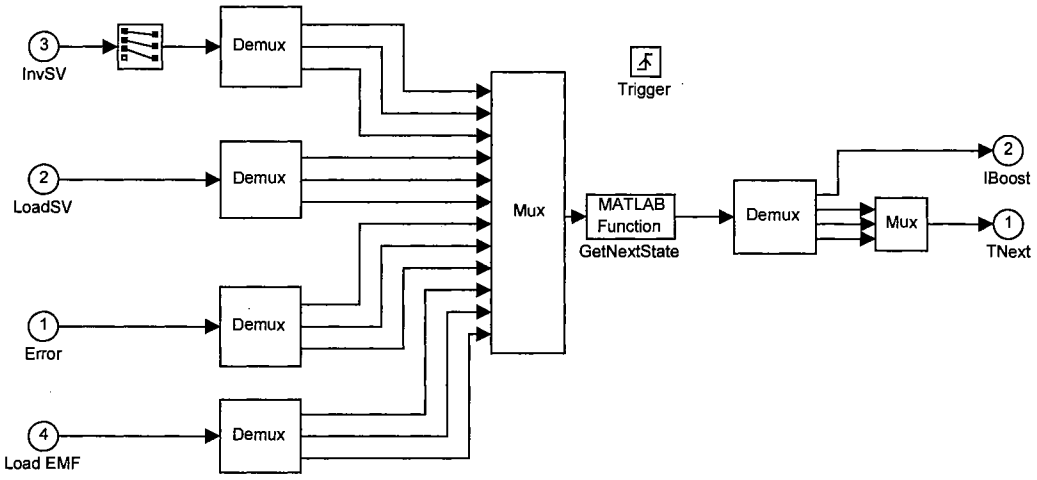

Figure B16. Internal view of the "Next State" block used in the PI current control implementation

B.6 SIMULINK Block Diagrams Unique to the Cost Function

Current Control Configuration

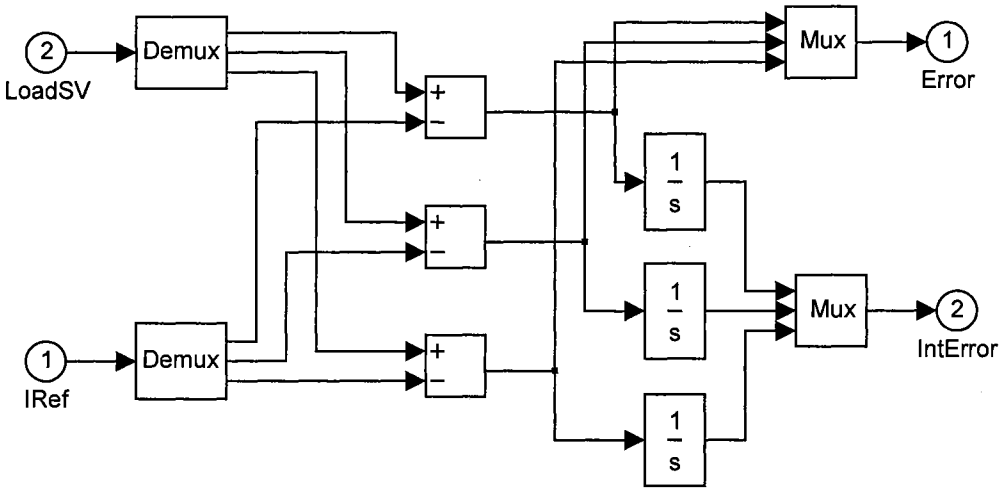

Figure B17. Internal view of the "Load Error" block used in the Cost Function Current Control implementation

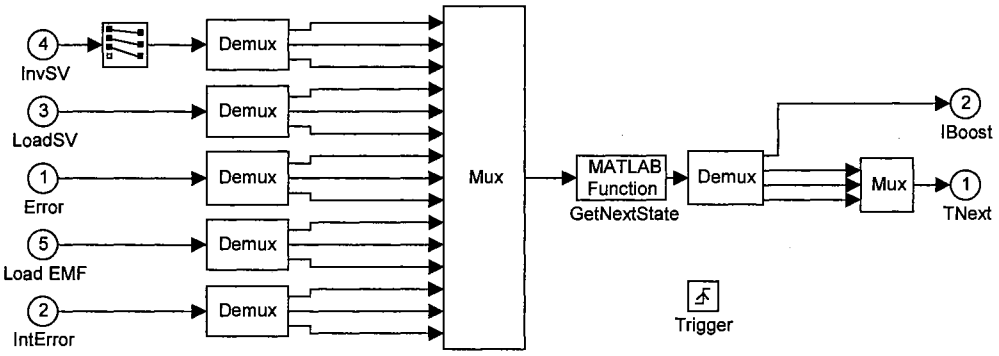

Figure B18. Internal view of the "Next State" block used in the Cost Function Current Control implementation

B.7 MATLAB Source Code Listings Unique to the PI

Current Control Configuration

B7.1 Init.m

```
clear
global OverrideTol PlotDelay PlotPeriod Vs Q EFixed I0 VDividerTol
global IBoostInit S Lr Cr Cdu Cdl Toff Vdiode Vswitch Vbswitch Rr
global Rs Ls Vt IRated  EMFPhase EMFMag IRef LoadRads EMFRads TNext
global LoadInitA LoadInitB IntLimit IntGain FixedLoad
FixedLoad = 1;
FixedBoost = 5;
VLine = 240;
OverrideTol = 1.0;
OutputFrequency = 60;
NominalFrequency = 60;
FileSampleTime = 5.0e-7;
PlotDelay = 1.0e-4;
PlotPeriod = 1.0/OutputFrequency;
Cdl = 500e-6;
Cdu = 500e-6;
Cr = 2.0e-6;
Lr = 2.0e-6;
IRated = 100;
IRef = 100;
EMFPhase = -0.6435;
IntGain = 10000;
IntLimit = 1;
IrInit = 0;
LoadInitA = 0;
LoadRads = 2*pi*OutputFrequency;
Ls = 1.59e-3;
Rs = .2;
S = [3 3 3];
TNext = [1 1 1];
Toff = 750e-9;
Q = 100;
Vs = 400;
I0 = (Vs/2)*sqrt(Cr/Lr);
VdlInit = Vs/2;
VduInit = Vs/2;
Vt = 5;
Vdiode = 1.7;
VDividerTol = 0.5;
Vswitch = 2.3;
EMFRads = 2*pi*OutputFrequency;
LoadInitB = IRef*sqrt(3)/2;
RefRads = 2*pi*OutputFrequency;
Rr = (1.0/(2*pi*Q)) * sqrt(Lr/Cr);
Vbswitch = Vswitch + 2 * Vdiode;
VrInit = Vs/2;
EMFMag = 141.9;
```

```
EMFMag = EMFMag*OutputFrequency/NominalFrequency
Leq = 1.5 * Ls;
Lp = (Lr * Leq) / (Lr + Leq);
Rhol = Lp / Leq;
%-----------------------------------------------------------------------
% If the FixedLoad flag is set, indicating that the worst case estimate
% of load interaction with the resonant link is used instead of a
% real time estimate, the fixed boost energy must be increased to
% account for the worst possible case of the load interfering with the
% resonant circuit.
%-----------------------------------------------------------------------
ILVD = real(sqrt((Cr/Lp)*(2.0*((sqrt(3)*EMFMag+Vs-Vs/2)*Rhol*(Vs)))))
if FixedLoad == 0
    EFixed = 0.5*Lr*(FixedBoost*FixedBoost + ILVD*ILVD);
else
    EFixed = 0.5*Lr*(FixedBoost*FixedBoost);
end
IBoostInit = IRated+FixedBoost +
             (Lr/(2.0*Q))*(IRated*IRated+(4.0*I0*IRated/pi)+0.5*I0*I0);
%=======================================================================
% Init.m ends.
%=======================================================================
```

B7.2 GetNextState.m

```
function [Result] = GetNextState(u)
global OverrideHighU OverrideHighL OverrideTol Vs Tto IRef I0 EFixed
global VDividerTol S TNext Ls Rs Lr Cr Cdu Cdl FixedBoost IRated Q
global Toff MatchFlag FixedLoad
%=======================================================================
%
% u(1) -> Vdu
%
% u(2) -> Vdl
%
% u(3) -> Vr
%
% u(4) -> Ia
%
% u(5) -> Ib
%
% u(6) -> Ic
%
% u(7) -> ErrorA
%
% u(8) -> ErrorB
%
% u(9) -> ErrorC
%
% u(10) -> Ea
%
% u(11) -> Eb
%
% u(12) -> Ec
%=======================================================================
```

```
Vdu    = u(1);
Vdl    = u(2);
Vr     = u(3);
Ia     = u(4);
Ib     = u(5);
Ic     = u(6);
ErrorA = u(7);
ErrorB = u(8);
ErrorC = u(9);
Ea   = u(10);
Eb   = u(11);
Ec   = u(12);
%-------------------------------------------------------------------------
% Get the switch states that will exist when the next L mode is
% entered.
%-------------------------------------------------------------------------
if Vr > 0
    if S(1) == 1
        SS(1) = 1;
    else
        SS(1) = 3;
    end
    if S(2) == 1
        SS(2) = 1;
    else
        SS(2) = 3;
    end
    if S(3) == 1
        SS(3) = 1;
    else
        SS(3) = 3;
    end
else
    if S(1) == 3
        SS(1) = 3;
    else
        SS(1) = 1;
    end
    if S(2) == 3
        SS(2) = 3;
    else
        SS(2) = 1;
    end
    if S(3) == 3
        SS(3) = 3;
    else
        SS(3) = 1;
    end
end
%-------------------------------------------------------------------------
% Set TNext based on the integrated voltage error.
%-------------------------------------------------------------------------
TNext(1) = 0;
TNext(2) = 0;
TNext(3) = 0;
if Vr > 0
    if SS(1) == 3
```

```
        if ErrorA > 0
            TNext(1) = 1;
        end
    end
    if SS(2) == 3
        if ErrorB > 0
            TNext(2) = 1;
        end
    end
    if SS(3) == 3
        if ErrorC > 0
            TNext(3) = 1;
        end
    end
else
    if SS(1) == 1
        if ErrorA < 0
            TNext(1) = 1;
        end
    end
    if SS(2) == 1
        if ErrorB < 0
            TNext(2) = 1;
        end
    end
    if SS(3) == 1
        if ErrorC < 0
            TNext(3) = 1;
        end
    end
 end
%=========================================================================
% If the voltage divider node is seriously out of balance and the
% selected state change will likely just make things worse, override
% the state selection and make no state change.
%=========================================================================
if Vdu - Vdl >= OverrideTol
   %-----------------------------------------------------------------
   % Get the requested switched load current.
   %-----------------------------------------------------------------
   Ix = TNext(1)*Ia + TNext(2)*Ib + TNext(3)*Ic;
   %-----------------------------------------------------------------
   % If Ix <= 0, the requested transiton will help drive the error to
   % zero, so honor the request. However, if Ix > 0, allowing the
   % requested transition to execute will at least partially cancel out
   % any improvements that elevating the boost current will yield and
   % will make things worse of Ix is sufficiently large. Therefore, if
   % Ix > 0, disallow the requested transition.
   %-----------------------------------------------------------------
   if Ix > 0
      if Vdu - Vdl <= 1.5*OverrideTol
         if OverrideHighU == 0
            %-----------------------------------------------------------
            % Nullify the requested transiton.
            %-----------------------------------------------------------
            TNext(1) = 0;
            TNext(2) = 0;
```

```
            TNext(3) = 0;
         end
      else
         if Vdu - Vdl <= 2*OverrideTol
            if OverrideHighU < 2
               %-------------------------------------------------------
               % Nullify the requested transiton.
               %-------------------------------------------------------
               TNext(1) = 0;
               TNext(2) = 0;
               TNext(3) = 0;
            end
         else
            %-------------------------------------------------------
            % Nullify the requested transiton
            %-------------------------------------------------------
            TNext(1) = 0;
            TNext(2) = 0;
            TNext(3) = 0;
         end
         %-------------------------------------------------------
         % Increment the decimation counter and roll it over if it
         % exceeds 2.
         %-------------------------------------------------------
         if OverrideHighU < 2
            OverrideHighU = OverrideHighU + 1;
         else
            OverrideHighU = 0;
         end
      end
   end
   %-----------------------------------------------------------
   % Clear the decimation counter for the case where Vdl > Vdu.
   %-----------------------------------------------------------
   OverrideHighL = 0;
end
if Vdl - Vdu >= OverrideTol
   %-----------------------------------------------------------
   % Get the requested switched load current.
   %-----------------------------------------------------------
   Ix = TNext(1)*Ia + TNext(2)*Ib + TNext(3)*Ic;
   %-----------------------------------------------------------
   % If Ix >= 0, the requested transiton will help drive the error to
   % zero, so honor the request. However, if Ix < 0, allowing the
   % requested transition to execute will at least partially cancel
   % out any improvements that elevating the boost current will yield
   % and will make things worse if Ix is sufficiently large.
   % Therefore, if Ix < 0, disallow the requested transition.
   %-----------------------------------------------------------
   if Ix < 0
      if Vdl - Vdu <= 1.5*OverrideTol
         if OverrideHighL == 0
            %-------------------------------------------------------
            % Nullify the requested transiton.
            %-------------------------------------------------------
            TNext(1) = 0;
            TNext(2) = 0;
```

```
            TNext(3) = 0;
         end
      else
         if Vdl - Vdu <= 2*OverrideTol
            if OverrideHighL < 2
               %-------------------------------------------------------
               % Nullify the requested transiton.
               %-------------------------------------------------------
               TNext(1) = 0;
               TNext(2) = 0;
               TNext(3) = 0;
            end
         else
            %-------------------------------------------------------
            % Nullify the requested transiton.
            %-------------------------------------------------------
            TNext(1) = 0;
            TNext(2) = 0;
            TNext(3) = 0;
         end
         %-------------------------------------------------------
         % Increment the decimation counter and roll it over if it
         % exceeds 2.
         %-------------------------------------------------------
         if OverrideHighL < 2
            OverrideHighL = OverrideHighL + 1;
         else
            OverrideHighL = 0;
         end
      end
   end
   %-----------------------------------------------------------------
   % Clear the decimation counter for the case where Vdu > Vdl.
   %-----------------------------------------------------------------
   OverrideHighU = 0;
end
%=================================================================
% If the inverter is in a zero state and no transitions are set to
% occur, transition to the other zero state so that Lr can be
% initialized durring the next L mode.
%=================================================================
if Vr > 0
    if ((SS(1) + SS(2)+ SS(3)) == 9)
        if (TNext(1) + TNext(2) + TNext(3)) == 0
            TNext(1) = 1;
            TNext(2) = 1;
            TNext(3) = 1;
        end
    end
else
    if ((SS(1) + SS(2)+ SS(3)) == 3)
        if (TNext(1) + TNext(2) + TNext(3)) == 0
            TNext(1) = 1;
            TNext(2) = 1;
            TNext(3) = 1;
        end
    end
```

```
end
%=========================================================================
% Compute the required boost current.
%=========================================================================
%-------------------------------------------------------------------------
% Compute parameters unique to this function.
%-------------------------------------------------------------------------
Leq = 1.5 * Ls;
Lp = (Lr * Leq) / (Lr + Leq);
Rho1 = Lp / Leq;
%-------------------------------------------------------------------------
% Use the sign of Vr to determine VrInitial and VrFinal.
%-------------------------------------------------------------------------
if Vr > 0
    VrInitial = Vdu;
    VrFinal = - Vdl;
else
    VrInitial = - Vdl;
    VrFinal = Vdu;
end
%-------------------------------------------------------------------------
% If phase leg k will be connected to the upper rail during the
% upcoming transition, let Ut(k) = 1. Otherwise, let Ut(k) = 0.
%-------------------------------------------------------------------------
Ut = [0 0 0];
if SS(1) == 3
    if TNext(1) == 0
        Ut(1) = 1;
    end
end
if SS(2) == 3
    if TNext(2) == 0
        Ut(2) = 1;
    end
end
if SS(3) == 3
    if TNext(3) == 0
        Ut(3) = 1;
    end
end
%-------------------------------------------------------------------------
% There are three scenarios to consider:
%
% Case 0: None or all of the load phase terminals are transitioning
% during the upcomming T mode.
%
% Case 1: Exactly one of the load phase terminals is transitioning
% during the upcomming T mode.
%
% Case 2: Exactly two of the load phase legs are transitioning during
% the upcomming T mode.
%
% The equivalent load model parameters depend on whether one or two
% terminals are transitioning. If none are transitioning, imbalance in
% the voltage divider node potential still needs to be considered.
% To effectively remove the effect of the load in this case, set Leq
% equal to 1000H and Eeq equal to the potential of the voltage divider
```

```
% node.
%-------------------------------------------------------------------------
switch(TNext(1) + TNext(2) + TNext(3))
    %---------------------------------------------------------------------
    % Handle the case where either none or all load terminals are
    % transitioning.
    %---------------------------------------------------------------------
case {0, 3},
    Eeq = Vdl;
    Leq = 1000.0;
    Lp = (Lr * Leq) / (Lr + Leq);
    Rhol = Lp / Leq;
    %---------------------------------------------------------------------
    % Handle the case where exactly one load terminal is transitioning.
    %---------------------------------------------------------------------
case 1,
    if TNext(1) == 1
        Eeq = Ea + 1.5*Ia*Rs - 0.5*(Eb + Ec) + 0.5*(Vdu + Vdl)*(Ut(2) +
              Ut(3));
    elseif TNext(2) == 1
        Eeq = Eb + 1.5*Ib*Rs - 0.5*(Ea + Ec) + 0.5*(Vdu + Vdl)*(Ut(1) +
              Ut(3));
    else
        Eeq = Ec + 1.5*Ic*Rs - 0.5*(Ea + Eb) + 0.5*(Vdu + Vdl)*(Ut(1) +
              Ut(2));
    end
    %---------------------------------------------------------------------
    % Handle the case where exactly one of the load terminals is NOT
    % transitioning.
    %---------------------------------------------------------------------
case 2,
    if TNext(1) ~= 1
        Eeq = (Vdu + Vdl)*Ut(1) - Ea - 1.5*Ia*Rs + 0.5*(Eb + Ec);
    elseif TNext(2) ~= 1
        Eeq = (Vdu + Vdl)*Ut(2) - Eb - 1.5*Ib*Rs + 0.5*(Ea + Ec);
    else
        Eeq = (Vdu + Vdl)*Ut(3) - Ec - 1.5*Ic*Rs + 0.5*(Ea + Eb);
    end
end
%-------------------------------------------------------------------------
% Get Ix.
%-------------------------------------------------------------------------
Ix = TNext(1)*Ia + TNext(2)*Ib + TNext(3)*Ic;
%-------------------------------------------------------------------------
% Compute the boost energy associated with load effects and the voltage
% divider. If the FixedLoad flag is set, compensate only for the
% voltage divider node potential error. If FixedLoad is set, the value
% of Ifixed computed in init.m includes a current component capable of
% handling the worst case that could develop in terms of the load
% influencing the resonant circuit.
%-------------------------------------------------------------------------
if Vr > 0
   if FixedLoad == 0
      ILVD = real(sqrt((Cr/Lp)*(Vdl*Vdl - Vdu*Vdu + 2.0*(Eeq -
                  Vdl)*Rhol*(Vdu + Vdl))));
   else
      ILVD = real(sqrt((Cr/Lp)*(Vdl*Vdl - Vdu*Vdu)));
```

```
   end
else
   if FixedLoad == 0
      ILVD = real(sqrt((Cr/Lp)*(Vdu*Vdu - Vdl*Vdl - 2.0*(Eeq -
                  Vdl)*Rhol*(Vdl + Vdu))));
   else
      ILVD = real(sqrt((Cr/Lp)*(Vdu*Vdu - Vdl*Vdl)));
   end
end
ELVD = 0.5*Lr*ILVD*ILVD;
%-------------------------------------------------------------------------
% Compute the estimated disipated energy in the resonant circuit.
%-------------------------------------------------------------------------
if Vr > 0
   Edisp = (Lr/(2.0*Q))*(Ix*Ix - (4.0*I0*Ix/pi) + 0.5*I0*I0);
else
   Edisp = (Lr/(2.0*Q))*(Ix*Ix + (4.0*I0*Ix/pi) + 0.5*I0*I0);
end


%-------------------------------------------------------------------------
% Compute the total boost current.
%-------------------------------------------------------------------------
Eboost = ELVD + Edisp + EFixed;
IBoost = sqrt(2.0*Eboost/Lr);
%-------------------------------------------------------------------------
% Adjust for device turn-off effects.
%-------------------------------------------------------------------------
sin1 = sin(0.5*Toff*sqrt(1.0/(Lr*Cr)));
IBoost = (Vs*Toff/(4*Lr))*(sqrt(1 +
         4*Lr*IBoost*IBoost/(Vs*Vs*Cr*sin1*sin1)) - 1.0);
%-------------------------------------------------------------------------
% If the voltage divider is out of balance, adjust the boost current.
%-------------------------------------------------------------------------
if Vr >= 0
   if Vdu > Vs/2 + VDividerTol
      if Vdu - Vdl >= 0
         IBoost = max(IBoost,IRated);
      end
   end
else
   if Vdl > Vs/2 + VDividerTol
      if Vdu - Vdl < 0
         IBoost = max(IBoost,IRated);
      end
   end
end
%-------------------------------------------------------------------------
% Combine the results and return.
%-------------------------------------------------------------------------
Result(1) = IBoost;
Result(2) = TNext(1);
Result(3) = TNext(2);
Result(4) = TNext(3);
%=========================================================================
% Function GetNextState ends.
%=========================================================================
```

B.8 MATLAB Source Code Listings Unique to the Cost Function

Current Control Configuration

B8.1 Init.m

```
clear
global OverrideHighU OverrideHighL OverrideTol S PlotDelay PlotPeriod
global Vs Q Gamma EFixed I0 VDividerTol IBoostInit S Lr Cr Cdu Cdl
global Toff Vdiode Vswitch Vbswitch Rr Rs Ls Vt IRated  EMFPhase EMFMag
global IRef LoadRads EMFRads TNext LoadInitA LoadInitB IntLimit IntGain
global FixedLoad
FixedLoad = 1;
FixedBoost = 5;
OverrideHighU = 0;
OverrideHighL = 0;
OverrideTol = 1.5;
OutputFrequency = 60;
NominalFrequency = 60;
FileSampleTime = 5.0e-7;
PlotDelay = 1.0e-4;
PlotPeriod = 1.0/OutputFrequency;
Cdl = 500e-6;
Cdu = 500e-6;
Cr = 2.0e-6; ;
Gamma = 0.025
IRated = 100;
IRef = 100;
EMFMag = 141.9 * OutputFrequency/NominalFrequency;
EMFPhase = -.6435;
IntGain = 10000;
IntLimit = 1;
IrInit = 0;
S = [3 3 3];
LoadInitA = 0;
LoadRads = 2*pi*OutputFrequency;
Lr = 2.0e-6;
Ls = 1.59e-3;
Rs = .2;
S = [3 3 3];
TNext = [1 1 1];
Toff = 750e-9;
Q = 100;
Vs = 400;
I0 = (Vs/2)*sqrt(Cr/Lr);
VdlInit = Vs/2;
VduInit = Vs/2;
Vt = 5;
Vdiode = 1.7;
VDividerTol = 0.5;
Vswitch = 2.3;
EMFRads = 2*pi*OutputFrequency;
LoadInitB = IRef*sqrt(3)/2;
```

```
RefRads = 2*pi*OutputFrequency;
Rr = (1.0/(2*pi*Q)) * sqrt(Lr/Cr);
Vbswitch = Vswitch + 2 * Vdiode;
VrInit = Vs/2;
Leq = 1.5 * Ls;
Lp = (Lr * Leq) / (Lr + Leq);
Rhol = Lp / Leq;
ILVD = real(sqrt((Cr/Lp)*( 2.0*((sqrt(3)*EMFMag + Vs -
            Vs/2)*Rhol*(Vs)))))
if FixedLoad == 0
   EFixed = 0.5*Lr*(FixedBoost*FixedBoost + ILVD*ILVD);
else
   EFixed = 0.5*Lr*(FixedBoost*FixedBoost);
end
IBoostInit = IRated+FixedBoost+(Lr/(2.0*Q))*
             (IRated*IRated+(4.0*I0*IRated/pi)+0.5*I0*I0);

%=========================================================================
% Init.m ends
%=========================================================================
```

B8.2 NextState.m

```
function [Result] = GetNextState(u)
global OverrideHighL OverrideHighU OverrideTol Vs Toff I0 EFixed
global VDividerTol S TNext Ls Rs Lr Cr Cdu Cdl IRated Q FixedLoad
%=========================================================================
%
% u(1) -> Vdu
%
% u(2) -> Vdl
%
% u(3) -> Vr
%
% u(4) -> Ia
%
% u(5) -> Ib
%
% u(6) -> Ic
%
% u(7) -> ErrorA
%
% u(8) -> ErrorB
%
% u(9) -> ErrorC
%
% u(10) -> Ea
%
% u(11) -> Eb
%
% u(12) -> Ec
%
% u(13) -> IntErrorA
%
% u(14) -> IntErrorB
```

```
%
% u(15) -> IntErrorC
%
%=========================================================================
Vdu    = u(1);
Vdl    = u(2);
Vr     = u(3);
Ia     = u(4);
Ib     = u(5);
Ic     = u(6);
ErrorA = u(7);
ErrorB = u(8);
ErrorC = u(9);
Ea   = u(10);
Eb   = u(11);
Ec   = u(12);
IntErrorA = u(13);
IntErrorB = u(14);
IntErrorC = u(15);
Error(1) = ErrorA;
Error(2) = ErrorB;
Error(3) = ErrorC;
EMF(1) = Ea;
EMF(2) = Eb;
EMF(3) = Ec;
IntError(1) = IntErrorA;
IntError(2) = IntErrorB;
IntError(3) = IntErrorC;

%-------------------------------------------------------------------------
% Get the switch states that will exist when the next L mode is
% entered.
%-------------------------------------------------------------------------
if Vr > 0
    if S(1) == 1
        SS(1) = 1;
        PhaseState(1) = 0;
    else
        SS(1) = 3;
        PhaseState(1) = 1;
    end
    if S(2) == 1
        SS(2) = 1;
        PhaseState(2) = 0;
    else
        SS(2) = 3;
        PhaseState(2) = 1;
    end
    if S(3) == 1
        SS(3) = 1;
        PhaseState(3) = 0;
    else
        SS(3) = 3;
        PhaseState(3) = 1;
    end
else
    if S(1) == 3
```

```
        SS(1) = 3;
        PhaseState(1) = 1;
    else
        SS(1) = 1;
        PhaseState(1) = 0;
    end
    if S(2) == 3
        SS(2) = 3;
        PhaseState(2) = 1;
    else
        SS(2) = 1;
        PhaseState(2) = 0;
    end
    if S(3) == 3
        SS(3) = 3;
        PhaseState(3) = 1;
    else
        SS(3) = 1;
        PhaseState(3) = 0;
    end
end

%-------------------------------------------------------------------------
% Apply a cost function to determine the next state based on the
% integrated load current error.
%-------------------------------------------------------------------------
PMState = PhaseState(1) * 4 + PhaseState(2) * 2 + PhaseState(3);
switch PMState
case 0,
    CandidateNextState =     [0 1 1 1 1 1 1 1];
case 1,
    if Vr > 0,
        CandidateNextState = [1 1 0 0 0 0 0 0];
    else
        CandidateNextState = [0 1 0 1 0 1 0 1];
    end
case 2,
    if Vr > 0,
        CandidateNextState = [1 0 1 0 0 0 0 0];
    else
        CandidateNextState = [0 0 1 1 0 0 1 1];
    end
case 3,
    if Vr > 0,
        CandidateNextState = [1 1 1 1 0 0 0 0];
    else
        CandidateNextState = [0 0 0 1 0 0 0 1];
    end
case 4,
    if Vr > 0,
        CandidateNextState = [1 0 0 0 1 0 0 0];
    else
        CandidateNextState = [0 0 0 0 1 1 1 1];
    end
case 5,
    if Vr > 0,
        CandidateNextState = [1 1 0 0 1 1 0 0];
```

```
    else
        CandidateNextState = [0 0 0 0 0 1 0 1];
    end
case 6,
    if Vr > 0,
        CandidateNextState = [1 0 1 0 1 0 1 0];
    else
        CandidateNextState = [0 0 0 0 0 0 1 1];
    end
case 7,
        CandidateNextState = [1 1 1 1 1 1 1 0];
end

NextPMState = OptimalNextState(PMState,CandidateNextState,
                               Error,IntError, EMF);
switch NextPMState,
case 0,
    PNext = [0, 0, 0];
case 1,
    PNext = [0, 0, 1];
case 2,
    PNext = [0 ,1, 0];
case 3,
    PNext = [0 ,1 ,1];
case 4,
    PNext = [1, 0, 0];
case 5,
    PNext = [1, 0, 1];
case 6,
    PNext = [1 ,1, 0];
case 7,
    PNext = [1 ,1, 1];
end

if PNext(1) ~= PhaseState(1)
    TNext(1) = 1;
else
    TNext(1) = 0;
end

if PNext(2) ~= PhaseState(2)
    TNext(2) = 1;
else
    TNext(2) = 0;
end

if PNext(3) ~= PhaseState(3)
    TNext(3) = 1;
else
    TNext(3) = 0;
end
%=========================================================================
% If the voltage divider node is seriously out of balance and the
% selected state change will likely just make things worse, override
% the state selection and make no state change.
%=========================================================================
if Vdu - Vdl >= OverrideTol
```

```
   %-------------------------------------------------------------------
   % Get the requested switched load current.
   %-------------------------------------------------------------------
   Ix = TNext(1)*Ia + TNext(2)*Ib + TNext(3)*Ic;
   %-------------------------------------------------------------------
   % If Ix <= 0, the requested transiton will help drive the error to
   % zero, so honor the request. However, if Ix > 0, allowing the
   % requested transition to execute will at least partially cancel
   % out any improvements that elevating the boost current will yield
   % and will make things worse of Ix is sufficiently large.
   % Therefore, if Ix > 0, disallow the requested transition.
   %-------------------------------------------------------------------
   if Ix > 0
      if Vdu - Vdl <= 1.5*OverrideTol
         if OverrideHighU == 0
            %-------------------------------------------------------
            % Nullify the requested transiton.
            %-------------------------------------------------------
            TNext(1) = 0;
            TNext(2) = 0;
            TNext(3) = 0;
         end
      else
         if Vdu - Vdl <= 2*OverrideTol
            if OverrideHighU < 2
               %-------------------------------------------------------
               % Nullify the requested transiton.
               %-------------------------------------------------------
               TNext(1) = 0;
               TNext(2) = 0;
               TNext(3) = 0;
            end
         else
            %-------------------------------------------------------
            % Nullify the requested transiton
            %-------------------------------------------------------
            TNext(1) = 0;
            TNext(2) = 0;
            TNext(3) = 0;
         end
         %-------------------------------------------------------
         % Increment the decimation counter and roll it over if it
         % exceeds 2.
         %-------------------------------------------------------
         if OverrideHighU < 2
            OverrideHighU = OverrideHighU + 1;
         else
            OverrideHighU = 0;
         end
      end
   end
   %-------------------------------------------------------------------
   % Clear the decimation counter for the case where Vdl > Vdu.
   %-------------------------------------------------------------------
   OverrideHighL = 0;
end
if Vdl - Vdu >= OverrideTol
```

```
   %-------------------------------------------------------------------
   % Get the requested switched load current.
   %-------------------------------------------------------------------
   Ix = TNext(1)*Ia + TNext(2)*Ib + TNext(3)*Ic;
   %-------------------------------------------------------------------
   % If Ix >= 0, the requested transiton will help drive the error to
   % zero, so honor the request. However, if Ix < 0, allowing the
   % requested transition to execute will at least partially cancel
   % out any improvements that elevating the boost current will yield
   % and will make things worse of Ix is sufficiently large.
   % Therefore, if Ix < 0, disallow the requested transition.
   %-------------------------------------------------------------------
   if Ix < 0
      if Vdl - Vdu <= 1.5*OverrideTol
         if OverrideHighL == 0
            %-------------------------------------------------------
            % Nullify the requested transiton.
            %-------------------------------------------------------
            TNext(1) = 0;
            TNext(2) = 0;
            TNext(3) = 0;
         end
      else
         if Vdl - Vdu <= 2*OverrideTol
            if OverrideHighL < 2
               %-------------------------------------------------------
               % Nullify the requested transiton
               %-------------------------------------------------------
               TNext(1) = 0;
               TNext(2) = 0;
               TNext(3) = 0;
            end
         else
            %-------------------------------------------------------
            % Nullify the requested transiton
            %-------------------------------------------------------
            TNext(1) = 0;
            TNext(2) = 0;
            TNext(3) = 0;
         end
         %-------------------------------------------------------------
         % Increment the decimation counter and roll it over if it
         % exceeds 2.
         %-------------------------------------------------------------
         if OverrideHighL < 2
            OverrideHighL = OverrideHighL + 1;
         else
            OverrideHighL = 0;
         end
      end
   end
   %-------------------------------------------------------------------
   % Clear the decimation counter for the case where Vdu > Vdl.
   %-------------------------------------------------------------------
   OverrideHighU = 0;
end
%-------------------------------------------------------------------
```

```
% If the inverter is in a zero state and no transitions are set to
% occur, transition to the other zero state so that Lr can be
% initialized durring the next L mode.
%-----------------------------------------------------------------------
if Vr > 0
    if ((SS(1) + SS(2)+ SS(3)) == 9)
        if (TNext(1) + TNext(2) + TNext(3)) == 0
            TNext(1) = 1;
            TNext(2) = 1;
            TNext(3) = 1;
        end
    end
else
    if ((SS(1) + SS(2)+ SS(3)) == 3)
        if (TNext(1) + TNext(2) + TNext(3)) == 0
            TNext(1) = 1;
            TNext(2) = 1;
            TNext(3) = 1;
        end
    end
end
%=======================================================================
% Compute the required boost current.
%=======================================================================
%-----------------------------------------------------------------------
% Compute parameters unique to this function.
%-----------------------------------------------------------------------
Leq = 1.5 * Ls;
Lp = (Lr * Leq) / (Lr + Leq);
Rhol = Lp / Leq;
%-----------------------------------------------------------------------
% Use the sign of Vr to determine VrInitial and VrFinal.
%-----------------------------------------------------------------------
if Vr > 0
    VrInitial = Vdu;
    VrFinal = - Vdl;
else
    VrInitial = - Vdl;
    VrFinal = Vdu;
end
%-----------------------------------------------------------------------
% If phase leg k will be connected to the upper rail during the
% upcomming transition, let Ut(k) = 1. Otherwise, let Ut(k) = 0.
%-----------------------------------------------------------------------
Ut = [0 0 0];
if SS(1) == 3
    if TNext(1) == 0
        Ut(1) = 1;
    end
end
if SS(2) == 3
    if TNext(2) == 0
        Ut(2) = 1;
    end
end
if SS(3) == 3
    if TNext(3) == 0
```

```
        Ut(3) = 1;
    end
end
%-------------------------------------------------------------------------
% There are three scenarios to consider:
%
% Case 0: None are all of the load phase terminals are transitioning
%         during the upcomming T mode.
%
% Case 1: Exactly one of the load phase terminals is transitioning
%         during the upcomming T mode.
%
% Case 2: Exactly two of the load phase legs are transitioning
%         during the upcomming T mode.
%
% The equivalent load calculation depends on whether one or two
% terminals are transitioning. If none are transitioning, imbalance
% in Vdu and Vdl still need to be considered. To effectively remove
% the effect of the load in this case Leq is set equal to 1000H
% and Eeq is set equal to the voltage divider node potential.
%-------------------------------------------------------------------------

switch(TNext(1) + TNext(2) + TNext(3))
    %---------------------------------------------------------------------
    % Handle the case where either none or all load terminals are
    % transitioning.
    %---------------------------------------------------------------------
case {0, 3},
    Eeq = Vdl;
    Leq = 1000.0;
    Lp = (Lr * Leq) / (Lr + Leq);
    w = 1.0 / sqrt(Cr * Lp);
    Rhol = Lp / Leq;
    %---------------------------------------------------------------------
    % Handle the case where exactly one load terminal is
    % transitioning.
    %---------------------------------------------------------------------
case 1,
    if TNext(1) == 1
        Eeq = Ea + 1.5*Ia*Rs - 0.5*(Eb + Ec) + 0.5*(Vdu + Vdl)*(Ut(2) +
Ut(3));
    elseif TNext(2) == 1
        Eeq = Eb + 1.5*Ib*Rs - 0.5*(Ea + Ec) + 0.5*(Vdu + Vdl)*(Ut(1) +
Ut(3));
    else
        Eeq = Ec + 1.5*Ic*Rs - 0.5*(Ea + Eb) + 0.5*(Vdu + Vdl)*(Ut(1) +
Ut(2));
    end
    %---------------------------------------------------------------------
    % Handle the case where exactly one of the load terminals is NOT
    % transitioning.
    %---------------------------------------------------------------------
case 2,
    if TNext(1) ~= 1
        Eeq = (Vdu + Vdl)*Ut(1) - Ea - 1.5*Ia*Rs + 0.5*(Eb + Ec);
    elseif TNext(2) ~= 1
        Eeq = (Vdu + Vdl)*Ut(2) - Eb - 1.5*Ib*Rs + 0.5*(Ea + Ec);
```

```
    else
        Eeq = (Vdu + Vdl)*Ut(3) - Ec - 1.5*Ic*Rs + 0.5*(Ea + Eb);
    end
end
%-------------------------------------------------------------------
% Get Ix.
%-------------------------------------------------------------------
Ix = TNext(1)*Ia + TNext(2)*Ib + TNext(3)*Ic;
%-------------------------------------------------------------------
% Compute the boost energy associated with load effects and the voltage
% divider. If the FixedLoad flag is set, compensate only for the
% voltage divider node potential error. If FixedLoad is set, the value
% of Ifixed computed in init.m includes a current component capable of
% handling the worst case that could develop in terms of the load
% influencing the resonant circuit.
%-------------------------------------------------------------------
if Vr > 0
   if FixedLoad == 0
      ILVD = real(sqrt((Cr/Lp)*(Vdl*Vdl - Vdu*Vdu + 2.0*(Eeq -
                  Vdl)*Rhol*(Vdu + Vdl))));
   else
      ILVD = real(sqrt((Cr/Lp)*(Vdl*Vdl - Vdu*Vdu)));
   end
else
   if FixedLoad == 0
      ILVD = real(sqrt((Cr/Lp)*(Vdu*Vdu - Vdl*Vdl - 2.0*(Eeq -
                  Vdl)*Rhol*(Vdl + Vdu))));
   else
      ILVD = real(sqrt((Cr/Lp)*(Vdu*Vdu - Vdl*Vdl)));
   end
end
ELVD = 0.5*Lr*ILVD*ILVD;
%-------------------------------------------------------------------
% Compute the estimated disipated energy in the resonant circuit.
%-------------------------------------------------------------------
if Vr > 0
   Edisp = (Lr/(2.0*Q))*(Ix*Ix - (4.0*I0*Ix/pi) + 0.5*I0*I0);
else
   Edisp = (Lr/(2.0*Q))*(Ix*Ix + (4.0*I0*Ix/pi) + 0.5*I0*I0);
end
%-------------------------------------------------------------------
% Compute the total boost current.
%-------------------------------------------------------------------
Eboost = ELVD + Edisp + EFixed;
IBoost = sqrt(2.0*Eboost/Lr);
%-------------------------------------------------------------------
% Adjust for device turn-off effects.
%-------------------------------------------------------------------
sin1 = sin(0.5*Toff*sqrt(1.0/(Lr*Cr)));
IBoost = (Vs*Toff/(4*Lr))*(sqrt(1 +
4*Lr*IBoost*IBoost/(Vs*Vs*Cr*sin1*sin1)) - 1.0)
%-------------------------------------------------------------------
% If the voltage divider is out of balance, adjust the boost current.
%-------------------------------------------------------------------
if Vr >= 0
   if Vdu > Vs/2 + VDividerTol
      if Vdu - Vdl >= 0
```

```
            IBoost = max(IBoost,IRated);
        end
    end
else
    if Vdl > Vs/2 + VDividerTol
        if Vdu - Vdl < 0
            IBoost = max(IBoost,IRated);
        end
    end
end
%-------------------------------------------------------------------------
% Combine the results and return
%-------------------------------------------------------------------------
Result(1) = IBoost;
Result(2) = TNext(1);
Result(3) = TNext(2);
Result(4) = TNext(3);
%=========================================================================
% Function GetNextState ends.
%=========================================================================
```

B8.3 OptimalNextState.m

```
function [NextState] = OptimalNextState(CurrentState, CandidateStates,
Error, IntError, EMF);
global Ls Rs Lr Cr Vs Gamma
T = 2 * pi * sqrt(Lr * Cr);
%=========================================================================
% Get the (U,V) coordinates of the current state output voltage,
% Current Error, and EMF.
%=========================================================================
V1 = GetUVVoltage(CurrentState, Vs);
ErrorUV = [Error(1), (2 / sqrt(3)) * Error(2)];
E = [EMF(1), (2 / sqrt(3)) * EMF(2)];
IntErrorUV = [IntError(1), (2 / sqrt(3)) * IntError(2)];
%=========================================================================
% Find the pseudo-optimal state for the next half-cycle of the
% auxiliary link.
%=========================================================================
BestResidualIntError = 1.0e38;
NextState = CurrentState;
for i = 1:8,
    if CandidateStates(i) == 1
        V2 = GetUVVoltage(i-1, Vs);
        Vavg = (V1 + V2)/2;
        %ErrorUV = ErrorUV + 0.05*IntErrorUV/(T/2);
        DeltaInt = ((Vavg - E)/(3 * Ls / 2))* (T / 2);
        EUV(1) = ErrorUV(1) + Gamma *  IntErrorUV(1)/(T/2);
        EUV(2) = ErrorUV(2) + Gamma *  IntErrorUV(2)/(T/2);
        EndingIntError = EUV + DeltaInt;
        EndError = EndingIntError.*EndingIntError;
        CandidateResidualIntError = EndError(1)*EndError(1) +
                                    EndError(2)*EndError(2);
        if CandidateResidualIntError < BestResidualIntError
```

```
            BestResidualIntError = CandidateResidualIntError;
            NextState = i-1;
        end
    end
end
%=========================================================================
% Function OptimalNextState ends.
%=========================================================================
```

B.9 MATLAB Source Code Listings Common to PI and Cost Function Current Control Configurations

B9.1 On_LL.m

```
function On_LL()
global S
%=========================================================================
% Set the switch states of any transitioning phase legs to L (i.e. 1).
%=========================================================================
if S(1) == 2
    S(1) = 1;
end
if S(2) == 2
    S(2) = 1;
end
if S(3) == 2
    S(3) = 1;
end
%=========================================================================
% Function On_LL ends.
%=========================================================================
```

B9.2 On_LU.m

```
function On_LU()
global S
%=========================================================================
% Set the switch states of any transitioning phase legs to U (i.e. 3).
%=========================================================================
if S(1) == 2
    S(1) = 3;
end
if S(2) == 2
    S(2) = 3;
end
if S(3) == 2
    S(3) = 3;
end
%=========================================================================
% Function On_LU ends.
%=========================================================================
```

B9.3 On_TL.m

```
function On_TL()
global S TNext
%=========================================================================
% Set the switch states of any transitioning phase legs to T (i.e. 2).
%=========================================================================
if TNext(1) == 1
    S(1) = 2;
end
if TNext(2) == 1
    S(2) = 2;
end
if TNext(3) == 1
    S(3) = 2;
end
%=========================================================================
% Function On_TL ends.
%=========================================================================
```

B9.4 On_TU.m

```
function On_TU()
global S TNext
%=========================================================================
% Set the switch states of any transitioning phase legs to T (i.e. 2).
%=========================================================================
if TNext(1) == 1
    S(1) = 2;
end
if TNext(2) == 1
    S(2) = 2;
end
if TNext(3) == 1
    S(3) = 2;
end
%=========================================================================
% Function On_TU ends.
%=========================================================================
```

B9.5 SampleSwitchState.m

```
function [Result] = SampleSwitchState(u)
global S
Result(1) = S(1);
Result(2) = S(2);
Result(3) = S(3);
%=========================================================================
% Function SampleSwitchState ends.
%=========================================================================
```

APPENDIX C

SPRDL INVERTER STATE-VARIABLE SIMULATION MODEL

C.1 Top Level SIMULINK Block Diagrams Used to Simulate the SPRDL Inverter

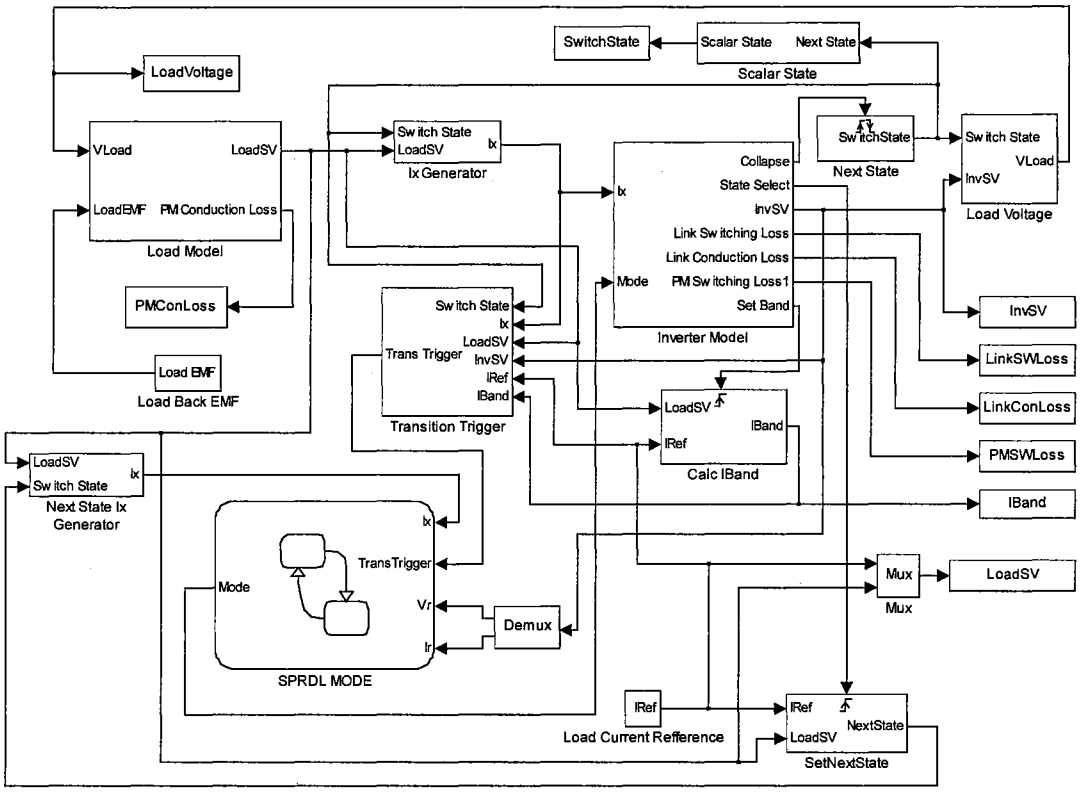

Figure C1. Top level block diagram of the SPRDL inverter state-variable simulation model

C.2 STATEFLOW Block Diagram

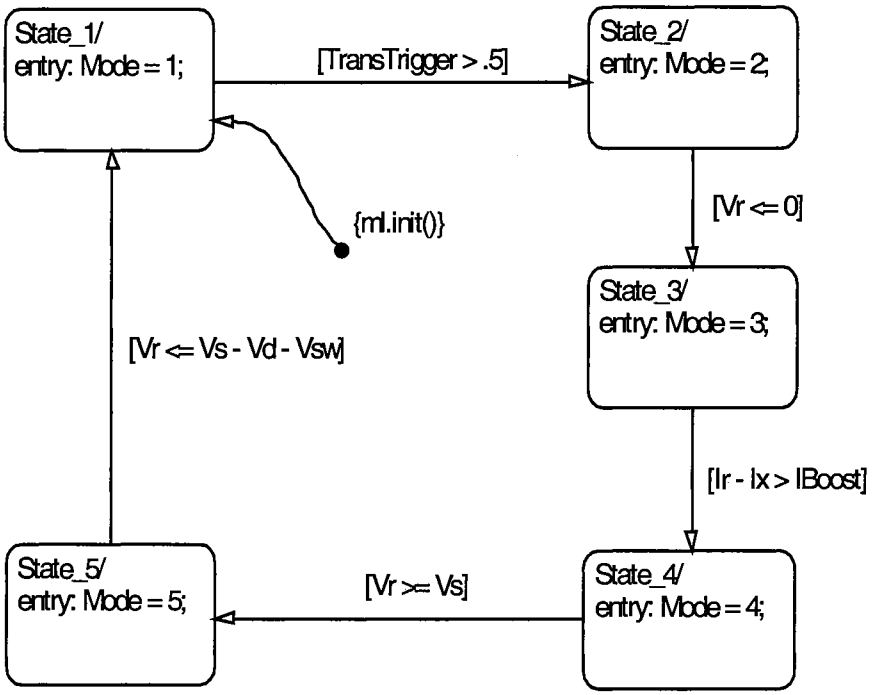

Figure C2. Internal view of the "SPRDL Mode" block constructed using STATEFLOW

C.3 Internal Views of SIMULINK Block Diagrams Used to Model the SPRDL Inverter and Load

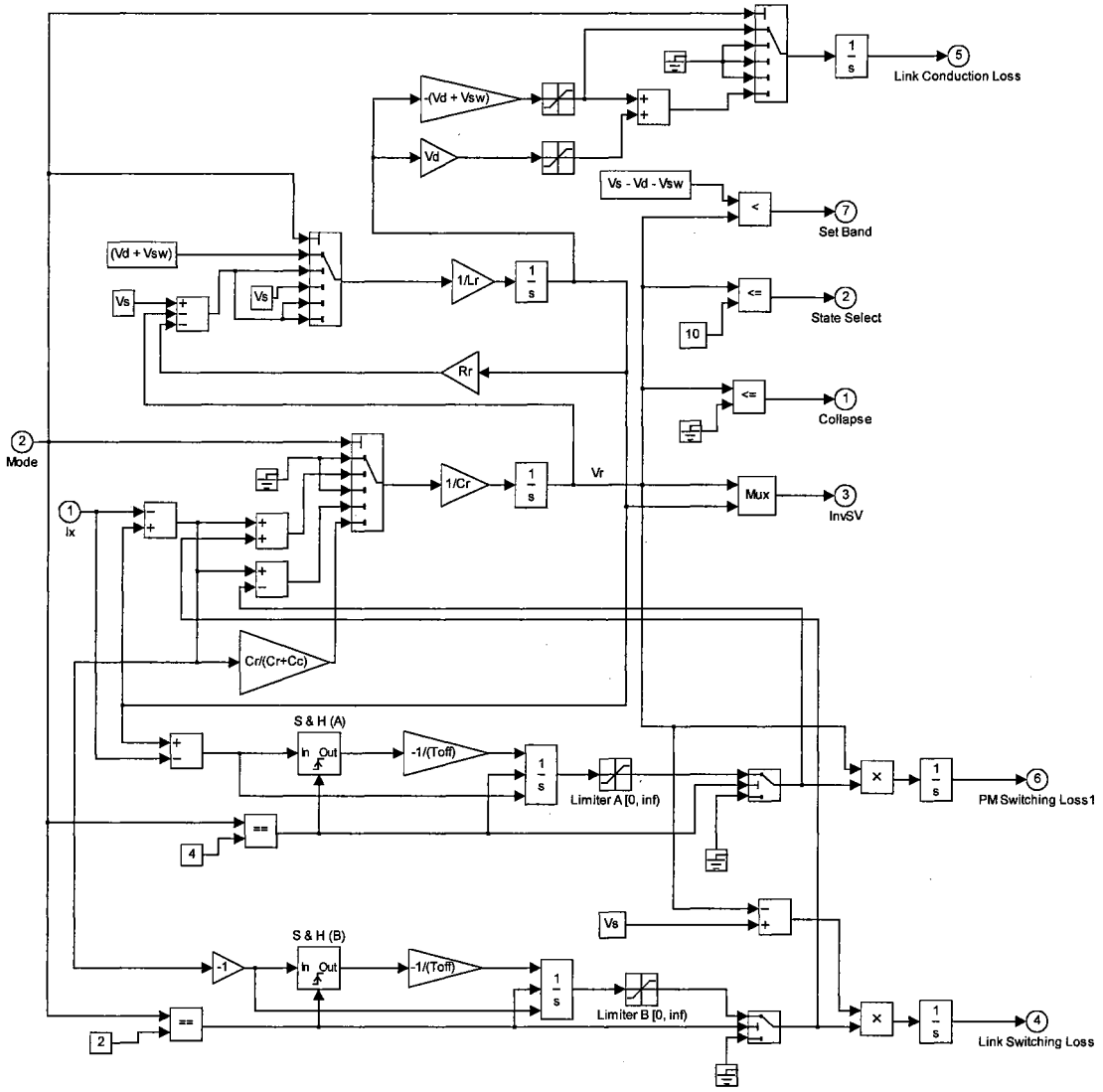

Figure C3. Internal view of the SIMULINK "Inverter Model" block

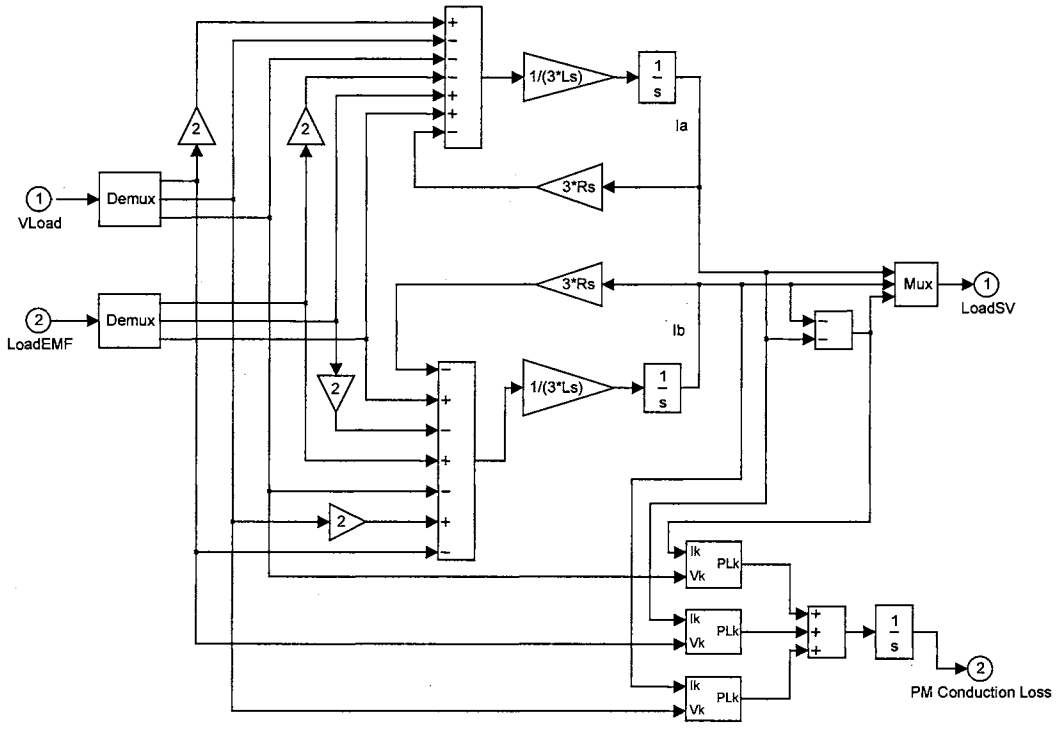

Figure C4. Internal view of the "Load Model" block

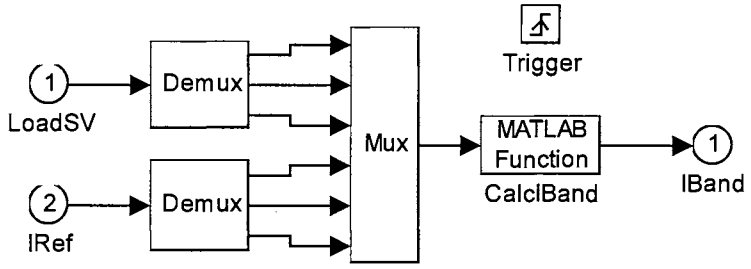

Figure C5. Internal view of the "Calc IBand" block

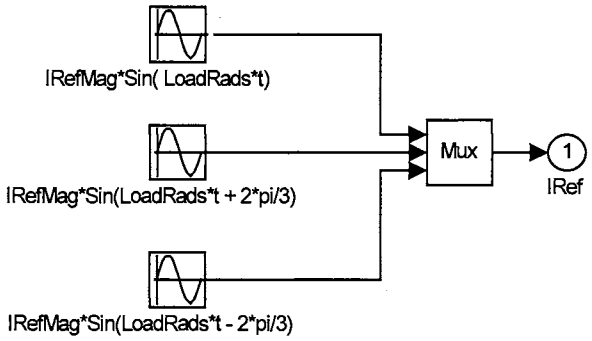

Figure C6. Internal view of the "Load Current Reference" block

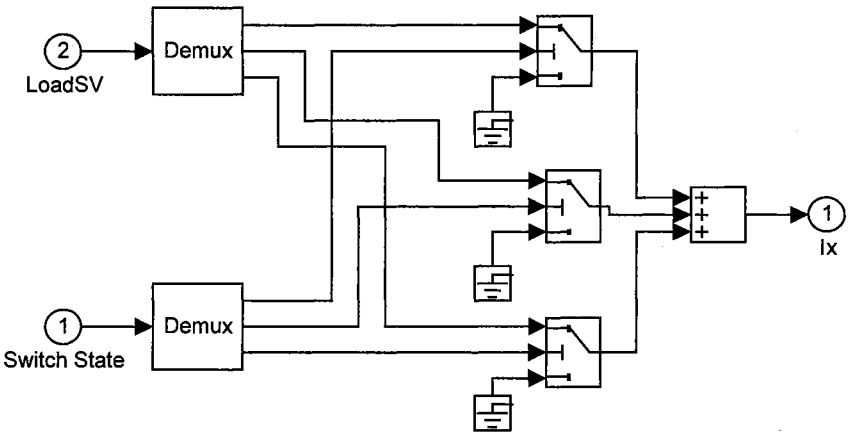

Figure C7. Internal view of both the "Ix Generator" and "Next State Ix Generator" blocks

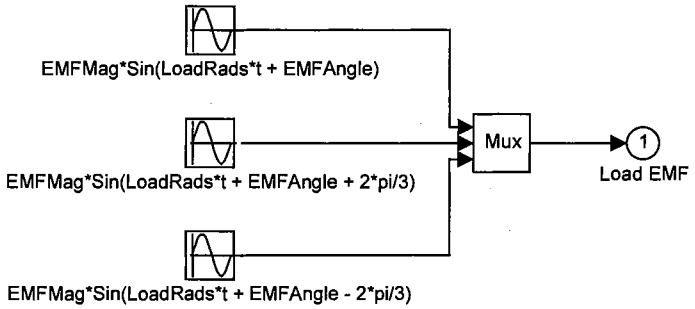

Figure C8. Internal view of the "Load Back EMF" block

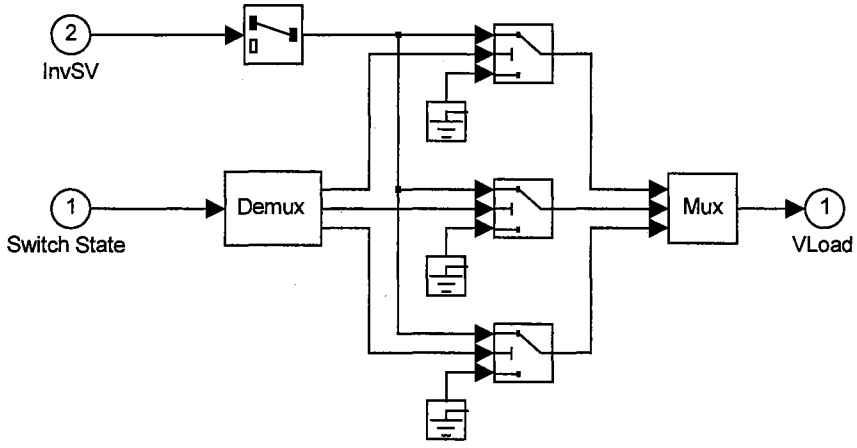

Figure C9. Internal view of the "Load Voltage" block

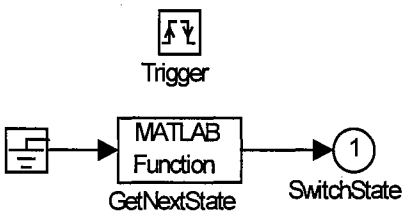

Figure C10. Internal view of the "Next State" block

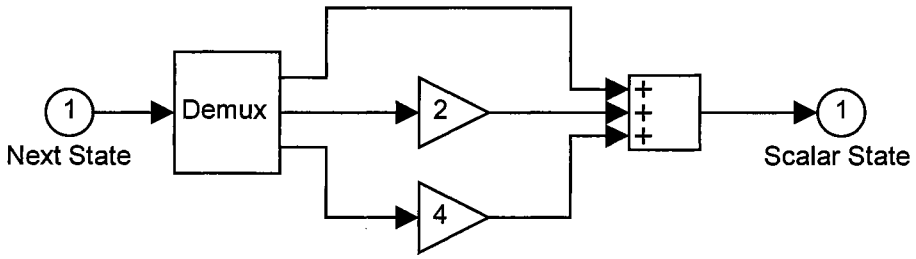

Figure C11. Internal view of "Scalar State" block

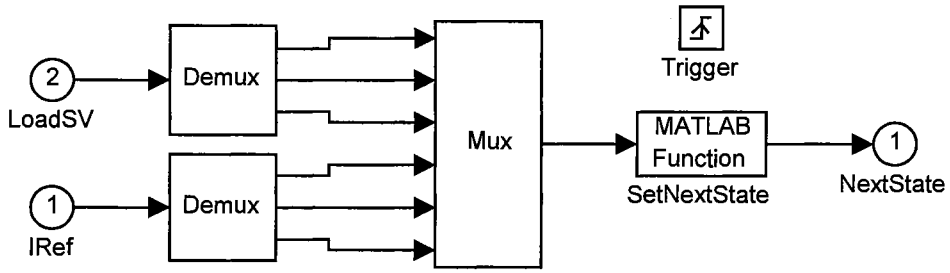

Figure C12. Internal view of "Set Next State" block

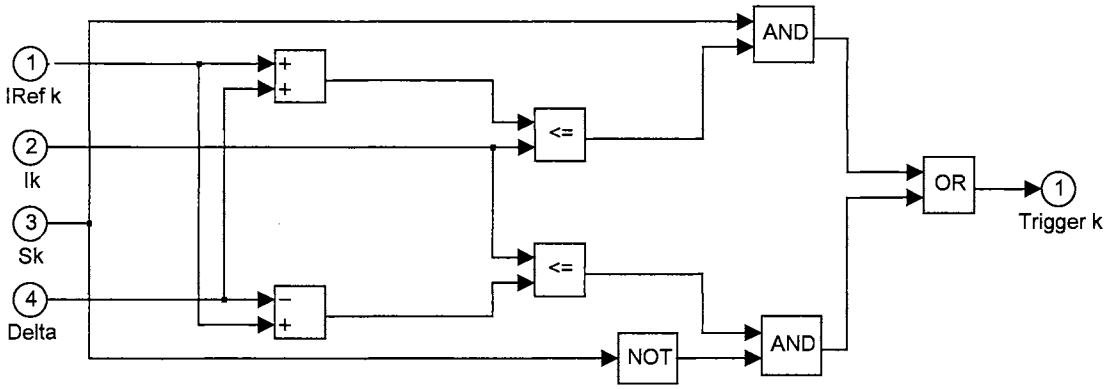

Figure C13. Internal view of the "Phase A Transition," "Phase B Transition," and "Phase B Transition" blocks

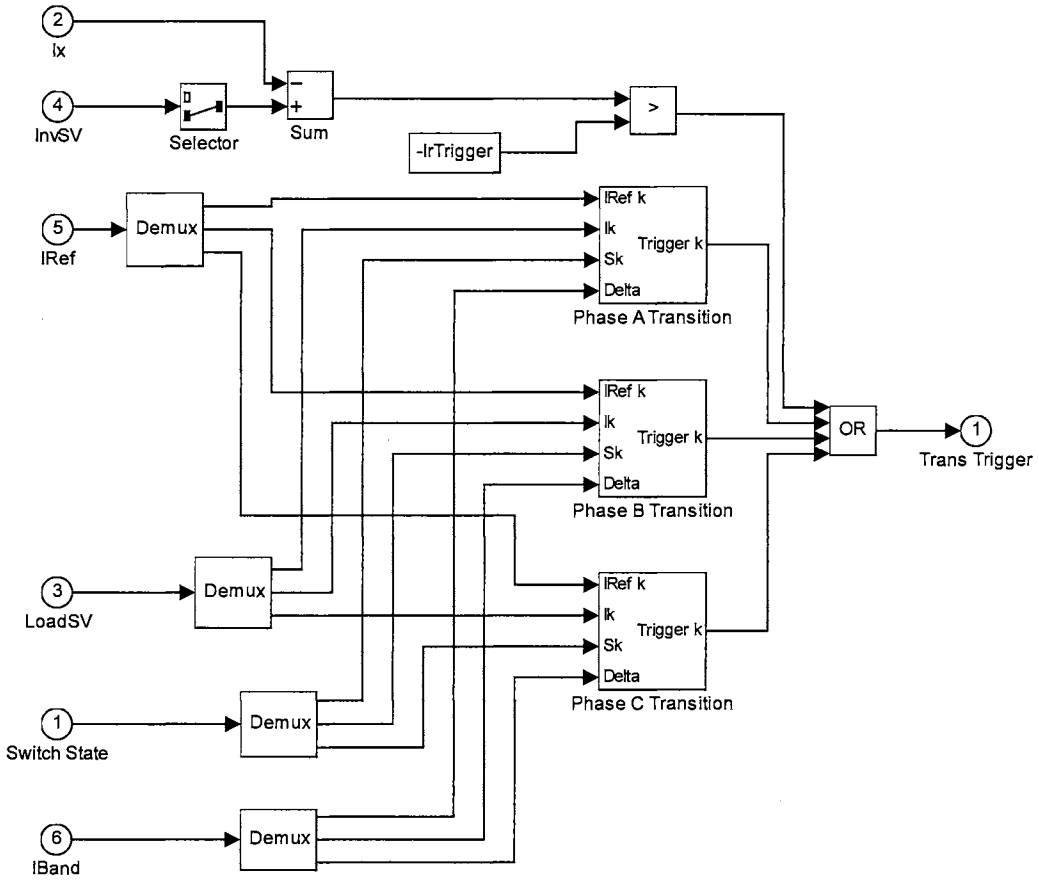

Figure C14. Internal view of the "Transition Trigger" block

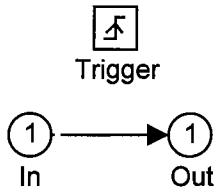

Figure C15. Internal view of the "S & H" block

C.4 MATLAB Source Code Listings Used in the SPRDL Model

C4.1 Init.m

```
clear;
LoadNomFreq = 60;
LoadFreq = 60;
global FileSampleTime Ls Rs Lr Rr Cr Cc Vs Vd Vsw EMFAngle
global EMFMag Toff LoadRads IRefMag S SNext IrTrigger
global LastError LastBand
FileSampleTime = 5e-7;
VLine = 240;
Ls = 1.59e-3;
Rs = 0.2;
Lr = 9.0e-6;
Cr = .44e-6;
Cc = 8.0e-6;
Vs = 400;
Vd = 1.7;
Vsw = 2.3;
EMFAngle = 0;
IRefMag = 100;
LoadRads = LoadFreq*2*pi;
Q = 100;
Rr = (1.0/(2*pi*Q)) * sqrt(Lr/Cr);
EMFMag = 141.9;
EMFMag = EMFMag * LoadFreq/LoadNomFreq
VrInit = Vs - Vd - Vsw;
IaInit = 0;
IbInit = IRefMag*sqrt(3)/2;
IBoost = 100;
S = [1 1 1];
LastError = [0 0 0];
Toff = 750e-9;
SNext = [0 0 0];
IrTrigger = 1.05*(Vs)*sqrt(Cr/Lr);
IrInit = 1.5*(-IrTrigger - IRefMag);
LastBand = [1 1 1];
%=====================================================================
% Initialization file init.m ends.
%=====================================================================
```

C4.2 CalcIBand.m

```
function [Result] = CalcIBand(u)
global IDelta LastError LastBand
%-------------------------------------------------------------------------
% Extract signals into recognized variables.
%-------------------------------------------------------------------------
Ia = u(1);
Ib = u(2);
Ic = u(3);
Ira = u(4);
Irb = u(5);
Irc = u(6);
%-------------------------------------------------------------------------
% Compute the current error associated with each phase.
%-------------------------------------------------------------------------
ErrorA = (Ia - Ira);
ErrorB = (Ib - Irb);
ErrorC = (Ic - Irc);
%-------------------------------------------------------------------------
% Make a copy of the last band tolerance that was used.
%-------------------------------------------------------------------------
Result = LastBand;
%-------------------------------------------------------------------------
% Act on the individual phase current error bands.
%-------------------------------------------------------------------------
if LastError(1) * ErrorA < 0
    Result(1) = abs(ErrorA);
end
if LastError(2) * ErrorB < 0
    Result(2) = abs(ErrorB);
end
if LastError(3) * ErrorC < 0
    Result(3) = abs(ErrorC);
end
%-------------------------------------------------------------------------
% Recorde the present phase current errors for use on the next call.
%-------------------------------------------------------------------------
LastError(1) = ErrorA;
LastError(2) = ErrorB;
LastError(3) = ErrorC;
%-------------------------------------------------------------------------
% Return the result.
%-------------------------------------------------------------------------
LastBand = Result;
%=========================================================================
% Function CalcIBand ends.
%=========================================================================
```

C4.3 GetNextState.m

```
function [Result] = GetNextState(u)
global SNext
Result(1) = SNext(1);
Result(2) = SNext(2);
Result(3) = SNext(3);
%==========================================================================
% Function GetNextState ends.
%==========================================================================
```

C4.4 GetNextState.m

```
function [Next] = SetNextState(u)
global SNext
%--------------------------------------------------------------------------
% Use recognizable variables.
%--------------------------------------------------------------------------
Ia = u(1);
Ib = u(2);
Ic = u(3);
Ira = u(4);
Irb = u(5);
Irc = u(6);
%--------------------------------------------------------------------------
% Set the next phase leg state based on the phase current error.
%--------------------------------------------------------------------------
if Ia > Ira
    SNext(1) = 0;
else
    SNext(1) = 1;
end
if Ib > Irb
    SNext(2) = 0;
else
    SNext(2) = 1;
end
if Ic > Irc
    SNext(3) = 0;
else
    SNext(3) = 1;
end
%--------------------------------------------------------------------------
% Return the result.
%--------------------------------------------------------------------------
Next = SNext;
%==========================================================================
% Function SetNextState ends.
%==========================================================================
```

VITA

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