AC-COUPLED SUBSTRATE-INTEGRATED WAVEGUIDE SLOT ANTENNA IN CMOS FOR TERAHERTZ APPLICATIONS

By

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Bachelor of Science

in Electrical and Computer Engineering

Bangladesh University of Engineering and Technology

Dhaka, Bangladesh

October 2017

Submitted to
the Faculty of the Graduate College of
Oklahoma State University
in partial fulfillment of
the requirements for
the Degree of
MASTER OF SCIENCE
December 2021

AC-COUPLED SUBSTRATE-INTEGRATED

WAVEGUIDE SLOT ANTENNA IN CMOS

FOR TERAHERTZ APPLICATIONS

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ACKNOWLEDGEMENTS

All praises go to almighty Allah, the most glorified, for giving me enough strength throughout the journey of my graduate education. I want to express my sincere gratitude towards my supervisor, Dr. Wooyeol Choi, for his guidance, support, and encouragement. Without his valuable insights and contributions, none of this thesis work would have been possible. I want to express my heartiest gratitude to Dr. John O'Hara and Dr. Ekin Sabit for being a part of my defense committee. I am also grateful to my lab mate Saad Azmeen-ur-Rahman for his valuable suggestion which helped me to write this thesis. Thanks to my father Monsur Ahmed and my mother Fajilatun Nessa, my siblings, and those who are directly or indirectly involved with this thesis work for their encouragement. Finally, I am grateful to the ECE department and graduate college of Oklahoma State University for providing me the opportunity and financial assistance to pursue my MS degree in this prestigious institution.

Name: MD TOAHA ANAS

Date of Degree: DECEMBER 2021

Title of Study: AC-COUPLED SUBSTRATE-INTEGRATED WAVEGUIDE SLOT ANTENNA IN CMOS FOR TERAHERTZ APPLICATIONS

Major Field: Electrical Engineering

Abstract:

Substrate-integrated waveguide (SIW) technology exhibits an emerging and very promising candidate for the development of circuits and components in the millimeter-wave region. As a part of the high frequency wireless communication system, on-chip antenna is playing an important role. However, designing on-chip antenna presents significant challenges due to the design-rule restrictions posed by the foundries. Also, antenna performance degrades owing to the process limitation and the conventional structure. In this thesis, an on-chip SIW slot antenna has been designed in TSMC 65-nm CMOS process to improve the radiation efficiency and to minimize the radiation leakage of the antenna. The antenna shows radiation efficiency of 35% and −10-dB bandwidth of 20 GHz at 410 GHz. However, characterizing on-chip antennas at this THz frequency range is difficult due to parasitic radiations from the measurement apparatus such as THz probes. One way to measure the antenna response is to integrate a detector circuit. Typically, a detector circuit needs RF and DC signal isolation. However, the SIW structure of the antenna is DC-shorted in the sidewall which poses a great challenge to build a detector circuit. Therefore, an AC-coupled SIW slot antenna has been presented by exploiting the antenna sidewall as a DC capacitor. Therefore, the SIW slot antenna including the DC capacitor can work well as expected. The designed AC-coupled SIW slot antenna integrated detector exhibits voltage responsivity of 316 V/W and 37 pW/Hz$^{1/2}$ at 410 GHz.

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CHAPTER I

INTRODUCTION

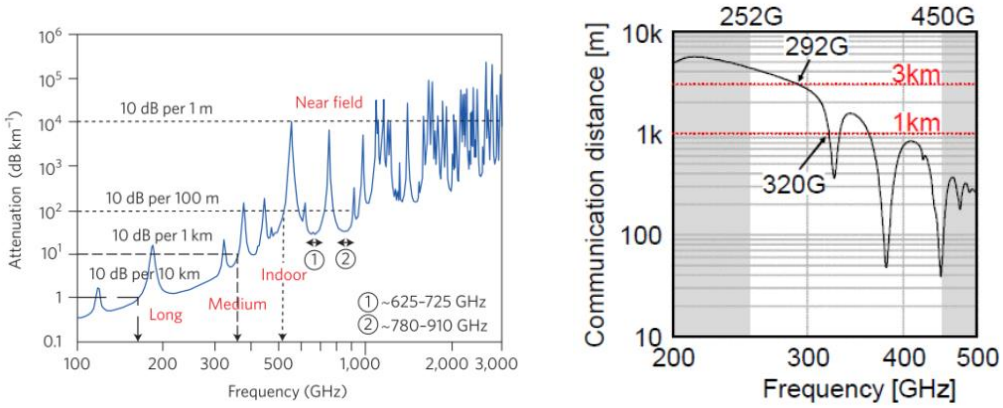
1.1 Terahertz Signal

Terahertz signal (0.1 THz-10 THz) generation has become an attractive field to the researchers as it has potential applications in the field of spectroscopy, active and passive imaging for detection of concealed weapon and chemical agents, high data rate wireless communication and networking design [1]- [4]. THz region is located in between the RF microwave and the IR region in the EM spectrum as shown in Fig. 1 [1]. This region exhibits some inherent advantages compared to microwave and RF electronics such as- wider bandwidths, higher spatial resolutions, and component compactness. Also, it offers promising application in novel and new sensing modalities. However, the THz gap shows significant challenges which include extreme atmospheric attenuation, standing wave interference, and weak interaction signatures etc. during practical sensor implementation and development. There are some fundamental challenges to implement electronic devices in this frequency range where the EM wavelength is on the order of component size. To meet up this challenges, modern efficient design model is needed.

Figure 1.1. Representation of the THz region in the EM spectrum [1]

1.2 Frequency consideration

In modern wireless system, the frequency spectrum beyond 275 GHz is a good research scope as it limits the potential interference with the existing bands [5]. Frequencies between 231 GHz and 320 GHz suffer less from atmospheric attenuation, or path loss, of a decibel (dB) every kilometer, as shown in fig. 2a [6]. It is clear from fig. 2b that these frequencies can be used for long-distance communications [7]. Also, fig. 2b illustrates that higher frequencies can be used for indoor and near field applications. The global regulatory bodies have started taking steps to setup standards for these frequency bands. In 2019, the federal commission created a new category of licenses for the spectrum beyond 95 GHz [8]. This frequency band has also been recommended by the International Telecommunication Union (ITU) for further research and the Institute of Electrical and Electronics Engineers (IEEE) formed the IEEE 802.15.3d task force for global Wi-Fi use at frequencies from 252 GHz to 325 GHz [9].



(a) (b)

Figure 1.2. Atmospheric characterization in THz band: (a) atmospheric attenuation [6] and (b) communication distance at 10 dB attenuation [7].

As high frequency waves create shorter free-space wavelength, the component size of wireless system become smaller. At THz frequency range, antennas can be integrated on-chip that results into reduction of antenna size as well as the cost because expensive and lossy packaging and interconnects can be avoided. However, the design of on-chip antennas is challenging due to some process limitations given by the foundries [4]. To compensate for the increased path loss compared to the lower frequencies that are widely used today, highly directive antennas need to be designed. For this reason, communications using THz signals makes it resistant to interception. According to the Friis' transmission equation, it also turns out that THz signals are inherently more directional due to shorter wavelengths and so are affected less by free-space diffraction [10].

1.3 Motivation

As a vital part of the THz signal generation, realization of on-chip antenna has become a point of interest to the researchers. The latest CMOS technologies is providing simple and less costly ways to design the antenna in the on-chip process. These antennas should perform less radiation leakage, higher radiation efficiency, and wider fractional bandwidth at the operating frequency. Yet it is really challenging to detect the THz signal at this frequency range. Because the on-chip antenna response measurement is very difficult and complex process. One way to characterize on-chip antennas is to integrate a demonstrator circuit that can effectively detect the response and gives a good understanding of the on-chip antenna performance.

This thesis is to realize the performance of a 410 GHz on-chip Substrate Integrated Waveguide (SIW) slot antenna by building a demonstrator circuit. Along with the antenna the demonstrator circuit contains a detector based on a diode connected NMOSFET. The substrate integrated waveguide structure inherently suffers from the DC short problem due to the shorted sidewall. An AC-coupled structure has been embedded in the antenna structure which resolve this DC short problem at 410 GHz. The full demonstrator circuit has been sent to the foundry for the fabrication. After receiving the chip, the antenna will be characterized.

1.4 Thesis outline

The rest thesis is organized as follows:

- Chapter II gives the relevant background of on-chip antenna along with the working principle of the SIW slot antenna. Also, shows the literature review of on-chip antenna

- Chapter III discusses the design and optimization of the SIW slot antenna
- Chapter IV presents the design and performance of the 410 GHz AC-coupled SIW slot antenna detector circuit
- Chapter V discusses the conclusion, contribution, and the future work

CHAPTER II

REVIEW OF LITERATURE

2.1 Terahertz on-chip antennas

Terahertz antennas usually work in the range of 300 GHz to 3 THz of the EM spectrum.-Typically, silicon-based technologies provide low-cost THz on-chip antennas which is better alternative than costly III-V technologies. Table 2.1 lists some on-chip antennas including their performance with operating frequency.

Table 2.1 State-of-the-art of some on-chip antennas

Reference	Process	Structure	Frequency (GHz)	-10 dB Bandwidth	Gain (dBi)
[11]	0.18µm CMOS	Yagi, dipole, loop	60	53-65, 54-65, N/A	-8
[12]	65nm CMOS	Dipole	28	N/A	N/A
[13]	Standard CMOS	Cavity-backed slot antenna	140	135-141	-2
[14]	Thin GaAs substrate	Log periodic	94	87-99.5	4.8

[15]	45nm CMOS	Patch	410	N/A	0.41
[16]	65nm CMOS	SIW slot	460	N/A	0.09

2.2 On-chip antennas state-of-the-art

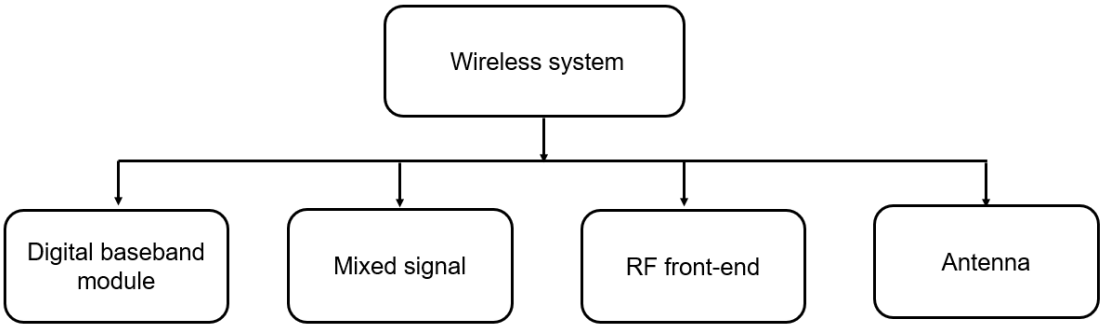


Figure 2.1. Modern wireless system

Modern wireless system consists of four major functional modules (shown in fig. 2.1): the digital baseband module handling the signal processing, the mixed-signal module provides signal conditioning, the radio frequency (RF) front-end providing the RF carrier with modulated data, and the antenna for transmission of the signals [4]. Engineers are trying to integrate these different modules either in horizontal or vertical manner. However, it is hard to integrate these modules as each of them are suitable to different technologies. Moreover, integrating these different technologies at higher frequencies become difficult due to lossy interconnects. As a major part of wireless communication module, antenna plays an important role which is usually the largest component of the system. The antenna dimension becomes smaller at THz frequency range and PCB antenna can no longer be used in the system. Therefore, Advance silicon technologies (such as CMOS) have provided the on-chip integration of the antenna without any transitions from one

technology to another. However, there are number of challenges associated with on-chip antennas such as- low antenna radiation efficiency resulting from losses in low-resistivity silicon substrates, layout restrictions due to metallization density rules in foundry process [4].

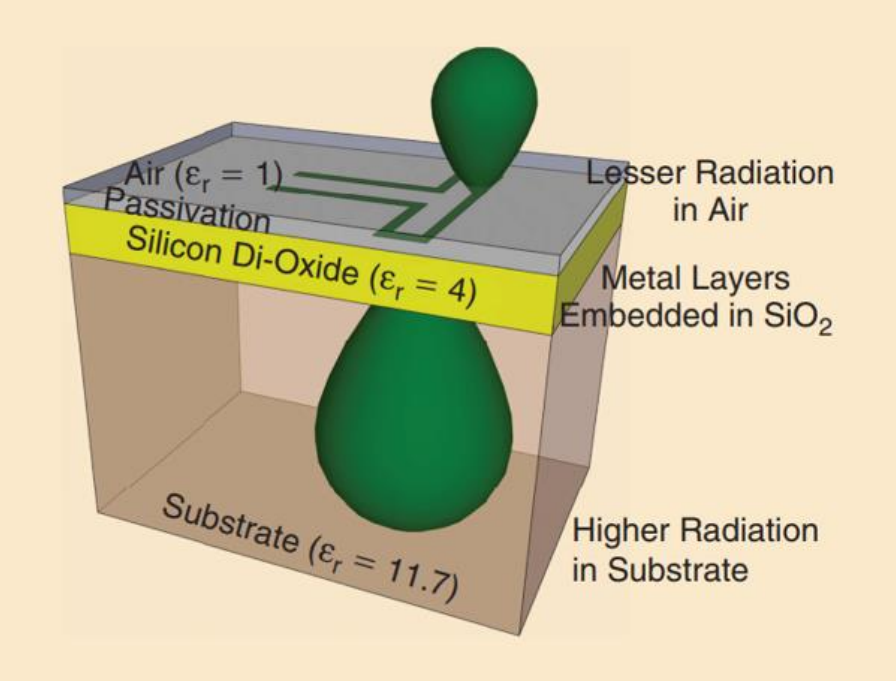


Fig. 2.2. EM radiation from on-chip antennas in silicon technology [4]

In 2006, Babakhani et al. [17] designed a 77 GHz 4-element phase array receiver with on-chip dipole antenna in silicon. Since the on-chip dipole antenna usually does not need any ground metal it suffers from power flow towards the lossy silicon substrate. A typical on-chip dipole antenna EM radiation is shown in figure 2.2. As a result, it showed very low antenna gain and radiation efficiency (approximately 3%). This power loss problem was solved by attaching lens in the backside of the antenna, but it significantly increased the antenna cost. Later, the on-chip antenna with PCB backside reflector [18] was used to replace the lens. Yet it requires impractical thin wafer

which reduces the mechanical strength. Moreover, it exhibited largely lateral directional coupling due to loosely confined wave in the substrate and tilted radiation beam. On the other hand, on-chip antenna with ground shielding structure such as patch antenna resolve the previous problem by using closely spaced top and ground metal along with ground ring around the structure. In [19], Han et al. designed a 280-GHz on-chip patch antenna with a ground ring around the structure which showed radiation efficiency of 21% and -10dB bandwidth of 7GHz. This on-chip patch antenna does not show higher radiation efficiency due to RF EM power leakage through the sidewall. Also, this antenna needs extra ground ring isolation around the structure to minimize EM radiation interaction with surrounding circuitry. For this reason, scientists are trying to find the on-chip antenna with higher radiation efficiency and low EM power leakage. In this regard, Substrate Integrated Waveguide (SIW) slot antenna has become a point of interest towards the modern engineers. On-chip SIW slot antenna is shielded around the sides which does not require any extra ground ring and there is less change of EM power leakage around the structure. A comparison among different on-chip antennas has been shown in table 2.2. From the comparison table, in terms of antenna bandwidth, radiation efficiency, isolation and cost Substrate integrated waveguide (SIW) slot antenna is the best candidate. Therefore, I am interested in exploring on-chip SIW slot antenna.

Table 2.2 On-chip antenna comparison

Parameter	**Dipole Antenna**	**Patch Antenna**	**Substrate Integrated Waveguide (SIW) slot antenna**
Bandwidth	Wider	Narrower	Medium

Radiation Efficiency	Lower (Higher without lens)	Medium	Higher
Isolation	Not Needed	Needed	Not Needed
Cost	Low (High without lens)	Low	Low

2.3 Terahertz Detectors

Terahertz signal can be detected by the demonstrator circuit. These THz signal detectors are the most known devices in the THz imaging field. A detector is a fundamental building block, and it is getting attention due its low cost, high yield, and excellent capability of integration with other circuits. There are three commonly used devices in CMOS process to build a THz detector circuit. They are unbiased FET (ColdFET) [22], Schottky Barrier Diode (SBD) [23], and diode-connected FET (DCFET) [24]. In 2009, Ojefors et al. designed a 0.65 THz Focal-Plane Array (FPA) in a 250-nm CMOS Process Technology [22], where the array was built with 3x5 pixels and each array consisting of ColdFET with a patch antenna. The designed FPA exhibited 80kV/W voltage responsivity, and NEP of 300 pW/√Hz. The THz signal detection in ColdFET process can be understood using non-resonant plasma-wave phenomenon [20]. Later, CMOS-compatible SBDs were used in detector circuits due to their high cutoff frequency (few THz) and fabrication simplicity. In 2011, Han et al. demonstrated a 280-GHz Schottky diode detector in 130-nm digital CMOS process [23]. The single pixel unit of the 280 GHz Schottky detector exhibited voltage responsivity of 250 V/W and noise equivalent power (NEP) of 33 pW/$Hz^{1/2}$. The full imager was made with 2x2 array of the detector unit cell, and it performed with 48 dB of Signal to Noise Ratio

(SNR). But the SBD needs a customized model which usually is not provided by the foundry. The detector circuit can also be built by using DCFET's. As an example, Kim et al. reported an 820-GHz 8x8 array of diode-connected NMOS transistor detector circuit in 130-nm CMOS process for active imaging in 2016 [24]. The single pixel of this diode connected transistor-based detector exhibits a voltage responsivity of 273 V/W and an NEP of 42 pW/$Hz^{1/2}$ at 860 GHz. The advantage of the detector with diode connected transistor is that the transistor diode model is given by the foundry therefore the design process can be more straightforward.

2.4 Substrate integrated waveguide

In recent years, the more compact and broadband wireless communication device for millimeter wave application has been increased. A new technology is needed to keep up with this high frequency devices considering optimum performance. As an advanced modification of conventional rectangular waveguide, which plays an important role in millimeter and microwave RF system, subtracted integrated waveguide (SIW) is employed. SIW has a crucial advantage over the conventional waveguide structure as can easily be integrated in the microwave and millimeter integrated circuits [25]. In SIW technology, both the active and passive components can be integrated in the same substrate [26]. Also, it has high power handling capability with good electrical shielding. Moreover, it alleviates the need of transition between different technologies when one or more chipsets are needed to be mounted on the same substrate. As there is no transition between different technologies, it reduces the losses and parasitics.

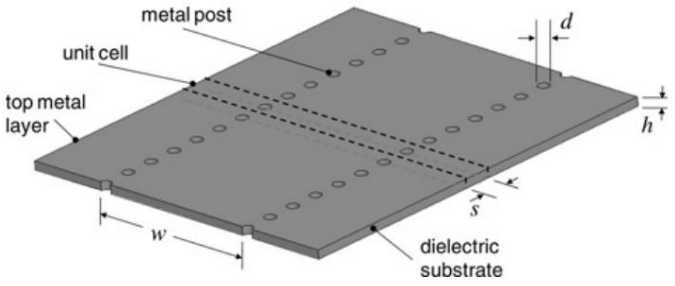


Fig 2.3. Geometry of substrate integrated waveguide [25].

Figure 2.3 shows a typical substrate integrated waveguide implemented on a planar circuit board (PCB). In this figure, some critical dimensions of SIW are its height h, width w, via diameter d, and via spacing s. The top and bottom metal plate of the SIW and the rectangular waveguide are same. The sidewalls of the SIW structure are replaced by the periodically spaced hollow cylinders with metallic walls. As there is a certain space between the sidewall metallic vias, the EM power propagating through the SIW structure may leak through the sidewall. So, the sidewall vias need to place closely to minimize the EM leakage through the sidewall. The typical design rule to minimize the radiation leakage through the sidewall is: the diameter of vias $d<\lambda_g/5$, and the pitch p should be less than 2d. In our SIW design, the guided wavelength λ_g=373μm. SIW structure shows similar propagation characteristics like the rectangular metallic waveguide considering the metallic vias are closely spaced and radiation leakage can be neglected. But due to the sidewall gaps, TM mode is not supported by the SIW structure whereas TE mode can propagate through the structure. Specifically, the fundamental mode TE_{10} mode is supported by the SIW structure. Because of the similarity between the SIW and rectangular waveguide, there is an established empirical relationship between the geometrical dimension of SIW and the effective width W_{eff} of rectangular waveguide with the same propagation characteristics [27]. This relationship is as follows

$$W_{eff} = W - \frac{d^2}{0.95s} \quad (1)$$

Where, d is the diameter of the metal vias, w represents their transverse spacing, and s is longitudinal spacing.

2.5 Slot antenna

A slot antenna is a kind of aperture antennas with a rectangular slot cut from the aperture surface which forms an omnidirectional microwave antenna. Slot antennas usually integrate the feed and radiating structure in the same metal by placing slots in the top wall of the aperture. The SIW slot behaves like a special type of conductor-backed slot antenna.

2.5.1 Babinet's principle

The working principle of the aperture slot antenna comes from the Babinet's principle [28]. It states that when the field behind a screen with an opening is added to the field of a complementary structure, the sum is equal to the field when there is no screen. According to the theory, the aperture slot is an absence of an electric dipole antenna which works a magnetic dipole. As a result, the E and H field exchange with each other. The polarization of the slot antenna rotates 90º compared to conventional Electric dipole antenna. Hence, the radiation from a vertical slot is horizontally polarized. The whole phenomenon is shown in figure 2.4.

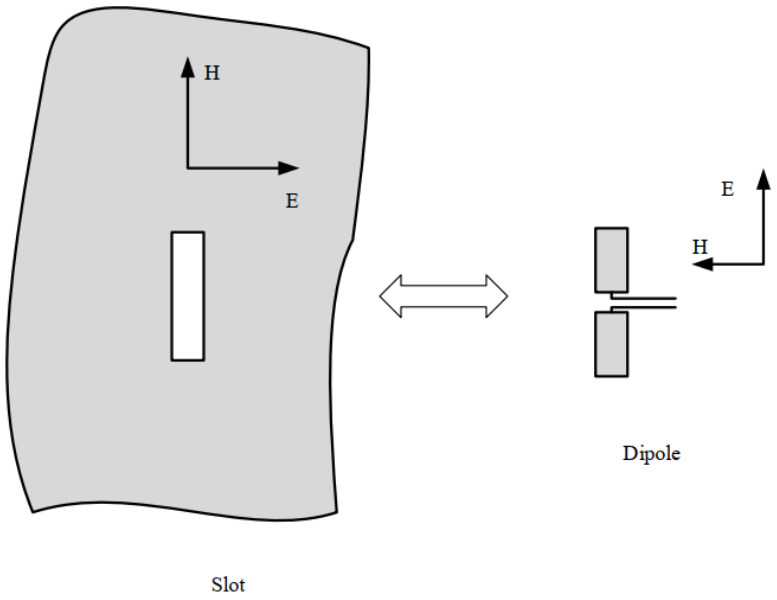


Figure 2.4 Slot antenna equivalent magnetic dipole according to Babinet's principle [29].

2.5.2 SIW slot radiators radiating principle

A longitudinal slot cut into the top wall of SIW interrupt the transverse current flowing into the wall, which focuses the current to travel around the slot and thereby introduces in the slot [29]. The current flow in the waveguide surface depends on the position of the slot. The position of the slot creates an impedance to the transmission line and the amount of energy coupled to the slot which finally radiates from the slot.

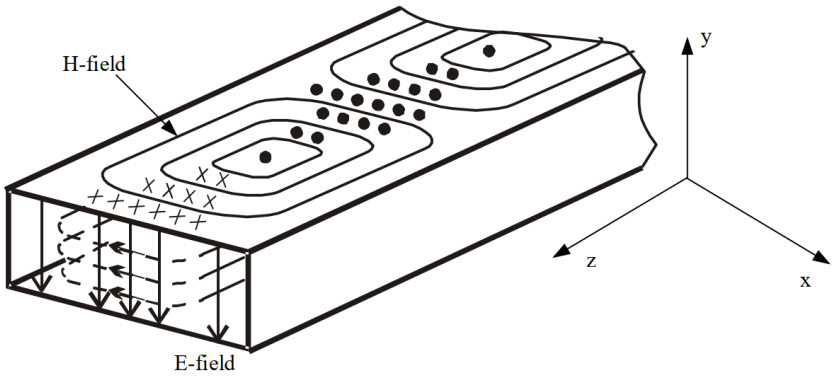


Figure 2.5. Electromagnetic field distribution for TE_{10} mode of a rectangular waveguide [29].

Figure 2.5 exhibits the E field distribution for TE10 mode of a of a rectangular waveguide. The E filed is distributed in the y-direction of the waveguide and its symmetric about the centerline of the rectangular waveguide. Current flowing though the walls of the waveguide proportional to the difference in the Electric field between any two points. So, any slot placing exactly at the center of the waveguide does not radiate as the E-field is symmetrical around the center of the waveguide. The slot moving away from the centerline creates difference in the E-field intensity between the edges of the slot. For this reason, it interrupts the flow of more current and couples more energy to the slot and increases the radiated power. But keeping the slot close to the sidewall couples very low amount of energy as the sidewall are shorted and E-field is very small, so the difference of the E-field on the two edges are very small. So, there is an optimum distance of placing the slot from the centerline which gives maximum radiation from the waveguide surface [29].

CHAPTER III

410 GHz SIW slot antenna design

This chapter describes the Taiwan Semiconductor Manufacturing Company (TSMC) 65nm CMOS process design-rule restrictions and the way to minimize the design rule restrictions for SIW slot antenna design.

3.1 65-nm CMOS process layout design rule restrictions

To design the detector circuit in CMOS process, the 410 GHz AC-coupled SIW slot on-chip antenna was designed in Taiwan Semiconductor Manufacturing Company (TSMC) 65nm CMOS process. Figure 3.1 shows the cross-section of the TSMC 65nm process metallization with dielectric layers. There is total 10 metal layers (Metal 1 to Metal 10) in TSMC 65nm process. From metal 1 to metal 9, all the layers are copper layers and the top metal 10 is made of aluminum layer. Besides, there are 9 vias in between the adjacent metal layers. Also, there are 29 dielectric layers: D0, D1, D2, …..., D28 and four passivation layers. But the dielectric layers differ in thickness. Metal 1 to Metal 6 is shorted together and they are considered as the ground of the SIW slot antenna. Metal 10 is designed as top metal layers (EM signal radiating layer) of the SIW slot antenna. The sidewall of SIW is comprised of 10 metal layers from Metal 1 to Metal 10. The layout of SIW is much different from any other process due to some layout design-rule restrictions provided by the CMOS technology. These layout design rule significantly impact the SIW design.

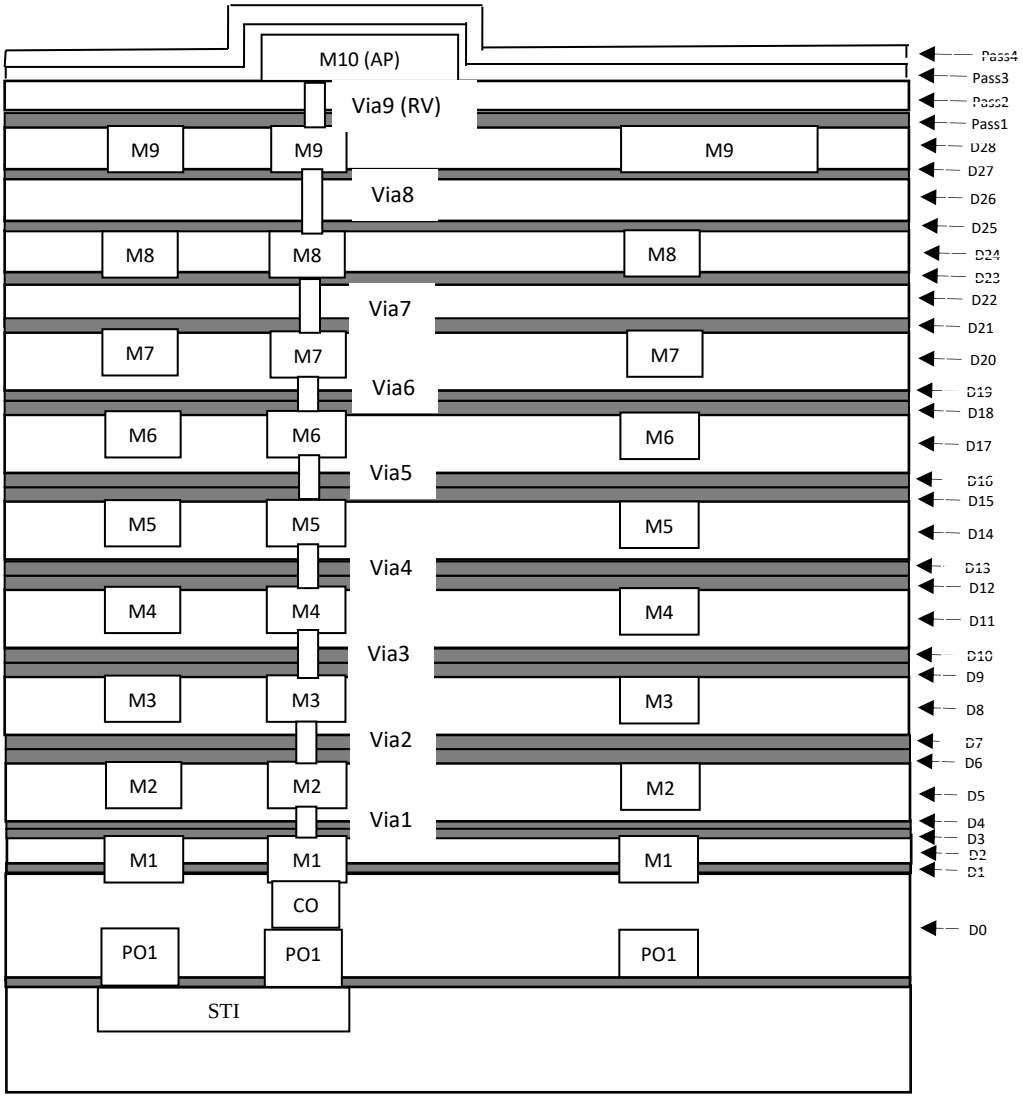
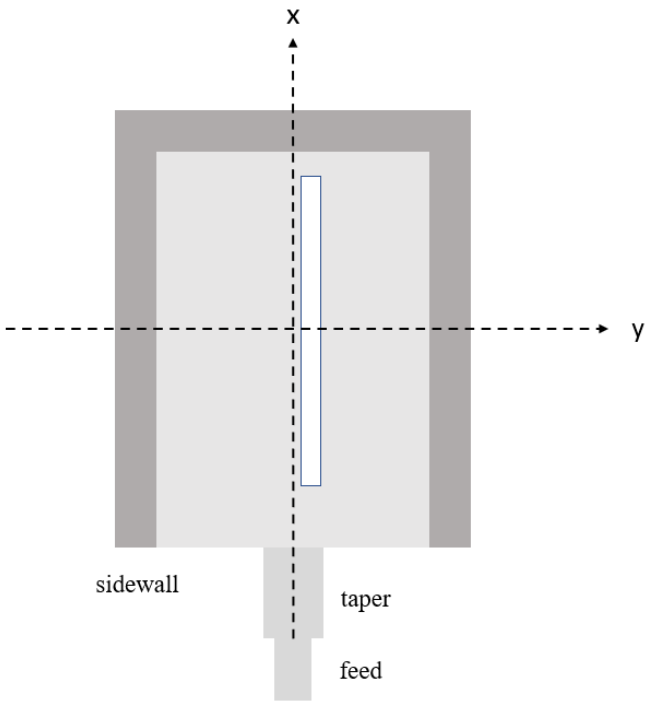
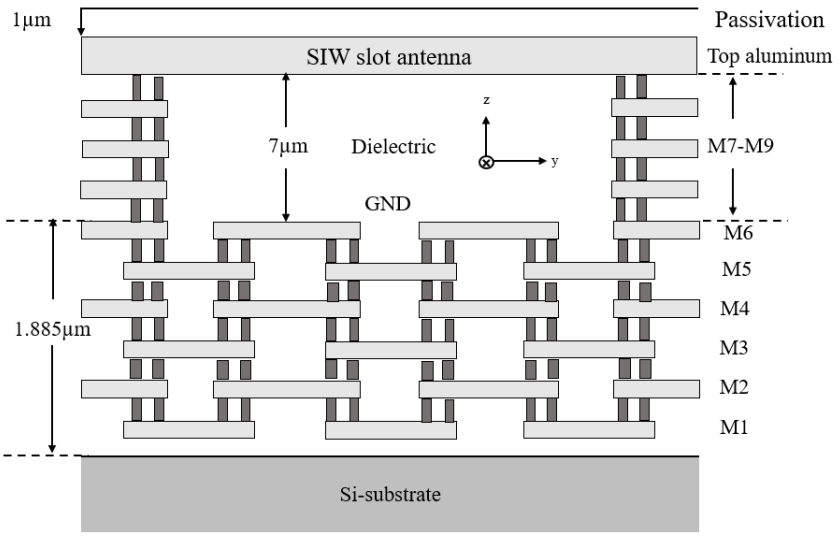


Fig. 3.1. TSMC 65 nm metal layer cross section



(a)



(b)

Fig 3.2. (a) Top view and (b) cross section view of SIW slot antenna layout

The maximum density for metal 1 is 80% with 50 µm steps in each 100 µm x 100 µm window. In metal 1, square holes of 10 µm x 10 µm with 10 µm spacing were created. For the internal metal layers (metal 2 to metal 9), the minimum metal density is 10% and maximum density is 80%. However, in some level's waiver were offered by the foundry for metal 7 to metal 9 and kept these metal levels empty. Also, dummy block layers were kept around the metal level to avoid the random dummy metal in the structure that may change the performance of the antenna detector.

The SIW slot antenna layout top view is shown in fig. 3.2 (a). And the cross section view of the antenna is shown in figure 3.2 (b). The top metal layer (metal 10) is aluminum, and it is used as the radiating structure of the antenna which radiates the EM power into the air. As the metal 10 is the vital layer of the TSMC 65nm process, it is used very carefully in the design. The minimum and maximum metal density for metal 10 level is 10% and 70% respectively. The maximum width for metal 10 is 35 µm and minimum is 3 µm. The width for metal 10 level is maintained 35 µm in each unit cell and minimum 3-µm square punch hole was created to satisfy the design rule. Also, a slot was cut out from the metal 10 layer, and it is considered the vital part of the EM radiation. No hole was created within 20 µm of the slot considering the layout restrictions as it can change the radiation performance.

3.2 SIW slot antenna design

In our antenna design, we approximated the dielectric layers into one layer by calculating effective dielectric constant of all the 29 dielectric layers. The calculated effective dielectric constant is 3.87 for considering this dielectric layer and all the four passivation layers were kept same. The height of the SIW structure is Metal 1 to Metal 10 layers, which is 9.575 µm in our CMOS process. The maximum size of the via 9 (RV) is 3 µm x 3 µm and for spacing we used minimum spacing of 3 µm. The minimum spacing between the via 9 ensures lowest RF EM power leakage from the sidewall of the SIW structure. The width of the SIW is 280 µm for our case and it allows only single mode (TE_{10}). The cutoff frequencies of the different modes in the equivalent rectangular waveguide are given by the following equation:

$$f_{c_{mn}} = \frac{c}{2\pi\sqrt{\varepsilon_r}}\sqrt{(\frac{m\pi}{w})^2 + (\frac{n\pi}{h})^2} \qquad (3.1)$$

Here, c is the speed of light in free space, ε_r is the dielectric constant of the material in the waveguide and w, h are the width and height of the rectangular waveguide where m, n are the mode numbers.

The top view of the SIW slot antenna with dimensions are shown in figure 3.6. The width of the antenna is 280 µm and the slot length is 330 µm in our case. The slot dimension of the SIW antenna is approximated by the following equation:

$$L = \frac{\lambda_0}{\sqrt{(2\varepsilon_r+1)}} \qquad (3.2)$$

The slot width of the antenna is 21 µm, and it the position of the slot is 5 µm away from the centerline. A microstrip feed along with a taper are used as the antenna feeding structure. Feed width is 24 µm and taper is 36 µm in width. Besides the sidewall is 30 µm width.

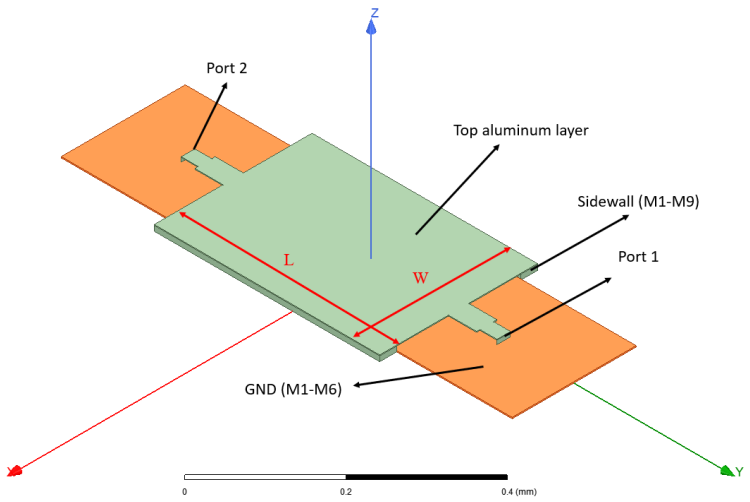


Figure 3.3 On-chip back-to-back SIW-microstrip transition structure

To understand the SIW structure, initially a back-to-back SIW-microstrip transition structure with two port system was created like figure 3.3. Here, the top layer is aluminum, and the bottom layer is ground which is M1-M6 and the sidewall is shorted M1-M9. The whole structure is integrated into a silicon dioxide. Figure 3.4 and 3.5 shows the simulated S-parameter for the two port SIW-microstrip structure for different width of the SIW structure. It is conspicuous from these two figures that 280µm of SIW width gives highest S_{21} and lowest S_{11} at 410 GHz.

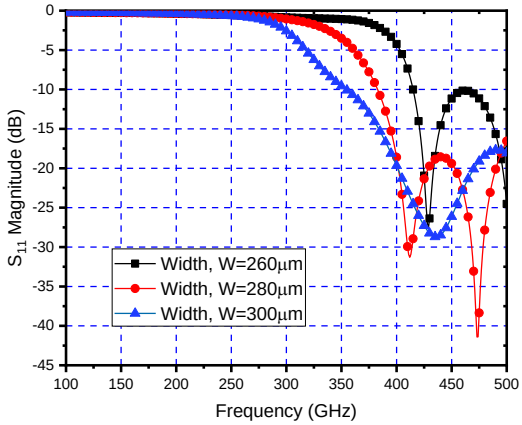


Figure 3.4. Simulated S_{11} magnitude for different width of the two port SIW structure

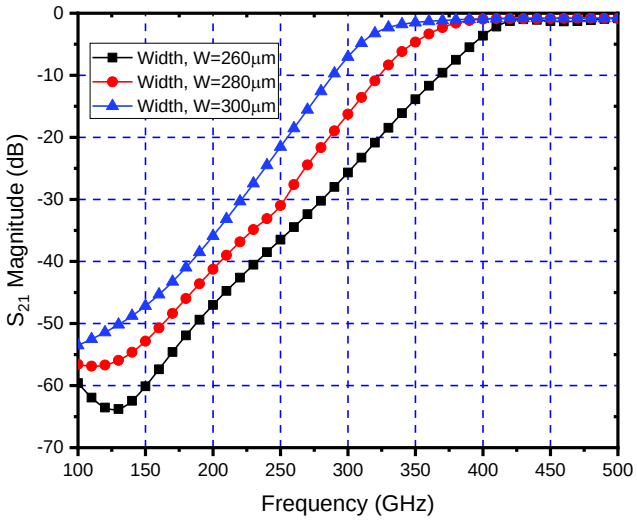


Figure 3.5. Simulated S_{21} for the two port SIW structure

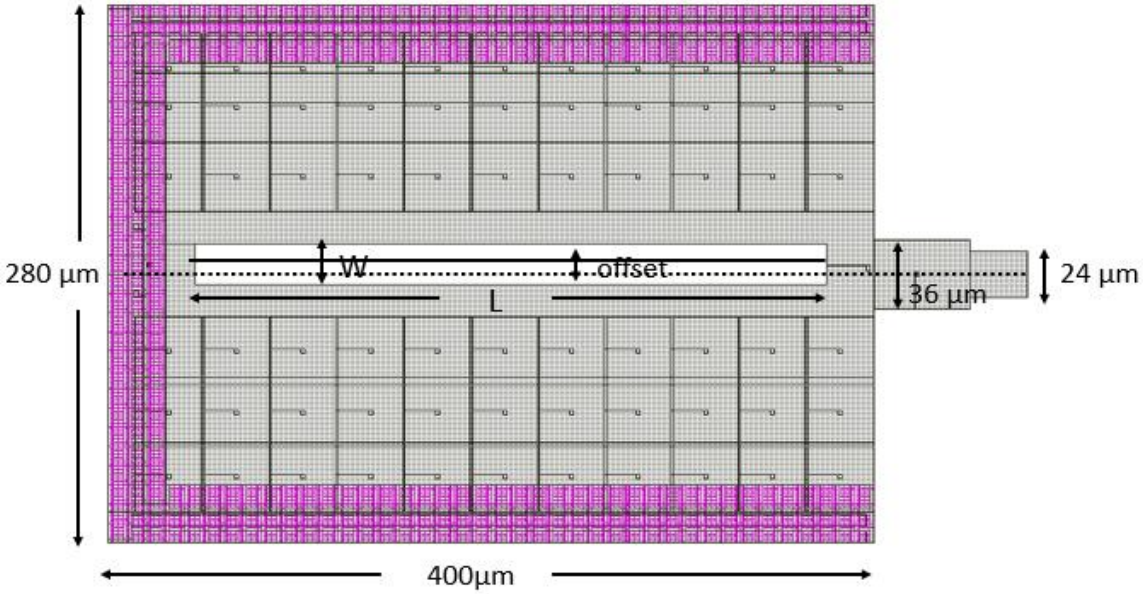


Fig 3.6. Top view of the SIW slot antenna with dimensions

To optimize the antenna-dimension some engineering analysis has been used. The slot length L, width W and the slot offset from the centerline of the antenna has impact on the resonant frequency

of the antenna. According to fig 3.7, the higher slot length decreases the S11 magnitude of the antenna which means the resonant frequency is decreasing with larger slot length.

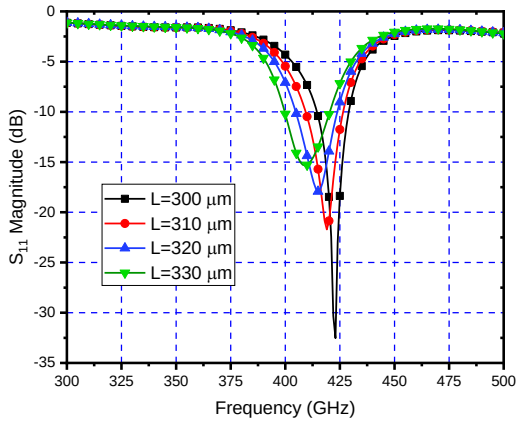


Fig 3.7. The impact of slot length on antenna resonant frequency

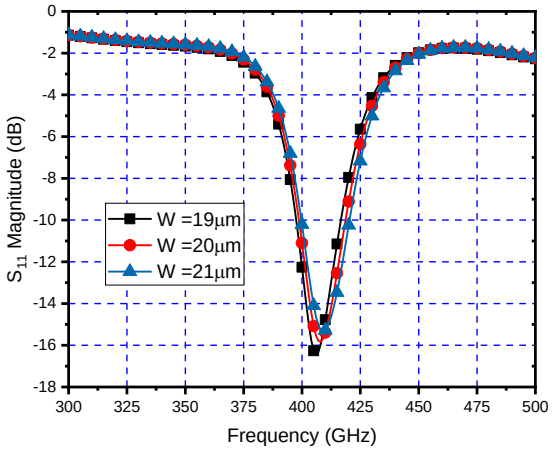


Fig 3.8. The impact of slot width on antenna resonant frequency

Figure 3.8. represents the impact of the slot width on the antenna resonant frequency. The larger slot width increases the resonant frequency.

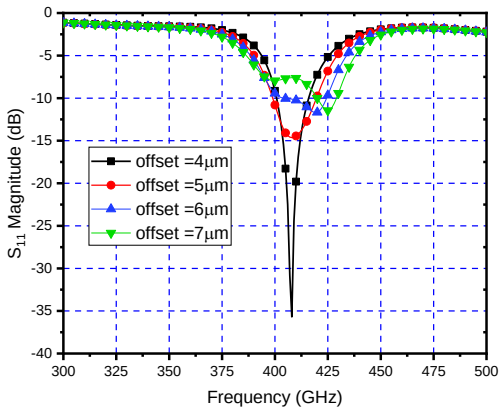


Fig 3.9. The impact of slot offset from centerline on antenna resonant frequency

It is conspicuous from figure 3.9 that the slot offset from centerline of the antenna increases antenna resonant frequency. From the simulation figure 3.7, 3.8, and 3.9 we observed that changing the antenna slot length, width and offset from the centerline changes the resonant frequency of the antenna. We used this behavior to optimize the antenna and make it work at 410 GHz with a moderate impedance bandwidth and radiation efficiency.

3.3 SIW slot antenna simulation in Ansys HFSS

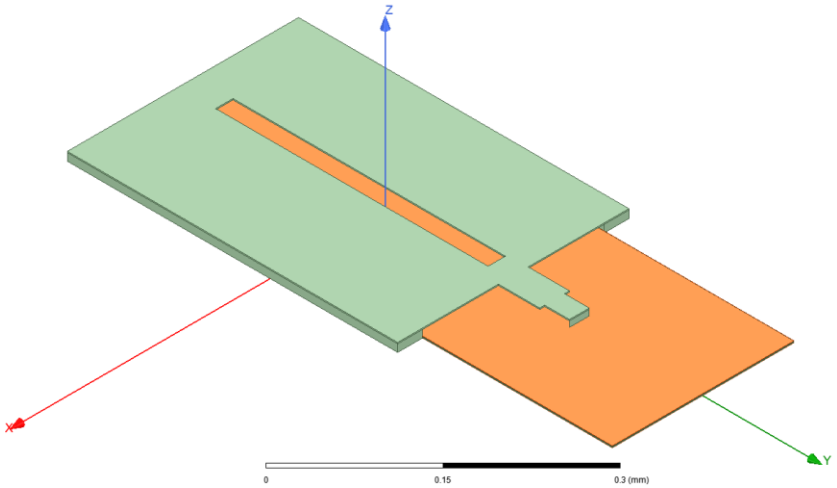


Fig 3.10. Ideal SIW slot antenna generated in Ansys HFSS

For the SIW slot antenna, the complete simulation and optimization was analyzed in Ansys HFSS 19.2. Firstly, the antenna simulation was done in Ansys HFSS considering approximate dielectric layers with top (M10 AP) and bottom metal layers (M1-M6) as solid metals. The metal conductivity was calculated from the thickness and sheet resistance value taken from the process design kit (PDK) document given by the TSMC 65-nm CMOS process. The conductivity for each metal followed the equation below:

$$\rho = \frac{1}{\sigma} = \frac{1}{R_{Sheet} T_{metal}} \tag{3.3}$$

Here, T_{metal} is the thickness of the metal sheet, ρ is the resistivity, R_{sheet} is the sheet resistance and σ is the conductivity of the material

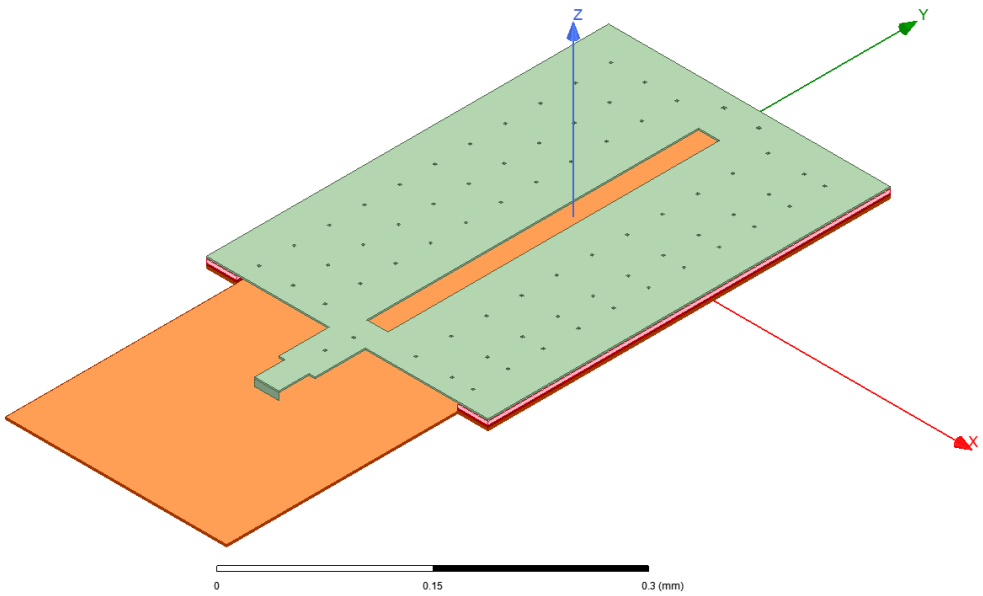


Fig 3.11. AP_only SIW slot antenna generated in Ansys HFSS

With all the values of the metal conductivity, an ideal SIW slot antenna was created in HFSS which contains all the solid metals in every layers. This SIW slot antenna model is named as Ideal SIW slot antenna due to all solid metal layers and it is shown in figure 3.10. After the parametric simulations of the ideal SIW slot antenna geometry in the HFSS, the optimum performance was

achieved. Then the optimized dimension was used to create the layout of the on-chip SIW slot antenna in Cadence Virtuoso layout design. However, it is impossible to generate the exact antenna Cadence layout in Ansys HFSS because of the limited memory of the computer. Because the Cadence layout contains many tiny metals and vias to satisfy the process design-rule restrictions and it is not possible to import exact same cadence layout in HFSS. Therefore, to mimic the actual antenna while keeping the vital places unchanged, we approximated some of the metal layers as total solid metal. All the metal layers from M1 to M9 was designed as a solid metal in HFSS while keeping the top aluminum layer (M10) exactly same as the cadence layout. Because the top aluminum layer is the most important layer that controls the EM radiation characteristics of the antenna. Moreover, we kept via 9 (RV) as same as the real layout because it is the largest via in dimension which controls most of the characteristics of the SIW sidewall. This SIW slot antenna model is named as AP_only model because of the exact metal 10 layers (AP layer) from the Cadence layout and keeping all the metal layers as solid. The AP_only model is shown in figure 3.11. To import the AP_only model in the HFSS software, the GDS file of the antenna layout model was exported from the Cadence virtuoso. Later, the GDS file was imported into HFSS software for which the tech file was needed to define each metal and vias of the GDS file. Tech file is usually created by the designer, and it contains layer number along with the elevation of the metal layer. The Process Design Kit (PDK) document given by the foundry was used to create the tech file where the layer number came from the stream file. After importing the GDS file in the HFSS, the tech file needs to be loaded to perfectly placed the metal layers according to the elevation of the metal layers. Finally, by appropriately assigning the metal conductivity of each metal layers mimics the actual antenna design in the HFSS. The tech file for TSMC 65 nm process is shown in Appendix A.

Table 3.1 410 GHz SIW slot antenna dimension

Name	Dimension
Feed length	30 µm
Feed width	24 µm
Taper length	50 µm
Taper width	36 µm
Slot length	330 µm
Slot width	21 µm
Slot offset from centerline	5 µm
Sidewall width	30 µm
Antenna length	480 µm
Antenna width	280 µm

3.4 SIW slot antenna radiation pattern

The simulated gain of the antenna is 0.1592 dBi. The E-plane and H-plane of the antenna are shown in figure 3.12 and figure 3.13 respectively. The half power beamwidth (HPBW) of the antenna in E-plane and H-plane are 142.2º and 57.64º respectively.

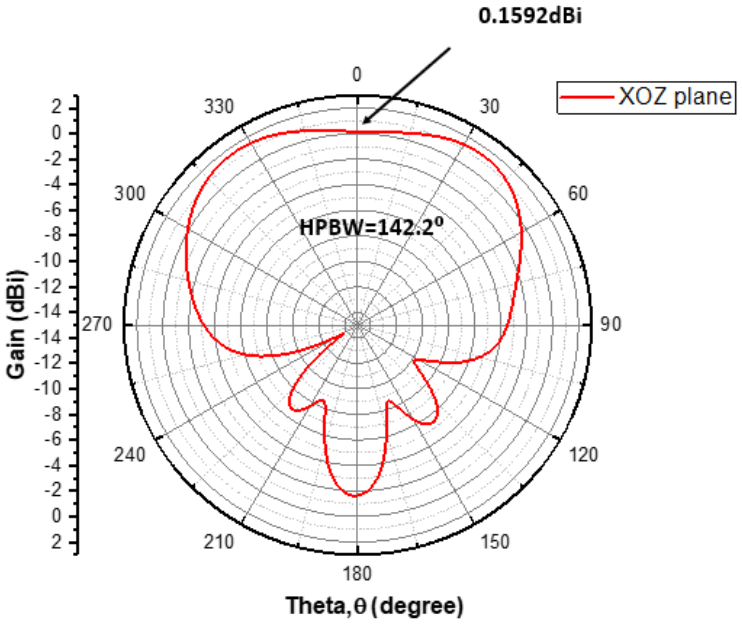


Fig 3.12. 2D radiation pattern of the SIW slot antenna at 410 GHz (E-plane; φ=0º)

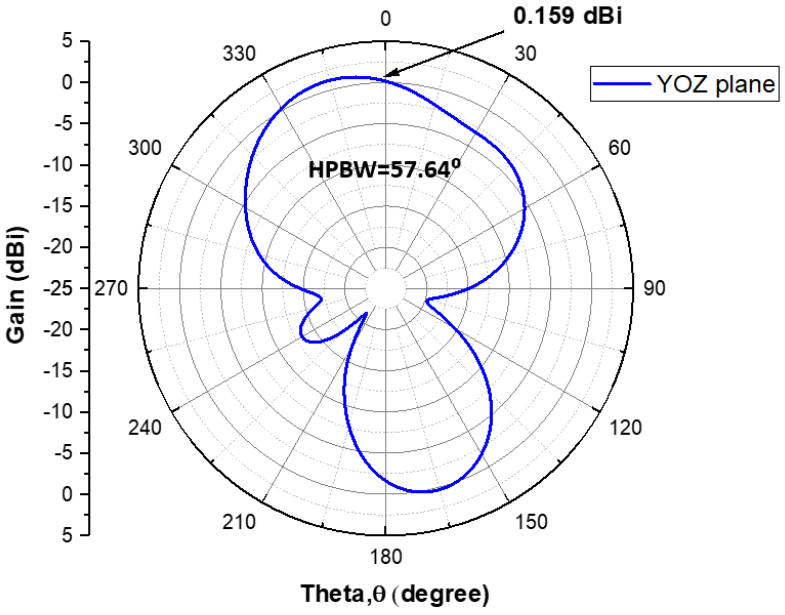


Fig 3.13. 2D radiation pattern of the SIW slot antenna at 410 GHz (H-plane; φ=90º)

Antenna radiation efficiency is one of the key factors of the antenna that explains how efficiently antenna radiates EM signal in the air. In our case, we simulated radiation efficiency of the antenna for both cases (Ideal model and AP_only model).

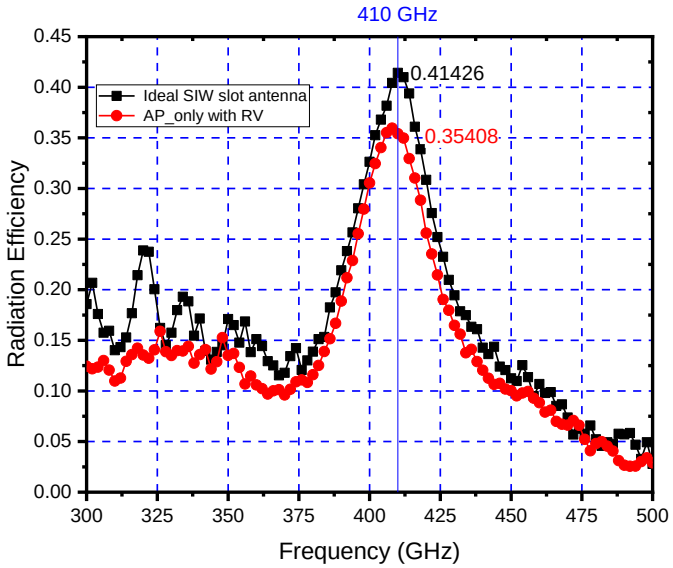


Fig 3.14. Comparison of SIW slot antenna radiation efficiency at 410 GHz

The ideal model exhibits antenna radiation efficiency of 41.4% at 410 GHz and the AP_only model shows radiation efficiency of 35.4%. The AP_only model shows little less radiation efficiency than the ideal model due to the real Aluminum layer structure which contains few punch holes, and it degrades the antenna radiation efficiency by a few percent. Moreover, we calculated and compared the -10dB bandwidth of the antenna for both cases. Each structure shows the -10-dB bandwidth of 20 GHz. Figure 3.15 shows the antenna bandwidth for both type of structures.

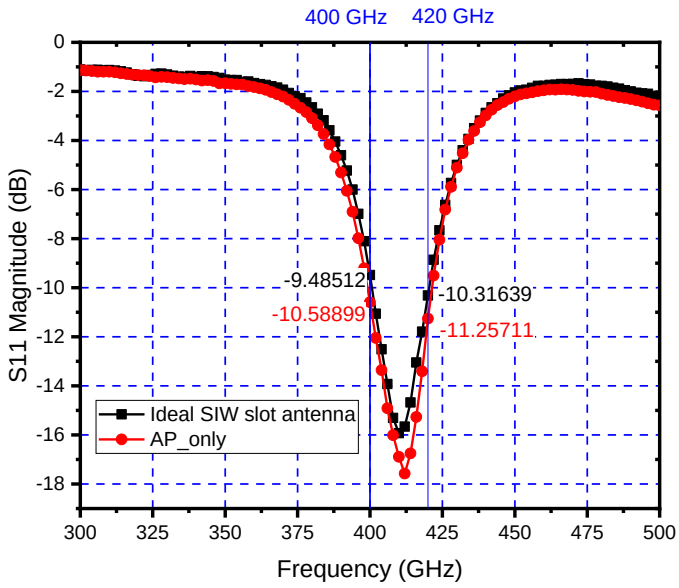


Fig 3.15. SIW slot antenna bandwidth comparison for both cases at 410 GHz

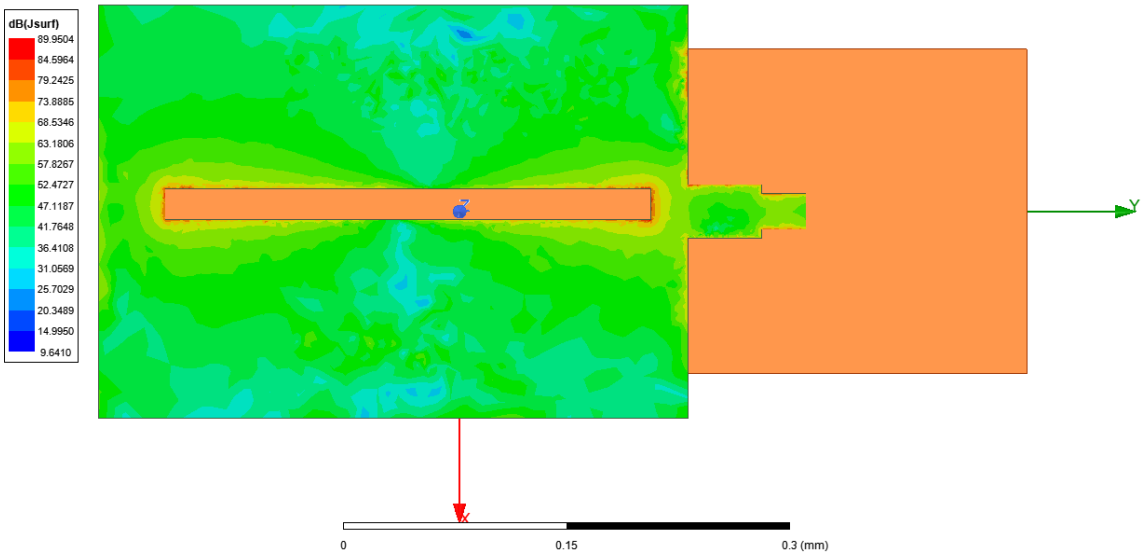


Fig 3.16. Surface current distribution of the antenna at 410 GHz

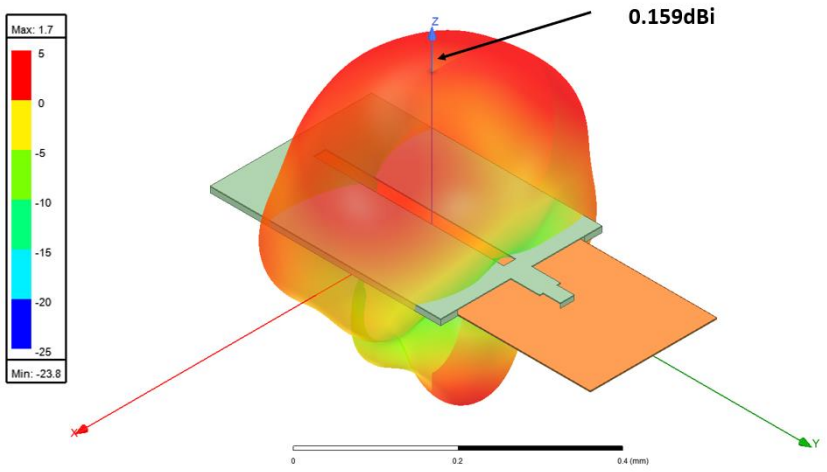


Fig 3.17. SIW slot antenna 3D radiation pattern

Fig. 3.16 and fig 3.17 shows the surface current distribution and 3D radiation pattern of SIW slot antenna. A comparison table of on-chip antennas has been shown in table 3.2.

Table 3.2 Comparison among different on-chip antennas

Reference	**This work**	[30]	[19]	[18]	[16]
Antenna type	SIW slot	SIW dual slot	Patch	Planar dipole	SIW slot
Frequency	410 GHz	270 GHz	280 GHz	540 GHz	460 GHz
-10 dB fractional bandwidth	4.9%	14.8%	2.5%	N/A	5.4%
Radiation efficiency	35%	~22%	21%	28% (w/ metal reflector)	30%
Polarization	Linear	Circular	Linear	Linear	Linear
Process	65nm CMOS	65nm CMOS	130 nm CMOS	40nm CMOS	65nm CMOS

From table 3.2, it is observed that our designed SIW slot antenna exhibits better radiation efficiency and moderate fractional bandwidth than all other advanced on-chip antennas.

CHAPTER IV

AC-COUPLED SIW SLOT ANTENNA DETECTOR CIRCUIT

4.1 On-chip antenna response measurement

It is challenging to measure the response of the on-chip antenna working at THz frequency range. One was to measure the performance is to build a demonstrator circuit. A demonstrator circuit mainly consists of three basic blocks: (1) On-chip antenna, (2) Matching network, and (3) diode connected transistor. It is easier to measure the antenna response by measuring the detector response. Typically, three different devices are used for THz signal detection such as- ColdFET, Schottky barrier diode (SBD), and Diode connected transistor. We used diode connected transistor due to the model availability in TMSC 65nm CMOS process.

4.2 Building AC-coupled SIW slot antenna structure

There is a minor problem with building the detector circuit with SIW slot on-chip antenna. At very high frequency (specially in THz frequency range), it is hard to achieve an ac coupling due to shorted sidewall of the SIW structure. A possible solution to resolve this issue is to work with an AC coupled SIW slot antenna. In this purpose, we have manipulated the sidewall of the SIW slot antenna to build a dc blocking capacitor. The sidewall (from metal 1 to metal 6) of the SIW structure is arranged such a way that metal 1, metal 3, and metal 6 are connected to the top structure which receive the RF EM signal. The meal 2, metal 4, and metal 6 are connected to ground. As a result,

the sidewall from metal 1 to metal 6 layers of SIW forms a capacitance between the layers as shown in figure 4.1. This capacitance works as a big chunk of series DC capacitance connected in series with the SIW slot antenna. This is how the SIW slot antenna turns into AC-coupled SIW slot antenna.

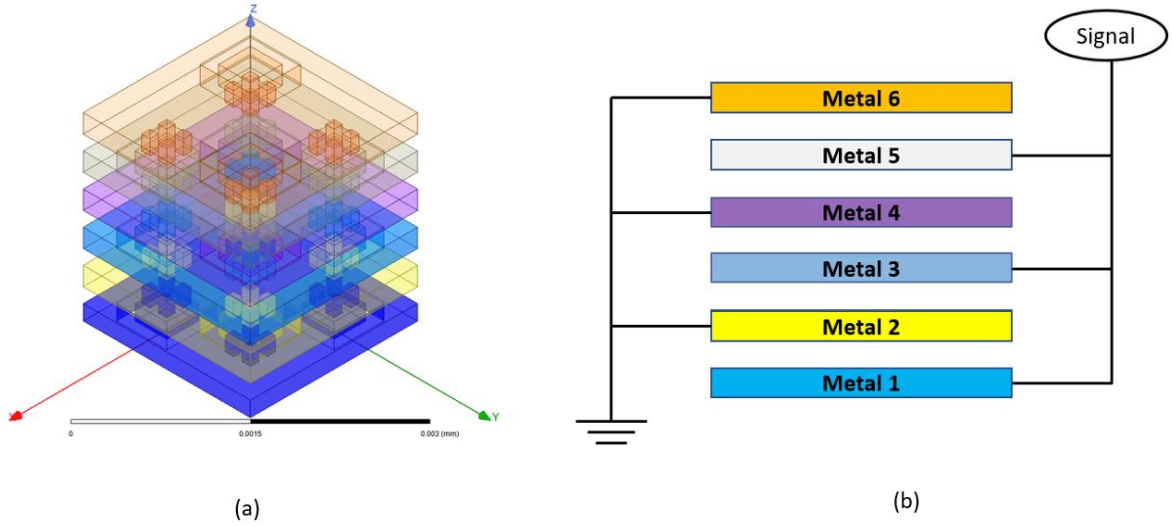


Figure 4.1. Arrangement of the SIW sidewall to build dc blocking capacitor
(a) unit cell HFSS structure (b) simplified structure

A simple representation of the SIW sidewall to build a dc blocking capacitor is shown in figure 4.1. Our total sidewall provides approximately 200 fF ac coupling capacitance that blocks dc signal from the SIW slot antenna. This capacitance isolates the RF signal from the DC bias signal coming from the diode bias applied to the transistor. The AC-coupled SIW slot antenna structure is a new idea which alleviate the need of extra DC capacitance tot the detector circuit.

4.3 410 GHz SIW slot antenna detector design

The SIW slot antenna detector consists of three different blocks: (1) AC coupled SIW slot on-chip antenna (2) Diode connected transistor, and (3) matching network in between transistor and antenna.

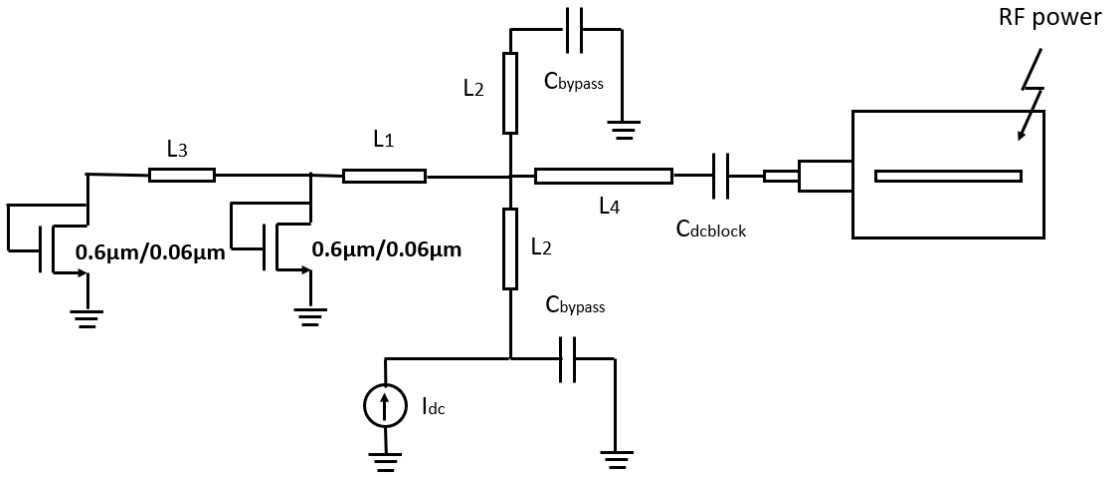


Figure 4.2. Schematic of AC-coupled SIW slot antenna detector at 410 GHz

The schematic of the 410 GHz AC-coupled SIW slot antenna detector is shown in figure 4.1. The full schematic contains one AC-coupled SIW slot antenna which receives the RF power. The AC-coupling phenomena is shown as a dc blocking capacitor ($C_{dcblock}$) in the schematics connected in series with the SIW slot antenna. The SIW slot antenna along with the dc blocking capacitor mimics the AC-coupled SIW slot antenna. For the diode connected transistor, we selected nmos_rf MOSFET from the TMSC65 nm PDK. Also, we used minimum transistor gate length of 0.06µm and minimum width of 0.6µm with number of fingers of 2. The nMOS RF transistors gate and drain are shorted together to work it as a diode connected configuration. To improve the power transfer

efficiently matching network is needed between the transistor and the antenna. A matching network built with Ground Coplanar Waveguide (GCPW) transmission line has been used between the diode connected transistor and the antenna. The microstrip transmission lines are L1, L2, L3, and L4 as shown in figure 4.2. The microstrip transmission line are in metal 9 level and the width of the GCPW transmission line was optimized to get 50-Ω characteristics impedance. The width of the metal 9 transmission line for 50-Ω characteristics impedance is 4μm. The GCPW microstrip transmission line characteristics impedance has been calculated using the S-parameters from two port simulations following the equation of reference [31].

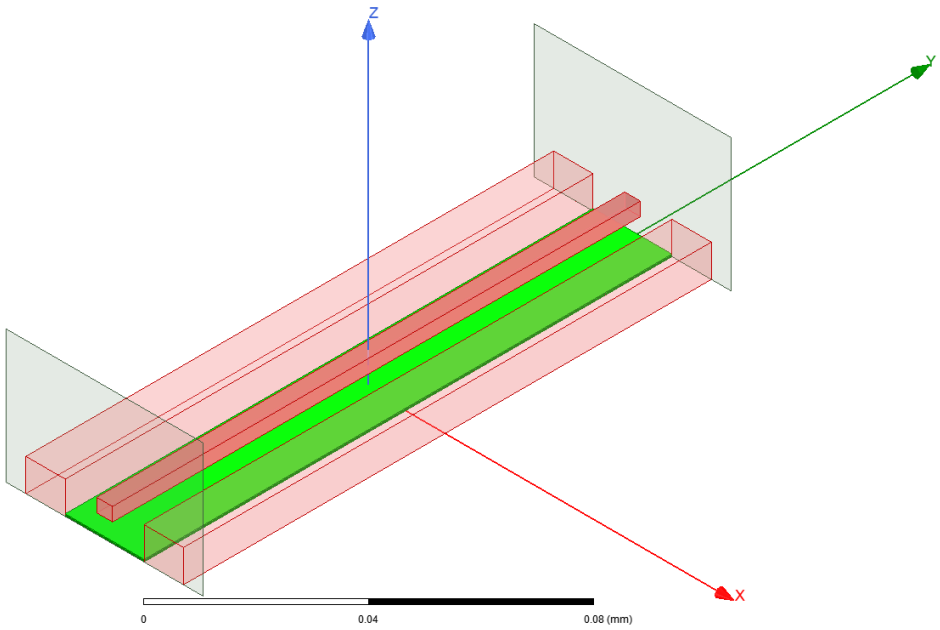


Figure 4.3. GCPW microstrip transmission line in HFSS

Figure 4.3 shows the GCPW microstrip transmission line structure generated in HFSS. For the GCPW configuration, shorted metal 1 and metal 2 is considered as ground (shown as green color in figure 4.3) where metal 9 is the signal layer. The whole GCPW transmission line is surrounded

by a ground line (pink color in figure 4.3) by shorting metal 1 to metal 9 together. To match the antenna with the diode connected transistor block, a GCPW transmission line of L4 (20 μm) is used. This is the shortest possible transmission line directly connected to the antenna feed line. The transmission line L4 is connected to a symmetric T-junction which contains short stub line of L2 (25 μm) on both sides. Other end of each L2 transmission lines is connected to bypass capacitance each containing a capacitance of 337 fF. The bypass capacitances shorted the 410 GHz RF signals. One of the transmission lines of L2 is directly connected to the DC current bias pad (Idc) to provide the bias current to the transistors. The bias current for the optimum performance of the detector is 5 μA. The T-junction is finally connected to the transistor through a GCPW series transmission line of L1 (17 μm).

The transistor gate and drain are in metal 1 layer but the incoming RF signal comes from the metal 9 layer through the GCPW transmission line matching network. Due to this high frequency RF signal flowing from metal 9 level to metal 1 level of the transistor it creates some parasitic in the transistor structure. The parasitic elements need to be included in the transistor structure to get the actual response from the simulation.

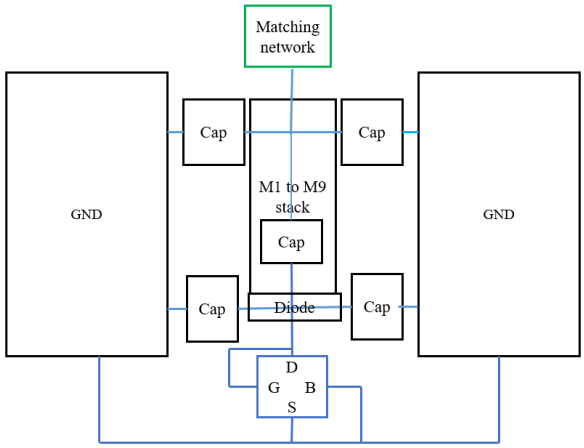


Figure 4.4. Transistor interconnect metal parasitic model

Figure 4.4 shows the transistor interconnect parasitic between the metals. This parasitic model can be representing as a π-network consists of capacitance (Cp), inductance (Lp), and resistance (Rp).

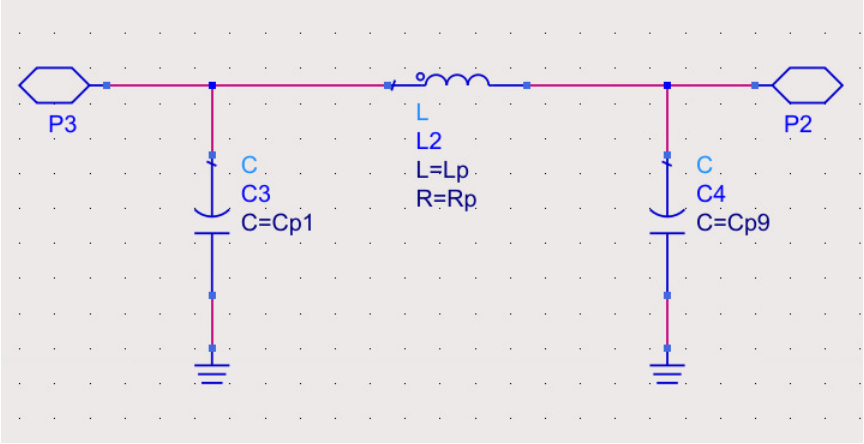


Figure 4.5. Transistor parasitic π-network model

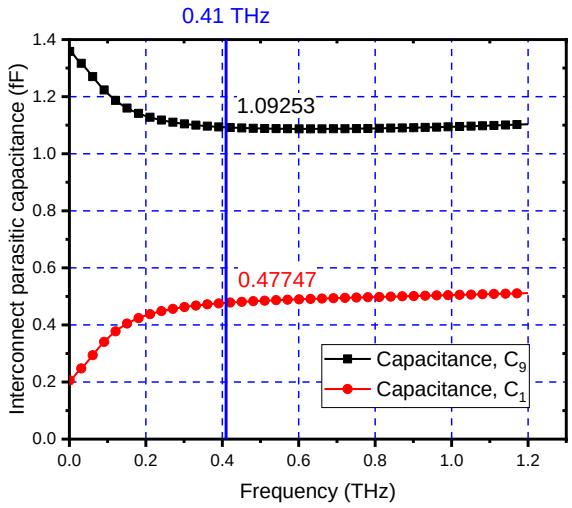


Figure 4.6. Interconnect parasitic capacitance

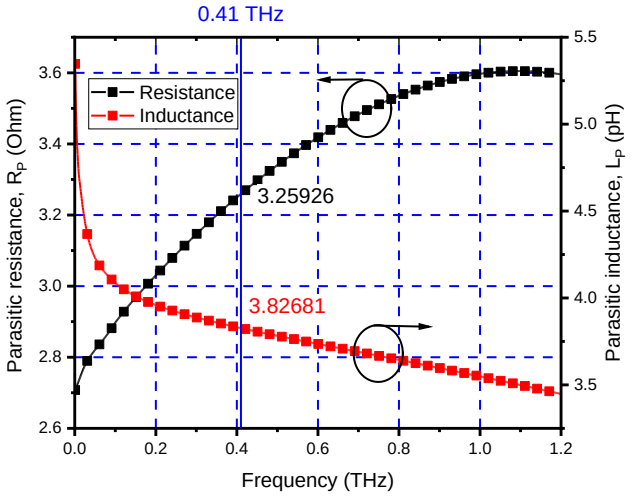


Figure 4.7. Interconnect parasitic resistance and inductance

From the S-parameter simulation, the transistor interconnect metal parasitic has been calculated. Measured parasitic inductance and resistances are 3.83 pH (Ls) and 3.26 Ω (Rp) respectively as

shown in figure 4.7 . The interconnect capacitances are 0.47 fF (Cp1) and 1.092 fF (Cp9) at 410 GHz as shown in figure 4.6. The transistor 3D interconnect metal is shown in figure 4.8. The interconnect metal starts from metal 1 and ended up at metal 9 where the blue and green structure are metal 1 and metal 2 respectively.

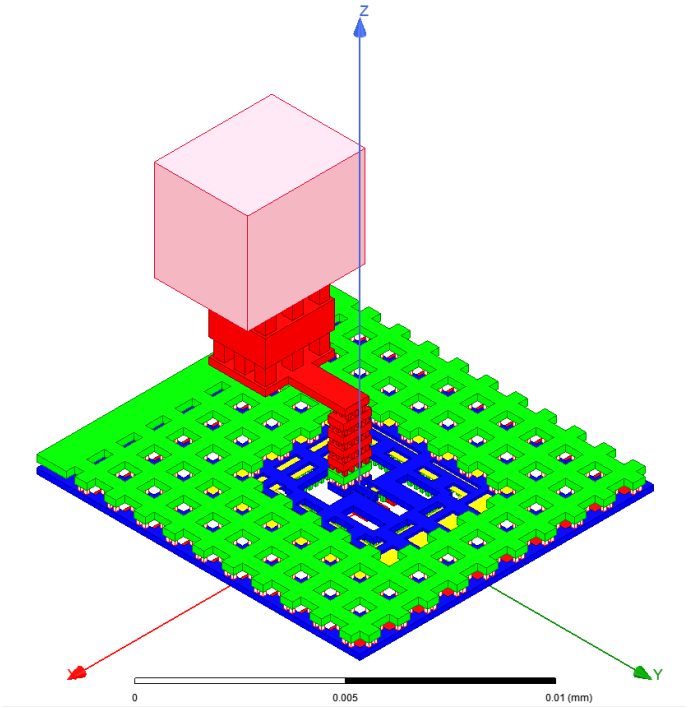


Figure 4.8. Transistor interconnect metal 3D structure

4.4 Detector performance

The full detector circuit contains an AC-coupled SIW slot antenna, a matching network, and two branch of parallelly diode connected NMOS transistors each containing two transistors. The full detector circuit is shown in figure 4.9 exported from the Cadence layout and approximated to HFSS version considering crucial metal layers as same as the man structure.

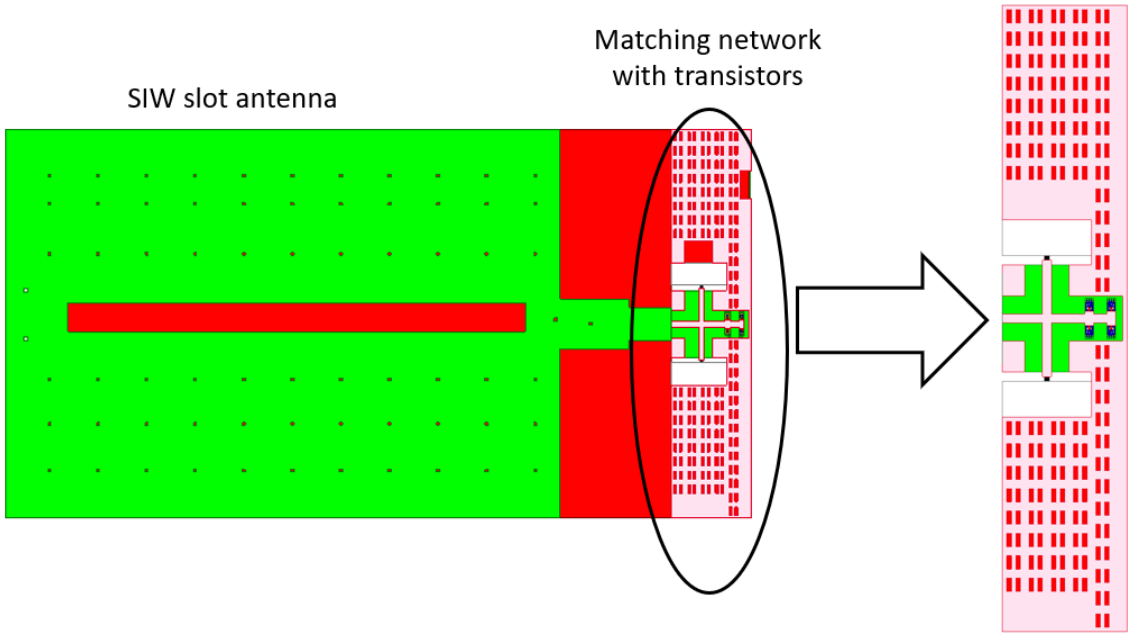


Figure 4.9. 410 GHz AC-couped slot antenna detector circuit

Since demonstrator circuit is called square law detector circuit, its output voltage is proportional to the input incident RF power to the antenna. One of the key performance parameters of this detector is voltage responsivity (R_V) which is the ratio between the rectified DC output voltage and the input power.

$$\text{Voltage responsivity, } R_V = \frac{\triangle V}{P_{in}} \tag{4.1}$$

Another key performance metric for the detector is the Noise Equivalent Power (NEP). NEP is defined as the input RF power level at which the detector signal to noise ratio (SNR) is unity for 1-Hz bandwidth. Alternatively, it is the ratio between the output noise voltage spectral density and the detector voltage responsivity. With the interconnect parasitic model of the transistor, the number of diodes connected transistor is varied to get the optimum performance from the detector.

We found four number of branches proves highest voltage responsivity and minimum Noise Equivalent Power (NEP).

$$\text{NEP} = \frac{\sqrt{\overline{V}_{n,out}^2}}{R_V} \tag{4.2}$$

Here, $\sqrt{\overline{V}_{n,out}^2}$ is the output noise spectral density.

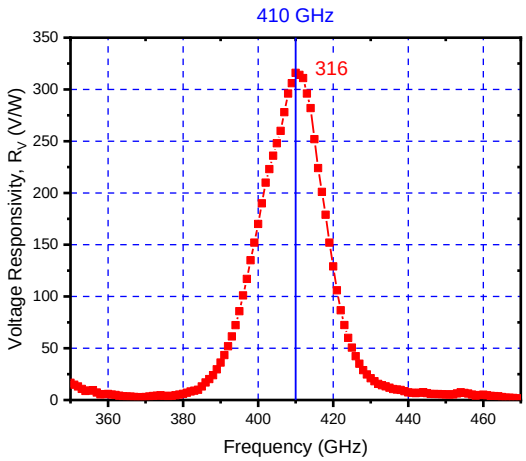


Figure 4.10. Voltage responsivity for the 410 GHz detector

Figure 4.10 represents the voltage responsivity of the detector circuit. The responsivity follows the antenna radiation efficiency variation with respect to frequency and peaks at 410 GHz. The voltage responsivity for the 410 GHz SIW slot antenna detector is 316 V/W.

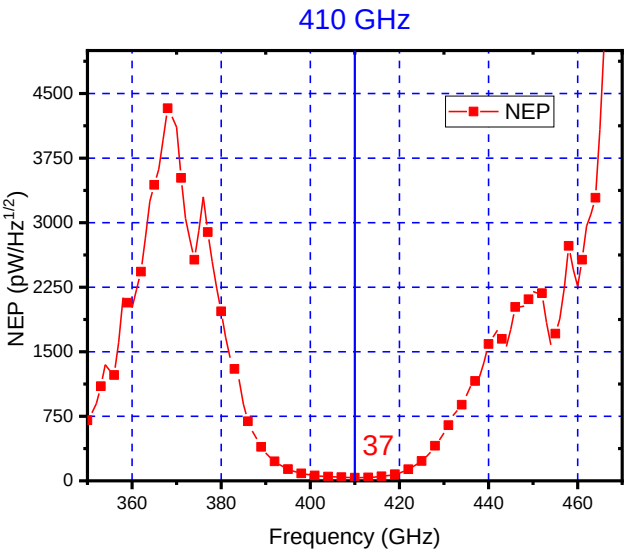


Figure 4.11. Noise Equivalent Power (NEP) for the 410 GHz detector

The simulated flicker noise corner frequency is 1 MHz, and the output noise spectral density is 11.7 nV/√Hz. From the responsivity and the output noise spectral density of the detector the NEP at 410 GHz is 37 pW/√Hz. Table 4.1 compares among different detector performance with their processing technology.

Table 4.1 Comparison among different detector performance

Detector type	Frequency	Antenna	Max responsivity (kV/W)	Min NEP ($pW/Hz^{1/2}$)	Reference
Diode-NMOS in 130nm CMOS	823 GHz	patch	2.56	36.2	[36]
65 nm SOI NMOS	650 GHz	Folded dipole+si.lens	1.93	17	[32]
130nm NMOS	600 GHz	Bow-tie	216	25.9	[35]
130nm SiGe HBT	315 GHz	dipole	6.1	21.2	[34]
130nm SiGe HBT	260 GHz	Diff. ring	2600	8.4	[33]
Diode-NMOS in 65nm CMOS	410 GHz	SIW slot	.316	37	This work

CHAPTER V

CONCLUSION, CONTRIBUTION, AND FUTURE WORK

5.1 Thesis summary

A 410-GHz AC-coupled SIW slot antenna integrated with a detector circuit has been designed in this thesis for THz applications. This detector circuit can be used for THz imaging. The full detector circuit was designed in TMSC 65nm CMOS process and sent to the foundry for fabrication. The chip will be characterized later after receiving the circuit from the foundry.

Chapter 1 introduces the THz signal and its importance in modern wireless communication and medical applications. Along with the importance of sub-millimeter wave the motivation to build a detector circuit for on-chip antenna response measurement has been shown.

Chapter 2 presented the state-of-the-art of on-chip antenna, possible challenges to build on-chip antenna and their response measurement. Moreover, it also illustrates the common ways to build a detector circuit and their use in on-chip antenna performance measurement and imaging applications. Finally, it shows how a SIW slot antenna works following Babinet's principle.

Chapter 3 describes the on-chip SIW slot antenna design in TSMC 65 nm CMOS process. In this purpose, the TSMC 65nm metal stack layer has been shown and the how this metal layer has been manipulated to design the SIW slot antenna. Also, the limitation of the Ansys HFSS software to

mimic the actual layout of the antenna in this software has been shown. The tech file and the metal rules imposed by the foundry has been shown here. To find the dimensions of the antenna has been shown using different parametric simulation. After explaining all the things, the performance of the on-chip SIW slot antenna has been presented. The radiation efficiency of the antenna is 35% and the -10dB bandwidth is 4.9%.

Chapter 4 demonstrates the possible ways to a build detector circuit. The diode connected NMOS transistor detector circuit configuration has been used here owing to the availability of the transistor model files. The transistor interconnect parasitic extraction and matching network has been shown. Moreover, it is also presented that how the sidewall of SIW structure has been used to make an AC-coupled SIW slot antenna. The performance of the detector says that the proposed detector shows voltage responsivity of 316 V/W and the NEP of 37 pw/$Hz^{1/2}$.

5.2 Contributions

The 410 GHz SIW slot antenna presented in this thesis:

- Radiation efficiency is 35% at 410 GHz
- Achieved 20 GHz bandwidth at 410 GHz

The AC-coupled SIW slot antenna presented in this thesis:

- The SIW slot antenna sidewall usually DC shorted which is a great problem to build a detector circuit. The sidewall of the SIW slot antenna is used as DC capacitor which converted typical SIW slot antenna to AC-coupled SIW slot antenna. This AC-coupled idea is novel in this kind of structure.

The 410 GHz detector using AC-coupled SIW slot antenna:

- The detector exhibits the voltage responsivity of 316 V/W
- The detector shows NEP of 37 pW/Hz$^{1/2}$

5.3 Future work

To measure the performance of the detector circuit the measurement plan is in progress. After receiving the full chip from the foundry, the measurement will be done in the lab. The measurement setup is shown in figure 5.1

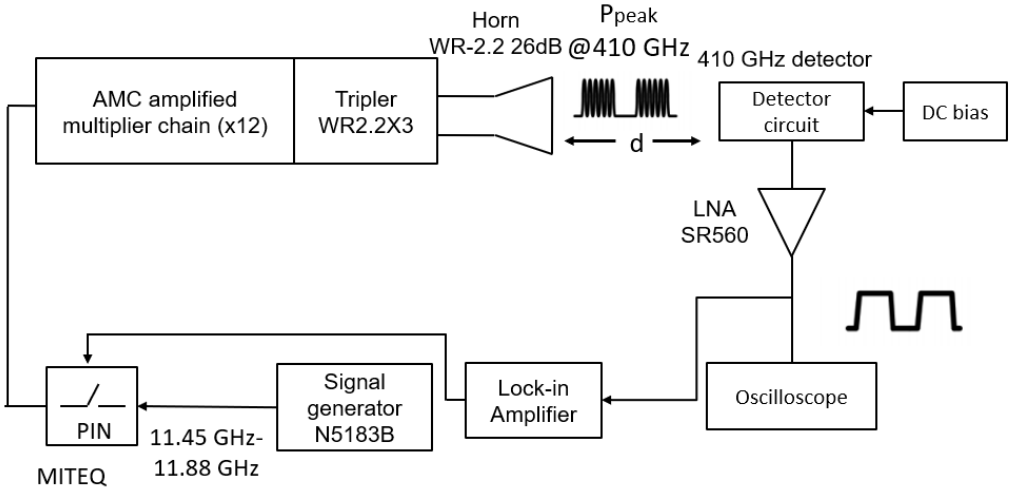


Fig 5.1 410 GHz detector circuit measurement set-up

The 410 GHz signal will be generated through equipment's. A signal generator N5183B will be used to generate 11.4 GHz AM modulated signal from the source. Followed by the signal generation, the signal will be passed through an AMC amplified multiplier chain with a factor of 12 and output power of 300 mW. Then, the signal will be passed through a frequency tripler which

will be used as an input to the WR-2.2 horn antenna with gain of 26 dBi. The horn antenna will radiate the peak power at 410 GHz. The distance between the horn antenna and the detector circuit can be controlled by the setup. The detector circuit needs to be biased with a current bias source which is 4155 and the required bias is 5µA. As the output signal from the detector is very low it will be needed to amplify to a certain value so that the oscilloscope can detect the signal. Since there was no on-chip low noise amplifier (LNA) in our circuit, an off-chip amplifier is needed to connect with the output. The LNA model is SR 560. The output will be taken at a chopping frequency of 1 MHz Finally, the output can be calculated from the oscilloscope.

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Appendix A

TSMC 65nm Tech file

Layer number	Layer name	Color	Elevation (nm)	Thickness (nm)
74	AP	green	9575	1450
85	RV	blue	8775	800
39	M9	pink	5375	3400
58	Via 8	red	4635	740
38	M8	red	3735	900
57	Via7	red	3140	595
37	M7	red	2920	220
56	Via6	red	2745	175
36	M6	red	2525	220
55	Via5	red	2350	175
35	M5	red	2130	220
54	Via4	red	1955	175
34	M4	red	1735	220
53	Via3	red	1560	175
33	M3	red	1340	220
52	Via2	red	1165	175
32	M2	green	945	220
51	Via1	snow	770	175
31	M1	blue	590	180
30	CO	green	400	190
17	PO	red	300	100
76	CB	white	590	8185
86	CB2	black	7075	0
3	NW	yellow	680	0

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