POWER OPTIMIZATION THROUGH CLOCK GATING STANDARD CELLS DESIGNED FOR OSU VLSIARCH SKY130 PROCESS

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POWER OPTIMIZATION THROUGH CLOCK GATING STANDARD CELLS DESIGNED FOR OSU VLSIARCH SKY130 PROCESS

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Abstract: This thesis proposes the integration of a D-Latch based clock gating cell into the OSU VLSIARCH SKY130 standard cell set, for power optimization purposes. In practice, clock gating is highly effective and easy to implement, making it ideal for standard cell set characterization. The integration of the proposed D-Latch clock gating cell provides a power reduction benefit to any design it is implemented into, though some designs benefit far more than others. Providing a powerful yet simple power optimization cell to the SKY130 cell set helps to improve standard cell performance, as well as final design benchmarks.

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CHAPTER I

INTRODUCTION

With the continued rise in the popularity of mobile applications, paired with decreasing feature sizes, power consumption reduction has become an ever increasing issue. Power optimization is a leading issue in the field of complementary metal-oxide semiconductors (CMOS) and the reduction of power consumption is now a key design principle for all modern CMOS logic. [1] and [2] showcase the criticality of power optimization for Very Large Scale Integration (VLSI) logic. For example, standards such as [1] and [2] are implemented to standardize the practice of power optimization in the academic and professional fields. Modern CMOS design processes rely on these power optimization standards in order to produce power forward design and synthesis processes. With power optimization becoming an ever-increasing aspect of VLSI logic design, this thesis looks to explore a current power reduction option for integration into the OSU VLSIARCH SKY130 nm cell set.

Power consumption for typical CMOS logic can be defined in two parts, static power and dynamic power. Static power manifests as a form of leakage current while the system is in a standby state. Though reduction techniques are available, static power only accounts for 10%-15% of total power consumption on average. The goal of this thesis is to reduce the dynamic power of the system. Dynamic power is produced primarily due to switching in the device, paired with active signaling. With switching power dissipation being responsible for a majority of dynamic power consumption, clock gating became a simple yet effective candidate for power consumption reduction.

The clock of a device can be directly related to switching and thus to switching

power dissipation. With this in mind the goal is to utilize clock gating as a method to optimize the dynamic power in the device. This method of power reduction is based around gating the clock signal before the other devices, in order to disable devices that are not in use. In practice, this reduces the clock tree at the cost of a slight increase to logical complexity. When implemented properly, clock gating can be a simple solution to reap large power savings. As can be seen from [3], [4] and [5], clock gating is a common method of power reduction in the field of CMOS. This new cell provides sizable reduction in the active power consumption of a device with minimal logical impact. Providing more utility than just power reduction, works such as [6] explore the use of clock gating cells for logic structure reduction. Finally, along with low logical impact and large performance benefit, a clock gating cell can also take on many forms. In [7], several designs for clock gating cells are demonstrated and highlighting how each design alters performance. Taking into account the logical simplicity, ample layout variety and benefit of clock gating cells in standard CMOS logic, it is easy to see how a clock gating standard cell benefits a standard cell set. It is for this reason this thesis implements clock gating to further optimize power performance of the Skywater 130nm standard cell set. However, even with the inherent advantages that come with clock gating, there is little documented work currently implementing these cells for power optimization in standard cell sets.

From [8], it is clear that clock gating can be an essential tool when looking to reduce power consumption. This thesis explores the use of standard cell clock gate integration. Though this work discusses the benefits of implementing a clock gate into a standard cell set, it focuses on the comparison of clock gate design. For this reason, it lacks the scope to show case the capabilities of clock gating cells to enhance existing sets. Better representing the scope of this paper, [9] presents a clock gating standard cell for the TMSC 250nm, 2.5V process. In this thesis a clock gating cell is designed and implemented to optimize a two-point calibration processor. Though this

helped to guide the decision to implement clock gating in the Skywater Technology 130nm (SKY130) cell set, the design presented in [9] is singular to the TSMC 250nm process. As discussed later, this is a drawback of using standard cells. Though they allow for easy placement and routing of designs, standard cell sets must be created and maintained for the process they are designed to characterize. With this in mind, the goal is to expand upon these works in order to further optimize the SKY130 standard cell set.

With modern CMOS designs rapidly reaching the trillions of transistors, the automatic placement and routing process of cells for a design layout has become an essential tool. In this process a layout is fed into the Place and Route (PnR) tool along with a Standard Cell Set. Using the characterized metric data of the cells in a cell set, a PnR tool is able to place all cells in a design and route the connections for them. With the ever increasing prevelance of the PnR process in the CMOS field, there is an equally large need for adequate standard cell sets. The OSU SKY130 standard cell set is a full suite, multi-track standard cell set created for the Skywater Technology 130nm process. Though the standard cell set is capable of synthesizing complex designs such as the RISC-V SoC, it is lacking in power optimization options. With clock gating cells being simple in design and implementation, they became an obvious option to further optimize the cell set. This paper will explore the use of clock gating devices and their effectiveness in the reduction of power consumption when implemented in the OSU SKY130 standard cell set.

The organization of this thesis is as follows. Section II will focus on the design of the clock gating cell for the SKY130 cell set. In this section we will begin by detailing the importance of standard cell sets, as well as how they are properly defined . We then explore the advantages of the proposed cell set additions, while discussing cell functionality. To add the most flexibility possible to the cell set, this section will also explore the design of a positive and negative edge triggered design for the proposed

cell. Finally, this section will further detail the advantages of the cells that were previously discussed. With a basis for the design and functionality of the proposed cell, we can then look at implementing and testing the proposed design in devices of varying complexity.

Section III discusses the design and gating of the three test circuits, each with increasing degrees of complexity; a basic 6-bit counter, a shift and add multiplier and finally we will look at the cell's capabilities when gating the datapath of a RISC-V System on Chip (SoC). In order to fully assess the functionality and effectiveness of the proposed clock gate, each implemented design will be probed in a passive and active stimulus state.

The use of the Cadence Design System and the Synopsys Design System, as well as the testing stimulus, will be discussed in IV.For passive stimulation, we will allow the synthesizing tool to derive an average power consumption with no additional user input. Conversely, for active we will provide stimulation to the synthesis process and probe the power consumption over the period of activity. By looking at both the passive and active scenarios, one can determine the effectiveness of the proposed cell at reducing power in average and stressed activity scenarios. The difference in the power consumption of these states helps to demonstrate the use of the proposed cell in a range of scenarios.

The results that were gathered will be compiled and discussed in Section V. All results are found using the Cadence Design System and Synopsys Design Systems and the cells were characterized using the OSU VLSIARCH SKY130 design flow. This thesis is able to quantify the effects of the proposed design, as well as directly speak to the efficiency of clock tree reduction via clock gating. Finally, comparisons of the Energy-Delay Product (EDP) of each implementation in order to determine the performance of each design with and without the clock gating cell. This final metric helps to quantify the efficacy of each design and allow for a more direct comparison of

their performance. Final observations, comparisons and remarks are made in Section VI.

CHAPTER II

BACKGROUND

A standard cell is a pre-characterized cell used in System on Chip (SoC) design. The pre-characterized information contained in a standard cell pertains to the cells metrics, such as; timing, delay, power consumption data and critical path information to name a few. The key design trait most standard cells in a set share is equivalent height. This equivalent height allows standard cells to fit easily beside one another within the defined tracks.

In comparison, custom logic cells are fully customizable cells that are designed from scratch for a specific application. The key difference between standard and custom cells, as outlined above, is the equivalent height and precharacterized nature of the standard cell. While full-custom cells are highly optimizable and completely flexible, they are also very design intensive, expensive to create and can only be used for the application they were designed for. By comparison, though a standard cell is predefined with set height and metric data, the cells are reusable in a variety of designs. Moreover, when using an automatic place and route tool, standard cells drastically reduce the required computation time and allow for easier placing of the cells by the tool.

Modern CMOS logic is rapidly reaching trillions of transistors, automatic Placement and Routing (PnR) has become essential to the completion of designs. With automatic PnR being a key step to realizing modern CMOS logic, it is clear to see how standard cell sets have also become essential to the process. By combining a defined list of standard cells into a library,one can fully realize CMOS design logic

through the placement and routing of the standard cells.

2.1 Building a Valid Standard Cell Set

Though briefly touched on in Section I, the development of a reliable and versatile standard cell set is a key step in the production of modern CMOS logic. Outlined in [10], standard cell sets provide critical data to the PnR tool in order to produce functional designs. Key aspects of standard cell completeness are as follows; functional completeness is essential, sets must include cell metric data such as power dissipation, delay and capacitance and finally the cell set should include cells of varying track size and drive strength. The functional completeness of a cell set is a tool dependent list of cells that must be included in the input cell set for the PnR tool to function. This list typically consists of a latch, flip-flop, buffer, inverter and either (AND and OR) or ($NAND$ and NOR) cell. These cells are considered to be the baseline set required for the PnR tool to operate. A key note however is that these cells merely give the tool enough to initialize basic HDL logic. In order to improve the performance of the cell set, and subsequently the PnR process, each cell is reproduced with varying track sizes and multiple drive strengths.

Introducing a variety of size and drive strength cells to the tool allows for the cell set to generate increasingly accurate designs. The inclusion of cell variety creates a more flexible cell set that is capable of characterizing a wider range of designs. In the case of the SKY130 cell set this is realized through the introduction of three track sizes and three drive strengths; 18 track, 15 track, 12 track and high strength, medium strength and low strength. By creating the most versatile standard cell set possible and properly characterizing the library, one can optimize CMOS logic. However, there is a current lack of power optimization options in the SKY130 cell set. With this in mind, and with the simplicity and effectiveness shown in Section I, we explore the introduction of a clock gating cell to the current SKY130 standard cell set.

2.2 Introducing the Clock Gate

The clock gate is a common means of power optimization that sees most of its use in synchronous systems. As stated before, the basic idea behind the clock gating cell is to act as an intermediate signal buffer between the device clock and device logic. Through the clock gating cell, the clock tree can be pruned to prevent sub-sections of the device from receiving a clock signal when not in use. This can lead to high reductions in dynamic power dissipation, as we are reducing concurrent switching activity as well as passive power dissipation due to clocking. Being capable of such power reductions while maintaining a simple structure makes clock gating a good choice for standard cell libraries, especially with power conservation in mind. This simplicity extends to both the positive and negative edge activation cases, as shown below.

As briefly discussed in the introduction, currently there are no power aware cells in the SKY 130 standard cell set that assist in power optimization. This means that though the standard cell set is capable of abstracting the functionality of logic, it is not finding the optimal result. The addition of the clock gating cell allows for greater flexibility of the cell set, while maintaining ease of implementation. These cell introductions also allow the OSU SKY130 standard cells to synthesize designs with more competitive power benchmarks. With simplicity the goal for many standard cell sets, this thesis integrates a latch-based clock gate for power reduction needs.

2.3 Positive-Edge Triggered Clock Gate

The design for our positive-edge triggered clock gate can be seen in Figure 2.1. In this design, an enable and active-high scan enable signal are integrated into a NOR gate. The NOR output is then used as the D-latch enable signal, on the D-port of our latch. Finally, in order to achieve proper clock gating on ECK, we must AND together the

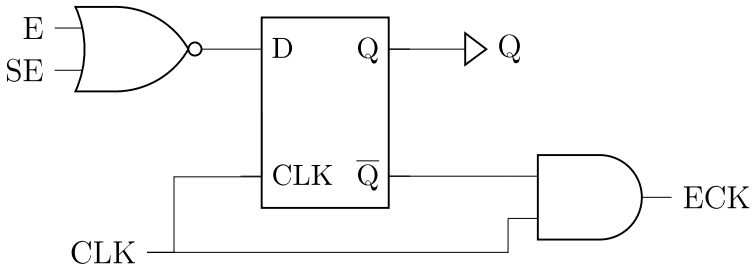

Figure 2.1: Positive-Edge Triggered Clock Gate Design

latched output signal with the clock. What this achieves is a controlled clock signal that is only active when E = 1, SE = 1 or E = SE = 1.Table 2.3 demonstrates the complete truth table for the positive-edge clock gate.

From Truth Table 2.3, the functionality of the positive-edge clock gate is defined. On line one we can see the active-high functionality we are expecting. In this state we set the next Q state, Q[n+1], and the next gated clock state,ECK[n+1], to be the current latch output. It is interesting to note that this activation state is performed regardless of the input of either E or SE. This is because on the activation cycle, regardless of the D-latch output, the OR gate will activate and produce an ECK signal. We use the latch in order to control whether or not the clock will be emulated on ECK output pin for the gated device upon clock cycle [n+1].

Lines two through four of Truth Table 2.3 pertain to how the output pin of the latch will be updated in the [n] state. It can be seen that that this decision is made between the NOR gate and the latch during the negative clock state. What this means

CLK	E	SE	Q[n+1]	ECK[n+1]
1	x	x	Q[n]	Q[n]
0	0	0	0	0
0	1	x	1	0
0	x	1	1	0

Table 2.1: Truth Table for Positive-Edge Design

for the proposed design is that though the clock gating cell as a whole is positively triggered, our D-latch must be triggered by the negative clock edge. This is so we are able to update the latch output in the half-cycle before state [n+1] occurs. Knowing this we can see in the zero clock state, lines two through four, we observe standard D-latch functionality. With the cell updating in the half-cycle before [n+1], we are able to set the proper state for line one of table 2.1. Now knowing the full functionality we are able to generalize the functionality of the proposed cell as follows. While in a negative clock state the cell will read the enable signals and will make a decision on the output for state [n+1]. Upon the start of state [n+1] we are in the latching state for the integrated D-latch, which holds the negative clock state decision. Finally, pairing the latched output with the clock signal will determine the output of ECK and thus if ECK will emulate the clock signal in state [n+1].

Given this functionality, it is evident that clock gating cells are capable of pruning the clock tree. When enabled the clock gating cell acts as a simple buffer, it allows the clock signal to reach the device relatively unaffected. There is naturally a slight increase in delay due to the addition of the extra logic. However, due to the negatively triggered update cycle, paired with simple decision logic, the additional delay is nearly negligible. In theory, when implemented the proposed cell grants massive power reduction benefits due to the pruning of the inactive branches of the clock tree. We will see in Chapter III that the delay introduced by the proposed cell is greatly outweighed by the power savings in most designs. Moreover, the simplicity of the logic allows for the cell to be implemented on several clock paths meaning we can optimize individual sections of a device.

Finally, in this thesis the functional While fully defined 18 and 12 track design sets, as well as high and low strength 15 track designs, are created for cell set integration, only the 18 track, medium strength synthesized designs are discussed in this thesis.

All layouts presented in this thesis are developed using the Magic VLSI tool [11].

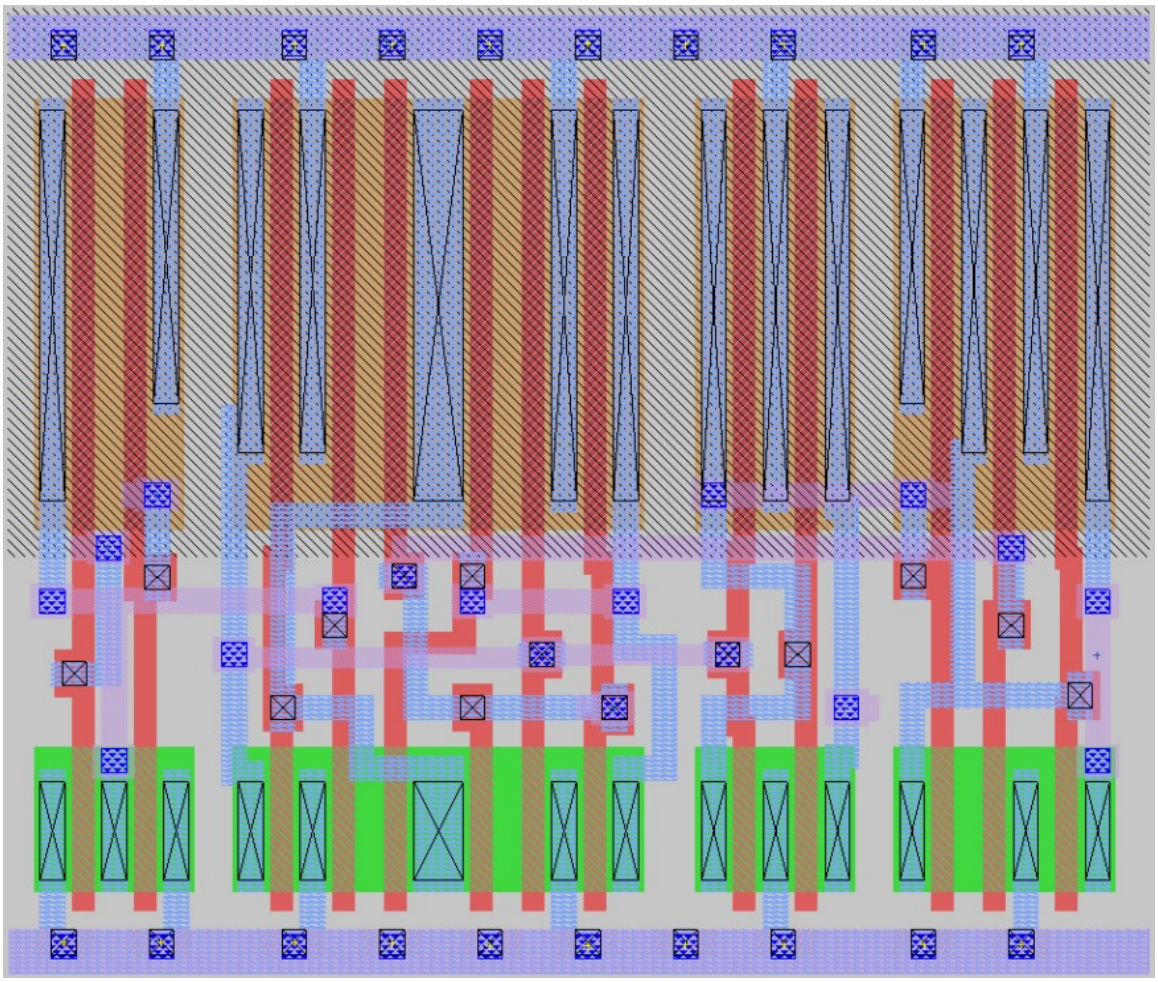

Figure 2.2: Functional Layout for SKY130 18 Track, Medium Strength Clock Gate

Recall that the clock gating cell to be integrated in the cell set was created using cells already native to the SKY130 kit. Designing the clock gates for each track and strength allowed for seamless integration of the clock gate into the cell set. Figure 2.3 has been included to clarify layout functionality.

2.4 Negative-Edge Triggered Clock Gate

The main goal for the addition of this clock gate is to increase power optimization but also to improve the flexibility of the SKY130 standard cell set. In order to better achieve this, the addition of a negative-edge triggered clock gate is also necessary. By implementing both trigger cases for the standard cell set, we can ensure that we are

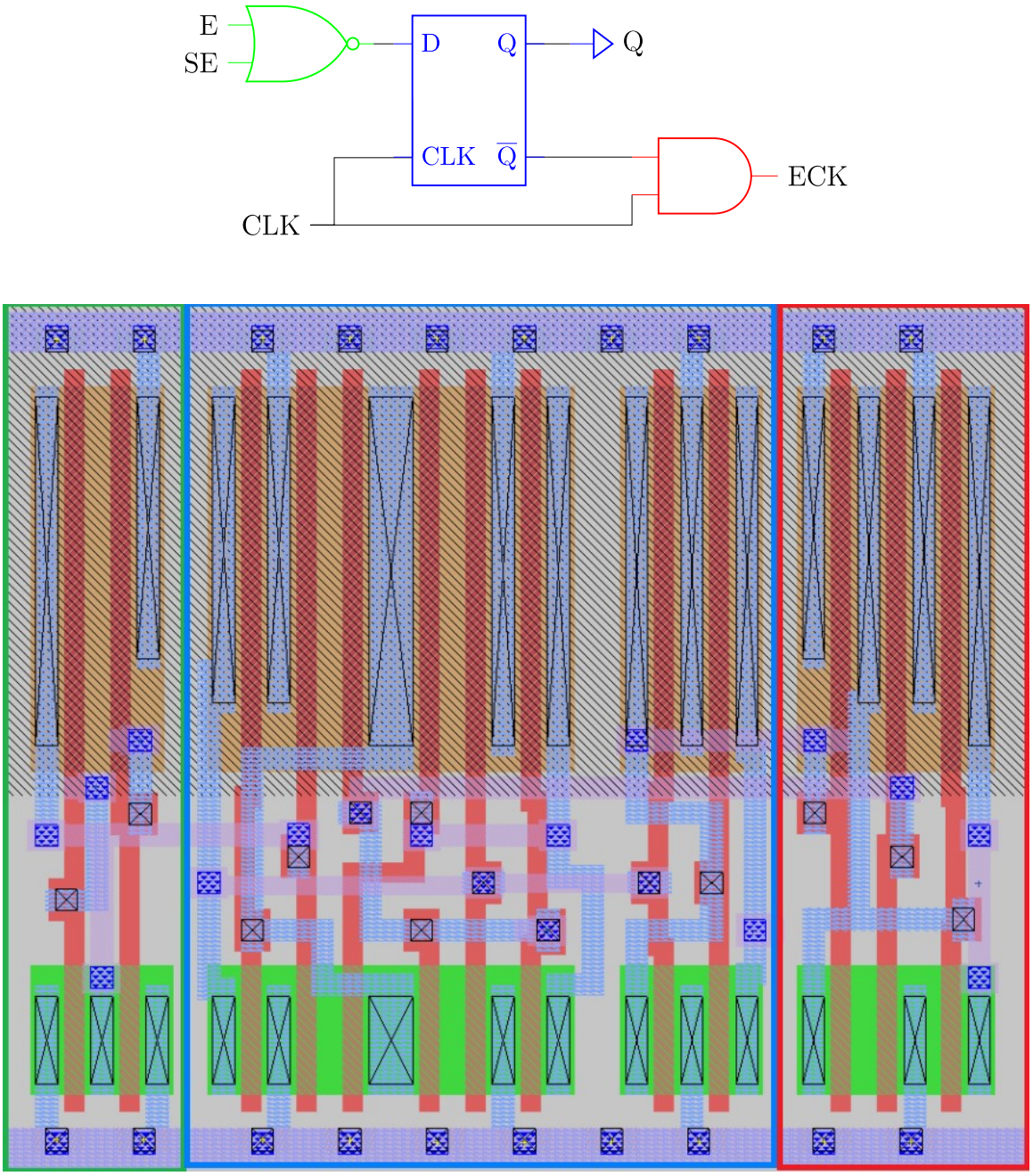

Figure 2.3: Annotated Layout With Coded Schematic

able to optimize power in any design using the SKY130 cell set. The negative-edge triggered clock gate is similar to the positive edge with the key difference being the inverted latch functionality paired with an OR gate for the decision output. This results in our cell being driven on an active-low signal, while performing the updating cycle in the positive clock state, opposite of the positive triggered gate.

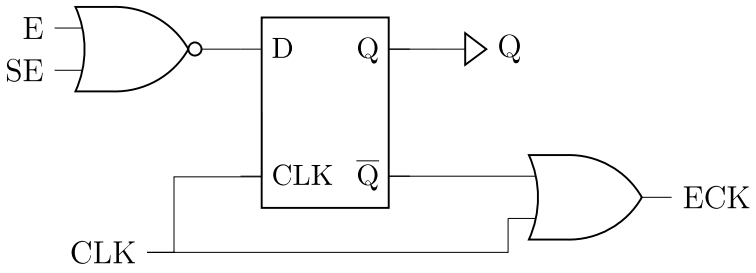

Figure 2.4: Negative-Edge Triggered Clock Gate Design

Table 2.2 displays the functionality of the negative edge triggered clock gate. Compared to the positive edge gate we discussed from table 2.1, this cell performs its activation cycle during the negative clock state. The negatively triggered gate then performs its updating cycle in the positive clock state. Therefore, the D-latch that is implemented in Figure 2.4 must be triggered on the positive edge. This clocking difference can be best seen in the layout for the negatively triggered clock gate.

The highlighted region in Figure 2.5 displays the key difference between the two designs, except for the decision logic cell discussed earlier. Here we are simply altering the path of the clock through the latching logic. Combined with the altered decision logic cell to determine ECK, this change was enough to produce the negatively triggered clock gate. Figures 2.2 and 2.5 only further illustrate the potential of the proposed clock gating design. The designs have low logical complexity, a small cell foot print and can be designed using the existing cells from the SKY130 process. All of which make the proposed cell designs strong candidates for use in the SKY130

CLK	E	SE	Q[n+1]	ECK[n+1]
0	x	x	Q[n]	Q[n]
1	0	0	1	1
1	1	x	0	1
1	x	1	0	1

Table 2.2: Truth Table for Negative-Edge Design

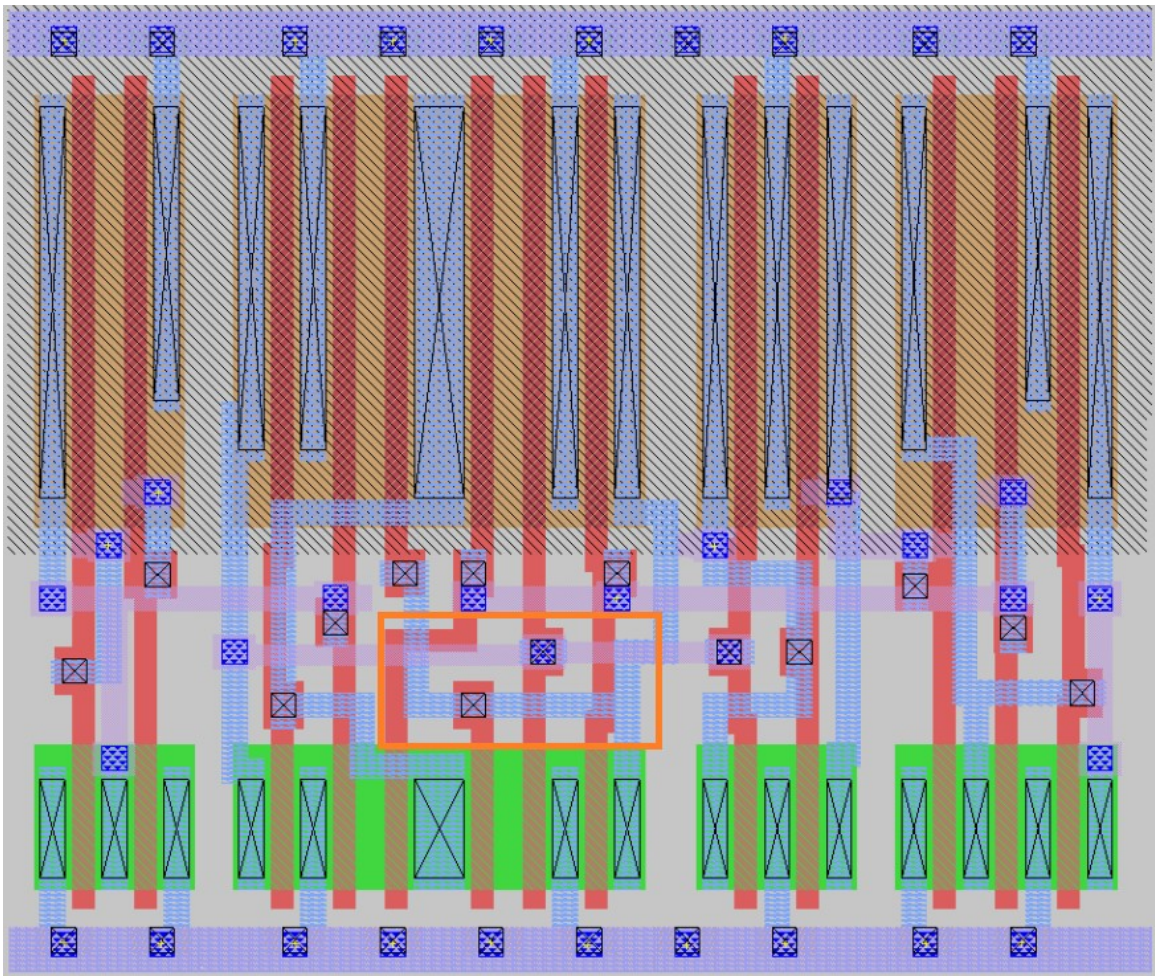

Figure 2.5: Layout of Negatively Triggered Clock Gate

process.

From this discussion we have explored, in detail, the functionality of both the positively and negatively triggered clock gate designs. The simplicity and efficiency of these designs makes them great candidates for a power aware standard cell library. Moreover, the theorized power savings greatly out weighs any increase in logical complexity or delay for most designs. With knowledge of the functionality and shortcomings of the designs, we are now able to characterize the new cells for integration into a standard cell library.

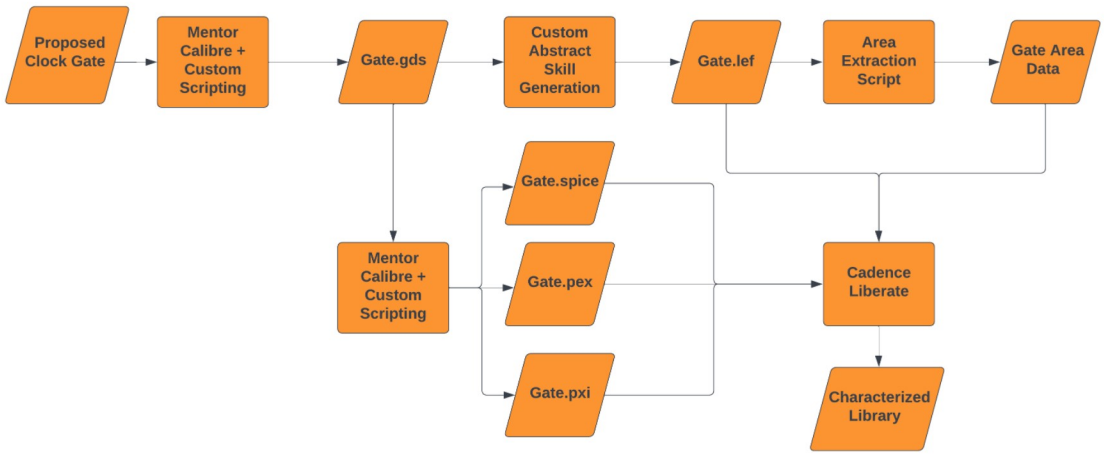

Figure 2.6: OSU VLSIARCH SKY130nm Characterization Flow

2.5 Standard Cell Set Characterization

Figure 2.6 outlines the characterization process for the SKY130 cell set. In this flow we first read the cell layouts and using an in house scripting flow, the GDS files for the layouts are created. The GDS file is a binary file format that represents information about the layout, such as geometric shapes and text labels, in a hierarchical form. This file is able to be used as an input to detail the device design for many modern VLSI tools as we can see above. We then import the GDS into two in house scripting flows, one to generate pin placement information and another to generate a set of SPICE files. Using the pin placement information from the LEF file we are then able to generate an area data file. Finally, once we have generated the SPICE, LEF and area extractions we then import the data into the Cadence Design System (CDS). The CDS is able to take the input information and generate power, timing and other design metrics for each specified input cell. Once the metrics have been generated for the set of defined cells, all data is then compiled into the final characterized library. It is this output library, along with HDL that will be outlined in Section III, that is used for synthesis.

The final note of mention is the fact that there is little support for the characteri-

zation of these cells. Due to the clock being required for normal clocking functionality in the cell, as well as being used for an output decision variable, the characterization tool struggles to recognize functionality. With this being the case, much of the flow needed to be extensively refined and customized to account for the new clock gating cells. This included a naming and mapping of all connections in the gate to allow us to force the characterization tool to probe certain pin locations. With an updated and customized flow, the ability to effectively characterize and implement the proposed clock gates is achieved.

CHAPTER III

IMPLEMENTATION

The key use of the clock gating circuit is for power optimization. In this section, through the gating of increasingly complex designs, it is demonstrated that the proposed clock gating devices are capable of significant power reduction. As discussed in Chapter I, we will be looking at the benefit of using the proposed clock gates when implemented in a 6-bit counter, a shift and add multiplier, and finally in a RISC-V SoC. These designs were chosen to show a large range of complexity as well as a large variety of power consumption amounts. This will allow us to see how the proposed cells will react under a full range of scenarios to best compare performance in a variety of scenarios. Note that all designs and power estimations were generated using the Synopsys Synthesis tools.

3.1 6-Bit Counter

The proposed test counter is a synchronous 6-bit counter, made from the combination of two 3-bit counters, which store their current count to a register bank. This is a good baseline design to test the clock gating cells on, as at any given time one to two of the 3-bit counters and their associated register cells will be inactive. With this being the case, we are able to use our gate to disable the clock signal to those subsections to deactivate them while they are idle, thus reducing concurrent switching power. By deactivating the sub-sections of the counter when not in use we expect to see a reduction in the power consumption of the counter. The design of the 6-bit counter ,as well as associated HDL code, is given below.

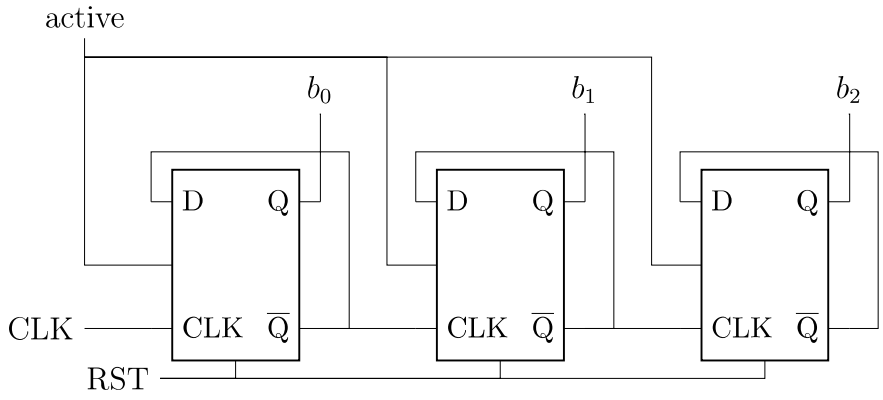

Figure 3.1: Basic 3-Bit Up Counter with active signal

With the 3-bit counter designed, the 6-bit counter was the simple combination of two 3-bit counters. I built the counter this way specifically to have two separate devices contributing to the count. This would mean that one device, in our case C_1, would handle a heavier load than the second counter, C_2. This is due to the fact that C_1 is incriminating the three least significant bits of the final count. Because of this, C_2 will only ever need to increment, in other words be active, once $temp_1 = 3'b111$. We will explain the implications of this design in Section 3.1.1. Figure 3.2 shows the

```
‘timescale 1ns / 1ns

module counter(input active,
               input clk,
               input rst,
               output reg [2:0] count);



        always @(posedge clk or posedge rst)
                if(rst)
                        count <= #1 3’b0;
                else if (active)
                        count <= #1 count + 1;
endmodule
```

Listing III.1: Verilog Code for a 3-Bit Counter

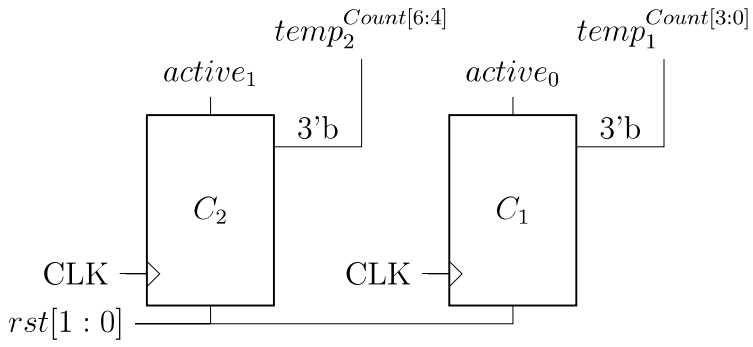

Figure 3.2: 6-Bit Counter

design of the 6-bit counter, this figure is accompanied by the relevant HDL code.

3.1.1 Clock Gate Implementation

The 6-bit Counter was intentionally designed with the testing of the clock gating logic in mind. In figure 3.2, we can see that the final count is effected by two distinct devices, each with a connection to the clock. It is on these clock signal lines that we

```
`include "counter.sv"

module multi_count(input [1:0] active,
                   input clk,
                   input [1:0] rst,
                   output [5:0] count);

        reg [2:0] temp1;
        reg [2:0] temp2;

        counter c1 (active[0],clk,rst[0],temp1);
        counter c2 (active[1],clk,rst[1],temp2);

        assign count = {temp2,temp1};

endmodule
```

Listing III.2: Verilog Code for a 6-Bit Counter

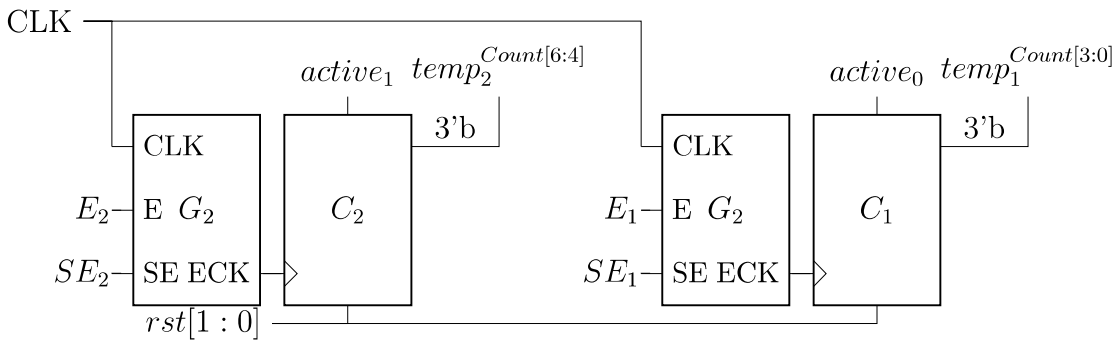

Figure 3.3: Gated 6-Bit Counter

can add the proposed clock gating logic.

We are now able to see the benefit in designing the 6-bit counter using two 3-bit counters. By doing so there are now two devices that we can control the activity of. This allows us to control when the devices are functioning, or in this case we control when the counter will begin incrementing. As discussed before, C_1 will be

```
‘timescale 1ns / 1ns
‘include "counter.sv"
module gated_multi_count(input [1:0] active,
                    input clk,
                    input [1:0] rst,
                    output [5:0] count,
                    output [1:0] q);
        reg [2:0] temp1;
        reg [2:0] temp2;
        sky130_osu_sc_18T_ms__pcgate gate1
                (.ECK(eck0), .Q(q[0]), .E(active[0]),.SE(1'b0), .CK(clk));
        sky130_osu_sc_18T_ms__pcgate gate2
                (.ECK(eck1), .Q(q[1]), .E(active[1]),.SE(1'b0), .CK(clk));
        counter c1 (active[0],eck1,rst[0],temp1);
        counter c2 (active[1],eck2,rst[1],temp2);
        assign count = {temp2,temp1};
endmodule
```

Listing III.3: Verilog Code for a Gated 6-Bit Counter

incrementing the three least significant bits of the count. This means that until we need to increment C_2, which is every time $temp_1 = 3'b111$ or every seven clock cycles, it is being actively clocked and consuming power. By gating the clock of the device and disabling the counter when it is not needed we are able to save large sums of power. In Listing III.3, we can see the ease of implementation when using these clock gating cells. There is no need for additional I/O logic or internal routing logic other than the insertion of the clock gate into the clock path of the 3-bit counters. By then routing the output of the clock gate, pin ECK, into the clock input for the counters, as shown in Figure 3.3 we are able to control when each device will receive a clock signal. Finally, we disable the Scan Enable (SE) pin in order to use the same input $active_{[1:0]}$, to control activation of all logic in the design.

3.2 Shift and Add Multiplier

The second test case that will be explored is a shift and add multiplier (SAM). The SAM was chosen for the second test case since multipliers are known high power consumption devices. With this in mind we present the HDL code and flow chart for the SAM to be synthesized.

As can be seen from Listing III.4 and Figure 3.4, the functionality of the SAM device will be as follows; following activation, the device will read in two input values A and B, then initialize the $Product$ register. At the positive edge of the clock, assuming $rst = 0$, the zero bit of input B, B_0, will under go a check. If $B_0 = 1$, the current value for A will be added to the $Product$. After this addition, and in the case of $B_0 = 0$, the multiplier will then shift the A register one bit to the left and

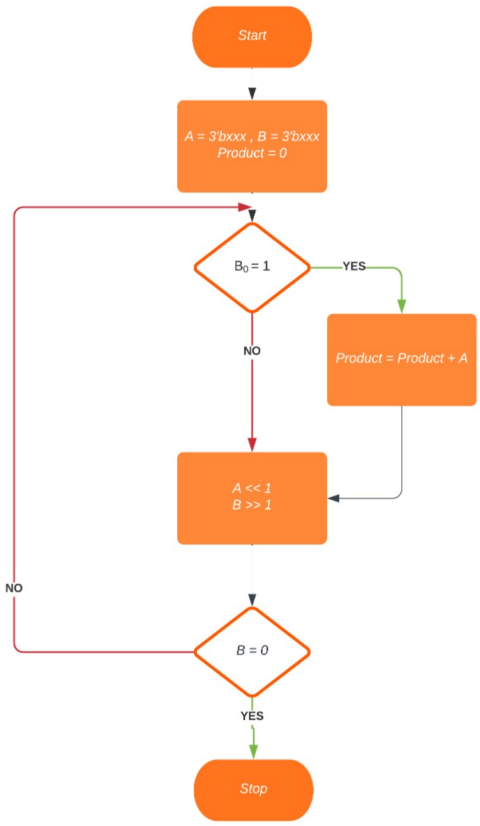

Figure 3.4: Logic Flow for Shift and Add Multiplier

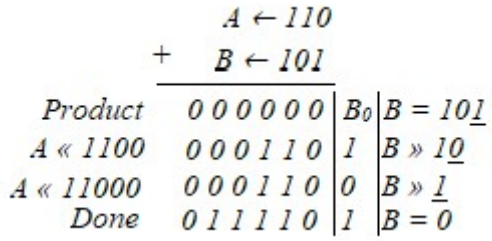

Figure 3.5: Shift and Add Multiplication Example

the B register one bit to the right. When done repetitively, the central check for B_0 will add A to itself B times, thus producing $A \times B$. The final logic pertains to the stopping function for the multiplier. This is realized through the use of a flag that will be activated once $B = 0$. Remember that the B register is being shifted to the left and used for a decision input. This implies that so long as $B > 0$, there is still an addition that must occur. However, once $B = 0$ we have exhausted all additions, thus the multiplication operation is completed. A simple example multiplying $A = 110$ and $B = 101$ can be found in Figure 3.5.

3.2.1 Clock Gate Implementation

Again, the SAM device was designed in such a way that the proposed clock gating cell would exhibit the most effectiveness. This was done through the extension of the zero flag to an I/O port. Recall that the zero flag will be disabled while the multiplier is active, then will be set to 1 while idle. By inverting the zero flag value and using it to activate the clock gate, we are able to take advantage of the logic of the multiplier to also control the clock gate. This means that though there will be a slight increase to device complexity due to the gate, there is no additional control logic needed to properly gate the clock of the SAM device. The proposed design to be tested can be seen in Listing III.5

```
`timescale 1ns/1ns
module sam (input reg [2:0] A,
            input reg [2:0] B,
            input clk,
            input rst,
            output reg zf,
            output reg [5:0] Product);
        reg[5:0] temp_Prod;
        reg[5:0] A_shift;
        reg[2:0] B_shift;

        reg zero_flag;
        assign zf = zero_flag;
        always @ (posedge clk or posedge rst) begin
                if(rst) begin
                        temp_Prod <= 6'b000000;
                        A_shift <= 3'b000+A;
                        B_shift <= B;
                        zero_flag <= 0;
                end else if (!zero_flag && !rst && (B_shift != 0)) begin
                        temp_Prod <= (B_shift[0] == 1) ?
                                (temp_Prod + A_shift) : temp_Prod;
                        A_shift <= A_shift<<1;
                        B_shift <= B_shift>>1;
                end

                zero_flag <= (B_shift == 0 && !rst) ? 1'b1 : 1'b0;
        end
        assign Product = temp_Prod;
endmodule
```

Listing III.4: Verilog Description of SAM

3.3 RISC-V Datapath

Our final test case will involve the gating of the clock signal of the data path of a RISC-V processor designed and synthesized using the SKY130nm cell set. The design is a fully functioning RISC-V SoC, capable of processing the full RV32 instruction

```
‘timescale 1ns/1ns
module gated_sam (input reg [2:0] A,
             input reg [2:0] B,
             input clk,
             input rst,
             output q,
             output reg zf,
             output reg [5:0] Product);

         sky130_osu_sc_18T_ms__pcgate gate1
           (.ECK(eck), .Q(q), .E(!zf), .SE(1'b0), .CK(clk));

         sam sam
           (.clk(eck),.A(A),.B(B),.rst(rst),.zf(zf),.Product(Product));
endmodule
```

Listing III.5: Verilog Code for a Gated SAM

set. RISC-V is an open standard ISA based on reduced instruction set principles [12]. The ISA comes in 32 and 64 bit variants and due to its open-source nature, along with proven capabilities, it is ideal for academic use. The design that is proposed is a fully functioning RISC-V SoC, capable of processing the RV32 instruction set. This design serves as the final integration test for all cells in the SKY130 cell set. By incorporating new standard cells into the set and re-synthesizing the design we can compare how cell additions will effect performance output. These tests will be covered in more detail in Section IV

3.3.1 Clock Gate Implementation

Due to the chosen clocking location we will mainly be looking at the difference gating can make when implemented into the data-path clock. This means that we will be performing a very general test of the cell. Note that the benefits of the clock gating could be greatly increased by gating the sub devices of the data-path. However, this

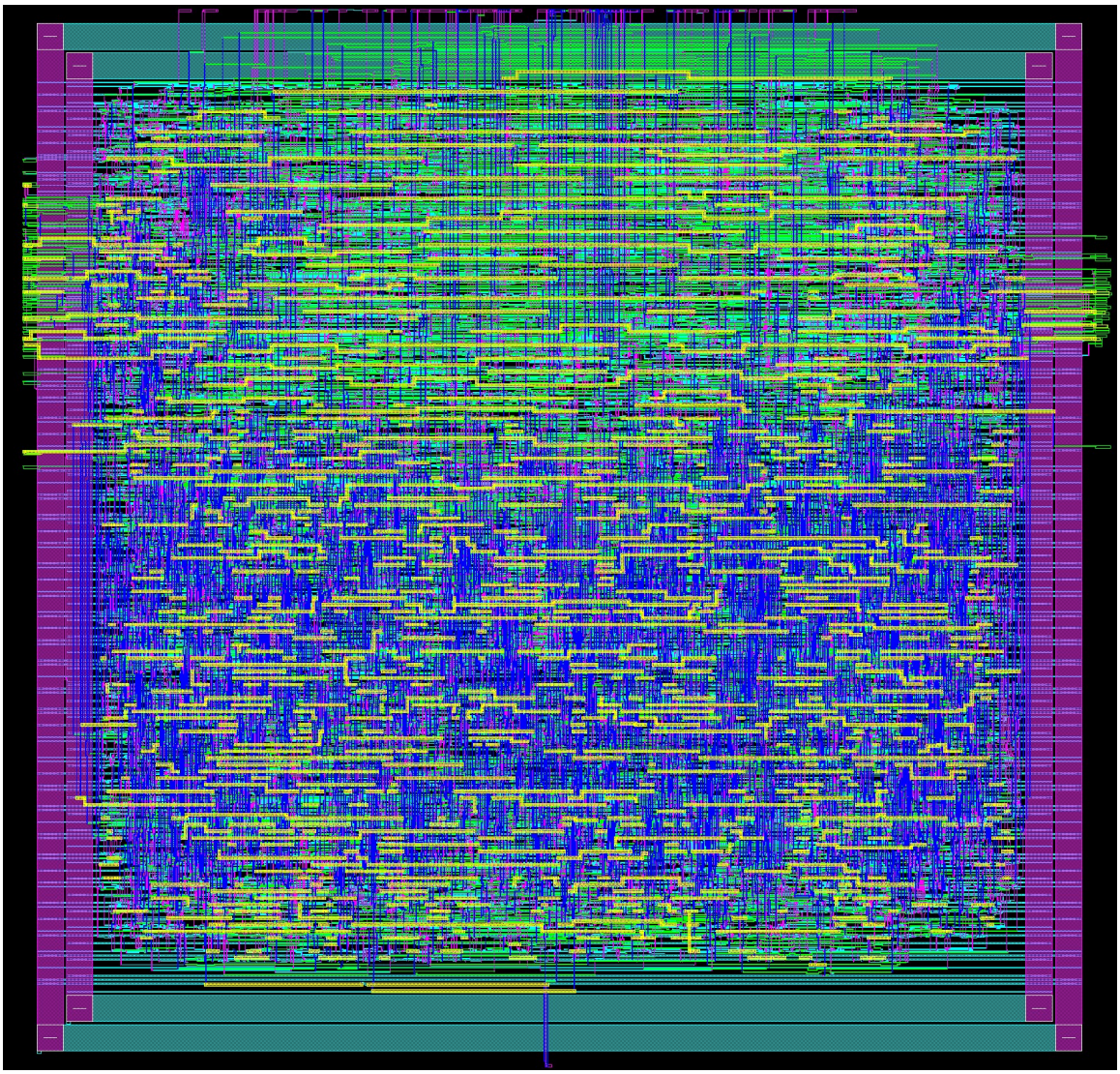

Figure 3.6: Result of Automatic PnR Process on Gated RISC-V SoC

is far too refined of a test for cell set functionality and integration testing. For this reason we will only look at the scenario when the data-path is clocked in order to ensure proper functionality of the gating cell, along with proper interaction of the new gating cell with the rest of the cell set.

Finally to ensure proper functionality of the standard cell set with the new gating cells integrated, we perform the PnR process. Recall that it is during this automatic PnR process that the layout presented in Figure 3.6 is created using the provided set of characterized cells.

CHAPTER IV

TESTING

All testing for this paper was done using a combination of the Cadence Design Systems and Synopsys Design Systems. Using the Cadence Design System we are able to characterize the standard cell set. The characterization process produces a database of metrics for each of the cells in the SKY130 cell set. By combining the characterized metrics of the standard cell set, along with HDL code to define the layout of the cells, we can accurately simulate a design using Synopsys tools.

HDL, along with a characterized standard cell database, are both required to properly synthesize and probe a design in the Synopsys design suite. Once the design is successfully synthesized it will be probed in order to determine design characteristics such as timing, critical path and power consumption. It is from the output of this probing that we derive the results for Section V. All designs were clocked with a period of 20ns, or frequency of 50 MHz, which is an average clock speed for the SKY130 cell set.

4.1 Passive Stimulation Testing

Testing was done in two phases, using passive stimulus and using active stimulus. For the purposes of this paper, Passive Stimulation is used to define a test scenario in which we provide no stimulus to the synthesis and probing of the designs. Passive stimulation testing relies more on the estimations of the tool for the functionality of the design. In these cases, the Sysnopsys synthesis tool is given no directive for the switching in the design, hence the passive nature of the tests. This output first

completes the synthesis process, then will attempt to determine the average power consumption of the device by estimating switching activity. By taking into account the design under passive stimulus, both gated and not gated, we will be able to quantify the efficiency of the proposed gating cells. In order to refine our metric estimations, we are able to provide stimulus data in the form of a switching activity file.

4.1.1 Datapath Stimulus

As briefly discussed in Section III, the passive stimulus test of the clock gating cell when incorporated into the RISC-V SoC will be the only test performed on this device. There are two reasons for testing the device this way; firstly, due to the positioning of the clock gating cell any test that is performed on the device will activate the gated clock. This means that we will derive very little information from the active case as the clock gate will always be active. Therefore, we primarily only perform the passive case in order to reduce the redundancy of our final data. Along the same lines as reducing our final redundancy, we also want to maintain our scope of testing.

Due to the construction of the SoC there are only two viable clock gating options; in the top level where presented in Section III and within the data path device. The top level of the design was chosen to maintain our scope of testing. This top level gating in the passive stimulus state still gives insight on the interaction of the new cells with the current cell set and to the effectiveness of the gating cell. This means that while gating each sub portion of the SoC would lead to a larger benefit overall, it doesn't contribute any new information toward the effectivness of the proposed cell. It is for these reasons that the full SoC will remain passively stimulated for the purposes of this paper

4.2 Active Stimulation Testing

By incorporating the switching activity file, we provide the synthesis tool with a directed test to simulate design switching activity. We define tests incorporating a switching activity file to be Active Stimulus tests. The addition of the switching activity reinforces the design functionality as well as providing state data for the synthesis tool to use during probing. Generating the more directed tests will generate refined performance data and thus a better estimation of the power efficiency of the designs discussed in Section III.

4.2.1 Counter Stimulus

The directed stimulus for the 6-bit counter was the first test generated and least power intensive design to be tested. During the testing period the counter, after initialization, will be activated and begin counting. The test will allow for the design to increment from 6'b000000 to 6'b111111 at which point the device is deactivated and the probing period is concluded. This test file is able to provide switching data for every state of the 6-bit counter. By incorporating this data into the synthesis tool we are able to measure power consumption under high device activity. Stimulus of the 6-bit counter, both gated and not gated can be seen below.

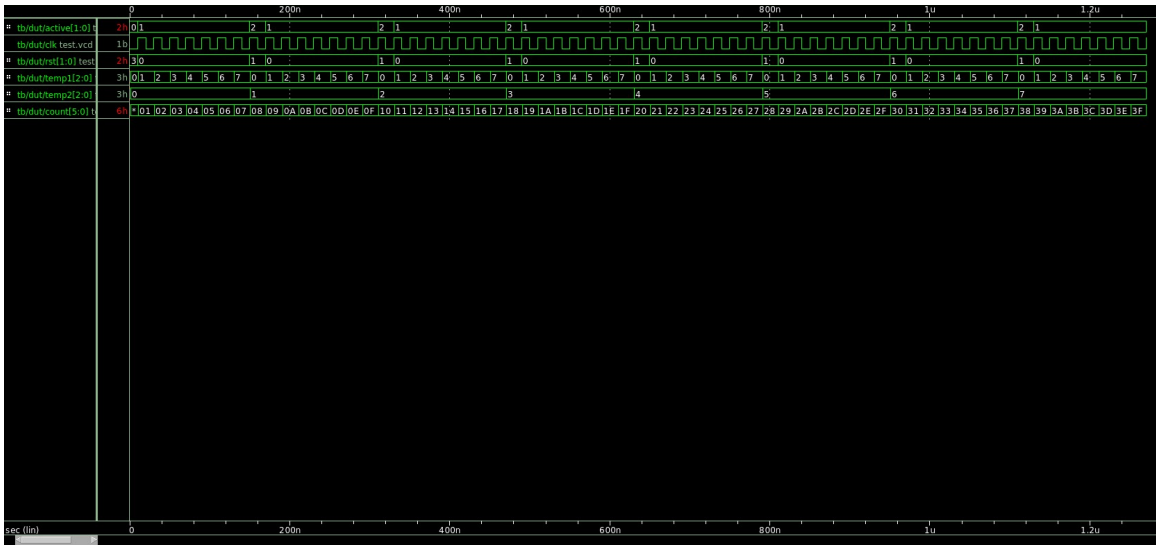

Figure 4.1: Active Stimulus for the Non-gated 6-bit counter

Note that in Figure 4.2 there are two ECK wave form lines. These correspond to the two output signals from the proposed clock gating cells. Notice that for both cells, the clocking signal is disabled during periods of inactivity. By disabling the clock to the second counter we are able to remove unnecessary power consumption from the design. Further discussion of the testing results will be presented in Section V.

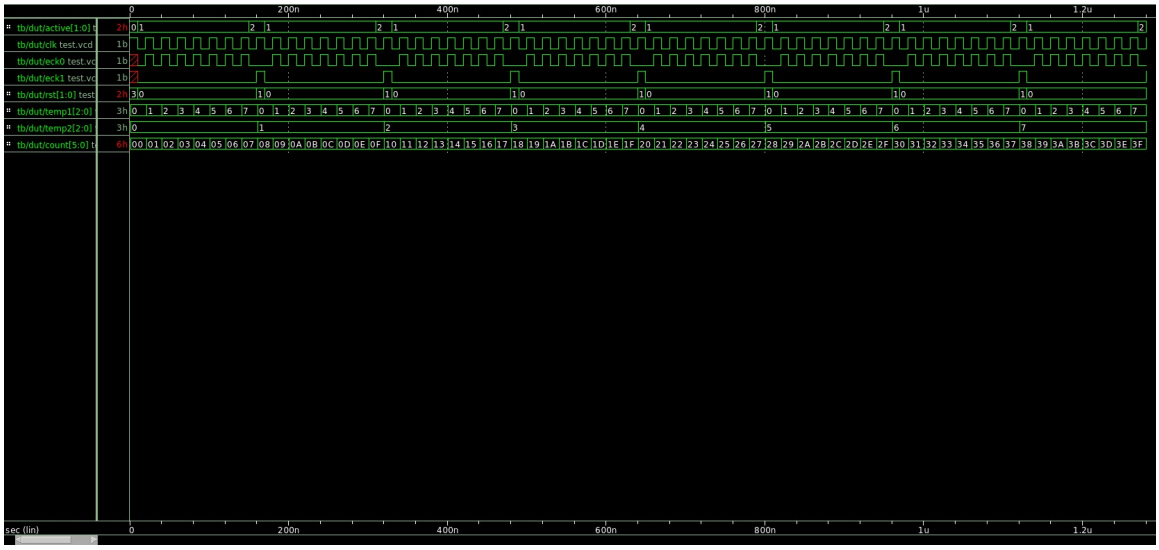

Figure 4.2: Active Stimulus for the Gated 6-bit counter

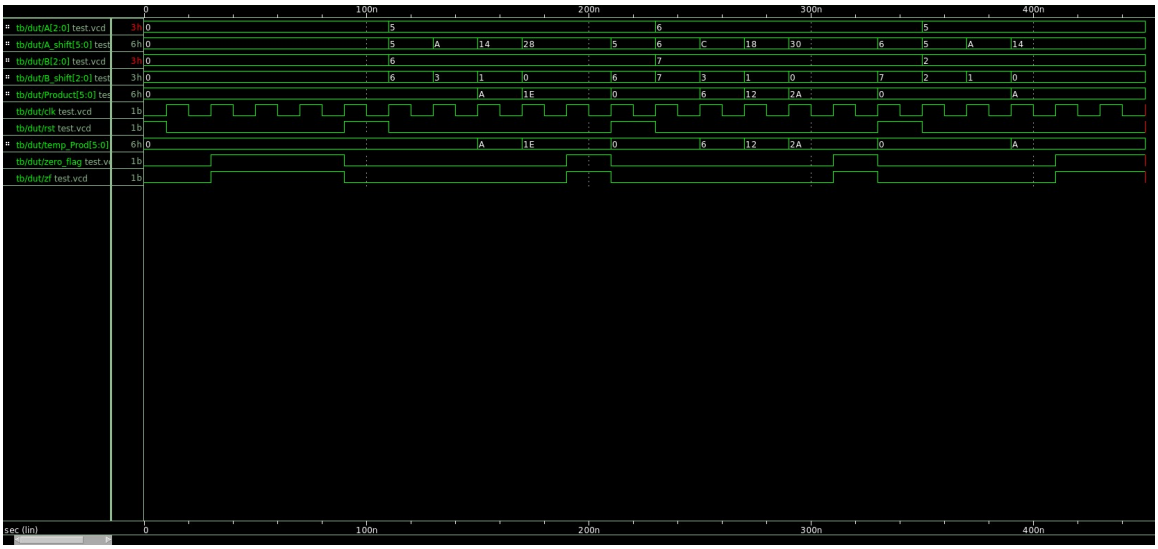

Figure 4.3: Active Stimulus for the Non-gated 6-bit Shift and Add Multiplier

4.2.2 Shift and Add Multiplier Stimulus

Testing for the Shift and Add Multiplier cell was straight forward, with the main goal to examine the reduction of idle power consumption in a design. This is due to how the Shift and Add Multiplier was designed. Recall in Section III that the control logic for the clock gate consists of the inverted stopping signal for the Shift and Add Multiplier. With this in mind, the clock for the design should be allowed for most of the test with intermittent breaks to reset the device. Knowing this, and to return the most accurate metrics, we probe the Shift and Add Multiplier while it performs three multiplications; (5∗6) or (3'b101∗3'b110), (6∗7) or (3'b110∗3'b111) and finally (5∗2) or (3b'101∗3'b010). The set of multiplications that were chosen were done so arbitrarily, however the test ensured enough stimulation to provide a reliable metric estimation. The stimulation files for the Shift and Add Multiplier testing can be seen below.

Again, from the images of the stimulus files we are able to see the reduction in activity of the device when not in use. Note that the results from this test could be further expanded upon by increasing the delay between each successive multiplication.

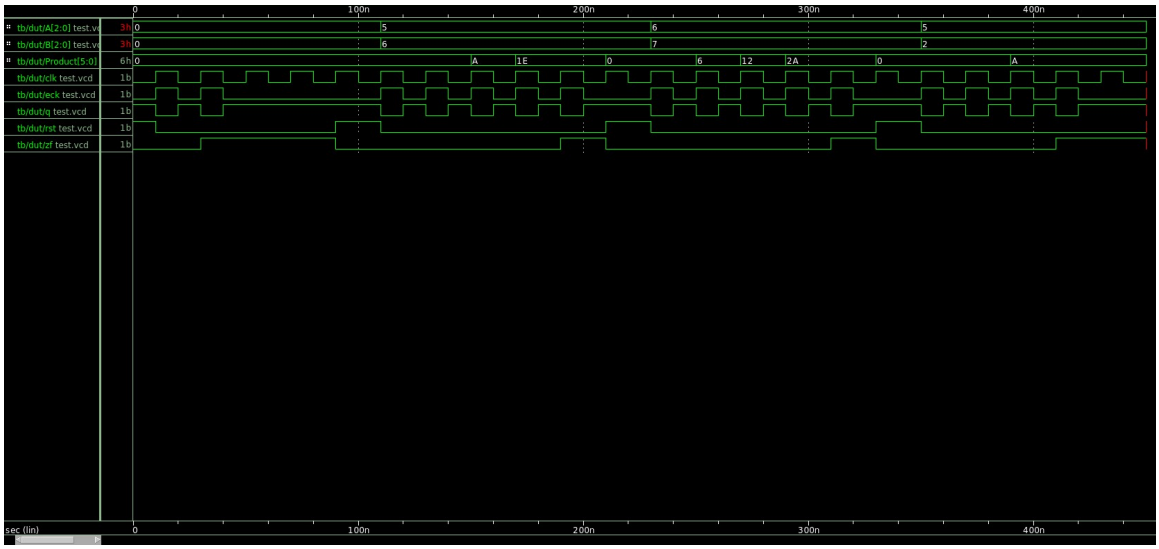

Figure 4.4: Active Stimulus for the Gated Shift and Add Multiplier

This would contribute to an increase in the idle time of the device and thus would show more defined regions of inactivity. However, this also artificially increases the power consumption as well as the power consumption reduction seen by the proposed cell. For this reason, the minimum delay time to properly represent full functionality is presented.

CHAPTER V

RESULTS

In this section we will explore the metrics that were estimated by the Synopsys synthesis tools. We will first determine the effectiveness of the proposed gating cell in reducing power consumption. To do so we will discuss the estimated power metrics for each test scenario when the design is both gated and non-gated. Looking at the power metrics of both stimulus states, we will determine the capability of the proposed cell at reducing dynamic power consumption.

We will then calculate the Energy-Delay Product for each design in order to quantify performance. The EDP of a design is considered because it accounts for power and delay in each design. This helps to provide a metric for the comparison of all test cases, in order to see the full effect of the proposed gating cell.

5.1 Passive Stimulation Results

To reiterate, passive stimulation, for the purposes of this paper, is defined as the testing state when the user provides no stimulus device probing. These tests provide estimations for the average power that the device will consume. Below we will discuss the effectiveness of the proposed clock gating cell in each passive stimulus scenario.

5.1.1 Power Estimation for 6-Bit Counter

In Figure 5.1 we can see the power estimations provided by the Synopsys synthesis tool. Here we can see an itemized table for the power consumed by the non-gated and gated synthesized 6-Bit Counters. Recall from Section II our key goal with the

Power Estimation for 6-bit Counter Under Passive Stimulation						
Non-gated design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	8.79	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	3.01	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	5.83E-03	Register Power	8.15	1.12	3.86E-03	9.27
		Sequential Power	0	0	0	0
Total Dynamic Power	11.82	Combinational Power	0.64	1.90	1.97E-03	2.54
		Total Power	8.79	3.01	5.83E-03	11.82
Gated Design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	1.098	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	0.25	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	4.92E-03	Register Power	7.60E-04	4.27E-04	1.98E-03	0.76
		Sequential Power	2.69E-04	2.14E-04	1.44E-03	0.27
Total Dynamic Power	1.35	Combinational Power	6.91E-05	0.25	1.49E-03	0.27
		Total Power	1.098	0.25	4.92E-03	1.35

Table 5.1: Power Estimation for 6-Bit Counter Under Passive Stimulation

proposed gating cell is to reduce the dynamic power of the device under test and thus the total consumed power. Along with this, we know from Section I that the switching power of the device is a large contributor to the dynamic power consumption. Knowing this we look for a reduction in the switching power and total power consumed by the device under test. When comparing both the net switching power and the total dynamic power from Figure 5.1 we are able to see a reduction of 2.76 μw, or 91.68%, in switching power and a reduction of 10.47 μw, or 88.58%, in total dynamic power.

As can be seen the proposed clock gating cell is capable of achieving the desired functionality and produces massive power savings. However, it must also be noted that the synthesis tool doesn't have the capability of estimating the full functionality of the device. It is for this reason, and reasons we will see later, that we look at the effectiveness of the device while in both passive and active stimulus. While passive stimulus can confirm the functionality of the proposed device, active stimulus controls the switching input for the synthesis tool. Controlling this switching helps refine the power estimations and produce estimates for the designs under stress, as we will see later. We will next discuss the results of the passively stimulated SAM.

Power Estimation for Shift and Add Multiplier Under Passive Stimulation						
Non-gated design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	16.85	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	30.66	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	2.05E-02	Register Power	15.66	23.01	1.12E-02	38.68
		Sequential Power	0	0	0	0
Total Dynamic Power	47.51	Combinational Power	1.19	7.65	9.23E-03	8.85
		Total Power	16.85	30.66	2.05E-02	47.51
Gated Design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	0	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	0	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	1.88E-03	Register Power	0	0	0	0
		Sequential Power	0	0	0	0
Total Dynamic Power	0	Combinational Power	0	0	1.88E-03	1.88E-03
		Total Power	0	0	1.88E-03	1.88E-03

Table 5.2: Power Estimation for Shift and Add Multiplier Under Passive Stimulation

5.1.2 Power Estimation for Shift and Add Multiplier

Figure 5.2 displays the power estimations for the passively stimulated shift and add multiplier, both non-gated and gated.

This test case was included not only to show the effectiveness of the proposed clock gating cell at pruning inactive clocking signals, but also to highlight the importance of the two test types. We observe a near 100% reduction in the theoretical power consumption for the shift and add multiplier, save for nanowatts of power leakage due to control signals. To explain this, recall from Section III how the multiplier was designed to make the most effective use of the proposed clock gating cell. By controlling the activity of the multiplier this way, we observe a complete reduction of power consumption because the synthesis tool sees an inactive device. It it for this reason, as well as the reasons previously discussed, that we must take both passive and active testing cases into consideration.

Power Estimation for RISC-V SoC Under Passive Stimulation						
Non-gated design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	1.06E+03	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	934.46	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	1.22	Register Power	9.10E+02	2.30E+01	0.67	9.30E+02
		Sequential Power	0	0	0	0
Total Dynamic Power	1.99E+03	Combinational Power	1.50E+02	9.10E+02	0.55	1.06E+03
		Total Power	1.06E+03	9.30E+02	1.22	1.99E+03
Gated Design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	48.61	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	401.52	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	2.09	Register Power	0.21	0.00	0.0011	0.21
		Sequential Power	2.33	0.01	0.85	3.19
Total Dynamic Power	450.13	Combinational Power	46.08	401.51	1.24	448.83
		Total Power	48.61	401.52	2.09	452.22

Table 5.3: Power Estimation for RISC-V SoC Under Passive Stimulation

5.1.3 Power Estimation for RISC-V SoC

The final design to be passively tested was the RISC-V SoC. This was by far the most complex device to be tested and allows us to benchmark the proposed cell when used in a vast range of complexity.

Again, we are able to observe large power savings in the RISC-V SoC when the clock gating cell is used to control the data path clock. With a 57.07% reduction to the switching power and a 77.38% it is clear to see that the proposed clock gating cell will provide a massive benefit to the SKY130 cell set.

5.2 Active Stimulation Results

The active stimulus results help to estimate how a design will perform under a set operating load. By creating these switching activity files we are able to put the synthesized device in high activity states. Evaluating the power reduction due to the proposed gating device while in these high stress states helps to illustrate the full benefit of the cell. Moreover, we are also able to know the exact switching activity for the probing period of the power estimation. This removes the unknown switching

Power Estimation for 6-Bit Counter Under Active Stimulation						
Non-gated design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	10.69	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	6.74	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	6.76E-03	Register Power	9.01	2.27	4.71E-03	11.29
		Sequential Power	0	0	0	0
Total Dynamic Power	17.42	Combinational Power	1.68	4.46	2.05E-03	6.14
		Total Power	10.69	6.74	6.76E-03	17.27
Gated Design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	6.98	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	3.34	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	5.84E-03	Register Power	4.82	1.70	2.01E-03	6.52
		Sequential Power	1.81	0.24	2.11E-03	2.05
Total Dynamic Power	10.32	Combinational Power	0.35	1.39	1.72E-03	1.74
		Total Power	6.98	3.34	5.84E-03	10.32

Table 5.4: Power Estimation for 6-Bit Counter Under Active Stimulation

activity introduced by the tool for the probing period, thus helping to refine the power consumption results.

5.2.1 Power Estimation for 6-Bit Counter

Figure 5.4 shows the power consumption for the 6-Bit counter when under the active stimulus outlined in Section IV. From this power report we are able to see that the clock gating is still successful at greatly reducing the power consumption of the gated device. However, for the active test we see a reduction of 3.4 μw , or 50.45%, in the switching power and a reduction of 7.1 μw, or 40.76%, in the dynamic power. Though the power consumption reduction isn't as significant, these metrics provide much closer estimates to the effectiveness of the gating cell.

5.2.2 Power Estimation for Shift and Add Multiplier

The final test for the proposed clock gating cell yet again highlights the benefits of using both testing methods. In the passive testing of the shift and add multiplier, the synthesis tool was unable provide inputs for A and B. This lead to the device remaining off for the entire synthesis cycle, thus leading to the complete reduction

Power Estimation for Shift and Add Multiplier Under Active Stimulation						
Non-gated design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	21.92	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	73.43	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	2.10E-02	Register Power	18.63	46.96	1.25E-02	65.60
		Sequential Power	0	0	0	0
Total Dynamic Power	95.35	Combinational Power	3.29	26.47	8.47E-03	29.77
		Total Power	21.91	73.43	2.10E-02	95.37
Gated Design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	0.297	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	0.84	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	1.88E-03	Register Power	0	0	0	0
		Sequential Power	0	0	0	0
Total Dynamic Power	1.13	Combinational Power	0.30	0.84	1.88E-03	1.13
		Total Power	0.30	0.84	1.88E-03	1.13

Table 5.5: Power Estimation for Shift and Add Multiplier Under Active Stimulation

of power consumption seen in Table 5.2. By providing switching data to the tool we are able to eliminate this issue and derive power estimates for the shift and add multiplier. Here we see a 72.59 μw, 98.86%, reduction in switching power and a 94.22 μw,98.81%, reduction to total dynamic power consumption.

5.2.3 Energy-Delay Product

With the power consumption reduction capabilities of the proposed gating cell shown earlier in this section, we look to the Energy-Delay Product (EDP) to provide an easy metric for performance comparison. The EDP of a device is a figure of merit that is used to directly quantify a devices performance. By combining the delay and into the figure of merit we are able to ignore the increase in power due to clock frequency. This helps to equalize the comparison metric for all cases. The works of [13] and [14] present the theory and show the effectiveness of the EDP metric. ADD MORE

As it sounds, the EDP is computed by taking the product of the energy and the delay. The EDP is an extension of the Power-Delay Product (PDP) of a device, which represents the average energy required to perform a computation and is a the product of the power and the delay. From this we can see how EDP extends from PDP, as

if PDP $= (P \times D) \rightarrow$ EDP $=$ PDP $\times D = (P \times D) \times D$. The PDP of a device is also known as the average switching power of a device, which is a metric we already have.By combining what we know with the derivations presented in [15] and [16] we are able to prove this fact.

Define:

-$t_p \equiv$ average switching time

-$delay = f_{max} \times t_p$

Assuming a maximum switching frequency of $f_{max} = \frac{1}{2*t_p}$, then

$$PDP = (\text{Switching Power}) \times f_{max} \times t_p = \frac{(\text{Switching Power})}{2} \tag{5.1}$$

$$EDP = PDP \times t_p \tag{5.2}$$

To further reinforce the usefulness of using the EDP of a device to classify its performance, we can look to [13]. The authors of this work propose the usage of EDP to characterize the energy efficiency of various power reduction techniques. Using the theory of this paper, we are able to implement a simple metric for comparison.

As mentioned in Section IV, the Synopsys synthesis tool probes the synthesised design for more than just power and also outputs timing information for the device under test. Using this timing information we are able to calculate the PDP and EDP for all five tests.

Non-Gated Designs				
Design	**Switching Power (uW)**	**Delay (ns)**	**PDP**	**EDP**
Passive 6-Bit Counter	3.01	0.64	1.51	0.96
Passive Shift and Add Multiplier	30.66	11.69	15.33	179.21
Passive RISC-V SoC	934.46	19.70	467.23	9,204.43
Active 6-Bit Counter	6.74	0.64	3.37	2.16
Active Shift and Add Multiplier	73.43	11.69	36.72	429.20
Gated Designs				
Design	**Switching Power (uW)**	**Delay (ns)**	**PDP**	**EDP**
Passive 6-Bit Counter	0.25	10.24	0.13	1.28
Passive Shift and Add Multiplier	0.00	12.40	0.00	0.00
Passive RISC-V SoC	401.52	18.70	200.76	3,753.41
Active 6-Bit Counter	3.34	10.24	1.67	17.10
Active Shift and Add Multiplier	0.84	12.40	0.42	5.21

Table 5.6: Table of Energy-Delay Products

Figure 5.6 shows us that though there is a power reduction in all designs, sometimes the performance detriment is not worth the power savings. This is the case for the 6-Bit counter under active stimulus. We can see here that the switching power of the design is reduced by 3.4 μw, which is a reduction of 50.44%. However, due to the large increase in the delay the device actually takes an overall performance loss due to the addition of the clock gating circuit. This means that clock gating, in the form presented in this paper, is not a cover all solution for power reduction as it can lead to performance decreases in some scenarios

CHAPTER VI

CONCLUSION

In this paper we have explored the background, design and implementation of a clock gating cell designed for the Oklahoma State University VLSIARCH SKY130 standard cell set. The proposed clock gating cell was tested when incorporated into designs of varying degrees of complexity. In order to fully realize the potential of the proposed gating cell, five tests were performed then compared to extrapolate the cell's general efficacy.

The clock gate cell testing returned very promising results overall. We were able to successfully reduce both the switching power consumption and dynamic power consumption in all test cases. More than power reduction, the test set was also able to show case the wide range of versatility for clock gating cells. Finally, we calculated the Energy-Delay Product of each device and showed the possible pit falls of using clock gating where not needed. Though clock gating is an easy to implement solution, there is not an abundance of current work presenting the idea. This is due to that fact that many design processes are closely guarded and kept out of publishing. As discussed, the creation of a standard cell set is expensive, making most current standard cell sets inaccessible. SKY130 is an open source standard cell design set, which makes it an ideal candidate for standard cell set optimization work. With this in mind, future work looks to explore a wider variety of standard cell clock gating solutions.

Future work will focus on the optimization and enhancement of the clock gating standard cell design. The design presented in this paper was an easy to implement,

low logic impact, D-latch based clock gate. However, works such as [17], show case the addition of Look Ahead logic to improve clock gate performance.By using the EDP performance metric proposed in [13], we will look to implement and compare the ideas of [17] and [8]. A comparison of the work proposed in this paper along with that proposed in [17] and [8] would present a more comprehensive optimization of the standard cell. With further performance capability possible, such cell enhancements will be considered for future cell set optimization and further works.

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APPENDICES

APPENDIX A: Negative Edge Triggered Clock Gate Results

In this appendix we will display the output metric estimations derived by the Synopsys Synthesis tool for the negative clock edge triggered clock gating cells. Note that all test cases that were presented in IV were replicated for the negative activation cell. The test case results will be presented in the same order as presented in V. Finally, after the power estimations of each test case has been given, a table to compare the EDP values will be presented.

Power Estimation for 6-Bit Counter Under Passive Stimulation						
Non-gated design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	8.97	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	17.75	Black Box Power	0	0	0	0
		Clock Network Power	0.27	15.00	8.55E-05	15.71
Cell Leakage Power	5.75E-03	Register Power	8.08	1.12	3.86E-03	9.20
		Sequential Power	0	0	0	0
Total Dynamic Power	26.72	Combinational Power	0.62	1.64	1.80E-03	2.26
		Total Power	8.97	17.75	5.75E-03	26.72
Gated Design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	0.8	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	0.25	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	7.82E-03	Register Power	0.39	4.27E-04	1.82E-03	0.39
		Sequential Power	0.29	2.33E-03	4.21E-03	0.30
Total Dynamic Power	1.05	Combinational Power	0.12	0.25	1.78E-03	0.37
		Total Power	0.80	0.25	7.82E-03	1.06

Table 1: Power Estimation for Negatively Clocked Counter Under Passive Stimulation

Power Estimation for Shift and Add Multiplier Under Passive Stimulation						
Non-gated design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	20.4	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	70.84	Black Box Power	0	0	0	0
		Clock Network Power	0.27	40.24	8.55E-05	40.51
Cell Leakage Power	2.06E-02	Register Power	18.94	22.89	1.12E-02	41.84
		Sequential Power	0	0	0	0
Total Dynamic Power	91.24	Combinational Power	1.19	7.72	9.23E-03	8.92
		Total Power	20.04	70.84	2.36E-02	91.27
Gated Design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	0	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	0	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	1.88E-03	Register Power	0	0	0	0
		Sequential Power	0	0	0	0
Total Dynamic Power	0	Combinational Power	0	0	0.00	1.88E-03
		Total Power	0 mW	0	1.88E-03	1.88E-03

Table 2: Power Estimation for Negatively Clocked SAM Under Passive Stimulation

Power Estimation for RISC-V SoC Under Passive Stimulation						
Non-gated design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	1.06E+03	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	934.46	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	1.22	Register Power	9.10E+02	2.30E+01	0.67	9.30E+02
		Sequential Power	0	0	0	0
Total Dynamic Power	1.99E+03	Combinational Power	1.50E+02	9.10E+02	0.55	1.06E+03
		Total Power	1.06E+03	9.30E+02	1.22	1.99E+03
Gated Design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	56.42	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	394.27	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	2.09	Register Power	0.29	2.14E-04	9.5E-04	0.21
		Sequential Power	2.35	1.19E-02	0.85	3.22
Total Dynamic Power	450.13	Combinational Power	53.78	394.26	1.32	449.36
		Total Power	56.42	394.27	2.17	452.86

Table 3: Power Estimation for Negatively Clocked RISC-V SoC Under Passive Stimulation

Power Estimation for 6-Bit Counter Under Active Stimulation						
Non-gated design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	10.84	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	21.38	Black Box Power	0	0	0	0
		Clock Network Power	0.27	14.997	8.62E-05	15.27
Cell Leakage Power	6.82E-03	Register Power	8.92	2.27	4.71E-03	11.19
		Sequential Power	0	0	0	0
Total Dynamic Power	32.22	Combinational Power	1.64	4.11	2.03E-03	5.76
		Total Power	10.84	21.38	6.82E-03	32.23
Gated Design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	11.69	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	14.41	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	8.38E-03	Register Power	3.32	0.83	1.59E-03	4.14
		Sequential Power	6.55	2.27	4.52E-03	8.83
Total Dynamic Power	26.09	Combinational Power	1.82	11.31	2.27E-03	13.12
		Total Power	11.69	14.41	8.38E-03	26.10

Table 4: Power Estimation for Negatively Clocked Counter Under Active Stimulation

Power Estimation for Shift and Add Multiplier Under Active Stimulation						
Non-gated design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	25.84	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	108.79	Black Box Power	0	0	0	0
		Clock Network Power	0.26	38.87	8.92E-05	38.75
Cell Leakage Power	2.09E-02	Register Power	22.41	44.92	1.22E-02	67.34
		Sequential Power	0	0	0	0
Total Dynamic Power	134.63	Combinational Power	3.16	25.38	8.54E-03	28.56
		Total Power	25.84	108.79	2.09E-02	134.65
Gated Design						
Section Power	**Amount (uW)**	**Subsection Power**	**Internal Power (uW)**	**Switching Power (uW)**	**Leakage Power (uW)**	**Total Power (uW)**
Cell Internal Power	0.14	I/O Pad Power	0	0	0	0
		Memory Power	0	0	0	0
Net Switching Power	0.38	Black Box Power	0	0	0	0
		Clock Network Power	0	0	0	0
Cell Leakage Power	1.88E-03	Register Power	0	0	0	0
		Sequential Power	0	0	0	0
Total Dynamic Power	0.52	Combinational Power	1.40E-01	3.80E-01	1.88E-03	5.18E-01
		Total Power	0.14	0.38	1.88E-03	0.52

Table 5: Power Estimation for Negatively Clocked SAM Under Active Stimulation

Non-Gated Designs				
Design	**Switching Power (uW)**	**Delay (ns)**	**PDP**	**EDP**
Passive 6-Bit Counter	17.75	10.79	8.88	95.76
Passive Shift and Add Multiplier	70.84	15.05	35.42	533.07
Passive RISC-V SoC	934.46	19.70	467.23	9,204.43
Active 6-Bit Counter	21.38	10.79	10.69	115.35
Active Shift and Add Multiplier	108.79	15.05	54.40	818.64
Gated Designs				
Design	**Switching Power (uW)**	**Delay (ns)**	**PDP**	**EDP**
Passive 6-Bit Counter	0.25	0.06	0.13	0.01
Passive Shift and Add Multiplier	0.00	15.10	0.00	0.00
Passive RISC-V SoC	394.27	18.70	197.14	3,685.64
Active 6-Bit Counter	14.41	0.06	7.21	0.43
Active Shift and Add Multiplier	0.38	15.10	0.19	2.87

Table 6: Power Estimation for Negatively Clocked SAM Under Active Stimulation

This is the end of Appendix A.

VITA

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