UNIVERSITY OF OKLAHOMA

GRADUATE COLLEGE

DESIGN AND FABRICATION OF A FREQUENCY-AGILE AND SURFACE MOUNTABLE SUSPENDED INTEGRATED STRIP-LINE (SISL) BANDPASS FILTER

A THESIS

SUBMITTED TO THE GRADUATE FACULTY

in partial fulfillment of the requirements for the

Degree of

MASTER OF SCIENCE

By

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Norman, Oklahoma
2022

DESIGN AND FABRICATION OF A FREQUENCY-AGILE AND SURFACE MOUNTABLE SUSPENDED INTEGRATED STRIP-LINE (SISL) BANDPASS FILTER

A THESIS APPROVED FOR THE
SCHOOL OF ELECTRICAL AND COMPUTER ENGINEERING

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Acknowledgments

I am deeply grateful to my advisors, Dr. Jay McDaniel and Dr. Hjalti Sigmarsson, for their guidance in carrying out this research. They have made me a better engineer, thinker, and person through their mentor-ship. I am sure I will carry their lessons with me as I continue my engineering career.

I also appreciate the great people I have met in my time at the Advanced Radar Research Center. Whether they helped me learn a new fabrication technique or provided a great conversation, they are a part of my work here. I especially want to thank Jon Knowles, Patrick O'Connor-Lynch, and Clayton Blosser for their friendship and support. Graduate school is never easy, but it has helped so much to go through it with others. They made classes bearable, lightened the mood, and even gave insights into my research, and I am deeply grateful for all of it. I wish them luck in their future endeavors and am confident they will excel.

I would also like to thank my parents, Ron and Amy Wells, for supporting me over the years. I appreciate everything they have done for me and know they have made me who I am.

Finally, I would like to thank Teresa Deutchman for her love and support over the years. She was always there for me during the highs and lows of my college career, and I will forever be grateful to her for that.

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Abstract

Modern radar and communications systems have increasingly high demands for low cost, size, weight, and power (C-SWaP) that will prove a challenge to satisfy. Surface mount technology is an excellent way to place components densely at low cost, but lumped element components perform poorly at high frequencies. Distributed components perform better at higher frequencies, and planar components are both cheap and relatively small. However, planar components cannot simply be surface mounted because they require specific electromagnetic field distributions to operate correctly. The challenge is therefore developing packaging that is surface mountable and does not disturb the component's field distributions, allowing integration into a larger system.

This thesis aims to increase integration of microwave systems by designing and fabricating a novel surface mount technique using castellated vias and suspended integrated strip-line (SISL) technology. The proposed technique uses SISL as a low-loss and highly integrated packaging that preserves the electromagnetic field distribution of planar components while castellated vias allow the package to be surface mounted easily. A DC-4 GHz thru-line is presented, demonstrating the low loss of the technique. It is then applied to a varactor-based filter tunable from 2.4 to 3.9 GHz, demonstrating further possibilities to reduce C-SWaP.

Chapter 1

Introduction

1.1 Motivation

Radio frequency (RF) and microwave systems will need to continue to evolve to meet future demands for low cost, size, weight, and power (C-SWaP) due to developments in next-generation radar and communications systems (5G). As higher frequencies are used, lumped element components no longer behave as designed, forcing the use of distributed element components. However, these designs can be difficult to integrate into a system because they either restrict the designer to simple planar structures or to connectorizing the individual components. These are not optimal solutions because the connectors add loss, take up more space, and have a risk of cantilevering. In addition, connecting different components using planar structures requires each design to use the same substrate which might not be feasible for a larger system. Finally, simple planar structures, such as microstrip, are not always the ideal transmission line technology because they can be lossy and noisy.

Several solutions to the above problems have been investigated, but one attractive solution is to integrate components into a system using surface mount technology (SMT). SMT is a method of mounting electronics directly onto the surface of a printed circuit board (PCB) which has become dominant throughout the PCB

industry. SMT allows components to be placed more densely, eliminates the loss and expense of connectors, and minimizes the risk of cantilevering [7]. Unfortunately, surface mounting distributed element components is not so straightforward as soldering them to a carrier board. Planar transmission lines require specific field distributions to operate properly, so some form of fully board-embedded packaging must be used to enable surface mounting of the overall package without disrupting the electromagnetic fields of the individual components.

Another avenue to improve C-SWaP is through the use of tunable filters. Filters are used in various systems to block signals at undesired frequencies, allowing only desired signals through. Many modern devices rely on filter banks, a device that switches among a series of fixed filters. By replacing a bank of filters with a single tunable filter, significant weight can be eliminated. Another significant advantage can be found in the flexibility of tunable filters. The frequency spectrum is becoming increasingly crowded, especially within S-band and the extremely crowded industrial, scientific, and medical band of 2.4 GHz [1]. Figure 1.1 illustrates this crowding in the United States. Filters are essential to ensure signals do not bleed into other bands and cause interference. As the spectrum becomes increasingly crowded, one solution is to allow systems to shift to a less crowded band of operation based on surrounding spectral usage. For this to work, there must be a filter that can tune with them.

1.2 Transmission Line Technology

Microstrip is one of the most popular planar transmission line technologies because it is easy to fabricate and integrate into a system. Figure 1.2 presents the geometry and field distribution of a microstrip transmission line. This consists of

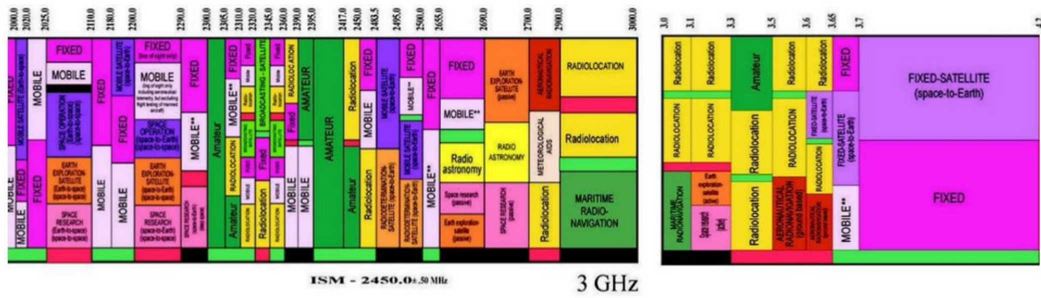


Figure 1.1: Frequency spectrum allocations within S-band. Adapted from [1]

a copper trace on a dielectric with a lower ground plane. Most of the fields are contained within the dielectric, but some are in the air surrounding the center trace. A portion of these fields within air can radiate away from the circuit and contribute additional loss. This loss will increase with operating frequency and can couple into nearby components, introducing possible interference.

One alternative to microstrip is strip-line whose geometry and field distribution are shown in Figure 1.3. The center trace is now embedded in the middle of the substrate with ground planes above and below. There will be almost no radiated losses, but there will still be dielectric loss, especially if the substrate chosen has a high loss tangent.

Suspended substrate strip-line (SSS) is a transmission line that aims to mitigate the losses inherent to both microstrip and strip-line [8]. SSS suspends a thin sub-

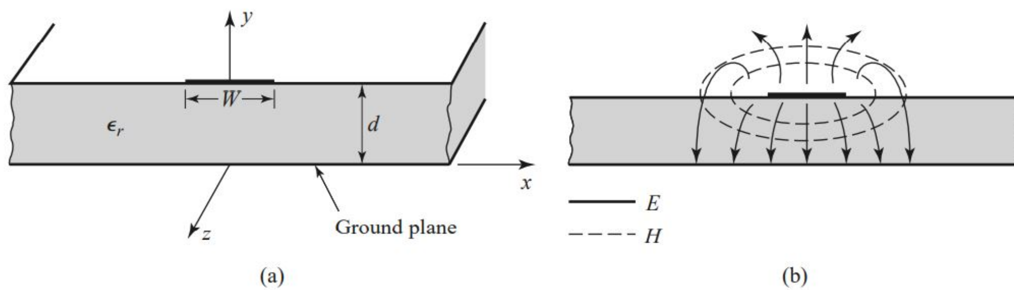


Figure 1.2: Microstrip transmission line geometry and field distribution [2]

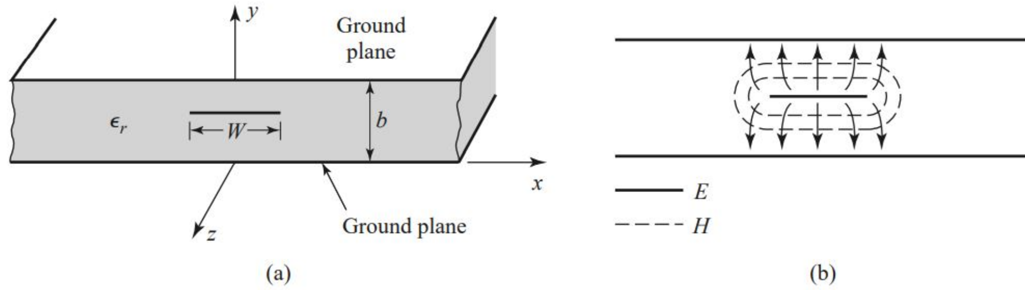


Figure 1.3: Strip-line transmission line geometry and field distribution [2]

strate in air, housing it in a metal cavity, as shown in Figure 1.4. This improves performance because most of the fields are propagating in low-loss air rather than dielectric. Further, the metal cavity minimizes the radiation and interference issues of microstrip. However, the cavity is heavy and expensive to fabricate. Substrate integrated suspended line improves on SSS, replacing the metal cavity with a five-layer PCB stack-up as shown in Figure 1.5 [4]. This maintains the desirable characteristics of SSS while being significantly cheaper and easier to fabricate.

Suspended integrated strip-line (SISL) is a relatively new transmission line topol-

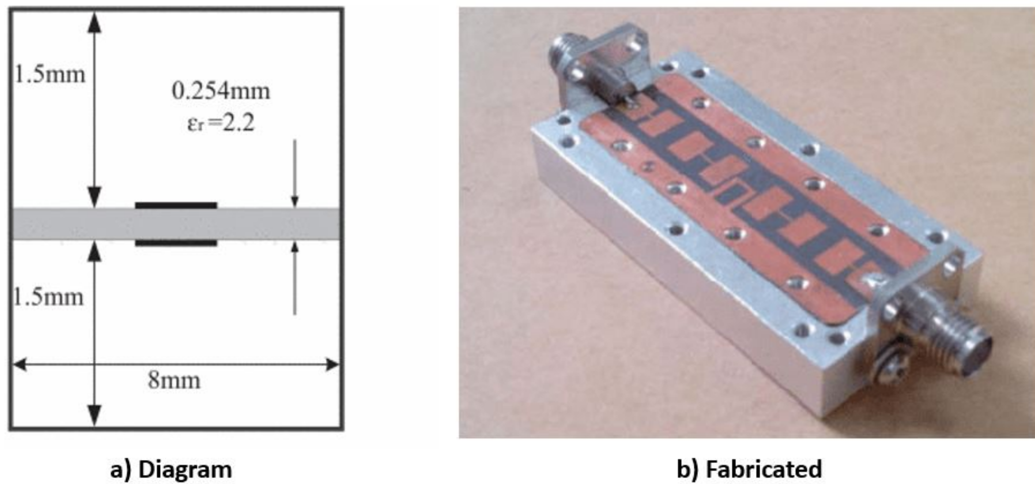


Figure 1.4: Cross-section of SSS and a fabricated filter without the top housing. Adapted from [3]

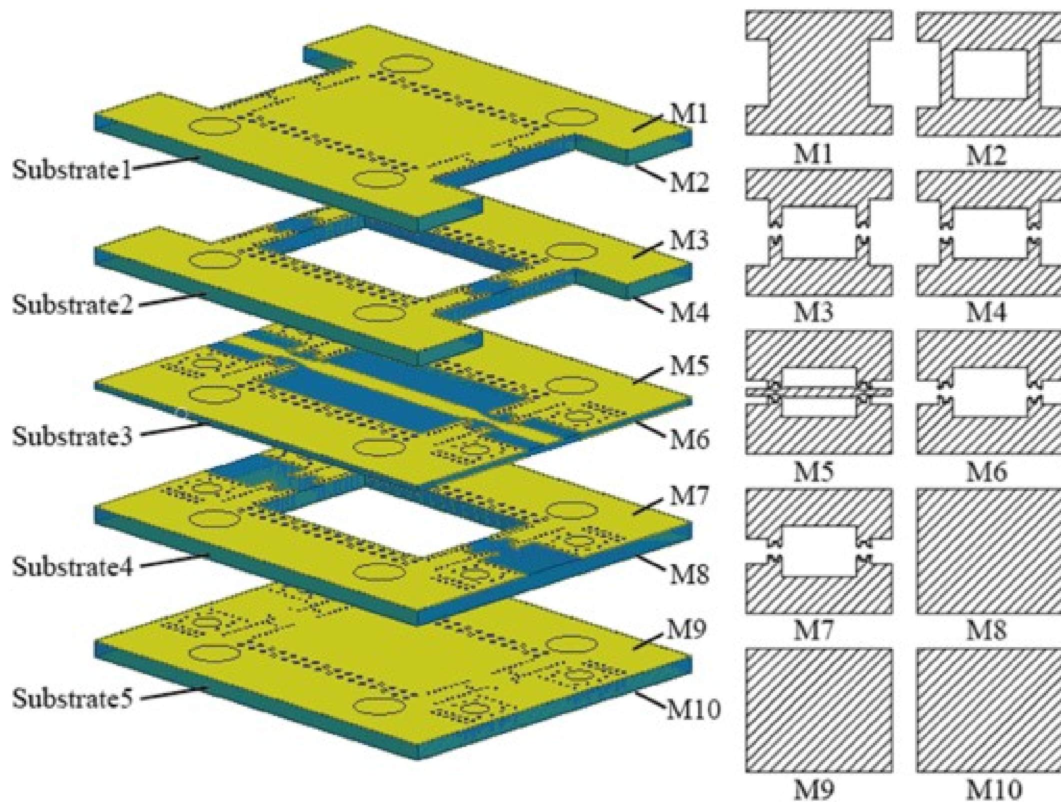


Figure 1.5: Stack-up of a substrate integrated suspended line thru-line [4]

ogy that maintains all the benefits of substrate integrated suspended lines while also being fully board-embedded. This is achieved by reusing the same five-layer stack-up; the top and bottom layers serve as ground planes while the middle layer is a thin, low-loss dielectric that suspends the strip-line. The substrates above and below the strip-line are hollowed out so the line will be surrounded by air. Finally, plated vias are used to create a metal fence around the cavity which mimics solid metal walls at low enough frequencies. Rather than creating a transition from ground-backed co-planar waveguide (CPWG) as in [4], [5] created a CPWG-to-strip-line vertical via transition, making the component fully board-embedded. A CPWG trace is placed on metal layer 1 (M1), the top of Substrate 1, while the strip-line is placed on either the top or bottom of the middle substrate. Figure 1.6 shows how the SISL

air cavity is accessed. Numerous devices have been designed using the SISL technology, including mixers [9], power dividers [10], and filters [11, 12], illustrating its adaptability.

SISL has multiple advantages over more traditional transmission line structures. First, the radiated losses are minimized because the top and bottom layers and plated vias contain the electromagnetic (EM) fields within the cavity. Figure 1.7 illustrates the electric fields within the cavity. This also minimizes the risk of a component's fields interfering with another component in the overall system [13]. Further, the dielectric losses are minimized because most of the fields are propagating in the air rather than higher loss dielectrics in a traditional strip-line [5]. Finally, SISL designs are fully board-embedded and self-packaged and can more easily be integrated into microwave systems than traditional suspended strip-line which requires mechanical housing [14].

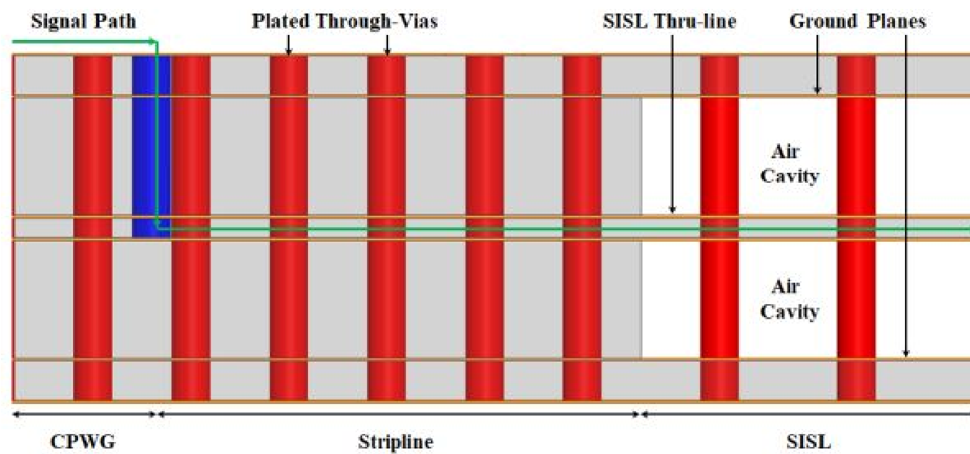


Figure 1.6: Profile of the SISL Via Transition [5]

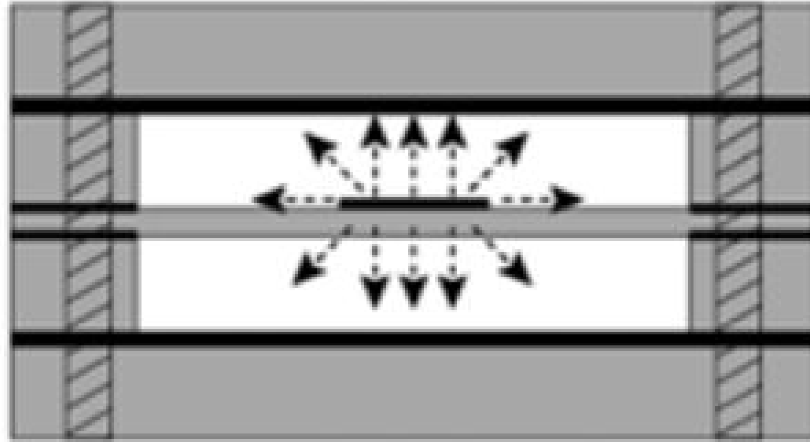


Figure 1.7: Cross Section of a SISL Cavity Illustrating Electrical Fields [4]

1.3 Surface Mounting

Surface-mount technology is a method in which electrical components are mounted onto the top layer of a printed circuit board. It is ubiquitous in modern electronics, ranging from simple components (inductors, capacitors, resistors) to entire circuits (integrated circuits). However, SMT becomes less applicable as frequencies get higher because the inductances and capacitances associated with the packaging become significant. At high enough frequencies, the packaging will cause the component to resonate, making it unusable. This is known as the self-resonant frequency.

To design components at higher frequencies, distributed elements (transmission lines) can be used. These do not have the self-resonance of lumped elements and can be designed for any frequency assuming the dimensions are properly chosen, although they still suffer from harmonics. Further, these are very cheap to implement because they only require patterning on a circuit board. However, these components can be hard to integrate into an overall system. In [15], a cavity filter was

surface mounted by creating the first and last resonators in CPWG and using the circuit board as the lower wall of the cavity. A similar solution was demonstrated in [16] and [17], although these designers demonstrated that an iris or microstrip stub could be used to couple from substrate integrated waveguide to the SMT cavity filter. Both of these designs allow effective surface mounting of a waveguide filter, but these have not demonstrated that they can be extended to planar transmission lines. Waveguides are not always the optimal structure because they are bulkier and more expensive than PCBs.

In [18], both a thru-line and filter were demonstrated using the SISL technology. This achieved an SMT design using only cheap PCBs through the use of a via transition from the carrier board to the component layer. However, the SMT design in [18] is based on the "flip-chip" SMT topology which requires precise alignment and increases assembly complexity. This thesis proposes a structure that keeps the low cost and ease of integration of [18] while easing alignment and assembly.

1.4 Tunable Filters

Tunable filters are very useful because they allow a system to operate over a range of frequencies while still rejecting undesirable signals [19]. They are also useful in applications concerned about weight, such as airborne, space borne, and marine-based systems since a single tunable filter can cover the same frequency range as a bank of fixed filters, reducing weight. In general, tunable filters have been implemented using several technologies, including varactor diodes [20, 21, 22], RF microelectromechanical systems (MEMS) [23], and ferroelectric capacitors [24]. The goal of all these technologies is to vary capacitance, changing the center frequency of the filter.

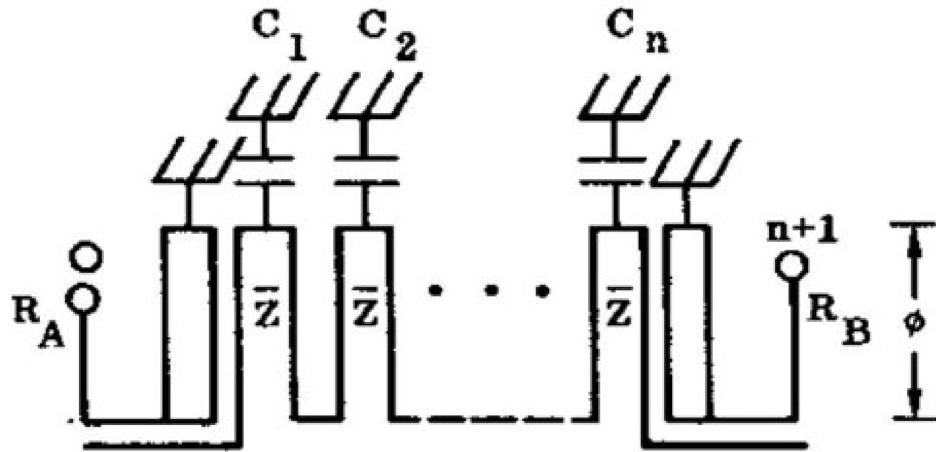


Figure 1.8: Common layout of a combline bandpass filter [6]

A number of tunable filter structures have been used, but one of the most useful is the combline, whose traditional implementation in microstrip is shown in Figure 1.8. The length of the resonators is chosen, and shunt capacitors are added to the ends of the resonators to achieve resonance at the desired frequency. The desired bandpass response and bandwidth can then be achieved by adjusting the external and inter-resonator couplings. In [25], a tunable combline filter was implemented in SISL similarly to [4]. The fixed capacitors of a traditional combline were replaced with varactor diodes, providing tunability.

1.5 Research Objective

In this thesis, a new method of surface mounting a component using suspended integrated strip-line technology is proposed. A DC-4 GHz SISL thru-line is designed, fabricated, and measured to verify the design and demonstrate the feasibility

of this surface mounting scheme.

The work is then extended to the design of a frequency-agile bandpass filter using the combline structure, varactor diodes, and DC biasing lines. A second-order Butterworth bandpass filter with center frequencies tunable from 2.3-3.9 GHz and a 0.5 GHz bandwidth is designed, fabricated, and measured.

1.6 Thesis Outline

Chapter 2 demonstrates the design of an SMT SISL thru-line. The chapter gives a detailed design procedure for each element in the structure, culminating in the full thru-line design. The chapter concludes with a simulation of the full design which will be verified in measurement.

In Chapter 3 a tunable bandpass filter (BPF) is designed to integrate it into the SMT SISL structure. The design procedure for a tunable filter is discussed, together with additional considerations to integrate it into the SISL structure. The full design is then simulated, demonstrating the feasibility of the SMT-able design.

Chapter 4 gives an overview of the fabrication for both the thru-line and tunable filter as well as the measured results. The results are then analyzed to confirm the feasibility of using castellated vias to access the SISL structure.

Chapter 5 concludes by summarizing the research and suggesting future work. Both improvements to this work and possible avenues for future research on increasing integration are also discussed.

Chapter 2

SISL Thru-line Design

The purpose of this chapter is to provide a detailed design procedure of the SISL technology, focusing on modifications necessary for surface mounting. This chapter will also offer several design considerations to ease the implementation of the surface mount SISL technology. A DC-4 GHz SISL thru-line is used as the design example throughout this chapter to illustrate that the surface mounting is effective.

2.1 SISL Design and Implementation

Figure 2.1 shows the exploded 3-D view of the proposed surface mount SISL design. This consists of a stack-up of five substrates. Substrates 2 and 4 are hollowed out to create the air cavity around the suspended line while Substrate 1 acts as both the carrier board and bottom metal wall (M2). Finally, Substrate 5 acts as the top metal wall for the cavity. The air cavity is surrounded by plated vias that create the metal side walls. The vias must have a spacing less than $\lambda/10$ to mimic a solid metal wall [26]. The thru-line is implemented on metal layer M5, but it is moved to M6 for illustration purposes.

The SISL air cavity is accessed through a CPWG-to-strip-line castellated via

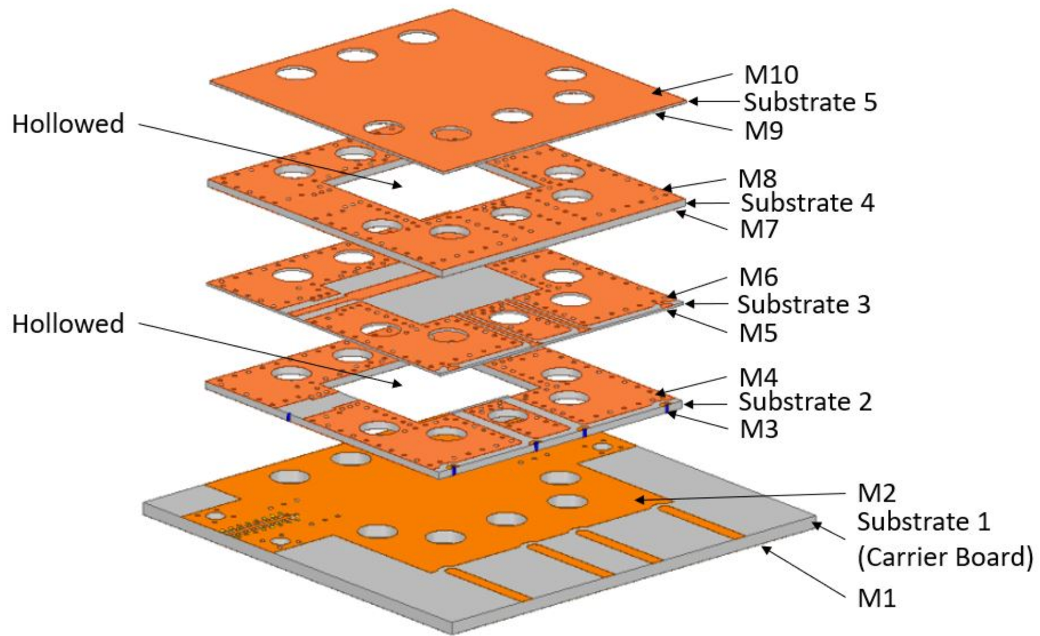


Figure 2.1: Exploded view of the proposed surface mount SISL thru-line

transition. The CPWG trace is placed on M2, the top copper of Substrate 1 which serves as the carrier board. The strip-line trace can be placed on either M5 or M6, the bottom and top of Substrate 3, respectively. Placing the strip-line on M5 eliminates the necessity of a plated via through Substrate 3, simplifying fabrication greatly. Therefore, this is the only solution investigated in this work. The strip-line then transitions to SISL when it reaches the air cavity. No special taper is required; instead, both lines are designed to 50Ω and joined together where the cavity begins. There is then a transition from SISL back to strip-line, followed by another castellated via transition to CPWG on the carrier board. In a real system, the CPWG traces on the carrier board would connect to other components, integrating the surface mount SISL into the larger system. Figure 2.2 illustrates half the signal path. It should be noted that the vias used to create a metalized wall around the SISL cavity are removed for clarity.

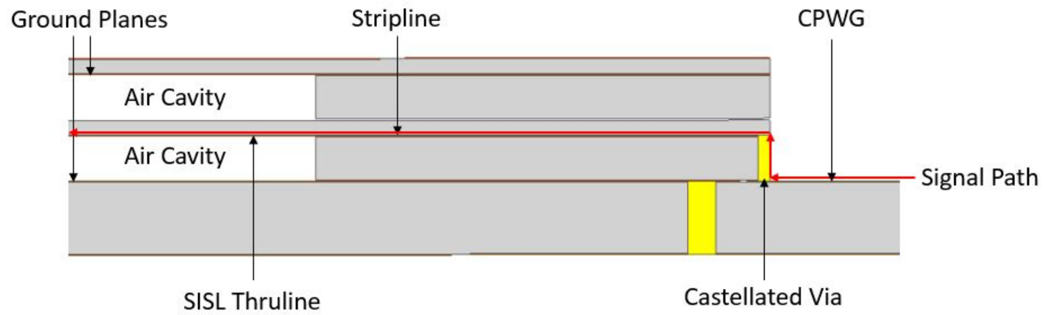


Figure 2.2: Side-view to illustrate castellated via transition

One of the great advantages of SISL is that each section can be designed separately and integrated at the end as long as they are designed for a characteristic impedance of 50Ω [5]. Therefore, the SISL cavity can be designed separately from the via transition and transmission lines. The following sections will cover the design of each sub-component necessary to implement a surface mount SISL thruline. This proof-of-concept will illustrate the feasibility of the design and isolate the losses introduced by the packaging. The bulk of the design is carried out using ANSYS High Frequency Structure Simulator (HFSS).

2.1.1 Material Stack-Up

The first step in designing any SISL component is to select the material stack-up because this will have significant effects on each of the later components. Substrate 5 is the least important because it exclusively acts as a metal wall for the SISL cavity. Substrates 2-4 are essential to the SISL design, while Substrate 1 will determine the design of the CPWG traces.

According to [5], Substrates 2-4 should all be the same material, ideally with a relative permittivity close to air, and the dielectric loss tangent should be as low as possible. To maintain approximate symmetry, Substrates 2 and 4 should be of

the same thickness while Substrate 3 should be as thin as possible. The materials chosen will determine the dimensions of the SISL thru-line and the strip-line trace.

For this design, Rogers Corporation's RO3000 series laminates are chosen [27]. These are ceramic-filled PTFE composites specifically developed for high frequency PCB design. These boards have very low loss, and their dielectric constant is extremely stable over frequency. In addition, the mechanical properties are designed such that they remain constant for boards with different dielectric constants which allows multiple boards of different dielectric constants to be integrated into a single stack-up.

For the SISL thru-line depicted in Figure 2.1, the substrates are chosen as follows: Substrate 1 is 50 mil thick RO3010 ($\epsilon_r = 10.2$, $tan\delta = 0.0022$) material, Substrates 2 and 4 are 30 mil thick RO3003 ($\epsilon_r = 3.0$, $tan\delta = 0.0010$) material, and Substrates 3 and 5 are 10 mil thick RO3003 ($\epsilon_r = 3.0$, $tan\delta = 0.0010$) material. Substrate 1's copper is electrodeposited, while all other substrates have rolled copper foil. All copper claddings are half-ounce (17.5 μm) thick.

2.1.2 CPWG Design

CPWG is chosen for the carrier board because it gives the designer greater control over the transmission line's dimensions. In microstrip, only the width of the trace and substrate material and thickness can be adjusted to achieve a specific characteristic impedance. Realistically, the substrate is generally chosen early in the design process and cannot be changed, so the width of the trace is the only variable under the designer's control. One of CPWG's benefits is that both the width of the trace and the gap between the trace and side grounds can be adjusted to achieve a desired characteristic impedance. This gives the designer two variables to adjust

and provides much greater flexibility in designing the transmission line.

Keysight Advanced Design System's (ADS) LineCalc tool is the easiest way to design a CPWG transmission line. The tool has a CPWG template which requires the desired characteristic impedance (Z_0), thickness and dielectric constant of the substrate, thickness of the copper, and either the width of the center trace, W, or the gap between the trace and side grounds, G. One of the limitations is that LineCalc can only solve for a width given a gap, or vice versa. Therefore, the designer must somehow choose which dimension to fix and what size to make it.

Typically, fabrication concerns are the easiest way to choose which dimension to fix. One of the main limitations is how narrow of a gap can be fabricated. A safe assumption is that the gap should be at least 10 mil. Similarly, the center trace can not be made too narrow for two reasons. First, extremely narrow lines are very hard to fabricate. Second, the line should not be smaller than the connector's center pin. For this application, there is an additional consideration in choosing the center trace's width. The trace cannot be made wider than the pad for the castellated via, which will be discussed in more depth later in this chapter. Therefore, designing a CPWG trace is typically a game of adjusting either the gap or width until both fall within manufacturable tolerances while still providing a good match.

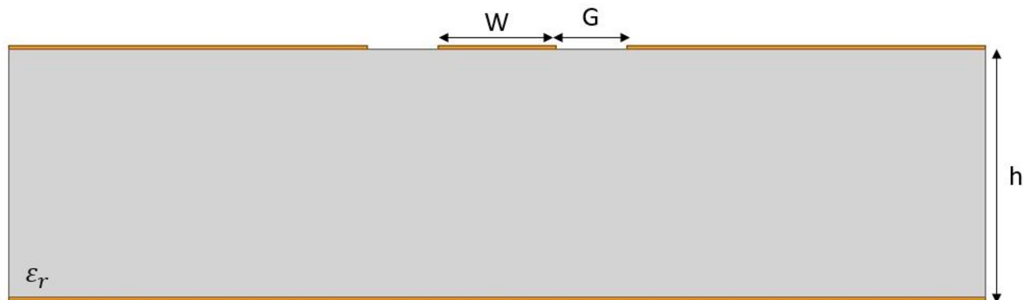


Figure 2.3: Cross-section of an ideal CPWG illustrating important dimensions

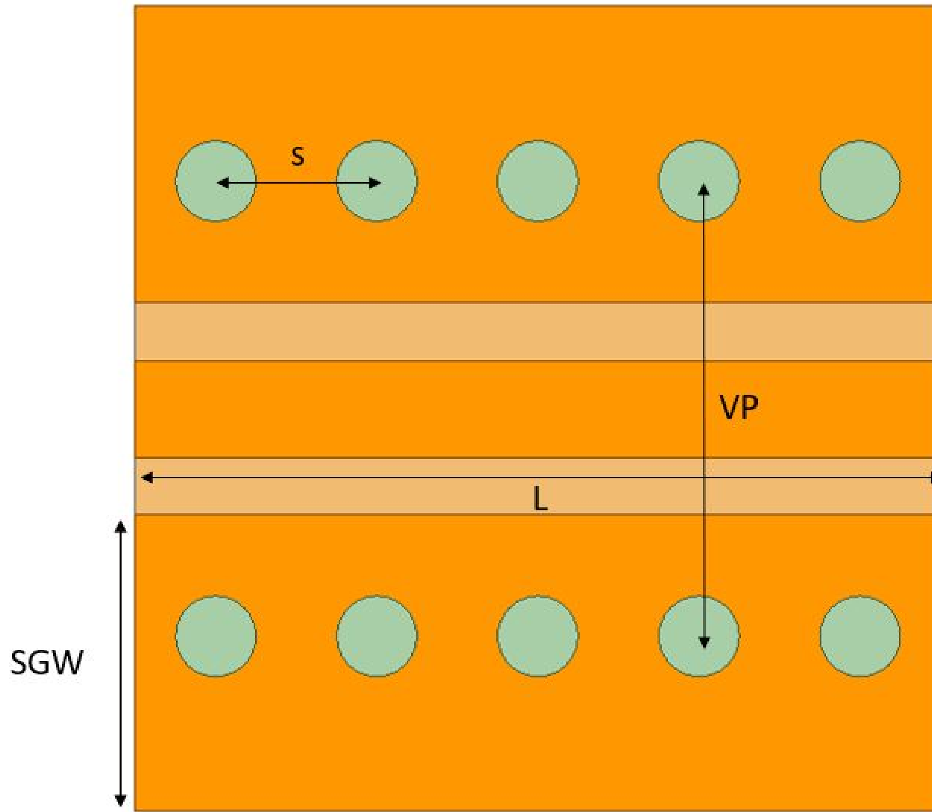


Figure 2.4: Top view of the CPWG, illustrating stitching vias and their dimensions

Figure 2.4 shows a CPWG modeled in ANSYS HFSS. It can be seen that there are a series of plated vias along both sides of the center trace, connecting the side grounds to the lower ground plane. [28] provides a detailed procedure to take a CPWG design from ADS to HFSS. However, the solution can be summarized as choosing the correct via spacings and locations. Without the vias, the signal would couple into the side grounds and radiate at higher frequencies. The dominant resonant mode can be found, where L is the length of the CPWG, and SGW the width of its side grounds without the stitching vias:

$$(f_r)_{110} = \frac{c}{2\pi\sqrt{\epsilon_r}}\sqrt{\left(\frac{\pi}{L}\right)^2 + \left(\frac{\pi}{SGW}\right)^2} \quad (2.1)$$

ADS avoids this resonance because it assumes there is a direct path from the side ground to the lower ground plane ($SGW = 0$). This assumption is impossible to satisfy, but stitching vias can provide a close approximation. Vias cannot be placed directly on the edge of the side grounds, but they can be close. That then makes the effective SGW small and pushes the resonance higher out of the frequency band of interest.

The vias' placement away from the side ground edge can also be thought of as forming a waveguide. The vias make the sides while the lower ground plane and center trace make the bottom and top, respectively. It can generally be assumed the vias are much further apart than the substrate is thick, so the cutoff frequency of the waveguide can be calculated, where VP is the distance from one via wall to the other:

$$f_c = \frac{c}{2VP\sqrt{\epsilon_r}} . \tag{2.2}$$

Again, it can be seen that placing the vias closer to the side ground edge (reducing VP) will push any waveguide modes higher in frequency. Since the design equations indicate closer to the edge is better, the via placement is limited by fabrication requirements alone. Typically, one via diameter is considered a good distance from the edge of the side ground since it can be readily manufactured while still minimizing the distance between the via walls.

Even with the vias close enough to the edge of the side ground, there are still two other possible resonances that can arise. First, if the stitching vias end too far from the edge of the board, the signal can still couple into the side grounds and resonate. This is easily fixed by again minimizing the distance of the first via from the board's edge, typically one via diameter. Second, if the vias forming the wall are too far apart, the signal can still get into the side grounds. The spacing between

vias, shown as s in Figure 2.4, should be at least a quarter wavelength ($\lambda/4$) apart [29]. However, it is generally safer to use a spacing of one-tenth to one-twentieth of a wavelength ($\lambda/10 - \lambda/20$). If the spacing between vias becomes too small to fabricate, a second row of vias can be added slightly offset from the first to ensure no modes are excited within the side grounds [30]. If these design rules are followed, a matched CPWG trace can be designed for the necessary frequency band.

The HFSS model of Figure 2.4 initially used LineCalc's values of $G = 14.007$ mil and $W = 23.622$ mil (0.6 mm). HFSS was then used to tune the CPWG to achieve a good match. The width remains unchanged, but the gap is optimized to $G = 15.196$ mil. The stitching vias have a diameter of 0.5 mm. They are spaced $s = 1$ mm apart which is approximately one-tenth of a wavelength for a frequency of 10 GHz, well above the intended frequency band for this design. Additionally, the via to via spacing $VP = 2.872$ mm corresponds to a cutoff frequency of 16.35 GHz. A return loss of better than 25 dB is achieved, and the resulting S-parameters are shown in Figure 2.5.

An edge launch connector from Southwest Microwave will be used to excite the CPWG trace in the fabricated design, so it must be modeled as well. There are several versions available, but not all are acceptable for this design. The connector model must be chosen based on the diameter of the launch pin and the diameter of the dielectric surrounding it. First, the pin needs to be narrower than the center trace of the CPWG. Southwest Microwave offers models with diameters of 5, 7, and 10 mil so all are acceptable for this design. However, the diameter of the dielectric must also be larger than the sum of the CPWG's center trace and gaps to ensure the connector housing does not extend into the CPWG's gaps and compromise the match. For this design, the sum of the widths and gaps is 54.014 mil. The 1092-03A-5 has the smallest acceptable dielectric diameter of 63.5 mil and a

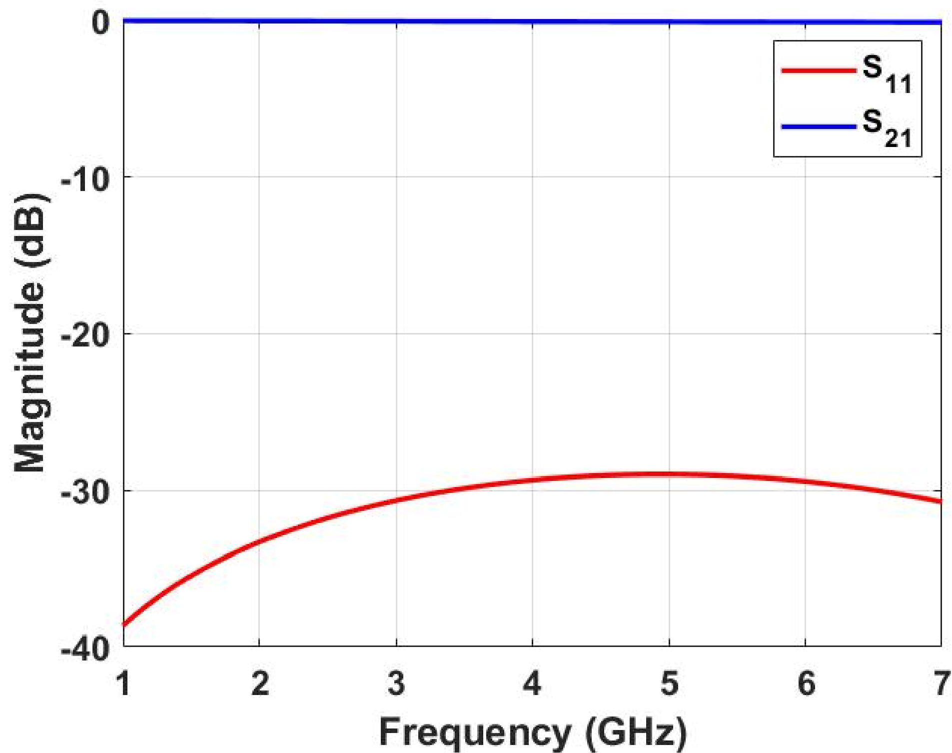


Figure 2.5: Simulated S-parameters of the tuned CPWG

10 mil launch pin, so it is selected for this design [31]. It has actually been replaced by the 1092-03A-6, which is identical except that its mounting bolts do not extend above the connector body, but a set of 1092-03A-5 connectors were already available for use. An HFSS model of the newer connector is available from Southwest Microwave, and it is used to create more detailed simulations.

From Figure 2.6, it can be seen that there is a center pin that extends from the edge launch connector to the center trace. This pin adds capacitance to the design and must be compensated for to get a truly optimized simulation. This capacitance can be compensated for by adding inductance to the design. For CPWG, this inductance can be added by tapering the center trace for the length of the center pin [32]. Ideally, the width at the edge of the board should be exactly the same as the

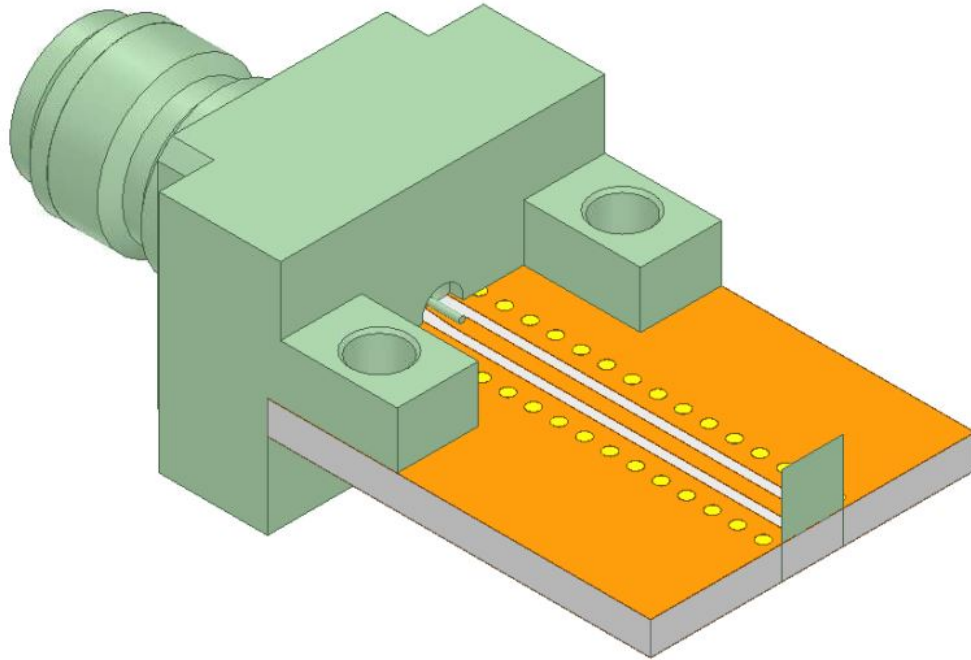


Figure 2.6: HFSS model of the connector to CPWG transition

center pin's width, but this is not practical for physical implementation since there will inevitably be some misalignment. Therefore, the center trace is left slightly wider than the center pin. Figure 2.7 illustrates the final taper dimensions achieved. The width at the edge of the board is $W_1 = 16$ mil while the length of the taper is $L = 50$ mil.

The connector also requires specific pads to mount to the substrate because it should not be soldered to the CPWG center trace or grounds. These are presented in Figure 2.8. First, two bolt holes with a diameter of 2 mm must be added, spaced 375 mil center to center (X_b) and 110 mil from the edge of the substrate (Y_b). Four plated vias should be added surrounding the bolt holes to ensure there are good connections to ground around the bolts. The connector is exactly 12.7 mm wide (500 mil), so the side-ground to side-ground width (X_s) should be at least that

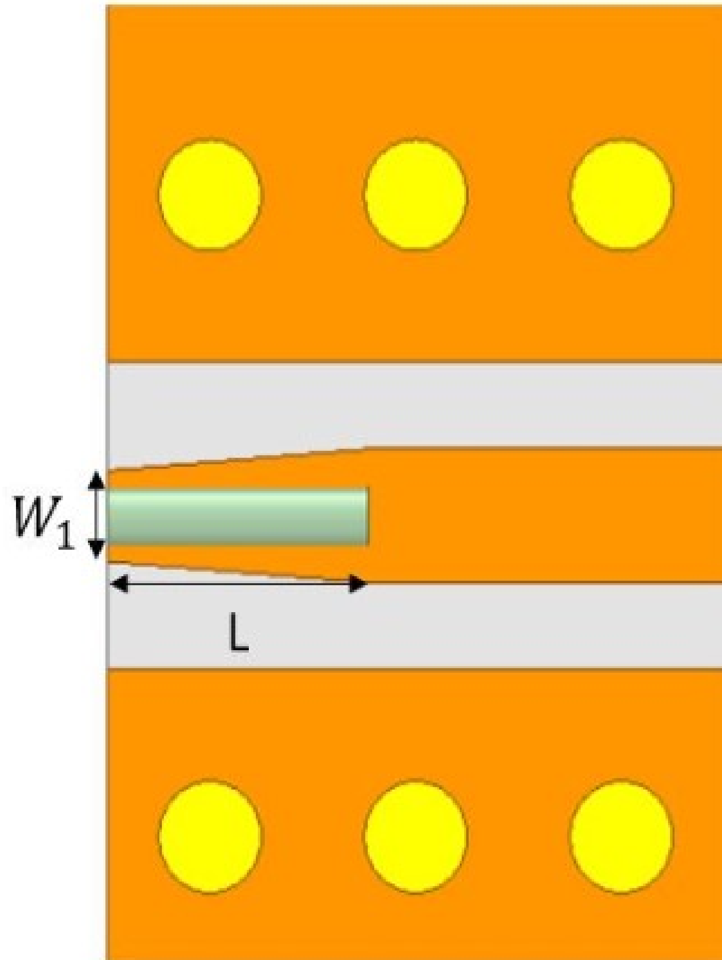


Figure 2.7: Top down view of the taper to illustrate its dimensions

wide. For this design, it is made 13.5 mm to avoid any alignment issues.

The original CPWG model is then modified so one side has the Southwest Microwave connector and taper while the other side feeds into a wave port. In the full SISL structure, one end of the CPWG should go into the castellated via transition, which should be designed for 50Ω and can be modeled as a wave port for now. Figure 2.9 shows the S-parameters of this model. It can be seen that the return loss remains better than 20 dB, and insertion loss remains negligible.

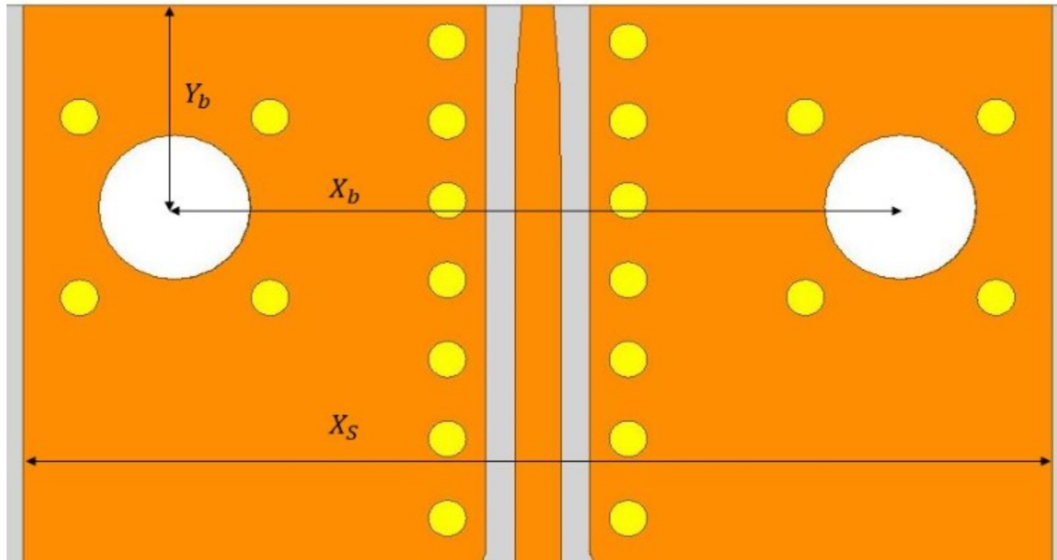


Figure 2.8: Top down view to illustrate pads for the Southwest Microwave connectors

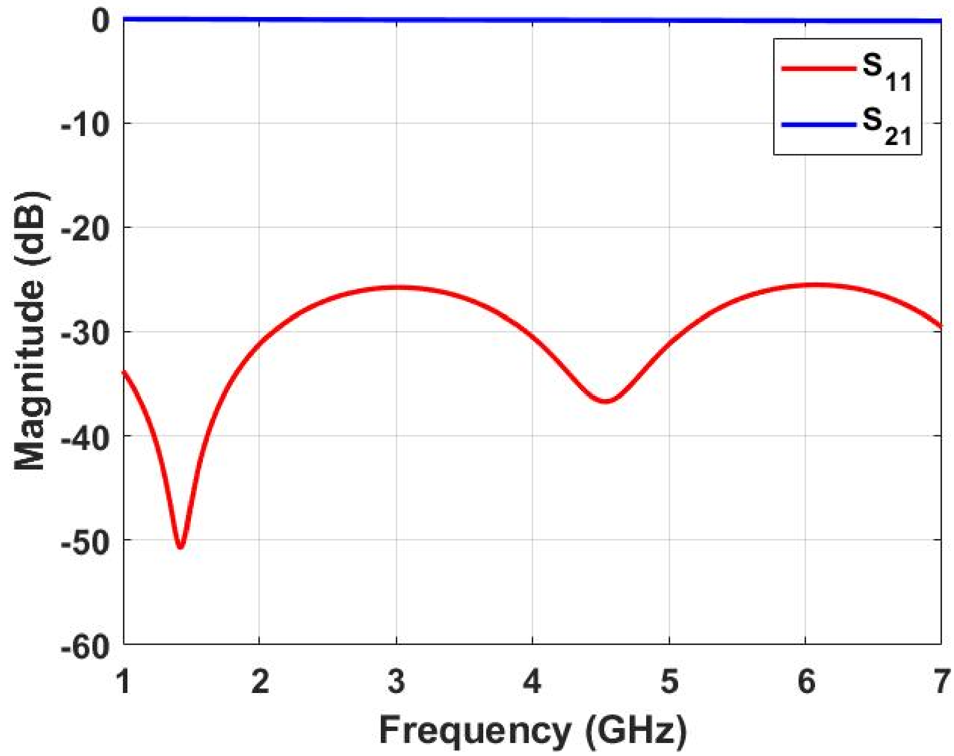


Figure 2.9: S-parameters of the tapered CPWG with connector model

2.1.3 Strip-Line Design

Figure 2.10 shows the geometry and field distributions of a strip-line trace. The characteristic impedance of this transmission line is controlled by both the width of the center trace, W, and the space between the ground planes, b. The biggest difference between CPWG and strip-line is that all fields are contained within the substrate. Because of this, there will be almost no radiated loss and the losses will be dominated by the dielectric which is why choosing materials with a low dielectric loss tangent is important.

Figure 2.11 shows the strip-line for this design modeled in HFSS. The only major change from Figure 2.10 is the addition of sidewall vias. Much like in the CPWG design, these vias are necessary to suppress any parallel plate modes that could be excited. These can be avoided by restricting the sidewall width to less than half wavelength ($\lambda/2$) through the use of plated vias [2]. Additionally, the sidewall vias should be close to the board edge and run the length of the strip-line as discussed in the CPWG design.

Closed form equations are provided by [2], but they are not very useful for this design because they assume the strip-line trace is perfectly centered in the middle of the dielectric. However, this design is made up of three substrates, so the center

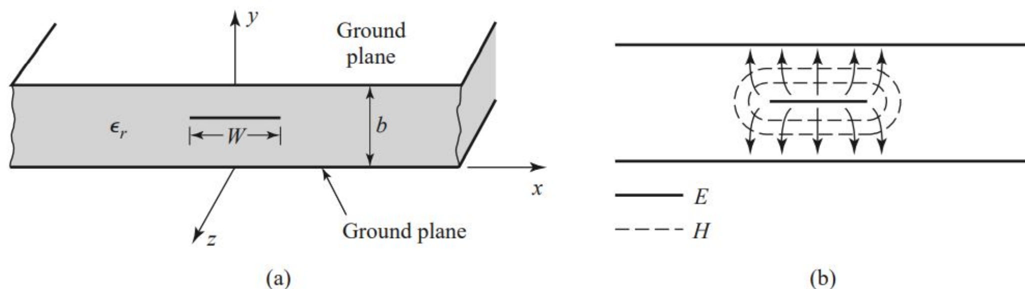


Figure 2.10: Geometry and field distributions of a strip-line [2]

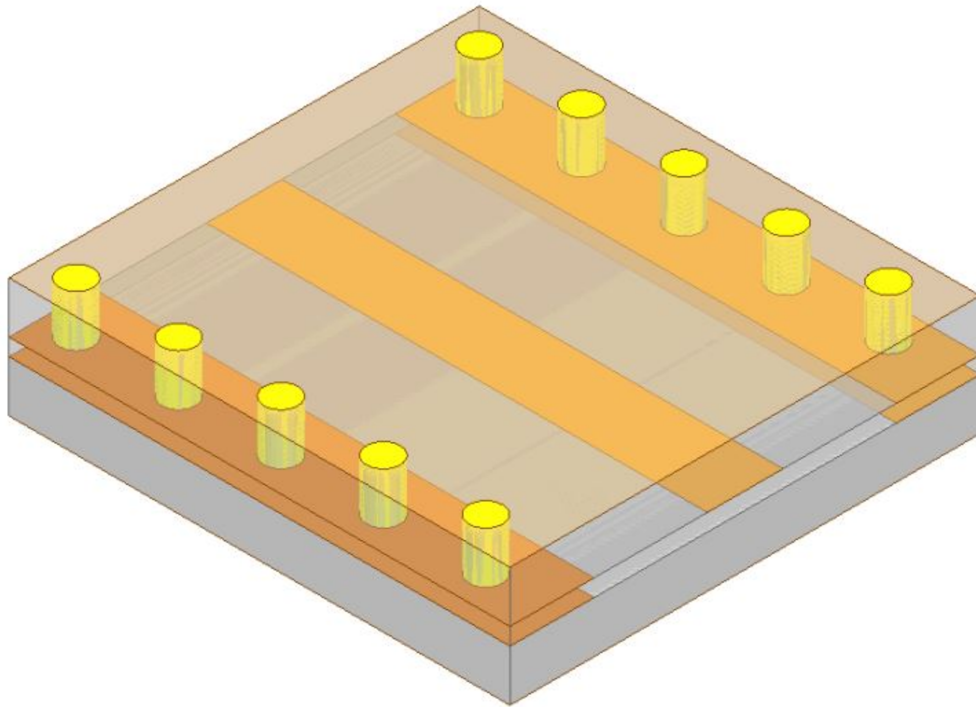


Figure 2.11: HFSS model of the strip-line transmission line

trace is not centered perfectly between the two ground planes, creating an offset. Fortunately, LineCalc includes an offset strip-line template, as shown in Figure 2.12 which accounts for the effects of the offset and provides an accurate design.

Typically, the goal is to solve for the center trace width (W) that provides a 50Ω characteristic impedance. The space between ground planes (b), offset (s), and copper thickness (t) are all necessary for the calculator. In the SISL structure, the spacing between the ground planes is determined by the thicknesses of Substrates 2-4. For the substrates chosen earlier, $b = 70$ mil. The offset is determined by the thickness of Substrate 3, so $s = 10$ mil. Finally, $t = 17.5\ \mu m$ because all substrates have half-ounce copper. Entering these values into LineCalc's SLINO template produces a width of 42.3 mil.

The above dimensions are then used to model the strip-line trace in HFSS, as

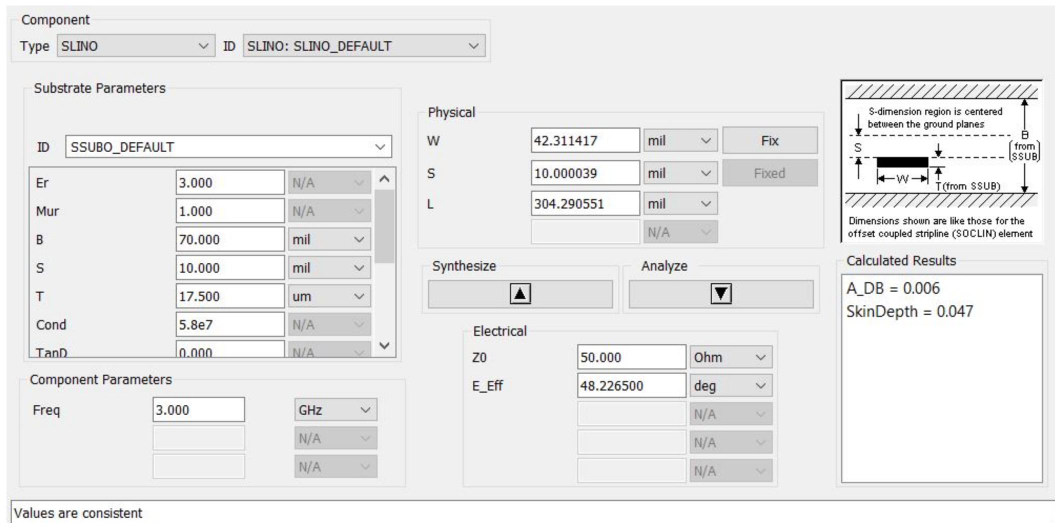


Figure 2.12: Example offset strip-line template within ADS

shown in Figure 2.11. Wall vias with a diameter of 0.5 mm are placed every 1.524 mm, which is less than $\lambda/10$ for an upper frequency of 10 GHz. The width of the strip-line is then tuned to 44.25 mil using HFSS. The return loss of the simulated strip-line transmission line is better than 30 dB, indicating a good match. The S-parameters are shown in Figure 2.13.

2.1.4 Castellated Via Transition

A castellated via has been chosen as the best way to access the SISL cavity. Castellated vias are standard vias that have been cut in half, making the conductive plating external. This avoids the alignment and soldering issues of [18] because the signal via is now readily accessible and can easily be inspected and soldered to the carrier board. Figure 2.14 shows the proposed via transition together with the CPWG and strip-line traces that have already been designed.

There are two challenges to designing a signal via transition. First, the via needs to be matched to the system's characteristic impedance over the frequency band of

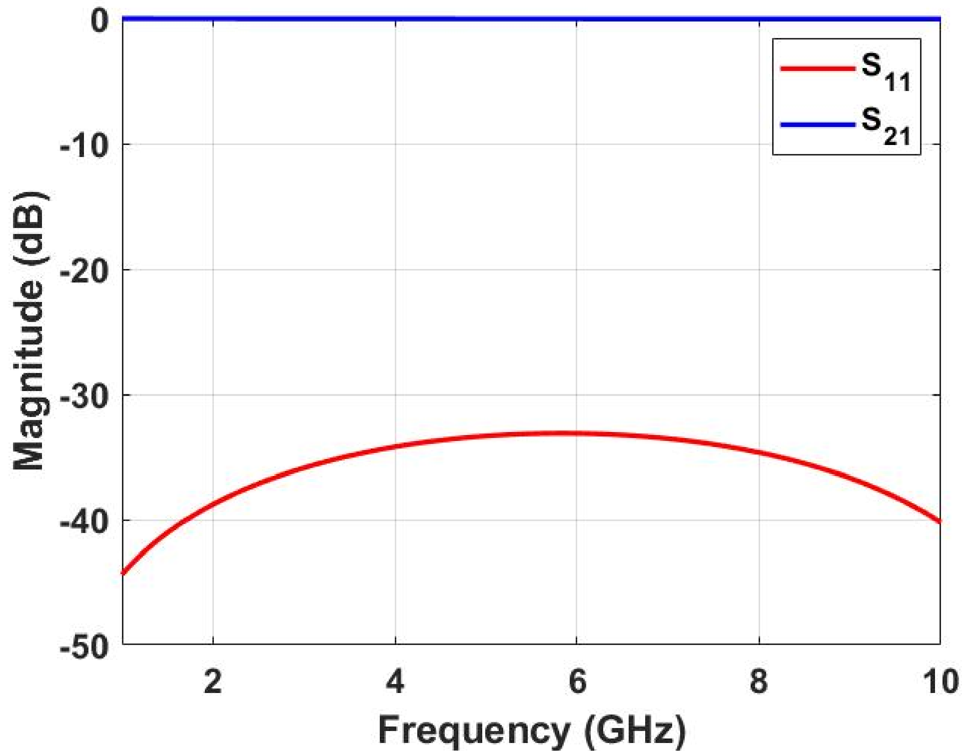


Figure 2.13: Simulated S-parameters of the tuned strip-line

interest to minimize losses. The transition's characteristic impedance is given by (2.3) which illustrates that it is a ratio of the inductance per unit length to capacitance per unit length. Therefore, the inductance must be 2,500 times the capacitance to achieve a 50Ω match. Second, the via transition looks like a low pass filter (LPF) because of its associated capacitances and inductances. The capacitances and inductances must be carefully designed to ensure the cutoff frequency of the LPF is well above the frequency band of interest. These are controlled by the via's length, diameter, pads, and anti-pads. By making either the inductance or capacitance bigger, the cutoff frequency of the LPF will be shifted lower in frequency. Therefore, the via transition design process must make both the inductance and capacitance sufficiently small to push the LPF cutoff out of the band of interest while also mak-

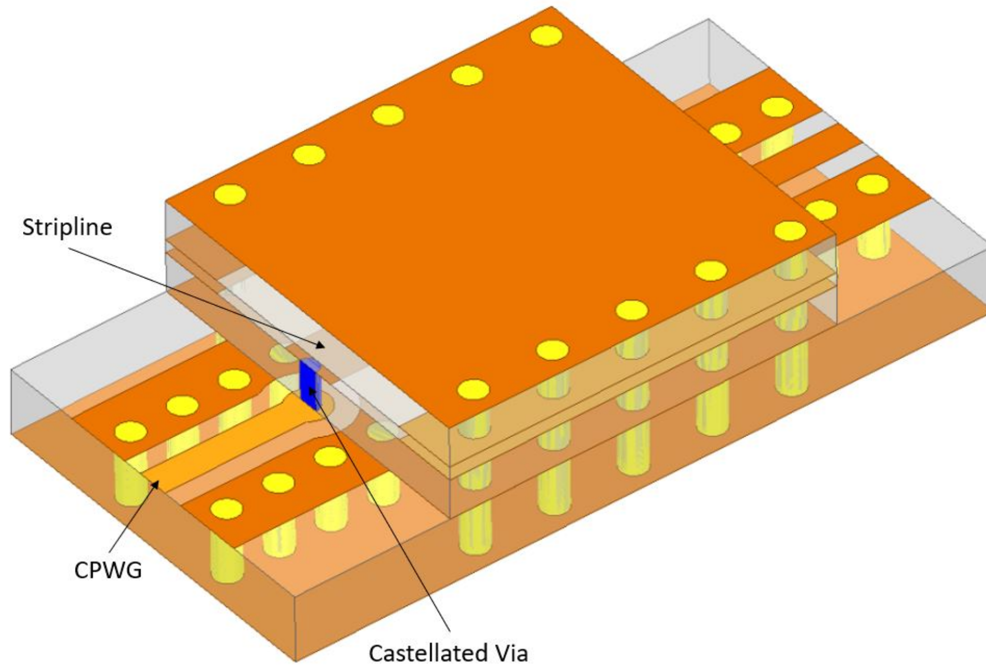


Figure 2.14: HFSS model used to design the castellated via

ing the inductance big enough to achieve a good match:

$$Z_0 = \sqrt{\frac{L}{C}}. \tag{2.3}$$

Equations to calculate the capacitances and inductances for given dimensions have been synthesized for standard vias, but none have been synthesized for castellated vias [33]. Intuitively, the capacitances should be halved while the inductances should be doubled when going from a standard via to castellated. The inductances are controlled by the length of the via and the diameter. The diameter of the via should be fixed to a value that can be fabricated and plated while the length of the via is determined by the substrate and cannot be adjusted. Instead, most of the tuning should be done with the capacitances which are controlled by the gaps between the via pad and its anti-pad (cutout to avoid a short), as shown in Figure 2.15.

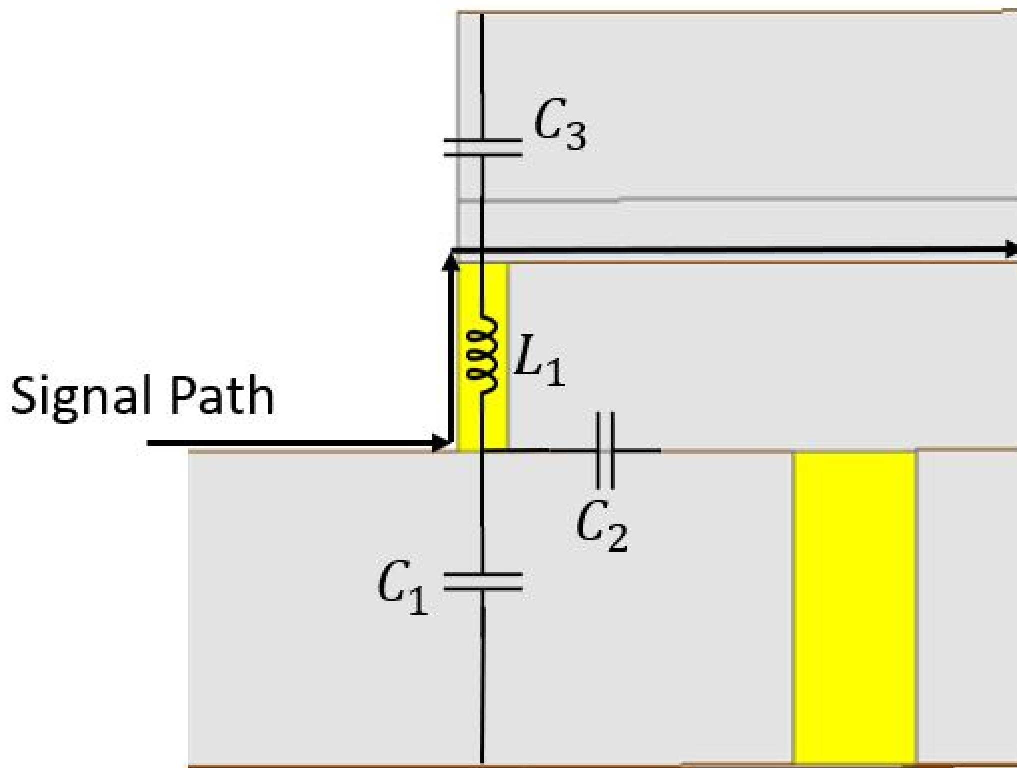


Figure 2.15: Side-view of the castellated via transition to illustrate its capacitances and inductance

Although the capacitances can be tuned, there are still some limitations due to manufacturing requirements. Gaps cannot be made too small to fabricate (typically less than 10 mil), and there are size restrictions on both the pad and anti-pad. The pad's diameter should be twice the diameter of the via to ensure proper plating and avoid any alignment issues. The anti-pad's size restrictions are less specific, but too big of an anti-pad will result in degradation of the strip-line trace's S-parameters because it takes away from the lower ground plane of the strip-line trace. This places a fundamental limitation on how small the capacitance can be made, which also places a limit on the inductance necessary to maintain a good match. All of this means that the LPF cutoff frequency can only be pushed so high in frequency.

A model is created in HFSS since design equations for castellated vias are not

readily available. Figure 2.14 shows the model used to tune the design. There is a carrier board of 50 mil thick Rogers RO3010 material that has the CPWG input and output traces designed previously. The CPWG traces go directly into the castellated vias which are joined together by the strip-line trace designed before. The CPWG and strip-line were designed to 50Ω and confirmed to be well matched, so any potential mismatches in the design can be attributed to the castellated vias. The dimensions of the via transitions can then be tuned to achieve a good match and transmission.

The via's length is constrained by Substrate 2's height of 30 mil. This length is not necessarily optimal for the castellated via design, but it is required for the SISL design. Initial experimentation found that a smaller diameter via is easier to achieve a good match for because it makes the inductance large enough that a realizable capacitance can be used. Therefore, the diameter is set to 0.4 mm because it is a relatively small via that can consistently be plated. This then leaves only three capacitances to tune. C_1 can be tuned by removing copper from the ground plane directly beneath the via. Similarly, C_3 can be tuned by removing copper from the upper ground plane. However, neither is desirable because it will introduce an extra fabrication step for both the carrier board and top substrate. Further, these capacitances have less of an impact on the via's behavior due to the distance between the via and the ground planes. This leaves only C_2 to be adjusted by tuning the anti-pad. Simulations are run for various anti-pad diameters, and the anti-pad is adjusted until acceptable S-parameters are achieved. The final anti-pad diameter is 0.8 mm.

The model is simulated from 1-10 GHz, and its S-parameters are then plotted, as shown in Figure 2.16. It can be seen that the return loss is nearly 35 dB from 1-6 GHz which indicates a very good match. It remains better than 20 dB almost as high as 10 GHz, well above the frequency band of this design. Additionally, the

insertion loss is better than 0.35 dB up to 6 GHz, and better than 1 dB up to 10 GHz, indicating the vias do not introduce significant losses.

In the above model, the carrier board also acts as the lower metal ground plane for the strip-line trace and SISL cavity. In [18], the SMT design has both a carrier board and additional 10 mil thick substrate which acts as the lower ground plane. This earlier design takes that of [5] and makes it surface mount by flipping the design and placing it on a carrier board. This introduces extra capacitance and inductance, as shown in Figure 2.17. First, the via becomes longer and is now modeled as two inductances, L_1 and L_2. There is also a second capacitance between the via and its anti-pad, modeled as C_3.

The additional capacitance introduces another dimension to tune which can be

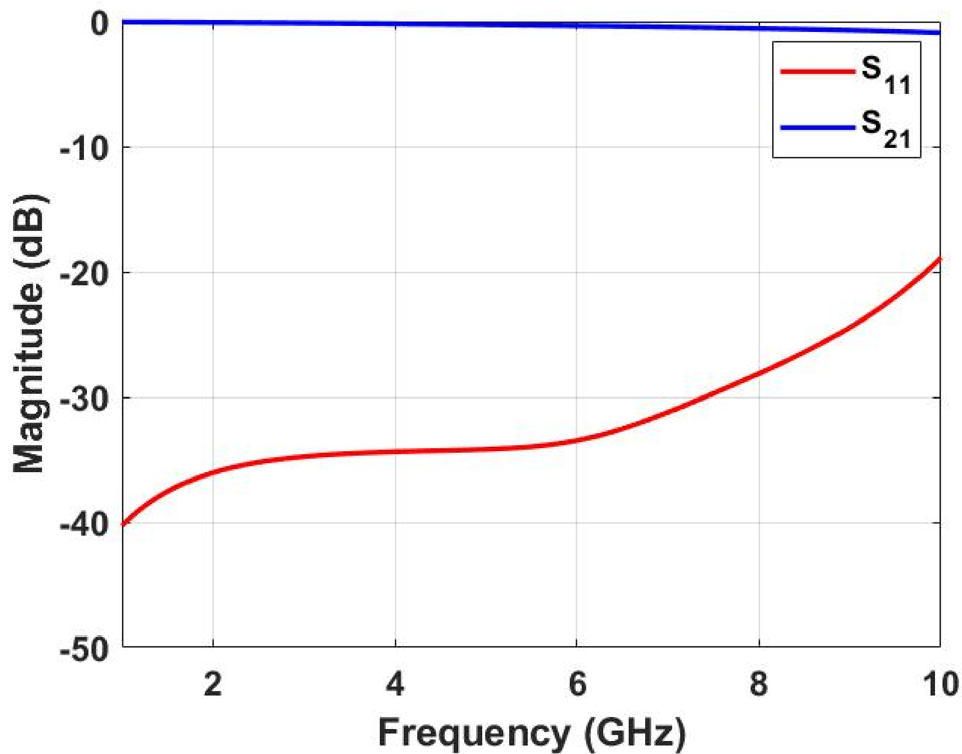


Figure 2.16: S-parameters of the final castellated via transition

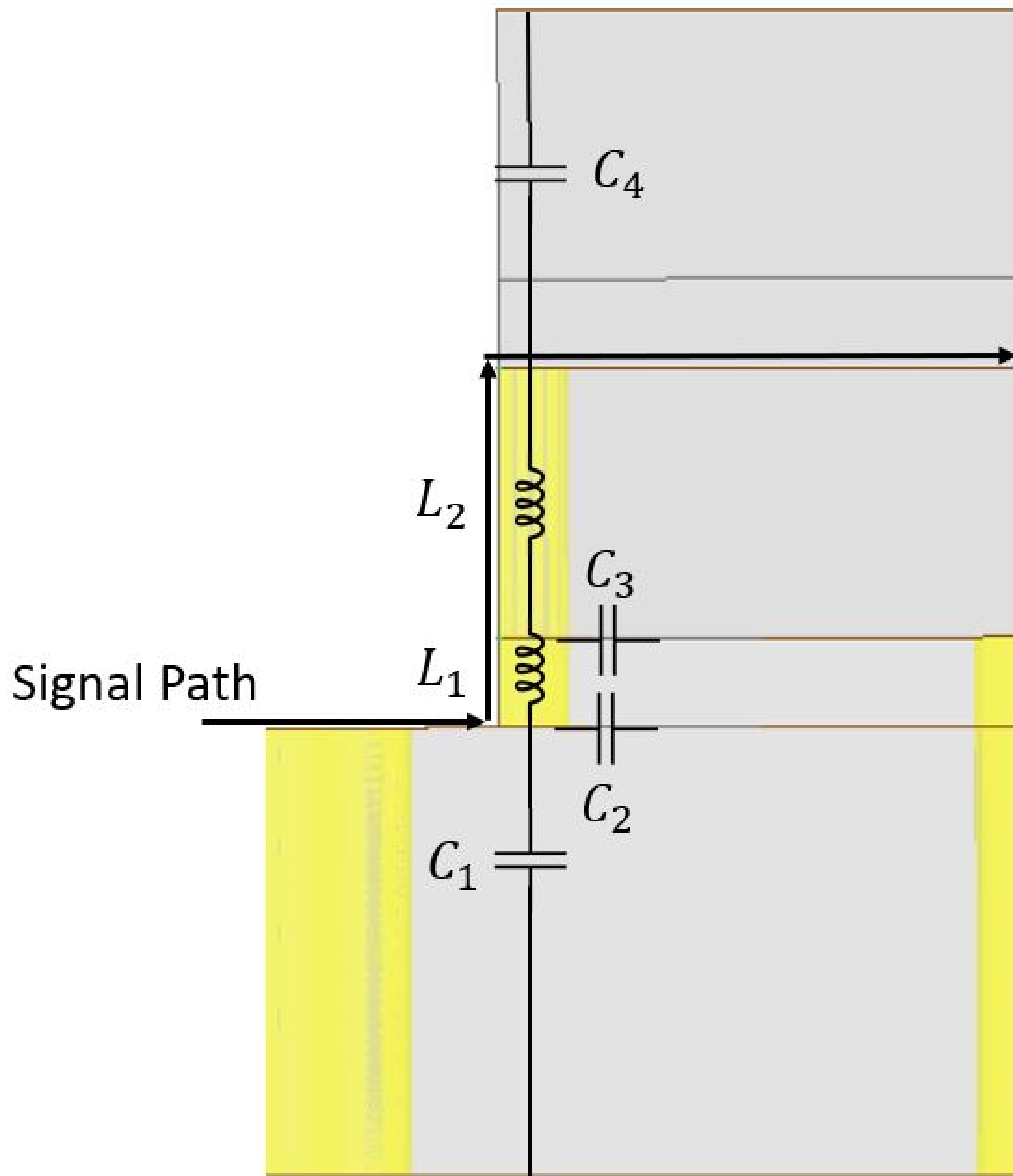


Figure 2.17: Side-view of the castellated via transition with additional substrate

useful in getting an excellent match. However, the additional inductance is a problem for getting a wide-band via transition because it lowers the cutoff frequency of the transition. This effect is illustrated in Figure 2.18. An additional substrate is added between the carrier board and Substrate 2 to emulate the transition of [18] and illustrate the benefit of removing it. The transition remains castellated, and

each simulation's anti-pads are tuned to achieve a good match. It is very clear that the usable bandwidth decreases as the extra substrate gets thicker. With no extra substrate (the design explored earlier), the return loss is better than 20 dB up to 9.75 GHz. Adding a 10 mil thick substrate lowers the well matched bandwidth to 9.15 GHz. Thickening the extra substrate continues to lower the well matched bandwidth, reaching less than 8 GHz with a 40 mil thick board. Clearly, removing the additional substrate and reducing the inductance is key in making the castellated via transition useful over a wider frequency range.

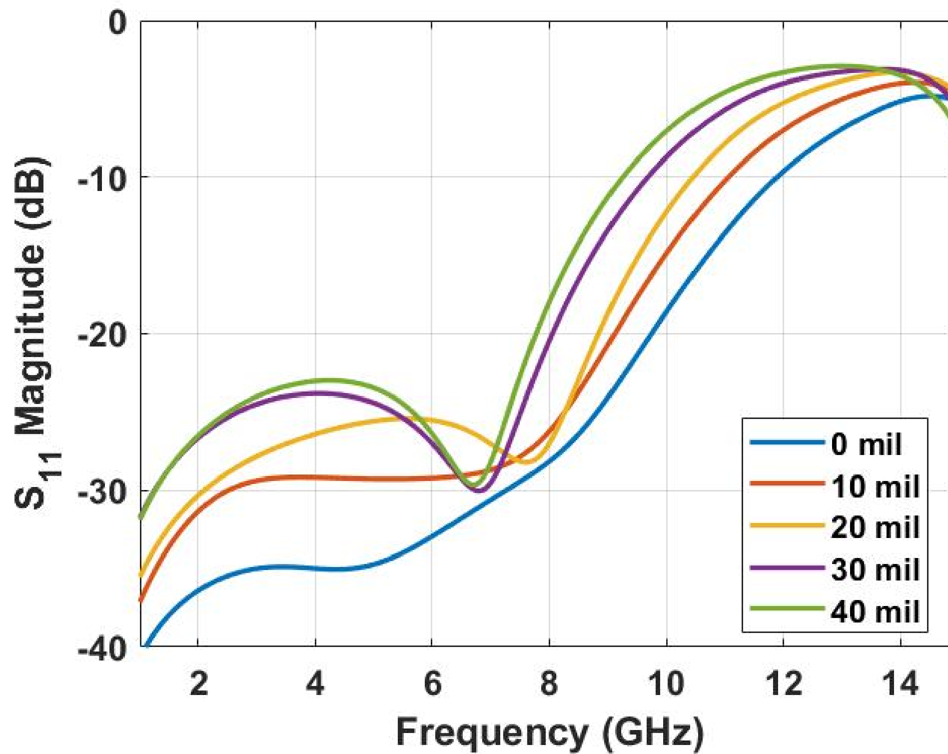


Figure 2.18: S_{11} of the castellated via transition comparing different thicknesses of the extra substrate with no additional substrate

2.1.5 SISL Thru-line Design

The effective permittivity (ϵ_{eff}) of the SISL air cavity is an important consideration when designing SISL components. The length and width of transmission lines are extremely important in achieving a good match, and they are controlled by the dielectric constant. The SISL cavity is mostly air, but its effective permittivity will not be exactly one because Substrate 3 loads the cavity. Since Substrate 3 is very thin (10 mil) and has a low dielectric constant (3), it will not significantly increase the effective permittivity of the cavity.

In [5] a way to measure the effective permittivity using both ADS and HFSS simulations was determined, but newer versions of HFSS have greatly simplified the procedure. First, the cavity and its wall vias should be modeled in HFSS, as shown in Figure 2.19. Note that all other portions of the model have been deleted. Waveports are placed along the entirety of the open ends of the cavity, where the

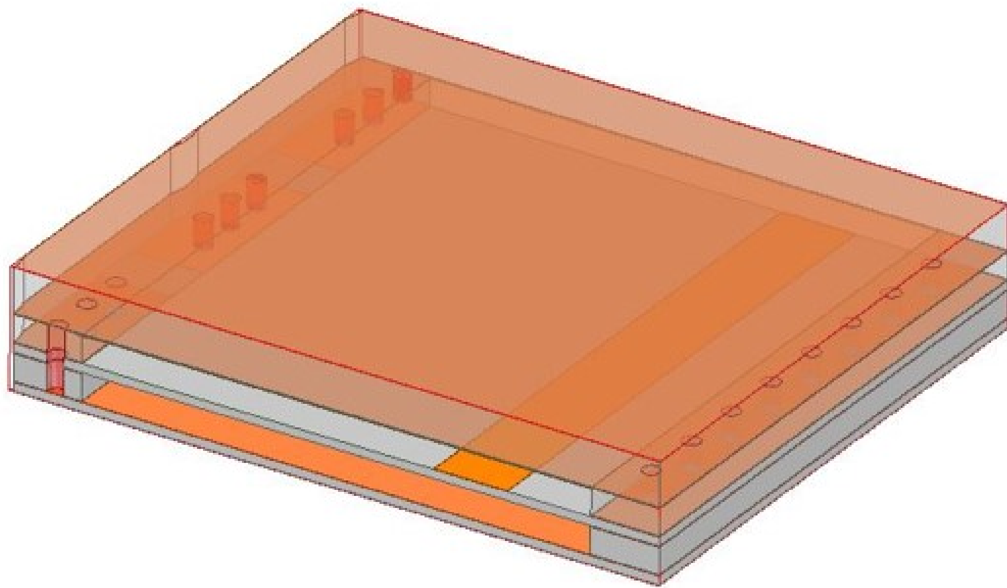


Figure 2.19: HFSS model used to calculate ϵ_{eff}

strip-line traces would connect with the SISL cavity. An air box is then drawn within the cavity to ensure it is properly modeled as air. The thru-line can be added to the model, but it will have minimal impact on the result of the simulation.

A driven modal simulation is run from $1 - 7$ GHz. In the plot results menu where S-parameters are normally selected, 'Epsilon' should be chosen instead. This then produces the effective permittivity of the cavity across the frequency sweep as shown in Figure 2.20. Initially, it seems like the effective permittivity fluctuates greatly with frequency, but it only ranges from $1.2065 - 1.2078$ which is small enough to be a rounding error. Rounding these values off produces an effective permittivity of 1.21 which is used for the next stage of the design.

With the effective permittivity determined, the thru-line's width can then be

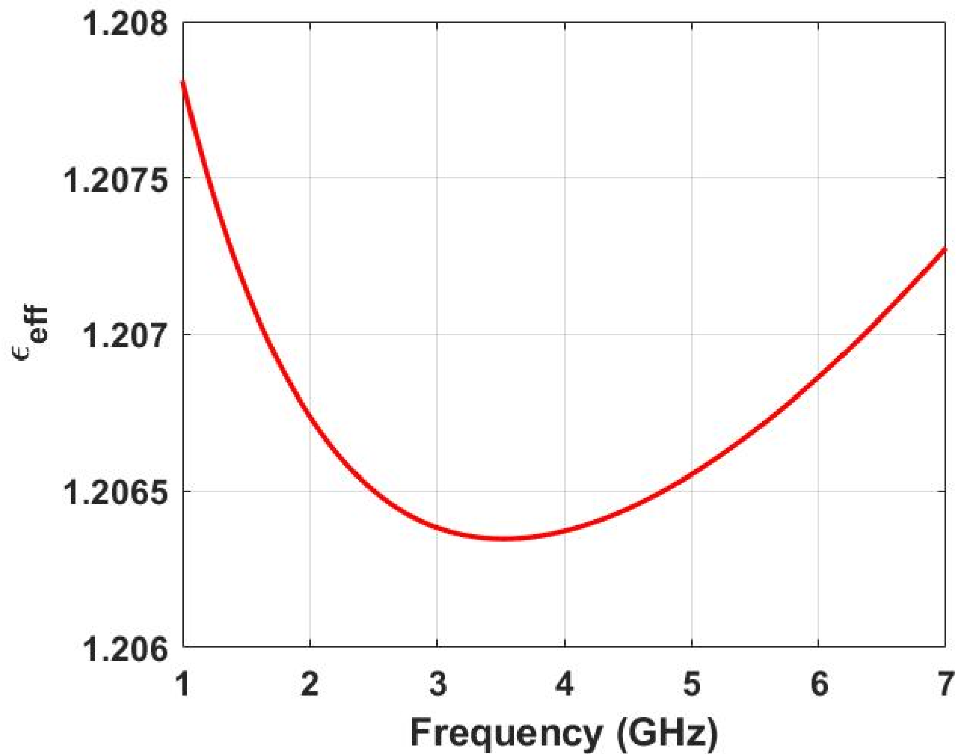


Figure 2.20: Effective permittivity of the cavity over frequency

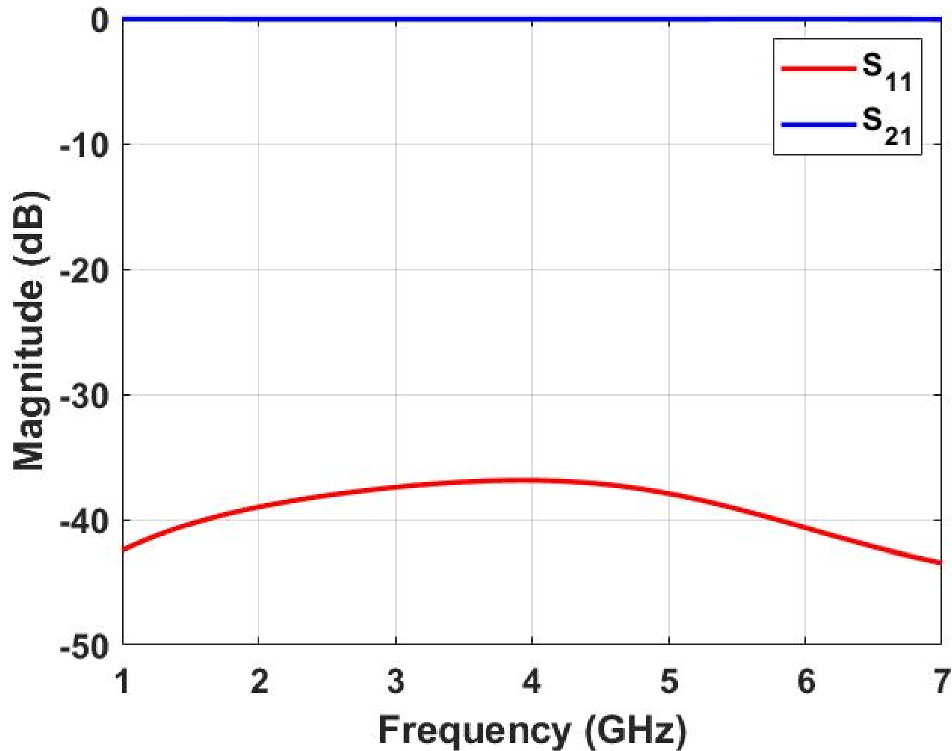


Figure 2.21: S-parameters of the optimized SISL thru-line

determined. SISL can be modeled as a strip-line within a dielectric with a dielectric constant of the effective permittivity of the cavity. Therefore, the same SLINO template from LineCalc can be used, and all that must change is relative permittivity used. Entering 1.21 produces a width of 84.244 mil to achieve a 50Ω match. Figure 2.19 is then used to optimize the width to 84.1 mil. The resulting S-parameters are shown in Figure 2.21. The S-parameters are better than 35 dB across the entirety of the simulation, indicating an excellent match.

2.2 SISL Cavity Design

Plated vias around the edges of the cavity are necessary to create metal side-walls which will isolate the cavity from the rest of the packaging and avoid uninten-

tional excitation of parallel plate modes. The location of these vias will effectively determine the dimensions of the cavity, and they must be carefully chosen because they create an effective waveguide together with copper layers M2 and M9. This can cause the excitation of other waveguide modes which are not desirable within the passband.

The three important dimensions of the SISL cavity are width (a), height (b), and length (c). The height is determined by the thickness of Substrates 2, 3, and 4, together with their associated copper thicknesses. The width and length are measured from via-to-via, as shown in Figure 2.22, because the vias act as the metal walls of the cavity.

The first parasitic waveguide mode that can be excited is TE_{10}. This mode is excited because the width of the cavity is greater than the height. If the cavity becomes too wide, the TE_{10} mode will be excited at a frequency within the passband,

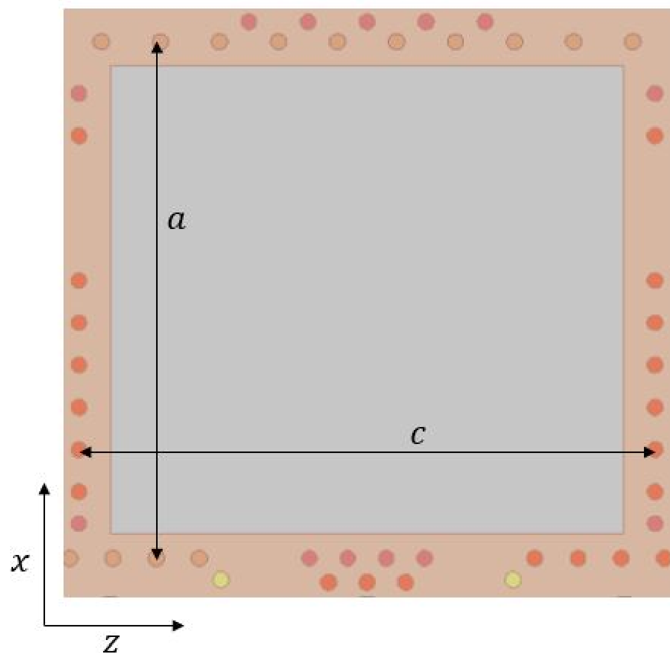


Figure 2.22: Via-to-via dimensions of the SISL cavity

which will cause mode-splitting and degrade the performance. Therefore, the width should be made small enough that the cutoff frequency of the waveguide is above the band of interest. Equation 2.4 can be used to calculate the waveguide's cutoff frequency where c is the speed of light, ϵ_{eff} is the effective relative permittivity calculated for the SISL cavity, and a is the width of the cavity:

$$(f_c)_{10} = \frac{c}{2a\sqrt{\epsilon_{eff}}} \quad (2.4)$$

For this design, $a = 16.3$ mm which results in a cutoff frequency of 8.36 GHz. This is well above the frequency band of interest, so no issues should arise.

The SISL cavity will also become a resonant cavity at some point, and it is essential to keep this resonance outside of the passband. The first resonant mode is TE_{101} because the length (c) of the cavity is greater than the width and height. This resonance can be calculated using (2.5):

$$f_{r101} = \frac{c}{2\sqrt{\epsilon_{eff}}}\sqrt{\left(\frac{1}{a}\right)^2 + \left(\frac{1}{c}\right)^2} \quad (2.5)$$

For this design, the via-to-via length is $c = 18.1625$ mm. This produces a resonance at 11.23 GHz, again outside the frequency band of interest.

The dimensions of this cavity are much larger than necessary for the thru-line, but they are chosen to allow the future tunable filter to fit within. The goal is to allow both designs to be placed within the same stack-up, minimizing the number of PCBs that must be fabricated. Further, gaps in the via cage are made for the tunable filter design while a second row of wall vias are added. These changes will be discussed in more depth in Chapter 3.

2.3 Surface Mount SISL Thru-line Simulations

Now that the sub-components of the design have been modeled in HFSS, they are combined into the complete model. This consists of the thru-line, two strip-line sections, two castellated via transitions, and two CPWG traces. Bolts are used to hold all of the substrates together, so 4 mm diameter holes are drilled. An HFSS simulation is then run to ensure the bolts' location do not create any unintentional resonances. A 3D model of the final design is shown in Figure 2.23. The castellated vias and transmission lines on the right side of the carrier board are not necessary for this design, and they are not connected to anything on Substrate 3. HFSS simulations determined that they have no impact on this design's performance, but they will be essential to the design in Chapter 3.

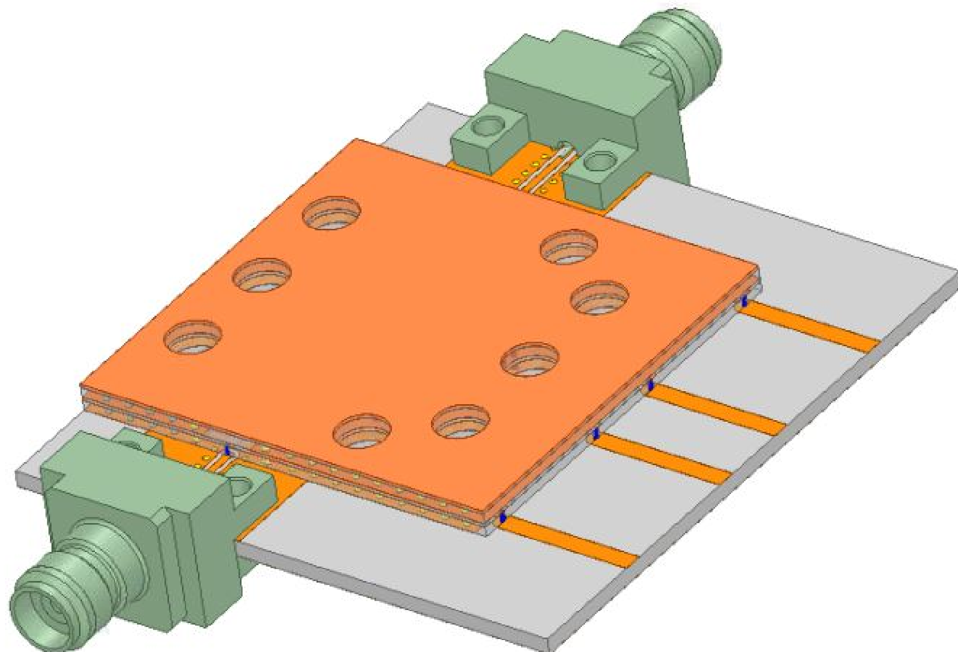


Figure 2.23: 3-D model of the final SISL thru-line design

The design is then simulated from $1-7$ GHz, and Figure 2.24 shows the result. It can be seen that the return loss is better than 20 dB across S-band which indicates a good match. The insertion loss is better than 0.25 dB across S-band and is still better than 0.41 dB at 7 GHz. Even with the castellated vias and connectors, the system is still well matched and has relatively low loss which indicates the feasibility of this surface mounting technique.

With the feasibility of the novel surface mountable structure confirmed, it is time to explore a more practical application of the technology. It would be useful to investigate the possibility of adding additional via transitions to fully demonstrate the SMT capability of the design. Tunable filters are a popular method to reduce C-SWaP, benefit from the SISL cavity's radiation capture, and require some

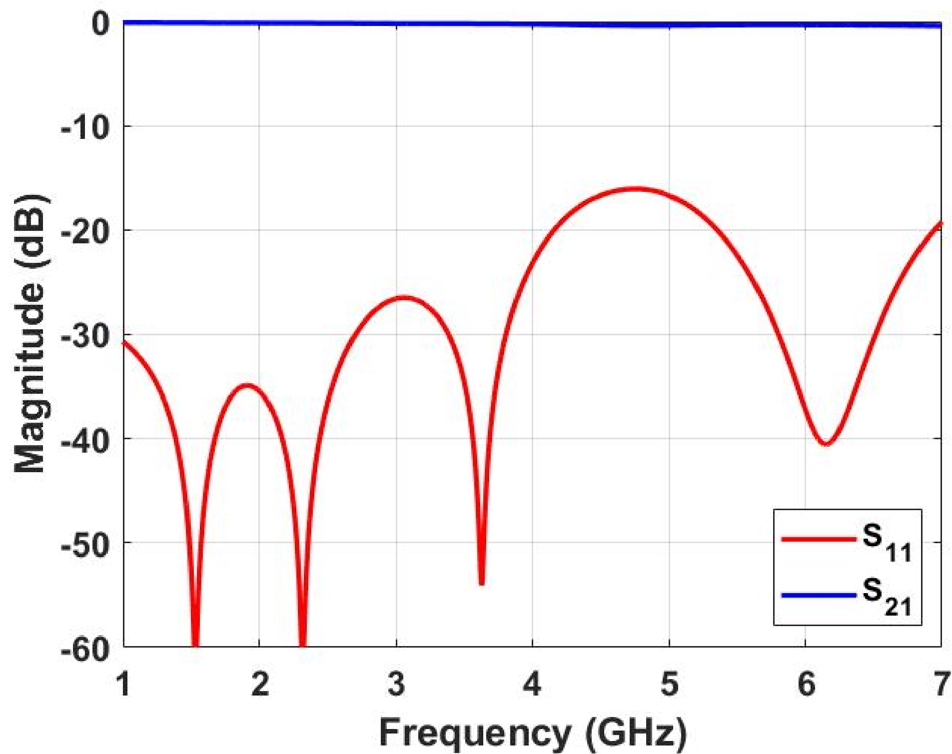


Figure 2.24: Simulated S-parameters of the full surface mount SISL thru-line

biasing structure to enable frequency tuning. Therefore, a tunable filter design is an interesting application for the SMT design which will be explored in the next chapter.

Chapter 3

Tunable Filter Design and Implementation

The purpose of this chapter is to apply the surface mount SISL technology to the design of a tunable filter. This chapter will provide design guidelines and additional considerations. A second-order Butterworth bandpass filter with center frequencies tunable from 2.3-3.9 GHz and a 0.5 GHz bandwidth is designed, fabricated, and measured to demonstrate the technology. This design will illustrate several of the advantages of the SMT SISL design.

3.1 SISL Tunable Filter Design

Figure 3.1 shows the exploded view of the tunable BPF implemented in the SMT SISL technology. Because the passband of the filter will be within the frequency band the thru-line of Chapter 2 was designed for, no modifications need to be made to the stack-up or the castellated via transition. Therefore, only the thru-line section needs to be replaced by the SISL filter design. Another advantage of using the same stack-up is that it allows multiple designs to be manufactured and tested by replacing a single layer (Substrate 3).

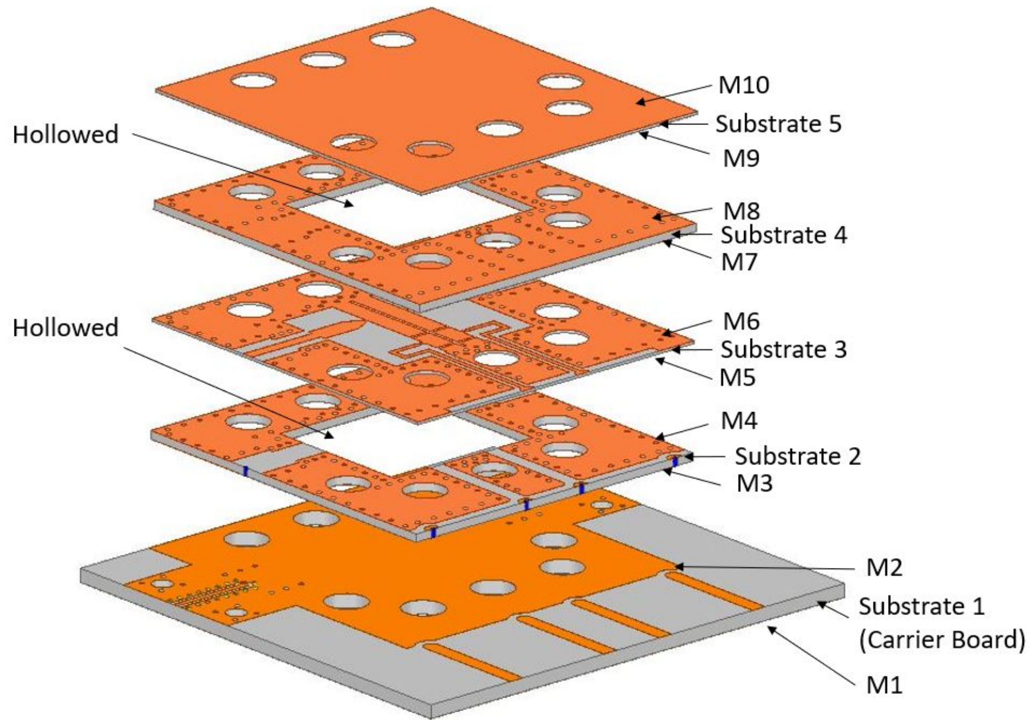


Figure 3.1: Exploded view of the proposed surface mount SISL filter

3.1.1 Filter Characteristics

This filter is designed to operate in S-band because that band is one of the most used and is becoming increasingly crowded, making it prime real estate for the benefits of a tunable filter. Therefore, the center of the tuning range is set to 3 GHz with the goal of tuning the center frequency (f_0) as far as possible higher and lower. S-band covers 2-4 GHz, so ideally the filter would be able to cover the entire range. Since this design is a proof-of-concept, a second-order Butterworth response is chosen.

A combline topology is chosen for this filter because it is one of the easiest structures to make tunable. The fixed capacitors of a traditional combline filter just need to be replaced with variable capacitors. For this work, Skyworks SMV1405

varactor diodes are chosen [34]. The diodes' capacitance can change from 2.67-0.63 pF as reverse bias from 0-30 V is applied. By varying the capacitance, the electrical length of the resonator is varied, changing the resonant frequency.

3.1.2 Design Equations

The first step in designing a filter is to use the filter type and order to calculate the prototype coefficients. The prototype coefficients for a Butterworth filter with a source impedance of 1Ω and cutoff frequency of 1 rad/s can be calculated using (3.1) and (3.2), where N is the order desired and r is the index.

$$g_r = 2sin\left(\frac{(2r-1)\pi}{2N}\right), r = 1, 2, ..., N \tag{3.1}$$

$$g_{N+1} = 1 \tag{3.2}$$

For the second-order filter desired, this produces $g_1 = g_2 = 1.4142$ and $g_3 = 1$ while $g_0 = 1$ for any Butterworth filter design. The other important specification is the fractional bandwidth, Δ. This is a ratio of the desired passband bandwidth to the center frequency of the filter. For a Butterworth filter, the bandwidth is measured as the frequencies 3 dB below the insertion loss at the center of the passband. The fractional bandwidth can be found using (3.3). For this tunable design, it was decided to design for a center frequency (f_0) of 3 GHz and bandwidth (BW) of 500 MHz, producing a fractional bandwidth of $\Delta = 0.1667$.

$$\Delta = \frac{BW}{f_0} \tag{3.3}$$

Two parameters control the shape and performance of a filter: inter-resonator (or internal) coupling and external quality factor. Inter-resonator coupling is a measure

of how strongly the fields of one resonator couple into the next. For most planar filters, this can be controlled by the gap between the resonators, where a smaller gap creates a stronger coupling. The external quality factor is a measure of the external coupling, with a higher external quality factor corresponding to weaker coupling.

The ideal inter-resonator coupling coefficient, $k_{1,2}$, is calculated using (3.4), where Δ is the fractional bandwidth calculated with (3.3). For a center frequency of 3 GHz and bandwidth of 0.5 GHz, this results in $k_{1,2} = 0.11785$. For higher-order filters, coupling coefficients between them can be calculated in the same way.

$$k_{1,2} = \frac{\Delta}{\sqrt{g_1 g_2}} \tag{3.4}$$

The ideal external quality factor can then be calculated using (3.5) and (3.6). Equation (3.5) calculates the external quality factor of the input while (3.6) calculates it for the output. For this design and many others, the prototype coefficients have symmetry and result in equal external quality factors. With the fractional bandwidth calculated in (3.3), $Q_{ext} = 8.4852$ for this work.

$$Q_{ext} = \frac{g_0 g_1}{\Delta} \tag{3.5}$$

$$Q_{ext} = \frac{g_N g_{N+1}}{\Delta} \tag{3.6}$$

Since the fractional bandwidth is calculated using center frequency, it will change as the filter's center frequency is tuned. This will then change both the inter-resonator coupling and external quality factor across the frequency band. Figure 3.2 shows the variation in $k_{1,2}$ and Q_{ext} necessary to maintain a bandwidth of 500 MHz and a Butterworth response. $k_{1,2}$ must decrease with frequency, indicating the inter-resonator coupling should weaken while Q_{ext} should increase with frequency,

indicating the external coupling should get weaker as well. However, an actual filter's couplings will not vary to maintain the ideal Butterworth response. Therefore, the filter is designed to meet the required specifications at a center frequency of 3 GHz because it is at the center of the tuning range. As the center frequency is tuned away from 3 GHz, the response will gradually degrade until it is no longer matched nor a Butterworth response.

3.1.3 Internal and External Coupling

A bandpass filter can be designed by matching the actual internal and external couplings to the calculated ideal values. This consists of modeling the actual transmission lines of the filter and adjusting physical properties until there is good alignment. For a combline filter, this consists of adjusting the spacing between the individual resonators and adjusting the tap point.

Cadence Microwave Office (MWO) can simulate high-frequency designs much more quickly than HFSS, so it can be used to save time on the initial filter design. While MWO does not have a SISL model, it was stated in 2.1.5 that the SISL cavity

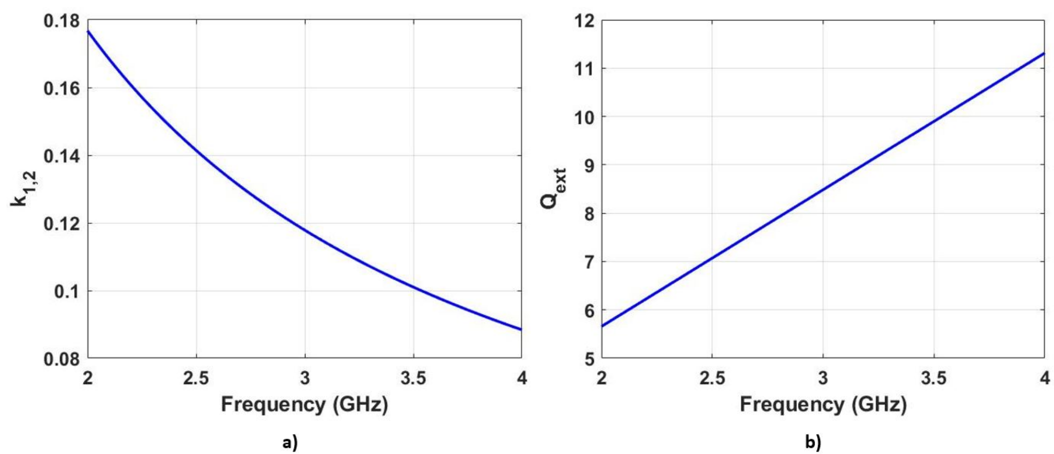


Figure 3.2: $k_{1,2}$ and Q_{ext} necessary to maintain the ideal bandwidth and shape across the tuned center frequencies

can be modeled as a strip-line whose dielectric constant is the effective permittivity of the cavity. Therefore, a strip-line substrate with a dielectric constant of 1.21 is defined. Unfortunately, MWO does not have an offset strip-line model to most accurately represent the actual structure, but its standard strip-line model allows approximate values to be determined, providing a starting point for final tuning in ANSYS HFSS.

Before calculating the external quality factor or inter-resonator coupling, a single resonator is designed. The combline structure will be used because it simply consists of a transmission line shorted to ground on one end and terminated in a lumped capacitor on the other. By replacing the lumped capacitor with a variable one, the center frequency of the resonator can be varied by changing the electrical length. Another way of thinking of this resonator is as a resonant tank circuit where the transmission line provides the inductance and the variable capacitor provides the capacitance. These circuits should resonate at $\frac{1}{\sqrt{LC}}$, so varying the capacitance will change the resonant frequency.

In [35], it was determined that the transmission line should have an electrical length of $53°$, measured at the center of the tuning range, to minimize both bandwidth fluctuations and insertion loss. The wavelength can be calculated using (3.7), where c is the speed of light, ϵ_{eff} is the effective dielectric constant, and f_0 is the center of the tuning range. The optimal length, L, can then be found using (3.8) where the electrical length is set to $53°$. For this design at 3 GHz, $\lambda = 90.462$ mm and $L = 13.36$ mm.

$$\lambda = \frac{c}{\sqrt{\epsilon_{eff}} f_0} \tag{3.7}$$

$$L = \lambda \frac{53°}{360°} \tag{3.8}$$

Skyworks SMV1405 varactor diodes are chosen for this design due to their relatively low loss and useful tuning range. A DC bias of 0 to 30V produces a capacitance of 2.67 to 0.63pF. One important consideration in choosing the varactor diodes is considering how they should be biased and connected to the filter. The combline topology requires a capacitance to ground at the end of the resonator, while the varactors require a reverse bias. Therefore, a single varactor cannot be placed at the end of the resonator because the combline topology's requirements can't be satisfied. One end of the resonator needs to be grounded while the other end needs to be terminated in a capacitance to ground. However, a varactor can only look like a capacitance if it is reverse biased. These conflicting requirements mean that a slightly more complicated solution is required. Instead, placing two varactors in series and flipping the orientation of the second varactor allows them both to be biased and connects the resonator to ground. Adding the series capacitances produces a tuning range of 1.335 to 0.315pF.

With the length of the resonator calculated and the varactors chosen, the final step is to choose the width of the resonators. The resonator width, length of the resonators, center frequency, and capacitor value are all related by (3.9), where C_{var} is the tuned capacitance, Z_{res} is the characteristic impedance of the resonator, θ_0 is the electrical length of the resonator, and f_0 is the tuned center frequency. For a center frequency of 3 GHz, electrical length of 53°, and capacitance of 0.75pF, the characteristic impedance of the resonator should be 53.5Ω. Using the effective permittivity of the cavity, this corresponds to a width of 2mm.

$$C_{var} = \frac{1}{Z_{res}} \frac{cot(\theta_0)}{2\pi f_0} \tag{3.9}$$

With an individual resonator designed, the next step is to investigate what ge-

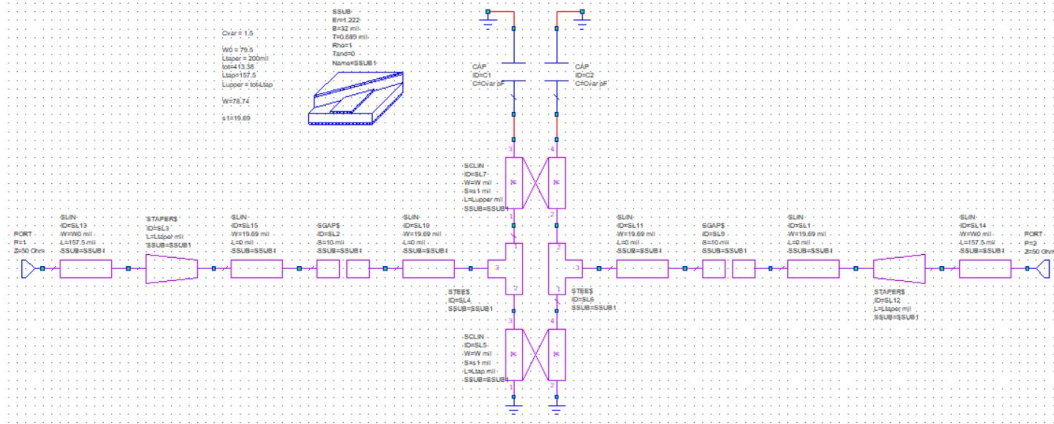


Figure 3.3: MWO schematic to extract inter-resonator coupling

ometries can achieve the desired inter-resonator and external couplings. Inter-resonator coupling can be controlled by adjusting the spacing between the two resonators. Figure 3.3 shows the MWO schematic used to determine the spacing that will produce the necessary inter-resonator coupling. This schematic consists of two resonators together with inputs and outputs. The resonators are weakly coupled due to the gaps in the input and output traces. The inter-resonator coupling is modeled by the coupled lines and can be adjusted by varying the spacing between them (s_1).

First, an arbitrary spacing between the coupled lines is chosen, and a simulation is run, producing a result similar to Figure 3.4. It is clear that S_{21} is weakly coupled, and there are also two discrete peaks. These peaks are located at the even and odd resonant frequencies, f_e and f_o respectively. Using (3.10), the inter-resonator coupling coefficient can be calculated.

$$k_{1,2} = \frac{f_e^2 - f_o^2}{f_e^2 + f_o^2} \tag{3.10}$$

By adjusting the spacing between the resonators, $k_{1,2}$ can be adjusted until it eventually matches the ideal value calculated before. For this work, MWO predicts

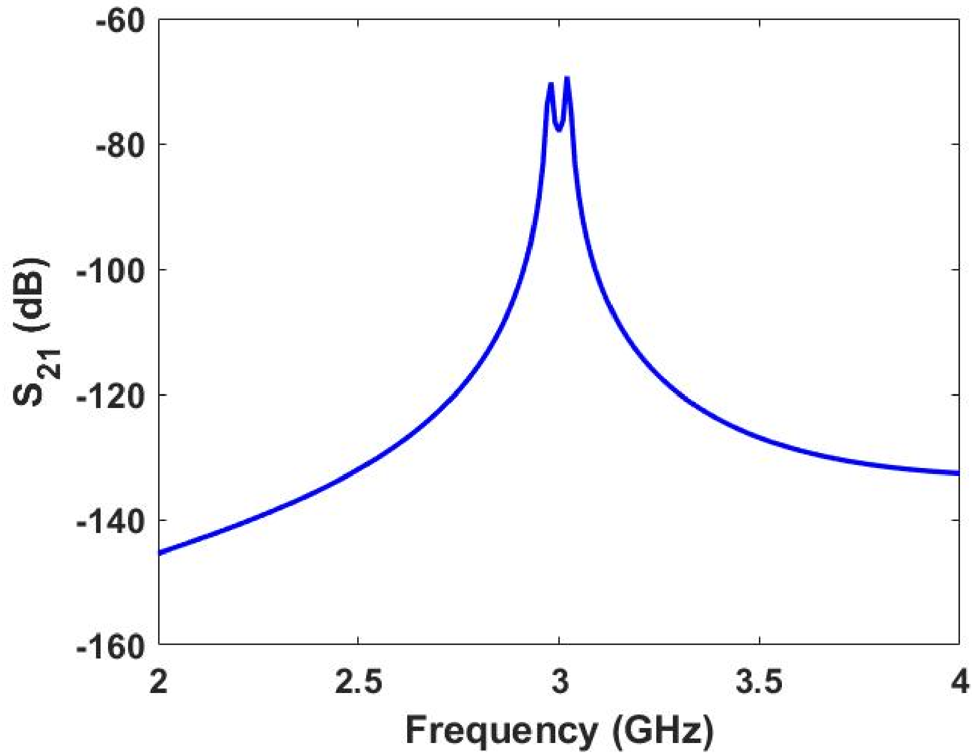


Figure 3.4: S_{21} of the MWO simulation to extract inter-resonator coupling

a spacing of approximately 0.25 mm will produce the necessary coupling at 3 GHz. The design to extract inter-resonator coupling is then implemented in HFSS, as shown in Figure 3.5. This design is essentially the same as implemented in MWO but placed within the SISL cavity of Chapter 2. The gaps in the input and output lines are 5 mil, providing the weak coupling necessary. A parametric sweep of the gap between the resonators is run from 0.2 to 0.6 mm, and $k_{1,2}$ is calculated for each of these. The resulting values are shown in Figure 3.6. The ideal value of 0.11785 occurs at approximately 0.35 mm, wider than MWO predicted.

Next, the external coupling mechanism is designed. There are two common ways to design the external coupling in a combline filter. The first is to run the input and output transmission lines parallel to the resonators, using the same coupling

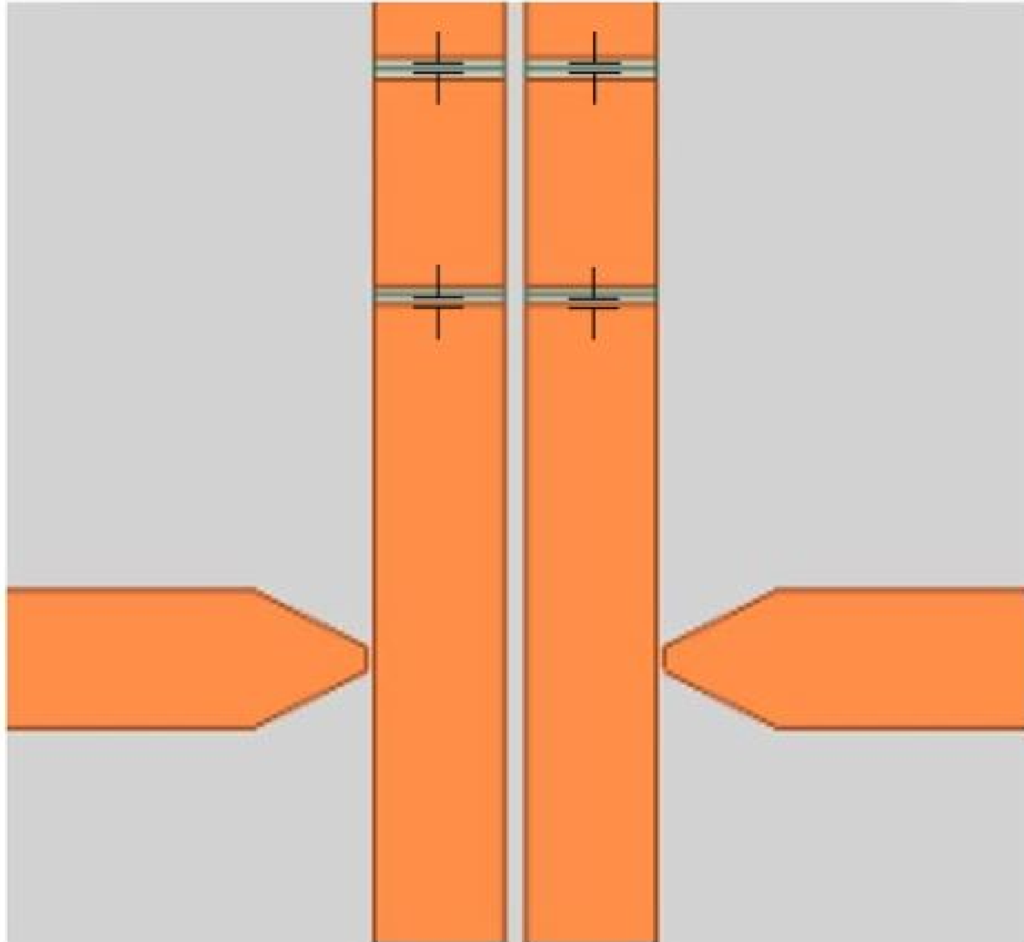


Figure 3.5: HFSS filter layer to extract $k_{1,2}$

mechanism as that between the resonators. The strength of the coupling is again controlled by varying the spacing between them. The second option is to use tapped coupling, an example of which is shown in Figure 3.7. In this scheme, the coupling is controlled by the location of the input and output traces on the resonators (the tap point).

To extract the external quality factor, only a single resonator is necessary, as shown in Figure 3.7. A simulation is then run, and the unfolded phase of S_{11} is plotted as shown in Figure 3.8. The tunable capacitor should be adjusted until 3

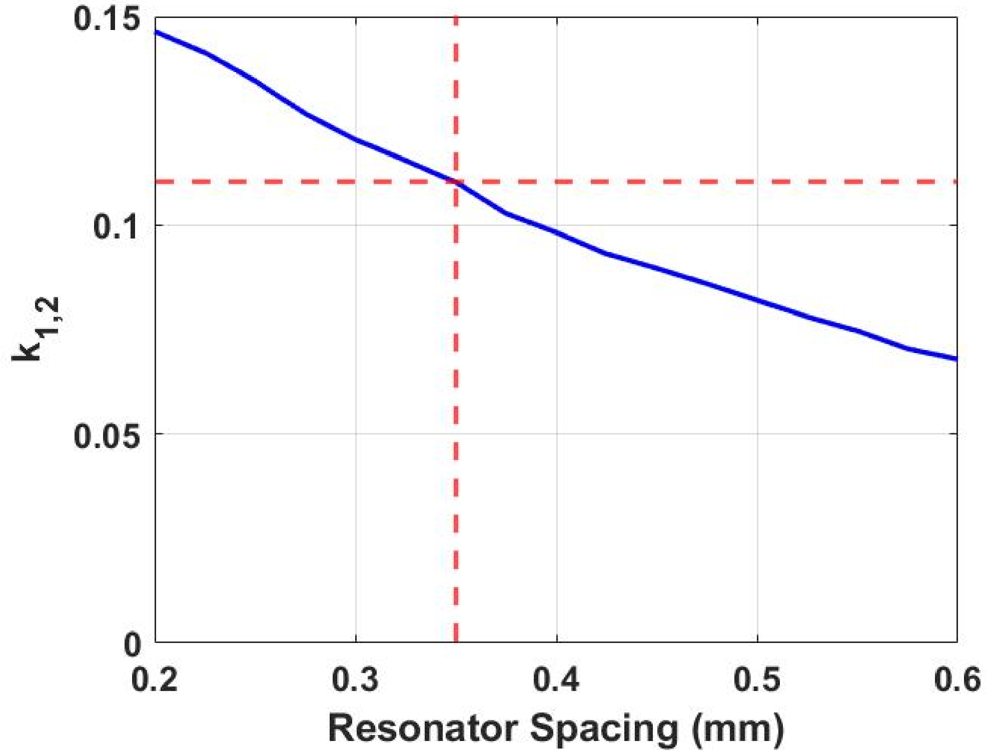


Figure 3.6: $k_{1,2}$ plotted against gap between resonators

GHz is roughly in the center of the unwrapped phase plot. Then, the frequencies $90°$ above and below the resonant frequency should be selected and denoted as f_a and f_b. Using (3.11), the external quality factor of the configuration can then be calculated. By adjusting the tap point, the simulated external quality factor can eventually be tuned to the ideal calculated before. MWO predicted a tap position of approximately 4.7 mm from the grounded end of the resonator.

$$Q_{ext} = \frac{f_0}{f_b - f_a} \tag{3.11}$$

The design to extract the external quality factor is then implemented in HFSS as shown in Figure 3.9. It remains nearly identical to the MWO schematic but is placed within the SISL air cavity on Substrate 3. The position of the tap is swept from 3

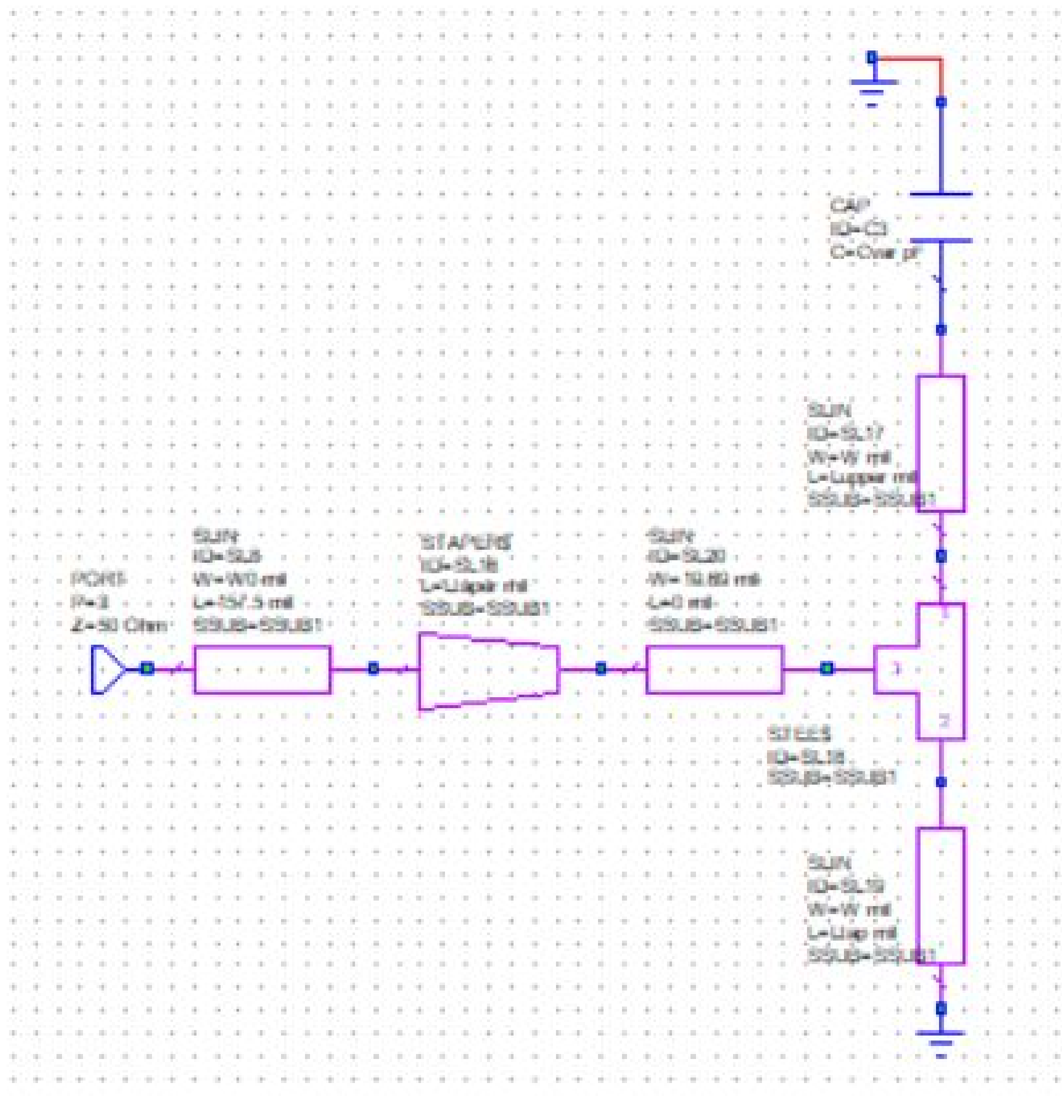


Figure 3.7: MWO schematic to extract external quality factor

to 6 mm (12° to 24° electrical length) and the external quality factor is calculated. A tap position of 4.5 mm (18°) produces the external quality factor calculated by (3.5).

Figure 3.10 illustrates the relationship between Q_{ext} and the tap position's electrical length from ground for a resonator at 3 GHz. A large external quality factor (weak external coupling) can be achieved by placing the tap point closer to ground, while stronger external coupling can be achieved by placing the tap point further up

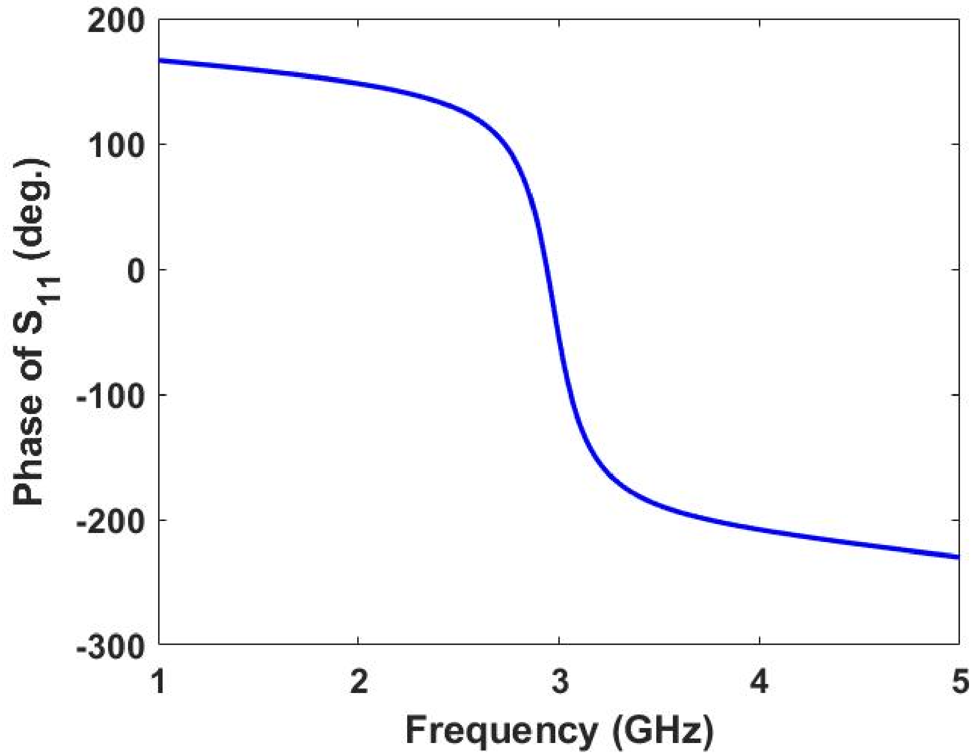


Figure 3.8: Unfolded phase of S_{11} of the MWO simulation to extract external quality factor

the resonator. The coupling can only be made so strong because the tap point will eventually reach the end of the resonator. For this structure, the smallest Q_{ext} theoretically possible is 2.11. This corresponds to a fractional bandwidth of 0.67, which is extremely wide band. For a filter with a center frequency of 3 GHz, this corresponds to a bandwidth of just over 2 GHz. While this does present a fundamental limitation on tapped coupling in combline filters, it is a large enough bandwidth it should very rarely be relevant.

One limitation in designing a filter with tunable center frequency is that the couplings are only equal to the ideal for a single tuned center frequency. At other frequencies, they will only be able to approximate the desired couplings, leading to increasing degradation in the response as the center frequency is tuned further

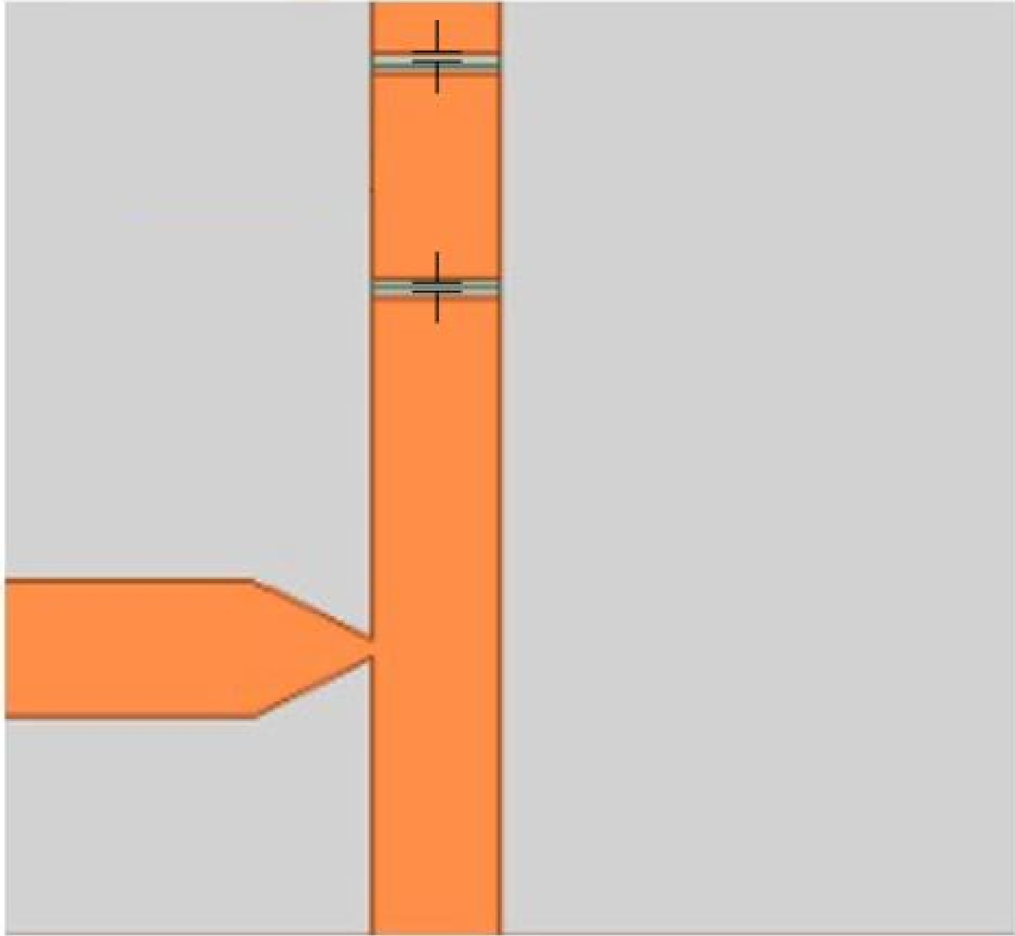


Figure 3.9: HFSS layout to extract Q_{ext}

from 3 GHz. Figure 3.11 presents a comparison of the simulated $k_{1,2}$ and Q_{ext} and the ideal values that would maintain the filter response as center frequency is tuned. It can be seen that the simulated $k_{1,2}$ follows the trend of the ideal $k_{1,2}$, so variations in the bandwidth will not be large. However, Q_{ext} decreases as the center frequency is increased, giving the opposite behavior desired. This means the ideal filter shape will be maintained only over a very narrow range of center frequencies where the ideal values are approximated. Away from those frequencies, the filter will no longer have a well matched Butterworth response.

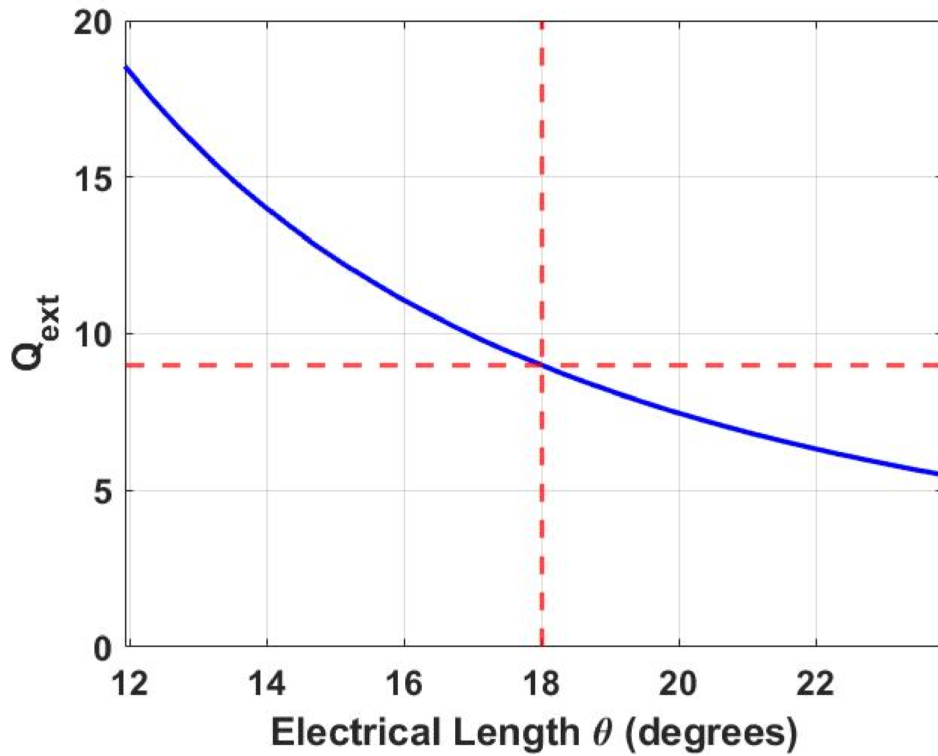


Figure 3.10: Tap position compared to external quality factor at 3 GHz

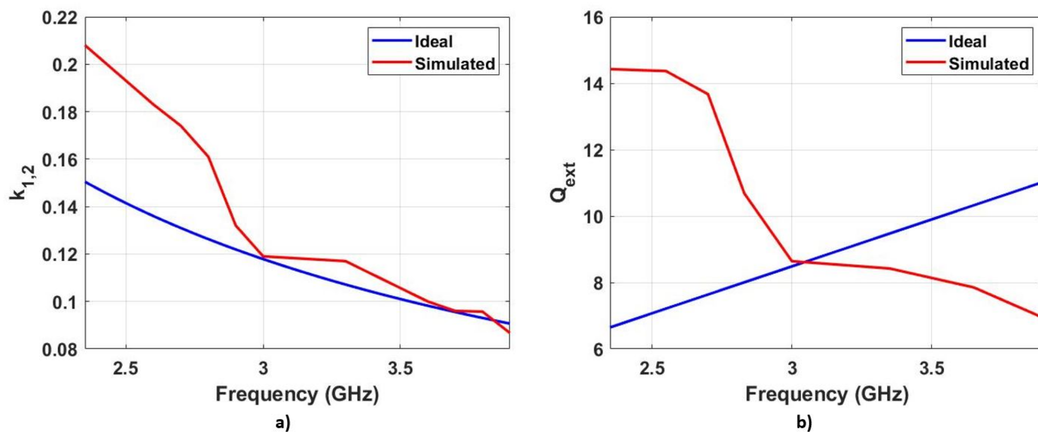


Figure 3.11: Comparison of ideal and simulated $k_{1,2}$ and Q_{ext}

3.2 SMT SISL Filter Design

With the internal and external couplings tuned using both MWO and HFSS, the full filter can be designed and simulated. Figure 3.12 shows the design that is

ultimately created. The important dimensions are $L_1 = 10$ mm, $L_2 = 1.9$ mm, $L_3 = 4.375$ mm, and $S = 0.35$ mm. The tap point is at 4.5 mm as calculated before, but L_3 only measures to the lower edge of the tap. In addition, the varactors and RF chokes have been included in the model, together with a biasing scheme.

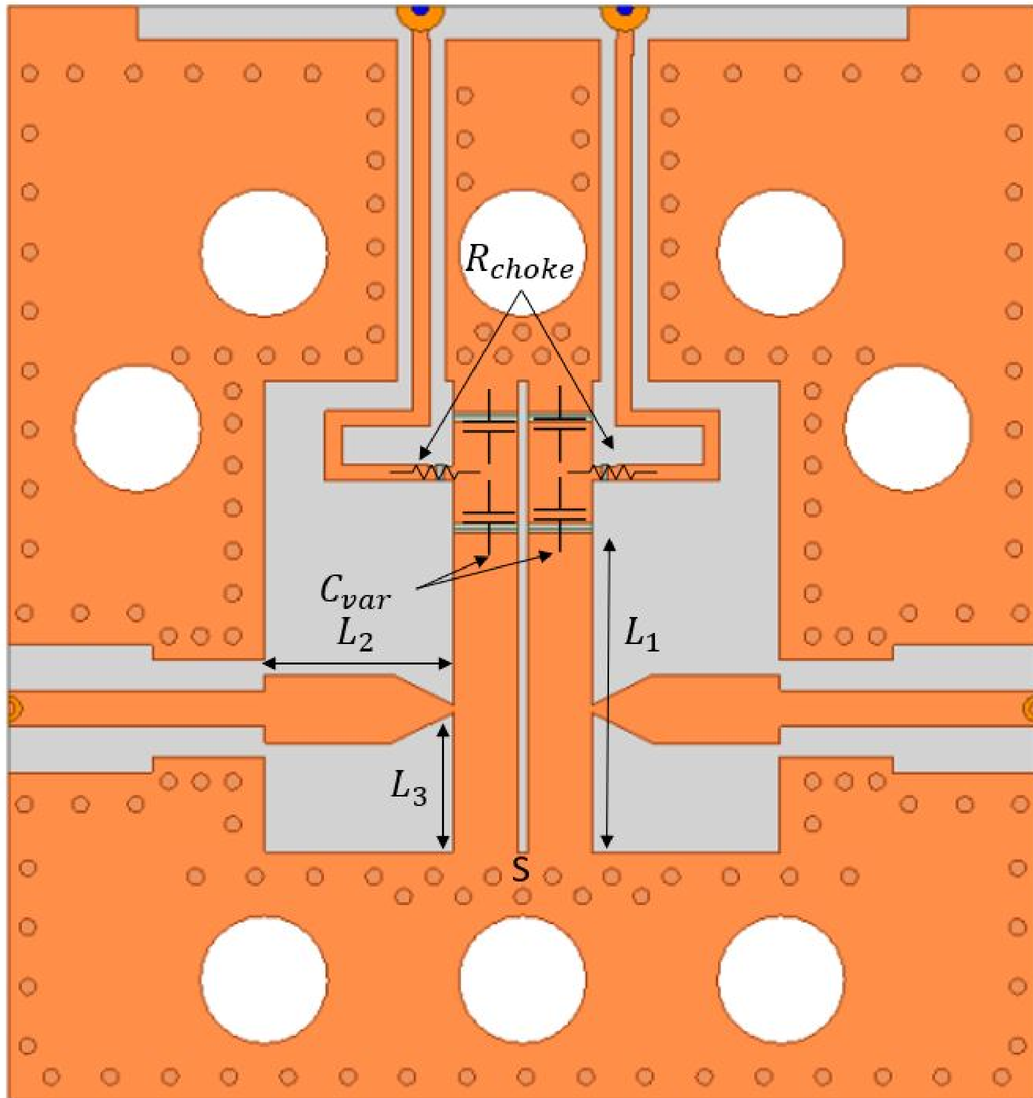


Figure 3.12: Tunable combline filter in the middle layer (M5)

3.2.1 Varactor Layout and Modeling

The varactors are no longer modeled as ideal capacitors since they have resistance of 0.8Ω according to the data sheet. Ignoring packaging effects, the varactors are modeled as RLC boundary conditions in HFSS, consisting of a variable for the capacitance in series with the resistance from the data sheet. By changing the capacitance variable, the filter can be tuned to different frequencies. For the purpose of simulating the filter's tuning, ten different capacitances ranging from 0.63 pF to 2.67 pF are chosen and implemented as a parametric sweep of the capacitance boundary condition.

3.2.2 Biasing Scheme

There are two sets of bias lines, one for each resonator. Ideally, only a single bias would be necessary to tune the resonators, but manufacturing tolerances lead to slight variations in the capacitance of the varactors. Further, solder can add slightly more capacitance to one of the two resonators. Therefore, it is important to be able to tune each resonator separately and compensate for any variations in their resonant frequency.

Figure 3.13 shows the biasing scheme of the carrier board. There are four bias lines (two per power supply) and two castellated vias. The outermost bias lines feed into the top copper of the carrier board. This forms the lower ground plane of the structure and is connected to the other grounds by plated vias. To make the design fully surface mountable, the middle bias lines must access the middle layer through castellated vias. However, the dimensions are not constrained as in the signal via design because only DC signals should be on these vias. Therefore, arbitrary dimensions are chosen. For this work, the vias are 0.5 mm in diameter, the

pads are 1.5 mm in diameter, and the vias are 30 mil long. Copper around the via pads is removed to ease fabrication and ensure there is no risk of a short.

On the filter layer (M5), the castellated vias transition to the final DC bias lines. Again, these lines can be any width because they should only carry a DC signal. However, they should not be too wide because the cutout around them will also get very wide. If the cutout becomes too wide, the via wall around the SISL cavity will be compromised and potentially allow some of the RF signal to leak into other parts of the stack-up. Therefore, the line is made 0.5 mm wide with a gap of 0.5 mm on either side. In addition, wall vias are added that run the length of the bias lines to ensure no RF signals can leak into the side grounds through the bias lines' cutout.

The final consideration in the scheme is making sure that RF signals do not go back to the DC power supplies used for tuning, and that DC signals do not get into the VNA used for measuring the filter. A simple solution to protect the power supplies from DC is to add an RF choke, as shown in Figure 3.12. These resistors are selected to have a very high impedance ($470\text{k}\Omega$) to attenuate RF signals while still allowing a DC bias on the varactors. They are modeled as an RLC boundary

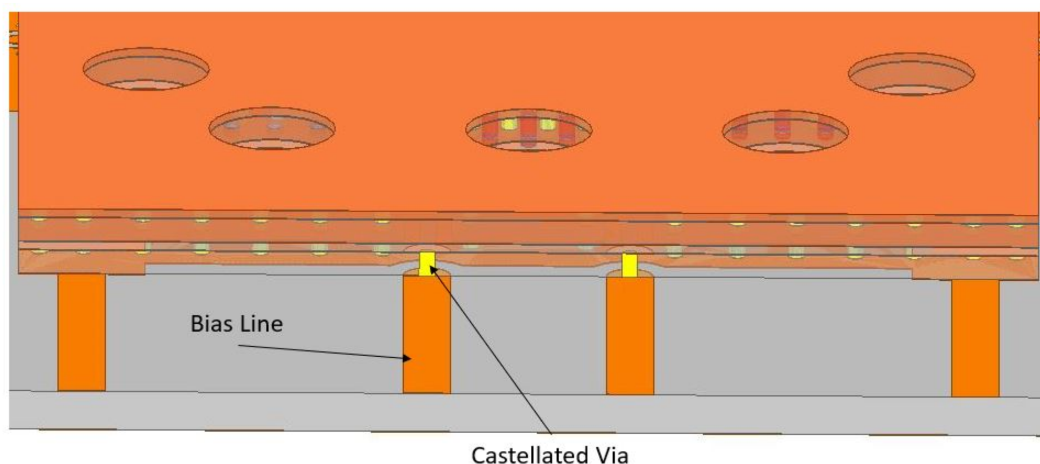


Figure 3.13: HFSS model illustrating the castellated bias vias

in HFSS. Alternatively, a choke inductor could be used to the same effect by taking advantage of inductors' LPF behavior. However, inductors are not practical for this design because they must provide a large enough impedance at S-band. Large inductors will have a self-resonance within or lower than S-band, meaning they will act like a capacitor at the filter's frequency of operation and potentially allow RF signals through. Therefore, a resistor is the only option to provide a large choke impedance at higher frequencies. In order to protect the VNA from DC signals, DC block capacitors are necessary. These work opposite of RF chokes, presenting a very high impedance at low frequencies, and a negligible impedance at high frequencies. Discrete capacitors can be added in series with the input and output transmission lines in order to protect the VNA, or SMA DC blocks can be connected to the edge-launch connectors. For this work, the SMA blocks are used because they are easier to connect and are foolproof. The only change is that they must be included in the VNA's calibration to ensure accurate filter measurements.

3.3 SMT SISL Filter Simulations

Now that the full filter has been designed, including the biasing scheme, it is integrated into the full SISL stack-up of Chapter 2. The thru-line is removed and replaced by the filter layer. The old carrier board, castellated via transitions, and strip-line sections seamlessly integrate with the new filter structure. The only addition is two castellated vias to connect the bias lines on the filter layer to the carrier board. The design is then simulated from 1 to 7 GHz with the varactors tuned to 1.5 pF, resulting in Figure 3.14. It can be seen that the filter response is centered at 3 GHz with a return loss better than 20 dB. Further, the insertion loss is approximately 2.11 dB at 3 GHz, and the bandwidth is approximately 500 MHz as desired.

The full thru-line simulation had an insertion loss of approximately 0.2 dB, so the varactor diodes introduce approximately 1.9 dB of additional loss.

With the design confirmed for a single frequency, a parametric sweep is run to demonstrate center frequency tuning. The results are shown in Figure 3.15 while Table 3.1 provides a summary of the important characteristics. The filter's center frequency is tunable from 2.3 to 3.9 GHz with performance worsening as the center frequency is tuned away from 3 GHz. The filter could be tuned above 4 GHz, but the performance was very poor. This fits the expectations of the design and demonstrates an SMT-able filter is feasible.

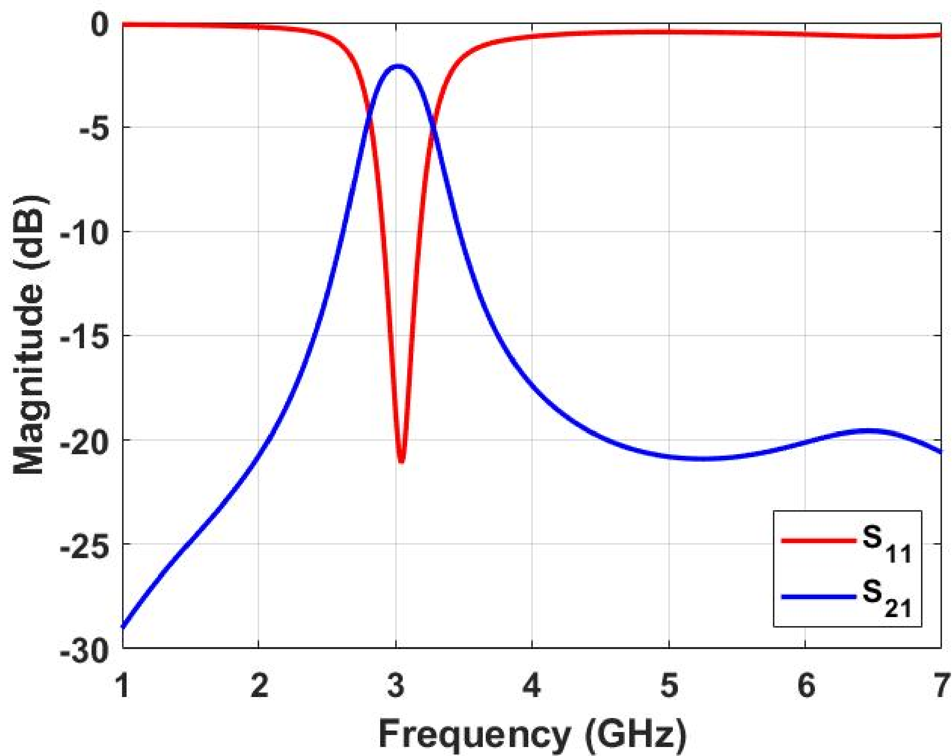


Figure 3.14: Simulated S-parameters of the full SMT SISL filter tuned to 3 GHz

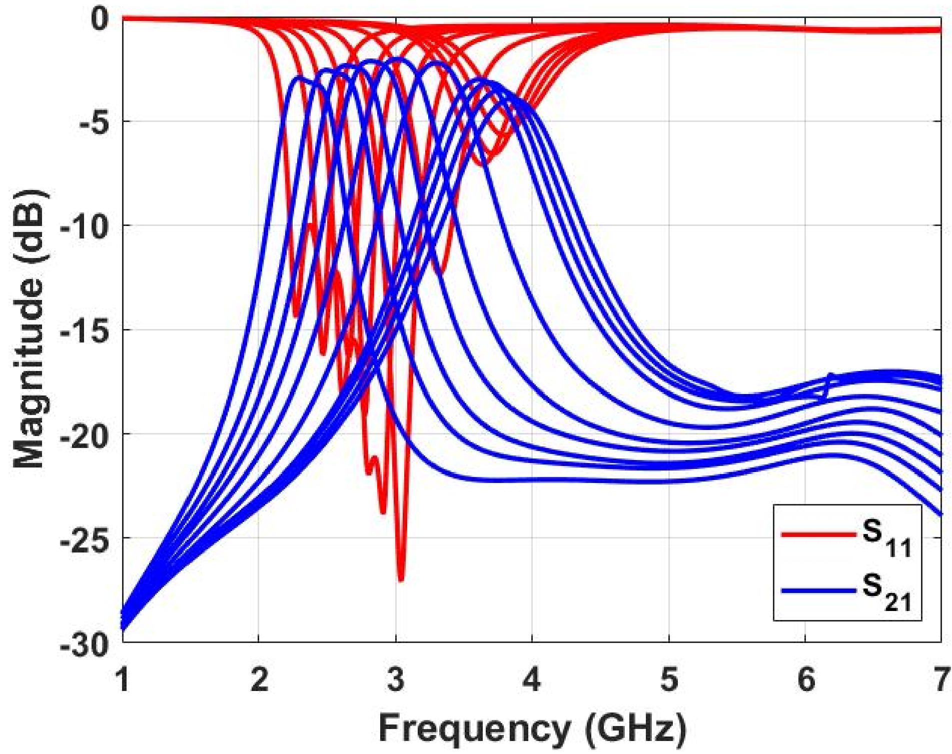


Figure 3.15: Simulated S-parameters of the full SMT SISL filter demonstrating tuning range

C_{var} (pF)	f_0 (GHz)	BW (GHz)	IL (dB)
0.8	3.9	0.685	4.09
0.85	3.8	0.680	3.77
0.9	3.7	0.655	3.71
0.95	3.6	0.63	3.21
1.2	3.3	0.545	2.45
1.5	3.0	0.495	2.11
1.75	2.8	0.475	2.15
2.0	2.7	0.46	2.36
2.25	2.6	0.445	2.59
2.67	2.4	0.42	2.98

Table 3.1: Simulated filter characteristics for tuned varactor capacitances

3.3.1 Leakage and Wall Vias

Initial simulation of the design achieved a good filter response, but the stop band did not roll-off as expected at higher frequencies. Instead, it decreased to roughly

$S_{21} = -20$ dB and stayed there. This seems to indicate that a signal is leaking through the structure and reaching the output without passing through the filter. With a multi-layer stack-up, there are plenty of possible avenues for leakage, and HFSS is used to eliminate each possibility.

Radiation from the input trace reaching the output trace is the first possible source of leakage investigated. By placing a perfect electric conductor (PEC) cap over the entire top of the stack-up, the input and output are effectively isolated except through the SISL structure. Simulation found the leakage was not reduced, indicating radiation was not the source. This then means the leakage must be somewhere within the structure.

The next possible sources of leakage are Substrates 1 or 5. Theoretically, a signal can leak into it at one end and propagate to the other end because the top and bottom copper acts as parallel plates. This is tested by replacing a strip of PEC across the substrates, effectively dividing them in half. If a signal is propagating through the parallel plates, it will encounter the PEC wall and be prevented from reaching the other end of the substrate. Simulation confirmed this had no effect, eliminating Substrates 1 and 5 as possible sources of error.

This then leaves Substrates 2-4 as possible paths for leakage. These layers are investigated by running a simulation at 6.5 GHz (within the leakage) and investigating the current densities throughout the structure. The objective is to find strong current densities outside the SISL cavity, indicating there is a path through the larger structure. If any paths are found, they can then be removed through the use of plated vias.

Figure 3.16 presents the five groups of plated vias ultimately used in this structure. All of these vias extend through Substrates 2-4, but are only shown on Substrate 3 to illustrate their positioning relative to the filter. Group 1, the strip-line

wall vias, were designed in 2.1.3 to suppress any parallel plate modes within the strip-line section and remain unchanged in the filter design. Similarly, Group 2, the cavity wall vias, were designed in 2.2 to isolate the cavity from the rest of the structure. The remainder of the vias are added due to the investigation of leakage.

An obvious path of potential leakage is through the cutouts required by the biasing lines. A simple check is to run a simulation wherein the bias lines have been made non-model objects, confirming RF signals are not propagating on them. However, Group 3 is added to be entirely sure no signals are leaking through the cutouts. Plated vias are run along both sides of the bias lines to isolate the side grounds from the cavity and cutouts. These 0.5 mm diameter vias are spaced such that they appear like a solid metal wall up to 10 GHz, ensuring there will be no leakage into the structure at the frequency band of operation.

Simulating the current density on the resonators found significant concentra-

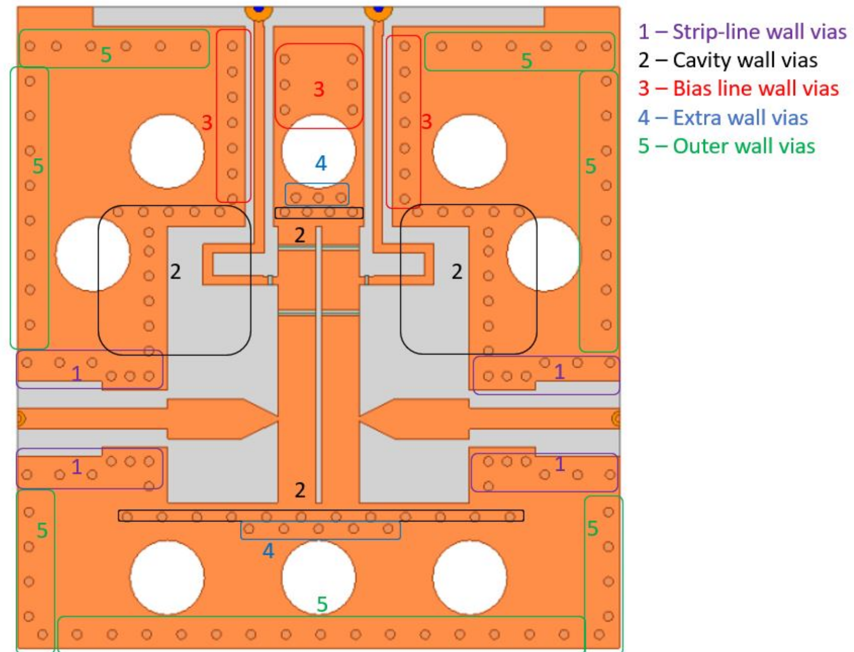


Figure 3.16: Grouped wall vias used in the design

tions at the ends of the resonators that were also leaking through the cavity wall vias. Group 4 serves as a second row of vias at both ends of the resonators to act as a second layer in the ‘fencing’. They are offset from the first row of vias and positioned between them such that the current densities are contained and shunted to ground rather than escaping into the structure.

A final obvious possibility is radiated fields coupling into the side grounds and propagating through them to the output. This is counteracted by Group 5, a series of vias around the entire perimeter of the structure. These again act as a metal wall, preventing any external signals getting into the side grounds. This is a fairly common feature in complicated board designs because there are often concerns about external radiation coupling into the structure. Ultimately, none of these vias solved the leakage issue, but they provided slight improvement in performance and are best practice to ensure the design is electromagnetically isolated. Although the leakage could not be isolated to a specific portion of the structure, a similar behavior was observed in MWO simulations which do not account for the larger structure of the stack-up, so it appears the leakage is inherent to the filter itself.

With the tunable filter designed and simulated, the next step is to fabricate both it and the thru-line of Chapter 2. These fabrications follow the same procedure since both designs take advantage of the same structure. Once fabricated, measurements must be taken to confirm the HFSS simulations fully capture the performance of the designs.

Chapter 4

Fabrication and Measured Results

This chapter details the fabrication and measured results for the SISL thru-line of Chapter 2 and the tunable filter of Chapter 3. The measured results are also analyzed to illustrate the effectiveness of the surface mounting technique.

4.1 Fabrication

This section provides an overview of the steps to fabricate both the SISL thru-line and tunable filter. An in-house photolithography procedure was used to etch Substrate 3 because the material is so thin, while an ProtoMat S104 was used to mill the remaining layers. LPKF ProConduct was used to metallize all of the wall vias, while an in-house copper electroless plating and electroplating procedure was used to plate all of the vias in Substrate 2, including the castellated signal and bias vias. Initially, these vias were plated using the same ProConduct procedure, but the castellated vias did not prove durable enough over time. The castellated cut and bolt holes were cut by the S104, and the full package was bolted together using machine screws and nuts. Appendix A has a step-by-step fabrication procedure, but the basic steps are summarized below. The following procedure is used to fabricate Substrates 1, 3, 4, and 5.

1. Mill Board Design
2. ProConduct Process
3. Cut Out Board Design
4. Assemble Layers

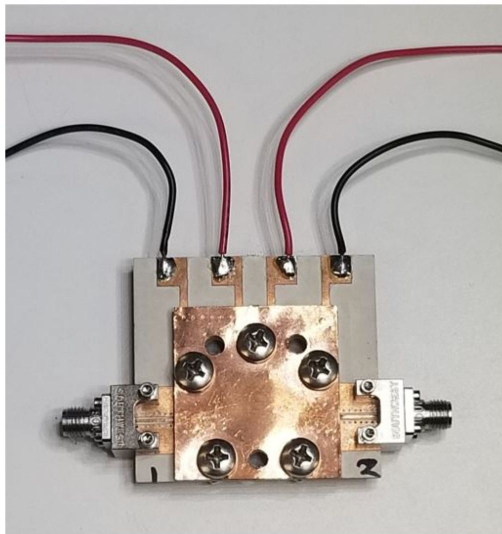
For Substrate 2, an electroplating procedure was used, necessitating a different fabrication procedure.

1. Drill Vias
2. Electroless Plating Process
3. Electroplating Process
4. Mill Board Design
5. Cut Out Board Design

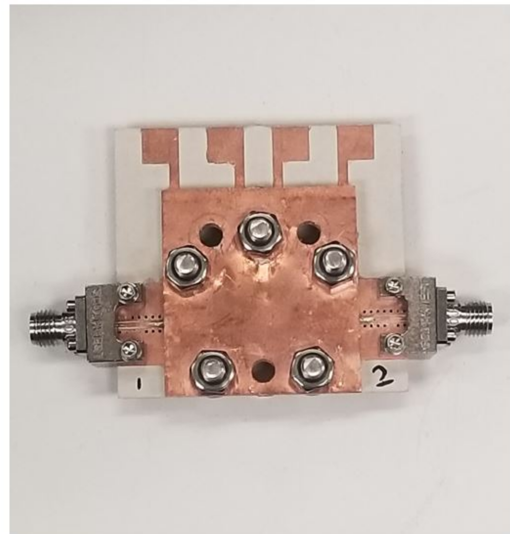
Both the thru-line and tunable filter were manufactured following these steps. Figure 4.1 shows both designs fully assembled while Figure 4.2 shows the individual layers. The stack-up is identical except for the design on Substrate 3, so the thru-line and filter can easily be tested by replacing one with the other.

4.2 Thru-line Results

The SMT SISL thru-line was measured first to determine the effectiveness of the castellated vias as well as their associated losses. An Agilent Technologies N5225A PNA calibrated using an Agilent N4691-60006 electronic calibration module was used for this measurement. The simulated and measured S-parameters are shown in



a) Tunable Filter



b) Thru-line

Figure 4.1: Fabricated filter (a) and thru-line (b)

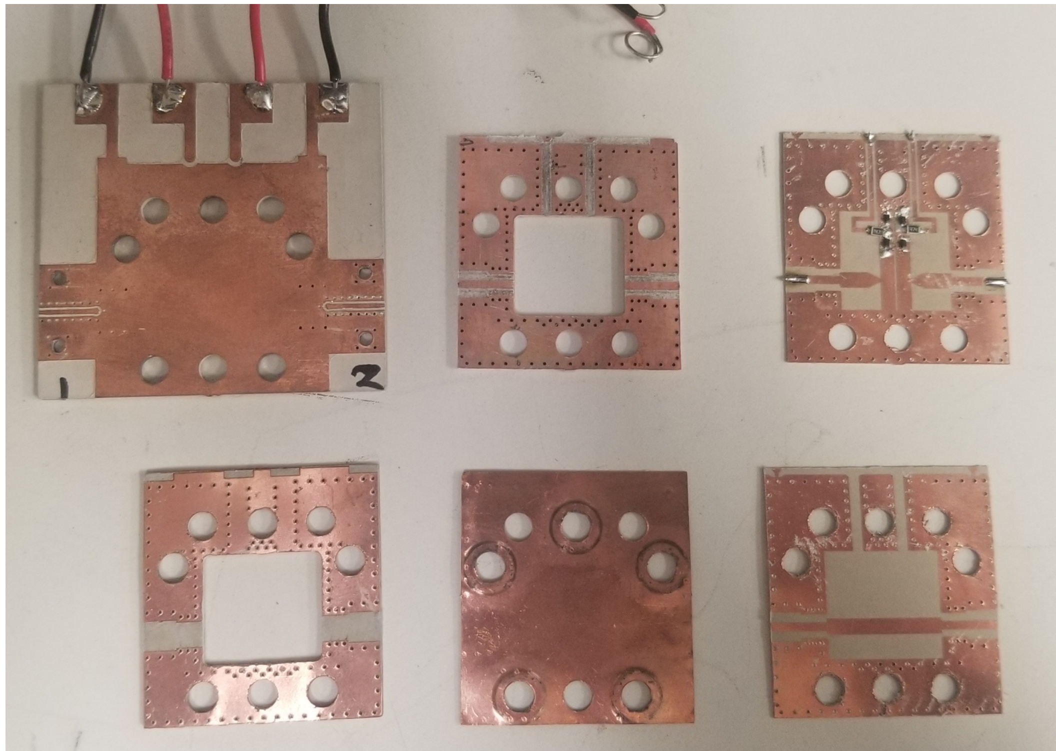


Figure 4.2: Individual stack-up layers: Substrate 1 (top left), Substrate 2 (top middle), Filter (top right), Thru-line (bottom right), Substrate 5 (bottom middle), Substrate 4 (bottom left)

Figure 4.3. There is generally good agreement with the simulated design, and the return loss is better than 25 dB across the entirety of S-band while the insertion loss is better than 0.86 dB.

Focusing on S-band, the thru-line closely follows the expected response. However, Figure 4.4 shows only simulated and measured S_{21} to allow closer inspection. There is good alignment from 2 to 3 GHz, but there is a clear dip in S_{21} at 3.5 GHz that distorts the measured response. Ignoring this non-ideal effect for the moment, the measured insertion loss ranges from 0.32 dB at 2 GHz to 0.55 dB at 4 GHz while the simulated values are 0.147 dB and 0.262 dB respectively. Taking the ratio between the measured and simulated insertion loss produces 2.18 at 2 GHz and 2.10 at 4 GHz. This indicates that within the band of interest the measured insertion loss

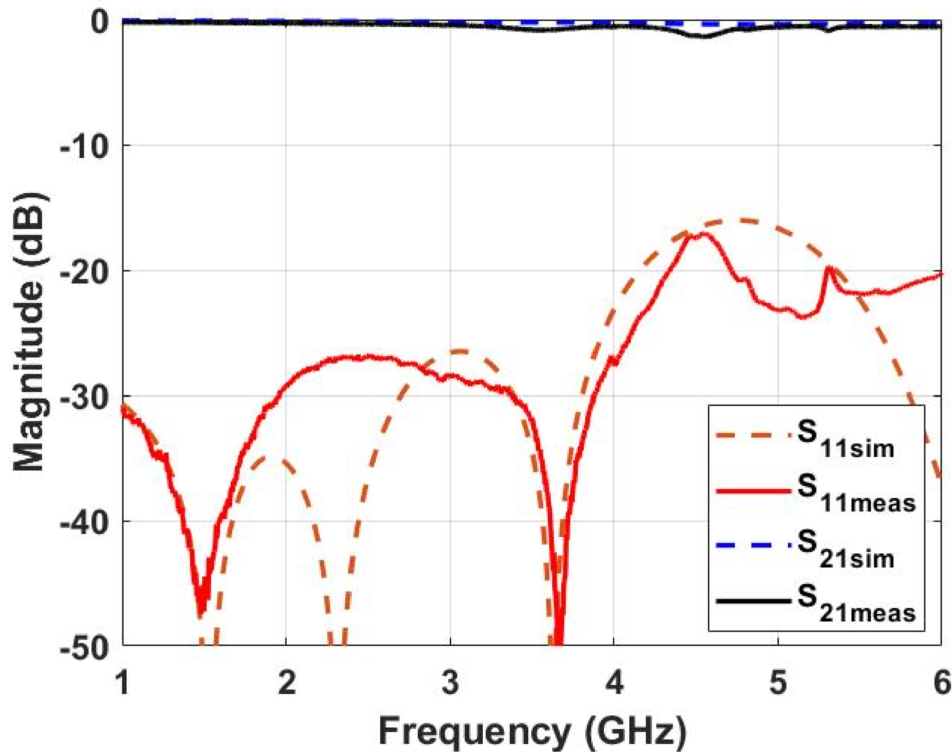


Figure 4.3: Simulated and measured S-parameters of the SMT thru-line

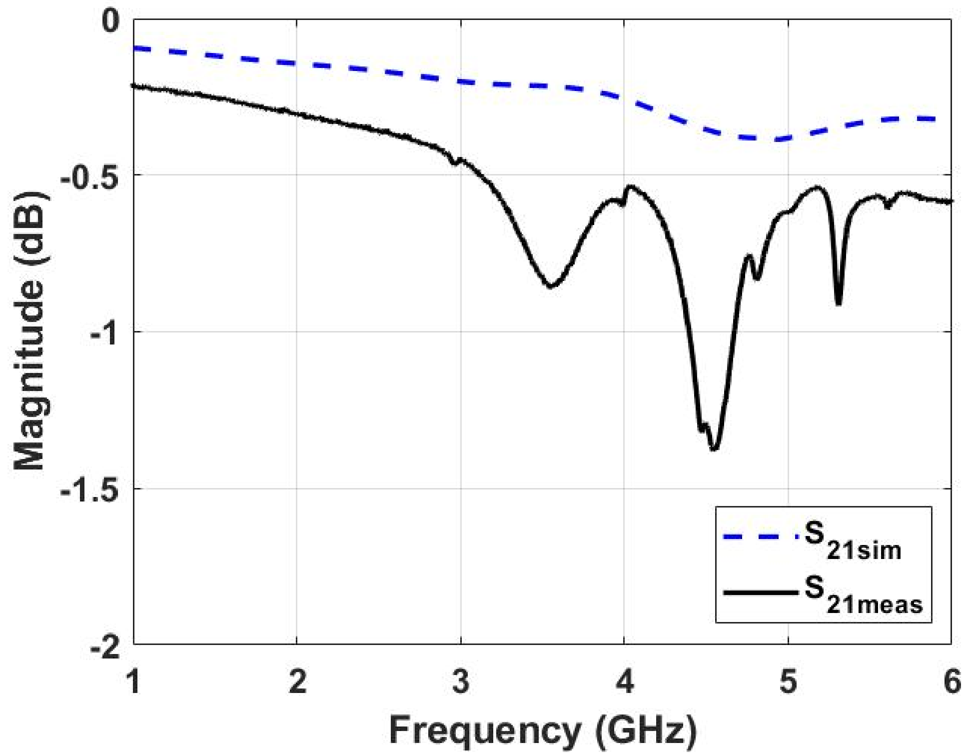


Figure 4.4: Zoomed-in comparison of simulated and measured S_{21}

is following the same general trend but with increased loss. This additional loss can be attributed to the non-ideal conductivity of copper, possible dielectric losses, and slight mismatches introduced by imperfect alignment and fabrication of the layers. The connectors were included in simulation, so they should not contribute to this loss.

The dip in S_{21} has a maximum insertion loss of 0.86 dB, while simulation predicts a loss of 0.21 dB. Looking at S_{11} is not enough to explain the dip, but S_{22} provides significant insight. Figure 4.5 shows S_{22} together with the measurements presented before. At lower frequencies, S_{22} does not align with either the simulated or measured S_{11} and can account for some of the increased insertion loss measured. Most significantly, there is a clear minimum in S_{11} at 3.5 GHz, but there is a local

maximum in S_{22} at that same frequency. This decreased match aligns with the dip in S_{21} which indicates it is a likely culprit for the extra loss. This could be a weak resonance within the structure, and there are much clearer resonances around 4.5 and 5 GHz.

A measurement up to 15 GHz was taken, shown in Figure 4.6, to investigate further non-ideal effects in the fabricated design. First, it should be noted that S_{11} and S_{22} agree very well past 6 GHz, so only S_{11} is necessary to analyze the system. In the simulated design, there is a clear resonance at 11.75 GHz, and the insertion loss is beginning to roll off significantly. This roll-off could indicate the LPF behavior of the via transition is coming into effect. However, in measurement this roll-off seems to follow the same trend as the simulation, which indicates the cutoff

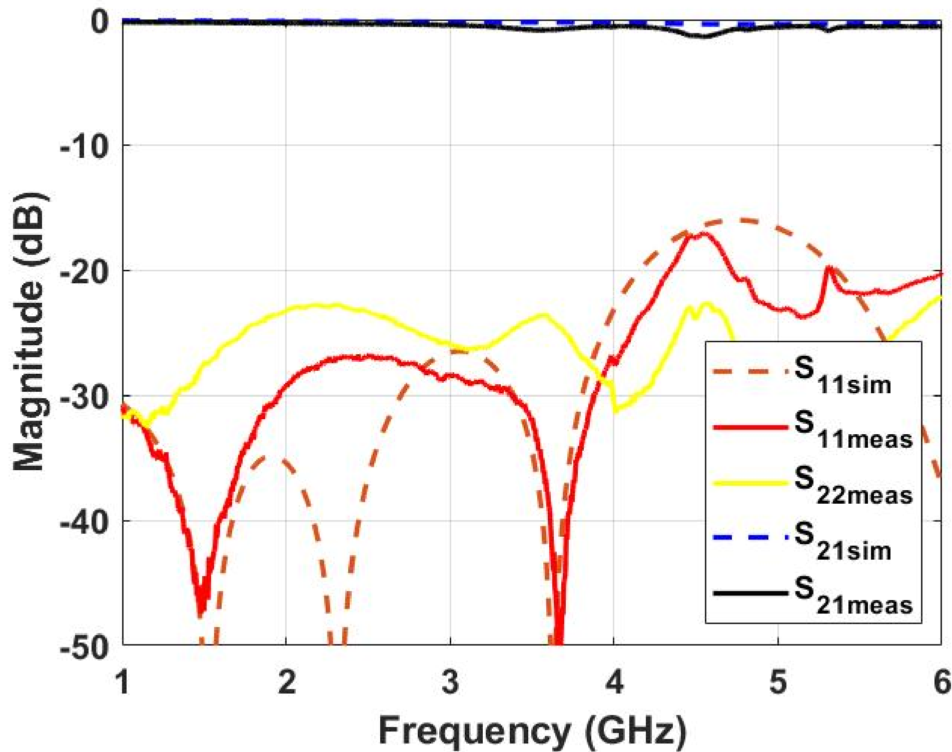


Figure 4.5: Measured and simulated S-parameters of the thru-line including S_{22}

frequency of the via transition has not been shifted lower in frequency. This indicates there is very little extra inductance or extra capacitance in the via transition, which means the solder used to connect the carrier board to the via transition is not having a significant effect. However, most of the degradation in the high frequency response can likely be attributed to the cavity beginning to allow wave guide modes to propagate. The cutoff should be around 8.4 GHz, so most of the degradation in the high frequency response can likely be attributed to mode-splitting. Further, the cavity should resonate around 11.23 GHz according to calculations, and the simulation predicts a resonance at roughly 11.8 GHz. This is also a source of degradation in the response. If the via transition's LPF cutoff frequency has been shifted lower than simulated, it is only minor. Instead, almost all of the degradation at high frequencies can be attributed to wave guide modes within the cavity.

4.3 Tunable Filter Results

The SMT SISL tunable filter was measured using the same Agilent Technologies N5225A PNA. In this case, MCL 15542 DC blocks on the input and output were included in the calibration. The resonators of the BPF are tuned separately using two DC power supplies, eliminating any asymmetries in them due to inconsistencies in the varactors. A comparison of the simulated and measured S-parameters is shown in Figure 4.7.

The measured filter is tunable from 2.4 to 3.9 GHz with a return loss of better than 10 dB and can be tuned down to 2.3 GHz with a return loss better than 8.5 dB. Insertion loss ranges from 2.54 to 4.7 dB within the filter's tuned passbands. The simulated response varied from 2 to 3.5 dB, and the losses are dominated by the varactor diodes. Figure 4.8 shows the insertion loss compared to the center frequency.

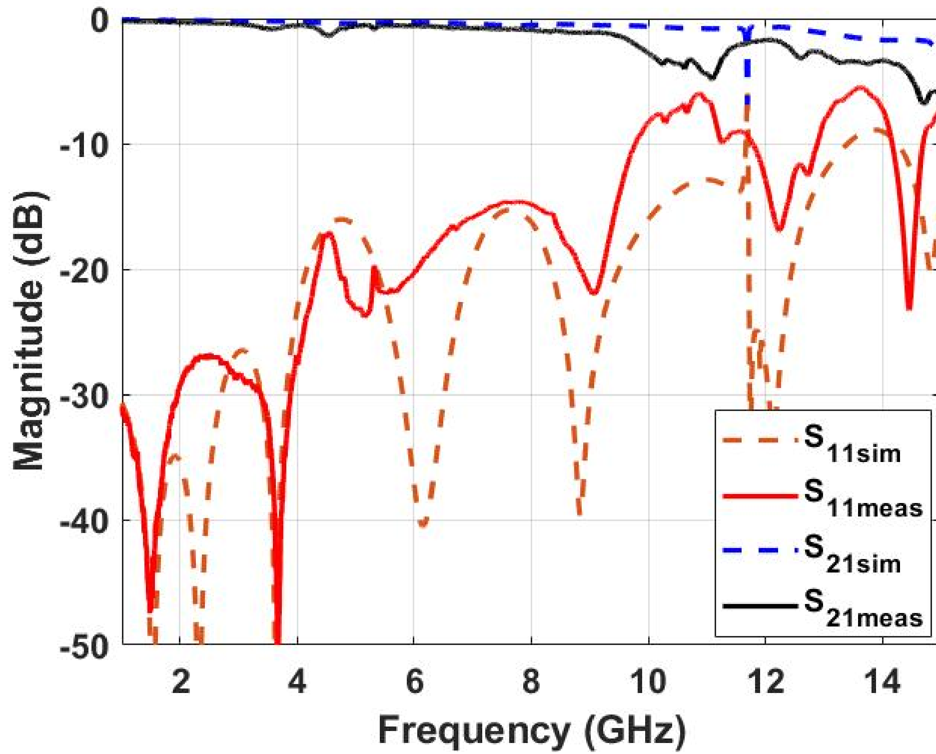


Figure 4.6: Measured and simulated S-parameters of the thru-line up to 15 GHz

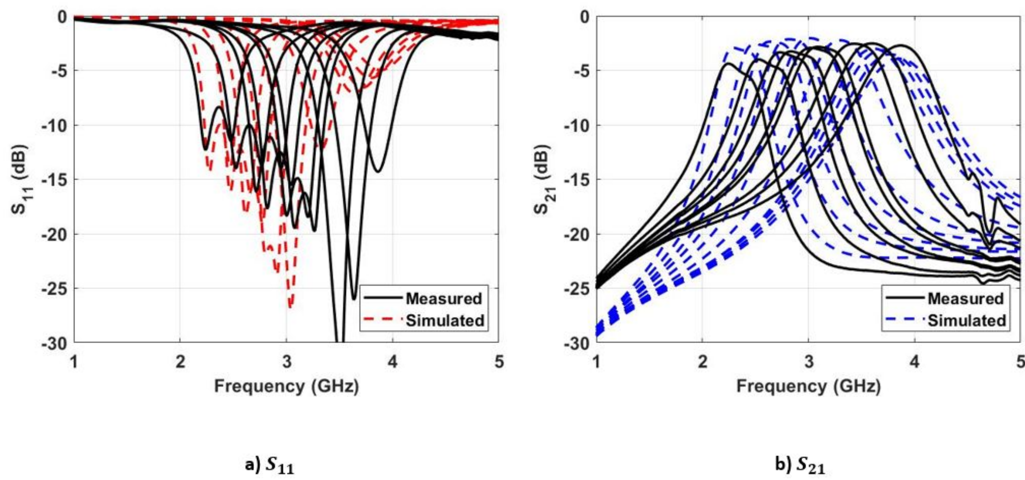


Figure 4.7: Comparison of the simulated and measured S-parameters

The measured insertion loss is generally worse than the simulated, but it does not follow the trend simulation predicted. This is likely due to the simulated and mea-

sured filter responses not aligning perfectly. The best measured filter response was at approximately 3.5 GHz which is also near the best measured insertion loss while the best simulated filter response is at 3 GHz which is also near the best insertion loss simulated.

Although the measured filter response is not identical to the simulated, the differences between them can be attributed to variations in the manufacturing process. Most significantly, the photolithography procedure used to fabricate the filter layer did not etch enough copper. This altered the critical dimensions of the filter, shown in Figure 4.9 and Figure 4.10. The gap between the lines should be 0.35 mm but is only 0.3mm, which will strengthen the inter-resonator coupling. The resonators are approximately 0.22 mm wider than desired which weakens the external coupling,

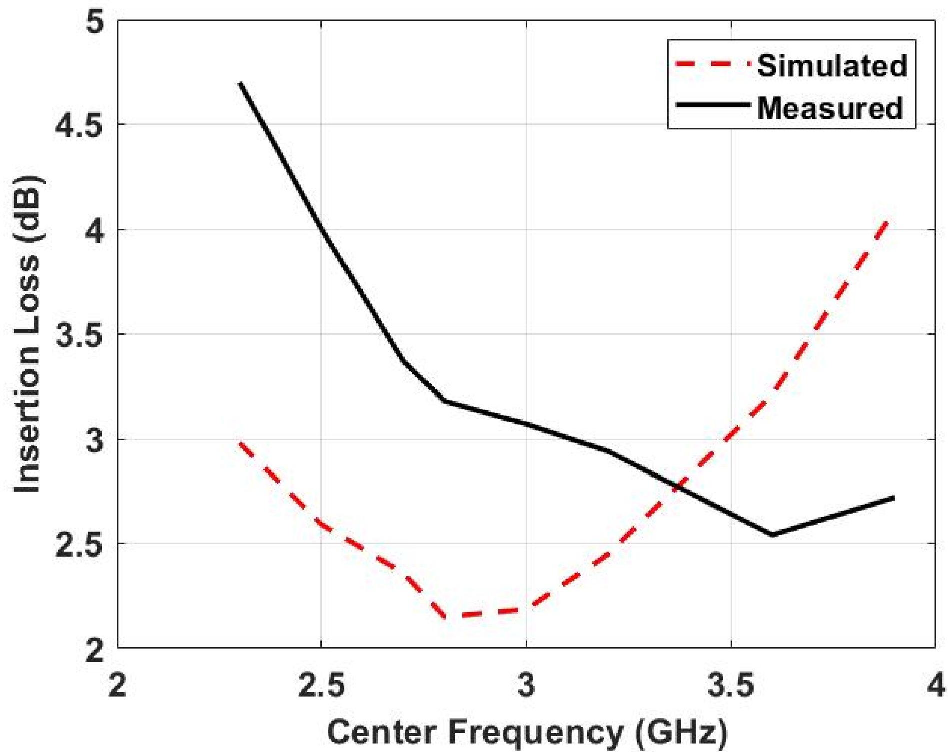


Figure 4.8: Measured and simulated insertion loss of the filter as a function of the center frequency

while the tap point is approximately 0.25 mm wider than desired, strengthening the external coupling slightly. Finally, the length of the taper is 0.07 mm shorter than desired, weakening the external coupling. The net effect is to have stronger inter-resonator coupling and weaker external coupling.

The strengthened internal coupling indicates the measured filter should have a wider bandwidth than the simulated design. A comparison of the simulated and measured bandwidths is presented in Figure 4.11. The measured bandwidths are larger than those simulated up to 3.3 GHz. This discrepancy can likely be attributed to how bandwidth is measured. For this design, bandwidth is defined as 3 dB below the smallest insertion loss at the center frequency. The simulated design had significantly higher insertion loss than measured at frequencies above 3.3 GHz. This

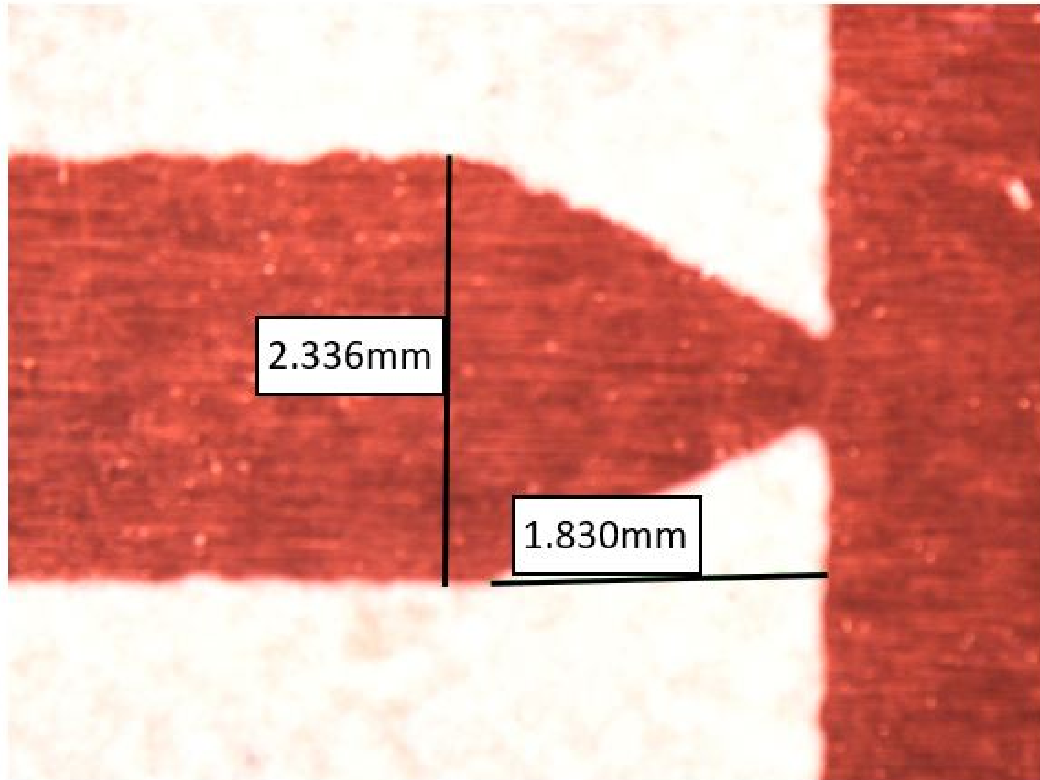


Figure 4.9: Dimensions of the fabricated filter's taper

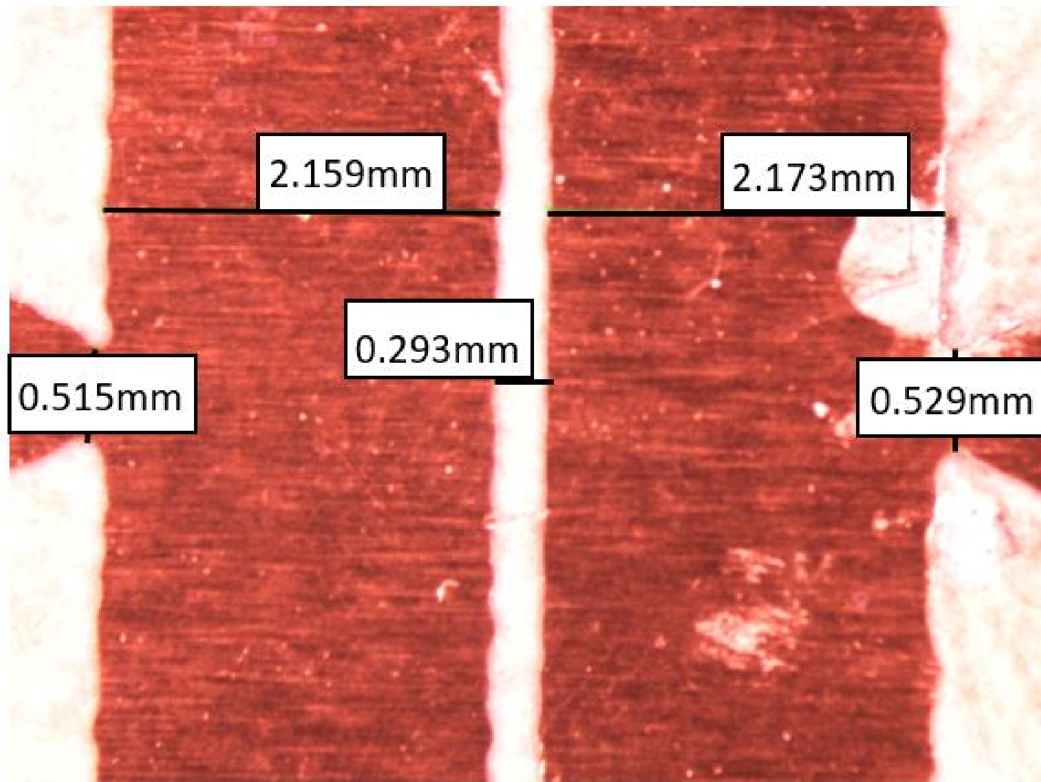


Figure 4.10: Dimensions of the fabricated filter's resonators

high insertion loss flattens the peak of the BPF, widening the 3 dB bandwidth.

The simulated response at 3 GHz has the ideal Butterworth shape, but the weaker external coupling of the manufactured filter indicates that there should be an increased ripple. In other words, the filter response should look more like a Chebyshev response at 3 GHz, and the ideal Butterworth shape should be shifted to a higher frequency where the external coupling is correct. An HFSS simulation was run with the physical dimensions and compared to the measured results in Figure 4.12.

Figures 4.13 and 4.14 show comparisons of the S_{11} of the original simulation, measurement, and simulation with physical dimensions when the center frequency is tuned to 3 GHz and 2.65 GHz, respectively. In the first plot, the original simu-

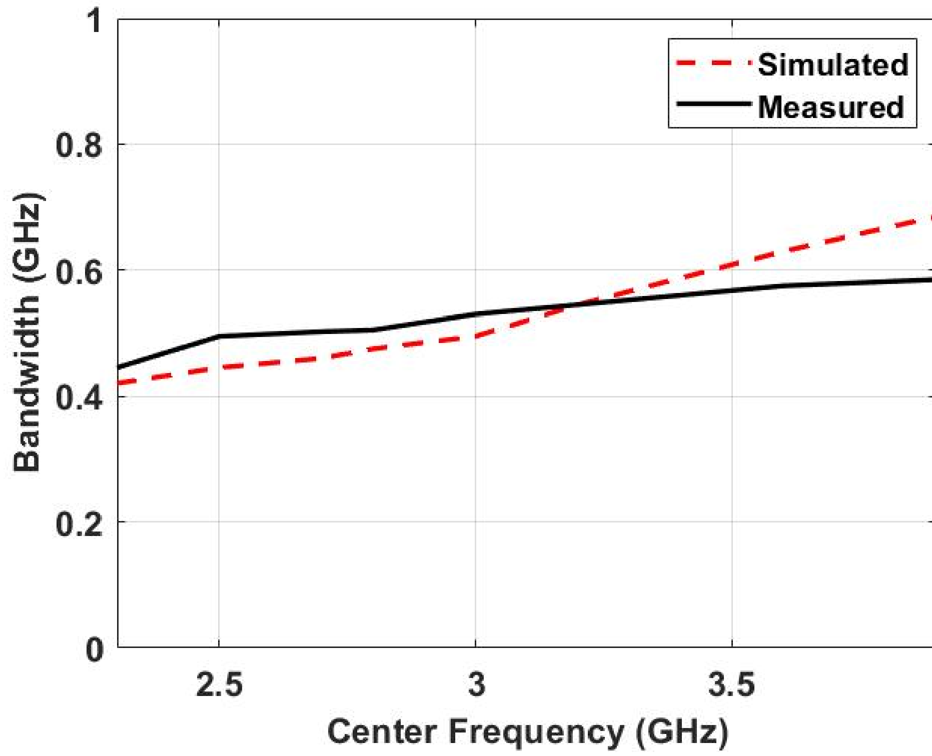


Figure 4.11: Measured and simulated bandwidth of the filter as a function of center frequency

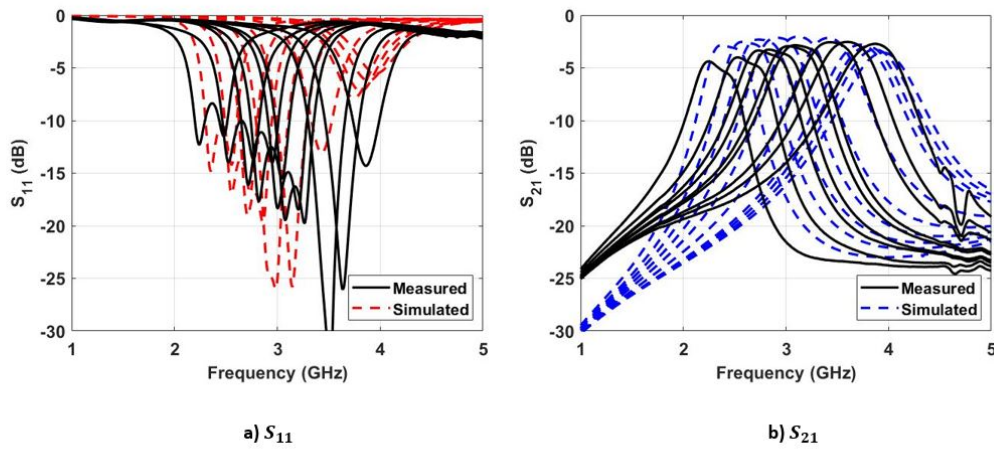


Figure 4.12: S-parameters of the measured filter and simulated with physical dimensions

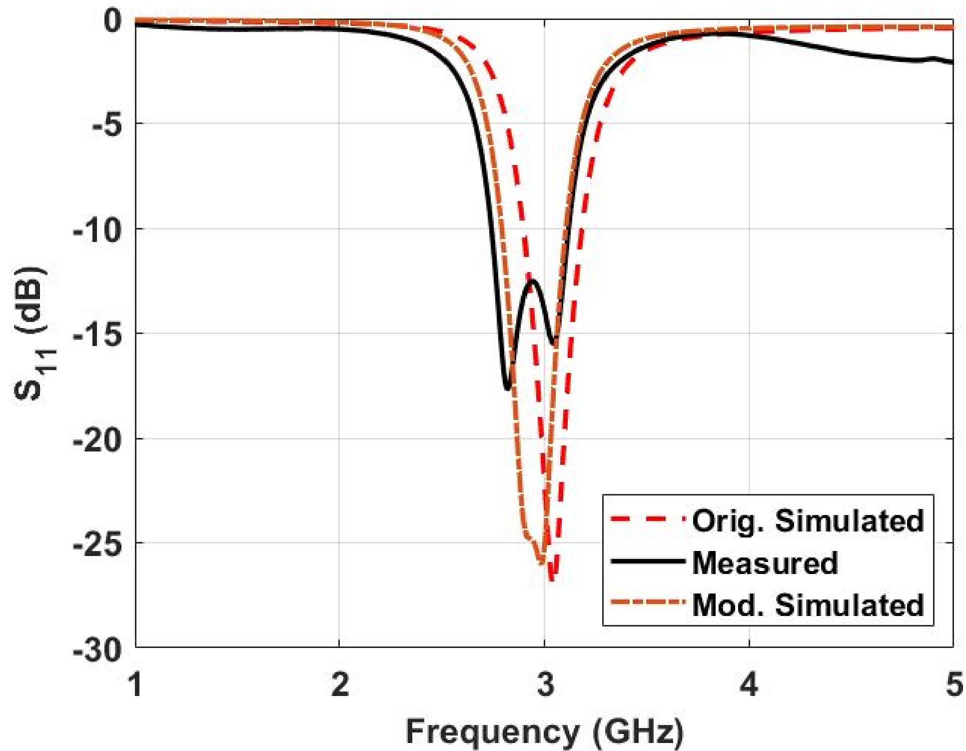


Figure 4.13: S_{11} of the original simulated, and simulated with physical dimensions tuned to 3 GHz

lation shows the ideal Butterworth response at 3 GHz while the measured response appears like a Chebyshev response. The simulated response with physical dimensions clearly has some ripple in it and is no longer Butterworth, but it does not have significant ripple like the measured response. This indicates that the modified external coupling is weaker than the original simulation, but it is not weak enough to recreate the measured response. The simulated response when tuned to 2.65 GHz lends itself to a similar conclusion. In this case, all three have Chebyshev shape, but the height of the ripples varies. The original simulation has a ripple of less than 3 dB while the measured has a ripple of almost 4 dB. Finally, the modified simulation has a ripple of 3.34 dB, again moving in the direction of the measured response. This trend is found at any given center frequency for the filter which indicates that

the physical dimensions can explain part of the altered external coupling but cannot explain the full change.

While simulating with the physical dimensions is not enough to get an exact match with the measured results, it does prove the dimensions' effects on the overall filter response bring it closer to the measured response. One possibility for the discrepancy is that the modified simulation does not entirely model the physical dimensions of the fabricated filter. The simulation's dimensions are an approximation of the dimensions shown in Figures 4.9 and 4.10, and they are likely not accounting for every non-ideal effect introduced by the under-etched design. The remainder of the shift can likely be attributed to an accumulation of other manufacturing variations. For example, a decrease in the air cavity's effective permittivity

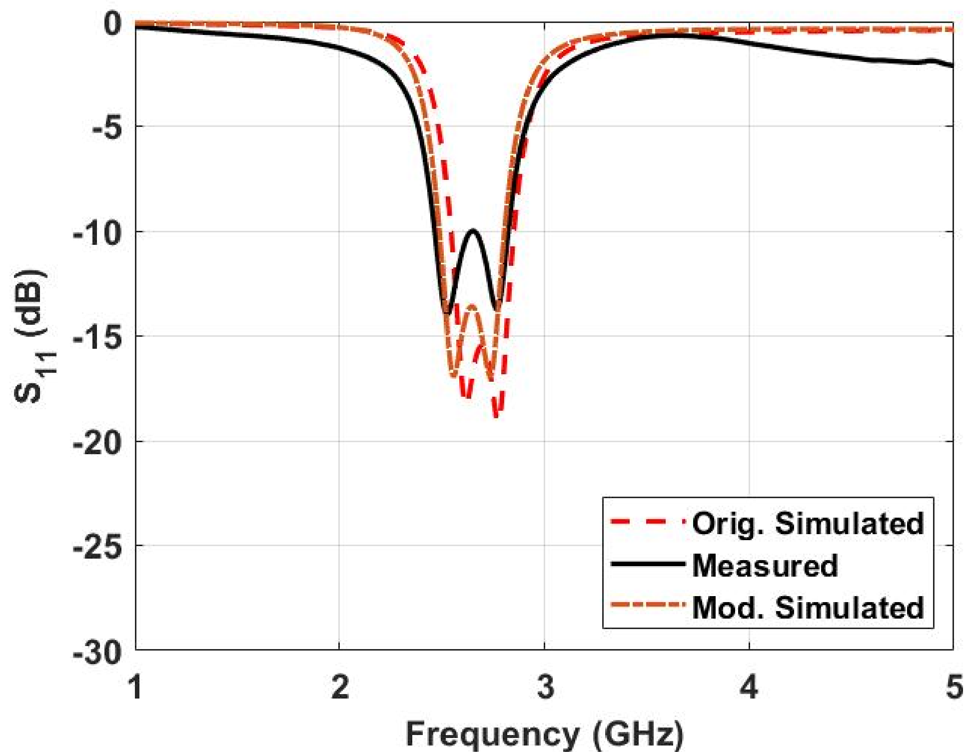


Figure 4.14: S_{11} of the original simulated, and simulated with physical dimensions tuned to 2.65 GHz

due to variation in Substrate 3's dielectric constant or a slightly thicker cavity due to warped boards would result in a shift higher in frequency. With a complicated, multi-layer structure, it is hard to account for all the possible non-ideal effects, but the modified simulation is trending in the direction of accurately recreating the measured filter response.

In this chapter, the designed thru-line and tunable filter were fabricated and measured, allowing comparison to the simulated results. The measured thru-line followed simulation well with only slight issues likely introduced by manufacturing tolerances. The center frequency of the tunable filter could be adjusted as desired, but bandwidth and shape did not match the simulated. The bandwidth variation could largely be attributed to the smaller inter-resonator gap of the fabricated filter. Similarly, other filter dimensions did not match their designed values, resulting in a net weakening of the external coupling. This could not explain the entirety of the issues with the filter's shape, but the general trend fits with measurement. Thought can now be given to the future of this surface mount SISL technology.

Chapter 5

Conclusions

The purpose of this chapter is to summarize the results of this work and consider future improvements. This chapter summarizes the findings in designing and fabricating a novel surface mounting structure for SISL while also demonstrating its application in a tunable filter design. This work also presents important considerations for system integration and packaging applications. Finally, there are improvements and future avenues of research in designing more highly integrated systems.

5.1 Summary

The purpose of this work was to develop a novel SMT SISL structure to enable greater integration for next-generation radar and communications systems. Future systems will require reductions in cost, size, weight, and power which requires higher integration.

First, an SMT SISL thru-line is designed as a proof-of-concept of the SMT structure using castellated vias. Chapter 2 demonstrates the design procedure behind SISL and focuses on the castellated via transition's design. The measured thru-line has an insertion loss of better than 0.85 dB across the entirety of S-band.

There was good agreement with the simulated results, indicating the HFSS model is capturing most of the design's intricacies. These results demonstrate the SMT technique is feasible and presents designers with a new method to realize highly integrated components.

The SMT SISL technology is then used to design a second-order Butterworth BPF that is tunable from 2.3 to 3.9 GHz. The entirety of the design, including the bias lines, is SMT-able, demonstrating an extension of the technology. The measured filter's tuning range is from 2.4 to 3.9 GHz with return loss better than 10 dB and insertion loss between 2.54 and 4.7 dB depending on center frequency. The measured response does not agree as well with simulated, but this can be explained by manufacturing errors, particularly photolithography, that would not be present in a professional fabrication run.

Overall, a novel technique for SMT has been designed and implemented, demonstrating an evolution of the SISL technology. The proposed designs maintain the SISL structure while being fully SMT-able without the difficulties of a "flip-chip" design.

5.2 Future Work

There are several areas of improvement on the existing design that is worth consideration. First, the existing design proved difficult to get a solid electrical connection from the carrier board to the middle layer with the use of bolts alone. Instead, solder proved necessary to get a good connection, and the best thru-line measurements were achieved by clamping the substrates together. The connection can possibly be improved in several different ways. One option is to investigate whether there are better bolt locations that achieve a more solid connection. An-

other option is to consider using rivets rather than bolts since they should be able to hold the structure together even more firmly. Finally, it could be worthwhile to laminate Substrates 2-5 together and solder the laminated substrates to the carrier board, rather than using bolts at all. This is also the closest to what a professional fabrication run would look like, and it seems like the most promising way to get excellent results.

Another useful avenue of research would be to investigate designs that take full advantage of the structure and its SMT-able nature. For example, removing Substrate 1 as in [18] allows Substrate 3 to be accessed without disassembling the stack-up. This allows the stack-up to be assembled and components soldered at a later time or even allows components to be reworked or replaced. Additionally, the other side of Substrate 3 (M6) can be used to locate additional components that do not fit on M5. These components can be reached through a simple via transition and introduce the possibility of adding additional tunable couplings to create a fully-reconfigurable filter among many possibilities.

It is also important to determine how high in frequency the castellated via transition can remain useful because radar and communications are increasingly moving to higher frequencies. A major challenge is pushing the LPF cut-off frequency higher while maintaining a good match. The cut-off frequency is improved by achieving smaller inductance or capacitance, but reducing one requires a reduction in the other to keep a good match. The inductance is easy to reduce by either shortening the via length or increasing its diameter, but the capacitance is limited by how big the anti-pads can be made. A more detailed investigation of combinations of via diameter, length, and anti-pad diameter to reach higher frequencies is especially important in extending this work to future designs.

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Appendix A

Fabrication Process

The detailed fabrication procedure for this work is presented in this appendix. All of the drilling steps are completed using an LPKF ProtoMat S104 milling machine [36]. The 10 mil thick substrates must be fabricated using the LPKF Protolaser U4 [37] or an in-house photolithography procedure because they are very difficult to mill on the S104. The SISL thru-line and filter builds are almost identical, with the only difference being which file to use for copper layer M5. The following Gerber and drill files are used to fabricate these designs:

1. CB_Top - metal layer 2 (M2)
2. M3 - metal layer 3 (M3)
3. M4 - metal layer 4 (M4)
4. M5_NotCastellated - metal layer 5 (M5) filter design
5. M5_Thru_NotCastellated - metal layer 5 (M5) thru-line design
6. M6_NotCastellated - metal layer 6 (M6)
7. M7 - metal layer 7 (M7)
8. CavCutout - cuts out the air cavity
9. CB_Outline - cuts out the carrier board
10. PreCastellatedCut_Outline - outline for Substrate 2 before the castellated cut

11. NonCastellated_Outline - cuts out Substrates 3, 4, 5 and makes the castellated cut on Substrate 2

12. BoltHoleDrills - NCD file to drill bolt holes to hold the design together

13. CB_Fiducials - NCD file to create alignment fiducials for the carrier board

14. Fiducials_PreCastellatedCut - NCD file to align Substrate 2 before the castellated cut is made

15. Fiducials_NonCastellated - NCD file to align Substrates 3, 4, 5

16. Drills_CB_Walls - NCD file to drill stitching vias for the carrier board

17. Drills_Connector - NCD file to drill via cage around the connector

18. ConnHolesCutout - NCD file to drill bolt holes for the connectors

19. SigViasOnly_D2 - NCD file to drill the signal and biasing vias that will be castellated later

20. D4_Drills - NCD file to drill stitching vias for Substrates 2, 3, 4

21. LithoMaskFiducials - NCD file to drill fiducials for mask alignment

22. LithoM5_AlignDrills - NCD file to read fiducials on S104 after photolithography

A.1 Layout File Generation

The first step to generate the above layout files is to delete the wave ports, connectors, radiation boundary, and all subtractions that were used to create vias. Then, each copper layer should be selected and exported as an AutoCad (dxf) file. Then use File, Import, AutoCad, and select the AutoCad file that was created in the previous step. The designer should then check for any errors in the layout (i.e. disconnected lines, missing contours) and correct any that are found. Once satisfied, a new layer should be created, called BoardOutline, and drawn around the area that

needs to be patterned. Then the layout can be exported, producing two Gerber files. The first file will be the pattern that needs to be milled while the second will be an outline of the board. This process should be repeated for every copper layer that needs to be patterned. The board outline for copper layers M5, M6, M7, M8, M9, and M10 can be reused since they all need to be the same size.

Substrate 2 is the layer that requires the castellated via, and this adds extra steps to the layout file generation. To create the castellated via, a standard via must first be drilled, plated, and then cut in half. This requires the designer to have two different outlines for this layer. The first outline must be large enough to encompass the entire via and will be used for the initial fabrication steps. The second outline should go through the middle of the via and will be used to cut it in half, creating the castellated via.

Since this is a multi-layer PCB stack-up, some of the vias will not go through all of the substrates. Therefore, the designer should start with a single substrate and select all of the vias that go through it. These should then be exported as an AutoCad file like before. Import these into HFSS once more, and select the via tool from the toolbar. Adjust the size of the via tool to the required via diameter and place a via on top of all the imported via layouts. Then export the file as NC Drill rather than Gerber. A dialogue box, shown in Fig. A.1, will open; change the units to millimeters and confirm the drill sizes match the design. Finally, change the significant figures to five for both integer and decimal and remember this selection. Repeat this process for each substrate layer that requires drills. Now that the board outlines, copper layers, and drill files have been generated, the design is ready for fabrication.

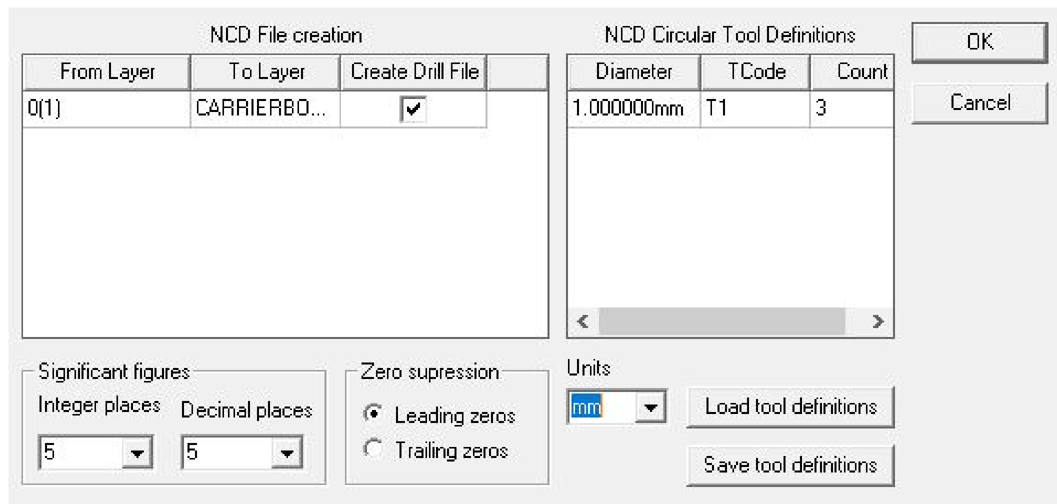

Figure A.1: Example settings to export NC Drill files

A.2 Detailed Fabrication Process

The fabrication process for Substrates 1, 3, 4, and 5 can be broken into five steps:

1. Mill Board Design
2. Photolithography Procedure
3. ProConduct Process
4. Cut Out Board Design
5. Assemble Layers

The fabrication process for Substrate 2 is similar but requires modification due to the electroplating procedure:

1. Drill Vias
2. Electroless Plating Process
3. Electroplating Process
4. Mill Board Design

5. Cut Out Board Design

A.2.1 Mill Board Design

For each substrate, the first step is to drill the alignment fiducials using either the S104 or U4. Next, the copper layers are milled. Substrates 1, 2, 4, and 5 can be milled on either the U4 or S104 while Substrate 3 must be milled using the U4 or photolithography procedure because it is so thin. The fiducials are used to align the machine to mill both the top and bottom of Substrate 2, and they must also be drilled in the other substrates for later fabrication steps. The milling is done before the via drills because of the requirements of the ProConduct processing.

A.2.2 Photolithography Procedure

One option to pattern Substrate 3 (the thru-line/filter layer) is to use an in-house photolithography procedure. This is especially useful for thin substrates that the S104 cannot handle or for creating a large number of designs in a single process.

1. Drill mask alignment fiducials using the S104.
2. Create masks in HFSS by importing design as AutoCad and arranging design.
3. Ensure masks are made black and negative before printing.
4. Print masks using the Canon D100. Ensure ink is printed on the rough side.
5. Apply photoresist film to the board using the laminator.
6. Align masks and tape them to the board.
7. Expose both sides to UV light.
8. Remove masks and protective film.
9. Wash the board in copper sulfate solution to remove the unexposed photoresist.

10. Place board in the etchant for 30 to 60 minutes.
11. Remove from etchant and use acetone to remove photoresist.
12. Wash with isopropyl alcohol and deionized water.

A.2.3 ProConduct Process

ProConduct is a process to create plated vias in-house for rapid prototyping of PCB designs [38]. The steps to plate the vias are as follows:

1. Apply the protective film to both sides of the milled circuit board.
2. Remove protective film around fiducials to allow the mill to read them.
3. Drill vias using the S104 mill.
4. Apply the conductive paste to the board and spread across the vias.
5. Turn on the vacuum table for 30 seconds to draw paste through the vias.
6. Repeat steps 4 and 5 for the other side of the circuit board.
7. Remove the protective film from both sides.
8. Cure the conductive paste in a hot-air oven for 30 minutes at 160°C.
9. Clean both sides of the board with the LPKF cleaning solution.

A.2.4 Cut Out Board Design

After the ProConduct process has been completed, the mill is used once more. First, bolt holes must be drilled in all of the layers so they can be held together. Additionally, bolt holes for the connectors are drilled for Substrate 1. Then the air cavities need to be cut out of Substrates 2 and 4. Finally, all of the boards' outlines should be cut. Substrate 2's cutout operation should cut through the middle of the signal and bias vias, making them castellated.

A.2.5 Substrate 2 Fabrication

For Substrate 2, the fiducials and vias must be drilled on the S104 first. The design is then ready to be plated using a two-part process. First, the electroless plating tank must be titrated to confirm it is within specification. Then, the electroless plating procedure can be carried out, following the directions available in the Fabrication Laboratory. This will apply a thin layer of copper to all the vias, but it is not thick enough for most designs. Therefore, the electroplating procedure must be carried out next. With the vias plated, no further special processing is required. The board may be milled and cut out exactly as Substrates 1, 3, 4, and 5 are.

A.2.6 Assemble Layers

Now that all of the boards are cut out, they need to be assembled. First, the layers are bolted together using M4 machine screws and nuts. Ideally, this should provide a good electrical connection without the need for solder, but getting a good connection between the castellated via and the filter or thru-line proved difficult. The filter or thru-line was implemented on a 10 mil thick board which seemed to flex too much to ensure a good connection. There are several options to ensure a solid connection. First, the castellated vias of Substrate 2 can be soldered to the carrier board. Substrate 3 cannot be soldered to Substrate 2 by hand, but there are several options. One is to apply solder paste to the pads and reflow using a heat gun. This should be acceptable, but it should be noted that ProConduct can generally handle a single reflow before it begins to fail. Another option is to use a clamp to compress the boards together, securing a very firm connection. Finally, bolt all the layers together and bolt the connectors onto the carrier board.

Appendix B

List of Acronyms and Abbreviations

ADS Advanced Design System

BPF - Bandpass Filter

BW - Bandwidth

CPWG - Co-planar Waveguide Grounded

C-SWaP - Cost, Size, Weight, and Power

EM - Electromagnetic

HFSS - High Frequency Structure Simulator

LPF - Lowpass Filter

MEMS - Microelectromechanical Systems

MWO - Microwave Office

PEC - Perfect Electric Conductor

PCB - Printed Circuit Board

RF - Radio Frequency

SMT - Surface Mount Technology

SISL - Suspended Integrated Strip-Line

SSS - Suspended Substrate Strip-Line