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InSb QUANTUM WELL STRUCTURES FOR ELECTRONIC DEVICE APPLICATIONS

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InSb QUANTUM WELL STRUCTURES FOR ELECTRONIC DEVICE APPLICATIONS

A DISSERTATION APPROVED FOR THE
HOMER L. DODGE DEPARTMENT OF PHYSICS AND ASTRONOMY

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This thesis is dedicated in memory of my father

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Introduction

The electron effective mass is smaller in InSb than in any other III-V semiconductor. Since the electron mobility depends inversely on the effective mass, InSb-based devices are attractive for field effect transistors, magnetic field sensors, ballistic transport devices, and other applications where the performance depends on a high mobility or a long mean free path. In addition, electrons in InSb have a large g-factor and strong spin orbit coupling, which makes them well suited for certain spin transport devices.

The first n-channel InSb high electron mobility transistor (HEMT) was produced in 2005 with a power-delay product superior to HEMTs with a channel made from any other III-V semiconductor. The high electron mobility in the InSb quantum-well channel increases the switching speed and lowers the required supply voltage. This dissertation focuses on several materials challenges that can further increase the appeal of InSb quantum wells for transistors and other electronic device applications.

First, the electron mobility in InSb quantum wells, which is the highest for any semiconductor quantum well, can be further increased by reducing scattering by crystal defects. InSb-based heteroepitaxy is usually performed on semi-insulating GaAs (001) substrates due to the lack of a lattice matched semi-insulating substrate. The 14.6% mismatch between the lattice parameters of GaAs and InSb results in the formation of structural defects such as threading dislocations and microtwins which degrade the electrical and optical properties of InSb-based devices. Chapter 1 reviews the methods and procedures for growing InSb-based heterostructures by molecular beam epitaxy.

Chapters 2 and 3 introduce techniques for minimizing the crystalline defects in InSb-based structures grown on GaAs substrates. Chapter 2 discusses a method of reducing threading dislocations by incorporating $Al_yIn_{1-y}Sb$ interlayers in an $Al_xIn_{1-x}Sb$ buffer layer and the reduction of microtwin defects by growth on GaAs substrates that are oriented 2° away from the [011] direction. Chapter 3 discusses designing InSb QW layer structures that are strain balanced. By applying these defect-reducing techniques, the electron mobility in InSb quantum wells at room temperature was significantly increased.

For complementary logic technology, p-channel transistors with high mobility are equally as important as n-channel transistors. However, achieving a high hole mobility in III-V semiconductors is challenging. A controlled introduction of strain in the quantum-well material is an effective technique for enhancing the hole mobility beyond its value in bulk material. The strain reduces the hole effective mass by splitting the heavy hole and light hole valence bands. Chapter 4 discusses a successful attempt to realize *p*-type InSb quantum well structures. The biaxial strain applied via a relaxed metamorphic buffer resulted in a significantly higher room-temperature hole mobility and a record high low-temperature hole mobility.

To demonstrate the usefulness of high mobility in a device structure, magnetoresistive devices were fabricated from remotely doped InSb QWs. Such devices have numerous practical applications such as position and speed sensors and as read heads in magnetic storage systems. In a magnetoresistive device composed of a series of shorted Hall bars, the magnetoresistance is proportional to the electron mobility squared for small magnetic fields. Hence, the high electron mobility in InSb QWs makes them highly preferable for geometrical magnetoresistors. Chapter 5 reports the fabrication and

characterization of InSb quantum-well magnetoresistors. The excellent transport properties of the InSb QWs resulted in high room-temperature sensitivity to applied magnetic fields.

Finally, Chapter 6 provides the conclusions obtained during this research effort, and makes suggestions for future work.

Chapter 1

Molecular Beam Epitaxy of InSb/AlInSb on GaAs (001)

1.1 Introduction

Molecular Beam Epitaxy (MBE) is a technique developed in the early 1970's for growth of high quality crystalline materials. It has advantages over other epitaxial methods like physical vapor deposition (PVD), chemical vapor deposition (CVD), atomic layer epitaxy (ALE), liquid phase epitaxy (LPE) and metal organic vapor phase epitaxy (MOVPE). Those advantages are very abrupt interfaces and the ability to precisely control thickness, composition and doping. By combining these features with the capability to rapidly change beam species, MBE has brought about a new era for the fabrication of sophisticated electronic and optoelectronic structures, such as high electron mobility transistors (HEMT), quantum-well detectors and superlattice lasers.

This chapter describes the MBE system installed at the University of Oklahoma, Department of Physics and Astronomy for growth of III-V semiconductor heterostructures, especially InSb/AlInSb quantum-well structures. First, basic components and their functions will be described. The next section describes source materials and effusion cells. The methods to create ultra high vacuum in the MBE system are described next. Then an *in-situ* analytical method called reflection high energy electron diffraction (RHEED) and its application during the MBE growth of InSb is addressed. Next, wafer preparation and InSb growth optimization on GaAs (001) are described. Finally some maintenance issues for MBE of pure semiconductors will be briefly described.

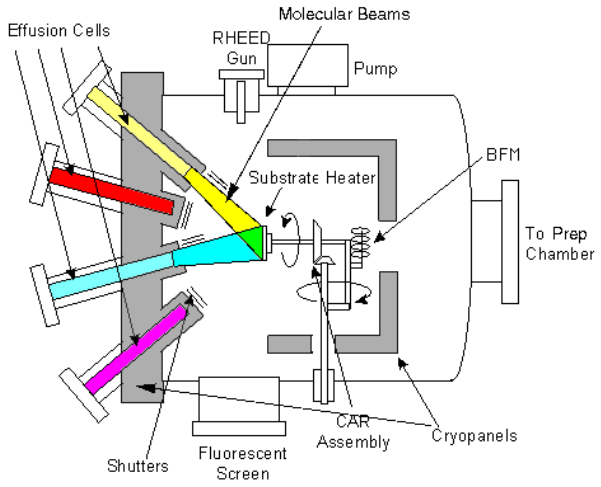


Figure 1.1 A growth chamber of a molecular beam epitaxy machine [1]

1.2 Basic components of MBE

The Intevac Gen II MBE system for III-V growth at the University of Oklahoma, consists of three stainless-steel ultra high vacuum (UHV) chambers: a load lock or entry-exit chamber, a buffer chamber which acts as a transition tube and an initial wafer preparation chamber, and a growth chamber. Each chamber is isolated from the others by a gate valve, which enables the substrate to be introduced into the growth chamber without breaking the vacuum. A schematic diagram of a typical MBE growth chamber is shown in Figure 1.1.

The entry-exit chamber is used to load cleaned wafers into and unload grown wafers from the MBE system. The wafer holder trolley is baked in the entry-exit chamber after each exposure to the atmosphere at 200 ^{0}C for a minimum of 2 hours. The wafer trolley sits on a rail and can be moved along the rail using a magnet. Loaded wafers are then stored in the buffer chamber. Wafers can be moved to the heated station in the buffer

chamber or loaded into the growth chamber via a magnetically coupled transfer rod. The wafer is degassed on the heated station, then transferred to the growth chamber. To obtain a uniform growth rate across the wafer, the wafer holder is designed to rotate azimuthally. This substrate manipulator is called the CAR (continuous azimuthal rotation) assembly. On the opposite side of the substrate holder there is an ion gauge to measure the beam equivalent pressure (BEP). The substrate holder is made out of Molybdenum (Mo) or Tantalum (Ta) which can be heated up to 1400 $^{\circ}$C without significant outgassing of impurities. There is a small chamber adjacent to the entry exit chamber for outgassing new effusion cells prior install into the growth chamber.

Analytic and diagnostic facilities included in the growth chamber are a quadrupole mass spectrometer for residual gas analysis (RGA) and leak detection, and a reflection high-energy electron diffraction (RHEED) arrangement. The RHEED assembly consists of a 10KeV electron gun and a fluorescent screen. More details of RHEED will be discussed in Section 1.5. Analytic facilities, x-ray photoelectron spectroscopy and scanning tunneling microscope, are available in separate vacuum chambers. Those chambers are designed such that wafers can be transfered to them without breaking the vacuum.

1.3 Beam sources

Molecular beams are generated from materials held in the crucible of an effusion cell. Intensities are controlled by the cell temperatures regulated through proportional (P), integral (I) and derivative (D) controllers. Shutters in front of each cell aperture switch individual beams on and off. The cells are thermally isolated from each other by heat

shields filled with chilled alcohol at -37 °C. All shutters and cell temperatures are computer controlled.

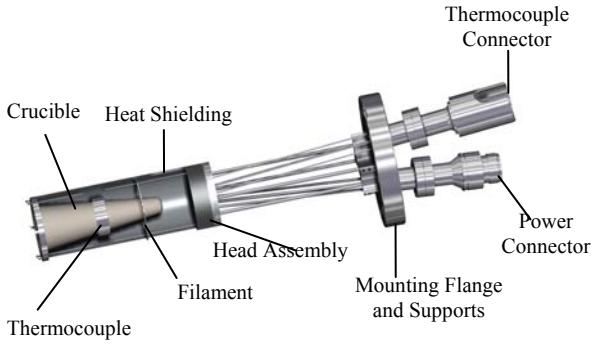


Figure 1.2 Effusion cell (Knudsen cell) from Veeco designed for monoatomic sources and its basic components [1]

There are eight ports available for effusion cells in the Gen II MBE system and one is currently used as a viewing window. The available source materials are Al, In, Ga, Sb, As, Si (n-type dopant) and Be (p-type dopant). All the group III cells produce mono-atomic beams. An effusion cell (Knudsen cell) designed as a mono-atomic source is shown in Figure 1.2. The 50 cc conical crucible is made of pyrolytic boron nitride (PBN). PBN is a material that is easy to outgas and non-refractive. PBN has the ability to withstand elevated temperatures so that it does not chemically contaminate the source material within it [3].

Group V source beams consist of tetra-atomic molecules when coming directly from the elemental source (As_4, Sb_4 and P_4). The tetramers can dissociate into dimers by passing through a high temperature stage (cracker). For Sb, there is a two-zone Knudsen cell where second stage temperature (900 °C) is much higher than the first stage

temperature (400-500 °C). A valved cracker for As is installed in order to obtain As dimers. The source material is loaded into a large capacity crucible. A needle valve which can be operated using an automated valve positioner, regulates the flux of As_2 molecules that enters the growth chamber. The cracking zone temperature is maintained at 950 °C. A diagram of a valved cracker is shown in Figure 1.3. Since the cracker cells extended outside the alcohol shroud, cooling water is circulated around both As and Sb crucibles to dissipate heat from the crucible.

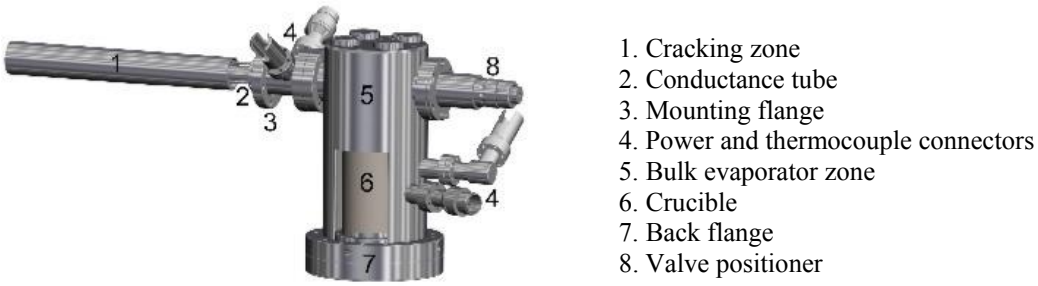


Figure 1.3 A valved cracker from Veeco and its basic components [1]

Careful solidification and melting is required for Al and Ga cells. The Al melting point is 680 °C. Solidifying too quickly will result in cracking the crucible since Al adheres to the crucible wall and contracts during solidification. In order to minimize damage due to Al leaking through the cracks after subsequent melting, the Al charge is loaded into a double walled crucible or a single walled crucible with an insert. If the Al source is melted too quickly, the source material can creep over the lip of the crucible. The Ga melting point is around 30 °C. In a power failure, chilled alcohol cooling will bring the Ga cell temperature to 30 °C rapidly and rapid freezing can damage the crucible.

To avoid the sudden cooling in a power failure, a back up system was designed to provide power to the Al and Ga cells.

1.4 Creating an ultra high vacuum

An important factor for good functioning of a MBE system is maintaining a UHV environment including minimizing the partial pressure of O_2, H_2O, CO_2 and CO in the order of 10^{-11} Torr. To achieve UHV conditions, MBE systems are made from low vapor pressure materials that can be outgassed for a long period (~ 7-10 days) at temperatures around 150-200 °C. After opening to the atmosphere, a UHV condition is typically achieved in two pumping steps. A rough pump down up to ~ 10-100 mTorr is achieved by using a diaphragm pump and a molecular drag pump mounted on a separate cart. A liquid nitrogen cooled cryoshroud, located between the chamber walls and the CAR (as shown in Figure 1.1), a helium cryopump, and a sputter ion pump bring the pressure in the growth chamber down to UHV levels. A titanium sublimation pump (TSP) is also run when necessary.

The MBE system has two cryopumps, one connected to the entry-exit chamber and one connected to the growth chamber. The main parts are the compressor, expander and cold head. A closed loop helium refrigerator, or compressor, cools the cold head. Gases are pumped by cryo-condensation (N_2, O_2, Ar at 10-20K; CO_2 and H_2O at 50-80K) and cryo-adsorption (H_2, He and Ne). The pressure that can be obtained using a cryopump is around 10^{-8} Torr in the entry-exit chamber and $<10^{-10}$ Torr in the growth chamber.

Two ion pumps are operating to pump gasses in the growth and buffer chambers. There are several pumping mechanisms that occur in the ion pump. A high electric field ionizes molecules. Positive ions accelerate towards a cathode. Magnets increase the path lengths of the accelerated electrons which increases the ionization probability. The positive ions sputter Ti ions from the cathode and the Ti getters reactive gases to form more stable oxides, nitrides, carbides, and hydrides. H_2 directly adsorbs onto freshly exposed Ti surfaces of the cathode. The ultimate pressure obtainable is 10^{-11} -10^{-12} Torr.

In a Ti sublimation pump, the Ti filament is heated up to 1000-1500 °C by applying an electric current. Ti vaporizes or sublimes at 1000-1500 °C. Ti atoms condense on surfaces surrounding the source, and getters with reactive gas molecules to produce stable products with negligible vapor pressures. Chemically inert gases (He, Ne, Ar) are not pumped by a TSP.

1.5 Reflection high energy electron diffraction (RHEED)

RHEED is a common *in-situ* tool for studying surface roughness, growth modes and growth rates during the MBE growth. A high energy (10-100 keV) electron beam is incident on the wafer surface at a gracing angle (1-3°). Electrons do not penetrate deep into the wafer. Therefore, RHEED is surface sensitive and the diffraction occurs primarily from the two-dimensional lattice of atoms on the surface. The reciprocal lattice of a two-dimensional lattice in real space is a series of infinite rods.

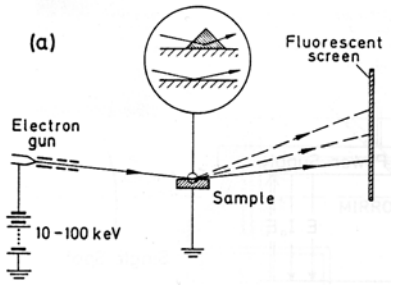


Figure 1.4 A schematic diagram of a RHEED assembly [4]

1.5.1 Surface morphology

An ideal crystal gives diffraction spots when the rods of the reciprocal lattice intersect the Ewald's sphere of the incident electrons. If the surface is amorphous, no diffraction pattern is observed, only a diffuse background. If the surface is polycrystalline, the diffraction pattern is diffuse rings. Three-dimensional rough surfaces give a spotty pattern. These surface conditions and the corresponding RHEED patterns are schematically drawn in figure 1.5.

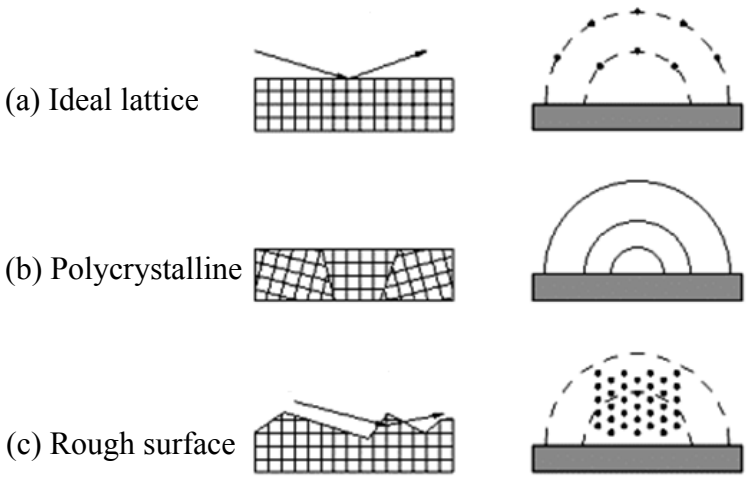


Figure 1.5 Schematics of RHEED patterns observed for different surface conditions. (a) Ideal surface (b) Polycrystalline surface (c) Rough surface [5]

1.5.2 Surface reconstruction

RHEED can be used to identify the surface reconstruction, which provides a clear indication of correct stoichiometric growth at a given temperature and flux ratio.

The surface of a semiconductor layer is different from the bulk. In order to minimize the surface energy, the surface atoms rearrange to change the periodicity and symmetry. Often they form dimers, which reduce the number of unsaturated dangling bonds [6]. Wood's notation for reconstructed surfaces can be expressed as;

$$c\left(a_{1S}/a_{1B}\times a_{2S}/a_{2B}\right)R \qquad 1.1$$

Where, a_{1S} and a_{2S} are unit translation vectors of the reconstructed surface [6]. a_{1B} and a_{2B} are unit translation vectors of the bulk crystal. R stands for a rotation of the surface mesh with respect to the bulk. The symbol c is for centered mesh.

GaAs (001) substrate has a (2×4) reconstruction at 580 °C. InSb grown on GaAs (001) at around 420°C with a V/III growth rate ratio of 1.2, has an asymmetric (1×3)

(pseudo (1×3)) reconstruction. At a specific lower temperature value, under a static condition (only Sb_2 shutter is open), this reconstruction changes to *c*(4×4). A sharp transition was observed when the thermocouple (TC) reading for the substrate is 365 °C and the Sb/In ratio is ~ 1.5 [7]. The transition temperature can be used to calibrate the substrate temperature. Under a static condition, the InSb transition temperature was investigated by A.G. Oliveira *et al.* [8] and found to be 390 °C. A schematic representation of RHEED pattern evaluation (phase transition) for InSb or $Al_xIn_{1-x}Sb$ is shown in Figure 1.6. The transition temperature observed for $Al_xIn_{1-x}Sb$ (265-305 °C) is lower than InSb (340-365 °C after growth of ~ 3μm).

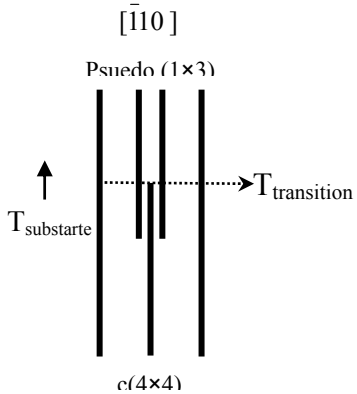


Figure 1.6 A schematic representation of RHEED pattern evaluation (phase transition) of InSb or $Al_xIn_{1-x}Sb$

1.5.3 Growth rate calibration

The RHEED intensity oscillation frequency is a quick, accurate and direct measurement of the growth rate. The growth rate is determined by the intensity fluctuation of an individual diffraction spot, usually the specular spot. The maximum intensity is obtained from a completely grown layer. The minimum intensity is obtained

when the layer is approximately half grown. The period of the intensity oscillation is equal to the time to grow one monolayer.

Ga, Al and As growth rates can be obtained on a GaAs epilayer grown on a GaAs (001) substrate. Growth rates are calibrated at the growth temperature, typically 40°C above the oxide desorption temperature. In and Sb growth rates are calibrated on an InSb epilayer grown on a GaAs (001) substrate. Growth rates are calibrated around 25 °C below the transition temperature.

For Group III elements, a group III shutter is open for few seconds until a few monolayers are grown while keeping the group V shutter open. RHEED oscillations are recorded using a CCD camera and KSA 4000 software. When calibrating group V elements, the group V shutter is closed and the group III shutter is open for few seconds (10-15 seconds). Then the group III shutter is closed and the group V shutter is open, while recording the RHEED oscillations.

Beam equivalent pressure (BEP) is another tool to calibrate the growth rates in MBE. BEP is the reading from an ion gauge placed where the substrate is located during growth. BEP is proportional to the flux at the substrate surface, hence to the growth rate. A technique like composition and thickness calculation or a record of growth rate calibration are required to directly relate BEP to growth rate. The repeatability of BEP is uncertain due to coating and loss of sensitivity for the filament. A relation between growth rate calibrated from RHEED oscillations and BEP is shown in Figure 1.7 for In and Sb sources.

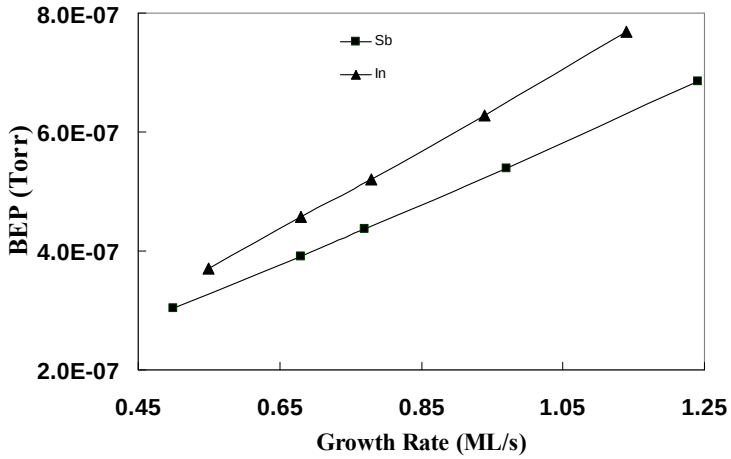


Figure 1.7 Relationship between BEP and Sb and In growth rates of the III-V MBE chamber at OU

1.6 Wafer surface preparation

An atomically cleaned substrate is the single most important step for successful epitaxial growth. The GaAs wafers used in this study are epi-ready. They are pre-cleaned and individually packed in a dry nitrogen (N_2) gas environment by the manufacturer. There is an intentional oxide layer grown in a controlled environment. Three-inch diameter wafers are cleaved into four quarters and blown with N_2 gas before loading. Care must be taken to minimize the amount of dust and scratching from handling. The quarter wafers are then mounted on wafer holders and loaded into the entry-exit chamber. New wafers are baked in the entry-exit chamber at 200 °C for a minimum of two hours. The wafers are then transferred to the buffer chamber. Before being transferred to the growth chamber, each wafer holder is out-gassed on the buffer chamber's heated station at 300 °C.

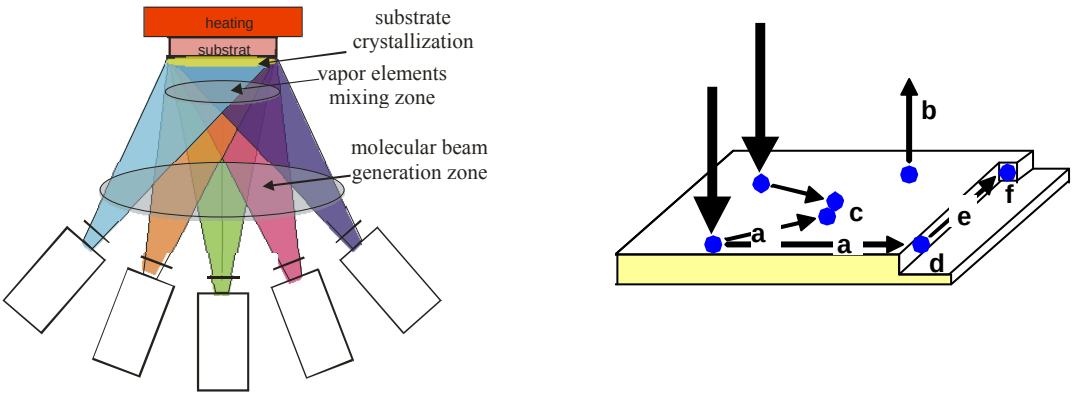
Prior to the growth, the oxide layer is thermally removed from the GaAs wafer under a group V flux. For GaAs, the group V flux is normally As_2. But in this study oxide desorption was done under a Sb_2 flux. Diffrences in carrier mobility were not observed in

layers grown under As_2 flux and Sb_2 flux. The base pressure during the InSb growth can be maintained at mid 10^{-10} Torr with the Sb_2 flux. Cross contamination of As in antimonide layers can be avoided by using an Sb_2 flux for oxide desorption. After seeing the clear streaky RHEED pattern (2× reconstruction can be seen clearly along [110] azimuthal, but 4× reconstruction cannot be observed clearly, instead facets are observed) indicating that the oxide is gone, the substrate temperature is increased by another 40 °C above the oxide desorbed temperature for another 15-20 minutes.

1.7 Growth optimization

A characteristic feature of MBE is the beam nature of the mass flow (neutral thermal beams) towards the heated substrate with a long mean free path. The growth chamber can be divided into three basic zones where three physical phenomena take place as schematically shown in the Figure 1.8(a). The generation of a molecular beam occurs in the first zone. The second zone is the mixing zone, where the beams from different sources intersect. In the third zone, vaporized elements mix together and form a special gas phase contacting the substrate area, where the crystallization takes place.

A series of processes are believed to happen on the surface of the substrate [9]. As illustrated in Figure 1.8(b), impinging atoms or molecules can take part in any of these processes; (a) surface diffusion (b) desorption (c) formation of two dimensional clusters (d) incorporation at steps (e) step diffusion and (f) incorporation at kinks [9]. All these steps are strongly dependent on substrate temperature, crystal orientation and flux ratios.



(a) (b)

Figure 1.8 Schematic illustration of (a) three basic zones where three physical phenomena take place (b) the surface processes occurring during the film growth. [1]

After oxide desorption, the substrate temperature is decreased to an optimum growth temperature under a beam of group V molecules (Sb_2 in this study). The optimum growth temperature was determined by measuring the electron mobility in InSb and $Al_{0.1}In_{0.9}Sb$ epilayers grown on GaAs substrates at different growth temperatures. A growth temperature of 380 °C, showed the highest mobility for $Al_{0.1}In_{0.9}Sb$. An InSb epilayer showed the highest mobility when the substrate temperature was 400 °C. The buffer layer is grown at 380 °C. After growth of the buffer layer, the InSb QW is grown at a temperature around 25-35 °C below the transition temperature of $Al_xIn_{1-x}Sb$ in order to get maximum Si doping efficiency [10].

There are five possible growth modes for epitaxial growth. Those are the Volmer-Weber mode, the Frank-van der Merwe mode, the Stranski-Krastanov mode, the columnar growth mode, and the step flow growth mode [11]. Initial growth of highly

mismatched InSb or $Al_xIn_{1-x}Sb$ on GaAs (001) takes the Volmer-Weber mode [12,17]. In this mode nucleation and coalescence of three dimensional islands occur.

For most of the III-V epitaxy, the group V flux is greater than the group III flux [13]. But in Sb related growth, a large excess of Sb enhances surface defects such as vacancies and clusters, since excess Sb accumulates on the surface [14, 15]. Michel *et al.* [14] observed the highest electron mobility in InSb epilayers when the In/Sb growth rate ratio is 0.8/1 at a growth temperature of $T_{transition}$ + 5 °C. An accurate control of III/V growth ratios is crucial for good stoichiometric growth. The V/III ratio was kept between 1.1 and 1.4 during the growth of InSb QWs in this study.

1.8 Maintaining the MBE

Proper maintenance of the MBE system is required for growth of high purity III/V semiconductors and a long lifetime of vacuum components. The MBE chamber is vented when cells need to be refilled with source materials, new components need to be installed, components malfunction (a shutter, pressure gauge, CAR, phosphor screen, *etc*.) or repair is required for a leak that cannot be eliminated by tightening the flanges.

When venting the MBE system for any of these reasons, it is a good practice to check the inventory of the necessary components (gaskets, MBE grade materials, crucibles, inserts, *etc*.) beforehand. A minimum exposure time to air minimizes the pumping time due to less water vapor, carbon monoxide and carbon dioxide adhered to the chamber interior [16]. It also a good practice to organize the order and schedule of the tasks that need to be done.

If there is a new effusion cell or furnace to be installed, then it should be degassed in the outgassing station adjacent to the entry-exit chamber. Once the new effusion cells are properly prepared according to the manufacturer, the existing effusion cell temperatures are lowered to 200 °C. The system is then warmed up by disconnecting the liquid N_2 supply and the cooling water supply, and valving off the alcohol chiller. Then the effusion cells are lowered to room temperature and the powers to the cells is turned off. The roughing line is pumped using the external pumping cart until below ~10 mTorr. Then the cryopump and ion pump are valved off from the growth chamber. The required torque for the ion pump valve is 25 foot-pounds. The pressure gauges are also powered off. The vent valve is slowly open to allow the chamber to fill with N_2 gas very slowly (15-20 minutes from UHV to atmospheric pressure).

Refilling of source material should be done as the last task. All the other maintenances should be done prior to material refilling. The order of the refilling is In, Sb, Si, Be, Ga, As and Al. Al is last since it oxidizes easily. After putting Ga into the crucible it should be melted using an ultra violet (UV) lamp. Effusion cell ports should be cleaned while loading the crucibles. Once a flange is opened, it should be covered with a clean piece of Al foil. Each gasket should replaced by a new copper gasket. The chamber is under a slight N_2 gas overpressure during the whole process. If the whole process takes more than one day then the chamber is pumped down after the end of the day and vented again the next day.

After all the flanges are sealed, the system is pumped down by the roughing pumps and then the cryopump valve is opened. Once the pressure of the chamber is on the order of 10^{-7} Torr, the ion pump valve is opened. A leak check is performed using He

gas and the RGA. Then the system is prepared for baking. All the non-bakeable wires and connections are removed and bakeable cables should be connected to thermocouples and heaters. The substrate heaters in the growth and buffer chambers are connected to pins A and F. Hoses for cooling water and compressed air should be disconnected. The valve between the cracker and bulk in the As source should be kept open during baking. The isolation valves between the chambers should be kept slightly open during baking to prevent the permanent deformation of their viton gaskets. The door of the entry-exit chamber, which has a viton gasket, is replaced with a blank that has a copper gasket. All the glass viewing ports are covered by Al foils to distribute heat evenly. The cell temperatures are slowly increased to 400 °C. After attaching the bake out panels, the baking temperature is slowly increased to its maximum value (~ 175 °C). Care must be taken during the temperature increase by monitoring the chamber pressure. The ion pump and the panel heaters turn off if the base pressure increases above 10^{-5} Torr. After venting the system, baking continues at least for ten days.

After the chamber cools down to room temperature, the base pressure should be ~ 10^{-10} Torr. The ion gauges and filaments of the TSP should be degassed. A leak check should be performed again. The residual gas spectrum should also be able to indicate of small leaks. Typical residual gas peaks observed in a MBE chamber are shown in Table 1.1. If there is a leak from atmosphere, a large water vapor peak (18), an oxygen peak (32), a large argon peak (40) and slightly larger N_2 (28) and CO_2 (44) peaks than normal will be evident in the RGA spectrum [16].

After the chamber is completely at room temperature (around 24 hours after baking is stopped), the liquid nitrogen line from the phase separator can be connected and

the valve opened to slowly fill the cryoshroud with liquid nitrogen. After another 3-4 hours, the cooling alcohol (methanol) to the source shroud should be restarted. After running the TSP, the pressure of the growth chamber should reach the 10^{-11} Torr range.

Mass/ Charge	Species
2	H_2^+
4	He^+
16	$CH_4^+ or O^+$
20	Ne^+
28	$N_2^+ or CO^+$
37.5	As^{++}
40	Ar^+
44	CO_2^+
75	As^+
150	As_2^+

Table 1.1 Typical residual gas peaks observed in a MBE chamber. [16]

Chapter 2

Low Defect Buffer Layers for Highly Mismatched InSb/GaAs Heteroepitaxy

2.1 Introduction

The ever increasing high number of compound semiconductor epitaxial materials needed for diverse electronic and optoelectronic applications all require high quality, single crystal substrates. Within the vast range of elemental, compound and alloy semiconductors very few are useful as a substrate for epitaxial growth of compound semiconductor structures. Available substrates are Ge, Si, GaAs, InP, GaSb, InAs, GaP sapphire (α-Al_2O_3), 6H-SiC and 4H-SiC. This leads to mismatched heteroepitaxy in which a material of different lattice constant is deposited onto a single crystal substrate. The interface between substrate and epilayer is coherent up to a certain critical thickness and the epilayer is strained to adopt the in-plane lattice parameter of the substrate. This type of strained layer growth is known as psuedomorphic growth. A difference in thermal expansion coefficient and the presence of impurities also causes strain in an epilayer [1]. After exceeding a critical thickness, misfit dislocations (MDs) (dislocations accommodate the misfit between two lattices) will be introduced in the epilayer to lower the strain energy. Since dislocations cannot end inside the crystal [2], a misfit dislocation should either run out to the edge of the substrate or have a segment that threads down to the back side of the substrate or threads up to the surface of the epilayer. These segments are called threading dislocations. Other structural planar crystal defects encountered in semiconductor heteroepitaxy include stacking faults, twins and inversion domain boundaries.

Dislocations degrade the device performance only when the dislocations penetrate the device structure. Mainly the presence of threading dislocations (TDs) and micro-twins (MTs) at the active area of the heterostructure degrade its electronic properties, affecting device performance and carrier lifetimes.

The main approach to solving the problem of a high density of defects in the device structure is the use of a buffer layer. Other techniques to control densities, types and arrangements of defects are patterned substrates [3], patterning and annealing [4], epitaxial lateral overgrowth [5] or compliant substrates [6,7]. These techniques remove or reduce exsiting defects from relaxed heteroepitaxial layers [1] or prevent the introduction of dislocations in the first place.

Because there is no semi-insulating substrate that is lattice matched to InSb, InSb QW structures in this study are grown on GaAs (001) substrates. GaAs wafers are available for a reasonable price (~$100 for 3" diameter wafers) and state of the art processing technologies make it popular as a substrate for many compound semiconductor systems. The lattice mismatch between InSb and GaAs is 14.6%. Structural defects, primarily threading dislocations (TDs) and micro-twins (MTs) are observed in a highly mismatched buffer layer grown between an InSb QW structure and a GaAs (001) substrate [8-11].

This chapter will first provide a brief review of stress and strain, critical thickness, defect structures and transmission electron microscopy. Different buffer-structure approaches for defect filtering and strain relief will be addressed next. Finally an approach for defect filtering in $Al_xIn_{1-x}Sb/Al_yIn_{1-y}Sb$ interfaces in the InSb/GaAs (001) system will be discussed.

2.2 Review of crystal defects and characterization

2.2.1 Biaxial stress, strain energy and lattice relaxation

In heteroepitaxial growth one usually assumes a biaxial stress, that is the in-plane (growth plane) stresses applied by the substrate in the *x*-and *y*-directions are equal and the out-of-plane (growth direction) stress is zero. When biaxial stress is applied to a cubic crystal the unit cell of the epitaxial layer become tetragonal with an in-plane lattice constant *a* and out of plane lattice constant *c*. Then the in-plane strain (ε_{11}) and out-of-plane strain $\varepsilon_{\perp}$ are defined by,

$$\varepsilon_{11} = \frac{a - a_0}{a_0} \tag{2.1}$$

$$\varepsilon_{\perp} = \frac{c - a_0}{a_0} \tag{2.2}$$

Where a_0 is the unstrained (relaxed) lattice constant for the epilayer.

The work done by the biaxial stress to deform the epilayer is converted to energy stored in the epilayer. This strain energy per unit area (E_ε) is related to the biaxial strain,

$$E_\varepsilon = \varepsilon_{11}^2 \gamma h \tag{2.3}$$

Where γ is the biaxial modulus (proportionality constant between in-plane strain and biaxial stress) and *h* is the layer thickness.

The lattice mismatch between epitaxial layer and the substrate is defined as,

$$f \equiv \frac{a_s - a_e}{a_e} \tag{2.4}$$

The mismatch *f* is positive or negative for tensile and compressive systems, respectively. For the pseudomorphic (coherent) growth, occurring for thin heteroepitaxial layers with less than ~ 1% mismatch, the in-plane strain equals the lattice mismatch. As

the layer thickness increases, strain energy increases and at a critical thickness h_c, it is energetically favorable for the introduction of misfit dislocations to relax some of the strain. In partially relaxed layers (part of the strain is accommodated by the misfit dislocations), the residual strain of the heteroepitaxial layer is a function of the mismatch and layer thickness. In thick layers, most of the mismatch can be accommodated by misfit dislocations. Some strain may be observed at different temperatures from the growth temperature due to the difference in thermal expansion coefficients of the substrate and the epilayer.

The critical layer thickness was calculated by Matthews and Blakeslee [13] in 1974. They assumed that a pre-existing TD is bent and forms a misfit dislocation at the interface once the critical layer thickness is reached. Here the critical layer thickness is calculated by equating the glide force to the line tension for the misfit segment. Later Matthews [14] calculated the critical layer thickness by balancing the strain energy with the energy of a grid of strain relieving misfit dislocations. In both approaches the expression for critical layer thickness is,

$$h_c = \frac{b(1-\upsilon\cos^2\alpha)[\ln(h/b)+1]}{8\pi|f|(1+\upsilon)\cos\lambda} \qquad 2.5$$

Where ν is the Poisson ratio, α is the angle between the Burgers vector and the line vector of the dislocation, b is the length of the dislocation and λ is the angle between the Burgers vector and the line in the interface plane that is perpendicular to the intersection of the glide plane of the interface. For (001) zincblende semiconductors it is assumed that cosα = cosλ = ½ and $b = a/\sqrt{2}$ [1].

2.2.2 Types and properties of dislocation

Dislocations are linear defects where interatomic bonding is disturbed relative to the perfect crystal. Along a dislocation line there are dangling bonds and large local strain field. There are two basic type of dislocations; namely screw and edge dislocations. Screw dislocations can be created by application of a shear stress on to a regular crystal as shown in Figure 2.1[58]. The arrangement of atoms around a screw dislocation forms a single surface helicoid (similar to a spiral stair case) [12]. An edge dislocation can also be created by applying a shear stress as shown by Figure 2.1. An extra half-plane of atoms is added to an otherwise perfect crystal. The edge of the extra plane coincides with the dislocation and gives its name [12].

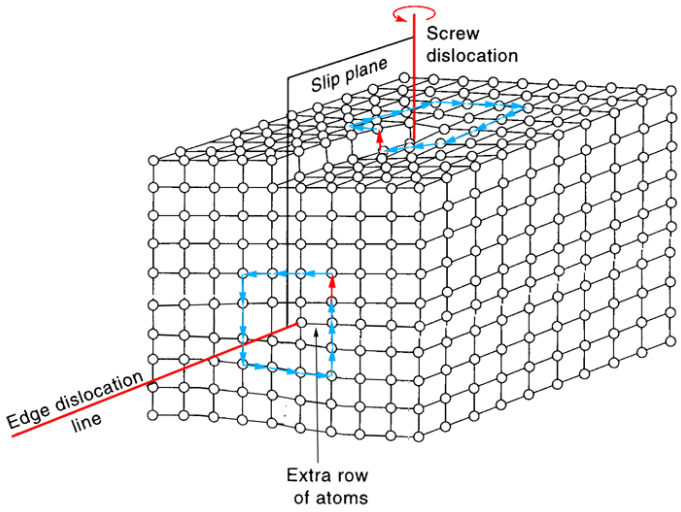


Figure 2.1 A screw and an edge dislocation [58]

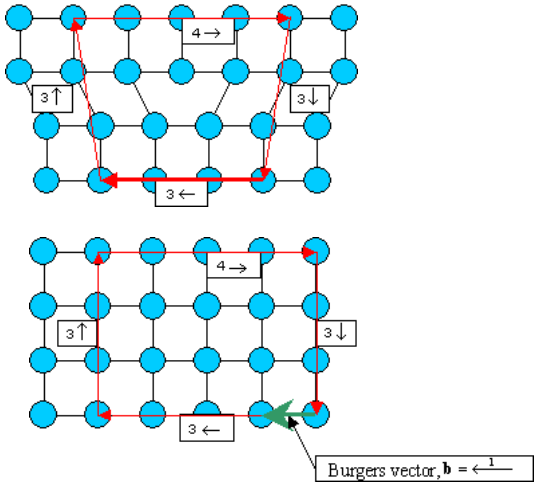


Figure 2.2 The Burgers circuit [58]

A dislocation is defined by its line vector, Burgers vector (***b***) and glide plane. The line vector is in the direction of the line of dislocation and usually expressed as a basic lattice translation or combination of lattice translations [1]. The method of defining the Burgers vector is shown in Figure 2.2. A closed cycle is made around a dislocation. The same circuit is made in a perfect crystal and if it fails to close, the lattice vector that is needed to complete the circuit is defined as the Burgers vector of the dislocation. For an edge dislocation the Burgers vector is always perpendicular to the line vector. Hence the edge dislocations sometimes referred to as 90^0 dislocations. For screw dislocations, the Burgers vector is parallel to the line vector. There are mixed dislocations like more common 60^0 dislocations where the angle between Burgers vector and the line vector is 60^0[1]. The Burgers vector is conserved for any dislocation passing through a crystal. Any dislocation that changes the direction (angle between Burgers vector and the line

vector) changes the character. In one part of line its path, a dislocation may be a screw and then it can be an edge or 60° dislocation elsewhere along its path.

Shear stress produces dislocations and further stresses on the crystal may cause a dislocation to move by a mechanism called slip, or glide. The slip direction is the same as the Burgers vector and the slip plane is the plane containing the Burgers vector and the line vector [12]. Dislocation climb can be also happen at very high temperatures [12].

A dislocation with a Burgers vector equals to a lattice translation vector (Burgers vector connects two lattice points in the perfect crystal) is called a perfect or unit dislocation. A perfect dislocation may dissociate into two partial dislocations, but the Burgers vector is conserved in the process [1]. A special dislocation reaction occurs between dislocations with opposite Burgers vectors. The result is the annihilation of both dislocations [1].

2.2.3 Dislocations in face centered cubic (fcc) crystals

The slip planes in a crystal are usually the planes with the highest density of atoms (close packed planes) [1]. These planes have the highest separation. The usual slip planes for cubic crystals are the {111} planes and the slip direction and the Burgers vector are of the type *a/2<011>*. There are twelve distinct slip systems in a cubic semiconductor (four {111} planes with three <110> directions in each). In Appendix A, the 12 slip systems of a cubic semiconductor is shown.

Dislocations on the 12 slip systems in a cubic lattice are pure edge, pure screw or 60^0 dislocations (because line vectors are <011> type). The most common dislocation observed in heteroepitaxial zincblende semiconductors is a 60^0 dislocation [1]. These 60^0

dislocations are further classified as α and β dislocations according to the atoms at their cores [1]. For zincblende semiconductor AB, α dislocations have A atoms as cores and β dislocations have B atoms as cores. α and β dislocations have shown differences in their mobility and dissociation into partial dislocation [1].

There are two dislocations common in heteroepitaxy, namely threading dislocation and misfit dislocation. Misfit dislocations accommodate the misfit between two lattices. Misfit segments that thread up to the surface of the epilayer are called threading dislocations. In zincblende semiconductor (001) heteroepitaxy, threading dislocations glide in the epitaxial layers along {111} planes and misfit dislocations are formed along the two orthogonal <110> directions.

2.2.4 Dislocation sources and multiplication

Lattice (strain) relaxation happens through the formation of misfit dislocations. Strain relaxation through MDs in low mismatch systems are said to be different than in high mismatch systems [49]. In high mismatch systems, strain relaxation occurs through the generation of initial 3D islands growth and the introduction of a large number of immobile edge dislocations and threading dislocations. Here the MD segments are short and one can observe a large TD density after the film forms a continuous layer. In the low mismatched case, the relaxation occurs by introducing mobile 60° dislocations and the misfit dislocation introduced are very long and the threading dislocation density is low.

According to Matthews and Blakeslee [13], misfit dislocations form from the bending of pre-existing (substrate) threading dislocations. According to MacPherson *et al*. [19], Si wafers have a TD density around 10^2-10^4 cm^{-2} and GaAs wafers have TD density

around 10^3-10^4 cm^{-2} (from Sumitomo Electronics). GaAs (001) wafers used in this study are from AXT Inc. and have a TD density (or etch pit dislocation (EPD) density) around 5×10^3 cm^{-2}. These densities are much lower than the TD densities observed above the interface of substrate and the epilayer [10]. This suggests that dislocation nucleation and multiplication occurs during the heteroepitaxy.

Homogeneous nucleation of half loops *i.e.* formation of two associated threading segments from a misfit dislocation segment was proposed by J.W. Matthews *et al.* [14,15]. They calculated that a large amount of energy was involved, so that the mismatch strain should be greater than 1.5% [1]. It is assumed that heterogeneous half loops are more likely to form in heteroepitaxy [1]. This refers to the nucleation of a half loop at an existing crystal defect such as a dislocation, void, precipitate, or scratch. The nucleation of a half loop is barely observed by TEM [1].

Two dislocation multiplication mechanisms were proposed by Frank and Read [16]. They suggested the formation of dislocation loops from pre-existing dislocations. Sources of dislocation multiplication are bowing of threading dislocations anchored or pinned at one (Frank-Read source) or two points (spiral source) in the presence of an applied stress.

Another mechanism for dislocation multiplication proposed by Hagen and Strunk [17] is the interaction of two gliding dislocations with the same Burgers vectors but on different glide planes. A repulsion force between these dislocations pushes the tip of one dislocation to the surface and splits it. These mechanisms suggest that lattice relaxation can happen not only from bending of preexisting TDs but from new sources or/and multiplication of existing dislocations [1].

2.2.5 Planar defects; stacking faults and twins

A perfect crystal can be considered as a stack of atomic layers occurring in a particular sequence. In the [111] direction, the atoms of a zincblende structure are arranged as ….ABCABC…Stacking faults can be made by inserting an extra plane of atoms (extrinsic stacking fault, ..ABCBABC..) or removal of a plane of atoms (intrinsic stacking fault, ...ABCBCABC...) from the original stack of atoms. Stacking faults which are planar defects result from the dissociation of perfect dislocations into partial dislocations.

A twin is another planar defect. Its boundary in diamond or zinc blend structures can be described as …ABCABACBA.... Twinned and normal crystals share a single plane of atoms and there is reflection symmetry about the twinning plane [12]. For a zincblende structure, twinning occurs about a {111} plane. If the growth plane is along (001), the surface of the twinned crystal is $(2\bar{2}1)$ plane and the (111) twinning plane is inclined 54.7^0 to the (001) surface. Twinning degrades device performance as it penetrates through the active layer.

2.2.6 Transmission Electron Microscopy (TEM)

Characterization of defect types and densities can be done using transmission electron microscopy (TEM) [18], crystallographic etching (etch pit density) [18,19], x-ray diffraction [20], photoluminescence (PL) microscopy [21] and electron beam induced current (EBIC) microscopy [18]. TEM is the most widely used technique for the observation of dislocations, stacking faults, microtwins and other crystal defects in heteroepitaxial layers.

In TEM, electromagnetic lenses focus high energy electrons through a thinned specimen to form an image on a phosphor coated screen. Up to 10^6 overall magnification with ~ 1.2 Å resolution can be achieved from a modern (JOEL 2010 F) TEM with a 200 keV source (field emission gun). There are several contrast mechanisms (amplitude contrasts like mass thickness contrast, diffraction contrast and Z contrast (high resolution TEM) and phase contrast (high resolution TEM)) and main imaging modes (Diffraction, Bright Field and Dark Field) [22]. A schematic of a basic TEM instrument is shown in Figure 2.3 with ray paths for diffraction pattern mode and conventional imaging mode. Collimated high-energy electrons from a condenser lens are transmitted through the thinned specimen (Procedures for thinning semiconductor specimens for plan view and cross sectional view are summarized in Appendix B) where they are scattered according to Braggs law in particular directions by the crystal specimen [1]. These diffracted beams are focused by the objective lens.

In the imaging mode, the intermediate lens transforms the inverted image of the specimen formed by the objective lens [1]. An aperture at the back focal plane can be used to select one diffracted beam (with specific reciprocal vector $\boldsymbol{g}$) from the image. If $\boldsymbol{g}$ = (000) is selected a bright field image is formed, otherwise a dark field image is formed. In the diffraction mode the first intermediate lens is focused on the back focal plane of the objective lens and captures the diffraction pattern. Each spot in diffracted beam on the screen corresponds to a particular diffraction vector $\boldsymbol{g}$.

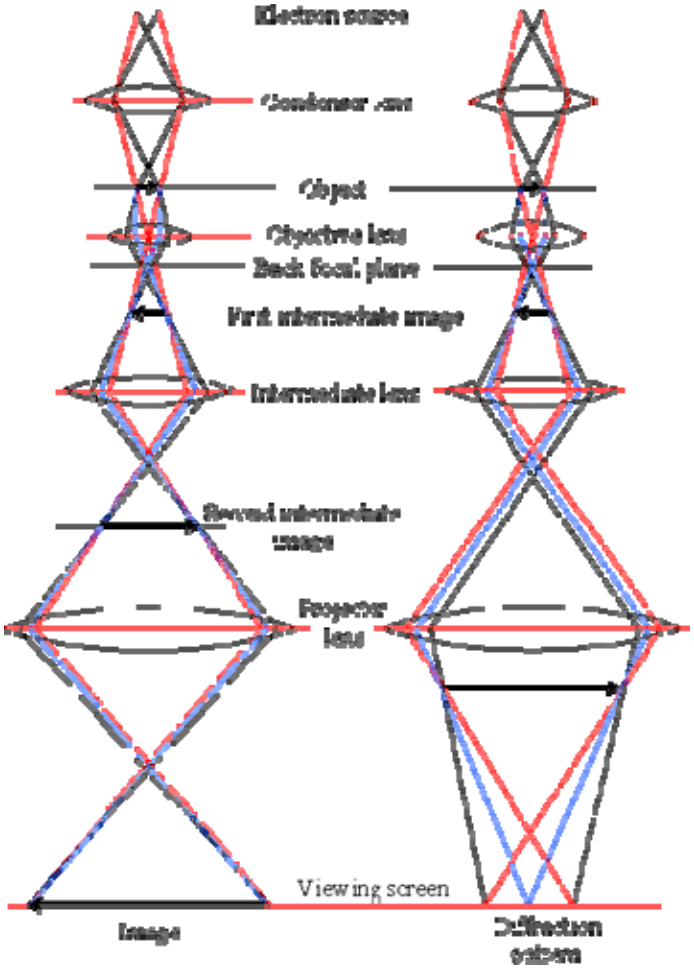


Figure 2.3 A schematic for basics of a Transmission Electron Microscope

Dislocations cause severe local distortions of the surrounding crystal [1]. It is strain in the crystal that makes the diffraction contrast of dislocations, not the core of the dislocation. The condition for image contrast by a crystal defect is $\boldsymbol{g.u} \neq 0$, where $\boldsymbol{u}$ is the vector by which each atom is displaced from its normal site. If $\boldsymbol{g.u} = 0$, there is no diffraction contrast originating from displacement $\boldsymbol{u}$. In practice, the magnitude of $\boldsymbol{g.u}$ should be sufficiently large to change the local intensity from the background intensity by at least by 10%. The rule of thumb is if $|\boldsymbol{g.u}| \leq 1/3$, there is no contrast associated with $\boldsymbol{u}$ [22]. This invisibility criterion can be applied to determine the Burgers vector of edge

and screw dislocations. If the Burgers vector is perpendicular to the active diffraction vector there is no contrast for that dislocation ($\boldsymbol{g.b} = 0$). For mixed dislocations there is no condition for which $\boldsymbol{g.u} = 0$ [1]. There will be a weak contrast even when $\boldsymbol{g.b} = 0$. If a dislocation is invisible or nearly invisible for two diffraction vectors (say $\boldsymbol{g_1}$ and $\boldsymbol{g_2}$), then the Burgers vector is perpendicular to both diffraction vectors and in the direction $\boldsymbol{g_1} \times \boldsymbol{g_2}$.

2.3 Buffer layer as threading dislocation filter

2.3.1 Review of buffer layer approaches

Buffer layers can be used to control the amount of misfit relief to match the lattice constant of the subsequent device layer structure, to control the threading dislocation density or both.

The simplest buffer layer has a uniform composition. The buffer layer in low misfit systems relaxes the misfit very slowly and needs to be very thick for complete lattice relaxation. It is found that the threading dislocation density increases as film thickness increases for low misfit systems [2]. This suggests that in planar growth modes misfit dislocations are short due to dislocation blocking [2]. On the other hand, in high misfit systems the threading dislocation density is inversely proportional to the layer thickness. In this system, misfit relief occurs in a relatively thin layer [1,2]. As the layer thickness increases, threading dislocations can react with each other through coalescence and annihilation. Coalescence refers to a reaction between two threading dislocations having different Burgers vectors [1]. The end result is a single TD created out of two TDs. Annihilation refers to the reaction of two dislocations having anti-parallel Burgers vectors [1]. The end result is removal of both TDs. Both processes occur during the

growth or subsequent thermal processing. It is found that post growth annealing further reduces the TD density to some extent [1]. TD density reduction by a thick uniform buffer layer was observed experimentally in different heteroepitaxial systems such as InAs/GaAs [23], GaAs/Ge/Si [23], GaAs/InP [23], InAs/InP[23], GaAs/Si[24] and ZnSe/GaAs[25,26]. However, a theoretical glide model found that a reasonably low TD density (~$10^7 cm^{-2}$) requires about 100μm of buffer layer [27,28]. A 1 μm thick buffer layer has $10^9 cm^{-2}$ TD density [27, 28]. Thicker layers may undergo cracking due to the difference in thermal expansions [29].

It is greatly beneficial for a device structure to have a thinner buffer layer with a low defect density. The linearly graded buffer layer is one method for achieving a lower defect density at the surface of a thin buffer. In this technique the composition (and consequently the lattice constant) is varied linearly during the growth. This method is currently applied in the fabrication of commercial devices such as $GaAs_{1-x}P_x$ light emitting diodes (LEDs) and $In_xGa_{1-x}As$ high electron mobility transistors (HEMTs) on GaAs substrates [1,2]. A graded buffer is studied in systems such as $GaAs_{1-x}P_x$/GaAs [30], $In_xGa_{1-x}As$/GaAs [31], Si_xGe/Si [32] and $In_xGa_{1-x}P$/GaP [32]. It is observed theoretically and experimentally that the threading dislocation density is proportional to the grading coefficient (change of mismatch with distance) and the growth rate. The TD density also depends on the growth temperature and final composition. The linearly graded buffers have achieved low dislocation densities around 10^5 to 10^6 cm^{-2}. A step graded buffer is another approach, but linear grading showed the most relaxation [33].

The strained layer superlattice (SLS) is the most studied defect filtering buffer layer. A SLS buffer has alternate layers with mismatch strain of opposite signs. The SLS

as a defect filtering buffer is studied intensively in the GaAs on Si system. Different super-lattices were used such as $GaAs_{0.5}P_{0.5}$/GaAs [34], $Ga_{0.9}In_{0.1}As$/GaAs [35], $(GaAs)_{0.8}(Si_2)_{0.2}$/GaAs [36] and $GaAs_{1-y}P_y/In_xGa_{1-x}As$ [37] to achieve a low (10^5-$10^6 cm^{-2}$) defect density. Similar results were observed in GaSb on GaAs using a GaSb/AlSb superlattice [38]. It is also observed that multiple superlattices are effective in high misfit systems. The SLS technique is not useful for reducing defects in II-VI mismatch systems and GaN on sapphire and Si (111) [1]. A SLS buffer is generally effective for zincblende semiconductor mismatch heteroepitaxy.

Another relatively simple (compared to SLS and graded buffer) yet effective method for reducing dislocations in mismatch heteroepitaxy is insertion of a single or a series of interlayers (or intermediate layers) to the matrix buffer. Low-temperature interlayer growth has shown improved crystaline quality in the GaN, AlN and AlGaN on sapphire systems by reducing the TD density [50]. Takano *et al*. reported a reduction of TDs by using InGaAs interlayers in GaAs layers grown on a 2^0 off-cut Si(100) substrate [54]. They observed a low TD density of 1.2×10^6 cm^{-2} by inserting an $In_xGa_{1-x}As$ interlayer with x=0.09. Our study of the effect of interlayer interfaces on reducing defects in the InSb/GaAs system will be discussed in next sections.

2.3.2 Defect reducing buffer layers for the $Al_xIn_{1-x}Sb$/GaAs (001) system

In our study, an interlayer buffer is intensively studied as a mean of dislocation filtering in $Al_xIn_{1-x}Sb$/GaAs(001) growth for low-defect InSb QW structures. Different types of buffer layers were engineered to minimize the defect density near the InSb QW. Table 2.1 summarizes the MT and TD densities at an InSb QW grown on four different

buffer layers. MT and TD densities were deduced using plan view TEM images. The buffer layer consisted of a 1μm AlSb or InSb nucleation layer, 1μm $Al_{0.09}In_{0.91}Sb$ layer, 50-300nm intermediate layer and a 2μm $Al_{0.09}In_{0.91}Sb$ layer. The intermediate layer's structure is either an $Al_{0.09}In_{0.91}Sb$/InSb SLS, an InSb interlayer or an $Al_{0.18}In_{0.82}Sb$ interlayer. The results show that an AlSb nucleation layer is more effective in reducing the micro-twin density than an InSb nucleation layer. It is also observed that InSb and $Al_{0.09}In_{0.91}Sb$ interlayers are more effective in reducing the threading dislocation density than the SLS. The lowest micro-twin (1×10^3/cm) and dislocation (2×10^8 cm^{-2}) densities were observed in wafer C which includes the AlSb nucleation layer and InSb interlayer. Wafer D which has the same nucleation layer as wafer C and an $Al_{0.18}In_{0.82}Sb$ interlayer also showed low defect densities ($1\times10^3 cm^{-1}$ for micro-twin density and 3×10^8 cm^{-2} for dislocation density).

Wafer	Nucleation layer	Intermediate layer	Micro Twin density (cm^{-1})	Dislocation density (cm^{-2})
A	InSb	9%AlInSb/InSb SLS	20×10^3	9×10^8
B	AlSb	9%AlInSb/InSb SLS	3×10^3	4×10^8
C	AlSb	InSb Interlayer	1×10^3	2×10^8
D	AlSb	18% AlInSb Interlayer	1×10^3	3×10^8

Table 2.1 Micro-twin and threading dislocation densities at the InSb QW of four wafers with different buffer layer structures. The total thickness of the buffer layer of each wafer is ~ 4 μm.

Although an AlSb nucleation layer is observed to be very effective in reducing the micro-twin density in an $Al_xIn_{1-x}Sb$ layer, there is a drawback for device applications. If the AlSb layer is exposed after mesa etching, it oxidizes more readily than InSb or Al_xIn_{1-}

$_x$Sb. An alternative method for micro-twin density reduction is the use of an off-cut substrate and is discussed in Section 2.4.

2.3.3 Threading dislocation filtering effect of $Al_xIn_{1-x}Sb/Al_yIn_{1-y}Sb$ interfaces

We investigated the TD filtering effect of $Al_xIn_{1-x}Sb/Al_yIn_{1-y}Sb$ interfaces formed by interlayer structures with a wide range of alloy composition, interlayer thickness and pre-existing TD density. Cross-sectional TEM analyses of tilted specimens and non-tilted specimens were used to evaluate the TD densities around the interfaces. Figure 2.4 shows a dark-field (DF) XTEM image of a 360nm $Al_{0.18}In_{0.82}Sb$ interlayer grown in a 3μm $Al_{0.09}In_{0.81}Sb$ matrix layer. Figure 2.5 (a) shows a XTEM image of the non-tilted specimen and Figure 2.5 (b) shows a XTEM image of a specimen tilted 31° toward the horizontal [110] axis. For a better understanding of the XTEM image, a schematic illustrations of the side view of the specimen and the front view of its e-beam projection are showed in Figure 2.5 (c) and (d).

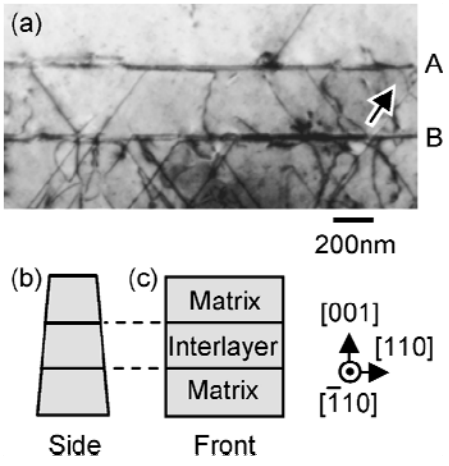


Figure 2.4 (a) XTEM image of an $Al_xIn_{1-x}Sb/Al_yIn_{1-y}Sb$ interlayer structure taken under dark-field conditions with the 220 reflection. The positions of the interlayer interfaces are indicated by A and B. A representative threading dislocation bent at the interface is indicated by an arrow.

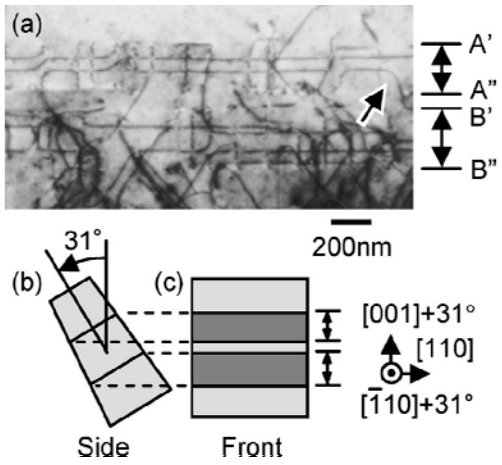


Figure 2.5 (a) XTEM image taken from the specimen tilted by 31^0 about the horizontal [110] axis as schematically viewed in the side (b) and front (c) views. A 220 dark-filed condition was used to take this image. The positions of the upper and lower interfaces are indicated by A'-A'' and B'-B'' in the image

In both non-tilted and tilted specimen images, the propagation of TDs towards the surface appears to cease at the interfaces. In Figure 2.5(a), there are vertical and horizontal dark contrasts which are identified as MDs along [110] and [$\bar{1}$10] located at the interfaces. In both XTEM images it can be clearly observed that some of the TDs are bent to make a MD segment at an interface and an example is indicated in Figures 2.4(a) and 2.5(a) by an arrow. More detailed analysis of bending of TDs will be discussed in the next section. In tilted XTEM image most of the vertical MDs are truncated at the same vertical positions *A'-A''* and *B'-B'',* indicating that [$\bar{1}$10] MDs are truncated at the front and back surfaces of the XTEM specimen. This length (l) can be used to calculate the thickness of the specimen (t) by knowing the specimen tilt angle (θ) where $t=l/Sin\theta$. The number of TDs (N) was counted above and below the interfaces and the areal density can be calculated as N/wt where w is the image width. TD areal densities of different

structures with different Al concentrations (x = 0-0.36 and y= 0-0.24), interlayer thicknesses (160-360nm or 6.3-12.6 times greater than the Matthews and Blakeslee critical thickness, h_c) and pre-existing TD densities in the interlayer or lower matrix layer, are calculated using the above method. The Al composition is higher in the interlayer than in the matrix layer for wafers 1-6 and vice versa for wafers 7 and 8. Wafers 2 and 7 are grown via GaSb/AlSb/GaAs buffer layers. The results are summarized in Table 2.2. Regardless of the different parameters for the buffer, it is observed that all the interfaces reduced the TD density. The upper interface of wafer 1 in which InSb was used as matrix layer material shows the highest TD reduction (69%). The next highest TD density reduction is observed in the upper interface of an InSb interlayer structure with an $Al_{0.09}In_{0.91}Sb$ matrix (wafer 7). Among the buffer structures with an $Al_xIn_{1-x}Sb/Al_yIn_{1-y}Sb$ interfaces (2-6 and 8) the lower interface of wafer 8 exhibits the highest TD reduction rate (59%).

	Material		Strain	Thickness		TD density (× 10^9 /cm^2)		TD density reduction (%)	
	Interlayer	Matrix		(nm)	(× h_c)	Upper interface Above / Below	Lower interface Above / Below	Upper interface	Lower interface
1	9%AlInSb	**InSb**	Compressive	180	**6.3**	0.56 / 1.8	1.9 / 4.2	**69**	55
2	18%AlInSb	9%AlInSb	Compressive	**360**	**12.6**	0.50 / 0.91	0.91 / **1.9**	45	52
3	24%AlInSb	12%AlInSb	Compressive	**160**	8.0	3.3 / 6.3	6.3 / 9.7	48	35
4	24%AlInSb	12%AlInSb	Compressive	**160**	8.0	1.4 / 2.0	2.1 / 3.0	30	30
5	24%AlInSb	12%AlInSb	Compressive	**160**	8.0	0.71 / 1.1	1.1 / 1.4	33	23
6	**36%AlInSb**	**24%AlInSb**	Compressive	240	12.0	4.6 / 8.4	9.3 / **13**	45	28
7	**InSb**	9%AlInSb	Tensile	200	7.0	0.86 / 2.4	2.5 / 4.5	64	44
8	12%AlInSb	**24%AlInSb**	Tensile	240	12.0	1.3 / 1.9	1.9 / 4.6	32	**59**

Table 2.2 TD densities and their reduction rates at the interfaces between the AlInSb interlayers and AlInSb matrix layers.

A triple interlayer and a series of non-interlayer structures with different thicknesses were grown. The TD densities were calculated using the XTEM technique as described above for the interlayer structure and using conventional plan-view TEM in non-interlayer structures. In Figure 2.6, the TD densities around the interlayers and the top most surfaces of the non-interlayer wafers are plotted as a function of the layer thickness. The interlayer structure has three periods of a 240nm $Al_{0.12}In_{0.88}Sb$ matrix layer and 160nm $Al_{0.24}In_{0.88}Sb$ interlayer (8 times the Matthews-Blakeslee critical thickness) grown directly on a GaAs(001) substrate, capped with a 400nm $Al_{0.12}In_{0.88}Sb$ layer. Each of five non-interlayer wafers has an $Al_{0.12}In_{0.88}Sb$ matrix layer directly grown on a GaAs (001) substrate. The TD densities of non-interlayer wafers decrease as the thickness increases. In the interlayer wafer, the TD density decreases more rapidly because of TD filtering by the six $Al_{0.12}In_{0.88}Sb/Al_{0.24}In_{0.76}Sb$ interfaces. A TD density of a 2.9μm thick non-interlayer wafer is 9.5×10^{8} cm^{-2}. The TD density of a 1.6μm interlayer structure is 6.0×10^{8} cm^{-2}. The 45% thinner interlayer structure has a 37% lower TD density than a 2.9 μm non-interlayer wafer.

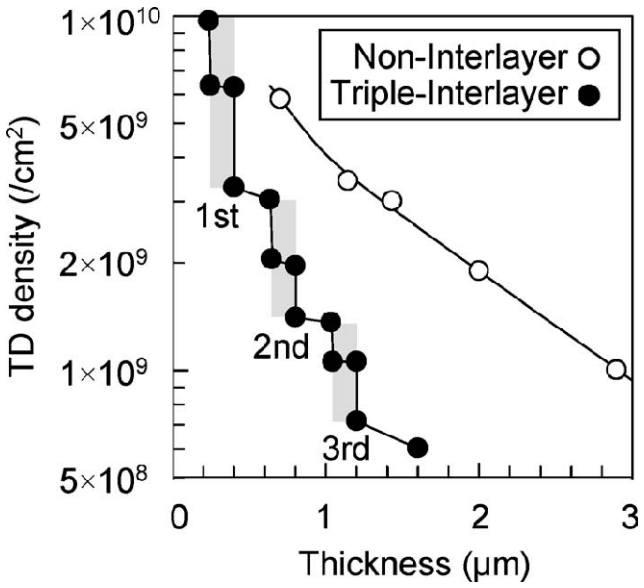


Figure 2.6 TD densities in an $Al_{0.24}In_{0.76}Sb/Al_{0.12}In_{0.88}Sb$ triple interlayer structure (filled circles) and series of non interlayer wafers (open circles) as functions of layer thickness. The gray rectangles highlight the positions of the three interlayers.

2.3.4 Effect of Al composition on filtering of threading dislocations

In most of the samples discussed above, the Al composition difference between the interlayer and matrix layer is 10%. In this section we study the effect of the interlayer's Al composition on defect reduction. Figure 2.7 shows a schematic illustration of the buffer layer structure for a series of samples. For all of the samples, a 0.5μm-thick $Al_{0.10}In_{0.90}Sb$ lower matrix layer was grown on the GaAs (001) substrate before growth of the first interlayer. Then a 0.2μm-thick first interlayer was grown, followed by a 0.3μm-thick intermediate matrix layer. Next, a 0.2μm-thick second interlayer was grown followed by 0.3μm-thick upper matrix layer. The Al composition of the matrix layer is 0.10 and the Al composition of the interlayers was 0.10, 0.15, 0.20, 0.25 or 0.30. Note that a 10% interlayer means that there was no interlayer. Using plan-view TEM imaging,

the threading dislocation density above the upper interface of the second interlayer was determined.

Figure 2.7 Schematic diagram of a layer structure of 1.5 µm total thickness and with two interlayers. The value of x was 0.10, 0.15, 0.20, 0.25 and 0.30 for different structures.

Figure 2.8(a) shows a representative plan-view TEM image of the structure with $Al_{0.25}In_{0.75}Sb$ interlayers. To get a clear understanding of the TEM image, two schematic diagrams of ion-milled specimens are shown in Figures 2.8(b) and (c). The TEM image was taken from the area that includes the edge of the interface between the upper matrix and second interlayer, which is indicated by arrows. This edge is formed by the thinning process of the TEM specimen, as illustrated in Figure 2.8(b). The curved edge line of the TEM image can be explained by a semi-spherical shape of removed material due to the ion milling process, as schematically shown in Figure 2.8(c).

In region A of Figures 2.8 (b) and (c), only the upper matrix can be viewed by TEM. On the other hand, the upper matrix, part of the second interlayer and their interface can be imaged in region B.

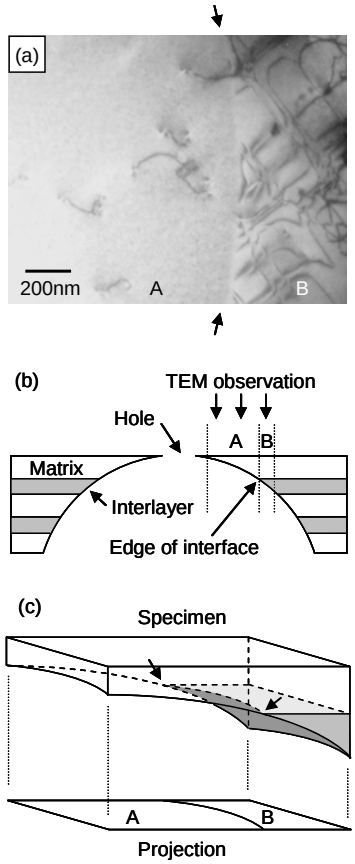


Figure 2.8 (a) Plan-view TEM image of region A (the $Al_{0.10}In_{0.90}Sb$ upper matrix layer and region B (the matrix layer, the $Al_{0.25}In_{0.75}Sb$ second interlayer and their interface). The edge of the interface is indicated by arrows. (b) Cross-sectional illustration of a TEM specimen, which shows the layers and interfaces contained in regions A and B. (c) Three dimensional schematic representation of a TEM specimen. The curved edge of the interface in (a) can be explained by a section between a sphere (part of material removed by ion milling) and plane (interface).

In region A of the TEM image, dark line contrasts, most of which are located independently, can be seen. They are interpreted as TDs propagating in the upper matrix layer. In region B of the image, however, a larger number of dark line contrasts, which preferentially align along the <110> directions, are visible. They are interpreted as misfit dislocations (MDs) located at the interface between the matrix and interlayer [8,56].

Previous TEM studies have reported that the formation of MDs at $Al_xIn_{1-x}Sb/Al_yIn_{1-y}Sb$ interfaces is an important process for the TD density reduction in this system [8,56]. In order to assess the effect of $Al_xIn_{1-x}Sb$ interlayers on TD density reduction, TDs in a total of 267 μm^2 of region A -type areas of the specimens is examined.

Figure 2.9 shows the TD density at the upper matrix layer of five structures with different Al compositions for the interlayers. The structure with no interlayers shows the highest TD density, $1.8\times10^9 cm^{-2}$. All the interlayer structures have a lower TD density compared to the non-interlayer structure. The TD density decreased as the Al composition of the interlayers is increased up to x=0.25. In contrast, the structure with x=0.30 shows a larger TD density than structures with x=0.20 or 0.25 but a lower TD density than the structure with x=0.15. The lowest TD density, which is $7.5\times10^8 cm^{-2}$, is observed in the structure with x=0.25. This structure has a TD density that is 59% of the TD density for the non-interlayer structure.

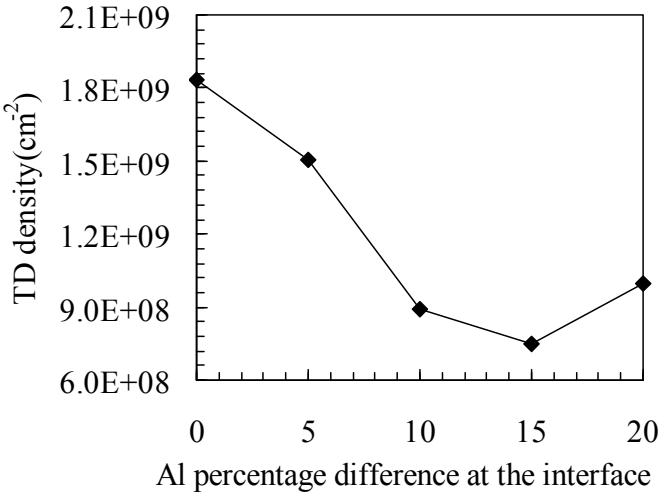


Figure 2.9 Threading dislocation density versus Al composition difference between the matrix layer and the interlayers.

A similar effect was observed in an $In_xGa_{1-x}As$ interlayer in the GaAs matrix layer [54]. The lowest defect density is observed when the In composition is 9% [54].

These experimental observations suggest that the control of the strain at the interface is an important parameter for dislocation filtering mechanisms that occur at the interfaces.

2.3.5 Interface study for threading dislocation evaluation

In this section, possible TD filtering mechanisms at $Al_xIn_{1-x}Sb/Al_yIn_{1-y}Sb$ interfaces are discussed. As discussed in Section 3.8.1, bending of a TD to form a MD can be observed in XTEM images. Higher resolution XTEM images of a buffer layer with a 160nm $Al_{0.24}In_{0.76}Sb$ interlayer grown between 240nm $Al_{0.12}In_{0.88}Sb$ matrix layers were further investigated to evaluate the behavior of dislocations at the interlayer interface.

Figure 2.10(a) is taken from near the $[\bar{1}10]$ direction with an operative reflection of $\boldsymbol{g}$ = 220. The dislocation A undergoes a TD-MD transformation at the interface. Dislocation B and C are used as position markers. A XTEM image of the same specimen with a 22^0 tilt about horizontal direction [110] is shown in Figure 2.10(b). Three perpendicular MDs (a, b and c) are clearly observed. Although the contrasts around the crossings are somewhat obscured due to the zigzag contrasts (due to the inclination of the MDs with respect to the electron beam direction [56]) an obvious splitting at the crossing of dislocations A and b can be observed.

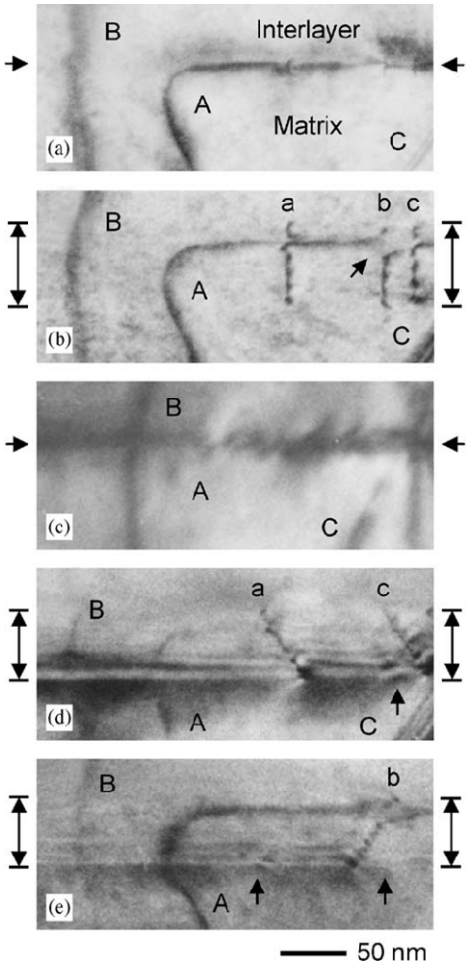


Figure 2.10 XTEM images taken (a) from near $[\bar{1}10]$ with g=220, (b) from 22^0 about [110] with g =220, (c) from near [010] with g=202, (d) from 20^0 about [110] and 12^0 about [001] with g=111, and (e) from 20^0 about [110] and -12^0 about [001] with g=$\bar{1}\bar{1}1$. The positions of dislocations B and C are used as position markers.

An invisibility criterion technique (discussed in Section 2.2.6) was performed to identify the dislocations A, a, b and c. Figure 2.10(c) and (d) shows XTEM images taken with **g** = 202 and **g** = 111. In Figure 2.10(c) faint residual contrast of dislocation *a* is seen and in Figure 2.10(d), part of dislocation A shows a broad residual contrast. By applying invisibility criterion, the Burgers vector of dislocation A is calculated as $\pm\, a/2[10\bar{1}]$,

where *a* is a cubic lattice constant. Therefore this dislocation is either a perfect dislocation or a narrowly dissociated pair of 30^0 and 90^0 partial dislocations. The MD segment of dislocation A is identified as a 60^0 perfect MD because of the angle between A ([110]) and **b** ($\pm a/2\ [10\bar{1}]$).

In Figure 2.10(d) the specimen is tilted 20^0 about the [110] direction and 12^0 about the [001] direction, MDs are observed as right-down tilted lines compared to Figure 2.10(b). In Figure 2.10(d) dislocation b almost loses its contrast in the X-TEM image taken with **g**=111. This indicates that dislocation *b* is a 60^0 perfect MD in the $[\bar{1}10]$ direction with either **b**= $\pm a/2[10\bar{1}]$ or $\pm a/2[01\bar{1}]$. In Figure 2.10(b), a splitting between dislocations A and b is observed. *i.e*. Burgers vectors of dislocation A and b are parallel to each other. Therefore, the Burgers vector of dislocation *b* should be $\pm a/2[10\bar{1}]$. Figure 2.10(e) shows a XTEM image taken with $\mathbf{g}=\bar{1}\bar{1}1$. The specimen tilt angles are 20^0 and -12^0 about the [110] and [001] directions, respectively, making $[\bar{1}10]$ MD contrasts in the image right-up tilted lines. Dislocations a and c are invisible in Figure 2.10(e) and that implies these dislocations are $[\bar{1}10]$ directional 60^0 perfect MDs with $\mathbf{b}=\pm a/2[101]$ or $\pm a/2[011]$.

2.3.5.1 Dislocation filtering mechanisms

Possible dislocation filtering mechanisms in fcc semiconductor heteroepitaxy were proposed by A.E. Romanov *et al*. [57]. Schematic illustrattions of different possible interactions between dislocations at the interface of a matrix layer and an interlayer are shown in Figure 2.11. Figure 2.11(a) shows that a TD experiences zero force and does

not bend at the interlayer interface (a similar situation occurs when the interlayer thickness is less than critical thickness). Figure 2.11(b) shows the bending or jogging of a dislocation that does not reduce the dislocation density. This may happen when interlayer thickness is equal to critical layer thickness. A dislocation can bend over completely and be removed by gliding all the way to the wafer edge as shown in Figure 2.11(c). Dislocations with opposite Burgers vectors may react (annihilate) as shown in Figure 2.11(d), resulting in a removal of two TDs. Finally, two dislocations can react to form a third dislocation resulting removal of one dislocation as schematically shown in Figure 2.11(e).

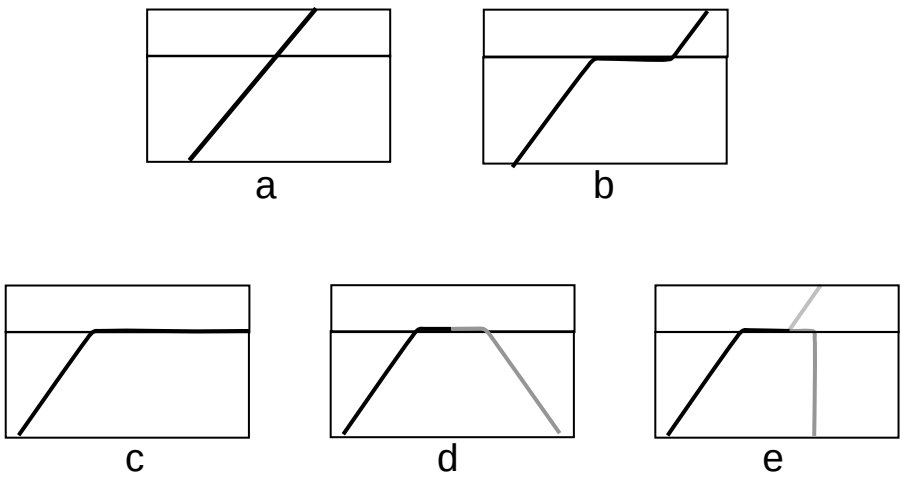


Figure 2.11 Five possible interactions between dislocations in an interlayer buffer. (a) No interaction, either the interlayer thickness is less than the critical thickness or no force acting on the TD. (b) Bending of a dislocation when the interlayer thickness is equal or greater than the critical thickness. (c) A dislocation can bend over and glide all the way to the sample edge. (d) Dislocations with opposite Burgers vectors can react and annihilate. (e) Two dislocations react to form a third dislocation (coalescence).

Experimental evidence of reactions a and b is observed in the TEM images of Figure 2.10 (a)-(e). In spite of disturbances of other orthogonal MDs, elongation of the MD segment of dislocation A is observed. This indicates possible longer MDs at the $Al_xIn_{1-x}Sb/Al_yIn_{1-y}Sb$ interface. The probability for the above TD filtering reaction mechanisms to occur (Figure 2.11 (c), (d) and (e)) is high when the MD segments are longer.

2.4 Electron mobility in InSb QW grown on interlayer buffer

The main purpose of introducing $Al_yIn_{1-y}Sb$ interlayers in an $Al_xIn_{1-x}Sb$ matrix layer is to obtain a low defect, thinner, buffer layer on which an InSb QW structure is grown. The ultimate goal is a high electron mobility in the InSb QW. Improvement of the electron mobility by reducing the TD density in the buffer layer is illustrated in Figure 2.12. InSb QW structures were grown on a 1.5μm thick $Al_{0.1}In_{0.9}Sb$ constant composition (non-interlayer) buffer (t151) or a 1.5μm thick double interlayer buffer (t145). The layer sequence of the double interlayer buffer is 0.5μm thick $Al_{0.1}In_{0.9}Sb$ matrix layer, 0.2μm thick $Al_{0.25}In_{0.75}Sb$ interlayer, 0.3μm thick $Al_{0.1}In_{0.9}Sb$ matrix layer, 0.2 μm thick $Al_{0.25}In_{0.75}Sb$ interlayer and 0.3 μm thick $Al_{0.1}In_{0.9}Sb$ matrix layer.

The room temperature electron mobility (density) in the QW structure without non interlayer or with an interlayer is 30,400 cm^2/Vs (6.3×10^{11} cm^{-2}) or 31,400 cm^2/Vs (6.5×10^{11} cm^{-2}) respectively. At 65K, the electron mobility (density) is 61,500 cm^2/Vs (5.3×10^{11} cm^{-2}) and 75,800 cm^2/Vs (5.5×10^{11} cm^{-2}) for structures without and with interlayers respectively. At 65K, the InSb QW grown on an interlayer buffer showed a ~23% higher electron mobility. At room temperature the electron mobility is not as sensitive to the TD density, presumably due to the increased importance of phonon

scattering. Further improvement of electron mobility by reducing the micro-twin density in the InSb QW structures will discuss in Section 2.5.

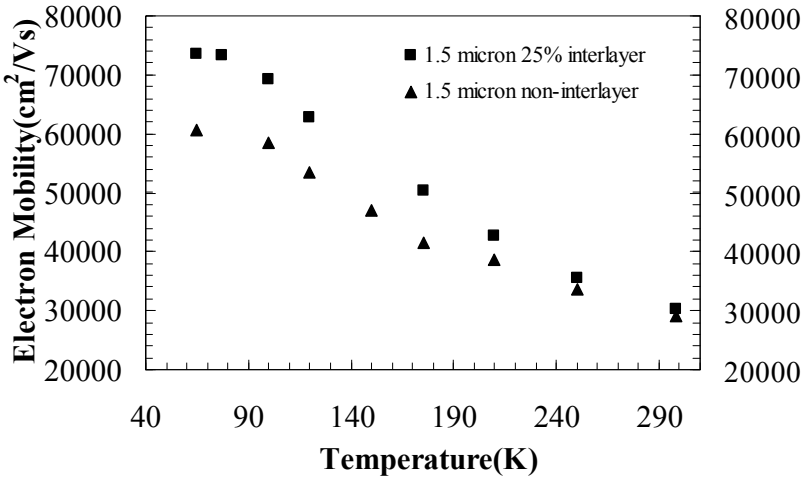


Figure 2.12 Electron mobility versus temperature of InSb QWs grown on a 1.5μm thick $Al_{0.1}In_{0.9}Sb$ buffer layer without an interlayer or with an $Al_{0.25}In_{0.75}Sb$ double interlayer.

An attempt has been made to observe the effect of the position of the first interlayer on the electron mobility. Several 1.5μm thick single interlayer structures (20 nm thick $Al_{0.2}In_{0.8}Sb$ interlayer) were grown with different positions of the inter-layer, such as 0.3, 0.5, 0.65 and 1 μm above the GaAs (001) 2° off-cut towards <110> substrate. Figure 2.13 shows the electron mobility of the InSb QWs. For clarity, the room temperature (298K) and low temperature (20K) electron mobility are shown using different scales. Higher electron mobilities are observed compared to the data in Figure 2.12 due to the use of off-axis substrates. Growth on off-cut substrates will be discussed in the next section. The dependence of the electron mobility on the interlayer position is similar at room temperature and low temperature. The electron mobility gradually increased with increasing distance of the inter-layer from the substrate surface until

0.65µm. The electron mobilities of the InSb QW when the interlayer is positioned at 0.65µm above the substrate surface are 38,400 cm^2/Vs (4.4×10^{11} cm^{-2}) at room temperature and 106,000 cm^2/Vs (3.5×10^{11} cm^{-2}) at 20 K. The QW structure with the interlayer positioned 1µm above the substrate showed the lowest electron mobility. The interlayer thickness of the structures plotted in Figure 2.13 is 200nm. In the highest mobility buffer structure, the thickness of the interlayer is reduced to 100nm. Then the electron mobility at both room temperature and low temperature was reduced to the lowest values among all the structures. These results suggest that pre-existing TD density is important for defect filtering from interlayers, and that control of the strain relaxation is an important parameter for defect filtering.

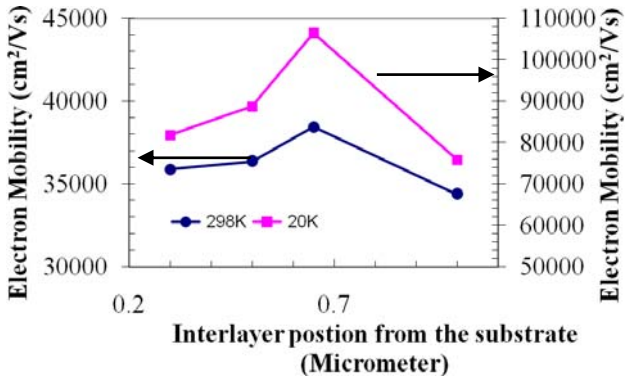


Figure 2.13 Electron mobility of InSb QWs grown on a single interlayer buffer as a function of the distance of the interlayer from the substrate surface. For clarity, the primary y-axis is used for 298K data and secondary y-axis is used for 20K data.

2.5 Micro twins in the highly mismatched InSb-GaAs system.

Another type of structural defect that reduces the electron mobility in an InSb QW grown on a GaAs(001) substrate is a planar defect called a micro-twin (MT). It is observed that a MT passing through an InSb QW can cause a structural offset and bending in the QW [39, 40, 41, 42]. Also it is evident that there is anisotropy in the MT

density and the electron mobility along <110> and $<\bar{1}10>$ directions [43]. The electron mobility along the $[\bar{1}10]$ direction is higher than along the [110] direction due to the preferential alignment of MTs along the [110] direction [43]. Growth of an AlSb nucleation layer on a GaAs substrate prior to the $Al_xIn_{1-x}Sb$ buffer layer was effective in reducing MTs. A drawback of using an AlSb layer in InSb QWs structures for device applications is possible increased oxidization during device processing. InSb QW growth on a vicinal GaAs (001) substrate (2^0 off-cut along a <110> direction) is also found to be very effective in reducing the defect density of MTs.

2.5.1 Growth on vicinal GaAs (001) substrate.

The use of vicinal substrates for semiconductor growth is reported for several heteroepitaxial systems such as AlGaAs/GaAs(001)[44], InGaAs/GaP(001) [45], ZnSe/GaAs(001)[46], ZnSe/Ge(001) [47,48] and GaAs/Si(001) [45]. Many of these materials systems exhibit a crystallographic tilt of the deposited semiconductor layers with respect to the substrate. *i.e.* terraces in the grown layer are tilted with respect to the step surface. A tilt was observed in pseudomorphic growth as well as in partially relaxed heteroepitaxial layers. For pseudomorphic layers the tilt is positive (away from the substrate normal) if the lattice constant of the substrate is larger than the epilayer and vice versa [1]. In partially relaxed layers it is observed to be opposite [1]. It is believed that both the steps at the interface and the misfit dislocations contribute to the crystallographic tilt. It is shown that an imbalance of the dislocation population in different slip planes may cause the tilt [1]. Another consequence observed in heteroepitaxial layers (especially in low mismatched systems) grown on a vicinal substrate is non-parallel misfit

dislocations at the interface and lower dislocation pile up densities. A low pile density results in less surface roughness for growth on vicinal substrates. This effect is observed in low misfit systems such as $In_xGa_{1-x}As/GaAs$ (x=0.1 and x=0.2) [51] and Ge/SiGe/Si [52].

In the InSb/GaAs system we observe another consequence of vicinal substrate growth; reduced micro-twin density in an $Al_xIn_{1-x}Sb$ buffer layer directly grown on GaAs (001) 2^0 off-cut towards a <110> direction compared to the MT density in an $Al_xIn_{1-x}Sb$ buffer directly grown on an on-axis GaAs (001) substrate. The average MT density of several InSb QW structures grown on off-axis and on-axis GaAs (001) substrates is 9.8×10^2 cm^{-1} and 7.6×10^3 cm^{-1}, respectively. The introduction of an off-axis substrate has reduced the MTs density by ~ 87%. According to Table 2.1, InSb QW structures grown on an $Al_{0.09}In_{0.91}Sb$ buffer following an AlSb nucleation layer on an on-axis GaAs substrate showed a MT density of 3×10^3 cm^{-1}. This micro-twin density is lower than in InSb QW grown on an $Al_{0.1}In_{0.9}Sb$ buffer directly grown on an on-axis GaAs (001) but higher than in an InSb QW grown on an $Al_{0.1}In_{0.9}Sb$ buffer directly grown on an off-axis GaAs(001) substrate. InSb QWs grown on off-axis substrates have a TD density of $\sim1\times10^9$ cm^{-2}. The TD density is not improved by using an off-axis substrate.

Our observation of improved electron mobility by introducing an off-axis substrate is shown in Figure 2.14. The electron density is plotted in Figure 2.15. The buffer layer in both structures is a 1.2 μm thick $Al_{0.1}In_{0.9}Sb$ layer. The QW layers and doping density are the same for both structures. The room temperature electron mobility (density) of the two QWs grown on on-axis (t081) and off- axis (t091) GaAs (001)

substrates is 24,700 cm^2/Vs (4.5×10^{11} cm^{-2}) and 29,300 cm^2/Vs (4.9×10^{11} cm^{-2}), respectively. The electron mobility (density) at low temperature (65K) is 37,200 cm^2/Vs (3.3×10^{11} cm^{-2}) and 51,600 cm^2/Vs (3.8×10^{11} cm^{-2}), respectively. Room temperature and 65K electron mobility improvements due to the growth on 2^0 off GaAs (001) are 18% and 39%, respectively.

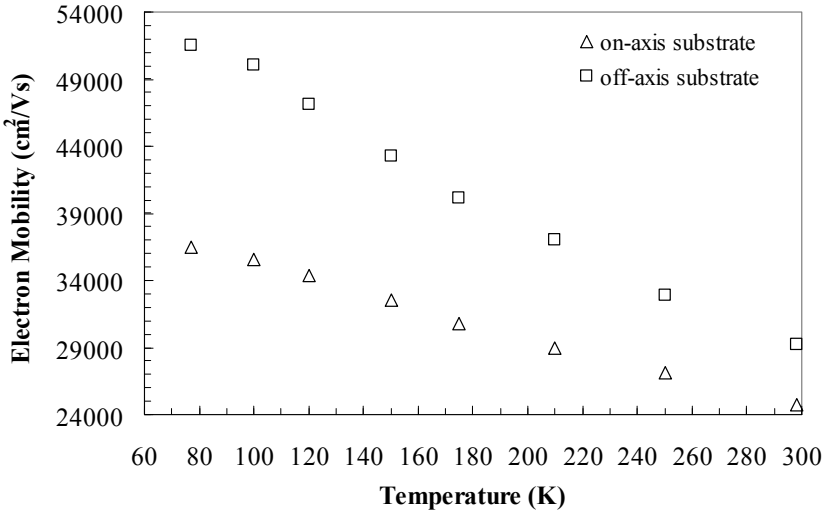


Figure 2.14 Electron mobility versus temperature of InSb QW structures grown on on-axis and off-axis (2^0 off towards <110>) GaAs (001) substrates.

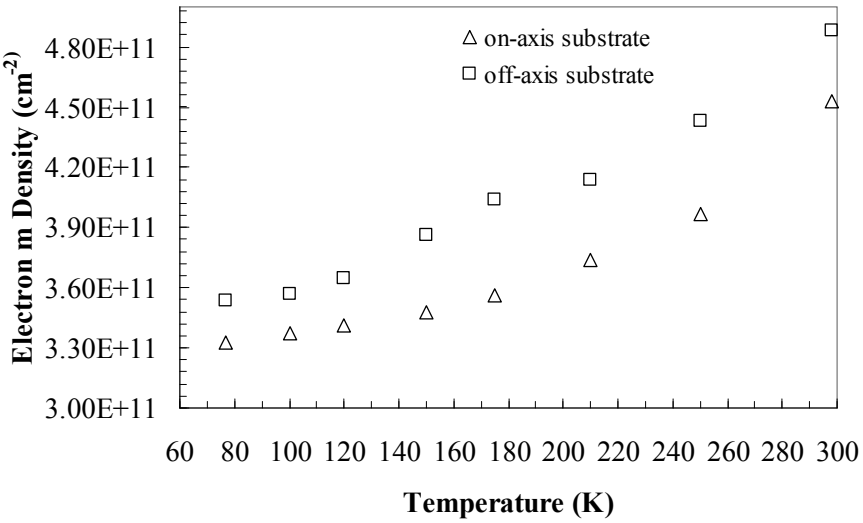


Figure 2.15 Electron density versus temperature of InSb QW structures grown on on-axis and off-axis (2^0 off towards <110>) GaAs (001) substrates.

Chapter 3

High Quality InSb Quantum Well Heterostructures Grown on 2^0 off-cut GaAs(001)

3.1 Introduction

In Chapter 2, buffer layer optimization for growth of QW structures was discussed. This chapter is devoted to engineering high mobility InSb/AlInSb QW heterostructures to grow on a relaxed, nearly lattice matched $Al_xIn_{1-x}Sb$ buffer layer (the template).

Well developed QW systems like GaAs-AlAs [1] on a GaAs substrate and $In_{0.53}Ga_{0.47}As$-$In_{0.52}Al_{0.48}As$ [2] on an InP substrate are lattice matched. In contrast, InSb-$Al_xIn_{1-x}Sb$ system has a lattice mismatch. The lattice mismatch between InSb and $Al_{0.2}In_{0.8}Sb$ is ~1%. Hence the InSb layer must be thinner than the critical thickness to avoid further introduction of defects. A conventional InSb QW heterostructure uses a relaxed $Al_xIn_{1-x}Sb$ layer as the lower barrier and the upper barrier. A higher Al percentage in the $Al_xIn_{1-x}Sb$ barriers provides better confinement of electrons in the InSb QW but also requires a thinner InSb layer. A larger lattice mismatch incurs a smaller critical thickness. A drawback of the thinner InSb QW is increased interface-roughness scattering which reduces the electron mobility. In order to have both a high Al percentage and a relatively thick QW, a strain compensated semiconductor structures is introduced [3].

A shallow QW (short surface to QW distance) is beneficial for devices with top gates and increases the sensitivity of magnetic field sensors [4,15]. It is also beneficial for device mesa defining because the required etch depth is lowered. The shallowness of the

QW leads to a thinner spacer layer, which again decreases the electron mobility due to large ionized dopant scattering. The scattering of by ionized dopant can be partially reduced by doping the barrier only on one side of the QW (asymmetrically doped).

This chapter first gives a brief review of the physics of QWs containing two-dimensional electron gases (2DEG). Then a brief introduction to the classical and quantum Hall effects will be given followed by a discussion of a new strain compensated semiconductor structure. Most of the potential devices based on InSb QWs are operated at room temperature. This study is mostly concentrated on optimizing the InSb QWs for high room-temperature electron mobility. Finally, the room temperature mobility improvement of new shallow InSb QW heterostructures grown on 2^0 off-cut GaAs (001) substrates will be discussed.

3.2 The physics of two-dimensional gases in quantum wells

3.2.1 Subbands

In a quantum well, electrons are free to propagate in the x-y plane but are confined by a potential *V(z)* in the *z* direction [5]. The electronic wave function and the energy dispersion relation in a 2DEG can be written as;

$$\psi(\bar{r}) = \phi_n(z)\exp(ik_x x)\exp(ik_y y) \qquad 3.1$$

$$E = E_c + \varepsilon_n + \frac{\hbar^2}{2m^*}(k_x^2 + k_y^2) \qquad 3.2$$

Where m^* is the effective mass, k_x and k_y are components of the electron wave vector and E_C is the energy of conduction band minimum.

The index *n* represents different subbands, each having a wave function $\varphi_n(z)$ and a cut off energy ε_n [5]. The term $(E_c+\varepsilon_n)$ is defined as the subband energy E_s.

E_s values are eigenvalues of the one-dimensional Schrödinger equation 3.3 in the z direction

$$\left[-\frac{\hbar^2}{2m^*}\frac{d^2}{dz^2}+V(z)\right]\varphi(z)=E_s\varphi(z) \qquad 3.3$$

The density of states (number of states per unit area per unit energy) is given by;

$$N_{2D}=\frac{m^*}{\pi\hbar^2}\theta(E-E_s) \qquad 3.4$$

Where, θ is the unit step function.

In the low temperature limit, the equilibrium electron density (n_s) can be calculated using the Fermi function f_0.

$$n_s=\int N_{2D}(E)f_0(E)dE$$

3.5

$$f_0\approx\theta(E_F-E) \qquad 3.6$$

$$n_s=N_{2D}(E_F-E_s) \qquad 3.7$$

In summary, the quantum confinement in the z direction leads to a piecewise constant density of states as shown by the Figure 3.1.

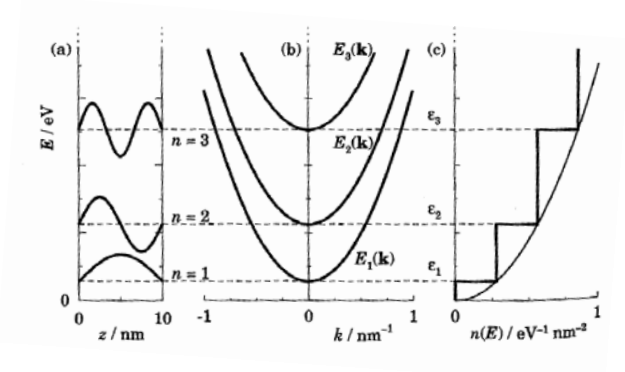


Figure 3.1 (a) Electronic wave function at subband energy levels (b) Energy dispersion relation for each subband and (c) Density of states of a two-dimensional electron gas. [6]

3.2.2 Low field magnetoresistance (classical Hall effect)

3.2.2.1 Drude model

Consider a 2DEG under an applied electric field **E** (No magnetic field) The electric field gives the conduction electrons a drift velocity $\boldsymbol{v_d}$ in the direction of the force $q\mathbf{E}$ where, q is the charge of the carrier. The mobility (μ) of the conduction electrons is defined as the ratio of the drift velocity to the electric field [5]. At steady state, the rate at which electrons receive momentum from the external field is equal to the rate at which they lose momentum due to scattering [5].

$$-\left[\frac{dp}{dt}\right]_{scattering} = +\left[\frac{dp}{dt}\right]_{field} \tag{3.8}$$

$$\frac{mv_d}{\tau_m} = qE \tag{3.9}$$

$$\left|\frac{v_d}{E}\right| = \frac{|q|\tau_m}{m} \equiv \mu \tag{3.10}$$

Where, τ_m is the momentum relaxation time.

Under an electric field and a weak magnetic field (**B**) perpendicular to the 2DEG, the momentum conservation equation can be re-written as;

$$\frac{mv_d}{\tau_m} = q\left[\vec{E} + \vec{v}_d \times \vec{B}\right] \tag{3.11}$$

In the tensor form;

$$\begin{bmatrix} \frac{m}{e\tau_m} & -B \\ B & \frac{m}{e\tau_m} \end{bmatrix} \begin{pmatrix} v_x \\ v_y \end{pmatrix} = \begin{pmatrix} E_x \\ E_y \end{pmatrix} \tag{3.12}$$

By using current density and the electron density relation $J = qv_d n_s$ and rearranging terms, one can re-write the tensor equation 3.12 as;

$$\begin{pmatrix} E_x \\ E_y \end{pmatrix} = \sigma^{-1} \begin{bmatrix} 1 & -\mu B \\ \mu B & 1 \end{bmatrix} \begin{pmatrix} J_x \\ J_y \end{pmatrix} \qquad 3.13$$

where $\sigma \equiv |q| n_s \mu = e n_s \mu$ is the zero field conductivity. The resistivity tensor is defined by;

$$\begin{pmatrix} E_x \\ E_y \end{pmatrix} = \begin{bmatrix} \rho_{xx} & \rho_{xy} \\ \rho_{yx} & \rho_{yy} \end{bmatrix} \begin{pmatrix} J_x \\ J_y \end{pmatrix} \qquad 3.14$$

Then $\rho_{xx} = \sigma^{-1}$ and $\rho_{yx} = -\rho_{xy} = \mu B / \sigma = B / e n_s$

ρ_{xx} is the longitudinal resistivity. The transverse resistivity ρ_{xy} is also called Hall resistivity and linearly increases with magnetic field.

3.2.2.2 Hall measurements

The Hall Effect measurement is an experimental way to determine the resistivity tensor and a basic characterization method in semiconductor thin films to deduce carrier density and mobility (using the low field resistivities). The experimental observation of the Hall effect can be made using a lithographically-defined rectangular Hall bar or a more-simple square specimen directly cleaved from the epitaxially grown wafer.

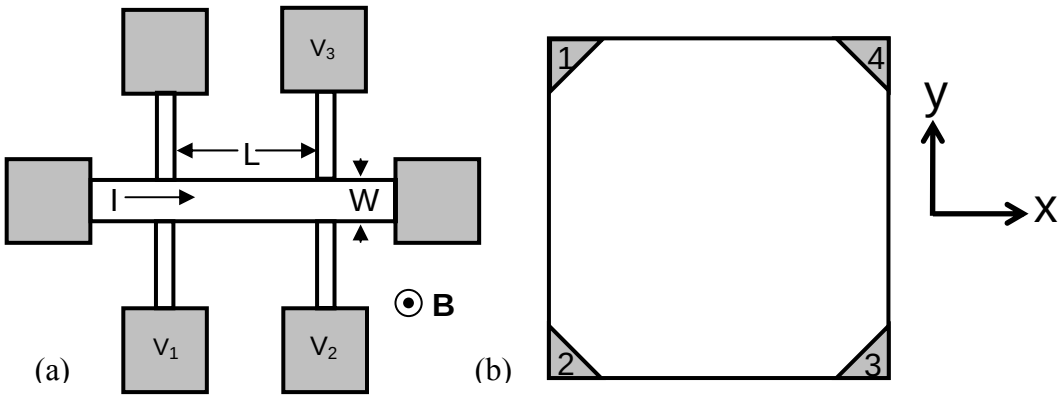


Figure 3.2 (a) Hall bar geometry and (b) square geometry for Hall measurements. The magnetic field is in the z direction perpendicular to the plane of the 2DEG

In a Hall bar with width W and length L as shown in Figure 3.2(a), a uniform current is made to flow in the x direction. The applied magnetic is perpendicular to the 2DEG (z direction). Typical values for W and L are 100μm and 300μm. The longitudinal voltage drop is measured as $V_x = V_1 - V_2$ and the transverse voltage drop is measured as $V_H = V_2 - V_3$. At steady state, the current density in the transverse direction is zero (J_y=0). Then,

$$E_x = \rho_{xx} J_x \quad ; \quad \rho_{xx} = \frac{V_x}{I}\frac{W}{L} \tag{3.15}$$

$$E_y = \rho_{yx} J_y \quad ; \quad \rho_{xy} = \frac{V_H}{I} \tag{3.16}$$

If the carriers are holes $V_H > 0$, while $V_H < 0$ if the carriers are electrons

The carrier density (n_s) and mobility (μ) of the semiconductor medium of the Hall bar can be obtained from ρ_{xx}(B=0) and ρ_{xy}.

$$n_s = \left[e\frac{d\rho_{xy}}{dB} \right]^{-1} = \frac{I}{e\, d V_H / dB} \tag{3.17}$$

$$\mu = \frac{1}{en_s\rho_{xx}} = \frac{I/e}{n_s V_x W/L} \qquad 3.18$$

In a square specimen the carrier density is given by the same equation 3.17. The resistivity of the specimen, however, is measured using the van der Pauw technique. van der Pauw described a method to calculate the resistivity of an arbitrary shaped specimen assuming that the layer is homogeneous in thickness , electrical contacts are point shaped and small, contacts are placed along the boundary and the surface of the specimen is simply connected (i.e. specimen does not have isolated holes) [7]. Then the formula for the longitudinal resistivity is,

$$\rho_{xx} = \frac{\pi}{\ln 2}\left[\frac{R_{12,43} + R_{43,12} + R_{23,14} + R_{14,23}}{4}\right] f\left[\frac{R_{12,43} + R_{43,12}}{R_{23,14} + R_{14,23}}\right] \qquad 3.19$$

where $R_{12,43} = \frac{V_{12}}{I_{43}}$ is a 4 point resistance, and

$V_{12} = V_1 - V_2$ is a dc voltage measured between contacts 1 and 2 without an applied magnetic field ($B = 0$).

I_{43} is the dc current I injected into contact 4 and taken out of contact 3.

$R_{43,12}$, $R_{23,14}$ and $R_{14,23}$ are likewise defined.

The function f is a correction for asymmetry in specimen geometry and finite contact size. For a square specimen with small contacts, f =1. The mobility can be calculated from measurements of a square specimen as,

$$\mu = \frac{1}{\rho n_s |e|} \qquad 3.20$$

The average diameters of the contacts and the specimen thickness must be much smaller than the distance between the contacts [8]. To minimize the errors due to non-

zero contact size compared to the specimen size, the largest possible square (8×8 mm) that can be fitted to the tungsten sheet in the annealing station is used for low field (up to 0.12T) Hall measurements

.

3.2.2.3 Temperature dependent electron mobility

InSb QWs grown using Molecular Beam Epitaxy are characterized from room temperature to 20K using a closed cycle He refrigerator. An (8×8) mm square specimen is cleaved and In contacts are deposited using a soldering iron. Then the specimen is annealed at 230 ^{0}C for 7 minutes while purging with 20% nitrogen 80% hydrogen forming gas, in order to minimize surface oxidization. Specimens are then mounted to a holder and the contacts are wire bonded to terminals on the holder using thin gold wires.

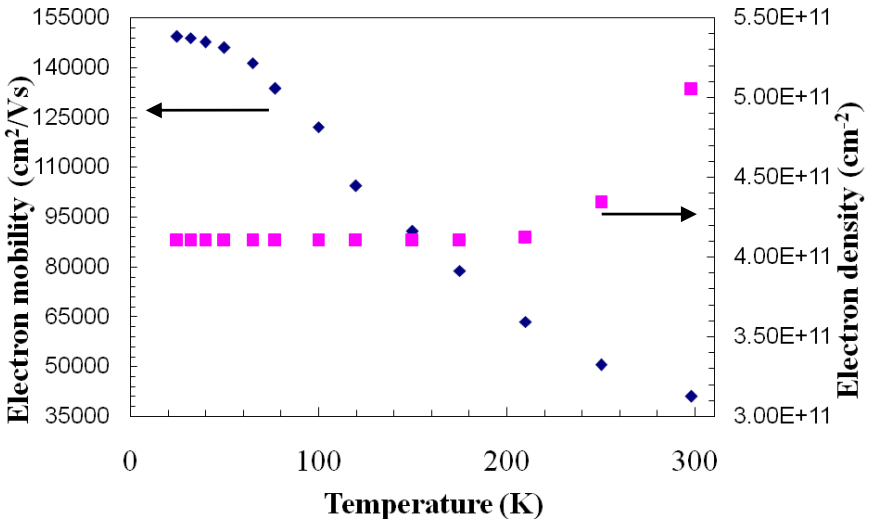


Figure 3.3 Temperature dependence of electron mobility and density of an InSb quantum well grown on GaAs(001)

The temperature dependence of electron mobility and density in an InSb QW is shown in the Figure 3.3. The electron density decreases with decreasing temperature and

saturates at low temperatures. The electron mobility increases as temperature decreases and saturates at low temperatures. Various scattering processes are present in the InSb/AlInSb heterostructure including scattering by optical and acoustic phonons, remote ionized dopants and background impurities. Phonon scattering is a dominant scattering mechanism for electrons at higher temperatures. Acoustic phonons (sound like waves with long wavelengths) interact with electrons through the deformation potential or strain induced piezoelectric potential in compound semiconductors [9]. Optical phonons occur when the unit cell of the crystal has more than one atom. Electrons are scattered by the electric field that arises from charged atoms, moving in opposite directions in the unit cell, and are significant at only high temperatures (normally above 77K) because of a high exchange energy requirement. The scattering rate of optical phonons falls off rapidly compared to acoustic phonons [9]. At low temperatures the strongest scattering effect arises from remote ionized donors. As discussed in Section 3.5, defect scattering is important at all temperatures. Other possible scattering mechanisms include interface roughness, inter-subband scattering, alloy scattering due to the penetration of the carriers into the $Al_xIn_{1-x}Sb$ barrier layers, and band edge discontinuity due to randomness of the alloy and surface states [9].

3.2.3 High field magnetoresistance (Integer Quantum Hall Effect)

At higher magnetic fields (applied perpendicular to the 2DEG) the longitudinal resistance shows an oscillatory behavior (Shubnikov-de Hass oscillations) with B, while the Hall resistance shows plateaus at minimas in the longitudinal resistance (Figure 3.4(b)). The Shubnikov-de Hass (SdH) oscillations arise because of Landau level

formation in the 2DEG density of states under an external magnetic field. *i.e.* step like density of states break up into a sequence of peaks spaced by $\hbar\omega_c$ [5] as illustrated in Figure 3.4(a). Broadening of the peaks is due to the scattering and disorder in the system.

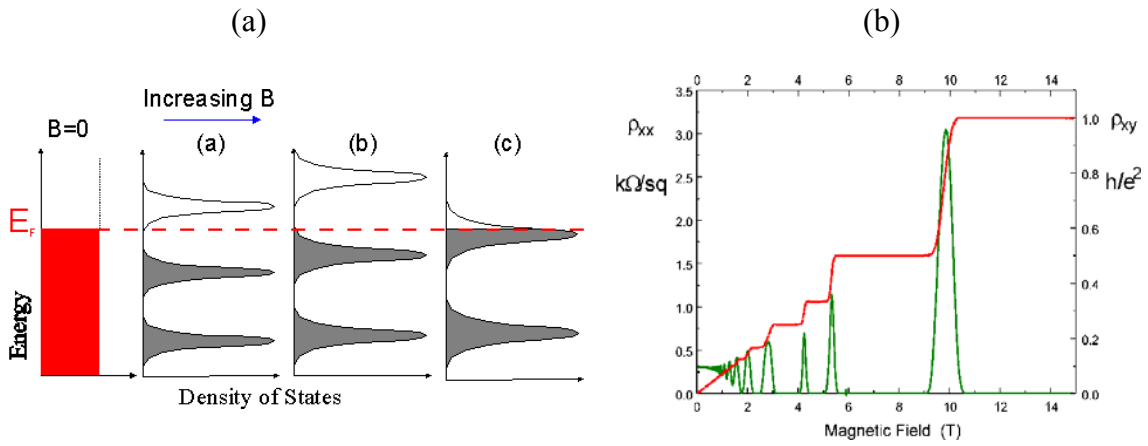


Figure 3.4 (a) Density of states and (b) transverse and longitudinal resistivity of a GaAs two dimensional electron gas under a strong magnetic field [10].

The density of states and allowed energies of a spinless 2DEG system can be written as (Zeeman splitting is not considered);

$$N_s(E,B) = \frac{2eB}{h}\sum_{n=0}^{\infty}\delta\left[E - E_s - (n+\frac{1}{2})\hbar\omega_c\right] \qquad 3.21$$

$$E = E_C + E_S + (n+\frac{1}{2})\hbar\omega \qquad 3.22$$

Where $\omega_c = eB/m^*$ is the cyclotron frequency and n is a quantum number (n = 0, 1, 2…). Since the degeneracy of the Landau levels $D = 2eB/h$, and the spacing between Landau levels are proportional to B. The Fermi level is nearly independent of B. The ρ_{xx} goes through a series of oscillations as the centers of Landau levels pass through the Fermi level. De-population of a Landau level with increasing magnetic field is schematically

shown in the Figure 3.4(a). SdH oscillations can also be observed by keeping the magnetic field constant and changing the electron density by means of a gate voltage [11].

Electron density n_s can be calculated from the number of occupied of Landau levels at a given magnetic field. The number of occupied of Landau levels is $\upsilon = n_s / D$, for a specific field B. When this number (the Landau level filling factor) is a half integer, then the Fermi level is at a center of a Landau level. Hence if the magnetic fields corresponding to two successive peaks are B_1 and B_2 then;

$$\frac{n_s}{2eB_1/h} - \frac{n_s}{2eB_2/h} = 1 \qquad 3.23$$

$$n_s = \frac{2e}{h}\frac{1}{(1/B_1)-(1/B_2)} \qquad 3.24$$

In the original publication on the integer quantum Hall effect [12], the Hall resistivity plateaus separated by resistance h/e^2 were explained by the existence of localized states. But there were some experimental observations that could not be understood by this picture [13]. For instance, how can one explain the flow of current with a minimum resistance (almost zero resistance) in a device that is hundreds of micron long?

The edge channel conduction approach explains the paradox of having current when there is a minimum density of states at the Fermi energy. The edge states are formed at the edge of the device due to a confinement potential. Formation of edge channels in a disordered semiconductor is schematically shown in the Figure 3.5 (a), (b) and (c). At higher magnetic fields, when the Fermi level lies between Landau levels, the only states at the Fermi level are edge states. Edge states carrying current in opposite directions are spatially separated in higher magnetic fields. This suppresses

backscattering. Suppressed backscattering is the fundamental aspect of the edge state picture for explaining the quantum Hall effect.

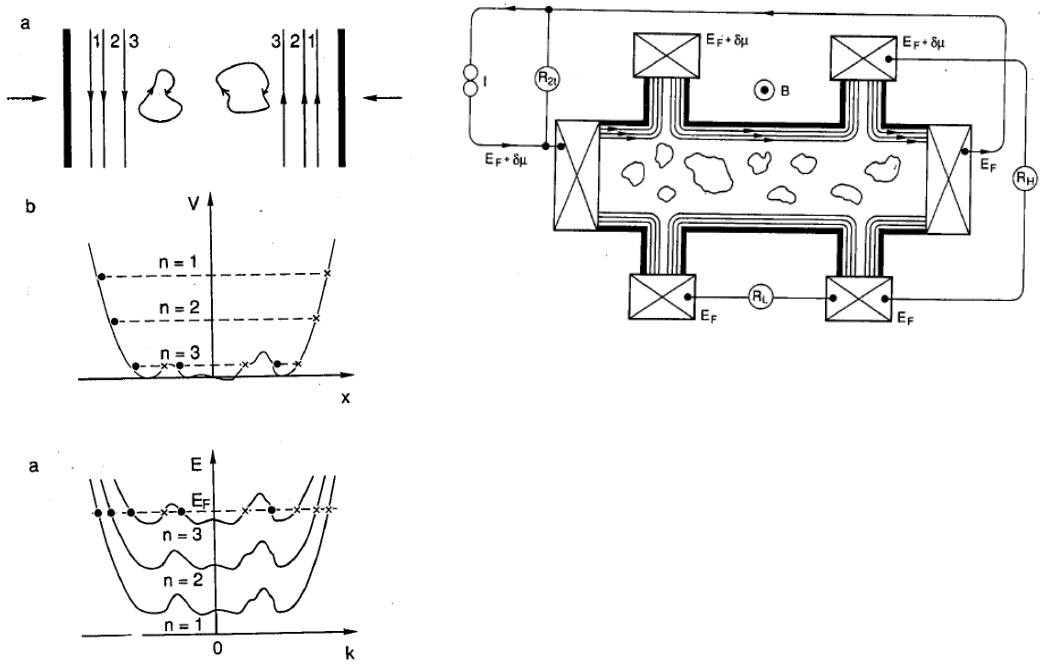


Figure 3.5 Formation of edge channels (a) extended states near the sample boundaries and localized states (b) Slowly varying confinement potential energy along the cross section of Hall bar (c) Total energy of a state along the cross section [13].

Under an applied bias (suppose, under bias, the chemical potential difference between two current terminals is $\delta\mu$) electrons originating from one contact go to the other contact along the device edge. If the system is at a local equilibrium, contacts along one directional electron path are at the same potential [5, 13]. Hence, the longitudinal voltage is zero. The Hall voltage measured between contacts on opposite edges of the device is just $\delta\mu/e$. The current carried by each edge state is $e/h\ \delta\mu$ (Landauer's formula) The number of edge states carrying current is the number of occupied Landau levels (N)

below the Fermi level. Then the Hall resistance is $h/e^2 N$. This explains the plateaus in the Hall resistivity at the same magnetic field as minima in the longitudinal resistivity.

3.3 Strain compensated semiconductor structures

Better quantum confinement and better device performance can be achieved with a higher potential barrier. A higher Al percentage in the AlInSb gives a higher potential barrier. But a higher Al percentage in the AlInSb causes a larger lattice mismatch with InSb. A larger lattice mismatch incurs a lower critical thickness as shown in the Figure 3.6. In the old QW structure, the lower barrier ($Al_xIn_{1-x}Sb$) alloy is the same as the relaxed buffer. There is no room to increase the QW thickness while increasing the Al percentage of the barrier.

A new method of engineering the heteroepitaxial layers is introduced to increase the potential barrier [3]. This method can overcome the ordinary critical thickness limitation. The ordinary method is shown in Figure 3.7. The growth of layer 2 on layer 1 does not increase the dislocation density when the thickness of layer 2 is smaller than the ordinary critical thickness. The point O in Figure 3.6 is an example of an ordinary critical thickness for around 1.3% lattice mismatch.

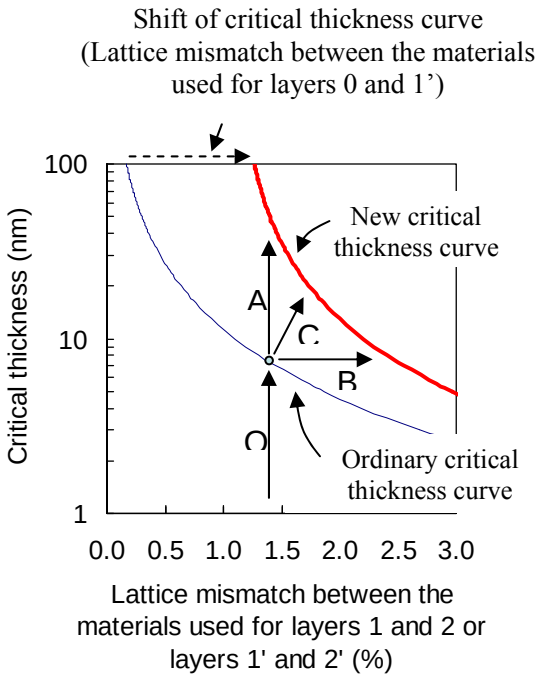


Figure 3.6 Critical thickness of an epilayer made using the new method (thick solid curve) and critical thickness calculated by the Matthews-Blakeslee criterion (thin solid curve)

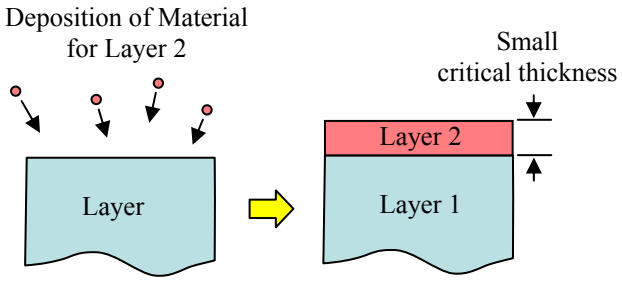


Figure 3.7 Formation of layer 2 under the ordinary method. The thickness of layer 2 is limited by the Matthews-Blakeslee's critical thickness.

Figure 3.8 shows the proposed new method. This method makes it possible to increase the critical thickness for layer 2 (indicated by the arrow A in Figure. 3.6), the lattice mismatch between the materials used for layers 1 and 2 (arrow B in Figure 3.6) and both of them (the arrow C in Figure 3.6). These three objectives can be attained by:

a) Choosing materials for layers 1' and 2' whose lattice mismatch is equal to or larger than that of the materials used for layers 1 and 2. b) Using a relaxed layer, labeled layer 0, as a substrate whose lattice constant is between those of the materials for layers 1' and 2'. c) Depositing layer 1' on top of layer 0 up to the ordinary critical thickness calculated with the lattice mismatch of the materials used for layers 0 and 1'. d) Growing layer 2' on layer 1' up to the ordinary critical thickness calculated with the lattice mismatch of the materials used for layers 0 and 2'.

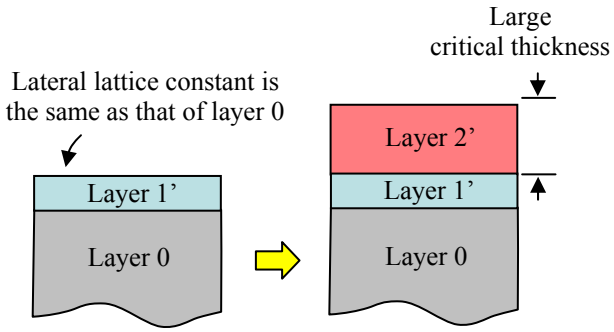


Figure 3.8 Formation of layer 2' under the new method. A strained layer 1' is grown on layer 0. Layer 0 acts as a substrate to layer 1'. Both the critical thickness and lattice mismatch for layer 2' can be increased by growing layer 2' on layer 1'.

When the growth of layer 1' is completed, the lateral lattice constant of layer 1' is the same as that of the material used for layer 0 due to an elastic deformation in layer 1'. Therefore, the critical thickness for layer 2' should be calculated for the lattice mismatch of the materials used for layers 0 and 2', not layers 1' and 2'. This means that a new critical thickness curve for the layer 2' growth should be plotted by shifting the ordinary critical thickness curve horizontally by the amount of lattice mismatch between the

materials used for layers 0 and 1', as shown in Figure 3.6. The shape of the curve can be slightly altered depending on the difference in other material parameters. Figure 3.6 clearly shows that all the three objectives a) – c) are attainable using the new method.

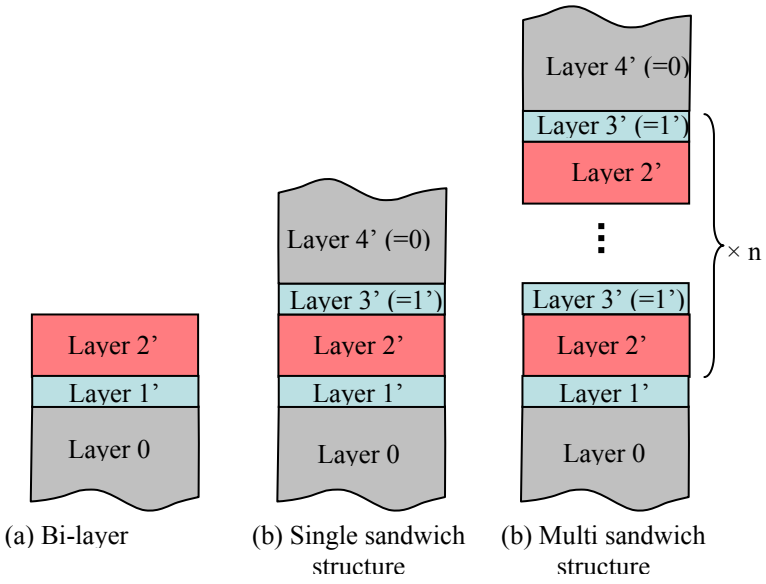


Figure 3.9 Three types of layer structures that can be made by the new method. When the layer 3' is made out of the same material used for layer 1', a symmetric sandwich structure can be made. When the layer 4' is made out of the same material used for layer 0, the structure is more mechanically stable.

The layer structure described thus far is a simple bi-layer structure shown in Figure 3.9(a). The new method can also be used to make single (Figure 3.9(b)) or multi (Figure 3.9(c)) sandwich structures in a similar fashion: on top of layer 2', layer 3' which consists of a material whose lattice constant is near or equal to those of the materials used for layers 0 or 1' is deposited up to the critical thickness of the materials used for layers 0 and 3'. Sandwich structures with either symmetric or asymmetric material properties can be made, depending on the choice of the layer 3' material. When a material whose lattice

constant is the same as that of layer 0 is used for layer 3' or layer 4', the sandwich structure is more mechanically stable than a simple bi-layer structure.

Since many device designs are optimized by having thicker active layers and using materials with larger lattice mismatch difference, the new method can improve the performance of existing semiconductor devices, as we have already demonstrated with InSb quantum well devices. In addition, this method can make it possible to realize previously unfeasible device designs due to a wider choice of materials for the constituent layers.

3.4 InSb quantum well structure for high room temperature electron mobility

A schematic of the new InSb QW structure designed according to the new method described in the Section 3.3 is shown in Figure 3.10(b). A schematic of the old QW structure is shown in Figure 3.9(a) for comparison. The ordinary critical thickness (according to Matthews and Blakeslee [14]) of an InSb QW on an $Al_{0.2}In_{0.8}Sb$ lower barrier is around 9nm. The Al composition of the relaxed buffer (or layer 0) is 10%. According to the new method (single sandwich structure), the new critical thickness for the InSb layer (or layer 2') grown on 20nm of $Al_{0.2}In_{0.8}Sb$ (or layer 1') is 20nm. The thickness of the $Al_{0.2}In_{0.8}Sb$ upper barrier layer (or layer 3') is 20nm. After the upper barrier, a 30nm $Al_{0.1}In_{0.9}Sb$ layer is grown. The InSb QW is only 50 nm below the surface. The cap layer's lattice constant is the same as for the relaxed buffer layer ($Al_{0.1}In_{0.9}Sb$). Therefore, if necessary, it is possible to grow a thicker cap layer without introducing further dislocations. The spacer layer thickness for Si delta doping near the QW is 10nm. The second Si delta doped layer, nearer the surface, is 20nm below the

surface. Modulation doping of the QW is designed such that the doping is performed after the growth of the InSb layers. This doping profile minimizes the scattering from segregated Si atoms, where it assumes that Si segregates along the growth direction.

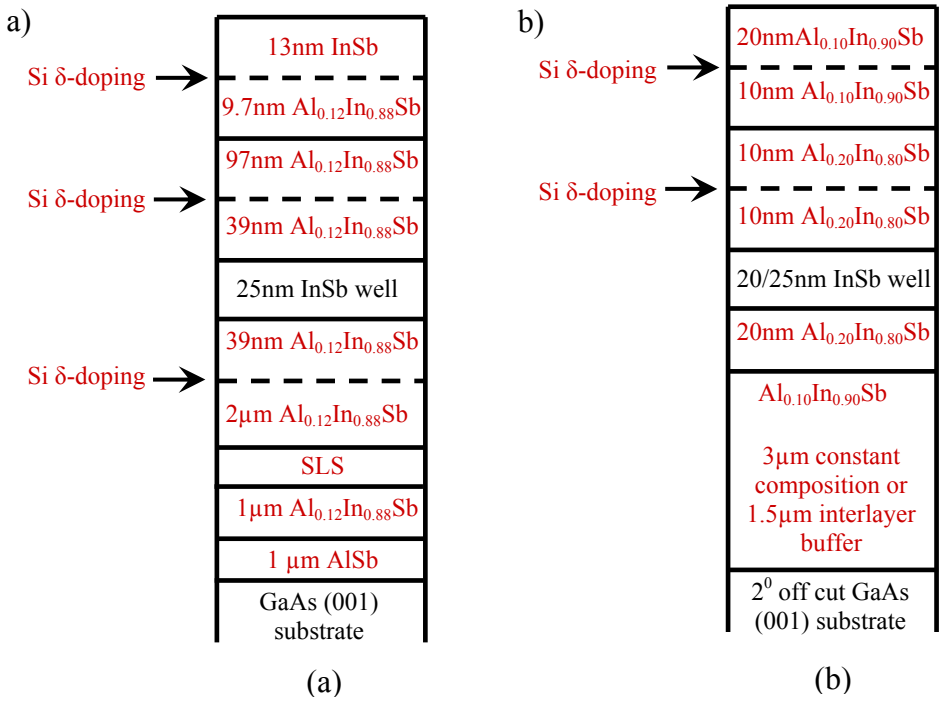


Figure 3.10 (a) Deep InSb QW structure. Barrier layers have the same Al percentage as the buffer layer. There is limited freedom for a higher potential barrier. (b) The new shallow InSb QW structure has more freedom for a higher potential barrier.

3.5 Electron mobility in modulation doped InSb QW

3.5.1 Asymmetrically doped QWs

For the initial experimental realization of the new structure, three types of 20 nm thick InSb QW structures were grown on GaAs (001) substrates. Figure 3.11 shows schematics of the three QW structures. *A* has the new structure, a similar structure as shown in Figure 4.10(b). Both the QW and the barriers are strained. *B* has a structure

where only the InSb layer is strained and the barrier alloy ($Al_{0.1}In_{0.9}Sb$) is the same as the buffer alloy. In structure *C* the barrier and buffer layers consist of $Al_{0.2}In_{0.8}Sb$ and the QW thickness is 20nm, which is above the critical thickness (~9nm). All three structures have the same Si doping densities near the QW and the surface. Electron mobility and density are summarized in Table 3.1 at temperatures of 298 K, 150K, 77K and 15K.

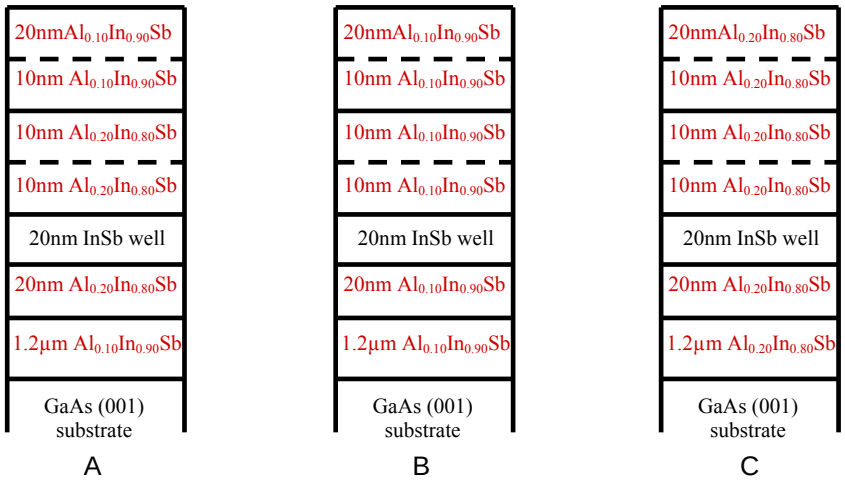


Figure 3.11 Three InSb QW structures. Structure A has a similar structure as shown in Figure 4.10(b). In structure B, only the InSb layer is strained and the barrier alloy ($Al_{0.1}In_{0.9}Sb$) is the same as the buffer alloy. In structure C, the barrier and buffer layers consist of $Al_{0.2}In_{0.8}Sb$ and the QW thickness is 20nm, which is above the critical thickness.

Sample	298K		150K		77K		15K	
	Mobility cm^2/Vs	Density cm^{-2}	Mobility cm^2/Vs	Density cm^{-2}	Mobility cm^2/Vs	Density cm^{-2}	Mobility cm^2/Vs	Density cm^{-2}
A(t081)	24,700	4.5×10^{11}	32,500	3.5×10^{11}	36,500	3.3×10^{11}	38,600	3.4×10^{11}
B(t082)	10,500	1.5×10^{11}	11,900	1.2×10^{11}	13,000	1.1×10^{11}	13,500	1.1×10^{11}
C(t083)	10,800	4.4×10^{11}	10,100	3.4×10^{11}	9,100	3.4×10^{11}	9,400	3.5×10^{11}

Table 3.1 Electron mobility and density in three InSb QW structures: A, B and C

The strain compensated structure, *A*, showed the highest room- temperature and low-temperature electron mobility compared to structures *B* and *C*. Structure *C* showed the lowest quality, presumably due to dislocation nucleation at the InSb/$Al_{0.2}In_{0.8}Sb$ interfaces. These experimental observations confirmed the validity of the proposed new structure for thick InSb QWs with large potential barriers (higher Al percentage in the AlInSb barriers).

The above mentioned structures were grown on 1.2µm-thick buffer layers for simplicity. The QW structure *A* was grown on an optimized buffer for lower defect density. The buffer layer was a constant-composition, thick (~ 3µm) layer on 2º off GaAs (001) or a thin (~1.5µm) double-interlayer buffer on a 2º off GaAs (001) substrate. The temperature dependence of the electron mobility and density are shown in Figure 3.12 and Figure 3.13 for representative 20nm and 25nm thick InSb QWs with $Al_{0.2}In_{0.8}Sb$ barrier layers. Filled and open squares represent two 20nm QWs. The difference between the two structures is the buffer. The solid squares represent a 3µm $Al_{0.1}In_{0.9}Sb$ constant-composition buffer and the open squares represent a 1.5µm-thick double-interlayer buffer. Filled and open circles represent two 25nm QWs. Both have a 3µm constant-composition buffer. All four structures showed excellent room-temperature electron mobilities in the range 38,300 to 40,800 cm^2/Vs. The electron density at room temperature in the four QWs varied from 4.6×10^{11} to 5×10^{11} cm^{-2}. The highest low-temperature (20K) electron mobility is observed for the 20nm QW with a 3µm buffer. Also it showed the lowest electron density (3.4×10^{11} cm^{-2}).

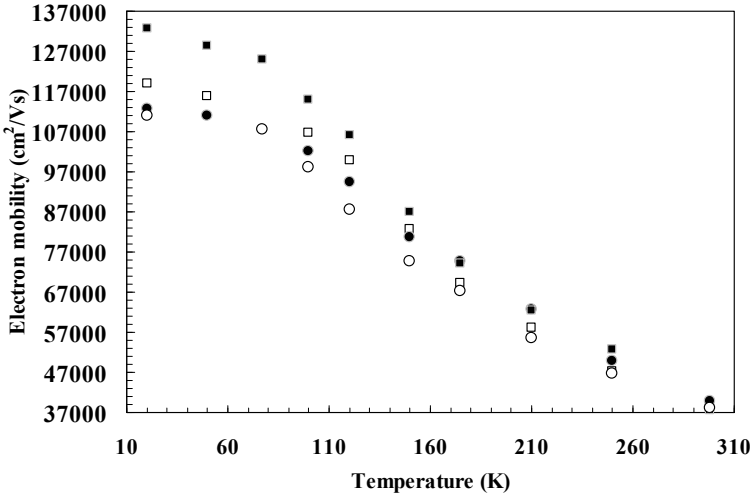


Figure 3.12 Temperature dependent electron mobility in 20nm and 25nm thick InSb QWs with $Al_{0.2}In_{0.8}Sb$ barrier layers. Filled and open squares represent two 20nm QWs. Filled squares represent a QW with a 3µm $Al_{0.1}In_{0.9}Sb$ constant-composition buffer and open squares represent a QWs with a 1.5 µm-thick double-interlayer buffer. Filled and open circles represent two 25nm QWs. Both have a 3µm constant-composition buffer.

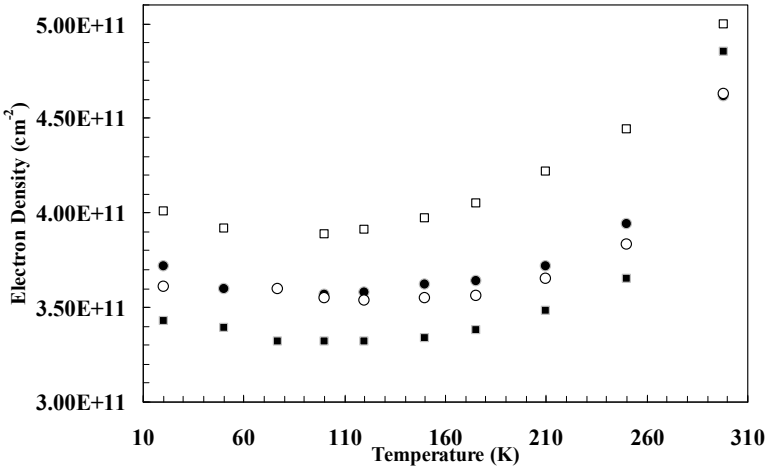


Figure 3.13 Temperature-dependent electron density of 20nm and 25nm thick InSb QWs with $Al_{0.2}In_{0.8}Sb$ barrier layers. Filled and open squares represent two 20nm QWs. Filled squares represent a QW with a 3µm $Al_{0.1}In_{0.9}Sb$ constant composition buffer and open squares represent a QW with a 1.5 µm-thick double-interlayer buffer. Filled and open circles represent two 25nm QWs. Both have 3µm constant composition buffer.

Figures 3.14 and 3.15 show the quantum Hall effect and Shubnikov-de Haas (SdH) oscillations observed at 4.2K in a 20nm QW and a 25nm QW, respectively. Deep minima in the longitudinal resistance and flat plateaus in the Hall resistance are observed in both QWs at high magnetic fields. The resistance minimum of the 20nm QW approaches zero at a magnetic field of 3.8T. The corresponding Landau-level filling factor is 4. In the 25nm QW, the resistance minima almost approach zero at a magnetic field as low as 2.5T, where the filling factor is 6. These data suggest that there are no parallel conducting paths in the structure at 4.2K. Possible parallel conducting paths are carriers in the modulation doped region due to excess doping and occupation of more than one subband in the QW. The buffer does not consist of any layers with low resistivity. The values for electron density obtained from the Hall effect and the frequency of the SdH oscillations are in good agreement. However, the electron mobility of the 20nm QW is lower than that of the 25nm QW, which is opposite what was observed from classical low-temperature Hall effect measurements at 20K.

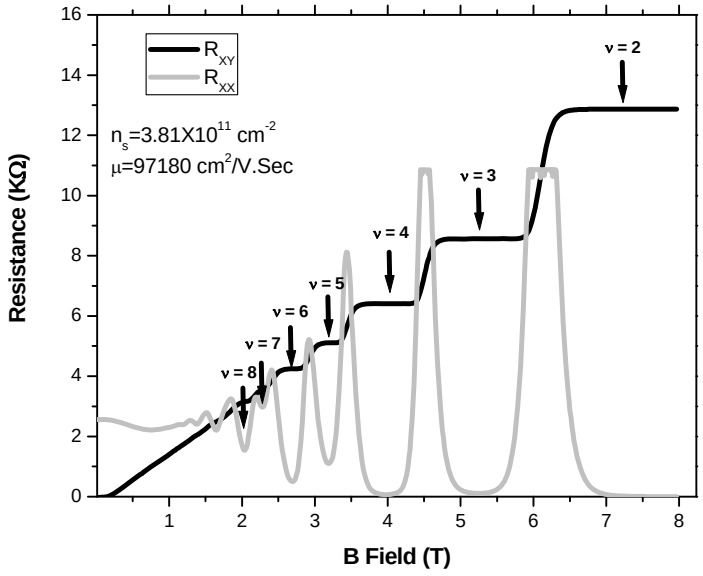


Figure 3.14 Transverse and longitudinal resistance of InSb structure t134 at 4.2K.

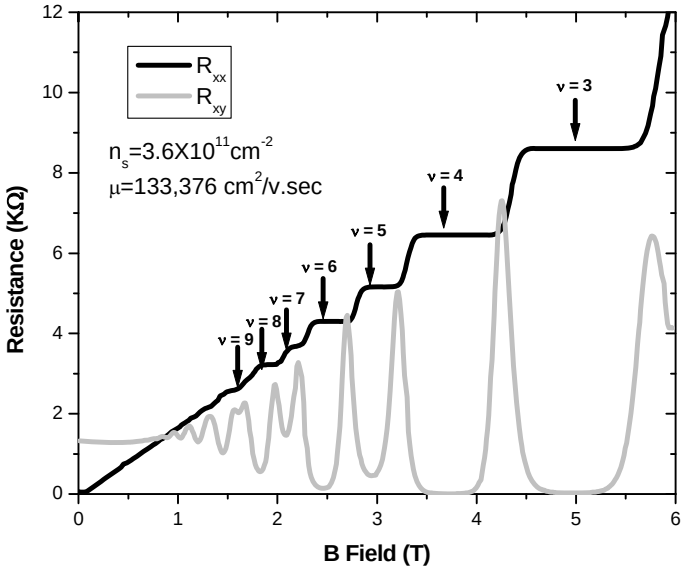


Figure 3.15 Transverse and longitudinal resistance of InSb structure t162 at 4.2K.

The room-temperature electron mobility as a function of electron density for several InSb QWs is shown in Figure 3.16. The solid triangles represent a 20nm InSb QW with a 20nm $Al_{0.2}In_{0.8}Sb$ barrier grown on an $Al_{0.1}In_{0.9}Sb$ buffer. The solid circles represent a 25nm InSb QW with a 20nm $Al_{0.2}In_{0.8}Sb$ barrier grown on an $Al_{0.1}In_{0.9}Sb$ buffer. The solid squares represent a 70nm InSb QW with a 10nm $Al_{0.2}In_{0.8}Sb$ barrier grown on an $Al_{0.05}In_{0.95}Sb$ buffer. The average electron mobility of 20nm-thick InSb QWs with an electron density between 3.7 and 5.5×10^{11} cm^{-2} is 39,400 cm^2/Vs. Those QWs have either a 3μm constant-composition buffer or a 1.5μm-thick double-interlayer buffer. An electron mobility of 42,500 cm^2/Vs with a density of 4×10^{11} cm^{-2} is observed in a QW with a 4μm buffer with two interlayers. Following the new method of engineering thick QWs with higher composition barriers, a 70nm-thick QW with an $Al_{0.2}In_{0.8}Sb$ barrier is grown on a 3μm thick $Al_{0.05}In_{0.95}Sb$ buffer. An electron mobility as high as 37,000 cm^2/Vs was obtained with a carrier density of 1.8×10^{12} cm^{-2}.

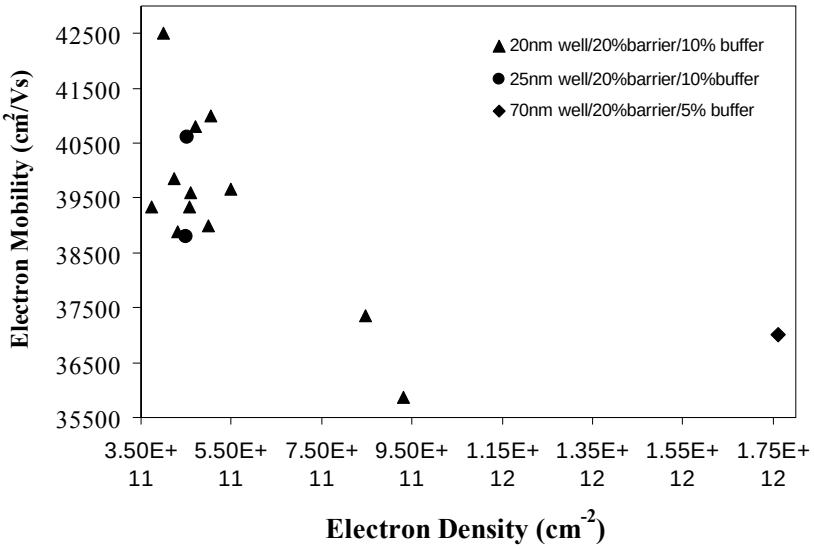
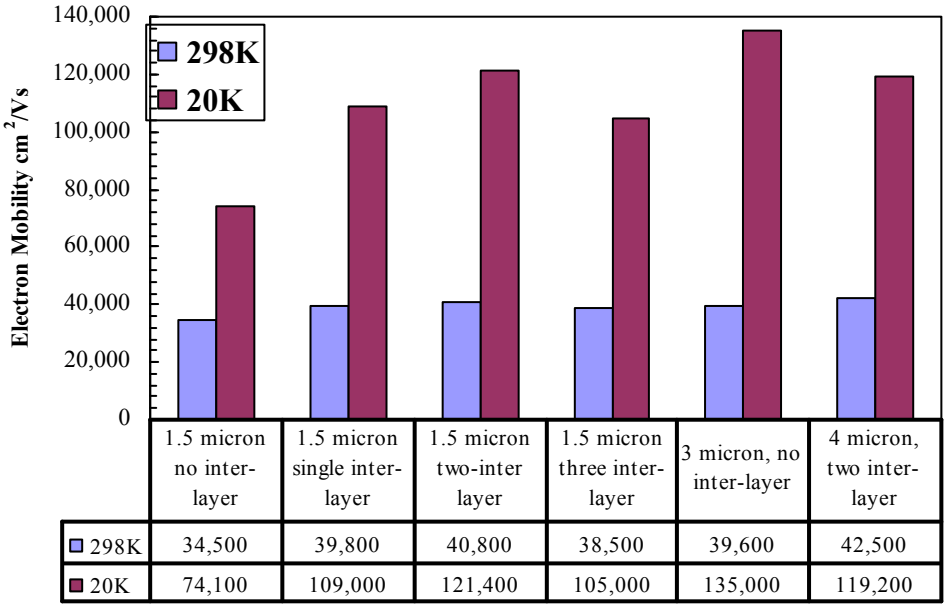


Figure 3.16 Room temperature electron mobility as a function of electron density for InSb QWs with different well thicknesses.

Table C.1 in the Appendix C summarizes asymmetrically-doped shallow InSb QW structures grown on 2° off GaAs (001) substrates. The wafers listed were not grown continuously, but rather over a 10 month period. The electron mobility and density values for those structures confirm the excellent repeatability of the high room-temperature electron mobility under careful calibration of effusion cell temperatures of the MBE system.



	1.5 micron no inter-layer	1.5 micron single inter-layer	1.5 micron two-inter layer	1.5 micron three inter-layer	3 micron, no inter-layer	4 micron, two inter-layer
298K	34,500	39,800	40,800	38,500	39,600	42,500
20K	74,100	109,000	121,400	105,000	135,000	119,200

Figure 3.17 Electron mobilities at 298 K and 20K of some of the milestone InSb QW structures.

Figure 3.17 presents the electron mobilities of some of the milestone InSb QW structures. All the structures are strain-compensated and shallow, have a well width of 20nm and $Al_{0.2}In_{0.8}Sb$ barriers, and were grown on 2º off GaAs (001) substrates. The structures have either an interlayer or constant-composition buffer and the total thickness of the buffer varies from 1.5µm to 4µm.

The room-temperature mobility of the 1.5μm constant-composition buffer is 34,500 cm^2/Vs. This value is comparable with the electron mobility in a deep InSb QW (around 150nm below the surface) grown on a buffer more than 4μm thick (old structure as shown in Figure 3.10 (a)). It is observed that the room-temperature electron mobility in an InSb QW is similar when grown on several different buffer layers: a 1.5μm-thick single-interlayer buffer, a 1.5μm thick buffer with two interlayers, and a 3μm-thick buffer with a constant composition. The low-temperature electron mobility increases as the number of interlayers increases from 0 to 2. This behavior is explained by the scattering mechanisms dominant at high temperature and low temperature. As explained in Section 3.2.2.3, phonon scattering is dominant at room temperature. Defects in QWs grown on a 1.5μm-thick constant-composition buffer have a lower mobility at both room temperature and low temperature. Below the defect density obtained using a single interlayer, a further reduction in defect density may possibly not significantly affect the room-temperature mobility. At low temperatures, scattering from ionized impurity and defects are more dominant. The above structures have similar doping densities near the QW and near the surface. Hence it is evident that reduced defect densities improved the low temperature electron mobility. At 20K, the electron mobility of this specific QW structure with a 3μm constant-composition buffer, is higher than a QW with a 1.5μm thick two-interlayer buffer. But according to Table C.1 in Appendix C, the 20K mobility of an InSb QW grown on a 3μm thick buffer varies from 100,000 cm^2/Vs to 140,000 cm^2/Vs. The 1.5 μm-thick three-interlayer buffer did not improve the electron mobility at room temperature or low temperature. In fact, it showed a significantly lower electron mobility at 20K. This may be possibly due to the upper interface of the third interlayer.

This interface is only 0.32μm below the QW. Interface roughness and misfit dislocation arrays may act as scattering centers.

An InSb QW grown on a two-interlayer buffer with a thickness of 4μm or 5μm (5μm-buffer data is not shown in Figure 3.17) showed a small improvement in room-temperature mobility. The QW with a 5μm buffer has an electron mobility of 149,000 cm^2/Vs at 20K. This high mobility may be a result of parallel conduction. Very thick buffer layers are not recommended because of a possible cracking effect due to a difference in thermal coefficients [16].

The electron mobilities in the InSb quantum wells shown in Table 3.2 suggests that below a certain defect density, a further reduction of defects at the QW is not effective on increasing the electron mobility in the new structure at room temperature as well as at low temperature. Other scattering mechanisms such as ionized impurities and interface roughness limit the mobility. Reducing ionized impurities is challenging in the new structure due to the limits on the thickness of the barrier layer.

3.5.2 Symmetrically doped InSb QWs

The growth of symmetrically doped InSb QWs using the new strain compensated structure is challenging because of the thinner spacer layer, which leads to large ionized impurity scattering. The $Al_{0.2}In_{0.8}Sb$ barrier-layer thickness for an $Al_{0.1}In_{0.9}Sb$ buffer is 20nm. Then the spacer layer thickness for upper and lower delta-doped layers near the QW is less than 20nm. The room-temperature and 20K electron mobility (density) of symmetrically doped InSb QWs with a 10nm spacer layer (same layer structure as in Figure 3.10 (b) except the extra delta-doped layer at 10nm below the 20nm InSb layer) is

29,600cm^2/Vs (7.3×10^{11} cm^{-2}) and 58,000cm^2/Vs (6.5×10^{11} cm^{-2}). Both room-temperature and low-temperature electron mobilities are dramatically reduced compared to the asymmetrically doped InSb QWs.

An effort has been made to increase the electron mobility by putting the doped layers at 60nm above and below the QW. Now the Si δ-doped layers are not in the $Al_{0.2}In_{0.8}Sb$ barrier but in the $Al_{0.1}In_{0.9}Sb$ buffer and cap layer. Here the structure is not preferred because of the possibility of trapping electrons at the $Al_{0.1}In_{0.9}Sb/Al_{0.2}In_{0.8}Sb$ interface. Trapped electrons may act as an extra parallel conducting path to the InSb QW. The electron mobility (density) of a symmetrically doped InSb QW with a 60nm spacer at room temperature and 20K is 31,100 cm^2/Vs (4.2×10^{11} cm^{-2}) and 102,500 cm^2/Vs (2.5×10^{11}cm^{-2}), respectively with negligible parallel conduction at 4.2K. An increased spacer layer thickness improved the low-temperature mobility but the room-temperature mobility is not improved. Table C.2 in Appendix C summarizes the few symmetrically-doped InSb QWs grown using the new structure.

Chapter 4

P-Type InSb Quantum Well Structures Grown on GaAs (001)

4.1 Introduction

In 2005, Datta *et al.* reported the first n-type InSb quantum-well field effect transistor (QWFET) [1]. The InSb QWFET showed a 50% a higher speed and ten times less power dissipation (>300 GHz at 0.5V) than a conventional Si metal oxide field effect transistor (Si MOSFET) [1]. The InSb QWFET shows the best performance among III-V semiconductor QWFETs, including InAs and InGaAs [2], because it has the highest room-temperature electron mobility. This makes InSb QWs potentially useful for future low-power high-speed transistor applications.

Advanced logic technologies, like CMOS technology require a p-channel FET. Bulk III-V semiconductors do not have superior hole mobility compared to Si. Electron and hole mobilities of bulk semiconductors are shown in Table 4.1. Although bulk InSb has the highest room temperature electron mobility (77,000 cm^2/Vs), bulk Ge has the highest hole mobility (1,900 cm^2/Vs). The hole mobility of bulk InSb is 850 cm^2/Vs and the electron mobility of bulk Ge is 3,900 cm^2/Vs.

The hole mobility in III-V semiconductors is lower than the electron mobility due to the large effective mass for heavy holes. Since strain and confinement lift the degeneracy of the heavy-hole (HH) and light-hole (LH) valence bands [3], strain engineered energy bands can enhance the hole mobility in a III-V QW.

First, some physics of the valance band of III-V semiconductors and the effects of confinement and strain on valence band splitting will be discussed. Next a brief review of

hole mobilities reported in different semiconductor channels will be given. Then our realization of p-type strained InSb QWs is discussed. This is the first study of p-type InSb QWs grown on GaAs (001).

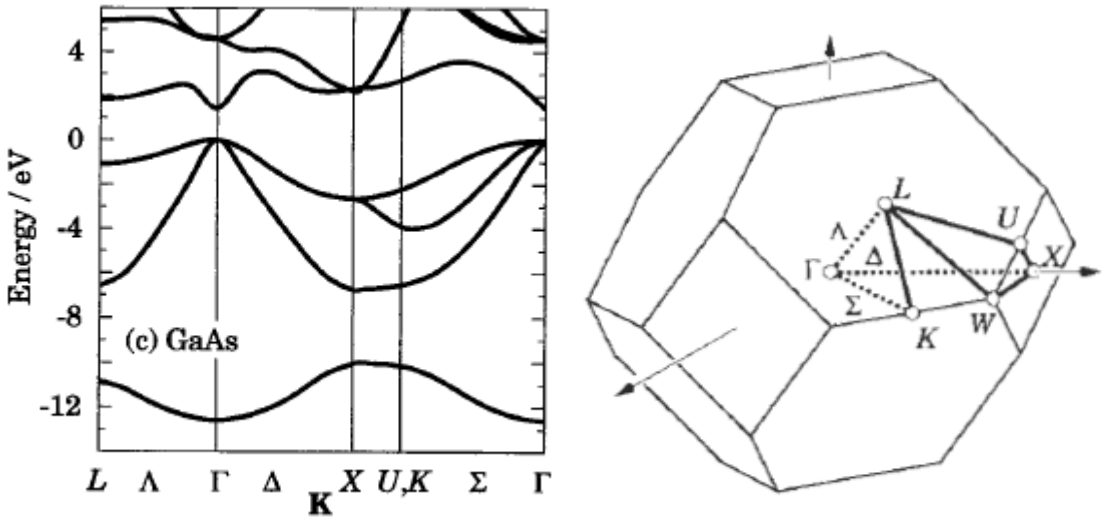
Material	μ_e cm^2/Vs	μ_h cm^2/Vs
Diamond	2,200	1,800
Si	1,350	480
Ge	3,900	1,900
InP	5,400	200
GaAs	8,500	400
$In_{0.53}Ga_{0.47}As$	12,000	300
InAs	40,000	500
GaSb	3,000	1,000
InSb	77,000	850

Table 4.1 Electron and hole mobilities of some bulk semiconductors at room-temperature. InSb has the highest bulk electron mobility and Ge has the highest hole mobility.

4.2 Strain and confinement effects on the valence band of semiconductors

The valence bands of III-V semiconductors are more complicated than the conduction bands. The basic approach to study and calculate the band structure is the use of the cubic crystal symmetry of compound and elemental semiconductors. The band structure of GaAs, a direct gap semiconductor, is shown in Figure 4.1(a). Spin-orbit coupling is not considered in Figure 4.1(a). The valence band maximum of all group III-

V and IV semiconductor is at the Γ point [4]. The Γ point is the origin in k-space of the first Brillouin zone, drawn using the Wigner-Seitz cell of a three dimensional body centered cubic (bcc) lattice. A bcc lattice is the reciprocal lattice of a face centered cubic (fcc) lattice, including zincblende and diamond structures. Figure 1(b) shows the first Brillouin zone, the standard notation for the points of high symmetry and directions of a bcc reciprocal lattice. At the Γ point the two heavy hole (HH) and the single light hole (LH) bands are degenerate (3 fold degeneracy).



(a) **(b)**

Figure 4.1 (a) Band diagram of bulk GaAs, a direct gap semiconductor. At the Γ point, the two heavy hole (HH) and the light hole (LH) bands are degenerate. (b) The first Brillouin zone with the standard notation for the points of high symmetry and directions of a bcc lattice in reciprocal space. [5]

A simple explanation for the behavior of the valence band is given using the fact that the wave functions at the top of the valance band have the symmetry of *p* orbitals [5]. The top three bands are formed from the three *p* orbitals where the highest energy band is doubled. Consider the symmetry of the p_z orbital, where overlap between neighboring

orbitals is higher along the *z* direction and lower in the *x* and *y* directions. Therefore the mobility is higher (and the hole mass lower) in the *z* direction and the mobility is lower (and the hole mass higher) in the *x* and *y* directions, giving an anisotropic band structure. The other two directions have a similar behavior. Adding contributions from all three directions gives the cubic symmetry shown in the Figure 4.1(a) with a doubly degenerate heavy band.

However, the valence band is more complicated than the simple isotropic parabolic dispersion explained above. A more realistic representation of the valence band is shown in Figure 4.2(a). The energy dispersion *E(k)* is non-parabolic and anisotropic with respect to the direction of the momentum vector, **k**. This is shown by the constant-energy surfaces, which can be visualized as warped spheres in Figure 4.2(b). The theoretical model that describes the dispersion relation of the valence band is the Lüttinger Hamiltonian [5, 6]. In Figure 4.2(a), the spin orbit (SO) interaction is taken into account. According to **k.p** models such as the 8×8 Kane model, electronic states have a total angular momentum of j=3/2 and j=1/2. These states are separated by an energy gap, Δ (SO gap) [6].

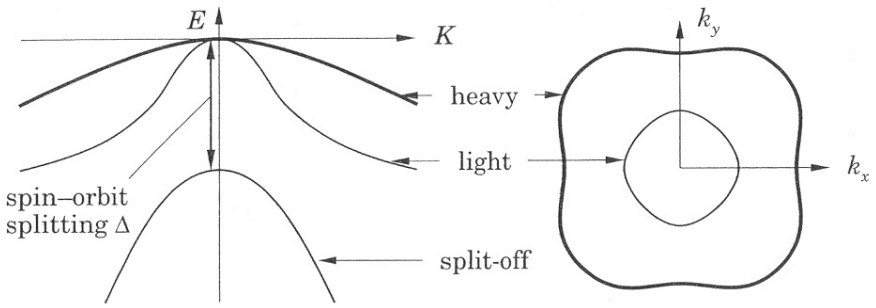


Figure 4.2 (a) Top of the valence band energy diagram (b) constant energy surfaces for holes. [5]

Confinement due to formation of a quantum well lifts the degeneracy of the HH and LH states at **k**=0. When lifting the degeneracy, the bands that are heavy along the *z* direction (confinement direction) are deeper into the quantum well than the band that is lighter in the *z* direction. As mentioned earlier, the bands that are heavy in the *z* direction have a hole mass that is light in the *x*-*y* plane [5]. The quantum confined energies of an unstrained quantum well are shown in Figure 4.3(a). Confined states have a pure heavy hole or light hole character near **k**=0. Away from **k**=0, the light and heavy hole bands anti-cross, mixing the light and heavy characters as shown by Figure 4.3(b).

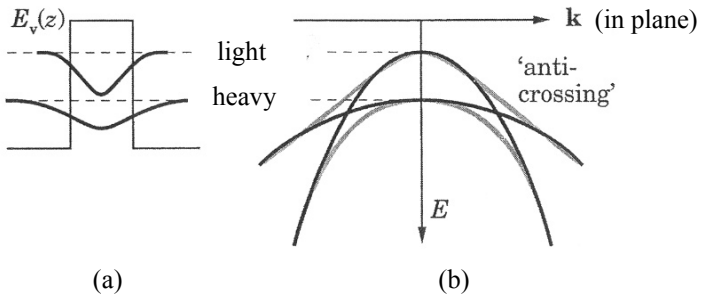


Figure 4.3 (a) Quantum-confined energy states of an unstrained quantum well. (b) The energy dispersion shown for higher k values. Energy bands are anti-crossed, mixing the light and heavy characters of holes. [5]

Biaxial strain breaks the cubic symmetry of III-V semiconductors, which lifts the degeneracy of the valence band at **k**=0 (Γ point) and alters the HH and LH bands in a quantum well. An anisotropic band structure of a bulk semiconductor under a biaxial tension and compression are shown in Figure 4.4(b) and 4.4(c) respectively. For comparison, the band structure of an unstrained tetrahedral semiconductor is shown in Figure 4.4(a). The effect of biaxial compression is similar to the effect of confinement; splitting takes place such that the band is heavy along the growth direction ($k_\perp$) and

comparatively light in the plane ($k_{\parallel}$). The effect is opposite in a tensile strained semiconductor.

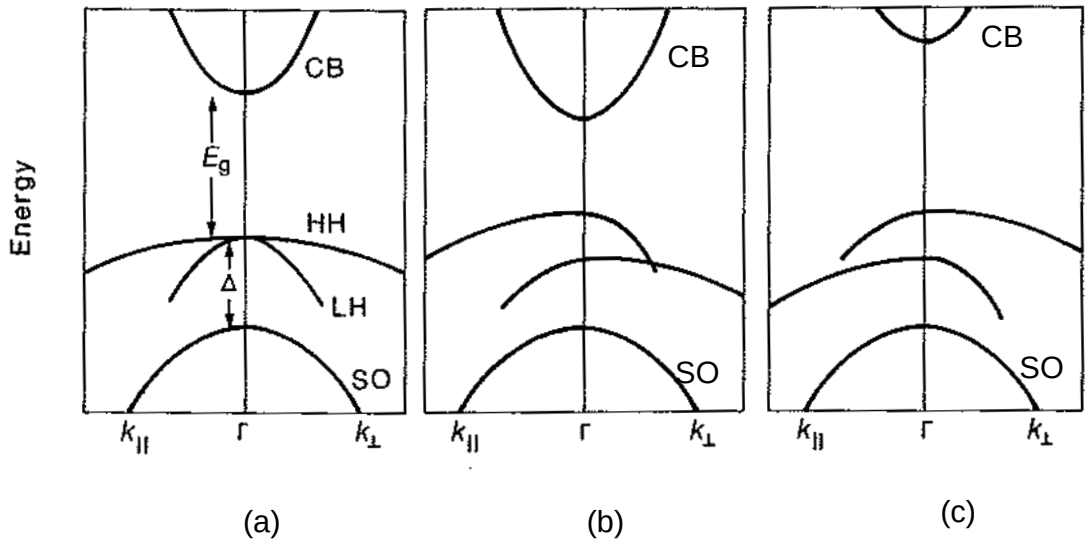


Figure 4.4 (a) The band structure of an unstrained tetrahedral semiconductor. The effect of (b) biaxial tension and (c) biaxial compression on the energies of band and their dispersion. [7]

The energy bands of a strained quantum well are affected by both the confinement and the strain. In a quantum well under a biaxial compression, the heavy hole band edge shifts upwards with respect to the light-hole band edge. This increases the energy splitting between the highest confined heavy hole and light hole states [7]. The splitting is reversed for a tensile strained quantum well and it is possible to have the light-hole state as the highest confined state. Figure 4.5 (a), (b) and (c) schematically show the effects of strain on the energy states of a quantum well. Experimentally determined values for hole splittings in compressively strained InSb layers are given in Ref.[21].

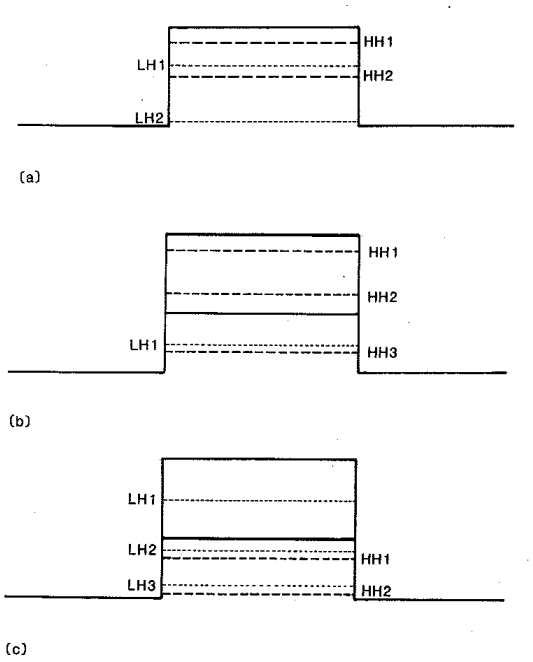


Figure 4.5 The valence band energy states of (a) an unstrained, (b) a compressively strained, and (c) a tensile strained quantum well. [7]

4.3 Review of hole mobility in p-type semiconductor channels

CMOS transistor scaling and Moore's Law continue using Si technology with recent breakthroughs such as metal-gate/high-k stacks, hole and electron mobilities enhancements by applying both uniaxial and biaxial strain, and the non-planar fully depleted Tri-gate CMOS transistor architecture [8].

Biaxial tensile strain enhances the electron mobility in the Si channel of a SiGe NMOS structure [9]. The biaxially strained SiGe channel grown on Si enhances the hole mobility of the PMOS structure [10, 11]. However the biaxially strained PMOS structure is not attractive due to its mobility degradation at higher electric fields. A process induced-uniaxial compressive strain is applied in current Si-CMOS technology to

enhance the performance of PMOS devices (in the earlier technology epi-SiGe acts as the transistor source and drain regions). At the same time a uniaxial tensile strain is applied in NMOS devices by introducing a silicon nitride cap. Over 200% mobility enhancement is reported in Si channel p-MOSFETs with 2GPa uniaxial compressive strain induced by a $Si_{0.8}Ge_{0.2}$ source and drain [12]. The highest electron and hole mobilities reported in strained Si inversion layers are 2,900 and 2,200 cm^2/Vs respectively.

The biaxial strained Ge QW as the channel material in a p-type FET is attractive due to the higher hole mobility of bulk Ge. It is also compatibile with a strained Si n-type QW [13,14] (electron mobility of 2,600 cm^2/Vs with density of 2×10^{11} cm^{-2}) in a SiGe heterostructure in CMOS circuits. Myronov *et al*. reported a 3,100 cm^2/Vs hole mobility with a hole density of 4.1×10^{12} cm^{-2} in a compressively-strained 20nm-thick Ge QW with $Si_{0.45}Ge_{0.55}$ barriers grown on a Si (001) substrate [15]. This is the highest reported carrier mobility in a p-type semiconductor channel.

The III-V n-type QWFETs have shown better performance than scaled Si MOSFETs [1, 2, and 3]. The major challenge with replacing existing Si CMOS logic circuit technology with a III-V technology is the low hole mobility. Observed room temperature hole mobilities in $In_xGa_{1-x}As$ QWs are 260 cm^2/Vs [16], 265 cm^2/Vs [17] and 295 cm^2/Vs [18] for x=0.2, 0.53 and 0.82 respectively. Recently Bennett *et al*. [19] demonstrated a hole mobility of 1,500cm^2/Vs in a 7.5nm-thick $In_{0.4}Ga_{0.6}Sb$ QW with a $Al_{0.7}Ga_{0.3}Sb$ barrier.

4.4 A simplified method to calculate sub band energies of a p-type QW

The method for calculation of subband energies and hole densities is briefly described below.

In-plane strain can increase or decrease the energy gap of a semiconductor [22]. An approximate expression for the modified band gap $E_g^{'}$ is shown in Equation 4.1 [21, 22, 23].

$$E_g^{'} = E_0 + [a(2 - 2\frac{C_{12}}{C_{11}}) \pm b(1 + 2\frac{C_{12}}{C_{11}})]\varepsilon_{//} \quad 4.1$$

where $\varepsilon_{//}$ is the in-plane strain, C_{12} and C_{11} are elastic constants and a and b are deformation potentials. The minus sign gives the light hole gap and the plus sign gives the heavy hole gap.

In metamorphic QW structures, both the InSb well and $Al_xIn_{1-x}Sb$ barrier layers are strained.

For InSb;

$$E_g^{'} = \left[0.240 + (-6.71 \mp 3.76)\frac{\left(-0.343)x_{buffer}\right)}{6.46}\right]eV \quad 4.2$$

$$E_g^{+} = (0.240 + 0.556x_{buffer})eV \quad 4.3$$

$$E_g^{-} = (0.240 + 0.157x_{buffer})eV \quad 4.4$$

where x_{buffer} is the Al compositions of the buffer layers. Dai *et al*. determined the band offsets of the InSb/$Al_xIn_{1-x}Sb$ system and found that the conduction band offset is 62% of the gap difference [24]. Accordingly, barrier heights of InSb QW structure can be expressed as,

$$\Delta E_c = 0.62\left[2.06x_{barrier} - 0.157x_{buffer}\right]eV \quad (4.5)$$

$$\Delta E_v = 0.38\left[2.06x_{barrier} - 0.157x_{buffer}\right]eV \quad (4.6)$$

where $x_{barrier}$ is the Al composition of the barrier layer. Subband energies were calculated using a finite square well method where subband energies are given by solutions of the transcendental equations;

$$\varepsilon \tan\varepsilon = \sqrt{\frac{m^*\Delta E_v L^2}{2\hbar^2} - \varepsilon^2} \quad (4.7)$$

$$-\varepsilon \cot\varepsilon = \sqrt{\frac{m^*\Delta E_v L^2}{2\hbar^2} - \varepsilon^2} \quad (4.8)$$

$$\varepsilon = \sqrt{\frac{m^* E_n L^2}{2\hbar^2}} \quad (4.9)$$

The effective hole mass to use in Eqn. 4.7, 4.8, and 4.9 is the value in the growth direction. For a QW doped on one side and with one occupied subband, the carrier density dependence on the spacer thickness d can be expressed as [25],

$$n \approx \frac{\Delta E - E_1}{\frac{\pi\hbar^2}{m^*} + \frac{q^2 d}{\kappa\varepsilon_o}} \quad (4.10)$$

where ΔE is the barrier height, E_1 is the lowest subband energy, and κ is the relative permittivity of InSb (≈18). This expression assumes that the Fermi level is pinned to the band edge at the delta-doped layer. This assumption is valid only if the number of dopants N_d is larger than the carrier density predicted by Equation 4.10. If N_d is smaller,

then the carrier density will be equal to N_d. The effective hole mass to use in Equation 4.10 is the value perpendicular to the growth direction.

4.5 Compressively strained p-type InSb quantum wells

4.5.1 Layer Structure

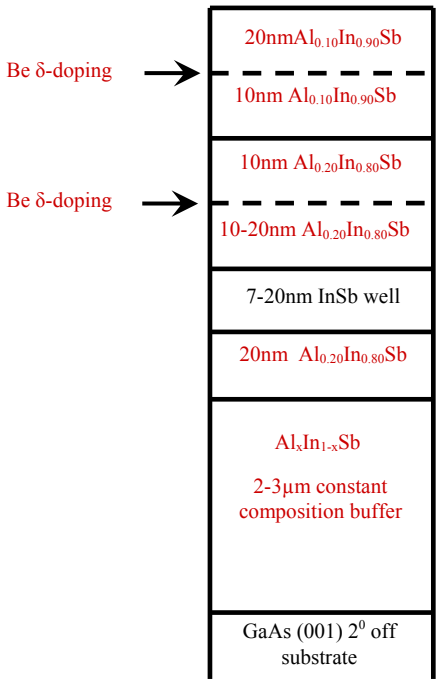


Figure 4.6 A schematic diagram of the layer structure of a p-type InSb quantum-well structure. The Al composition x of the buffer layer takes the value 0.1, 0.15, 0.18 or 0.20.

We have investigated a series of compressively strained InSb QWs with $Al_xIn_{1-x}Sb$ barriers doped with Be. The structures were grown on 2° off-cut GaAs (001) substrates. Beryllium (Be) atoms act as *p*-type dopants in III-V semiconductors by incorporating in Ga sites. The strain of the QW was controlled by changing the Al composition of the $Al_xIn_{1-x}Sb$ buffer layer. Quantum confinement in the wells was obtained using $Al_{0.2}In_{0.8}Sb$ barriers. Figure 4.6 shows a schematic layer structure of an InSb quantum well that is remotely doped with Be. The Al composition *x* of the buffer

layer takes the value 0.1, 0.15, 0.18 or 0.20. The InSb channel is in 0.53%, 0.80%, 0.95% or 1.06% biaxial compression, respectively.

Since all the structures have an $Al_{0.2}In_{0.8}Sb$ barrier, the effect of confinement on the valence band splitting depends only on the well thickness. The wafer sets t187-t190, t193-t200, t212, t241-t242, and t249-t250 were grown in different cell calibration cycles.

4.5.2 Results and discussion

Table 4.2 summarizes the hole mobilities in InSb QWs grown on 2° off-cut GaAs (001) substrates. All the QWs are *p*-type at low temperature and nearly all were *p*-type at room-temperature.

Sample	Buffer layer structure	QW barrier and cap structure	InSb QW thickness/ N_d near QW and surface	Strain at QW	Electron mobility and density at 298K		Electron mobility and density at 20K	
					Mobility cm^2/Vs	Density cm^{-2}	Mobility cm^2/Vs	Density cm^{-2}
t188	2 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$ 10nm spacer 30nm $Al_{0.1}In_{0.9}Sb$ cap	20nm $2\times10^{11}cm^{-2}$	0.53%	4860	2.0E+11	-21,500	-4.5E+11
t190	2 µm $Al_{0.15}In_{0.85}Sb$	20nm $Al_{0.2}In_{0.8}Sb$ barrier 10nm spacer 30nm $Al_{0.1}In_{0.9}Sb$ cap	15nm $2\times10^{11}cm^{-2}$	0.796%	-560	-1.1E+12	-16,900	-5.0E+11
t193	3 µm $Al_{0.15}In_{0.85}Sb$	20nm $Al_{0.2}In_{0.8}Sb$ barrier 10nm spacer 30nm $Al_{0.1}In_{0.9}Sb$ cap	17nm $2\times10^{11}cm^{-2}$	0.796%	-270	-2.3E+12	-17,200	-4.6E+11
t194	2 µm $Al_{0.15}In_{0.85}Sb$	30nm $Al_{0.2}In_{0.8}Sb$ barrier 20nm spacer 30nm $Al_{0.1}In_{0.9}Sb$ cap	15nm $2\times10^{11}cm^{-2}$	0.796%	-460	-1.1E+12	-26,300	-3.1E+11

t198	2 μm $Al_{0.15}In_{0.85}Sb$	20nm $Al_{0.2}In_{0.8}Sb$ barrier 10nm spacer 30nm $Al_{0.15}In_{0.85}Sb$ cap	15nm $2\times10^{11}cm^{-2}$	0.796%	-570	-9.8E+11	-21,500	-5E+11
t199	2.65 μm $Al_{0.18}In_{0.83}Sb$	30nm $Al_{0.2}In_{0.8}Sb$ barrier 20nm spacer 30nm $Al_{0.1}In_{0.9}Sb$ cap	15nm $2\times10^{11}cm^{-2}$	0.955%	-530	-8.9E+11	-7,200	-3.5E+11
t200	2 μm $Al_{0.15}In_{0.85}Sb$	20nm $Al_{0.2}In_{0.8}Sb$ barrier 20nm spacer 30nm $Al_{0.15}In_{0.85}Sb$ cap	15nm $2\times10^{11}cm^{-2}$	0.796%	-540	-5.2E+11	-20,200	-4.3E+11
t212	2 μm $Al_{0.2}In_{0.8}Sb$	30nm $Al_{0.2}In_{0.8}Sb$ barrier 20nm spacer 30nm $Al_{0.2}In_{0.8}Sb$ cap	9nm $2\times10^{11}cm^{-2}$	1.06%	-660	-7E+11	-20,000	-3.5E+11
t241	1 μm $Al_{0.05}In_{0.95}Sb$ 2 μm $Al_{0.2}In_{0.8}Sb$	30nm $Al_{0.2}In_{0.8}Sb$ barrier 20nm spacer 30nm $Al_{0.2}In_{0.8}Sb$ cap	7nm $4\times10^{11}cm^{-2}$ No doping to surface	1.06%	11,200	2.9E+11	-55,600	-4.7E+11
t242	1 μm $Al_{0.05}In_{0.95}Sb$ 2 μm $Al_{0.15}In_{0.85}Sb$	30nm $Al_{0.2}In_{0.8}Sb$ barrier 20nm spacer 30nm $Al_{0.15}In_{0.85}Sb$ cap	12nm $2\times10^{11}cm^{-2}$	0.796%	N type	N type	-52,500	-4.1E+11
t249	3 μm $Al_{0.15}In_{0.85}Sb$	30nm $Al_{0.2}In_{0.8}Sb$ barrier 20nm spacer 30nm $Al_{0.15}In_{0.85}Sb$ cap	12nm $4\times10^{11}cm^{-2}$	0.796%	-370	-1.6E+12	-37,100	-3.7E+11
t250	3 μm $Al_{0.2}In_{0.8}Sb$	30nm $Al_{0.2}In_{0.8}Sb$ barrier 20nm spacer 30nm $Al_{0.2}In_{0.8}Sb$ cap	7nm $4\times10^{11}cm^{-2}$	1.06%	-700	-9.1E+11	-24,000	-4E+11

Table 4.2 Summary of p-type InSb quantum well structures.

A simplified calculation was performed to obtain subband energies and hole densities of p-type InSb QWs at low temperature as described in Section 4.4. The density calculations assumed that only the first subband is occupied. The results are summarized

in Table 4.3. Experimentally observed hole densities (n_{exp}) for QW structures with the same delta doping densities are included for comparison. According to the calculation, a smaller well width with the same strain from the metamorphic buffer lowers the hole density. But a combination of a lower well width and higher strain from the buffer have a tendency to increase the hole density. An increase in spacer layer thickness lowers the hole density.

Experimentally observed hole density behaves in a similar manner for similarly doped QW structures. But experimentally observed densities are lower compared the calculated values. This may be due to a low value for N_d of the delta doped layer. This may also explain why the drop of the hole density with spacer layer is not sharp as predicted by calculation as shown in Figure 4.7.

Well width (nm)	**20**	**17**	**15**	**15**	**12**	**9**	**7**
Al (x) in buffer	**0.1**	**0.15**	**0.15**	**0.15**	**0.15**	**0.2**	**0.2**
E_1 (eV)	**0.007**	**0.01**	**0.012**	**0.012**	**0.017**	**0.026**	**0.032**
E_2(eV)	**0.03**	**0.039**	**0.049**	**0.049**	**0.068**	**0.101**	**0.127**
d(nm)	**10**	**10**	**10**	**20**	**20**	**20**	**20**
n (cm^{-2})	**1.16E+12**	**1.19E+12**	**1.17E+12**	**6.30E+11**	**6.00E+11**	**5.60E+11**	**5.30E+11**
n_{exp}(cm^{-2})	**4.50E+11**	**4.60E+11**	**5.00E+11**	**4.30E+11**	**4.10E+11**	**3.50E+11**	
	21540	**17250**	**16920**	**21160**	**52590**		
Wafer #	**t188**	**t193**	**t190**	**t200**	**t242**	**t212**	

Table 4.3 Calculated subband energies and hole densities for different well widths, buffer and spacer thicknesses. All structure had $Al_{0.20}In_{0.80}Sb$ barrier layers. Experimentally observed hole densities, n_{exp} ,for these structures are also given.

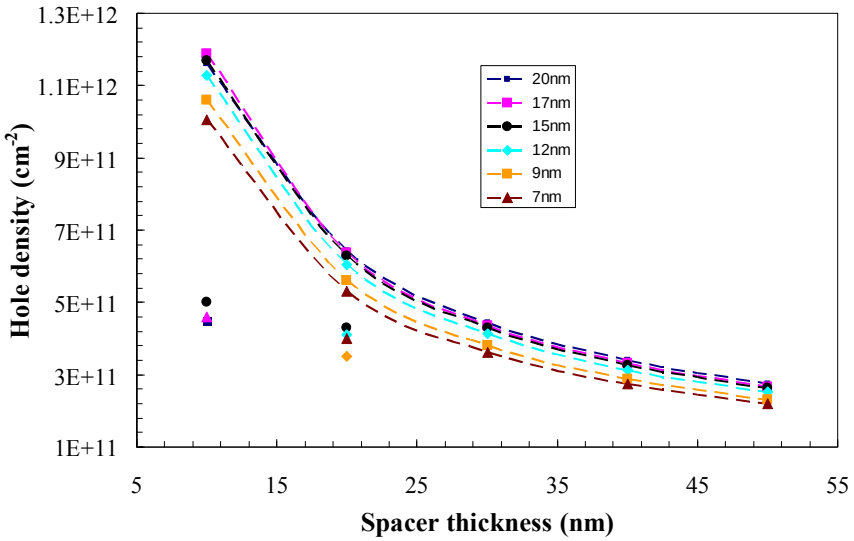


Figure 4.7 Calculated (connected by dashed lines) and experimental hole densities with the spacer thickness for a set of strained QWs

The 20 nm thick InSb quantum wells with 0.53% biaxial compressive strain were not p-type at room-temperature. They were n-type at room temperature, possibly due to the thermally excited electrons. The combination of low *x* and low doping may have prevented pinning of the Fermi level at the acceptor energy in the doped layer. At a sufficiently low temperature they became p-type (< 250K). Increased Be doping (near the QW and near the surface) decreased the low temperature hole mobility as well as the room temperature electron mobility as a result of increased dopant impurity scattering. Both the room temperature electron density and the low temperature hole density increased as Be doping increased. The room temperature electron density increased as the hole density increased possibly due to the increased density of thermally excited electrons, which may be proportional to the hole density. According to the calculation even further increase in doping density could make the QW *p*-type. The highest 20K hole

mobility observed from a 0.53% compressively strained InSb quantum well is 24,900cm^2/Vs with a hole density of $3.3\times10^{11}cm^{-2}$.

Room temperature p-type conduction was observed in an InSb quantum well (t190) by further increasing the compressive strain and the quantum confinement. The strain is increased to 0.8% by introducing an $Al_{0.15}In_{0.85}Sb$ buffer layer. The quantum confinement is increased by decreasing the quantum well thickness to 15nm. The higher strain and stronger confinement can further split the HH and LH bands. The HH band has a higher hole occupation, resulting in a higher room temperature hole mobility [19]. However, the low temperature hole mobility in wafer t190 is lower than the less strained QW (t188), with a similar doping and a spacer layer thickness. This may be due to the slightly higher hole density. The simple calculation also showed an increased hole density in a QW with increased strain and lower well thickness.

As expected, increasing the spacer layer from 10nm to 20nm increased the low temperature mobility of a 0.8% strained 15nm thick QW (t194). These two structures (t190 and t194) have a 30nm $Al_{0.1}In_{0.9}Sb$ cap layer and an $Al_{0.15}In_{0.85}Sb$ buffer layer. When the cap layer is $Al_{0.15}In_{0.85}Sb$, a QW with a thinner (10nm) spacer gave a higher mobility (t198) compared to a structure with an $Al_{0.10}In_{0.9}Sb$ cap layer (t190). This may be due to less or no misfit dislocation formation at the interface of the upper barrier layer and cap layer as discussed in Chapter 3. However, the increased spacer of a structure with an $Al_{0.15}In_{0.85}Sb$ cap reduced both room temperature and low temperature hole density, but had no impact on room temperature and low temperature mobility (t200). The highest room temperature and 20K hole mobility (density) observed from a 0.8% strained 15nm-

thick InSb QW are 570cm^2/Vs (9.8×10^{11}cm^{-2}) and 26,300cm^2/Vs (3.1×10^{11}cm^{-2}), respectively.

The increased strain of a 15nm QW with an $Al_{0.18}In_{0.82}Sb$ metamorphic buffer lowered the low-temperature mobility (t199). The room-temperature hole mobility is nearly the same. A possible reason may be the 15nm QW thickness. The critical thickness of a 0.95% strained QW may be lower than 15nm. The scattering from misfit dislocations would lower the low-temperature hole mobility.

Reducing the QW thickness from 15nm to 12nm lowers the hole density as predicted from the calculation. But the QW is n-type at room-temperature, possibly due to thermally excited carriers (a result of lower hole density). Nevertheless, a hole mobility of 52,500cm^2/Vs with a density of 4.1×10^{11}cm^{-2} was observed at 20K. This high mobility is possibly due to the lower misfit dislocation at the interface. Increasing the doping near the QW and the surface made the QW p-type at room-temperature. The 12nm-thick QW with higher doping had an increased mobility of 370cm^2/Vs (for a density of 1.64×10^{12}cm^{-2}) at room-temperature and 37,140 cm^2/Vs (for a density of 3.7×10^{11}cm^{-2}) at low-temperature.

A further increase of biaxial strain of the InSb QW to 1.06% and a decrease of quantum well thickness to 9nm and 7nm showed a decrease in hole density and an increase in hole mobility at room-temperature. The highest low-temperature mobility (55,600 cm^2/Vs with a hole density of 4.7×10^{11}cm^{-2}) was observed in the 7nm QW. This narrow QW also showed n-type behavior at room-temperature. After increasing the doping density, the highest room-temperature mobility, 700cm^2/Vs, is observed in the 7nm QW structure with a density of 9×10^{11}cm^{-2}. But the low temperature mobility was

not improved in the 7nm QW compared to the 9 nm QW. This may be due to the increased importance of interface scattering at low temperature.

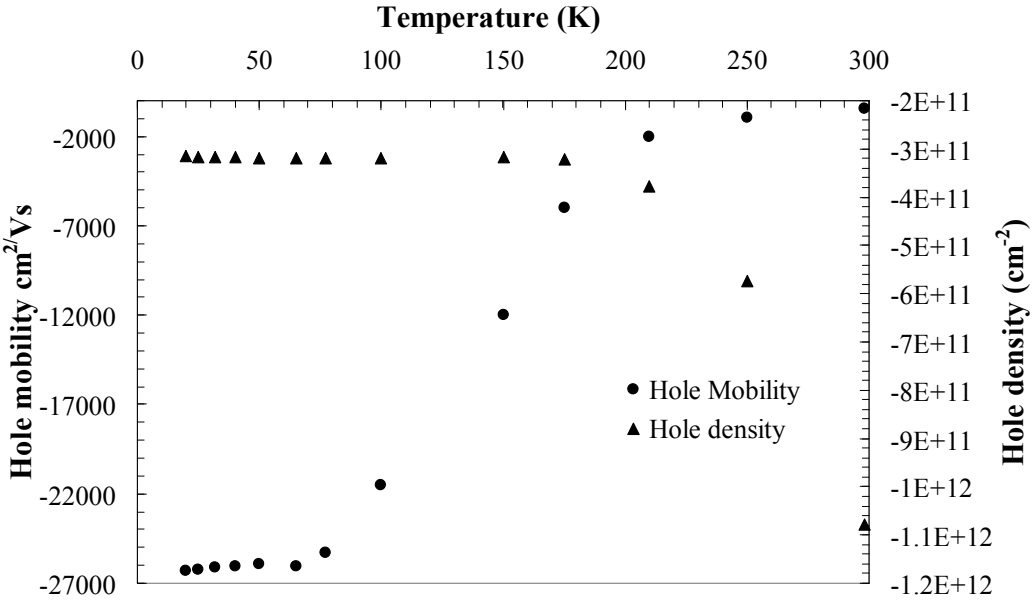


Figure 4.8 Temperature dependent hole mobility and density of a Be delta-doped InSb quantum-well structure (t194)

The temperature-dependent hole mobility and density of QW structure t194 are plotted in Figure 4.8. The hole mobility increases as temperature decreases, as expected for a two-dimensional hole gas. The hole density drops rapidly to $1.1\times10^{12}cm^{-2}$ from $3.2\times10^{12}cm^{-2}$ when the temperature drops from room temperature to 175K. Below 175K, the hole density is relatively constant (negligible density of thermally excited carriers).

A Hall measurement at 4.2K was performed on t196, which shows the lowest hole density. The longitudinal (R_{xx}) and transverse (R_{xy}) resistances are shown as a function of the magnetic field B in Figure 4.9. The quantum Hall effect was clearly observable,

which indicates the presence a two-dimensional hole gas. The highest plateau on the R_{xy} curve corresponds to a filling factor of $\upsilon = 1$.

Due to the large electron g-factor (-51) of InSb, the Zeeman splitting of Landau levels is well resolved at moderate B in Shubnikov de Hass oscillations of n-type InSb QWs (as shown in Figure 3.14 and 3.15 in Section 3.5.1). In a typical set of SdH oscillations for an n-type InSb QW, the minima at low B are deeper for even filling factor than for odd filling factors. This occurs because the Zeeman splitting is smaller than half the Landau level spacing. In contrast, Figure 4.9 shows stronger features at low B for odd filling factors. (Note that there is no minimum for $\nu=6$ and the minimum for $\nu=4$ is weak) This result may be explained by a larger m^*g product for holes. According to calculations of Babayev *et al.* [20] the g-factor for light holes in an InSb QW is ~ -70, which is 1.4 higher than for electrons. Measured in-plane effective mass (discussed in the next section) of the heavy hole band of the InSb QW is varying from $0.04m_0$ to $0.09m_0$, which is around 2.8 to 6.4 times higher than the electron effective mass ($0.014m_0$). Hence at lower magnetic fields, the Zeeman splitting is resolved more easily than the Landau-level spacing.

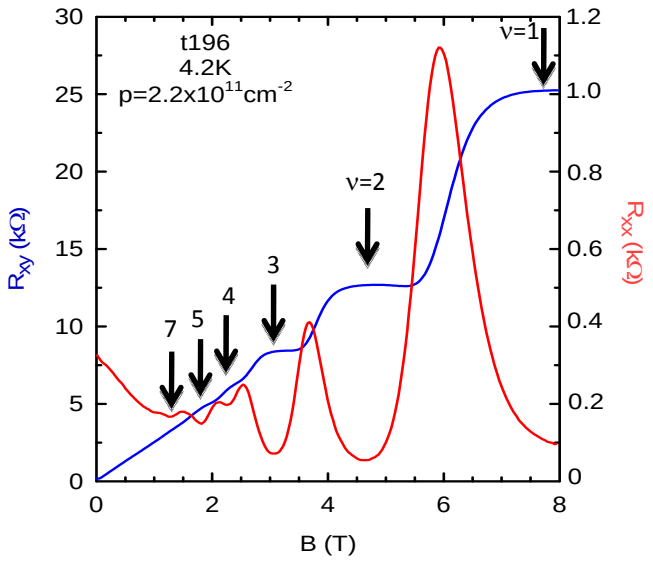


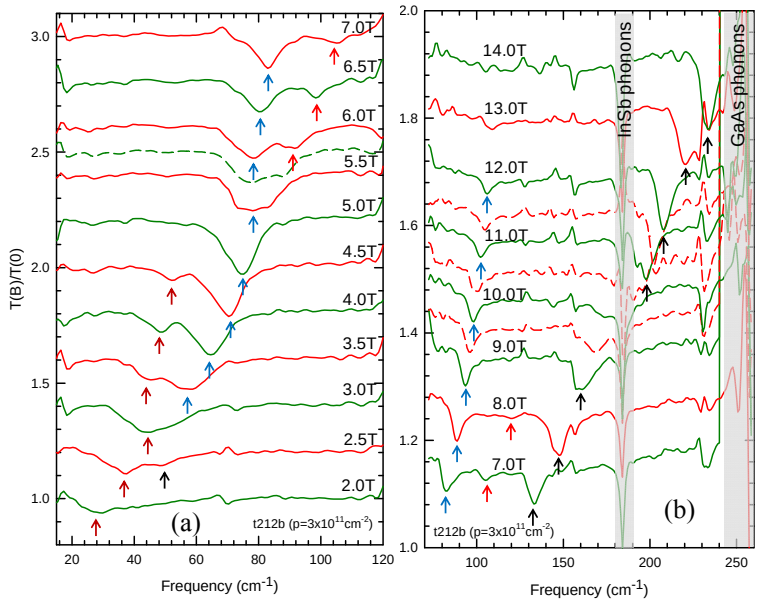
Figure 4.9 Transverse and longitudinal resistance of a p-type InSb QW (t196) at 4.2K.

4.6 Determination of hole mass

Magneto-optical measurements are useful tools for understanding the band structure of holes in InSb quantum wells (QWs). A Fourier Transform Infrared (FTIR) spectrometer is used to induce transitions between levels in a QW at low temperature. Minima in the transmission spectrum are observed at the transition energies. The experiments are performed in the Faraday geometry, where the direction normal to the plane of the QW is parallel to the direction of the applied magnetic field and the propagation direction for the incident radiation. This geometry enables cyclotron resonance transitions (from an occupied Landau level to a neighboring unoccupied Landau level with the same spin and in the same subband) in doped QWs.

Cyclotron-resonance results for *p*-type InSb QWs with different strain and doping parameters were obtained [26]. Examples of the transmission spectra are shown in Figure

4.10. At fields less than 4T, a hole effective mass of 0.04 to 0.09m_o is deduced for densities of 2 to $5\times10^{11}cm^{-2}$, which is up to a factor of 5 smaller than observed in p-type $In_xGa_{1-x}As$ QWs and suggests that higher hole mobilities are possible.



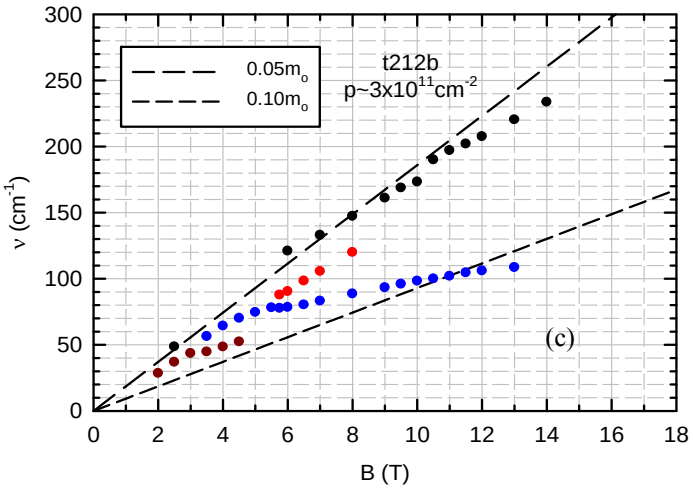


Figure 4.10 Normalized transmission spectra for cyclotron resonance transitions in a 2D hole system in an InSb QW at a temperature of 4.2K. a) Data taken using a mercury lamp, b) data taken using a globar, c) observed resonance frequencies as a function of applied magnetic field.

Chapter 5

Geometrical Magnetoresistors

5.1 Introduction

Magnetic sensors have diverse applications such as proximity sensors, gear-tooth sensors and read heads. There are two types of magnetic sensors made from semiconductors or layered magnetic materials. These are Hall-effect sensors and magnetoresistors. Magnetoresistors come in different types: Anisotropic magnetoresistors (AMR), giant magnetoresistors (GMR), tunneling magnetoresistors (TMR) and colossal magnetoresistors (CMR). These have a physical or material dependent electrical resistance that is sensitive to an externally applied magnetic field. There is another type of magnetoresistor called a geometrical magnetoresistor, where the magnetic field sensing mechanism depends on the geometry of the device.

The classical geometrical magnetoresistors, shorted Hall bars and Corbino disks, are unusable in magnetic recording technology because of their negligible sensitivity at small magnetic fields (~0.05T). The magnetic field, however, in many electronic or mechanical applications is in the range of 0.01 to 0.3T [15].

Most of the commercial sensors in the automotive industry, like Hall sensors and shorted Hall bars, are made of thin semiconductor films. In geometrical magnetoresistors such as shorted Hall bars, the change in resistance is a function of mobility squared when the product of the mobility (μ) and the magnetic field (B) is small ($\mu B<0.45$). Because of a high room-temperature electron mobility, narrow bandgap semiconductors, including InSb, InAs and HgCdTe are attractive materials to use as a geometrical magnetoresistors.

The geometrical magnetoresistance effect in shorted Hall bars is also a useful way to determine the carrier mobility of a semiconductor material.

This chapter discusses InSb QW multielement magnetoresistors, their sensitivity to magnetic field, and the extracted electron mobility from the magnetoresistance effect. First, a review is given of research on geometrical magnetoresistance towards future recording technology, issues are discussed concerning narrow-bandgap thin-film semiconductors as magnetoresistors, and high-mobility 2DEG, as a solution to those issues is discussed. Next, an expression for geometrical magnetoresistance and sensitivity will be explained. Then the magnetoresistance effect in magnetoresistors fabricated from InSb QW structures will be discussed.

5.2 A review of geometrical magnetoresistors

New geometries are being investigated for the possible application of semiconductor geometrical magnetoresistors as read heads in future recording technology. Solin *et al.* reported an extraordinary magnetoresistance (EMR) effect in a new geometry where a metallic shunt is embedded within a ring of thin-film narrow-gap semiconductor. A room temperature magnetoresistance of 100% at 0.05 Tesla and 750,000% at 4T was observed in a sensor fabricated from a 1.3μm thick InSb layer [3,4,5]. However it is a challenge to shrink this geometry to nanometer level to use as a read head sensors for ultra-high density hard drives.

Through conformal mapping of the internally shunted semiconductor ring to an externally shunted van der Pauw disk, Solin *et al.* successfully fabricate nanometer-level EMR devices out of InSb QWs [3,6,7,8,9]. The room temperauture EMR was 5% at

0.05T. Metal-semiconductor hybrid structures for EMR were also tried in InAs QWs [12]. Hitachi researchers have further optimized the EMR device structure for reading a narrow bit width and bit length [13].

The magnetic sensor currently used in almost all hard disk drives (HDDs) is the GMR sensor. However, other GMR based devices such as the tunneling magnetoresistor (TMR) are very promising for replacing the GMR sensors in the future scaling down of magnetic recording technology.

Solid state magnetic sensors are popular in the automotive industry. The Corbino disk, which is the extreme of a shorted Hall bar with an infinite width, has the highest geometrical MR effect, but has no practical applications because of low resistance [1], and consequently large power dissipation. To increase the resistance and decrease the power dissipation several shorted Hall bars are connected (multi-element magnetoresistors) in commercially available magnetoresistive sensors. The required practical resistance is in the order of 100-3000Ω [15]. Some of the magnetoresistive sensors incorporate a permanent magnet to bias the sensing field. Major manufacturers of semiconductor MR sensors are Murata [16] and Asahi-kasei EMD corporation [17]. Their MR sensor products are magnetic pattern recognition sensors and rotary sensors made of thin InSb layers.

The best candidates for magnetoresistors are narrow gap semiconductors, since the electron mobility is high in these materials. The drawback of the small band gap, however, is a strongly temperature dependent intrinsic carrier concentration; especially at and above room temperature. To reduce of this effect, the semiconductors are doped at a concentration above the intrinsic concentration. The disadvantages of this technique are

reduced electron mobility due to ionized dopant scattering and low resistance (high conductivity). Low resistance causes higher power consumption and is undesirable because of high heat dissipation. The sensitivity of MR sensor is lowered by the reduced mobility. Increasing the number of series elements increases the resistance, but also increases the device size. The other possibility is to decrease the layer thickness. In heteroepitaxial films, this is not a good solution due to the low electron mobility. A large dislocation density results from a large lattice mismatch between substrate and the epilayer. However, Asahi-kasei has improved the temperature sensitivity of MR devices by fabricating Sn doped InSb compared to Te doped InSb.

An ideal solution is a magnetoresistor made from remotely-doped QWs containing 2DEGs. The electron density in the 2DEG can be made large without greatly reducing the mobility. Another advantage of the 2DEG is its nearness to surface, which can increase the MR's sensitivity. A 2DEG at an InAs/inversion layer was used in magnetoresistors made by Heremans *et al.* [18]. They observed a maximum operation temperature as high as 300 °C, but the sensitivity was less than in InSb thin films. Behet *et al.* [19,20] investigated InAs/AlGaSb quantum-well MR sensors. They fabricated both Corbino disks and shorted Hall bars. They confirmed the electron mobility of 30,000 cm^2/Vs deduced from van der Pauw measurements by curve fitting the experimental data to the theoretical equation. Moreover, they reported a current sensitivity of 1,200 Ω/T and a voltage sensitivity of 1.75 T^{-1}.

5.3 Geometrical magnetoresistance in a short wide Hall element

A large magnetoresistance arises in a semiconductor Hall bar when its width (W) is much larger than its length (L), as schematically shown in the Figure 5.1. A magnetic field (B) is applied normal to the plane of the semiconductor slab. A current (I) passes through the two electrodes. In this geometry, the Hall voltage is not fully developed to balance the Lorentz force [14] (the length is not long enough). Carriers make an angle θ to the applied electric field. In homogeneous, non-magnetic materials with a single type of charge carrier, the angle θ can be expressed as $tan\theta=\mu B$ [15], where μ is the carrier mobility. The longer path, $L/cos\theta$, of carriers leads to a higher resistance $R(B)$ with respect to the zero magnetic field resistance $R(0)$.

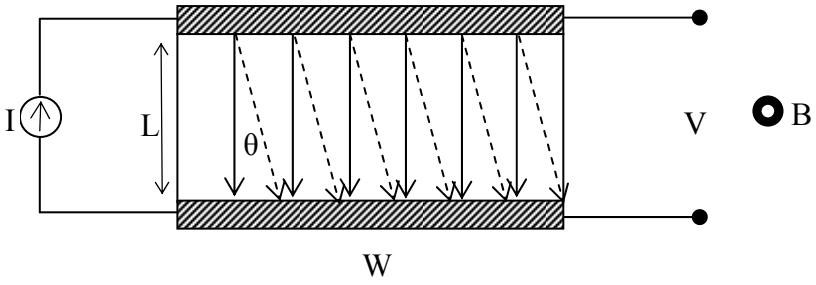


Figure 5.1 A schematic diagram of a short wide Hall bar, also known as a shorted Hall bar. Solid arrows show the zero field current path and dashed arrows show the current path under a perpendicular magnetic field, B.

An expression for magnetoresistance can be deduced as follows;

$$R(0)=\frac{\rho_0 L}{WT};\ \rho_0 \text{ is the zero field resistivity.} \qquad 5.1$$

$$R(B)=\frac{\rho_B L}{WT\cos\theta}\ ;\ \ \rho_B \text{ is the effective resistivity.} \qquad 5.2$$

The effective resistivity can be derived using the conductivity tensor;

$$\overline{J} = \frac{\sigma_0}{1+\mu^2 B^2}\begin{bmatrix} 1 & -\mu B \\ \mu B & 1 \end{bmatrix}\overline{E} \qquad 5.3$$

Since there is no Hall voltage E_y=0. The magnitude of the current density

$$|j| = \frac{\sigma_0}{\sqrt{1+\mu^2 B^2}}|E_X| \qquad 5.4$$

and the effective resistivity is,

$$\rho_B = \rho_0\sqrt{1+\mu^2 B^2} \qquad 5.5$$

Therefore transverse electric field is,

$$E_X = \frac{V}{L} \qquad 5.6$$

And plugging

$$\tan\theta = \mu B \quad ; \quad \cos\theta = \frac{1}{\sqrt{1+\mu^2 B^2}} \qquad 5.7$$

into the Equation 5.2 gives

$$R(B) = \rho_0\sqrt{1+\mu^2 B^2}\,\frac{L}{WT}\sqrt{1+\mu^2 B^2} \qquad 5.8$$

$$R(B) = R(0)(1+\mu^2 B^2) \qquad 5.9$$

A geometry dependent correction factor *G* is introduced for finite values of the width to length ratio.

$$\frac{R(B)}{R(0)} = \left(1 + G(W/L)\mu^2 B^2\right) \qquad 5.10$$

By using the conformal mapping technique, an expression for *G(W/L)* was calculated by Lipmann and Kurtz [16]. The expression when $L/W \leq 0.35$ and $\mu B \leq 0.45$ is, $G(W/L) = (1-0.5428L/W)$.

The highest magnetoresistance is observed in an infinitely wide device. The Corbino geometry shown in Figure 5.2 is equivalent to an infinitely wide Hall device.

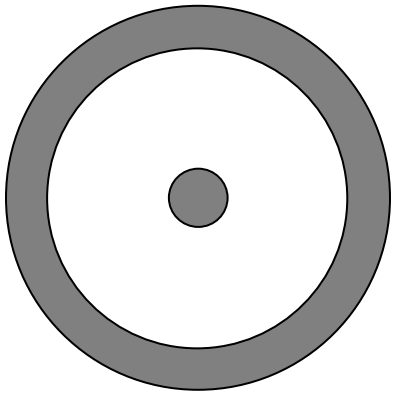


Figure 5.2 A schematic of a Corbino disk which is equivalent to an infinitely wide Hall bar.

The carrier mobility in a semiconductor material or QW can be deduced by fitting Equation 5.10 to the experimental relative resistance $R(B)/R(0)$. Sensitivity is an important figure of merit for a sensor. The current sensitivity (S_i) of a magnetoresistor in constant current mode is defined as;

$$S_i = \frac{1}{I}\frac{dV}{dB} = \frac{dR(B)}{dB}\left(\frac{\Omega}{T}\right) \tag{5.11}$$

$$S_i = 2R(0)\mu^2 B(1-0.5428\frac{L}{W}) = 2N_{el}\rho(0)\frac{L}{W}\mu^2 B(1-0.5428\frac{L}{W}) \tag{5.12}$$

Voltage sensitivity (S_v) (when a constant applied voltage drives the current) is defined as;

$$S_v = \frac{1}{V}\frac{dV}{dB} = \frac{1}{R(0)}\frac{dR(B)}{dB} \tag{5.13}$$

$$S_v = 2B\mu^2(1-0.5428\frac{L}{W}) \tag{5.14}$$

5.4 InSb multi-element magnetoresistors (Shorted Hall bars)

5.4.1 Device processing

A standard optical photolithography technique was used to define the magnetoresistor devices. First, the Hall bar mesa was defined using a positive photolithography technique where the resist-coated area exposed to ultraviolet (UV) radiation is soluble in a developer. Wet chemical etching was performed to remove uncovered areas of the MBE grown material, thus defining the Hall bar mesa. After removing the photoresist, contact pads and metal shunts in the middle of the Hall bar were defined using a negative photolithography technique where the UV exposed area is non-soluble in a developer. Then a metal (In or Ti/Au) is evaporated and the metal on the unexposed regions is removed. The defined area is the metal contact pads and metal strips in the middle of the Hall bar.

Using a specially designed dicing set-up, devices were separated without damaging the metal strips in the middle of the Hall bar. Separated individual multi-element geometrical magnetoresistors, or shorted Hall bars, were then annealed in a forming gas environment (80% Nitrogen and 20% Oxygen) at 230°C for 5 minutes. Annealed devices were then mounted on a plastic chip carrier (PLCC) using silver paste. Gold wires were bonded for current (I) and voltage (V) leads. A processed InSb QW multielement magnetoresistor is shown Figure 5.3.

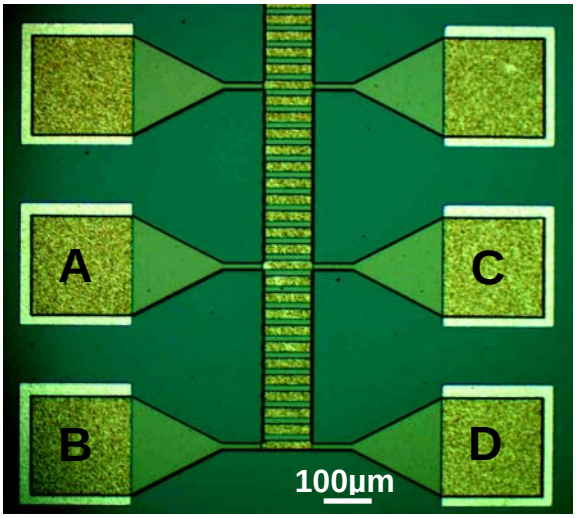


Figure 5.3 A multi-element magnetoresistor fabricated from an InSb QW.

Magnetoresistors with different width (W) to length (L) ratios were fabricated from several InSb QW wafers. The defined widths of the Hall bars using the photolithography mask were not obtained after the wet etching due to isotropic etching (both vertical and horizontal etching). After performing wet chemical etching with a ~0.5µm/min etch rate, aiming for 3µm of vertical etching, ~5µm from horizontal etching also occurred. This resulted in a Hall bar that was 90µm wide instead of 100 µm wide.

5.5 Experimental issues

While ramping the magnetic field up to 0.21 T in 100 steps, the voltage drop was measured between leads C and D (Figure 5.3). The current passing through leads A and B is 100 nA (Figure 5.3). Magnetic field dependent resistance $R(B)$ values are plotted in Figure 5.4 for up ramped (0 to 0.21T) and down ramped (0.21T to 0) magnetic fields. The magnetoresistor device consists of eleven magnetoresistors in series. The width to length ratio is 9. Resistances taken during up and down ramping of magnetic field are different. The difference is found to be a result of a resistance drop of the device with the time. The

resistance starts to drop after inserting the stainless steel shield to cover the device. It takes around 48 hours to stablize the resistance of a device. However, the measurements were taken without waiting for stabilization of resistance. The magnetoresistance data taken during the up ramped magnetic field gave a lower mobility than the down ramped data as will be seen in Section 5.5. This is because of the relative magnetoresistance ($R(B)/R(0)$), which is lower for up ramped and higher for down ramped magnetic field.

The magnetic field is not zero when the power supply to the magnet is turned off. Raising the device above the poles of the electromagnet gives the exact zero field resistance. If you lower the device to the magnetic field fast enough, it is observed that there is no significant difference between the real zero field resistance value and the first resistance reading of the magnetic field ramping data. Otherwise a decrease of resistance with time may give a different zero field resistance.

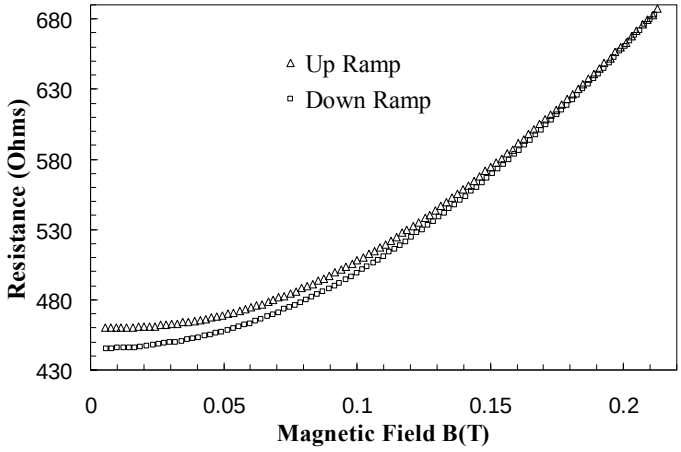


Figure 5.4 Magnetic field vs. resistance of a magnetoresistor device. The magnetoresistor device consists of 11 shorted Hall bars in series with a width to length ratio of 9.

The semiconductor areas under the metal deposited rectangle strips in the middle of the Hall bars were expected to have negligible resistivity after thermal annealing. The resistivity of the metal deposited area was calculated using the Equation 5.15. The zero field resistance *R(0)* of a multi-element magnetoresistor device can be expressed using the dimensions of the magnetoresistor device,

$$R(0) = \rho_{MR} \frac{L \times N}{W} + \rho_S \frac{L \times (N+1)}{W} \qquad 5.15$$

Where ρ_{MR} and ρ_S are resistivities of an active magnetoresistor area and an area under a metal strip, respectively. W is the width of the Hall bar and L is the length of a magnetoresistor. N is the number of magnetoresistor elements in series in between the current and voltage contact pads. Equation 5.15 assumes that the resistivity of the material under every metal area is the same for a given multi-element magnetoresistor device. The calculated metal area resistivity of several magnetoresitor devices is summarized in Table 5.1. The semiconductor area resistivity (ρ_{MR}) was assumed to be 286 Ω/□ , 411 Ω/□ or 405 Ω/□ for three different devices. The metal area resistivity is 12% to 50% of ρ_{MR} and varies from device to device. Hence, the experimentally measured magnetoresistance includes some non-negligible series resistance from the semiconductor area covered by metal.

Different metals were used to improve the metallic behavior and metal diffusion uniformity. In addition to In, Ti and Pd were studied. A thin Au layer was deposited on top of a Ti or Pd layer. The calculated series resistance showed a similar behavior to In. The magnetoresistance effect was not observed to be dependent on the metal used.

W/L ratio	Average resistivity of metal deposited area; ρ_s(Ω/□)			
	t127 ρ_{MR}=286 Ω/□	t171 ρ_{MR}=411 Ω/□	t233 ρ_{MR}=405 Ω/□	
	In	In	In	Ti/Au
9	36	75	182	148
4.5	152	104	196	167
3.5	120			
3	135	132		

Table 5.1 Average resistivity of the material under metal deposited area of several magnetoresistor devices.

The Equation 5.10 is corrected for non-negligible series resistance from the area under the metal. The experimental zero field resistance $R(0)$ and the resistance at a magnetic field $R(B)$ are sums of both resistance from the active area (R_{MR}) and some series resistance (R_s) from the metal covered areas.

$$R(0) = R_{MR}(0) + R_S(0) \tag{5.16}$$

$$R(B) = R_{MR}(B) + R_S(B) \tag{5.17}$$

The normalized experimental magnetoresistance can be expressed as,

$$\frac{R(B)}{R(0)} = \frac{R_{MR}(B) + R_S(B)}{R_{MR}(0) + R_S(0)} \tag{5.18}$$

If it is assumed that the semiconductor under the metallic area behaves similarly to the active area in a magnetic field, then Equation 5.18 can be written as;

$$\frac{R(B)}{R(0)} = \frac{R_{MR}(0)(1+\mu_1^2 BG_1) + R_S(0)(1+\mu_2^2 BG_2)}{R_{MR}(0) + R_S(0)} \tag{5.19}$$

$$\frac{R(B)}{R(0)} = 1 + \frac{R_{MR}(0)\mu_1^2 BG_1}{R_{MR}(0) + R_S(0)} + \frac{R_S(0)\mu_2^2 G_2}{R_{MR}(0) + R_S(0)} = 1 + C_1\mu_1^2 BG_1 + C_2\mu_2^2 BG_2 \tag{5.20}$$

$$\text{where } C_1 = \frac{R_{MR}(0)}{R_{MR}(0) + R_S(0)}\ ,\ C_2 = \frac{R_S(0)}{R_{MR}(0) + R_S(0)} \text{ and } C_1 + C_2 = 1 \tag{5.21}$$

If the mobility of the metal covered area (μ_2) is much smaller than the active area mobility, then the last term of the Equation 5.20 can be neglected. The values of $R_{MR}(0)$ and $R_S(0)$ for each device can be calculated using Equation 5.15, assuming the resistivity of the active area is the same as the resistivity obtained from van der Pauw measurements performed for a simple square geometry.

5.6 Results and discussion

5.6.1 Electron mobility

The geometry dependent magnetoresistance of a magnetoresistor device fabricated from an InSb QW structure (t127) is shown in Figure 5.5. The t127 structure has an electron mobility of 39,700cm^2/Vs and electron density of 5.5×10^{11}cm^{-2} at room temperature. A maximum geometrical magnetoresistance of 53% was observed at 0.21T in a device with a *W/L* ratio of 9. The theoretical (Equation 5.14) geometry dependent magnetoresistace data for a 38,000 cm^2/Vs electron mobility is shown in Figure 5.6. A 60% magnetoresisitance is expected from a device with *W*/*L*=9 at 0.21 T. A lower magnetoresistance is observed experimentally than is theoretically predicted. This is partially due to the series resistance from the lower-mobility metal-deposited area. A lower magnetoresistance effect can also be expected from the device processing. Epilayer degradation during the device processing can reduce the InSb QW electron mobility. However, the room temperature electron mobility, resistivity and electron density observed from a processed 90μm Hall bar from structure t171 were comparable to values observed from an unprocessed simple square van der Pauw geometry.

In the experimental magnetoresistance data, the device with W/L=3 showed a higher MR effect than when W/L=3.5. The device with W/L=3.5 has a higher zero field resistance. The large zero field resistance is due to the small Hall bar width (35 μm). The devices with W/L=9, 4.5 and 3 are 90μm wide (W) and processed on the same piece of wafer t127. The devices with W/L=3.5, 1.75 and 1.16 are 35μm wide and processed on another piece of wafer t127. Two sets of devices separately followed the geometry dependent behavior. However, the devices with the lower Hall bar width showed a large series resistance compared to the zero field resistance, which is also indicated by the lower C_1 value in Table 5.2. The large effect from the low mobility areas has lowered the magnetoresistance of the device with W/L=3.5.

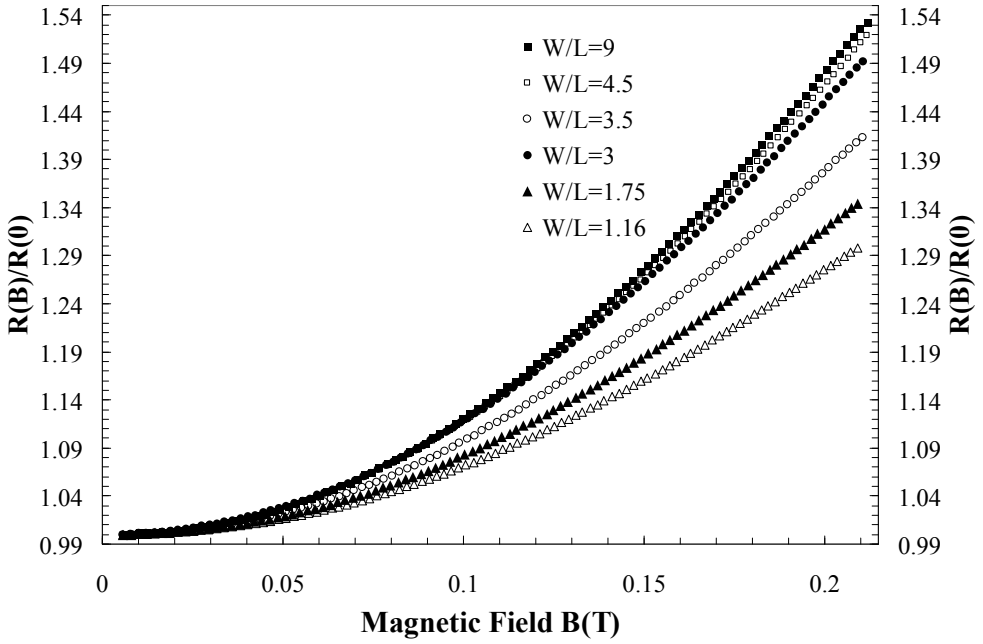


Figure 5.5 Geometry dependent magnetoresistance effect of multi-element magnetoresistor devices fabricated from InSb QW wafer t127 with various width to length ratios.

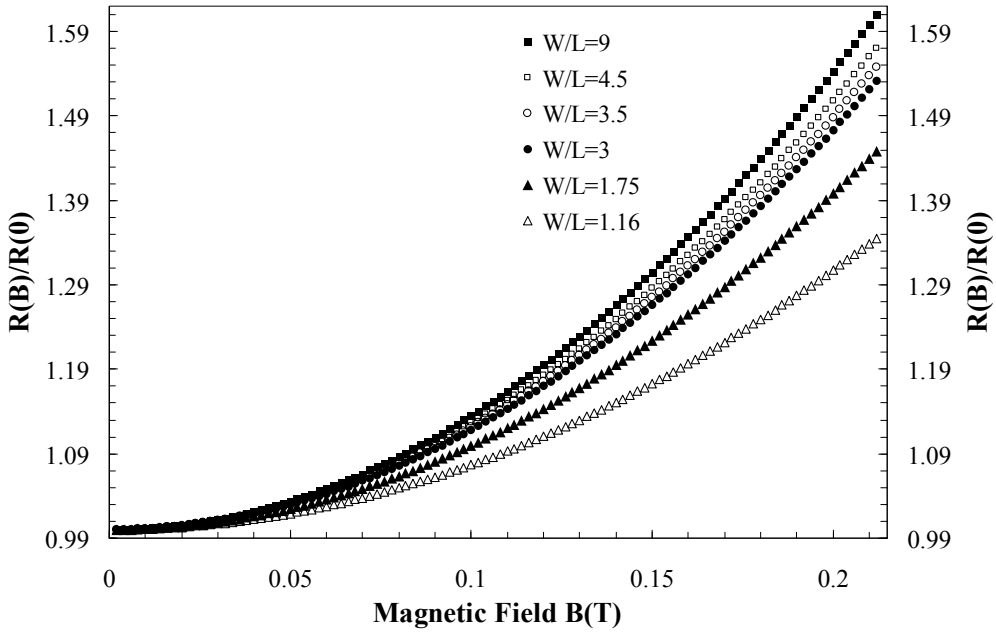


Figure 5.6 Theoretically calculated geometrical magnetoresistance (Equation 5.10). The calculation was performed assuming an electron mobility of 38,000 cm^2/Vs.

W/L ratio	Sweep direction of the magnetic field	$R(0)$	ρ_S	C_1	Mobility from eq. 5.17 (cm^2/Vs)		Mobility with magnetic field independent series resistance (cm^2/Vs)		Mobility with magnetic field dependent series resistance (cm^2/Vs)	
9	up	460	38	0.76	32,500	34,050	37,400	38,800	37,000	38,500
	down	445	33	0.78	35,600		40,200		40,000	
4.5	up	907	158	0.63	32,900	34,550	41,200	42,700	40,700	42,750
	down	879	145	0.65	36,200		44,300		44,800	
3.5	up	1800	138	0.50	32,200	32,900	45,500	46,350	44,100	44,950
	down	1779	131	0.51	33,600		47,200		45,800	
3	up	913	121	0.73	36,300	37,100	42,400	43,200	42,100	42,900
	down	901	118	0.74	37,900		44,000		43,700	

Table 5.2 Mobility extracted from linear curve fitting of the experimental data taken from magnetoresistors fabricated from InSb QW wafer t127.

W/L ratio	Sweep direction of the magnetic field	$R(0)$	ρ_S	C_1	Mobility without considering series resistance		Mobility with magnetic field independent series resistance (cm^2/Vs)		Mobility with magnetic field dependent series resistance (cm^2/Vs)	
9	up	726	77	0.69	33,200	34,150	39,900	40,850	39,500	40,450
	down	712	73	0.70	35,100		41,800		41,400	
4.5	up	1070	117	0.77	30,600	33,650	34,900	37,850	34,700	37,650
	down	1012	90	0.81	36,700		40,800		40,600	
3	up	1195	132	0.80	32,800	32,800	36,600	36,600	36,200	36,200

Table 5.3 Mobility extracted from linear curve fitting of the experimental data taken from magnetoresistors fabricated from InSb QW wafer t171.

The mobility was extracted by curve fitting Equations 5.14 and 5.20 to the experimental data taken at low magnetic fields (0 to 0.1T). Equation 5.20 was used with and without the last term. Figure 5.7 shows the curve fitted data (solid line) and the experimental data (open circles) for W/L=9 and W/L=3.5 (other geometries were omitted for clarity). The curve fitting was performed assuming that the series resistance is dependent on the magnetic field and the field dependence is similar to a semiconductor area. Table 5.2 summarizes the electron mobilities of several devices fabricated from

wafer t127. Table 5.3 summarizes the mobilities of several devices fabricated from wafer t171.

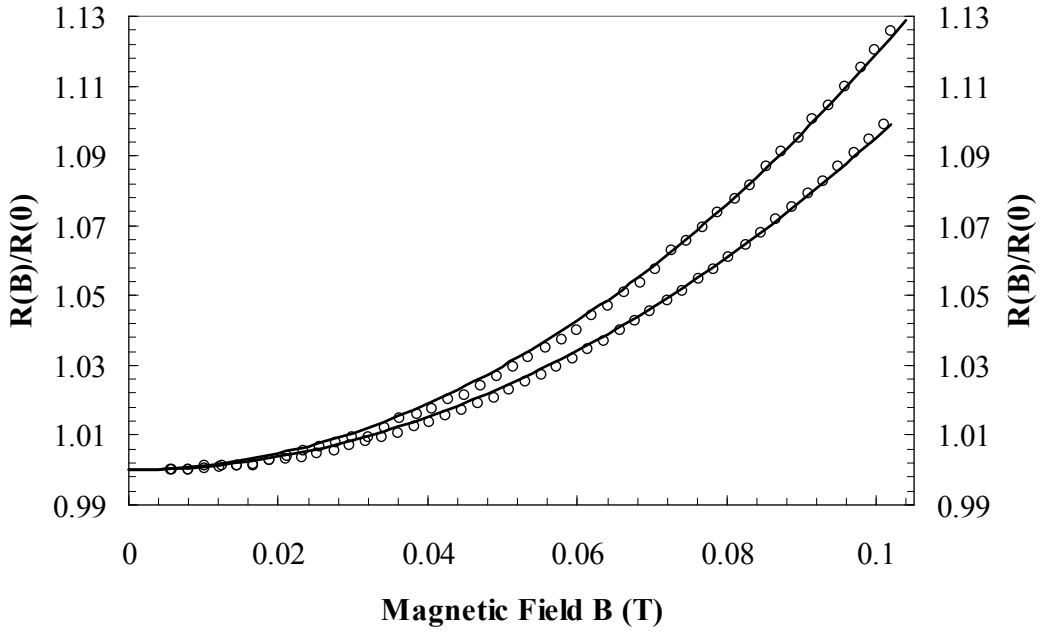


Figure 5.7 Curve fitted and experimental relative magnetoresistance of multi-element magnetoresistors with width to length ratios of 9 and 3.5. Open circles are experimental results and solid lines are theoretical fittings.

As a result of the resistance drop with the time, the data taken during ramping up the magnetic field gave lower mobility than down ramping data. The mobilities extracted without considering the series resistance from the metal covered areas are lower than the mobility observed from the Hall measurements. The electron mobility (density) deduced from Hall measurements of wafers t127 and t171 are 39,700cm^2/Vs ($5.5\times10^{11}cm^{-2}$) and 38,800cm^2/Vs ($4.6\times10^{11}cm^{-2}$) respectively. The mobility extracted when considering magnetic field independent series resistance was slightly larger when magnetic field dependent series resistance was considered.

The high quality device (in terms of lower series resistance) which is closest to an ideal magnetoresistor has a large C_1 value (closer to 1). From devices fabricated from wafer t127, large C_1 values were observed with W/L=9 and W/L=3. Before correcting for series resistance, these two devices gave 34,000 cm^2/Vs and 37,000 cm^2/Vs for an average electron mobility, respectively. After correcting for series resistance, these two devices gave 38,500 cm^2/Vs (3% lower) and 42,900 cm^2/Vs (8% higher) average electron mobility, respectively. The fitting gave 8,000 cm^2/Vs and 8,500 cm^2/Vs for the mobilities in the metal deposited area.

The devices fabricated from wafer t171 had slightly lower mobility than devices from wafer t127 according to the fittings. The behavior is as expected when compared to the results from conventional Hall effect measurements. The up ramped data of the device with W/L =4.5 gave a lower mobility. The resistance measured during ramping up of the magnetic field for the device with W/L =4.5 showed a fast resistance drop at lower magnetic field. The result is a bowing of resistance before it starts to increase with the magnetic field. The fittings gave relatively lower mobilities for the data taken for that device as shown in the Table 5.3.

5.6.2 Sensitivity of the InSb QW magnetoresistor

The sensitivity of InSb QW magnetoresitors is an important figure of merit for magnetic sensing applications in which high sensitivity is required. Current sensitivity values for 330 μm long and 90 or 35μm wide magnetoresistor devices at 0.1 T and 0.19 T is summarized in Table 5.4. According to Equation 5.12, the current sensitivity S_i of magnetoresistor devices fabricated from material with the same mobility depends on the

zero field resistance and the *W*/*L* ratio. All the 35μm wide devices showed higher sensitivity compared to 90μm wide devices. This is because the zero field resistance is higher for narrow Hall bars. The highest sensitivity was observed from a 35μm wide device with 11 elements and a *W*/*L* ratio of 3.5. This is possibly due to the large *W*/*L* ratio (3.5 is the highest *W*/*L* ratio device among all 35μm wide devices) and the large number of devices in series for the given device length (330 μm).

A large *W*/*L* ratio gives a large magnetoresistance effect (smaller edge effects). At the same time a large *W/L* ratio reduces the zero field resistance. There is some optimized W/L ratio that maximizes the current sensitivity of a magnetoresistor. The series resistance from metal deposited areas can also lower the sensitivity to a magnetic field. 10-100 times lower contact or series resistance is preferential to avoid sensitivity degradation [18]. However, magnetoresistors with narrower Hall bar width (*W*) with some optimized *W/L* ratio will give a higher sensitivity for device applications.

Sample #	Width of the Hall bar(μm)/No. of elements in series (N)	Average zero field resistance; R(0)(Ω)	W/L Ratio	Average Current Sensitivity; Si (Ω/T)	
				B=0.1 Tesla	B=0.19 Tesla
t127	90/11	400	9	1,000	2,100
	90/9	800	4.5	2,200	3,600
	35/11	1,800	3.5	3,600	**6,000**
	90/7	900	3	2,000	3,500
	35/9	2,300	1.75	**3,800**	5,200
	35/7	2,200	1.16	3,400	5,600
t171	90/11	720	9	1,500	3,200
	90/9	1,000	4.5	2,200	3,900
	90/7	1,200	3	2,200	4,300

Table 5.4 Current sensitivity of 330 μm long and 90 or 35 μm wide multi-element magnetoresistor devices at 0.1 T and 0.19 T.

Table 5.5 summarizes the current sensitivities of narrow gap semiconductor geometrical magnetoresistors found in the literature. InSb epilayer magnetoresistors showed a 6,700 Ω/T sensitivity with 20 elements in series (the device dimensions are unknown). An InSb QW magnetoresistor with W/L=3.5 and 11 element in series showed about 6,000 Ω/T current sensitivity. The sensitivity can doubled by increasing the number of elements in series to 22. But at the same time, an increase in the number of elements increases the device size. Lowering the width of the Hall bar and finding good metallization with lower series resistance will further increase the sensitivity.

	S_i (Ω/T)	W/L	B(T)	No. of elements
InAs epilayer magnetoresistor [15]	4000	-	0.19	-
InSb epilayer magnetoresistor [15]	6700	~2	0.19	>20
InAs QW magnetoresistor [20]	195	infinite	0.15	1
InSb QW magnetoresistor [this study]	**6034**	**3.5**	**0.19**	**11**

Table 5.5 Current sensitivities of devices made from narrow gap semiconductors.

The high mobility shallow InSb QW magnetoresistors demonstrate the potential for magnetic sensing applications.

Chapter 6

Conclusions and suggestions for future work

In the first half of the dissertation, our approaches to minimize structural defects in InSb QW structures was discussed. It was observed that the $Al_xIn_{1-x}Sb/Al_yIn_{1-y}Sb$ interfaces of an interlayer buffer were effective in reducing threading dislocations. A 1.6μm thick $Al_{0.12}In_{0.88}Sb$ epilayer with three $Al_{0.24}In_{0.76}Sb$ interlayers had a similar threading dislocation density ($6.0\times10^8 cm^{-2}$) to a twice thicker $Al_{0.12}In_{0.88}Sb$ epilayer without interlayers. A 1.6μm thick $Al_{0.12}In_{0.88}Sb$ epilayer without interlayers had a ~ 4 times higher threading dislocation density. The use of a 2° off-cut GaAs substrate was effective in reducing the density of microtwins. The microtwin density at a QW grown on a 2^0 off-cut GaAs (100) is typically ~100 cm^{-1}, a factor of ~80 smaller than for growth on an on-axis substrate.

A method of forming thicker QWs with high barriers through strained-balanced heteroepitaxy was introduced and successfully applied to InSb QW structures on GaAs substrates. A combination of all the techniques gives a typical electron mobility of 40,000cm^2/Vs at room temperature with an electron density of $4\times10^{11} cm^{-2}$ in 20nm-thick InSb QWs with $Al_{0.2}In_{0.8}Sb$ barriers.

The strain-balanced technique is necessarily to obtain a thick QW with high potential barriers and positioned at less than ~50nm from the surface, features which are often advantageous in device applications. However, this requires a narrow separation between the dopants and the QW. A method for growing InSb QW structures with $Al_xIn_{1-x}Sb$ barriers larger than ~50nm will be beneficial for additional scientific and device

applications. It is reported in the literature that microtwin formation depends on the terrace size of the vicinal substrate. Finding an optimized vicinal angle for a minimum twin density in the InSb/GaAs system should further improve the transport properties of InSb QWs. Integration of the optimized buffer and the strain-balanced InSb QW structure on a Si substrate via an AlSb nucleation layer may demonstrate better performance than other III-V semiconductor QWs grown on Si substrates.

Two-dimensional hole systems in InSb QWs were realized by doping the barrier layers with Be instead of Si and altering the biaxial strain in the QW via a metamorphic buffer. The highest room-temperature hole mobility from a *p*-type InSb QW (700 cm^2/Vs with $9\times10^{11}cm^{-2}$ hole density) is higher than the observed in $In_xGa_{1-x}As$ QWs but lower than in $In_xGa_{1-x}Sb$ QWs. The highest low temperature (20K) hole mobility observed from a *p* type InSb QW is 55,000 cm^2/Vs. Further optimization of the doping density, strain in the well and the well thickness is required for further improvement.

The geometrical magnetoresistance data confirmed the high room-temperature electron mobility in InSb QWs grown on GaAs (001) substrates. However, the series resistance from metal deposited areas affected the magnetoresistance. Deduced mobility values are within 14% of the measured Hall mobilities, with no correction for the series resistance. Deduced mobility values are within 3% of the measured Hall mobilities, with a correction for the series resistance. The current sensitivity (6000 Ω/T) of InSb QW devices grown on GaAs compares favorably with other narrow-gap magnetoresistors.

Further optimization of device size and width to length ratio will give high magnetic sensitivity. Better metallization and annealing technique like rapid thermal annealing may improve the metal diffusion and hence lower the series resistance. A

knowledge of the temperature stability of InSb QW magnetoresistors is beneficial for future device applications. All the geometrical magnetoresistor devices were fabricated using InSb QWs positioned at 50nm from the surface. However a comparison of sensitivity of those magnetoresistors with magnetoresistors fabricated from a deeper QW structure would be useful.

From the research conducted during this dissertation work, we were able to reduce the buffer layer thickness to 1.5μm from 3-4μm. A thinner buffer with low defect density is beneficial for devices fabricated from InSb QWs as well as InSb epilayers grown on GaAs. Improved room-temperature electron mobility was achieved from the thicker but near-surface QWs with higher potential barriers. High electron mobility in InSb QWs and the realization of the first *p*- type InSb QW demonstrate a bright future for InSb as a material for future device technology.

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Appendix A

Glide Plane	Burgers Vector
(111)	$\frac{a}{2}[10\bar{1}]$
(111)	$\frac{a}{2}[01\bar{1}]$
(111)	$\frac{a}{2}[1\bar{1}0]$
$(\bar{1}\bar{1}1)$	$\frac{a}{2}[101]$
$(\bar{1}\bar{1}1)$	$\frac{a}{2}[011]$
$(\bar{1}\bar{1}1)$	$\frac{a}{2}[1\bar{1}0]$
$(\bar{1}11)$	$\frac{a}{2}[101]$
$(\bar{1}11)$	$\frac{a}{2}[01\bar{1}]$
$(\bar{1}11)$	$\frac{a}{2}[110]$
$(1\bar{1}1)$	$\frac{a}{2}[10\bar{1}]$
$(1\bar{1}1)$	$\frac{a}{2}[011]$
$(1\bar{1}1)$	$\frac{a}{2}[110]$

Table A.1 Slip systems in diamond and Zincbende crystals [1].

Appendix B

Cross sectional TEM specimen preparation

1. Cleave two specimens of size 2-3 mm^2 from the wafer.
2. Cleave similar size two dummy specimens from Si or GaAs wafers.
3. After cleaning surfaces, stack and glue the pecimenss and dummies using G1 adhesive.
4. Two pieces from the wafer to be looked at with TEM should be at the middle of the stack and should be glued face to face. Stacking sequence is shown in Figure B.1(a).
5. Put the stack in a vice and put on a hot plate until the glue is hardened.
6. Wire saw the sandwich and make 0.7 mm thick slices as shown in Figure B.1(b).

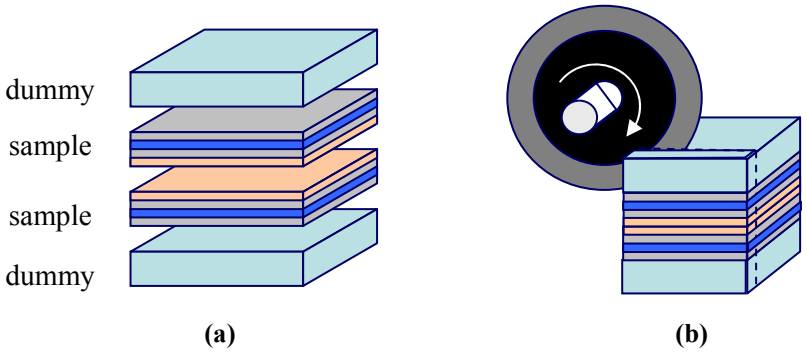

Figure B. 1 (a) Stacking sequence of specimens and dummies (b) Wire saw the adhered stack and make slices.

7. Mechanically polished both sides of the sandwich until its thickness is around 400µm.
8. Mount the 400µm thick specimen slice on a Cu TEM grid and further polish it until the specimen is ~ 100µm.
9. Mount the specimen into the *DIMPLER* and dimple the specimen until the thickness of the specimen is ~10 µm.
10. Mount the specimen into the Gatan Ion Miller (Ar) and ion mill the specimen.

Appendix C

Sample	Buffer layer structure	Upper and lower barrier	InSb QW thickness	Electron mobility and density at 298K		Electron mobility and density at 20K	
				Mobility cm^2/Vs	Density cm^{-2} (Si doping time is seconds)	Mobility cm^2/Vs	Density cm^{-2}
t093	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm	39,000	5.0E+11 (44,35)	101,560	4E+11
t100	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm	35,160	9.5E+11 (90,70)	135,690	7.4E+11
t101	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm	38,890	4.3E+11 (44,35)	100,340	3.2E+11
t109	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm	37,350	8.5E+11 (90,35)	190,000	5E+11
t116	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm	37,790	3.3E+11 (30,20)	91,240	1.9E+11
t117	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm	39,340	3.9E+11 (30,25)	116,080	2.6E+11
t126	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm	39,590	4.6E+11 (30,30)	134,880	3.4E+11
t127	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm	39,660	5.5E+11 (30,35)	140,100	4E+11
t128	1.5 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm	34,520	4.1E+11 (30,30)	74,100	3.2E+11
t129	[0.65 µm $Al_{0.1}In_{0.9}Sb$/0.2 µm $Al_{0.2}In_{0.8}Sb$/0.65 µm $Al_{0.1}In_{0.9}Sb$] = 1.5µm	20nm $Al_{0.2}In_{0.8}Sb$	20nm	39,850	4.2E+11 (30,30)	108,870	3.4E+11
t134	[0.5 µm $Al_{0.1}In_{0.9}Sb$/0.2 µm $Al_{0.2}In_{0.8}Sb$/0.3 µm $Al_{0.1}In_{0.9}Sb$/0.2 µm $Al_{0.2}In_{0.8}Sb$/0.3 µm $Al_{0.1}In_{0.9}Sb$] = 1.5µm	20nm $Al_{0.2}In_{0.8}Sb$	20nm	40,800	4.7E+11 (30,30)	121,430	3.9E+11
t135	[0.2 µm $Al_{0.1}In_{0.9}Sb$/0.2 µm $Al_{0.2}In_{0.8}Sb$/0.2 µm $Al_{0.1}In_{0.9}Sb$/0.2 µm $Al_{0.2}In_{0.8}Sb$/0.2 µm $Al_{0.1}In_{0.9}Sb$/0.2 µm $Al_{0.2}In_{0.8}Sb$/0.3 µm $Al_{0.1}In_{0.9}Sb$/] = 1.5µm	20nm $Al_{0.2}In_{0.8}Sb$	20nm	38490	4.7E+11 (30,30)	104,990	3.8E+11
t138	[0.2 µm $Al_{0.1}In_{0.9}Sb$/0.2 µm $Al_{0.2}In_{0.8}Sb$/0.2 µm $Al_{0.1}In_{0.9}Sb$/0.2 µm $Al_{0.2}In_{0.8}Sb$/0.2 µm $Al_{0.1}In_{0.9}Sb$/0.2 µm $Al_{0.2}In_{0.8}Sb$/0.3 µm $Al_{0.1}In_{0.9}Sb$/] = 1.5µm	20nm $Al_{0.2}In_{0.8}Sb$	20nm	38390	3.7E+11 (30,30)	91,070	3.2E+11
t162	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	25nm	40600	4.5E+11	113,540	3.7E+11
t171	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	25nm	38800	4.6E+11	111,620	3.6E+11
t172	[0.5 µm $Al_{0.1}In_{0.9}Sb$/0.2 µm $Al_{0.2}In_{0.8}Sb$/0.3 µm $Al_{0.1}In_{0.9}Sb$/0.2 µm $Al_{0.2}In_{0.8}Sb$/2.8 µm $Al_{0.1}In_{0.9}Sb$] = 4 µm	20nm $Al_{0.2}In_{0.8}Sb$	20nm	42500	4.0E+11	119,270	3.0E+11

t173	[0.5 µm $Al_{0.1}In_{0.9}Sb$/0.2 µm $Al_{0.2}In_{0.8}Sb$/0.3 µm $Al_{0.1}In_{0.9}Sb$/0.2 µm $Al_{0.2}In_{0.8}Sb$/3.8 µm $Al_{0.1}In_{0.9}Sb$] = 5 µm	20nm $Al_{0.2}In_{0.8}Sb$	20nm	41000	5.0E+11	149,230	4.1E+11
t203	3 µm $Al_{0.05}In_{0.95}Sb$	10nm $Al_{0.2}In_{0.8}Sb$	70nm	37000	1.8E+12	142,980	4.1E+11

Table C.1 Summary of asymmetrically doped shallow InSb QW structures grown on 2^0 off GaAs (001) substrates.

Sample	Buffer layer structure	Upper and lower barrier	InSb QW thickness and spacer layer thickness	Electron mobility and density at 298K		Electron mobility and density at 20K	
				Mobility cm^2/Vs	Density cm^{-2}	Mobility cm^2/Vs	Density cm^{-2}
t148	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm 10nm	29,600	7.3E+11	58,000	6.5E+11
t158	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm 60nm	27,700	9.3E+11	118,800	7.4E+11
t159	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm 60nm	25,000	1E+12	100,000	7.4E+11
t161	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm 10nm	28,700	4.6E+11	38,000	3.8E+11
t164	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm 60nm	31,300	6.2E+11	123,700	3.2E+11
t170	3 µm $Al_{0.1}In_{0.9}Sb$	20nm $Al_{0.2}In_{0.8}Sb$	20nm 60nm	31,100	4.2E+11	102,500	2.5E+11

Table C.2 Summary of symmetrically doped InSb QW structures grown on 2° off GaAs (001) substrate.