A TRANSISTORIZED DECADE RING COUNTER

By

BILLY WAYNE WHITLOW

Bachelor of Science

Oklahoma State University

Stillwater, Oklahoma

1958

Submitted to the faculty of the Graduate School of
the Oklahoma State University
in partial fulfillment of the requirements
for the degree of
MASTER OF SCIENCE
May, 1959

A TRANSISTORIZED DECADE RING COUNTER

Thesis Approved:

Paul A. McCollum
Thesis Adviser

Harold Tristor

Robert MacVicar
Dean of Graduate School

PREFACE

In recent years rapid advances in the field of digital computing has created the need for high-speed ring counters which are small in size and weight, dependable, and require very little operating power. Most ring counters require a switching device which can be triggered "on" by an electrical pulse and remains "on" after the pulse has terminated. Such a switching device is said to be bistable. The most common bistable device is the Eccles-Jordan type which employs, in principle, two active elements, one of which is conducting at all times. This means a decade ring counter, using twenty active elements, will have ten active elements conducting all the time resulting in considerable power consumption. In the following work, a ring counter is developed using a transistor bistable device as the basic building block, which has both active elements conducting at the same time while in the "on" state or both nonconducting while in the "off" state. Using this type of bistable device, only two active elements will be consuming electrical energy at any one time.

The author wishes to express his sincere appreciation to Professor Paul A. McCollum for the guidance and support so generously given in the preparation of this thesis. He also is indebted to Dr. Harold T. Fristoe for his valuable guidance and to his wife, Bonnie, for reading the proof and typing the manuscript.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF PLATES

CHAPTER I

INTRODUCTION

This work is concerned primarily with the study and development of a transistorized decade ring counter employing an asymmetrical bistable circuit as the fundamental building block.

Basically, a ring counter is a series of bistable devices in which only one (usually) is in the "on" or "off" state.[1] If the ring is "closed", the "on" state automatically proceeds from the last stage to the first stage. The ring arrangement is analogous to a stepping switch where each electrical pulse will cause an advance of one step. Some of the important applications[2] include storage in a digital computer, direct counting, measurement of frequency, time, and speed.

Richards[3] describes several types of ring counters in their "block" form using counter components with two stable states. Most of these employ, in principle, some sort of a delay circuit for proper operation. There is one, however, that requires no delay units whatsoever giving rise to a relatively fast and simple counter circuit.

---

[1] R. K. Richards, Arithmetic Operations in Digital Computers, D. Van Nostrand, New Jersey, 1955, p. 205.

[2] Jacob Millman and Herbert Taub, Pulse and Digital Circuits, McGraw-Hill Book Company, Inc. New York, Toronto, London, 1956, p. 344.

[3] R. K. Richards, Op. Cit. p. 206.

It will be seen that no limitations are placed upon the counter operating speed, except for that imposed by transition times of the flip-flop driver and the counter stages themselves. On this basis, it was chosen as the counter to be studied. In the following paragraphs, the theory of operation of this type of counter is discussed without considering the actual circuity involved.

Theory of Operation of The Counter

Let it be assumed that the first bistable stage in the counter of Figure 1 will be in the "on" condition as indicated by the X.

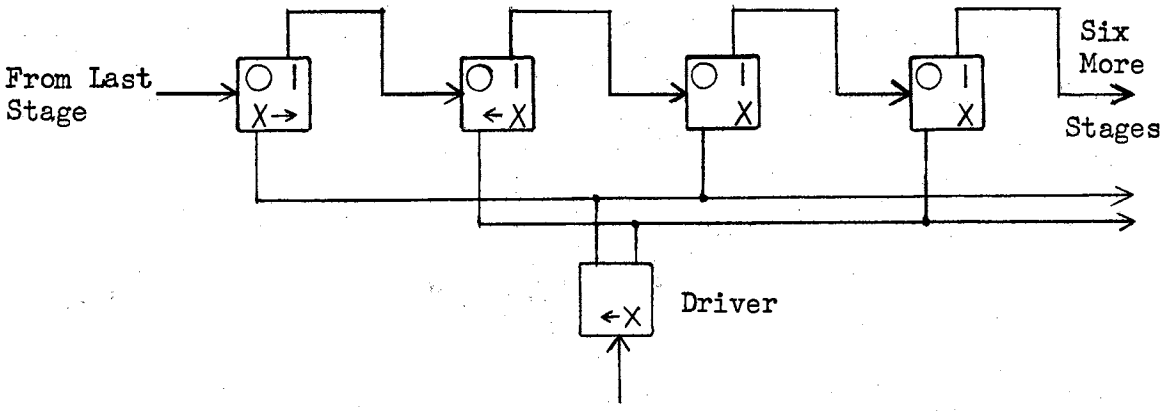


Figure 1. Block Diagram of Ring Counter.

The driver is also a bistable device which will give a positive pulse alternately from each output. Upon the arrival of the first electrical pulse, the left side of the driver will put out a positive pulse to turn off stage number one. Since all other odd stages are initially in the "off" state, they will not be affected. As stage one turns off, it will provide a negative pulse required to turn stage number two on.

As stage two is being turned on, the right side of the driver is delivering a negative pulse to it and all other even stages, but due to circuit design will have no effect. The second electrical pulse received by the driver will cause a positive output on the right side and a negative output on the left. Since no change is caused by a negative pulse, only the positive pulse need be considered. As before, an "on" stage, which is now stage 2, will be turned off and it in turn will trigger the next stage.

Thus for each electrical pulse, the "on" state is caused to advance to the following stage.

The ring counter is a device which, as seen on the preceding page, utilizes pulses for its operation; and since transistors have properties which make them particularily suitable for pulse circuits, they were chosen instead of tubes for circuit design. Transistors also possess relative advantages over tubes in that they are smaller in size and weight; they require no filament power and have an appreciably longer life.

Although point contact transistors have the advantage of a negative input impedance under proper circuit conditions thus affording a "one" transistor bistable device,[4] the junction transistor was chosen because of its availability.

---

[4]R. K. Richards, Digital Computer Components and Circuits, D. Van Nostrand,, New York, 1957, p. 140.

CHAPTER II

CIRCUIT ANALYSIS

Development Of The Basic Bistable Circuit

The initial selection of the basic bistable circuit to be used in the ring counter was based on the fact that if PNP and NPN junction transistors are connected as shown in Figure 2, there exists the basis of a fast switching circuit, because the gain of the regenerative loop is the highest possible.[5] To provide stability in both the "on" condition and "off" condition further refinements were necessary. Referring to Figure 3, it is seen that if both transistors are conducting heavily near the saturated region, the collector to emitter voltage of both transistors will be very small. Under this condition, the bias to both transistors is approximately E_2 in magnitude resulting in a need for base current limiting resistors R_b and R_c. R_a and R_d provide low impedance paths for the collector currents in T_1 and T_2, respectively, during the "on" state. Stability during the "off" state is provided by the difference in supply voltages E_1 and E_2. Assume T_2 to be cut off allowing the collector voltage of T_2 to return to ground. Since no bias is now applied to T_1, it will also be in a low conduction state with only the collector leakage current flowing. Since this current is generally very small, and R_a is in the order of 10 K ohms or less,

---

[5] J. J. Moll, et al,. PNPN Transistor Switches, Proc, IRE, vol 44, pp. 1174-1182, September, 1956.

only a few millivolts will be developed across R_a. Thus it is seen that a voltage ΔV (difference between T_1 and T_2) will be the bias applied to T_2 to hold it in the off state.

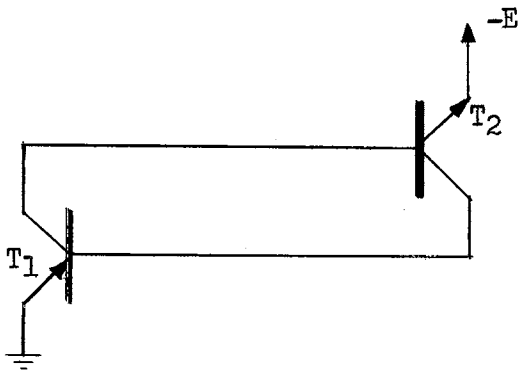


Figure 2. Basic Switching Circuit.

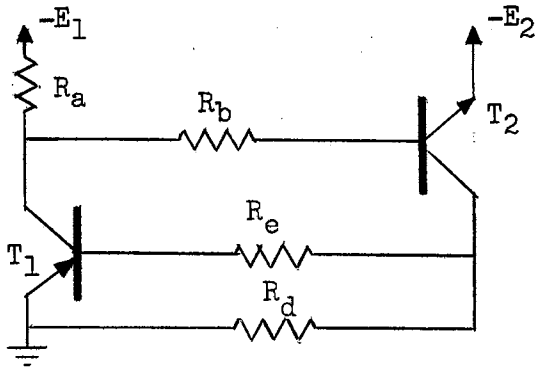


Figure 3. Additional Refinements of Basic Switching Circuit.

The introduction of the base current limiting resistors places a high impedance in the regenerative loop and is a deterrent to fast switching time. This problem may be overcome by bypassing the resistors during the transient period with coupling capacitors C_b and C_c giving the complete basic circuit shown in Figure 4. Experimentation in the laboratory has shown that the capacitors improve the "turn on" time considerably but increases the "turn off" time. If the capacitance is made too large, however, there will be an overshoot of collector voltage of T_2 at "turn on".

For simplification purposes, the transistors are allowed to saturate causing a longer "turn off" time due to minority carrier storage effect. However, this did not present a major problem in the design of the counter because each stage is in the "off" condition nine-tenths of the total cycle of operation.

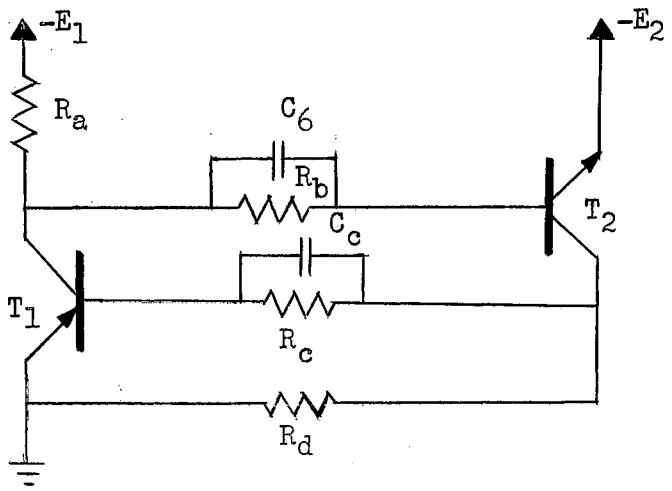


Figure 4. Final Bistable Circuit With Commutating Capacitors.

Because the maximum duty ratio is only 0.1 in the decade counter, considerable power is saved by employing a bistable circuit such as the one now being discussed. Another advantage of having both transistors turned on at the same time is that both a fast negative and a fast positive pulse may be obtained simultaneously. This is not so with the conventional Eccles-Jordan flip-flop for which one of the stable states of both transistors is in the saturated region.

Steady State Analysis of the Basic Counter Circuit

Because the circuit in Figure 5 is regenerative over a wide range of frequencies, including zero, a technique which is useful in analyzing multivibrators[6] may be equally as useful in analyzing the basic circuit employed in the counter. This technique is to open the circuit at some convenient point and calculate a static characteristic of these

---

[6] J. J. Suran and F. A. Reibert, Two Terminal Analysis and Synthesis of Junction Transistor Multivibrators, IRE Transactions, CT3, p. 26, 1956.

terminals, treating the rest of the circuit as a proverbial "black box". Once a static characteristic has been obtained, it is only necessary to insert a resistance representing the proper dc load line to effect the required mode of operation. As later calculations will prove, only two modes of operation will be possible--bistable and monostable.

Initially, the circuit will be assumed to be in the "off" condition. T_2 is biased in the cutoff condition due to a difference in supply voltages E_{b1} and E_{b2}. T_1 is in a low conduction state since I_{b1} is zero and no bias is used to reduce the collector current, I_{c1}, to zero. This initial condition is labeled the "O" point on the static characteristic (see Figure 6). If V_{e1} in Figure 1 is now increased, the base current in T_1 will increase causing the collector current to increase. Since most of the collector current in T_1 flows through R_{L1}, a voltage drop will appear across R_{L1} causing the base current in T_2 to increase. If V_{e1} is made large enough, I_{b2} will eventually increase from its original negative value until T_2 conducts. This is point "P" on the static characteristic. At this point, both transistors become active; the circuit is regenerative and the terminals will now indicate a negative resistance. The emitter current, I_{e1}, will now increase with a decrease in voltage, V_{e1}, until one of the transistors in the regenerative loop becomes saturated causing the loop gain to decrease to a value less than unity. Later results will prove the validity of the assumption that T_1 is the first transistor to saturate. This point of saturation is represented by point "Q" on the static characteristic curve.

Because of the decrease in loop gain, a positive resistance will once more appear at the terminals meaning that V_{e1} must now increase

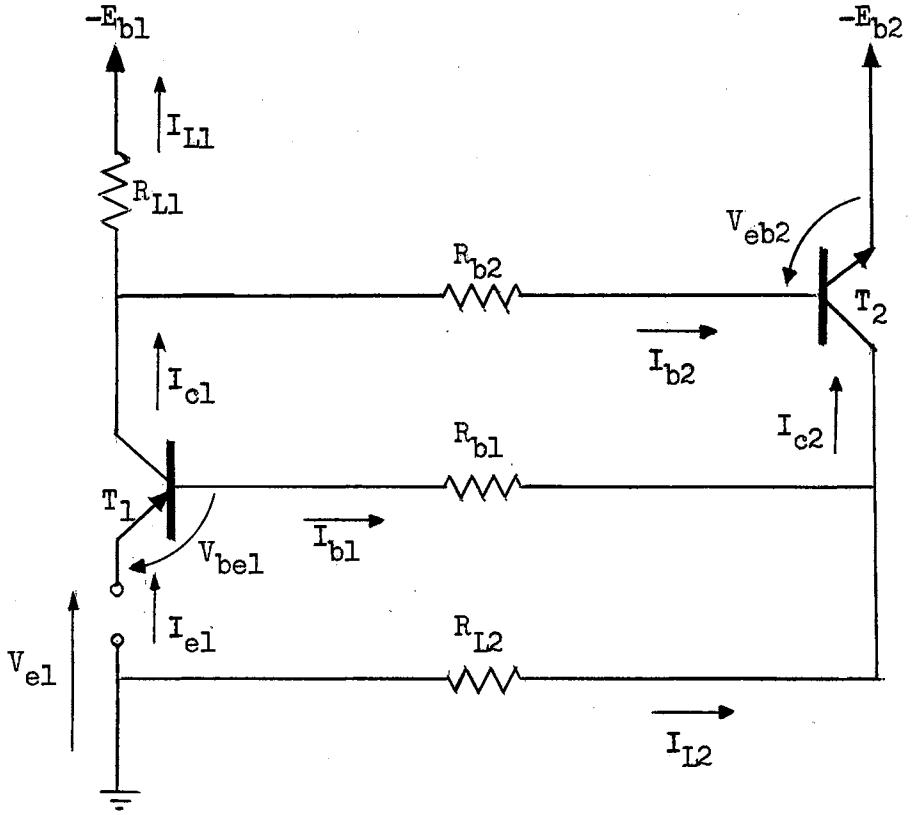


Figure 5. Equivalent Circuit for Static Analysis.

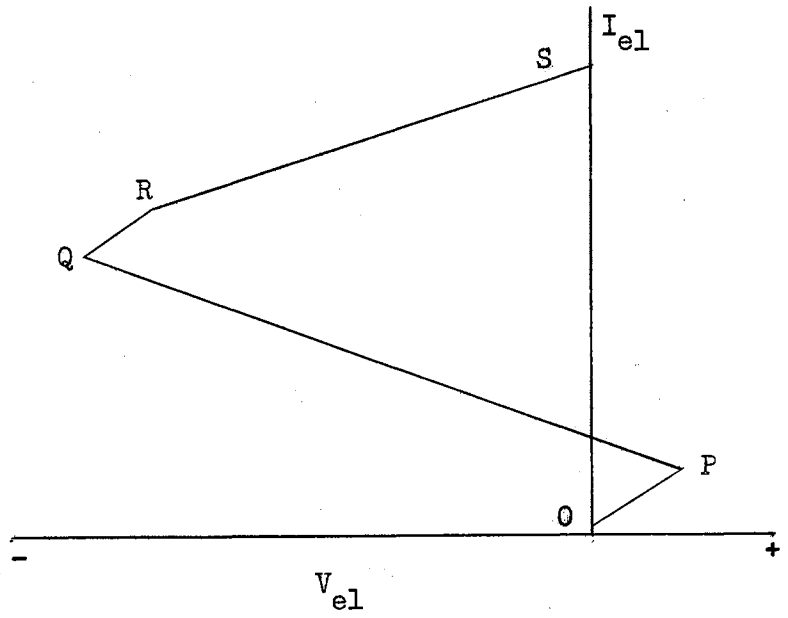


Figure 6. Typical Static Characteristic of the Circuit in Figure 5.

to obtain an increase of emitter current, I_{e1}. Allowing V_{e1} to increase enough will eventually cause T_2 to saturate as represented by point "R" on the static characteristic. After both transistors become saturated, the driving-point impedance at the terminals is determined by the values of R_{L1}, R_{b1}, and R_{b2}. These values may be used to determine the slope of the static characteristic from point "R" to point "S". This final point "S" represents the emitter current, I_{e1}, when the circuit is in the "on" condition.

In deriving the static characteristic curve, all capacitors will be neglected. The internal emmiter-to-base voltage is assumed to be constant for a conducting transistor and the collector-to-base voltage for a saturated transistor is assumed to be equal to zero. The slopes of the regions between the points, will be assumed constant.

Using the above assumptions the various points on the static characteristic may now be evaluated.

Point "O". If I_{b2} is less than $-I_{co2}$, the collector current in T_2 will be zero. Since V_{e1} and I_{c2} are zero, the base current in T_1 is zero giving the collector current in T_1 as $I_{co1}/(1 - \alpha_1)$.[6]

$V_{e1o} = 0$ (The subscript on V_{e1} and I_{e1} refers to point "O".)

$$I_{e1o} = \frac{I_{co1}}{1 - \alpha_1} .$$

Point "P". Since T_2 is the only transistor in the non-conducting state, the circuit will exhibit a loop gain greater than unity as soon as T_2 becomes active. The terminals will now indicate a negative

---

[6] Jacob Millman and Herbert Taub, Op. cit, p. 562.

characteristic. Just as T_2 becomes active

$$V_{b2} = V_{e2} . \tag{1}$$

$$I_{b2} = 0 \tag{2}$$

This gives

$$I_{c2} = \frac{I_{co2}}{1 - \alpha_2} . \tag{3}$$

If I_{b2} is zero and $V_{b2} = V_{e2}$ then

$$V_{c1} = -E_{b2} . \tag{4}$$

From Figure 1

$$-E_{b1} + I_{L1}R_{L1} = -E_{b2} . \tag{5}$$

Solving for I_{L1} and setting equal to I_{c1} when I_{b2} is equal to zero

$$I_{c1} = \frac{E_{b1} - E_{b2}}{R_{L1}} . \tag{6}$$

Using Kirchhoffs' voltage law gives

$$V_{e1} = V_{be1} + I_{b1}R_{b1} - I_{L2}R_{L2} . \tag{7}$$

It follows that

$$V_{e1} = V_{be1} + I_{b1}R_{b1} - (I_{c2} - I_{b1})R_{L2} . \tag{8}$$

Now, using the fact that

$$I_{c1} = \alpha_1 I_{e1} + I_{co1} = I_{e1} + I_{b1} , \tag{9}$$

results in

$$I_{b1} = I_{c1}\frac{(1-\alpha_1)}{\alpha_1} - \frac{I_{co1}}{\alpha_1} . \qquad (10)$$

Substituting equation (3) and equation (10) into equation (8)

$$V_{e1} = V_{be1} + \left[I_{c1}\frac{(1-\alpha_1)}{\alpha_1} - \frac{I_{co1}}{\alpha_1}\right](R_{b1} + R_{L2}) - \frac{I_{co2}}{1-\alpha_2}R_{L2} . \qquad (11)$$

From equation (6)

$$V_{elp} = V_{be1} + \left[\frac{(E_{b1} - E_{b2})(1-\alpha_1)}{R_{L1}\qquad\alpha_1} - \frac{I_{co1}}{\alpha_1}\right](R_{b1} + R_{L2}) - \frac{I_{co2}R_{L2}}{1-\alpha_2} . \qquad (12)$$

$$= V_{be1} + \frac{(E_{b1} - E_{b2})}{R_{L1}}(R_{b1} + R_{L2})\frac{(1-\alpha_1)}{\alpha_1}$$

$$- \frac{I_{co1}(R_{b1} + R_{L2})}{\alpha_1} - \frac{I_{co2}}{1-\alpha_2}(R_{L2}) . \qquad (13)$$

The value of α for low emmiter current densities should be used for for calculating V_{elp} and I_{elp}. To calculate the current I_{elp} when T_2 just becomes active, equate equation (6) and equation (9) and solve for I_{elp}.

$$I_{elp} = \left[\frac{E_{b1} - E_{b2}}{R_{L1}} - I_{co1}\right]\frac{1}{\alpha_1} . \qquad (14)$$

Point "Q". When T_1 becomes saturated, V_{c1} may be approximated as V_{b1} by assuming the collector-to-base voltage is zero. Using Kirchoff's voltage law:

$$V_{e1} = V_{be1} + I_{L1}R_{L1} - E_{b1} \cdot \tag{15}$$

Using Kirchoff's current law

$$I_{L1} = I_{c1} - I_{b2} \cdot \tag{16}$$

Solving equation (9) for I_{c1} in terms of I_{b1}

$$I_{c1} = \left[I_{b1} + \frac{I_{co1}}{\alpha_1} \right] \frac{\alpha_1}{1 - \alpha_1} \cdot \tag{17}$$

Using Kirchoff's voltage law again yields

$$I_{b2} = \frac{V_{e1} - V_{be1} + E_{b2} - V_{eb2}}{R_{b2}} \cdot \tag{18}$$

Using the subscripts (2), and solving equation (9) for I_{c2} in terms of I_{b2}

$$I_{c2} = \left[I_{b2} + \frac{I_{co2}}{\alpha_2} \right] \frac{\alpha_2}{1 - \alpha_2}$$

$$= \left[\frac{(V_{e1} - V_{be1} + E_{b2} - V_{eb2})}{R_{b2}} + \frac{I_{co2}}{\alpha_2} \right] \frac{\alpha_2}{1 - \alpha_2} \cdot \tag{19}$$

Using Kirchoff's current law

$$I_{c2} = I_{b1} + I_{L2} \cdot \tag{20}$$

Solving for I_{L2}

$$I_{L2} = \frac{V_{e1} - V_{be1} - I_{b1}R_{b1}}{-R_{L2}} . \tag{22}$$

Putting equation (21) into equation (19)

$$I_{c2} = I_{b1} + \frac{V_{e1} - V_{be1} - I_{b1}R_{b1}}{-R_{L2}} . \tag{23}$$

Equating equation (19) and (23)

$$I_{b1} + \frac{V_{e1} - V_{be1} - I_{b1}R_{b1}}{-R_{L2}} = \left[\frac{(V_{e1} - V_{be1} + E_{b2} - V_{eb2})}{R_{b2}}\right] \frac{\alpha_2}{1 - \alpha_2} + \frac{I_{co2}}{1 - \alpha_2} . \tag{24}$$

Solving for I_{b1}

$$I_{b1} = \frac{\dfrac{(V_{e1} - V_{be1} + E_{b2} - V_{eb2})\alpha_2}{R_{b2}(1 - \alpha_2)} + \dfrac{I_{co2}}{1 - \alpha_2} + \dfrac{(V_{be1} - V_{e1})}{-R_{L2}}}{1 + \dfrac{R_{b1}}{R_{L2}}} . \tag{25}$$

Substituting into equation (17) gives

$$I_{c1} = \frac{\alpha_1}{1-\alpha_1}\left[\frac{(V_{e1} - V_{be1} + E_{b2} - V_{eb2})\alpha_2}{R_{b2}(1-\alpha_2)\left(1+\frac{R_{b1}}{R_{L2}}\right)} + \frac{I_{co2}}{(1-\alpha_2)\left(1+\frac{R_{b1}}{R_{L2}}\right)} + \frac{V_{be1} - V_{e1}}{-R_{L2}\left(1+\frac{R_{b1}}{R_{L2}}\right)}\right] + \frac{I_{co1}}{1-\alpha_1} \quad (26)$$

Substituting equation (26) and (18) into equation (16) gives

$$I_{L1} = \frac{\alpha_1}{1-\alpha_1}\left[\frac{(V_{e1} - V_{be1} + E_{b2} - V_{eb2})\alpha_2}{R_{b2}(1-\alpha_2)\left(1+\frac{R_{b1}}{R_{L2}}\right)} + \frac{I_{co2}}{(1-\alpha_2)\left(1+\frac{R_{b1}}{R_{L2}}\right)} + \frac{V_{be1} - V_{e1}}{-R_{L2}\left(1+\frac{R_{b1}}{R_{L2}}\right)}\right] + \frac{I_{co1}}{1-\alpha_1}$$

$$- \frac{(V_{e1} - V_{be1} + E_{b2} - V_{eb2})}{R_{b2}} \quad (27)$$

Substituting equation (27) into equation (15) yields

$$V_{e1} = V_{be1} - E_{b1} + \frac{I_{co1}R_{L1}}{1-\alpha_1} - R_{L1}\left[\frac{V_{e1} - V_{be1} + E_{b2} - V_{eb2}}{R_{b2}}\right] + \frac{\alpha_1 R_{L1}}{1-\alpha_1}\left[\frac{(V_{e1} - V_{be1} + E_{b2} - V_{eb2})\alpha_2}{R_{b2}(1-\alpha_2)\left(1 + \frac{R_{b1}}{R_{L2}}\right)}\right.$$

$$\left. + \frac{I_{co2}}{(1-\alpha_2)\left(1 + \frac{R_{b1}}{R_{L2}}\right)} + \frac{V_{be1} - V_{e1}}{-R_{L2}\left(1 + \frac{R_{b1}}{R_{L2}}\right)}\right]. \qquad (28)$$

Rearranging

$$V_{e1} = V_{be1} - E_{b1} + \frac{I_{co1}R_{L1}}{1-\alpha_1} - \frac{R_{L1}}{R_{b2}}\left[-V_{be1} + E_{b2} - V_{eb2}\right] - \frac{V_{e1}R_{L1}}{R_{b2}} + V_{e1}\left[\frac{\alpha_1 R_{L1}\alpha_2}{(1-\alpha_1)(R_{b2})(1-\alpha_2)\left(1 + \frac{R_{b1}}{R_{L2}}\right)}\right]$$

$$+ V_{e1}\left[\frac{\alpha_1 R_{L1}}{(1-\alpha_1)R_{L2}\left(1 + \frac{R_{b1}}{R_{L2}}\right)}\right] + \frac{\alpha_1 R_{L1}}{1-\alpha_1}\left[\frac{(-V_{be1} + E_{b2} - V_{eb2})\alpha_2}{R_{b2}(1-\alpha_2)\left(1 + \frac{R_{b1}}{R_{L2}}\right)} + \frac{I_{co2}}{(1-\alpha_2)\left(1 + \frac{R_{b1}}{R_{L2}}\right)} + \frac{V_{be1}}{-R_{L2}\left(1 + \frac{R_{b1}}{R_{L2}}\right)}\right]. \qquad (29)$$

Solving equation (29) for V_{e1}

$$V_{be1} - E_{b1} + \frac{I_{co1}R_{L1}}{1-\alpha_1} - \frac{R_{L1}}{R_{b2}}\left[-V_{be1} + E_{b2} - V_{eb2}\right] + \frac{\alpha_1 R_{L1}}{1 + \frac{R_{b1}}{R_{L2}}\ 1-\alpha_2}\left[\frac{(-V_{be1} + E_{b2} - V_{eb2})\alpha_2}{R_{b2}(1-\alpha_2)} + \frac{I_{co2}}{1-\alpha_2} - \frac{V_{be1}}{R_{L2}}\right]$$

$$V_{e1Q} = \frac{}{1 + \frac{R_{L1}}{R_{b2}} - \frac{\alpha_1 R_{L1}}{(1-\alpha_1)R_{L2}\left(1 + \frac{R_{b1}}{R_{L2}}\right)} - \frac{R_{L1}\alpha_1\alpha_2}{(1-\alpha_1)R_{b2}(1-\alpha_2)\left(1 + \frac{R_{b1}}{R_{L2}}\right)}} \quad (30)$$

Solving equation (9) for I_{e1}, and substituting equation (26) into the results gives the emitter current at the point of saturation of T_1.

$$I_{e1Q} = \left[\frac{(V_{e1} - V_{be1} + E_{b2} - V_{eb2})\alpha_2}{R_{b2}(1-\alpha_2)} + \frac{I_{co2}}{(1-\alpha_2)} + \frac{V_{be1} - V_{e1}}{-R_{L2}}\right] \frac{1}{(1-\alpha_1)\left(1 + \frac{R_{b1}}{R_{L2}}\right)} + \frac{I_{co1}}{1-\alpha_1} . \quad (31)$$

The value of α for high emitter current densities should be used for calculating V_{e1Q} and I_{e1Q}.

Point "R". This point represents the saturation point for T_2. The collector-to-base voltage may now be assumed to be zero for both transistors.

Using Kirchoff's voltage law

$$V_{e1} = V_{be1} + I_{b2}R_{b2} + V_{eb2} - E_{b2} . \tag{32}$$

Solving equation (9) in terms of I_{c2}

$$I_{b2} = I_{c2} \frac{(1 - \alpha_2)}{\alpha_2} - \frac{I_{co2}}{\alpha_2} . \tag{33}$$

Using Kirchoff's current law

$$I_{c2} = I_{L2} + I_{b1} . \tag{34}$$

where $$I_{L2} = \frac{E_{b2} - V_{eb2}}{R_{L2}} . \tag{35}$$

$$I_{b1} = \frac{(V_{e1} - V_{be1}) - (-E_{b2} + V_{eb2})}{R_{b1}} . \tag{36}$$

Substituting equation (35) and equation (36) into equation (34)

$$I_{c2} = \left[\frac{E_{b2} - V_{eb2}}{R_{L2}} + \frac{E_{b2} - V_{eb2} - V_{eb1} + V_{e1}}{R_{b1}} \right] . \tag{37}$$

Using equation (37) and equation (33) in equation (32) and solving for V_{e1}

$$V_{elR} = \frac{V_{bel} + R_{b2}\left[\frac{1-\alpha_2}{\alpha_2}\left(\frac{E_{b2} - V_{eb2}}{R_{L2}} + \frac{E_{b2} - V_{eb2} - V_{bel}}{R_{b1}}\right) - \frac{I_{co2}}{\alpha_2}\right] + V_{eb2} - E_{b2}}{\left(1 + \frac{R_{b2}}{R_{b1}}\right)\frac{(1-\alpha_2)}{\alpha_2}} . \quad (38)$$

To solve for I_{e1} when T_2 becomes saturated, note that the emitter current is the sum of the collector current and the two base currents.

$$I_{e1} = I_{L1} + I_{b1} + I_{b2} . \quad (39)$$

where

$$I_{b1} = \frac{V_{e1} - V_{bel} + E_{b2} - V_{eb2}}{R_{b1}} , \quad (40)$$

$$I_{b2} = \frac{V_{e1} - V_{bel} + E_{b2} - V_{eb2}}{R_{b2}} , \quad (41)$$

and

$$I_{L1} = \frac{V_{e1} - V_{bel} + E_{b1}}{R_{L1}} . \quad (42)$$

Adding equation (40), equation (41) and equation (42)

$$I_{elR} = (V_{e1} - V_{bel} + E_{b2} - V_{eb2})\left[\frac{1}{R_{b1}} + \frac{1}{R_{b2}}\right] + \frac{V_{e1} - V_{bel} + E_{b1}}{R_{L1}} . \quad (43)$$

Point "S". After both transistors saturate, the driving point impedance may be considered as being equivalent to R_{L1}, R_{b1}, and R_{b2} all being in parallel to ground.

$$R_{in} = \frac{R_{L1}R_{b2}R_{b1}}{R_{L1}R_{b1} + R_{L1}R_{b2} + R_{b2}R_{b1}} = \frac{1}{G_{in}} . \qquad (44)$$

The characteristic curve may now be considered as having the slope of the input conductance. Since it will be a straight line, the intercept of the current axis may be found by using the slope-intercept form for a straight line. The coordinates of point R which lies on the line may be substituted into the equation leaving the only unknown to be the intercept of the "current" axis.

This gives

$$V_{els} = 0. \qquad (45)$$

$$I_{els} = I_{elR} - V_{elR}G_{in}. \qquad (46)$$

Summary of Results of The Static Analysis

Point "O".

$$V_{elO} = 0. \qquad (47)$$

$$I_{elO} = \frac{I_{col}}{1 - \alpha_1} . \qquad (48)$$

Point "P".

$$V_{elP} = V_{bel} + (R_{bl} + R_{L2}) \left[\frac{(E_{bl} - E_{b2})(1 - \alpha_1)}{R_{L1}\alpha_1} - \frac{I_{col}}{\alpha_1} \right] - \frac{I_{co2}R_{L2}}{1 - \alpha_2} \quad . \tag{49}$$

$$I_{elP} = \left[\frac{E_{bl} - E_{b2}}{R_{L1}} - I_{col} \right] \frac{1}{\alpha_1} \quad . \tag{50}$$

Point "Q".

$$V_{elQ} = \frac{V_{bel} - E_{bl} + \frac{I_{col}R_{L1}}{1 - \alpha_1} - \frac{R_{L1}}{R_{b2}}\left[-V_{bel} + E_{b2} - V_{eb2}\right] + \frac{\alpha_1 R_{L1}}{(1 - \alpha_1)\left(1 + \frac{R_{bl}}{R_{b2}}\right)}\left[\frac{(-V_{bel} + E_{b2} - V_{eb2})\alpha_2}{R_{b2}(1 - \alpha_2)} + \frac{I_{co2}}{1 - \alpha_2} - \frac{V_{bel}}{R_{L2}}\right]}{D} \quad . \tag{51}$$

where $$D = 1 + \frac{R_{L1}}{R_{b2}} - \frac{\alpha_1 R_{L1}}{(1 - \alpha_1)(R_{L2})\left(1 + \frac{R_{bl}}{R_{L2}}\right)} - \frac{R_{L1}\alpha_1\alpha_2}{R_{b2}(1 - \alpha_1)(1 - \alpha_2)\left(1 + \frac{R_{bl}}{R_{L2}}\right)}$$

$$I_{elQ} = \left[\frac{(V_{elQ} - V_{bel} + E_{b2} - V_{eb2})\alpha_2}{R_{b2}(1 - \alpha_2)} + \frac{I_{col}}{1 - \alpha_2} + \frac{(V_{bel} - V_{el})}{-R_{L2}} \right] \frac{1}{(1 - \alpha_1)\left(1 + \frac{R_{bl}}{R_{L2}}\right)} + \frac{I_{col}}{1 - \alpha_1} \quad . \tag{52}$$

Point "R".

$$V_{elR} = \frac{V_{bel} + R_{b2}\left[\frac{1-\alpha_2}{\alpha_2}\left(\frac{E_{b2} - V_{eb2}}{R_{L2}} + \frac{E_{b2} - V_{eb2} - V_{bel}}{R_{b1}}\right) - \frac{I_{co2}}{\alpha_2}\right] - E_{b2} + V_{eb2}}{\left(1 - \frac{R_{b2}}{R_{b1}}\right)\frac{(1-\alpha_1)}{\alpha_2}} \quad . \tag{53}$$

$$I_{elR} = (V_{elR} + E_{b2} - V_{bel} - V_{eb2})\left[\frac{1}{R_{b1}} + \frac{1}{R_{b2}}\right] + \frac{V_{elR} + E_{b1} + V_{bel}}{R_{L1}} \quad . \tag{54}$$

Point "S".

$$V_{elS} = 0. \tag{55}$$

$$I_{elS} = (I_{el})_R + (V_{elR})/R_{in} \quad . \tag{56}$$

where,

$$R_{in} = \frac{R_{b1}R_{b2}R_{L1}}{R_{L1}R_{b2} + R_{L1}R_{b1} + R_{b1}R_{b2}} \quad . \tag{57}$$

Approximate Equations

It is apparent that the preceding equations would be much too cumbersome for "everyday" utility and that approximate equations would be preferred if they are not too inaccurate. Fortunately, such approximations as :

$$I_{co1} \approx I_{co2} \approx 0, \tag{58}$$

$$R_b/R_L \gg 1,$$

$$V_{be1} \approx V_{be2} \approx 0,$$

$$\alpha_1 \approx \alpha_2 ,$$

together with the fact that

$$R_{L1} = R_{L2} , \tag{59}$$

$$R_{b1} = R_{b2} , \tag{60}$$

will result in equations which are much more desired if only a "ball park" answer is sufficient.

Using the approximations and conditions stated above gives the following equations defining the necessary points to predict the static characteristic curve.

Approximate Equations for Static Characteristic

Point "O".

$$V_{elo} = 0. \tag{61}$$

$$I_{elo} \approx 0.$$

Point "P".

$$V_{elp} \approx \frac{R_{b1}(E_{b1} - E_{b2})}{\beta\ R_{L1}} \tag{62}$$

where $\beta = \frac{\alpha}{1 - \alpha}$ (63)

$$I_{elp} \approx \frac{E_{b1} - E_{b2}}{R_L\ \alpha_1} \tag{64}$$

Use β for low emitter current density in equation (62).

Point "Q".

$$V_{elQ} \approx \frac{-E_{b1} - E_{b2}\frac{R_L}{R_b} + \left[\frac{(\beta R_L)^2}{(R_b)^2}\right] E_{b2}}{1 - \beta\frac{R_L}{R_b} - \frac{(\beta R_L)^2}{(R_b)^2}} . \tag{65}$$

$$I_{elQ} \approx \left[\frac{\beta(V_{elQ} + E_{b2})}{R_b} + \frac{V_{el}}{R_L}\right](1 + \beta)\frac{R_L}{R_b} . \tag{66}$$

Point "R".

$$V_{elR} \approx \frac{\frac{R_b E_{b2}}{\beta R_L} - E_{b2}}{1 - \frac{1}{\beta}} \tag{67}$$

$$\approx -E_{b2}(1 - R_b/\beta R_L) \tag{68}$$

$$I_{elR} \approx (V_{el} + E_{b2})^2/(R_b)^2 + V_{el} + E_{b1}/R_L \qquad (69)$$

Use β for high emitter current density in equations (65), (66) and (67).

Point "S".

$$V_{els} = 0 \qquad (70)$$

$$I_{els} \approx (I_{el})R - (V_{elR})/R_{in} \qquad (71)$$

Where

$$R_{in} = \frac{R_b R_L/2}{R_b/2 + R_L} \quad . \qquad (72)$$

Bistable Circuit Design Equations

Because the flip-flop operates in the saturated region, the selection of R_{b1} and R_{b2}, that will insure two stable states, is not critical. In designing the circuit, it will be assumed that equal load resistances and equal base current limiting resistances are to be used. The base current limiting resistances must be small enough to insure saturation of the transistor with the lowest value of α, and the load resistances should be large enough to limit the emitter current to I_c (max) for any given supply voltage less than the transistor punch-through voltage. Since E_{b1} is the largest supply voltage, and transistors of approximate equal ratings and characteristics are assumed to be used, the approximate minimum value of R_{L1} is determined by E_{b1} (max) divided by I_{c1}(max) if $R_{L1} \ll R_{b1}$.

To insure that T_2 is cutoff, the base current, I_{b2}, must have a value less than $-I_{co2}$ and the collector current in T_1 will be $I_{col}/1-\alpha$. Using Kirchoff's voltage law and Figure (4):

$$E_{b2} + I_{L1}R_{L1} = E_{b1} + I_{b2}R_{b2} - V_{eb2} . \tag{73}$$

Solving for R_{b2} when $I_{b2} = -I_{co2}$ and $I_{c1} = I_{col}/(1-\alpha)$

$$R_{b2} \leq \frac{-E_{b1} + E_{b2} + V_{eb2} + \left[\frac{I_{col}}{1-\alpha_1} + I_{co2}\right] R_{L1}}{-I_{co2}} . \tag{74}$$

Since R_{b2} must be positive

$$E_{b2} \leq E_{b1} - V_{eb2} - \left[\frac{I_{col}}{1-\alpha} + I_{co2}\right] R_{L1} . \tag{75}$$

For a margin of safety in providing stability in the off condition, subtract 1 or 2 volts from the right side of the inequality. Better stability may be obtained by subtracting a larger value, but this would increase the minimum amplitude required to trigger the circuit.

In the on condition, T_1 is biased by $(E_{b2} - V_{eb2})/R_{b1}$ and T_2 is biased by $(E_{b2} - V_{eb1})/R_{b2}$ neglecting the collector base voltages at saturation. I_{b2} must be at least as great as

$$(I_{c2}\ \max)(1-\alpha_2)/\alpha_2 - I_{co2}/\alpha_2 , \tag{76}$$

for saturation to occur in T_2.

This gives

$$(E_{b2} - V_{eb1})/R_{b2} \geq I_{c2}(\max)(1-\alpha_2)/\alpha_2 - I_{co2}/\alpha_2 . \tag{77}$$

Solving for R_{b2}

$$R_{b2} \leqq \frac{E_{b1} - V_{eb1}}{I_{c2}(max)(1 - \alpha_2)/\alpha_2 - I_{co2}/\alpha_2} \quad . \tag{78}$$

Similiarly, I_{b1} must be at least as great as

$$I_{c1}(max)(1 - \alpha_1)/\alpha_1 - I_{co1}/\alpha_1 \quad . \tag{79}$$

For saturation of T_1

$$R_{b1} \leqq \frac{E_{b2} - V_{eb2}}{I_{c1}(max)(1 - \alpha_2)/\alpha_2 - I_{co2}/\alpha_2} \quad . \tag{80}$$

Summary of Design Equations for Bistable Operation

1. Select $R_{L2} = R_{L1} \approx \dfrac{E_{b1}(max)}{I_{c1}(max)}$ (81)

2. Select E_{b2} where

$$E_{b2} \leqq E_{b1} - V_{eb2} - \left[\frac{I_{co1}}{1 - \alpha_1} + I_{co2}\right] R_{L1} - X \tag{82}$$

where X is a 1 or 2 volt safety factor.

3. Select $R_{b2} = R_{b1}$ where

(a) $$R_{L1} \ll R_{b2} < \frac{E_{b2} - E_{b1} + V_{eb2} + \left[\dfrac{I_{co1}}{1 - \alpha_1} + I_{co2}\right] R_{L1}}{- I_{co2}} \quad , \tag{84}$$

and

$$(b) \quad R_{L1} \ll R_{b2} < \frac{E_{b2} - V_{eb1}}{I_{c2(max)} \dfrac{1 - \alpha_2}{\alpha_2} - \dfrac{I_{co2}}{\alpha_2}}, \tag{84}$$

where $I_{c2}(max) \approx E_{b2}/R_{L2}$ (85)

$$(c) \quad R_{L1} \ll R_{b2} < \frac{E_{b2} - V_{eb2}}{I_{c1(max)} \dfrac{1 - \alpha_2}{\alpha_2} \dfrac{I_{co1}}{\alpha_1}}. \tag{86}$$

NOTE: All three inequalities must be satisfied.

Monostable Mode of Operation

To change the mode of operation of the bistable circuit to monostable circuit, it is noted that a resistor must be used which has a value greater than V_{elp}/I_{elp}. This will cause the stable state to be in the "off" condition.

To allow the circuit to be turned on, the resistor is bypassed by a capacitor so that the effective load line coincides with the current axis at time equal to zero. As time increases, the effective impedance of the parallel combination increases until it is large enough to cause the circuit to cut off. If the duration of the total "on" period is several times greater than the transient "turn on" period, then the input impedance at the "V_{el}-I_{el}" terminals may be considered as the parallel combination of R_{L1}, R_{b1}, R_{b2}. To find the effective impedance of the parallel combination of R and C, the equivalent circuit in

Figure 7 may be used. Employing Laplace transformation techniques and assuming a unit input voltage, the input impedance may be calculated as

$$Z_{in} = \frac{R_1 + R}{\frac{R}{R_1} e^{-\frac{t(R + R_1)}{R R_1 C}} + 1} \tag{87}$$

where the parallel combination of R_{L1}, R_{b1}, and R_{b2} is represented by R_1.

The effective input impedance of the parallel combination of R and C is

$$R_{eff} = Z_{in} - R_1$$

$$= \frac{R_1 + R}{\frac{R}{R_1} e^{-\frac{t(R + R_1)}{R R_1 C}} + 1} - R_1 . \tag{88}$$

Solving for C

$$C = \frac{-t \frac{R + R_1}{R R_1}}{\ln\left[\frac{R_1}{R}\left(\frac{R_1 + R}{R_1 + R_{eff}} - 1\right)\right]} \tag{89}$$

where t is the required time for the parallel combination of R and C to obtain a value of R_{eff}. At this time, the effective load line has rotated in the clockwise direction to a value corresponding to R_{eff}. If R_{eff} is V_{elp}/I_{elp}, the circuit will begin to turn off.

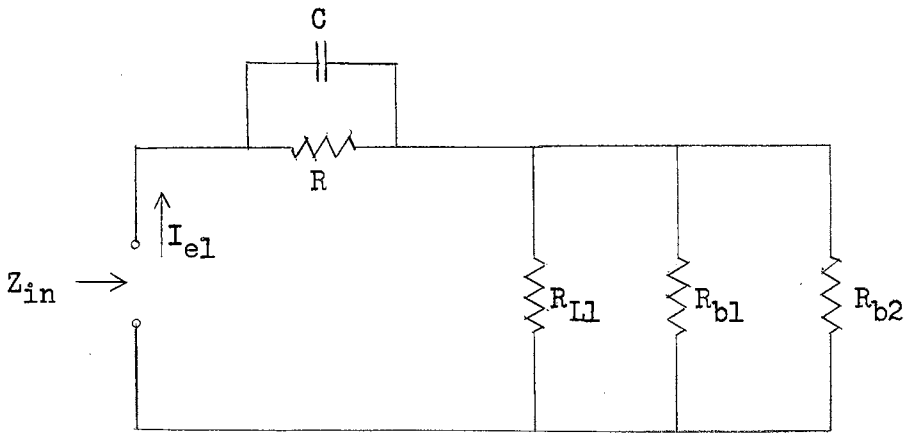


Figure 7. Equivalent Circuit for Calculating R_{eff}.

Transient Considerations

Although a complete and rigorous analysis of the transient "turn on" and "turn off" period would be desirable, an exact analysis does not warrant the effort because of the complexity of the problem and the relative low frequency at which the counter is to be operated.

In the analysis for determining the static characteristic at the opened terminals of Figure 1, it was seen that the circuit exhibited a negative impedance during the time that both transistors were active. The analysis, however, did not consider the impedance under a transient condition. One method described by Suran and Reibert[7] for determining the maximum frequency of operation, is to calculate the complex driving point impedance at the terminals during the active period of both T_1 and T_2. It would consist of a negative real component and an imaginary component. The real part would be a function of frequency and would

---

[7] J. J. Suran, op. cit. p. 26.

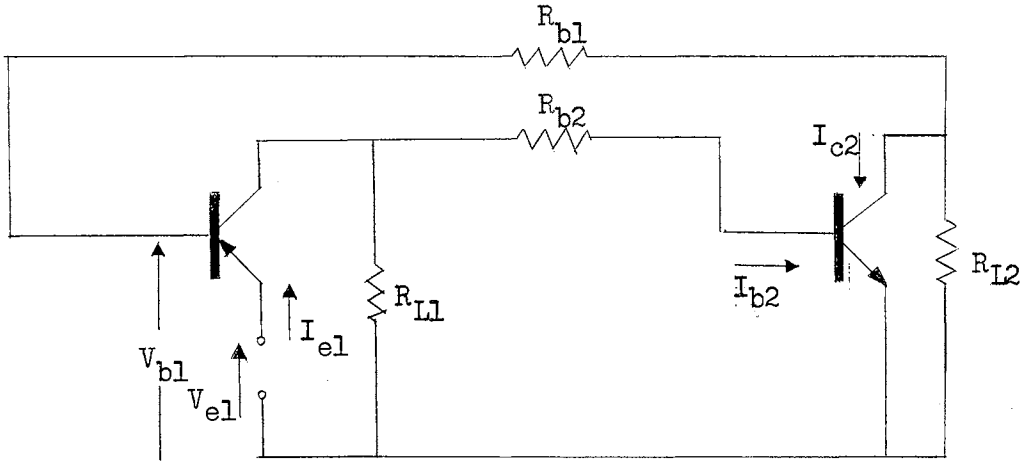


Figure 8. Equivalent Circuit for Negative Resistance Calculations.

go to zero as the frequency tends to infinity. Setting the real part to zero and solving for the frequency would give the limiting frequency of operation.

Referring to the AC equivalent circuit in Figure 8.

$$i_{c1} = \alpha_1 i_{e1} \tag{90}$$

Also
$$v_{c1} = i_{c1}\left[R_{L1}(R_{k2} + R_{i2})/(R_{L1} + R_{b2} + R_{i2})\right] \tag{91}$$

$$i_{b2} = v_{c1}/(R_{k2} + R_{i2}) \tag{92}$$

where R_{i2} is the input impedance of T_2.

Using equations (80) and (81)

$$i_{b2} = i_{c1}\left[R_{L1}/(R_{L1} + R_{b2} + R_{i2})\right] . \tag{93}$$

Using the common emitter current gain

$$i_{c2} = \beta_2 i_{b2} \tag{94}$$

results in

$$-v_{b1} = i_{c2}R_{L2} . \tag{95}$$

Combining equations (90), (93), (94) and (95)

$$v_{b1} = -\beta_2 \alpha_1 R_{L1} R_{L2} i_{e1} / (R_{L1} + R_{b2} + R_{i2}) . \qquad (96)$$

Note also that

$$v_{e1} = i_{e1} r_{1b} + v_{b1} \qquad (97)$$

where r_{1b} is the input resistance of T_1 for a grounded base connection.

Substituting equation (96) into equation (97) and taking the derivative of v_{e1} with respect to i_{e1}

$$r_{e1} = d_{ve1}/d_{ie1} = r_{1b} - \beta_2 \alpha_1 R_{L1} R_{L2} / (R_{L1} + R_{b2} + R_{i2}). \qquad (98)$$

In most practical circuits r_{1b} may be neglected. If R_{b2} is bypassed by a capacitor at high frequencies, then it too may be neglected. Assuming the above conditions exist and putting the first-order frequency approximations for α_1 and β_2 yields

$$r_{e1} = -\beta_{2o} \alpha_{1o} R_{L1} R_{L2} / (R_{L1} + R_{i2}) \left[\frac{1}{(1 + j\omega/\omega_\alpha)(1 + j\omega/\omega_\beta)} \right] . \qquad (99)$$

This leads to

$$r_{e1} = \beta_{2o} \alpha_{1o} R_{L1} R_{L2} / (R_{L1} + R_{i2}) \left[\frac{-(1 - \omega^2/\omega_\alpha \omega_\beta) + j(\omega/\omega_\alpha + \omega/\omega_\beta)}{(1 - \omega^2/\omega_\alpha \omega_\beta)^2 + (\omega/\omega_\alpha + \omega/\omega_\beta)^2} \right] . \qquad (100)$$

Clearly the negative component will be zero when

$$\omega^2 / \omega_{\alpha 1} \omega_{\beta 2} = 1 . \qquad (101)$$

Leading to a maximum frequency of operation of

$$\omega_{max} = \sqrt{\omega_{\alpha 1}\omega_{\beta 2}} \quad . \tag{102}$$

if

$$\omega_{\beta 2} = \omega_{\alpha 2}/\beta_o \tag{103}$$

then $$\omega_{max} = \sqrt{\omega_{\alpha 1}\omega_{\beta 2}} \div \sqrt{\beta_{2o}} \quad . \tag{104}$$

It should be noted that the foregoing analysis applies only to nonsaturating transistors and does not take into account the minority storage effects encountered in saturated circuits.

If the alpha cutoff frequency of T_1 and T_2 are equal, then the maximum possible operating frequency becomes

$$F_{max} = F_\alpha / \sqrt{\beta_o} \quad . \tag{105}$$

CHAPTER III

NUMERICAL SYNTHESIS OF CIRCUITS

Synthesis of Bistable Element

Using the design equations developed in Chapter II, the basic bistable circuit may now be derived. Transistors were selected having equal ratings and characteristics. Since the punch-through voltage was 15 volts, the supply voltage E_{b1} was chosen as 12 volts to give a margin of safety. I_{c1} (max) was chosen to be approximately 3 ma.

Given $E_{b1} = 12$ volts

$I_{c1}\ (\max) \approx 3$ ma.

$\beta_1 \approx \beta_2 = 40$ (for high emitter current densities) $\beta_1 \approx \beta_2 = 56.3$ (for low emitter current densities)

$V_{be1} = .28$ volts $V_{eb2} = .14$ volts

$I_{co1} = .8 \times 10^{-6}$ amps $I_{co2} = 1.46 \times 10^{-6}$ amps

Using the design procedure from equations (81) through (86)

1. Select $R_{L1} = R_{L2} \approx E_{b1}/I_{c1}$

$\approx 12/3 = 4$ k ohms.

R_{L1} was chosen to be 3.9 kohms.

2. Select E_{b2} where

$$E_{b2} \leq E_{b1} - V_{eb2} - (I_{co1}/1-\alpha_1 + I_{co2})R_{L1} - X$$

Using the value of α for large emitter current densities

$$\leqq 12 - .14 - (.8 \times 10^{-6}/1-.976 + 1.46 \times 10^{-6})3900 - X$$

$$\leqq 11.73 - X$$

If X is 1.73 volts E_{b2} may be 10 volts

$$\therefore \text{ Choose } E_{b2} = 10 \text{ volts}$$

This will provide good stability in the "off" condition and still allow the minimum trigger amplitude to be approximately 1 volt.

3. Select $R_{b2} = R_{b1}$

(a) $$R_{L1} \ll R_{b2} < \frac{E_{b2} - E_{b1} + V_{eb2} + (I_{co1}/1-\alpha_1 + I_{co2})R_{L1}}{-I_{co2}}$$

$$3.9 \text{ k} \ll R_{b2} < \frac{10 - 12 + .14 + (.8 \times 10^{-6}/1-.976 + 1.46 \times 10^{-6})3900}{-1.46 \times 10^{-6}}$$

$$3.9 \text{ k} \ll R_{b2} < 1.184 \times 10^{-6} \text{ ohms.}$$

(b) $$R_{L1} \ll R_{b2} < \frac{E_{b2} - V_{be1}}{E_{b2}/R_{L2}(1-\alpha_2/\alpha_2) - I_{co2}/\alpha_2}$$

$$3.9 \text{ k} \ll R_{b2} < \frac{10 - .28}{(10/3.9 \times 10^3)(1-.976/.976) - (1.46 \times 10^{-6})/.976}$$

$$3.9 \text{ k} \ll R_{b2} < .155 \times 10^6 \text{ ohms.}$$

(c) $$R_{L1} \ll R_{b2} < \frac{E_{b2} - V_{eb2}}{E_{b1}/R_{L1}(1-\alpha_2/\alpha_2) - I_{co1}/\alpha_1}$$

$$3.9 \text{ k} \ll R_{b2} < \frac{10 - .14}{(12/3.9 \times 10^3)(1-.976/.976) - .8 \times 10^{-6}/.976}$$

$$3.9 \text{ k} \ll R_{b2} < .135 \times 10^6 \text{ ohms.}$$

Since R_{b2} must satisfy the three inequalities, (a, b, and c), choose R_{b2} equal to 100 k ohms.

Using the steady state equations developed earlier, the static characteristic curve of Figure (10) may be calculated. It is important to note that the value for α for point "P" will generally be greater than that for point "Q" where the emitter density is greater.

In the selection of components, 10 percent resistance tolerances may usually be used without any great error. The actual resistances used for calculations were 3.8 K ohms for the load resistances and 96 K ohms for the base current limiting resistances.

To obtain the static characteristic curve experimentally, the circuit in Figure 9 was used. Because the "V_{el}, I_{el}" terminals exhibit a negative characteristic during the time both transistors are conducting, an approximate current source was employed to obtain the data. The reversing switch is shown in the position for obtaining the portion of the curve having positive voltages.

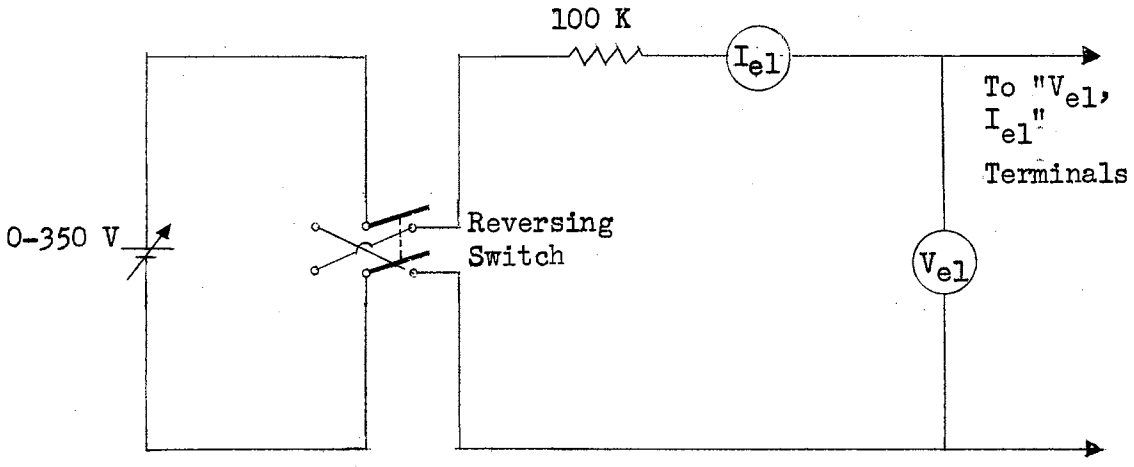


Figure 9.

Arrangement for Obtaining Static Characteristic Curve.

Both the approximate and exact calculations are compared with experimental results in Figure (10) and Table I. It is noticed that during the transient period, i.e., the negative impedance region, the nonlinear effects of α causes some discrepancy from the calculated values. Since only the end points of this region of the curve were considered in deriving the equations for the static characteristic, the values for α at these end points must be used if reasonable results are to be obtained.

The complete circuit (Figure 11) shows a coupling capacitor of 60 uuf. Experimentally, this seemed to be the best choice. A smaller capacitance gave a rapid deterioration of "good" rise time and a larger capacitance caused transient overshoot at "turn on" as well as a longer "turn off" period. From the transient consideration in Chapter 2, it was assummed that R_b was essentially bypassed at the higher operating frequencies. For this to occur, the time constant of R_b and C_b must be considerably greater than $\sqrt{\beta_o}/F_\alpha$. Using the selected values of R_b and C_b, F_α of 4×10^6 cps, and an average value of β_o as 48.2 gives

$$R_b C_b > \sqrt{\beta_o}/F_\alpha$$

$$6 \times 10^{-6} > 1.73 \times 10^{-6}$$

showing that the inequality is satisfied.

Base triggering is employed for increased sensitivity throughout the entire counter. It is necessary that all transients "die out" from each "turn on" or "turn off" pulse before another is received to change the condition back again. Since the flip-flop is preceded by nine other stages, the transient from the "turn off" pulse may be roughly nine times as long as the transient from the "turn on" pulse. A

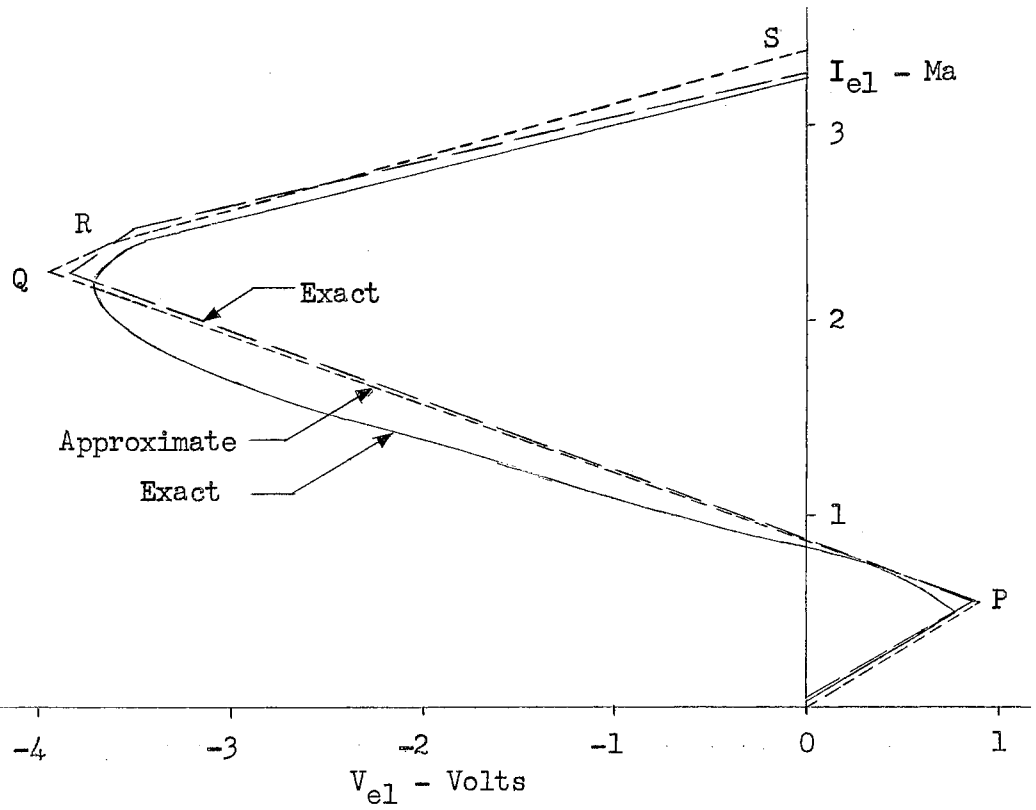


Figure 10. Static Characteristics for the Bistable Circuit

TABLE I

COORDINATES OF POINTS FOR FIGURE 10

Point		Exact	Approximate	Experimental
O	V_{elO} (volts)	0	0	0
	I_{elO} (ma.)	.083	0	.02
P	V_{elp} (volts)	.889	.898	.77
	I_{elp} (ma.)	.537	.54	.48
Q	V_{elQ} (volts)	-3.83	-3.97	-3.72
	I_{elQ} (ma.)	2.21	2.26	2.2
R	V_{elR} (volts)	-3.52	-3.7	-3.47
	I_{elR} (ma.)	2.2861	2.37	2.38
S	V_{els} (volts)	0	0	0
	I_{els} (ma.)	3.2861	3.42	3.27

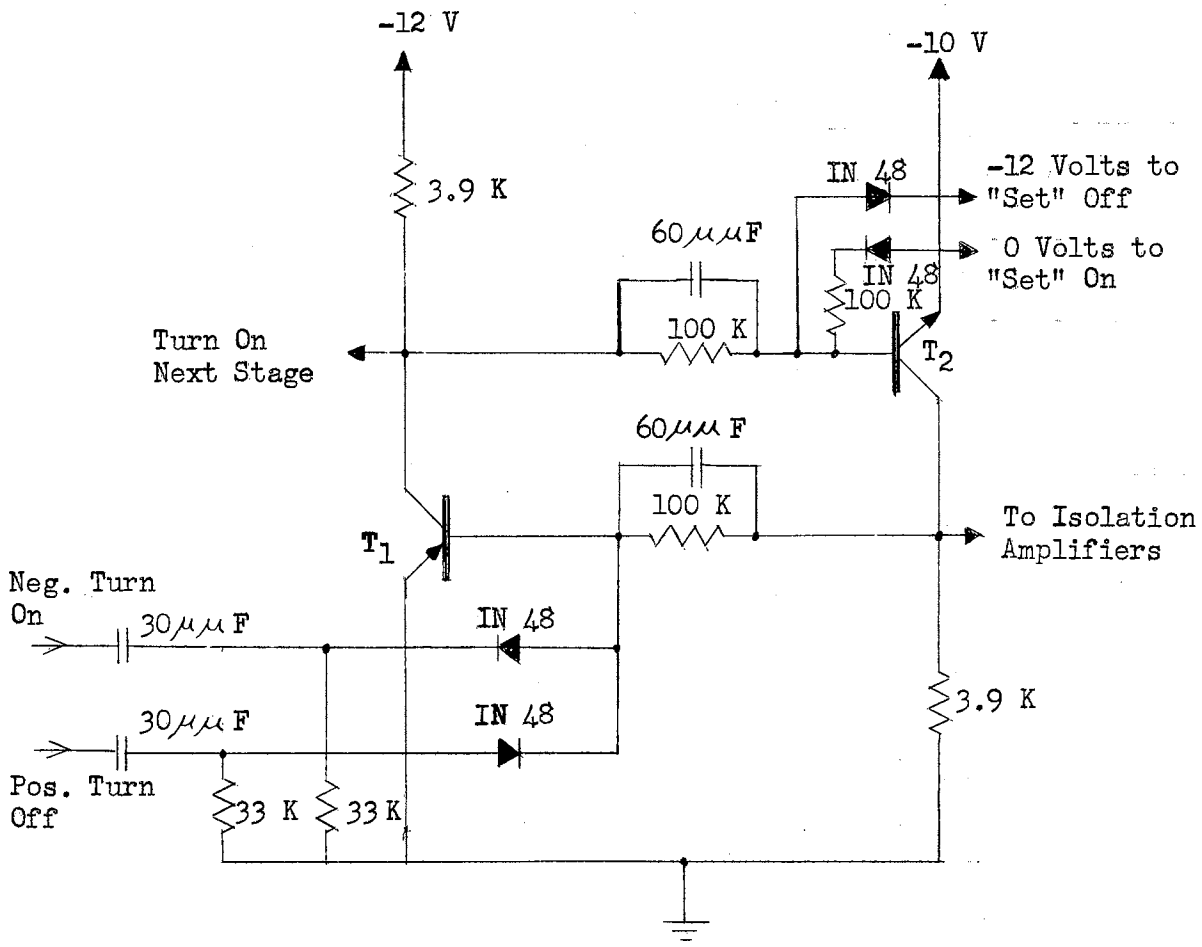


Figure 11.

Complete Bistable Circuit

negative pulse obtained from the collector of the PNP transistor of the preceding stage is used to provide the "turn on" pulse, and will occur when the preceding stage is "turned off" by the bistable driver. The only difference in the triggering circuits for "turn on" and "turn off" is the direction of the diodes. The 33 K ohm resistor is used to eliminate part of the transient effects after the application of a pulse. Without it, the decay time for the voltage between a capacitor and a diode was 65 usec. Using the 33 K ohm resistor this time was decreased to only 5 usec. Although this time may be decreased further by using a smaller value of resistance, the amplitude of the pulse will be decreased so much that it will not trigger the flip-flop. A reduction in the size of the capacitor will cause the same deterrent effects. The circuit may be set to the "off" condition simply by connecting the base of the NPN transistor directly to the 12 volt supply. Since nine stages must be initially set in the "off" state, diodes must be used between each stage to provide isolation during the operation period. An alternate procedure, but much less preferred, would be to employ nine separate switches for connecting to base to the voltage supply. A connection of the base to ground potential will provide the bias required to set the flip-flop in "on" condition. Because this bias is large, a 100 K base current limiting resistor is used.

Bistable Driver

To drive the ring counter, a conventional Eccles-Jordon flip-flop was chosen because it could be readily triggered from one point using steering diodes. A complete design procedure is given by Shea[8], and

[8]R. F. Shea, Transistor Circuit Engineering, Wiley, New York, 1957, p. 330.

therefore only the results of the design will be given here. Using a supply voltage of 12 volts and matched PNP transistors having a value β of 35, $F_\alpha = 4 \times 10^6$ cycles per second, and $V_{be} = .18$ volts, the circuit shown in Figure (12) was synthesized. The 100 ohm resistor was carefully chosen experimentally to give as large a collector swing as possible without saturating the transistors during their conduction period.

The usable range of input pulse amplitude may be increased by biasing the steering diodes with the collector voltages as shown in Figure (12). It was found experimentally that a trigger pulse amplitude of -2.7 volts with a duration of 2 microseconds would trigger the driver from zero to 320 kc if input capacitors with values of 270 uuf were used. This value of capacitance is a compromise because a larger value would decrease the necessary trigger pulse amplitude, but would decrease the maximum pulse repetition rate.

The output voltage of the driver is taken from the collectors of the transistors. The collector voltage of T_1 is used to "turn off" any odd stage in the ring counter which happens to be on, whereas the collector voltage of T_2 is utilized in "turning off" any even numbered stage. Because there are a total of ten stages in the counter, each collector voltage must be capable of driving five stages. Although each stage will introduce a direct shunt on the regenerative loop and will tend to downgrade the performance[9], the placement of all five stages on the collector had a negligible effect.

---

[9] N. F. Moody and C. D. Flordia, Some New Transistor Bistable Elements for Heavy Duty Operation, IRE Transactions, CT 4, 1957, p. 241.

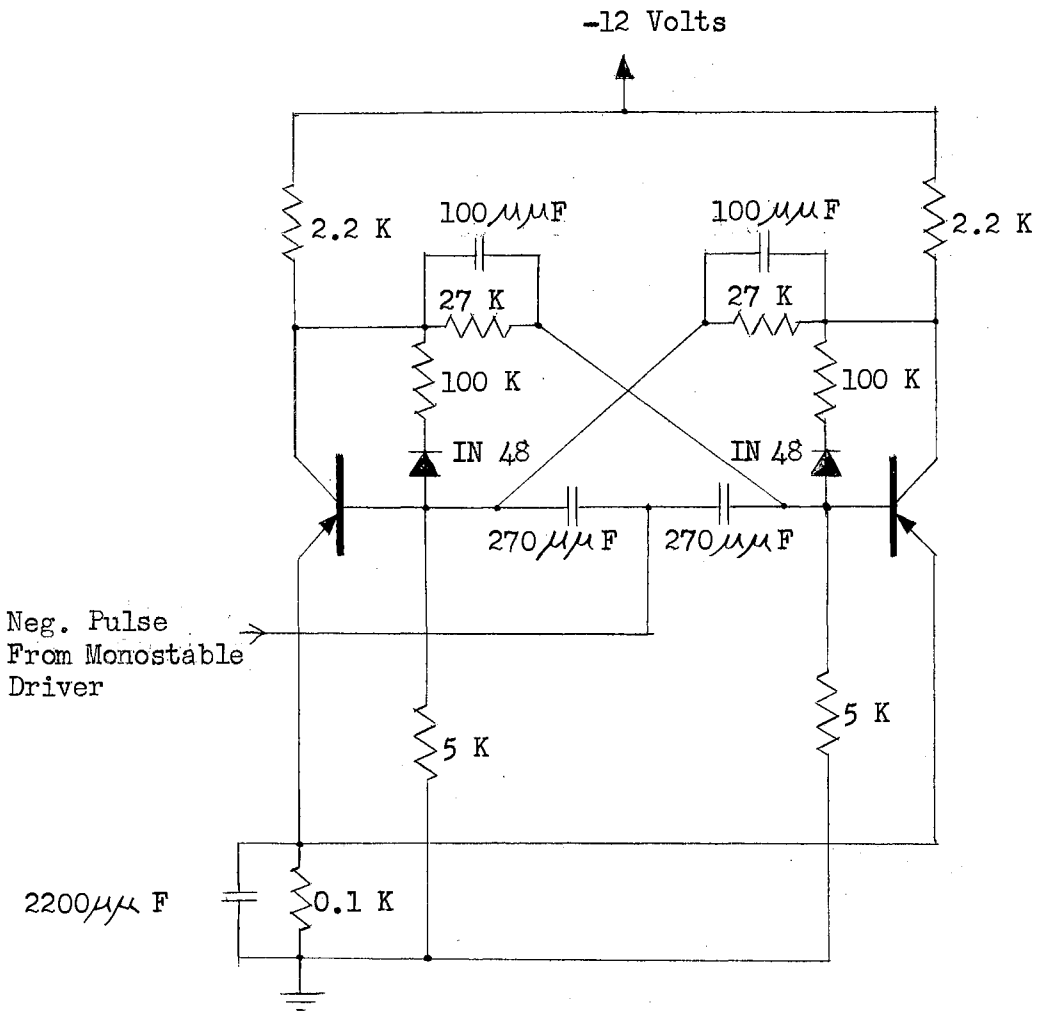


Figure 12.

Complete Circuit for the Bistable Driver.

Synthesis of Monostable Driver

The bistable flip-flop used to drive the counter will operate over a wide frequency range only when the trigger pulse is of the proper amplitude and duration. To provide a triggering pulse for the driver, a monostable driver may be employed (see Figure 16). The proper amplitude of the pulse may be obtained by dividing the load resistor of the monostable driver into two resistors so that the sum of these is still equal to the value of the load resistor. This is simply a voltage divider. The proper duration of the trigger pulse may be obtained by designing the monostable circuit to have an "on" time equal to this duration.

The monostable driver was designed using the same supply voltage as the bistable circuit, but using different values of load and base current limiting resistors. The selected transistors had the following characteristics:

$\beta_1 = 100$ $\beta_2 = 74$ for low emitter current densities.

$\beta_1 = 74$ $\beta_2 = 64$ for high emitter current densities.

$I_{co1} = 1.5 \times 10^{-6}$ $I_{co2} = 1.5\ 10^{-6}$

$V_{be1} \approx .24$ volts $V_{eb2} \approx .18$ volts

Employ design equations (81) through (86) and select I_{c1}(max) as 5.5 ma.

1. Select $R_{L1} = R_{L2} \approx E_{b1}/I_{c1} = 12/.0055 = 2.18$ k

use 2.2 k ohms.

2. Select E_{b2}

$$E_{b2} < 12 - .15 - (1.5 \times 10^{-6}/1 - .985 + 4.3 \times 10^{-6})\ 2.200 - X$$

$$< 11.62 - X$$

If X is 1.62, E_{b2} may be 10 volts.

$\therefore$ Use E_{b2} 10 volts.

3. Select $R_{b2} = R_{b1}$

(a) $2200 \ll R_{b2} < 10 - 12 \quad .15 \quad .2241/4.3 \times 10^{-6}$

$2200 \ll R_{b2} < .378 \times 10^{6}$ ohms

(b) $$2200 \ll R_{b2} < \frac{10 - .2}{10/2.2(1-.985/.985) - 4.3 \times 10^{-6}/.985}$$

$2200 \ll R_{b2} < .147 \times 10^{6}$ ohms.

(c) $$2200 \ll R_{b2} < \frac{10 - .15}{12/2200(1-.985/.985) - 1.5 \times 10^{-6}/.985}$$

$2200 \ll R_{b2} < .1176 \times 10^{6}$

Choose 100 k ohms to satisfy all three inequalities.

The final selection of R_L and R_b to be used in the monostable driver may now be used to calculate the static characteristic curve for the circuit. Both exact and approximate calculations are compared with the experimental results in Figure (11). The circuit in Figure (9) was used to obtain the experimental results. Table 2 gives the coordinates of each of the points of the curve as calculated and measured.

To provide monostability, a resistor must be placed across the terminals "V_{el}-I_{el}", that has a value greater than V_{elp}/I_{elp}. Using the experimental values from Table 2 gives a resistance of 990 ohms, so a value of 4000 ohms was selected to provide a margin of safety. The dc load line of this resistor is drawn in Figure (13) to indicate a stable "off" condition. Employing equation (89) in Chapter 2, C may be calculated to be $1.08 \times 10^{-3}t$ where t is the total time that the circuit will be maintained in the "on" condition. The calculated values

are compared with the experimental results in Figure 14. Note that for small values of capacitance, the experimental results are somewhat non-linear because the total "on" time is of the same order of magnitude as the time required for "turn on" and "turn off". A value of C of 2200 uuf was selected to give an approximate 2.4 microsecond "on" time. One factor which is neglected in the preceding calculations is the base current drive used to trigger the circuit. It was discovered that a large base drive would give a relatively longer "on" time than a small one. The proper pulse amplitude of 2.7 volts to be applied to the bi-stable driver was obtained by using a 0.6 K resistance along with another of 1.6 K as a voltage divider. Since the maximum pulse amplitude at the collector is -10 volts, a ratio of 0.6 to 2.2 will result in approximately -2.7 volts. This neglects loading effect.

As a rule, base driven flip-flops are far more sensitive than collector-driven flip-flops. Furthermore, if positive trigger pulses are to be used, they should be routed to the NPN transistor. The input capacitor of 270 uuf seemed to be the best choice to provide good trigger sensitivity and still maintain a maximum pulse repetition rate of 320 kc. The monostable circuit as shown in Figure (16) will operate satisfactorily from zero to 50,000 pulses per second using triggering pulses having a minimum amplitude of 3.5 volts. Figure 15 gives the minimum pulse amplitude required for satisfactory operation for a pulse repetition rate to 300,000 pps.

Isolation Amplifiers

To prevent loading on the flip-flop and still provide both negative and positive outputs, two isolation amplifers are employed. Both

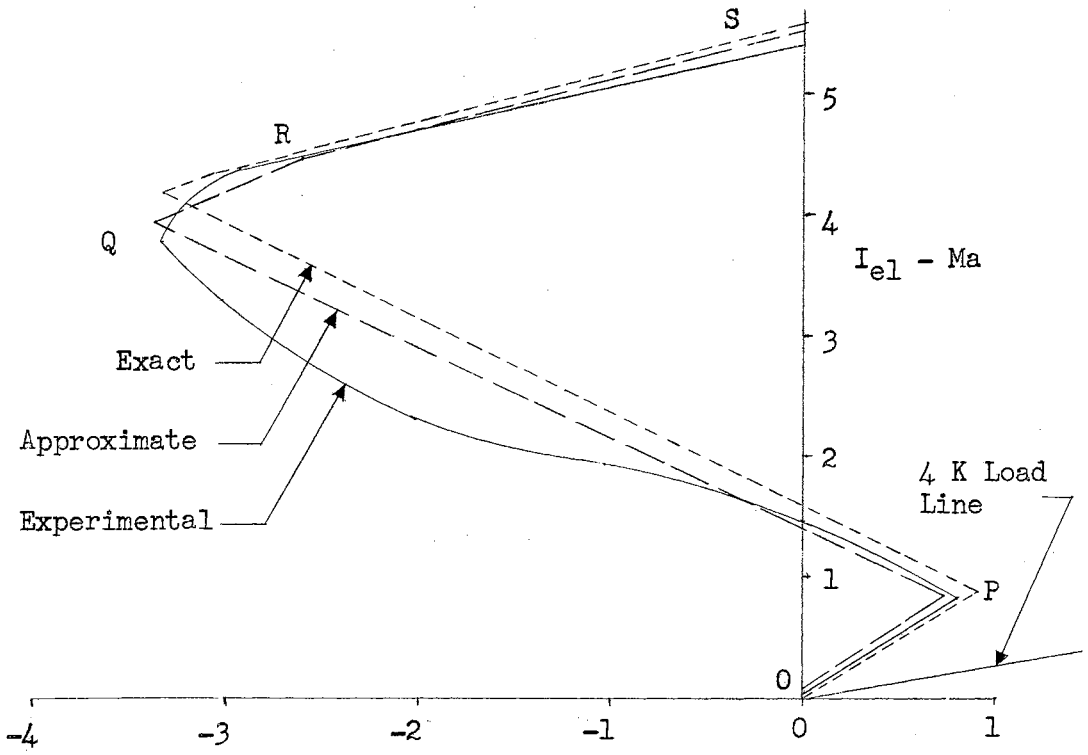


Figure 13. Static Characteristics for the Monostable Circuit.

TABLE II

COORDINATES OF POINTS FOR FIGURE 13

Point		Exact	Approximate	Experimental
O	V_{el0} (volts)	0	0	0
	I_{el0} (ma.)	.15	0	.05
P	V_{elp} (volts)	.769	.91	.82
	I_{elp} (ma.)	.912	.921	.85
Q	V_{elQ} (volts)	-3.43	-3.37	-3.5
	I_{elQ} (ma.)	3.92	4.12	3.75
R	V_{elR} (volts)	-2.58	-3.1	-3
	I_{elR} (ma.)	4.31	4.14	4.2
S	V_{els} (volts)	0	0	0
	I_{els} (ma.)	5.53	5.6	5.5

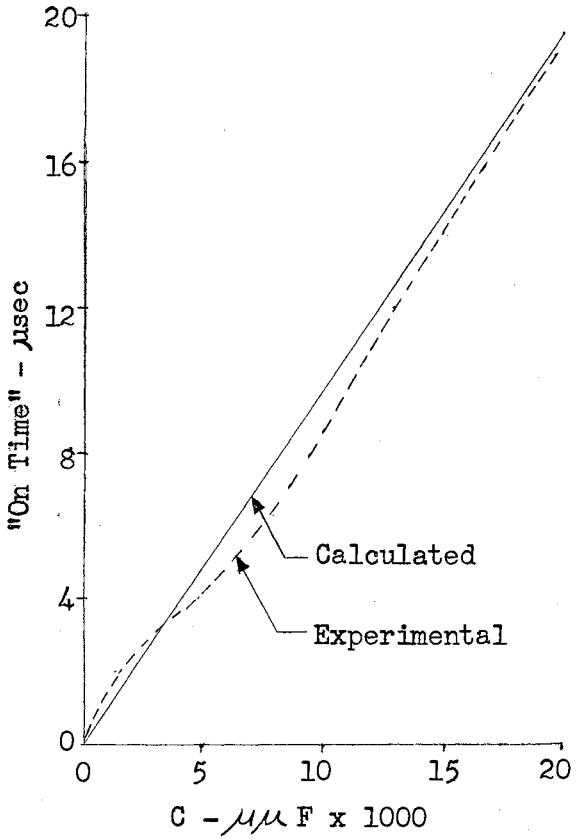


Figure 14.
"On Time" vs. Capacitance

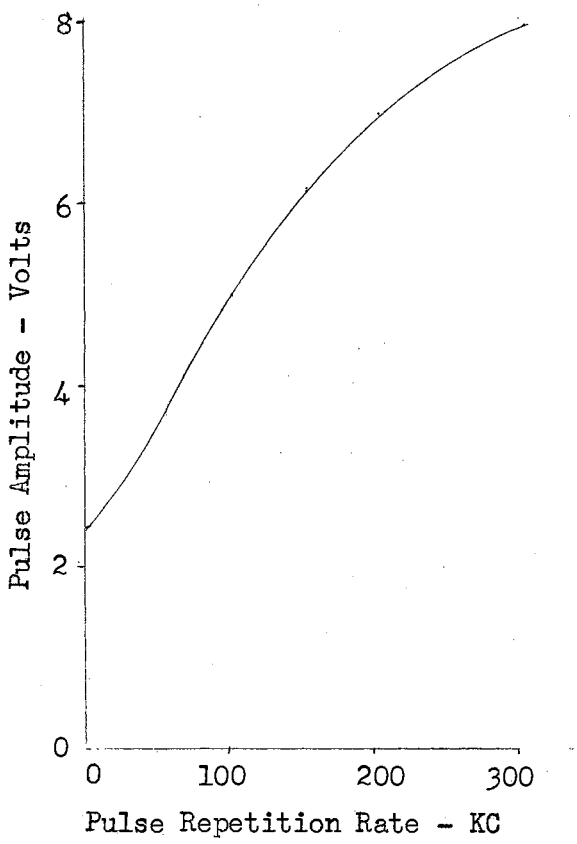


Figure 15.
Minimum Trigger Amplitude for
Satisfactory Operation

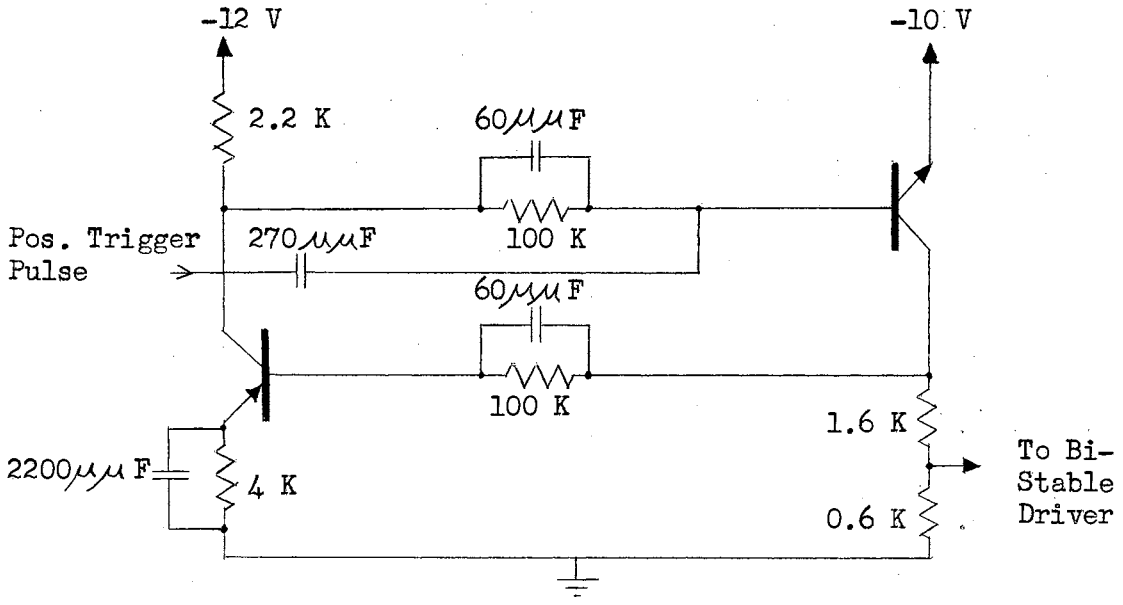


Figure 16. Complete Monostable Circuit

of the circuits (Figure 17) are non-conducting except when the bistable circuit is conducting. This gives the advantage of a fast "turn on" because minority storage effects do not enter into the picture. Another advantage is smaller power consumption due to the low duty ratio. Both amplifiers are driven from the negative pulses obtained from the collector of the NPN transistor. In order to obtain both a positive and negative pulse, it was necessary to use one common emitter PNP stage and one common collector PNP stage. The load resistors for each stage was selected as 6.2 K. Because the input impedance of the common collector stage is very high, only 680 ohms were needed as a base current limiting resistor. The output impedance of a typical common collector stage is in the order of 600 ohms while that of a common emitter stage is in the order of 20 K ohms. The same values of base current limiting resistors and coupling capacitors were used as those employed in the basic flip-flop. Any transistor with a current gain of 20 or greater will operate satisfactorily in the common emitter circuit using the 100 K ohm base current limiting resistor and the 6.2 K ohm load resistor.

No further investigation of these amplifiers seems necessary since they are rather common in the literature and are not actually a part of the counter circuit.

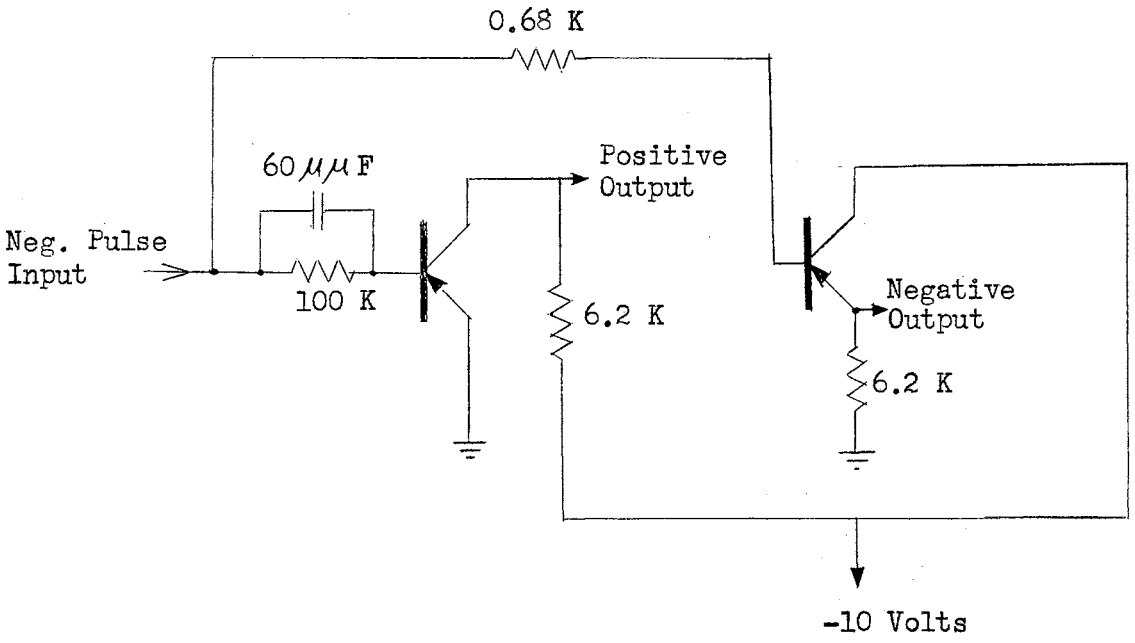


Figure 17.

Isolation Amplifiers.

CHAPTER IV

COUNTER PERFORMANCE

Using the circuits developed in Chapter III, the entire counter was constructed and tested in the laboratory with very good results. Both a fast "negative" and "positive" ten volt output was obtained simultaneously. The "turn on" time of each of these outputs was 0.2 micro-seconds while the "turn off" time was 2.5 micro-seconds. The minimum triggering pulse required for satisfactory operation increased with the pulse repetition rate according to Figure (15) in Chapter III. The maximum pulse repetition rate measured in the laboratory was 320,000 pulses-per-second. As a reliability test, the counter was allowed to operate continuously for several hours. At the end of this time no apparent failure had occured.

The power demanded from the two power supplies was measured for various pulse repetition rates. The current drain from the 12 volt power supply varied from 9 to 10 milliamperes as the pulse repetition rate was varied 0 to 320,000 pulses-per-second, while the current drain from the 10 volt power supply varied from 6 to 7 milliamperes. This gives a total power consumption of 168 and 190 milliwatts for low and high pulse repetition rates respectively. Transistors having a current gain from 40 to 100 were used without necessitating any change of circuit components. Figure (18) shows only the first and second stages of the counter connected to the monostable and bistable driver as an integral unit. The last eight stages are identical to the second stage.

It should be noted that the only difference between the first and second stages is the "set" circuit. Stage one had been designed to turn on when the "set" switch is closed while stage two and the remaining eight are designed to turn off when their "set" switches are closed. The output of the diode of the last nine stages may be connected together since the diodes serve to isolate them from each other. Thus only a DPST switch is needed to "set" the entire counter. In order to cause "turn off" of stage one with the application of the first electrical pulse, the bistable driver should be set to deliver a positive pulse from the collector of the transistor connected to the odd numbered stages. No provision was made to "set" the bistable driver since the counter's particular application was not known.

TABLE III

VALUES OF CIRCUIT COMPONENTS FOR FIGURE 18

R	Components (ohms)	C	Components (uuf)
R_1	3.9 K	C_1	60
R_2	100 K	C_2	270
R_3	0.68 K	C_3	30
R_4	6.2 K	C_4	100
R_5	33 K	C_5	2200
R_6	2.2 K		
R_7	27 K		
R_8	0.1 K		
R_9	0.6 K		
R_{10}	4 K		
R_{11}	1.6 K		

Note: All diodes are General Electric IN48

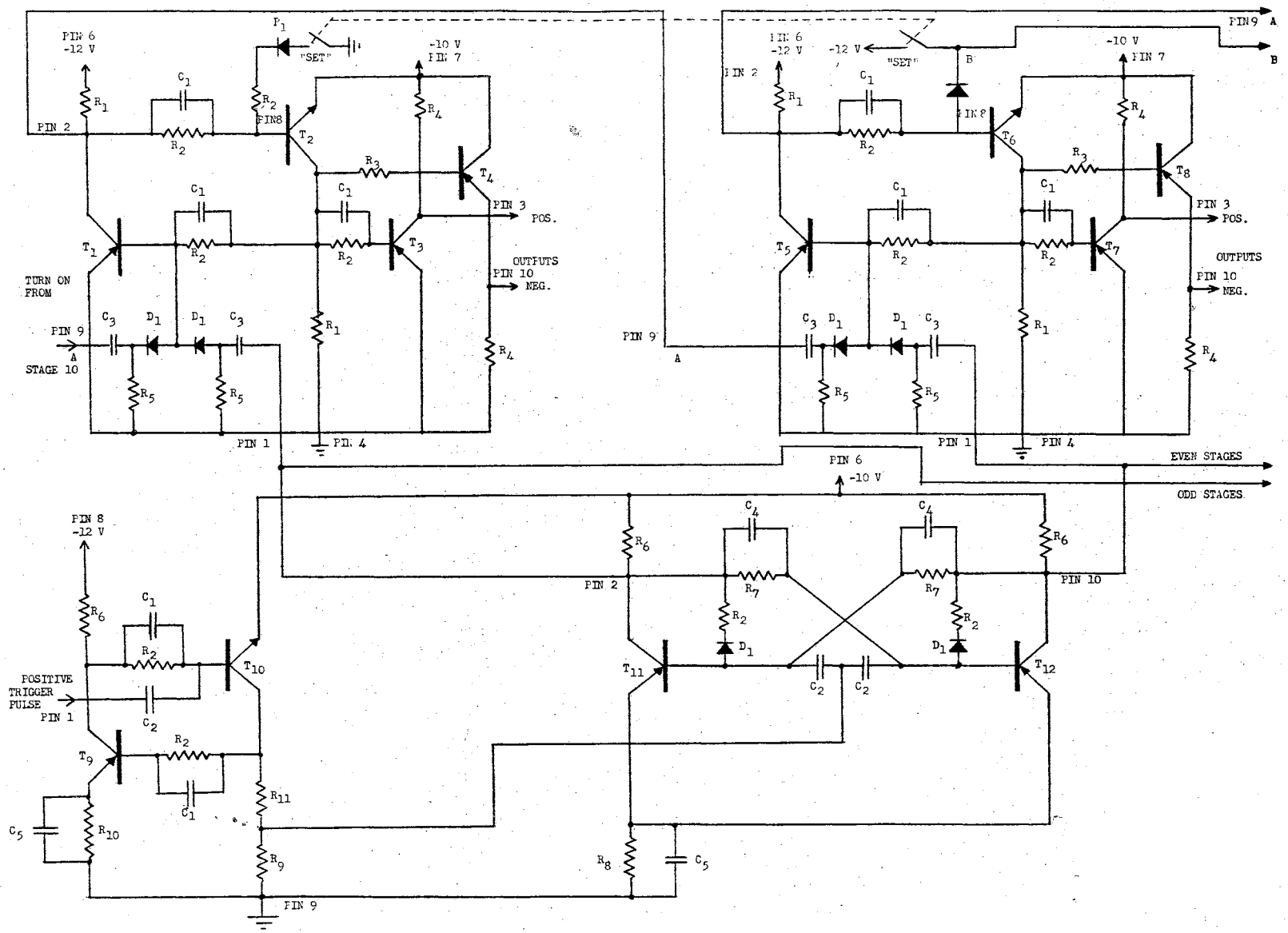
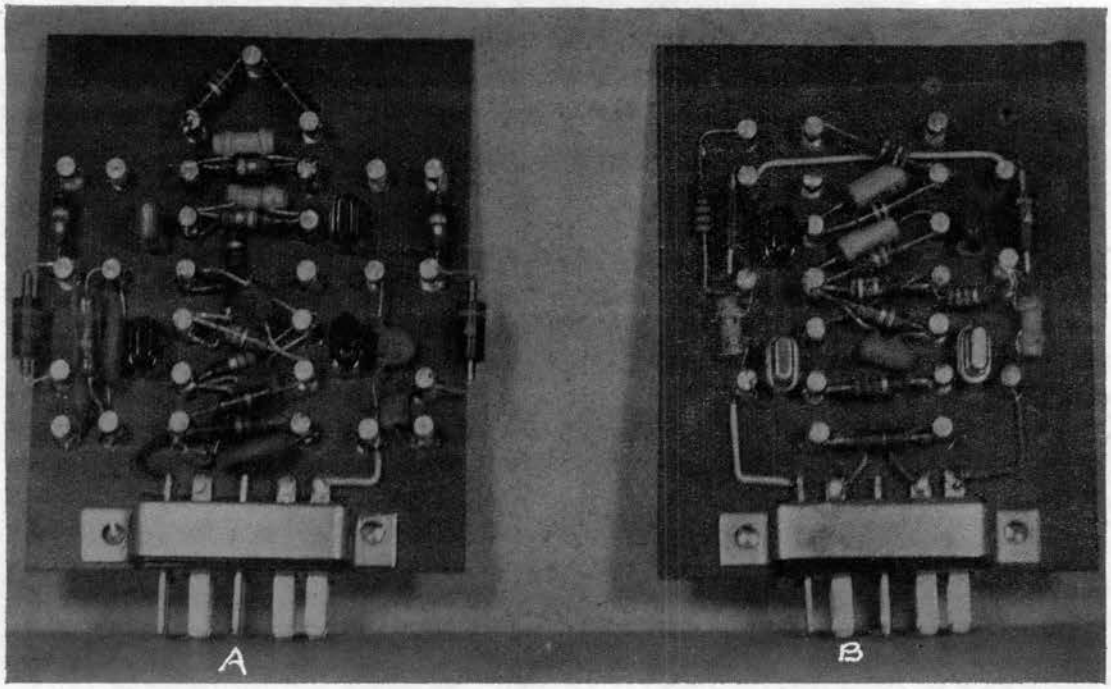


Figure 18. Counter Circuit with the First and Second Stages Only.

PLATE I



A. Driver Circuit

B. Typical Stage

CHAPTER V

SUMMARY

Before any attempt was made to design the ring counter, several types of counters were investigated. It was found that most of these employed a delay unit in principle. The counter which seemed to have the most favorable characteristics employed no delay units, whatsoever, and was dependent only upon the transition times of the basic bistable building block and a bistable driver. A basic bistable device was developed and rigorously analyzed for static conditions using a negative impedance technique. Both exact and approximate equations were derived for calculating these characteristics which are necessary for predicting the circuit's mode of operation. Following the static analysis, a procedure was given for determining the proper sizes of resistors to insure a bistable mode of operation. These values in turn may be used in the static equations to determine the actual static characteristics of the circuit. The only proof given for the validity to the equations were analytical checks and experimental results. Since such a proof would be quite rigorous, it was felt that it would be beyond the scope of this work and might be suggested as an area for further investigation. Once the static equations were developed, it was seen that by placing a simple resistor in the circuit, monostability could be obtained. A method was given for obtaining monostability and predicting the "on time". Little attention was directed toward an analysis of the transient "turn on" and

"turn off". First, this problem might well be the subject of work of this scope, and secondly, the counter was to be operated at relatively low repetition rates. An analysis was given, however, of the maximum possible frequency at which the counter could be operated. Employing the design equations, a numerical synthesis of the bistable circuit and the monostable circuit was given. The components determined by the design equations were then used in the equations for determining the static characteristic. Both exact and approximate equations were used and were compared with experimental results. In both cases it was seen that the approximate equations are satisfactory for most engineering purposes and agreed with results measured in the laboratory. Since a conventional Eccles-Jordon flip-flop was used as the bistable driver, little attention was directed toward presenting its design theory. The same may be said for the isolation amplifiers which were built to provide an isolation between the main counter and its load.

Using the results of Chapter III, the counter was built and tested in the laboratory as an integral unit. It was operated over long periods of time without any apparant failure and up to a maximum pulse repetition rate of 320,000 pulses per second. Power requirements were less than 0.2 watts for all frequencies of operation.

It is felt by the author that much higher speeds of operation might be obtained if different triggering techniques could be employed. Also, since the load resistors of the basic flip-flop place a direct shunt on the regenerative loop, a transient analysis might lead to the conclusion of employing inductances in series with these resistors. This is suggested as another possible area of investigation.

SELECTED BIBLIOGRAPHY

Millman, Jacob and Taub, Herbert. Pulse and Digital Circuits, McGraw-Hill Book Company, Inc. New York, Toronto, London, 1956.

Moll, J. J., et al. PNPN Transistor Switches, Proc, IRE, Vol. 44, September, 1956.

Richards, R. K. Arithmetic Operations in Digital Computers, D. Van Nostrand, New Jersey, 1955.

Richards, R. K. Digital Computer Components and Circutis, D. Van Nostrand, New York, 1957.

Suran, J. J. and Reibert, F. A. Two Terminal Analysis and Synthesis of Junction Transistor Multivibrators, Proc, IRE, Vol. 1, CT-3, March, 1956.

VITA

Billy Wayne Whitlow

Candidate for the Degree of

Master of Science

Thesis: A TRANSISTORIZED DECADE RING COUNTER

Major Field: Electrical Engineering

Biographical:

Personal Data: Born at Black Rock, Arkansas, January 4, 1934, the son of Martin E. and Maxine B. Whitlow.

Education: Attended grade school in Hoxie, Arkansas; graduated from Hoxie High School in 1951; attended two years at Arkansas State College, Jonesboro, Arkansas; received Bachelor of Science Degree from Oklahoma State University, with a major in Electrical Engineering, in January, 1958.

Professional Experience: Entered the United States Army, August 25, 1954, and served as a Nike Missile Mechanic until released in May 24, 1956. Was employed by Union Carbide Chemical Corp. during the summer of 1957 as assistant in an analogue computer laboratory, and by the Federal Aeronautical Administration during the summer of 1958. During the spring semester, 1959, he was an instructor in the Department of Electrical Engineering for Oklahoma State University. He is a member of the American Institute of Electrical Engineers and Institute of Radio Engineers.