PNPN FOR MOTOR CONTROL

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PREFACE

In recent years there has been much work done trying to reduce the size of workable circuits to something that would save weight and space and at the same time increase performance.

It is the object of this study to develope a workable motor control circuit using semiconductor devices wherever possible. It is desirable to develope a circuit that could, when powered by ac, control a dc motor.

I would like to express my graditude to Dr. H. T. Fristoe for his suggestions and assistance. I am also indebted to Mr. Frank Carden for his contribution to this paper.

Finally, I would like to thank my wife, Marilyn, for her work in typing this thesis.

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CHAPTER I

THE SEMICONDUCTOR

In the early days of the electrical industry much was done in the way of research into the conductivity of different materials. The basic needs of the industry were good conductors and poor conductors or insulating materials. Very little attention, if any, was paid to the materials that fall between these extremes. However since 1948 a great deal of interest has arisen in the materials in this weak conductor or semiconductor range.

In 1948 a team of engineers and scientists from the Bell Telephone Laboratories announced the developement of the transistor. This seems to be the starting point of a greater part of the developement as well as the advances and refinements in semiconductor materials. Many types of semiconductors have been developed, both elemental and compound types, but because of the nature of this discussion and the similarity of all the types, only the material silicon will be considered.

Silicon is an elemental type semiconductor and appears in the fourth column of the periodic table along with diamond, lead, germanium and tin. The silicon atom has four electrons in its outer orbit that readily react or combine with other atoms. Because of this characteristic, under controlled conditions, molten silicon can be solidified into a single crystalline structure in which each atom is equidistant from four adjoining atoms forming a co-valent bond. Figure 1 is a two dimensional representation of this structure. In this figure each circle represents the silicon nucleus and the orbital electrons, except the valence electrons, and has an electronic charge of plus four. The dashed lines represent the valence electrons and the co-valent bond that holds the atomic structure together. These electron pairs can only be disrupted by the expenditure of energy. In the case of silicon the energy required to move an electron from the valence band to the conduction band is approximately 1.1 electron volts.

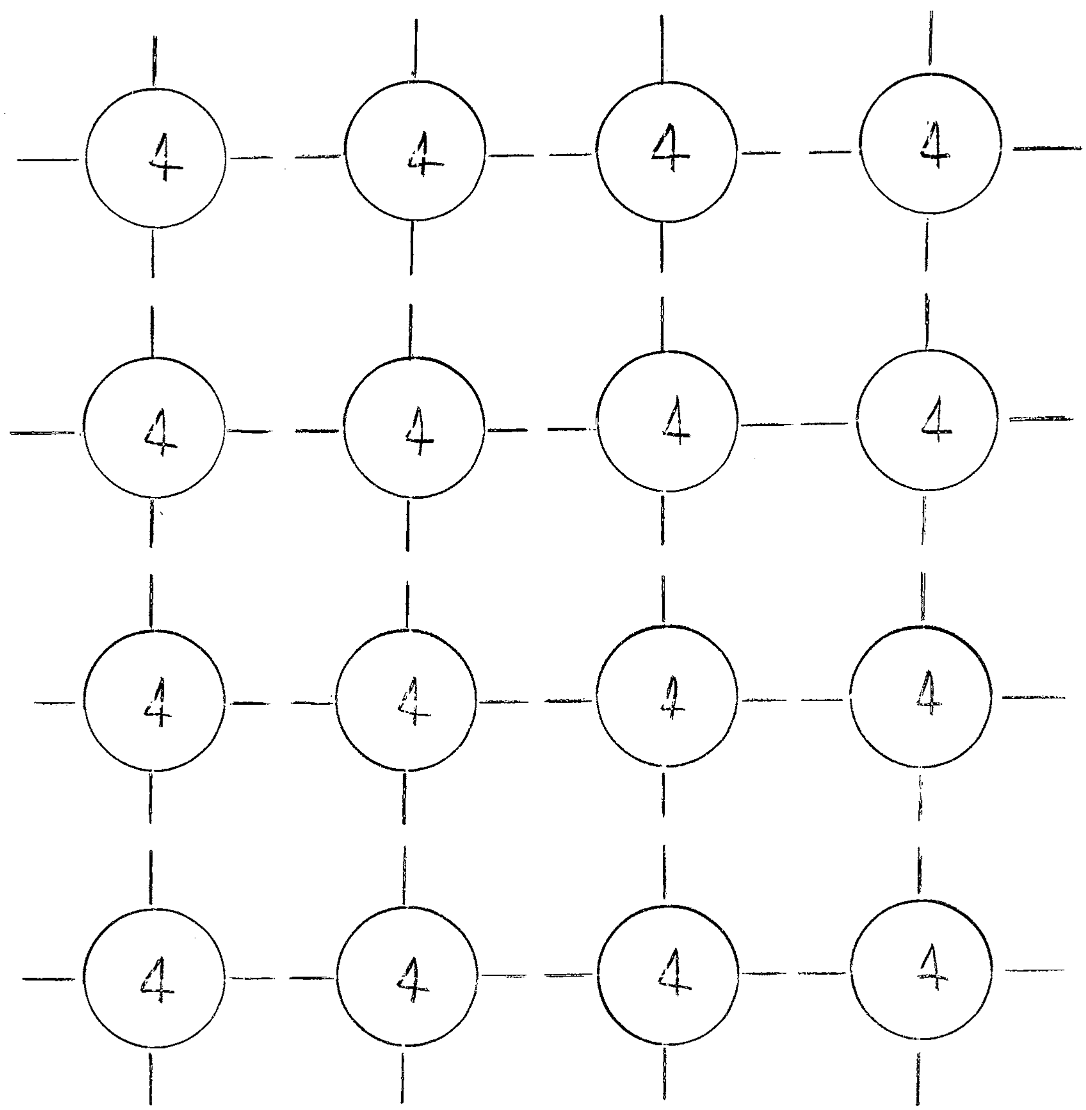


Figure 1. Silicon Crystalline Structure

Because of the thermal energy present at any temperature other than absolute zero, the crystal lattice is in a state of continuous random motion. Because of this random motion the co-valent bond is sometimes broken allowing one of the electrons to move about freely and leaving a hole free to acquire another electron under favorable conditions. The free electron now is allowed to move about in much the same manner as a molecule in a gas.

If an electric field is impressed upon the crystal the free electron will be attracted to the positive pole and repelled from the negative pole. Since there will be more than one free electron in the crystalline structure there will be a movement of all these free electrons in the direction of the positive pole. This movement represents the flow of current carried by electrons.

Returning to the point where one of the electrons broke free from the co-valent bond, the absence of the electron, indicated by a hole, is free to receive another electron. When this hole is filled with a different electron it means, not the loss of a hole, but the existance of a hole in the place where that electron came from. In effect then, we have a movement of holes from place to place and, in the presence of a field, a current carried by holes in the direction of the negative pole. Since this hole current is both opposite in polarity and reverse in direction, it in reality is an addition to the current carried by the electrons.

This hole current might be better visualized if the movement of electrons in the valence band were considered. When the electrons left the valence band to go into the conduction band, they left a positively charged atom which seeks another electron. These electrons are still in the valence band and are not free to move at random, hence their movement is somewhat slower than the movement of the electrons in the conduction band. Their total movement is in the same direction as the movement of the conduction band electrons, therefore they constitute an electron current in the same direction as the previously described current. The total current then is the sum of the two. The conductivity of an intrinsic or pure semi-conductor can be represented by the equation:

$$\sigma = q n \mu_N + q p \mu_P$$

where σ is the drift conductivity in mhos per cm.

q is the charge of the electron (or hole) in coulombs.

p is the concentration of holes per cubic cm.

n is the concentration of electrons per cubic cm.

μ_N, μ_P is mobility of free electrons and holes, cm per sec./volt per cm.

The total current therefore can be represented by the equation:

$$i_t = E\sigma = E q N_i (\mu_P + \mu_N)$$

where E is the applied electric field in volts/cm. and

$N_i = p = n$

Of course the concentration of electrons and holes is dependent upon temperature. This relationship is shown by the equation:

$N_i = AT^{3/2} e^{-qE/2KT}$

where A is a constant for the material.

T is the absolute temperature.

e is the natural logarithm base.

K is Boltzmann's constant.

If an impurity, such as indium, were introduced into the crystal structure, there would result a structure with an excess of holes. This would come about because of the atomic structure of indium. It has a valence of three, therefore, in forming a co-valent bond with the silicon the excess of holes would show up. If we now apply an electric field to the crystal the holes may move. This movement of holes would be in excess of the normal electron and hole movement found in an intrinsic semiconductor. Addition of these impurities creates what is commonly called a P-type semiconductor since the majority of electronic carriers can be considered as positive charges. Extremely small amounts of an impurity can greatly alter the electrical properties of a semiconductor. Valence three impurities are acceptor impurities because they can accept an electron from the valence band leaving a positive hole.

Impurities with five valence electrons enter into chemical bond, forming N-type semiconductors. When such an impurity is added to silicon, four of these electrons enter into the normal co-valent bonds. The remaining electron is loosely bound to the impurity atom, say antimony, and corresponds to an electron in the conduction band which is free to conduct upon application of an electric field. Valence five impurities are called donor impurities because they donate an electron to the conduction band. The action at the junction of two of these types will be described in chapter two.

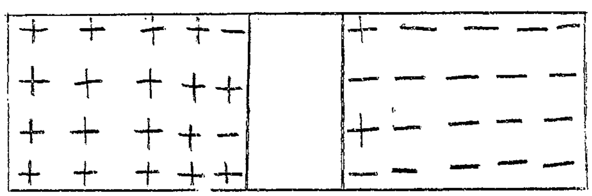
CHAPTER II

P-N JUNCTIONS

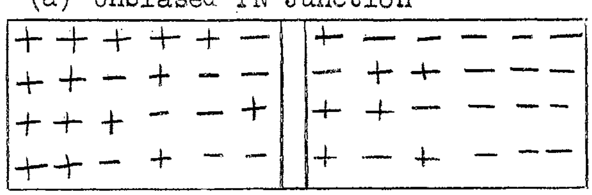
Consider a boundry between a P-type region and an N-type region in the same crystal. This boundry is known as a P-N junction. Figure 2-A represents such a junction. There is a tendency for some of the P-type carriers to difuse into the N region and for some of the N-type carriers to difuse into the P region. Or putting another way, the holes and electrons in the junction area combine, and the resulting ions produce an electric field to drive the remaining holes and electrons away from the junction, which in turn uncovers more ions. This field is called a barrier field and is on the order of 0.3 volts with the N region positive and the P region negative.

With the polarity noted above, holes produced in the N region, by the breaking of co-valent bonds, flow freely across the junction. In fact the polarity of the barrier field aids the flow of these holes and also the flow of the electrons from the P region. In the unbiased junction the flow of the intrinsic minority carriers is exactly counter-balanced by an equal and opposite flow of majority carriers which have acquired from thermal sources the energy required to travel across the junction against the barrier field potential. The width of the uncovered region adjusts itself so that the resulting value of the energy required makes the number of carriers crossing against the barrier field equal to the number of intrinsic carriers that cross the junction with the aid of the field. Equilibrium is thus automatically maintained.

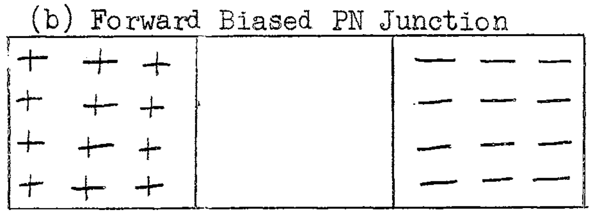
If an external electrical field is applied to the above crystal in such a way that the P region is made positive with respect to the N region, the junction is said to be forward biased. Figure 2-B represents such a junction. Since the P region is now positive the holes in the P region are repelled or pushed into the N region and the N region being negative repells electrons or pushes them into the P region. The holes in the N region then travel on toward the negative end of the region but as they travel they recombine with the electrons. Because of this the density of the holes in the N region is greatest near the junction and decreases toward the thermal equilibrium value as the distance away from the junction increases. The same reasoning holds true for the electrons in the P region. Figure 3-A is a graphical representation of the effect on minority carrier densities when the junction is forward biased. As shown in figure 3-B the density of majority carriers is so much greater than the density of the minority carriers, that it (majority carrier density) is almost constant.



(a) Unbiased PN Junction



(b) Forward Biased PN Junction



(c) Reverse Biased PN Junction

Figure 2. PN Junctions

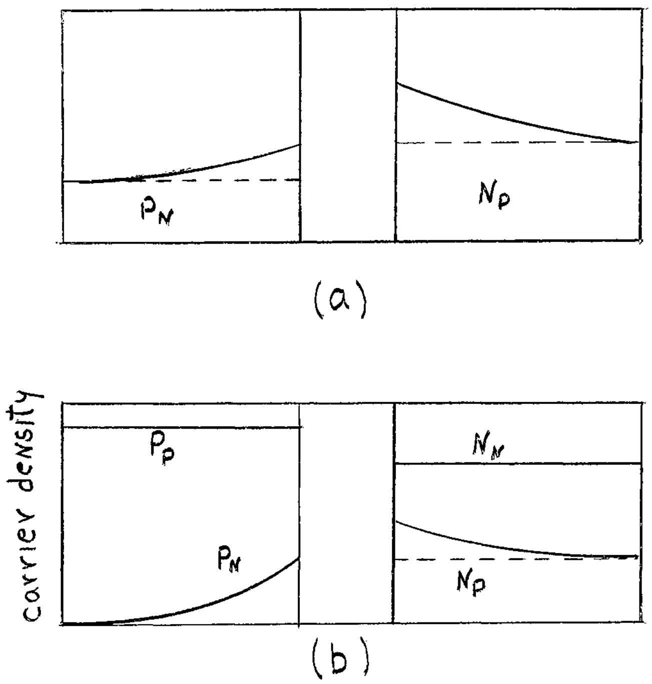


Figure 3. Carrier Diffusion

The mechanism causing the flow of current by minority carriers is called diffusion. If the recombination did not take place the two regions would attain new values of minority carrier density. However, holes continue to be repelled into the N region as long as the applied voltage is maintained. The diffusion of these holes away from the junction into the N region constitutes a current. This current is referred to as the diffusion current and is represented by the equation:

$$i_{dP} = q K \text{ grad } p$$

Where the constant of proportionality is called the diffusion constant for holes, D_p ; and grad p (∇p) is the density gradient of holes, therefore,

$$i_{dP} = q D_P \nabla_P$$

The same equation for electron flow then can be written as:

$$i_{dN} = q D_N \nabla_N$$

Now there are four elements of current flow in the biased P-N junction. Electron and hole flow due to drift and electron and hole flow due to diffusion. The total electron and hole current then are:

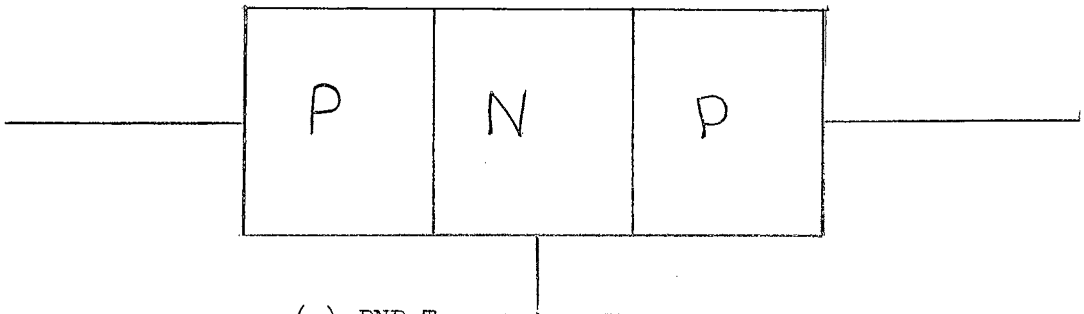
$$i_P = q\mu_P PE - qD_P \nabla_P$$

$$i_N = q\mu_N NE - qD_N \nabla_N$$

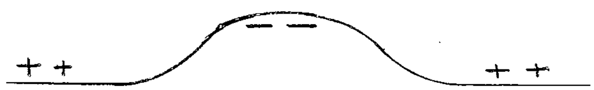
The direction of the currents is the same in both cases. Because of the opposite charge signs of holes and electrons, hole diffusion current flows in the direction of decreasing hole density, while electron diffusion current flows in the direction of increasing hole density. In other words, for each type carrier, drift current is proportional to the carrier density and to the potential gradient, while the diffusion current is proportional to the carrier density gradient.

It should be noted that the hole current in the N region depends upon the physical characteristics of the N region and the electron current in the P region depends on the physical properties of the P region. Therefore, by altering the conductivities of these two regions, the ratio of the current to electron current can be altered. Now if the external field is reversed, that is, the positive portion of the crystal is made negative and the negative portion positive, the junction is said to be reversed biased. Figure 2-C is a representation of this type of bias across a P-N junction.

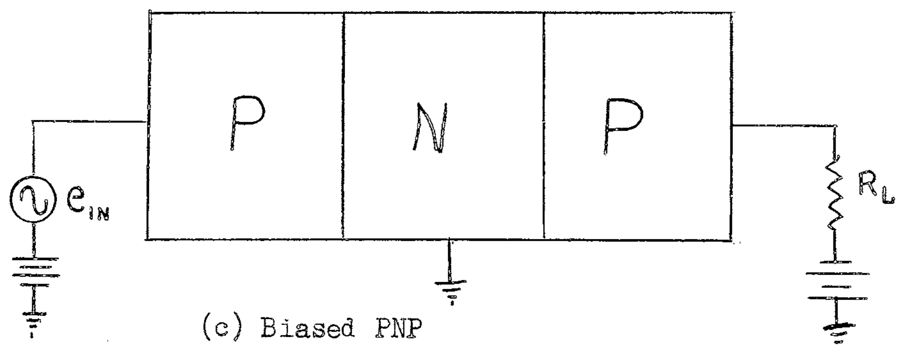
When the reverse bias is applied the action is similar to the action in the forward bias situation except opposite. The potential barrier that is already set up across the P-N junction, positive on the N side and negative on the P side, is increased by the application of the reversed field. This increase in the potential barrier tends to decrease the number of electrons leaving the N side and the number of holes leaving the P side. However, since the electrons in the P side are falling down the potential hill, as are the holes in the N side, their flow will not be effected. Instead of recombination after entering the P material, the holes from the N region join with the P material holes and drift away from the junction. The electrons in the P material act in much the same way. From this discussion it appears that the total current flowing in the reversed biased P-N junction is the sum of the holes in the N region and the electrons in the P region, crossing the junction and the drift of holes and electrons toward the negative and positive ends of their respective regions. It could be said then that the total flow of current across the junction is made up of the minority carriers in the N and P regions crossing to the opposite region. These principals will be used in the following chapter in defining a transistor.



(a) PNP Transistor Structure

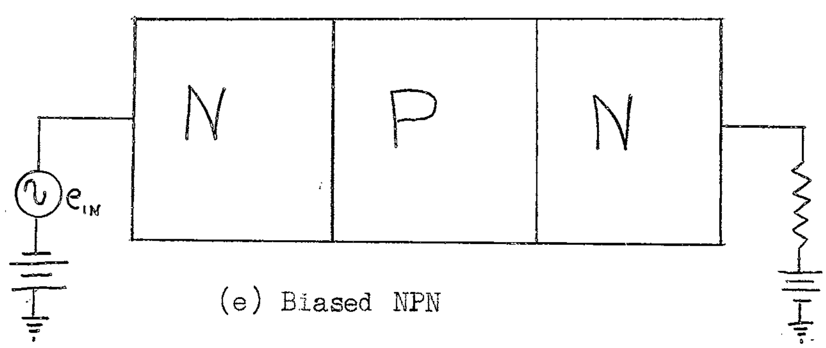


(b)Energy Diagram of Unbiased
Transistor



(c) Biased PNP

(d) Energy Diagram of a Biased
Transistor



(e) Biased NPN

Figure 4. Transistors

CHAPTER III

THE TRANSISTOR

The transistor is a single crystal with three different regions. Figure 4-A is a representation of an unbiased PNP type transistor. In the unbiased state the junctions between the P and N types behave as previously described. When the transistor is biased as shown in figure 4-C it yeilds very usable results. The emitter junction, as can be seen from chapter two, is forward biased. This is the direction of low resistance through the junction. Biasing the junction in this manner lowers the potential barrier between emitter and base to both electrons and holes. However, since the P type material is normally doped much heavier than the N type, (that is, there are more P type carriers in the emitter than there are N type carriers in the base) most of the current across the emitter junction will consist of holes flowing from the P-type emitter to the N-type base.

The collector junction then is reversed biased. This is the high resistance direction through the junction. The potential across this junction is made higher than in the unbiased case making the flow of holes from the P-type to the N-type almost impossible. Since the P-type material in the collector has a higher concentration of holes than the base has electrons, there is virtually no current flow across the junction due to the base and collector by themselves. It is their combination with the emitter that gives the desired results.

The emitter is firing holes across the emitter junction with very little resistance to their flow. In order that the holes do not combine with the electrons in the N region, the N region is made very narrow. In this manner the holes from the emitter diffuse through the N region with very little loss to recombination. This gives a great number of holes at the collector junction which is biased in such a way as to allow the holes to fall down the potential barrier into the P region and join the flow of holes in the P material to the positive end. It is this flow of holes that gives the power gain that is desired.

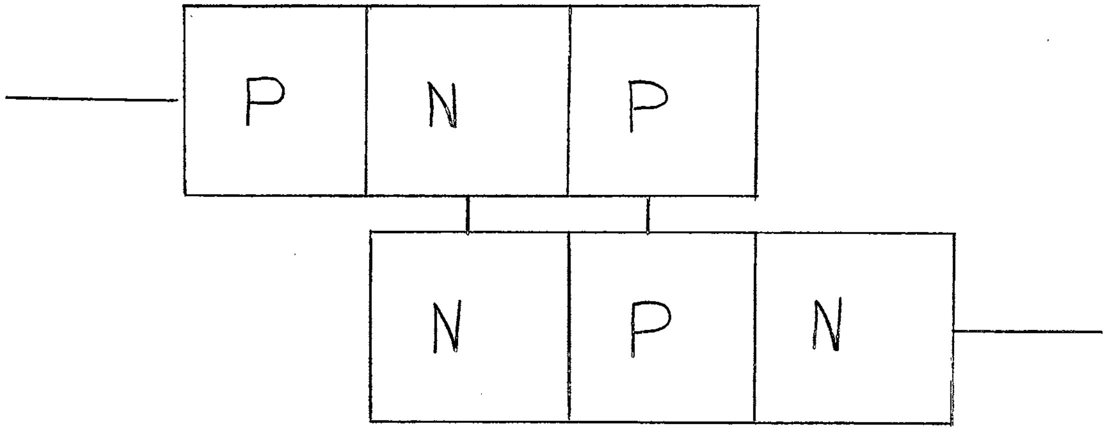
Power gain is achieved in the transistor because of the different impedance levels of the emitter and collector junctions. The impedance level of the emitter input to the transistor is essentially the impedance of a P-N junction biased in the forward direction. The current increases very nearly expotentially with voltage, therefore, this impedance could be expected to be very low and decrease for increasing emitter currents. In practice it may be in the order of 50 ohms. The collector junction is reverse biased and for large changes in applied voltage the current change is negligible. From this the collector could be expected to have very high output impedance. In practice this impedance may be a megohm or more. Because of this characteristic a load can be placed in the output circuit that will in effect reduce the voltage across the collector junction which in turn reduces the potential barrier somewhat. Since the current that is flowing is made up almost entirely of holes flowing down the potential barrier the current does not change. Since the current flowing in the collector circuit is the same current that crossed the low resistance forward biased P-N junction, the emitter and collector current will be approximately equal. Therefore, the power gain turns out to be a ratio of the load resistance to the emitter resistance. This is quite sufficient for this type device.

Figure 4-E represents a second type of junction transistor which, has found wide usage. This is the NPN transistor. The operation of this device is much the same as the PNP described above. The emitter junction is again biased in the forward direction (which means that for NPN structure the emitter will normally be negative with respect to the base). The collector is again reverse biased, therefore, the collector will be positive with respect to the base.

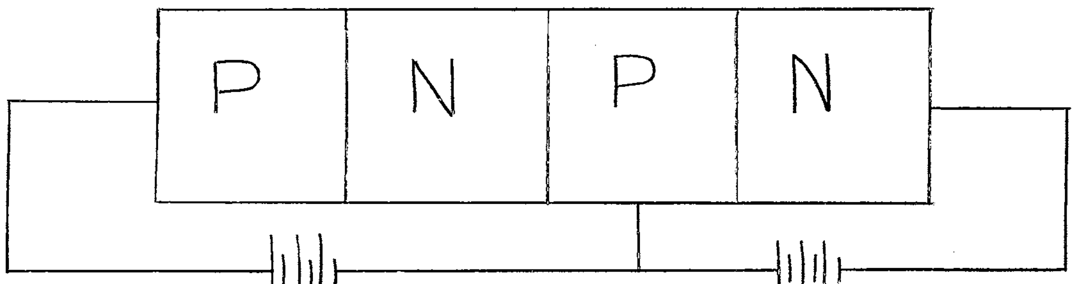
The N regions will be larger than the P region and will have a higher concentration of electrons than the P region has holes. It is clear then that the majority of the current across the NP junction will be of the electron type flowing from N-type emitter to P-type base. Again the base is a narrow region and the majority of the electrons that cross the N-P junction into the base will diffuse over to the PN junction. This junction is reverse biased and allows the large number of electrons that have crossed the P-type base to roll down the potential barrier into the N-type region. There these electrons join in the drift of electrons toward the positively biased end of the device. The power amplification is gained in the same manner as in the PNP type transistor. In fact the entire operation of the NPN is the same as that for the PNP except that the NPN device uses electron flow for its major carrier where the PNP uses holes. In a sense these transistors are compliments of one another and very often a circuit designed for one may be used with the other merely by changing the polarity of the biasing potentials. In certain types of circuits, this complimentary symmetry can be utilized to decided advantage, thereby allowing the transistors to be used in circuits in a manner not possible with vacuum tubes.

The device to be considered in this paper could be considered a combination of PNP and an NPN type transistor. The total result being PNPN.

Figure 5-A shows the mental picture one might use in thinking about the PNPN while figure 5-B shows the graphical representation of the PNPN and how it is biased. Figure 5-C represents the energy diagram of the unbiased PNPN semiconductor. 5-D shows the biased energy diagram. The theory of operation of the PNPN will be discussed in detail in chapter four.

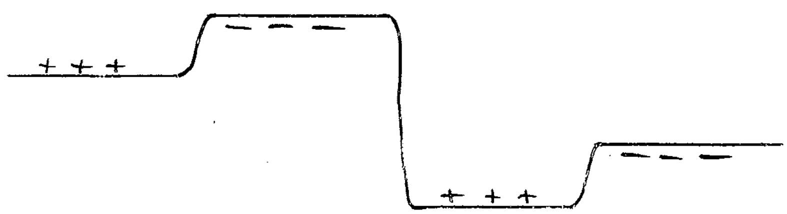


(a) Two Transistor Representation

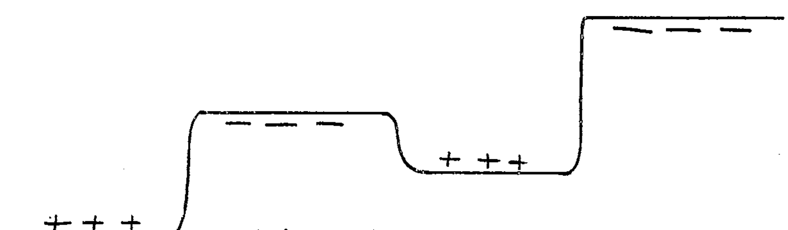


(b) Biased PNPN

(c) Unbiased Energy Level Diagram



(d) Biased Energy Level Diagram



(e) Reversed Bias Energy Level Diagram

Figure 5. The PNPN

CHAPTER IV

THE PNPN

The PNPN can be considered as a combination of a PNP and an NPN transistor. Figure 5-A shows the connections that would be made in this consideration. Figure 5-B is a graphical representation of the PNPN with 5-C being the energy diagram for the unbiased device. As shown in figure 5-B there are three junctions in the device. In the unbiased state there is a potential barrier set up across each junction. The first PN junction (J_1) has a negative to positive potential across it and the NP junction (J_2) a positive to negative. J_3 also has a negative to positive potential across it. These potentials can be observed in figure 5-C.

With the device biased as in figure 5-B the potential barriers across J_1 and J_3 are reduced and the barrier across J_2 is increased, as shown in figure 5-D. The results of bias in this manner are, junctions J_1 and J_3 forward biased and junction J_2 reverse biased. Fore reference, J_1 and J_3 are called emitter junctions and J_2 the collector junctions. The percentage of holes leaving J_1 that reach J_2 is called alpha one and the percentage of electrons leaving J_3 that reach J_2 is alpha two. As the bias is increased across the device the potential barrier to holes is decreased allowing more holes to flow into the alternate N region and on to J_2 and down the potential barrier into the second P region. J_3 is also forward biased which allows free movement of holes across J_3 into the end N region. This increase in holes flow from the first P region increases the value of alpha one and at the same time increases the number of electrons that leave the end N region across J_3 to the middle P region. This increase in electron flow across J_3 increases the number of electrons that are free to fall down the electron potential hill into the interior N region. This increases the value of alpha two and at the same time increases the number of electrons reaching the positive potential at the end of the outside P region. This, in turn, increases the number of holes coming into the P region which means more holes are free to go through the process just completed. This process continues until the device breaks down and conducts freely with very little drop across it. The total current flowing in the circuit is the sum of three currents. (1) The holes leaving J_1 that reach J_2, $(I\alpha_1)$, (2) The electrons leaving J_3 that reach J_2, $(I\alpha_2)$ and (3) The reverse current I_{co}. In equation form this can be written as:

$$I = I\alpha_1 + I\alpha_2 + I_{co}$$

$$\text{or } I - I\alpha_1 - I\alpha_2 = I_{co}$$

$$\text{or } I(1 - \alpha_1 - \alpha_2) = I_{co}$$

$$\therefore I = \frac{I_{co}}{1 - \alpha_1 - \alpha_2}$$

From this equation it can be seen that the current flowing in the external circuit, I, is dependent upon the value of alpha one and alpha two. The reverse current that flows is almost independent of the bias across the unit so the value of the quantity $(\alpha_1 + \alpha_2)$ had control over the firing of the device. As A alpha-one plus alpha-two approaches a value of unity the current through the PNPN increases until at a unit α_t, $(\alpha_1 + \alpha_2)$, the current is limited only by the external circuit. This condition shall be referred to as the on-state of the device.

It is clear now that the value of   is the controlling factor in firing the unit and must be controlled. One obvious method of control would be to determine what value of voltage is necessary across the unit below a certain value, alpha remains fairly constant, however, upon reaching this voltage level the value of alpha increases very rapidly and the PNPN switches from off to on. This value of voltage that causes the device to fire is referred to as V_{bo}, the breakover voltage. A second method of increasing alpha would be to increase the amount of current flowing through some portion of the unit. This is where the connection to the interior P region is used. In addition to the bias already across the PNPN an additional bias can be applied between the interior P region and the end N region (see figure). This reduces the level of the potential barrier across J_3 and while pumping more holes into the P region and more electrons into the N region allows more holes from the P region to cross J_3 into the N region which in turn increases the number of electrons crossing J_3 which increases alpha two and through the process described above increases alpha one. This second method of controlling α_t allows the device to be fired with a lower potential across it than was necessary in the first case. In either case, once the unit fires it stays in the on state until the current falls below some value I_h, the holding current.

To turn the PNPN off after it has one fired requires a great deal more current than was necessary to turn it on. For example a very small current in the gate, (the connection to the interior P region), can turn the device on and start a current thousands of times larger than the gate current flowing in the external circuit. However, this same gate current reversed will not turn the PNPN off. If the current is small enough a negative current pulse on the gate can turn it off. This would be a special case however and can not be considered as a means of turning the device off. The most acceptable method seems to be to remove the voltage that is applied to the element. This constitutes some problems with dc but works very well using ac.

With external bias applied as in figure 5-C the potential barrier across J_1 is very large and the same condition exists at J_3. J_2 has a much smaller potential barrier across it but this has very little effect on the amount of current that flows in the external circuits. The same current equations hold for the element as in the above case but because of the reverse bias condition on J_1 and J_3, alpha one and alpha two are small. Equation (1):

$$I = \frac{I_{co}}{1-\alpha_1-\alpha_2}$$

shows the total current on the external circuit, with alpha one and alpha two small, approaches I_{co}. Therefore in the off state the total current is approximately equal to the reverse current I_{co}.

From the discussion above it appears the PNPN has about the same characteristic as a gas filled thyratron. As such it should make a very good semiconductor device for controlling small motors. The PNPN also exhibits possibilities as a switch or relay and in other ways a pulse circuit element. The use of the element for control of small motors will be considered in chapters five and six.

CHAPTER V

CIRCUIT THEORY

In order to control the speed of small direct current motors there is need for control of armature current. If the PNPN is going to be used in any way for control of speed there must be found some way to control the turning on and off of the semiconductor device. As was stated in chapter four the element can be switched from the off condition to the conducting or on-state with the application of a current pulse to the gate of the device. This switching action only takes place if the PNPN is properly biased, as shown in chapter four. Having the switch in the on position merely allows current flow through the device and through the armature of the dc motor as shown in figure 6. There would be no speed control of the motor and it could only be turned off by opening the armature or

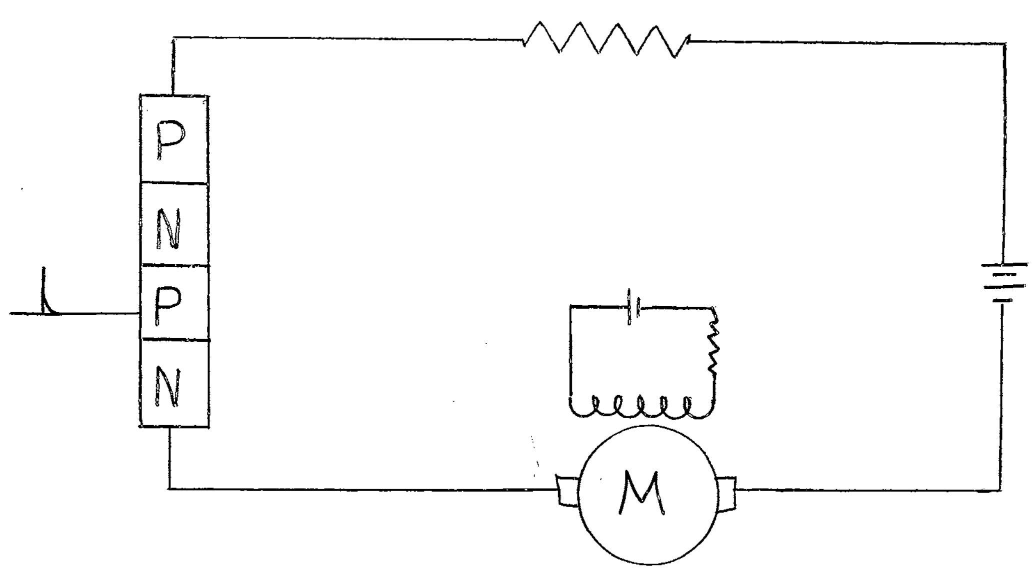


Figure 6. DC Motor Circuit

field circuits. Since the PNPN cannot be turned off effectively with a reverse gate current it serves only as an on switch hence serves no useful purpose. It could well be replaced by an on - off type mechanical switch.

In order to gain some type of gate control of the switch, consider an ac voltage applied instead of the dc in figure 6. Figure 7 represents the connections for the circuit under these circumstances.

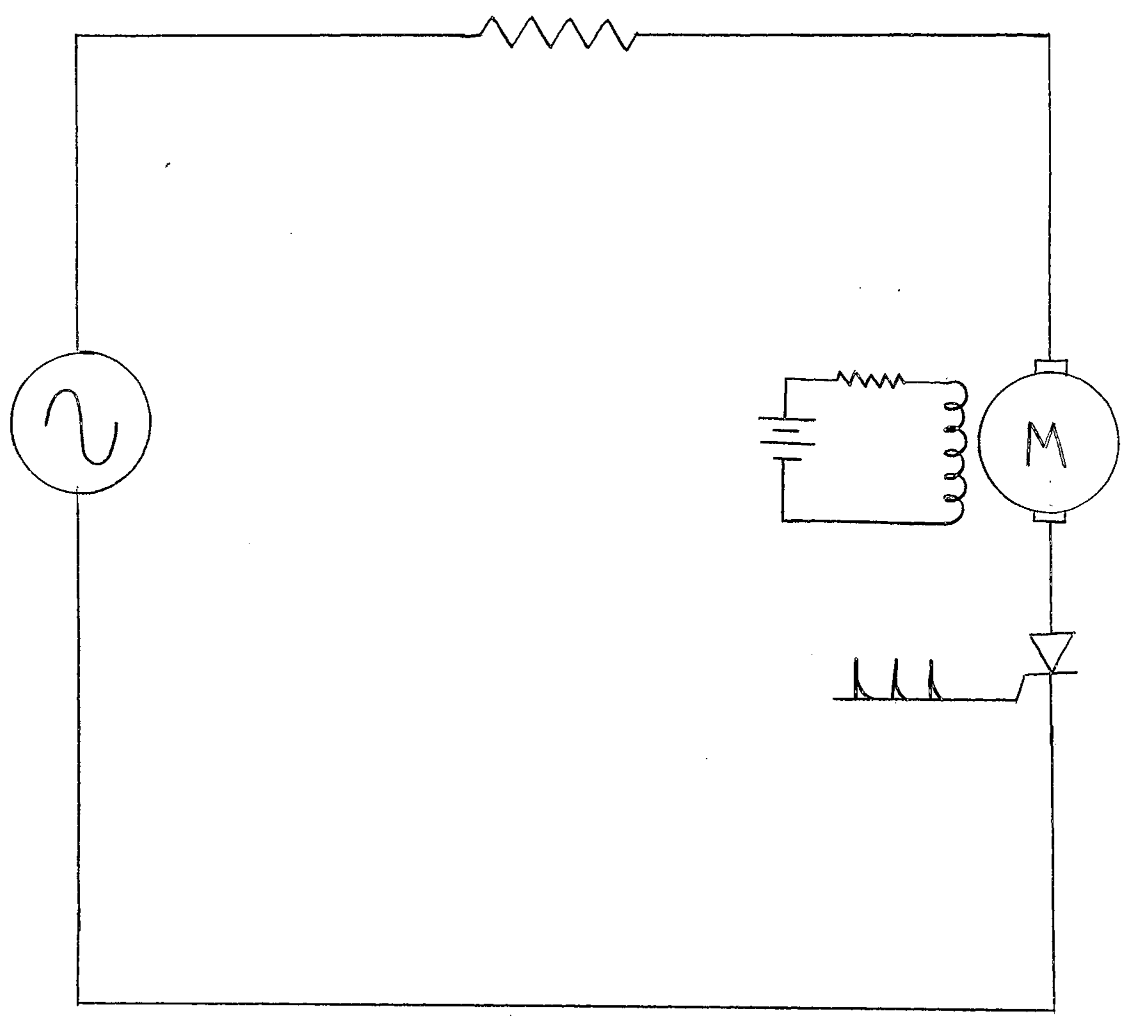


Figure 7. AC Driven DC Motor

The ac would have to be smaller in peak magnitude than the V_{bo} of the unit in the circuit. If it were larger the PNPN would conduct at least half of the positive half of the sine wave and could not be turned off except by opening the armature circuit. However, if the peak voltage of the sine wave is less than the breakover voltage of the PNPN the armature of the motor will have no current through it until the positive current pulse is applied between the gate and outside N region or the emitter. The application of a positive gate pulse while the positive half of the sine wave is on the outside P region, or the collector, will switch the device from the off to the on condition. At the end of the positive half cycle the collector starts going negative with the negative half cycle of the sine wave and the element switches from the on to the off stage. The PNPN will then stay in the no-conducting state until such time that the gate pulse occurs again during the positive half of the sine wave. With a series of current pulses being applied to the gate at intervals such that one occurs on the gate at the same relative time during each positive half cycle, the PNPN will switch on and off each cycle and can be made to stay in the off position by removing the gate current pulses. This circuit then gives a method of controlling the armature current without opening and closing the armature circuit.

With the current pulse applied early in the positive going half cycle the PNPN will conduct the remainder of that half cycle and armature cirrent will flow. Figure 8 is a graphical representation of the voltages and currents in the circuit.

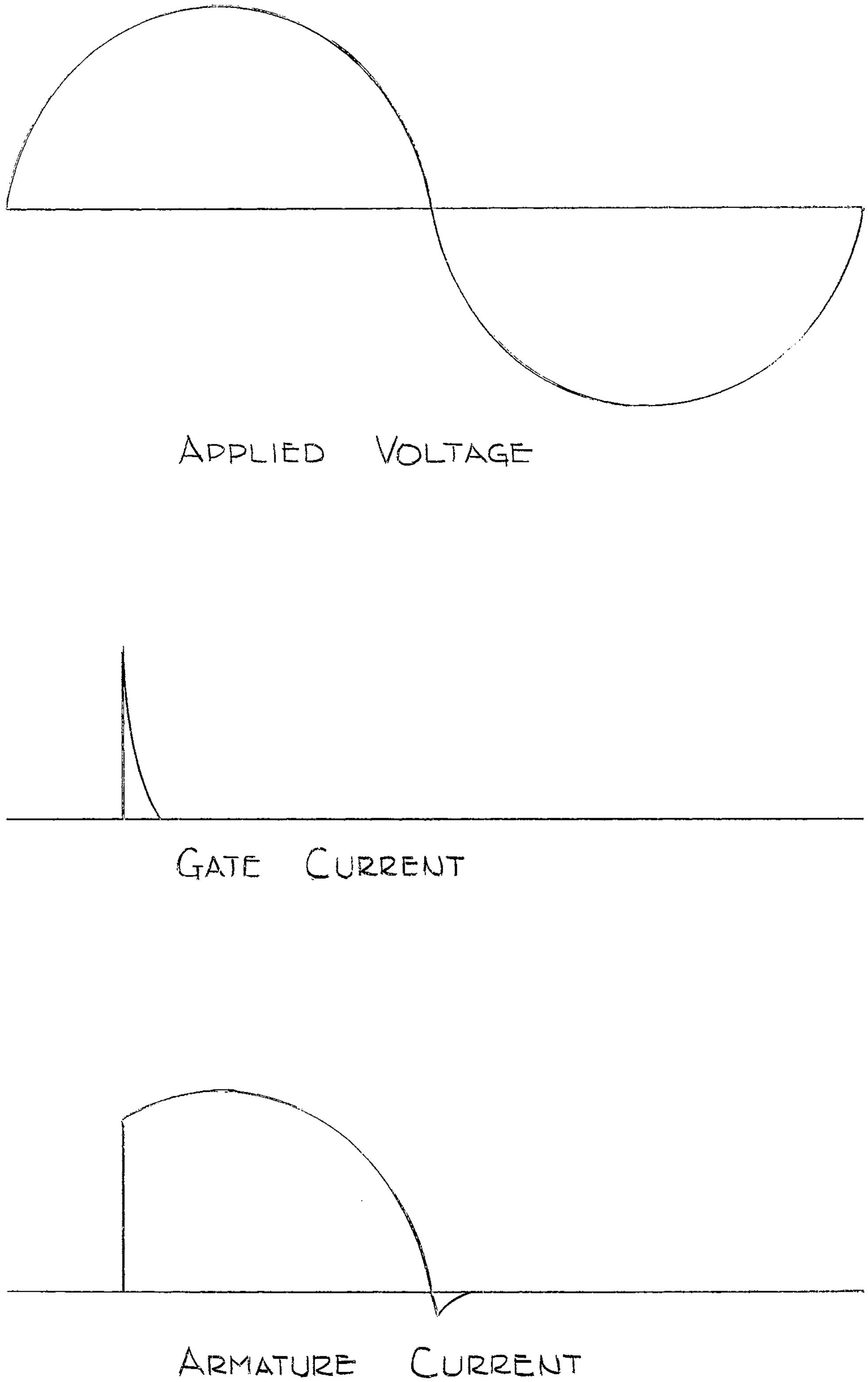


Figure 8. Armature Waveforms

A current pulse of this type can be obtained from a free running pulse circuit of the type pictured in figure 9.

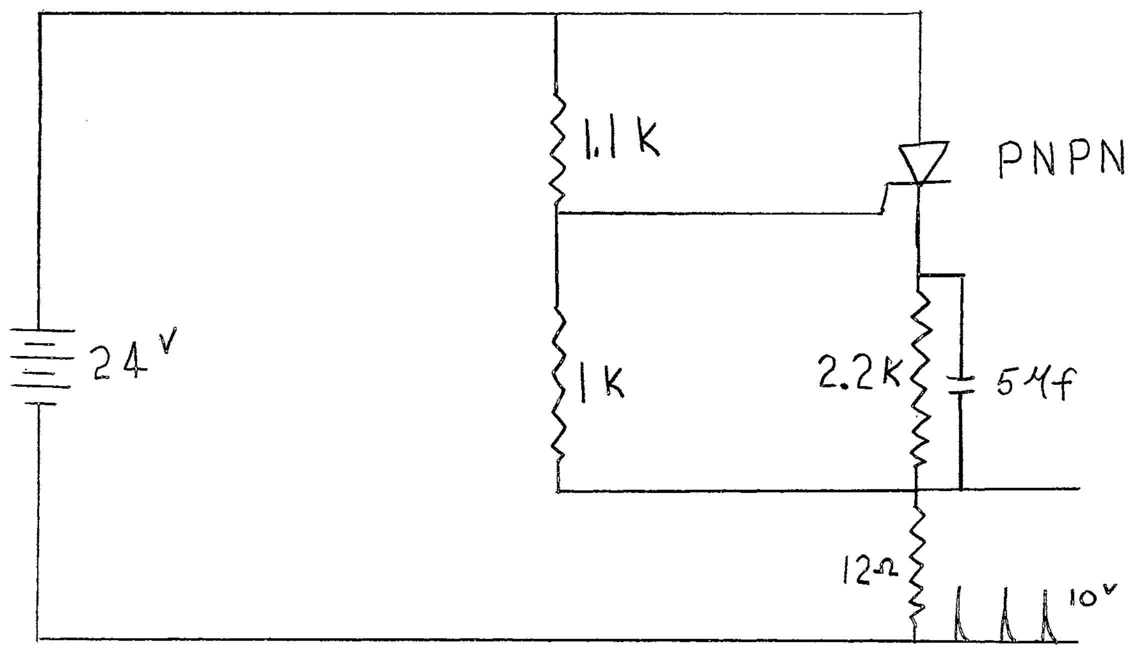


Figure 9. PNPN Pulse Circuit

This circuit was developed in the spring of 1960 at Oklahoma State University by Mr. F. F. Carden, Jr. For a complete analysis of the circuit operation see Mr. Carden's paper on this subject. It will be published during the summer of 1960.

The frequency of the output pulses can be varied by varying the resistance in parallel with the five microfared capacitance. This gives a sixty cycle pulse repetition rate but there is no control over when these pulses will occur with respect to the positive going half of the sine wave across the PNPN. Since the voltage difference between the gate and emitter controls the firing of the PNPN consider what would happen if a sine wave, in phase with the voltage across the unit, were applied across the 1K resistor in figure 9. Because the negative half of this sine wave lowers the voltage difference between gate and emitter the PNPN should never fire during the negative half cycle. The positive half cycle on the otherhand should add to the regular circuit action and cause the PNPN to fire at some time earlier than normal. This should synchronize the output pulses of figure 9 to the positive going half of the applied sine wave. Figure 10 shows the combined circuits.

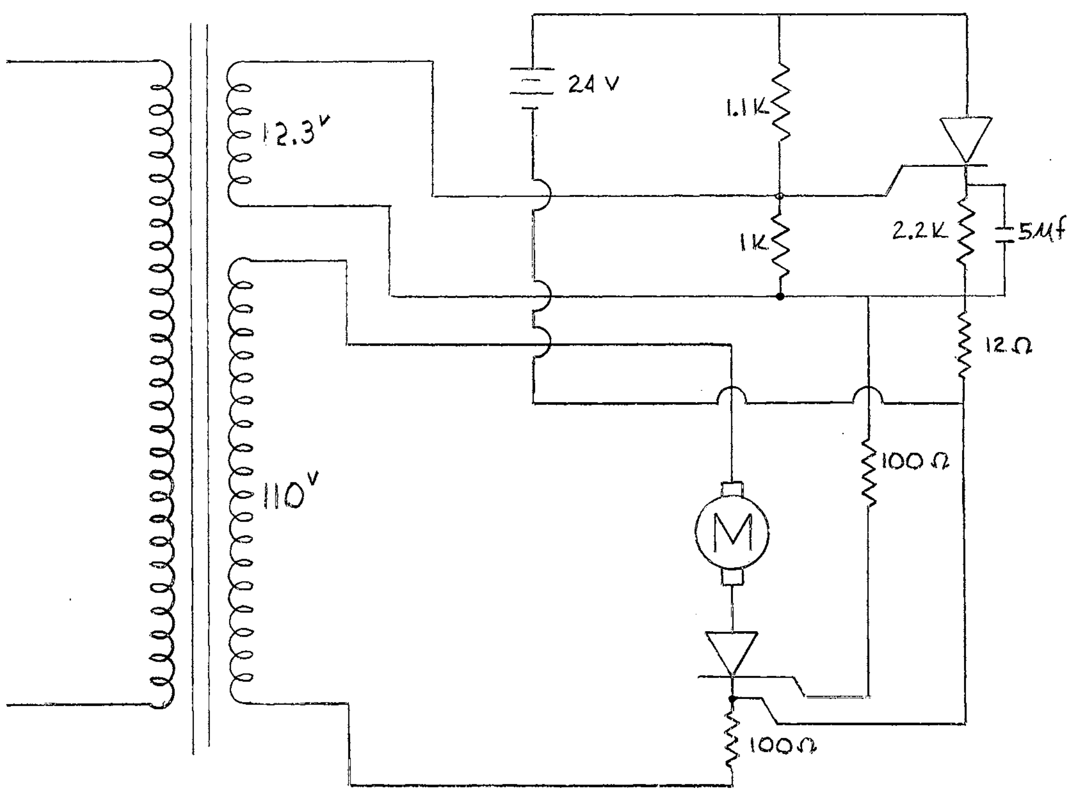


Figure 10. Pulse Triggered Motor Control Circuit

We now have a positive current pulse appearing at the gate of the motor control device early in the positive going half of the voltage sine wave applied to the motor armature circuit. This allows a large portion of the positive half cycle of the sine wave to cause current to flow through the armature. After a few cycles of operation the current through the armature would come to some average value that would yeild a fairly steady dc current. This would give a constant speed to the output shaft. In order to be able to control the speed of the motor the armature current must be varied. One method for varying armature current would be to control the time in the applied sine wave that the PNPN fires. This can be done by controlling the time at whcih the pulse appears on the gate. Figure 11 is a circuit that should control the time the pulse appears.

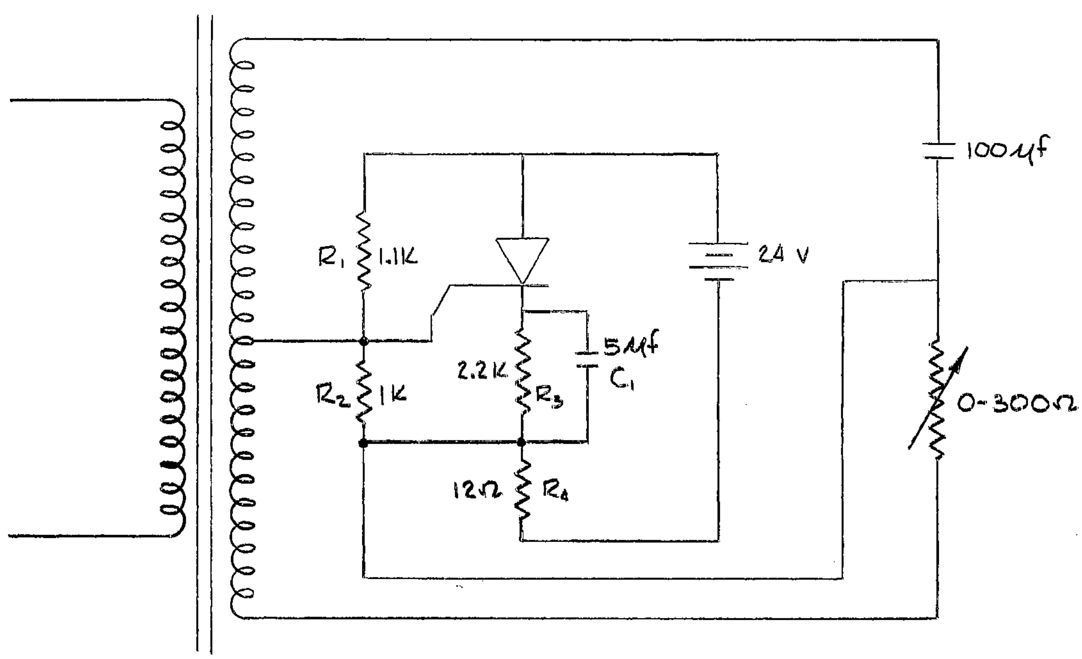


Figure 11. Time Variable Pulse Circuit

The phase shifting bridge will shift the phase of the output sine wave from in phase at R 0 to 180° out of phase at R ∞ with this control over the phase of the sine wave that is applied to the resistor R_2, the output pulses should be controlable over a large portion of the 180° of the positive half of the applied voltage wave. This then would allow control of the firing to vary over this same range. This would yield motor speed control from zero rpm to the maximum speed attainable with the full half wave of current flowing in the armature. Figure 12 is the complete circuit.

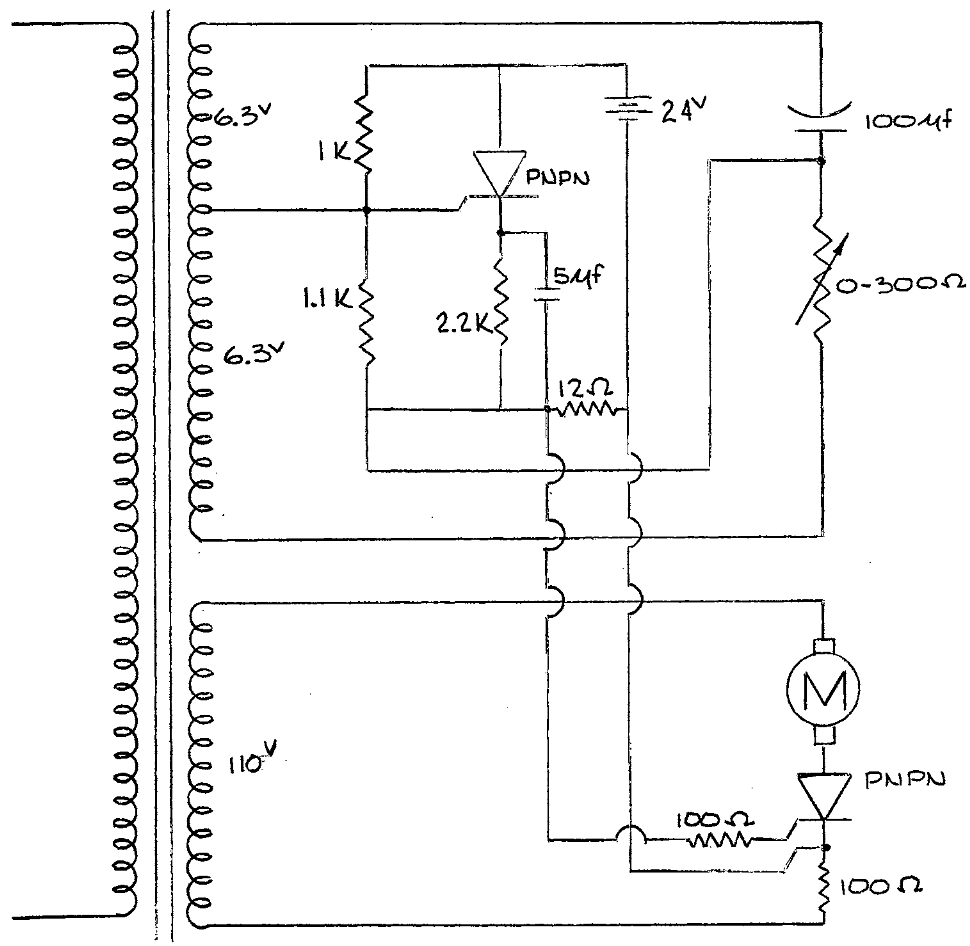


Figure 12. Time Variable Pulse Triggered Motor Control Circuit

It is apparent that the average value current through the armature is going to be small because of only half wave ac flowing through the armature circuit. If some method could be devised that would allow full wave rectified ac to flow through the armature the average value of current would be increased and much smoother motor operation would result.

The PNPN passes current only when it has the proper voltages applied and can never conduct when the negative half of the sine wave is on the anode. It is clear then that at least two units must be used to allow a full wave rectified ac to flow through the armature. Figure 13 shows one way these units may be arranged.

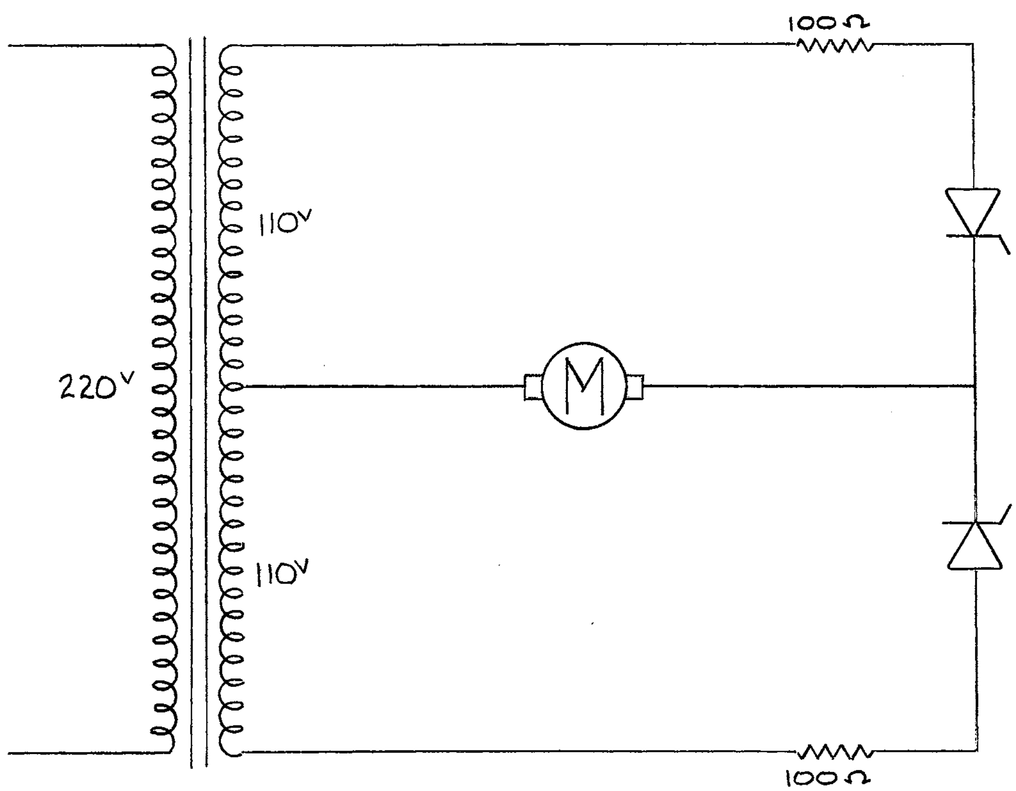


Figure 13. Full Wave Armature Circuit

Here again the breakover voltage of the PNPN's must be less than the positive peak of the applied ac. When one anode or collector is positive going the other is negative going so they cannot fire at the same time. The problem now is to get the positive pulses to the respective gates at the proper time. Since one PNPN cannot fire while the other is conducting regardless of the signal on the gate it would be all right to put a positive pulse on each gate each half cycle. This would fire unit one when its collector is going positive and unit two would be restrained from firing because of its negative going collector even though there would be a positive pulse on its gate. The next half cycle unit two would fire and unit one would be held off. Again this pulse must be variable in time over 180° of the 60 cycle sine wave. One circuit that should produce such a variable pulse is shown below.

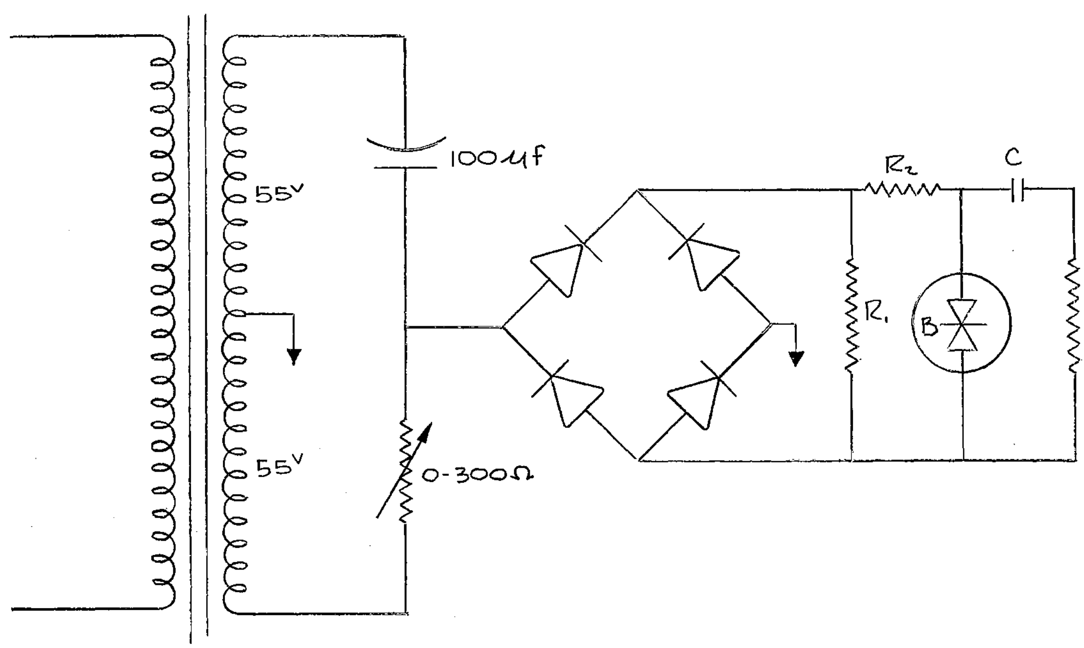


Figure 14. R-C Pulse Circuit

The phase shifting bridge is the same as before with its output going into a diode bridge. The output of the diode bridge would be a rectified sine wave which would be dropped some in magnitude before being applied to a diode clipper. This device acts as a short circuit, until the voltage across it builds up to around fifteen volts, then opens. The output from the diode clipper is a fifteen volt peak square wave which is differentiated to obtain the output wave form shown. If it were necessary the negative going pulses could be clipped leaving only the 120 pulse per second positive pulse train. However, the negative going pulse just accentuates the turning off of the unit that was firing before the next positive pulse occurs. Both circuits are combined in figure 15.

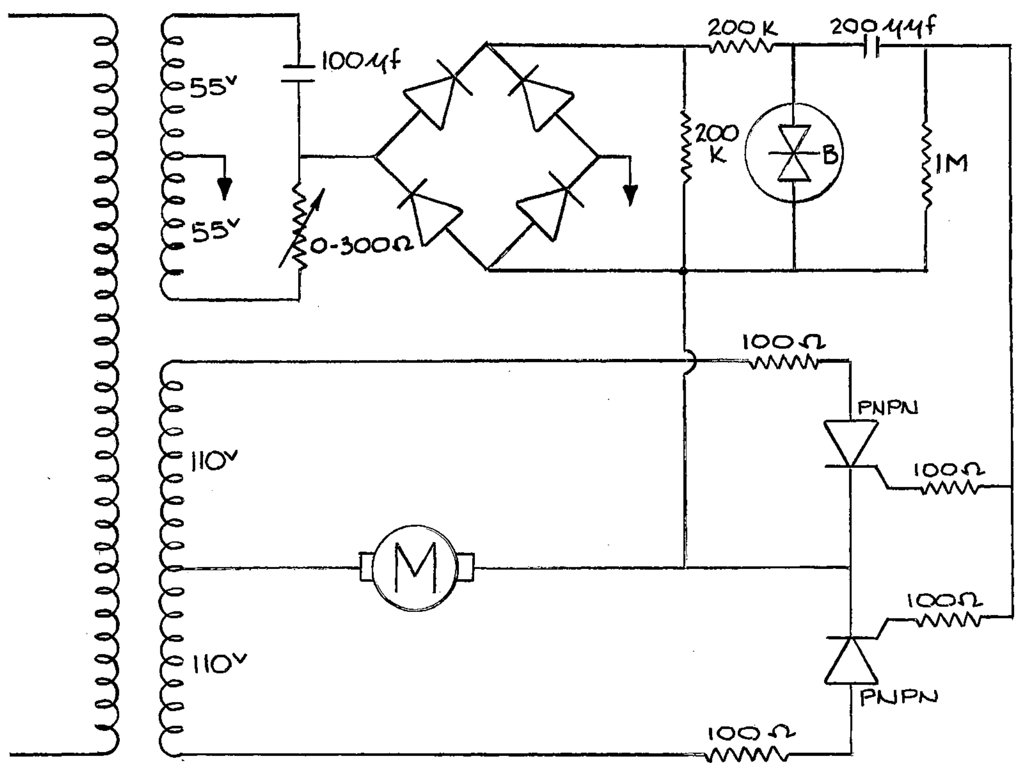


Figure 15. R-C Pulsed Full Wave Circuit

A second circuit for producing a positive pulse at 120 pulses per second is shown in figure 16. This circuit is a combination of the circuits of figures 9 and 14.

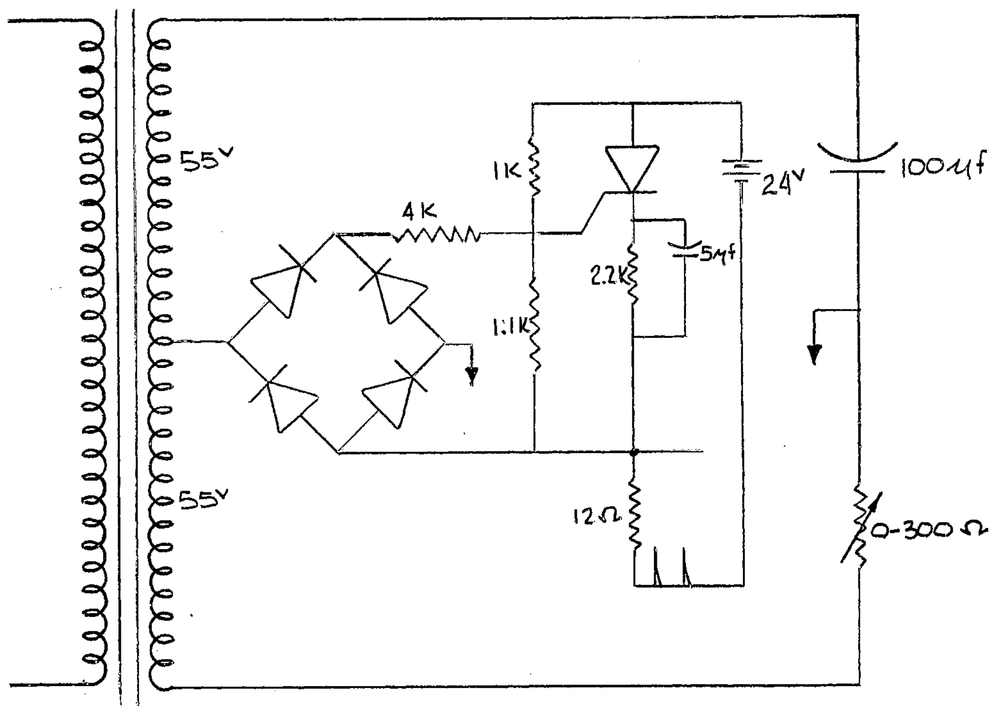


Figure 16. PNPN Pulse Circuit

As before the phase shifting bridge controls the phase of the sine wave that is applied to the diode bridge. The output of the diode bridge is applied through a dropping resistor to the resistor R_2. As before the positive going half sine wave controls the time that the circuit allows the PNPN to fire. Now, however, there is no negative going half sine wave, instead there is another positive going wave. This should result in an output pulse for each half wave and since the phase of the original sine wave can be shifted over 180° the time of the output pulses can be controlled with respect to the voltage applied to the armature circuit. The combination of figures 16 and 13 yeilds figure 17. This should be a useable circuit for controlling the speed of a dc motor.

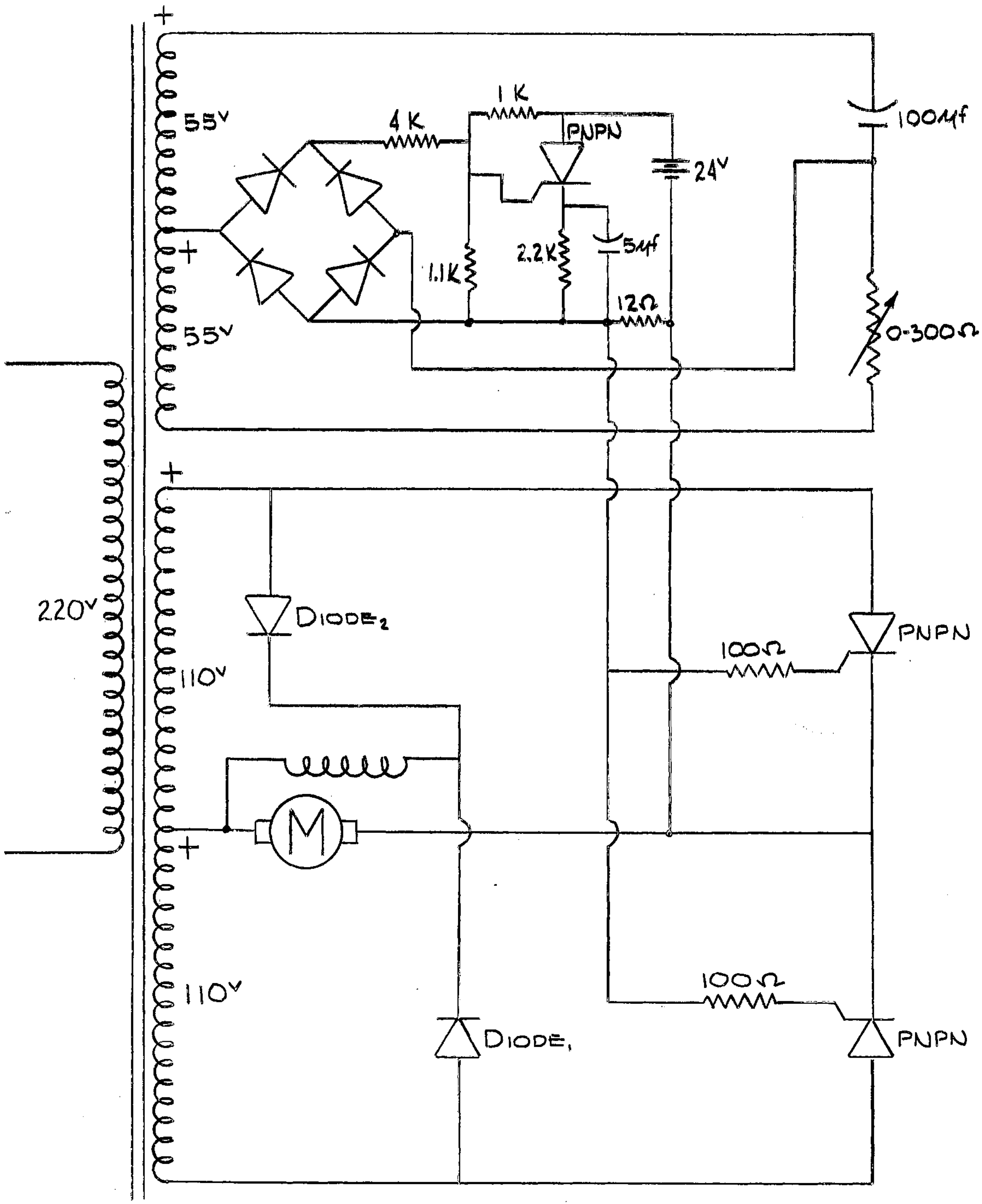


Figure 17. Completed Circuit

The addition of the diodes and the field circuit in the ac circuit makes it possible to get full wave rectified ac flowing in the field winding. This givea a constant value of dc for field exicitation. The circuits discussed in this chapter were designed and used in the development of the final circuit presented in figure 17. The parts of the circuits that were used in the final circuit will be considered in the following chapter. Design consideration for the final circuit and results of the experimental circuit will be presented.

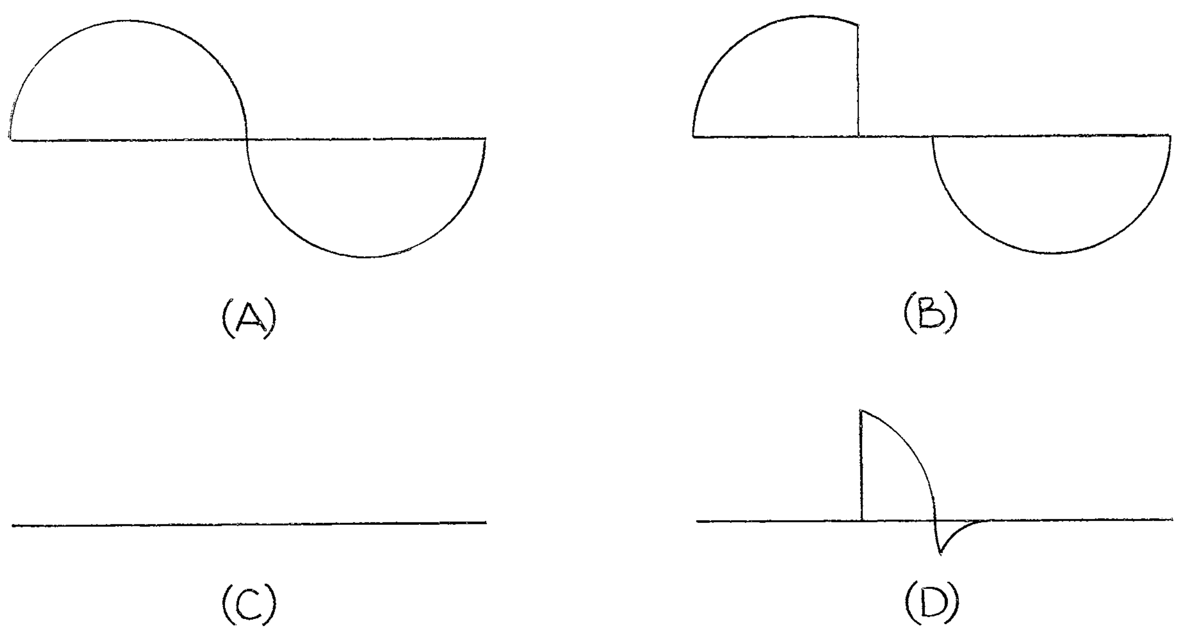
CHAPTER VI

CIRCUIT DESIGN AND RESULTS

The pulse circuit in figure 9 was used as designed by Mr. Carden. The only addition being the application of the sine wave for synchronization. The PNPN used in this circuit was a TI131 with a breakover voltage of 150 volts. This type unit has a gate current limit of 100 milliamps. For this reason the sine wave applied to R_2 was held to a peak voltage of 15 volts. This was accomplished by supplying the phase shifting bridge from the 12.5 volts secondary winding of the transformer. From the center tap of the transformer to the connection between the R and C of the bridge the voltage is a 6.25 volt sine wave that can be shifted in phase with respect to the input. This bridge yeilds a constant voltage output regardless of the value of the resistor. As much phase shift as possible is desired out of the bridge. The maximum possible shift is 180^o, but to obtain this the resistance must be variable from zero ohms to open circuit. Where the impedance of the capacitor is equal to the impedance of the resistance the phase shift is 90^o. A 100 microfared capacitor was used and at 60 cycle its impedance was 26.5 ohms. It was found that a resistor that varied from zero to 10 x_c would give about 160^o of controllable phase shift from 10^o to 170^o out of phase. When this sine wave was applied to R_2 of the pulse circuit the output of that circuit was a 10 volt peak pulse. The pulse had a rise time of .5 microseconds and was 2 microseconds wide at the ten percent points. This pulse was to be used to trigger the PNPN in the motor control circuit figure 5-7. This unit was a type TI132 with a breakover voltage of over 200 volts. Again the gate current for this unit was to be no more than 100 milliamps. The 10 volt pulse was then fed to the gate through a resistor that would limit the current peak to 100 milliamps.

The voltage fed to the armature circuit in figure 12 was 115 volts ac. This gives a peak voltage of 150 volts which was at least 50 volts below the breakover voltage of the unit involved.

A phase meter was used to check the phase of the sine wave out of the phase shifting bridge. It worked as predicted and was 170° out of phase with the voltage across the armature circuit when the power was applied. Figure 18-A represents the voltage across the PNPN at this setting and then 18-B with the value of R reduced slightly. 18-C and 18-D represent the voltage across the armature circuit for the respective PNPN voltage.



(A) (B) (C) (D)

Figure 18. Armature And PNPN Voltages

Varying the value of R in the phase shift bridge all the way down to zero shifted the speed of the motor from stopped to rated rpm.

The action of this circuit was not entirely satisfactory. The motor ran a little rough and heated up rather fast due to only half wave current flowing in the armature. Because of the unsatisfactory operation of this circuit the action of the motor was not investigated. Instead the circuit of figure 15 was investigated.

In this case a 110 volt center tapped secondary was used with the same resistor and capacitor as before to give a 55 volt sine wave that could be shifted in phase. Using the phase meter, the phase was again found to be variable from 10° to 170° out of phase. This time the output of the phase shifting bridge was fed to the diode bridge which was made up of four type 1N2069 diodes. The output was taken across a 200 K resistor and fed through another 200 K to the diode clipper. The diode clipper action gave a 15 volt square wave output with a one millisecond rise time and 8 milliseconds wide. The rise time left something to be desired but could have been useable if there had been no other difficulty. It was found almost impossible to come up with a differentiating circuit that would give a useable pulse output that would remain useable when the circuit was coupled into the PNPN. When the gate of the PNPN goes positive with respect to the emitter the junction allows conduction and the resistor in the differentiating circuit is practically short circuited.

The need for a pulse generator whose output was independent of the input of the next stage led back to the pulse circuit used in figure
The output of the diode bridge, a 75 volt peak rectified sine wave, was taken across the resistor R_2 in the pulse circuit. The total output was dropped across 5K since the peak to be applied to the gate was to be 15 volts or less and R_2 was 1K. The voltage divider equation gave a 4K value

to the second R needed.

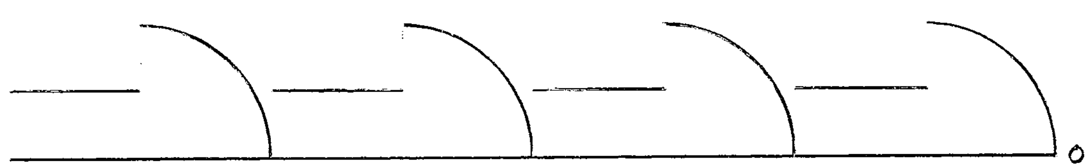
$$\frac{R_2 \cdot 75}{R_d + R_2} = 15^V$$

$$15 R_d = 1000(75-15)$$

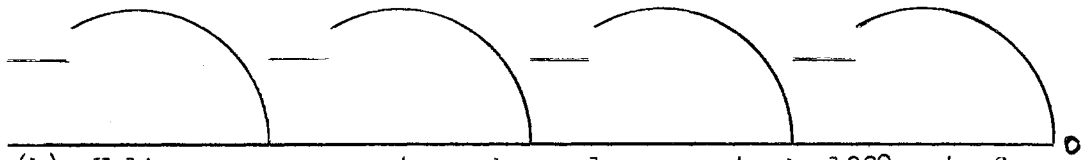
$$R_d = 1000\left(\frac{75-15}{15}\right) = 4000\,\Omega$$

This 15 volt peak rectified ac across R_2 caused the pulse circuit to fire at the same time each half cycle and to yeild an output pulse of 10 volts peak with the same dimensions as before. Again this pulse was fed through 100 ohm resistors to the gates of the PNPN's. As in the first circuit the PNPN's were TI132 type semiconductors with breakover voltages in excess of 200 volts. The diodes used for the field supply are type 1N1096. The circuit was connected as shown in figure 17 and was found superior in every way to the half wave type of control circuit discussed above. The motor operation was smooth over the entire range of operation and heating was a great deal less than in the previous case.

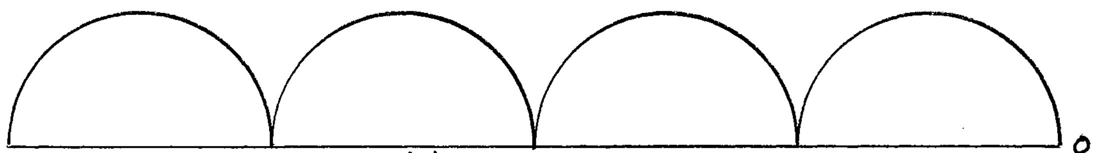
The voltages across the motor armature and field were observed as shown below. A discussion of the armature voltage wave shape can be found in Engineering Electronics by John D. Ryder.



(a) Voltage across armature when pulse on gate is 100° out of phase with the applied voltage wave.



(b) Voltage across armature when pulse on gate is 130° out of phase with the applied voltage wave.



(c) Field Voltage

Figure 19. Armature Voltage Wave Forms

The current through the armature will have some harmonic content and therefore I_{rms} will be greater than I_{dc}. This means that for a given average torque whcih will be proportional to I_{dc}, a motor will run better when supplied by this circuit than when operated from a dc line. This is the reason for the heating in the motor and causes the need for derating dc motors in controlled rectifier service. Although this paper is not directly concerned with the armature and field currents it must be noted that the PNPN devices used to control the current have a capacity of 3 amperes. This then would limit the armature current to something less than 6 amperes. The diodes controlling the field current have a maximum capacity of 2.5 amperes at 25°C, therefore limiting the field current to 5 amperes. The figures given above are for temperatures up to 75° C and must be derated as temperature rises. For example the forward current limit at 125°C for the PNPN's used is 1 ampere. This would automatically set a limit to the size of motor to be controlled that would vary inverseley with temperature.

CHAPTER VII

SUMMARY

This circuit works very well with the manually controlled phase shifting circuit and could be made automatic by having some type of mechanical control of the potentiometer in that circuit. Another possibility for automatic control would be to place a dc control signal level between gate and emitter of the PNPN to control the time the unit fires on the sine wave that is applied. The circuit could be made to work entirely from ac power by converting the rectified ac from the bridge to a 24 volt dc for application to the pulse circuit. This circuit is not limited to 60 cycle since the pulse circuit will synchronize with any power frequency above its resonant frequency. Frequencies up to 400 cycles were investigated and found to synchronize the pulse circuit at whatever frequency was being checked. With the exception of the current limitation noted previously this circuit is temperature independent from room temperatures to 150° C. A further improvement in this circuit would be some method for reversing direction of current flow through the armature. This would involve a circuit to control phase over 360° and some different method of arranging the PNPN's in the armature circuit.

This solid state device circuit has some advantages over an equivalent electron tube circuit. Besides the obvious savings in size and weight there is also a considerable increase in life expectancy of the semiconductor over the vacuum tube. Also involved in some cases is the faster switching time of the PNPN over the gas tube. At present the cost of the semiconductor devices may be higher than the electron tubes they replace but this cost differential will be reduced and eventually reversed with imprpved manufacturing techniques.

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