

THE SILICON CONTROLLED RECTIFIER
LOGIC BLOCK

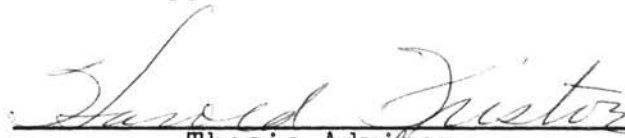
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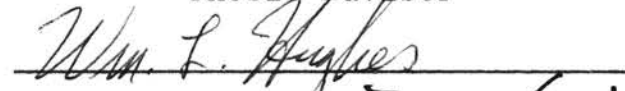
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PREFACE

The rapidly increasing number of applications of logic circuits makes the silicon controlled rectifier logic block of particular interest at this time. This study has provided for me, as I hope it will for the reader, an insight into the principles of logic blocks and the nonlinear circuit elements of which they are constructed.

This investigation was sponsored by Texas Instruments, Incorporated, and I wish to thank them for their generous financial assistance by way of the fellowship I received as well as the technical help of their engineering staff. The encouragement and help of my adviser, Dr. H. T. Fristoe, during this study as well as in the classroom has been indeed valuable. I would also like to thank Dr. W. L. Hughes who helped in the final preparation of this paper.

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CHAPTER I

INTRODUCTION

It has been said that the silicon controlled rectifier introduced the renaissance of the control era. Certainly this device has many applications in the control of large amounts of electrical power. Its small size and giant power handling capability have eliminated the bulky rotating machinery necessary to supply power to d.c. motors and the large reostats used for light dimmers. Position and speed control systems using the efficient silicon controlled rectifier are presently under development. This solid state device is also used in many situations where electromagnetic relays were previously used.

As the silicon controlled rectifier is well suited to control large electrical loads, perhaps it is reasonable to investigate methods of utilizing this device in equipment exercising control on a smaller scale. Logic circuits are examples of such equipment. However, other more compelling reasons suggest the application of the silicon controlled rectifier to logic circuitry. It has several prominent characteristics that are similar to other electronic devices (e.g., the transistor, thyatron, and solid state rectifier) used in switching or logic circuits. These similarities

will be pointed out at the appropriate time.

The general purpose of the project reported in this thesis is to study applications of the silicon controlled rectifier to logic or switching circuits. Two specific objectives were outlined in the early stages of the study. These are: 1. Develop and study the feasibility of binary logic blocks using the silicon controlled rectifier. 2. Optimize the design of the logic circuits for speed, temperature stability, and component tolerance. It will be pointed out in the body of the thesis below that the inherent characteristics of the silicon controlled rectifier, as well as certain restrictions placed on the electrical parameters of the units presently available, have severely limited the practicability of this type of logic block. These limitations have forced the consideration of a new switching circuit, the alternate mode logic circuit.

The presentation of material in this thesis is in much the same sequence as the various stages of the study. First, logic circuits are discussed with emphasis on the electrical requirements of the NOR logic block. A description of switching circuits previously developed is included here. The second topic is a study of the characteristics of the silicon controlled rectifier. With this background the third step is to explore various logic circuit arrangements suggested by work done in the past. These we shall call direct mode logic blocks. It soon became obvious that conventional logic circuitry would not easily adapt to the

silicon controlled rectifier, and the fourth phase of the program was initiated. Thus the fourth section of the thesis describes and discusses the alternate mode logic circuit. In the conclusion of this thesis a general evaluation is made of the feasibility of using the silicon controlled rectifier in logic circuits.

CHAPTER II

LOGIC CIRCUITS

Logic circuits are becoming increasingly important in all areas of electronics. One well known application is the general purpose electronic computer. Large machines may also be controlled by logic circuits.

Consider the following hypothetical application of a simple logic circuit. It is necessary to provide a safety control for the firing of a rocket carrying a man into space. The safety control must not allow the rocket to fire until the astronaut is ready nor while the fuel pumps are pumping fuel into the storage tanks on the rocket. When the astronaut is ready and the fuel tanks are full, the project director presses a button and the motors start. A logic circuit using three electromagnetic relays could easily provide the necessary control. In the diagram shown below the contacts of the relays are connected in series, and when all contacts are closed the rocket motors fire. A switch indicating the astronaut is ready closes the contacts of relay number 1. When the fuel pump is turned off, the coil of relay number 2 is de-energized and its contacts close. Note here that the absence of an electrical signal provides the necessary switching function. The third relay

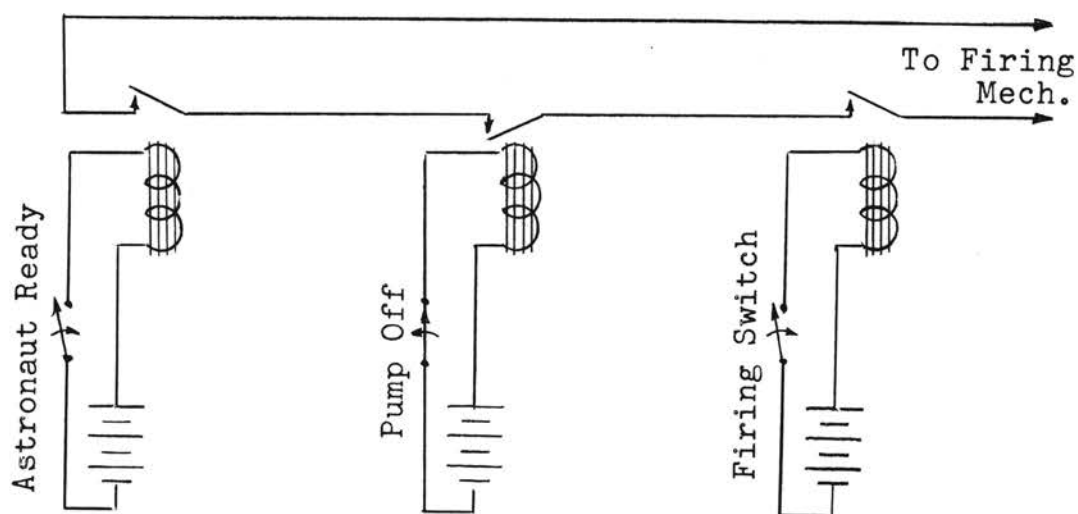


Fig. 1 Rocket Safety Control

is controlled by a button on the project director's instrument panel and is pressed to fire the rocket.

The circuit has performed the function described by the following sentence. The rocket motor fires when the astronaut is ready and the fuel pump motors are not running and the project director gives the signal. This electric circuit may be called a logic circuit. We define a logic circuit as an electrical connection of elementary systems arranged to provide an output signal when the necessary signals (more properly stated, valid information) are present at the input.

Boolean Algebra

George Boole, in 1854, introduced an algebra of logic that expresses the relation between the required validity of the input information and the output.¹ As an example of Boolean algebra let us again consider the rocket safety control. Let A indicate the astronaut is ready and \bar{A} indicate he is not ready. In the same manner P will indicate the fuel pumps are on while \bar{P} will indicate off. If the project director's firing switch is open, we will say he is not ready and indicate this by \bar{D} ; D will indicate the firing switch has been closed. At the time the logic sentence stated above becomes valid, we want the control circuit to produce an output to fire the rocket, symbolized by F . In Boolean algebra notation we write:

$$F = A \times \bar{P} \times D \qquad \text{Eq. 1}$$

The rocket motor fires	<u>when</u>	the astronaut is ready	<u>and</u>	the fuel pump is not on	<u>and</u>	the direct- or presses the button.
------------------------------	-------------	------------------------------	------------	-------------------------------	------------	--

Note that when \times is interpreted as the connective, AND, the Boolean algebra expression corresponds to the logic sentence written below it. This algebraic expression is to the engineer a wiring formula that fixes the connection between the elementary switching circuits or logic blocks necessary to form the output signal.

¹George Boole, The Laws of Thought (Chicago, 1940), p. 24.

A complete or highly rigorous discussion of Boolean algebra will not be presented here. However, certain basic principles are necessary for an understanding of the application of the logic block. We will see how one function, the NOR function, can perform all of the Boolean operations. The importance of this fact is that the silicon controlled rectifier can be adapted to perform the NOR function.

The algebra of logic is said to have been developed by philosophers in the nineteenth century who were attempting to reduce logic to a mathematical science.² As the philosopher attempts to reduce every situation to true or false, the Boolean algebra is the algebra of variables having only two values. Note that in the hypothetical situation presented previously the astronaut was either ready or not ready; the fuel pumps were either on or off. Similarly logic circuits utilize only double valued variables. A relay contact, for example, is either open or closed, and a voltage is at either an up or a down level. Since there are only two integers in the base two number system, logic circuits may be used to handle numbers greater than two expressed in the base two number system. Using one of a number of similar binary schemes, an electronic computer can handle algebraic functions of a multiple valued variable as well as

²Rene A. Higonnet and Rene A. Grea, Logical Design of Electrical Circuits (New York, 1958), p.8.

very large numbers.³

We will represent the two distinct values of the variable A by A and \bar{A} . We have seen that A can indicate the astronaut is ready, while \bar{A} can indicate he is unready. Such a variable might represent any other double valued condition. Often in the literature a portion of the area of a square represents all statements of a particular kind. This representation is called a Venn diagram.⁴ As this interpretation lends itself to the illustration of the principles of the Boolean algebra, we shall consider several examples.

The first square below represents the set of all statements under consideration and is called the universal set or referential. Let us consider the statements of a particular kind A represented by the shaded area in Fig. 2. The other value of the variable A is the unshaded area indicated by \bar{A} , called NOT A or the complement of A ; it represents all statements different from A . The selection of a second group of statements B , having a common property indicated by the dotted area in Fig. 3, does not in any way change the areas previously called A and \bar{A} . Note that the variable B also has two values B and \bar{B} in the universal set.

³R. K. Richards, Arithmetic Operations in Digital Computers (New York, 1958), p. 177 ff.

⁴Ivan Flores, Computer Logic (Englewood Cliffs, 1960), p. 132.

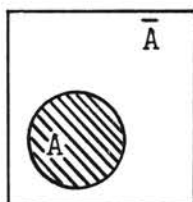


Fig. 2
Diagram of
 A and \bar{A}

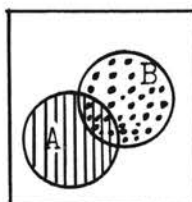


Fig. 3
Diagram of
 A and B

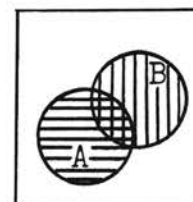


Fig. 4
Diagram of
 $A + B$ and $A \times B$

We may now illustrate the Boolean operations $+$ and \times . These symbols should not be confused with their arithmetic counterparts, as they are not exactly parallel. The function $A + B$ is called the logical sum and is interpreted to include all statements of type A OR B , represented by the entire shaded area in Fig. 4. It may be said that statements of either type A OR type B lie in the set of statements $A + B$. The $+$ operation is called the OR operation.

The function $A \times B$ is called a logical product and in this case includes all statements that qualify to be of type A AND B . This is represented geometrically in Fig. 4 as the dark shaded area. Since this function included statements of type A AND B , the \times operation is called the AND operation.

The following theorems are proved in several places.⁵

⁵Montgomery Phister, Logical Design of Digital Computers (New York, 1959), pp. 31-45.

We shall state the more important theorems of Boolean algebra and illustrate them by using the Venn diagram. The two operations logical sum and logical product were illustrated with two variables. The same operations on one variable give the following results:

$$\text{Theorem I} \quad A + A = A$$

$$\text{Theorem II} \quad A \times A = A$$

The first statement may be illustrated by saying that the logical sum of the set of statements of type A OR the set of statements of type A is a set of statements containing type A only. Similarly, the second statement is interpreted as a logical product of the set of statements of type A AND the set of statements of type A , which is a set containing all of the statements of type A . Another important theorem dealing with only one variable states that:

$$\text{Theorem III} \quad (\overline{\overline{A}}) = A$$

This theorem may be readily verified by observing that in Fig. 2 all of the statements that are NOT of the type NOT A are of the type A .

An important theorem dealing with two variables states that:

$$\text{Theorem IV} \quad A + (A \times B) = A$$

Fig. 5 illustrates the fact that the set of statements of

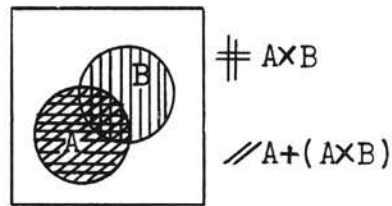


Fig. 5 Diagram of
 $A + (A \times B)$

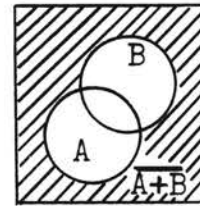


Fig. 6
Diagram of
Theorem V

type A AND B joined by a logical sum with statements of type A is the set A .

DeMorgan's theorem is the following function involving two variables:

$$\text{Theorem V} \quad \overline{A + B} = \bar{A} \times \bar{B}$$

Note that the area representing statements NOT of type A OR B in Fig. 6 is identical to the area designated by the logical product of statements \bar{A} AND \bar{B} . This theorem is an illustration of a general rule for any number of variables, which states that the complement of a function is equal to a function obtained by changing all + signs to \times , all \times signs to + , and replacing each variable in the original function by its complement. For example:

$$\overline{A + B \times C} = \bar{A} \times \bar{B} + C \quad \text{Eq. 2}$$

To illustrate a Boolean function let us again consider the safety control circuit for the rocket. Recall that the

functional equation is:

$$A \times \bar{P} \times D = F \quad \text{Eq. 1}$$

Since each of the statements corresponding to a variable can be true or false, let us represent a true statement by a 1 and a false statement by a 0 . The following table contains all of the possible combinations of true and false statements.

TABLE I
TRUTH TABLE FOR EQUATION 1

A	P	D	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Note that when P is false, \bar{P} must be true since P AND \bar{P} contain all valid statements. Thus when A and D are true and P is false, the Boolean function F is true. Table I above is often called the truth table of the function because it indicates the true and false statements necessary to make the function true.

There are sixteen possible functions of two variables.⁶

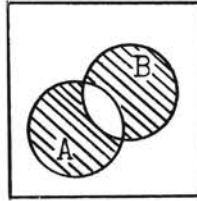


Fig. 7 Diagram of the Exclusive OR Function

The AND function $A \times B$ and the OR function $A + B$ were previously illustrated. Of those remaining three are of particular importance. The exclusive OR function $(A \times \bar{B}) + (\bar{A} \times B)$ is illustrated by the shaded area in Fig. 7. This function differs from the OR function since it excludes all statements of type A AND B . The exclusive OR is the Boolean function representing the binary addition of two numbers which we will demonstrate in Chapter 5. The Peirce function is the expression $\bar{A} \times \bar{B}$ and is sometimes represented by $A \downarrow B$ (read A peirce B .)⁷ Applying DeMorgan's theorem we may write:

$$\bar{A} \times \bar{B} = \overline{A + B}, \quad \text{Eq. 3}$$

which is read NOT, A OR B . The common practice in engineering is to call this important function a NOR function.⁸

⁶Ibid., p. 53.

⁷after C. S. Peirce, an American logician.

⁸A corresponding NAND function is occasionally referred to by engineers. It is more properly called the Sheffer stroke function, $\bar{A} + \bar{B} = A \mid B$ (read A stroke B .)

A primary feature of this function is the fact that the other logical operations can be performed by the NOR function. For example, the variable A peirced with itself yields the complement \bar{A} .

$$A \downarrow A = \bar{A} \times \bar{A} = \overline{A + A} = \bar{A} \quad \text{Eq. 4}$$

The AND function is obtained by applying Theorem III in the following manner:

$$\begin{aligned} A \times B &= \bar{\bar{A}} \times \bar{\bar{B}} = \overline{\bar{A} + \bar{B}} = \bar{A} \downarrow \bar{B} \\ &= (A \downarrow A) \downarrow (B \downarrow B) \end{aligned} \quad \text{Eq. 5}$$

The OR operation can also be performed exclusively by the NOR function:

$$A + B = \overline{\bar{A} \times \bar{B}} = \overline{\bar{A} \downarrow \bar{B}} = (A \downarrow B) \downarrow (A \downarrow B) \quad \text{Eq. 6}$$

Now apply the principles listed above to the rocket safety circuit function:

$$\begin{aligned} F &= A \times \bar{P} \times D = (A \times D) \times \bar{P} \\ &= [(A \downarrow A) \downarrow (B \downarrow B)] \times \bar{P} \\ &= [(A \downarrow A) \downarrow (B \downarrow B)] \times [P \downarrow P] \\ &= \left\{ [(A \downarrow A) \downarrow (B \downarrow B)] \downarrow [(A \downarrow A) \downarrow (B \downarrow B)] \right\} \\ &\quad \downarrow \left\{ [P \downarrow P] \downarrow [P \downarrow P] \right\} \end{aligned} \quad \text{Eq. 7}$$

Mathematically this expression is very complicated. We re-

call that the complement of a variable is given by the NOR operation on the variable. Using this fact we may substitute above and have:

$$F = \{[\overline{A} \downarrow \overline{B}]\} \downarrow \{\overline{P}\} = \{[\overline{A} \downarrow \overline{B}]\} \downarrow \{P\} , \quad \text{Eq. 8}$$

which is a much simpler function and is suitable for a logic circuit design using NOR logic blocks.

The NOR function is easily performed by logic circuits using transistor or vacuum tubes. The property of the NOR function that allows it to perform all of the other operations is valuable to the logic circuit designer. With a NOR block he can form any logic circuit. It is with good reason, then, that the NOR logic block is called a universal logic block, and we place all of the effort in this study on the development of the silicon controlled rectifier NOR logic block.

Logic Blocks

A logic block may be defined as an elementary system performing a logical operation, such as AND, OR, or NOR. In some cases logic blocks are referred to as switching circuits. More accurately, however, switching occurs within the logic block, as a transistor may switch from the on to off condition.

There are three important reasons for including a discussion of common logic blocks in our study of the application of the silicon controlled rectifier. First, present

logic circuit techniques will provide a motive for the suggested silicon controlled rectifier circuits. In the second place, some insight into the electrical requirements of silicon controlled rectifier logic blocks will be gained. Finally this discussion will provide the background for comparing the silicon controlled rectifier logic block with other electron devices to determine its practicability.

Recently a logic block shorthand was developed which we will find convenient to use.⁹ The more important abbreviations are listed below.

DLC - Diode logic circuit

TRL - Transistor resistor logic

CML - Current Mode logic

Diode logic circuits are almost universally accepted as a simple, efficient, and fast computer component.¹⁰ Their primary disadvantage is the fact that a signal deteriorates as it passes through each block and must eventually be amplified and the wave shape corrected. The signals we shall be dealing with may be classified into two types. In a circuit utilizing the positive signal convention a true or 1 statement would be denoted by a positive d.c. voltage level, while a negative voltage or no voltage at all would correspond to a false or 0 statement. Correspondingly a

⁹General Electric Company, Transistor Manual (Syracuse, 1957), pp. 134-135.

¹⁰R. K. Richards, Digital Computer Components and Circuits (New York, 1957), pp. 36-63.

negative voltage indicates a true statement in a system using the negative signal convention.

A positive signal AND diode logic block and its corresponding truth table are shown in Fig. 8. When both lines A and B are at a low or negative voltage, the diodes D_1 and D_2 are forward biased and current flows through R.

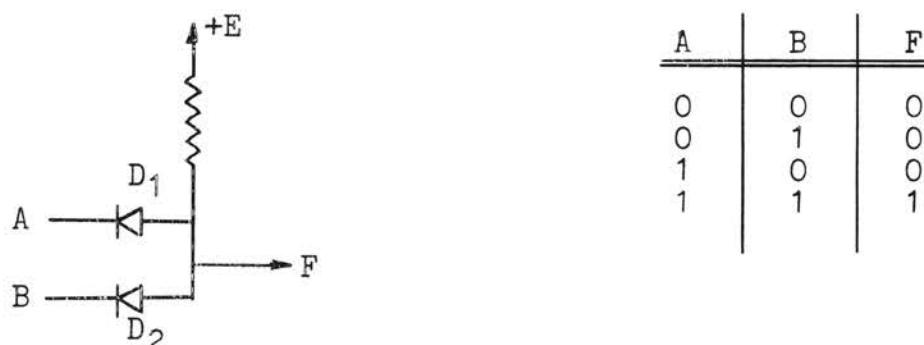


Fig. 8 AND Diode Logic Block

The voltage of the output line is at a low level. Even if line A is raised to a high positive voltage, D_2 continues to conduct, holding the output line at a low voltage; diode D_1 becomes back biased. If both lines A and B are raised to a high positive level, the output voltage will also rise. The up level of the output line indicates that both A and B are present on the input.

Fig. 9 illustrates the OR diode logic block. Note that if the negative signal convention is used, the circuit

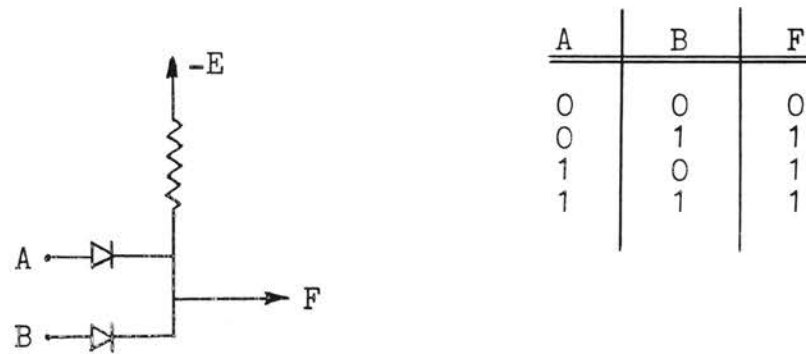


Fig. 9 OR Diode Logic Block

shown in Fig. 9 becomes an AND block. See Fig. 10. If lines A and B are at a high level, indicating 0, the output line will also be up since current will flow through diodes D_1 and D_2 producing a voltage drop across R. If the voltage of line A is reduced to a lower level, corresponding to 0, diode D_2 will continue to conduct and the output line will remain up as before. Making both lines A and B sufficiently negative, however, causes the output voltage to fall to a negative level, indicating a 1.

A description of a transistor resistor NOR logic block, the most common transistor logic operation, follows.¹¹ A detailed discussion would begin with semiconductor or solid state theory. However, our purpose is to present the TRL block so as to form a background for our discussion of the

¹¹"Silicon Transistor Logic Circuits for Industrial Systems" Texas Instruments Application Notes, Feb. 1960, p.4.

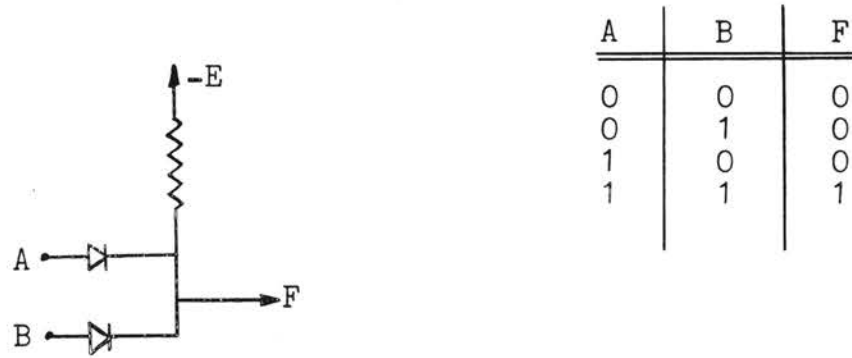


Fig. 10 AND Diode Logic Block

silicon controlled rectifier logic block. We can illustrate the necessary points by thinking of the transistor as a three terminal device having characteristics as illustrated in Fig. 11.

The transistor circuit shown in Fig. 12 performs the NOR operation on variables A , B , and C . See accompanying truth table. Here we specify the positive signal convention. The collector and emitter terminals of the transistor are in series with the collector resistor R_C . Assuming the load on the output of the stage to be negligible, we can select a current I_C , compute the drop across R_C , $I_C R_C$, and determine the collector-emitter output voltage,

$$V_{CE} = V_{CC} - I_C R_C . \quad \text{Eq. 9}$$

This is plotted as the load line in Fig. 11. Note that the input base current determines the collector current and

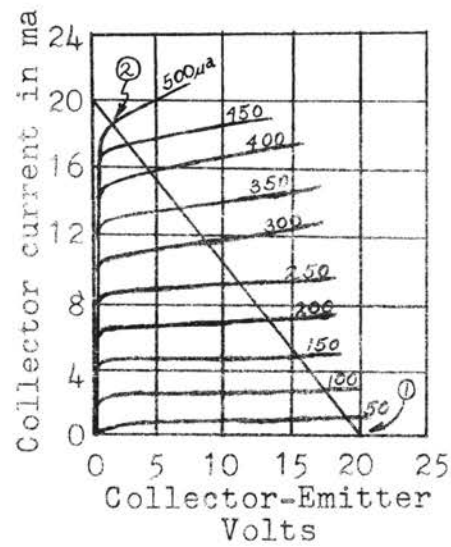
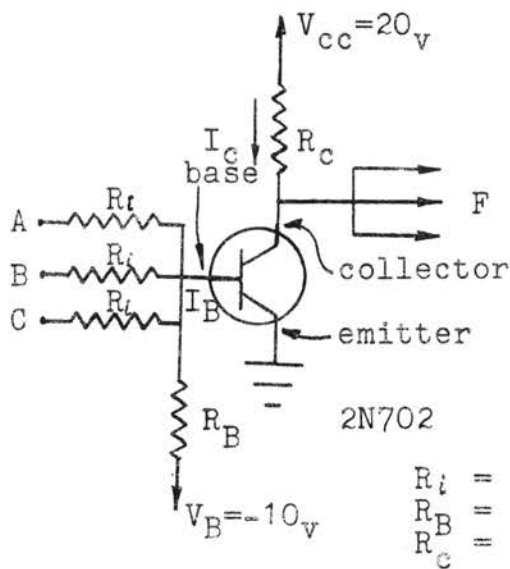


Fig. 11 2N702 Transistor
Collector Characteristics



A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Fig. 12 Transistor Resistor NOR Logic Block

output voltage of the circuit. We state now that the base to emitter input impedance of the transistor is very low, about 500 ohms, and very much less than R_B . If all the inputs A, B, and C are open, a negative base current I_B , about 0.6 ma will flow. This holds the transistor at point 1 on the load line and results in an output voltage of 20 volts. If a step of 3.5 volts is applied to input line A, a current of about 500 μ a will flow into the base of the transistor, switching its operating point to 2. The low level of output voltage corresponds to a 0 in the truth table. A similar voltage on one or a combination of the other input lines would hold the transistor in its on condition in the neighborhood of point 2.

The speed of the TRL block is a statement of the rapidity with which it switches from off to on and vice versa.¹² The collector current I_C of the circuit would appear as shown in Fig. 13 if a square wave of current were placed on the input. There are three principal reasons why the collector current does not appear as a perfect square wave.

1. The collector current flows through the semiconductor material via atomic particles of matter. A finite time is required for the movement of these particles, much as the transit time in a vacuum tube. Thus a current change does not occur instantaneously.

¹²Lloyd P. Hunter, ed., Handbook of Semiconductor Electronics by J. C. Logue (New York, 1956), Sec. 15-30.

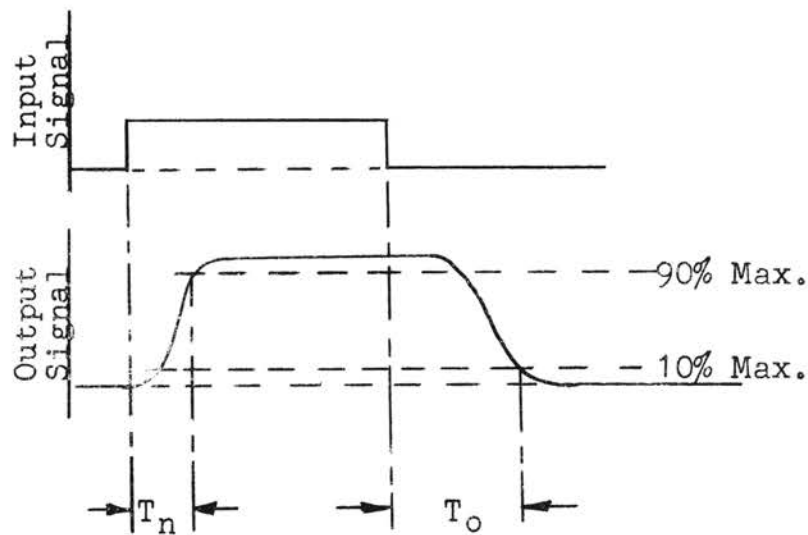


Fig. 13 Turn-on & Turn-off Times of a Transistor

2. As with any physical electronic device, certain capacities are involved which must be charged and discharged as the transistor switches from one state to another.
3. With increasing frequency the decrease in current gain of the transistor also changes the shape of the square wave.

The AND operation may be performed by the TRL NOR block using the wiring arrangement described by Eq. 5.¹³ In this circuit (See Fig. 14) an input signal only on line A causes the voltage at point 1 to drop, while a voltage at point 2 remains up. The up level at either point 1 or 2 sets transistor 3 full on and places the output line F

¹³Texas Instruments Application Notes , p. 4.

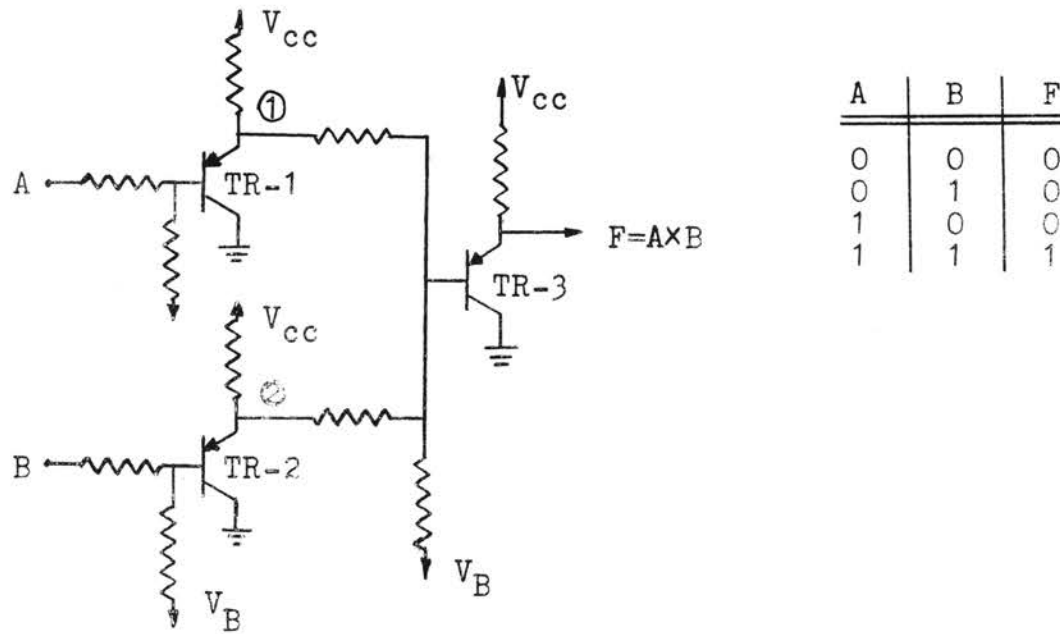


Fig. 14 AND Logic Circuit Using TRL Block

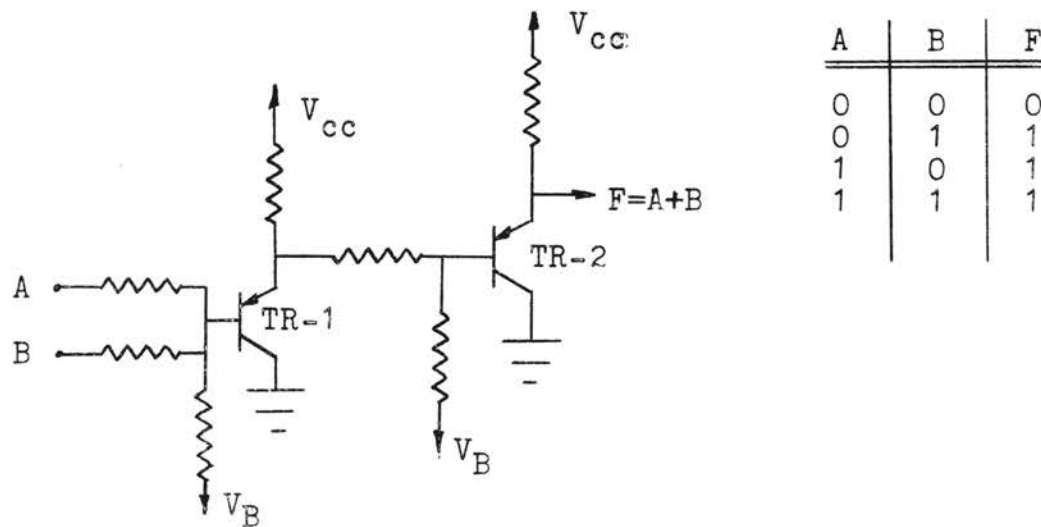


Fig. 15 OR Logic Circuit Using TRL Block

at a low level. Fig. 15 shows an OR circuit constructed from TRL NOR blocks.¹⁴

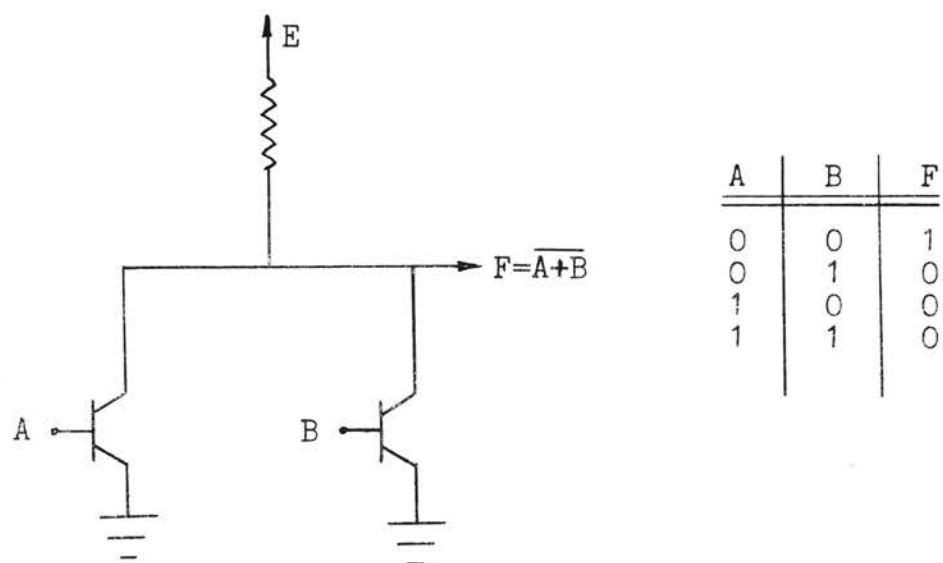
The logic blocks we have discussed thus far may be classified as voltage mode logic. This denotes the fact that the input was observed to be true or false by the magnitude of the voltage. In 1955, a paper prepared by Beter, Bradley, Brown, and Rubinoff indicated that a current could be thought of as carrying logic information.¹⁵ This technique of logic block design is known as current mode logic, abbreviated CML. While the placement of components in a CML block may resemble the previously discussed TRL, the action is quite different. Here the transistor is biased from a constant current source. Its effective change in resistance with changing base drive serves to switch the current through the transistor or through the load or following logic block. The voltage excursion at the output is very small and a 1 or a 0 is indicated by the presence or non-presence, respectively, of a current at the point. NOR and NAND current mode logic blocks are illustrated in Fig. 16.

Electrical Requirements

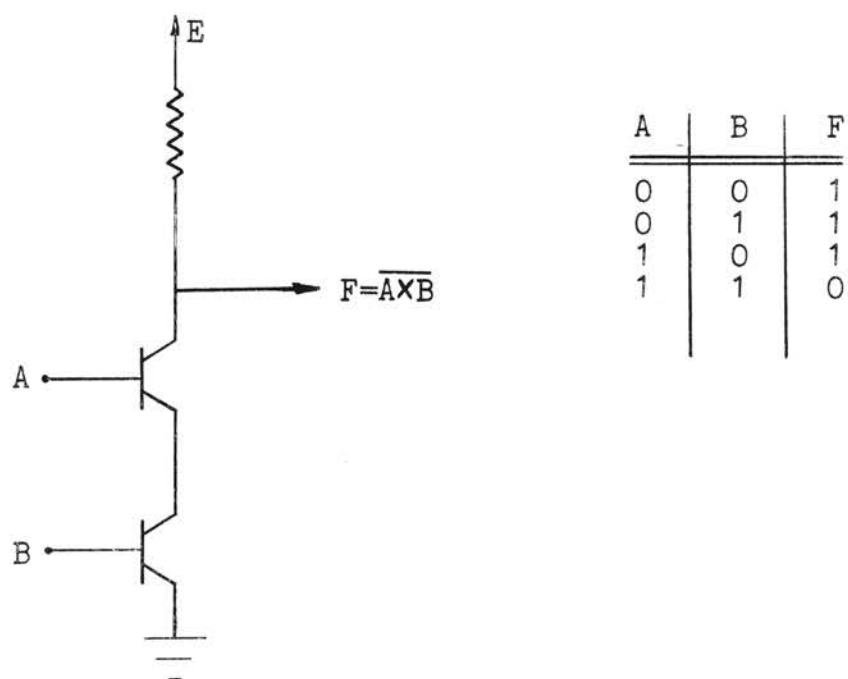
The first objective of this study was to determine the

¹⁴Ibid.

¹⁵W. E. Bradley et al., "Surface Barrier Transistor Computing Circuits," IRE Convention Record, Part IV, pp. 139-145.



(a) Current Mode NOR Circuit



(b) Current Mode NAND Circuit

Fig. 16 Current Mode Logic Circuits

feasibility of logic blocks using the silicon controlled rectifier. To prepare for the evaluation to follow, we need to outline the basic requirements of a logic block.

1. Universality of the Logic Block. From the material presented previously one sees that a great number of NOR logic blocks would be used in even a simple counting device, perhaps several hundred or several thousand. It is desirable, from this standpoint, to have a universal logic block, in other words, a logic block that may be connected with other logic blocks in a variety of ways without designing each separate stage. There are two considerations here. First, voltages and impedances must be considered to assure efficient, reliable operation of the circuit under the adverse effects of component tolerance and power supply fluctuations. The second limitation is more important to our discussion. In most applications logic blocks with several input and output lines are required, and it is often difficult to provide the logic circuit requirements and to continue to meet the electrical qualifications listed as the first consideration. Mr. J. C. Logue, writing in the Handbook of Semiconductor Electronics, makes the following statement:

It has been found from experience that, if an amplifier or logic block can drive at least three other amplifiers, it can be satisfactorily used in a computing system. If it can drive only two others, the design of the computing system becomes difficult. If it can drive only one other amplifier, it is practically impossible to use it in a computing system.¹⁶

In addition many recently developed logic circuits utilize blocks having as many as ten input and output lines.

2. Reliability of the Logic Block. A high speed computer or control system functioning in a defense network must be highly reliable. Thus each individual component or logic block must be carefully designed to prevent failure.

Errors may be caused in solid state logic circuits due to temperature changes, as well as conventional component failures. Many considerations, such as speed and low power consumption, require voltage levels and signal changes to be small. Since the characteristics of transistors and diodes are very sensitive to temperature, the output voltage of a NOR circuit may erroneously indicate a 0, if the circuit is improperly stabilized.

3. Component Count. The number of components required to perform a logical operation is important to the design engineer for two reasons. First, the number of components is a direct indication of relative cost of the system. In the second place, the probability of errors in construction as well as the possibility of component failure will rise as the number of components increases.

4. Logic Block Switching Speed. For the electronic computer to multiply two 10 digit numbers in one millisecond to one hundred microseconds, its logic circuitry must operate extremely fast. Switching speeds on the order of a

¹⁶Hunter, Sec. 15-29.

microsecond are frequently required. On the other hand, some computing systems such as business machines operate at much slower speeds. In some cases logical operations at the rate of sixty cycles per second are adequate.

5. Power Requirements. Much of the work in logical control systems has aimed at reducing the size and power requirements of the components. This would be of prime importance in a satellite. In many cases, however, weight and power requirements are relatively unimportant. For example, the few hundred watts required by a control system would be insignificant in comparison to the thousands of kilowatts that the motors in a steel mill require.

CHAPTER III

THE SILICON CONTROLLED RECTIFIER

Characteristics

The solid state theory of the silicon controlled rectifier has been presented in detail in other places.¹⁷ Because we are dealing with the circuit applications of the device, we are not directly concerned with the theory of the internal conduction mechanism. Thus a discussion of the terminal characteristics will provide the background necessary for this study, and the atomic action will be presented only where necessary. Often the name silicon controlled rectifier is abbreviated SCR; we shall use this notation.

The schematic symbol for the silicon controlled rectifier is shown in Fig. 17a. The device is constructed of four layers of semiconductor material arranged, as shown in Fig. 17b, in alternate P type and N type layers.

The characteristics of the SCR are often explained¹⁸

¹⁷I. M. Mackintosh, "The Electrical Characteristics of Silicon PNP Triodes," Proceedings of the IRE, XLVI (1958), 1229-1235.

¹⁸J. M. Goldey, "PNPN Switches-Diodes and Triodes," Control Engineering, October 28, 1960, pp. 101-104.

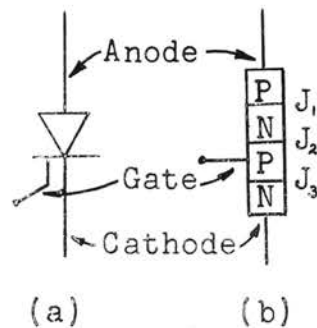


Fig. 17 Symbol for
Silicon Controlled
Rectifier

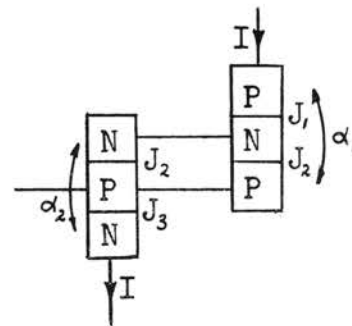


Fig. 18 Two-Transistor
Analogy of Silicon
Controlled Rectifier

using a two-transistor analogy. We note that the four layer structure shown in Fig. 17b can be separated into the two three layer groups shown in Fig. 18. The three layer group on the right may be thought of as a PNP transistor, while the layers on the left resemble an NPN transistor. The collector base and emitter regions of the transistor are labeled. The junctions in the analogous transistor arrangement are numbered to correspond to the junctions of the four layer structure. If a positive voltage is applied to the anode lead in Fig. 18, junction J_1 and J_3 will be forward biased, while junction J_2 will be reverse biased. This corresponds to the common emitter operation of each of the transistors.

The current gain for each transistor is shown in Fig. 18. The current across the junction J_2 will be com-

posed of three parts, the hole current in the PNP transistor $I\alpha_1$, the electron current in the NPN transistor $I\alpha_2$, and the leakage current I_{CO} typical of the reverse biased junction J_2 . As this current is equal to the current I in the external circuit, we have:

$$I = \alpha_1 I + \alpha_2 I + I_{CO} \quad \text{Eq. 10}$$

This can be rewritten in the form:

$$I = \frac{I_{CO}}{1 - (\alpha_1 + \alpha_2)} \quad \text{Eq. 11}$$

The importance of this result may be seen by considering the increase in I as $\alpha_1 + \alpha_2$ approaches unity. This is in fact the action that takes place in the SCR.

The current gain α of a transistor is a function of the emitter current as shown in Fig. 19.

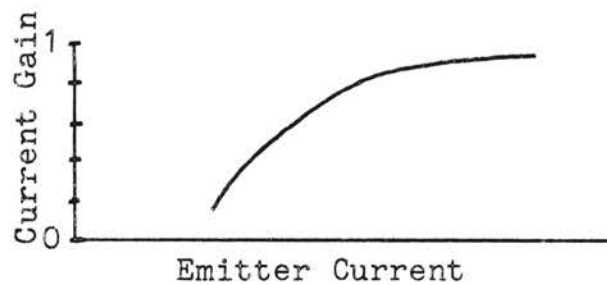


Fig. 19 Current Gain α as a Function of Emitter Current

As the anode-cathode voltage of the SCR is increased, the current I increases only slightly at first. However, as I increases, the α 's also increase causing an additional increase in I . At some value of anode voltage, called breakover voltage BV_F , this action becomes unstable and the current I increases until it is essentially limited only by the external circuit resistance. To illustrate this action a plot of the current through the SCR as a function of the voltage across it is shown in Fig. 20a. If the polarity of the voltage applied to the device is increased, junctions J_1 and J_3 will be reverse biased. The volt-ampere characteristic of the SCR in this condition is shown in Fig. 20b; it is similar to a reverse biased diode.

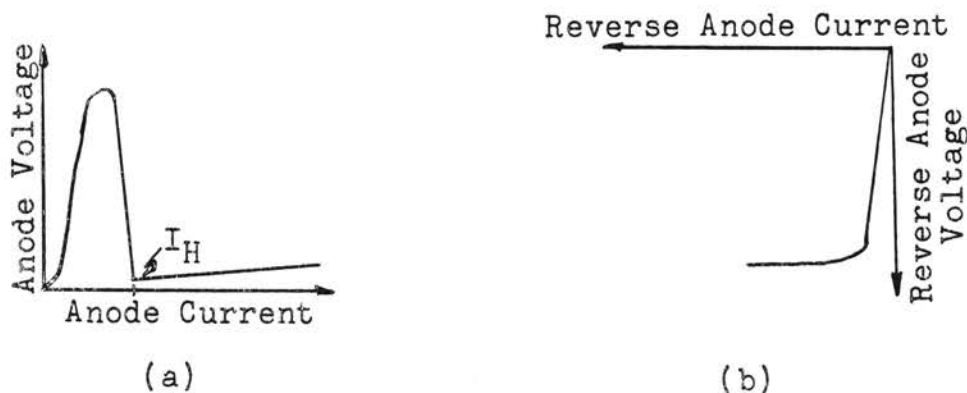


Fig. 20 Characteristics of Silicon Controlled Rectifier

Since α is a function of the emitter current, a current flowing from the gate to the cathode or the emitter of

the NPN transistor will increase α_2 . Thus a current into the gate can also cause the SCR to switch to a conducting state. The effect of increasing the gate current I_G is shown by the family of forward volt-ampere curves in Fig. 21b.

The gate current required to fire the SCR in the elementary circuit shown in Fig. 21a can be determined by graphical analysis. A load line of slope $1/R_a$ is plotted from point E_a on the ordinate to point E_a/R_a on the abscissa axis as shown in Fig. 21b.

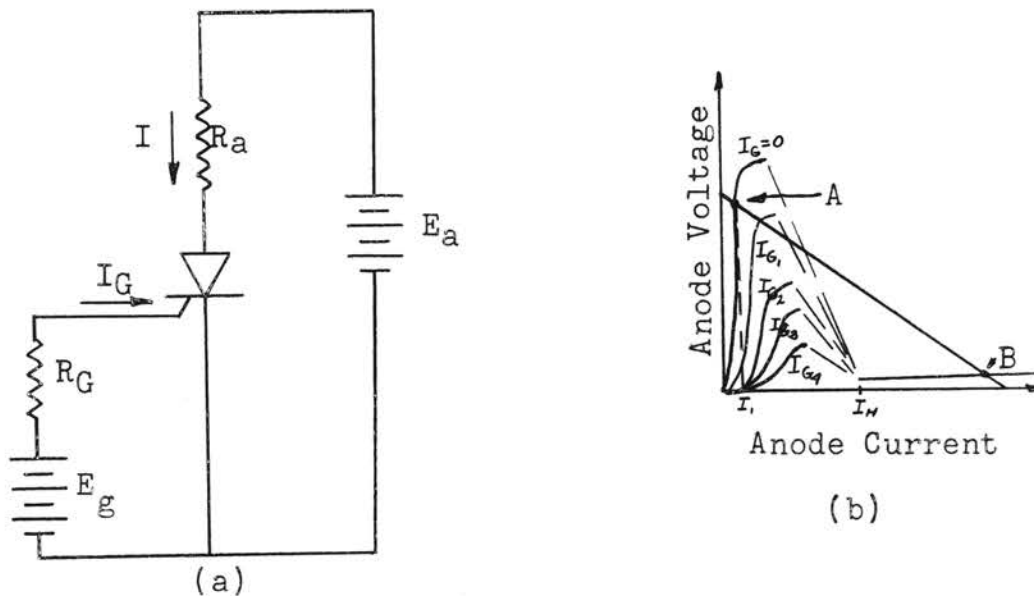


Fig. 21 Gate Turn-on Characteristic of SCR

If the gate current is zero when the anode voltage is applied, a small current I_1 will flow and the circuit will

stabilize at point A . If gate current equal to I_{G3} is applied, it will cause the circuit to switch to point B . At this point the current through the SCR and R_a are equal, and the sum of the voltages across the SCR and R_a equals the applied voltage E_a . If the gate current is removed, $I_G = 0$, the circuit will continue to operate at point B since the anode current I has increased sufficiently to cause $\alpha_1 + \alpha_2 = 1$. Any method for reducing $\alpha_1 + \alpha_2$ to a low value will cause the SCR to switch to the high impedance state, point A . A large current I_{G0} flowing out of the gate lead will reduce the number of carriers crossing junction J_3 and thus, reducing α_2 , will switch the SCR to point A . In addition, if the current I is momentarily reduced to zero, the device will switch to the high impedance state. Consequently, removing the voltage E_a momentarily or shorting the circuit around the SCR will turn the unit off.

It should be mentioned at this time that an anode current I_H (called the holding current) exists, below which $\alpha_1 + \alpha_2$ is not large enough to hold the device in the conducting or on state. This current corresponds to the point I_H in Fig. 20a and Fig. 21b. The magnitude of the holding current is very sensitive to temperature.

The gate to cathode connection through the silicon controlled rectifier includes the PN junction J_3 . For this reason the gate and cathode terminals have a diode volt ampere characteristic when no anode current exists.

This characteristic is shown in Fig. 22. On the other hand, if the SCR is conducting, junction J_3 will be forward biased by the carrier flow across it. If a small negative voltage is now applied to the gate, the junction will appear as a relatively low non-linear resistance. When a sufficiently large reverse gate current flows, a large portion of the carriers from the P region of the SCR will be removed. The SCR will switch off, and the gate cathode volt ampere curve will switch from point A to B. See Fig. 22.

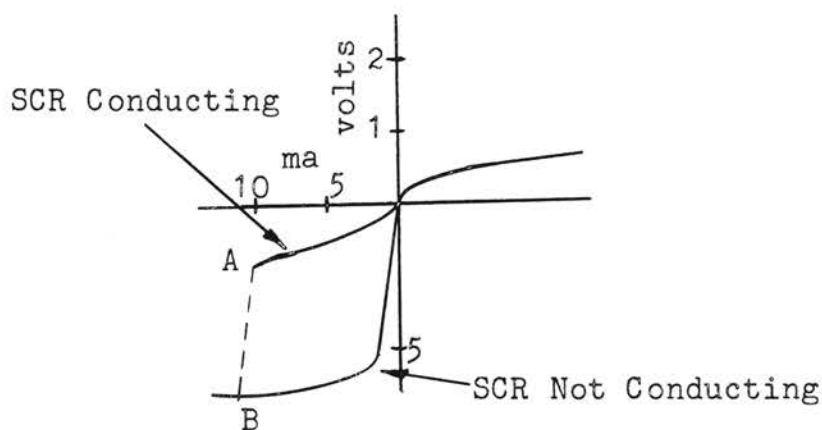


Fig. 22 Gate Cathode Volt-Ampere Characteristic of SCR

It has been found that by placing a resistance of about 1000 ohms in parallel with the gate - cathode junction,

the reliability of the SCR can be improved. This resistance shunts part of the current that would flow across J_3 , thus reducing the sensitivity of α_2 with respect to gate and anode currents. In terms of SCR parameters this resistance increases the breakover voltage BV_F and increases the forward gate current required to turn the SCR on. Recently Texas Instruments, Inc. has built this shunting resistance into the semiconductor structure.

In addition to the parameters previously defined, two other terms will be important in our discussion of direct mode logic blocks. We define the forward current gain to be the ratio of the maximum forward anode current of the SCR in the conducting state to the gate current required to switch the unit on. The reverse current gain, on the other hand, is the ratio of the anode current gain which can be switched off to the reverse gate current required to switch the SCR off.

Transient Behavior

The transient characteristics of the silicon controlled rectifier are similar to those of the transistor. However, additional consideration must be given to the turn-off mechanism.¹⁹ A circuit which might be used to determine the response of the silicon controlled rectifier is

¹⁹Walt Matzen, Switching Time of NPNP Triodes (Texas Instruments, Inc. Memorandum.)

shown in Fig. 23. The step of anode voltage, $E_a < BV_F$, is applied, followed by the gate signal. After the silicon controlled rectifier has switched to the conducting state, the gate signal is removed. As the anode voltage drops to zero the device will turn off. The relative timing of the anode and gate voltages is shown in Fig. 24. The shape of the anode current with the prescribed input is shown in sketch c.

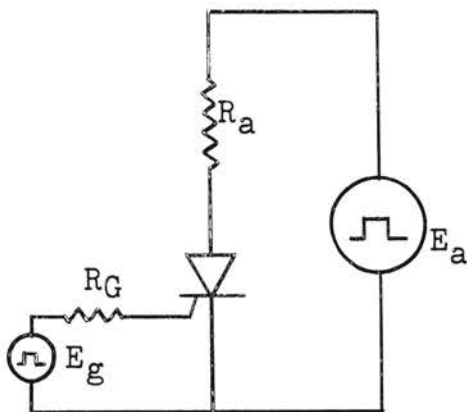


Fig. 23 SCR Transient Test Circuit

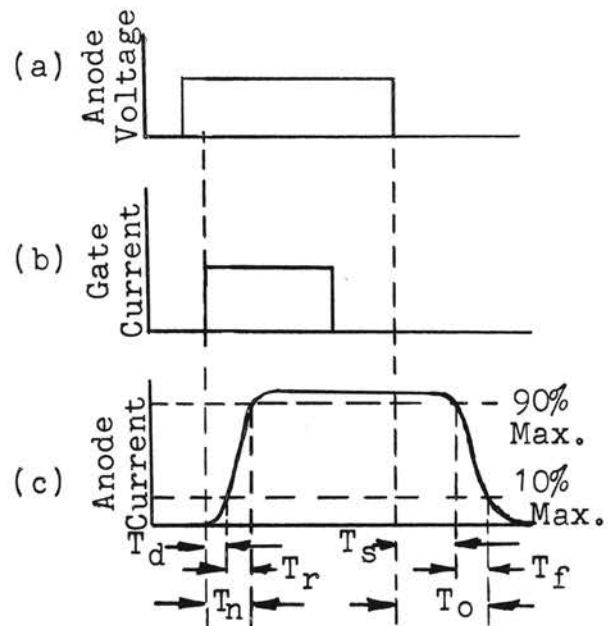


Fig. 24 Transient Response of SCR

The delay time T_d is the time after the gate signal is applied during which the SCR is relatively inactive. The time required for the current to rise from 10% to 90% of its final value is called the rise time T_r . The total

turn-on time T_n is the sum of the delay time and the rise time. The finite turn-on time is due principally to the time required for the carriers to distribute themselves in the base regions of the PNP structure. The turn-on time of the silicon controlled rectifier is important to the proper operation of the alternate mode logic block and will be discussed in more detail in Chapter 5.

While the silicon controlled rectifier is in the conducting state, the base regions are heavily saturated with minority carriers. After the anode voltage is removed, the junction J_2 will remain forward biased for a short time while the carriers distribute themselves in the crystalline structure. The time during which J_2 is forward biased is called the storage time T_s . The fall time T_f is the time required for the carriers to return to the steady state condition. The total turn-off time T_o is largely a function of the anode current present before turn-off. Turn-off time is generally 5 to 10 microseconds.

Ratings

The ratings of several commercial silicon controlled rectifiers are presented in Table II. Only the parameters which are considered to be important to this discussion are listed. It should be noted that units having higher forward and reverse breakdown voltages than those listed are available in the 2N159, 2N160, and TI-1 series. The TI-116 and the corresponding series have the built in gate-cathode

shunting resistance described previously. Note also the higher gate current required to turn this series on, due to the shunting resistance.

As with all solid state devices, the principal limit to the power handling capacity of the SCR is the temperature of the semiconductor material. The upper limits to the power dissipated in the silicon controlled rectifier will, in general, be of little concern in this discussion. Certainly the power required by a logic block must be as small as possible if hundreds of them are to be connected in a control circuit.

The turn-on and turn-off current gains for several units are listed in Table III. The turn-off characteristics for the last three units are not listed on the manufacturers specification sheet. Tests of the gate turn-off characteristics of a TI-118 unit were made in the laboratory, and the results are shown in Fig. 25. The turn-off current gain for this unit is 1.87 with an anode current of 15 ma.

TABLE II
RATINGS OF TYPICAL SILICON CONTROLLED RECTIFIERS

Type	BV _F	BV _R	I _{Fmax}	I _{Gmax}	I _{GT}	I _{GO}	I _{FS}	I _H
	volts		amps	milliamps				
TI-010	60	60	1	100	5	5	10	5
TI-025	60	60	1	100	10	10	25	10
TI-050	60	60	1	100	20	20	50	25
2N1595	60	60	1	100	10*			25
2N1600	60	60	3	100	10*			25
TI-116	240	240	1	100	50			50

*1000 ohm gate shunt resistance

Abbreviations used above:

- BV_F - minimum forward breakdown voltage at 125°C
 BV_R - minimum reverse breakdown voltage at 25°C
 I_F - maximum average rectified forward current at 80°C
 I_G - maximum forward gate current at 125°C
 I_{GT} - maximum gate current to trigger at 25°C
 I_{GO} - maximum gate current to switch off at 25°C
 I_{FS} - maximum anode current for gate switching off at 25°C
 I_H - maximum holding current at 25°C

TABLE III
TURN-ON AND TURN-OFF CURRENT GAIN OF SEVERAL SCR'S

Type	Turn-on Current Gain	Turn-off Current Gain
TI-010	200	2
TI-025	100	2.5
TI-050	50	2.5
2N1595	100	
2N1600	300	
TI-116	20	

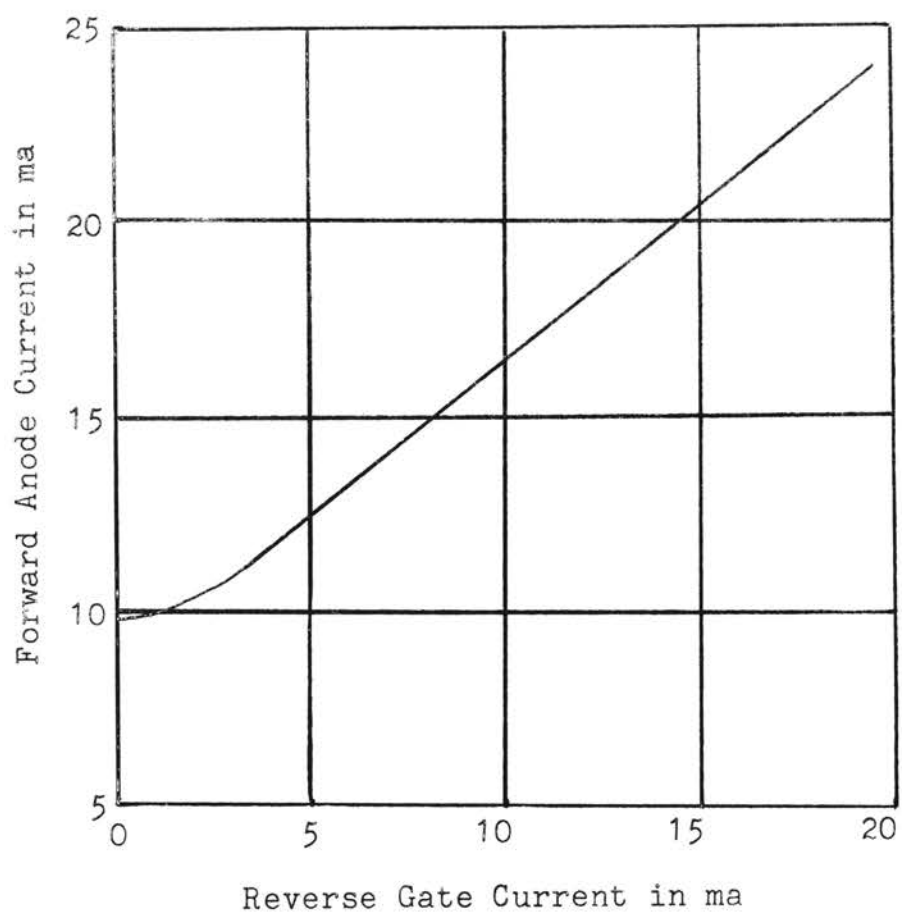


Fig. 25 Reverse Gate Current Turn-off Characteristics of Typical TI-118

CHAPTER IV

THE DIRECT MODE LOGIC BLOCK

The three proposed silicon controlled rectifier logic blocks discussed in this chapter are classified as direct mode logic blocks. This terminology implies that the input signal to the logic block determines the output directly and immediately. Later we shall contrast this to an arrangement, called the alternate mode, in which the output of the logic block will be valid only at a specific time. We shall consider three types of SCR NOR logic blocks in this section, the reverse gate bias logic block, the holding current logic block, and the capacitor coupled logic block.

Reverse Gate Bias Logic Circuit

The reverse gate bias logic circuit utilizes a current flowing out of the gate to switch the SCR off. Consider the circuit and associated truth table shown in Fig. 26. Let us assume lines A and B are both open (or 0.) The gate bias circuit R_g and E_g is arranged to provide sufficient reverse gate current to turn the device off when it is conducting. The anode-cathode impedance of the SCR in the off condition is very much greater than the anode re-

sistance R_a and practically all of the anode voltage will appear at the output E_o , indicating 1. If sufficient current is driven into either line A or B or both, the device will be turned on and the output voltage will drop to a low level, indicating a 0.

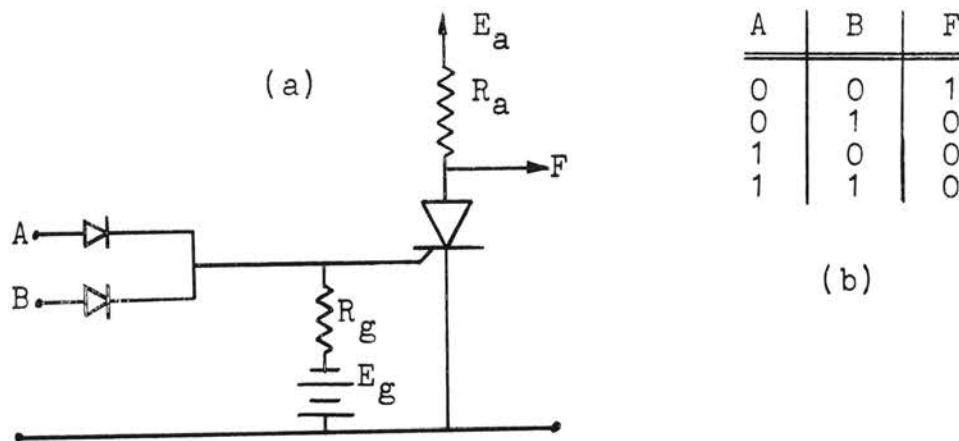


Fig. 26 Reverse Gate Bias NOR Logic Block

We observe that the only time a 1 is present on the output line is when A and B are both zero. This is indicated in the truth table. The Boolean function

$$F = \bar{A} \times \bar{B} \quad \text{Eq. 12}$$

corresponds to this situation. This function was defined previously to be the 'universal' NOR function, and thus the logic block is a NOR logic block.

Two of the requirements of logic blocks discussed in

Chapter II are important here. These are: 1. The logic block must be of universal design. In other words, a circuit with fixed component values must fit anywhere in the logic system. 2. To be useful in a logic circuit design a logic block must have three or more input and output lines. An analysis of the reverse gate voltage logic block will proceed on the basis of these requirements.

Consider the two NOR logic blocks, one driving the other, shown in Fig. 27.

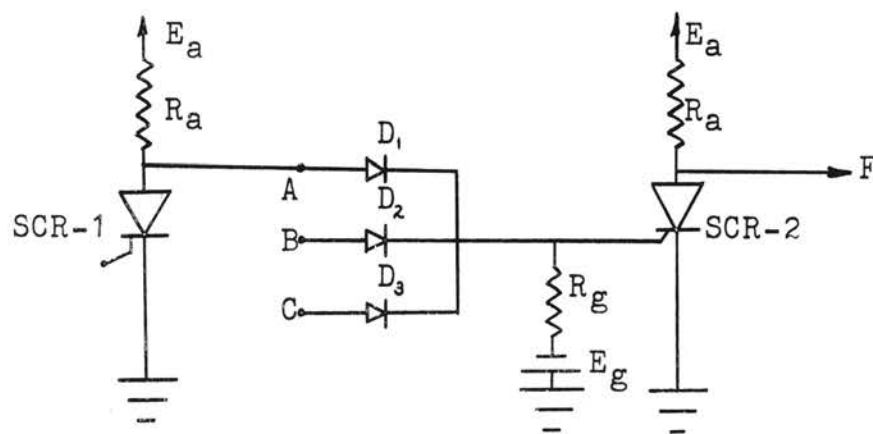


Fig. 27 Reverse Gate Bias NOR Logic Circuit

The elements R_g , R_a , and E_g play the same role as in Fig. 26. The diode D_1 serves to isolate the anode of SCR no. 1 from other logic blocks connected to lines B and C. The actual specification of circuit parameters is very simple. Let us consider the TI-025. This unit is

specified in Table II as requiring a maximum of 10 ma reverse gate current to switch off 25 ma anode current. We begin the design by selecting an anode supply of 25 volts. Since the specifications do not guarantee that a reverse gate current of 10 ma will switch off anode current in excess of 25 ma, and since, as we shall see later, it is desirable to design the circuit to operate into a maximum load, we specify an anode current of 25 ma. Thus R_a must be 1 k ohm. A 10 ma reverse gate bias is required to turn the 25 ma anode current off. If we select E_g to be 10 volts, R_g will be fixed at 1 k ohm. We have neglected the gate to cathode impedance, about 50 ohms, in series with the 1000 ohm resistance R_g .

All of the component values have been specified on the basis of the reverse gate current required to turn the device off with no voltage present at A, B, or C. This would be the case if SCR no. 1 and similarly connected SCR's at B and C were in the conducting state. Now assume SCR no. 1 to be turned off. As the potential at point A is increased, the forward gate current must be sufficient to turn SCR no.2 on. An equivalent circuit for this action is shown in Fig. 28. The loop current equations are:

$$25 + 10 = i_1 (1000 + 1000) - i_2(1000) \quad \text{Eq. 13}$$

$$- 10 = -i_1 (1000) + i_2(1050) \quad \text{Eq. 14}$$

Solving these we find that the forward gate current i_2 is

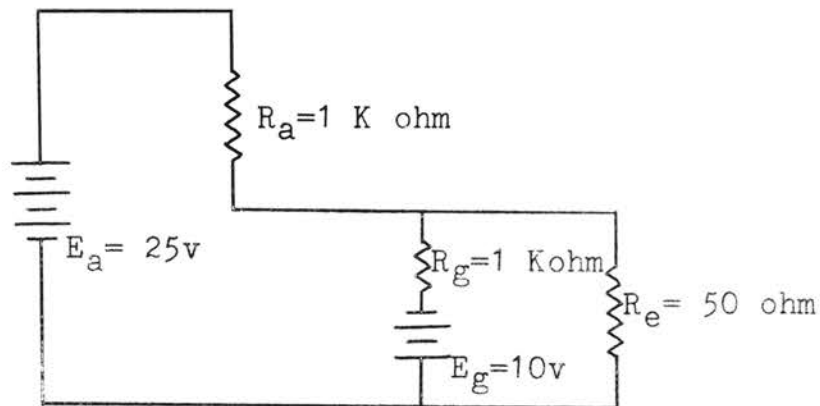


Fig. 28 Equivalent Circuit of Reverse Gate Bias Logic Circuit

13.6 ma. As the maximum gate current required to turn the device on is 10 ma, our circuit design will fit universally with other logic blocks of the same type. Thus the requirement above is satisfied.

On the other hand, it should be noted that an additional load paralleling the gate circuit of SCR no. 2 would reduce the voltage at point A. Consequently, the forward gate current i_2 would be reduced. If the additional load is a gate bias circuit similar to the one discussed here, the forward gate current into SCR no. 2 will be decreased by some 50%. Thus the current would not be large enough to turn SCR no. 2 on. It is evident that this reverse gate voltage circuit can provide only one output line; this fact was termed 'practically impossible to use in a computing system' in Chapter II. Thus the second requirement above is not satisfied.

This limiting factor can be overcome with a higher gate turn-off gain. As the turn-off gain is increased, the bias resistance R_g can be increased; thus the load on SCR no. 1 is reduced. Several more output lines could then be handled by one logic block, and this SCR NOR logic block would be practical for applications in control and computing equipment.

Capacitor Coupled Logic Block

A capacitor coupled NOR logic block was devised and is discussed briefly here. A circuit diagram illustrating this connection is shown in Fig. 29.

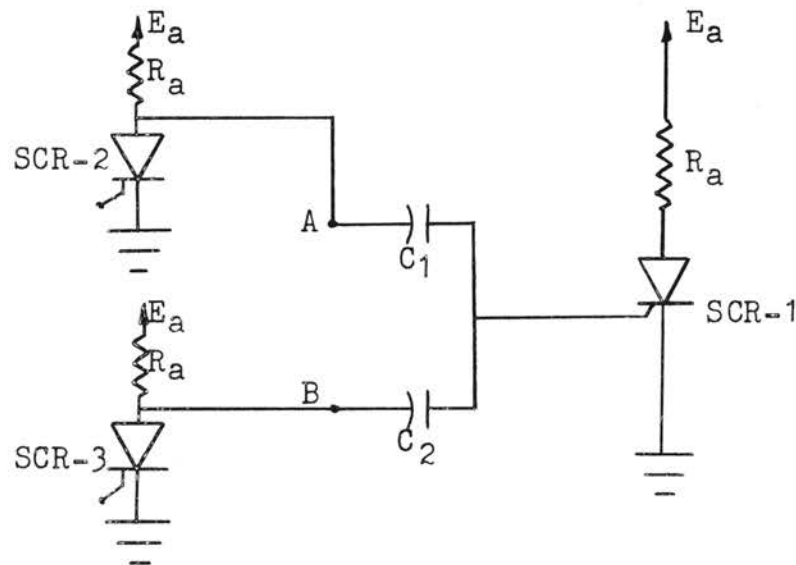


Fig. 29 Capacitor Coupled NOR Logic Block

The capacitor and gate resistance of the SCR act as a dif-

ferentiating circuit. If a square wave of voltage is applied to the capacitor terminal, a current will flow into the gate as the capacitor charges up, turning the device on. When the voltage at the input falls, the capacitor will discharge and a reverse gate current will flow. This reverse current will serve to turn the SCR off if sufficient energy has been stored in the capacitor.

It is impractical to provide for more than one input line to this circuit. Consider the anodes of each of two SCR's to be connected to the input lines A and B as shown in Fig. 29. Let us assume that SCR no. 1 is off and SCR's no. 2 and 3 are conducting. If we desire to switch SCR no. 1 on, we could, for example, turn unit no. 2 off, thus applying a step of voltage at point A. The difficulty here lies in the fact that point B is held at ground potential and capacitor C_2 shunts a majority of the "turn-on" current pulse to ground. In addition to a limit of one input, the number of output lines this circuit can drive is restricted. This problem is similar to the one outlined for the reverse gate logic block. If two output lines are driving similar SCR capacitor coupled logic blocks, the anode resistance of the device must be lowered to allow pulses of current having sufficient magnitude to flow into each gate circuit. On the other hand, when the "driver" SCR is turned on, it must also carry additional current due to the reduced anode impedance. The result is that this unit will not switch off. Since the capacitor coupled NOR

logic block is restricted to one input and one output line, it does not meet the requirements discussed previously.

Holding Current Logic Block

We noted in the discussion of the reverse biased and capacitor coupled logic blocks the problems associated with turning the silicon controlled rectifier off. We recall from Chapter III that if the anode current of the device is below a certain level, called the holding current, the SCR will turn off when the gate signal is removed. It is natural to attempt to utilize this characteristic in the design of a direct mode logic block.

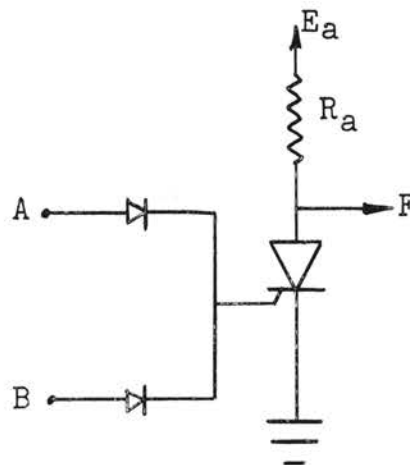


Fig. 30 Holding Current NOR Logic Block

A circuit diagram of a holding current NOR logic block is shown in Fig. 30. The minimum holding current I_H of

the SCR is assumed to be known. Values of R_a and E_a are selected to allow an anode current smaller than I_H to flow when the SCR is on. For example, assume the holding current is 12 ma; an anode current of 10 ma would be low enough to assure that the device would turn off when the gate signal is removed. The output of this circuit would be connected through an isolating diode to the gate of the following logic block. When the SCR is switched off, the anode potential will rise and a current will flow into the gate of the following unit, turning it on. Note that the value of R_a and E_a fix the anode current below the level of the holding current; thus the maximum current that can flow in the output circuit when the SCR is off is less than the holding current of the device.

The maximum output current available from the logic block again limits the number of output lines. Often the gate driving current for an SCR is only slightly less than the holding current. Production distributions of gate currents and holding currents are shown in Fig. 31 and 32. The gate current level shown is the maximum gate current required to turn the SCR on. It can be seen from Fig. 32 that present manufacturing methods do not yield silicon controlled rectifiers having a high holding current. In addition, Fig. 32 shows the reduction in holding current with increasing temperature. The logic block was designed to operate with an anode current of 10 ma. If the temperature of the SCR were increased to 150°C, the holding current would drop

to around 9 ma and the device would not turn off with the removal of the gate signal. The holding current NOR block is more sensitive to changes in temperature than the other direct logic blocks.

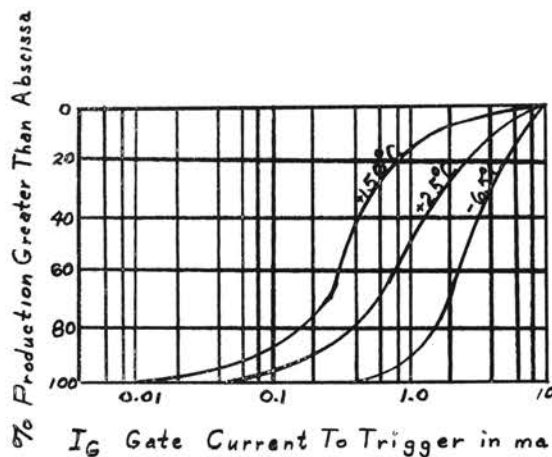


Fig. 31 Production Distributions of Gate Current to Trigger

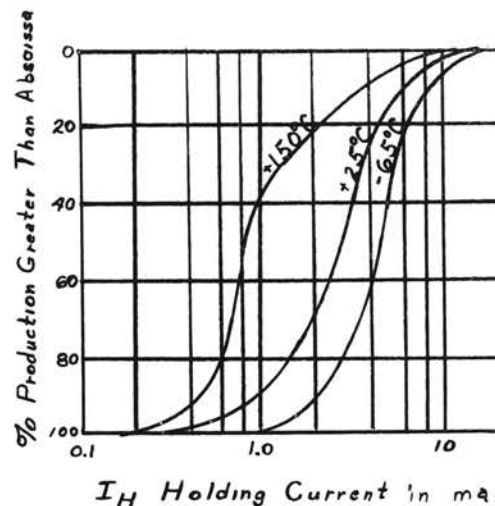


Fig. 32 Production Distributions of Holding Current

Evaluation of the Direct Mode Logic Blocks

A restriction common to all of the direct mode logic blocks is the limit of one output line. According to the requirements outlined in Chapter II this is wholly unsatisfactory. The holding current design is restricted to one output line by the minimum holding current of the device and the maximum gate current to trigger the following stage.

The capacitor coupled and reverse gate bias logic blocks are restricted to one output line by the maximum anode current which can be switched off by a reverse gate current. However, both of these restrictions can be controlled by the design of the device.

Compared to the other SCR arrangements, the holding current NOR circuit is highly sensitive to temperature. While the forward and reverse gate currents required to trigger the SCR in the other circuits are sensitive to temperature, the required current levels decrease with increasing temperature, actually improving the circuit operation in some cases. Because an increase in temperature may cause the holding current logic circuit to become inoperative, it is impractical.

The limit to the number of input lines of the capacitor coupled logic circuit is unsatisfactory. This difficulty could be eliminated if higher turn-off and turn-on gains were practical. On the other hand, the action of the capacitor coupled logic block is unsound from a reliability standpoint. After the SCR has been switched on by the applied signal, no forward gate current is present to maintain the unit in the on state. The ability of the SCR to continue to conduct with no signal applied is used to advantage in some applications. In a logic circuit design, however, this unreliable action would not be satisfactory.

The reverse gate bias NOR logic block, then, is probably the most feasible of the direct mode logic circuits.

As stated previously this logic block appears to be limited to one output line. However, when a silicon controlled rectifier with high turn-on and turn-off current gains becomes available, this limitation will be eliminated.

The principal effect of an increase in temperature on the reverse bias logic block is the increase in leakage current through the SCR in the off state. The increase in leakage current is, in effect, a decrease of the high "off" impedance of the device. However, any reasonable change in leakage current will have little effect on the operation of the logic block, since the SCR is shunted by the low impedance gate circuit of the following NOR block. As a result, the reverse bias arrangement has a very definite on-off condition. This highly desirable feature will give improved reliability in a logic circuit.

Since silicon controlled rectifiers with high turn-on and turn-off current gains are not available in production quantities at this time, other logic block arrangements were investigated. The next chapter is a discussion of one of these, the alternate mode logic block.

CHAPTER V

THE ALTERNATE MODE LOGIC BLOCK

The logic blocks discussed previously were called direct mode logic blocks. The term direct was used because the input signal caused the silicon controlled rectifier to be switched from one state to another. The principal feature of this operation is the continuous output signal. In other words, the output of the circuit indicates the state of the input (with regard to the logic function being performed) continuously. The direct mode action is highly desirable where the speed of the logic circuit is of utmost importance. However, some of the recent applications of logic circuits do not require fast switching times; a few even operate at sixty cycle per second switching rates. If the speed of the circuit is not important, we might agree to look at the output line only at specific times. The condition of the output at the time specified would indicate the condition of the input information during the same period. This system we call the alternate mode logic system.

The Silicon Controlled Rectifier

Alternate Mode NOR Logic Block

The difficulty in turning the silicon controlled recti-

fier off through the gate-cathode circuit was pointed out in Chapter IV. Generally, it is much easier to turn the SCR off in the anode-cathode circuit. There are two principal methods for doing this. 1. Removing the anode voltage will switch the SCR to the high impedance state. 2. As the SCR has some small internal impedance, a switch or similar device may shunt the anode current around the SCR, causing it to switch to the blocking state. The second method of turning the SCR off can be eliminated from consideration here. It would require an additional SCR or transistor to switch the anode current; thus the logic block would, comparatively speaking, contain an excessive number of components. On the other hand, the first turn-off method, removal of anode voltage, merits closer consideration.

Let us agree to alternately remove and apply the anode voltage of the SCR at specific intervals of time and observe the output of the logic block only during the period of time the anode voltage is applied. A NOR circuit devised to operate on this scheme is shown in Fig. 33. The anode voltage generator V_A alternately applies and removes the anode voltage. Several voltage wave forms could be developed by the anode generator which would be alternately on and off. For example, a square wave would provide the necessary change. In Fig. 34 we illustrate the anode voltage wave shape and the times during which the output of the logic block will be valid. Let us take the anode voltage of the SCR to be zero at time T_0 as indicated. We will assume

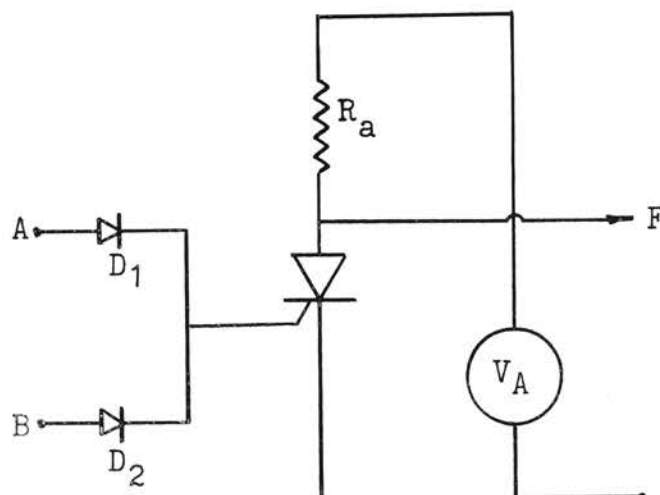


Fig. 33 Alternate Mode NOR Logic Block

the voltage of the input lines A and B to be zero at time T_1 when the anode voltage rises to the V_A level. As this voltage is not sufficient to turn the device on ($V_A < BV_F$) with no gate signal applied, a voltage will appear at the output during the period T_1 to T_2 . At some time T_a the gate voltage on line A will rise to the level V_G . If this gate voltage rise comes while the anode is at a low level, there will be no effect on the output. At time T_3 , however, the anode voltage will step to the level V_A and the SCR will switch to the on state. During the period T_3 to T_4 the gate voltage may fall to zero, time T_b , but the SCR will remain on if the anode current is greater than the holding current. At time T_4 the anode voltage will drop, turning the SCR off. The condition of the output from time T_5 to T_6 will again be determined

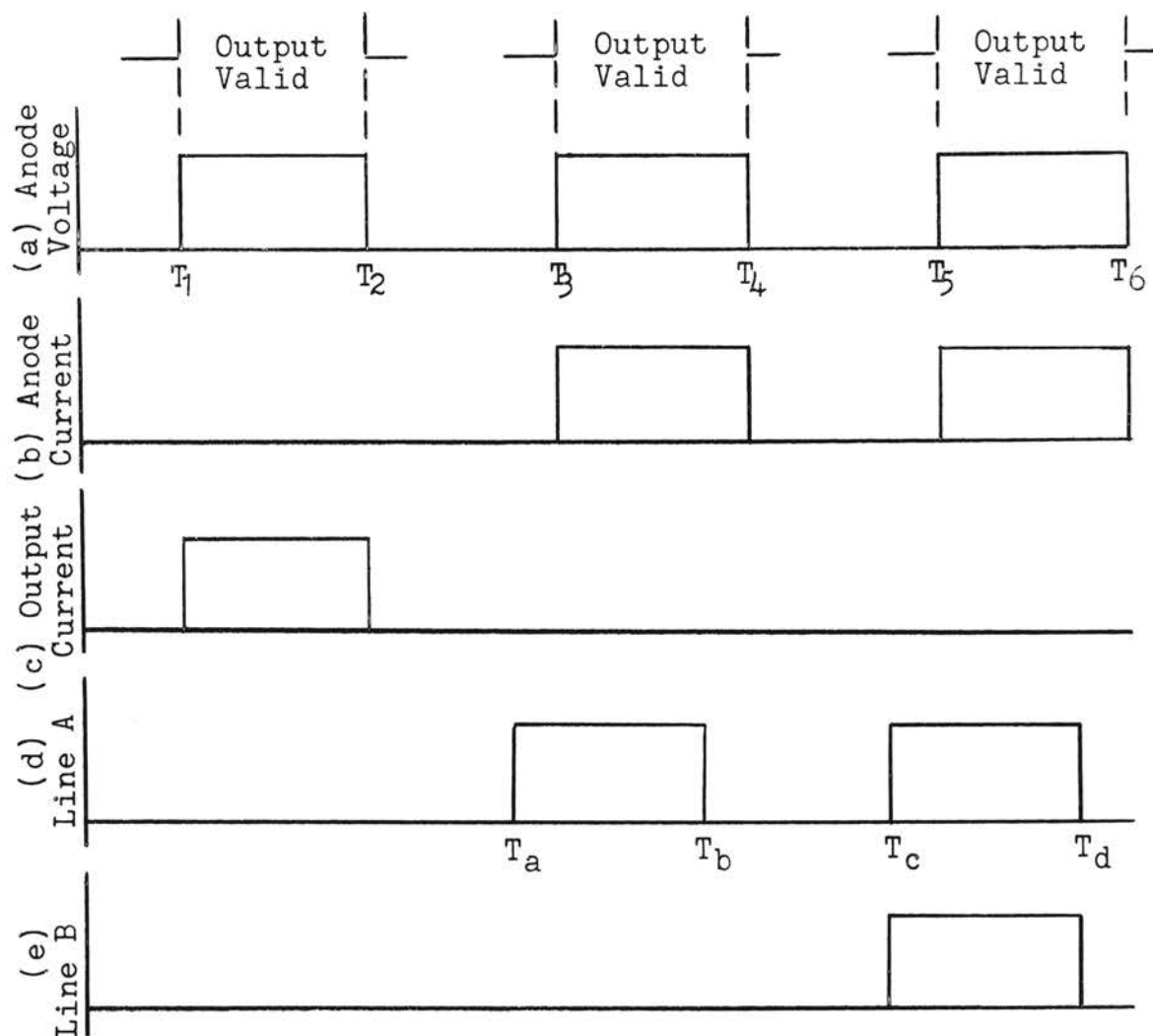


Fig. 34 Voltage and Current Waveforms of the Alternate Mode NOR Logic Block

by the signal of line A or B at time T_5 .

Referring to the circuit in Fig. 33 we see that an output appears at F only when lines A and B are in a 0 or "no signal" state. As with the circuits discussed previously this corresponds to the Boolean function

$$F = \bar{A} \times \bar{B} = A \downarrow B, \quad \text{Eq. 15}$$

the NOR function. This alternate mode logic block, then, is called a NOR block.

We have called the signals in Fig. 33 and 34 voltages. However we may, using the current mode of operation, call the current the signal. As the silicon controlled rectifier is more properly a current control device, this will be more convenient. If the anode resistance R_a is very large compared to the load, the logic block will be driven by essentially a constant current generator. The silicon controlled rectifier will serve to switch the current into the load if it is off or to the ground if it is turned on.

Waveform of the Anode Voltage Generator

At the present time the silicon controlled rectifiers available in production quantities are high current devices. A gate current from 10 to 20 ma is generally required to turn the SCR on. As a result, the anode voltage generator will be required to supply a relatively large amount of power to the alternate mode logic block.

We previously assumed the anode voltage generator to

be a square wave generator. However, the actual wave shape is relatively unimportant. Since a sine wave can be generated more easily than a square wave, it is natural to investigate the possibility of using a high power sine wave generator. If a sine wave is used as the anode voltage, the SCR will be reverse biased during the negative half of the cycle. The insignificant leakage current will have little, if any, effect on the circuit action. The load connected to the anode may present a problem in some cases. This will be considered in more detail later.

Perhaps we could extend the speed of the alternate mode logic circuit by shortening the interval during which the device is switched off. An investigation of the operation of this circuit using a full wave rectified sine wave was made. This voltage wave form was found to be satisfactory at low repetition rates and if the inductance and capacity of the circuit are negligible. However, as the frequency of the applied voltage is increased, the operation becomes less reliable. At a sufficiently high frequency the storage time of the SCR and any inductance present in the circuit (e.g., a transformer in the driving circuit) will prevent the anode current from dropping to zero. The SCR will not turn off and current will continue to flow in the anode-cathode circuit regardless of the state of the input signal. For this reason a full wave anode voltage is not recommended; we shall assume a complete sine wave to be used in the remainder of the discussion.

Analysis of Switching in the Alternate Mode Logic Block

The three direct mode logic blocks discussed in Chapter III were found to be unsatisfactory due to the limited number of outputs available from each logic block. The alternate mode logic block, on the other hand, can provide several output lines. The number of outputs available from the reverse biased block is limited by the anode current the reverse gate signal can turn off. As the alternate mode logic block does not rely on the reverse gate current to turn the SCR off, it is not restricted in this way. The limit to the number of output lines the alternate mode logic circuit can drive is set by the maximum anode current of the silicon controlled rectifier. When the SCR is switched on by a gate signal, the current that would normally flow through the load is switched to ground. The silicon controlled rectifier must be capable of carrying this current.

The number of input lines to the capacitor coupled logic block was limited by the lack of isolation between inputs. This problem is avoided in the alternate mode circuit, as in the reverse biased block, by isolating each line with a diode. This is shown in Fig. 33. The voltage level of one input line does not effect the presence of a current in another. For example, if a current is driven into line A while line B is shorted to ground by a conducting SCR, diode D_2 will be back biased and the current will flow

into the gate of the SCR as required.

The diodes also serve to prevent reverse current flow when the sine wave anode voltage generator swings into the negative half cycle. If the gates of the SCR were directly connected as the load of a logic block, a reverse gate current would flow during the negative half cycle. A large current could damage the silicon controlled rectifier. Thus the input diodes serve to protect the gate of the SCR from damage as well as to isolate the input lines of the logic block.

It is interesting to note the similarity of the input connection to the SCR and the diode OR logic circuit shown in Fig. 8. In fact the action is the same. The silicon controlled rectifier inverts and amplifies the output of the OR circuit.

To this time we have not considered the nature of the signals applied to the gate of the silicon controlled rectifier. If the alternate mode NOR logic block is to be considered a universal logic block, one stage must provide the proper signal to drive another stage. We previously considered the loading and isolation of the logic block and found that the alternate mode logic block performed satisfactorily. The next important consideration is the timing and shape of the applied gate signal.

The test circuit shown in Fig. 35 will be used to illustrate the voltage and current relations of the alternate mode NOR logic circuit. Silicon controlled rectifier C is

considered to be under test. A load similar to the load of an identical logic block is provided by R_L . The first two stages of the circuit are arranged to provide a gate signal for SCR-C identical to the output signal of an alternate mode logic block.

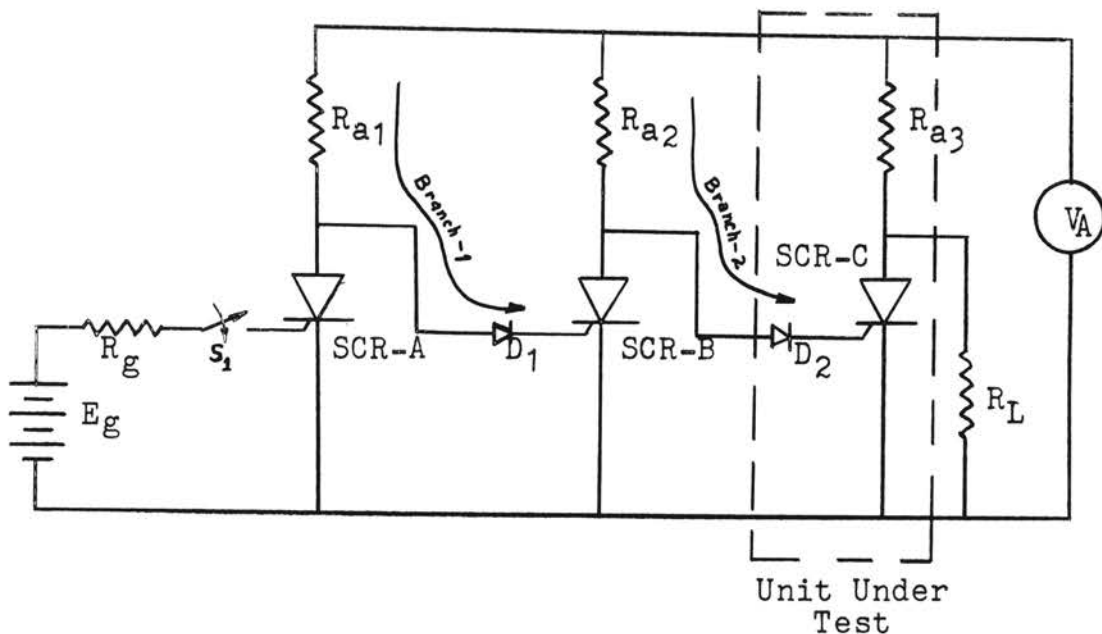


Fig. 35 Alternate Mode Logic Block Test Circuit

The voltage and current relations of test unit C are shown in Fig. 36. The generator voltage is shown at a and the other curves are referenced to this.

The first two cycles show the current voltage relations with no signal applied to the input line of C. Consider switch S_1 to be open and SCR-A in the high impedance state.

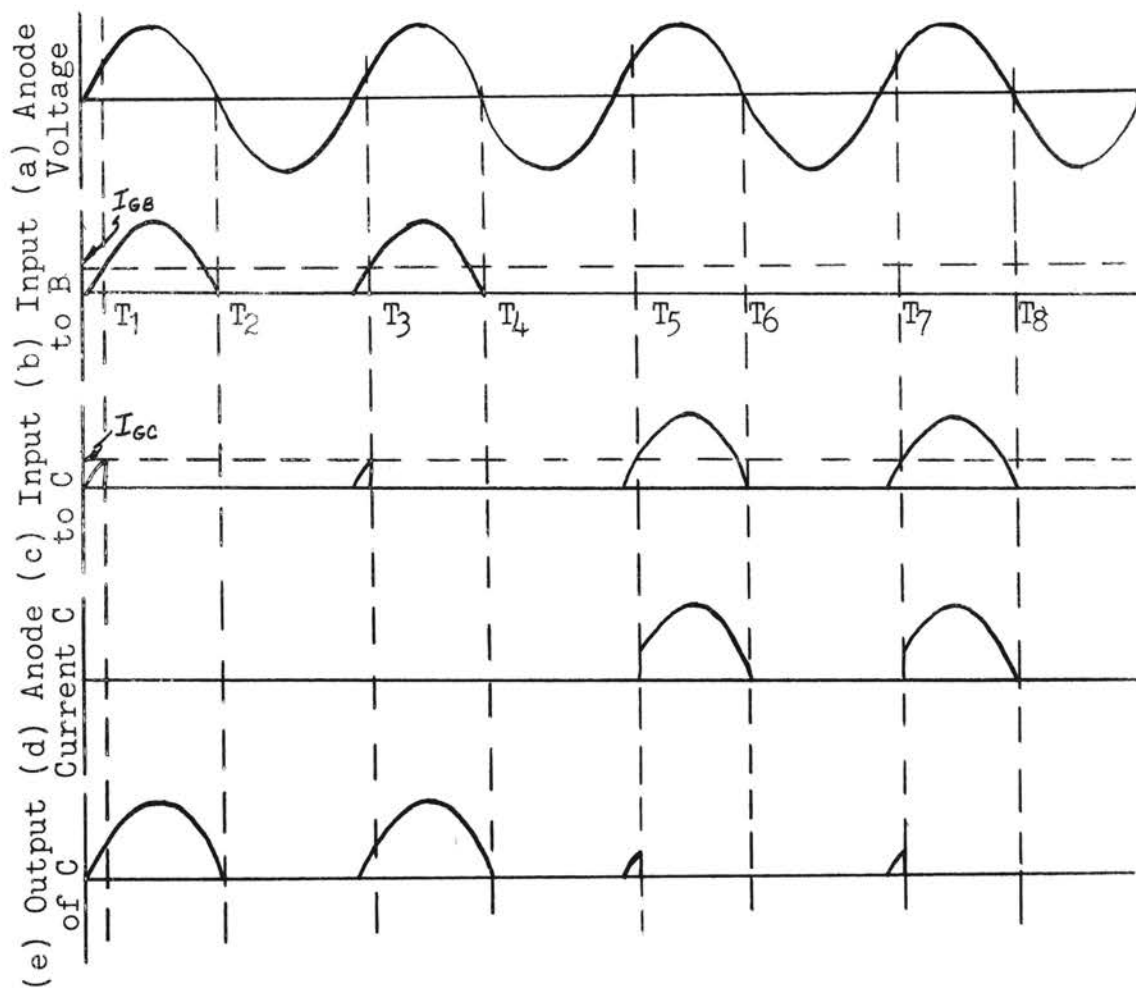


Fig. 36 Voltage and Current Waveforms of the Alternate Mode Logic Block - Sine Wave Anode Voltage

A half sine wave of current shown in b will flow through R_{a1} , D_1 , and the gate of SCR-B. Let us assume the turn-on current of SCR-B is I_{GB} and the gate current reaches this level at times T_1 and T_3 shown. When the gate current rises above I_{GB} , SCR-B will turn on and the output current of this unit, the gate current to SCR-C, will drop to zero as shown in c. As this gate current is insufficient to turn SCR-C on, its anode-cathode current will be zero (shown in d.) The resulting output current of SCR-C is shown in e.

If switch S_1 is closed, the action of the test circuit will be reversed. SCR-A will short diode D_1 to ground and no gate current will flow in SCR-B. Since SCR-B remains off during the positive half cycle, D_2 and the gate of unit C carry the current from R_{a2} . This is shown in c. If the turn-on current of SCR-C is I_{GC} , it will turn on at times T_5 and T_7 and the anode current shown in d will result. Under this condition the current in the load R_L is the relatively small current shown in e.

We consider the gate or input signal as well as the output signal to be valid only during the time T_1 to T_2 , T_3 to T_4 , T_5 to T_6 , etc. A signal \bar{A} at the input diode D_2 is indicated by the low current level during times T_1 to T_2 and T_3 to T_4 ; see curve c. The output of SCR-C carrying a current during the specified times is shown in e. Thus the output indicates A . This inversion property of the one input NOR logic block was described mathe-

matically in Chapter II.

We have presented a somewhat idealized picture of the circuit operation in Fig. 36. Actually an important problem regarding the universality of the logic block exists and will be discussed below.

We label the effective impedance of each diode R_d and the impedance of the gate-cathode path through the silicon controlled rectifier R_e . With good approximation it may be assumed that the impedance of the first branch shown in Fig. 35,

$$R_1 = R_{a1} + R_{d1} + R_{eB} , \quad \text{Eq. 16}$$

is equal to the impedance of the second branch,

$$R_2 = R_{a2} + R_{d2} + R_{eC} . \quad \text{Eq. 17}$$

This is permissible since R_{a1} equals R_{a2} , and R_a is very much greater than $R_d + R_e$.

Let us consider now the action of the circuit if the gate current required to turn SCR-B on, I_{GB} , is greater than I_{GC} . If the switch S_1 in Fig. 35 is open, all of the current through R_{a1} flows into the gate of SCR-B. At time T_0 both SCR's B and C will be off. As the generator voltage increases, equal currents will begin to flow in each branch of the circuit. After a short period of time the current in branch 2 will reach the level of the gate turn-on current I_{GC} , and SCR-C will switch to the conducting state. Since the turn-on current of SCR-B is greater than

I_{GC} , it will not switch on at this time. At some later time, however, the current in branch 1 will have reached the level I_{GB} and SCR-B will then switch to the conducting state. Note that now there is no input and no output to the test NOR logic block, SCR-C. This violates the NOR logic operation on one variable and the circuit fails.

In reality this problem is not as serious as it may first appear. A group of silicon controlled rectifiers were tested in the laboratory to determine the gate current required to switch them on in a circuit similar to that in Fig. 35. From this group units were selected having I_G 's of 10 ma to 15 ma. The selected units were then placed at random in a logic circuit composed of seven blocks. The circuit functioned perfectly, despite the fact that several of the NOR blocks were preceded by stages having higher gate current requirements as described in the previous paragraph.

There are two reasons the test circuit functioned properly. In the first place, the output current of each stage is "softened" by the turn-on characteristics of the silicon controlled rectifier. And secondly, the relatively long turn-on time of the silicon controlled rectifier may prevent improper switching in certain cases. Both of these phenomena will be discussed in detail below.

The volt-ampere characteristic for a typical TI-118 silicon controlled rectifier is shown in Fig. 37a. This curve differs from that in Fig. 21b since the horizontal

and vertical scales have been expanded several times. We see from the curve for $I_G = 10$ ma that an anode current of about 3 ma flows through the device before it assumes the forward blocking state. This causes the output current of the SCR-B to be "softened," i.e., does not allow the current to reach the level predicted previously.

The output current we are concerned with is the current through the diode D_2 and the gate cathode path of SCR-C shown in Fig. 35. The series combination of the diode and the gate of the following stage is a nonlinear resistance in parallel with the volt-ampere characteristic of SCR-B. The diode and gate volt-ampere characteristic is plotted in Fig. 37a. Using conventional nonlinear circuit graphical analysis technique, we sum the voltage drop across each element for a fixed current. The resulting composite curve is shown in Fig. 37a.

The volt-ampere characteristic for the parallel combination of the SCR and the composite curve is drawn in Fig. 37b. This was obtained by selecting a particular voltage and summing the current through the SCR and the nonlinear load.

We have, for this example, selected the anode resistance R_a to be 10 k ohms and the peak anode voltage to be 150 volts. Note the resistance R_a is very much greater than the effective impedance of the parallel combination of SCR-B and its load. Thus R_a and E_a may be assumed to be a constant current generator. The current of this gen-

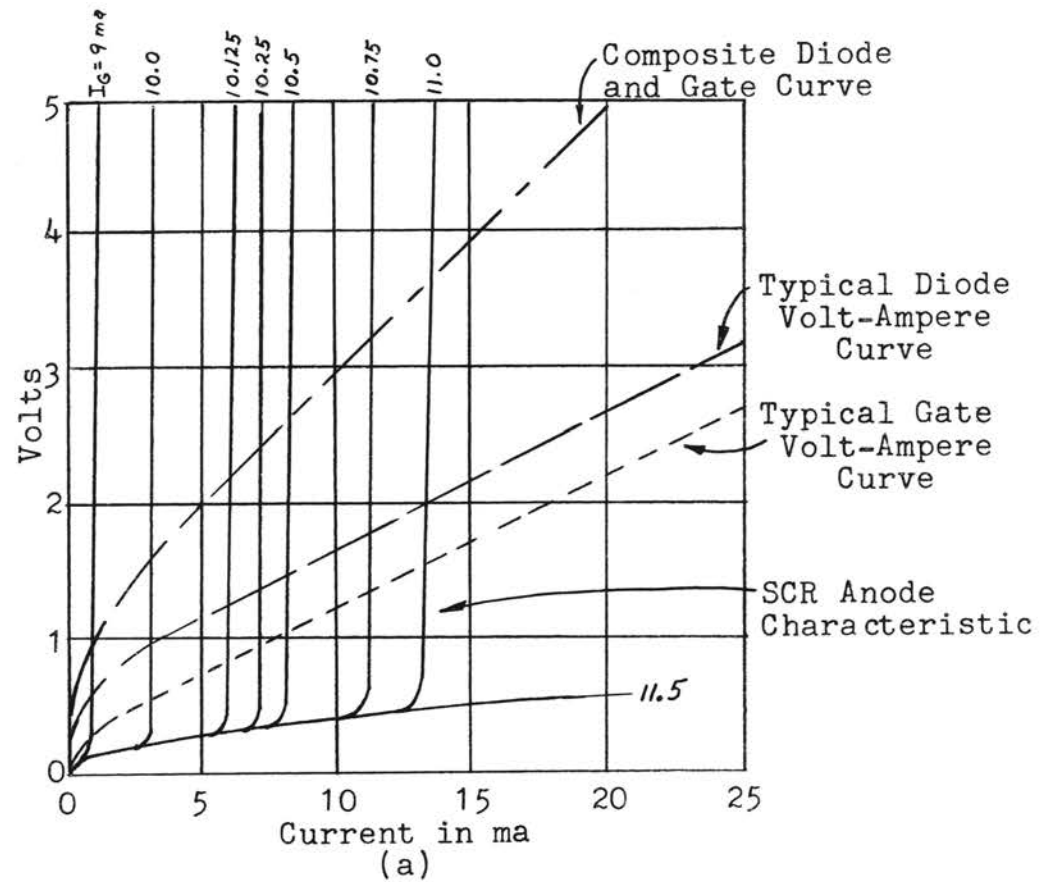


Fig. 37 Volt-Ampere Curve of the Silicon Controlled Rectifier and the Nonlinear Load

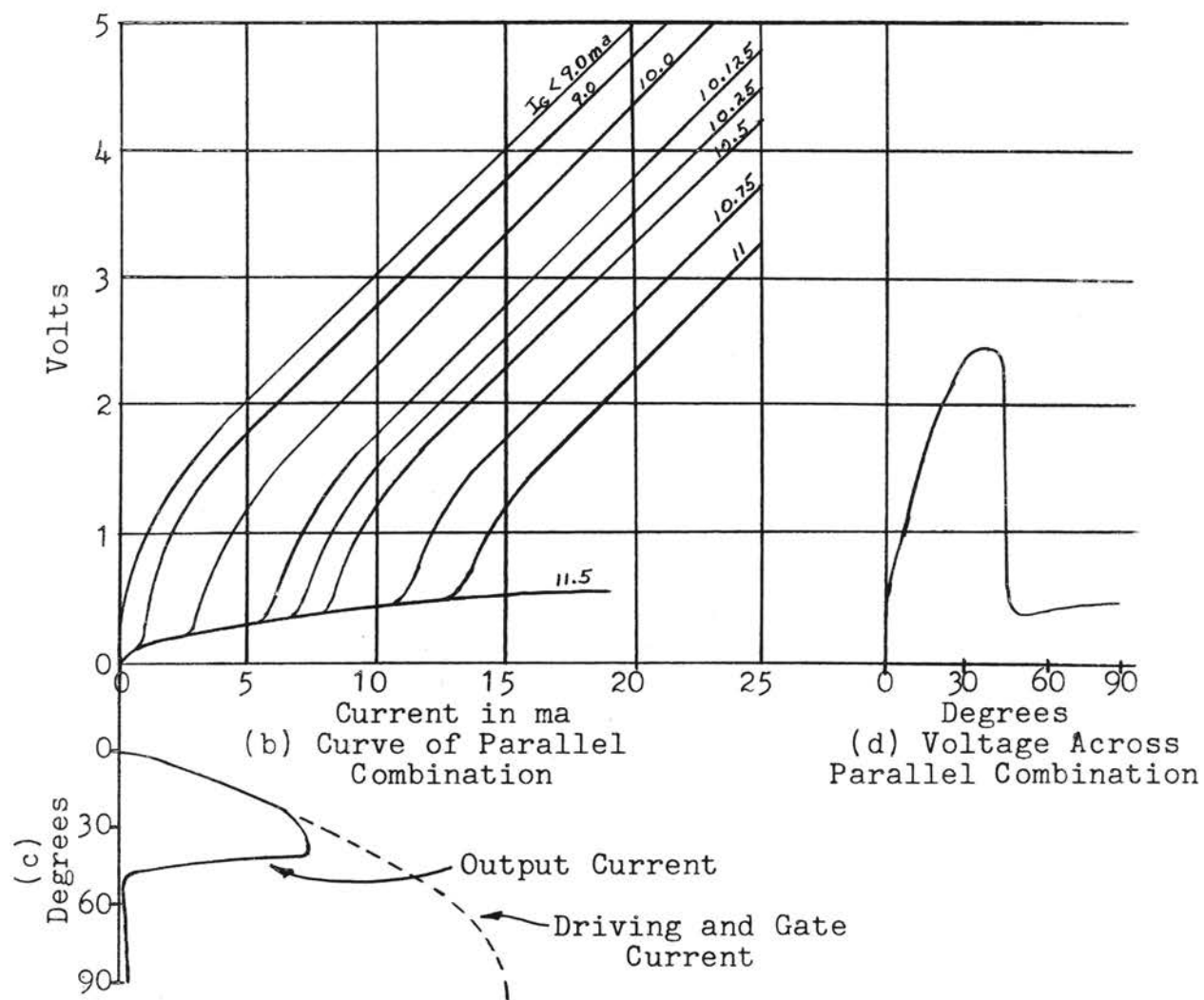


Fig. 37 Volt-Ampere Curve of the Silicon Controlled Rectifier and the Nonlinear Load

erator is shown in Fig. 37c. Only the first 90° of the cycle is plotted since we are interested in the turn-on characteristic.

Since SCR-A is assumed to be in the forward blocking state (S_1 open), a current identical to the driving current described previously will flow into the gate of SCR-B.

The voltage across SCR-B and its load is obtained in the following manner. For a given angle, say 40° , we obtain the value of the gate and driving current from Fig. 37c. We find the corresponding point on the curve in Fig. 37b. The voltage across the parallel combination is then read from the abscissa and plotted in Fig. 37d.

The output current, the current through diode D_1 and the gate of SCR-C, is now obtained from the composite curve in Fig. 37a and the voltage across the parallel combination. The output current is shown in Fig. 37c.

The important fact here is that SCR-B has a turn-on current of about 11 ma. However, the peak current in the output line is seen to be 7.5 ma rather than the 11 ma predicted by the ideal picture of the silicon controlled rectifier. This specific example indicates that the gate current required to trigger the following logic block could have been 80% of that of the driving circuit, and the system would have functioned properly.

It is difficult to correlate the leakage current of the silicon controlled rectifier with the turn-on current of the unit. Consequently, it is also difficult to deter-

mine the maximum tolerance in gate current that will allow universal interchange of NOR logic blocks. However, tests on a number of units in the laboratory indicate that if the gate switching currents fall within a $\pm 10\%$ range, the alternate mode logic block will operate satisfactorily.

In addition it may be possible to extend the range of the gate current if the finite turn-on delay time of the device is utilized. Let us examine in more detail the action of SCR-C in Fig. 35 during the initial part of the cycle.

Fig. 38a shows the gate current of SCR-C. We note that the wave shape has been idealized from that indicated in Fig. 37c. However, the fact that the current is not softened will improve the validity of our analysis. Thus we have chosen the "worst case" and shall proceed on this basis.

The gate current shown in Fig. 38a is part of a sine wave of current between the start of the cycle T_0 and the time at which SCR-B turns on, T_2 . Thus the peak gate current in SCR-C, I_{G2} , is given by:

$$I_{G2} = \frac{E_a}{R_{a2} + R_{d2} + R_{e2}} \sin \omega T_2$$

$$= I_{a2} \sin \omega T_2 \quad \text{Eq. 18}$$

The time T_2 is the time at which the current in branch 1 of Fig. 35 reaches the gate turn-on current I_{GB} of SCR-B. This is expressed by the relation:

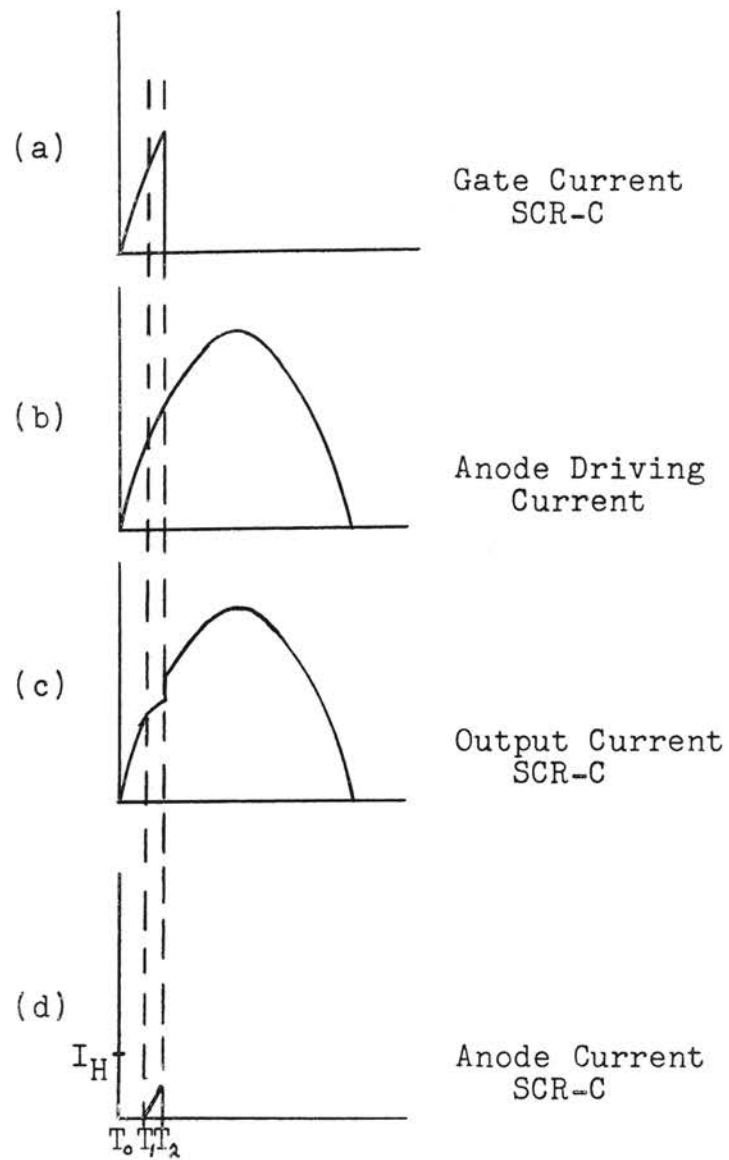


Fig. 38 Effect of SCR Delay Time on Alternating Current Mode Logic Block

$$\begin{aligned}
 I_{GB} &= \frac{E_a}{R_{a1} + R_{d1} + R_{e1}} \sin \omega T_2 \\
 &= I_{a1} \sin \omega T_2
 \end{aligned}
 \tag{Eq. 19}$$

However, at time $T_1 < T_2$ the current in branch 2 is assumed to be equal to the turn-on current of SCR-C, I_{GC} . This time is given by:

$$\begin{aligned}
 I_{GC} &= \frac{E_a}{R_{a2} + R_{d2} + R_{e2}} \sin \omega T_1 \\
 &= I_{a2} \sin \omega T_1
 \end{aligned}
 \tag{Eq. 20}$$

At time T_1 silicon controlled rectifier C begins to turn on. However, the finite delay time in switching to the conducting state causes the anode current to rise slowly at first, as shown in Fig. 38d. If the anode current shown does not reach the holding current level, the device will switch off at time T_2 when the gate current drops to zero.

The delay time of the silicon controlled rectifier is defined as the time required for the anode current to change from zero to 10% of its final value and is labeled T_d in Fig. 24. The holding current will generally be much greater than 10% of the maximum anode current in this NOR logic block. Thus we may assume that if

$$T_2 - T_1 < T_d \tag{Eq. 21}$$

the silicon controlled rectifier will not switch on. Re-

writing Equations 19 and 20 and applying Maclaurin's series expansion for the inverse sine, we have:

$$T_1 = \frac{1}{\omega} \sin^{-1} \frac{I_{GC}}{I_{a_2}} = \frac{1}{\omega} \left[\frac{I_{GC}}{I_{a_2}} + \frac{1}{6} \left(\frac{I_{GC}}{I_{a_2}} \right)^3 + \dots \right] \quad \text{Eq. 22}$$

$$T_2 = \frac{1}{\omega} \sin^{-1} \frac{I_{GB}}{I_{a_1}} = \frac{1}{\omega} \left[\frac{I_{GB}}{I_{a_1}} + \frac{1}{6} \left(\frac{I_{GB}}{I_{a_1}} \right)^3 + \dots \right] \quad \text{Eq. 23}$$

Thus:

$$T_2 - T_1 = \frac{1}{\omega} \left\{ \frac{I_{GB}}{I_{a_1}} - \frac{I_{GC}}{I_{a_2}} + \frac{1}{6} \left(\left[\frac{I_{GB}}{I_{a_1}} \right]^3 - \left[\frac{I_{GC}}{I_{a_2}} \right]^3 \right) + \dots \right\} \quad \text{Eq. 24}$$

Since the current ratios are always less than one, we may neglect the higher order terms and have:

$$T_2 - T_1 \approx \frac{1}{\omega} \left(\frac{I_{GB}}{I_{a_1}} - \frac{I_{GC}}{I_{a_2}} \right) \quad \text{Eq. 25}$$

Thus if the logic block is to function properly:

$$T_d > \frac{1}{\omega} \left(\frac{I_{GB}}{I_{a_1}} - \frac{I_{GC}}{I_{a_2}} \right) \quad \text{Eq. 26}$$

We stated at the outset of this discussion that we would assume the impedance of branch 1 and branch 2 to be equal. If this is the case, we see that

$$I_{a_1} = I_{a_2} \quad \text{Eq. 27}$$

and Equation 26 will simplify to:

$$T_d > \frac{I_{GB} - I_{GC}}{\omega I_{a_1}} \quad \text{Eq. 28}$$

Equation 28 points up the fact that increasing the current I_a and the frequency of the anode driving voltage increases the reliability of the alternate mode logic block.

Laboratory tests of the analysis presented above verified the theory. However, a significant increase in the tolerance of the gate turn-on current sought here was not observed.

The circuit shown in Fig. 39 was set up in the laboratory using the equipment listed below.

Anode voltage generator

Hewlett Packard Audio Oscillator - Model 200 AB

Heath Co. 70 watt Power Amplifier - Model W-6M

A Hewlett Packard Model 456A a.c. current probe in conjunction with a Textronix 515A oscilloscope was used to monitor the current wave form in the load. Since the input was assumed to be in the 0 state at all times, the shape of the load current wave form indicated whether the logic block was functioning properly or not.

A silicon controlled rectifier having a gate switching current of 9.1 ma was used for SCR-C. Units having gate turn-on currents from 11.75 to 19 ma were tested in the SCR position B.

The silicon controlled rectifier requiring a gate current of 11.75 ma to fire was found to operate at all frequencies from 20 cps to 6 kc with an anode resistance R_{a1} of 7 k ohms. This corresponds to the desirable 'universal circuit.' Since the circuit operated satisfactorily over

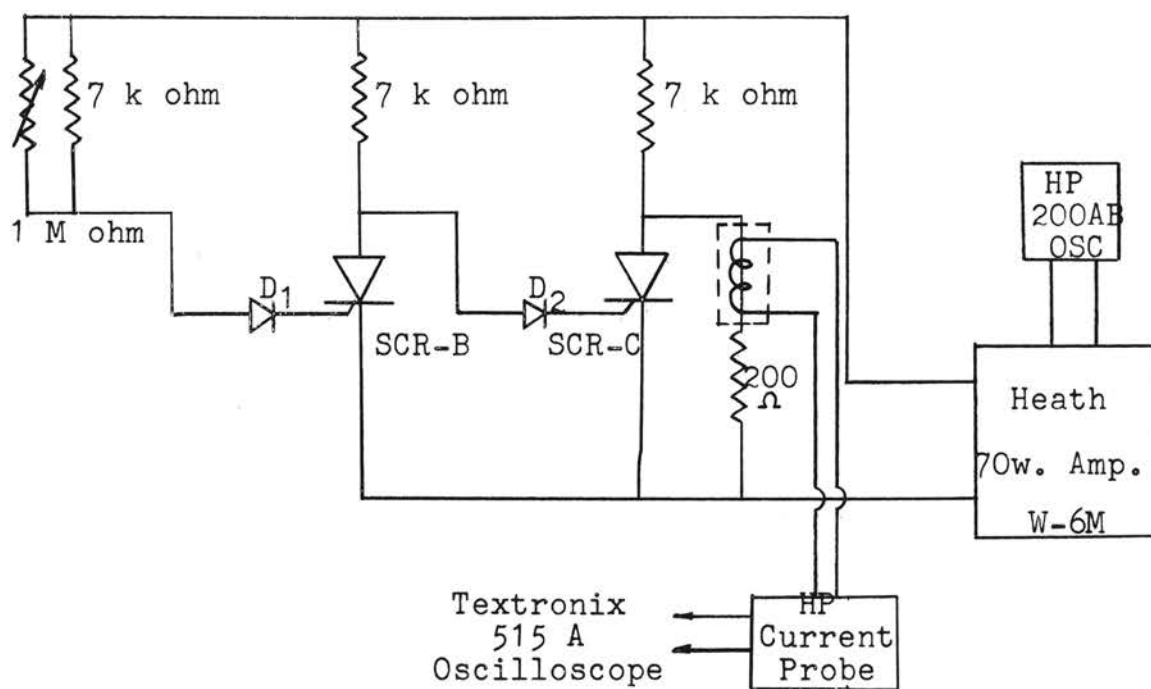


Fig. 39 Alternate Mode Logic Block
Laboratory Test Circuit

a wide frequency range, it was concluded that the delay time required to switch the unit to the conducting state actually had no effect in this case.

A second unit having an I_{GB} of 13.7 ma was tested, and different results were obtained. With R_{a1} set at 7 k ohms as before the circuit was observed to "mis-fire" at all frequencies from 20 cps to 6 kc. However, when R_{a2} was reduced to 6 k ohms, the result predicted by Equation 26 was observed. At a low frequency the time $T_2 - T_1$ was longer than the delay time T_d and SCR-C fired, causing the logic block to fail to function properly. As the frequency was increased, the time $T_2 - T_1$ decreased as predicted by Equation 25. At a sufficiently high frequency, F_0 , $T_2 - T_1$ was less than the delay time T_d and the logic block functioned properly. Further tests proved that as the driving current I_{a1} increased, the frequency at which $T_2 - T_1$ was less than T_d decreased as indicated in Equation 25. The results of the test for two values of anode resistance and various anode voltages are shown in Table IV. The tests on the other units gave similar results.

At the frequency F_0 the time $T_2 - T_1$ is barely less than the delay time T_d , and Equation 25 may be used to approximate the delay time of the silicon controlled rectifier. The time calculated in this manner is consistent with that determined by other methods.²⁰

²⁰Ibid.

TABLE IV
ALTERNATING CURRENT MODE DELAY TIME CHARACTERISTICS

R_{a_2}	R_{a_1}	E_a	I_{a_1}	I_{a_2}	F_o	I_{GB}/I_{a_1}	I_{GC}/I_{a_2}	T_d
k ohms		vrms	ma		kc			μs
7.0	6.0	100	23.6	20.2	3.9	0.497	0.450	1.92
7.0	6.0	120	28.2	24.2	3.2	0.416	0.376	1.99
7.0	6.0	140	33.0	28.2	2.8	0.356	0.322	1.95
7.0	6.0	160	37.7	32.2	2.5	0.312	0.282	1.91
7.0	5.5	100	25.7	20.2	0.82	0.457	0.450	1.36
7.0	5.5	120	30.9	24.2	0.72	0.380	0.376	0.89
7.0	5.5	140	36.0	28.2	0.65	0.326	0.322	0.98
7.0	5.5	160	41.2	32.2	0.57	0.286	0.282	1.12

The delay time of the silicon controlled rectifier is a function of the gate current, the anode voltage, and the temperature of the unit. This fact accounts for the variation in the calculated values since the anode voltage and gate current changed during the test.

As it was necessary to reduce the anode resistance R_{a_2} to observe the delay time effect, no decisive conclusions can be drawn with regard to an increase in the gate current tolerance. To extend this analysis let us assume the delay time of the silicon controlled rectifier to be $1 \mu \text{ sec}$. If we take I_{a_1} to be 30 ma and I_{GC} to be 9.1 ma, Equation 28 becomes

$$1 \times 10^{-6} > \frac{I_{GB} - 9.1 \times 10^{-3}}{\omega (30 \times 10^{-3})} \quad \text{Eq. 29}$$

or

$$\begin{aligned}
 I_{GB} &< \omega (1 \times 10^{-6})(30 \times 10^{-3}) + 9.1 \times 10^{-3} \\
 &< F(0.19 \times 10^{-6}) + 9.1 \times 10^{-3}
 \end{aligned}
 \tag{Eq. 30}$$

Taking the frequency F to be 15 kc, we have:

$$\begin{aligned}
 I_{GB} &< (15 \times 10^3)(0.19 \times 10^{-6}) + 9.1 \times 10^{-3} \\
 &< 11.95 \text{ ma}
 \end{aligned}
 \tag{Eq. 31}$$

However, the silicon controlled rectifier used in the tests above had an I_G of 11.75 ma; it was found to function properly when $R_{a1} = R_{a2}$ at all frequencies. Thus no significant increase in the gate current tolerance is realized.

It is not practical to increase the frequency of the anode voltage much above 5 kc since the delay time of the silicon controlled rectifier becomes too great a part of the cycle. When this happens, the time during which the output is valid becomes very short and the alternate mode logic block lacks the necessary reliability.

An Application of the Alternate Mode Logic Block

A common logic system found in electronic computers is the half-adder.²¹ The name half-adder is used to indicate that only two binary numbers are summed. A full adder, on the other hand, is a more complicated system summing two

²¹Flores, pp. 150-152.

numbers and a carry. The truth table for the binary summation is indicated in Fig. 40a.

S	A	A
B	0	1
B	1	0

(a)

K	A	A
B	1	0
B	0	0

(b)

Fig. 40 Truth Tables for Summation of Two Binary Numbers

Note in Fig. 40b that when 1 and 1 are summed, the result is 0 with 1 carried to the next place. The half-adder circuit has an output line corresponding to the carry.

The sum output of the half-adder S may be represented by the Boolean function:

$$S = (A \times \bar{B}) + (\bar{A} \times B) \quad \text{Eq. 32}$$

This is the exclusive OR function described previously. Its function may be written in a more suitable form by applying DeMorgan's theorem:

$$S = \overline{(A \times \bar{B}) \times (\bar{A} \times B)} \quad \text{Eq. 33}$$

Using Equation 3 we may rewrite the above result using only the NOR and complement operation:

$$S = \overline{(\bar{A} \downarrow B) \downarrow (A \downarrow \bar{B})} \quad \text{Eq. 34}$$

The Boolean function,

$$K = A \times B \quad \text{Eq. 35}$$

expresses the proper operation on A and B to produce the carry signal. Again applying DeMorgan's theorem and re-writing the equation in terms of NOR logic, we have:

$$K = \overline{A + B} = A \downarrow B \quad \text{Eq. 36}$$

A block diagram indicating the operation to be performed on each variable A and B is shown in Fig. 41. Each NOR block may now be replaced by an alternate mode NOR logic block as shown in Fig. 42.

This circuit was tested in the laboratory using silicon controlled rectifiers of type TI-118. Units having gate turn-on currents from 9.0 to 11.0 ma were selected. Assuming a mean value of gate switching current of 10 ma and recognizing that a maximum of two output lines were required, the peak anode current for each unit was selected to be 30 ma. This was found to allow the SCR to fire early in the cycle and thus provide sufficient 'valid output' time to indicate reliably the state of the output line. An anode resistance of 7 k ohms and voltage of 150 vrms was found to provide the necessary current peak.

The output circuit shown in Fig. 42 was devised to indicate the presence of a 1 or a 0 on the output line. The circuit performed exactly as specified by the half-adder truth tables in Fig. 40.

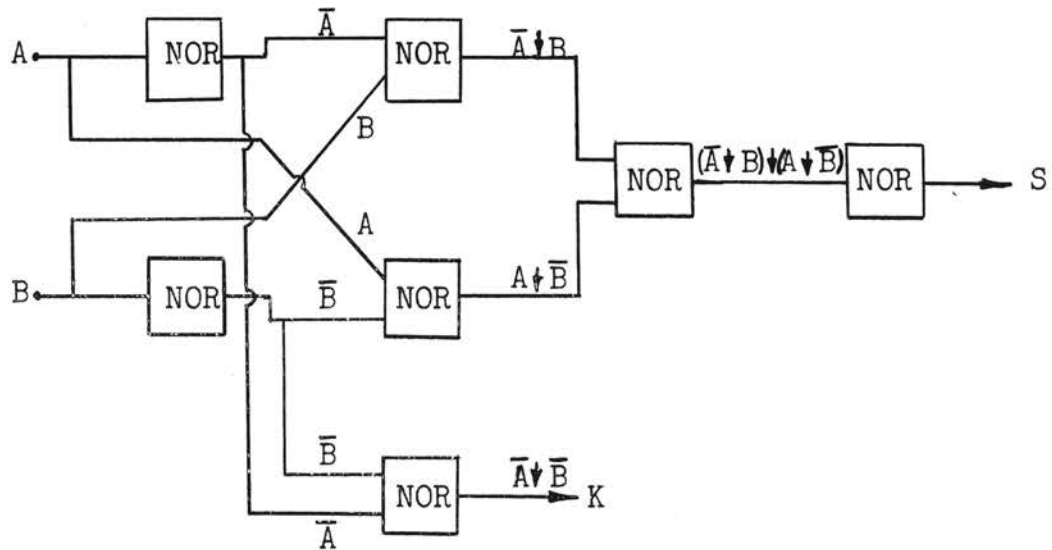


Fig. 41 Block Diagram of Half-Adder

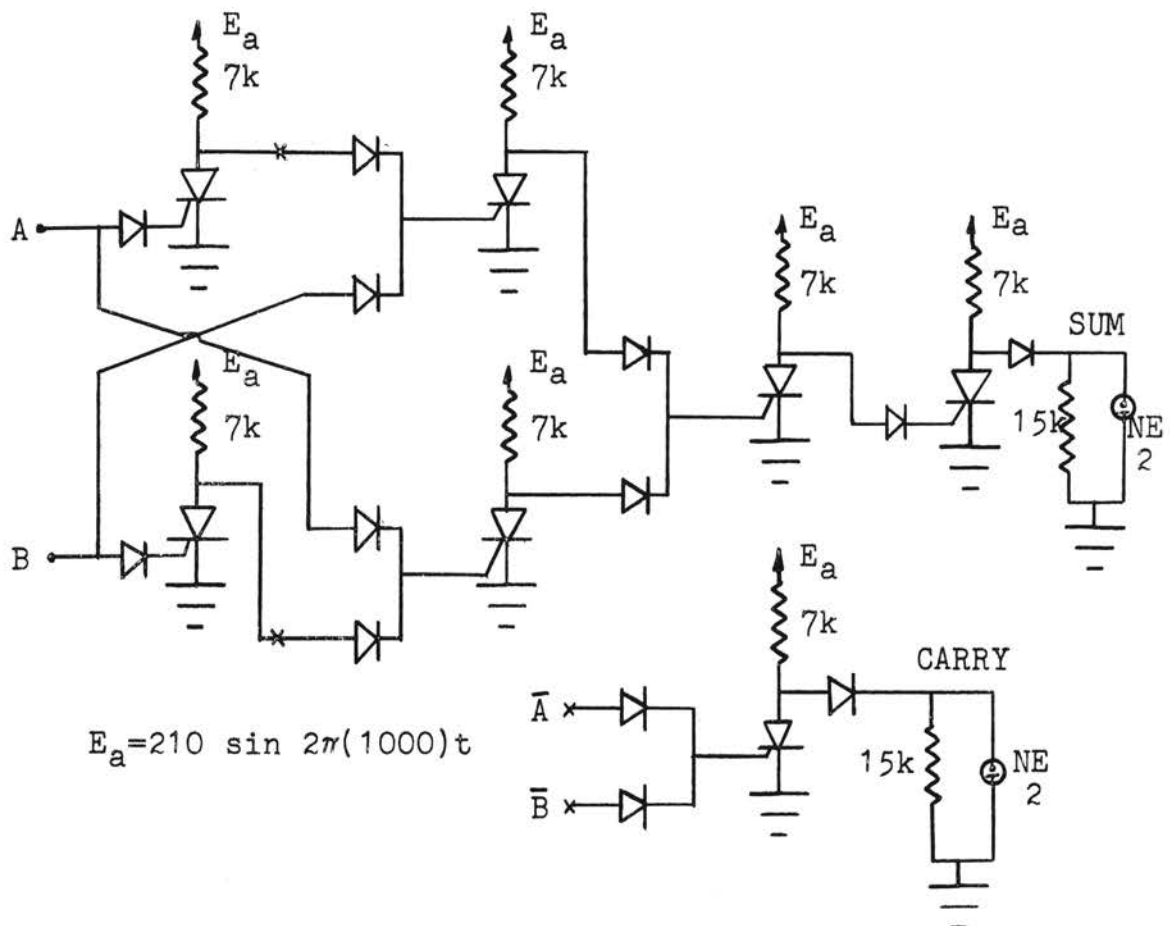


Fig. 42 Alternate Mode Logic Block Half-Adder Circuit

CHAPTER VI

CONCLUSION

The main objective of this study, stated in Chapter I, was to investigate the feasibility of a silicon controlled rectifier logic block. It was necessary first, however, to define the logic operations to be performed by the logic block and discuss the form of logical mathematics, Boolean algebra. It was shown in Chapter II that all of the logical operations could be performed by one function, the NOR function. The NOR logic circuits used in computers and control equipment were also discussed, and a list of the requirements of a logic block was presented.

The characteristics and ratings of the silicon controlled rectifier were presented in Chapter III, followed by a discussion of several direct mode logic systems. As pointed out in Chapter IV the capacitor coupled NOR logic block could provide only one output and input line, and the holding current logic block had a maximum of one output line. It was indicated there, however, that if silicon controlled rectifiers with high turn-on and turn-off gains become commercially available, the reverse gate bias NOR logic block could prove to be practical as a solution for the first objective.

The theory of the alternate mode logic block was presented in Chapter V. It was described as fulfilling all of the requirements of a logic block with the possible exception of the universality criterion. Subsequently, it was shown that if certain restrictions were placed on the characteristics of the silicon controlled rectifier, the alternate mode NOR block would be a universal logic block. To illustrate an application of the alternate mode NOR logic block, a half-adder was described.

It may be concluded that the alternate mode NOR logic block is a feasible solution to the first objective. Several factors influencing the design of this logic block were discussed. It was indicated that the upper limit to the speed of the operation of this logic block is the delay time of the silicon controlled rectifier.

There are a number of matters associated with the alternate mode logic block which require additional study. It would certainly be useful to determine with more precision the range of gate turn-on characteristics of silicon controlled rectifiers suitable for a universal logic block. In addition, a detailed study of the design of the SCR, keeping in mind the requirements of this particular application, could lead to a unit that would improve the circuit substantially. In particular the power requirements of the SCR NOR logic block are excessive. Sufficiently lowering the gate currents required to turn the device on could make the SCR logic block comparable in power requirements to the "milli-

watt" transistor circuits.

One suggestion for future study was that the Zener diode might be used in the gate lead of the SCR to increase the reliability of the circuit and to utilize units with a greater range of gate turn-on currents.

An alternate mode logic system utilizing a multi-phase anode voltage would be another topic for investigation. Here the anode voltage of one logic block would lead that of the following block. This system could eliminate the universality problem of the alternate mode circuit.

It appears that the alternate mode NOR logic block could presently fulfill the need for a reliable medium or slow speed logic block. Perhaps, then, at some future date the silicon controlled rectifier will be used to perform the logic functions in a machine control system as well as to rectify the current to drive the motors of the machine.

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