A BIDIRECTIONAL SHIFT REGISTER

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PREFACE

This paper is concerned with some of the problems encountered in building a low-power bidirectional shift register. The specifications set forth for the shift register are that it must be capable of shifting in either direction, with or without recirculation, at speeds up to 20 kc.

I would like to express my appreciation to my advisor, Paul A. McCollum for his extra interest and advise on this project.

Also, I would like to express my thanks to Bobby E. Baker and Arno L. Lindorfer for their advise on improving the experiment and thesis. I would also like to express my indebtedness to my former employer, Larry Labarthe, for his past assistance in circuit design. I would like to express my thanks to Kathy Mulholland for helping draw the figures included in this thesis.

Last of all, my deepest gratitude belongs to Liz. My desire to both start and finish a Master's program was gained from her.

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CHAPTER I

SHIFT REGISTER PURPOSES

The basic utilization of a shift register is to accept data in either series or parallel form and to shift it out in either series or parallel form. This thesis will be concerned only with parallel input-series output, and series input-series output. Generally the data is of binary form or to the base two; therefore, a binary, core, or some other two state device can be used to store the data.

A simplified block diagram of a series output shift register is shown in Figure 1. Assume that the shift register is connected to

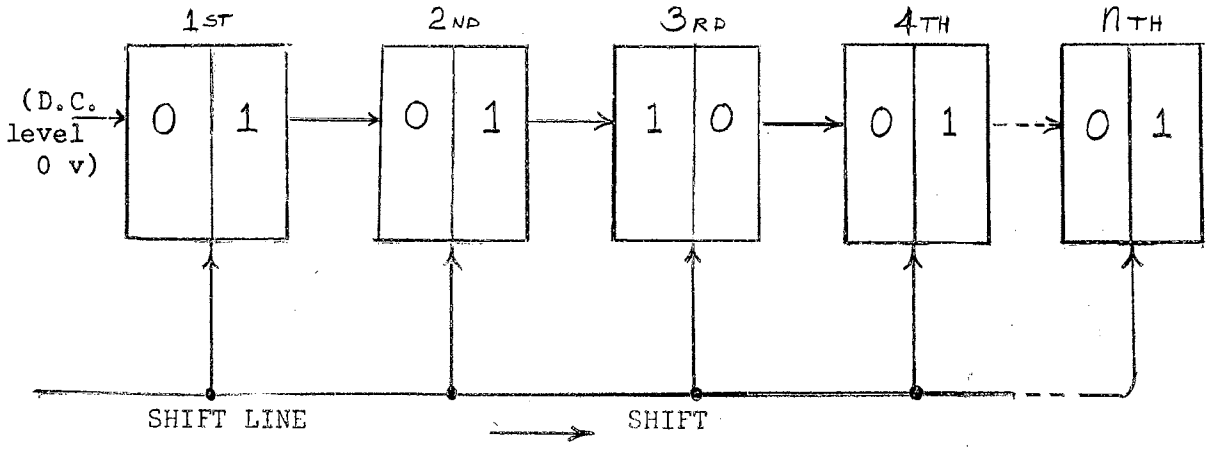


Figure 1. Simplified Block Diagram of Series Output Shift Register

shift to the right. As each shift pulse arrives, the data of the preceding binary is shifted to the right. This is shown in Table I.

TABLE I

TRANSFER OF DATA TO THE RIGHT

Rest	1	1	0	1
First Shift	0	1	1	0
Second Shift	0	0	1	1
Third Shift	0	0	0	1

It can be seen that after the first shift pulse arrives, the data that was in the third binary is in the fourth binary. Likewise, after the second shift pulse arrives, the data that was in the second binary is in the fourth binary. If there were n binaries, it would take (n - 1) shift pulses to make the data from the first binary appear in the n^{th} binary.

Also, after (n - 1) shift pulses (three in this case), the last column is identical to the first row. It is this unique property that gives the series shift register its primary value. Instead of monitoring the output of each binary separately, it is only necessary to monitor the output of the last binary. Furthermore, the data can be handled one bit at a time.

CHAPTER II

PURPOSE OF DELAY

Before going any further, one possible question should be answered. Assume that the new binary conditions are reached instantaneously. Referring to Figure 1, when a shift pulse appears, the fourth binary will assume the condition of the third binary. The third binary is (1 0), but on the same shift pulse will change to (0 1).

The question is, how does the fourth binary know whether to assume the old condition or the new condition corresponding to that of the third binary? One method of solving this problem is to employ delays between the binaries. The binaries will still change states instantaneously, but the effects of the change will not be felt in the following binary until after the shift pulse has ended. This is illustrated in Figure 2.

From Figure 2 it can be seen that the width of the shift pulse and the time of delay are related. For instance, if the shift pulse suddenly became three times as wide, the delay would not be long enough. However, in order to make the shifting action as fast as possible, the delay must be kept small forcing the width of the shift pulse to be even smaller. But since an extremely narrow shift pulse is achievable, this will not cause any difficulties. Instead, the limit will be set by the regeneration time of the binaries. Once the pulse becomes too

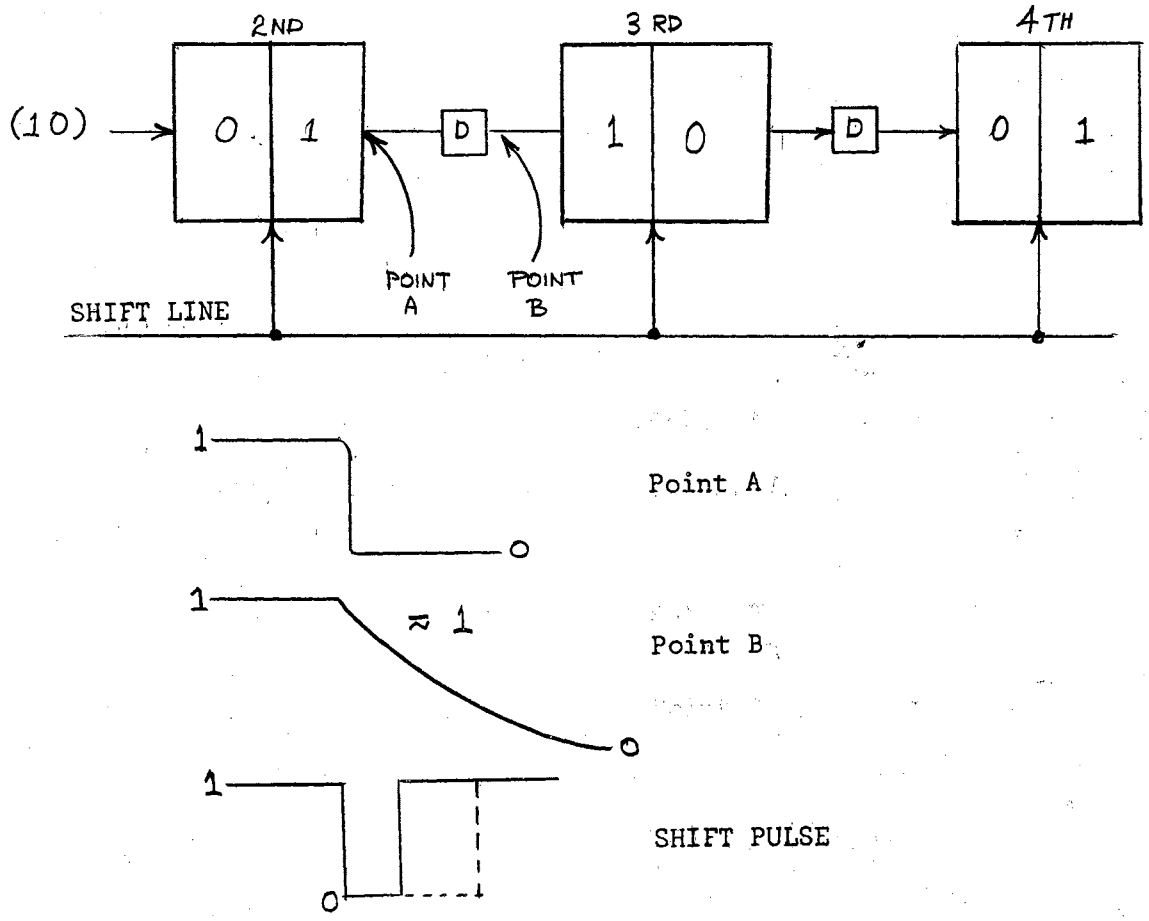


Figure 2. Simplified Block Diagram of Series Output Shift Register with Delays

narrow, the binaries will not safely regenerate.

Another method of solving this problem is to employ an additional binary per stage to act as a temporary storage. It has the disadvantage of requiring considerable more components. This method is discussed by R. K. Richards (1958) and in other books.

CHAPTER III

ARITHMETICAL EFFECT OF SHIFTING

The effects of shifting to the left and to the right are illustrated in Table II. As can be seen from Table II, a shift of one place

TABLE II

ARITHMETIC EFFECT OF SHIFTING DATA BOTH DIRECTIONS

	Shift Right								Shift Left							
Rest	0	0	0	1	1	0	1	(13)	0	0	0	1	1	0	1	(13)
First Shift	0	0	0	0	1	1	0	(6)	0	0	1	1	0	1	0	(26)
Second Shift	0	0	0	0	0	1	1	(3)	0	1	1	0	1	0	0	(52)
Third Shift	0	0	0	0	0	0	1	(1)	1	1	0	1	0	0	0	(104)

changes the effective value of the number stored by the power of 2.

Shifting to the right causes the number to be divided by 2 with each shift. By knowing the number of shifts, the original number can be known within ± 1. In other words, shifting to the right causes loss of the least significant bit, and the number remaining will in many cases be sufficiently accurate.

Shifting to the left causes the number to be multiplied by 2 with each shift. If a digit is lost due to shifting, it will be the most significant bit. Referring to Table II, if a fourth shift pulse

occurred, the most significant bit would not have a place to be stored, and the number 1 1 0 1 0 0 0 (104) would be changed to 1 0 1 0 0 0 0 (80).

Therefore, a limit must be placed on the number of shifts depending upon the locations of the least and most significant bits and the accuracy required.

The outstanding feature of most shift registers is that the rate of output is independent of the rate of input, and vice versa. This is possible since the data is held in static storage. Therefore, data can arrive at random and then be shifted out at random. For example, data could be accumulated from a magnetic tape at a relatively slow rate, and then could be shifted out at a much faster rate.

It should be reiterated that random input and output of data is only possible if the data is held in static storage. For instance, in a paper by Richard W. Hofheimer (1960) a type of shift register is explained which has a capacitive storage. In this case, if the data is not shifted out by some maximum time, it will be lost.

CHAPTER IV

DISCUSSION OF BINARY INPUT CONDITIONS

The type of binary used in this experiment is shown in Figure 3.

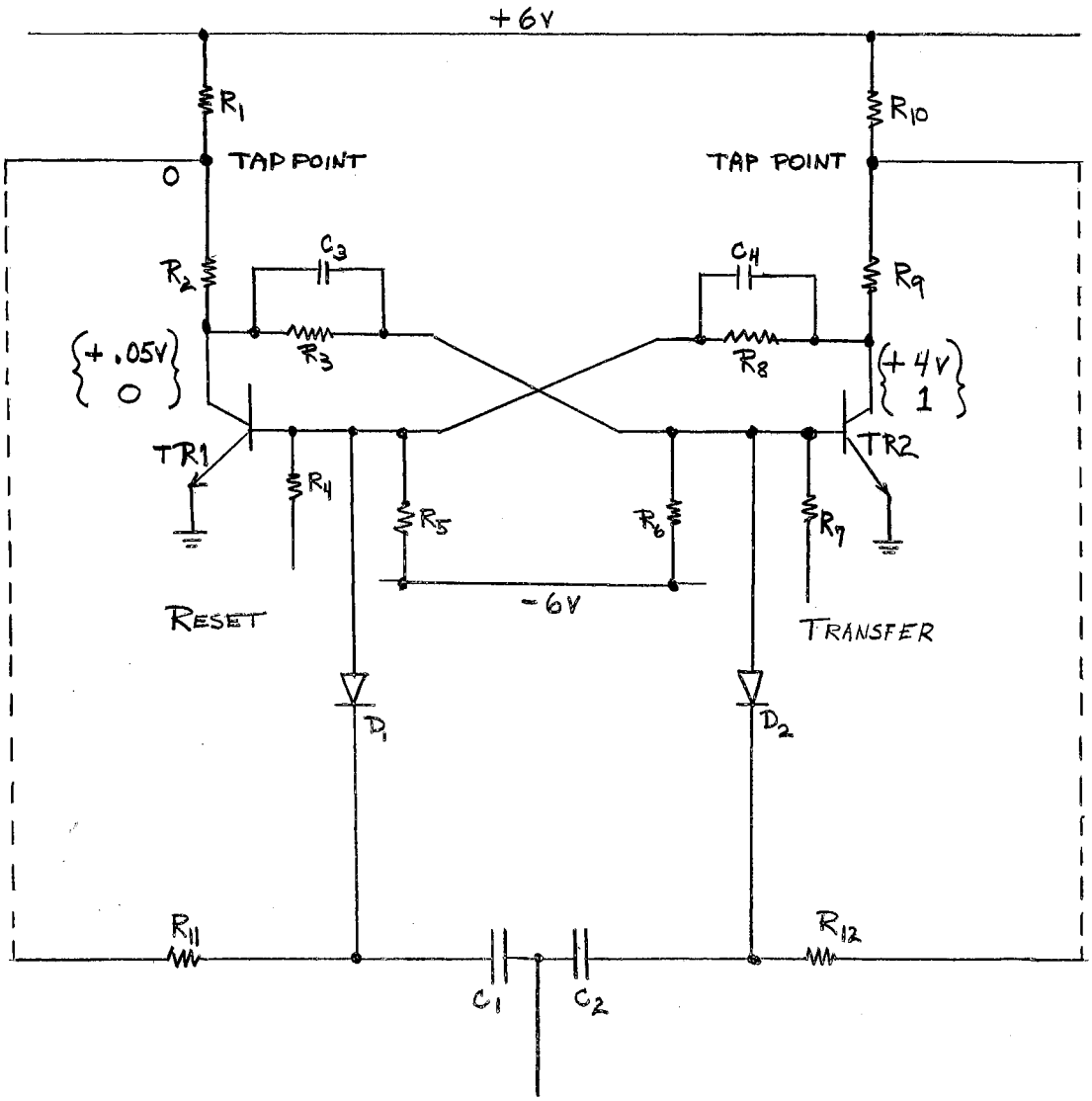


Figure 3. Typical Binary

The type used is similar to most binaries except for R_2 and R_9. R_2 is small compared to R_1 and is used to bias the tap point to approximately +0.4v when TR1 is on. R_9 serves the same purpose when TR2 is on.

Since the binary number system is used, two d.c. conditions are necessary to represent 0 and 1. Let +.05v or +.4v represent the 0 state and +4v represent the 1 state.

The binary will change states if it receives a negative trigger on its input, and if the inputs to R_{11} and R_{12} are the correct state or D.C. level.

The four possible static conditions are shown in Figure 4 (4-a, 4-b, 4-c, and 4-d). An arrow is used to show the change that occurs when a 3 volt negative pulse is applied to the capacitor.

1-1 Condition (Figure 4-a)

When a 3 volt negative pulse is applied to the capacitor, the cathode of the diode will step to +1v, but the diode will not conduct.

1-0 Condition (Figure 4-b)

When a 3 volt negative pulse is applied to the capacitor, the cathode of the diode will step to -2.6v. The diode will conduct, and the base of the transistor will be driven to -2.0v. However, the transistor was already off, or in the 1 state, so a change of state will not occur.

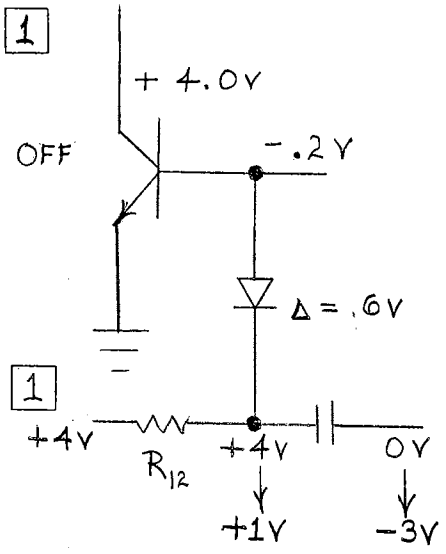


Figure 4-a

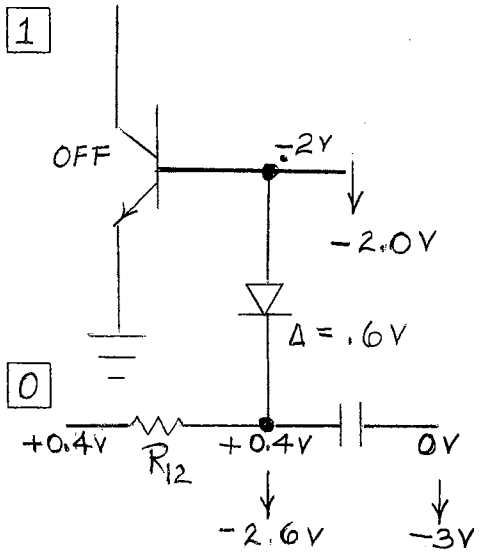


Figure 4-b

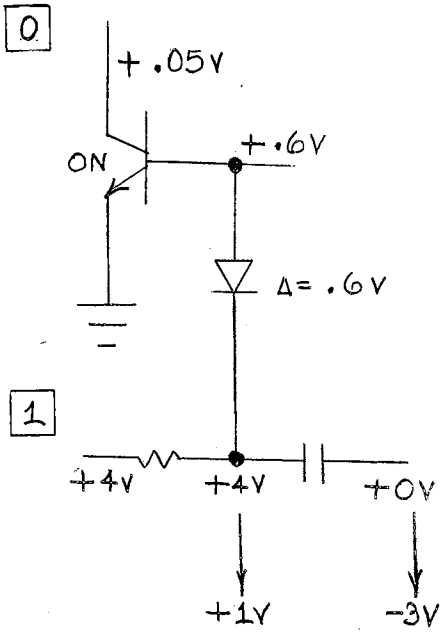


Figure 4-c

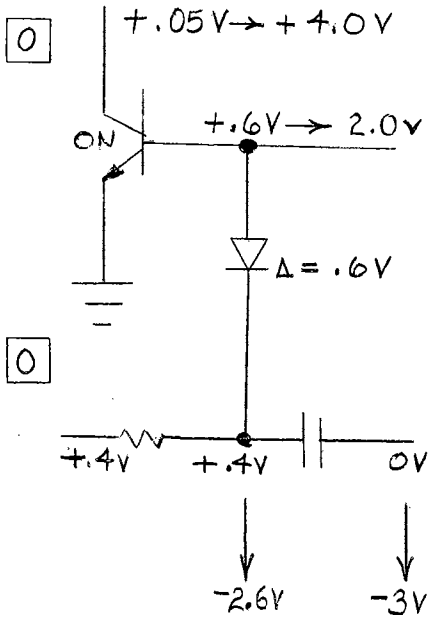


Figure 4-d

Figure 4. Four Possible Static Input Conditions for a Binary

0-1 Condition (Figure 4-c)

The results are identical to the 1-1 condition.

0-0 Condition (Figure 4-d)

When a 3 volt negative pulse is applied to the capacitor, the cathode of the diode will step to -2.6v. The diode will conduct, and the base of the transistor will be driven from +.6v to -2.0v. The transistor will be turned off, and a change of state will occur. Therefore, the 0-0 condition is unique.

In a monostable multivibrator the steering resistors are connected internally to the tap points as shown by the dashed lines in Figure 3. Therefore, one side of the binary will always be in the 0-0 condition, and a change of state will occur every time a negative pulse arrives at the input.

CHAPTER V

CASCADED BINARIES

It is possible to make a shift register by properly interconnecting a set of cascaded binaries. Instead of connecting the steering resistors internally, connect them to the opposite tap points of the preceding binary. Figure 5 shows three binaries connected in this manner.

Assume a negative pulse appears at the input of the binary. The preceding binary will determine whether or not the binary changes state.

By connecting the inputs together, the three binaries can be pulsed simultaneously. It will be of interest to see what happens when each shift pulse occurs.

Assume that a 0 and 1 are being held into R_{111} and R_{112} respectively, and that the binaries are resting in the (0 1), (1 0), and (0 1) state.

First Pulse

TR1 of the first binary is in the 0-0 condition, so a change of state will occur. Also, TR2 of the second binary and TR1 of the third binary are in the 0-0 condition. Therefore, the three binaries will change to (1 0), (0 1), and (1 0).

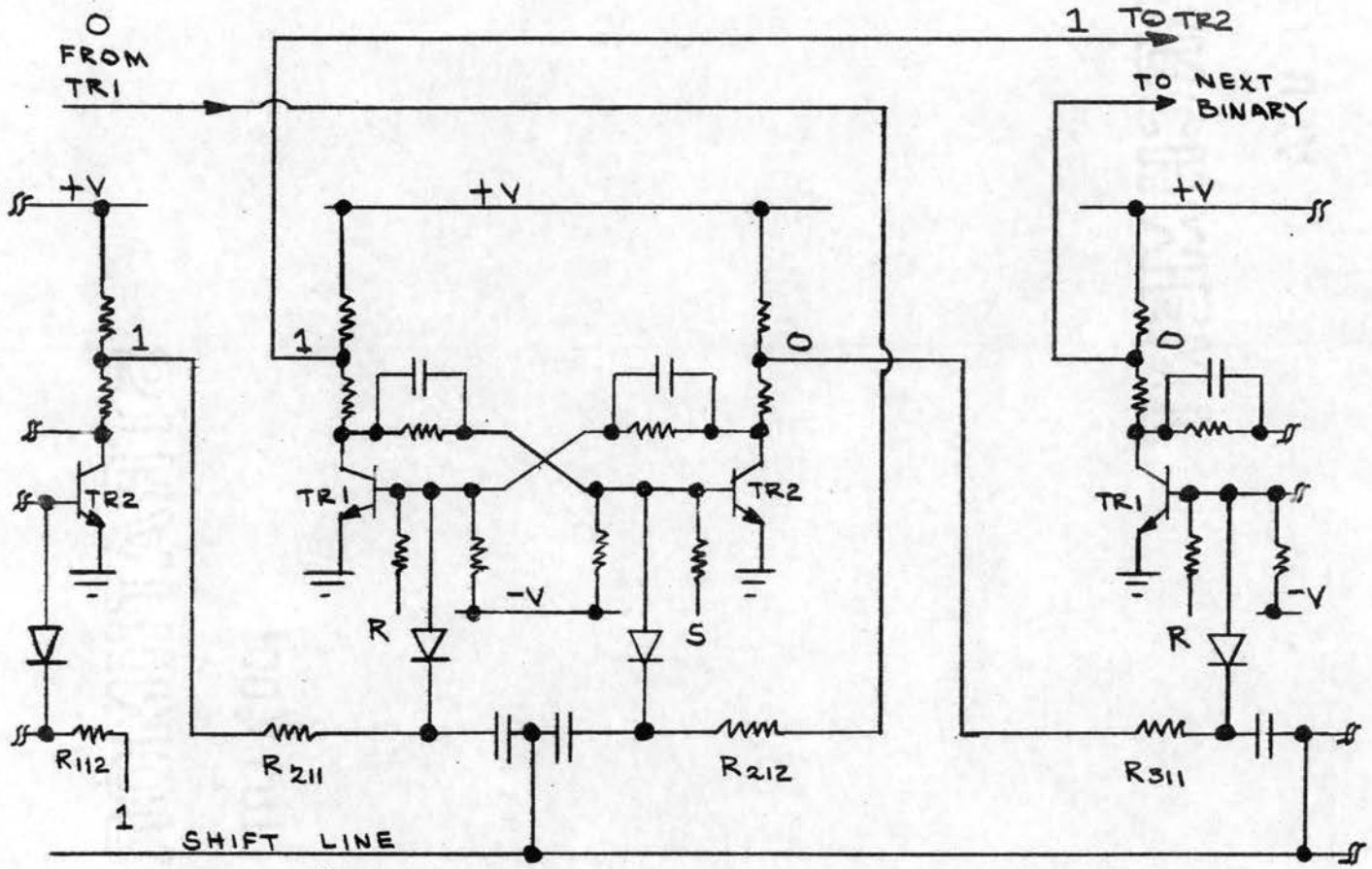


Figure 5. Binaries Cascaded to Form a Shift Register

SECOND PULSE

TR1 of the first binary is in the 1-0 condition, and TR2 is in the 0-1 condition; therefore, a change of state will not occur. TR1 of the second binary and TR2 of the third binary are in the 0-0 condition, so a change of state will occur in them. The three binaries will now be (1 0), (1 0), and (0 1).

THIRD PULSE

Both sides of the first two binaries are either in the 0-1 condition or the 1-0 condition, therefore, a change of state will not occur in them. But the third binary is in the 0-0 condition, so the three binaries will now be (1 0), (1 0), and (1 0).

FOURTH PULSE

Both sides of the three binaries are either in the 1-0 or 0-1 condition. Therefore, a change of state will not occur in any of them. Regardless of how many additional input pulses occur, the binaries will not change states again.

Using TR2 as the output, Table III can be made. As each pulse arrives, the data of the preceding binary is shifted to the right. This satisfies the requirements of a shift register. If the data is D.C. entered at R_{7n}, this would be a parallel input-series output shift register.

Since the 0-0 condition is easily recognizable, a step-by-step analysis is not required. All that is necessary is to know how the binaries are cascaded together, and their condition preceding

each shift pulse.

TABLE III

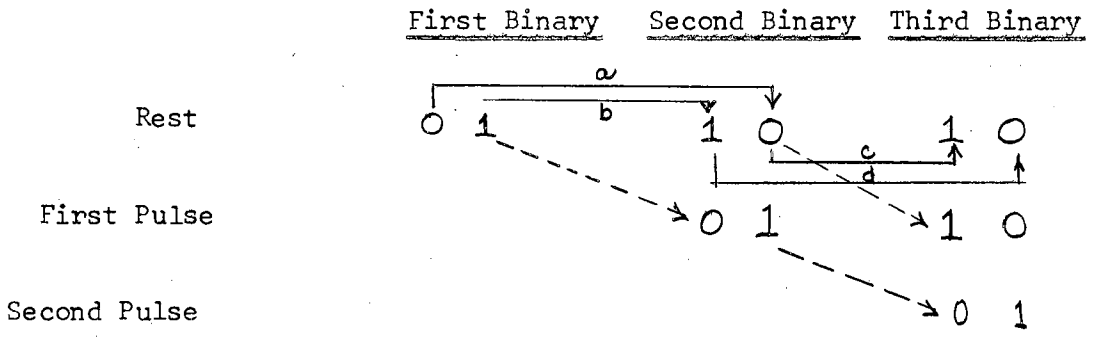
OUTPUT OF TR2

Rest	1	0	1
First Pulse	0	1	0
Second Pulse	0	0	1
Third Pulse	0	0	0
Fourth Pulse	0	0	0
n^{th} Pulse ($n > 2$)	0	0	0

For instance, in Figure 5 the right output of the (n - 1) binary controls the left input of the n binary. This is illustrated in Table IV. In Table IV, at rest, line a has the only 0-0 condition; therefore, when

TABLE IV

DATA SHIFTED TO THE RIGHT



the first pulse arrives, the second binary will change states. Since the input condition to the first binary is not shown, its new state will be unknown. When the second shift pulse arrives, line d will have the only 0-0 condition.

It will be of interest to study what will happen if the right output of the (n - 1) binary controls the right input of the n binary. This is illustrated in Table V. There are 5 stages with a static (0 1) into

TABLE V

RANDOM DATA TERMINATING IN ALTERNATING STATES

	0 1 ← Input conditions									
Rest	1	0	0	1	1	0	1	0	0	1
First Pulse	1	0	0	1	1	0	0	1	0	1
Second Pulse	1	0	0	1	1	0	0	1	1	0
Third Pulse	1	0	0	1	1	0	0	1	1	0

the first binary.

When connected in this way, the binaries change state only when the preceding binary has the same state. When the binary does change state, it cannot change again unless the preceding binary changes. However, the input conditions into the first binary are static; therefore, it will either change once or not at all depending upon its original state. Its output will now act like a static input into the second binary. This will continue until the binaries are in alternating states. The number of pulses necessary for this to happen depends upon the original states of the binaries.

Another interesting case occurs if, instead of holding a constant 0 and 1 into R_{111} and R_{112}, the outputs of the last binary are used to drive R_{111} and R_{112}. This is shown in Figure 6 and Table VI.

After the fifth shift pulse, the binaries will return to the rest

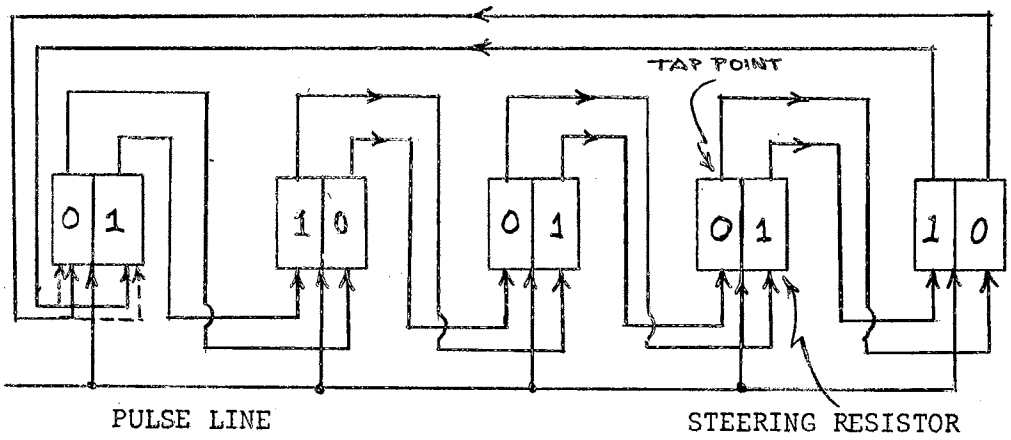


Figure 6. Recirculating Shift Register

TABLE VI

RECIRCULATION OF DATA

Rest	0	1	1	0	0	1	0	1	1	0	
First Shift	1	0	0	1	1	0	0	1	0	1	
Second Shift	0	1	1	0	0	1	1	0	0	1	one cycle
Third Shift	0	1	0	1	1	0	0	1	1	0	
Fourth Shift	1	0	0	1	0	1	1	0	0	1	
Fifth Shift	0	1	1	0	0	1	0	1	1	0	

state. The data is recirculating and is not being destroyed by the shifting operation. Once the initial data has been introduced, the binaries will preform as a series input-series output shift register. If there are n stages, it will take n pulses for one complete cycle. This is known as a "recirculating shift register".

In Figure 6 let the right side of the output binary control the right side of the first binary instead of controlling the left side. The results are shown in Table VII. Connected in this way, the com-

TABLE VII

DATA SHIFTED TO THE RIGHT AND COMPLEMENTED

Rest	0	1	1	0	0	1	0	1	0	1	Word
First Pulse	1	0	0	1	1	0	0	1	0	1	
Second Pulse	1	0	1	0	0	1	1	0	0	1	
Third Pulse	1	0	1	0	1	0	0	1	1	0	
Fourth Pulse	0	1	1	0	1	0	1	0	0	1	
Fifth Pulse	1	0	0	1	1	0	1	0	1	0	$\overline{\text{Word}}$
Sixth Pulse	0	1	1	0	0	1	1	0	1	0	
Seventh Pulse	0	1	0	1	1	0	0	1	1	0	
Eighth Pulse	0	1	0	1	0	1	1	0	0	1	
Ninth Pulse	1	0	0	1	0	1	0	1	1	0	
Tenth Pulse	0	1	1	0	0	1	0	1	0	1	Word

plement of the word will be shifted out every other time. This could be used to complement a set of binaries with n pulses and then, if required, shift out the complement.

This property is accomplished by the uniqueness of the first stage. It always introduces the complement of the output stage into the shift register.

In all of the examples so far, the data has been shifted to the right. However, if the binaries are cascaded so that the n binary controls the (n - 1) binary, the data will be shifted to the left. The first stage will now be the output stage.

Figure 7 shows five binaries connected to shift to the left, and Table VIII illustrates a case of shifting to the left.

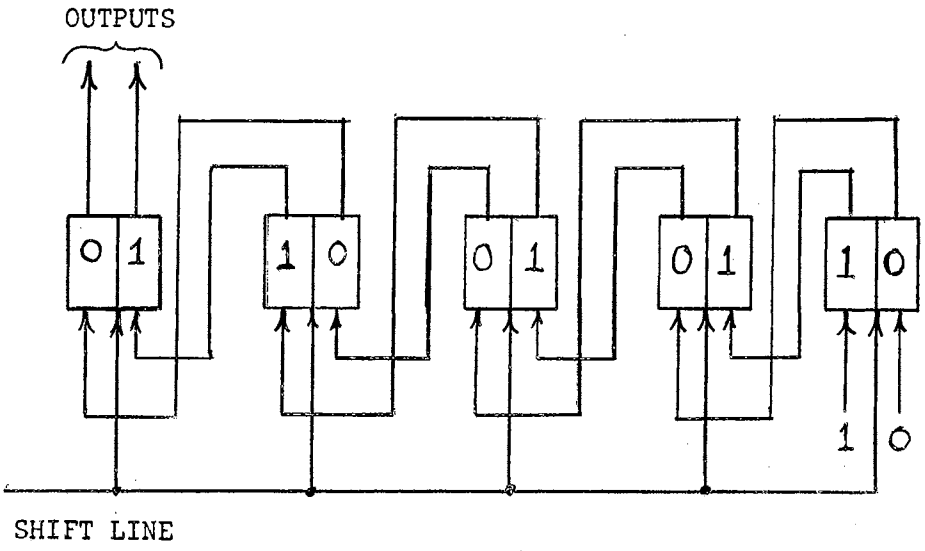


Figure 7. Binaries Cascaded to Shift to the Left

This chapter has dealt with different ways of cascading binaries, some of which are compatible with the requirements for a shift register. This group has one thing in common. The right side of the "control binary" must always control the left side of the "controlled binary". This is true regardless of whether the shift register shifts to the left or to the right, and regardless of whether

the input to the first binary is static or recirculated.

TABLE VIII

DATA SHIFTED TO THE LEFT

Rest	0	1	1	0	0	1	0	1	1	0	Input
First Pulse	1	0	0	1	0	1	1	0	1	0	
Second Pulse	0	1	0	1	1	0	1	0	1	0	
Third Pulse	0	1	1	0	1	0	1	0	1	0	
Fourth Pulse	1	0	1	0	1	0	1	0	1	0	
	Output										

CHAPTER VI

BIDIRECTIONAL SHIFT REGISTER EMPLOYING INTERSTAGE GATING

Some applications require that a shift register be able to shift in either direction. One means of accomplishing this would be to employ a set of gates between each binary. By using two control lines, in a manner somewhat similar to a reversible counter, the binaries will shift either direction.

Figure 8 shows three shift register binaries and the two control lines. By establishing the following conditions, a truth table can be constructed.

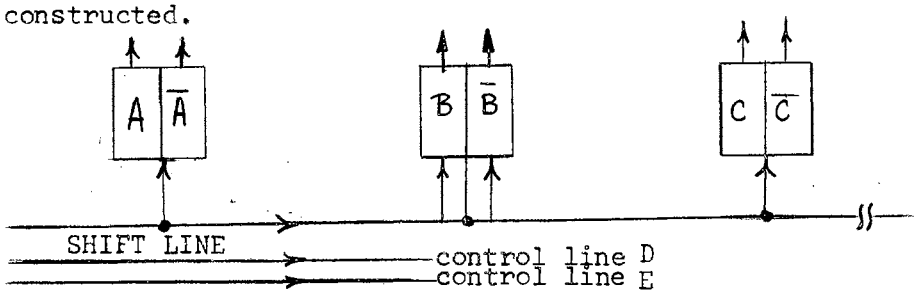


Figure 8. Basic Connections for a Bidirectional Shift Register

First of all, assume that a 0 on line D causes the shift register to shift to the right and a 0 on line E causes it to shift to the left. Also assume that the shift register does not have a rest state. In other words, lines D and E must be (0-1) or (1-0) but never (0-0) or (1-1). Therefore, the (0-0) and(1-1) conditions are DON'T CARE STATES.

Next, consider the input to $\overline{B}$. When the shift register shifts to the right the input to $\overline{B}$ must be the same as the output of A. Likewise,

when it shifts to the left the input to $\overline{B}$ must be the same as C. The input to B can be obtained by inverting the input to $\overline{B}$. The following truth table can be constructed.

TABLE IX

TRUTH TABLE FOR BIDIRECTIONAL SHIFT REGISTER WITH DON'T CARE STATES

	← E	→ D	C	A	input to $\overline{B}$	B	f_{min}	Block
	0	0	0	0	d			
I	0	0	0	1	d			
	0	0	1	0	d			
	0	0	1	1	d			
	0	1	0	0	0	1		
II	0	1	0	1	0	1		
	0	1	1	0	1	0	$\overline{E}D\overline{C}\overline{A}$	3
	0	1	1	1	1	0	$\overline{E}DC\overline{A}$	7
	1	0	0	0	0	1		
III	1	0	0	1	1	0	$E\overline{D}\overline{C}\overline{A}$	9
	1	0	1	0	0	1		
	1	0	1	1	1	0	$E\overline{D}C\overline{A}$	10
	1	0	0	0	d			
	1	0	0	1	d			
IV	1	0	1	0	d			
	1	0	1	1	d			

I - DON'T CARE STATE
II - SHIFT TO LEFT
III - SHIFT TO RIGHT
IV - DON'T CARE STATE

A Veitch diagram can now be drawn from Table IX. By taking advantage of some of the DON'T CARE STATES the minimum disjunctive form of f is

TABLE X

VEITCH DIAGRAM

	E		$\bar{E}$		
	d 1	d 2	0110 3	 4	$\bar{A}$
D	d 5	d 6	0111 7	 8	
	1001 9	1011 10	d 11	d 12	A
$\bar{D}$	 13	 14	d 15	d 16	$\bar{A}$
	$\bar{C}$		C	$\bar{C}$	

$$f = A\bar{D} + C\bar{E} \; . \tag{6-1}$$

Although the following circuits are limited to one type of logic, this is only for demonstrative purposes.

Referring to Appendix B, the diode logic is shown in Figure 9.

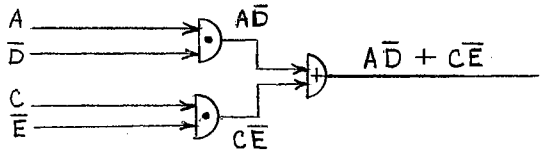


Figure 9. Interstage Diode Logic for a Bidirectional Shift Register

Demorgan's Law can also be used to change f into a form which will be compatible with NOR circuitry. Thus,

$$f = A\bar{D} + C\bar{E} = \overline{\bar{A} + D} + \overline{\bar{C} + E}\ , \text{ therefore,} \qquad (6\text{-}2)$$

$$f = \overline{\overline{\left(\bar{A} + D\right)} + \left(\bar{C} + E\right)}\ . \qquad (6\text{-}3)$$

Referring to Appendix B, the NOR logic is shown in Figure 10.

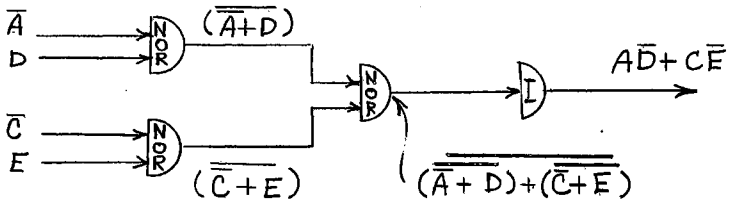


Figure 10. Interstage NOR Logic for a Bidirectional Shift Register Employing Four Gates

When a function is minimized by the Harvard or Veitch diagram it is not the only form of the minimized function. The complement of the function, $\bar{f}$, can also be minimized. The original function can then be obtained by taking the complement of the the complement, $\bar{\bar{f}}$, which yields f.

When inverting logic is used, such as NOR and NAND, complements must always occur. For this reason, $\bar{\bar{f}}$, may be a more desirable form than f. Actually, $\bar{\bar{f}}$, can be obtained directly from f by repeated use of Demorgan's Law.

There is one important exception to the last statement. If DON'T CARE STATES are available, some or all of them may be used to obtain the minimum function f. Since these states are redundant, some

of the same ones may be used to obtain $\bar{f}$. In this case, $\bar{\bar{f}}$ can not be obtained from f. Since this is so, the Boolean form of the output will not be the same. However, for the input conditions that are possible, the outputs will be the same. Also, since $\bar{\bar{f}}$ can not be obtained from f, one circuit may be more simple than the other.

The earlier example of NOR logic can be used to demonstrate most of these properties.

From the Veitch diagram, the original function f_1, without the use of DON'T CARE STATES, is

$$f_1 = A\bar{D}E + CD\bar{E} \quad . \tag{6-4}$$

By the use of DON'T CARE STATES, $\bar{f}_1$ can be reduced to

$$f_2 = A\bar{D} + C\bar{E} \quad . \tag{6-5}$$

The complement of the original function, f_1, is

$$\bar{f}_1 = DE + \bar{D}\bar{E} + \bar{A}\bar{D} + \bar{C}\bar{E} \quad . \tag{6-6}$$

By excluding some of the DON'T CARE STATES, $\bar{f}_1$ can be reduced to

$$\bar{f}_3 = \bar{A}\bar{D} + \bar{C}\bar{E} \tag{6-7}$$

which gives

$$\bar{\bar{f}}_3 = \overline{\bar{A}\bar{D} + \bar{C}\bar{E}} = \overline{(\overline{A + D}) + (\overline{C + E})} \quad . \tag{6-8}$$

Referring to Appendix B, the NOR logic is shown in Figure 11.

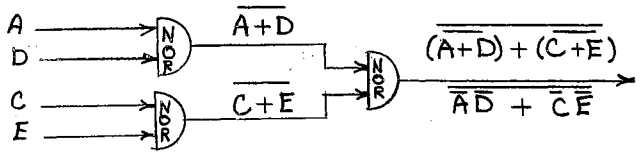


Figure 11. Interstage NOR Logic for a Bidirectional Shift Register Employing Three Gates

As stated before, the Boolean outputs of Figure 10 and Figure 11 appear to be different. However, for the states of D and E that are possible, they are the same. Yet, the circuit in Figure 11 requires one less stage. For this to be possible there must be a form of f that will yield the circuitry shown in the later figure. From the Veitch diagram let f_4 be

$$f_4 = AC + AE + CD + DE, \tag{6-9}$$

$$f_4 = (A + D)(C + E), \tag{6-10}$$

$$f_4 = \overline{\overline{(A + D)} + \overline{(C + E)}} \quad . \tag{6-11}$$

This is the same as $\overline{\overline{f}}_3$ obtained by the earlier method.

This implies that if DON'T CARE STATES are used the minimum form of f depends on the type of circuitry involved and not just on the least number of terms. In fact, this is true in general with or without DON'T CARE STATES.

In order to be more precise, let the circuit in Figure 11 be used between each stage. The shift register obtained in this manner is shown in Figure 12. Table XI is the corresponding truth table. Referring to Table XI, when line D is 0, the input to $\overline{B}$ is indentical to the output of A. Likewise, when line E is 0, the input to $\overline{B}$ is identical to the output of C. This satisfies the initially desired conditions.

Although this method would work, another type of bidirectional shift register was used. This later method is discussed in Chapter VII.

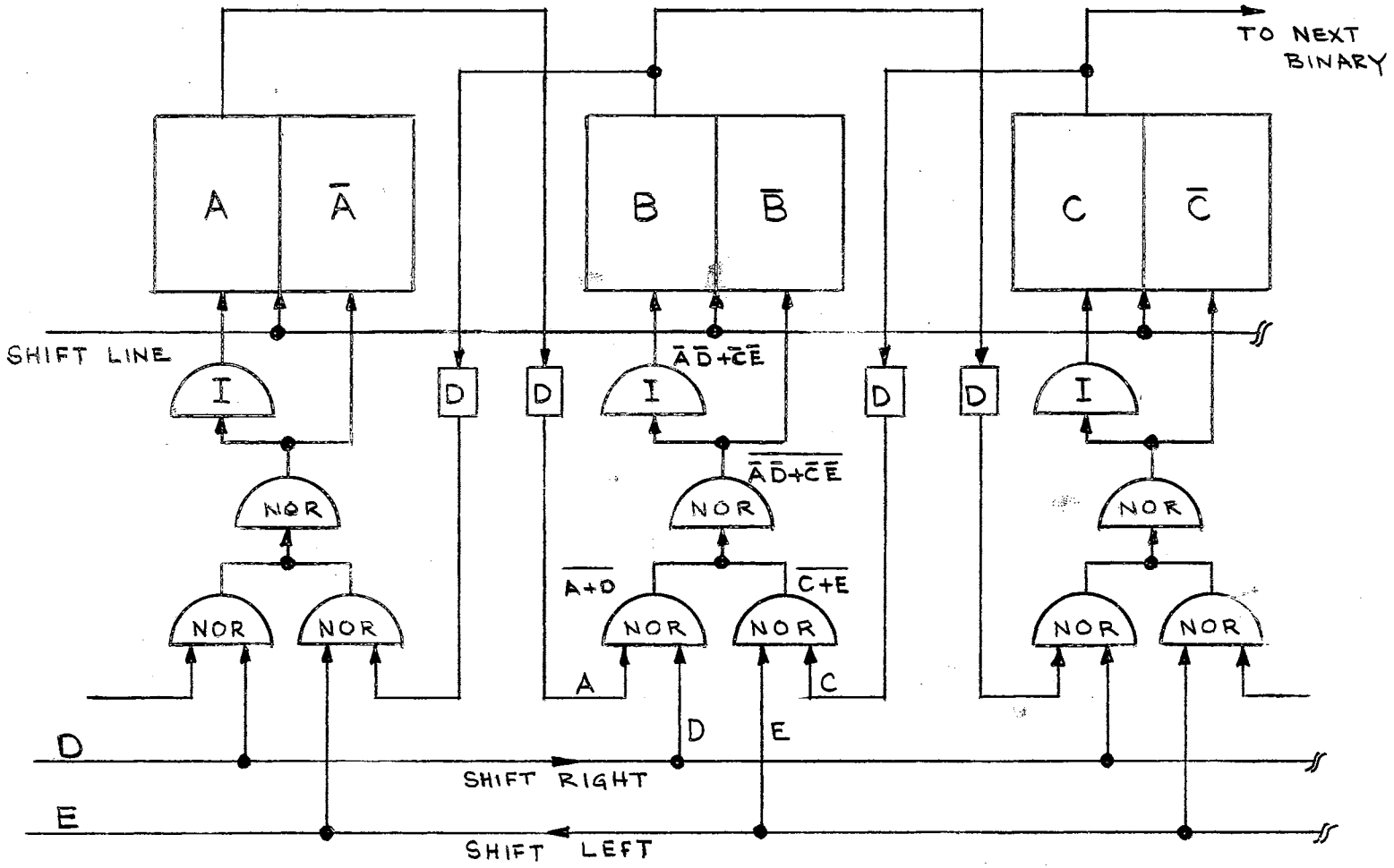


Figure 12. Bidirectional Shift Register Employing Interstage NOR Logic

TABLE XI

TRUTH TABLE FOR BIDIRECTIONAL SHIFT REGISTER WITHOUT DON'T CARE STATES

	Shift left ← E	Shift right → D	C	A	$\overline{A + D}$	$\overline{C + E}$	Input to $\overline{B}$: $\overline{(\overline{A + D}) + (\overline{C + E})}$	Input to B: $(\overline{A + D}) + (\overline{C + E})$
II	0	1	0	0	0	1	0	1
	0	1	0	1	0	1	0	1
	0	1	1	0	0	0	1	0
	0	1	1	1	0	0	1	0
III	1	0	0	0	1	0	0	1
	1	0	0	1	0	0	1	0
	1	0	1	0	1	0	0	1
	1	0	1	1	0	0	1	0

II (C Control)
III (A Control)

CHAPTER VII

BINARY EMPLOYING TWO SHIFT LINES

Another means of making a bidirectional shift register is to employ two independent sets of steering components. Let one set be steered by the binary on the left, and the other set be steered by the binary on the right. Depending on which shift line is pulsed, the binaries will shift either to the left or to the right.

A binary of this type is shown in Figure 13. Assume that it is the (n - 1) binary in a string of n binaries. The lower set of steering components is controlled by the (n - 2) binary. When its input is pulsed the binaries shift to the right. This is identical to the connection shown in Figure 6. Likewise, the upper set of steering components is controlled by the n binary. When its input is pulsed the binaries shift to the left. This is identical to the connection shown in Figure 7. Except for a few considerations, which are discussed in Chapter VIII, the two sets of steering components are independent.

Five such binaries are used in this experiment. By means of a four pole-six position switch, the binaries will shift either direction, with or without recirculating. Thus, it has four distinct modes of operation.

The interconnection between binaries and the switch are shown in Figures 14 and 15, respectively.

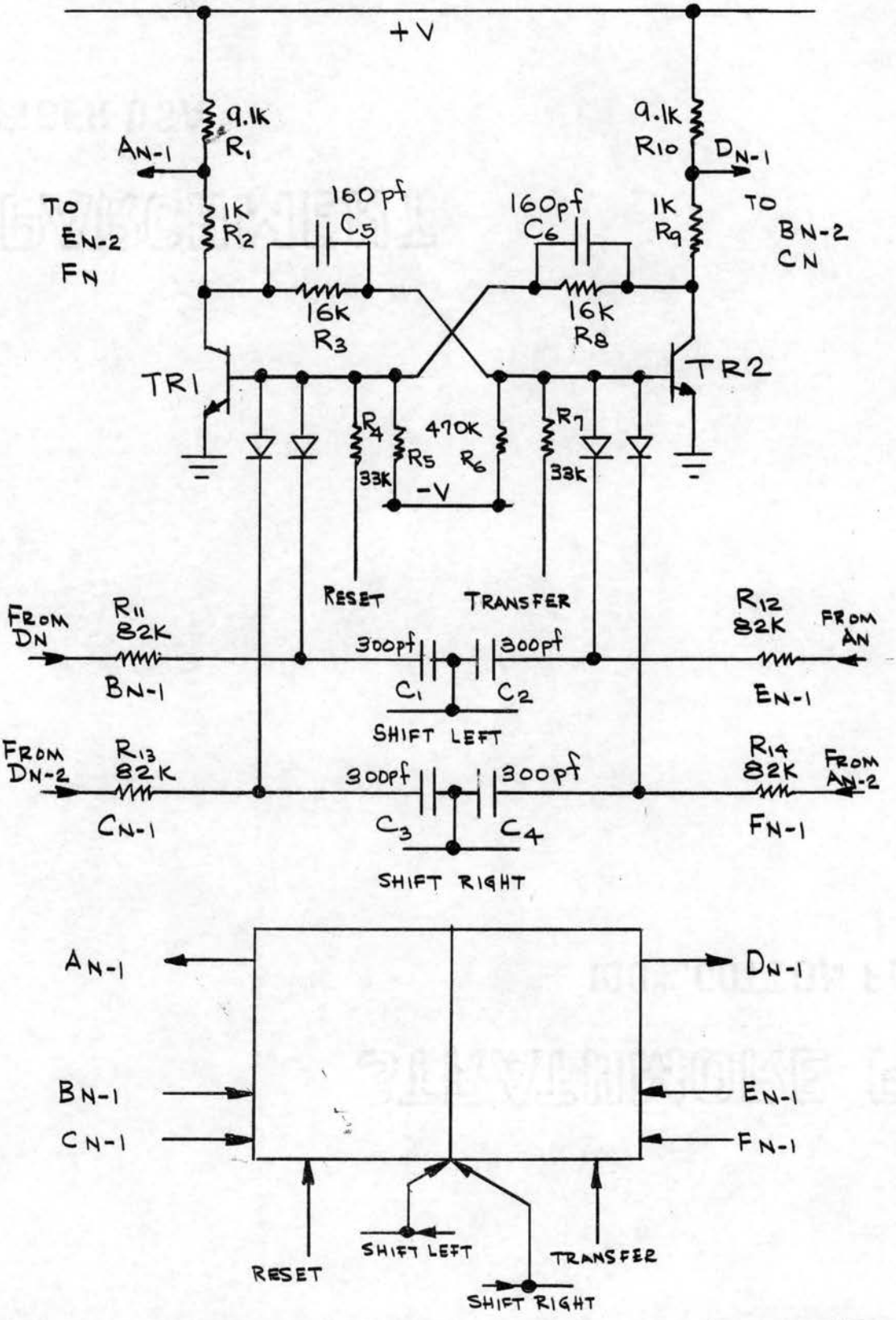


Figure 13. Schematic and Block Diagram of Binary Employing Two Shift Lines

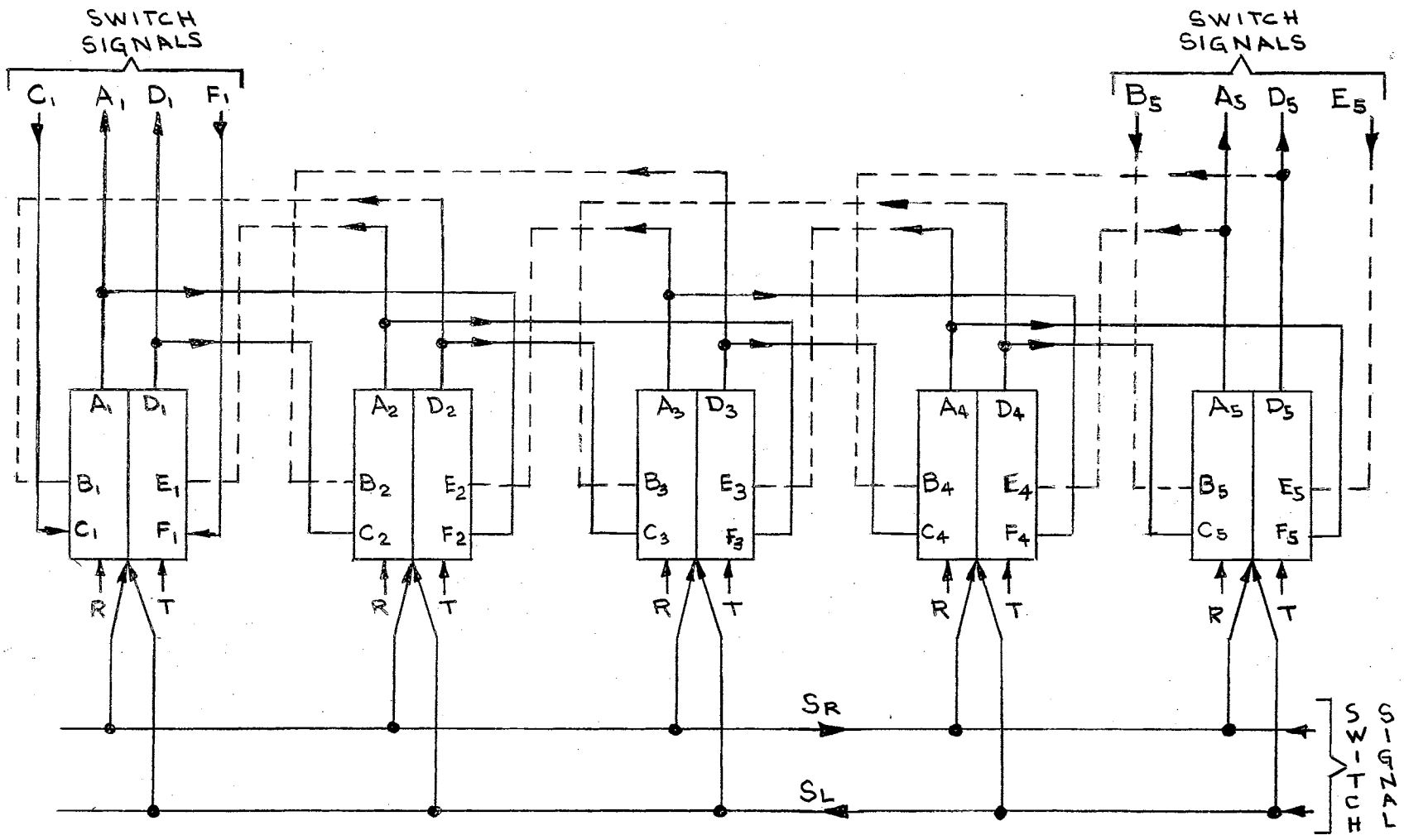
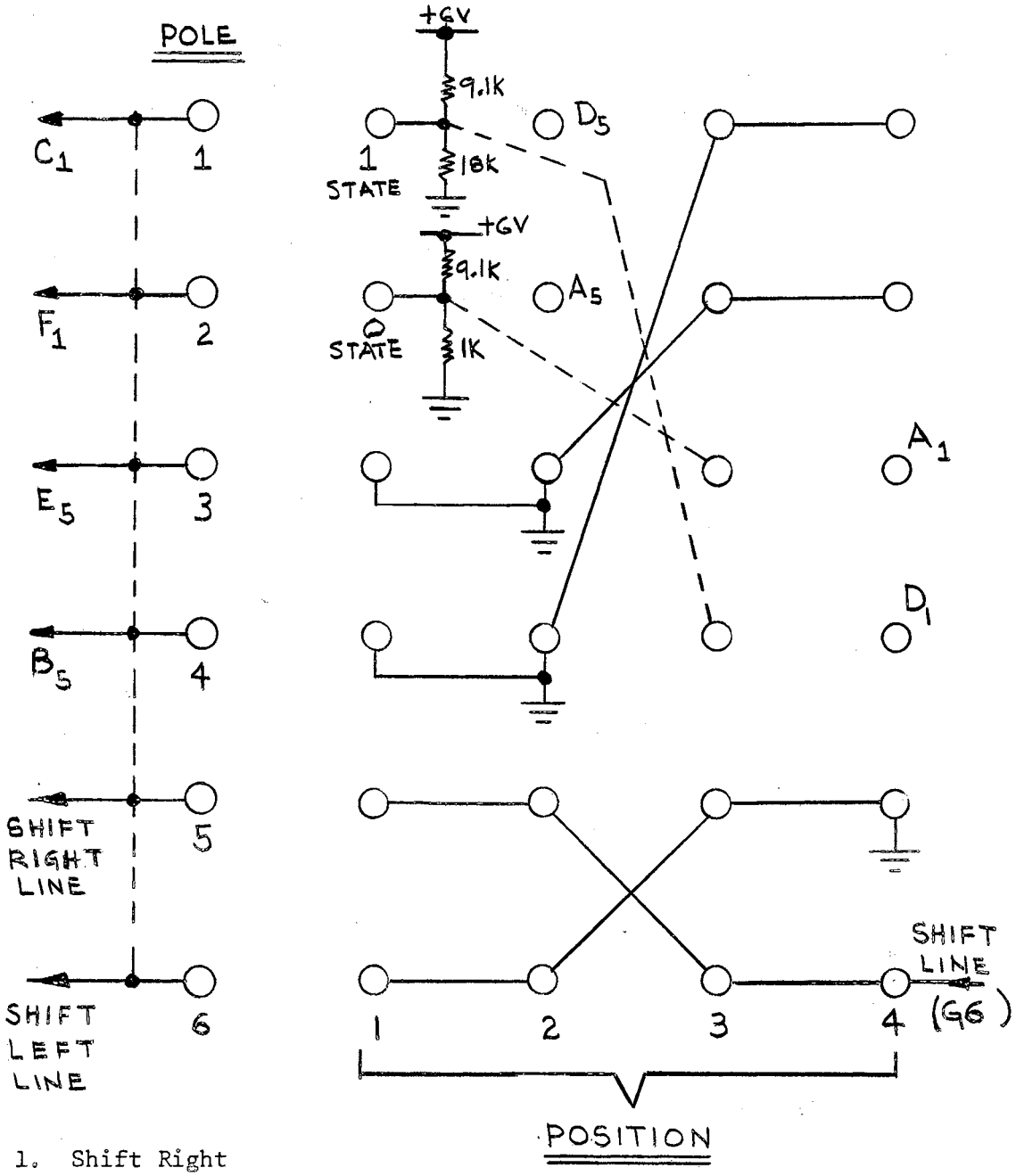


Figure 14. Block Diagram of Bidirectional Shift Register Employing Two Shift Lines



Position 1. Shift Right
Position 2. Recirculate to Right
Position 3. Shift Left
Position 4. Recirculate to Left

Figure 15. Schematic of Bidirectional Shift Register Mode Switch

CHAPTER VIII

SHIFT REGISTER BINARY DESIGN

This chapter is concerned with the important design considerations of the binary shown in Figure 13.

The binaries are completely symmetrical in that components serving similar purposes will have identical values. For instance, all of the steering resistors will have the same value. Thus, it is only necessary to write the equations for one binary state. Furthermore, similar component symbols can be freely interchanged in an equation.

Electron current will be used in the derivation of the equations.

D. C. Collector Current

In the steady-state condition the capacitors are disregarded. Assume that TR2 is saturated and TR1 is cut off. Also assume that no current flows in the off transistor. This is a valid assumption since in a silicon planar epitaxial mesa transistor I_{cbo} is less than 0.2 microamps.

Assume the leakage in D_1 is less than one microamp and can be neglected. The following partial circuit can be draw as shown in Figure 16.

The D.C. collector current in TR1, I_{cdc}, will be

$$I_{cdc} = I_3 - (I_1 + I_2) \qquad (8\text{-}1)$$

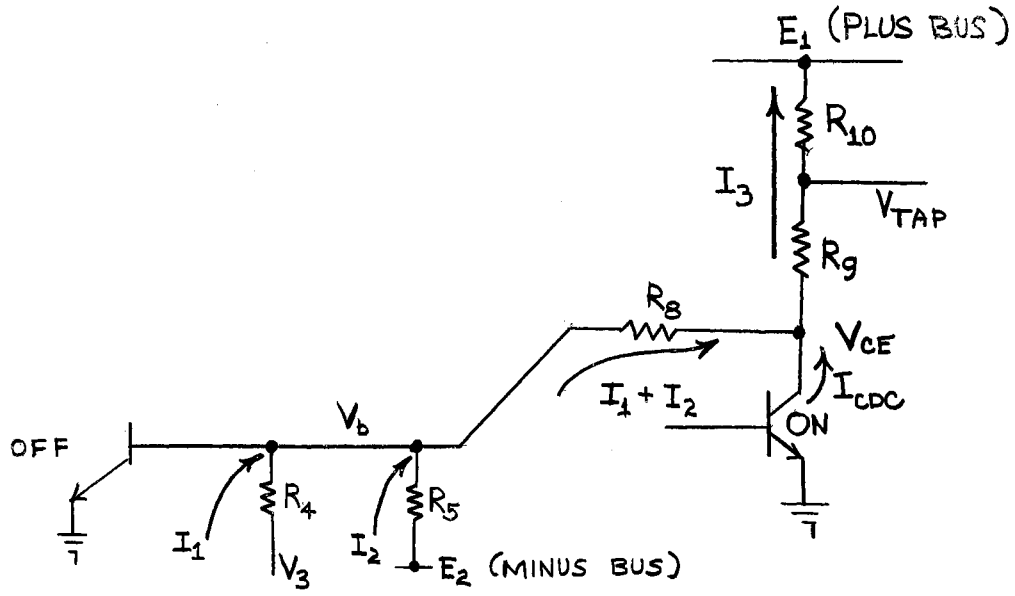


Figure 16. Partial Circuit for D.C. Collector Conditions

which can be written as

$$I_{cdc} = \frac{E_1 - V_{ce}}{R_9 + R_{10}} - \frac{(V_{ce} - V_b)}{R_8} \quad . \tag{8-2}$$

In most cases $(V_{ce} - V_b)$ is much less than $(E_1 - V_{ce})$ and R_8 is larger than $(R_9 + R_{10})$. With this in mind, Equation 8-2 can be simplified to

$$I_c = \frac{E_1 - V_{ce}}{R_9 + R_{10}} \quad . \tag{8-3}$$

Down Tap Voltage

The down tap voltage (0 state) can be used to relate R_9 and R_{10}.

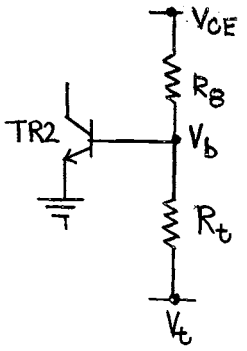
$$\frac{V_{tap} - V_{ce}}{R_9} = \frac{E_1 - V_{tap}}{R_{10}} \tag{8-4}$$

or

$$R_{10} = \frac{E_1 - V_{tap}}{V_{tap} - V_{ce}} R_9 \quad (8\text{-}5)$$

Transistor Off Bias

Figure 17 is obtained from Figure 16 by writing a Thevenin's circuit of R_4, R_5, V_3, and E_2. The off bias, V_b, can be obtained from Figure 17 by using voltage division.



$$R_t = \frac{R_4 R_5}{R_4 + R_5}$$

$$V_t = E_2 + \frac{(E_2 - V_3)}{R_4 + R_5} R_5$$

Figure 17. Partial Circuit for Transistor Off Bias

$$V_b = \frac{V_t - V_{ce}}{R_t + R_8} R_t \quad (8\text{-}6)$$

Neglecting V_{ce}, Equation 8-6 can be written as

$$V_b = \frac{\{E_2 (R_4 + R_5) + (E_2 - V_3) R_5\} R_4 R_5}{\{R_4 R_5 + R_8(R_4 + R_5)\} R_4 + R_5} \quad (8\text{-}7)$$

Since the binary is completely symmetric and V_3 equals V_4, the off bias for TR1 is

$$V_b = \frac{\{E_2(R_7 + R_6) + (E_2 - V_5)\ R_6\}R_7\ R_6}{\{\ R_7\ R_6 + R_3(R_7 + R_6)\}(R_7 + R_6)} \qquad (8\text{-}8)$$

Base Equations

The base equations can be obtained from the following partial circuit as shown in Figure 18.

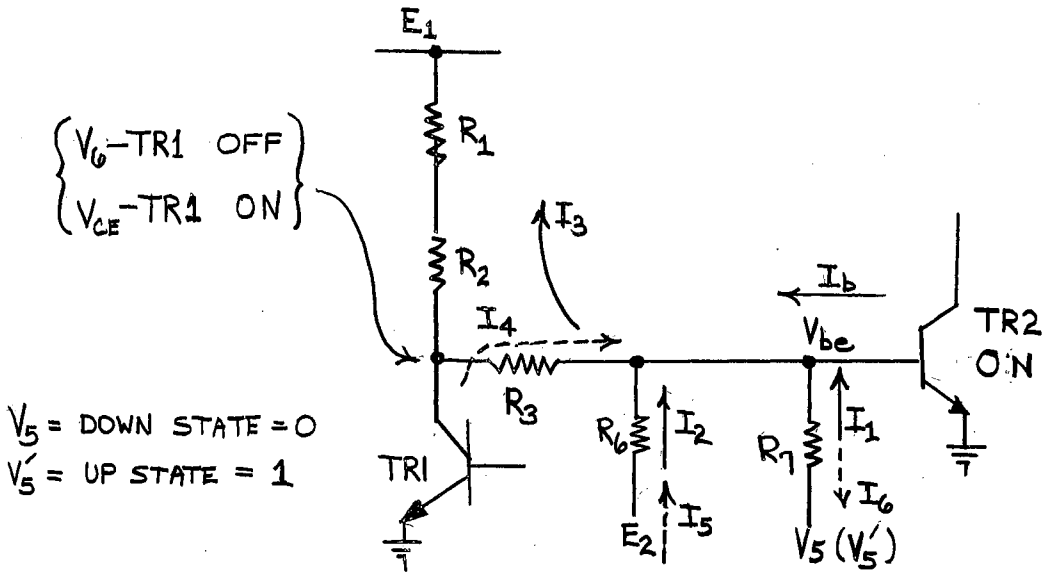


Figure 18. Partial Circuit for D.C. Base Conditions

Since R_7 is a reset or set resistor, two cases of base drive must be considered. First, consider the case where the base drive is being furnished via R_3, and V_5 is 0. This shown by the solid arrows in Figure 18.

The base current will be

$$I_b = I_3 - I_2 - I_1 \ . \qquad (8\text{-}9)$$

which can be written as

$$I_b = \frac{E_1 - V_{be}}{R_1 + R_2 + R_3} - \frac{(V_{be} - E_2)}{R_6} - \frac{(V_{be} - V_5)}{R_7} \quad (8\text{-}10)$$

If the off collector of TR1 has an external load, the following equation must be used.

$$I_b = \frac{V_6 - V_{be}}{R_3} - \frac{(V_{be} - E_2)}{R_6} - \frac{(V_{be} - V_5)}{R_7} \quad (8\text{-}11)$$

Next, consider the case where TR2 is off and V_5 is 0. When V_5 goes from 0 to 1, TR2 will be turned on. The binary can not change states instantaneously, so for a short time both transistors will be on. As TR1 starts towards a 1, I_4 will decrease and then reverse directions. Therefore, the minimum I_b occurs at the initial turn on of TR2. The initial turn on is shown by the dashed arrows in Figure 18. The equation for minimum I_b is

$$I_b = \frac{V_5' - V_{be}}{R_7} - \frac{(V_{be} - E_2)}{R_6} - \frac{(V_{be} - V_{ce})}{R_3} \quad (8\text{-}12)$$

Diode Leakage

The following partial circuit can be used to study the effects of diode leakage. The down tap voltage, set by R_1 and R_2 in the adjacent binary is chosen so the diode will have a safe off bias. The diode leakage, I_L, will cause a voltage rise across the steering

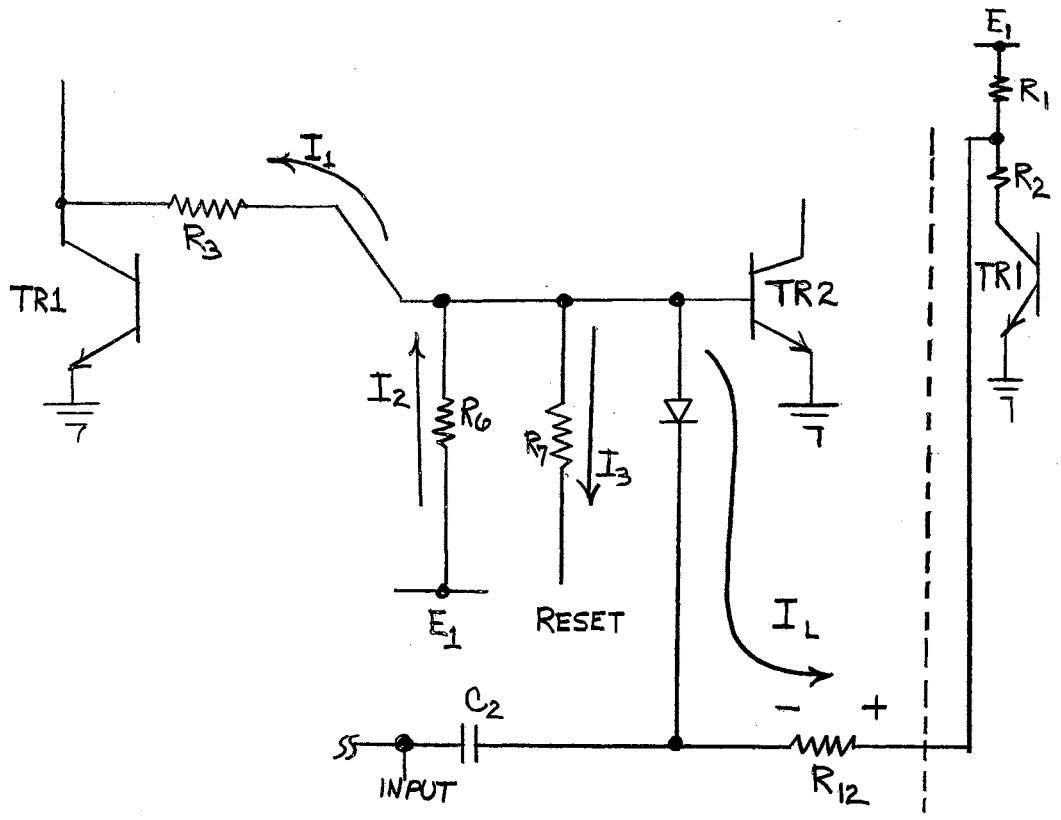


Figure 19. Partial Circuit for Diode Leakage

resistor, R_{12}. As I_L increases the diode off bias will decrease. Therefore, the maximum diode leakage should be considered before the diode off bias is chosen.

I_L also effects the off bias of TR2. Since the bias current I_2 is practically constant, as I_L increases, I_1 and I_3 must decrease. Therefore, the transistor off bias will decrease.

Rise Time of Off Collectors

The pulse conditions can be obtained from Figure 20.

Referring to Figure 20, the output of the first binary drives two sets of steering components which are not shown. The steering resistors and input capacitors are assumed to be large

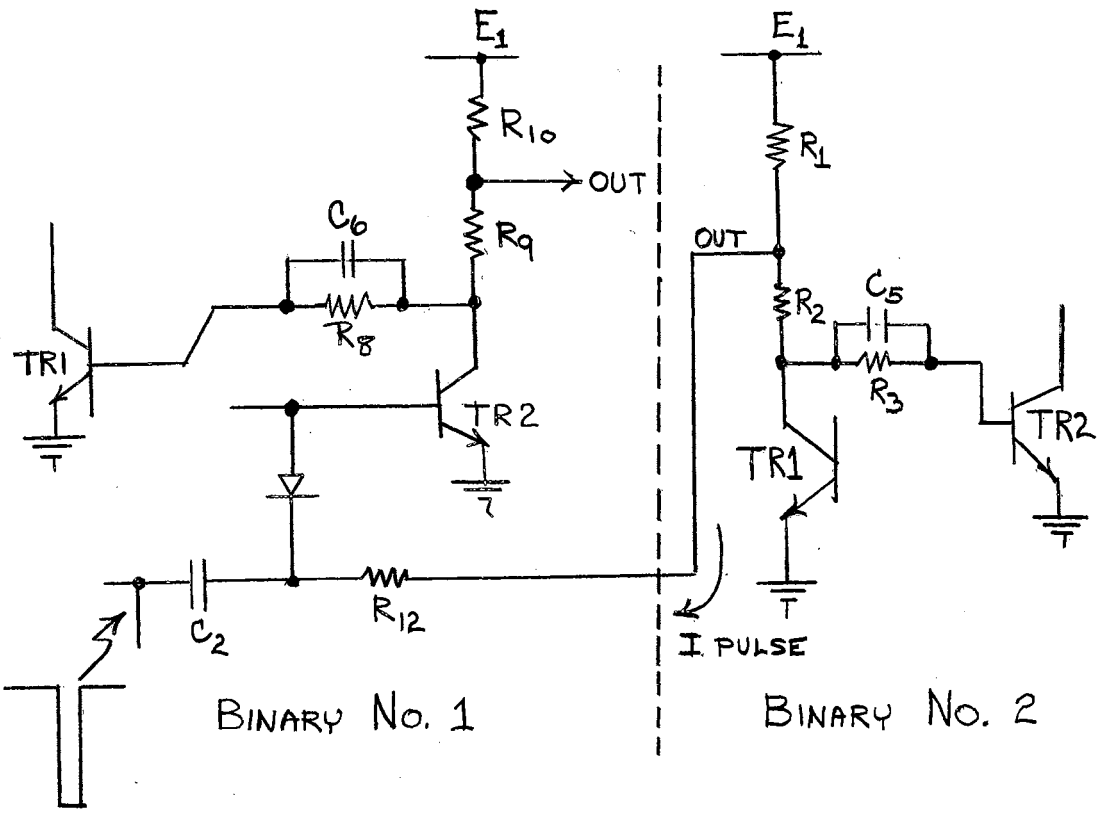


Figure 20. Partial Circuit for Binary Pulse Conditions

enough so the cross-coupling capacitor is 90% charged before the input capacitors have any appreciable change of charge. In other words, assume the steering components do not load the off-going collector. Otherwise, the two time constants will interact. This assumption is based on a later discussion concerning collector superimposed voltage. Also assume the transistor capacitance is negligible.

The 10% to 90% rise time is given by

$$t_r = 2.2\ R_e C_e \qquad (8\text{-}13)$$

Referring to Figure 20, neglecting the transistor input impedance, the time of rise, t_r, is approximately

$$t_r = 2.2 \frac{(R_9 + R_{10})\, R_8}{R_9 + R_{10} + R_8} C_6 \quad . \tag{8-14}$$

Rise and Fall Time of Cathode of Diode--Case I

Case I occurs when TR1 of the second binary is off. Referring to Figure 20, the equivalent resistance R_e is

$$R_e = R_{12} + \frac{(R_2 + R_3)\, R_1}{R_1 + R_2 + R_3} \quad . \tag{8-15}$$

This assumes that the output impedance of the circuit driving the binary input is small compared to the resistances in Equation 8-15.

Because of the completely symmetric property, Equation 8-15 can be written as

$$R_e = R_{12} + \frac{(R_8 + R_9)\, R_{10}}{R_8 + R_9 + R_{10}} \quad . \tag{8-17}$$

The approximate 10% to 90% rise time, t_I, is given by

$$t_I = 2.2 \left[R_{12} + \frac{(R_8 + R_9)\, R_{10}}{R_8 + R_9 + R_{10}} \right] C_2 \tag{8-18}$$

Rise and Fall Time of Cathode of Diode--Case II

Case II occurs when TR2 of the second binary is on. The 10%

to 90% rise and fall time, t_{II}, is approximately

$$t_{II} = 2.2 R_{12} C_2 . \qquad (8\text{-}19)$$

Actually, the parallel resistance of R_1 and R_2 acts in series with R_{12}, but this resistance is small compared to R_{12} and can be neglected. It should be observed that the cathode of the diode never changes states instantaneously. Therefore, the input capacitor and the steering resistor act as the delay between the two binaries.

Equation 8-18 and 8-19 differ only by the

$$\frac{(R_8 + R_9) R_{10}}{(R_8 + R_9 + R_{10})}$$

term. This term is usually small enough, compared to R_{12}, to neglect. Thus, the two times, t_I and t_{II}, are approximately the same.

Collector Superimposed Voltage

Referring to Figure 20, assume TR1 of the second binary is off and a shift pulse occurs at C_2. The shift pulse will be superimposed on the TR1 output of the second binary. To keep this superimposed voltage small, R_{12} must be large compared to the equivalent output impedance of the adjacent binary.

Regardless of how large the steering resistor is, some amount of the shift pulse is superimposed on the off collector. If the cross-coupling capacitor, C_5, is capable of coupling this negative voltage onto the on base of TR2, the binary will erroneously change states. For this reason, the cross-coupling time constant is small compared to the input time constant. This fact was used in an earlier approximation.

Collector Pulse Current

Referring to Figure 20, assume TR1 of the second binary is off and a shift pulse occurs at C_2. Also, assume that the second binary changes states due to the same shift pulse on its input. The waveform of the pulse that occurs on the cathode of the diode is shown in Figure 21. This assumes that the pulse is narrow enough that no appreciable change of charge occurs on the input capacitor, C_2.

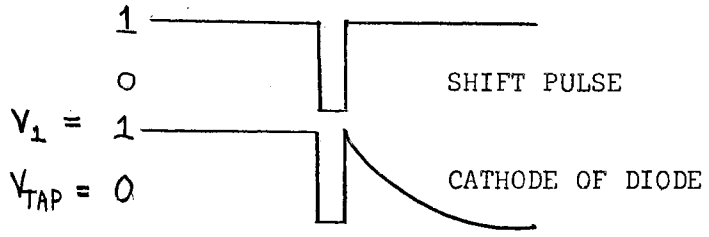


Figure 21. Cathode of Diode Pulse Waveforms

The voltage in the 1 state, V_1, is

$$V_1 = (E_1 - V_{be}) \frac{R_2 + R_3}{R_1 + R_2 + R_3} . \qquad (8\text{-}20)$$

The voltage in the 0 state or tap voltage is

$$V_{tap} = (E_1 - V_{ce}) \frac{R_2}{R_1 + R_2} . \qquad (8\text{-}21)$$

Because the cathode of the diode does not change states instantaneously, a pulse current will flow through the steering resitor. The pulse current will be a maximum when the binary initially changes state and then will decay to zero. Since there are two shift lines, the maximum pulse current, I_{cp}, will be

$$I_{cp} = \frac{V_1 - V_{tap}}{R_{12}} \quad 2 \qquad (8\text{-}22)$$

Approximate Collector Current

Combining Equation 8-3 and Equation 8-22, the total collector current is approximately

$$I_c = \frac{E_1 - V_{ce}}{R_9 + R_{10}} + 2 \left[\frac{V_1 - V_{tap}}{R_{12}}\right]. \qquad (8\text{-}23)$$

Referring to Equation 8-23, the steering resistor, R_{12}, should be large to keep the pulse component of the collector current small as possible.

There are at least four factors which involve the choice of R_{12} or the steering resistor. The maximum value is limited by the diode leakage and the rise and fall time of the cathode of the diode. The minimum value is limited by the collector pulse current and the superimposed voltage on the off collector of the adjacent binary.

In order to put Equation 8-23 in a usable form, the following approximations are made. Assume V_1 will not exceed 75% of the plus bus, E_1. Also assume that V_{tap} is equal to V_{ce}. In regard to the previous paragraph, assume that the steering resistor is at least eight times as large as $R_9 + R_{10}$. For most binaries these approximations are very pessimistic.

Equation 8-23 can be written as

$$I_c = \frac{E_1 - V_{ce}}{R_9 + R_{10}} - \frac{2(.75\ E_1 - V_{ce})}{8(R_9 + R_{10})} \qquad (8\text{-}24)$$

This simplifies to

$$I_c = \frac{9.5\,E_1 - 10\,V_{ce}}{8(R_9 + R_{10})} \quad . \tag{8-25}$$

Actual Design

The previous equations can not be used to design a binary since the number of unknowns will exceed the number of equations. Therefore, some of the unknown conditions must be either implied or given by the specifications and/or the nature of the problem.

Assume the following specifications are given:

1. The shift register must be capable of reading at rates up to 20 kc.
2. The maximum power per stage must not exceed 5 milliwatts.
3. E_1 and E_2 will be plus and minus six volts, respectively.

Assume the following conditions are either known or chosen:

1. The 1 and 0 state of the reset and transfer line are +7v and -0.3v, respectively.
2. A down tap voltage of +0.4 v is sufficient diode off bias.
3. A transistor off bias of -0.6v is sufficient.

From the transistor characteristics the following conditions are known:

1. V_{ce} of a saturated NPN transistor is approximately +.05v.
2. V_{be} of a silicon NPN transistor is approximately +0.6v. However, V_{be} changes about 2mv/C°. Therefore,

V_{be} ranges from approximately +0.4v to +0.8v as the temperature ranges from -50°C to +100°C.

Most of the power dissipated in the binary will be due to collector current. For a first approximation let the power be 3 mw. The D.C. collector current will be

$$I_{cdc} = \frac{P}{E_1 - V_{ce}} = \frac{3 \text{ mw}}{6\text{v} - .05 \text{ v}} = 0.505 \text{ ma}. \quad (8\text{-}26)$$

Equation 8-3 will be

$$R_9 + R_{10} = \frac{(6 - .05)\text{v}}{0.505 \text{ ma}} = 10 \text{ K} \ . \quad (8\text{-}27)$$

The maximum collector current due to the pulse condition can be found from Equation 8-25. It is

$$I_c = \frac{9.5(6\text{v}) - 10(.05)}{8(10 \text{ K})} = .700 \text{ ma}. \quad (8\text{-}28)$$

The values of R_9 and R_{10} can be obtained from Equation 8-5 and 8-27, respectively.

$$R_{10} = \frac{(6.0 - 0.65)}{0.65 - 0.5} R_9 \simeq 9 R_9 \ , \quad (8\text{-}29)$$

$R_9 + 9 R_9 = 10$ K, therefore, $R_9 = 1$ K, and

$$R_{10} = 9.1 \text{ K}.$$

The amount of base drive, I_b, depends largely upon the amount

of safety desired. The beta of the transistor is lowest cold, therefore, the minimum I_b necessary to hold the transistor in saturation for a particular I_c is observed when the transistor is cold. Figure 22 represents a hypothetical case.

Suppose $I_{b_{min}}$ is 20 microamps. For a safety factor of 6, I_b will be 120μa. When the temperature increases, the beta increases. Thus, The storage may become excessive. Whether or not the increase in

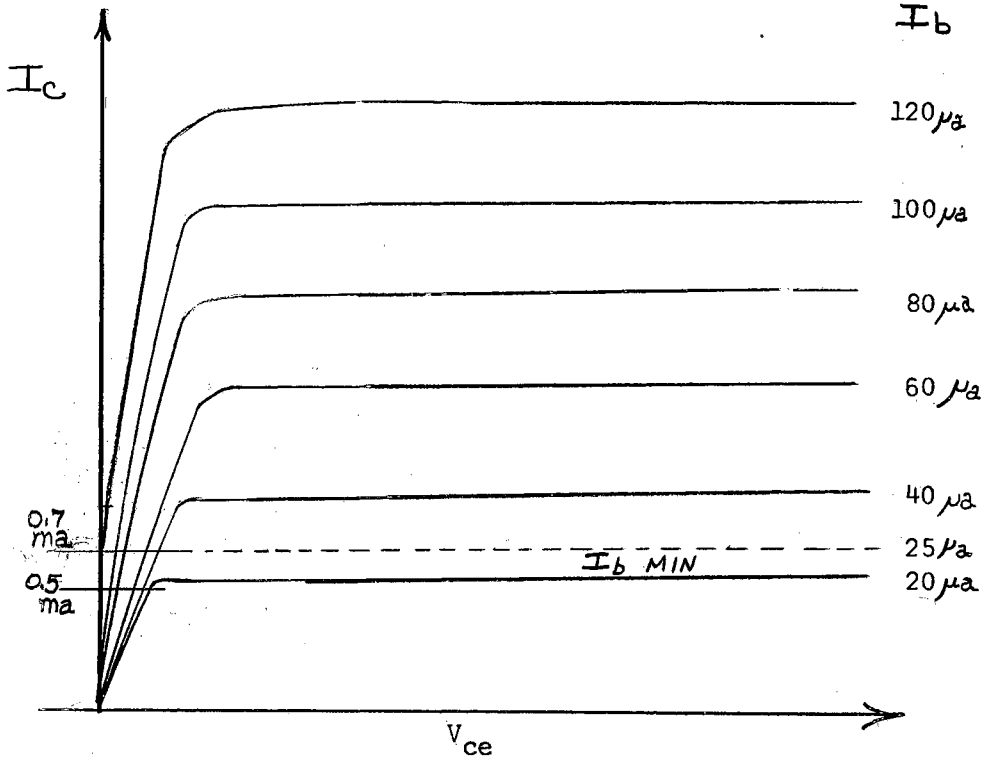


Figure 22. Transistor Characteristic Curves

storage time can be tolerated depends on the allowable switching time.

Equations 8-6, 8-12, and 8-10 can be solved for R_3, R_6, and R_7. Equation 8-6 will be

$$-0.6v = \frac{\{-6v(R_7 + R_6) + (-6.v + .3v)R_6\}R_7R_6}{\{R_7R_6 + R_3(R_7 + R_6)\}\ (R_7 + R_6)} . \qquad (8\text{-}30)$$

Assuming that an input pulse can not occur during reset, the collector current will be 500 microamps. For a safety factor of 6, I_b will be 120 microamps. Equation 8-12 will be

$$0.120 \text{ ma} = \frac{(7 - .8)v}{R_7} - \frac{(0.8 + 6)v}{R_6} - \frac{(0.8 - .05)v}{R_3} . \qquad (8\text{-}31)$$

Under normal conditions the collector pulse current must be considered. Referring to Figure 22, for a safety factor of 6, I_b will be 150 microamps. Equation 8-10 will be

$$0.150 \text{ ma} = \frac{(6 - 0.8)v}{(10\text{ K} + R_3)} - \frac{(0.8 + 6.0)v}{R_6} - \frac{(0.8 + 0.3)v}{R_7} . \qquad (8\text{-}32)$$

The solution of these three equations, to the closest standard resistor value, is

$$R_3 = R_8 = 16\text{ K},$$

$$R_6 = R_5 = 470\text{ K, and}$$

$$R_7 = R_4 = 33\text{ K}.$$

The solution of the three equations is somewhat tedious. Usually they are solved by trial and error based on previous experience.

From an earlier discussion, the steering resistor will be at least

eight times as large as $(R_9 + R_{10})$. Therefore, let R_{12} be 82 K. By knowing the maximum readout rate, Equation 8-18 can be used to solve for the input capacitors.

$$t_I = 2 \times 10^{-4} = (2.2)\ 82\ K + \frac{17\ K(9.1\ K)}{16\ K + 1\ K + 9.1\ K}\ C_2 \quad . \qquad (8\text{-}33)$$

The input capacitor will be

$$C_2 = \frac{10^{-4}}{2\ (2.2)(87.9\ K)} = 270 \times 10^{-12} \text{ farads.} \qquad (8\text{-}34)$$

In the constructed circuit the input capacitors are 300 pf.

The cross-coupling capacitors were determined experimentally. They are small enough so the superimposed voltage is not coupled onto the opposite base, but large enough to aid regeneration.

This completes the theoretical design, but only starts the actual design. In order to justify the approximations and to study non-linearities, which are only partially predictable, the binary should be breadboarded and studied with an oscilloscope.

CHAPTER IX

BIDIRECTIONAL SHIFT REGISTER EMPLOYING TWO SHIFT LINES

Once the method of cascading the binaries has been decided, the rest of the shift register will depend on the requirements of the input and output conditions. For instance, it is reasonable to assume that the circuits required to generate a shift pulse from a D.C. level input signal and a 100 kc input signal are different.

There are two types of input signals employed in this shift register. The first type is a solid chain of pulses. When this type is used, the shift pulses occur in groups of five. The frequency within the group will be approximately the same as the input frequency. The second type is produced by a manual operation. When this type is used, a single shift pulse will occur.

Referring to Figure 23, this shift register can be divided into the following sections:

1. Shift register binaries
2. Sequence binaries (W, X, and Y)
3. One-shots and gating necessary to produce groups of pulses
4. Pulse detection binary
5. Binary driver circuit

The circuit schematics are shown in Appendix A. The reasons for the various delays shown in Figure 23 will be discussed as their need arises.

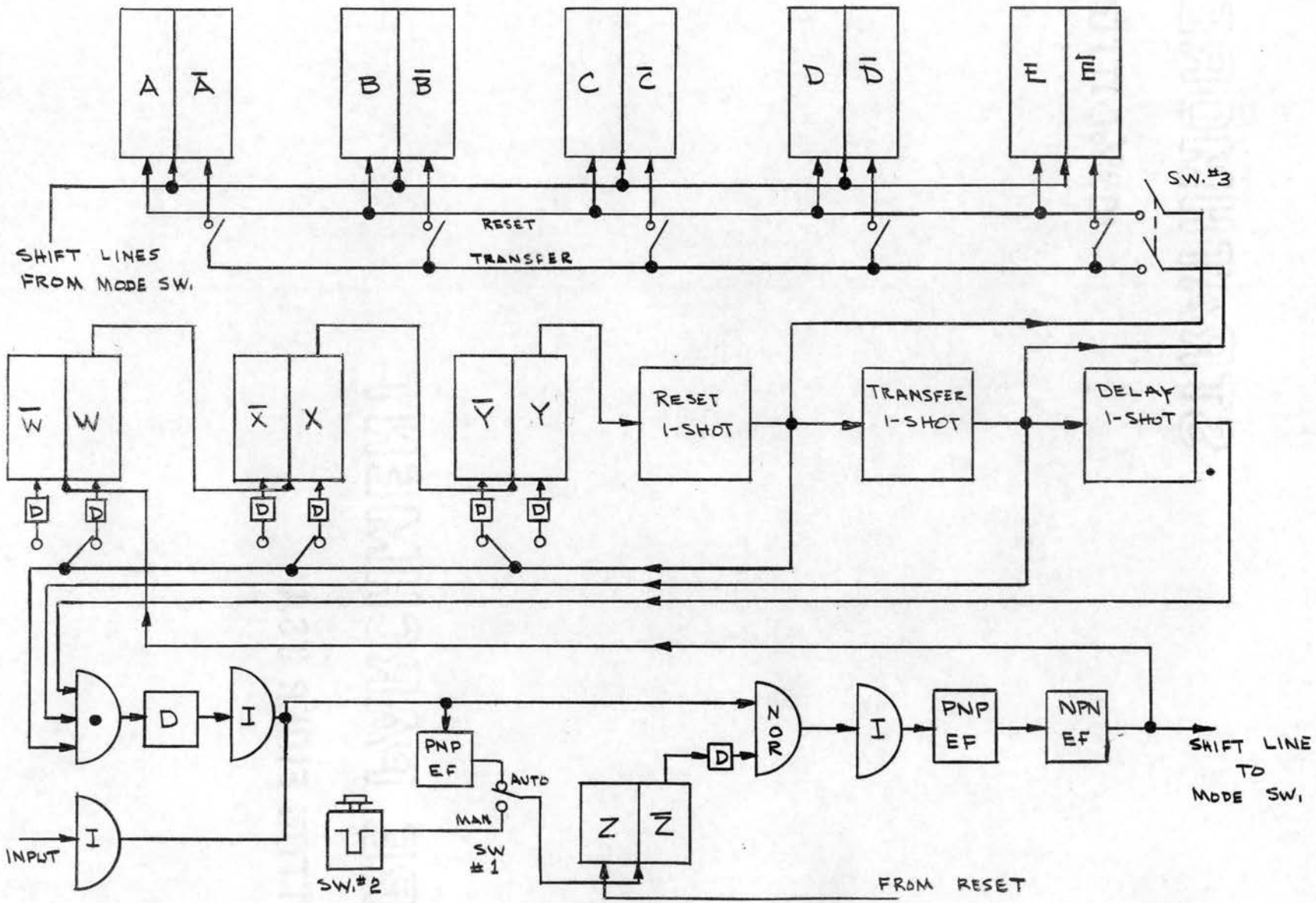


Figure 23. Shift Register Block Diagram

Shift Register Binaries

The shift register binaries need no further explanation. The detail interconnection is omitted from Figure 23. Since the mode of operation is selected by a manual switch, it is purely academic.

Sequence Binaries

The sequence binaries count the input pulses. When the Y output of the $Y\overline{Y}$ binary goes from 1 to 0 it will trigger the reset one-shot which will temporarily inhibit the input pulses. By means of single pole - two position toggle switches, the sequence binaries can be reset to any number from zero through seven. Reset in this manner, the sequence binaries will allow one to eight pulses per group.

Table XII illustrates a case where the sequence binaries are reset to three.

TABLE XII

POSSIBLE INITIAL CONDITIONS FOR SEQUENCE BINARIES

	Binaries			
	W	X	Y	
Reset	0	1	1	
First Pulse	1	0	0	
Second Pulse	1	0	1	
Third Pulse	1	1	0	
Fourth Pulse	1	1	1	← Reset one-shot triggered
Fifth Pulse	0	0	0	

When the fifth input pulse occurs, the Y output will drive the

reset one-shot.

One-shots and Gates Necessary to Produce Groups of Pulses

The reset, transfer, and delay one-shots are three series cascaded one-shots. When the reset one-shot is triggered, it will reset the shift register binaries, sequence binaries, and $Z\overline{Z}$. Also, the reset one-shot introduces a 1 into the G_1' gate. Thus, the output of the G_1' and G_1 gate will be 0 during the time of the reset one-shot. When the reset one-shot ends (goes from 1 to 0) it will trigger the transfer one-shot.

The transfer one-shot is a means of entering data into the shift register binaries. Each binary is connected to the output of the transfer one-shot by means of a two position slide switch. If the switch is open, the binary will remain in the reset condition when the transfer one-shot goes. When the shift pulses arrive, the newly introduced data will be shifted out.

Also, the transfer one-shot introduces a 1 into the G_1' gate. Thus, the output of the G_1' and G_1 gate will be a 0 during the time of the transfer one-shot. When the transfer one-shot ends, it will trigger the delay one-shot.

The delay one-shot provides a delay between the end of the transfer one-shot and the shift pulses. It accomplished this by introducing a 1 into the G_1' gate.

When the three one-shots end, the output of the G_1 gate will depend only on the state of the input pulse. After a predetermined amount of input pulses have been admitted, the Y binary will change states and start the one-shot action again. Hence, the input pulses will be

temporarily blocked.

Figure 24 illustrates a case where the sequence binaries are reset

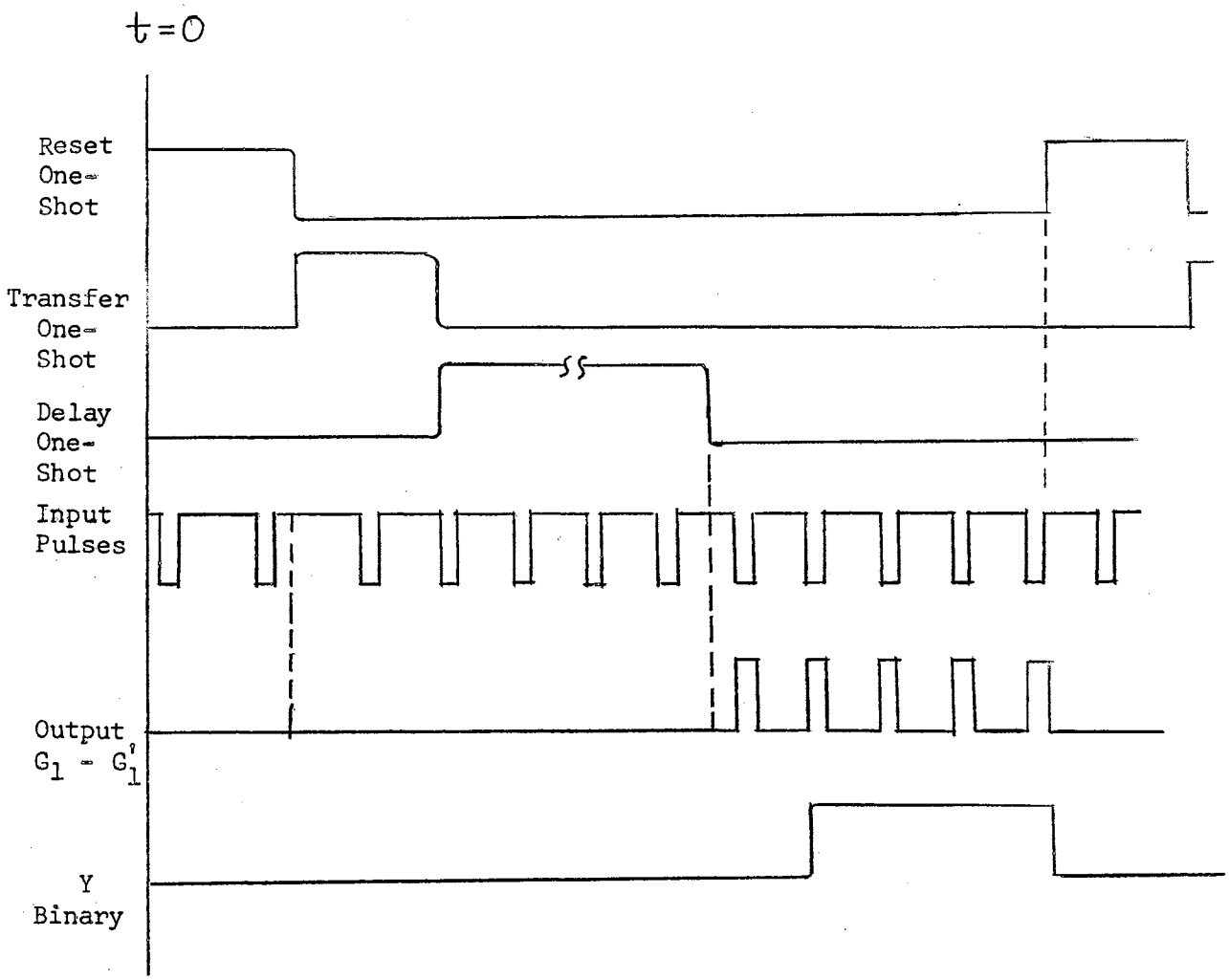


Figure 24. Timing Diagram of One-shots

to three. Referring to Figure 24, the trailing edge of the one-shot triggers the following one-shot. Since the following one-shot can not go from 0 to 1 instantaneously, a time will exist when both outputs are approximately 0. Hence, the output of the G_1 and G_1' gates will erroneously pulse to a 1. This is illustrated in Figure 25a.

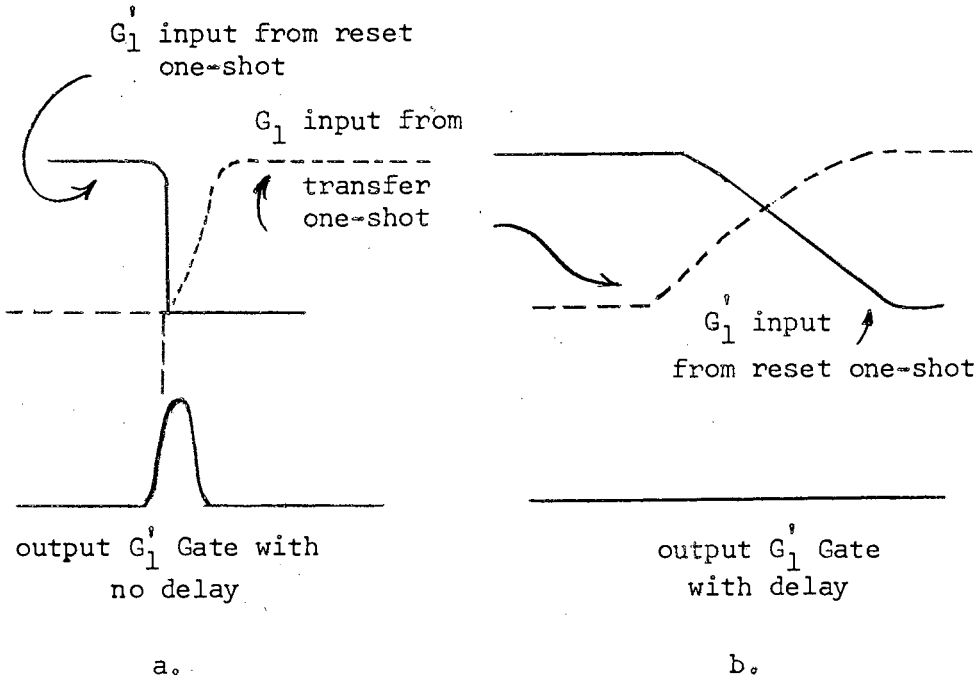


Figure 25. G_1 and G_1' Gate Output

This problem is solved by employing a delay on the input of the G_1' gate.

Pulse Detection Binary

Referring to Figure 24, suppose the delay one-shot ends during a shift pulse. The first pulse out of the G_1 and G_1' gates will not be as wide as the input pulse. If the shift pulse were derived directly from their output, its initial width would be unpredictable. In fact, the pulse might become so narrow that it could trigger some of the binaries but, due to difference in regeneration time, fail to trigger others. The $Z\bar{Z}$ binary solves this problem.

Referring to Figure 23, the Z output of the $Z\bar{Z}$ binary in the reset

state holds a 1 into the G_3 gate. Thus, the output of G_3 rests at 0. Unless $Z\overline{Z}$ changes states, G_3 will remain at 0 regardless of the output of G_2. In other words, the effect of G_2 upon G_3 is blocked by the 1 from the $Z\overline{Z}$ binary. Now assume G_2 has an output pulse. If the pulse is wide enough, it will trigger $Z\overline{Z}$. Assuming the delay from Z into G_2 is longer than the pulse, the output of G_3 will remain 0. However, until $Z\overline{Z}$ is reset, the remaining pulses out of G_2 will not be blocked. Thus, the pulses out of G_3 will always have the same width. These pulses, after going through the binary driver circuit and the mode switch, are used to shift the shift register. The $Z\overline{Z}$ binary serves a different purpose during manual operation. This is explained in Chapter X.

Binary Driver Circuit

The binary driver circuit is a PNP-NPN double emitter follower. The NPN emitter follower provides a low impedance path for the binary input capacitors to recharge through. This keeps the trailing edge of the shift pulse from being loaded.

The PNP emitter follower provides a negative trigger to the binaries that will not be loaded when the binaries are toggled.

CHAPTER X

TESTING

The system was tested automatically and manually in the four modes of operation. Figure 26 is a timing diagram for a complete automatic cycle when the data is not recirculated. The timing diagram is started in the reset condition. Consider the data as (1 0 1 0 1), assuming the static input conditions to the $A\overline{A}$ binary cause the A side to rest at 0 after the first shift pulse.

When the transfer one-shot goes, it will transfer the data into the shift register binaries. The $Z\overline{Z}$ binary will be triggered by the first input pulse (or part of a pulse) that occurs after the delay one-shot ends. Because of the delay from Z into the G_3 gate, the next input pulse will be the first shift pulse.

Referring to Figure 26, the following table can be made.

TABLE XIII

TEST DATA SHIFTED TO THE RIGHT WITHOUT RECIRCULATION

	A	B	C	D	E
Rest	1	0	1	0	1
First Shift	0	1	0	1	0
Second Shift	0	0	1	0	1
Third Shift	0	0	0	1	0
Fourth Shift	0	0	0	0	1
Fifth Shift and Reset	0	0	0	0	0

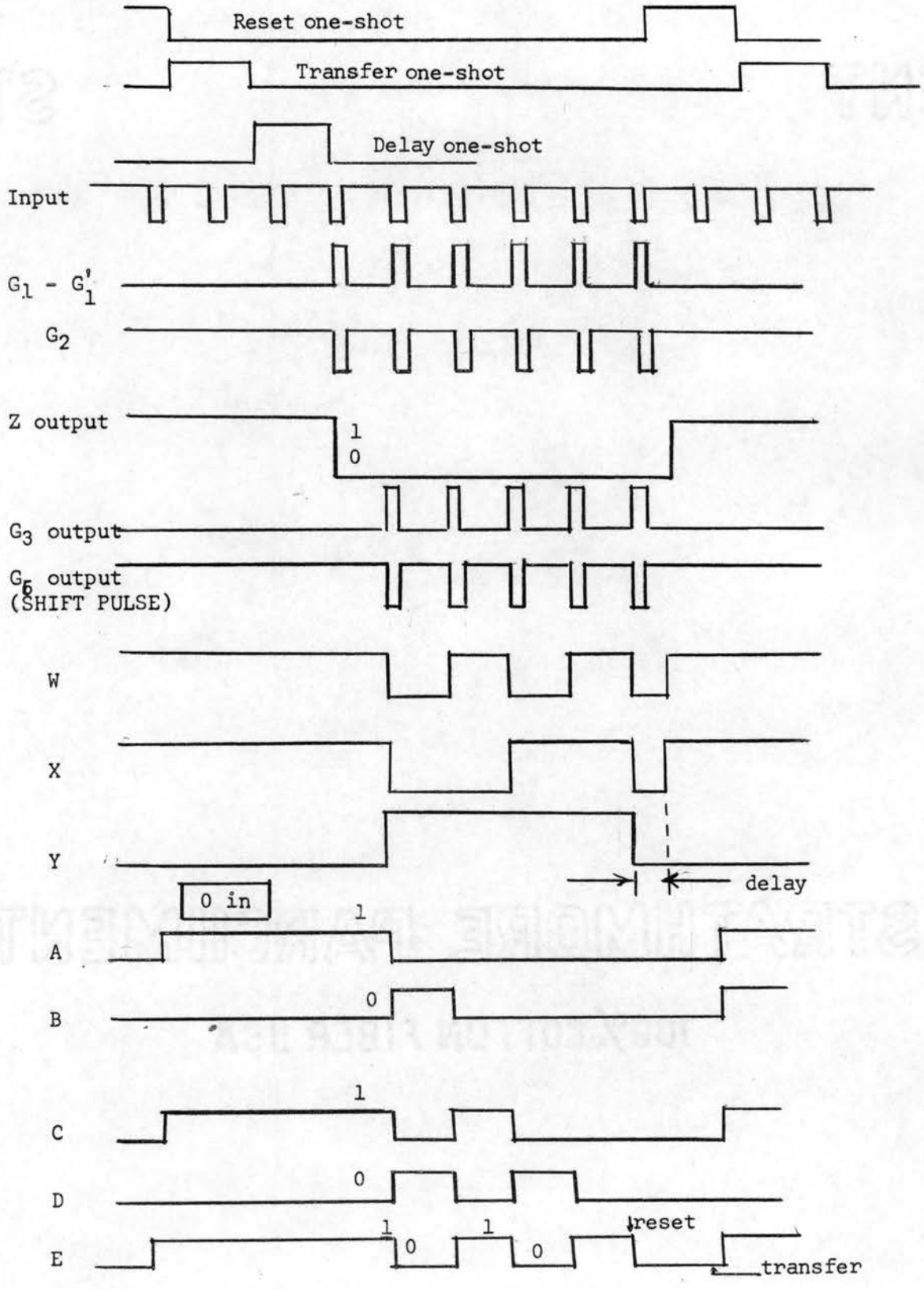


Figure 26. Automatic Cycle Timing Diagram Without Recirculation

Several interesting things can be observed either from Figure 26 or Table XIII. It takes only (n - 1) pulses to shift the data from n binaries. This fact was mentioned earlier in Chapter I. This implies that the output binary must be monitored either before or as the first shift pulse arrives. In other words, if the data in the binary preceding the output binary and the data in the output binary are different, the output binary must change when the first pulse arrives. Therefore, to know the initial condition of the output binary it must be monitored before or as the first shift pulse arrives.

Because of the static conditions into the $A\overline{A}$ binary, the binaries will rest at a zero after the fifth shift pulse. Likewise, if the static input conditions into the $A\overline{A}$ binary are reversed, the binaries will rest at a one after the fifth shift pulse. However, reset would immediately reset the binaries to zero, thus causing a spike on the output of the shift register.

The following question may arise. If the fifth shift pulse can return the binaries to the reset condition, why have a reset? Likewise, if reset is present, why have an n^{th} shift pulse (in this case, fifth)? This will depend entirely upon the requirements of the shift register.

For instance, in recirculating the shift register the n^{th} shift pulse is necessary to keep recirculating the data. In this case the n^{th} pulse does not return the binaries to the reset condition. Reset is necessary to cancel the present data so that new data can be entered for recirculation.

Also, in some cases the n^{th} shift pulse may be necessary and the reset pulse is only a redundant safety feature.

The purpose of the delay into G_1' and G_3 is twofold. The reset one-shot is triggered on the leading edge of the n^{th} shift pulse,

which in turn resets the $Z\bar{Z}$ binary. The delay into G_1' keeps the reset one-shot from blocking what remains of the n^{th} pulse. Likewise, the delay into G_3 keeps the $Z\bar{Z}$ binary from blocking the G_2 pulse, or in effect, the remaining part of the n^{th} pulse. In other words, the two delays keep the n^{th} shift pulse from being a partial pulse.

After the system has been reset, the transfer one-shot will enter new data. Figure 26 shows a (1 1 1 0 1) being entered.

The system was tested under the same conditions except the data was recirculated. The lower part of Figure 27 has been redrawn to illustrate this case. Consider the data as (1 1 0 0 1). Since the data is being recirculated, the reset and transfer one-shots can not be allowed to drive the shift register binaries until new data is desired. This is the purpose of switch 3.

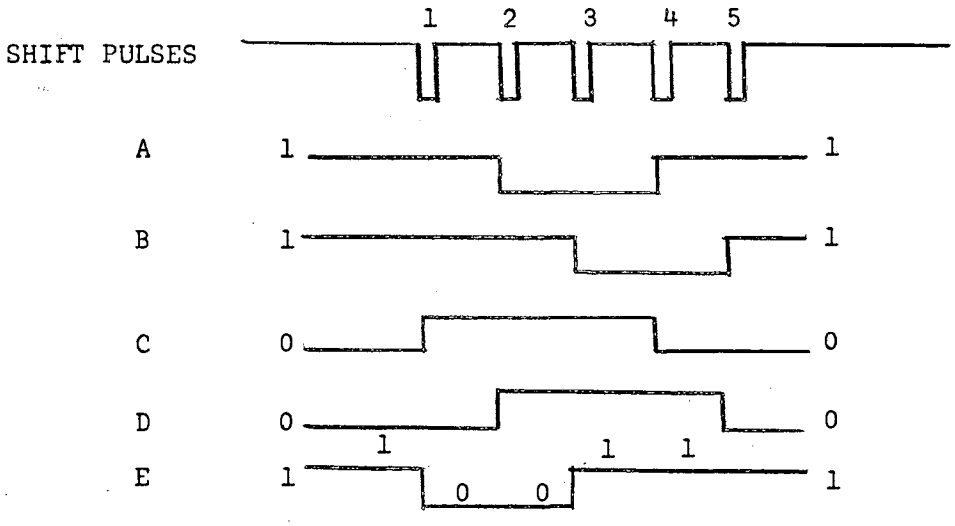


Figure 27. Automatic Cycle Timing Diagram with Recirculation

At the end of the (n - 1) shift pulse the data is (1 0 0 1 1). Therefore, the n^{th} shift pulse is necessary to return the binaries to the initial condition. However, the binaries will never return to the reset conditions unless they are externally reset.

Suppose, by means of the mode switch, the binaries are connected to shift to the left. Assuming that all of the initial data conditions are the same, if the first binary is used as the output binary, the timing diagram in Figure 26 and Figure 27 will be the same. The design considerations and methods of testing are the same regardless of the direction of shifting.

The manual means of operation is only provided for the convenience of test and demonstration. Provided the maximum input frequency is not exceeded, the shift register is independent of the input frequency. Therefore, the timing diagram in Figure 26 and Figure 27 will be basically the same. Only the time between shift pulses and the corresponding events will be changed.

Figure 28 is a timing diagram illustrating the new data being entered and then shifted one place. The sequence binaries are reset in the (1, 1, 1) condition for W, X, and Y. Switch 1 should be in the manual position. Again consider the data to be entered as (1 0 1 0 1). The cycle will start by manually triggering the $Z\overline{Z}$ binary.

Referring to Figure 28, the input pulses still enter at a constant frequency. Also, unless one of the one-shots is blocking them, the G_1, G_1', and G_2 gates are pulsing. However, with switch 1 in the manual position the $Z\overline{Z}$ binary will not be triggered.

When the $Z\overline{Z}$ binary is manually triggered, it changes states and

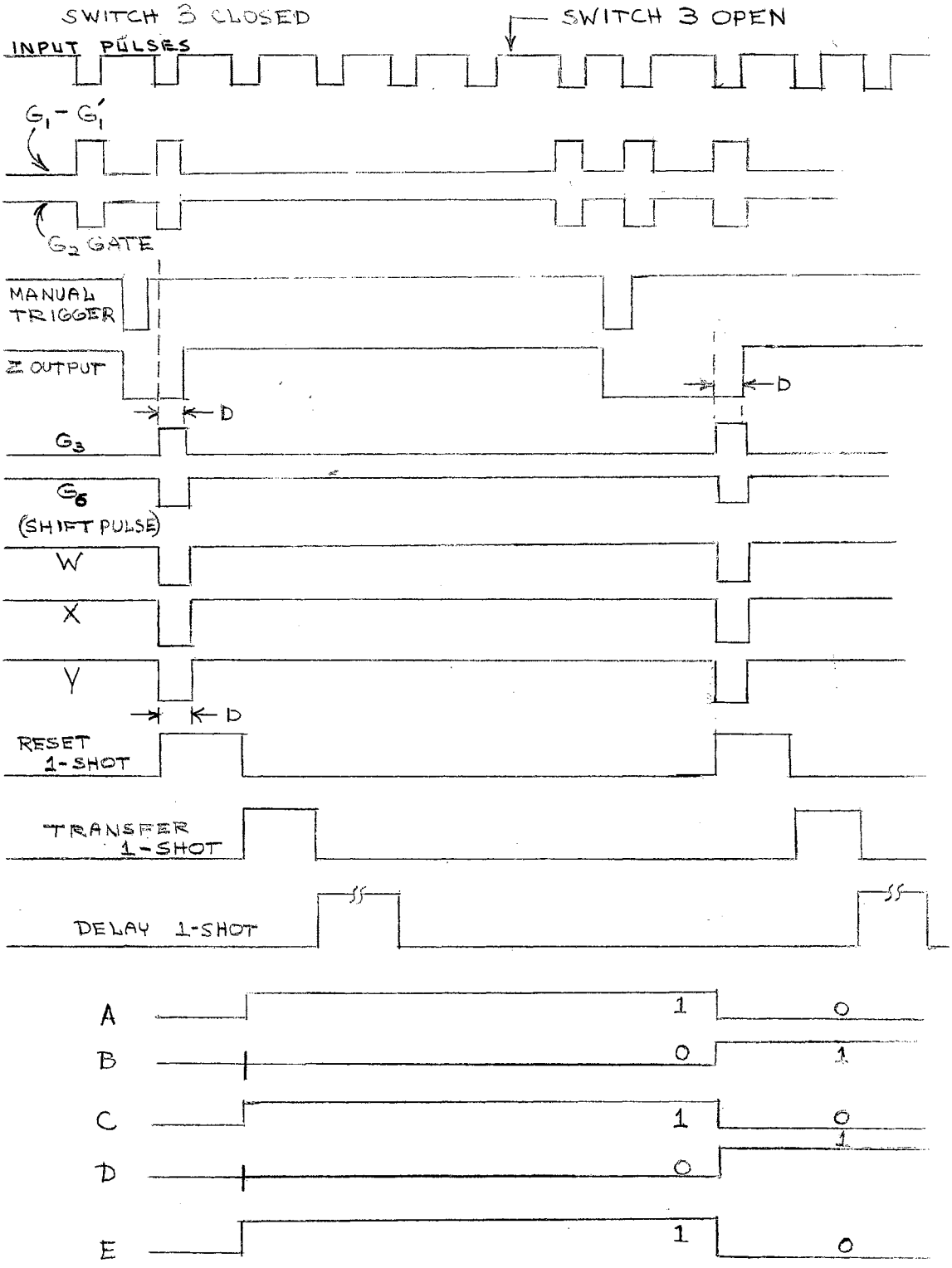


Figure 28. Manual Cycle Timing Diagram

and unblocks the G_3 gate. With the G_3 gate unblocked, a shift pulse will occur.

Since the sequence binaries are reset in the (1, 1, 1) condition it will take only one pulse to change them to the (0, 0, 0) condition, hence, triggering the reset one-shot. The reset one-shot immediately resets the sequence binaries back to (1, 1, 1). The delays into the sequence binaries retard this action and allow their output pulse to be more substantial than it would normally be.

Also, the reset one-shot will temporarily block the input pulses and reset the $Z\bar{Z}$ binary. The $Z\bar{Z}$ binary will again block the G_3 gate. Therefore, only one shift pulse will occur.

When the reset one-shot ends it will trigger the transfer one-shot and the new data will be entered into the shift register binaries. When the delay one-shot ends, the G_1, G_1', and G_2 gates will start pulsing again. The system will remain in this condition until the $Z\bar{Z}$ binary is manually triggered again.

Switch 3 should be opened before the $Z\bar{Z}$ binary is triggered again. Otherwise, the next cycle will reset the shift register binaries and enter new data. A shifting process will not occur; however, with switch 3 open the shift pulse will shift the data one place for each manual trigger. The mode of operation has no effect upon this action.

The following steps summarize manual operation:

1. Data is entered by closing switch 3 and triggering the $Z\bar{Z}$ binary.
2. With switch 3 open the data is shifted one place for each manual trigger.
3. New data can be entered by closing switch 3 and triggering the $Z\bar{Z}$ binary, then reopening the switch.

The A.C. conditions of the shift register binaries were checked to verify the approximations made in Chapter VIII.

Equation 8-14 gives the approximate rise time of the off going collector. The time is

$$t_r = 2.2 \frac{(10.1\ K)(16\ K)}{26.1\ K} (160 \times 10^{-12}) \text{ seconds} =$$

$$2.16 \text{ microseconds.}$$

The measured time was 2.5 microseconds.

Equation 8-19 gives the approximate rise and fall time of the cathode of the diode. The time is

$$t = 2.2(82 \times 10^{3})(300 \times 10^{-12}) \text{ seconds} =$$

$$54.1 \text{ microseconds.}$$

The measured time was 58 microseconds.

CHAPTER XI

SUMMARY

The original problem was to discuss and build a low-power bidirectional shift register capable of shifting at rates up to 20 kc. To better understand the problems that would be encountered, a considerable amount of discussion was devoted to shift registers in general.

Two types of bidirectional shift registers are included in this paper. One type depends upon gating between stages. Whereas, the second type depends upon two sets of steering components.

In actual operation the latter type seems to satisfy all of the requirements of the desired bidirectional shift register. In other words, it shifts either direction, with or without recirculating, at rates up to 20 kc. Its large advantage over the first type discussed is that it takes considerably few transistors per stage (four in this case).

A bidirectional shift register can be further investigated by either finding a method entirely different from these two or by using cores, thin films, or some other two-state device for storage elements.

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APPENDIX A

With the exception of the shift register binary, the schematics of the circuits used in this thesis are shown in this appendix.

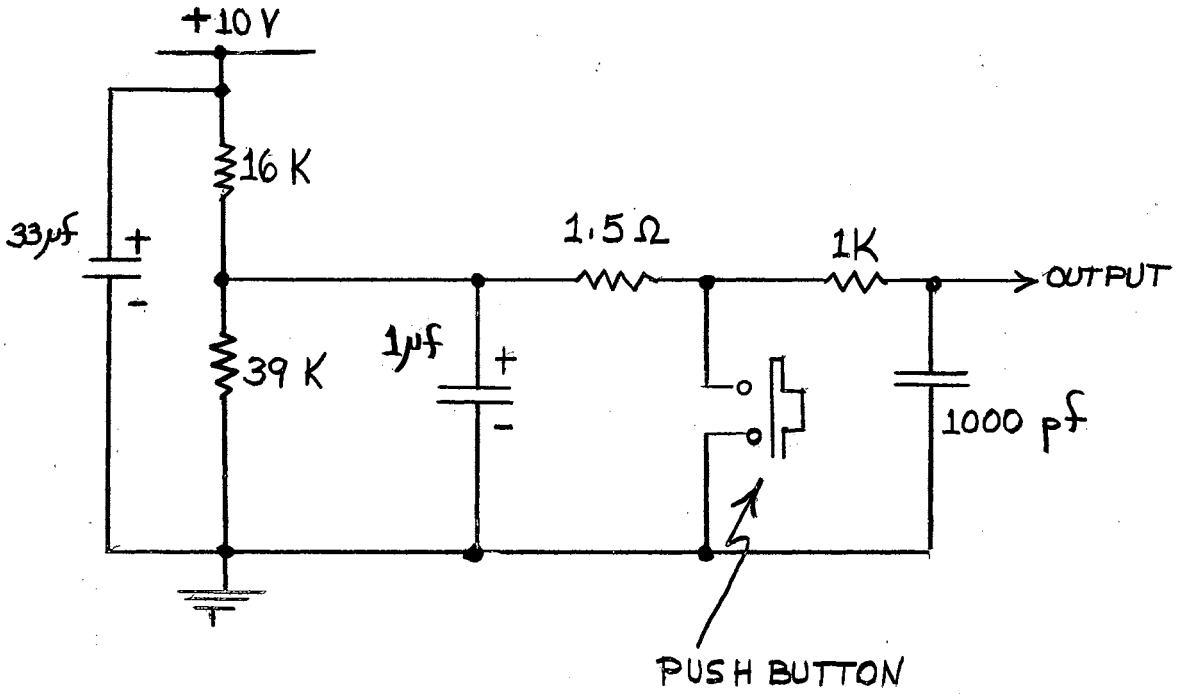


Figure 29-a. Manual Trigger Circuit

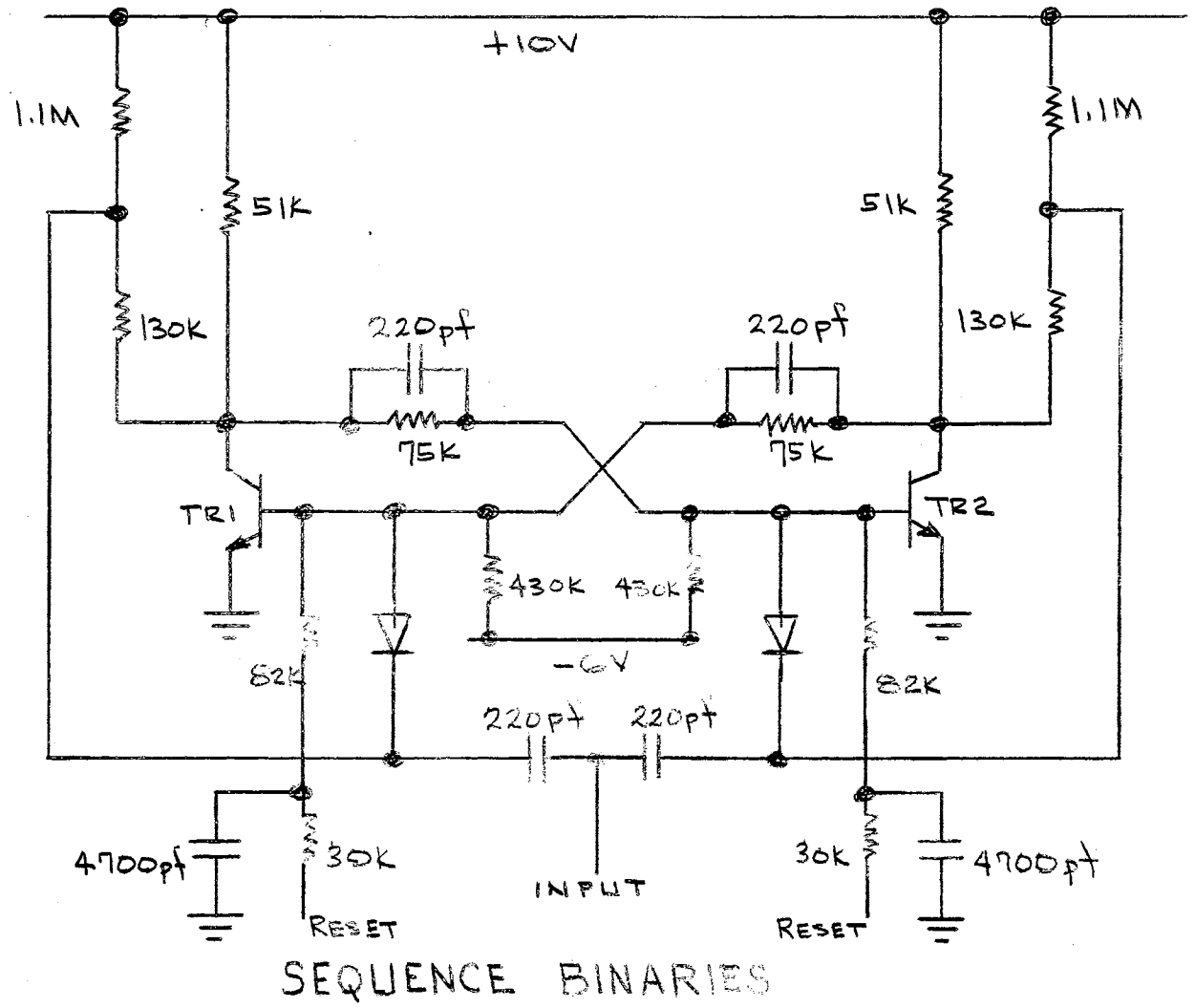


Figure 30-a. Schematic of Sequence Binaries

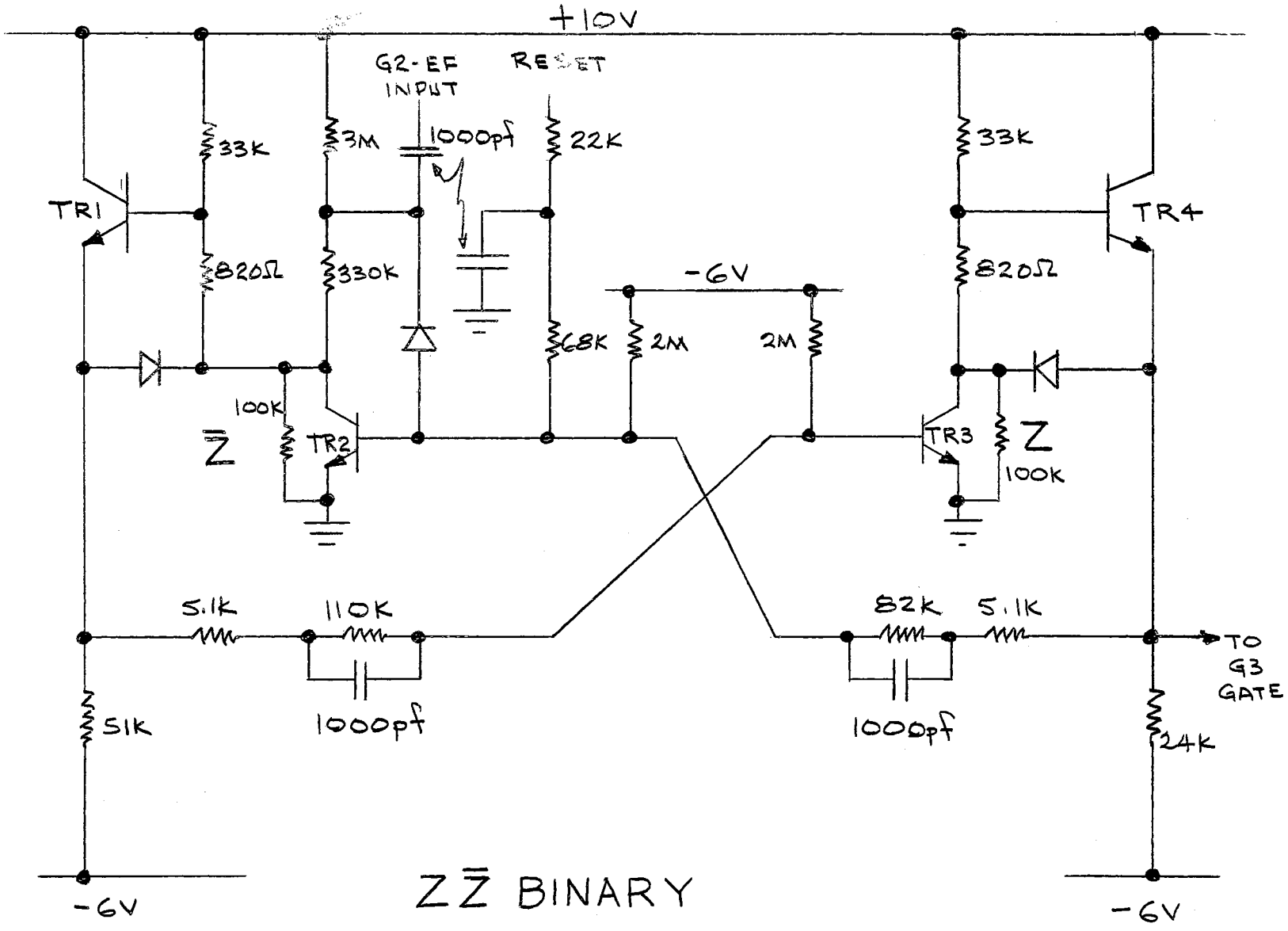
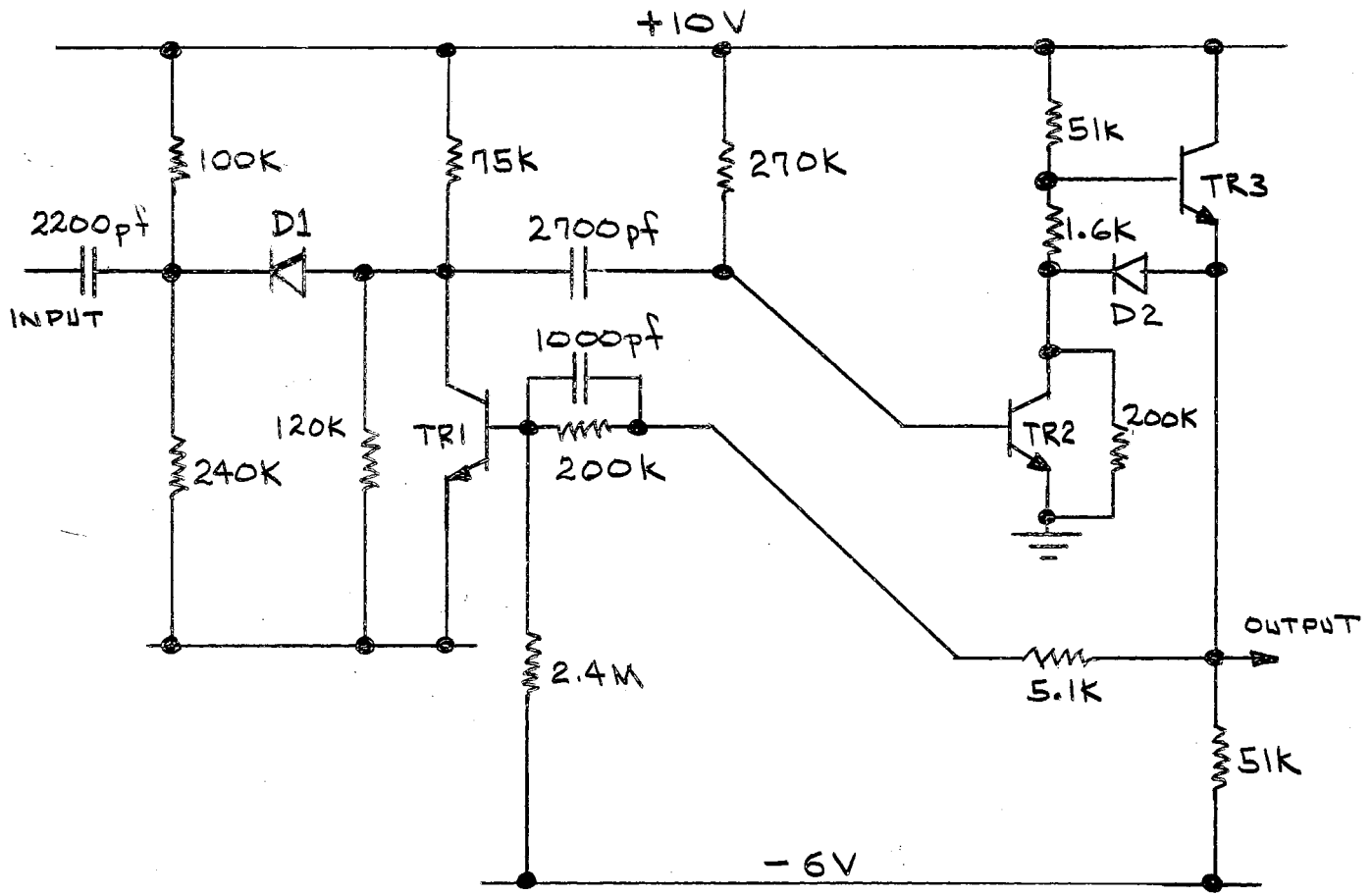


Figure 31-a. Schematic of $Z\bar{Z}$ Binary



ONE-SHOTS

Figure 32-a. Schematic of One-Shots

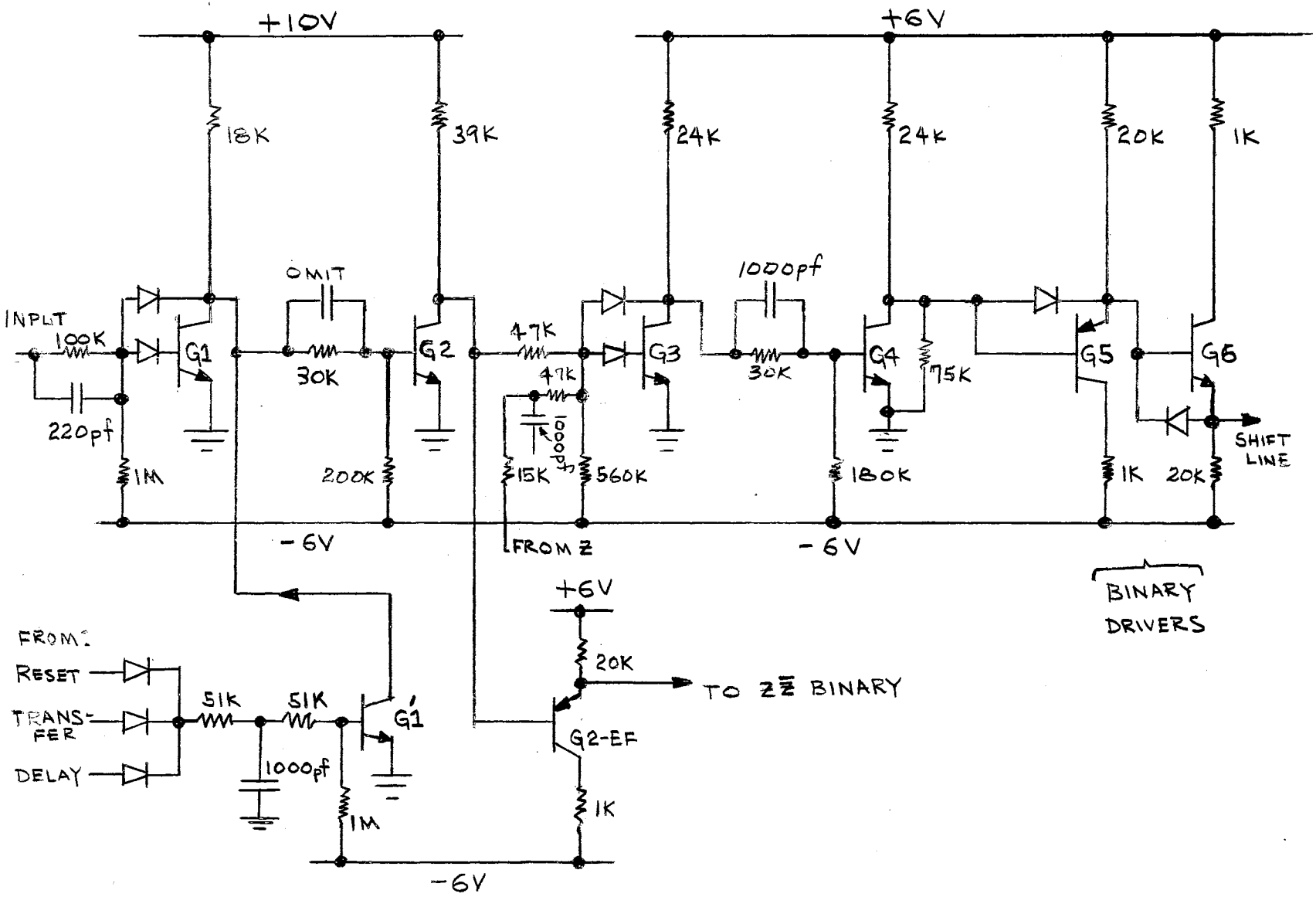


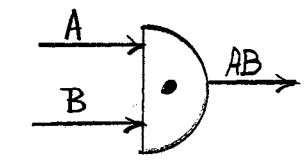
Figure 33-a. Schematic of Gating

APPENDIX B

LOGIC SYMBOLS

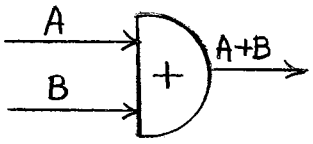
The logic symbols used in this thesis are listed below. Positive logic convention is used.

AND GATE



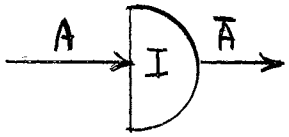
Inputs		Output
A	B	AB
0	0	0
1	0	0
0	1	0
1	1	1

OR GATE



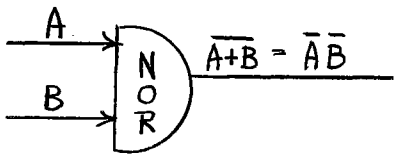
Inputs		Output
A	B	A + B
0	0	0
1	0	1
0	1	1
1	1	1

INVERTER



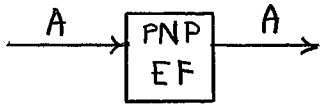
Inputs	Output
0	1
1	0

NOR GATE



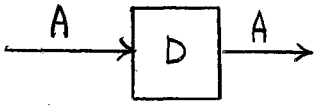
Inputs		Output
A	B	$\overline{A + B} = \bar{A} \cdot \bar{B}$
0	0	1
0	1	0
1	0	0
1	1	0

An emitter follower employing a PNP transistor is represented as follows.

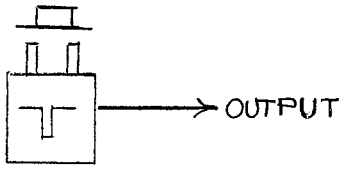


An emitter follower employing a NPN transistor is represented as follows.

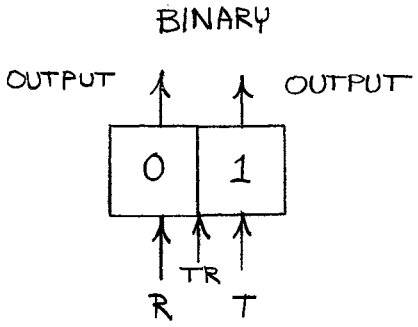
A R-C circuit used to delay a signal is represented as follows.



A circuit used to generate a single negative pulse for each operator is represented as follows



R, TR, and T denote the reset, trigger and transfer input lines, respectively.



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Honor Organizations: Phi Kappa Phi.