A BINARY ARITHMETIC UNIT FOR A MAGNETIC DRUM DIGITAL SYSTEM

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PREFACE

Since digital computers are commonplace in all fields of engineering today, it is fundamental that the engineer possess a working knowledge of them. With this in mind, the School of Electrical Engineering of the Oklahoma State University has undertaken the design and construction of a small digital system to be used for demonstration and instructional purposes in computer engineering courses. The operational aspects of one type of digital system, one using a magnetic drum for the memory unit, have been thoroughly described in the literature. (1). The design of this system was based on the maximum utilization of a quantity of components donated by the Continental Oil Company of Ponca City, Oklahoma. Full use of available components resulted in the design of a binary, parallel, single-address magnetic drum machine.

Physical realization of this system is now under way. Work is being done on a power supply for the machine, and on the read/write mechanism. A memory address selection system has been completed and satisfactorily tested. (2). This study is concerned with the design, construction, and operation of another main system component, the arithmetic unit.

The author expresses sincere thanks to his adviser, Professor Paul A. McCollum, for his counsel, guidance, and encouragement. These contributions are greatly appreciated.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER I

THE MAGNETIC DRUM DIGITAL SYSTEM

This study is concerned with an ARITHMETIC UNIT for a magnetic drum digital system. To provide a full understanding of the design, construction, operation and testing of a unit such as this, one must begin by considering the system as a whole.

The purpose of any digital system is to perform operations on input information, transforming it into output information. There are numerous methods of entering, transforming, and discharging these quantities, each having its individual application.

In a binary, parallel, single-address system, information is obtained from the memory and placed in a storage register. There, the information is analyzed and executed, the latter possibly involving the obtaining from or storing into the memory of information. The major components of this system include the following:

(A) The MAGNETIC DRUM. The drum used has 3072 locations for storage of 20 bit words. It rotates at a nominal 3450 revolutions per minute, and has a permanently machined timing track which

provides 2560 timing pulses per drum revolution. These are divided into groups of five pulses, 6.8 microseconds apart, to provide a word time of 34.0 microseconds. The five pulses are denoted as 0 time (the first pulse in one word time), 1 time, 2 time, 3 time, and 4 time (the last pulse in the sequence). The next pulse would then be 0 time for the following word. Another representation of the pulses is T0, T1, T2, T3, and T4.

(B) The word DISTRIBUTOR, or D-REGISTER. This unit is used to store the current information which it receives from the drum and delivers to the drum.

(C) The INSTRUCTION COUNTER, used to keep track of the location of the next instruction. (2).

(D) The ARITHMETIC UNIT, or ACCUMULATOR, which performs the computational operations. In simple systems, a basic unit called an ACCUMULATOR, which adds and stores, sometimes suffices. For more sophisticated operations, auxiliary registers such as a shift register are necessary, forming an ARITHMETIC UNIT.

The system is powered by a regulated power supply furnishing 12.6 VAC, 200 VDC, 110 VDC, 90 VDC, -140 VDC, and -160 VDC.

Figure 1 shows a block diagram of the system.

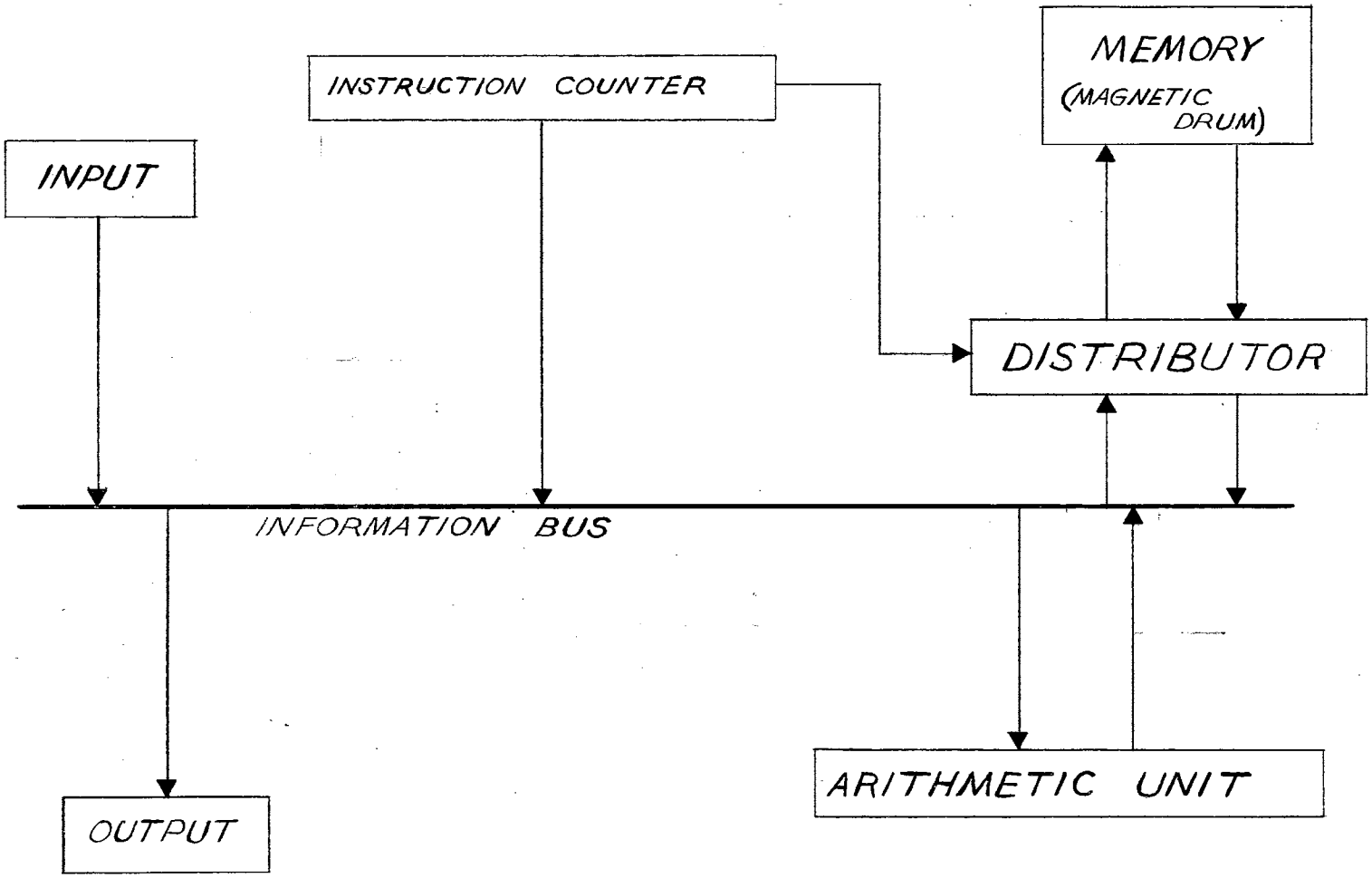


Figure 1. A Magnetic Drum Digital System

FIGURE II

OPERATION OF THE ARITHMETIC UNIT

The first step in the design of an ARITHMETIC UNIT or an ACCUMULATOR is the definition of the rules of operation and the logic used. In a binary system, the only possible states are 0 and 1. These values may in actuality be any two different quantities. Due to the availability of 90 VDC and 110 VDC, these levels are used in the circuitry. A logical 0 will also be referred to as DOWN, LOW, TURNED ON, or CONDUCTING, and a logical 1 referred to as UP, HIGH, TURNED OFF, or NON-CONDUCTING in subsequent discussions.

It is desired that this system perform addition, subtraction, and multiplication of 18 bit binary numbers. These numbers are stored in the system in "sign and magnitude" binary form. A single operation is to be executed in a maximum of 27 microseconds, in order that an answer be available by 4 time (27.2 microseconds after T0). The unit will provide space for an 18 bit UPPER ACCUMULATOR REGISTER, an 18 bit LOWER ACCUMULATOR REGISTER, a SIGN bit, and a TALLY or TEST bit, for a total of 38 spaces. These registers also will be referred to individually as UPPER and LOWER, or together as the ACCUMULATOR. It must

be capable of receiving information into either the UPPER or LOWER REGISTER, of shifting the contents of the entire ACCUMULATOR either to the right or to the left, and of entering the left-most digit into the right-most space on a left shift operation (end-around carry). Other requirements are ease of entering and discharging information, reliability, simplicity, and ease of diagnosing and correcting malfunctions. A desired feature is adaptability to minor system changes, since the machine was designed for use as an instructional computer.

Although in combination with the shift register the ACCUMULATOR performs all the mentioned arithmetic operations, the unit is basically capable only of addition and shifting. These two operations are sufficient, however, since subtraction, division, and multiplication are possible with proper use of them.

In an addition operation, the contents of the DISTRIBUTOR are added to the contents of the UPPER or LOWER REGISTER, together with the accompanying signs. If two positive numbers are added, the answer is positive and correct, and no end-around carry must occur (presence of an end-around carry in this case indicates an overflow of the register). If two negative numbers are added, the answer must be complemented, and end-around carry must occur (absence indicating overflow). If two numbers of opposite signs are added, overflow is impossible, and the presence of an end-around carry indicates no complement is necessary

(answer is correct), while the absence of an end-around carry indicates the need to complement the answer. A negative number in the DISTRIBUTOR is complemented before addition into the UPPER/LOWER ACCUMULATOR, and along with this, a word composed entirely of 1's is added into the LOWER/UPPER ACCUMULATOR. A negative ACCUMULATOR number as an augend requires that the entire ACCUMULATOR be complemented before addition takes place. Since subtraction is identical to the addition of a negative addend to an augend, the operations described above are sufficient to add or subtract positive and/or negative numbers. Table I shows examples of each of the four possible combinations. The registers have been abbreviated to 4 bit capacity in this illustration, since the principles are valid with registers of any capacity.

Multiplication involves repeated sequences of shifting, testing, and addition. The multiplier is placed in the UPPER and the LOWER is set to zero. The multiplicand is placed in the DISTRIBUTOR. The first operation is a left shift of the entire ACCUMULATOR, resulting in the left-most multiplier digit being placed in the TEST position. If the test reveals a "1", the contents of the DISTRIBUTOR are added to the LOWER, and the ACCUMULATOR is then shifted left again. If the test shows a "0", no addition is performed, and the shift follows directly. These operations are continued until 18 sequences (corresponding

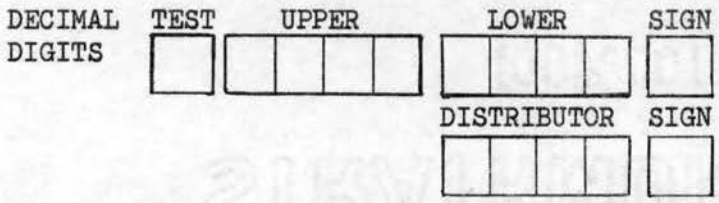
to the number of bits in the number) have been completed. No overflow is possible, since the maximum product of two 18 bit numbers is a number 36 bits in length, the length of the entire ACCUMULATOR. The sign bits are not added or shifted. The sign is set to "0" (positive) if both multiplier and multiplicand are of the same sign, and to "1" (negative) if the signs are opposite. Table I shows a sample multiplication using 4 bit words.

Although not a specific design requirement, the ARITHMETIC UNIT could be made to perform division in a similar fashion, using shifting, subtraction, and testing. Several suitable methods might be devised, differing perhaps in the initial location of divisor and dividend, and restrictions as to their relative magnitudes.

TABLE I

BINARY ADDITION AND MULTIPLICATION

FORMAT



DESCRIPTION/OPERATION

CASE I ADDITION OF TWO POSITIVE NUMBERS

+4	0 0 0 0	0 1 0 0	0	ACCUMULATOR at start
+3		0 0 1 1	0	DISTRIBUTOR at start
+7	0 0 0 0	0 1 1 1	0	Correct answer

CASE II ADDITION OF TWO NEGATIVE NUMBERS

-4	0 0 0 0	0 1 0 0	1	ACCUMULATOR at start
-3		0 0 1 1	1	DISTRIBUTOR at start
	1 1 1 1	1 0 1 1	1	ACCUMULATOR complement
	1 1 1 1			Add 1's to UPPER
		1 1 0 0	1	DISTRIBUTOR complement
	1 1 1 1 1	1 0 0 0	0	Partial sum
			1	Add the end-around carry
	1 1 1 1	1 0 0 0	1	Complement is necessary
-7	0 0 0 0	0 1 1 1	1	Correct answer

CASE III ADDITION WITH AUGEND POSITIVE, ADDEND NEGATIVE

+4	0 0 0 0	0 1 0 0	0	ACCUMULATOR at start
-3		0 0 1 1	1	DISTRIBUTOR at start
	1 1 1 1	0 1 0 0	0	Add 1's to UPPER
		1 1 0 0	1	DISTRIBUTOR complement
	1 0 0 0 0	0 0 0 0	1	Partial sum
			1	Add the end-around carry
+1	0 0 0 0	0 0 0 1	0	Correct answer

CASE IV ADDITION WITH AUGEND NEGATIVE, ADDEND POSITIVE

-4	0 0 0 0	0 1 0 0	1	ACCUMULATOR at start
+3		0 0 1 1	0	DISTRIBUTOR at start
	1 1 1 1	1 0 1 1	1	ACCUMULATOR complement
		0 0 1 1	0	DISTRIBUTOR
	1 1 1 1	1 1 1 0	1	Partial sum. No end-around carry. Complement is necessary.
-1	0 0 0 0	0 0 0 1	1	Correct answer

TABLE I (Continued)

MULTIPLICATION OF TWO POSITIVE NUMBERS

+4	0 0 1 0 0	0 0 0 0 0	ACCUMULATOR at start
+3		0 0 1 1 0	DISTRIBUTOR at start
	0 1 0 0 0	0 0 0 0 0	ACCUMULATOR Left Shift number 1
			Test shows 0
	1 0 0 0 0	0 0 0 0 0	ACCUMULATOR Left Shift number 2
			Test shows 1, Add
		0 0 1 1 0	DISTRIBUTOR
	1 0 0 0 0	0 0 1 1 0	Partial sum
	0 0 0 0 0	0 1 1 0 0	ACCUMULATOR Left Shift number 3
			Test shows 0
	0 0 0 0 0	1 1 0 0 0	ACCUMULATOR Left Shift number 4
			Test shows 0
+12	0 0 0 0 0	1 1 0 0 0	Correct answer

CHAPTER III

ACCUMULATOR AND SHIFT REGISTERS

The word "accumulator" usually brings to mind a device which stores a number, and, upon reception of another number, adds the numbers and stores the sum. It may be said that "counting" is involved, or more specifically pertaining to this system, binary counting. Since binary counting involves only two digits, 0 and 1, a device such as a FLIP-FLOP, having two stable states, might well be used for the purpose. Associated components necessary to perform the counting function could be devices such as LOGIC CIRCUITS (AND, OR, NAND, NOR, etc.), DELAY devices, and INVERTERS. As in any number system, when addition of two digits results in a sum equal to or greater than the base of the number system, a "carry" will appear. The binary carry occurs when the counter of any order passes from the state representing 1 to the state representing 0, and this carry is added to the counter of the next higher order. One way of handling carries is to note the orders which have generated a carry and send these carries to the next higher order by addition. This addition may produce more carries; if so, the process is repeated. For example:

```
 01111
 00011
 01100  First sum
  11    Carries
 01010  Second sum
  1     Carry
 00010  Third sum
 1      Carry
 10010  Final sum
```

This system of handling carries is obviously slow, and its use would largely nullify the speed advantage which parallel operation has over serial operation. Another method, which is faster and in most cases uses fewer components, is the automatic or "ripple through" carry, whereby any carry generated automatically is sent to the next higher order. Many different forms of ACCUMULATORS may be designed from a variety of components. (3). Even if a single set of components is considered, a variety of functional arrangements is possible, differences appearing in the handling of carries.

One form of ACCUMULATOR is shown in Figure 2. To add, a pulse is applied to the add pulse line. For those orders which hold a 1 in the addend register, the pulse is sent through to the corresponding counter in the ACCUMULATOR. If the ACCUMULATOR changes from a 1 to a 0, a carry is generated, to be sent to the next higher order. Subsequent to the add pulse, a carry pulse is applied to AND circuit 2, and for those orders having a carry, this pulse passes through a delay device to the next higher order. If several consecutive counters in the ACCUMULATOR

indicate 1 and a carry is generated in the lowest order of the series, it travels through AND 3 to all appropriate counters.

A variation of this type which features carry storage is shown in Figure 3. This unit is often found in computers of a design such that signals from the addend register cannot be obtained after entry of the addend has been made.

Figure 4 illustrates a form of ACCUMULATOR which uses no delays. The carry gate is pulsed as in previous examples after addition has been performed. If a carry is contained in the storage device, it is transmitted through AND 2 to the next higher stage. This method is relatively slow, since the carry gate signal must be held operative until the carries have reached all orders.

Figure 5 shows still another variation, featuring slow but automatic carry propagation, requiring only a single add pulse for operation.

The type of ACCUMULATOR selected for use in the problem at hand is shown in Figure 6. It has several desirable features which make it an obvious choice. First, the unit has no delay devices. The main objection to delays is the difficulties presented in proper termination. Second, it is possible to generate the carry signals even before the entry of the addend into the ACCUMULATOR. This not only means an increase in the speed of operation, but gives a means for early determination of an overflow.

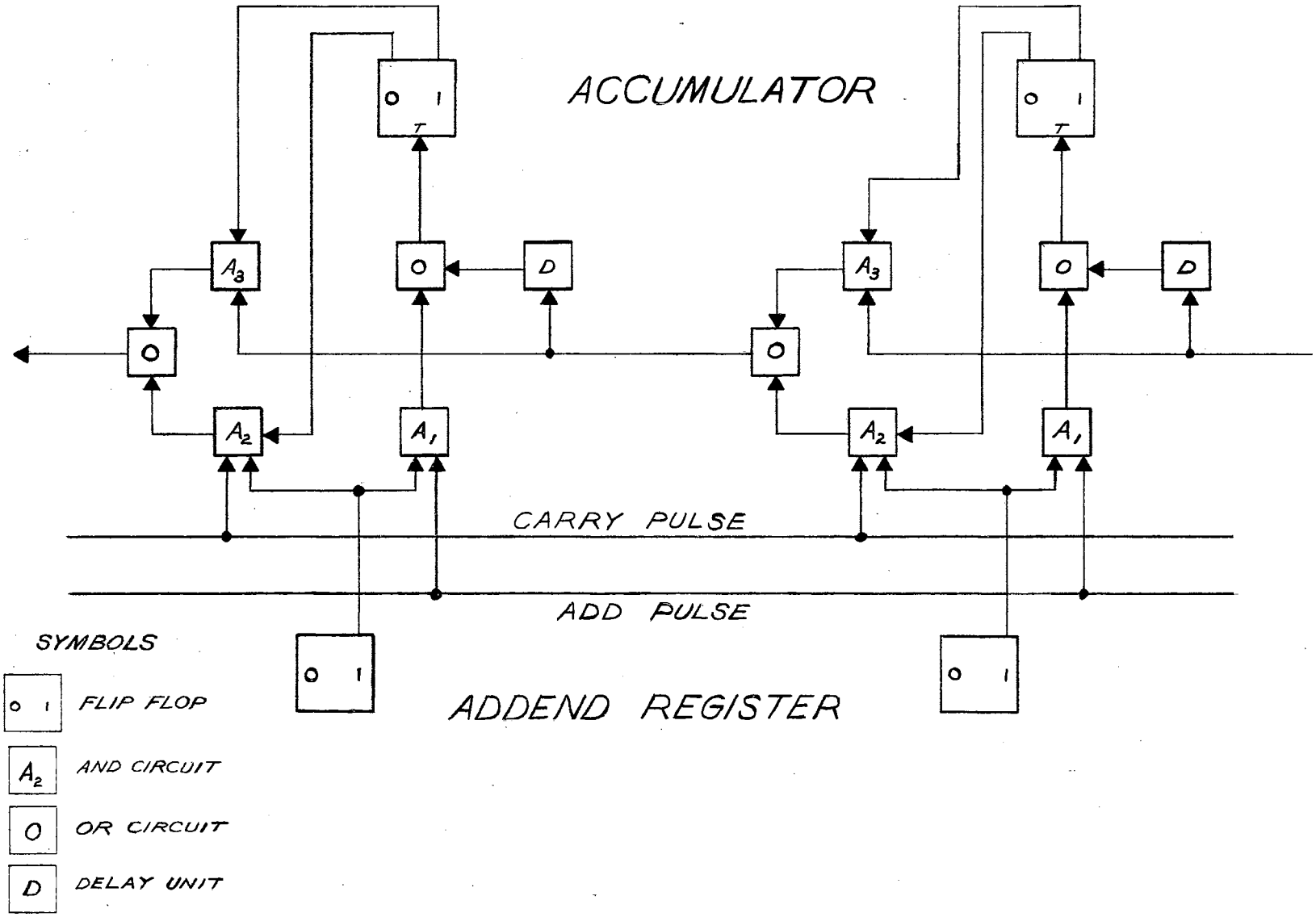
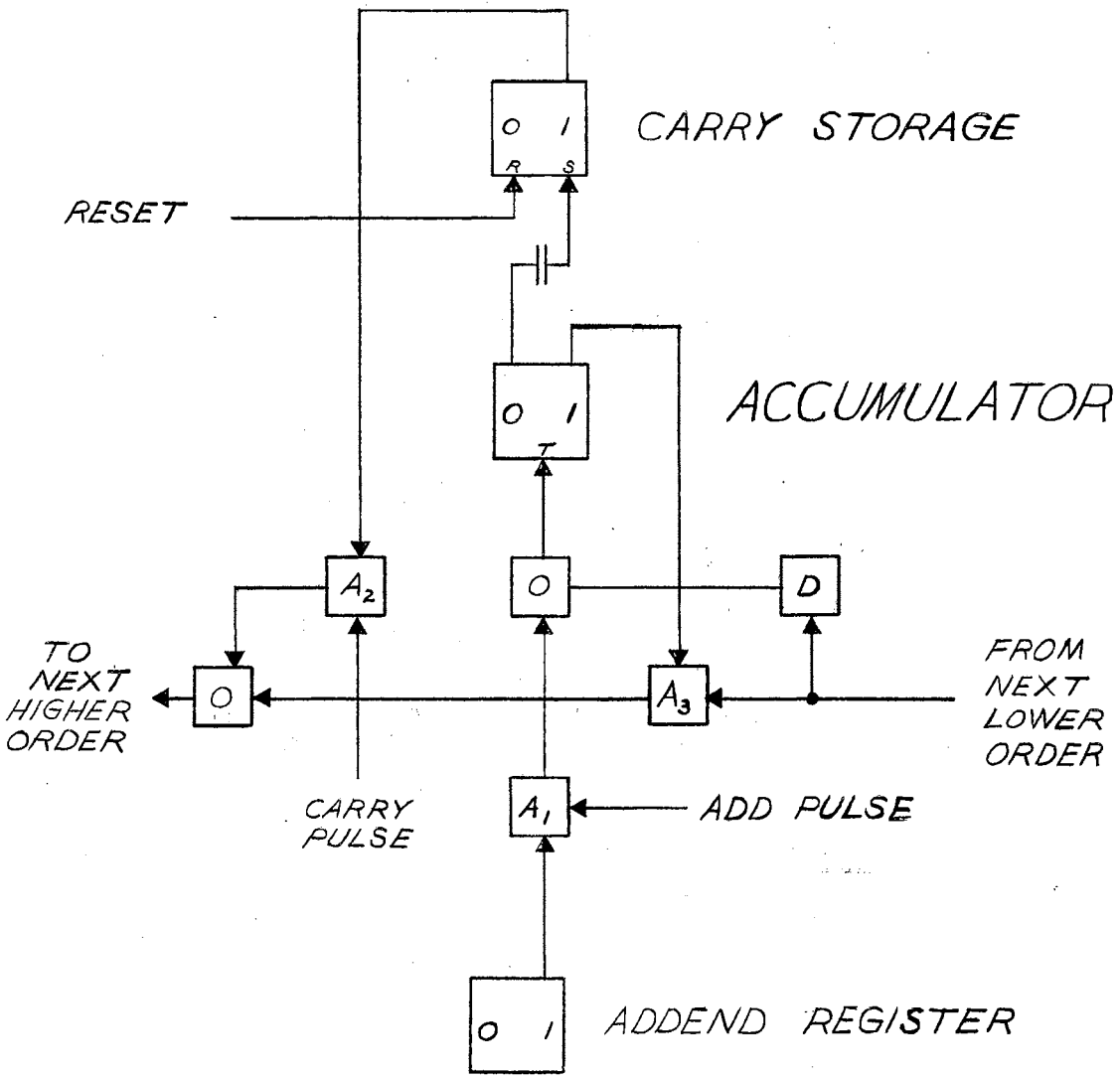


Figure 2. ACCUMULATOR



SYMBOLS

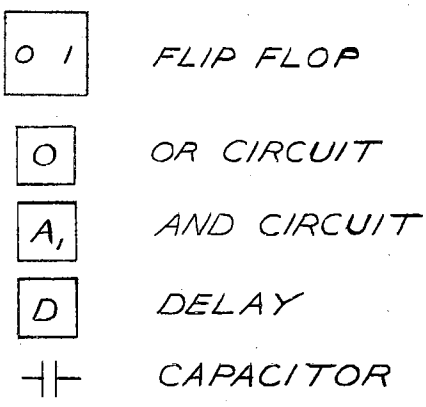


Figure 3. ACCUMULATOR With Storage

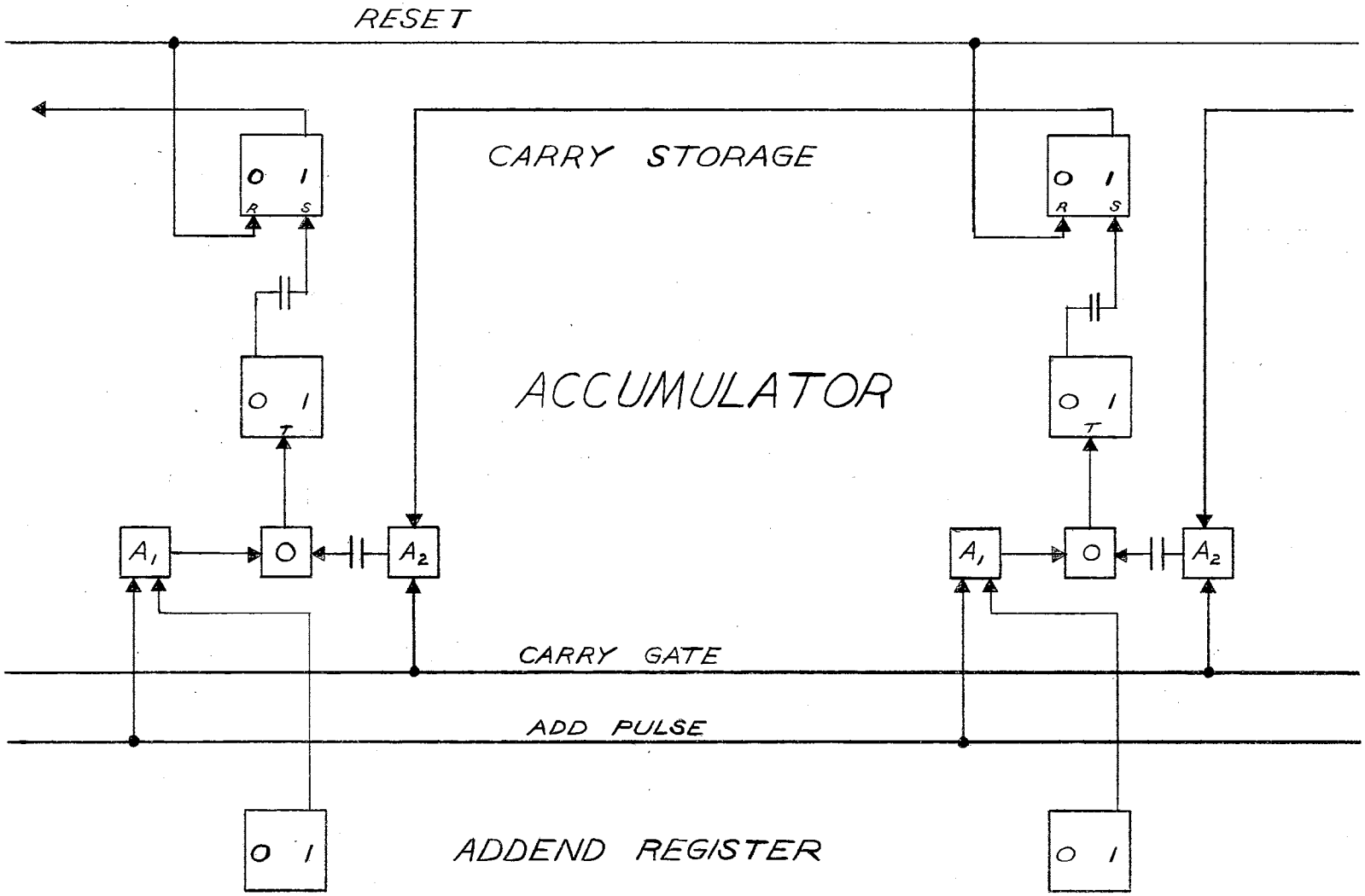


Figure 4. ACCUMULATOR With No Delay Units

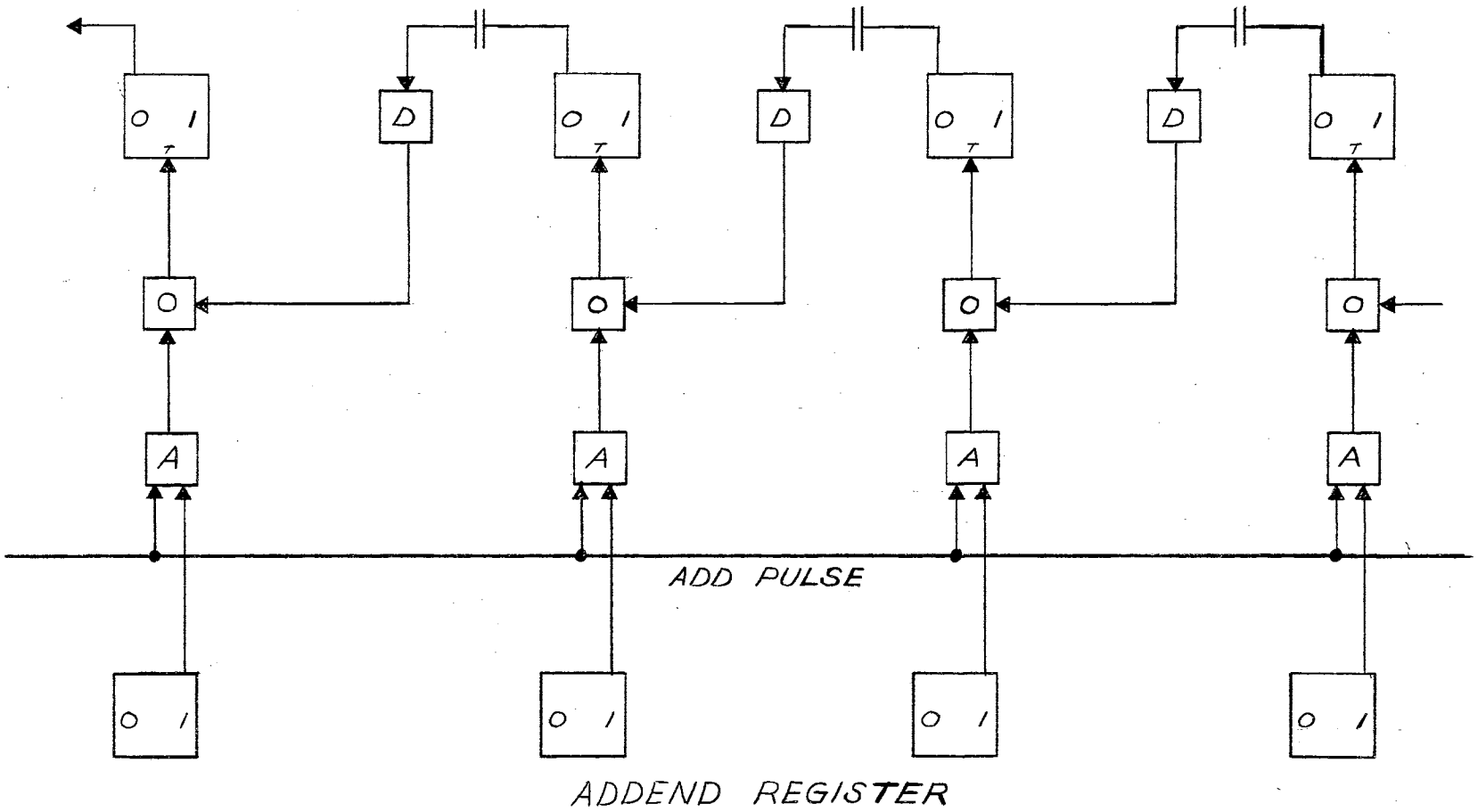


Figure 5. ACCUMULATOR With Automatic Carry

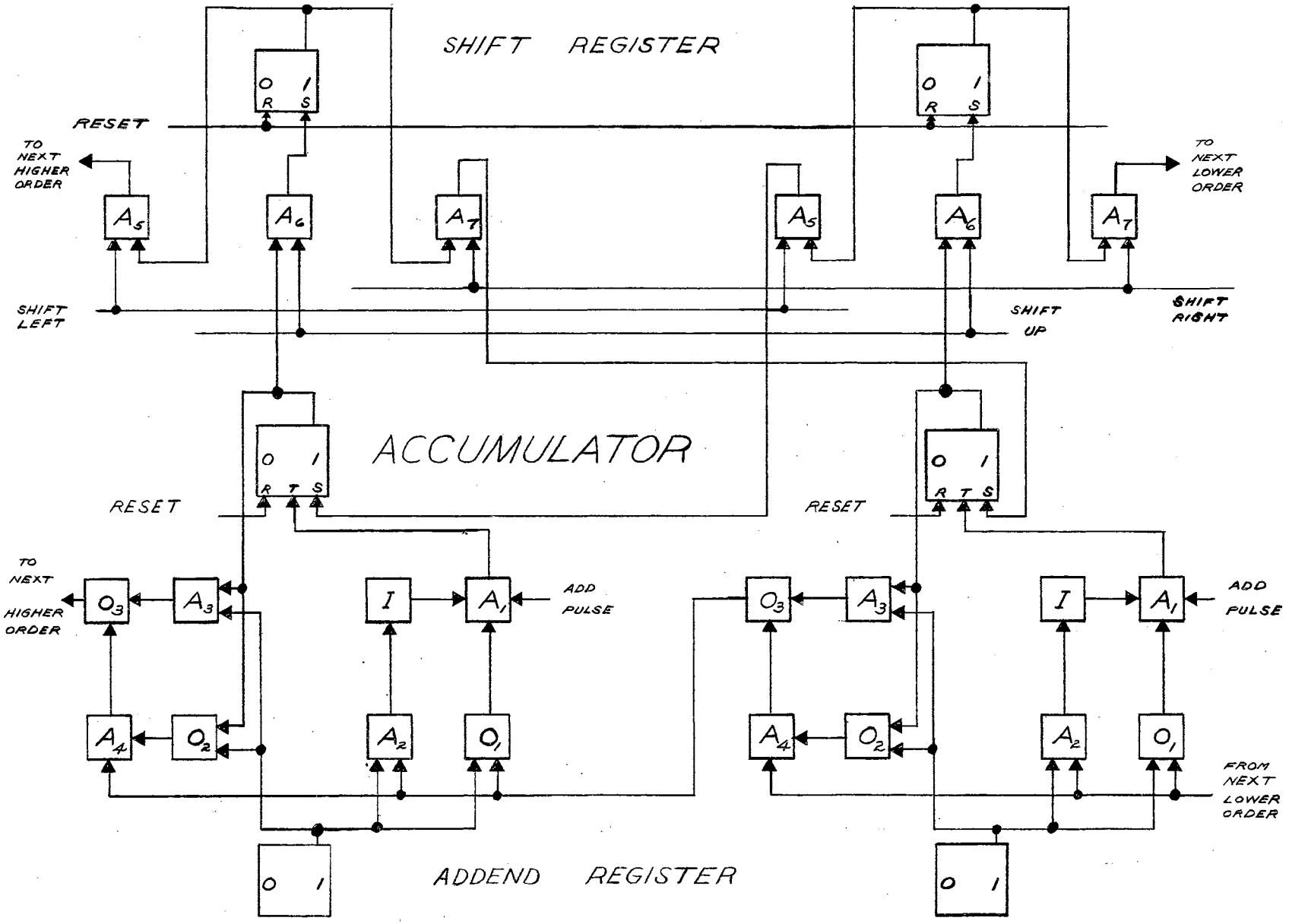


Figure 6. Selected ACCUMULATOR and Shift Register

Since one of the design criteria was that of overflow or end-around carry indication by 4 time, speed is an important consideration. Third, the unit uses only a single add pulse for operation. This reduces input requirements. Fourth, the unit has no need for carry storage, resulting in a design with fewer components. Fifth, the ACCUMULATOR has only one FLIP-FLOP for each counting position, increasing reliability. Sixth, parts were immediately available without expenditure. The basic register is composed of four AND circuits, three OR circuits, one INVERTER, and the FLIP-FLOP. Among the available components were many FLIP-FLOP/INVERTER plug-in units, which proved very satisfactory in both applications. The AND and OR circuits were formed using donated diodes, in conjunction with some salvaged resistors and condensers.

In the previously described circuits, it was necessary for a counter to change its state twice in an addition where it happened to receive a pulse both from the addend register and from the next lower order. With this arrangement, such an occurrence is unnecessary. If a 1 is indicated in the addend and from the next lower order, the inverter will be DOWN. This prevents the incoming add pulse from affecting the counter. At the same time, the output line to the next higher order will be UP, giving a carry indication. This process begins with the entry of the addend into the DISTRIBUTOR, and continues through the ACCUMULATOR as rapidly as the logic circuits allow.

Also shown in Figure 6 is the shift register. Although not necessary for ordinary addition, it is needed for multiplication and other processes, and, therefore, may be considered as an auxiliary to the ACCUMULATOR. A shift register may have several forms, depending on the design of the basic counting unit. This one is composed of a single FLIP-FLOP and three diode AND circuits, and operates from four sequenced pulses. Initially, the register contains a 0. Pulse 1 sets the FLIP-FLOP to the same state as the counter. Pulse 2 clears the ACCUMULATOR. Pulse 3 shifts the pulse either to the right or to the left, depending on direction of shift desired. Pulse 4 resets the shift register to 0. The actuating pulses are readily available from the timing marks on the magnetic drum.

CHAPTER IV

COMPONENT ANALYSIS OF THE ARITHMETIC UNIT

The FLIP-FLOP

The FLIP-FLOP circuit is shown in Figure 7. This circuit comes as a compact plug-in unit, called a "FLIP-FLOP/INVERTER", manufactured by the Electronic Engineering Company of California. The design is straightforward and of the Eccles-Jordan type, component values being selected in consideration of circuit parameters and operational requirements.

When voltages are initially applied to the FLIP-FLOP, one tube will be found to be non-conducting, or UP, and the other to be conducting, or DOWN. Several methods may be used to cause the unit to change states, or "flip." The method selected was the application of a positive pulse to the grid of the non-conducting tube.

Assume the left tube (A) is initially conducting and the right tube (B) non-conducting. The applied pulse raises the grid potential of B, causing the tube to begin to conduct. The resultant plate current flowing through the 12K resistor decreases the plate voltage. This voltage decrease is reflected through the 75K coupling

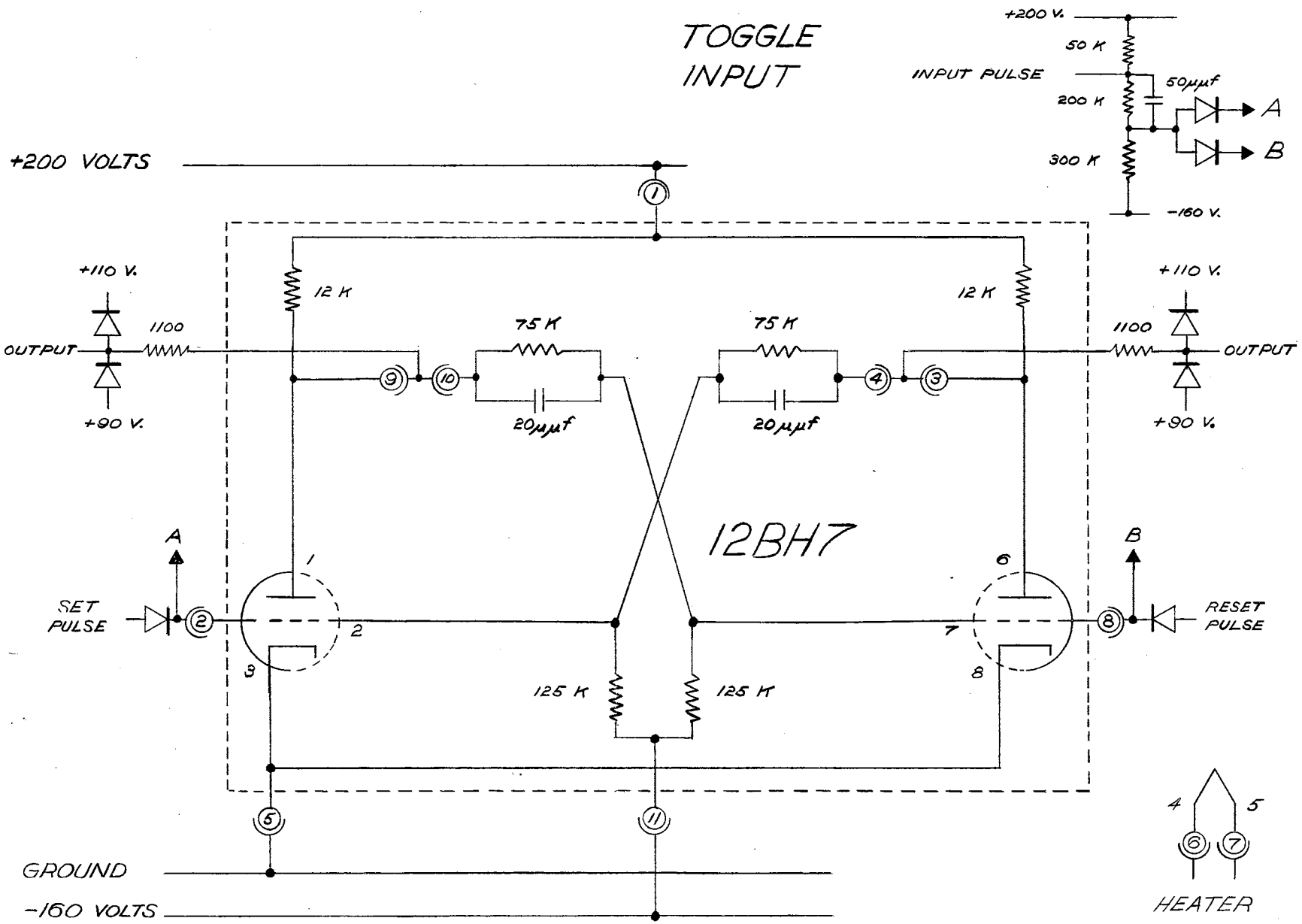


Figure 7. FLIP-FLOP

resistor to the grid of tube A, causing A to conduct less, therefore, decreasing plate current and increasing plate voltage. The latter raises the grid potential of B through the other 75K coupling resistor. This regenerative action continues until stability is reached with tube A cut off and B conducting. The 20 picofarad capacitors are used to overcome the effect of tube capacitance, increasing reliability of operation and speeding up response.

A toggle input may be used, whereby the triggering pulse is applied to both grids simultaneously. The effect of the pulse on the conducting tube is small compared to that on the non-conducting tube, and action occurs as described.

A 4 volt pulse of 1 microsecond width was found to result in reliable operation. Minimum switching time, or "resolution time," was found to be slightly less than 2.0 microseconds. Rise time of the plate voltage was observed to be approximately 0.1 microsecond.

The diode clamp circuit shown connected to the plates provides an output of 90 volts or 110 volts, depending on whether the tube in question is conducting or non-conducting, respectively. If the plate is DOWN, (about 65-70 volts), current flows from the 90 volt supply and through the 1.1K resistor, maintaining the output at 90 volts. If the tube goes UP, (about 125-135 volts), current flows through the 1.1K resistor into the 110 volt supply, maintaining output at 110 volts.

Plate I, 1, shows an oscilloscope presentation of the triggering and output waveforms.

The INVERTER

The INVERTER circuit is shown in Figure 8. Note that the only difference between it and the FLIP-FLOP is that of the external pin connections to the module. Each unit inverts, or reverses an input signal. In terms of logic, a "1" input will result in a "0" output, and vice versa.

The input signal, either 90 volts or 110 volts is applied to the grid through a voltage divider. The grid voltage with a 90 volt input is such (-12 volts) that a plate voltage of 130-135 volts results. A 110 volt input will give a plate voltage of 65-70 volts. The output is then clamped with diodes to provide 90/110 volt output. Obviously, if the input signal is not exactly 90/110 volts, the unclamped output will vary. However, tests have shown that an input variation of ±1 volt, an amount greater than is likely to be found, will produce proper output after clamping. Since the output is a function of the input signal, the unclamped waveshapes are almost identical, degradation not being serious.

Plate I, 2, shows a comparison of the input and output waveforms.

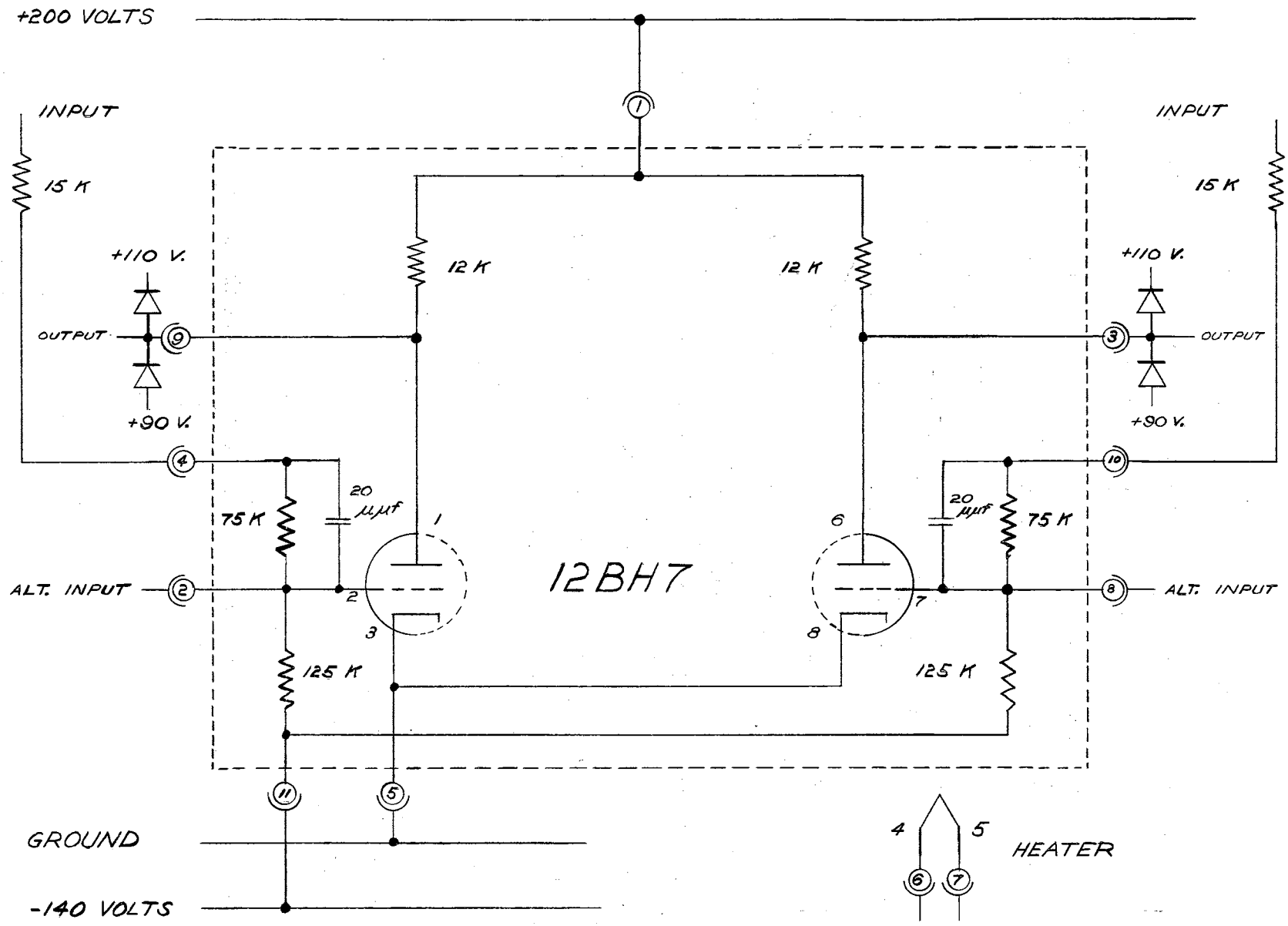


Figure 8. INVERTER

Logic Circuits

Two different diode logic circuits are used in the ARITHMETIC UNIT, the AND circuit and the OR circuit. Recalling that in positive logic systems a "1" or UP state is indicative that a quantity is present, and a "0" or DOWN state indicates its absence, the analysis of these circuits is easily accomplished.

In the diode AND circuit (Figure 9), all inputs must be present before an output will result. The ACCUMULATOR uses only two input and three input AND circuits; however, many inputs are sometimes used. With all inputs DOWN, current flows from the 200 volt supply through the dropping resistor, and then through the diodes. The voltage drop across the resistor will be 110 volts, giving 90 volts on the output line. The drop cannot be more, since the diodes would then cease to conduct. If one input should go UP, 110 volts would appear on the cathode of that input diode. The other diode(s) can still conduct down to an anode voltage of 90 volts, however, so the output remains at 90 volts. The only significant change is in the distribution of diode current. If all inputs go UP, the minimum voltage on the anodes is 110 volts; hence, the output goes UP. Thus, for the output to be UP, all inputs must be UP; otherwise, a path for current flow exists which will give a 110 volt drop across the resistor. It is easily seen that for proper functioning, the output may not be loaded

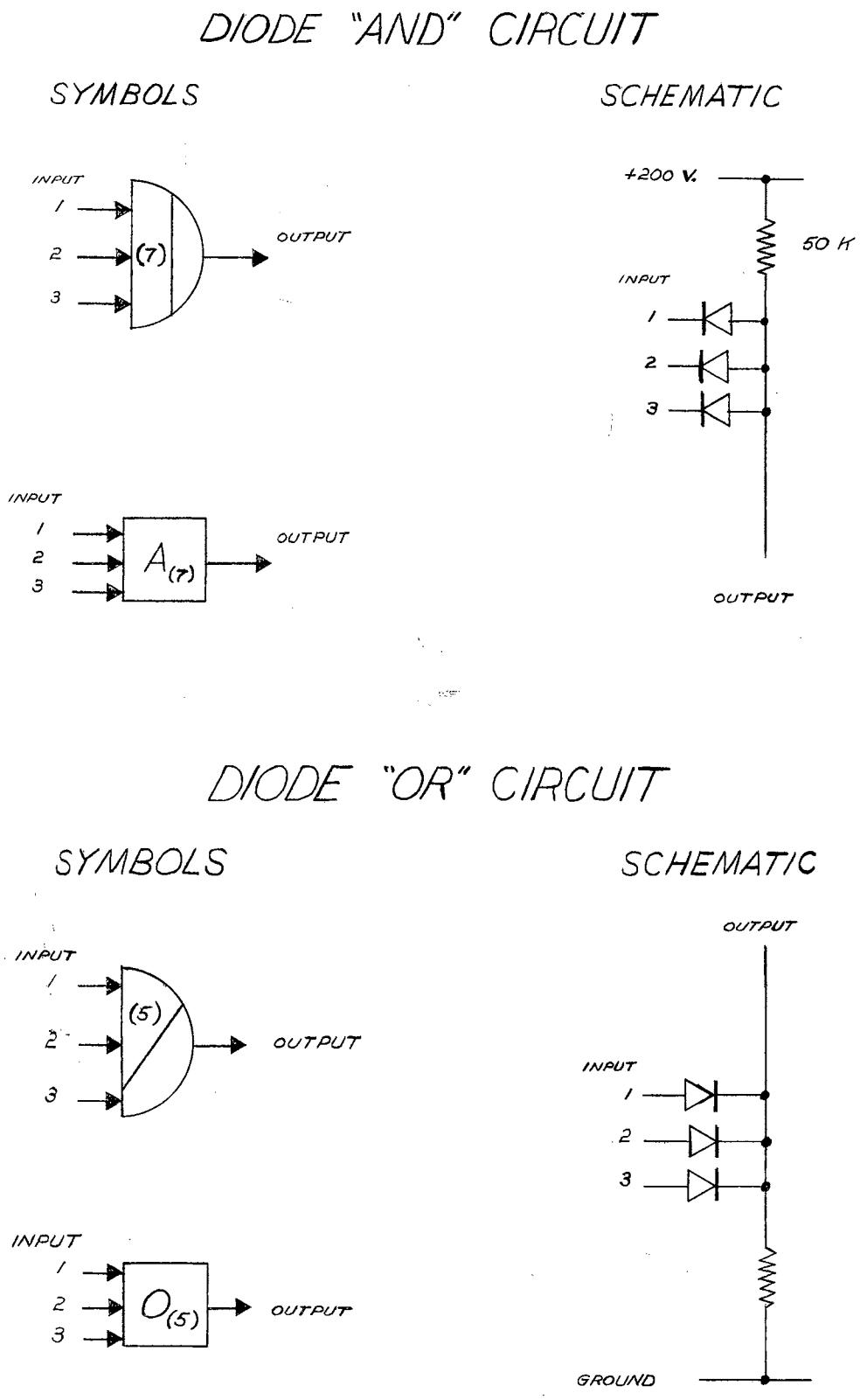


Figure 9. Diode Logic Circuits

appreciably. The maximum current which may be drawn by the following stage is that amount which will cause 110 volts drop across the resistor. A greater drop than this makes it impossible for the output to reach 110 volts. Since a high value of dropping resistance is desirable to prevent large diode current flow under varying load impedance, subsequent circuitry must be carefully evaluated to insure correct operation.

The diode OR circuit (Figure 9) functions in a somewhat similar manner, except that instead of all inputs being necessary for an output, only one input is required. If all inputs are DOWN, the voltage across the dropping resistor is 90 volts, as is the output voltage. If any input goes UP, the remaining input diodes are reverse biased. A 110 volt drop will occur across the resistor, causing increased current flow, and the output will rise to 110 volts. Additional inputs going UP will only affect individual diode current. Heavy circuit loading should be avoided to prevent large diode current flow.

Some waveshape distortion and time lag result in the AND and OR circuits. With proper choice of diodes, these factors can be held to a minimum. The diodes used in this ARITHMETIC UNIT were Hughes 1N116 diodes, placed in plug-in units containing 12 diodes each. The oscilloscope pictures of output waveforms with square wave input (Plate I, 3) show negligible distortion and small time lag.

CHAPTER V

OPERATION OF THE ARITHMETIC UNIT

A circuit diagram of a three section portion of the ARITHMETIC UNIT is shown in Figure 10. This circuit is an exact combination of three single bit position units of the type shown in Figure 6, with a double INVERTER added in the "to next higher order" line to isolate the logic stages. Figure 11 shows the relative location of these INVERTERS in block diagram form. The complete unit is composed of twelve of these sections, five being used as the LOWER REGISTER, five as the UPPER REGISTER, one as the TEST position, and one as the SIGN. All of these sections are identical in form and operation. In the SIGN bit section, the shift register is present, but not used. Additional sections may therefore easily be added to extend the capacity of the register to any desired number of bits.

It has been previously noted that in an arithmetic operation, the DISTRIBUTOR first enters a number into the UPPER or LOWER. A new number is then placed in the DISTRIBUTOR, and the numbers are added together. An example of the addition of binary one (001) to binary one (001) using a three bit register will now be considered. Prior

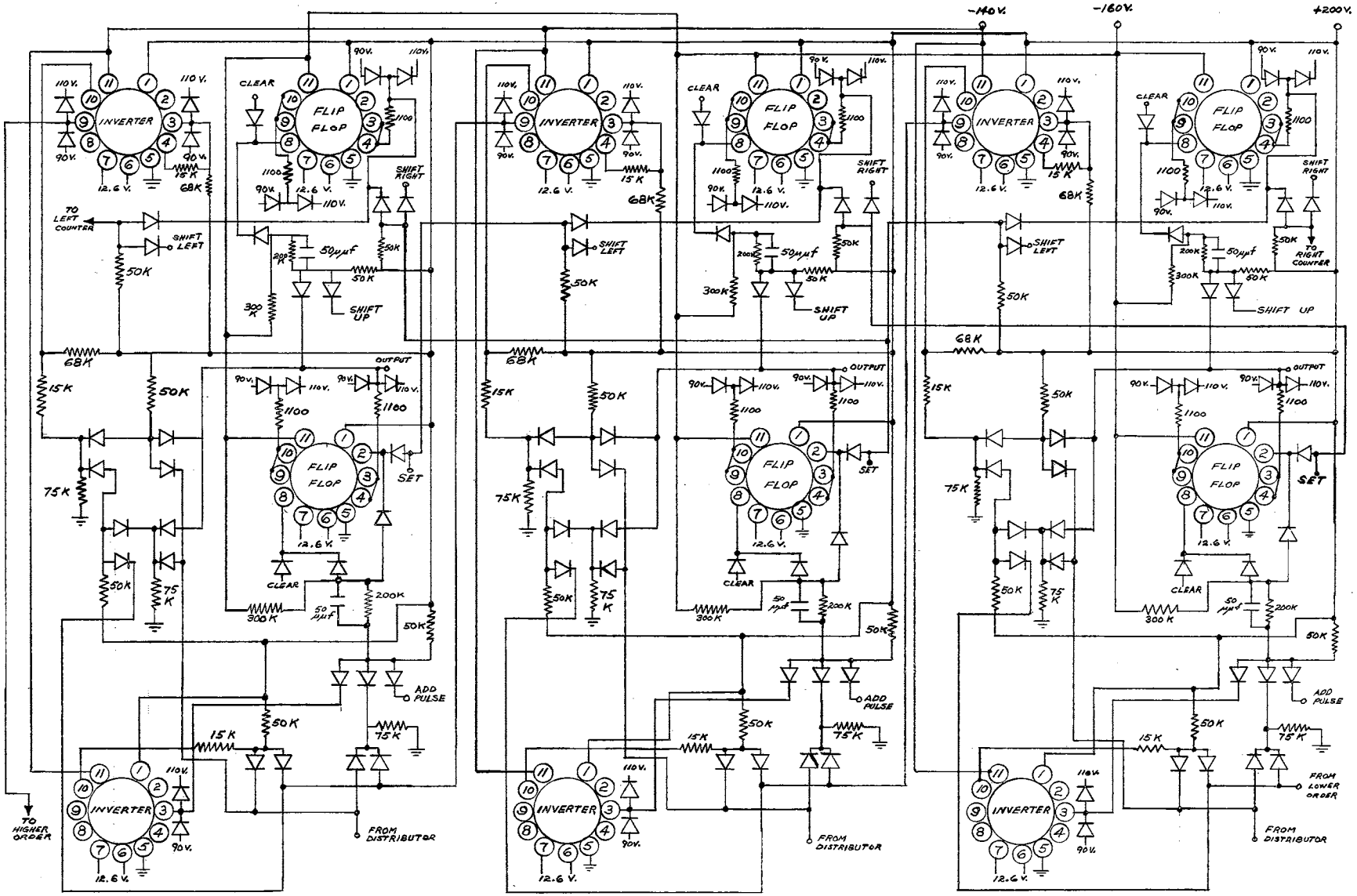


Figure 10. Sectional Schematic Diagram of the ARITHMETIC UNIT

to any operations, the ACCUMULATOR and DISTRIBUTOR are cleared to zero. The augend, 001, is then placed in the DISTRIBUTOR. Since the augend is desired to be in the ACCUMULATOR, the ADD line is pulsed. Consideration of the rightmost section (lowest order) reveals that initially, (cf. Figure 6, page 31), since there is no input from a lower order, OR1 will be UP due to the addend (001), AND2 will be DOWN, and the INVERTER will be UP. OR2 will be UP, AND3 is DOWN, AND4 is DOWN, and OR3 DOWN. When the ADD pulse occurs, AND1 will pass the pulse, and the FLIP-FLOP changes from 0 to 1. The second and third order positions will naturally contain all zeros throughout. The contents of the DISTRIBUTOR, 001, are now in the ACCUMULATOR. Since 001 is to be added to 001, the DISTRIBUTOR will remain unchanged for the second step. The 1 in the lowest order position of the DISTRIBUTOR causes OR1 to be UP, the INVERTER UP, OR2 UP, AND3 UP, AND4 DOWN and OR3 UP. When the ADD pulse is applied, the FLIP-FLOP will go DOWN, AND3 DOWN, and OR3 DOWN. In the second order position, OR1 is UP due to the input from OR3 in the lower order. In this second order, AND2 is DOWN and the INVERTER UP. The ADD pulse changes the FLIP-FLOP to 1, OR2 goes UP, AND3 is DOWN, AND4 goes DOWN and OR3 is DOWN. The ACCUMULATOR now contains 010 in the three orders. It is seen that the carry may be determined prior to addition, since the ADD pulse merely changes the FLIP-FLOP from 0 to 1 or 1 to 0, while a carry is determined by the "input

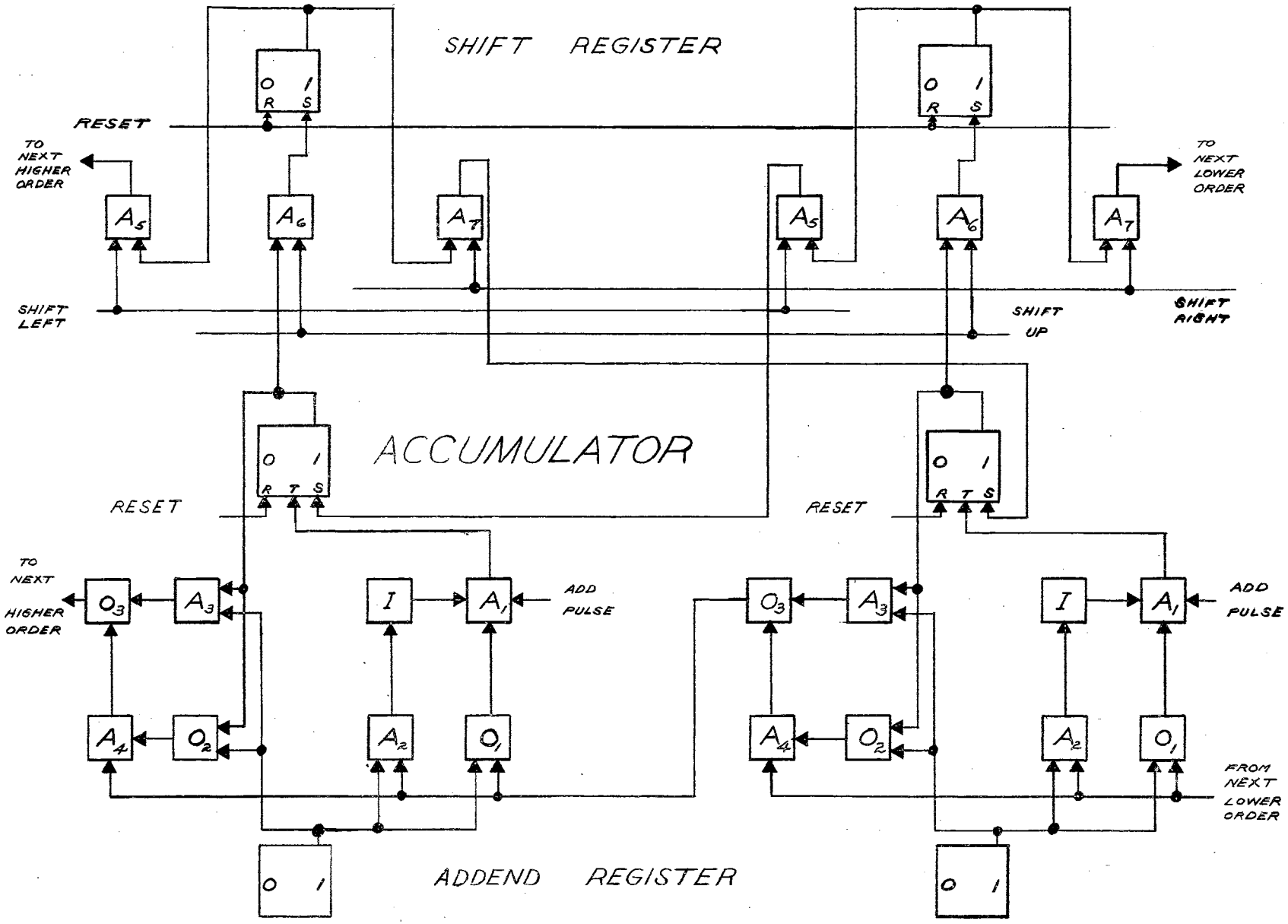


Figure 6. Selected ACCUMULATOR and Shift Register

from lower order" line.

A shift operation is now illustrated in which the middle digit (1) in 010 is shifted one position to the right, changing the number to 001. The shift register is initially set to zero. The SHIFT UP line is pulsed, and AND6 passes the pulse, changing the auxiliary FLIP-FLOP to 1 in the middle order. In the highest and lowest orders, AND6 will not pass the pulse, and the FLIP-FLOP remains at zero. The ACCUMULATOR is now cleared. The SHIFT RIGHT pulse is applied, and in the middle order, AND7 passes this pulse, setting the counter of the lowest order to 1. Since the auxiliary FLIP-FLOP in the highest order was 0, no pulse will pass AND7 to set either the second order or the highest order to 1. The ACCUMULATOR now contains 001. A similar operation using the SHIFT LEFT line would result in the ACCUMULATOR containing 100 after the operations were completed.

Operational tests were made to determine the performance of the unit. The first test was an examination of individual counter operation. A 1 was placed in the DISTRIBUTOR for an addend bit, and the input from the next lower order set at 0. As previously illustrated, the application of an ADD pulse will change the state of the ACCUMULATOR FLIP-FLOP. If the addend is left at 1 and the ADD pulse repeatedly applied, the FLIP-FLOP will continually change states at a rate determined by the frequency of the ADD pulses. Since the pulses available from the

magnetic drum occur one every 6.8 microseconds, the test was made with pulses spaced one each 5 microseconds (200 kc.), and the output of the FLIP-FLOP observed on the oscilloscope. Plate I, 4, shows the resultant waveform has a rise time of approximately 0.1 microseconds.

The second test was that of the carry logic. The presence of a carry causes OR3 to be UP. If the ACCUMULATOR and DISTRIBUTOR bits of all orders are 1, and a carry is introduced into the lowest order, this carry will be passed on through the logic to the highest order position. Therefore, a wave was applied to the lowest order carry input, and the output of several higher order logic circuits observed (Plate I, 5). The waveforms were fairly undistorted, but a straight time delay of approximately 0.5 microseconds was noted.

The third test involved the shifting circuit. A 1 was placed in one ACCUMULATOR position and the shift register set to 0. This 1 was then circulated through the shift register position and re-entered into the ACCUMULATOR position by continually shifting right. Plate I, 6, shows the bit as it appears in a counter position, referenced to the clock pulses.

A block diagram of the entire ARITHMETIC UNIT is shown in Figure 11. In normal operation, pulses may be required on the following lines: ADD, COMPLEMENT UPPER, COMPLEMENT LOWER, CLEAR UPPER, CLEAR LOWER, CLEAR SHIFT REGISTER, SHIFT UP, SHIFT RIGHT, SHIFT LEFT. External

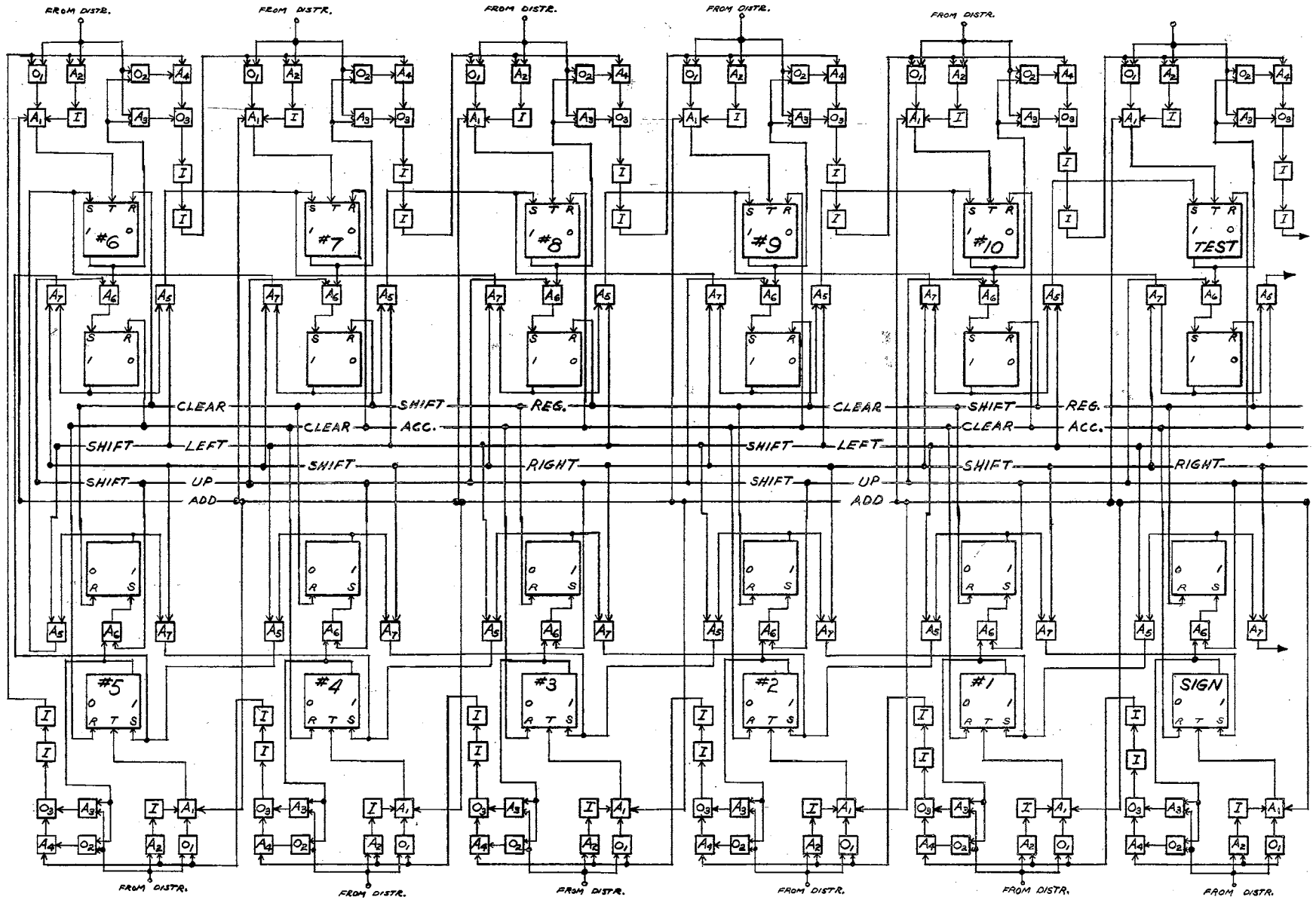
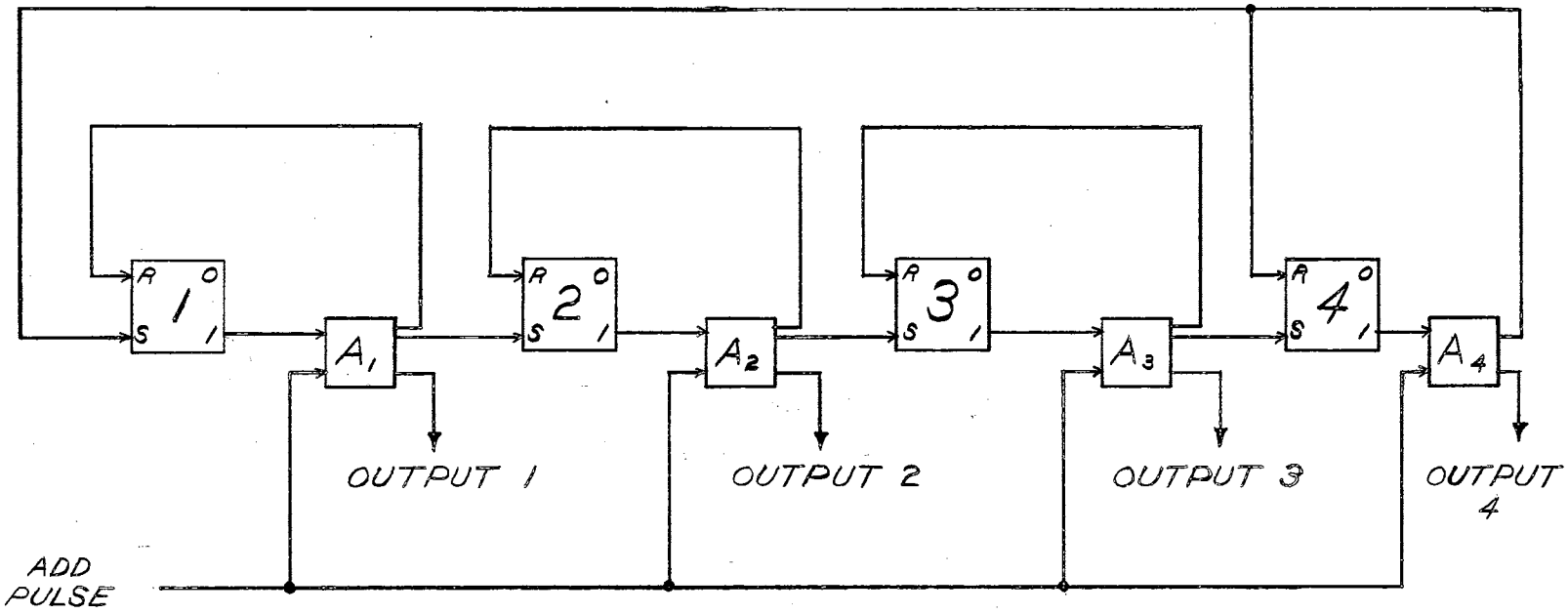


Figure 11. The ARITHMETIC UNIT

logic is necessary for proper pulse application. Also, it is needed to place the end-around carry where desired.

The applied pulses must be 0.7 to 1.5 microseconds in width, a minimum of 7.0 volts, and a maximum of 30.0 volts for reliable operation at high speed. The shift register was designed with the use of the 6.8 microsecond clock pulses from the drum in mind, and was, therefore, tested at this speed. A small pulse unit producing pulses on four individual output lines, sequenced in time 6.8 microseconds apart, and occurring in the order 1-2-3-4 was designed and satisfactorily used in the test (Figure 12). This unit is a simple Ring Counter, consisting of four FLIP-FLOPS. The output pulse appears on line 1, 2, 3, or 4, depending on which AND circuit allows it to pass. Initially, FLIP-FLOP 1 is set UP and 2, 3, and 4 set DOWN by a switch which grounds the appropriate grids. The first input pulse appears on output line 1 through AND1. It simultaneously is fed to the grids of FLIP-FLOPS 1 and 2, bringing the former DOWN and the latter UP. This causes the second input pulse to appear on output line 2 through AND2, whereby it brings FLIP-FLOP 2 DOWN and FLIP-FLOP 3 UP. The process continues in this fashion, FF3 going DOWN and FF4 UP on the next pulse. The fourth pulse returns the counter to its initial state, and the sequence of operation is repeated.

The ARITHMETIC UNIT requires 12.6 volts at 14.4 amperes, 200 VDC at 960 ma., 90 VDC at 360 ma., 110 VDC at -265 ma., -140 VDC at 36 ma., and -160 VDC at 95 ma.



INITIAL CONDITIONS: FF1 UP, FF2,3,4 DOWN

Figure 12. Ring Counter

CHAPTER VI

SUMMARY OF RESULTS AND UNIT INTEGRATION

The testing of the ARITHMETIC UNIT confirmed its compatibility with other components of the MAGNETIC DRUM DIGITAL SYSTEM. The FLIP-FLOPS changed state in much less than 1 microsecond (0.1 microseconds), well within the time between exciting pulses. The output carry pulse in a 38 bit register appears 20.0 microseconds after the DISTRIBUTOR receives the addend. Since one word time is 34.0 microseconds, the carry determination can be made 41.2 microseconds before 4 time in the ADD cycle, well within the specified limit. The shift register performed well with a 27 microsecond shift cycle.

For actual arithmetic operations to be performed by the ARITHMETIC UNIT, separate circuitry must provide the following:

1. ADD pulses of approximately 1.0 microsecond duration and magnitude greater than 7.0 volts but less than 30.0 volts.
2. Shift pulses on four separate lines for the shift operation. These pulses must have the above dimensions.

3. Logic for the complementation of the UPPER and/or LOWER REGISTERS.
4. Logic for the desired use of the end-around carry.
5. Logic for the TEST in multiplication operations.
6. Logic for counting the number of shifts performed (multiplication).
7. Logic for clearing the UPPER and/or LOWER REGISTERS.

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(4) Phister, Montgomery, Jr. Logical Design of Digital Computers. New York: John Wiley and Sons, Inc., 1959.

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(6) Ryder, John D. Engineering Electronics. New York: McGraw-Hill Book Company, Inc., 1957.

Plate I

1. FLIP-FLOP — Top - Plate Waveform 20 v/cm 2 μsec/cm
   Bottom - Triggering Pulse 5 v/cm
   2 μsec/cm

2. INVERTER — Top - Input Pulse 5 v/cm 2 μsec/cm
   Bottom - Plate Waveform 20 v/cm
   2 μsec/cm

3. DIODE "AND" and "OR" Circuits

   Left Half: AND Circuit — Top - Input
   Bottom - Output

   Right Half: OR Circuit — Top - Input
   Bottom - Output

   20 v/cm 10 μsec/cm

4. Repeated Addition of "1" into an ACCUMULATOR Counter Position

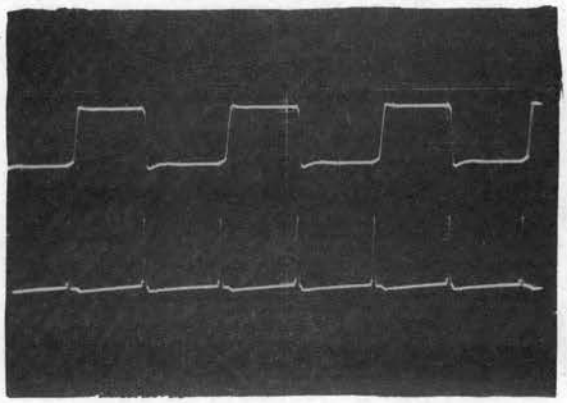
   Top - Output Waveform — 10 v/cm 2 μsec/cm
   Bottom - ADD Pulse — 5 v/cm 2 μsec/cm

5. Carry Logic — Top - Input Waveform
   Bottom - Output Waveform after 3 Logic Stages
   20 v/cm 2 μsec/cm

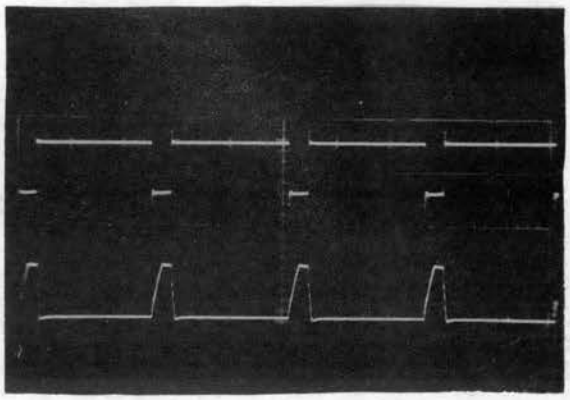
6. Shift Register - Circulation of a "1" Around a Counter/Shift Register Loop

   Top - Shift Register Output Plate
   Bottom - Sequenced Clock Pulses
   20 v/cm 5 μsec/cm

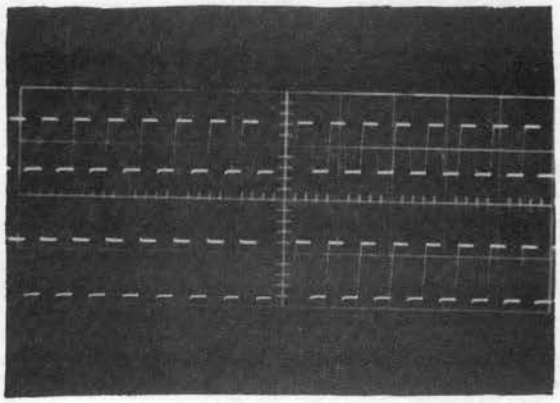
Plate I. Oscilloscope Waveforms



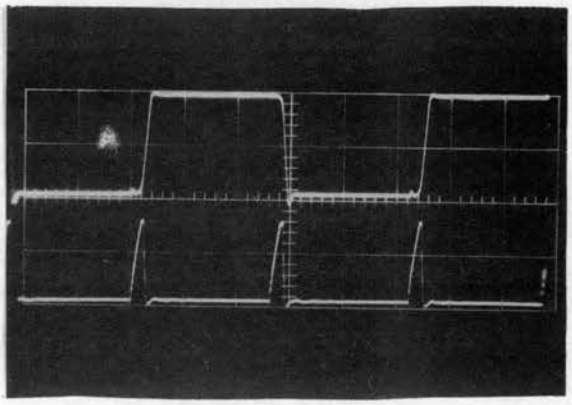
1. FLIP-FLOP
Input and
Output



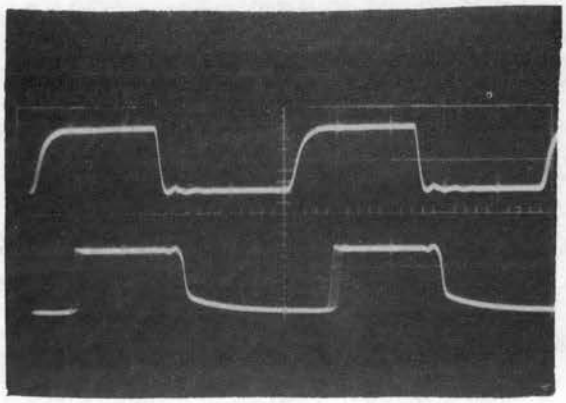
2. INVERTER
Input and
Output



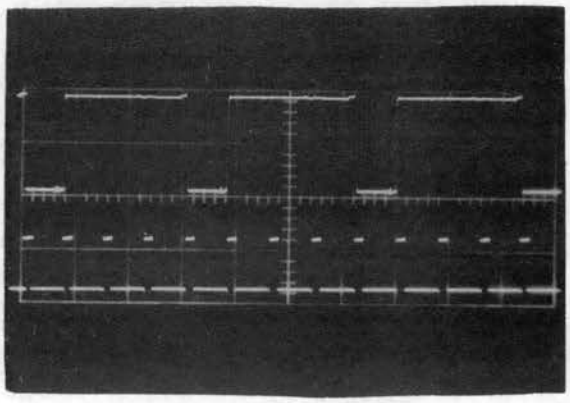
3. LOGIC CIRCUIT



4. Adding 1 Repeatedly Into
an ACC. Bit Position

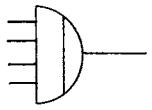


5. LOGIC OUTPUT
Several
Successive
Stages

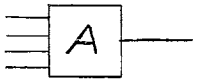


6. SHIFT REGISTER
Circulating a
1 Through
Several Stages

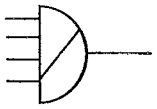
APPENDIX A
GRAPHICAL SYMBOLS



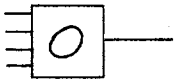
AND Circuit



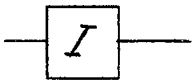
AND Circuit



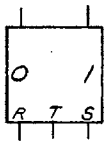
OR Circuit



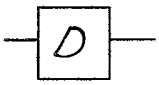
OR Circuit



INVERTER



FLIP-FLOP with Set, Reset, Toggle inputs



DELAY Device

DIODE

Plug-in Unit Terminal

CAPACITOR

VITA

Hugh Tallman Gunn

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Professional Organizations: Eta Kappa Nu, Institute of Radio Engineers.