A BIASED MAGNETIC CORE READ-ONLY MEMORY

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1960

Submitted to the Faculty of the Graduate School
of the Oklahoma State University
in partial fulfillment of the requirements
for the degree of
MASTER OF SCIENCE
May 27, 1962

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PREFACE

Some applications of modern computer technology require that large blocks of information be stored for long periods of time or even permanently. The computer application of language translation is one example. While the nature of the stored information may never be changed, it is important that the read-out time be very short and, of course, the overall cost and reliability is always an important facet to the design of any device.

To fulfill the need for a memory device that will store permanent information, and have the above mentioned characteristics, the read-only memory has come into being. There are many ways to design a read-only memory and this thesis is the study of one type of read-only memory, a biased magnetic core memory.

The first part of the thesis discusses the technique of operating a d-c current biased core. Then an individual core is investigated to determine some of the necessary characteristics, and finally the cores are arranged in matrix form and tested for various operating conditions. The main approach to the study was made through experimental procedures, but analytical aspects were not neglected.

I would like to express sincere appreciation to Professor Paul A. McCollum for his helpful advice and instruction, and for supplying the magnetic cores used in the study.

A special recognition is due to my wife and my parents for their interest and encouragement, and many thanks to Connie Beth Bruton who did the typing.

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CHAPTER I

INTRODUCTION

It would be difficult to over emphasize the importance of a memory unit to the operation of a digital computer. A digital computer could be operated without a memory by the sole use of input-output equipment, but it would be very slow and inconvenient. For instance, the operations to be performed could be read one by one from an input device, together with the initial data, then intermediate results could be written onto an output device and then transferred back through the input equipment as needed. This is not all that would be involved in operating a computer without a memory, but it does show the severe limitations imposed on the speed, flexibility, and reliability of a digital computer.

A memory is capable of retaining information written into it until, at some future time, the information is read-out and used by the arithmetic and/or logic circuits of the computer. Some of the most recently developed memory devices reflecting rather ingenious techniques include the twistor, magnetic cards (with a total practical capacity of five and one-half million characters), the phenomenon of spin echo (1), and cryoelectric memories (2).

In reading out the information from a memory, the read-out process can be either of a destructive or nondestructive nature.

Destructive read-out deletes the information from the memory. Non-destructive read-out either removes the information and immediately writes it back in, or the information is merely sensed and not removed at all.

A read-only memory might be classified as a memory with a fast read-out time and a comparatively infrequent write-in occurance. The extreme case would be to have the information permanently fixed into the memory and used for the read process only.

Interest in read-only memories has accelerated in the last few years due to the fact that they can fulfill certain applications in modern data processing at a saving in space and cost. Read-only memories can also have short access times plus extremely high reliability. The memory is normally used for storing any information that is used time after time and remains invariant, such as mathematical and vocabulary tables, payroll information, and language translation dictionaries.

A rather new and versatile application for a read-only memory is that of incorporating a replaceable memory into a general purpose computer, in which different applications of the computer would require certain read-only memory units designed for particular applications. Thus, an otherwise general purpose machine could be quickly converted to a specialized machine for specialized applications as Patrick (10) has mentioned. Replacement of the read-only memory unit could conceivably change the order code repertoire of the machine, as well as providing stored tables, etc. This would, in effect, customize a general purpose computer for any one particular application.

One type of read-only memory that should be seriously considered by virtue of the reliable operation associated with it is the core matrix memory.

A core matrix memory of the general purpose, write-in, read-out type, requires a write-in current pulse for the purpose of storing information in the cores. When adapted for read-only operation, the core matrix will have a d-c bias line appropriately threaded through the cores for establishing the stored information pattern. Thus, the direction the bias line takes through a given individual core establishes the nature of the information stored in that core. The stored information is permanent in as much as the bias line is always energized with a d-c current. Read-out is accomplished by the standard core reading technique of "disturbing" the core.

It can be seen then that the read-only core matrix memory will not need the write-in current drivers with the associated address selection logic as required by a general purpose core memory. Thus, a notable saving in cost and size is accomplished. Furthermore, it is conceivable that several bias windings could be threaded through the memory, each with its own information pattern, the desired pattern being selected by merely energizing the appropriate bias line. An illustration of a simple three by three matrix memory with two bias lines is shown in Figure 1.

A core matrix can also serve as a generator of control pulses for certain arithmetic control lines. For instance, in a shift register a certain combination of pulses may be required to shift the register two places right, whereas another combination is required

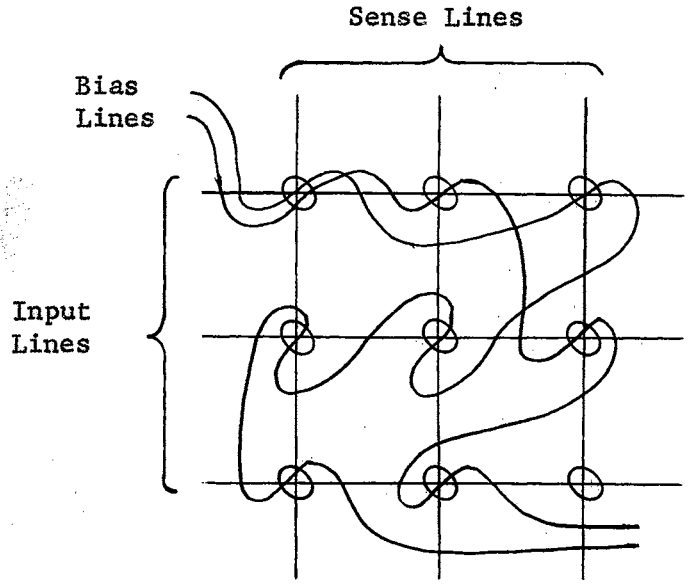


Figure 1. A Biased Magnetic Core Matrix Memory

to shift the register five places left. Thus, a different combination of pulses is required for each operation of the register. By using a core matrix, the combinations of pulses can be obtained by merely applying an interrogation pulse to the correct row in the matrix.

Some of the fixed read-only memories to date include the use of twistors (2), capacitor matrix (3), ferrite slugs (4), and magnetic cores (8).

This study is concerned with determining the operating conditions and some of the necessary characteristics of one individual tape wound core, and then the assembly of a four by four test matrix, operated as a biased core read-only memory, to study some of the problems associated with a memory matrix.

CHAPTER II

PROPERTIES OF MAGNETIC CORES AND THE READ-ONLY BIASED MAGNETIC CORE

Single Core Operation

An ideal magnetic core would have a magnetic characteristic as shown in Figure 2, however, a more realistic representation for the characteristic of a typical core is shown in Figure 3.

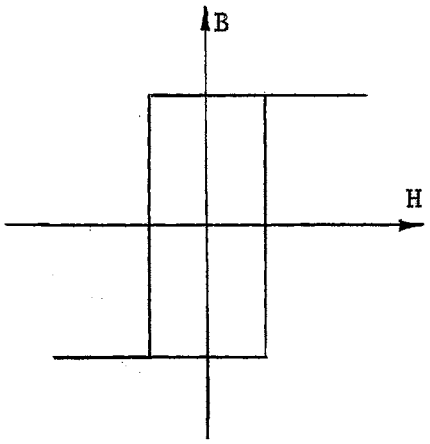


Figure 2. Ideal Magnetic Characteristic of a Core

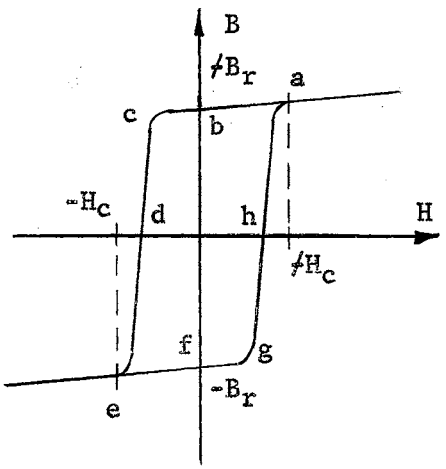


Figure 3. Realistic Magnetic Characteristic of a Core

If a wire is wound around a core and a current passed through the wire, a magnetic field is set up surrounding the wire and the core. A magnetomotive force, NI, (the number of turns of wire times the current in amperes flowing in the wire) is created which will

magnetize the core in one of two directions, as shown in Figure 4.

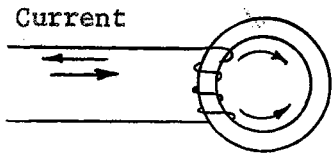


Figure 4. The Directions of Magnetization in a Core

The direction in which the core is magnetized depends upon the direction in which the current is flowing in the wire.

H, the magnetic field intensity, is proportional to magnetomotive force, NI, so that in Figure 3 the units of H will be proportional to ampere-turns. B is magnetic flux density and is proportional to magnetic flux ϕ, whose units are maxwells, so that B will be proportional to maxwells.

When an mmf (magnetomotive force) of $+H_c$ is applied, the core will have a flux density corresponding to point a in Figure 3. Then if the mmf is decreased to zero, the core flux density will move to point b, and the core will retain an amount of flux density equal to $+B_r$, until another mmf is applied. Likewise, if an mmf equal to $-H_c$ is applied and then removed, the state of the core will be at point f and an amount of flux density equal to $-B_r$ will be present in the core.

The ability of a core to store or retain information is called remanence and the value of flux density equal to B_r is called the remanent flux density. Therefore, if the core contains an amount of

flux equivalent to $+B_r$, we can arbitrarily assign this state a value of Boolean ONE, and if the core contains a $-B_r$ amount of flux density it is in the Boolean ZERO state. Thus, the magnet core is a binary storage device.

To change the state of the core from a ONE to a ZERO or vice versa, an mmf with a magnitude of at least H_c must be applied. If a small mmf such as $H_c/2$ or $H_c/3$ is applied, the core will not switch from one state to the other, but will return to almost the original state. This allows a core to be partially driven without changing the state of the core.

Coincident Current Operation

Because a core can be partially excited without changing its state, this enables one to arrange the cores in a matrix which can be used as a memory device. A simple coincident current matrix is shown in Figure 5a, along with the hysteresis loop for a core operated by coincident current shown in Figure 5b.

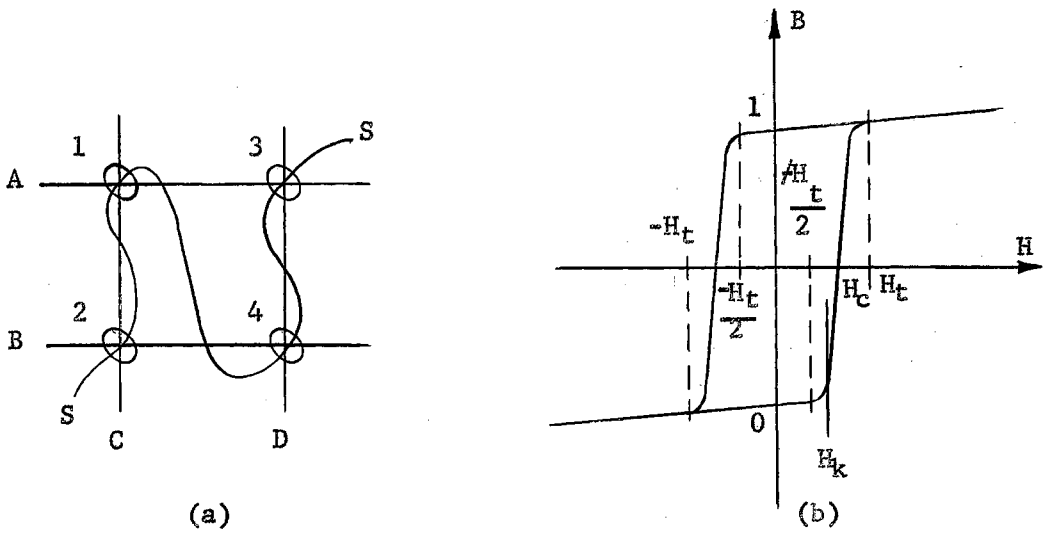


Figure 5. Coincident Current Matrix

If a current of $\pm I_t/2$ (where I_t produces an mmf of H_t) is applied to each of two intersecting wires, the core at the intersection will be forced into the ONE state. Similarly, if a current corresponding to $-H_t/2$ is applied to each of two intersecting wires, the core at the intersection will be forced into the ZERO state. For example, if lines B and D have half currents $I_t/2$ applied to them, respectively, core number four will be forced into the ONE state. At the same time, cores two and three will receive half currents, but this half current will not change their state. If core number four was in the ZERO state previously, it would have been changed into the ONE state, and a complete flux reversal would have occurred. But if the core was already in the ONE state when the half currents were applied, a small flux change would occur, but the core would remain in the ONE state.

If all the cores are linked by a sense line, or output line, the change in flux caused by the core changing from the ZERO state to the ONE state will induce a voltage and is detected at the terminals SS.

In general, to write information into the matrix, half currents of amplitude $-I_t/2$ are applied to all the lines, thus setting all the cores to the ZERO state. Then, the cores selected to be in the ONE state will be set, by applying a $\pm I_t/2$ current to the desired lines.

Coincident current selection in terms of the hysteresis loop is explained in Figure 5b. Half currents correspond to $H_t/2$ or $-H_t/2$. Full currents correspond to $\pm H_t$ or $-H_t$. The best suited cores are cores in which H_k exceeds $H_t/2$ by as large a factor as possible.

The sense line in a coincident current matrix memory links all the cores in a given plane. Therefore, when information is read out

of the matrix, undesired voltages induced by the half selected cores will be present. For example, in a sixty-four by sixty-four matrix, during one read cycle there will be the desired signal (either a ZERO or a ONE) plus small signals from 126 half selected cores. It can be seen that if these 126 small signals were to add they could present a signal as large or larger than the desired signal. This means that a ONE could be detected when the selected core actually contained a ZERO. Of course, if the hysteresis loop was perfectly flat in the saturation region, these half selected cores would not induce a voltage in the sense line. But since the hysteresis loop is not flat, this problem must be overcome. One way to approach this problem, is to link the sense winding through the matrix cores in alternating polarities, so that equal numbers of half-selected cores provide positive and negative signals. If the sense winding is linked correctly, the undesired signals will cancel, thus leaving only the desired signal. Besides having the sense winding linked correctly, the characteristics of all the cores must be uniform, and there must also be uniform driving functions in order for the undesired signals to cancel.

The operation of a coincident current matrix as described here, is one in which the information is read-out by resetting all the cores to ZERO, thus destroying the information. Usually, the information is then rewritten back into the memory for possible future use. If it is desired to read-out this same information a second time, it must first be rewritten into the matrix. This type of read-out is called destructive read-out.

The coincident current method of selection has been described

in order to gain a better understanding of the biased magnetic core read-only principles. Coincident current selection is probably the widest used method of magnetic core storage.

Biased Magnetic Core Read-Only Matrix

The biased magnetic core read-only matrix incorporates a different technique than the coincident current matrix. A three by three biased magnetic core matrix and the hysteresis loop for a biased core are shown in Figure 6a and 6b, respectively.

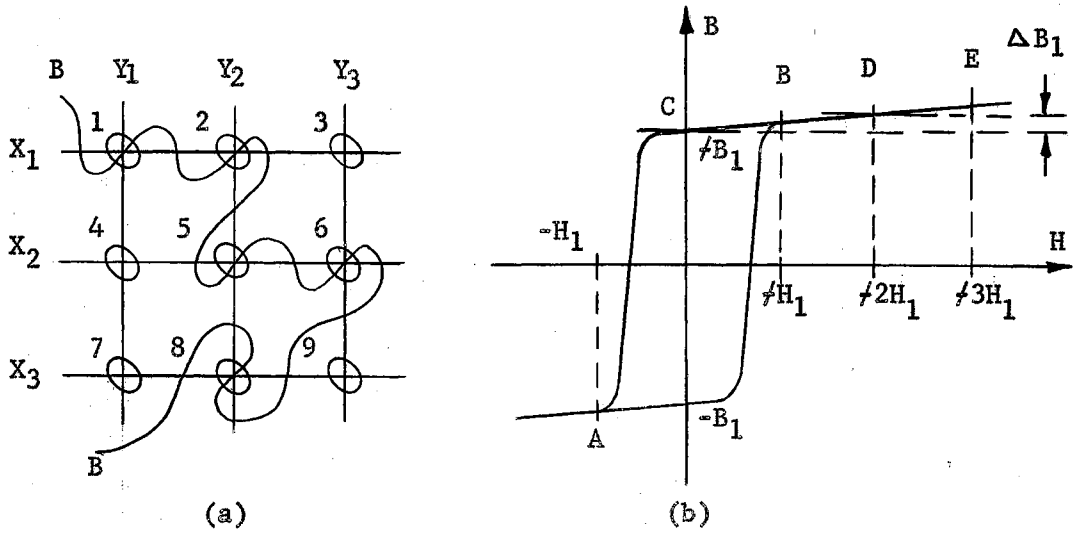


Figure 6. A Biased Core Matrix

The lines X_1, X_2, and X_3 are the interrogation lines, sometimes referred to as input lines. Y_1, Y_2, and Y_3 are the output or sense lines, and BB is the bias line. The bias line and the bias current are arranged to apply an mmf of $-H_1$ to those cores on which the bias line is wound. This bias will hold the state of the cores at point A, as shown in Figure 6b. The state of the cores without bias will be at point C, after they have once been pulsed. The interrogation

current will correspond to an mmf of $\nearrow 2H_1$. When the interrogation current is applied, the state of the biased cores will be forced to point B. Then when the current is removed, the state of the cores will snap back to point A. When the interrogation current is applied and removed to a core which is not biased, the state of the core will move from point C to point D and then back to point C.

As an illustration, assume that line X_1 is interrogated. Core number one and number two will undergo a complete flux change, that is, as the state of the core moves from point A to point B and back to point A, the flux density will change from $-B_1$ to $\nearrow B_1$ and then from $\nearrow B_1$ back to $-B_1$. Contrary to this, the state of core number three, moving from point C to point D and back to point C, will have a very small flux change, ΔB_1. Due to the large flux change in cores number one and two a large voltage will be induced in sense lines Y_1 and Y_2, respectively. Sense line Y_3 will have a relatively small voltage induced in it, since the flux change in core number three is very small.

The bias line could be threaded through all the cores, and still achieve the same pattern of information that was obtained by threading the bias line only through the cores intended to store a binary ONE. This is done by winding the bias line on the core intended to contain a binary ZERO, in such a manner that the bias current would apply an mmf equal to $\nearrow H_1$ to the core and the state of the core would then be biased at point B. When a core held at point B is interrogated, the state of the core will move from point B to point E. When the bias line is omitted from a core the state of the core moves from point C to point D when interrogated.

The amount of flux change that occurs is approximately the same for both methods, if the part of the hysteresis loop from point C to point E is linear. The choice of which method would be used when building a matrix would depend on which method is most convenient and economical in building.

From Figure 6a it is seen that the row X_1 stores the binary characters 110. Likewise row X_2 stores 011 and row X_3 stores 010. Therefore, any combination of ONES and ZEROS desired can be stored in the matrix, by properly winding the bias line.

A read-only core matrix will have only one line interrogated at a time. This is referred to as linear selection. The number of drivers associated with linear selection is considerably more than with a general purpose core memory. But as mentioned in the Introduction, the read-only core matrix does not require the write-in current drivers and the associated address selection logic as required by the general purpose core memory. A typical timing diagram for the matrix in Figure 6a is illustrated in Figure 7. Because only one input line is pulsed at any instant, only one signal is induced in the output line at that instant. The problems of having

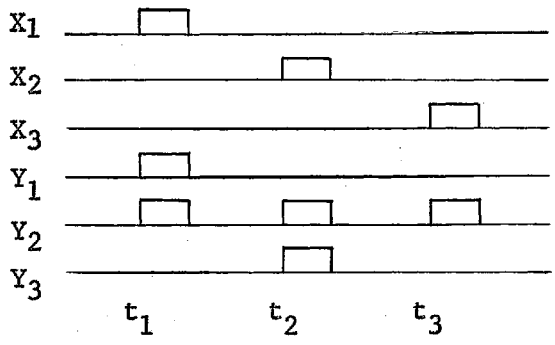


Figure 7. Timing Diagram

undesired signals in the output are practically non-existant as compared to the coincident current matrix.

The biased magnetic core matrix is truly a read-only memory. Once the bias line is wired into the matrix, the only way to alter the information would be to rewire the bias line. By originally wiring in more than one bias line, the matrix could be used to store different sets of information. The read-out time for this type of memory is in the order of 0.1 microsecond to 10 microseconds, depending on the characteristics of the specific cores used.

CHAPTER III

EXPERIMENTAL DETERMINATION OF THE OPERATING CONDITIONS

General Procedure

The magnetic characteristics of the tape wound cores selected for incorporation into an experimental matrix were unknown. One of the facets of the study then was to make suitable tests to determine some of the necessary characteristics of the cores.

The physical dimensions of the cores were found to be, 3/16 inch outside diameter, 3/16 inch in width, and total tape thickness 1/16 inch. The tape itself was approximately 1/4 mil in thickness.

Losses in a core are an important point to consider. The major losses associated with tape wound cores is accountable to eddy currents. (7), (9). The eddy current losses can be reduced by decreasing the thickness of the tape, but this has limiting factors. The major causes for the losses in a ferrite core are hysteresis loss and changes in permeability of the core. The relative losses in tape wound cores are generally less than the losses in ferrite cores.

For a core to operate acceptably, the values of input voltage and current and the bias current must be determined within a suitable range. The operation of a biased magnetic core requires that the input mmf be approximately twice that of the bias mmf.

If a small value of current corresponding to $-H_1$ is applied to the bias line, and a current corresponding to $\neq 2H_1$ applied to the input line, the hysteresis loop the state of the core will follow, will be similar to hysteresis loop number one in Figure 8. As the

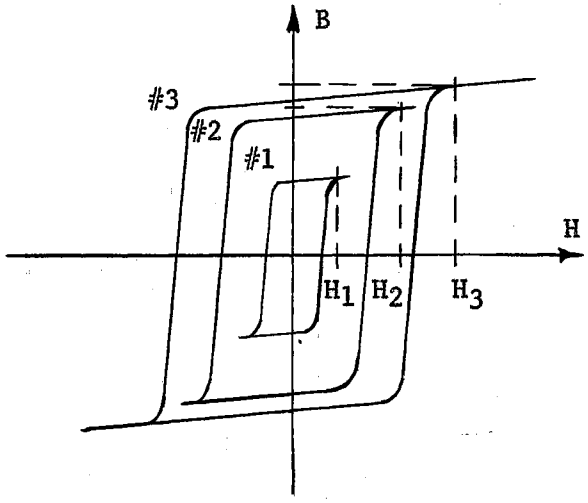


Figure 8. The Resulting Hysteresis Loops as the Input MMF and Bias MMF are Varied.

input current and bias current are increased, always keeping a 2:1 ratio, the resulting hysteresis loops of the state of the core are similar to hysteresis loops two and three. That is, when the core becomes saturated, increasing the bias and input mmf's will not produce an appreciable increase in the amount of flux change. Therefore, a bias current and input current corresponding to $-H_2$ and $\neq 2H_2$ would be the ideal operating currents. The ratio between the input and bias mmf's do not necessarily have to be exactly 2:1. But if the input mmf is too small, the core may not switch. So the input mmf should be just large enough to dependably switch the core.

Faraday's law of electromagnetic induction expresses the

relationship between electromotive force and rate of change of magnetic flux as,

$$E = -N \frac{\Delta \phi}{\Delta T}$$

where E is average emf in volts.

N is number of turns on the core.

ϕ is change in flux in webers.

T is time in seconds for the change in flux to take place.

The circuit constructed to conduct the tests is shown in Figure 9. The input current was supplied by a Rutherford Pulse Generator, Model B7B. A Lambda Model C-880M D-C power supply was used for the bias current. A Hewlett-Packard Current Probe, Model 456A, was used in conjunction with an oscilloscope to view the input current, bias current and output current. The output voltage was monitored with a Tektronix Oscilloscope, Model 545, with a 53/54C Dual-Trace Plug-In Unit. The Rutherford Pulse Generator is capable of an output pulse of fifty volts and having a variable repetition rate to two megacycles, variable pulse delays and widths to 10,000 microseconds, variable rise and fall times of fifteen millimicroseconds, and a permissible duty factor of thirty percent, at full amplitude. The output should be matched to fifty ohms and this gives the output pulse an amplitude of one ampere at fifty volts. The input pulse was chosen to be five microseconds in duration and have a repetition rate of 20,000 pps. There were five turns on the input winding, and two on the bias and output windings, respectively.

Output Voltage and Measurement of Change in Flux

The first attempts made to determine the operating input and

bias currents for a core, were based on the theory, that as the input and bias mmf's are increased, the saturation region would be

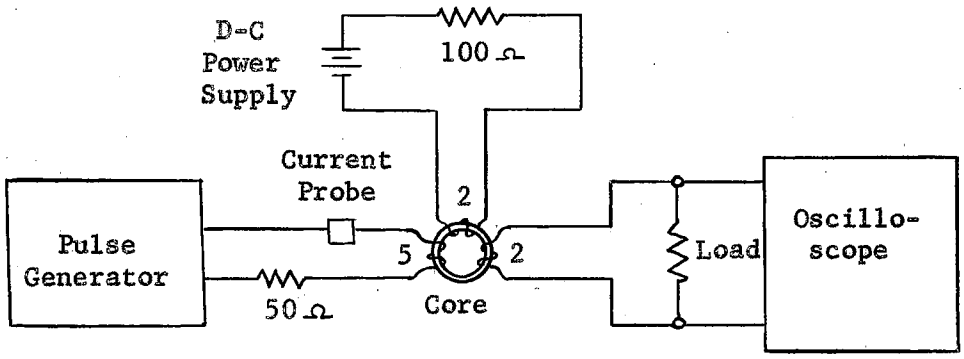


Figure 9. Test Circuit for One Core

reached, and the change in flux $\Delta\phi$ would then become constant. Likewise, the induced voltage, would also become constant. But this is true only if the time, ΔT, for the change in flux to take place, is constant. As the core is driven farther and farther into saturation, the time required for the flux to switch becomes shorter. So, the output voltage continues to rise, even though the $\Delta\phi$ has become constant. By viewing the output voltages on an oscilloscope, it is not apparent when the core becomes saturated, and the input and bias current could not be determined.

Since the voltage did not become constant as the input and bias mmf's are increased, the change in flux had to be investigated. By Faraday's law of electromagnetic induction, the magnetic flux is the integral with respect to time of the induced voltage. Thus, by integrating the output voltage, the total amount of flux change could be recorded.

A simple R-C integrating network was incorporated into the output circuit as shown in Figure 10.

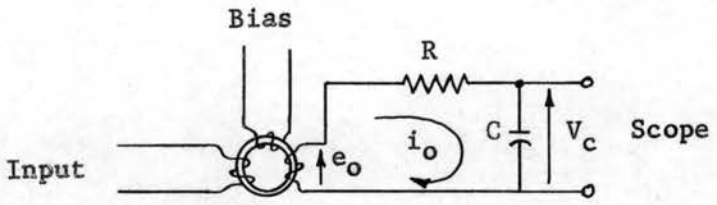


Figure 10. Test Circuit with a R-C Integrating Network

If the time constant of RC is much larger than the time length of the output voltage, then the network will give a fairly accurate integration of the output voltage. An electronic integrator, such as a d-c operational amplifier used in a wide-band analog computer, would have been more accurate, but for this application was not deemed necessary.

To clarify how the change in flux is found from this circuit, the differential equation for the induced output voltage is written,

$$e_o = i_o R + \frac{1}{C}\int_o^t i_o dt \tag{1}$$

$$\frac{e_o}{R} = i_o + \frac{1}{RC}\int_o^t i_o dt. \tag{2}$$

With RC sufficiently large, the term $\frac{1}{RC}\int_o^t i_o dt$ is much smaller than i_o therefore,

$$\frac{e_o}{R} \approx i_o \tag{3}$$

The voltage across the capacitor is,

$$V_c = \frac{1}{C}\int_o^t i_o dt \tag{4}$$

and substituting for the output current gives,

$$V_c = \frac{1}{C}\int_o^t \frac{e_o}{R} dt \tag{5}$$

or it can be written,

$$V_c RC = \int_o^t e_o dt. \tag{6}$$

From Faraday's Law,

$$\phi = \frac{1}{N} \int_o^t e_o dt \tag{7}$$

or

$$N\phi = \int_o^t e_o dt. \tag{8}$$

Equating (6) and (8) we obtain,

$$\phi = \frac{RC}{N} V_c \tag{9}$$

where RC is in seconds.

N is the number of turns on the output.

V_c is in volts.

ϕ is in webers.

Since one weber is equal to 10^8 maxwells, the change in flux in maxwells, is given by,

$$\phi = \frac{RC}{N} V_c \times 10^8 \tag{10}$$

The change of flux vs. the bias ampere turns with drive current equal to two times the bias current, is shown in Figure 11. From this curve it is noted that the saturation region is substantially reached at 0.45 ampere turns. Now it is known that if the core has a bias mmf of -0.45 ampere turns, and the applied input mmf is 0.9 ampere turns, the change in flux that occurs will be a maximum value.

Input Current

Another point of interest is the input current waveform. When the input current is not large enough to switch the core, the waveform is very square. But when the input current is large enough to switch the core, the waveform takes the shape similar to that shown

in Figure 12a.

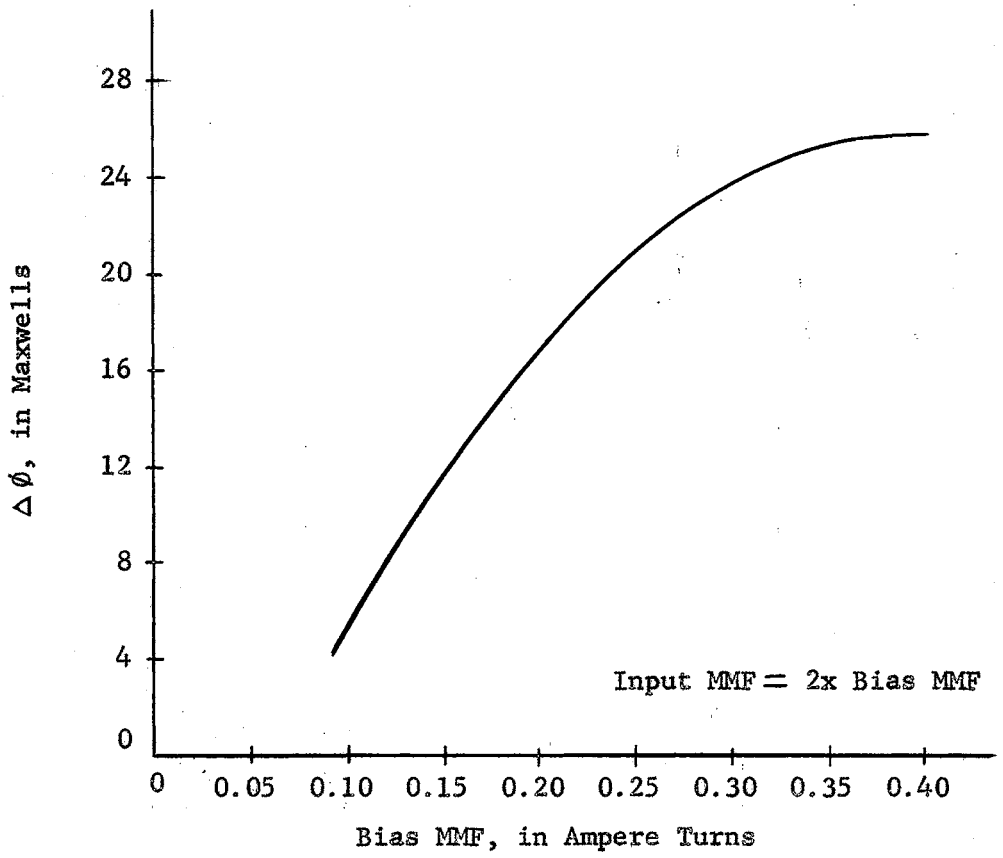


Figure 11. Total Flux Change vs. Bias MMF

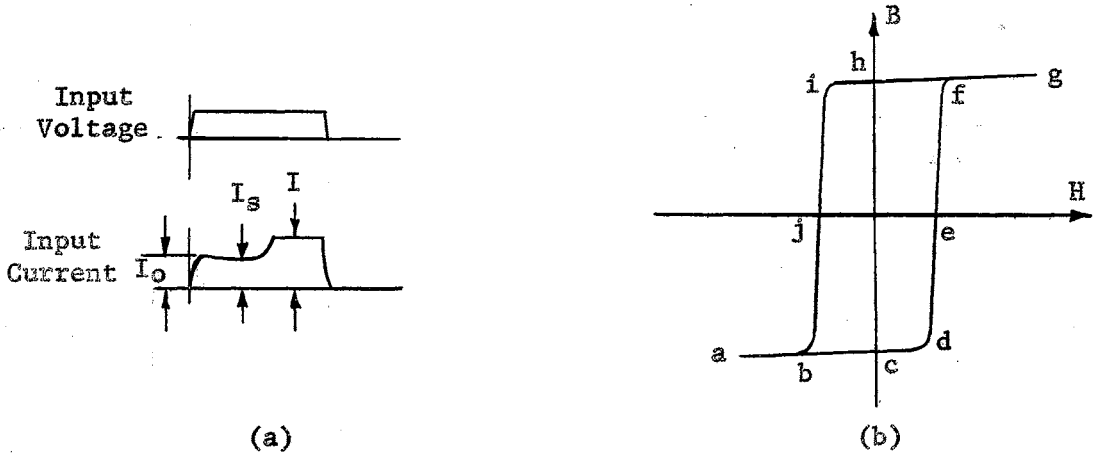


Figure 12. Input Current Waveform

When the input voltage is applied there is an initial current rise of I_o through the input winding. On the hysteresis loop in Figure 12, the current rise, I_o, occurs as the state of the core goes from point b to point d. Then the core switches, the back emf in the input winding limits the current to I_s. During the switching the core appears as a constant resistance R_s. As the core reaches the switching point f, the current reaches a value of I, equal to E/R, where R is the fifty ohm series resistor, and E is the applied input voltage, as shown in Figure 9.

The observance of this waveform is useful in getting a rough estimate of the amount of mmf to switch the core. By setting the bias mmf to a point selected at random, the input mmf can be varied from a small value (small enough so that the core is not switching), to a value large enough to switch the core. When the input current waveform begins to show a plateau, then the core is starting to switch. This procedure might have to be repeated with different values of bias mmf, in order to find the saturation region.

Figure 13c shows the input current when the core is switching. The bias mmf is 0.5 ampere turns and the input mmf is 1.0 ampere turn, with a 450 ohm load resistor on the output winding.

Bias Current

The bias current was supplied by a variable 0-50 volts d-c power supply. A 100 ohm resistor was used to limit the current to a range of 25-500 milliamperes. With two turns on the bias winding, a range of 0.25 ampere turn to 1.0 ampere turn, is available for the bias mmf.

The bias circuit to some extent will act as a load for the driving circuit. A voltage will be induced in the bias winding just the same as the induced voltage in the output winding. This means that in the bias circuit there will be a 20,000 pps current superimposed on the d-c current. The magnitude of the current pulses is controlled by the impedance in the bias circuit. This pulsing current is not desirable because the driving circuit must dissipate this wasted energy. The simplest solution is to put a series inductor in the bias circuit, and thereby provide a large impedance for the high frequency current pulses. Using the same circuit as shown in Figure 9, except that the Hewlett-Packard Current Probe was moved into the bias circuit, the bias current was examined. Inserting several inductors, ranging from about 5 microhenrys to 0.5 millihenry, into the bias circuit showed no appreciable change in the magnitude of the bias current. Therefore, it was decided that the addition of an inductor was not necessary, and that the 100 ohm resistor provided enough impedance. The bias current is shown in Figure 13e.

From the conclusions drawn from the tests, it was decided to bias the core at -0.5 ampere turns, and that the input driving mmf would be 1.0 ampere turn. With two turns and five turns on the bias and input windings, respectively, the bias current would be 250 milliamperes and the input current 200 milliamperes. Waveforms of the output voltage, output current, input current and bias current are shown in Figure 13. The output voltage is shown for a fifty ohm and a 450 ohm load resistor. The pictures of the output current, input current and bias current were taken with an output winding load

of 450 ohms.

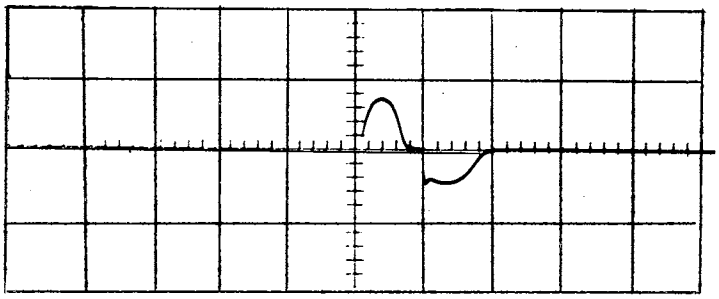


Figure 13a. Output Voltage with 50 Ohm Load
Vertical Scale: 1 volt/cm., Time Scale: 5 usec/cm.

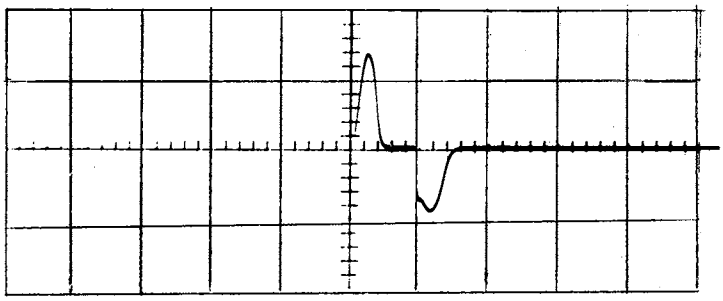


Figure 13b. Output Voltage with 450 Ohm Load
Vertical Scale: 2 volts/cm., Time Scale: 5 usec/cm.

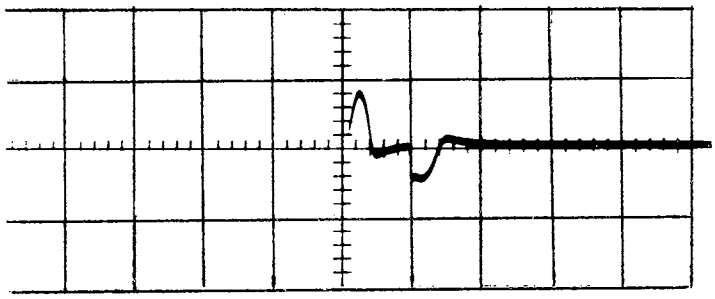


Figure 13c. Output Current with 450 Ohm Load
Vertical Scale: 5 ma./cm., Time Scale: 5 usec/cm.

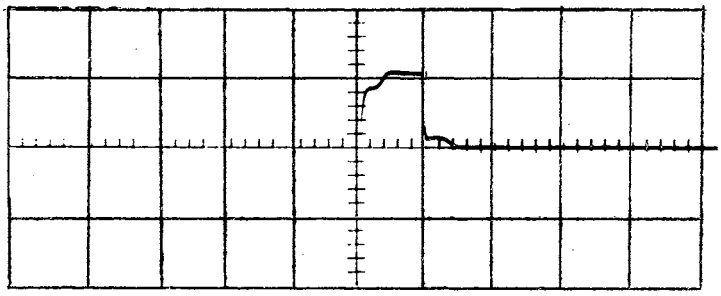


Figure 13d. Input Current with 450 Ohm Load
Vertical Scale: 50 ma./cm., Time Scale: 5 usec/cm.

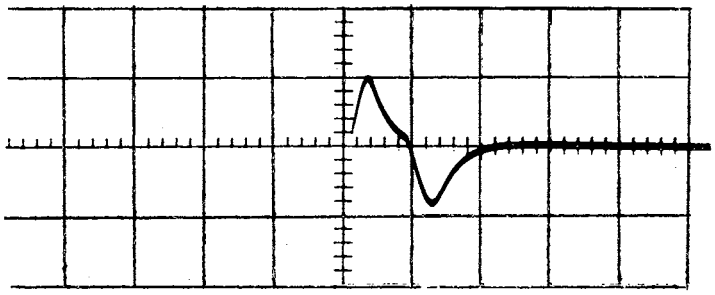


Figure 13e. Bias Current with 450 Ohm Load
Vertical Scale: 5 ma./cm., Time Scale: 5 usec/cm.

Figure 13. Waveforms with the Bias MMF at 0.5 A-T and Input MMF at 1.0 A-T.

CHAPTER IV

CHARACTERISTICS OF A BIASED CORE

Using the operating conditions established in Chapter III some of the characteristics of a core were investigated. The circuit shown in Figure 9 was used for the tests which include back voltage, output voltage waveform, switching time, and loading effects.

Back Voltage

The back voltage is the self induced voltage generated in the input winding on the core. Figure 14 shows the input pulse circuit with the back voltage being designated by e_1.

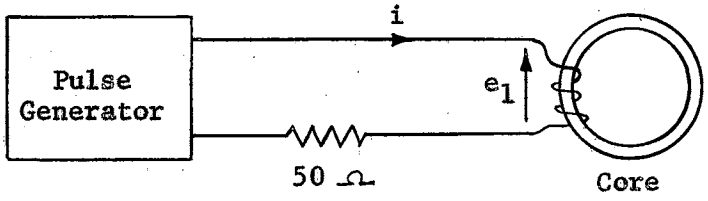


Figure 14. Input Circuit

The induced voltage is given by the relationship,

$$e_1 = -N \frac{d\phi}{dT} . \qquad (1)$$

An equivalent expression for the back voltage in terms of the input current is,

$$e_1 = -L \frac{di}{dt} \qquad (2)$$

where e_1 is in volts.

L is in henrys.

$\frac{di}{dt}$ is in amperes/second.

By writing equation (2) in the form,

$$L = \frac{-e_1}{di/dt} \qquad (3)$$

the inductance can be calculated from experimental data. The back voltage was measured with the Tektronix 545 oscilloscope and the input current was monitored on the scope by using the current probe. The risetime of the current was approximately 0.020 microseconds. The results are shown in Table I.

No. turns on Input Winding	Input Current	$-e_1$	Calculated Inductance	Inductance per turn
5	200 ma.	2 volts	0.2 uh	0.04 uh
2	500 ma.	2 volts	0.08 uh	0.04 uh

Table I. Back Voltage and Calculated Inductance

Output Voltage Waveform

The output voltage waveform is given by,

$$e_1 = -N \frac{d\phi}{dt} \qquad (4)$$

and depends upon the operating conditions applied to the core.

When the core is biased with an mmf equal to $-H_a$, and driven by an input pulse with an mmf equal to $\neq 2H_a$, as shown in Figure 15a, the relationship between the input voltage, input current, induced flux, and induced voltage is shown in Figure 15b. But when the core is overdriven, i.e., biased with an mmf equal to $-H_b$ and driven by an input pulse with an mmf equal to $\neq 2H_b$, the relationship of input

voltage, input current, induced flux, and induced voltage is altered to that shown in Figure 15c. In general, operating the state of the core between points A and A' would be acceptable operating conditions and operating between points B and B' would be overdriving the core.

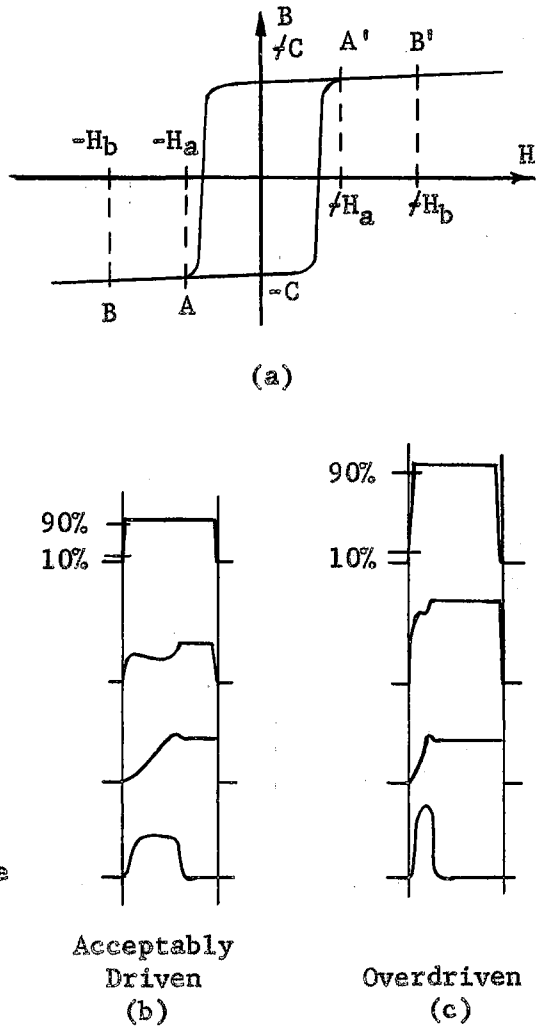


Figure 15. Comparison of Various Waveforms for Different Input Pulses.

Comparing the input voltage of the acceptably driven core with the input voltage of the overdriven core, it is noted that the amplitude of the latter is much larger. Even though the amplitudes are unequal, the risetime (10% to 90%) for each voltage will be very nearly equal. Thus the time for the state of the core to move from

A to A' is the same as to move from B to B'. This further means that the flux changes much faster when the core is overdriven than when it is not overdriven. This is shown in Figure 15.

Since a voltage is induced only when the flux is changing, the width of the induced voltage depends on the length of time the flux is changing. A slowly changing flux induces a wide voltage pulse, whereas a fast changing flux induces a narrow output voltage pulse. Thus a highly overdriven core will produce a very narrow output pulse.

A fast changing flux will also induce a larger voltage than a slowly changing flux. The term, $\frac{d\phi}{dt}$, in equation (4) is much larger for a fast changing flux than for a slowly changing flux. Therefore, as a core is farther and farther overdriven, the induced output voltage will become larger in magnitude and very narrow in width.

Figure 16 shows the induced voltage magnitude and width vs. bias ampere turns.

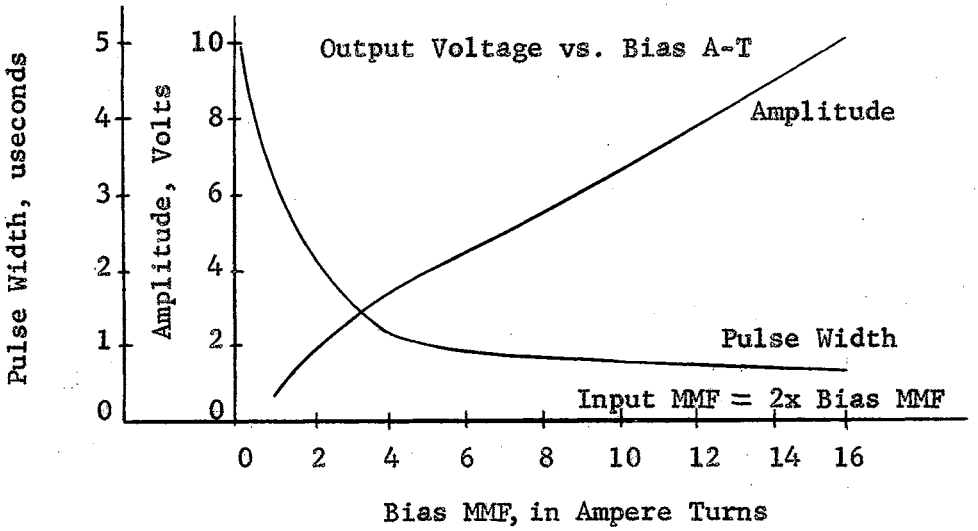


Figure 16. Output Voltage vs. Bias MMF

Positive and Negative Output Signal

The induced output voltage contains a positive and a negative pulse as shown in Figure 13a and 13b.

When the state of the core is biased at point A, in Figure 15a, with an mmf corresponding to $-H_a$, and driven by the input pulse to point A', the state of the core will then snap back to point A as soon as the input pulse falls to zero. The action of the flux density changing from approximately -C will induce a positive output voltage. As the flux density changes from +C back to -C a negative voltage will be induced in the output winding. Therefore, every time that a core is interrogated, a positive pulse as well as a negative pulse will be induced in the output winding. Since only one output pulse is necessary, the unwanted pulse can be removed by a simple diode circuit, or it may not be necessary to do this, because the circuits that receive the information from the core might inherently reject the unwanted pulse.

Switching Time

The switching time of a core is an important characteristic. By knowing the approximate switching time, an estimate of the access time for a memory unit can be made. The access time being the time interval between the instant at which the arithmetic unit calls for the information from the memory unit and the instant at which the information is delivered from the storage to the arithmetic unit. Access time might be a deciding factor as to whether a memory device is suitable for a computer memory.

The switching time, T_{sw}, is defined as the time interval between the 10% points of the output voltage waveform, as shown in Figure 17.

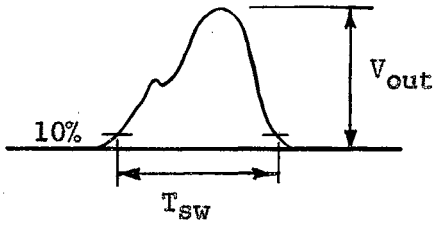


Figure 17. Output Voltage - Defining Switching Time, T_{sw}

From Figure 13b the switching time can be estimated to be 2.0 microseconds. At the expense of increasing the input mmf the switching time can be reduced to around 0.6 microseconds. This requires more power and would only be done when absolutely necessary.

Load Effects

The output from a memory is normally fed into a register or to some type of logic circuit. The information is either fed directly to these circuits or through a read amplifier. The input impedance of these devices may vary from a few ohms to the order of megohms, depending on whether tubes or transistors are used and in what kind of a circuit. It is therefore, important to find out what happens to the output pulse when subjected to various loads.

Figure 18 shows the amplitude and pulse width of the output voltage, vs. load resistance for loads varying from eighteen ohms to ten megohms.

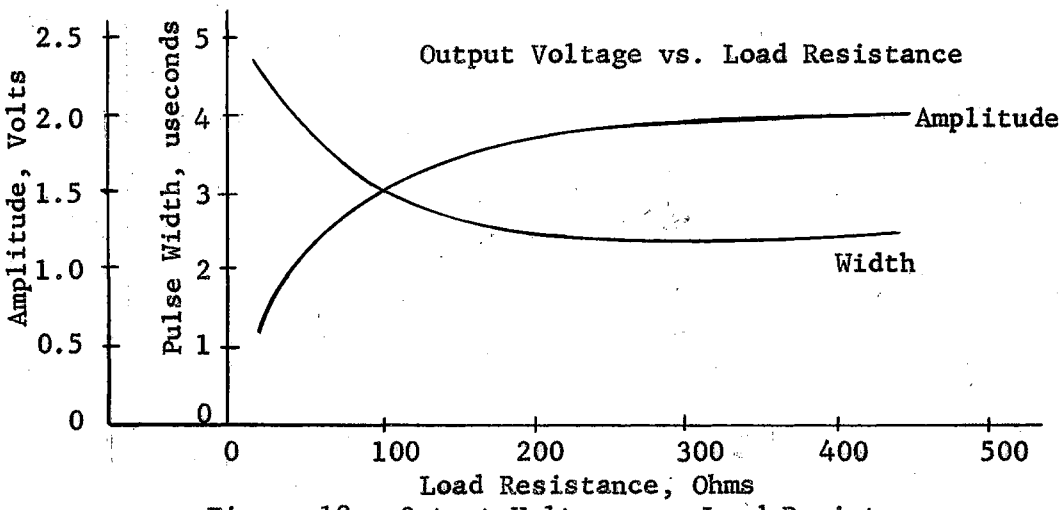


Figure 18. Output Voltage vs. Load Resistance

This shows that as the load increases from eighteen ohms to approximately 200 ohms the amplitude of the output pulse increases and the width decreases. Above 200 ohms the amplitude and width are relatively constant. The information from this test would help to decide what type of read amplifiers to use.

CHAPTER V

TESTING AND EVALUATION OF THE CORE MATRIX

Construction

To evaluate a biased core memory, a four by four test matrix was built. The cores used in the matrix are the same as the core described in Chapter III. A photograph of the memory matrix is shown in Figure 19.

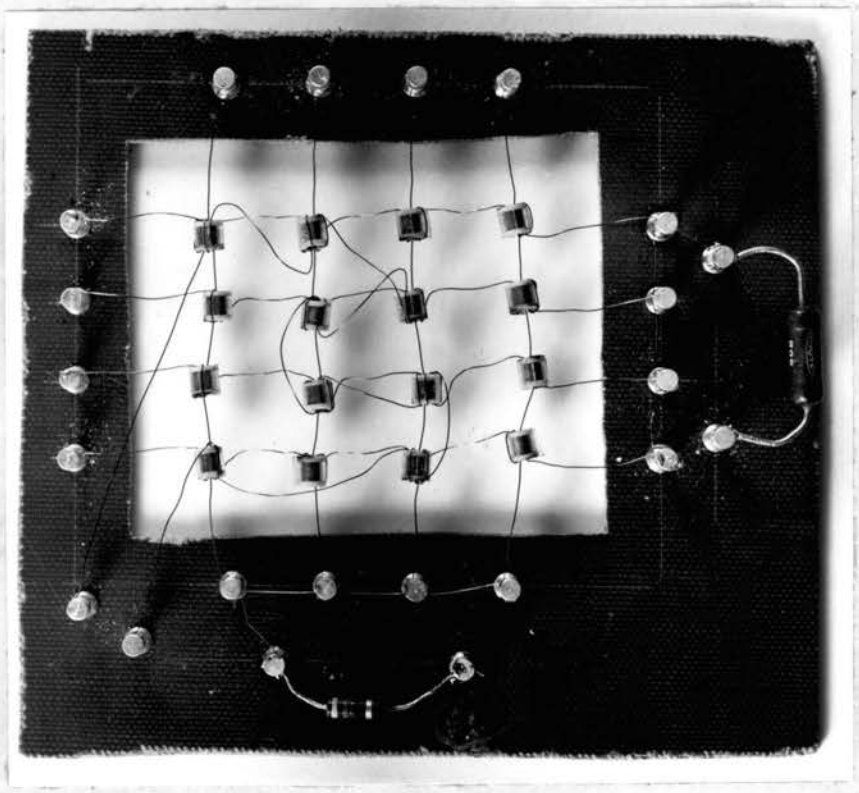


Figure 19. The Test Matrix

The input windings on the cores in rows 1, 2, and 3 have five turns, and the cores in row 4, two turns. The bias windings and sense windings on all the cores have two turns.

The location of the binary information was picked at random and the resulting configuration is shown in Table II.

Input Line	Sense Line 1	2	3	4
1	1	1	0	0
2	0	1	1	0
3	0	1	1	0
4	1	0	1	0

Table II. Bit Pattern Stored in the Memory

The wire used for the input lines, bias line, and sense lines was #32 AWG copper wire. The matrix was soldered to terminal posts that were mounted on a 1/16 inch thick phenolic frame.

Test Procedure

The test matrix was analyzed for various qualities. The matrix was subjected to various load resistances on the output windings, and a comparison of the binary ONES and ZEROS was made. The back voltage and intercoupling effects were also considered.

Results with Various Loads on the Output Winding

In this case, the information was read from the memory with no

load on the output winding, except for the scope which was ten megohms. This set of information is shown in Table III.

0.4	0.4	0.1	0.1
0.1	0.41	0.4	0.1
0.1	0.4	0.4	0.1
0.5	0.2	0.5	0.2

Table III. Output Voltages with No Load (Peak volts)

The average value for a binary ONE is 0.4 volts and for the binary ZERO is 0.1 volts, in the first three rows. The average value for the binary ONE is 0.5 volts and the average binary ZERO is 0.2 volts, in the fourth row. This gives a 4:1 ONE-to-ZERO ratio for rows 1, 2, and 3, and 2.5:1 ratio for row 4.

In the second case, a 450 ohm resistor was placed across the output windings and the results are shown in Table IV.

0.35	0.36	0.2	0.18
0.15	0.37	0.31	0.17
0.17	0.35	0.35	0.18
0.50	0.20	0.45	0.20

Table IV. Output Voltages with a 450 Ohm Load (Peak volts)

The average value for a binary ONE is 0.35 volts, and for the binary ZERO is 0.17 volts, yielding a ONE-to-ZERO ratio of approximately 2:1, for rows 1, 2, and 3. Row 4 has a ONE-to-ZERO ratio of 2.4:1, with average values of 0.475 volts and 0.2 volts for a binary ONE and ZERO, respectively.

Decreasing the load resistance to 20 ohms gave the information shown in Table V.

0.29	0.30	0.10	0.10
0.10	0.31	0.30	0.10
0.10	0.30	0.30	0.10
0.40	0.20	0.40	0.15

Table V. Output Voltages with a 20 Ohm Load (Peak volts)

The average binary ONE was 0.30 volts and the average binary ZERO was 0.10 volts for rows 1, 2, and 3, giving a ONE-to-ZERO ratio of 3:1. For the fourth row the average binary ONE and ZERO is 0.40 volts and 0.17 volts, respectively. The ONE-to-ZERO ratio is approximately 2:1.

Analyzing all three cases, the best ONE-to-ZERO ratio was 4:1 at no load, and the worst was 2:1. The waveforms of the binary ONE and ZERO, for a ONE-to-ZERO ratio of 4:1, are shown in Figure 20.

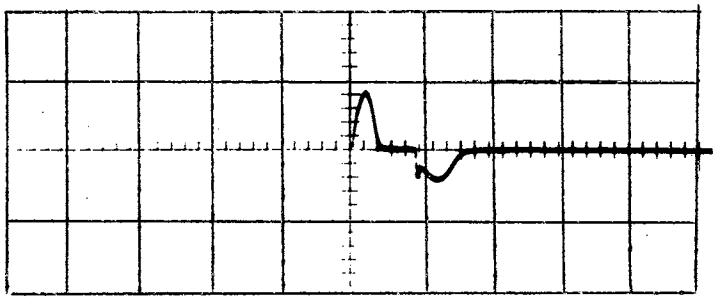


Figure 20a. Binary ONE

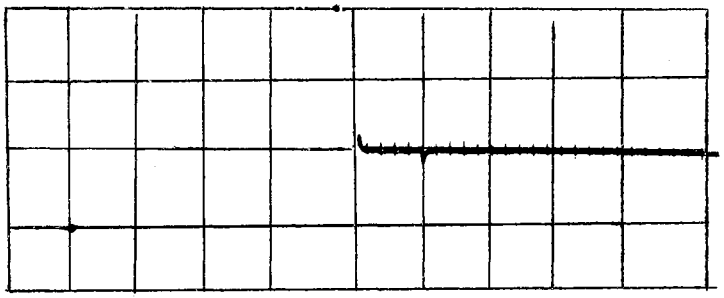


Figure 20b. Binary ZERO

Figure 20. Output Voltages of a Binary ONE and a Binary ZERO. Vertical scale: 0.5 volt/cm., Time Scale: 5 usec/cm.

These ratios are based on the peak amplitude of the output signal. Figure 20 shows that the width of the two pulses are quite different, and that the amplitude of the output signal should not be the only factor to consider in deciding on whether or not these two pulses are easily and acceptably detected as a binary ONE or a binary ZERO. The width of the binary ONE is approximately 2 to 2.5 microseconds in duration, and the average width of a binary ZERO is 0.2 microseconds. Therefore, even though the ONE-to-ZERO ratio of the amplitude is only 2:1 in the worst case, the difference in widths makes the pulses quite distinguishable.

The results also show that the output voltage amplitude of the binary ONE decreased in approximately the same manner, as the load resistance was decreased, as was discussed in Chapter IV. The output voltage representing the binary ZEROS is relatively independent of the load as compared with the output voltage representing the binary ONE, and therefore in considering which load would give the best output, the higher load resistances provide the largest ONE-to-

ZERO ratios.

Back Voltage

Consider the circuit shown in Figure 21 to be for row number one of the memory matrix.

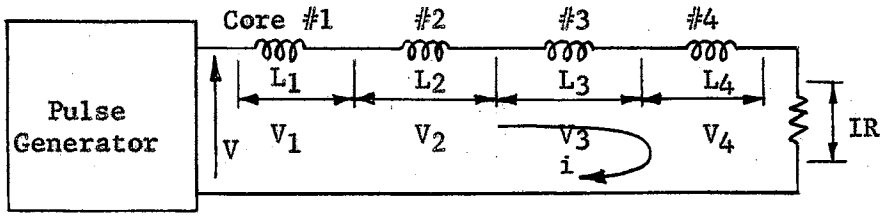


Figure 21. Circuit for an Input Line of the Test Matrix

L_1 is the inductance of the input winding corresponding to the core in column one, and likewise L_2, L_3, and L_4 correspond to the inductance of the input windings on the cores in columns 2, 3, and 4. The binary information stored in this circuit is 1100. Cores number one and two being biased while cores three and four are not biased. The circuit voltage equation is,

$$V = L_1 \frac{di}{dt} + M_1 \frac{di}{dt} + L_2 \frac{di}{dt} + M_2 \frac{di}{dt} + L_3 \frac{di}{dt} + L_4 \frac{di}{dt} \qquad (5)$$

where $V_1 = L_1 \frac{di}{dt} + M_1 \frac{di}{dt}$

$V_2 = L_2 \frac{di}{dt} + M_2 \frac{di}{dt}$

$V_3 = L_3 \frac{di}{dt}$

$V_4 = L_4 \frac{di}{dt}$.

The voltage drop across the input winding of core number one and core number two are made up of a self-induced voltage and a mutually induced voltage. The mutually induced voltage is caused by the bias winding and adds to the self-induced voltage.

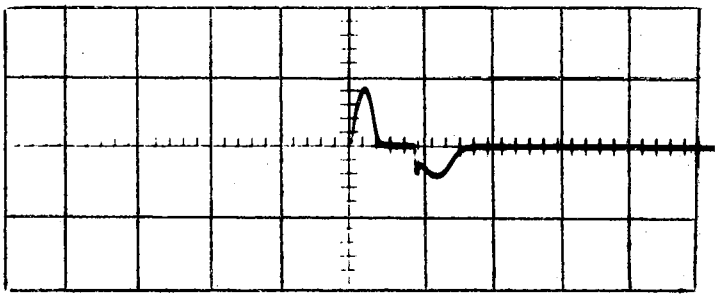
Using rows one and four of the test matrix the oscilloscope was used to measure the voltage drop around the circuit. The results are shown in Table VI.

	Row 1	Row 4
V_1	0.8 volt	0.7 volt
V_2	0.8 volt	0.3 volt
V_3	0.4 volt	0.6 volt
V_4	0.4 volt	0.3 volt
IR	6.0 volts	16.0 volts

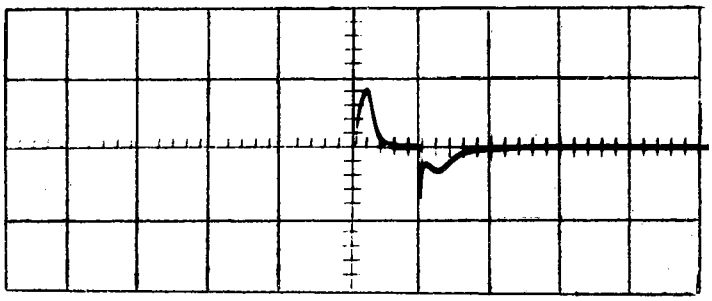
Table VI. Voltage Drops in the Input Circuit.

This table shows that the back voltage of a biased core is approximately twice that of an unbiased core. There is nothing significant about the fact that the back voltage of a biased core is twice that of an unbiased core, but there is a reason that it is larger. To explain this, consider the amount of flux change that is involved. Since the back voltage is proportional to the change in flux, the biased core will have a much larger flux change than an unbiased core, thus inducing a much larger back voltage. The action of the flux is explained in Chapter II.

The effect of the back voltage generated when four cores are put in series is illustrated in Figure 22. Figure 22a shows the



(a)
Binary ONE from the Matrix



(b)
Binary ONE from an Individual Core

Figure 22. Comparison of a Binary ONE when read from the Matrix to a Binary ONE Operated Individually Vertical Scale: 0.5 volt/cm., Time Scale: 5 usec/cm.

output voltage of a binary ONE when monitered from the matrix, and Figure 22b is the output voltage of a binary ONE when only a single core was operated.

The increased amount of back voltage, when the cores are in matrix form, makes the waveform of the binary ONE a little wider and cuts down on the large negative spike. The difference in the two waveforms is so small, it can be neglected for most applications.

In considering the construction of a large memory matrix, such as a sixty-four by sixty-four matrix, the back voltage of the cores would certainly be an important factor. The back voltage generated by each core will add, and therefore the capability of the drivers have to be considered. A driver must be capable of supplying the

correct voltage and current in order to switch the desired cores.

Intercoupling Effects

If two wires are parallel and have only a small seperation between them, most of the flux created by a current in one wire will link with the other wire providing good electromagnetic coupling. Also, the capacity between closely spaced wires is relatively high and a variation in the voltage in one wire will be effective in inducing a voltage in the other by electrostatic coupling.

The biased magnetic core memory investigated in this study has linear selection, which means that only one input line is pulsed at a time. By pulsing only one line at a time, the intercoupling effects are negligible. For example, when row two in Figure 19 is pulsed, the only signal available for each sense line has been initiated by the input from row two. Figure 22 shows that any intercoupling effects present in the matrix are negligible.

Switching Time

The switching time for a single core was discussed in Chapter IV, and this discussion is true for matrix operation also. The input pulse width used was five microseconds in duration, and this gave an output pulse of approximately two microseconds wide. The input pulse width was reduced from five microseconds to two microseconds and the output pulse did not change in amplitude or width, but of course, the negative part of the output pulse occured after two microseconds from the start of the cycle, instead of after five microseconds.

As mentioned in Chapter IV the output pulse width can be reduced

to around 0.6 microseconds by overdriving the core.

Variations of the Risetime of the Input Pulse

The Rutherford Pulse Generator, having an adjustment for the risetime of it's output pulse, makes it possible to test the matrix for an input pulse having different risetimes. The result of increasing the risetime of the input pulse enough to get an overshoot improved the risetime of the induced output pulse, produced a ripple on the leading edge, and increased the amplitude a slight amount. Decreasing the risetime enough to cause the leading edge of the input pulse to roll off produced a much slower risetime of the induced output pulse, and a decrease in amplitude. The slow risetime produced an unsatisfactory output pulse, whereas the slight ripple on the output pulse for the fast risetime would be acceptable.

CHAPTER VI

SUMMARY AND CONCLUSIONS

Summary

A biased magnetic core read-only memory was built and some of the problems involved in operating the memory device were studied. Using the following method a simple and effective technique was developed for reading information from a core matrix memory without destroying the information. A bias wire is threaded through the memory in such a manner that will give the desired configuration of binary ONES and ZEROS. When a row of the memory matrix is interrogated with a current pulse, the biased cores will undergo a complete flux reversal, thus inducing a voltage in the sense line. An unbiased core will have only a very small flux change and will induce a comparatively very small voltage, and therefore making the distinction between a binary ONE and a binary ZERO relatively uncomplicated.

One of the facets of the study was to make suitable tests to determine some of the necessary characteristics of the cores. To determine what value of bias mmf and input mmf would be acceptable to operate a core, several different approaches were used. These included analysis of the input current, width of the induced output voltage, amplitude of the output voltage, and measurement of the

amount of change in flux when the core is pulsed. The most informative of these approaches was the latter. To measure the change in flux, the output voltage was integrated, with respect to time, by means of a simple R-C integrating network, thus giving a fairly accurate approximation of the amount of changing flux.

The cores were assembled into a four by four matrix and then tested for different values of load resistance on the output winding. Also, effects of back voltage, intercoupling between wires, switching time, and variation in the width and risetime of the input pulse were analyzed.

In considering building a larger matrix of practical size, such as that mentioned in Chapter V, the biggest problem would be in obtaining drivers that could supply sufficient power to overcome the relatively large back voltage generated at the input winding of each core. If this can be done without sacrificing too much in space and economy, the core matrix will be a very good read-only memory.

Conclusions

The main conclusion to be drawn is that a read-only memory of this type furnishes positive identification of the information stored in the matrix, and that a core matrix is one of the most reliable memory units that can be built. The memory is economical because the cores and techniques used to produce a memory of this type have already been developed and are in use today.

A ONE-to-ZERO ratio of 4:1 was obtained with the binary ONE output voltage being 400 millivolts. The ratio could be made larger

by overdriving the cores, but this would mean an increase in input power. The memory proved to be very satisfactory, and because the matrix has linear selection, it is very reliable as far as noise is concerned.

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