n-PORT MODELING OF LARGE LINEAR NETWORKS

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CHAPTER I

INTRODUCTION

1.1 Statement of the Problem. Systematic methods for formulating the equations describing linear networks have resulted from the application of linear graph theory. Koenig and Blackwell (1) utilized linear graph theory in the development of methods of analysis of complex networks containing electrical and mechanical components. These authors extended the use of linear graph theory to obtain the n-port representation or characteristics of multiport networks. The terms multiport model and n-port model are used synonymously in this thesis to mean the port (or terminal) linear graph and the port (or terminal) equations.

The existence of systematic methods for obtaining network n-port models suggests the possibility of employing a digital computer to formulate and solve the required network equations. This thesis reports on a study to determine a means of employing a digital computer to formulate and compute the n-port models of large networks. Networks containing linear passive one-port and multiport devices and ideal drivers are considered. Basic to the study is the determination of a method to formulate the n-port models of large networks which contain algebraic (electrical conductance or mechanical damper) elements only, together with mixed (both through-variable-independent and across-variable-independent) drivers. Once this method is developed, it is extended to the formulation of multiport models of networks containing

energy storage devices (electrical capacitance and inductance or mechanical spring and mass elements).

Specifically, when the research was initiated, a method was sought which would divide the network into parts, solve each part separately, and form the required n-port model from the divided network solutions. A method was required which could be programmed on a digital computer so that the computer could accept simple input data and compute the desired model without manual analysis.

1.2 Previous Work in this Area. The most recent work in this area was done by Lucky (2). This work describes the obtaining of multiport models of networks containing resistances, ideal voltage and current drivers, and two-port components, specifically three-terminal linear algebraic components, and resulted in a computer program which computes the specified n-port representation for networks of limited size. The techniques used required simple input data to the computer, data obtained from a linear graph of the network.

Other digital computer programs have been written for analysis of electrical and mechanical networks. A program described by Branin (3) computes the d-c and transient responses of transistor circuits. The DYANA program of the General Motors Research Laboratories analyzes networks of arbitrary configurations (4). Both programs are able to formulate and solve the necessary mathematical equations from simple input data; however, neither obtain the network multiport model--the goal of the work reported in this thesis.

The idea of dividing the network into parts, or subnetworks, for analysis was suggested by Lucky. This idea of dividing a network into

smaller units in order to obtain a solution is not new. Kron used this idea in his method of tearing (5, 6). A summary of Kron's method of tearing is given in Appendix A.

1.3 Brief Outline of the Method of Solution. The method of solution involves dividing the network into subnetworks such that an n_i-subport model can be obtained for each subnetwork. The individual subnetwork models are combined to form an m-subport model of the entire network. The desired n-port model for the network is then obtained from the m-subport linear graph model.

The method of solution involves the following steps:

1. Divide the given network in accordance with certain topological restrictions and add driver branches to the ports of the subnetworks.
2. Determine a fundamental tree and cotree for each subnetwork.
3. Determine the fundamental cutset matrix for each subnetwork.
4. Determine the subport model for each subnetwork.
5. Form the composite or m-subport model of the given network by combining the subnetwork subport models.
6. Obtain the required n-port model of the given network from the composite model.

A detailed discussion of the method of solution as outlined above and the network division algorithm are presented in Chapter II. The tree-forming and cutset-forming algorithms are presented in Chapter III. The network information necessary for these algorithms is also discussed.

Chapter IV discusses the modeling of multiport components as individual subnetworks and presents the computer program for obtaining

n-port models of networks containing both one-port and multiport algebraic components. Examples are given.

In Chapter V the multiport modeling of networks containing passive energy storage one-port elements is defined, and the formulation of such models is discussed. The equations are derived to characterize the subnetwork models of such networks. The computer program for obtaining the state-space n-port models of these networks is discussed. Examples are given.

The method of solution which is developed in this thesis, as well as the algorithms and the computer programs derived from the solution method, is completely general and can apply to a variety of types of linear mechanical or electrical systems. The programs can be easily adapted, if they cannot be used in their present form, to systems containing both electrical and mechanical elements. However, in the interest of clarity of presentation, where it is necessary to discuss system elements and system variables, the elements and variables of the electrical network will be used in the following chapters.

CHAPTER II

THE METHOD OF SOLUTION AND THE NETWORK DIVISION ALGORITHM

2.1 Introduction. An n-port model of the following form:

$$\underline{I}_P = \underline{G}_P \underline{V}_P + \underline{G}_D \underline{E}_D + \underline{D}_D \underline{J}_D \qquad (2.1.1)$$

is sought for linear algebraic networks, where

$\underline{I}_P$ is the n-vector of the n-port currents,

$\underline{V}_P$ is the n-vector of the n-port voltages,

$\underline{E}_D$ is the p-vector of voltages of the p network voltage drivers,

$\underline{J}_D$ is the q-vector of currents of the q network current drivers,

and

$\underline{G}_P$, $\underline{G}_D$, and $\underline{D}_D$ are coefficient matrices of dimension n by n, n by p, and n by q, respectively.

The network models sought are based upon a Lagrangian tree--all of the branches of the modeling tree are incident to a common node. Thus the terms ports and port nodes are used synonymously to identify the nodes, other than the common node, of the modeling tree.

The commonly used terms of linear graph theory are used as defined by Seshu and Reed (7) and will not be redefined.

A method of obtaining the n-port model of large networks containing only one-port conductance (resistance) elements and driver elements is

presented in the following section. This basic method is then extended in subsequent chapters to networks containing energy storage (capacitance and inductance) elements and multiterminal components.

2.2 The Method of Solution. One step in obtaining an n-port model of a network is the simultaneous solution of a set of equations. The number of equations involved depends, in part, on the size of the network. Consider obtaining the n-port model characteristics $\underline{I}_p = \underline{G}_p \underline{V}_p$ of a network of passive elements with v nodes. The solution is of the nodal analysis form and requires v-1-n equations. Thus it is desirable, if possible, to divide the given large network into several smaller units or subnetworks and form the desired model from the subnetwork models.

Consider a large electrical network composed of one-port conductance elements and voltage and current drivers. Assume the network has a total of v nodes, among which are the n port nodes and the common node of the desired Lagrangian model. Divide or partition the network into disjoint subnetworks by placing arbitrary (with one restriction given below) groups of elements into each subnetwork such that only some of the v nodes are contained in more than one subnetwork. Define as subnetwork-port nodes, subport nodes, or simply subports those nodes which either belong to the set of n port nodes of the given network or are nodes which are common to two or more subnetworks (other than the common node); define the total number of subport nodes as m. In each subnetwork add subport voltage drivers between each subport and the reference or common node of the subnetwork model--the common node of the desired n-port model.

The constraint imposed upon the network division is that no

subnetwork may contain a circuit of subport and network voltage driver elements. If this restriction is observed, an n_i-subport model of the form

$$\underline{I}_{SP_i} = [\underline{G1}_i \ \underline{G2}_i] \begin{bmatrix} \underline{E}_{SP_i} \\ \underline{E}_{D_i} \end{bmatrix} + \underline{D}_i \ \underline{J}_{D_i} \qquad (2.2.1)$$

may be formulated for each of the subnetworks (refer to Chapter III) where

$\underline{I}_{SP_i}$ is the n_i-vector of currents of the n_i subport voltage drivers,

$\underline{E}_{SP_i}$ is the n_i-vector of voltages of the n_i subport voltage drivers,

$\underline{E}_{D_i}$ is the p_i-vector of voltages of the p_i subnetwork voltage drivers, a subset of the p-network voltage drivers,

$\underline{J}_i$ is the q_i-vector of currents of the q_i subnetwork current drivers, a subset of the q network current drivers,

and

$\underline{G1}_i$, $\underline{G2}_i$, and $\underline{D}_i$ are the coefficient matrices of dimension $n_i \times n_i$, $n_i \times p_i$, and $n_i \times q_i$, respectively.

This form of the subport model characteristics, where the vector $\underline{I}_{SP_i}$ is explicit in terms of the subport voltage driver, network voltage driver, and network current driver independent variables, is similar to the form sought for the given network n-port model (Equation 2.1.1). Again, each subnetwork model is based upon a Lagrangian tree.

The models of the subnetworks can be combined to form a composite m-subport model of the original network. The common node of each subnetwork model tree has been defined as, common to all subnetworks,

the common node of the desired model tree of the given large network. Thus the trees representing the individual subnetworks can be combined to form a composite Lagrangian tree for an m-subport model of the given network. Tree elements having common subport nodes represent subport voltage drivers of identical voltages; thus these paralleled elements of the composite model may be represented by a single element which represents the voltage of the subport drivers and the sum of the currents of the paralleled subport drivers.

The equations which characterize the composite m-subport model are formed by placing the elements of the individual subnetwork matrices $\underline{G1}_i$, $\underline{G2}_i$, and $\underline{D}_i$ in the appropriate element locations of the composite $\underline{G1}$, $\underline{G2}$, and $\underline{D}$ matrices, respectively. The composite matrix equation is

$$\underline{I}_{SP} = [\underline{G1}\ \underline{G2}] \begin{bmatrix} \underline{E}_{SP} \\ \underline{E}_D \end{bmatrix} + \underline{D}\ \underline{J}_D \qquad (2.2.2)$$

where

$\underline{I}_{SP}$ is the m-vector of all subport voltage driver currents,

$\underline{E}_{SP}$ is the m-vector of all subport voltage driver voltages,

$\underline{E}_D$ is the p-vector of all network voltage driver voltages,

$\underline{J}_D$ is the q-vector of all network current driver currents,

and

$\underline{G1}$, $\underline{G2}$, and $\underline{D}$ are coefficient matrices of the composite model.

Since the composite tree model is formed by paralleling certain subnetwork tree elements, certain of the elements of the composite $\underline{G1}$ matrix are sums of elements of the subnetwork $\underline{G1}_i$ matrices. The individual elements summed are conductances of the paralleled subnetwork

elements that are coefficients of the same subport voltage drivers. This is similar to the paralleling of n-port networks represented by indefinite admittance matrices discussed by Weinberg (8) on pages 52-53. An example follows which illustrates the forming of the composite model.

Consider the network shown in Figure 2.2.1(a). The network is divided into two subnetworks as shown in Figure 2.2.1(b) with appropriate subport voltage drivers added in the subnetworks. The Lagrangian trees which represent the two subnetworks are shown in Figure 2.2.1(c). The subnetwork models are characterized by

$$\begin{bmatrix} I_1^{(1)} \\ I_2^{(1)} \\ I_3^{(1)} \end{bmatrix} = \begin{bmatrix} g_{11}^{(1)} & g_{12}^{(1)} & g_{13}^{(1)} & g_{14}^{(1)} \\ g_{21}^{(1)} & g_{22}^{(1)} & g_{23}^{(1)} & g_{24}^{(1)} \\ g_{31}^{(1)} & g_{32}^{(1)} & g_{33}^{(1)} & g_{34}^{(1)} \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \\ E_5 \end{bmatrix} + \begin{bmatrix} d_{11}^{(1)} & d_{12}^{(1)} \\ d_{21}^{(1)} & d_{22}^{(1)} \\ d_{31}^{(1)} & d_{32}^{(1)} \end{bmatrix} \begin{bmatrix} J_1 \\ J_2 \end{bmatrix} \tag{2.2.3a}$$

and

$$\begin{bmatrix} I_2^{(2)} \\ I_3^{(2)} \\ I_4^{(2)} \end{bmatrix} = \begin{bmatrix} g_{11}^{(2)} & g_{12}^{(2)} & g_{13}^{(2)} & g_{14}^{(2)} \\ g_{21}^{(2)} & g_{22}^{(2)} & g_{23}^{(2)} & g_{24}^{(2)} \\ g_{31}^{(2)} & g_{32}^{(2)} & g_{33}^{(2)} & g_{34}^{(2)} \end{bmatrix} \begin{bmatrix} E_2 \\ E_3 \\ E_4 \\ E_6 \end{bmatrix} + \begin{bmatrix} d_{11}^{(2)} \\ d_{21}^{(2)} \\ d_{31}^{(2)} \end{bmatrix} \begin{bmatrix} J_3 \end{bmatrix} \tag{2.2.3b}$$

The superscripts indicate the subnetwork to which the equation elements belong. There are four subports, the two ports specified for the given

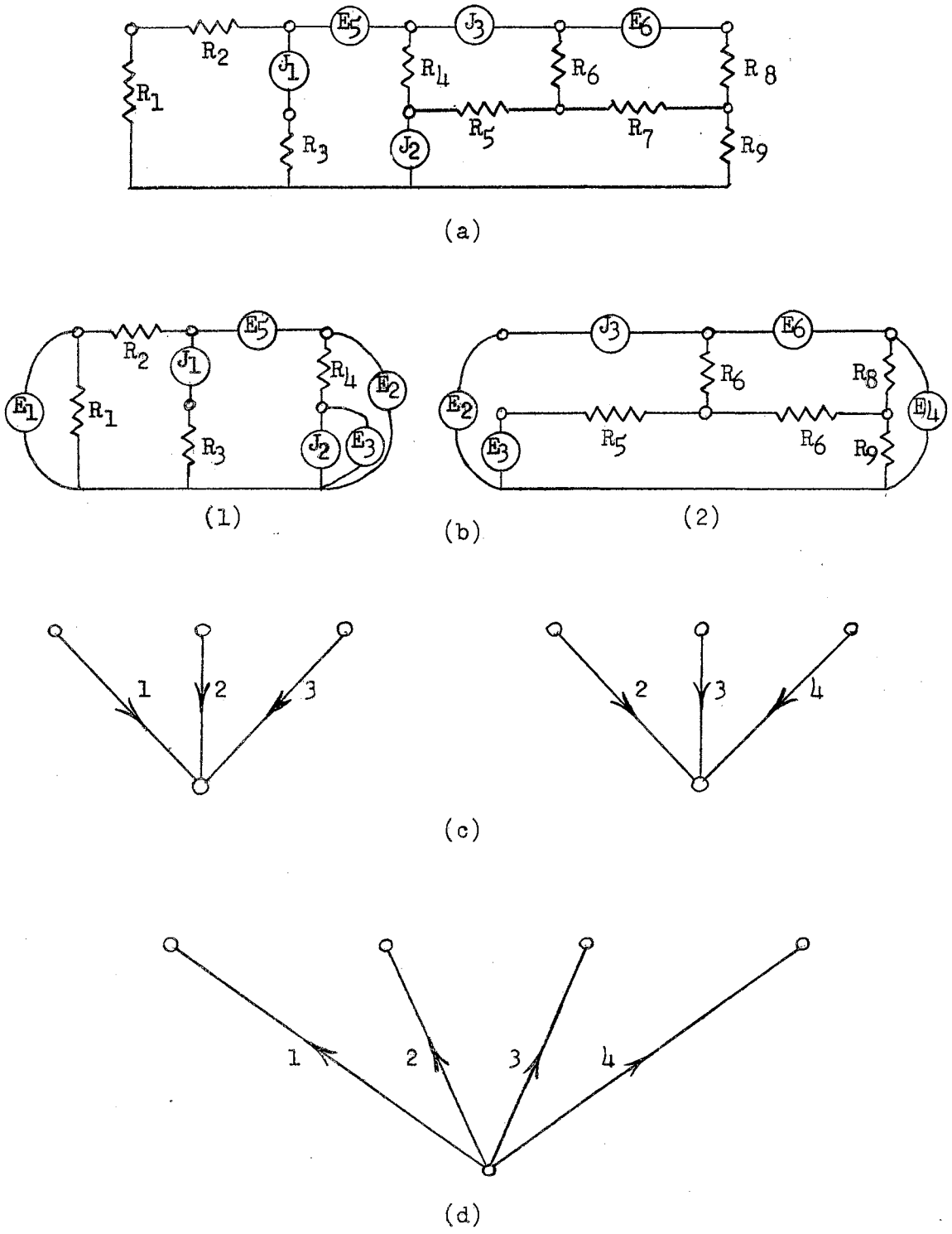


Figure 2.2.1. Example Network. (a) Given network. (b) Two subnetworks of given network. (c) Modeling trees for the two subnetworks. (d) Composite model tree.

network and the two corresponding to the two nodes common to both subnetworks. The composite network model tree is shown in Figure 2.2.1(d). The composite equations characterizing this four-subport model are:

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} I_1^{(1)} \\ I_2^{(1)} + I_2^{(2)} \\ I_3^{(1)} \quad I_3^{(2)} \\ I_4^{(2)} \end{bmatrix} = \begin{bmatrix} g_{11}^{(1)} & g_{12}^{(1)} & g_{13}^{(1)} & 0 & g_{14}^{(1)} & 0 \\ g_{21}^{(1)} & g_{22}^{(1)}+g_{11}^{(2)} & g_{23}^{(1)}+g_{12}^{(2)} & g_{13}^{(2)} & g_{24}^{(1)} & g_{14}^{(2)} \\ g_{31}^{(1)} & g_{32}^{(1)}+g_{21}^{(2)} & g_{33}^{(1)}+g_{22}^{(2)} & g_{23}^{(2)} & g_{34}^{(1)} & g_{24}^{(2)} \\ 0 & g_{31}^{(2)} & g_{32}^{(2)} & g_{33}^{(2)} & 0 & g_{34}^{(2)} \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \\ E_4 \\ E_5 \\ E_6 \end{bmatrix}$$

$$+ \begin{bmatrix} d_{11}^{(1)} & d_{12}^{(1)} & 0 \\ d_{21}^{(1)} & d_{22}^{(1)} & d_{11}^{(2)} \\ d_{31}^{(1)} & d_{32}^{(1)} & d_{12}^{(2)} \\ 0 & 0 & d_{13}^{(2)} \end{bmatrix} \begin{bmatrix} J_1 \\ J_2 \\ J_3 \end{bmatrix} \qquad (2.2.4)$$

Here the superscripts indicate from which subnetwork the composite equation elements originate.

The desired n-port model for the given network can be derived from the m-subport composite model. This is accomplished in a manner analogous to that described by Weinberg (8) for reducing an n-terminal network to a network with fewer terminals and determining a new indefinite admittance matrix for the network. The vector of currents

of the subports, which are not ports of the network, is set equal to zero; and the corresponding subport voltage vector is solved as a function of the voltage vector of the port drivers and the voltage and current vectors of the network drivers of the given network. If the m-subport model is formed so that the first n rows correspond to the n ports of the given network, the composite matrix equation, Equation 2.2.2, can be partitioned

$$\begin{bmatrix} \underline{I}_{PSP} \\ \underline{I}_{RSP} \end{bmatrix} = \begin{bmatrix} \underline{G}_{11} & \underline{G}_{12} & \underline{G}_{13} \\ \underline{G}_{21} & \underline{G}_{22} & \underline{G}_{23} \end{bmatrix} \begin{bmatrix} \underline{E}_{PSP} \\ \underline{E}_{RSP} \\ \underline{E}_{D} \end{bmatrix} + \begin{bmatrix} \underline{D}_1 \\ \underline{D}_2 \end{bmatrix} \underline{J}_D \qquad (2.2.5)$$

where $\underline{I}_{PSP}$ and $\underline{E}_{PSP}$ are the n-vectors of currents and voltages of the n-port drivers of the given network and $\underline{I}_{RSP}$ and $\underline{E}_{RSP}$ are the (m-n)-vectors of currents and voltages of the remaining subports. It follows then, that if $\underline{I}_{RSP}$ is made equal to zero, the vector $\underline{E}_{RSP}$ is

$$\underline{E}_{RSP} = - [\underline{G}_{22}]^{-1} [\underline{G}_{21} \underline{E}_{PSP} + \underline{G}_{23} \underline{E}_{D} + \underline{D}_2 \underline{J}_D] \qquad (2.2.6)$$

Substituting Equation 2.2.6 into Equation 2.2.5 results in the desired n-port model

$$\underline{I}_{PSP} = [\underline{G}_{11} - \underline{G}_{12} \underline{G}_{22}^{-1} \underline{G}_{21}] \underline{E}_{PSP} + [\underline{G}_{13} - \underline{G}_{12} \underline{G}_{22}^{-1} \underline{G}_{23}] \underline{E}_{D} + [\underline{D}_1 - \underline{G}_{12} \underline{G}_{22}^{-1} \underline{D}_2] \underline{J}_D \qquad (2.2.7)$$

which is of the form of Equation 2.2.1 where

$\underline{I}_P$ is equal to $\underline{I}_{PSP}$,

$\underline{V}_P$ is equal to $-\underline{E}_{PSP}$,

$\underline{G}_P$ is equal to $\underline{G}_{11} - \underline{G}_{12} \underline{G}_{22}^{-1} \underline{G}_{21}$,

$\underline{G}_D$ is equal to $\underline{G}_{13} - \underline{G}_{12}\,\underline{G}_{22}^{-1}\,\underline{G}_{23}$,

and

$\underline{D}_D$ is equal to $\underline{D}_1 - \underline{G}_{12}\,\underline{G}_{22}^{-1}\,\underline{D}_2$.

Network analysis requires: (1) that the mathematical relationships relating the variables (current and voltage for the electrical network) of each element be known, and (2) the existence of a means of specifying the network topology or the interconnections of the network elements. By specifying the element type and the element "value," the first requirement is satisfied. If the elements and nodes of the network are numbered, an array of numbers may be used for specifying the network topology. The algorithms and the analysis procedures developed and used in this study require only this basic network information.

2.3 The Network Division Algorithm. In addition to the theoretical constraint given in Section 2.2, a second constraint must be imposed on the network division process for practical reasons--the size of the computer memory limits the size of the subnetworks for which model characteristics are to be computed. Thus the number of elements in each subnetwork tree and each subnetwork cotree is limited by some maximum number. Subnetwork tree and cotree sizes can be calculated without knowning the specific elements which belong to either set. The number of tree elements is equal to the number of nodes of the subnetwork minus one; the number of cotree elements is equal to the total number of subnetwork elements minus the number of elements in the tree.

A third constraint in dividing a given network may be imposed if, for some reason, subnetworks of maximum size are not desired. Computation round-off errors may be checked by forming an n-port model two or more

times from different network divisions. Also, as is done in Chapters IV and V, a small network may be divided into small subnetworks in order to illustrate the process without requiring the use of large example networks. In either case, a subnetwork of minimum size may be specified, and the network division algorithm described below will add network elements to the subnetworks (form the subnetworks) until the minimum size is reached or exceeded.

The network division algorithm is developed around the above constraints. The following terms are specifically defined for the purpose of defining the algorithm. Attention is called to Section 2.1 for the meaning of the term port or port node. It should also be noted that the word network will be used exclusively to mean the given network, without port drivers, for which the n-port model is desired.

Definition 2.3.1. Subnetwork. In general the term subnetwork means any subset of elements of a given network. For the purpose of this thesis a subnetwork is defined as any one of the disjoint subsets of elements resulting from a dividing or partitioning of a given network such that:

(a) the union of all subnetworks is equal to the given network,

(b) the intersection of any pair of subnetworks is the null set,

(c) there exists no path made up exclusively of voltage driver elements between any pair of subports or any subport and the common node (reference Sections 2.2.1 and 2.2.2), and

(d) the size of the subnetwork does not exceed a prescribed maximum (reference Section 2.2.2).

Definition 2.3.2. Reference or common node. The node of the given

network which is selected as the common node of the desired n-port Lagrangian tree model is defined as the reference or common node. This node is further defined as the common node of all subnetwork models.

Definition 2.2.3. Subport. A subport is defined as a node of a subnetwork which either belongs to the set of the n port nodes of the given network or is a node, other than the common node, which appears in both a subnetwork and its complement.

Definition 2.3.4. x-node. An x-node is a node of the network, or of a subnetwork, that is connected to a port, subport, or to the common node by a path made up exclusively of network voltage drivers.

Definition 2.3.5. Interior node. An interior node is defined as a node which appears in only one subnetwork.

An interior node is thus a node of a subnetwork such that all elements incident to it in the network are incident to it in the subnetwork.

Definition 2.3.6. Subport driver. Subport drivers are the voltage drivers added to a subnetwork, between each subport and the common node, in order to establish the subport model of the subnetwork (refer to Chapter 6 of Koenig and Blackwell (1)).

Definition 2.3.7. Augmented subnetwork. An augmented subnetwork is defined as a subnetwork and its added subport drivers.

Each subnetwork is formed by selecting certain nodes, one at a time, to be made interior nodes of the subnetwork; that is, all of the elements incident to each selected node are placed into the subnetwork.

A node is said to be associated with a subnetwork after any element incident to the node has been placed into a subnetwork in the network division process. The steps of the network division algorithm follow.

1. Determine whether any network nodes are x-nodes. That is, determine those nodes which are connected to a network port or to the reference node by a path made up exclusively of network voltage drivers.
2. Select a node to be made an interior node of a subnetwork:
   (a) select a node from the list of x-nodes, or if no x-nodes exist,
   (b) select a node not associated with a subnetwork, or if all nodes are associated with subnetworks,
   (c) select a node which has elements remaining incident to it in the network.
3. Remove from the elements remaining in the network the elements incident to the selected node and
   (a) place the elements into the subnetwork, and
   (b) if any of these elements are network voltage drivers or network current drivers, add them to the appropriate list--voltage drivers to the branch list, the list of elements which comprise the tree of the subnetwork linear graph, and current drivers to the chord list, the list of elements which comprise the cotree of the subnetwork linear graph.

   Determine the other nodes to which these elements are incident and list the nodes; denote these nodes as k-nodes.
4. If network voltage driver elements which remain in the given network are incident to any node listed in the k-node list,

determine the other nodes to which these elements are incident and list these nodes in the x-node list. (These nodes are listed as x-nodes because the k-nodes may become subports.)

5. If a node of the k-node list appears in the x-node list, use this node as the next selected node to make an interior node of the subnetwork and return to Step 3. If no x-nodes are in the k-node list, go to Step 6.

6. Determine the number of branches and the number of chords there would be in the subnetwork if the subnetwork were completed by adding subport driver elements. If both are less than the minimums required, go to Step 7; if both are less than the maximum and one is larger than the minimum, go to Step 9; if either is larger than the maximum number allowed, go to Step 8.

7. Select a new node to be made an interior node of the subnetwork (a or b below) and go to Step 3:

   (a) Select a node from the k-node list which has elements remaining incident to it in the given network, or if no such k-node exists,

   (b) select any node which has elements remaining incident to it in the given network, or if no such network exists,

   (c) do not select a new node; go to Step 9.

8. Return all elements to the given network which were placed into the subnetwork since the previous size determination (Step 6) was made on the subnetwork. Also remove these elements from the branch and chord lists if they occur in the lists. Go to Step 9.

9. Add subport driver elements to the subnetwork to form the

augmented subnetwork. Each subport driver element is assigned a number which is equal to the number assigned to the subport (node) increased by the total number of elements in the given network.

10. If elements remain in the given network, return to Step 2 and start a new subnetwork. If no elements remain in the network, the process is completed.

This algorithm is the basis of the network division phases of the computer programs presented in Chapters IV and V. The algorithm will divide any given network of resistors, voltage drivers and current drivers, which has no circuits of voltage driver elements (including the port drivers of the n-ports) and no cutsets of current drivers, into subnetworks of the same class--no circuits of voltage drivers and no cutsets of current drivers--if such a division of the network is at all possible within the maximum size subnetwork constraints imposed. A test is given in the following section which may be applied to a given network to determine if the network can be divided into subnetworks of specified maximum size.

2.4 An Algorithm to Determine if a Network Can be Divided. It may not be possible to divide a given network into subnetworks of a given maximum number of branches and chords because of the manner in which a number of network voltage drivers are located in the network topology. This may or may not be determined by a superficial inspection of the network. However, a detailed manual procedure is available which tests a given network to determine if sufficient conditions exist in the network so that it can be divided. The steps of the procedure are:

1. Identify each set of nodes which is connected by one or more network voltage driver elements.

2. For each group containing a network port node, perform the following steps:

   (a) Count the number of nodes, n, excluding the port node.

   (b) Count the number of nodes, m, which are connected by network current driver or conductance elements to the n-nodes.

   (c) Sum b = n + m + 1.

   (d) Count the number of current driver and conductance elements, c, which connect n-nodes to m-nodes and n-nodes to other n-nodes of the same group.

3. For each group not containing a port node, perform the following steps:

   (a) Select the node (or one of the nodes) whose incident network current driver and conductance elements connect to the minimum number of nodes.

   (b) Consider this node as a port node and perform the steps 2(a) through 2(d).

4. For those groups of nodes which are connected by a single current driver or conductance element from a node of one group to a node of another group, determine the following:

   (a) $B = \sum_{i=1}^{N} b_i$; N groups so connected.

   (b) $C = N - 1 + \sum_{i=1}^{N} c_i$.

5. If all b's and B's are less than or equal to the maximum

number of branches allowed in a subnetwork and all $c^{\prime}s$ and $C^{\prime}s$ are less than or equal to the maximum number of chords allowed in a subnetwork, the network can be divided by the network division algorithm.

CHAPTER III

SUBNETWORK MODELING

3.1 Introduction. The formulation of the subnetwork models as defined in Chapter II by Equation 2.2.1 is accomplished by the application of linear graph theory as developed by Koenig and Blackwell (1). A formulation tree and its complement, the cotree, are formed for each augmented subnetwork. From the tree and cotree, the fundamental cutset matrix (or the fundamental circuit matrix) must be formed. The cutset matrix is used for reasons stated later. With the cutset matrix determined and the values of the augmented subnetwork branch and chord conductances known, the desired subnetwork model is formulated.

The tree-cotree algorithm is presented in Section 3.2, the algorithm for forming the cutset matrix is presented in Section 3.3, and the formulation of the subnetwork model is detailed in Section 3.4.

3.2 The Tree Formation Algorithm. Cummins and Thomason (9) developed a computer program based upon an algorithm by Minty (10) which lists all of the trees of a linear graph. The algorithm developed in this section is based upon the work of these authors, but it is different in that only one tree of the network is determined. Also, the algorithm developed here produces a tree which contains certain specified elements of the augmented subnetwork, and a tree complement or cotree, which contains other specified elements of the augmented

subnetwork--those elements determined to belong in the tree and cotree by the network division algorithm. This is necessary since all voltage driver elements must be in the tree and all current driver elements must be in the cotree in order to perform the required linear graph theory analysis.

The steps of the algorithm are:

1. Remove the elements from the augmented subnetwork which are contained in the subnetwork chord list created by the network division algorithm.
2. Select an element of the subnetwork branch list obtained by the network division algorithm.
3. Locate the nodes to which the selected branch element is incident in the augmented subnetwork. Remove the branch from the subnetwork and join together or identify the two nodes as one single node.
4. Remove from the subnetwork any self loop elements--elements with both ends incident at the same node--which are generated by the identification of two nodes in Step 3. Add these elements to the subnetwork chord list.
5. Return to Step 2 until all elements of the branch list, listed by the network division algorithm, have been selected and removed from the subnetwork.
6. If elements remain in the subnetwork, choose any element as a branch. Add the element to the subnetwork branch list and go to Step 3. If no elements remain in the subnetwork, the subnetwork tree and cotree are defined by the branch and chord lists, respectively.

3.3 The Cutset Matrix Formation Algorithm. An algorithm has been developed to form the fundamental circuit matrix (2). The development of the algorithm to form the fundamental cutset matrix is due to an attempt to simplify the obtaining of one matrix or the other. Either matrix may be used with equal facility in the subnetwork model formulation; however, the cutset matrix algorithm developed requires somewhat less input information than the earlier developed circuit matrix algorithm, based upon the computer program realization of both. The steps of the algorithm follow from the definitions of the cutset matrix and fundamental cutsets (7).

1. Create a matrix of zeros with as many rows as the number of entries in the subnetwork branch list and as many columns as the number of entries in the subnetwork chord list. Select the first entry in the branch list as the first cutset branch.
2. Determine one of the nodes to which the cutset branch is incident in the augmented subnetwork and determine if the branch is oriented away from the node.
3. List the node in the node list. List all the elements incident to the node, except the branch, in the cutset list.
4. If any elements of the cutset list are branch elements, select one and remove it from the cutset list. Determine the other node to which it is incident and go to Step 3.
5. When there are no branch elements in or remaining in the cutset list, remove both entries of all those elements which appear twice in the cutset list.
6. The cutset list formed is the list of cutset chords corresponding to the initially selected cutset branch. Select

the first chord in this list.

7. Determine if the selected chord is oriented away from any of the nodes in the node list.

8. If the orientation of the cutset branch (Step 2) and the orientation of the chord (Step 7) are both away from or both toward any of the nodes in the node list, the cutset matrix entry corresponding to the branch and chord is +1; if either the branch or chord orientation is away from and the other is toward any of the nodes in the node list, the entry is -1.

9. Place the entry determined in Step 8 in the matrix row corresponding to the cutset branch position in the subnetwork branch list and in the matrix column corresponding to the position in which the chord is located in the subnetwork chord list.

10. Select the next chord in the cutset list and go to Step 7. When all chords have been selected, go to Step 11.

11. Remove all entries from the node and cutset lists. Select the next branch in the branch list for the next cutset branch and go to Step 2. When all branches have been selected, the cutset matrix submatrix $\underline{S}$ is completed.

The complete cutset matrix representation is $[\underline{U}\ \underline{S}]$, where $\underline{U}$ is a unit matrix.

3.4 Subnetwork Modeling. The subnetwork model is computed from the cutset submatrix, $\underline{S}$, and the component values of the tree and cotree conductances. The matrix $\underline{S}$ is partitioned and provides both the fundamental cutset and fundamental circuit equations:

$$\begin{bmatrix} \underline{I}_{VD} \\ \underline{I}_{TG} \end{bmatrix} = - \begin{bmatrix} \underline{S}_{11} & \underline{S}_{12} \\ \underline{S}_{21} & \underline{S}_{22} \end{bmatrix} \begin{bmatrix} \underline{J}_{CD} \\ \underline{I}_{CG} \end{bmatrix} \qquad (3.4.1)$$

$$\begin{bmatrix} \underline{V}_{CD} \\ \underline{V}_{CG} \end{bmatrix} = \begin{bmatrix} \underline{S}_{11}^{T} & \underline{S}_{21}^{T} \\ \underline{S}_{12}^{T} & \underline{S}_{22}^{T} \end{bmatrix} \begin{bmatrix} \underline{E}_{VD} \\ \underline{V}_{TG} \end{bmatrix} \qquad (3.4.2)$$

where

$\underline{I}_{VD}$ and $\underline{E}_{VD}$ are the current and voltage vectors of the voltage drivers,

$\underline{J}_{CD}$ and $\underline{V}_{CD}$ are the current and voltage vectors of the current drivers,

$\underline{I}_{TG}$ and $\underline{V}_{TG}$ are the current and voltage vectors of the tree conductances, and

$\underline{I}_{CG}$ and $\underline{V}_{CG}$ are the current and voltage vectors of the cotree conductances.

The tree and cotree conductances provide two additional equations, the component equations

$$\underline{I}_{CG} = \underline{G}_{C} \underline{V}_{CG} \qquad (3.4.3)$$

and

$$\underline{I}_{TG} = \underline{G}_{T} \underline{V}_{TG} \qquad (3.4.4)$$

where $\underline{G}_{T}$ and $\underline{G}_{C}$ are diagonal matrices, the elements of which are the values in mhos of the tree and cotree conductances. The conductances are ordered in the same order as the corresponding elements are listed in the tree and cotree lists; thus the current and voltage vectors of Equations 3.4.3 and 3.4.4 are the same as those in Equations 3.4.1

and 3.4.2.

The subnetwork models are formulated as follows: From Equations 3.4.1 and 3.4.2 the following equations are written:

$$\underline{V}_{CG} = \underline{S}_{12}^{T} \underline{E}_{VD} + \underline{S}_{22}^{T} \underline{V}_{TG} \qquad (3.4.5)$$

$$\underline{I}_{VD} = - \underline{S}_{11} \underline{J}_{CD} - \underline{S}_{12} \underline{I}_{CG} \qquad (3.4.6)$$

Equation 3.4.5 is substituted into Equation 3.4.3 and the result substituted into Equation 3.4.6, resulting in an expression for $\underline{I}_{VD}$ in terms of driver current and voltage vectors and $\underline{V}_{TG}$:

$$\underline{I}_{VD} = - \underline{S}_{11} \underline{J}_{CD} - \underline{S}_{12} \underline{G}_{C} [\underline{S}_{12}^{T} \underline{E}_{VD} + \underline{S}_{22}^{T} \underline{V}_{TG}] \qquad (3.4.7)$$

Equation 3.4.1 also provides

$$\underline{I}_{TG} = - \underline{S}_{21} \underline{J}_{CD} - \underline{S}_{22} \underline{I}_{CG} \qquad (3.4.8)$$

Equations 3.4.4 and 3.4.3 are substituted into Equation 3.4.8. Equation 3.4.5 is substituted into the result. The following equation, containing the same variables as Equation 3.4.7, results:

$$\underline{G}_{T} \underline{V}_{TG} = - \underline{S}_{21} \underline{J}_{CD} - \underline{S}_{22} \underline{G}_{C} [\underline{S}_{12}^{T} \underline{E}_{VD} + \underline{S}_{22}^{T} \underline{V}_{TG}] \qquad (3.4.9)$$

Equation 3.4.9 is solved for $\underline{V}_{TG}$:

$$\underline{V}_{TG} = [\underline{G}_{T} + \underline{S}_{22} \underline{G}_{C} \underline{S}_{22}^{T}]^{-1} [- \underline{S}_{21} \underline{J}_{CD} - \underline{S}_{22} \underline{G}_{C} \underline{S}_{12}^{T} \underline{E}_{VD}] \qquad (3.4.10)$$

Equation 3.4.10 is substituted into Equation 3.4.7 to provide the expression for $\underline{I}_{VD}$, the vector of currents of all subnetwork voltage driver elements, in terms of the voltage vector of these driver elements and the current vector of the subnetwork current drivers. The result is

$$\underline{I}_{VD} = \underline{G}_{VD}\,\underline{E}_{VD} + \underline{D}_{VD}\,\underline{J}_{CD} \qquad (3.4.11)$$

where

$$\underline{G}_{VD} = \underline{S}_{12}\,\underline{G}_C\,\underline{S}_{22}^{T}\,[\underline{G}_T + \underline{S}_{22}\,\underline{G}_C\,\underline{S}_{22}^{T}]^{-1}\,\underline{S}_{22}\,\underline{G}_C\,\underline{S}_{12}^{T} - \underline{S}_{12}^{T} \qquad (3.4.12)$$

and

$$\underline{D}_{VD} = \underline{S}_{12}\,\underline{G}_C\,\underline{S}_{22}^{T}\,[\underline{G}_T + \underline{S}_{22}\,\underline{G}_C\,\underline{S}_{22}^{T}]^{-1}\,\underline{S}_{21} - \underline{S}_{11} \qquad (3.4.13)$$

Since only the representation of subport currents is desired, those equations expressing network voltage driver currents can be eliminated from Equation 3.4.11 to form the subnetwork subport model equivalent to Equation 2.2.1,

$$\underline{I}_{SP} = \underline{G}_{SP}\,\underline{E}_{VD} + \underline{D}_{SP}\,\underline{J}_{CD} \qquad (3.4.14)$$

where

$\underline{I}_{SP}$ is the vector of currents of the subport voltage drivers, a subset of the currents of the vector $\underline{I}_{VD}$ defined in Equation 3.4.1;

$\underline{E}_{VD}$ and $\underline{J}_{CD}$ are the vectors as defined for Equations 3.4.1 and 3.4.2; and

$\underline{G}_{SP}$ and $\underline{D}_{SP}$ are matrices derived from $\underline{G}_{VD}$ and $\underline{D}_{VD}$ of Equation 3.4.11 by deleting the appropriate rows.

CHAPTER IV

n-PORT MODELING OF NETWORKS COMPOSED OF ONE-PORT AND MULTIPORT RESISTIVE DEVICES AND IDEAL VOLTAGE AND CURRENT DRIVERS

4.1 Introduction. Networks or systems may contain multiport components in addition to one-port elements. The composition of such components need not be known in order to be able to model the characteristics of these devices. Models similar to the subnetwork models formulated in Chapter III can be formulated for individual multiport components. The analysis of networks containing these devices is carried out in a manner quite similar to the analysis of networks which contain only one-port elements.

The theory presented in the previous chapters is extended in this chapter to include systems containing components with more than one port. These components are considered as individual subnetworks of the given network in which they are connected and for which the n-port model is sought. Section 4.2 presents the manner in which suitable models of multiport components are determined so that these models can be added to the composite subport model discussed in Chapter II. The remainder of this chapter presents the computer program in detail, beginning with a discussion of the input data to the program and concluding with an example.

4.2 Multiport Component Modeling. Multiport components can be mathematically modeled by a terminal tree-graph and an associated set of terminal equations (1). It is assumed that the tree graphs which represent the components to be considered are of arbitrary form and that the terminal equations are of the form

$$\underline{I} = \underline{G}\,\underline{V} \qquad (4.2.1)$$

where $\underline{I}$ and $\underline{V}$ are the current and voltage vectors of the modeling tree elements and $\underline{G}$ is a matrix of short-circuit conductance parameters.

Subport models similar to those formulated for the subnetworks of one-port elements are formulated for multiport components from the given models. These subport models are formulated by considering each multiport component as an individual subnetwork. The augmented subnetwork in this case is defined as the multiport component plus the voltage drivers, both subport drivers and any necessary network voltage drivers, which are required to define the voltages of all of the terminals of the multiport component. This augmented multiterminal component subnetwork will hereafter be referred to as an m-c subnetwork.

The simplest subport model of a multiport component is a Lagrangian tree model with a subport branch element connecting the common node to each terminal of the component. Such a model can be obtained by a simple tree transformation of variables (1). However, this model will not always be feasible. Consider the case of a multiport component which has terminals that are connected to network nodes which are x-nodes or become defined as x-nodes by the division process. The voltages of each of these terminals is a function of both a subport driver and one or more network voltage drivers. Thus the models which

are to represent these components will contain both subport drivers and network drivers, and their linear graph models will contain tree branches in series.

The multiport component models are formulated by linear graph theory in a similar manner as was done in formulating the models in Chapter III. The cutset coefficient matrix $\underline{S}$ of the graph of each m-c subnetwork is required. The tree of this graph is formed by the subport and network voltage driver elements. The cotree is formed by the elements of the given model tree-graph.

Because of the characteristics of the linear graphs which represent m-c subnetworks, the cutset matrix $\underline{S}$ can be formed by a unique algorithm. It is assumed that the n-1 chord elements, the elements of the component terminal model tree graph, are numbered 1, 2, ..., n-1 and that the branch elements are labeled. The steps of the algorithm follow:

1. Select any terminal of the multiterminal component.
2. Create a vector $\underline{R}$ with n-1 emements by determining which of the n-1 chord elements are incident at the selected terminal. If element j is incident and oriented toward the terminal, $R_j = 1$, if oriented away from the terminal, $R_j = -1$. If element j is not incident at the terminal, $R_j = 0$.
3. Determine the path of tree elements which connect the selected terminal to the common or reference node. Determine the orientation of each element with respect to the path.
4. For each branch determined in Step 3, add a row to the $\underline{S}$ matrix; if the branch is oriented toward the component terminal node, the row added is the vector $\underline{R}$; if the branch

is oriented away from the component terminal, the row added is the vector $-\underline{R}$.

5. If all component terminals have not been selected, select one and return to Step 2. If all terminals have been selected, the matrix $\underline{S}$ is complete.

The subport model of a multiport component is now formulated. There are no tree conductance elements and no chord current driver elements in the m-c subnetwork; thus the cutset equations and the circuit equations are

$$\underline{I}_{VD} = - \underline{S}\, \underline{I}_{CG} \tag{4.2.2}$$

$$\underline{V}_{CG} = \underline{S}^T \underline{E}_{VD} \tag{4.2.3}$$

where the variables are the same as defined for Equations 3.4.1 and 3.4.2. The component equation

$$\underline{I}_{CG} = \underline{G}_C \underline{V}_{CG} \tag{4.2.4}$$

is the same as Equation 4.2.1, and $\underline{G}_C = \underline{G}$, the given short-circuit conductance matrix of the component. The three equations combine to formulate the model

$$\underline{I}_{VD} = \underline{G}_{VD} \underline{E}_{VD} \tag{4.2.5}$$

where

$$\underline{G}_{VD} = - \underline{S}\, \underline{G}\, \underline{S}^T \tag{4.2.6}$$

Equation 4.2.5, like Equation 3.4.12, gives the currents of all voltage drivers of the subnetwork. The subport model can be determined

by omitting the rows of the matrix Equation 4.2.5 which correspond to network voltage driver currents. The subport model is

$$\underline{I}_{SP} = \underline{G}_{SP}\, \underline{E}_{VD} \qquad (4.2.7)$$

where

$\underline{I}_{SP}$ is the vector of currents of the m-c subnetwork subport drivers, a subset of the currents of $\underline{I}_{VD}$,

$\underline{E}_{VD}$ is the vector as defined in Equation 3.4.2, and

$\underline{G}_{SP}$ is the matrix derived by deleting the rows from $\underline{G}_{VD}$ which lie in the same relative positions as the network voltage driver currents.

4.3 The Computer Program. A program, designated Program I, has been written which produces the coefficient matrices of the n-port models of large networks containing resistive one-port and multiport components, and current and voltage drivers. The program will produce a one- to five-port Lagrangian representation, as specified, of a network with up to forty nodes, with a maximum of ten elements incident at any node, 100 conductances, twenty voltage drivers, twenty current drivers, and any number of multiport components. Each multiport component may be a three-, four- or five-terminal component. The program is written in FORTRAN IV language for execution on the IBM 1410 computer. The length of the program requires that it be written in six phases or parts. The phases are executed in order, and data is transferred to succeeding phases by the use of the computer tape units. Five tape units are required. The input is by punched cards, and the output is printed by the computer line printer.

As stated earlier, in Chapter II, one requirement of network analysis is the mathematical description of the network topology. For analysis to be carried out by a computer, the mathematical description must be a numerical description which can be utilized efficiently by the analysis program. Thus the given network linear graph of one-port elements and the given tree-graphs of the multiport components must be converted to numerical descriptions. This is accomplished as follows.

The linear graph of one-port elements is labeled as follows: The v nodes of the graph (including the nodes to which only multiport components connect) are numbered 1, 2, ..., v. The nodes are not required to be numbered in any order; however, the node which is to be the common node of the desired n-port model tree must be numbered last, that is, its number is v. Each element of the graph is numbered 1, 2, ..., e. All conductance elements are numbered first; all current driver elements are numbered second, following the conductances; and the voltage driver elements are numbered last, following the current driver elements. Each of the elements must have an orientation. The orientation of the conductances is arbitrary. The orientation of the network driver elements is made to correspond to the polarities of the drivers they represent; arrows point away from the positive terminal of the voltage driver elements and in the same direction as the current flow in the current driver elements.

Each multiport (n-terminal) component terminal tree-graph is labeled as follows: The elements are numbered 1, 2, ..., n-1 to correspond with the order of the parameters in the short-circuit matrix representing the component--the order of the equations in Equation 4.2.1. Each terminal is numbered with the number of the network node

to which it connects.

Two numerical arrays and a list are now defined. These are obtained directly from the directed graphs labeled as described above and provide the network topology information to the computer program.

Definition 4.3.1. The network connection array NTWKCN. Given a directed graph with v nodes numbered 1, 2, ..., v and e one-port elements numbered 1, 2, ..., e. The network connection array NTWKCN = (a_{ij}) is defined by

a_{ij} = the number from the set 1, 2, ..., e identifying element j incident at node i. $1 \leq j \leq m$, where m elements are incident at node i.

Definition 4.3.2. The direction array DIRECT for multiport component. Given a directed tree-graph with elements numbered 1, 2, ..., n-1 and nodes numbered from the set 1, 2, ..., v, where v is the number of nodes of the network of which the component is a part. The direction array DIRECT = (a_{ij}) is defined by

a_{i1} = the number from the set 1, 2, ..., v identifying the node <u>from</u> which element i is directed,

a_{i2} = the number from the set 1, 2, ..., v identifying the node <u>to</u> which element i is directed.

Definition 4.3.3. The orientation list. Given a directed graph with v nodes numbered 1, 2, ..., v and e elements numbered 1, 2, ..., e. The orientation list ORIENT = (a_i) is defined by

a_i = the number from the set 1, 2, ..., v identifying the node from which element i is directed.

The computer program requires the following input data:

1. General network specifications:
   (a) the number of nodes
   (b) the number of one-port elements
   (c) the number of voltage drivers
   (d) the number of current drivers
   (e) the number of multiport components
   (f) the number of ports, and
   (g) the list of the network port nodes.
2. The terminal tree-graph direction array, DIRECT, and terminal conductance matrix $\underline{G}$ for each multiport component of the network.
3. The network connection array NTWKCN.
4. The orientation list ORIENT.
5. A list of the conductance values in mhos in the order in which the conductance elements are numbered on the network graph.

The following paragraphs describe the sequence of operations of Program I. Flow charts of the program phases are found in Appendix C. A list of definitions of the program FORTRAN variables which appear in the flow charts is found in Appendix B. Some of these variable names appear in the following paragraphs.

Phase 1 of the program performs two operations. First, the data of each multiport component is read, and the following computations are made in turn. The input array DIRECT is used to form a list, MTCTPT, of nodes to which the component terminals are connected in the network. The array DIRECT, the list MTCTPT, and the component matrix $\underline{G}$ are written on tape for use in Phase 2. During this operation, the

list, MTCPLT, of all network nodes to which the components connect, is compiled. The second operation of Phase 1 divides the network of one-port elements (one-port conductances and drivers) into subnetworks. The program, based upon the algorithm presented in Chapter II, computes for each subnetwork the augmented subnetwork connection array SBNWCN, the partial tree list TRESET, and the partial cotree list CRDSET, and writes this information on tape for use in Phase 2. A list of all voltage driver elements, SRBRLT, both network drivers and subport drivers, is compiled during the formation of the subnetworks. This list is compared with the list MTCPLT; any nodes appearing in MTCPLT and not in SRBRLT are added to SRBRLT. SRBRLT and the lists XNDLST, XNDREF, and XNDSRC formed during network division are placed on tape for Phase 2.

Phase 2 performs three operations. The entries of the voltage driver element list SRBRLT are numbered, forming the list LIST that specifies the order in which the voltage driver variables will appear in the composite subnetwork model. The second operation of Phase 2 computes the models for each multiport component in turn. The program based on the algorithm of Section 4.2 uses the lists XNDLST, XNDREF, and XNDSRC, the component array DIRECT and the component port list MTCTPT to compute the component-subnetwork-graph cutset matrix $\underline{S}$ and the voltage source position list SNVSLT. The m-c subnetwork model matrix $\underline{G}_{VD}$ is computed using the $\underline{S}$ matrix and the given component terminal matrix $\underline{G}$. The matrix $\underline{G}_{VD}$ and the list SNVSLT are written on tape for Phase 5. The final operation of Phase 2 is forming, in turn, the tree and cotree for each augmented subnetwork of one-port elements. The program first removes the rows of the subnetwork connection array

which correspond to nodes not in the subnetwork and produces the reduced array SBNWCN and compiles the list, SUBNOD, of nodes of the subnetwork in the order in which they appear in the reduced array. The programmed algorithm of Section 3.2 then completes the lists TRESET and CRDSET, forming the complete augmented subnetwork tree and cotree. The following are written on tape for Phase 3: the reduced array SBNWCN, TRESET, CRDSET, and SUBNOD.

Phase 3 uses the algorithm of Section 3.3 to form the cutset matrix $\underline{S}$. Upon the formation of each subnetwork cutset matrix, the following are computed: the subnetwork voltage driver list SNVSLT, the subnetwork current driver list SNCSLT, the list of conductances of the tree GTREE, and the cotree GCOTRE. The entries of these lists correspond to the positions in which the various elements are located in the cutset equation, Eqution 3.4.1. These lists and the matrix $\underline{S}$ are written on tape for use in Phase 4.

The program of Phase 4 computes the matrices $\underline{G}_{VD}$ and $\underline{D}_{VD}$ defined by Equations 3.4.12 and 3.4.13 for each of the one-port element subnetworks. These matrices and the lists SNVSLT and SNCSLT are written on tape for use in Phases 5 and 6.

Phase 5 forms the composite matrix $[\underline{G1}\ \underline{G2}]$ of Equation 2.2.2 by relocating the elements of the subnetwork $\underline{G}_{VD}$ matrices in accordance with the voltage driver position list SNVSLT of each subnetwork. When the composite matrix is formed, the coefficient matrices $\underline{G}_P$ and $\underline{G}_D$ defined by Equation 2.1.1 are computed and are written on tape to be printed out in Phase 6. Submatrices $\underline{G}_{12}$ and $\underline{G}_{22}^{-1}$ are written on tape for use in computing $\underline{D}_D$ in Phase 6.

Phase 6 forms the composite matrix $\underline{D}$ of Equation 2.2.2 using the

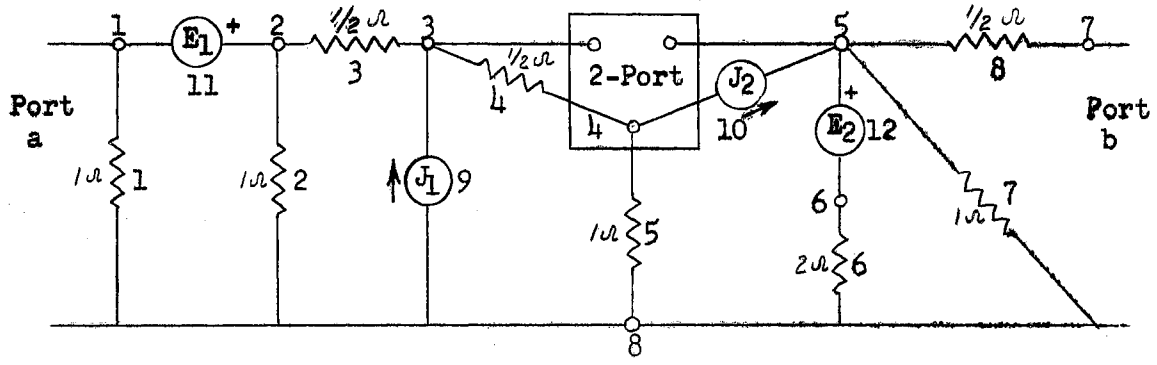
subnetwork lists, SNVSLT and SNCSLT, to properly locate the subnetwork $\underline{D}_{VD}$ matrix elements. The coefficient matrix $\underline{D}_D$ is then computed, and the n-port model matrices $\underline{G}_P$, $\underline{G}_D$, and $\underline{D}_D$ are printed.

4.4 Illustrative Example. The program was used to compute the models of a number of networks. The solution of one network follows:

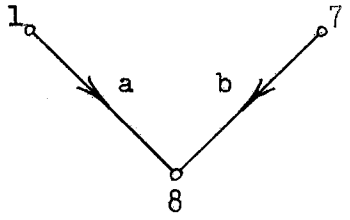
Example 4.4.1

The diagram of the network is shown in Figure 4.4.1(a), and the graph of the desired two-port model of the network is shown in Figure 4.4.1(b). The linear graph which represents the one-port elements of the given network and the model of the multiport (two-port) component of the network are shown in Figures 4.4.1(c) and 4.4.1(d). The input data for the computer program is shown in Table 4.4.1 as it is listed on the data input cards. The added entries on the first card, the general specification card, instruct the program to produce small subnetworks, if possible, with a minimum of four branches or four chords in the augmented subnetworks. The printed output from the computer as the program is executed is shown in Table 4.4.2. Three subnetworks of one-port network elements are formed (Phase 1), and the models of these subnetworks are computed (Phases 2, 3, and 4). These models and the model (computed in Phase 2) of the two-port component of the network are combined, and the coefficient matrices of the model sought are computed and printed at the end of the program (Phases 5 and 6). The resulting two-port model is

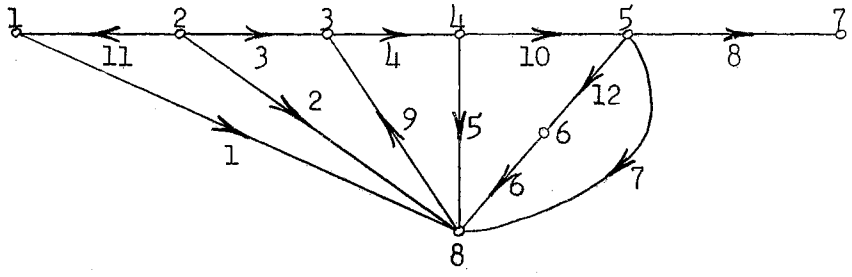
$$\begin{bmatrix} I_a \\ I_b \end{bmatrix} = \begin{bmatrix} 2.2923 & -0.3248 \\ -0.3248 & 1.147 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \end{bmatrix} + \begin{bmatrix} 1.923 & -0.0812 \\ -0.3248 & -0.2131 \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \end{bmatrix} + \begin{bmatrix} -0.5380 & 0.1928 \\ -0.1624 & -0.2436 \end{bmatrix} \begin{bmatrix} J_1 \\ J_2 \end{bmatrix} \qquad (4.4.1)$$



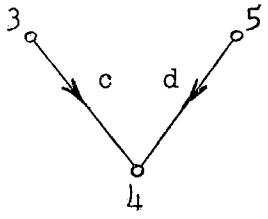
(a)



(b)



(c)



$$\begin{bmatrix} I_c \\ I_d \end{bmatrix} = \begin{bmatrix} 2 & -1 \\ -1 & 2 \end{bmatrix} \begin{bmatrix} V_c \\ V_d \end{bmatrix}$$

(d)

Figure 4.4.1. Network of Example 4.4.1. (a) Network diagram. (b) Desired model. (c) Linear graph of network one-port elements. (d) Model of two-port component of network.

where the reference directions of the currents and voltages are as shown in Figures 4.4.1(a) and 4.4.1(b).

TABLE 4.4.1

COMPUTER INPUT FOR EXAMPLE 4.4.1

```
General Network Specifications
     8    12     2     2     1     2     1     7                 4     4

Multiport Component Data -- DIRECT and G
     3     4     5     4

   2.0 E 00 -1.0 E 00
  -1.0 E 00  2.0 E 00

NTWKCN
     1    11
     2     3    11
     3     4     9
     4     5    10
     7     8    10    12
     6    12
     8
     1     2     5     6     7     9

ORIENT
   1  2  2  3  4  6  5  5  8  4  2  5

Conductance List
   1.0 E 00  1.0 E 00  2.0 E 00  2.0 E 00  1.0 E 00
   0.5 E 00  1.0 E 00  2.0 E 00
```

TABLE 4.4.2

COMPUTER OUTPUT FOR EXAMPLE 4.4.1

```
PHASE 1  NETWORK SUBDIVISION

    TOTAL NUMBER OF NETWORK ELEMENTS    12
    NUMBER OF VOLTAGE DRIVERS            2
    NUMBER OF CURRENT DRIVERS            2
    NUMBER OF CONDUCTANCE ELEMENTS       8
    NUMBER OF MULTITERMINAL COMPONENTS   1

    NUMBER OF PORTS   2
    COMMON NODE IS    8
    PORT NODES ARE    1    7

    NETWORK TWO-TERMINAL ELEMENT CONNECTION ARRAY
    1   11    0    0    0    0
    2    3   11    0    0    0
    3    4    9    0    0    0
    4    5   10    0    0    0
    7    8   10   12    0    0
    6   12    0    0    0    0
    8    0    0    0    0    0
    1    2    5    6    7    9


          SUBNETWORK   1

    SUBNETWORK CONNECTION ARRAY

    1   11   13    0    0    0
    2    3   11    0    0    0
    3    4    9   15    0    0
    4   16    0    0    0    0
    0    0    0    0    0    0
    0    0    0    0    0    0
    0    0    0    0    0    0
    1    2    9   13   15   16

    BRANCHES TO BE INCLUDED IN SUBNETWORK TREE ARE   11   13   15   16

    CHORDS TO BE INCLUDED IN SUBNETWORK COTREE ARE    9


          SUBNETWORK   2

    SUBNETWORK CONNECTION ARRAY

    0    0    0    0    0
    0    0    0    0    0
    0    0    0    0    0
   10   16    0    0    0
    7    8   10   12   17
    6   12    0    0    0
    8   19    0    0    0
    6    7   16   17   19

    BRANCHES TO BE INCLUDED IN SUBNETWORK TREE ARE   12   16   17   19

    CHORDS TO BE INCLUDED IN SUBNETWORK COTREE ARE   10


          SUBNETWORK   3

    SUBNETWORK CONNECTION ARRAY

    0    0
    0    0
    0    0
    5   16
    0    0
    0    0
    0    0
    5   16

    BRANCHES TO BE INCLUDED IN SUBNETWORK TREE ARE   16
```

TABLE 4.4.2 (Continued)

```
PHASE 2


LISTING OF XNODES, XNODE REFERENCE NODES
AND DRIVER BRANCHES CONNECTING XNODES TO REFERENCE NODES

     XNODE   0  2  0  0  0  6  0  0
     REFER   0  1  0  0  0  5  0  0
     DRIVER  0 11  0  0  0 12  0  0


COMPOSITE NETWORK SPECIFICATIONS

     NUMBER OF SUBPORTS          5
     NUMBER OF VOLTAGE DRIVERS   7

     VOLTAGE DRIVER LIST AND
     ORDER IN COMPOSITE REPRESENTATION

     DRIVER 11 12 13  0 15 16 17  0 19
     ORDER   6  7  1  0  3  4  5  0  2


MULTITERMINAL COMPONENT REPRESENTATION


         COMPONENT NUMBER  1

     COMPONENT PORT TERMINALS ARE   3   4   5

     GIVEN TERMINAL REPRESENTATION
      .2000E 01   -.1000E 01
     -.1000E 01    .2000E 01

     TRANSFORMATION CUTSET MATRIX
     -1   0
      1   1
      0  -1

     VOLTAGE DRIVER POSITION LIST   3   4   5

     SUBPORT REPRESENTATION MATRIX
     -.2000E 01    .1000E 01    .1000E 01
      .1000E 01   -.2000E 01    .1000E 01
      .1000E 01    .1000E 01   -.2000E 01


SUBNETWORK TREE FORMATION


          SUBNETWORK    1

     NUMBER OF TREE BRANCHES    4
     NUMBER OF COTREE CHORDS    5
     TREE BRANCHES ARE   11   13   15   16
     COTREE CHORDS ARE    9    1    2    3    4


          SUBNETWORK    2

     NUMBER OF TREE BRANCHES    4
     NUMBER OF COTREE CHORDS    4
     TREE BRANCHES ARE   12   16   17   19
     COTREE CHORDS ARE   10    6    7    8


          SUBNETWORK    3

     NUMBER OF TREE BRANCHES    1
     NUMBER OF COTREE CHORDS    1
     TREE BRANCHES ARE   16
     COTREE CHORDS ARE    5
```

TABLE 4.4.2 (Continued)

```
PHASE 3  CUTSET MATRIX FORMATION

    ORIENTATION LIST

    1    2    2    3    4    6    5    5    8    4
    2    5    8    8    8    8    8    8    8

    CONDUCTANCE LIST

    .1000E 01    .1000E 01    .2000E 01    .2000E 01    .1000E 01
    .5000E 00    .1000E 01    .2000E 01


          SUBNETWORK   1

    NUMBER OF BRANCHES  4     BRANCHES ARE   11   13   15   16
    NUMBER OF CHORDS    5     CHORDS ARE      9    1    2    3    4

    CUTSET MATRIX
      0  0  1  1  0
      0 -1 -1 -1  0
      1  0  0  1 -1
      0  0  0  0  1

    NOSNVS  4     SNVSLT    6    1    3    4
    NOGTRE  0      GTREE

    NOSNCS  1     SNCSLT    1
    NOGCOT  4     GCOTRE   .1000E 01   .1000E 01   .2000E 01   .2000E 01


          SUBNETWORK   2

    NUMBER OF BRANCHES  4     BRANCHES ARE   12   16   17   19
    NUMBER OF CHORDS    4     CHORDS ARE     10    6    7    8

    CUTSET MATRIX
      0 -1  0  0
     -1  0  0  0
      1 -1 -1 -1
      0  0  0  1

    NOSNVS  4     SNVSLT    7    4    5    2
    NOGTRE  0      GTREE

    NOSNCS  1     SNCSLT    2
    NOGCOT  3     GCOTRE   .5000E 00   .1000E 01   .2000E 01


          SUBNETWORK   3

    NUMBER OF BRANCHES  1     BRANCHES ARE   16
    NUMBER OF CHORDS    1     CHORDS ARE      5

    CUTSET MATRIX
     -1

    NOSNVS  1     SNVSLT    4
    NOGTRE  0      GTREE

    NOSNCS  0     SNCSLT
    NOGCOT  1     GCOTRE   .1000E 01
```

TABLE 4.4.2 (Continued)

```
PHASE 4  SUBNETWORK REPRESENTATION


          SUBNETWORK  1

     NUMBER OF VOLTAGE DRIVERS       4
     NUMBER OF CURRENT DRIVERS       1
     NUMBER OF COTREE CONDUCTANCES   4

     VOLTAGE DRIVER COEFFICIENT MATRIX
     -.3000E 01    .3000E 01  -.2000E 01  -.0000E-99
      .3000E 01   -.4000E 01   .2000E 01  -.0000E-99
     -.2000E 01    .2000E 01  -.4000E 01   .2000E 01
     -.0000E-99  -.0000E-99    .2000E 01  -.2000E 01

     VOLTAGE DRIVER POSITION LIST    6    1    3    4

     CURRENT DRIVER COEFFICIENT MATRIX
      .0000E-99
      .0000E-99
     -.1000E 01
      .0000E-99

     CURRENT DRIVER POSITION LIST    1


          SUBNETWORK  2

     NUMBER OF VOLTAGE DRIVERS       4
     NUMBER OF CURRENT DRIVERS       1
     NUMBER OF COTREE CONDUCTANCES   3

     VOLTAGE DRIVER COEFFICIENT MATRIX
     -.5000E 00  -.0000E-99  -.5000E 00  -.0000E-99
     -.0000E-99  -.0000E-99  -.0000E-99  -.0000E-99
     -.5000E 00  -.0000E-99  -.3500E 01   .2000E 01
     -.0000E-99  -.0000E-99   .2000E 01  -.2000E 01

     VOLTAGE DRIVER POSITION LIST    7    4    5    2

     CURRENT DRIVER COEFFICIENT MATRIX
      .0000E-99
      .1000E 01
     -.1000E 01
      .0000E-99

     CURRENT DRIVER POSITION LIST    2


          SUBNETWORK  3

     NUMBER OF VOLTAGE DRIVERS       1
     NUMBER OF CURRENT DRIVERS       0
     NUMBER OF COTREE CONDUCTANCES   1

     VOLTAGE DRIVER COEFFICIENT MATRIX
     -.1000E 01

     VOLTAGE DRIVER POSITION LIST    4
```

TABLE 4.4.2 (Continued)

```
PHASE 5

    1
  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99
  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99
  .0000E-99  .0000E-99 -.2000E 01  .1000E 01  .1000E 01  .0000E-99  .0000E-99
  .0000E-99  .0000E-99  .1000E 01 -.2000E 01  .1000E 01  .0000E-99  .0000E-99
  .0000E-99  .0000E-99  .1000E 01  .1000E 01 -.2000E 01  .0000E-99  .0000E-99

    1
 -.4000E 01  .0000E-99  .2000E 01  .0000E-99  .0000E-99  .3000E 01  .0000E-99
  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99
  .2000E 01  .0000E-99 -.6000E 01  .3000E 01  .1000E 01 -.2000E 01  .0000E-99
  .0000E-99  .0000E-99  .3000E 01 -.4000E 01  .1000E 01  .0000E-99  .0000E-99
  .0000E-99  .0000E-99  .1000E 01  .1000E 01 -.2000E 01  .0000E-99  .0000E-99

    2
 -.4000E 01  .0000E-99  .2000E 01  .0000E-99  .0000E-99  .3000E 01  .0000E-99
  .0000E-99 -.2000E 01  .0000E-99  .0000E-99  .2000E 01  .0000E-99  .0000E-99
  .2000E 01  .0000E-99 -.6000E 01  .3000E 01  .1000E 01 -.2000E 01  .0000E-99
  .0000E-99  .0000E-99  .3000E 01 -.4000E 01  .1000E 01  .0000E-99  .0000E-99
  .0000E-99  .2000E 01  .1000E 01  .1000E 01 -.5500E 01  .0000E-99 -.5000E 00

    3
 -.4000E 01  .0000E-99  .2000E 01  .0000E-99  .0000E-99  .3000E 01  .0000E-99
  .0000E-99 -.2000E 01  .0000E-99  .0000E-99  .2000E 01  .0000E-99  .0000E-99
  .2000E 01  .0000E-99 -.6000E 01  .3000E 01  .1000E 01 -.2000E 01  .0000E-99
  .0000E-99  .0000E-99  .3000E 01 -.5000E 01  .1000E 01  .0000E-99  .0000E-99
  .0000E-99  .2000E 01  .1000E 01  .1000E 01 -.5500E 01  .0000E-99 -.5000E 00


PHASE 6

    1
  .0000E-99  .0000E-99
  .0000E-99  .0000E-99
 -.1000E 01  .0000E-99
  .0000E-99  .0000E-99
  .0000E-99  .0000E-99

    2
  .0000E-99  .0000E-99
  .0000E-99  .0000E-99
 -.1000E 01  .0000E-99
  .0000E-99  .1000E 01
  .0000E-99 -.1000E 01

    3


N-PORT REPRESENTATION


NUMBER OF PORTS     2
NUMBER OF NETWORK VOLTAGE DRIVERS     2
NUMBER OF NETWORK CURRENT DRIVERS     2

  PORT VOLTAGE COEFFICIENT MATRIX

  .2923E 01 -.3248E 00
 -.3248E 00  .1147E 01

  NETWORK VOLTAGE DRIVER COEFFICIENT MATRIX

  .1923E 01 -.8121E-01
 -.3248E 00 -.2131E 00

  NETWORK CURRENT DRIVER COEFFICIENT MATRIX

 -.5380E 00  .1928E 00
 -.1624E 00 -.2436E 00
```

CHAPTER V

n-PORT MODELING OF NETWORKS COMPOSED OF ONE-PORT RESISTIVE, CAPACITIVE, AND INDUCTIVE ELEMENTS AND IDEAL VOLTAGE AND CURRENT DRIVERS

5.1 State-Space n-Port Modeling of Networks. The state-space model of a linear system is generally defined as a set of differential equations of the form

$$\dot{\underline{X}} = \underline{A}\,\underline{X} + \underline{B}\,\underline{M} \qquad (5.1.1)$$

and a set of algebraic equations of the form

$$\underline{Y} = \underline{C}\,\underline{X} + \underline{D}\,\underline{M} \qquad (5.1.2)$$

where

$\underline{X}$ is the vector of state variables,

$\underline{M}$ is the vector of input or driver variables, and

$\underline{Y}$ is the vector of output or response variables (11).

The state model of an n-port network is of the same form as the above general model and is defined as a set of algebraic equations

$$\underline{I}_P = \underline{G}_P\,\underline{V}_P + \underline{G}_D\,\underline{E}_D + \underline{G}_C\,\underline{E}_C + \underline{D}_D\,\underline{J}_D + \underline{D}_L\,\underline{J}_L \qquad (5.1.3)$$

and a set of differential equations

$$\begin{bmatrix} \underline{C} & \underline{0} \\ \underline{0} & \underline{L} \end{bmatrix} \begin{bmatrix} \dot{\underline{E}}_C \\ \dot{\underline{J}}_L \end{bmatrix} = \underline{A} \begin{bmatrix} \underline{E}_C \\ \underline{J}_L \end{bmatrix} + \underline{B} \begin{bmatrix} \underline{V}_P \\ \underline{E}_D \\ \underline{J}_D \end{bmatrix} \qquad (5.1.4)$$

where $\underline{I}_P$, the port current vector, is now defined as a function of

$\underline{V}_P$, the port voltage vector;

$\underline{E}_D$, the network voltage-driver voltage vector;

$\underline{J}_D$, the network current-driver current vector; and

$\underline{E}_C$ and $\underline{J}_L$, the state-variable capacitor voltage and inductor current vectors.

$\underline{C}$ and $\underline{L}$ are, respectively, diagonal matrices of capacitance and inductance values of the network components. The n-port model is thus completely characterized by the coefficient matrices $\underline{A}$, $\underline{B}$, $\underline{G}_P$, $\underline{G}_D$, $\underline{G}_C$, $\underline{D}_D$, and $\underline{D}_L$. The formulation of this model is described in the following paragraphs.

Blackwell and Grigsby (12) considered the network capacitor voltages and inductor currents as voltages and currents of ideal drivers in the formulation of the algebraic equations for a network state-space model. This basic idea permits any formulation technique, ordinarily used in the deriving of n-port models of networks containing only resistive devices, to be used in formulating the algebraic equation of the state model n-port representation of networks containing capacitors and inductors. Thus Equation 5.1.3 of the state model n-port representation for a large network can be formulated by using the theory developed in Chapters I, II, and III, considering capacitors as network voltage drivers and inductors as network current drivers. The partitioned composite subport equation, which corresponds to Equation

2.2.5, is

$$\begin{bmatrix} \underline{I}_{PSP} \\ \underline{I}_{RSP} \end{bmatrix} = \begin{bmatrix} \underline{G}_{11} & \underline{G}_{12} & \underline{G}_{13} & \underline{G}_{14} \\ \underline{G}_{21} & \underline{G}_{22} & \underline{G}_{23} & \underline{G}_{24} \end{bmatrix} \begin{bmatrix} \underline{E}_{PSP} \\ \underline{E}_{RSP} \\ \underline{E}_{C} \\ \underline{E}_{D} \end{bmatrix} + \begin{bmatrix} \underline{D}_{11} & \underline{D}_{12} \\ \underline{D}_{21} & \underline{D}_{22} \end{bmatrix} \begin{bmatrix} \underline{J}_{L} \\ \underline{J}_{D} \end{bmatrix} \tag{5.1.5}$$

where the variables are defined the same as in Equations 2.2.5, 5.1.3, and 5.1.4. Again as in Section 2.2, $\underline{I}_{RSP}$ is set equal to zero and $\underline{E}_{RSP}$ is determined:

$$\underline{E}_{RSP} = \underline{G}_{22}^{-1} [-\underline{G}_{21} \underline{V}_{P} - \underline{G}_{23} \underline{E}_{C} - \underline{G}_{24} \underline{E}_{D} - \underline{D}_{21} \underline{J}_{L} - \underline{D}_{22} \underline{J}_{D}] \tag{5.1.6}$$

Similarly, Equation 5.1.6 is substituted into Equation 5.1.5 forming the equation

$$\begin{aligned} \underline{I}_{PSP} = {} & [\underline{G}_{11} - \underline{G}_{12} \underline{G}_{22}^{-1} \underline{G}_{21}] \underline{E}_{PSP} + [\underline{G}_{13} - \underline{G}_{12} \underline{G}_{22}^{-1} \underline{G}_{23}] \underline{E}_{C} \\ & + [\underline{G}_{14} - \underline{G}_{12} \underline{G}_{22}^{-1} \underline{G}_{24}] \underline{E}_{D} + [\underline{D}_{11} - \underline{G}_{12} \underline{G}_{22}^{-1} \underline{D}_{21}] \underline{J}_{L} \\ & + [\underline{D}_{12} - \underline{G}_{12} \underline{G}_{22}^{-1} \underline{D}_{22}] \underline{J}_{D} \end{aligned} \tag{5.1.7}$$

which is of the form of Equation 5.1.3 where

$$\underline{I}_{P} = \underline{I}_{PSP}$$

$$\underline{V}_{P} = -\underline{E}_{PSP}$$

$$\underline{G}_{P} = \underline{G}_{11} - \underline{G}_{12} \underline{G}_{22}^{-1} \underline{G}_{21}$$

$$\underline{G}_{D} = \underline{G}_{14} - \underline{G}_{12} \underline{G}_{22}^{-1} \underline{G}_{24}$$

$$\underline{G}_{C} = \underline{G}_{13} - \underline{G}_{12} \underline{G}_{22}^{-1} \underline{G}_{23}$$

$$\underline{D}_D = \underline{D}_{12} - \underline{G}_{12}\,\underline{G}_{22}^{-1}\,\underline{D}_{22}, \text{ and}$$

$$\underline{D}_L = \underline{D}_{11} - \underline{G}_{12}\,\underline{G}_{22}^{-1}\,\underline{D}_{21}$$

The formulation of the subnetwork state model differential equation is similar to the differential equation formulation given by Brown (13), in which inductors are allowed to appear in the network tree, and capacitors are allowed in the network cotree (13). In the more restricted case considered here, the subnetwork is such that a tree and cotree exist such that all capacitors and voltage drivers are in the tree and all inductors and current drivers are in the cotree. The differential equation is formulated by considering the subnetwork cutset and circuit equations partitioned as follows:

$$\begin{bmatrix} \underline{U} & \underline{0} & \underline{0} & \underline{S}_{11} & \underline{S}_{12} & \underline{S}_{13} \\ \underline{0} & \underline{U} & \underline{0} & \underline{S}_{21} & \underline{S}_{22} & \underline{S}_{23} \\ \underline{0} & \underline{0} & \underline{U} & \underline{S}_{31} & \underline{S}_{32} & \underline{S}_{33} \end{bmatrix} \begin{bmatrix} \underline{I}_C \\ \underline{I}_D \\ \underline{I}_{TG} \\ \underline{J}_L \\ \underline{J}_D \\ \underline{I}_{CG} \end{bmatrix} = \underline{0} \qquad (5.1.8)$$

$$\begin{bmatrix} -\underline{S}_{11}^T & -\underline{S}_{21}^T & -\underline{S}_{31}^T & \underline{U} & \underline{0} & \underline{0} \\ -\underline{S}_{12}^T & -\underline{S}_{22}^T & -\underline{S}_{32}^T & \underline{0} & \underline{U} & \underline{0} \\ -\underline{S}_{13}^T & -\underline{S}_{23}^T & -\underline{S}_{33}^T & \underline{0} & \underline{0} & \underline{U} \end{bmatrix} \begin{bmatrix} \underline{E}_C \\ \underline{E}_D \\ \underline{V}_{TG} \\ \underline{V}_L \\ \underline{V}_D \\ \underline{V}_{CG} \end{bmatrix} = \underline{0} \qquad (5.1.9)$$

and the component equations

$$\begin{bmatrix} \underline{I}_{TG} \\ \underline{I}_{C} \\ \underline{I}_{CG} \\ \underline{V}_{L} \end{bmatrix} = \begin{bmatrix} \underline{G}_{T} & & & \\ & \underline{C} & & \\ & & \underline{G}_{C} & \\ & & & \underline{L} \end{bmatrix} \begin{bmatrix} \underline{V}_{TG} \\ \frac{d}{dt}\underline{E}_{C} \\ \underline{V}_{CG} \\ \frac{d}{dt}\underline{J}_{L} \end{bmatrix} \qquad (5.1.10)$$

where

$\underline{I}_C$ and $\underline{E}_C$ are the capacitor current and voltage vectors,

$\underline{I}_D$ and $\underline{E}_D$ are the voltage-driver current and voltage vectors,

$\underline{I}_{TG}$ and $\underline{V}_{TG}$ are the tree conductance current and voltage vectors,

$\underline{J}_L$ and $\underline{V}_L$ are the inductor current and voltage vectors,

$\underline{J}_D$ and $\underline{V}_D$ are the current-driver current and voltage vectors, and

$\underline{I}_{CG}$ and $\underline{V}_{CG}$ are the cotree current and voltage vectors.

By a procedure similar to that used by Brown, the cutset, circuit, and component equations are used to obtain the subnetwork state-model differential equation

$$\begin{bmatrix} \underline{C}_s & \underline{0} \\ \underline{0} & \underline{L}_s \end{bmatrix} \begin{bmatrix} \dot{\underline{E}}_{Cs} \\ \dot{\underline{J}}_{Ls} \end{bmatrix} = \begin{bmatrix} \underline{A}_{11s} & \underline{A}_{12s} \\ \underline{A}_{21s} & \underline{A}_{22s} \end{bmatrix} \begin{bmatrix} \underline{E}_{Cs} \\ \underline{J}_{Ls} \end{bmatrix} + \begin{bmatrix} \underline{B}_{11s} & \underline{B}_{12s} \\ \underline{B}_{21s} & \underline{B}_{22s} \end{bmatrix} \begin{bmatrix} \underline{E}_{Ds} \\ \underline{J}_{Ds} \end{bmatrix} \qquad (5.1.11)$$

where the s in the subscripts denotes subnetwork and where

$$\underline{A}_{11s} = \underline{S}_{13}\,\underline{G}_C\,\underline{S}_{33}^T\,[\underline{G}_T + \underline{S}_{33}\,\underline{G}_C\,\underline{S}_{33}^T]^{-1}\,\underline{S}_{33}\,\underline{G}_C - \underline{G}_C\,\underline{S}_{13}^T$$

$$\underline{A}_{12s} = \underline{S}_{13}\,\underline{G}_C\,\underline{S}_{33}^T\,[\underline{G}_T + \underline{S}_{33}\,\underline{G}_C\,\underline{S}_{33}^T]^{-1}\,\underline{S}_{31} - \underline{S}_{11}$$

$$\underline{A}_{21s} = \underline{S}_{11}^{T} - \underline{S}_{31}^{T}[\underline{G}_T + \underline{S}_{33}\,\underline{G}_C\,\underline{S}_{33}^{T}]^{-1}\,\underline{S}_{33}\,\underline{G}_C\,\underline{S}_{13}^{T}$$

$$\underline{A}_{22s} = -\underline{S}_{31}^{T}[\underline{G}_T + \underline{S}_{33}\,\underline{G}_C\,\underline{S}_{33}^{T}]^{-1}\,\underline{S}_{31}$$

$$\underline{B}_{11s} = \underline{S}_{13}\,\underline{G}_C\,\underline{S}_{33}^{T}[\underline{G}_T + \underline{S}_{33}\,\underline{G}_C\,\underline{S}_{33}^{T}]^{-1}\,\underline{S}_{33}\,\underline{G}_C - \underline{G}_C\,\underline{S}_{23}^{T}$$

$$\underline{B}_{12s} = \underline{S}_{13}\,\underline{G}_C\,\underline{S}_{33}^{T}[\underline{G}_T + \underline{S}_{33}\,\underline{G}_C\,\underline{S}_{33}^{T}]^{-1}\,\underline{S}_{32} - \underline{S}_{12}$$

$$\underline{B}_{21s} = \underline{S}_{21}^{T} - \underline{S}_{31}^{T}[\underline{G}_T + \underline{S}_{33}\,\underline{G}_C\,\underline{S}_{33}^{T}]^{-1}\,\underline{S}_{33}\,\underline{G}_C\,\underline{S}_{23}^{T} \quad \text{and}$$

$$\underline{B}_{22s} = -\underline{S}_{31}^{T}[\underline{G}_T + \underline{S}_{33}\,\underline{G}_C\,\underline{S}_{33}^{T}]^{-1}\,\underline{S}_{32}$$

A composite state-model differential equation for a network is made up from the subnetwork state-model differential equations of the form

$$\begin{bmatrix} \underline{C} & \underline{0} \\ \underline{0} & \underline{L} \end{bmatrix} \begin{bmatrix} \dot{\underline{E}}_C \\ \dot{\underline{J}}_L \end{bmatrix} = \begin{bmatrix} \underline{A}_{11c} & \underline{A}_{12c} \\ \underline{A}_{21c} & \underline{A}_{22c} \end{bmatrix} \begin{bmatrix} \underline{E}_C \\ \underline{J}_L \end{bmatrix} + \begin{bmatrix} \underline{B}_{11c} & \underline{B}_{12c} & \underline{B}_{13c} & \underline{B}_{14c} \\ \underline{B}_{21c} & \underline{B}_{22c} & \underline{B}_{23c} & \underline{B}_{24c} \end{bmatrix} \begin{bmatrix} \underline{E}_{PSP} \\ \underline{E}_{RSP} \\ \underline{E}_D \\ \underline{J}_D \end{bmatrix} \tag{5.1.12}$$

where the matrices $\underline{C}$ and $\underline{L}$ are diagonal matrices of values of all of the capacitors and inductors in the given network and the vectors $\underline{E}_{PSP}$, $\underline{E}_{RSP}$, $\underline{E}_D$, and $\underline{J}_D$ are the same as defined in Equation 5.1.5. The subscript c in Equation 5.1.12 denotes composite.

The composite matrices $\underline{A}_C$ and $\underline{B}_C$ are formed by the proper location of the elements of all of the subnetwork matrices $\underline{A}_S$ and $\underline{B}_S$. If each passive component--capacitor and inductor--is numbered in the order in which its associated variable appears in the state variable vector,

$[\underline{E}_C^T \; \underline{J}_L^T]^T$, and each driver is numbered in the order in which it appears in the composite differential equation, it is a simple process to locate the composite matrix element positions where the subnetwork matrix elements belong. Each component appears in only one subnetwork. The rows and columns of each subnetwork $\underline{A}_s$ matrix and the rows of each subnetwork $\underline{B}_s$ matrix can be labeled with the associated component numbers, the numbers being derived from the numbering of the components in the composite equation. The columns of the $\underline{B}_s$ matrices can be labeled with the numbers associated with the drivers of the subnetworks, the numbers being derived from the numbering of the drivers in the composite equation. The labeling of the rows and columns of the subnetwork matrices then indicate the proper composite $\underline{A}_c$ and $\underline{B}_c$ element positions for the elements of the subnetwork $\underline{A}_s$ and $\underline{B}_s$ elements.

The following is observed concerning the matrices as they are partitioned in Equations 5.1.11 and 5.1.12. The elements of the subnetwork submatrices $\underline{A}_{11s}$, $\underline{A}_{12s}$, $\underline{A}_{21s}$, and $\underline{A}_{22s}$ compose the submatrices $\underline{A}_{11c}$, $\underline{A}_{12c}$, $\underline{A}_{21c}$, and $\underline{A}_{22c}$, respectively. The elements of the subnetwork submatrices $\underline{B}_{11s}$ compose the submatrices $\underline{B}_{11c}$, $\underline{B}_{12c}$, and $\underline{B}_{13c}$; the elements of the subnetwork submatrices $\underline{B}_{21s}$ compose the submatrices $\underline{B}_{21c}$, $\underline{B}_{22c}$, and $\underline{B}_{23c}$; and the elements of the subnetwork submatrices $\underline{B}_{12s}$ and $\underline{B}_{22s}$ compose the submatrices $\underline{B}_{14c}$ and $\underline{B}_{24c}$, respectively.

Having formed the composite matrices of Equation 5.1.12, one step remains in obtaining the state-model differential equation, Equation 5.1.4, for the desired n-port model. The expression, Equation 5.1.6, for $\underline{E}_{RSP}$ is substituted into Equation 5.1.12. The result is the partitioned form of Equation 5.1.4

$$\begin{bmatrix} \underline{C} & \underline{0} \\ \underline{0} & \underline{L} \end{bmatrix} \begin{bmatrix} \dot{\underline{E}}_C \\ \dot{\underline{J}}_L \end{bmatrix} = \begin{bmatrix} \underline{A}_{11} & \underline{A}_{12} \\ \underline{A}_{21} & \underline{A}_{22} \end{bmatrix} \begin{bmatrix} \underline{E}_C \\ \underline{J}_L \end{bmatrix} + \begin{bmatrix} \underline{B}_{11} & \underline{B}_{12} & \underline{B}_{13} \\ \underline{B}_{21} & \underline{B}_{22} & \underline{B}_{23} \end{bmatrix} \begin{bmatrix} \underline{V}_P \\ \underline{E}_D \\ \underline{J}_D \end{bmatrix} \tag{5.1.13}$$

where

$$\underline{A}_{11} = \underline{A}_{11c} - \underline{B}_{12c}\,\underline{G}_{22}^{-1}\,\underline{G}_{24}$$

$$\underline{A}_{12} = \underline{A}_{12c} - \underline{B}_{12c}\,\underline{G}_{22}^{-1}\,\underline{D}_{21}$$

$$\underline{A}_{21} = \underline{A}_{21c} - \underline{B}_{22c}\,\underline{G}_{22}^{-1}\,\underline{G}_{24}$$

$$\underline{A}_{22} = \underline{A}_{22c} - \underline{B}_{22c}\,\underline{G}_{22}^{-1}\,\underline{D}_{21}$$

$$\underline{B}_{11} = -[\underline{B}_{11c} - \underline{B}_{12c}\,\underline{G}_{22}^{-1}\,\underline{G}_{21}]$$

$$\underline{B}_{12} = \underline{B}_{13c} - \underline{B}_{12c}\,\underline{G}_{22}^{-1}\,\underline{G}_{23}$$

$$\underline{B}_{13} = \underline{B}_{14c} - \underline{B}_{12c}\,\underline{G}_{22}^{-1}\,\underline{D}_{22}$$

$$\underline{B}_{21} = \underline{B}_{21c} - \underline{B}_{22c}\,\underline{G}_{22}^{-1}\,\underline{G}_{21}$$

$$\underline{B}_{22} = \underline{B}_{23c} - \underline{B}_{22c}\,\underline{G}_{22}^{-1}\,\underline{G}_{23} \qquad \text{and}$$

$$\underline{B}_{23} = \underline{B}_{24c} - \underline{B}_{22c}\,\underline{G}_{22}^{-1}\,\underline{D}_{22}$$

5.2 The Computer Program. A program, designated Program II, has been written which computes the coefficient matrices of the n-port state-space model of a network of one-port resistors, capacitors, inductors, current drivers, and voltage drivers. The program will compute a one- to five-port Lagrangian model, as specified, of a network

with up to forty nodes, with a maximum of ten elements incident at any node, 100 resistors, 20 capacitors, 20 inductors, ten voltage drivers, and ten current drivers. The program, like Program I, is written in FORTRAN IV language for execution on the IBM 1410 computer. The length of the program required that Program II be written in 13 phases. The phases are executed in sequence, and data is transferred to succeeding phases by means of six computer tape units. The program input is by punched cards, and the output is printed.

The input data is similar to that of Program I and is obtained in the same manner from the network graph as described in Section 4.3. The only difference is the numbering of the network graph elements and the omission of multiport component data in Program II. The network graph elements are numbered as follows: conductances first, inductors second, current drivers third, capacitors fourth, and voltage drivers last.

Program II requires the following input data:

1. General network specifications:
   (a) the number of nodes,
   (b) the number of elements,
   (c) the number of voltage drivers,
   (d) the number of current drivers,
   (e) the number of capacitors,
   (f) the number of inductors,
   (g) the number of ports, and
   (h) the list of network port nodes.
2. The network connection array, NTWKCN.
3. The orientation list, ORIENT.
4. A list of the conductance values in mhos in the order in which

the conductance elements are numbered on the network graph.

The following paragraphs describe the sequence of operations of Program II. Flow charts of the program phases are found in Appendix D. The FORTRAN variable names used in the flow charts and in the following paragraphs are defined in Appendix B.

Phase 1 performs the network division utilizing the algorithm of Chapter II. Capacitor and inductor elements are considered as voltage driver and current driver elements, respectively. The subnetwork connection array and the partial tree and cotree lists, TRESET and CRDSET, are computed for each subnetwork and are written on tape for Phase 2. A list, SRBRLT, of all voltage driver elements--network drivers, subport drivers, and capacitor elements--is compiled and written on tape for Phase 2.

Phase 2 performs two functions. First, the entries of the voltage driver list, SRBRLT, are numbered, forming the list, LIST, as in Phase 2 of Program I. The second function of Phase 2 is the computation of the tree and cotree for each subnetwork. Each subnetwork is processed in turn. The elements of the partial tree and cotree lists, obtained in Phase 1, are ordered numerically so that all capacitor and all inductor elements are listed first in the respective lists. The tree and cotree lists are completed the same as in Phase 2 of Program I.

Phase 3 is the same as Phase 3 of Program I except that four additional lists are compiled for each subnetwork: LISTE, the list of voltage driver elements; LISTJ, the list of current driver elements; LISTC, the list of capacitor elements; and LISTL, the list of inductor elements of the subnetwork. The lists SNVSLT and SNCSLT include both voltage driver and capacitor elements and current driver and inductor

elements, respectively. The lists along with the cutset matrix and GTREE and GCOTRE lists are written on tape for use in Phases 4 and 8.

Phase 4 is the same as Phase 4 of Program I.

Phase 5 forms the composite subport model matrix $\underline{G}$ (Equation 5.1.5) in the same manner as Phase 5 of Program I and computes the n-port model coefficient matrices $\underline{G}_P$, $\underline{G}_D$, and $\underline{G}_C$. These matrices are written on tape for Phase 13. The submatrix products $\underline{G}_{22}^{-1}\,\underline{G}_{21}$, $\underline{G}_{22}^{-1}\,\underline{G}_{23}$, and $\underline{G}_{22}^{-1}\,\underline{G}_{24}$ are computed and written on tape for Phases 10 and 12. The submatrices $\underline{G}_{22}^{-1}$ and $\underline{G}_{12}$ are written on tape for Phase 6.

Phase 6 forms the composite model matrix $\underline{D}$ (Equation 5.1.5) in the same manner as Phase 6 of Program I, computes the n-port model coefficient matrices $\underline{D}_L$ and $\underline{D}_J$, and writes the matrices on tape for Phase 13. The submatrix products $\underline{G}_{22}^{-1}\,\underline{D}_{21}$ and $\underline{G}_{22}^{-1}\,\underline{D}_{22}$ are computed and written on tape for Phases 10 and 12.

Phase 7 reads from tape the five submatrix products written by Phases 5 and 6 for Phases 10 and 12. The products are rewritten on the same tape in an order compatible for use by Phases 10 and 12.

Phase 8 computes for each subnetwork the matrix $\underline{A}$ and matrix $\underline{B}$ submatrices (Equation 5.1.11) and writes these on tape for Phases 9 and 11 together with the lists, LISTE, LISTJ, LISTC, and LISTL.

Phase 9 compiles the composite matrix $\underline{B}_C$ (Equation 5.1.12) from the subnetwork $\underline{B}_S$ submatrices, computed by Phase 8, by using the LISTC, LISTL, LISTE, and LISTJ lists to relocate the elements of the submatrices in the composite matrix. The two rows of submatrices of the partitioned composite $\underline{B}$ matrix are written separately on tape for Phase 10.

Phase 10 operates first on the top row and then on the bottom row

of composite $\underline{B}_c$-matrix submatrices, read from tape from Phase 9, to compute the following: the n-port model coefficient matrices $\underline{B}_{11}$, $\underline{B}_{12}$, $\underline{B}_{13}$, $\underline{B}_{21}$, $\underline{B}_{22}$, and $\underline{B}_{23}$ which are written on tape for Phase 13 and the submatrix products $\underline{B}_{12}\,\underline{G}_{22}^{-1}\,\underline{G}_{24}$, $\underline{B}_{12}\,\underline{G}_{22}^{-1}\,\underline{D}_{21}$, $\underline{B}_{22}\,\underline{G}_{22}^{-1}\,\underline{G}_{24}$, and $\underline{B}_{22}\,\underline{G}_{22}^{-1}\,\underline{D}_{21}$ which are written on tape for Phase 12.

Phase 11 compiles the composite matrix $\underline{A}_c$ (Equation 5.1.12) from the subnetwork $\underline{A}_s$ submatrices, computed by Phase 8, by using the LISTC and LISTL lists to relocate the elements of the submatrices in the composite matrix. The two rows of submatrices of the partitioned composite $\underline{A}$ matrix are written separately on tape for Phase 12.

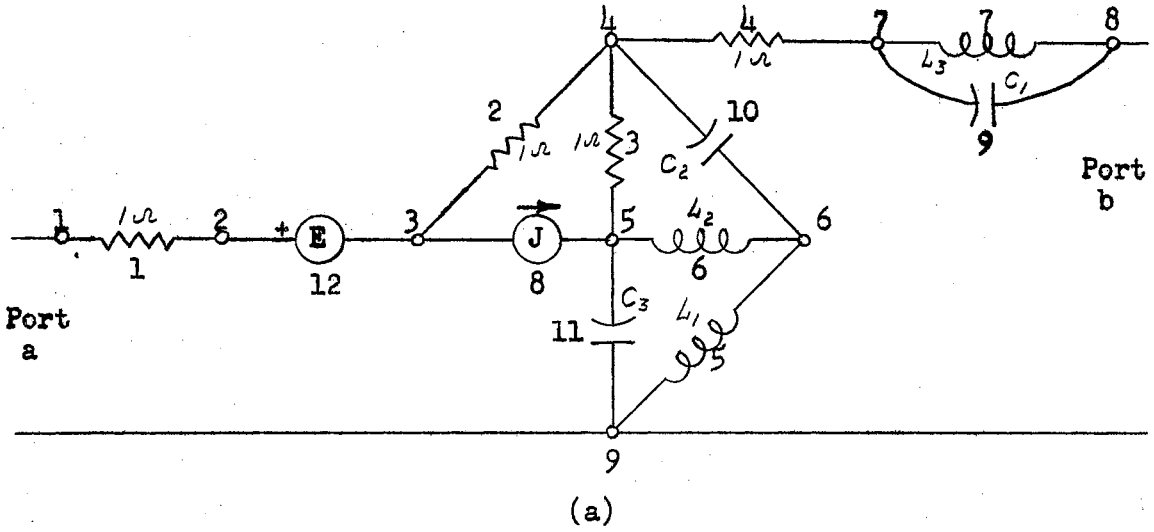
Phase 12 operates first on the top row and then on the bottom row of composite $\underline{A}_c$-matrix submatrices, read from tape from Phase 11, to compute the n-port model coefficient matrices $\underline{A}_{11}$, $\underline{A}_{12}$, $\underline{A}_{21}$, and $\underline{A}_{22}$ which are written on tape for Phase 13.

Phase 13 reads the coefficient matrices and prints the n-port model on the computer line printer.

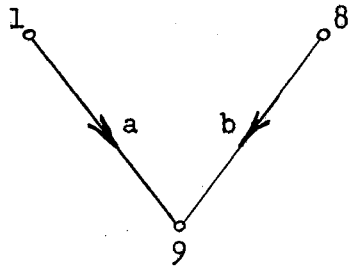
5.3 Illustrative Example. Program II was used to compute the n-port state-space model for a number of networks. One example follows.

Example 5.3.1

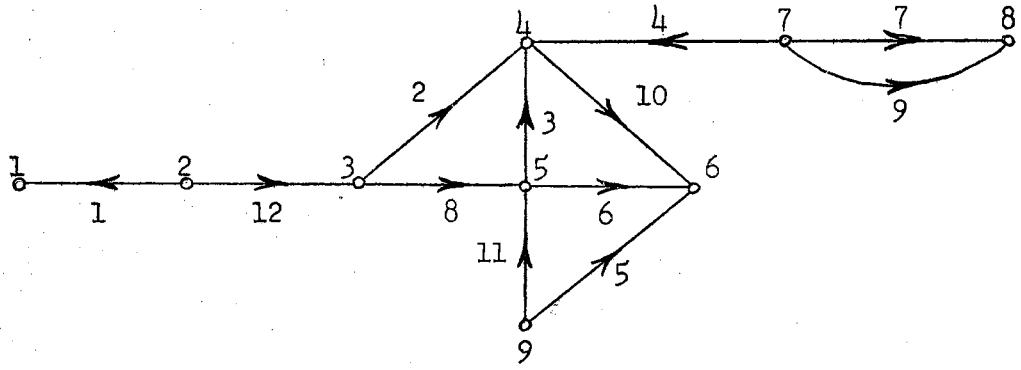
The network is illustrated in Figure 5.3.1(a), and the desired port model tree is shown in Figure 5.3.1(b). The data of Table 5.3.1 is the computer input data obtained from the network diagram and the linear graph, Figure 5.3.1(c), which represents the given network. Table 5.3.2 contains the output of the computer as the program is executed. The subnetwork connection arrays are given (Phase 1). The subnetwork trees, cotrees, and cutset matrices are computed (Phases 2



(a)



(b)



(c)

Figure 5.3.1. Network of Example 5.3.1. (a) Network diagram. (b) Desired model. (c) Linear graph of network.

and 3). The coefficient matrices of the subnetwork algebraic models and the submatrices of the subnetwork differential equation matrices $\underline{A}_s$ and $\underline{B}_s$ are printed in the output from Phases 4 and 8. The composite matrices are printed after the addition of each subnetwork model to the composite model in Phases 5, 6, 9, and 11. The coefficient matrices of the two-port model as printed by Phase 13 conclude Table 5.3.2.

TABLE 5.3.1

COMPUTER INPUT FOR EXAMPLE 5.3.1

```
General Network Specifications
     9    12     1     1     3     3     2     1     8           5     5

NTWKCN
     1
     1    12
     2     8    12
     2     3     4    10
     3     6     8    11
     5     6    10
     4     7     9
     7     9
     5    11

ORIENT
   2   3   5   7   9   5   7   3   7   4   9   2

Conductance List
   1.0 E 00  1.0 E 00  1.0 E 00  1.0 E 00
```

TABLE 5.3.2

COMPUTER OUTPUT FOR EXAMPLE 5.3.1

```
PHASE 1  NETWORK SUBDIVISION

     TOTAL NUMBER OF NETWORK ELEMENTS  12
     NUMBER OF VOLTAGE DRIVERS          1
     NUMBER OF CURRENT DRIVERS          1
     NUMBER OF CAPACITANCE ELEMENTS     3
     NUMBER OF INDUCTANCE ELEMENTS      3
     NUMBER OF CONDUCTANCE ELEMENTS     4

     NUMBER OF PORTS   2
     COMMON NODE IS    9
     PORT NODES ARE    1    8

     NETWORK CONNECTION ARRAY
     1     0     0     0
     1    12     0     0
     2     8    12     0
     2     3     4    10
     3     6     8    11
     5     6    10     0
     4     7     9     0
     7     9     0     0
     5    11     0     0


           SUBNETWORK   1

     SUBNETWORK CONNECTION ARRAY

     1    13     0     0
     1    12     0     0
     2     8    12     0
     2     3    10    16
     3     6     8    11
     5     6    10     0
     0     0     0     0
     0     0     0     0
     5    11    13    16

     BRANCHES TO BE INCLUDED IN SUBNETWORK TREE ARE   11   10   12   13   16

     CHORDS TO BE INCLUDED IN SUBNETWORK COTREE ARE    6    8    5


           SUBNETWORK   2

     SUBNETWORK CONNECTION ARRAY

     0     0     0
     0     0     0
     0     0     0
     4    16     0
     0     0     0
     0     0     0
     4     7     9
     7     9    20
    16    20     0

     BRANCHES TO BE INCLUDED IN SUBNETWORK TREE ARE    9   16   20

     CHORDS TO BE INCLUDED IN SUBNETWORK COTREE ARE    7
```

TABLE 5.3.2 (Continued)

PHASE 2 TREE FORMATION

COMPOSITE NETWORK SPECIFICATIONS

NUMBER OF SUBPORTS 3
NUMBER OF VOLTAGE DRIVERS 7

VOLTAGE DRIVER LIST AND
ORDER IN COMPOSITE REPRESENTATION

DRIVER	9	10	11	12	13	0	0	16	0	0	0	20
ORDER	5	6	7	4	1	0	0	3	0	0	0	2

SUBNETWORK 1

NUMBER OF TREE BRANCHES	6				
NUMBER OF COTREE CHORDS	5				
TREE BRANCHES ARE	10	11	12	13	16	1
COTREE CHORDS ARE	5	6	8	3	2	

SUBNETWORK 2

NUMBER OF TREE BRANCHES	3		
NUMBER OF COTREE CHORDS	2		
TREE BRANCHES ARE	9	16	20
COTREE CHORDS ARE	7	4	

TABLE 5.3.2 (Continued)

```
PHASE 3  CUTSET MATRIX FORMATION

    ORIENTATION LIST

    2    3    5    7    9    5    7    3    7    4
    9    2    9    9    9    9    9    9    9    9

    CONDUCTANCE LIST

    .1000E 01    .1000E 01    .1000E 01    .1000E 01


          SUBNETWORK   1

    NUMBER OF BRANCHES  6     BRANCHES ARE   10   11   12   13   16    1
    NUMBER OF CHORDS    5     CHORDS ARE      5    6    8    3    2

    CUTSET MATRIX
      1   1   0   0   0
      0  -1   1  -1   0
      0   0  -1   0  -1
      0   0  -1   0  -1
      1   1   0   1   1
      0   0   1   0   1

    NOSNVS  5      SNVSLT    6    7    4    1    3
    NRCAPS  2       LISTC    2    3
    NRVTSR  3       LISTE    4    1    3
    NOGTRE  1       GTREE   .1000E 01

    NOSNCS  3      SNCSLT    1    2    4
    NRINDS  2       LISTL    1    2
    NRCTSR  1       LISTJ    1
    NOGCOT  2      GCOTRE   .1000E 01    .1000E 01


          SUBNETWORK   2

    NUMBER OF BRANCHES  3     BRANCHES ARE    9   16   20
    NUMBER OF CHORDS    2     CHORDS ARE      7    4

    CUTSET MATRIX
      1   1
      0   1
      0  -1

    NOSNVS  3      SNVSLT    5    3    2
    NRCAPS  1       LISTC    1
    NRVTSR  2       LISTE    3    2
    NOGTRE  0       GTREE

    NOSNCS  1      SNCSLT    3
    NRINDS  1       LISTL    3
    NRCTSR  0       LISTJ
    NOGCOT  1      GCOTRE   .1000E 01
```

TABLE 5.3.2 (Continued)

```
PHASE 4  COMPUTATION OF SUBNETWORK MATRICES G AND D


          SUBNETWORK  1

     NUMBER OF VOLTAGE DRIVERS       5
     NUMBER OF CURRENT DRIVERS       3
     NUMBER OF COTREE CONDUCTANCES   2

     VOLTAGE DRIVER COEFFICIENT MATRIX
   .CCCOE-99    .0000E-99    .0C00E-99    .C000E-99    .0000E-99
   .CCCOE-99   -.1C0CE 01    .0000E-99    .0000E-99    .1000E 01
   .CCCOE-99    .CCCCE-99   -.5000E 00   -.5000E 00    .5000E 00
   .CCCOE-99    .CCCOE-99   -.5C00E 00   -.5000E 00    .5000E 00
   .CCCOE-99    .1CCCE 01    .5C00E 00    .5000E 00   -.1500E 01

     VOLTAGE DRIVER POSITION LIST    6    7    4    1    3

     CURRENT DRIVER COEFFICIENT MATRIX
  -.1000E 01   -.1000E 01    .C000E-99
   .CCCOE-99    .1CCCE 01   -.1000E 01
   .CCCOE-99    .CCCCE-99    .5000E 00
   .CCCCE-99    .0000E-99    .5000E 00
  -.1CCCE 01   -.1CCCE 01    .5000E 00

     CURRENT DRIVER POSITION LIST    1    2    4


          SUBNETWORK  2

     NUMBER OF VOLTAGE DRIVERS       3
     NUMBER OF CURRENT DRIVERS       1
     NUMBER OF COTREE CONDUCTANCES   1

     VOLTAGE DRIVER COEFFICIENT MATRIX
  -.1CCCE 01   -.1CCCE 01    .1000E 01
  -.1CCCE 01   -.1CCCE 01    .1C00E 01
   .1CCCE 01    .1CCCE 01   -.1000E 01

     VOLTAGE DRIVER POSITION LIST    5    3    2

     CURRENT DRIVER COEFFICIENT MATRIX
  -.1C00E 01
   .CC00E-99
   .CCCCE-99

     CURRENT DRIVER POSITION LIST    3


PHASE 5

     1
 -.5CCCE CC   .CCCCE-99   .5CCCE 00  -.5000E 00   .C000E-99   .0000E-99   .0000E-99
   .CCCCE-99  .CCCCE-99   .CCCCE-99   .0000E-99   .0000E-99   .0000E-99   .0000E-99
   .5CCCE CC  .0000E-99  -.1500E 01   .5000E 00   .0000E-99   .0000E-99   .1000E 01

     2
 -.5CCCE CC   .0000E-99   .5C00E 00  -.5000E 00   .0000E-99   .0000E-99   .0000E-99
   .CCCCE-99  -.1CCCE 01   .1000E 01   .0000E-99   .1000E 01   .0000E-99   .0000E-99
   .5CCCE CC   .1000E 01  -.25C0E 01   .5000E 00  -.1000E 01   .0000E-99   .1CCCE 01


PHASE 6

     1
   .CCCCE-99   .CCCCE-99   .CCCCE-99   .5000E 00
   .CCCCE-99   .0000E-99   .CCCCE-99   .0000E-99
  -.1CCCE 01  -.1CCCE 01   .CCCCE-99   .5000E 00

     2
   .CCCCE-99   .CCCCE-99   .CCCCE-99   .5000E 00
   .CCCCE-99   .0000E-99   .CCCCE-99   .0000E-99
  -.1CCCE 01  -.1CCCE 01   .CCCCE-99   .5000E 00
```

TABLE 5.3.2 (Continued)

```
PHASE 8  COMPUTE SUBMATRICES OF SUBNETWORK MATRICES A AND B

          SUBNETWORK     1

    LISTC     2     3
    LISTL     1     2
    LISTE     4     1     3
    LISTJ     1

    A22
 -.00000E-99  -.00000E-99
 -.00000E-99  -.00000E-99

    B22
 -.00000E-99
 -.00000E-99

    B21
  .00000E-99   .00000E-99   .10000E 01
  .00000E-99   .00000E-99   .10000E 01

    A21
  .10000E 01   .00000E-99
  .10000E 01  -.10000E 01

    A12
 -.10000E 01  -.10000E 01
  .00000E-99   .10000E 01

    B12
  .00000E-99
 -.10000E 01

    A11
  .00000E-99   .00000E-99
  .00000E-99  -.10000E 01

    B11
  .00000E-99   .00000E-99   .00000E-99
  .00000E-99   .00000E-99   .10000E 01


          SUBNETWORK     2

    LISTC     1
    LISTL     3
    LISTE     3     2

    B21
  .00000E-99   .00000E-99

    A21
  .10000E 01

    A12
 -.10000E 01

    A11
 -.10000E 01

    B11
 -.10000E 01   .10000E 01
```

TABLE 5.3.2 (Continued)

```
PHASE 9  COMPUTE COMPOSITE B MATRIX

SBNWNO  1
  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99
  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99
  .0000E-99  .0000E-99  .1000E 01  .0000E-99 -.1000E 01
  .0000E-99  .0000E-99  .1000E 01  .0000E-99 -.0000E-99
  .0000E-99  .0000E-99  .1000E 01  .0000E-99 -.0000E-99
  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99

SBNWNO  2
  .0000E-99  .1000E 01 -.1000E 01  .0000E-99  .0000E-99
  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99
  .0000E-99  .0000E-99  .1000E 01  .0000E-99 -.1000E 01
  .0000E-99  .0000E-99  .1000E 01  .0000E-99 -.0000E-99
  .0000E-99  .0000E-99  .1000E 01  .0000E-99 -.0000E-99
  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99


PHASE 11  COMPUTE COMPOSITE A MATRIX

SBNWNO  1
  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99
  .0000E-99  .0000E-99  .0000E-99 -.1000E 01 -.1000E 01  .0000E-99
  .0000E-99  .0000E-99 -.1000E 01  .0000E-99  .1000E 01  .0000E-99
  .0000E-99  .1000E 01  .0000E-99 -.0000E-99 -.0000E-99  .0000E-99
  .0000E-99  .1000E 01 -.1000E 01 -.0000E-99 -.0000E-99  .0000E-99
  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99

SBNWNO  2
 -.1000E 01  .0000E-99  .0000E-99  .0000E-99  .0000E-99 -.1000E 01
  .0000E-99  .0000E-99  .0000E-99 -.1000E 01 -.1000E 01  .0000E-99
  .0000E-99  .0000E-99 -.1000E 01  .0000E-99  .1000E 01  .0000E-99
  .0000E-99  .1000E 01  .0000E-99 -.0000E-99 -.0000E-99  .0000E-99
  .0000E-99  .1000E 01 -.1000E 01 -.0000E-99 -.0000E-99  .0000E-99
  .1000E 01  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99
```

TABLE 5.3.2 (Continued)

```
N-PORT REPRESENTATION


NUMBER OF PORTS    2
NUMBER OF NETWORK VOLTAGE DRIVERS    1
NUMBER OF NETWORK CURRENT DRIVERS    1
NUMBER OF CAPACITORS    3
NUMBER OF INDUCTORS    3


COEFFICIENT MATRICES OF ALGEBRAIC EQUATION

  PORT DRIVER COEFFICIENT MATRIX

  .4000E 00 -.2000E 00
 -.2000E 00  .6000E 00

  NETWORK VOLTAGE DRIVER COEFFICIENT MATRIX

 -.4000E 00
  .2000E 00

  CAPACITOR STATE-VOLTAGE COEFFICIENT MATRIX

 -.2000E 00  .0000E-99  .2000E 00
  .6000E 00  .0000E-99  .4000E 00

  NETWORK CURRENT DRIVER COEFFICIENT MATRIX

  .6000E 00
  .2000E 00

  INDUCTOR STATE-CURRENT COEFFICIENT MATRIX

 -.2000E 00 -.2000E 00  .0000E-99
 -.4000E 00 -.4000E 00  .0000E-99


COEFFICIENT MATRICES OF THE STATE DIFFERENTIAL EQUATION

  B MATRIX

  .2000E 00 -.6000E 00 -.2000E 00 -.2000E 00
 -.0000E-99 -.0000E-99  .0000E-99  .0000E-99
 -.2000E 00 -.4000E 00  .2000E 00 -.8000E 00
 -.2000E 00 -.4000E 00  .2000E 00  .2000E 00
 -.2000E 00 -.4000E 00  .2000E 00  .2000E 00
 -.0000E-99 -.0000E-99  .0000E-99  .0000E-99

  A MATRIX

 -.6000E 00  .0000E-99 -.4000E 00  .4000E 00  .4000E 00 -.1000E 01
  .0000E-99  .0000E-99  .0000E-99 -.1000E 01 -.1000E 01  .0000E-99
 -.4000E 00  .0000E-99 -.6000E 00 -.4000E 00  .6000E 00  .0000E-99
 -.4000E 00  .1000E 01  .4000E 00 -.4000E 00 -.4000E 00  .0000E-99
 -.4000E 00  .1000E 01 -.6000E 00 -.4000E 00 -.4000E 00  .0000E-99
  .1000E 01  .0000E-99  .0000E-99  .0000E-99  .0000E-99  .0000E-99
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CHAPTER VI

SUMMARY AND CONCLUSIONS

6.1 Summary. The motivation for this investigation has been the extension of work already accomplished in the development of mechanized methods for determining the multiport models of systems in general and electrical networks in particular. The investigation was based upon the use of the linear graph theory approach to network analysis and upon the preceding work of Lucky (2). Two main developments arose from the investigation, and two digital computer programs were written to illustrate the practical application for which the theory was intended.

The first and main development is the dividing of the large network into subnetworks and forming the required network model from a composite of the subnetwork models. This technique permits the modeling of a much larger network on a computer of a given size. Also, as a result of this technique, multiport devices represented by suitable terminal representations may be components of the network for which the n-port model is sought. In order to completely mechanize the procedure, three algorithms were developed. The first algorithm and basic to the study is the procedure of dividing the network into subnetworks. The other algorithms necessary are for forming the tree and cotree for each subnetwork and for producing the coefficient matrix of the fundamental cutset equations of each subnetwork. The

computer program written to demonstrate these techniques will accommodate a network with a maximum of 40 nodes, 20 voltage drivers, 20 current drivers, 100 resistors, and any number of multiterminal components. The latter components must be represented by a five- or fewer-terminal tree-representation.

The second development to come from this research is the mechanized determination of an n-port state-space model of a network containing energy-storage elements. Again, large networks are considered requiring the dividing of the network and forming the solution as outlined above. The computer program written to demonstrate this development will accommodate a network with a maximum of 40 nodes, 20 capacitors, 20 inductors, ten voltage drivers, ten current drivers, and 100 resistors.

A general restriction upon the networks to be considered is that some tree of the network must contain all of the voltage drivers and capacitors, and the cotree must contain all of the current drivers and inductors. In addition to this general restriction, sufficient conditions are given in Chapter II guaranteeing that a given network may be divided into sufficiently small subnetworks.

The n-port models of a number of example networks have been determined using the two computer programs. Two examples are included in this thesis to show the input data format and to illustrate the functioning of the programs by showing the printed computer output of the intermediate steps of the modeling process.

6.2 Conclusions. This investigation has demonstrated that the digital computer can be used to obtain the n-port model of large

networks whose elements are

(a) resistors,

(b) voltage drivers,

(c) current drivers, and

(d) passive, resistive multiport devices

by using a program which divides the network into parts to obtain the model. This investigation also has demonstrated that an n-port state-space model of a large network containing

(a) resistors,

(b) voltage drivers,

(c) current drivers,

(d) capacitors, and

(e) inductors

can be obtained by similar procedures. Only simple input data, basic to network analysis, is required; and the models are obtained without requiring any manual analysis.

Because of the basic similarity--that of dividing the network into subnetworks--between the method developed in this thesis and Kron's method of tearing, the following is given to present the differences between the two methods. The primary difference is in the forming of the subnetwork models and the forming of the torn network solutions; these are equivalent steps in the processes. The subnetwork models are multiport representations of the subnetworks; the torn network solutions of Kron's method are inverses of certain principal minors of the system matrix. Because some elements are removed from the network and do not appear in any of the network parts, the torn network solutions do not involve all of the network elements as do the

subnetwork models of the method developed in this thesis. Because of the form of the composite subport model, it is easy to obtain the desired multiport model for a network in terms of mixed network driver and port driver independent variables. Kron's method does not appear to lend itself easily to networks with mixed drivers. Finally, Kron's method does not provide for the inclusion of energy storage network elements and the formulation of the state-variable differential equations as developed in this work. Kron's method appears to be limited to, or at least is most applicable to, its intended use--solving large systems of linear algebraic equations.

6.3 Recommendations for Further Study. There are a number of possible extensions of this research and also one or two areas where the techniques of previous work and the techniques of this work may be combined to provide a more inclusive capability of network analysis.

It would be desirable to be able to include multiport components, along with one-port resistors, capacitors, inductors, and drivers in the networks for which the state-space model is determined. Including passive algebraic multiports does not appear difficult. However, an important extension would be to be able to include active components with energy storage; that is, multiport components represented by state-space models.

In order to accommodate ideal transformers as network components, it might be desirable to divide the network such that the transformers are embedded in the subnetworks and provide the necessary program derived from Lucky (2) to compute the subnetwork models.

It would be very desirable to be able to obtain n-port models of

networks which contain multiport components modeled by hybrid terminal characteristics since many mechanical and electromechanical components are represented by hybrid models. Thus, if the same approach were taken of dividing the network and treating multiport components as subnetworks, a hybrid composite model would result. This approach may be feasible and definitely represents a challenge. If some approach could be worked out, the resulting procedure would be of great aid in extending the procedures already available for the analysis of general electromechanical systems as well as other types of systems.

The procedures developed in this thesis obtain the n-port model similar to that of a Norton equivalent model; that is, the port currents are given as the dependent variables in terms of independent voltage and current driver variables. It may be desirable to obtain the dual of this model--a model similar to the Thevenin equivalent model--with the port voltages given as the dependent variables in terms of independent current and voltage driver variables. The model obtained in this thesis was chosen since it is easy to form the composite equations, Equations 2.2.5 and 5.1.5, by a simple algebraic addition of conductance matrix elements which represent paralleled subnetwork model elements. If the dual model is to be formulated, elements of resistance matrices must be combined which represent paralleled subnetwork model elements. This combining will not be a simple algebraic addition of elements, but the addition of certain inverses of submatrices of the subnetwork models. It may be desirable to investigate this problem and develop the procedures for formulating the composite Thevenin model of a network from the Thevenin models of its subnetworks.

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A P P E N D I X A

APPENDIX A

KRON'S METHOD OF TEARING

A technique for solving large systems of equations, known as the method of tearing, has been presented by Gabriel Kron.[1,2,3] The technique generally speeds up the solution time or makes possible the solution of systems too large to solve by direct means. The inversion of a system matrix can become a time consuming process even on very fast computers if the matrix is very large. It is estimated that the time required to invert an N x N matrix by the Gauss or Crout elimination processes is proportional to the cube of N.[4,5] By applying the method of tearing, a reduction in the solution time of the order of $2/n^2$ may be realized when the given system is divided or "torn" into n subsystems. This reduction is brought about because n subsystem matrices of

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[1] Gabriel Kron, "A Set of Principles to Interconnect the Solutions of Physical Systems," Journal of Applied Physics, XXIV (1953), pp. 965-980.

[2] Gabriel Kron, "A Method of Solving Very Large Physical Systems in Easy Stages," Institute of Radio Engineers Proceedings, XLII (1954), pp. 680-686.

[3] Gabriel Kron, "Inverting a 256 x 256 Matrix," Engineering, CLXXIX (1955), pp. 309-312.

[4] Alston S. Householder, Principles of Numberical Analysis (New York, 1953), pp. 82-83.

[5] V. N. Feddeeva, Computational Methods of Linear Algebra (New York, 1959), p. 65.

dimension N/n x N/n are inverted instead of the larger N x N given system matrix. The basic technique of the method of tearing is outlined in the following paragraph. Following this is a more detailed mathematical treatment.

Given a mathematical system of linear equations (or a physical system which is represented by)

$$\underline{I} = \underline{Y}\,\underline{E} \tag{A.1}$$

where $\underline{I}$ represents the vector of N unknown variables and $\underline{E}$ represents the vector of N unknown variables, it is desired to determine the solution

$$\underline{E} = \underline{Z}\,\underline{I} \tag{A.2}$$

where $\underline{Z}$, the solution matrix, is the inverse of $\underline{Y}$, the system matrix. The method of tearing requires that a network or circuit model be created or synthesized, if one does not already exist, which is represented by the system equation, Equation A.1. This network model is divided into several subnetworks by the removal of arbitrary branches which are called tie branches. The subsystem equations are then written and solved. These solution equations are then used to establish a system solution network connected together by the previously removed tie branches. The solution equation of the given system is determined by solving for or eliminating the constraints which appear where the tie branches have been replaced in the solution network. The following paragraphs give a general mathematical treatment of the steps outlined above; refer to Chapter 11 of Braae.[6]

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[6] R. Braae, Matrix Algebra for Electrical Engineers (Reading, Massachusetts, 1963), pp. 135-142.

Assume that the system equation, Equation A.1, is given and that an electrical network has been created which is represented by this equation. The vector $\underline{I}$ could represent the N currents of ideal drivers connected between each of the N network nodes and the reference node of the network. The vector $\underline{E}$ then would represent the N node-to-reference unknown voltage.

The network is divided into subnetworks by removing the tie branches which connect across arbitrary division lines which divide the network into n subnetworks. Assume that p branches are removed. The torn system matrix $\underline{Y}'$ is formed by deleting the removed tie branch admittance values from the system matrix $\underline{Y}$. This new matrix $\underline{Y}'$ is composed of N submatrices which are square and lie on the main diagonal and zero submatrices elsewhere.

To compensate for the removal of the tie branches, additional currents must be applied to the nodes from which the branches were removed in order that the torn network still represent the original system. For example, consider the q-th branch which is removed from its place between node i and node j. A current, $-I_{ij}$, must be "injected" into node i and a current I_{ij} "injected" into node j, where $I_{ij} = I_q$ is the current which, before tearing, flowed in branch q from node i to node j. This "injection" of currents to compensate for the removed branches may be accomplished mathematically by defining the total driver currents as

$$\underline{I}_{total} = \underline{I} + \underline{K}\,\underline{I}_{tb} \qquad (A.3)$$

where $\underline{I}$ is the current defined in Equation A.1, $\underline{I}_{tb}$ is the vector of tie branch currents, and $\underline{K}$ is an incidence matrix which has the general

form

$$\underline{K} = \begin{bmatrix} \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & -1 & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & +1 & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \end{bmatrix} \begin{matrix} \\ \\ \text{i-th row} \\ \\ \text{j-th row} \\ \\ \end{matrix} \qquad \text{(A.4)}$$

q-th column

where the q-th branch is removed from between node i and node j.

Note now that the current, which existed before tearing, from node i to node j produced a voltage difference $E_i - E_j = Z_q I_q$. The equation

$$\underline{K}^T \underline{E} = - \underline{Z}_{tb} \underline{I}_{tb} \qquad \text{(A.5)}$$

gives the relationship between the node voltages associated with the tie branches and the tie branch currents where $\underline{K}^T$ is the transpose of $\underline{K}$ and $\underline{Z}_{tb}$ is the diagonal matrix whose elements are the impedance values of the removed tie branches.

The torn system equation

$$\underline{I} + \underline{K} \underline{I}_{tb} = \underline{Y}' \underline{E} \qquad \text{(A.6)}$$

is solved for $\underline{E}$

$$\underline{E} = \underline{Z}' [\underline{I} + \underline{K} \underline{I}_{tb}] \qquad \text{(A.7)}$$

where $\underline{Z}' = \underline{Y}'^{-1}$. $\underline{Z}'$ is determined by forming the inverses of the submatrices on the main diagonal of $\underline{Y}'$ (a process much easier than

forming the inverse of the complete system matrix $\underline{Y}$. The solution of $\underline{E}$ in Equation A.7 is not explicit in terms of $\underline{I}$ alone, but it also contains $\underline{I}_{tb}$, the unknown tie branch currents. These unknowns are eliminated as follows. Equation A.6 is premultiplied by $\underline{K}^T$ and the result equated to Equation A.5, and an expression for $\underline{I}_{tb}$ is obtained:

$$\underline{I}_{tb} = -[\underline{Z}_{tb} + \underline{K}^T \underline{Z}' \underline{K}]^{-1} \underline{K}^T \underline{Z}' \underline{I} \qquad (A.8)$$

The solution equation, $\underline{E}$ given explicitly now in terms of $\underline{I}$, is

$$\underline{E} = \underline{Z} \underline{I} \qquad (A.9)$$

where the solution matrix $\underline{Z}$, the inverse of the system matrix $\underline{Y}$ is

$$\underline{Z} = \underline{Z}' - \underline{Z}' \underline{K}[\underline{Z}_{tb} + \underline{K}^T \underline{Z}' \underline{K}]^{-1} \underline{K}^T \underline{Z}' \qquad (A.10)$$

In summary, Kron's method of tearing may be outlined as follows: (1) representation of the physical system or mathematical system of equations by an equivalent network, (2) removing r elements of the network and forming the torn admittance matrix $\underline{Y}'$, (3) inverting $\underline{Y}'$ by inverting its main diagonal submatrices (all other submatrices are zero), (4) writing the incidence matrix $\underline{K}$, which describes the original connections of the removed tie branches, and the tie branch matrix $\underline{Z}_{tb}$, (5) inverting the r x r matrix $[\underline{Z}_{tb} - \underline{K}^T \underline{Z}' \underline{K}]$, and (6) forming the desired solution matrix $\underline{Z}$ given by Equation A.10.

A P P E N D I X B

APPENDIX B

FORTRAN VARIABLE NAMES AND DEFINITIONS

The following is a partial list of FORTRAN names used in Programs I and II and their definitions. Dimensioned variables--program lists, arrays, vectors, and matrices--are indicated by NAME(I) and NAME(I, J).

A(I, J) -- The matrix $\underline{A}$ defined by Equation 5.1.12.

B(I, J) -- The matrix $\underline{B}$ defined by Equation 5.1.12.

BOTNOD -- The second node located to which a tree element is incident.

BRANCH -- The tree element of the cutset.

CONDUC(I) -- The list of the two-terminal network conductance values.

CRDSET(I) -- The list of elements belonging to the subnetwork cotree.

CUTCRD -- A cotree element belonging to the cutset.

CUTSET(I) -- The set of cotree elements of a cutset.

D(I, J) -- Phase 4. The matrix $\underline{D}_{VD}$ defined by Equation 3.4.13.

D(I, J) -- Phase 6. The matrix $\underline{D}$ defined by Equations 2.2.2 and 2.2.5.

DIRECT(I, J) -- The array defined in Definition 4.3.2.

G(I, J) -- Phase 1. The matrix $\underline{G}$ defined by Equation 4.2.1.

G(I, J) -- Phase 4. The matrix $\underline{G}_{VD}$ defined by Equation 3.4.12

G(I, J) -- Phase 5. The matrix $\underline{G}$ defined by Equations 2.2.2 and 2.2.5.

G22INV(I, J) -- A dimensioned area of memory of Phases 5 and 6 used to temporarily store $\underline{G}_{VD}$ and $\underline{D}_{VD}$ matrices read in from tape before moving the elements to permanent locations G and D. Also used in computation of G_{22}^{-1}.

GCOTRE(I) -- The list of conductances of the cotree conductance elements in the order in which the elements appear in the cutset equations.

GTRANS(I, J) -- The matrix $\underline{G}_{VD}$ defined by Equation 4.2.5.

GTREE(I) -- The list of conductances of the tree conductance elements in the order in which the elements appear in the cutset equations.

IELEM(I) -- The list of elements added to the subnetwork connection array since the last size determination was made.

INODE(I) -- A temporary list equivalent to the list NODE(I) of Phase 1.

IROW(I) -- The vector used to store the elements of a row of the matrix $\underline{S}$ as they are computed in Phase 2.

ISUBPT(I) -- A temporary list equivalent to the list SBNWPT(I).

KNODE(I) -- A list with an entry for each node of the network. A number equal to the entry number indicates that node is to be a part of the subnetwork being formed if the subgroup of elements of IELEM list can be added to the subnetwork.

KVERTX(I) -- A temporary list equivalent to the list VERTEX(I).

LIST(I) -- A list with an entry for each node of the network. The number in each entry indicates the position that the SRBRLT listed elements appear in the composite subnetwork model.

LISTC(I) -- A list with an entry for each capacitor in the subnetwork. The entry position corresponds to the element position in the cutset equations. The number in the entry is the position of the capacitor in the composite subnetwork model.

LISTE(I) -- A list of subnetwork voltage driver elements defined similarly to LISTC(I) above.

LISTJ(I) -- A list of subnetwork current driver elements defined similarly to LISTC(I) above.

LISTL(I) -- A list of subnetwork inductor elements defined similarly to LISTC(I) above.

LTCAPT -- The element number of the capacitor with the largest number.

LTCTSR -- The element number of the current driver with the largest number.

LTINDT -- The element number of the inductor with the largest number.

MAXDEG -- The maximum number of two-terminal elements incident to any node of the network.

MAXSUB -- The maximum number of two-terminal elements incident to any node of the subnetwork.

MINBRS -- The minimum number of tree elements to be in a subnetwork.

MINCDS -- The minimum number of cotree elements to be in a subnetwork.

MNNWVS -- Equal to NOVTSR + NOCTSR + NOPNDS - 1.

MONODE -- The number of nodes minus one.

MRNODE(I) -- A list with an entry for each node of the network. A number in an entry equal to the entry position indicates the node is included in at least one subnetwork, that is, is an associated node.

MTCPLT(I) -- A list with an entry for each node of the network. A number in an entry equal to the entry position indicates the node is a terminal of at least one multiterminal component.

MTCTPT(I) -- A list of nodes which are multiterminal component terminals.

NCPPIN -- Equal to NOCAPS + NOINDS.

NCPSP1 -- Equal to NOCAPS + 1.

NNVSP1 -- Equal to NOVTSR + 1.

NOCAPS -- Number of capacitors of the network.

NOCDST -- The number of elements in the cotree.

NOCOND -- The number of conductance elements of the network.

NOCTSR -- The number of current drivers of the network.

NODE(I) -- Phase 1. A list with an entry for each node of the network. A number in each entry equal to the entry position indicates the node is included in the subnetwork but does not have all of its incident elements in the subnetwork.

NODE(I) -- Phase 3. A list of numbers of nodes which make up the super-node of the cutset.

NOELEM -- The number of network elements contained in the subnetwork.

NOGCOT -- The number of conductances in the subnetwork tree.

NOINDS -- Number of inductors of the network.

NOMTCT -- The number of multiterminal components.

NONODE -- The number of nodes of the network.

NONWEL -- The number of two-terminal elements of the network.

NONWVS -- The number of network voltage drivers.

NOPNDS -- The number of ports, or port nodes, of the desired network model.

NOPNP1 -- Equal to NOPNDS + 1.

NORMNG -- The number of network voltage drivers not yet used in defining x-nodes.

NOSBNW -- The number of subnetworks.

NOSNCS -- The number of current drivers and inductors in a subnetwork.

NOSNVS -- The number of voltage drivers, both network and subport drivers and capacitors, in a subnetwork.

NOTERM -- The number of terminals of a multiport component.

NOTRST -- The number of elements in the tree.

NOVTSR -- The number of voltage drivers of the network.

NOVTXS -- The number of nodes of a subnetwork.

NOXNDS -- The number of x-nodes not yet embedded in a subnetwork.

NPNPCP -- Equal to NOPNDS + NOCAPS.

NPNPPN -- Equal to two times NOPNPN.

NPNPVS -- Equal to NOPNDS + NOVTSR.

NRELEM -- The number of elements contained in the IELEM list.

NRCAPS -- Number of capacitors of a subnetwork.

NRCTSR -- Number of current drivers of a subnetwork.

NRINDS -- Number of inductors of a subnetwork.

NRVTSR -- Number of voltage drivers of a subnetwork.

NRSBNW -- Equal to NOSBNW + NOMTCT.

NSBPP1 -- Equal to NOSBPT + 1.

NSBPT1 -- Equal to NOSBPT + 1.

NSBPVS -- Equal to NOSBPT + NOVTSR.

NSPVS1 -- Equal to NOSBPT + NOVTSR + 1.

NTOTDV -- Equal to NOVTSR + NOCTSR.

NTWKCN(I, J) -- The network connection array defined by Definition 4.3.1.

ORIENT(I) -- The network element orientation list defined by Definition 4.3.3.

PORT(I) -- A list with an entry for each node of the network. A number in an entry equal to the entry position indicates the node is a subport of at least one subnetwork.

PORTND(I) -- The list of nodes which are ports of the desired representation.

S(I, J) -- The cutset equation coefficient matrix S.

SBNWCN(I, J) -- The subnetwork connection array. See definition for NTWKCN.

SBNWNO -- Subnetwork number.

SBNWPT(I) -- A list with an entry for each node of the network. A number equal to the entry number indicates that the node is a subport of the subnetwork.

SNCSLT(I) -- A list with an entry for each current driver in the subnetwork. The entry position corresponds to the current driver position in the cutset equations. The

number in the entry is the position of the current driver in the composite subnetwork representation. (Inductors are considered current drivers for this list.)

SNVSLT(I) -- A list with an entry for each voltage driver in the subnetwork. The entry position corresponds to the voltage driver position in the cutset equations. The number in the entry is the position of the voltage driver in the composite subnetwork representation. (Capacitors are considered voltage drivers for this list.)

SRBRLT(I) -- A list with an entry for each possible subnetwork voltage driver, both network and subport drivers. A number in an entry equal to the entry position indicates the voltage driver is a subnetwork voltage driver.

SUBNOD(I) -- A list of node numbers whose position in the list indicates the position of the nodes in the reduced subnetwork connection array.

TOPNOD -- The first node located to which the tree element is incident.

TRESET(I) -- The list of elements belonging to the subnetwork tree.

VERTEX(I) -- A list with an entry for each node of the network. A number equal to the entry indicates that the node is in the subnetwork.

XNDLST(I) -- A list with an entry for each node of the network. A number in an entry equal to the entry position

indicates the node is an x-node.

XNDREF(I) -- A list with an entry for each node of the network. The number in an entry is the number of the other node to which the voltage driver is incident which defines the x-node corresponding to the entry position.

XNDSRC(I) -- A list with an entry for each node of the network. The number in an entry is the number of the voltage driver element which defines the x-node corresponding to the entry.

XNODE(I) -- A list with an entry for each node of the network. A number in an entry equal to the entry position indicates the node is an x-node.

ZERORW -- A row of the subnetwork connection array (before the array is reduced) which contains no non-zero elements. This represents a network node not contained in the subnetwork.

A P P E N D I X C

APPENDIX C

FLOW CHARTS FOR PROGRAM I

Flow charts for the six phases of Program I are contained in the following Figures C-1 through C-6. In these charts the diamond-shaped symbol signifies a decision step and is used for the logical if statement. When the if statement is true, the logic flow is out the (right or left) side point of the diamond symbol; if the statement is false, the flow is out the lower point of the symbol.

Table C-1 gives a listing of the tape read/write statements which are referenced in the flow charts by number. A number of variables are written on tape as one FORTRAN name and later read from the tape and placed in memory under a different FORTRAN name. This is indicated by a variation in the list notation, for example, Statement 12, Table C-1:

12	3,4	5	5	GTRANS/G — G22INV

indicates that the variables GTRANS, read onto tape 5 in phase 3, and G, read onto tape 5 in phase 4, occupy the same relative position in the two write statements and are read out in phase 5 into the FORTRAN name G22INV. This is done to better utilize computer memory.

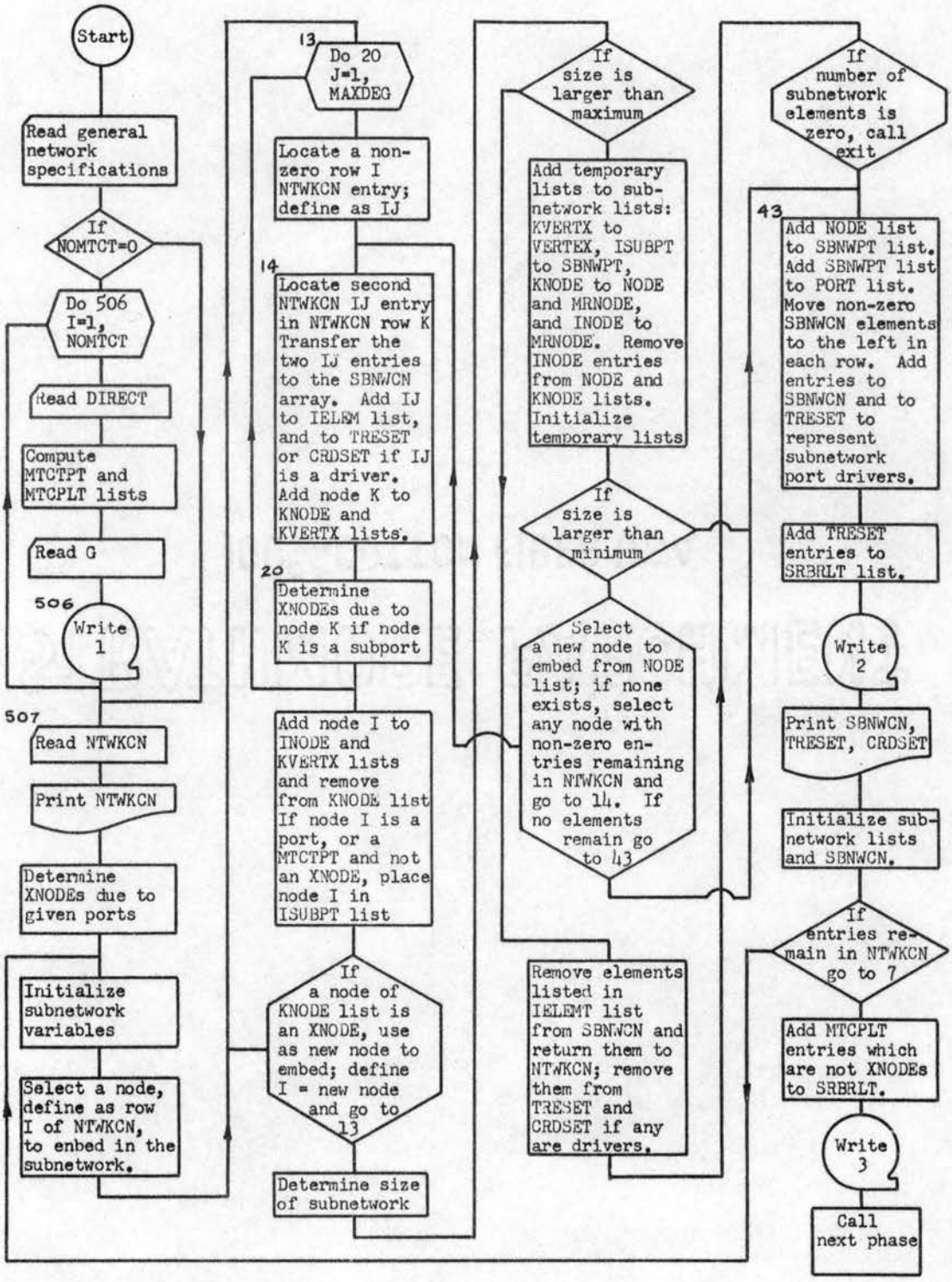

Figure C-1. Flow Chart for Phase 1.

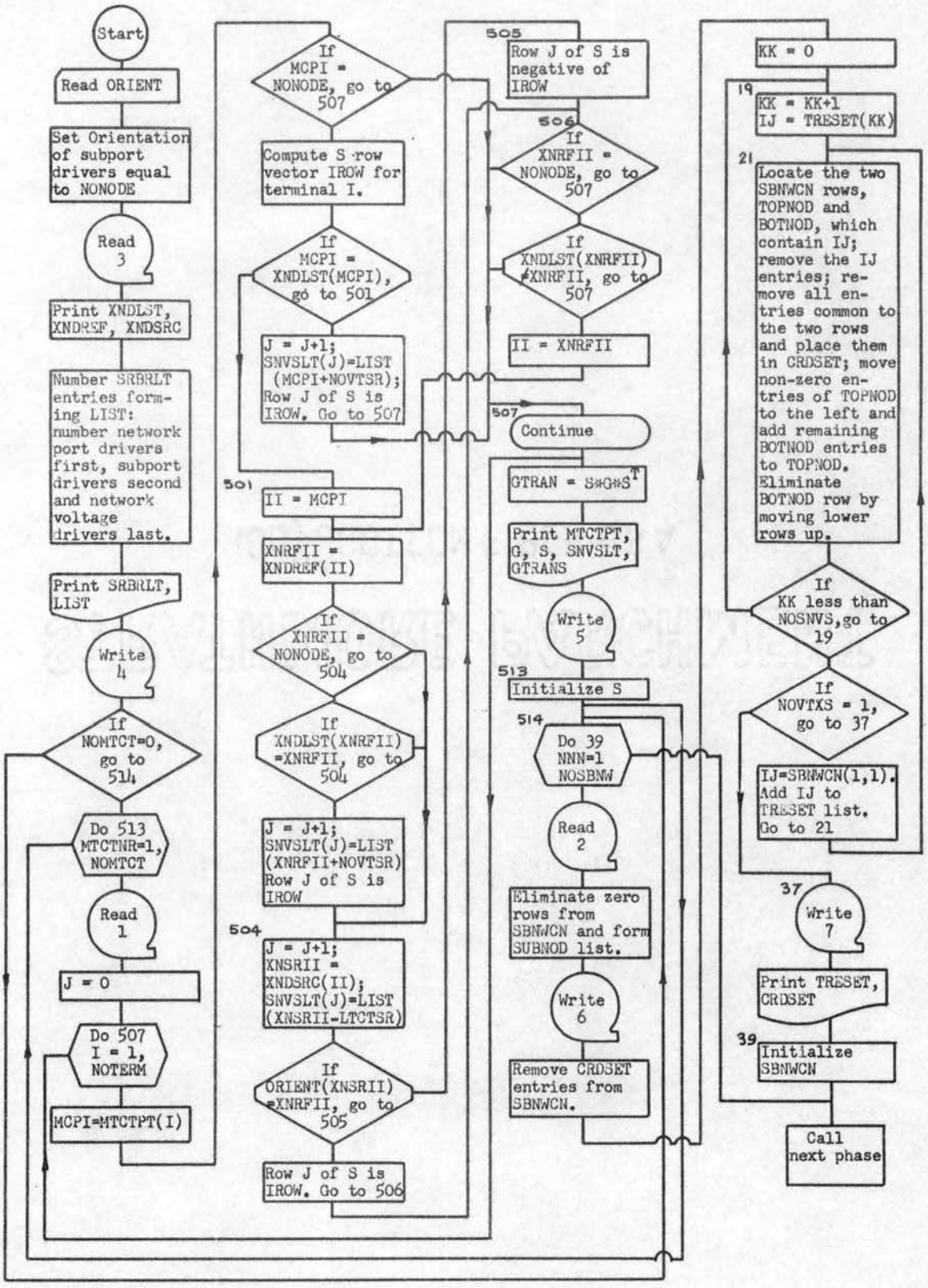

Figure C-2. Flow Chart for Phase 2.

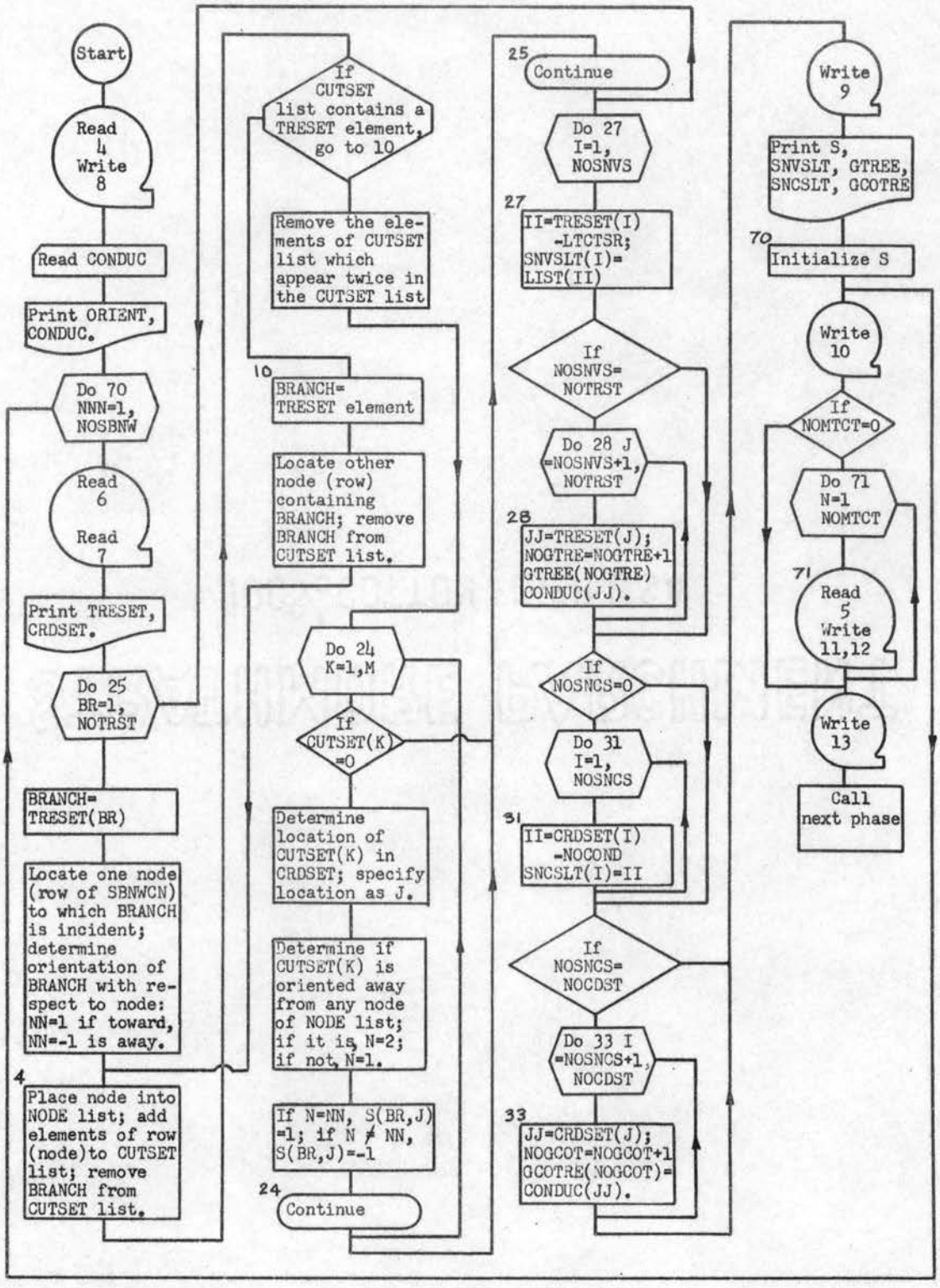

Figure C-3. Flow Chart for Phase 3.

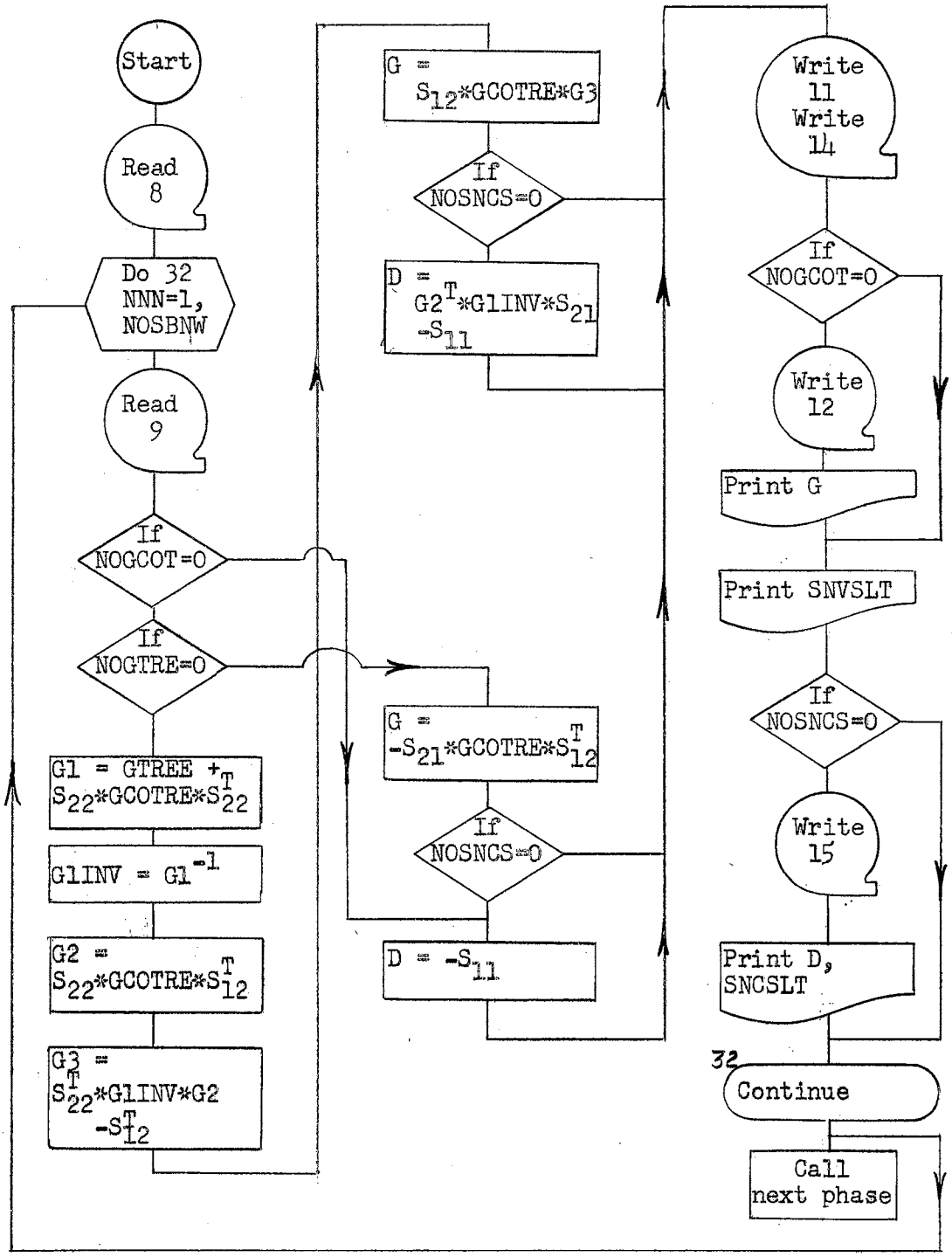

Figure C-4. Flow Chart for Phase 4.

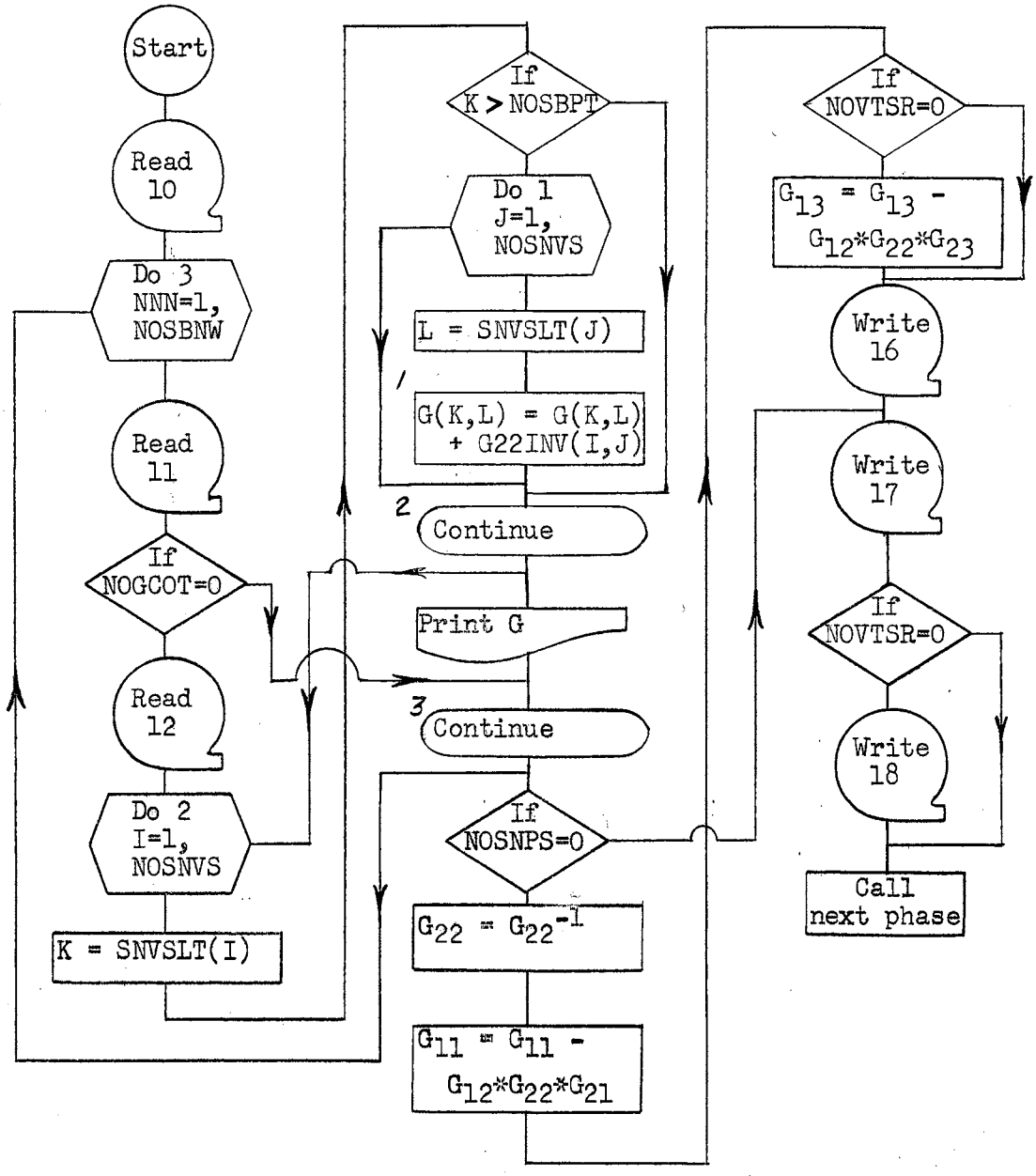

Figure C-5. Flow Chart for Phase 5

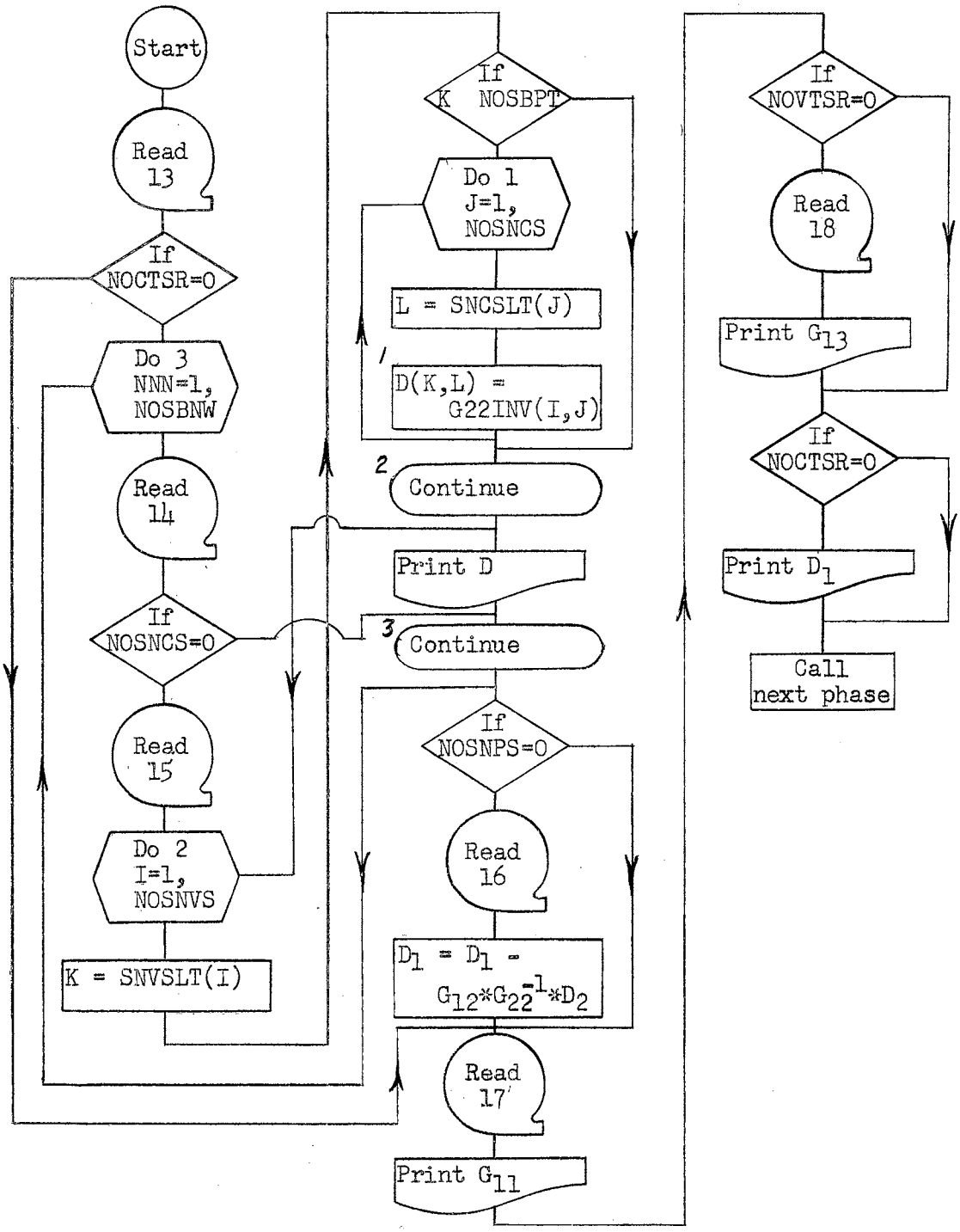

Figure C-6. Flow Chart for Phase 6.

TABLE C-1

READ/WRITE STATEMENT LISTING

Read/Write Statement	Write Phase	Read Phase	Tape Unit	FORTRAN Variables
1	1	2	5	MTCTNO, NOTERM, MTCTPT, DIRECT, G
2	1	2	4	SBNWNO, NOTRST, NOCDST, MAXSUB, SBNWCN, TRESET, CRDSET
3	1	2	6	NONODE, NOVTSR, NOCTSR, NOPNDS, NONWEL, NOSBNW, MNNWVS, NOMTCT, LTCTSR, XNDLST, XNDREF, XNDSRC, SRBRLT, PORTND, NOCOND
4	2	3	6	NONODE, NOVTSR, NOCTSR, NONWEL, NOPNDS, NOCOND, LTCTSR, NOSBNW, MNNWVS, NONWVS, NOMTCT, ORIENT, LIST
5	2	3	6	MTCTNO, NOSNVS, SNVSLT, GTRANS - G
6	2	3	5	SBNWNO, NOVTXS, MAXSUB, SBNWCN, SUBNOD
7	2	3	5	SBNWNO, NOTRST, NOCDST, NOSNVS, NOSNCS, TRESET, CRDSET
8	3	4	4	NONODE, NOVTSR, NOCTSR, NONWEL, NOPNDS, NOCOND, LTCTSR, NOSBNW, MNNWVS, NONWVS
9	3	4	4	SBNWNO, NOTRST, NOCDST, NOGTRE, NOGCOT, NOSNVS, NOSNCS, S, GTREE, GCOTRE, SNVSLT, SNCSLT
10	3	5	5	NRSBNW — NOSBNW, NOVTSR, NOCTSR, NONWVS, NOPNDS, NOSBPT, NSBPVS, NSBPT1, NOSNPS
11	3,4	5	5	MTCTNO/SBNWNO—SBNWNO, NOSNVS, NOGCOT
12	3,4	5	5	GTRANS/G—G22INV, SNVSLT
13	3	6	6	NOSBNW, NOVTSR, NOCTSR, NONWVS, NOPNDS, NOSBPT, NSBPVS, NSBPT1, NOSNPS
14	4	6	6	SBNWNO, NOSNVS, NOSNCS
15	4	6	6	D—G22INV, SNVSLT, SNCSLT
16	5	6	5	G_{12}—G12, G_{22}^{-1}—G22INV
17	5	6	5	G_{11}—G12
18	5	6	5	G_{13}—G12

A P P E N D I X D

APPENDIX D

FLOW CHARTS FOR PROGRAM II

Fow charts for the thirteen phases of Program II are contained in Figures D-1 through D-13. In these charts the diamond-shaped symbol signifies a decision step and is used for the logical if statement. When the if statement is true, the logic flow is out the (right or left) side point of the diamond symbol; if the statement is false, the flow is out the lower point of the symbol.

Table D-1 gives a listing of the tape read/write statements which are referenced in the flow charts by number. A number of variables are written on tape as one FORTRAN name and later read from the tape and placed in memory under a different FORTRAN name. This is indicated by a variation in the list notation, for example, Statement 16, Table D-1:

16	5	7	7	$G_{22}^{-1}*G_{21}$ — GG21

indicates that the variable product $G_{22}^{-1}*G_{21}$, read onto tape 7 in phase 5, is read out in phase 7 into the FORTRAN name GG21. This is done to better utilize computer memory.

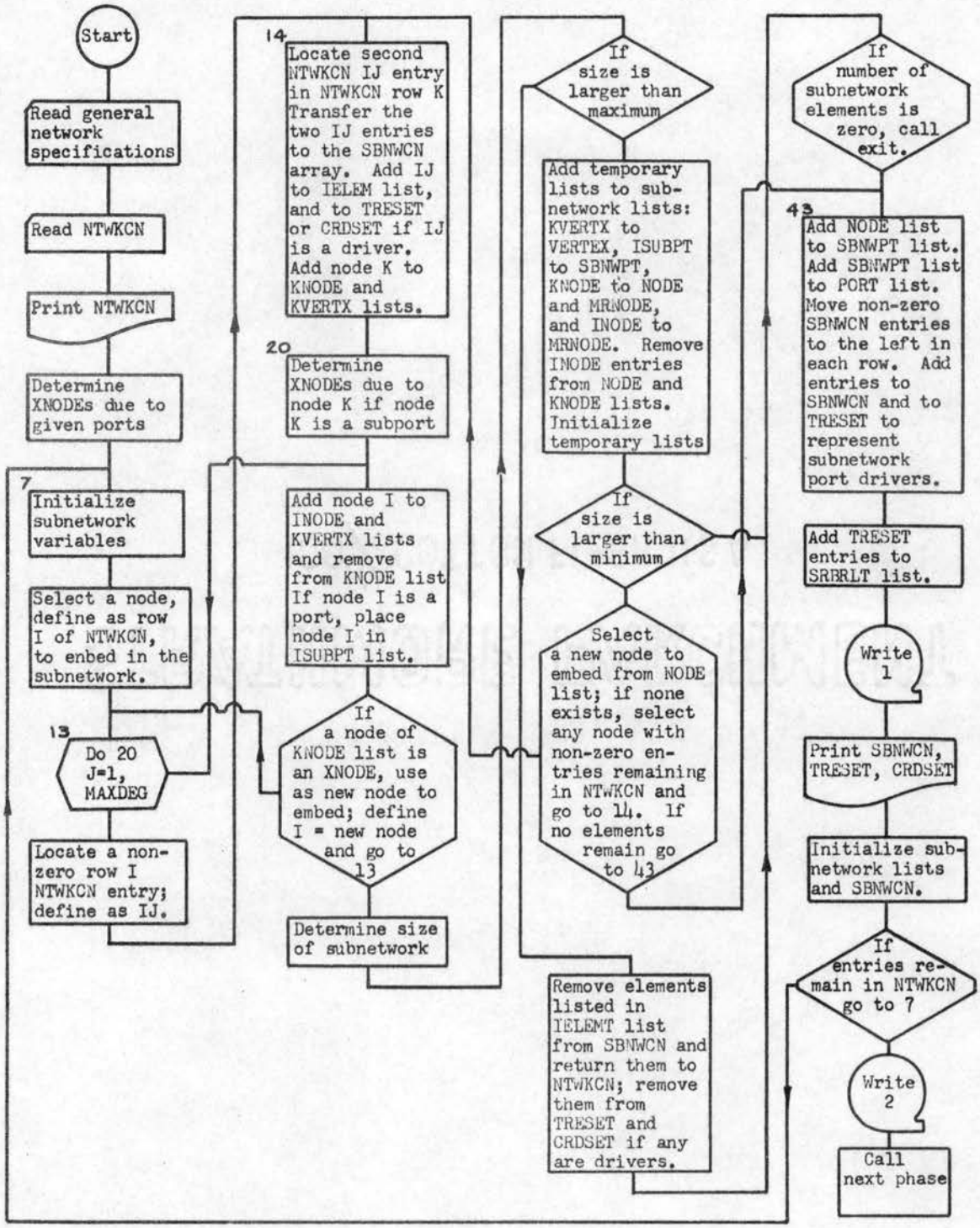

Figure D-1. Flow Chart for Phase 1.

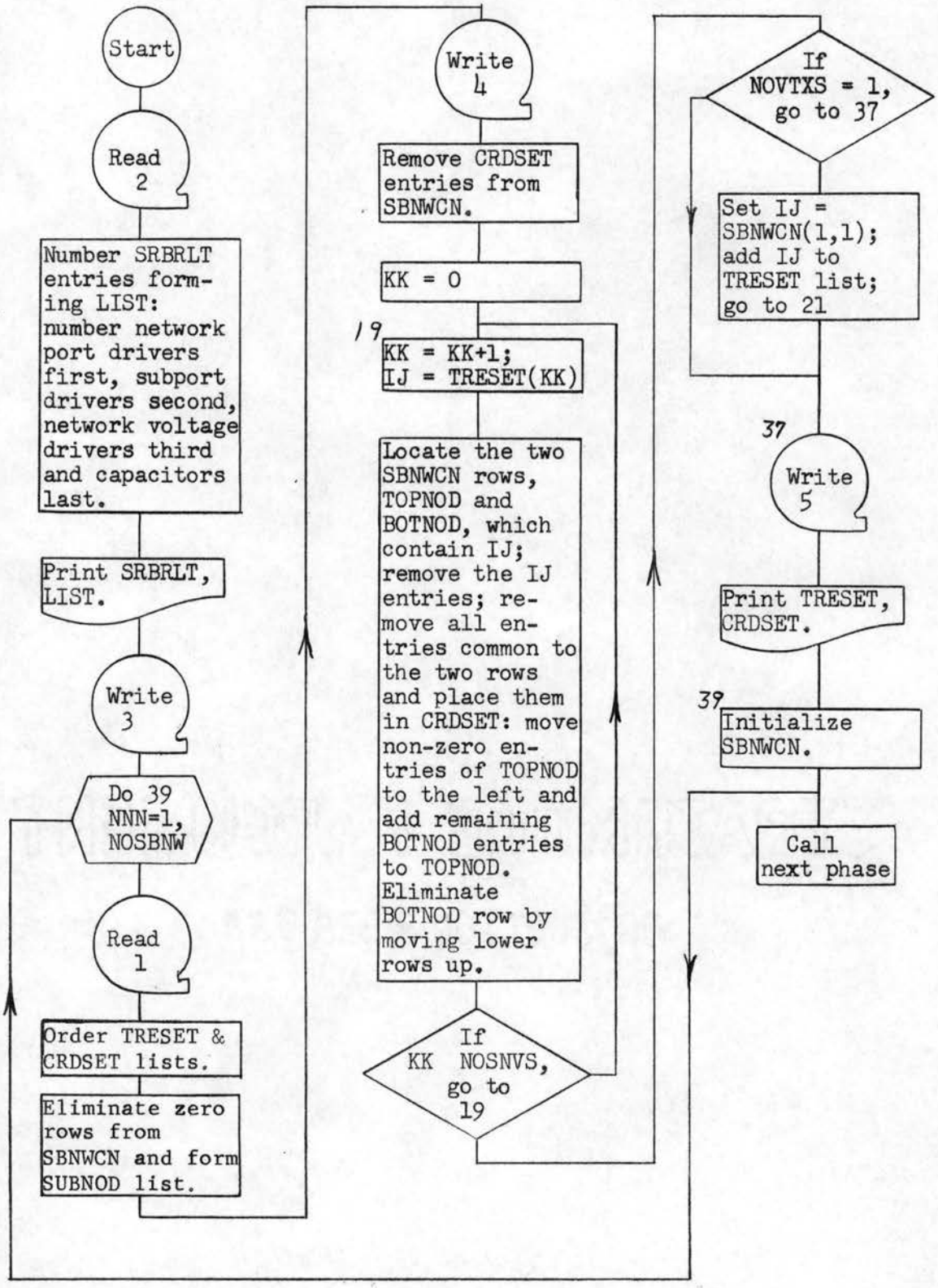

Figure D-2. Flow Chart for Phase 2.

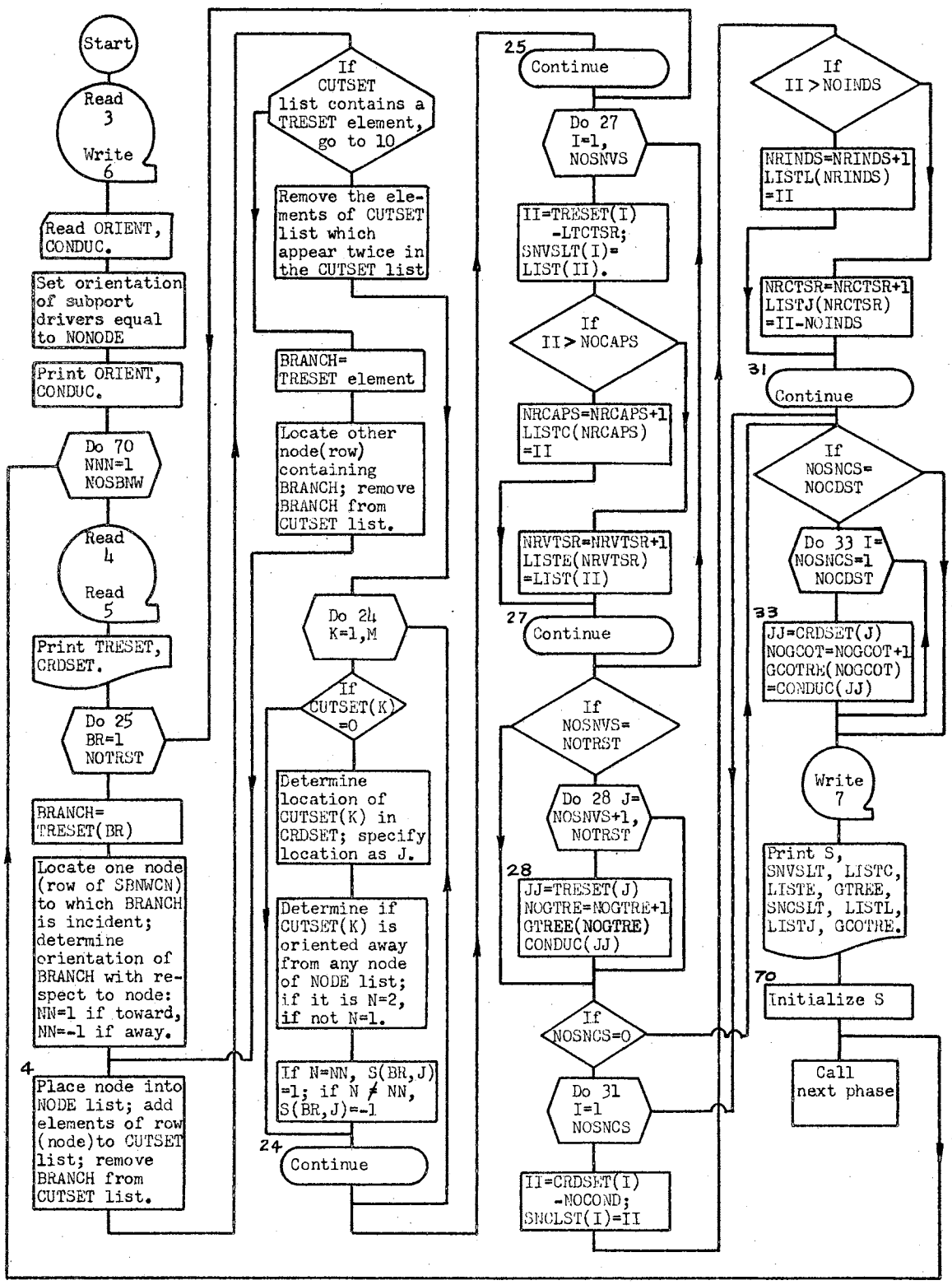

Figure D-3. Flow Chart for Phase 3.

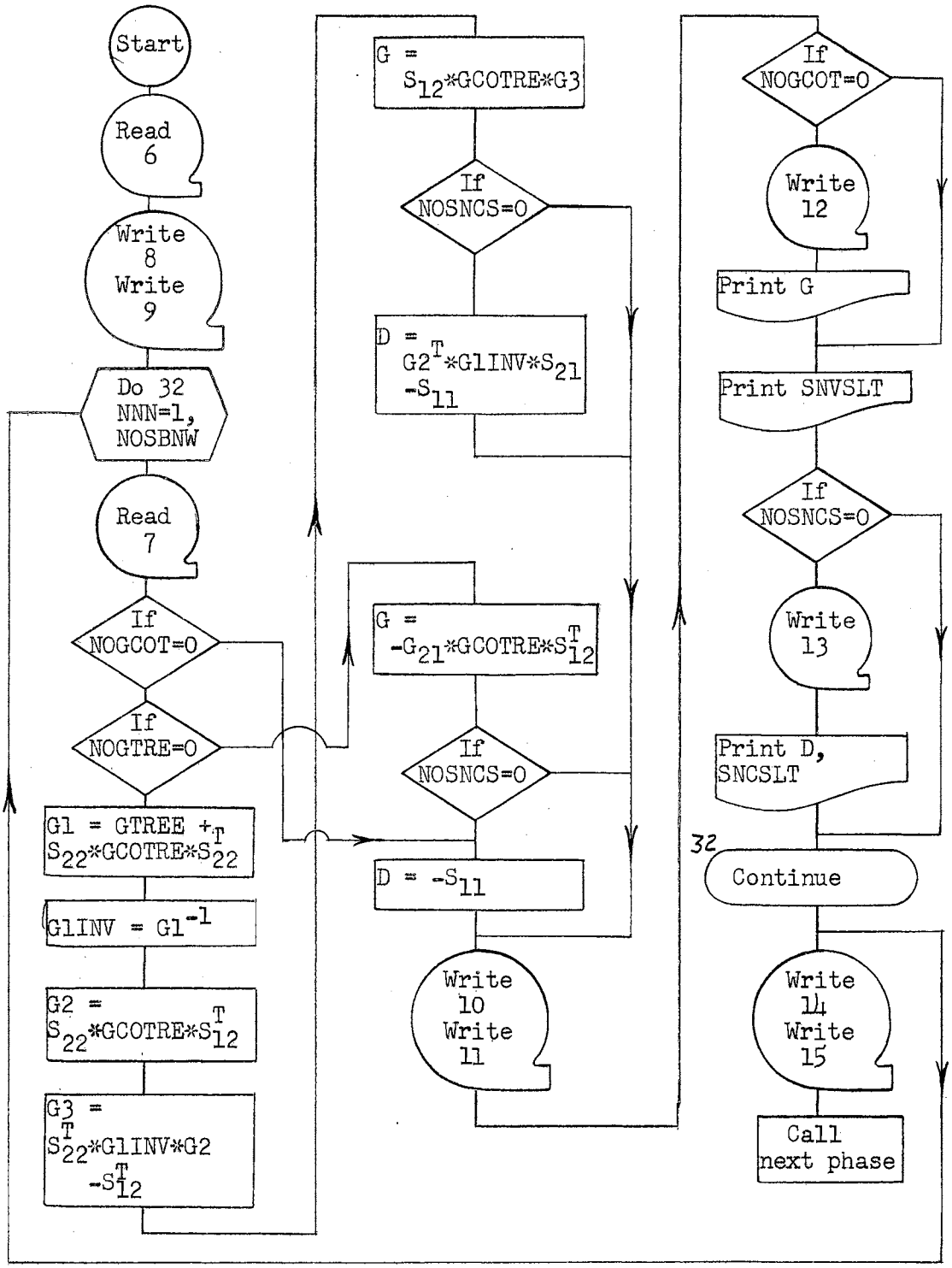

Figure D-4. Flow Chart for Phase 4.

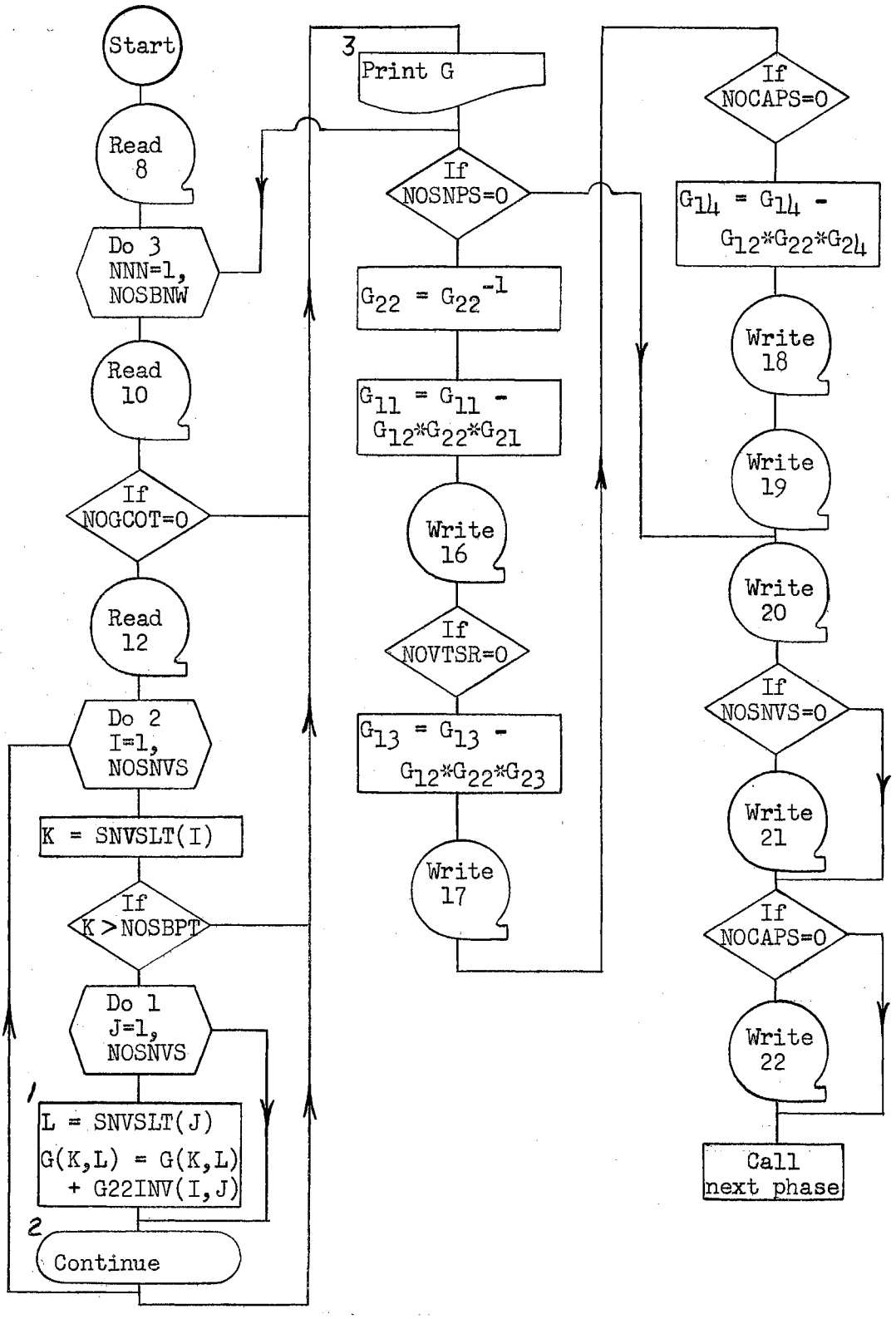

Figure D-5. Flow Chart for Phase 5.

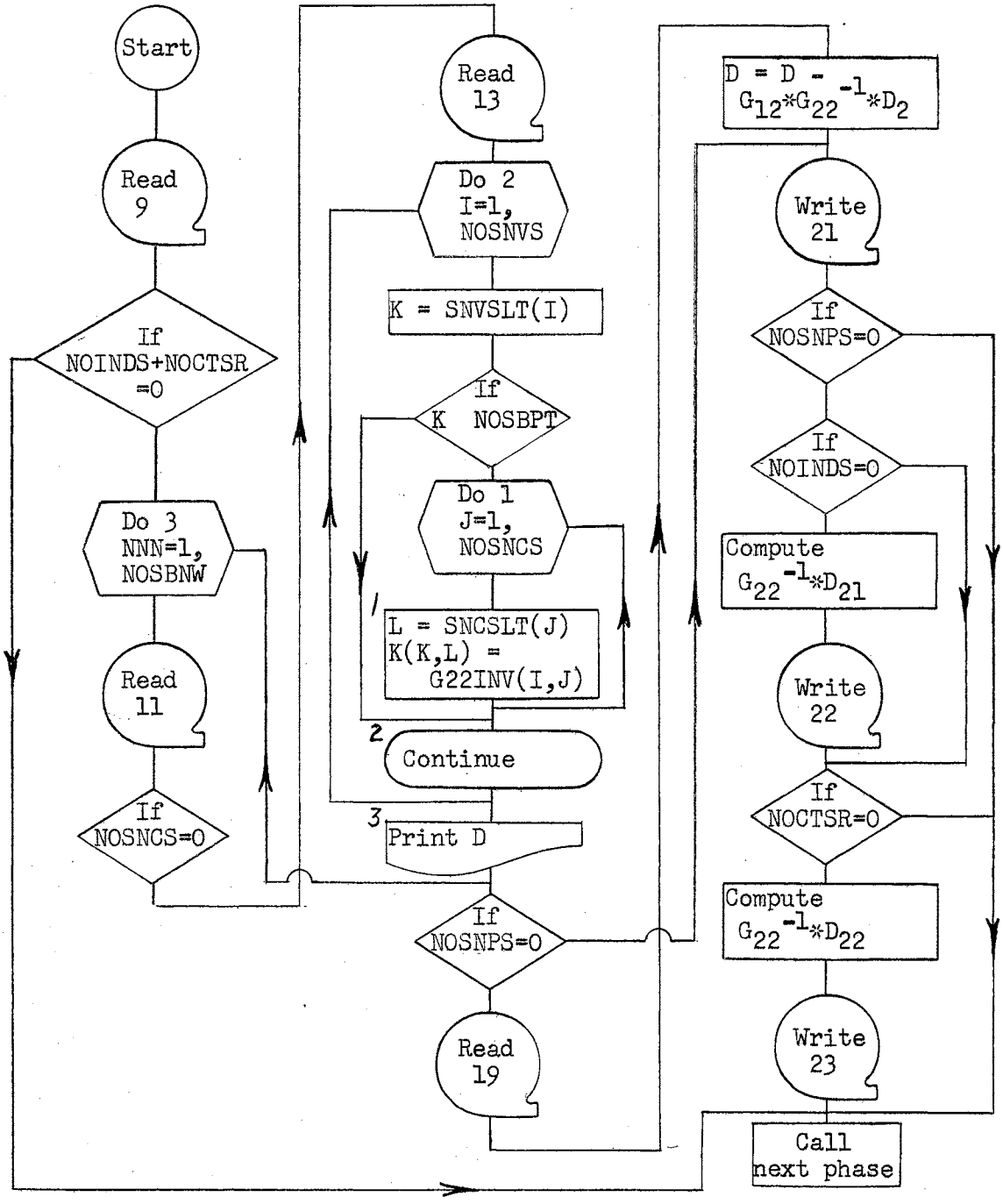

Figure D-6. Flow Chart for Phase 6.

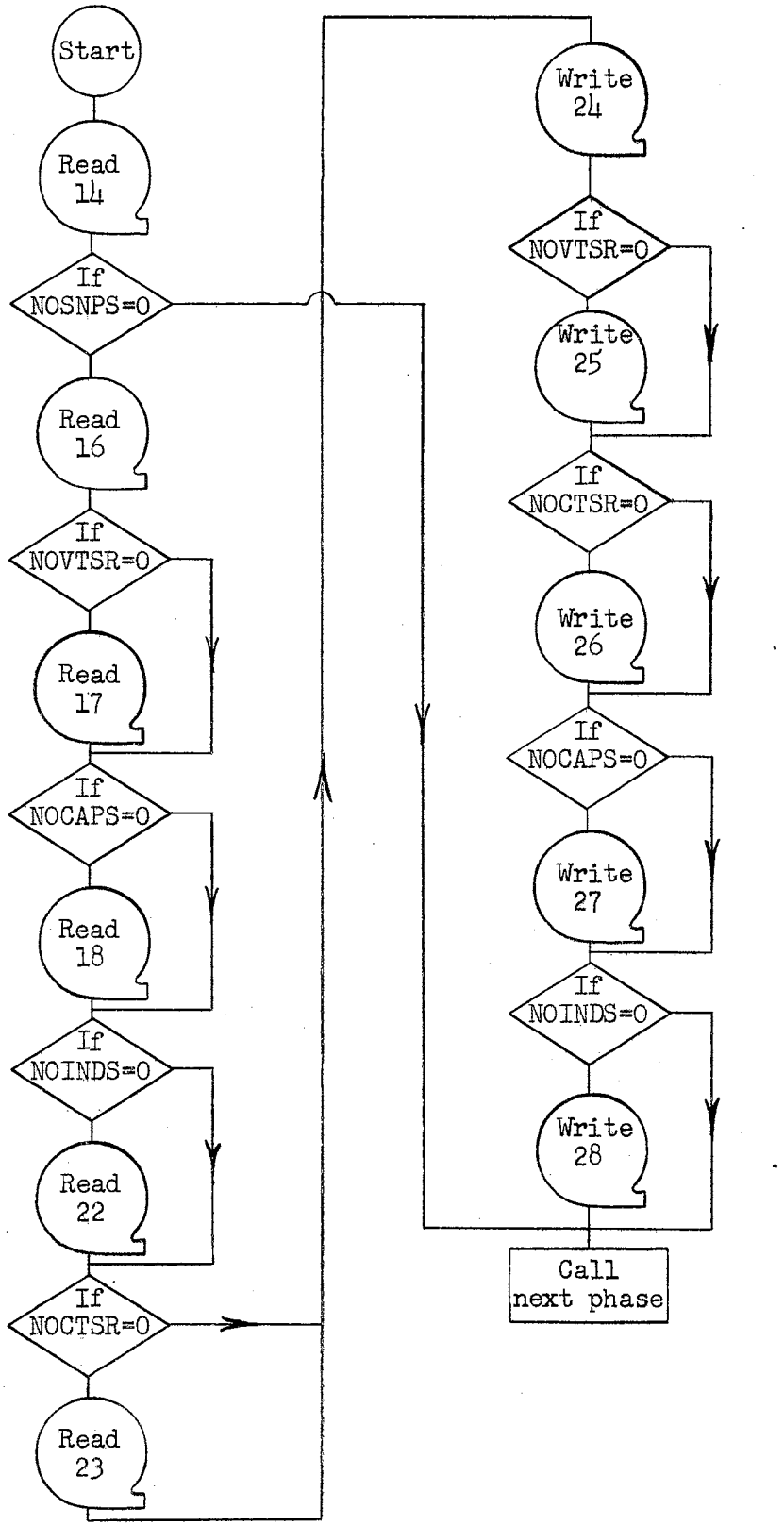

Figure D-7. Flow Chart for Phase 7.

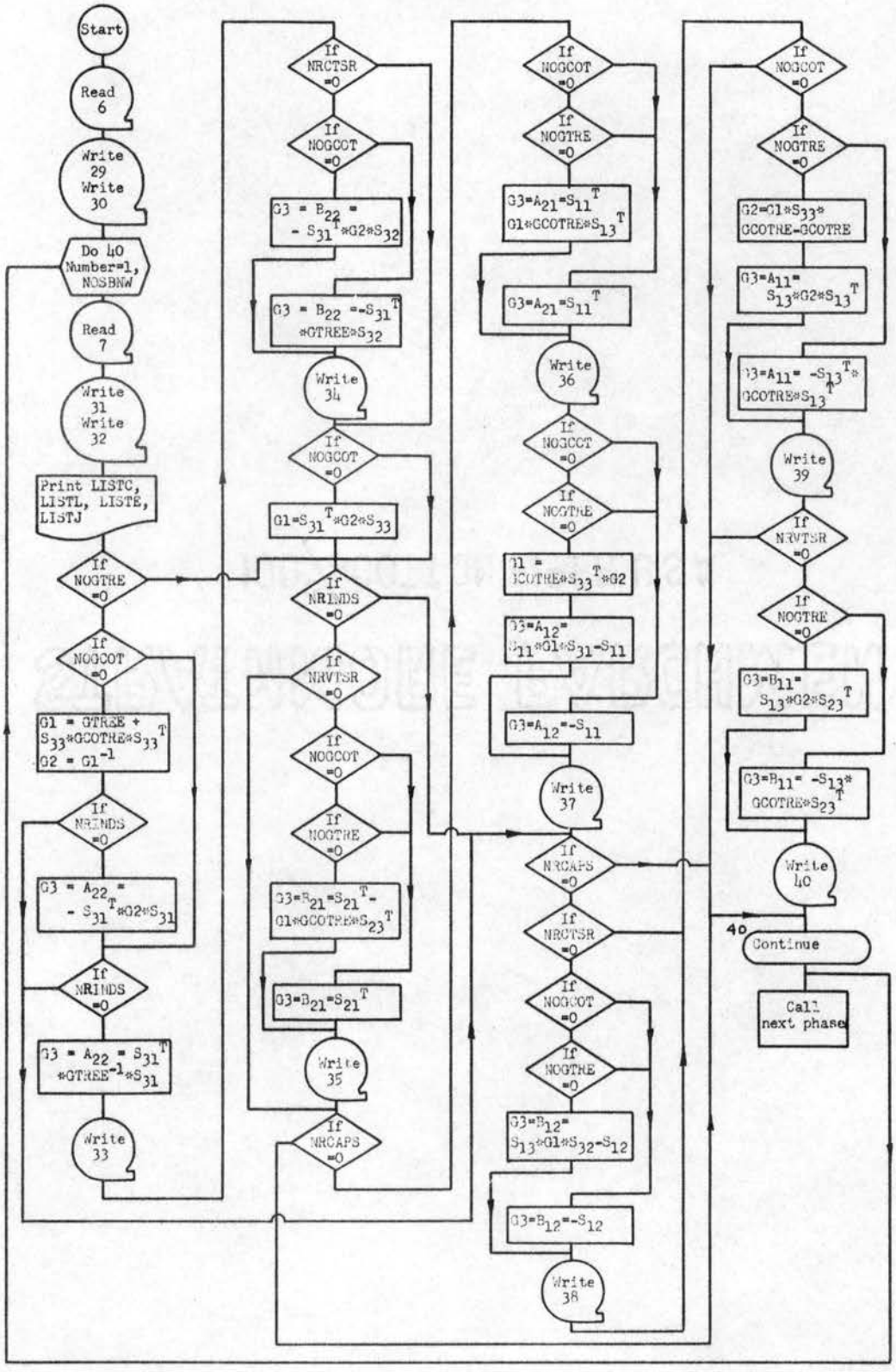

Figure D-8. Flow Chart for Phase 8.

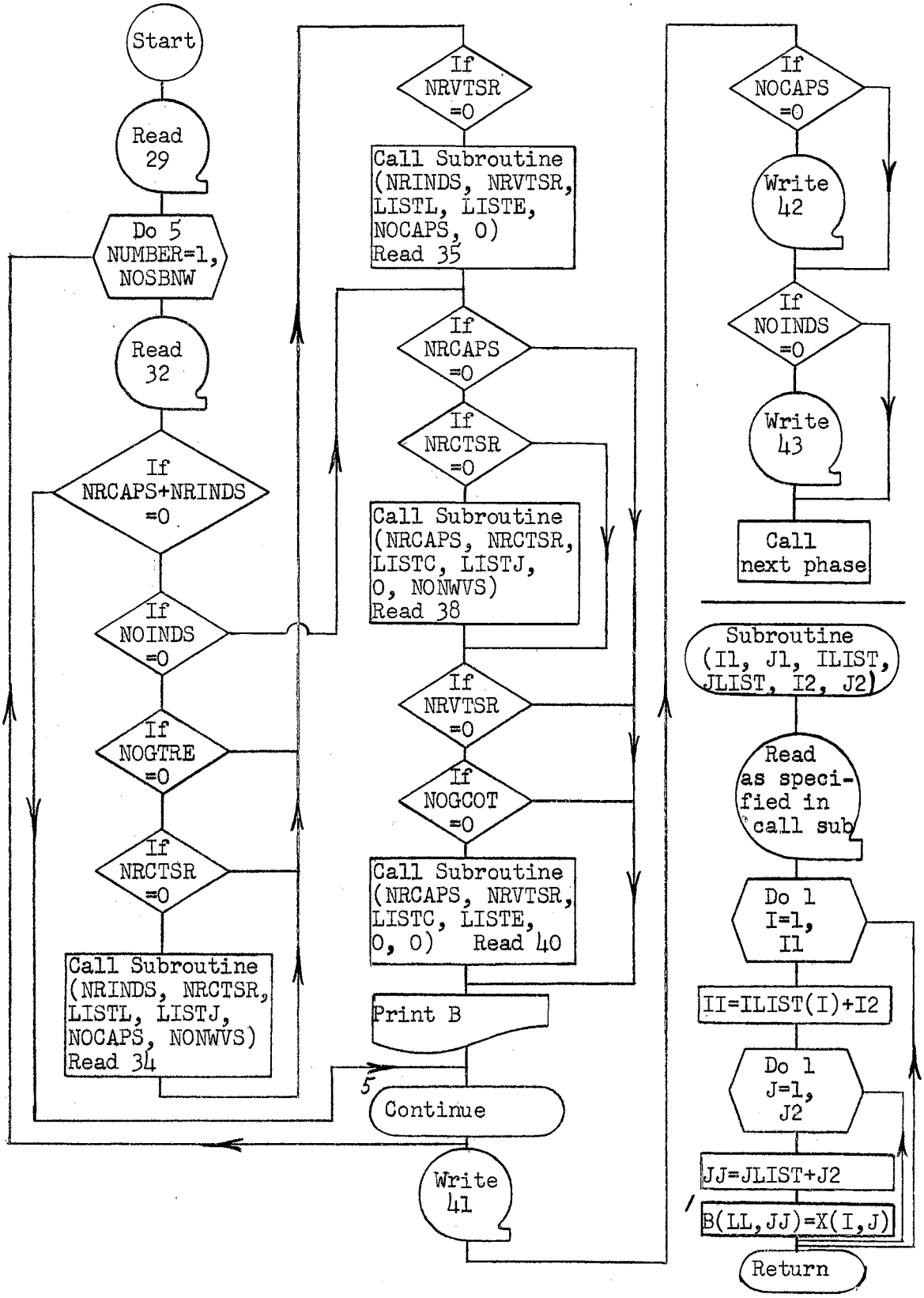

Figure D-9. Flow Chart for Phase 9.

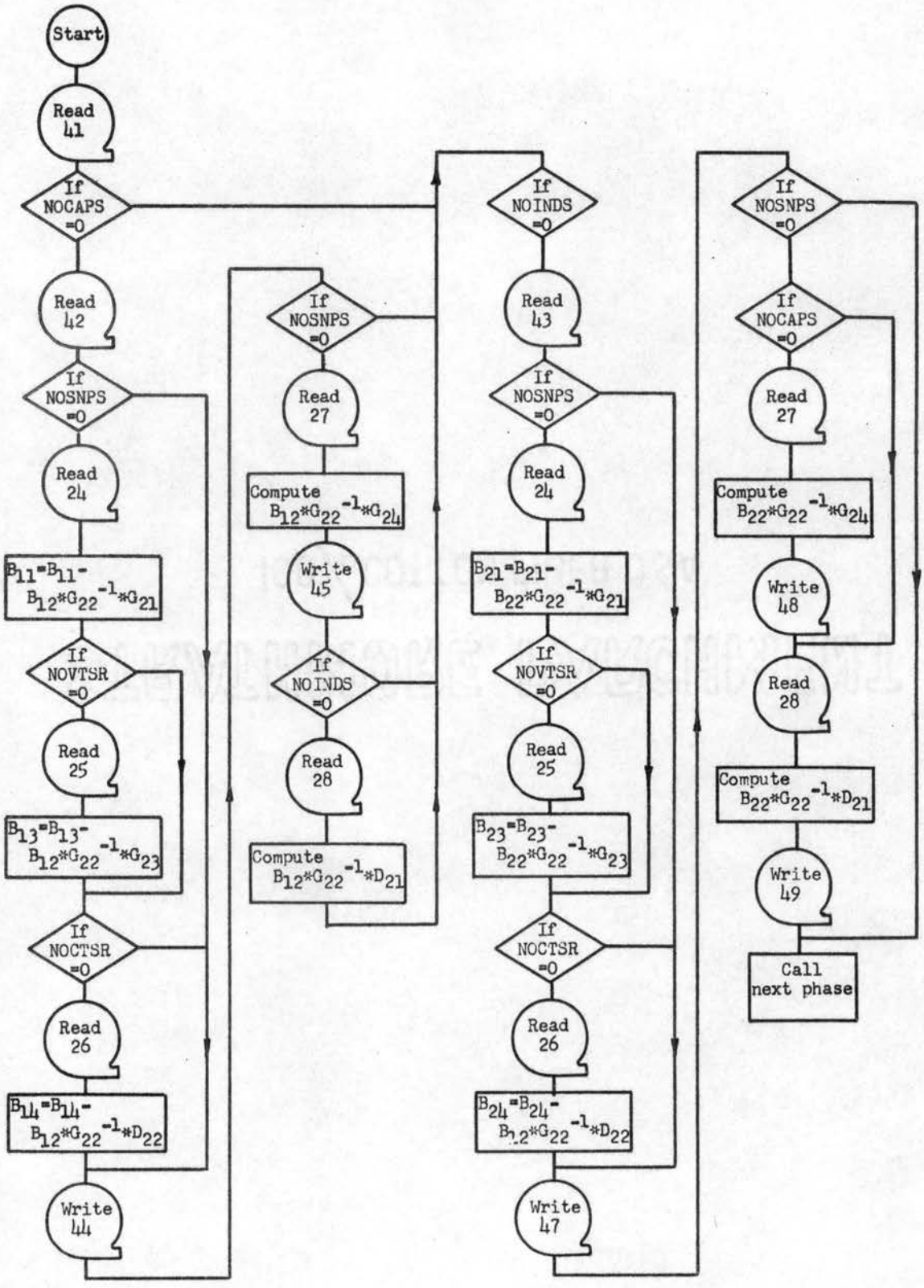

Figure D-10. Flow Chart for Phase 10.

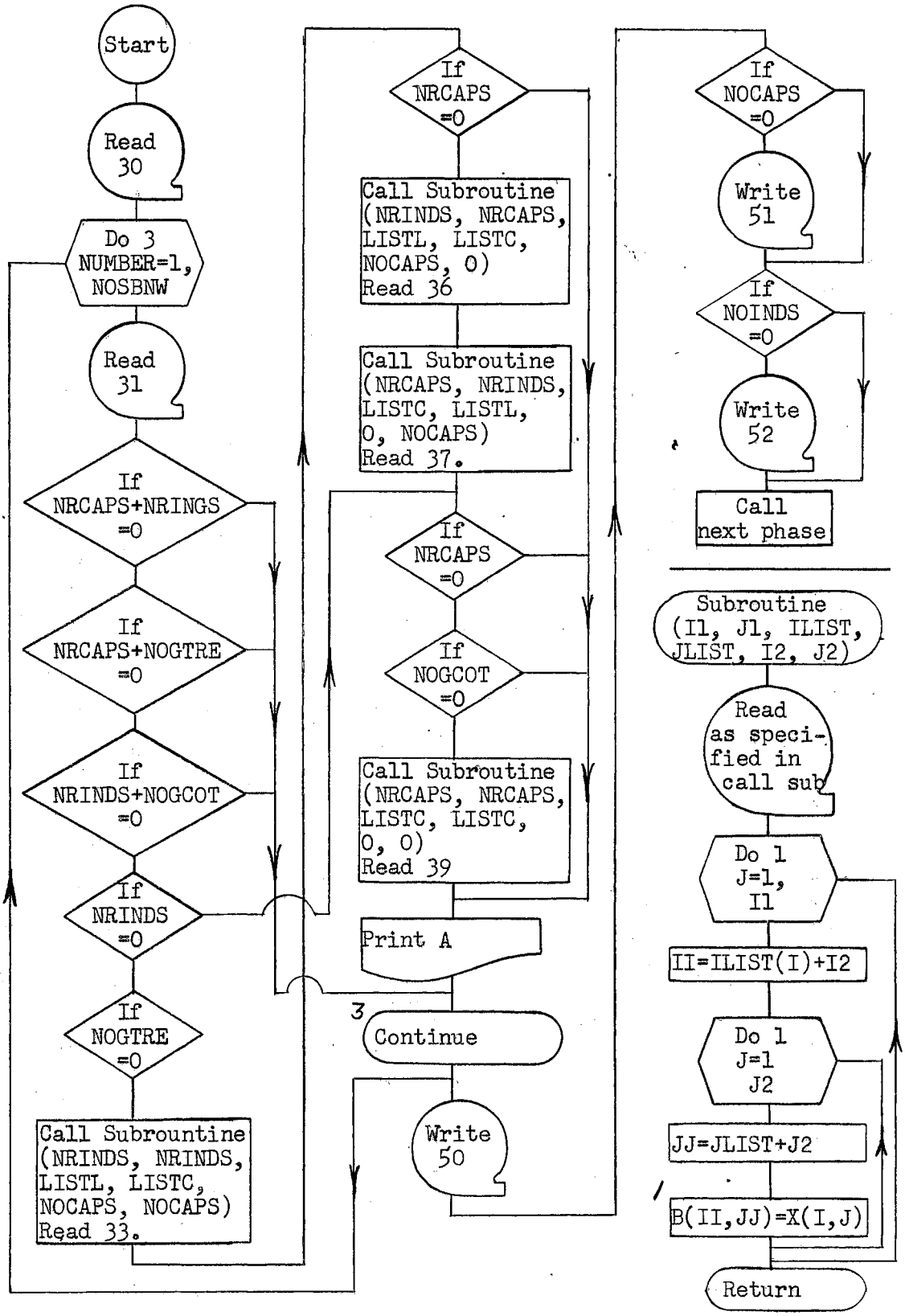

Figure D-11. Flow Chart for Phase 11.

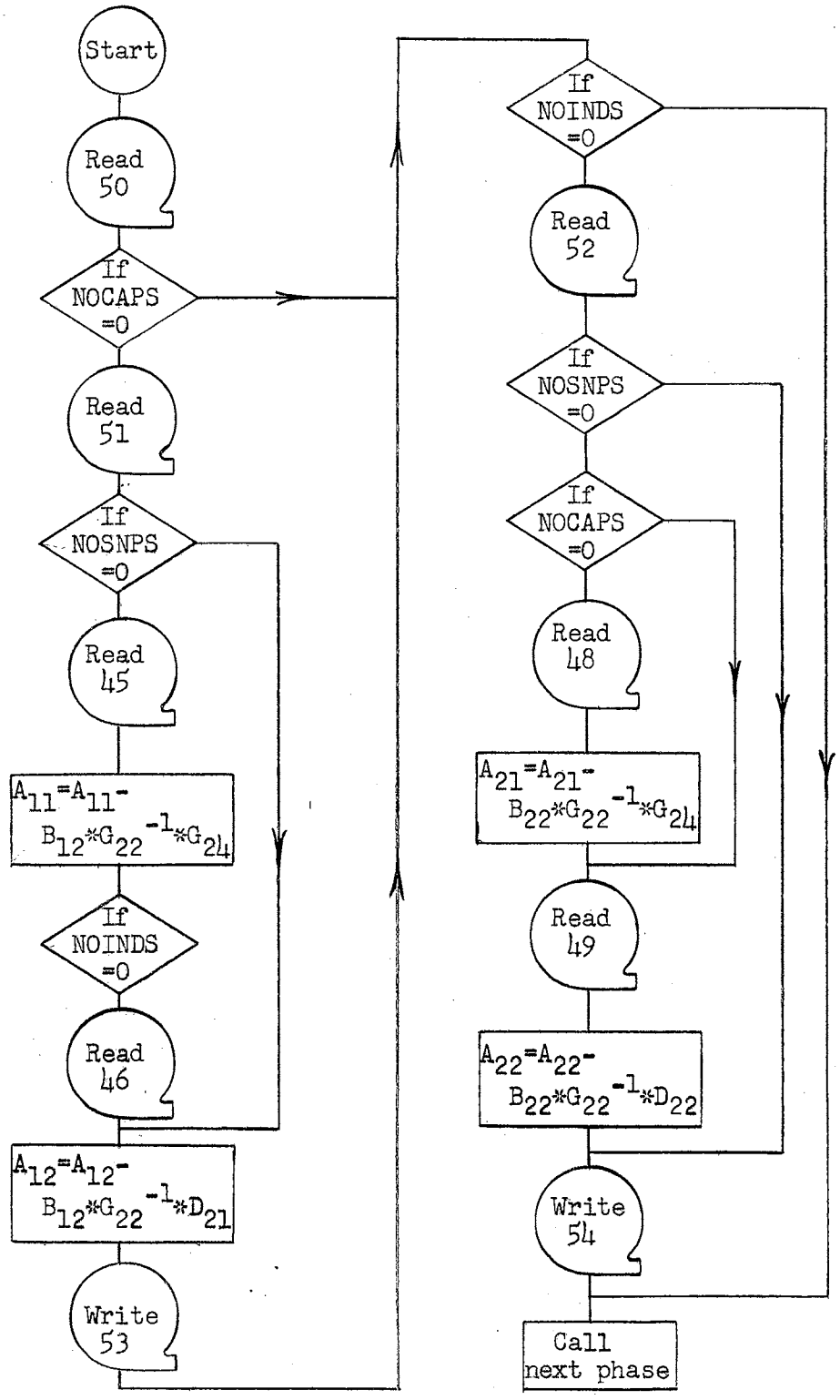

Figure D-12. Flow Chart for Phase 12.

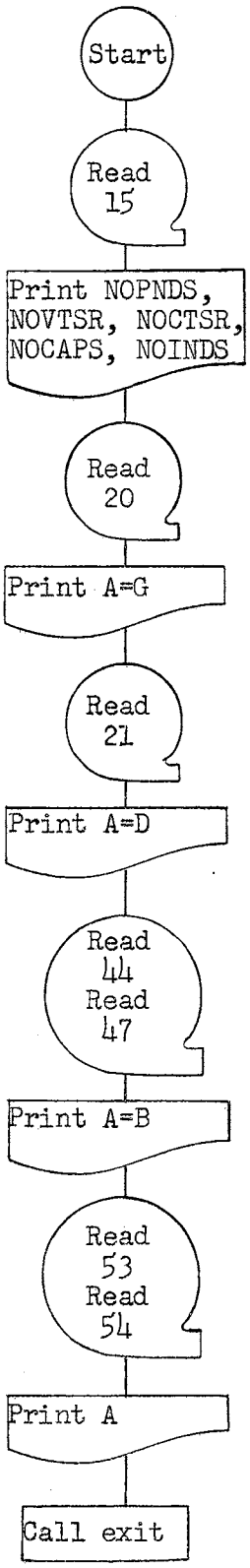

Figure D-13. Flow Chart of Phase 13.

TABLE D-1

READ/WRITE STATEMENT LISTING

Read/Write Statement	Write Phase	Read Phase	Tape Unit	FORTRAN Variables
1	1	2	4	SBNWNO, NOTRST, NOCDST, MAXSUB, SBNWCN TRESET, CRDSET
2	1	2	6	NONODE, NOVTSR, NOCTSR, NOCAPS, NOINDS, NONWEL, NOPNDS, NOCOND, LTINDT, LTCTSR, LTCAPT, NOSBNW, MNNWVS, SRBRLT, PORTND
3	2	3	6	NONODE, NOVTSR, NOCTSR, NOCAPS, NOINDS, NONWEL, NOPNDS, NOCOND, LTINDT, LTCTSR, LTCAPT, NOSBNW, MNNWVS, NONWVS, LIST
4	2	3	5	SBNWNO, NOVTXS, MAXSUB, SBNWCN, SUBNOD
5	2	3	5	SBNWNO, NOTRST, NOCDST, NOSNVS, NOSNCS, TRESET, CRDSET
6	3	4,8	4	NONODE, NOVTSR, NOCTSR, NOCAPS, NOINDS, NONWEL, NOPNDS, NOCOND, LTINDT, LTCTSR, LTCAPT, NOSBNW, MNNWVS, NONWVS
7	3	4,8	4	SBNWNO, NOTRST, NOCDST, NOGTRE, NOGCOT, NRCAPS, NRINDS, NOSNVS, NRVTSR, NOSNCS, NRCTSR, S, GTREE, GCOTRE, LISTC, LISTL, LISTE, LISTJ, SNVSLT, SNCSLT
8	4	5	5	NOSBNW, NOVTSR, NOCTSR, NOCAPS, NOINDS, NONWVS, NOPNDS, NOSBPT, NPNPVS, NPNPPN, NSBPVS, NPNPCP, NSBPT1, NSPVS1, NOPNP1, NOSNPS
9	4	6	6	Same as Statement 8.
10	4	5	5	SBNWNO, NOSNVS, NOGCOT
11	4	6	6	SBNWNO, NOSNVS, NOSNCS
12	4	5	5	G—G22INV, SNVSLT
13	4	6	6	D—G22INV, SNVSLT, SNCSLT
14	4	7	7	NOVTSR, NOCTSR, NOCAPS, NOINDS, NOPNDS, NOSNPS
15	4	13	8	NOVTSR, NOCTSR, NOCAPS, NOINDS, NOPNDS

TABLE D-1 (Continued)

Read/Write Statement	Write Phase	Read Phase	Tape Unit	FORTRAN Variables
16	5	7	7	G_{22}^{-1}*G_{21}—GG21
17	5	7	7	G_{22}^{-1}*G_{23}—GG23
18	5	7	7	G_{22}^{-1}*G_{24}—GG24
19	5	6	5	G_{12}—G12, G_{22}^{-1}—G22INV
20	5	13	8	G—A
21	6	13	8	D—A
22	6	7	7	G_{22}^{-1}*D_{21}—GD21
23	6	7	7	G_{22}^{-1}*D_{22}—GD22
24	7	10	7	GG21—G
25	7	10	7	GG23—G
26	7	10	7	GD22—G
27	7	10	7	GG24—G
28	7	10	7	GD21—G
29	8	9	6	NOCAPS, NCPSP1, NOINDS, NCPPIN, NOPNDS, NONWVS, NOVTSR, NOCTSR, NTOTDV, NOSBNW, NOSNPS, NOSBPT, NNVSP1, NSBPP1
30	8	11	5	NOCAPS, NCPSP1, NOINDS, NCPPIN, NOSBNW, NOSNPS
31	8	11	5	SBNWNO, NOGTRE, NOGCOT, NRCAPS, NRINDS, NRVTSR, NRCTSR, LISTC, LISTL
32	8	9	6	SBNWNO, NOGTRE, NOGCOT, NRCAPS, NRINDS, NRVTSR, NRCTSR, LISTC, LISTL, LISTE, LISTJ
33	8	11	5	G3=$\underline{A}_{22}$—X
34	8	9	6	G3=$\underline{B}_{22}$—X
35	8	9	6	G3=$\underline{B}_{21}$—X
36	8	11	5	G3=$\underline{A}_{21}$—X

TABLE D-1 (Continued)

Read/Write Statement	Write Phase	Read Phase	Tape Unit	FORTRAN Variables
37	8	11	5	G3=$\underline{A}_{12}$—X
38	8	9	6	G3=$\underline{B}_{12}$—X
39	8	11	5	G3=$\underline{A}_{11}$—X
40	8	9	6	G3=$\underline{B}_{11}$—X
41	9	10	6	NOCAPS, NCPSP1, NOINDS, NCPPIN, NOPNDS, NONWVS, NOVTSR, NOCTSR, NTOTDV, NOSBNW, NOSNPS, NOSBPT, NNVSP1, NSBPP1
42	9	10	6	B_1—B
43	9	10	6	B_2—B
44	10	13	8	B_{11}, B_{13}, B_{14}—A
45	10	12	4	$B_{12}*G_{22}^{-1}*G_{24}$—G
46	10	12	4	$B_{12}*G_{22}^{-1}*D_{21}$—G
47	10	13	8	B_{21}, B_{23}, B_{24}—A
48	10	12	4	$B_{22}*G_{22}^{-1}*G_{24}$—G
49	10	12	4	$B_{22}*G_{22}^{-1}*D_{21}$—G
50	11	12	5	NOCAPS, NCPSP1, NOINDS, NCPPIN, NOSBNW, NOSNPS
51	11	12	5	A_1—A
52	11	12	5	A_2—A
53	12	13	8	A_{11}, A_{12}—A
54	12	13	8	A_{21}, A_{22}—A

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