HIGH-FREQUENCY OPERATION OF SILICON CONTROLLED RECTIFIERS

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CHAPTER I

INTRODUCTION

There exist several important questions pertaining to the high-frequency operation of SCRs. (High frequencies will be considered in the text to be frequencies between 10 kH_Z and 30 kHz.)

Where and why can SCRs be used for high-frequency applications? There are many industrial applications where frequencies higher than commercial line frequencies are either needed or lead to definite advantages in equipment design. There has been a growing interest for the past few years in the application of SCRs to power equipment which operates at audio and ultrasonic frequencies up to 30 kHz, such as: generators (inverters) for ultrasonic cleaning, welding, cutting, mixing equipment and induction heating, radio (for VLF band) and sonar transmitters; cycloinverter supplies, the output of the cycloinverter itself being useful for all applications where a-c power is used. Electronic tubes are being used for all mentioned equipment up till now and even today. However, the potential advantages of solid state devices over tubes are well known. Also, for d-c to d-c SCR converters there are several advantages of using them with high-frequency carriers. The device is smaller in size

(because of reduction of size of all magnetic components) which implies lighter weight and lower cost of the device, too. Since the time constant of the output filter must be much greater than the period of the carrier, high frequency is responsible for the increase of break frequency in the transfer function of the filter; the feedback system is faster, thus dynamically better with less error without increasing the gain of amplifier which may produce parasitic oscillations. Also, using a SCR as a chopper in a d-c to d-c converter introduces a time delay equal to half of the period of the carrier signal, and, as is well known, the longer delays may produce an unstable system; i.e., operation at a higher frequency implies a more stable system with respect to the SCR's equivalent time delay.

What are the limitations of using SCRs for high-frequency applications? The energy per cycle that the SCR must dissipate to maintain thermal equilibrium comes from conduction losses (SCR is in ON state), blocking losses (SCR is in OFF state) and switching losses. For low-frequency applications the switching losses can be neglected, but for higher frequencies they comprise an appreciable part of the total SCR losses, so they must be taken into account. Since the power dissipation increases with increasing frequency, there exists some frequency limit where the total power dissipation of a given SCR reaches its maximum allowable value. The second problem which restricts the increasing of frequency is due to the time intervals required for

SCRs to switch from an OFF to an ON state (turn-on time) and from an ON to an OFF state (turn-off time) which is the time that has to elapse before the SCR can block the reapplied forward voltage.

Which SCR parameters are important for designing an SCR high-frequency device? The important SCR dynamic parameters are the maximum allowable di/dt and dv/dt and the turn-off time. For high-frequency applications a combined effect of these parameters exists, so they are interdependent and their characterization on an individual basis is not sufficient to insure satisfactory operation of the SCR. Therefore, for high-frequency SCRs the principle of concurrent characterization of the dynamic characteristics is necessary, and, as a result, such devices are adaptable to applications with excessive switching losses.

CHAPTER II

THEORETICAL CONSIDERATIONS ASSOCIATED WITH SCR'S HIGH-FREQUENCY OPERATION

P-N-P-N Device. Its V-I Characteristics and Transistor Analogue

The silicon controlled rectifier is a semiconductor p-n-p-n device with three junctions. It has electrical characteristics similar to the gas thyratron or ignitron, having both high- and low-impedance states. Figure 1 illustrates the V-I characteristics of a typical gate-controlled SCR.

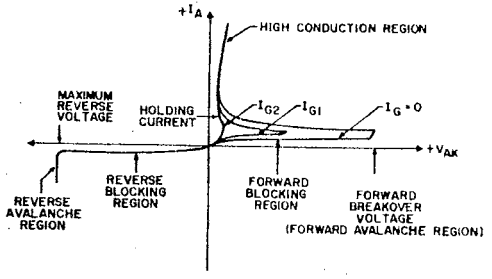


Figure 1. V-I Characteristics of an SCR

In the forward blocking region, increasing the forward voltage does not tend to increase leakage current until the

point is reached where avalanche multiplication begins to take place. Past this point, the leakage current increases quite rapidly until the total current through the device is sufficient to raise the internal loop gain to a value greater than or equal to one. Then the device will go into high conduction region, if the anode current is greater than the holding current. When the anode current drops below the holding current, the SCR reverts to its forward blocking state. In the reverse direction the p-n-p-n structure looks like two reverse-biased p-n junctions in series. In typical operation the SCR is biased well below its minimum forward breakover voltage, and triggering is accomplished by injecting current into the gate lead. Once the gate has been used to trigger the SCR into conduction it loses control and the only method of turning the conducting device off is to reduce the anode current below the holding current.

Diagrammatically, an SCR can be represented as shown in Figure 2(a). In the forward blocking region the junctions J1 and J3 are forward-biased, and the junction J2 is reverse-biased. In a simplified analysis the SCR can be visualized as consisting of two transistors, a p-n-p and an n-p-n (with current gains α_1 and α_2, respectively) interconnected to form a regenerative feedback pair as shown in Figure 2(b). The collector of the n-p-n transistor provides base drive for the p-n-p transistor, and the collector of the p-n-p transistor along with gate current I_g supplies the base drive for the n-p-n transistor. Let I_A and I_K be the

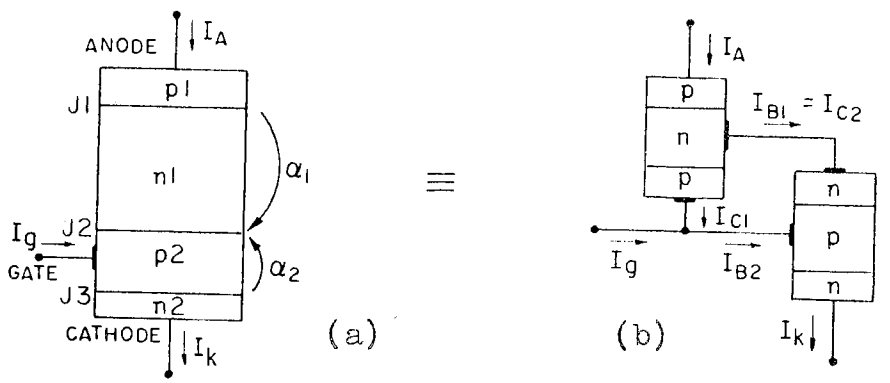


Figure 2. Structure and Transistor Analogue of an SCR

anode and cathode current of the SCR, respectively. Since the base current of the p-n-p transistor, using the conventional notation, is

$$I_{B1} = (1 - \alpha_1)I_A - I_{CBO1} \tag{2-1}$$

and the collector current of the n-p-n transistor is

$$I_{C2} = \alpha_2 I_K + I_{CBO2} \tag{2-2}$$

one may write:

$$(1 - \alpha_1)I_A - I_{CBO1} = \alpha_2 I_K + I_{CBO2} \, . \tag{2-3}$$

Since $I_K = I_A + I_g$ the last equation can be solved for

$$I_A = \frac{\alpha_2 I_g + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)} \tag{2-4}$$

where the $I_{CBO1} + I_{CBO2}$ is the leakage current of the center junction J2.

Both α_1 and α_2 increase with an increase in the anode current I_A, and with the proper gate current a regenerative effect will occur when $\alpha_1 + \alpha_2 = 1$. A positive-feedback condition results which causes both transistors to be driven into a saturated state and causes the junction J2 to become forward-biased to a point where it will no longer support the applied voltage. Moreover, this condition can occur without gate drive by other means which will be considered later.

Physical Theory

In Figure 3(a) is represented a nonbiased p-n-p-n device. At each junction a space-charge layer (a transition region in which donor and acceptor impurities are uncompensated by mobile charge carriers) develops which results in a "build-in potential." The hole and electron concentrations throughout the device are determined by the impurity doping levels, dimensions and temperature.

By applying a positive voltage (Figure 3(b)) to the anode of the device, electrons on the n-type side of J2 move toward the anode, leaving behind positively charged donors. In like manner, holes move toward the cathode, leaving negatively charged acceptors on the p-type side of J2. The space-charge layer of J2 spreads and creates a high electric field which sustains the applied voltage. The space-charge layer width required to support the applied voltage can be determined by solving Poisson's equation (1). Outside the

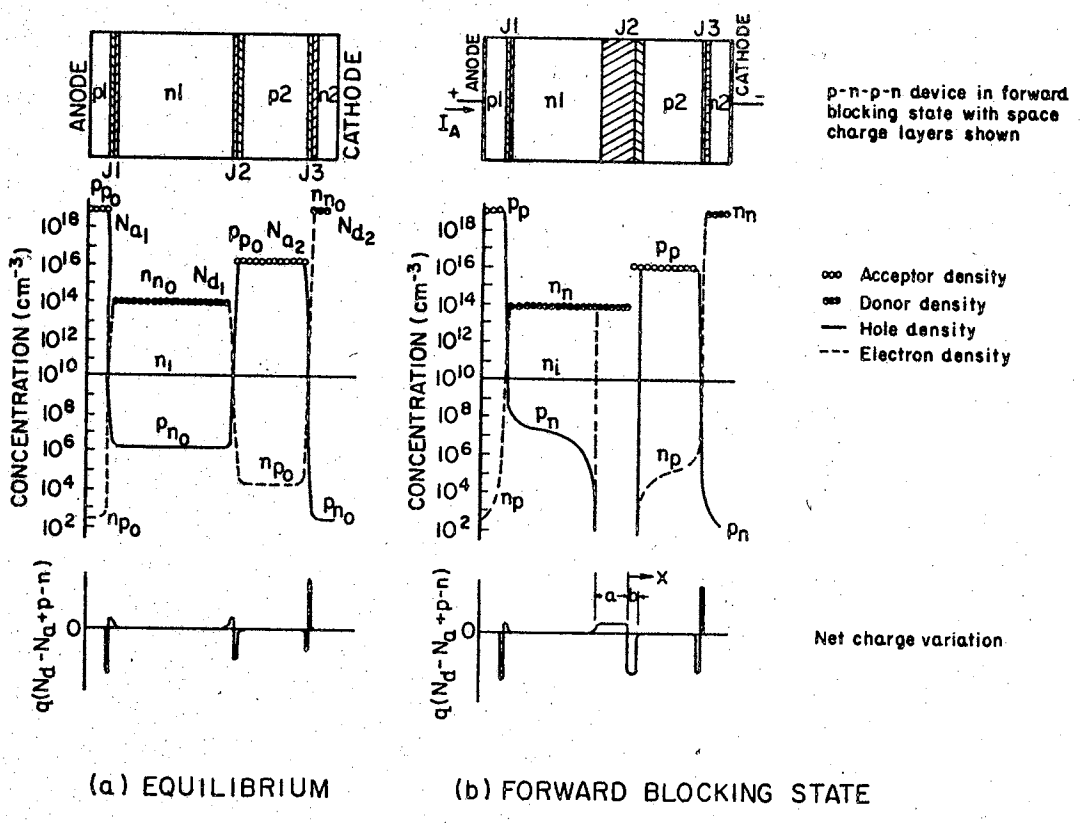


Figure 3. P-N-P-N Device at Equilibrium and in the Forward Blocking State

space-charge layers the semiconductor material is essentially in charge balance (i.e., the charges of the donors and acceptors are neutralized by the presence of free holes and electrons) which implies that outside the space-charge regions the device acts as a conductor with the negligible electric field.

Now, with J1 and J3 forward-biased, and J2 reverse-biased by a fixed applied voltage, one may examine the steady-state current-carrier flow. Throughout the

semiconductor, hole-electrons pairs are generated by thermal agitation. A gradient of minority carriers is formed in the base regions n1 and p2. Holes injected into or generated in the base region n1 diffuse toward J2 and are swept by its high electric field into region p2. In the same manner electrons in region p2 diffuse to J2 and are swept into n1. Carriers generated within the space-charge layer of J2 are also swept into adjoining base regions. Since n1 and p2 are essentially space-charge neutral, if a hole diffused from n1 is collected at J2, a hole must be injected from p1 to n1 or an electron from n1 to p1 to preserve charge neutrality.

If the anode current is I_A (in Figure 3(b)), then the hole current flowing into n1 is $\gamma_1 I_A$, where γ_1 is the injection efficiency of J1; the hole current which reaches J2 (some of holes recombined with electrons) is $\gamma_1 \beta_1 I_A = \alpha_1 I_A$, where β_1 is the transport factor. Thus, the total hole current I_p which is swept into p2 by the space-charge layer of J2 is:

$$I_p = \alpha_1 I_A + I_{pd} + I_{psc} \qquad (2\text{-}5)$$

where I_{pd} and I_{psc} are currents due to the holes thermally generated within n1 and the space-charge layer of J2, respectively.

Since J3 is also forward biased, electrons are injected from n2 across J2 to p2 and diffuse toward J2. The electron current at the p2 side of J2's space-charge layer is:

$$I_n = \alpha_2 I_K + I_{nd} \qquad (2\text{-}6)$$

where I_K is the cathode current, $\alpha_2 I_K$ is the electron current due to electrons injected from n2 and collected at J2, and I_{nd} is the current due to the electrons thermally generated in p2.

The total current flowing across the reference plane at the p2 of J2 is:

$$I_A = I_n + I_p \quad . \tag{2-7}$$

Since with gate drive

$$I_K = I_A + I_g \tag{2-8}$$

and denoting the total thermally generated diffusion current with $I_d = I_{pd} + I_{nd}$, combining the last equations and solving for I_A, yields:

$$I_A = \frac{\alpha_2 I_g + I_d + I_{sc}}{1 - (\alpha_1 + \alpha_2)} \tag{2-9}$$

where $I_{sc} = I_{psc}$, since that term of current is evaluated on the p2 side of J2's space-charge layer. Since α_1 varies with I_A, and α_2 varies with $I_A + I_g$, it is necessary only to increase I_g or to raise the device temperature (which causes $I_d + I_{sc}$ to rise) in order to cause $\alpha_1 + \alpha_2 \longrightarrow 1$. However, the switching would occur even before $\alpha_1 + \alpha_2 \longrightarrow 1$. It can be shown that switching will begin when the sum of the small-signal current gains α_{1s}, α_{2s} reaches unity (1). (Because the alphas of p-n-p-n may be a highly nonlinear function of current, α_{1s} and α_{2s} may be greater than the d-c values.)

Holes which are swept fron n1 into p2 raise the forward-bias voltage across J3, causing it to inject more electrons, which diffuse across p2 to J2 and are swept into

n1. This causes an increase in forward-bias across J1, so more holes are injected through J1 into n1. Thus, the process is a regenerative one which continues until the concentrations of carriers in both base regions exceed their zero-bias equilibrium values, and until the voltage across the device drops to the order of one volt. The current through the device in the conducting state must be limited by the external load resistance; otherwise, the device may be destroyed.

Characteristics of Steady-State Operation

Reverse and Forward Blocking Characteristics

As was shown in Figure 1, for voltages up to the reverse breakdown or the forward breakover regions, a relatively small leakage current flows. Using equation (2-9) with $I_g = 0$ one could obtain the form of the forward blocking current. However, to determine the magnitude of the current and the device parameters which contribute to it, a more fundamental analysis is required. Such an analysis is complicated by the nonlinear current gains associated with the device. In the forward blocking region, J2 is reverse-biased and J1 and J3 are slightly forward-biased due to the leakage current through the SCR. Thus, to determine the blocking current, the leakage current across J2 and the current resulting from injection (at J1 and J3) and diffusion across n1 and p2 must be calculated.

In the case of reverse blocking (cathode positive with respect to anode) J1 and J3 block the flow of current, whereas J2 is forward-biased. Usually J3 has very limited voltage-blocking capability and will go into avalanche breakdown with the application of a few volts. Thus, the n-p-n transistor of the SCR's analogue can be approximated with an avalanche diode in series with p-n-p transistor having no base connection. It can be shown that the blocking current should be of the form (1):

$$I = \frac{I_d + I_{sc}}{1 - \alpha_{pnp}} \quad . \qquad (2\text{-}10)$$

Forward Conducting Characteristics

The forward conducting voltage drop of an SCR is defined as the voltage drop V_{AK} from anode to cathode in the ON state, which includes lead and contact drops. The total voltage drop is approximately equal to the voltage across each junction. At low levels of load current the voltage drop across the base regions is negligible because most of the current flows by minority-carrier diffusion. (It must be remembered that a field current has a voltage drop associated with it, whereas a diffusion current does not.) It is highly advantageous to maintain the minority-carrier lifetimes at a high level to achieve low forward drops. Unfortunately, the short SCR turn-off time requires a smaller value of carrier lifetime.

Analyzing the flow of free carriers in an SCR in the conduction state is a rather complex process. However, an analysis can be carried out if each saturated (in this case) transistor of the SCR's analogue would be represented by two transistors, one normally polarized (with its normal α_n) and the other inversely polarized (with its inverse α_i) (1). Then, using the superposition principle (i.e., by applying voltage across each junction separately and then adding all currents) one can obtain for the sum of the voltage drops across all junctions J1, J2, J3:

$$V_T = V_{J1} + V_{J2} + V_{J3} = \frac{nkT}{q} \ln \frac{A_1 A_3}{A_2} + \left[\ln \left(\frac{I_{S_2} I}{I_{S_1} I_{S_3}} \right) \right] = V_{AK} \quad (2\text{-}11)$$

where I is the I_A's density, k is Boltzmann's constant, T is the absolute temperature, q is the magnitude of the carrier's charge; I_{S_1}, I_{S_2}, I_{S_3} are the saturation currents' densities of each junction with other junctions short-circuited; A_1, A_2 and A_3 are functions of the normal and inverse current gains; and n varies from 1 to 2.

Using the fact that at normal load currents might be $A_1A_3/A_2 = 1.62$, the experimental value $n = 1.5$, and an anode current density of 50 A/cm^2, one may determine the total voltage drop across the SCR to be 1.14 volts (it can be derived that the voltage drops across junctions are: $V_{J1} = 0.96V$, $V_J2 = -0.95V$, and $V_{J3} = 1.13V$).

For higher load currents one cannot neglect the voltage drops, $K\sqrt{I}$, across the body of the p and n regions and the

voltage drop across the lead resistance (IR). It yields:

$$V_{AK} = \frac{nkT}{q} \ln\left(\frac{I_{S_2} I}{I_{S_3} I_{S_1}}\right) + K\sqrt{I} + RI \qquad (2\text{-}12)$$

where K is a constant and $\ln(A_1 A_2/A_3)$ was neglected.

However, in the conduction region the forward characteristic of an SCR (as well as for a semiconductor rectifier) at low current density can be approximated by (2):

$$v = V_o + iR_f \qquad (2\text{-}13)$$

where V_o is the applied voltage necessary before appreciable forward conduction occurs (for SCRs it corresponds to the holding current) and R_f is the forward slope resistance which depends primarily on junction area. Typical values for V_o and R_f are 0.8 volts and 0.02 ohms, respectively.

Dynamic Operation

Triggering Methods. Dv/dt Capability

An SCR can be switched from the forward blocking state to the conducting mode by several methods: thermal turn-on, dv/dt triggering, voltage triggering and the normal gate triggering method.

As was previously described, leakage current ($I_d + I_{sc}$ in equation (2-9)) through an SCR increases exponentially with temperature. As temperature increases, more hole-electron pairs are created. This implies that $\alpha_1 + \alpha_2$ can approach unity and that thermal turn-on can occur. The forward breakover voltage therefore tends to be quite

temperature sensitive and at a high enough temperature the SCR loses completely its ability to block forward voltage.

A rapidly rising positive voltage applied to the anode of an SCR can turn it on if the rate of rise of voltage dv/dt and the applied voltage is sufficiently great. By considering the two-transistor analogue of an SCR and the capacitances across all three junctions it can be seen that a rapidly rising voltage V_{AK} can cause a current through the capacitance of J2 which may cause $\alpha_1 + \alpha_2$ to approach unity. A high dv/dt can be troublesome when it occurs in some SCR circuitry during transients. Most SCRs have a dv/dt capability of 50 to 100 V/μsec. The dv/dt capability of an SCR can be increased by a shorted-emitter design using an aluminum disk to cause a partial shorting of p2 and n2 regions; this implies a by-pass of some turn-on current (1).

Voltage triggering occurs when a blocking junction approaches its avalanche breakdown voltage point. As is well known, a junction avalanches when minority carriers in the space-charge layer are accelerated to a sufficient speed such that their collisions with the lattice result in the creation of more hole-electron pairs, i.e., carrier multiplication occurs.

Gate Turn-On

The triggering methods described in the preceding section represent undesired triggering methods in normal SCR operation. Intentional triggering is generally performed by

a gate pulse. To trigger an SCR into its conducting state, the blocking junction J2 (Figure 3(b)) must be discharged. Discharge is accomplished by increasing the concentration of majority carriers adjacent to J2. As indicated in equation (2-9) it is necessary only to increase I_g in order to initiate switching action. However, the load current I_A through an SCR does not respond immediately to the application of gate current. I_A can be characterized by a delay period t_d and a rise period t_r (Figure 4).

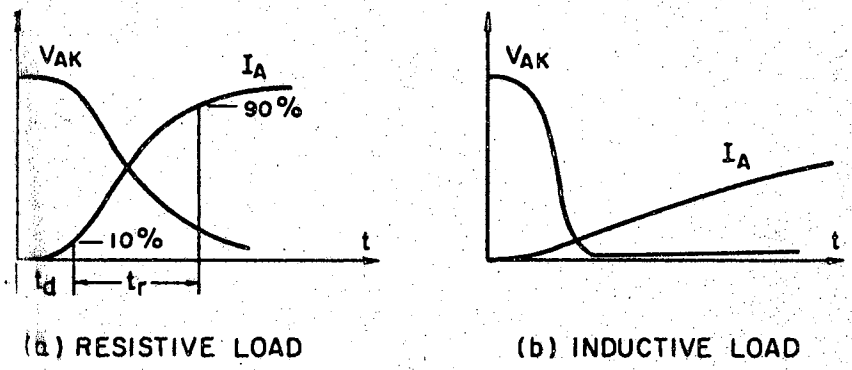


Figure 4. Voltage and Current Waveforms During Turn-on

Delay time is defined as the time between the ten per cent point of the leading edge of the gate current pulse and the ten per cent point of the anode voltage waveform. Similar to t_r of a transistor, t_d decreases as the amplitude of the gate current pulse is increased, but approaches a minimum value of 0.2 to 0.5 μsec for $I_g \geq 0.5A$ (3). This can be explained by the following. If the gate is biased

with a step function of current, electrons inject into base p2 and diffuse toward J2 which they reach after the base transit time of p2 ($t_{p2} = W_{p2}^2/2D_n$ where W_{p2} is the width of p2 and D_n—the diffusion constant of electrons). These electrons are swept in n1 and consequently holes are injected from p1 to n1 to maintain charge balance. They diffuse and reach J2 after the base transit time of n2 and are swept into p2, causing an increase in injected electrons by J3. This process continues until the current is limited by the load. Thus, the minimum t_d is equal to the sum of the base transit times. As a consequence of their wide base widths, high-voltage SCRs have longer delay and turn-on times than low-voltage SCRs.

Rise time t_r (Figure 4) is defined as the time required for the anode voltage to drop from 90% to 10% of its initial value. In a purely resistive circuit the current will rise in the same manner as the voltage falls. Rise time, as well as delay time, tends to be reduced by a large gate drive within the allowable gate dissipation ratings of the SCR. If $I_A >> I_g$ in a resistive circuit, experimental turn-on-current data can be approximated by the expression

$$i = A \exp[a(t - t_d)] \qquad (2\text{-}14)$$

where A and a are constants (1).

In an inductive circuit the rate of increase of current will be mainly determined by the time constant of the circuit. Inductance decreases t_r. However, one must be careful with the duration of the gate signal to avoid "slow

switching" (3).

Total turn-on time is defined as $t_{on} = t_d + t_r$. For an all-diffused and an alloy-diffused SCR structure the typical values of t_{on} are between 1 and 3 μsec; for a planar structure of an SCR (small-current SCR) $t_{on} = 1$ μsec.

Di/dt Effect

Gate turn-on is initiated in a small area near the gate, causing that part of the device, for a short time, to be ON and the remainder to be OFF with a voltage drop across SCR of several volts. The current during this period is space-charge limited by the mobile carriers. Consequently, fast-rising-currents cause heat to be generated at a very rapid rate and can readily cause failure in a large area device owing to a hot spot. For this reason, the rate of rise of anode current di/dt must be limited.

A saturable reactor in series with the SCR during turn-on switching interval will greatly reduce switching dissipation in the SCR (4). Attempts have been made to increase the di/dt capability of an SCR by increasing the number of gate injection points to avoid a hot spot. The gate drive requirements increased rapidly as gates were added. Usually SCRs have maximum allowable di/dt = 50 to 150 A/μsec, but the International Rectifier's new "accelerated cathode excitation SCR" has di/dt = 800 A/μsec (5). It should be mentioned that except for radar pulse modulators and high-frequency inverters, the load itself provides only

about 5 A/μsec at the most. But an RC network which is placed in parallel with the SCR to suppress the dv/dt effect, when discharged into the SCR can provide a very stringent di/dt to the device (6).

When an SCR must handle a large current in a short time in order to increase the di/dt capability of a device, there are special requirements for gate drive signal. The same requirements are imposed for high-frequency operation (usually t_r = 0.1 μsec of a gate signal).

Turn-Off Mechanism and Specifications

The turn-off process is generally initiated by reducing the load current to a value less than the holding current or by reversing the current flow through the structure. During this process excess minority- and majority-carrier charge in the regions must be swept out by an electric field (in the vicinity of the reverse-biased J1 and J3) or decay by recombination (in the vicinity of the forward-biased J2).

The current waveform can be divided into four regions (Figure 5). In region I the reverse current I_R is limited only by the external circuit impedance. When the excess minority carrier concentration at J3 reaches zero (time t_1), its space-charge layer begins to widen and J3 becomes reverse-biased; in this region (II) I_R decays until the relatively low avalanche-breakdown voltage of J3 is reached (t_2) when the voltage across J3 becomes essentially a constant voltage drop in series with p2-n1-p1, which still

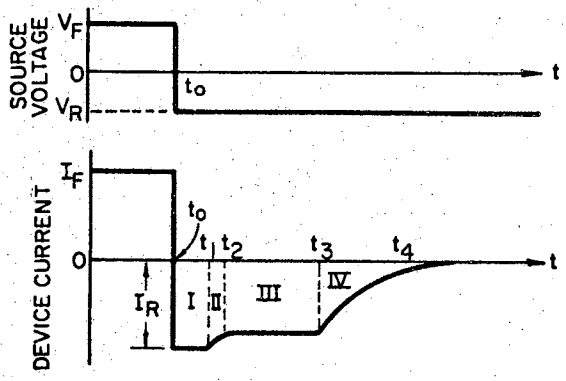


Figure 5. Waveforms During Turn-off

looks like a short circuit. At time t_3 the excess holes at J1 reach zero, the voltage across J1 begins to build up and the current decays to its steady-state blocking value. In most practical cases the reverse blocking capability of J3 is negligible and it is realistic to consider only the behavior of J1.

The SCR waveforms for turn-off time measurements can be shown in Figure 6. The time during which reverse recovery current I_R flows in the SCR (t_3 to t_6 which is the point where I_R has decayed to 10% of its peak value) is the reverse recovery time t_{rr}. This is the time required before the SCR can block reverse voltage.

The turn-off time of an SCR t_{off} is defined as the shortest interval between the time when forward current reaches zero and the time when the SCR is able to block reapplied forward voltage without turning on. The circuit turn-off time t_c (t_3 to t_8) must always be greater than t_{off}

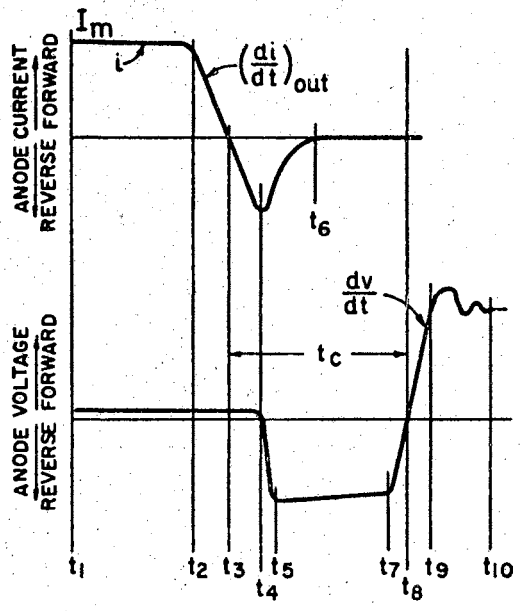


Figure 6. SCR Waveforms for Turn-off Time Measurements

The t_{off} is determined primarily by recombination of the holes in base n1 and using the charge controlled analysis it can be shown that for most high voltage SCRs it is (1):

$$t_{off} \cong \tau_p \ln \frac{I_F}{I_H} \qquad (2\text{-}15)$$

where τ_p is the lifetime of holes, I_F is the forward current of the SCR, I_H is the holding current of the SCR.

Obviously, τ_p is the primary controlling factor. It can be decreased by diffusing gold into the wafer during the manufacturing process. For high-frequency SCRs, t_{off} must be as small as possible; consequently, in this case, τ_p should be small and I_H large. The recombination current can be neglected in comparison with the reverse recovery current. Thus, with low-reverse-impedance circuits t_{rr}

(usually a few microseconds) is a small part of t_{off} for which typical values are between 20 and 80 μsec. For high-frequency SCRs t_{off} is less ($\tau_p \cong 5$ μsec in this case) (7).

Turn-off time was measured under specified conditions because it depends on several parameters (4), (8). It will increase with:

- an increase in junction temperature, T_J
- an increase in forward current amplitude, i_F,
- an increase in the rate of decay of forward current $(di_F/dt)_{out}$ (t_2 to t_3),
- a decrease in peak reverse current,
- a decrease in reverse voltage,
- an increase in the rate of reapplication of forward blocking voltage,
- an increase in forward blocking voltage.

Turn-off time can be decreased somewhat by a negative gate bias voltage. An external shunt gate resistance can also reduce t_{off} by assisting in recovering stored charge by raising the anode holding current and by requiring higher anode current to initiate re-triggering which, in fact, is an increasing in the circuit turn-off time, t_c (4).

CHAPTER III

SOME CALCULATIONS AND CONCURRENT CHARACTERIZATION OF HIGH-FREQUENCY SCRS

Calculations of the Theoretical Frequency Limitation

The maximum operating frequency f_m of an SCR depends on all the important SCR dynamic parameters, but primarily on turn-off time. But, because t_{off}, as has been shown, depends on several parameters, f_m implicitly depends on all these parameters. Thus, in practice, for specified conditions f_m can be found from the concurrent characteristics of a high-frequency SCR, which will be considered later. However, an estimate of the theoretical-frequency limitation may be obtained without such characteristics (1).

A-C Circuits

A circuit turn-off ratio, which gives the fraction of time that each SCR in a circuit is reverse-biased may be defined as

$$K_o = \frac{t_c}{T} \qquad (3\text{-}1)$$

where t_c is circuit turn-off time and T is a period of output

waveform (Figure 7).

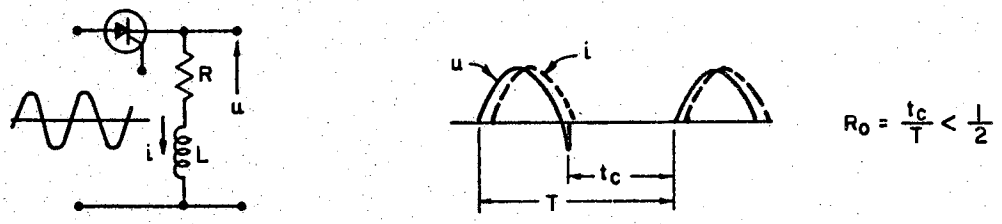


Figure 7. An Example of an a-c Circuit With SCR

Since, as is well known, $t_c \geq t_{off}$, the maximum operating frequency f_m is approached when the SCR turn-off time equals the circuit turn-off time, or $t_{off} = t_c$. This condition assumes that the dv/dt capability of the SCR is not limiting, and it neglects the time to reach zero current $t = \frac{I_m}{(di/dt)_{out}}$ (t_2 to t_3 in Figure 6). Substituting $t_c = t_{off}$ and $T = 1/f_m$ in equation (3-1), one can obtain

$$f_m = \frac{1}{t_{off}} K_o \qquad (3\text{-}2)$$

where t_{off} is the SCR turn-off time under the specified condition.

In practice the dv/dt capability of an SCR at its operating junction temperature may be frequency-limiting. Since the signal's $(dv/dt)_{sig}$ should be less than SCR's dv/dt, one may determine that in a-c circuits with a sinusoidal driving voltage and a resistive load, f_m is limited by the equation (3-2) and the following relation:

$$f_m \leq \frac{1}{2\pi E_m} \frac{dv}{dt} \qquad (3\text{-}3)$$

where E_m is a peak voltage of the supply. Usually the first condition is more severe than the second one.

D-C Circuit

In order to obtain f_m for d-c circuits (actually circuits with d-c supply) such as choppers and inverters one should calculate the total circuit forward recovery time t_{fr} (Figure 6, t_2 to t_{10}). In the cases of time-ratio modulation (Figure 8) and pulse-width modulation the limit condition of f_m is approached when $t_c = t_{off} \longrightarrow$ OFF time. In d-c circuits t_c, is a design variable determined by the time constant of the circuit. As an example, consider the chopper circuit of Figure 8 (L_c simulates the inductance effective in the circuit during the early part of the reverse recovery interval).

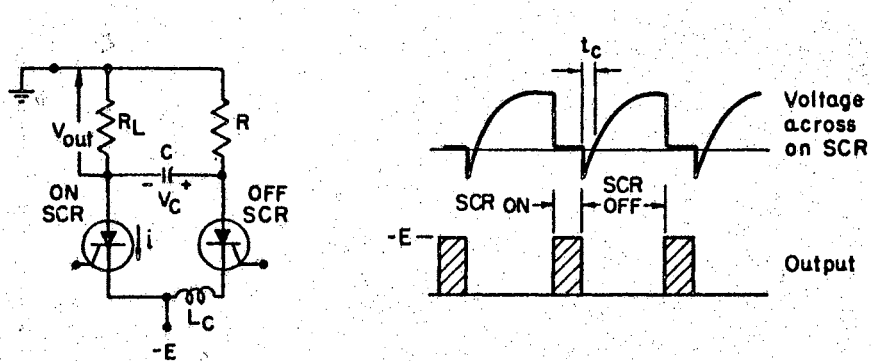


Figure 8. A Chopper Circuit for Time-Ratio Power Modulation

If one assumes the following circuit parameters: $E = 400V$, $R_L = 8$ ohms, $I_m = E/R_L = 50A$, $(di/dt)_{out} = -V_c/L_c =$ $= 25A/\mu sec$, the total circuit forward recovery time is

$$t_{fr} = \frac{I_m}{(di/dt)_{out}} + t_c + \frac{E}{dE/dt} \quad . \qquad (3\text{-}4)$$

Assume that the SCR is specified at its operating junction temperature for $t_{off} = 20$ μsec and an initial $dv/dt = 50V/\mu sec$. Then, if the maximum SCR capability is to be limiting, one may substitute limiting-device parameters for operating-circuit parameters by taking $t_c = t_{off}$ and $dE/dt = dv/dt$, or

$$t_{fr_{min}} = \frac{50}{25} + 20 + \frac{400}{50} = 2 + 20 + 8 = 30\mu sec \quad .$$

If a duty cycle of ON/(ON + OFF) = 50% is required, and if the total circuit OFF is consumed by $t_{fr_{min}}$, the maximum theoretical circuit operating frequency is

$$f_m = \frac{1}{2t_{fr_{min}}} = \frac{10^6}{2 \cdot 30} = 16.6 \text{ kHz} \quad .$$

Heat Generation Calculations

Introduction

Electrical energy is converted to heat, which must be dissipated to the heatsink, because of the following electrical power losses: 1. forward conduction losses, 2. reverse and forward blocking losses, 3. switching losses, 4. gate dissipation (triggering) losses, and sometimes 5. transient losses (due to changing the load or main source

voltage).

Forward conduction losses are the major source of a junction heating for a normal duty cycle and low frequencies. However, for high operating frequencies or very steep (high di/dt) current waveforms turn-on switching losses must be considered.

Forward Conduction Power Dissipation

The average forward conduction power dissipation P_C may be calculated from

$$P_C = \frac{1}{2\pi} \int_{\alpha}^{\alpha+\Psi} v \cdot i \, dt \qquad (3\text{-}5)$$

where the SCR is in its ON state between the angles α and $\alpha+\Psi$. If the current waveform is represented by $i = I_P \sin\Phi$ (where I_P is the peak forward current) then using equations (2-13) and (3-5) it was found for SCRs (for which $\alpha+\Psi = \pi$) (2)

$$P_C = \frac{I_M^2 \pi R_f}{4\sin^4 \frac{\Psi}{2}} \left[\frac{\Psi}{2} - \frac{\sin 2\Psi}{2}\right] + V_o I_M \qquad (3\text{-}6)$$

where the mean value of current is

$$I_M = \frac{1}{2\pi} \int_{\alpha}^{\pi} I_P \sin\Phi \, d\Phi = \frac{I_P}{\pi} \sin^2 \frac{\Psi}{2} \quad . \qquad (3\text{-}7)$$

If R_f is difficult to measure it can be eliminated by measuring the mean forward voltage drop across SCR

$$V_M = \frac{1}{2\pi} \int_{\alpha}^{\pi} (V_o + R_f I_P \sin\Phi) \, d\Phi \quad . \qquad (3\text{-}8)$$

Manufacturers' SCR specification sheets contain average forward power dissipation P_{AV} — average forward current I_{AV} curves for various conduction angles of SCR and for sinusoidal current waveforms. They are conservative for rectangular waveforms with the same average value and conduction angle.

At low frequencies, assuming $P_{AV} \cong$ total average power dissipation of an SCR, and using $P_{AV} - I_{AV}$ and $T_C - I_{AV}$ curves (T_C is maximum allowable case temperature), one may determine the required thermal resistance of the SCR heatsink.

Reverse and Forward Blocking Losses

Reverse or forward blocking current at any given junction temperature as a function of voltage can be approximated by the expression (Figure 9) (1):

$$i_R = I_o + mv_R \qquad (3\text{-}9)$$

where I_o is intercept current with no gate current, v_R is instantaneous reverse voltage $= V_p \sin\theta$ and m is the slope of i_R.

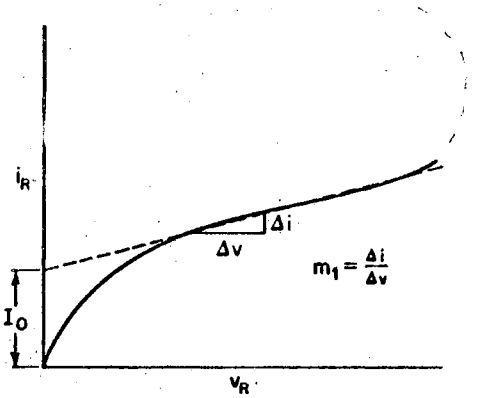


Figure 9. Approximation of a Blocking V-I Characteristic

Thus, the average reverse blocking power dissipation is:

$$P_{RB} = \frac{V_P}{2\pi} \int_{\alpha}^{\beta} (I_o \sin\theta + mV_P \sin^2\theta) d\theta \qquad (3\text{-}10)$$

where the SCR is in its blocking state between the angles α and β.

In the same manner one may calculate the average forward blocking power dissipation P_{FB} by using corresponding electrical angles. The total blocking losses P_B are, of course, equal to the sum P_{RB} and P_{FB}.

Turn-On Switching Loss

The accurate power dissipation during a turn-on interval could be found by multiplying the curves for v and i in Figure 4. It was pointed out that the total turn-on time depends on several circuit parameters, as well as on the SCR structure. Therefore, it is difficult to find the turn-on loss analytically. But voltage and current oscillograms taken during an experiment can be integrated numerically to find the turn-on energy (9). Also, if the L/R time constant of the circuit is appreciably longer than the turn-on time of the SCR, the turn-on switching power loss will be negligible. However, if the L/R time constant is short so that the build-up of current is determined by the collapse of voltage across the SCR, the average turn-on power dissipation, P_{ON}, can be predicted by the following formula (2):

$$P_{ON} = f \cdot V_A \cdot I_A \cdot 0.65 \cdot 10^{-6} \text{ W} \qquad (3\text{-}11)$$

where f is operating frequency, V_A is anode voltage immediately prior to switching, and I_A is anode current immediately after switching.

Turn-Off Switching Loss

As was previously discussed, during the reverse recovery time, t_{rr}, an SCR reverse recovery current, I_R flows (Figures 5 and 6). This current produces a power dissipation of a turn-off interval. The shape of this current and consequently the turn-off loss depends on the nature of the circuit. If the reverse blocking capability of the junction J3 is negligible the shape of I_R in an SCR is similar to the I_R in a diode (10). For instance, for a half-wave rectifier with an inductive-resistive load the voltage and current waveforms during commutation are represented in the Figure 10.

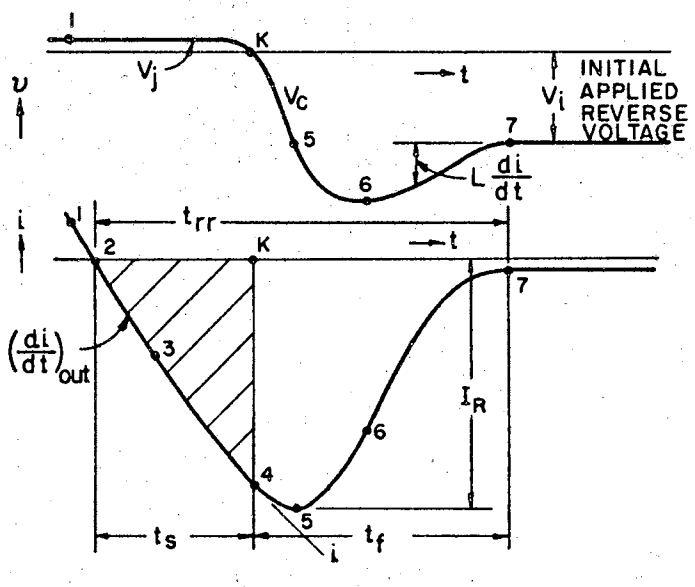


Figure 10. Voltage and Current During t_{rr}

The time period t_s (the junction recovery time) depends upon the device. During t_s, I_R is controlled by the circuit components, i.e., I_R follows exactly the circuit current, the semiconductor is practically a conductor. After t_s the device assumes a resistive character. During the time period t_f (the bulk recovery time), the current is determined by the diffusion process, i.e., t_f and I_R do not depend on the type of circuit used. Using the diffusion equation for a p-n junction, it was found that, if maximum values of forward and reverse current are adjusted to be equal, then

$$t_f = 0.228\ \tau_p \qquad (3\text{-}12)$$

where τ_p is the lifetime of holes (1). (For an SCR one considers holes in n1.)

It is known that, depending on the ratio $t_s:t_f$ there are two types of diode commutation behavior during reverse recovery time: snap-off and tail-off type (soft recovery) (11). SCRs generally have the former type though they do not have a severe snap characteristic. Empirically it has been found that $t_s \cong 0.6t_{rr}$ for a number of different commutation conditions (4). Usually, t_{rr} lasts a few microseconds. It should be stressed that turn-off loss is less than turn-on loss. In the worst case, i.e., a soft recovery, the turn-off loss in a diode is:

$$P_{off} = f \cdot Q_R \cdot E_C \qquad (3\text{-}13)$$

where Q_R is the total stored charge and E is the circuit reverse voltage. In the case of SCRs, since P_{off} occurs mostly during t_f, according to Figure 10:

$$Q_R \cong \frac{1}{2} I_R \cdot t_f \quad . \qquad (3\text{-}14)$$

As in the case of turn-on energy, the energy dissipated during turn-off interval can be found experimentally (9). In Figure 11 is shown a distribution of main losses of an SCR subjected to high-frequency operation. The results were found experimentally (9).

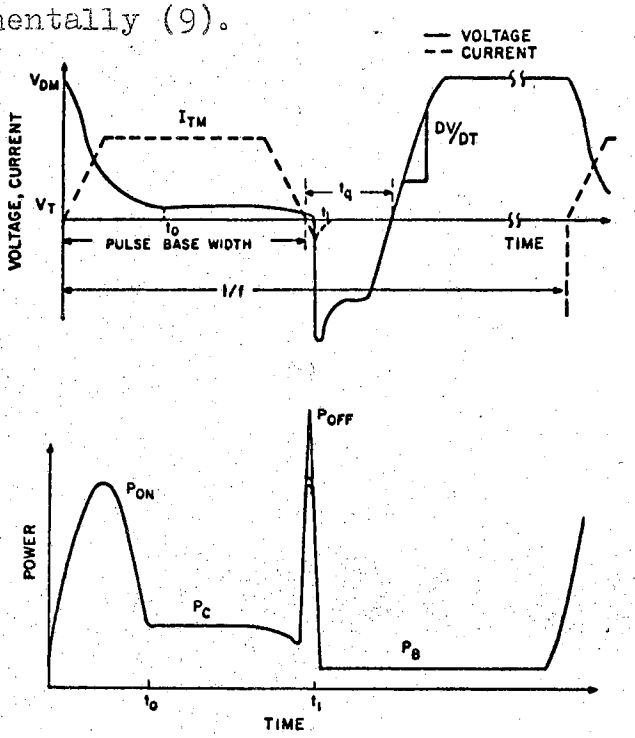


Figure 11. A Distribution of Losses for High-Frequency Operation

Gate Power Dissipation

The heat generated in the gate region of an SCR can be calculated in much the same manner as outlined for anode-to-cathode heat calculations (1). But, the peak rather than the average power should, generally, be used for

calculation of heating. For the medium current high-frequency SCRs one might estimate the gate and blocking losses together to have a value of one watt. However, a great deal of heat can be generated in the gate circuit if the reverse avalanche voltage of the gate-to-cathode junction is exceeded.

Transient Heating

If the load impedance or source voltage is instantaneously changed, the voltage across the SCR decays and the current through the SCR builds up, exponentially with time (1)

$$i \cong (I_M - I_I)[1 - \exp(-2.2t/t_r)] + I_I \qquad (3\text{-}15)$$

$$v \cong (V_M - V_F) \exp(-2.2t/t_r) + V_F \qquad (3\text{-}16)$$

where V_M, V_F are instantaneous voltages before and after switching, respectively; I_I, I_M are instantaneous current before and after switching, respectively; t_r is rise time.

The average transient power can be determined by integrating the product of v and i over the surge period.

Concurrent Characterization of the SCR Dynamic Parameters for High Frequency Operation

When SCRs are to be used in inverters and choppers or for high-frequency applications there exists a combined effect of the three most important dynamic parameters: the

rate of voltage rise dv/dt, the turn-off time t_{off} and the rate of current rise di/dt.

When SCRs are subjected to current pulses with high di/dt (10 to 100 A/μsec), incomplete utilization of the device junction area may exist, which results in an increased forward voltage drop. Consequently, power losses are increased which result in higher junction temperatures (T_j). Both turn-off time and dv/dt capability decrease with increasing T_j. Therefore, the presence of hot spots caused by localized heating, may cause circuit malfunction even though the specified value of any one of the three dynamic parameters was not exceeded from the standpoint of individual characterization. Thus, the need for the concurrent characterization is apparent.

Pulse Operation Test

Conventional turn-off time testing is an experiment which is performed with a low-level (10A), relatively long current pulse (50μsec) (4) (8). In order to take into account a localized heating due to hot spots a method of test has been developed which simulates the duty imposed by actual pulse applications in that dv/dt, di/dt and t_{off} effects are combined simultaneously (12). This is the pulse operation test for measuring the pulsed turn-off time t_{off}. Figure 12 shows the current and voltage waveforms applied to the SCR during the t_{off_p} test.

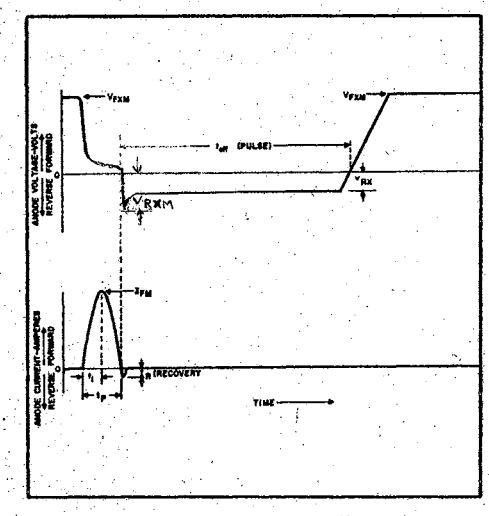


Figure 12. Current and Voltage Waveforms for t_{off_p} Test

The t_{off_p} test data was obtained using a current pulse of 100A peak with a base width of 20μsec (12). An RLC circuit is used to produce a desired current pulse. A linear dv/dt of forward blocking voltage is employed since it presents a more severe condition to the test device. In devices which develop hot spots under pulse operation the t_{off_p} may be three to four times longer than the conventional turn-off time t_{off}.

A so-called interdynamic factor, I.F. = t_{off}/t_{off_p} is defined. Ideal I.F. = 1 for medium current. General Electric Company's SCRs C140 and C141 have I.R. = 1, i.e., their t_{off} and t_{off_p} are equal (10 and 15μsec, respectively) (7).

As a result of concurrent characterization, these SCRs can be operated in inverter and chopper circuits to extreme

frequencies (about 25kH_z), power and case temperatures which, with conventional SCRs, are impossible to attain.

High-Frequency Ratings

The methods used for developing ratings on conventional SCRs cannot be used for high-frequency SCRs since switching losses must be considered. The problem is further complicated by the fact that the effective junction area is time dependent which creates major problems in determining the forward conducting voltage drop of an SCR (V_{AK}) and thermal impedance (junction-case), normally used in rating calculations. This V_{AK} is not only time dependent, but it also depends on the initial blocking voltage level and the applied gate trigger signal. The thermal impedance is difficult to calculate and even more difficult to measure in microsecond time range. Consequently, peak junction temperature T_{jp} cannot be readily determined. Concurrent characterization through the pulse turn-off time test provides a means to control T_{jp}.

High-Frequency Performance Curves

As was previously discussed, low-frequency SCRs curves are primarily based on forward conduction power losses. Therefore, for high-frequency operation low-frequency curves are useless. Thus, for special high-frequency SCRs manufacturers' specification sheets contain high-frequency performance curves; the principle of concurrent

characterization of the dynamic characteristics has been employed in the development of such curves (13).

Peak Current Rating Curves

Pulse turn-off time depends on many parameters, almost the same as conventional t_{off}. This implies that the peak forward current I_{PK} of an SCR used for high-frequency operation depends on the same parameters for specified t_{off_p}. If such dependence is denoted by Ψ, one may write

$$I_{PK} = \Psi(f, PW, T_C, di/dt, t_{off_p}, dv/dt, GD, V_{FXM}, V_{RX}, V_{RXM}) \quad (3\text{-}17)$$

where T_C is maximum case temperature of SCR; PW is pulse base width of forward conducting current, i_F; GD is gate drive characteristics; V_{FXM}, V_{RX}, V_{RXM} are forward and reverse voltages across SCR (Figure 13).

For a given SCR the last six parameters in equation (3-17) are specified (which requires specified corresponding circuit parameters) and, therefore, I_{PK} depends on first four variables, only. For sinewave i_F the peak current and pulse width of i_F determine di/dt; so in this case, the peak current curves are plotted for variable f and PW, for several values of T_C. When necessary the values of T_C may be re-plotted so that interpolation for other values of T_C may be easily performed. Also, for some specified PW an interpolation for all frequencies may be obtained. An example of such curves for the SCR C140 and C141 is given in Figure 13.

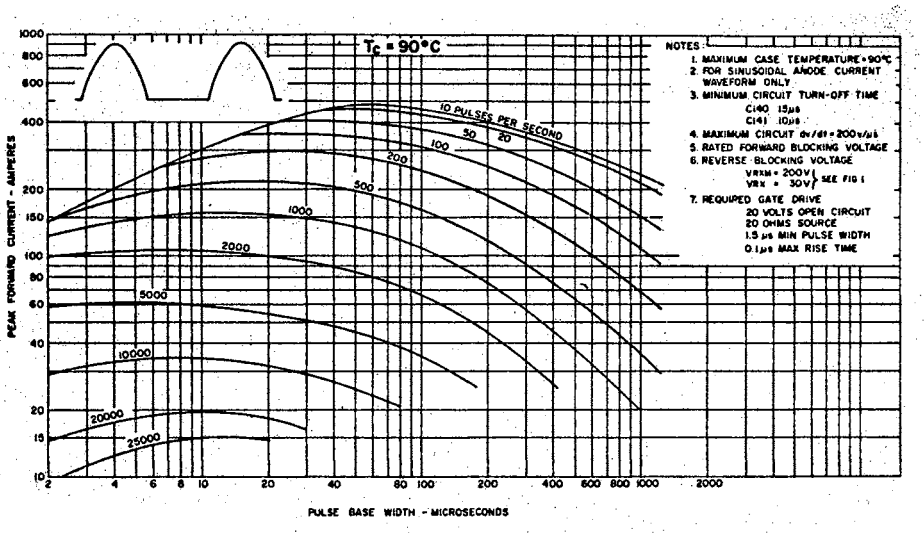


Figure 13. Maximum Allowable I_{PK} vs Pulse Width ($T_C = 90^{\circ}C$)

Power and Energy Curves

In Figure 14 are shown the energy curves for C140 and C141 (7). From these curves one may obtain, for required I_{PK} and PW, energy per pulse W_{PP}.

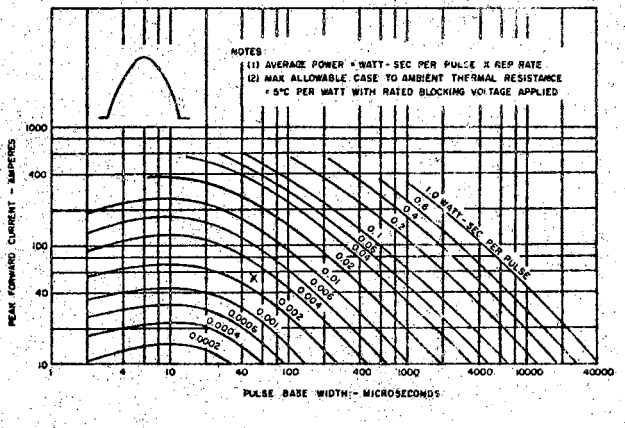


Figure 14. Energy per Pulse for Sinusoidal Pulses

Multiplication of W_{PP} by f yields average anode dissipation P_A which involves forward conduction loss as well as switching losses. Adding the gate and blocking losses (about 1W) to P_A one may obtain the total power dissipation P_T which ought to be used to determine the thermal resistance θ_H of a suitable heatsink by the definition

$$\theta_H = \frac{T_C - T_A}{P_T} \qquad (3\text{-}18)$$

where T_A is ambient temperature, and T_C was specified by using peak current curves.

For i_F waveforms similar to, but not sinusoidal, other energy curves are given, too.

Derivation of High-Frequency Performance Curves

Application of the pulse operation test over a wide range of pulse base widths, repetition rates, peak currents and case temperature results in rating curves of the type shown in Figure 14. At the wider values of PW, switching losses are small since di_F/dt is low. At the shorter PW the curves were developed through the use of concurrent characterization. The values of t_{off} and dv/dt are held constant throughout at their factory tested values. Whereas, allowing a longer t_{off} would result in higher I_{PK} without loss of commutation, this practice results in higher peak junction temperature. In the interests of long term device stability higher peak junction temperature should be avoided. Thus,

no increase in I_{PK} is permitted, even in circuits with longer t_c.

Curves for Non-Sinewave i_F

It should be stressed that for high-frequency operation a rectangular waveshape of i_F must be avoided since a rectangular pulse of power will always raise the temperature higher than any other pulse shape having the same peak and average value. But trapezoidal current waveforms are acceptable and corresponding curves for high-frequency, high-current SCR (General Electric C-158) were developed (9).

Unlike the sinewave, di/dt is not determined with known I_{PK} and PW for trapezoidal waveforms. Therefore, in this case a set of curves is required for each value of di/dt. Since the dynamic effects of switching losses on SCR operation were difficult to predict quantitatively an inverter test circuit has been developed to study these power losses and SCRs were subjected to various switching conditions (9).

Design Considerations of High-Frequency SCRs

In order to make an SCR with high di/dt and dv/dt capabilities and short t_{off} a delicate balance must be maintained among several factors.

For increasing dv/dt capability, a shorted-emitter design is employed which prevents the capacitive current through the SCR from reaching the switching point during

the application of a fast rising voltage. Some of this current is by-passed through the shorted emitter.

Short turn-off time is accomplished through control of the carrier's lifetime τ_p; it is achieved through the diffusion of gold into the silicon pellet.

For high di/dt capability in a high-frequency SCR, a distributed gate area (or several gates) is used to enlarge the initial area of turn-on.

Control of the above mentioned items is a compromise. Emitter shorting raises gate trigger currents. Short lifetime decrease t_{off}, but increases blocking currents, thereby reducing blocking voltage ratings, and also increases forward voltage drop V_{AK}.

CHAPTER IV

HIGH-FREQUENCY GENERATORS WITH SCRS

General Considerations

Classification

A high-frequency generator is basically a frequency changer device, it changes the main supply frequency to a high-frequency signal. Therefore, it can be a rectifier-inverter or cycloinverter.

The basic classification of inverter-converter circuits is based on methods of turn-off (4). For instance, in class A, commutation is performed by resonating the load; in class C, by C or LC switched by a load carrying SCR; in class F, by a-c line (cycloinverters).

Two main classes of inverters are parallel and series. In the parallel inverter (class C) a constant current is effectively switched from one transformer winding to another. This type is very useful at frequencies below about 1000 Hz, but for higher frequencies it is not suitable. The reasons are: 1. rectangular wave of current, which implies that SCRs are subjected to high di/dt, 2. the energy used to turn-off an SCR is lost and represents a considerable loss of power as the frequency of operation is raised, and

3. similar to the d-c or chopper circuits (Figure 8), the circuit turn-off time t_c is a small part of the full cycle, i.e., the maximum theoretical frequency is relatively low. On the other hand, the series inverter (class C) is the most suitable for high-frequency operation, i.e., above about 1000 Hz, because of the need for an LC resonant circuit which carries the full load current.

The Series Inverter

For high-frequency operation the series inverter has several advantages over the parallel type: 1. the current through an SCR is nearly sinusoidal and, therefore, the initial di/dt is relatively low, 2. the commutation energy is not lost since the current flowing into and out of the commutating capacitor traverses the load and thereby delivers energy to it, 3. similar to the a-c circuits (Figure 7), t_{off} of an SCR may be a substantial part (10% to 25%) of the full cycle, and 4. if the inverter is properly designed, SCRs switch at a point in the cycle where load current is at a low value, thus minimizing switching losses in SCRs.

The simplest form of the series inverter are the resonant turn-off circuits shown in Figure 15 (14), (4).

In Figure 15(a) when the SCR is fired a step of voltage is applied to the resonant circuit and a half-cycle of a sinusoidal current flows. As the current attempts to reverse, the SCR is turned off and the capacitor discharges

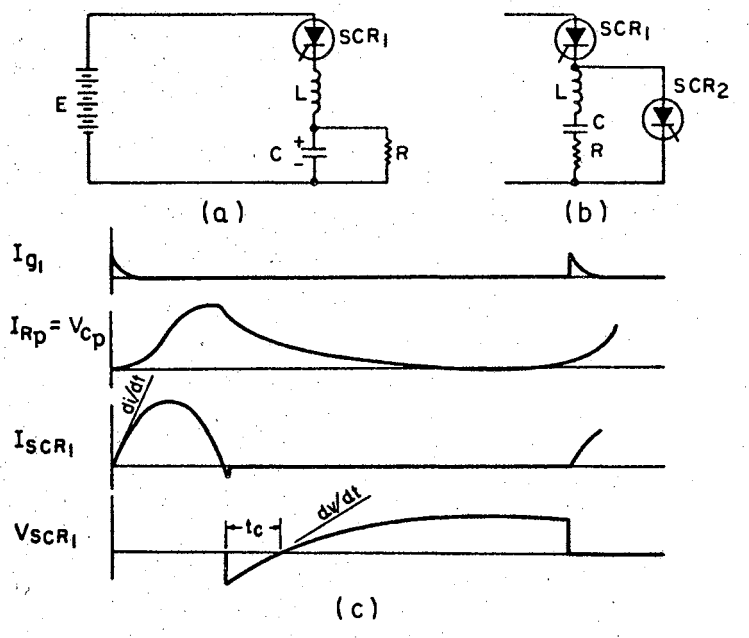


Figure 15. The Simplest Series Inverters

through the load.

The voltage across the load, $v_c(t)$, when SCR is ON is:

$$v_c(t) = E\left[1 - \frac{1}{\sqrt{1-\delta^2}} \exp\left(-\frac{t}{2RC}\right) \sin(\omega_r t + \Psi)\right] \qquad (4-1)$$

where

$\omega_r = \sqrt{1/LC - 1/4C^2R^2}$ is the corner resonant frequency,

$\delta = \frac{1}{2R}\sqrt{\frac{L}{C}}$ is the damping factor,

$\Psi = \cos^{-1}\delta$.

When SCR is OFF

$$v_c(t) = V_c \exp(-t/RC) \qquad (4-2)$$

where $V_c \cong 2E$ is the maximum value for $v_c(t)$ in equation (4-1). The circuit works only if:

$$\frac{1}{LC} > \frac{1}{4C^2R} \quad \text{or} \quad R > \frac{1}{2}\sqrt{L/C} \ . \qquad (4\text{-}3)$$

In Figure 15(b) when SCR1 is turned off, SCR2 should be fired. The current through the circuit on firing SCR1 is

$$i(t) = \frac{E}{\omega_r L} \exp(-\frac{R}{2L} t) \sin \omega_r t \qquad (4\text{-}4)$$

where $\omega_r = \sqrt{1/LC - R^2/4L^2}$. The circuit works only if

$$\frac{1}{LC} > \frac{R^2}{4L^2} \quad \text{or} \quad R < 2\sqrt{L/C} \ . \qquad (4\text{-}5)$$

Applications

There are many applications of SCR high-frequency generators:

1. Ultrasonic cleaning, welding, and mixing equipment.
2. Induction heaters.
3. Radio transmitters in the VLF and LF band.
4. Sonar transmitters.
5. D-C to d-c converters where the advantages of light weight, small size, low cost, and fast response due to the high-frequency link are very apparent. For instance: power supplies for computers, telephone equipment, radio transmitters, and battery chargers.
6. Step-up cycloinverter supplies. For instance: variable frequency constant-volt-second a-c supplies for driving a-c motors; h-f fluorescent lighting supplies for fluorescent lamp dimmers.

Advantages and Disadvantages of Using SCRs Instead of Tubes in h-f Generators

There are several advantages of using SCRs over tubes in h-f equipment (15). The conversion efficiency line to high-frequency signal is higher for the SCR generator comparing to tube generators. A second advantage is the elimination of high voltages, i.e., high-voltage transformers. Then, SCR generators have reduced size and weight (sometimes by a factor four); it results in lower heat losses. Heat and high voltage are a prime cause of failure in electronic equipment. Low voltage and low operating temperatures result in high reliability. SCR generators do not require delays caused by warm-up or start-up time. Also, they have larger power handling ability than tube generators.

The disadvantages of SCR h-f generators in comparing to tube types are: limited operating frequency range and producing of radio-frequency noise due to almost ideal switching characteristics of SCRs.

A Short Description of Several High-Frequency Generators Using SCRs

Thomson's Audio-Frequency Inverter

An audio-frequency (10 kHz) series inverter with a load connected in series with the commutating capacitor was first proposed by Thomson (16), but there are, also, a few

more articles concerning its applications (17), (18), (1). The original circuit is shown in Figure 16(a), however, the practical generator circuit (in Figure 16(b)) has a center-tapped capacitor, which, while not altering the basic circuit action, reduces the ripple current flowing from the supply.

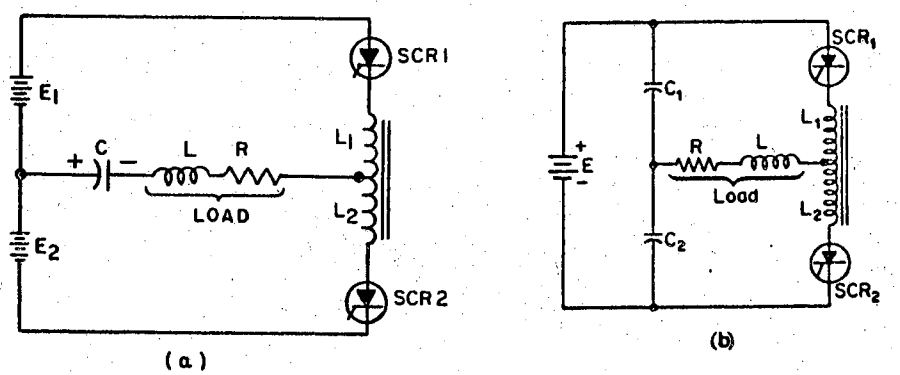
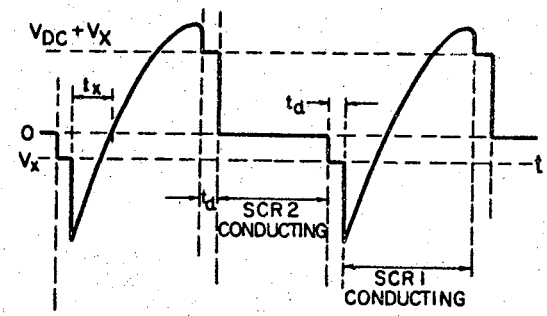


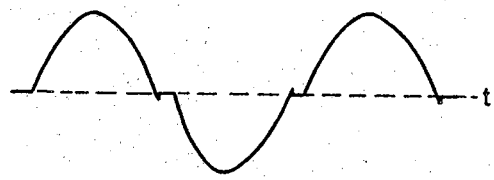
Figure 16. Original and Practical Basic Circuit of the Thompson's Inverter

Assume SCR1 (Figure 16(b)) is conducting and, as the current tries to reverse it turns off and is reverse biased by some V_X volts. After a time delay, t_d, SCR2 is fired, applying positive voltage to the left-hand side of the load. Simultaneously a voltage is developed across the bottom section of the choke of a polarity which drives the cathode of SCR1 more positive with respect to its anode during an intrinsic time delay, t_x. The waveforms of the voltages across SCR2 and the pure resistive load are shown in Figure 17. The circuit turn-off time is equal to $t_d + t_x$.

For operation of the circuit, the condition (4-5) must be satisfied.



(a) SCR 2 VOLTAGE WAVEFORM



(b) CURRENT THROUGH R

Figure 17. Idealized Waveforms of the Thomson's Inverter

The circuit described was used for high-frequency applications (17): for a d-c to d-c converter; for an ultrasonic generator driving a magnetrostrictive transducer (in this case frequency doubling is achieved by coupling the load to the center-tapped inductor).

Without special precautions, the inverter will develop a short circuit across d-c supply with light loads. At the other extreme, if load resistance is too low, circuit Q

becomes very high and can lead to excessive voltage on the SCRs; thus, this inverter requires high-voltage SCRs. A shortcoming more is that the circuit has poor load regulation since the load sees a constant-current source; also, the inverter is sensitive to reactive loads.

Sequential Inverter

This is a type of inverter (also proposed by Thomson (19)) that uses several previously described series inverters. The SCRs are triggered sequentially giving relatively long rest periods between anode-current pulses. Turn-off time of SCRs can be long; thus, SCRs with poor dynamic characteristics may be used in audio frequency inverters, or high speed SCRs may be used for radio transmitters in the VLF and LF band.

Figure 18 shows a circuit consisting of five simple inverters.

The gates are triggered sequentially 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 1, 2, etc. One of the requirements of this circuit is that the resonant circuit Q be high enough so that the voltage, to which each capacitor is charged, is greater than the peak voltage across the transformer primary. High power operation is limited to approximately 100 kHz due to the finite turn-on time and switching losses in SCRs.

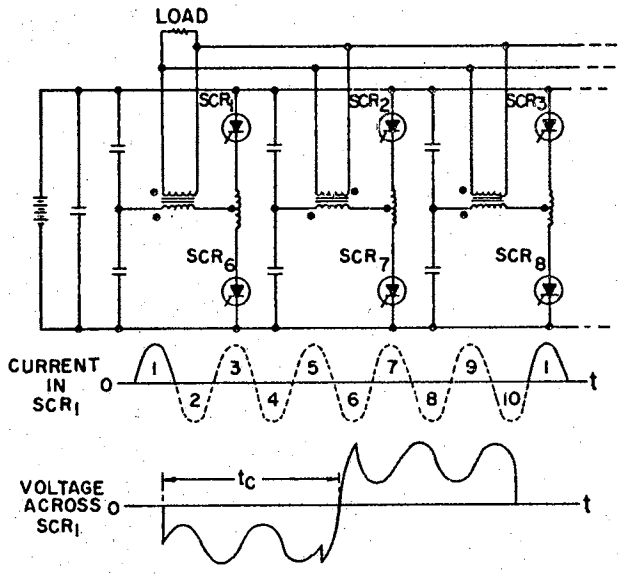


Figure 18. Sequential Inverter and Its Waveforms

Fry's Ultrasonic-Frequency Inverter

This type of inverter was developed to drive a magnetostrictive transducer of the spaced lamination type, for an ultrasonic cleaning generator (20). The basic circuit (in Figure 19(a)) has a constant-current source supplying a parallel resonance circuit and a load. A d-c blocking capacitor C_{BL} was placed in series with the load since the transducer requires a d-c bias current in order to increase the transducer efficiency.

Figure 19(b) shows how the transducer Z_L was connected into the circuit so that not only high-frequency voltage but also d-c bias current is supplied by the inverter. Because the transducer is a highly inductive load, the value of

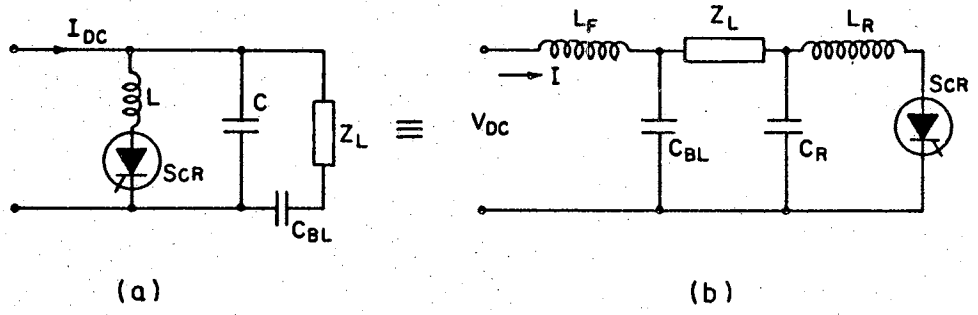


Figure 19. The Basic Parallel Resonant Circuit

C_{BL} is chosen such that partial power correction is achieved in order to reduce the a-c transducer impedance. The constant-current source was accomplished by the use of a voltage source and the choke L_F having a high impedance at the operating frequency.

Assume the resonant circuit capacitor C_R with a zero charge and SCR in its OFF state. The constant-current I will cause C_R to charge, thus applying a positive voltage to the SCR. When the C_R voltage reaches a certain value, a trigger pulse is applied to SCR causing it to go into conduction. Capacitor C_R will now discharge through the inductor L_R and will be charged in the reverse direction. The SCR will turn off and C_R now discharges at a constant-current through the power supply and then begins to charge up in a positive direction at the beginning of a new cycle. The operating frequency is $f_o \cong 19$ kHz.

The practical inverter and waveforms of its principal signals are shown in Figure 20.

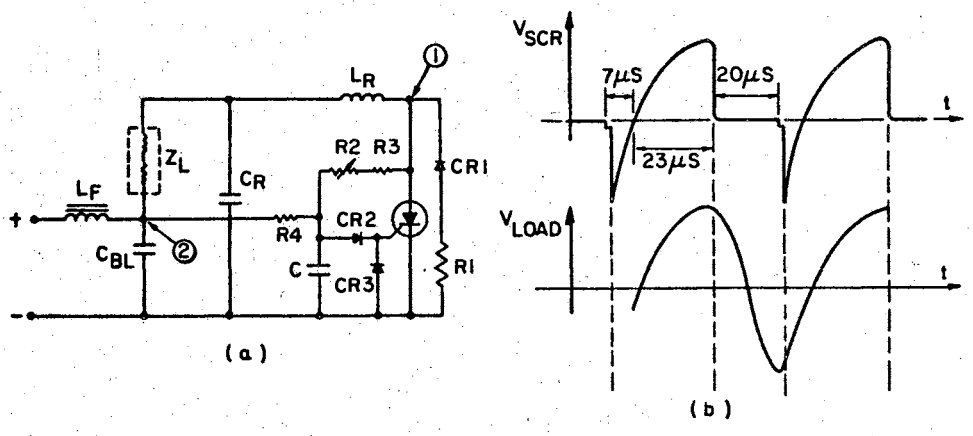


Figure 20. Fry's Ultrasonic Generator Circuit and Its Waveforms

The trigger signal for the SCR was taken, across feedback circuits, from the points 1 and 2 (in Figure 20(a)), since the signals in these points have the correct phase relationship to fire the SCR. Due to the feedback circuits the generator has the automatic frequency tracking (AFT) characteristic because the operating frequency f_o follows changes in the resonant frequency of the transducer when water level is changed due to objects being placed in the cleaning tank. Also, by changing the resistance of R2, f_o is manually adjustable from 16 to 21 kHz. The generator was designed for ultrasonic cleaning, only. In comparison with corresponding tube type generators it possesses the previously mentioned general advantages plus automatic frequency tracking ability which simplifies or completely eliminates manual tuning. The overall efficiency was increased since the ultrasonic transducer of the generator

is a magnetrostrictive device of the spaced lamination type. It has reduced the transducer impedance (usually high) as seen by the tank, thus improving its matching with radiation impedance.

The generator is not of general purpose type. It has poor load regulation and distorted sinewave output signal.

Step-Up Cycloinverter With a Synchronous Tap Changer

Step-up cycloinverters are circuits for conversion of power signal from low to high frequencies directly, without filtering the low-frequency signal. The advantages of such devices comparing to rectifier-inverter systems are eliminating the need for power filter components and commutation circuits. The serious disadvantage is: the high-frequency has the low-frequency source waveform as an amplitude-modulation envelope. This distortion needs to be removed for many applications. A synchronous tap changer is used for reduction of such distortion (21). In effect it is an active filter (Figure 21(b)) which is believed to have many advantages over a passive type filter.

The synchronous tap changer consists of a transformer with number of taps which are selected by a set of SCR switches. The peak value of secondary voltage waveform can be held constant if the turns ratio of the transformer is varied in proportion to (i.e., in syncronism with) the input envelope. This would require a tap for each cycle of high frequency. However, complexity, cost and reliability

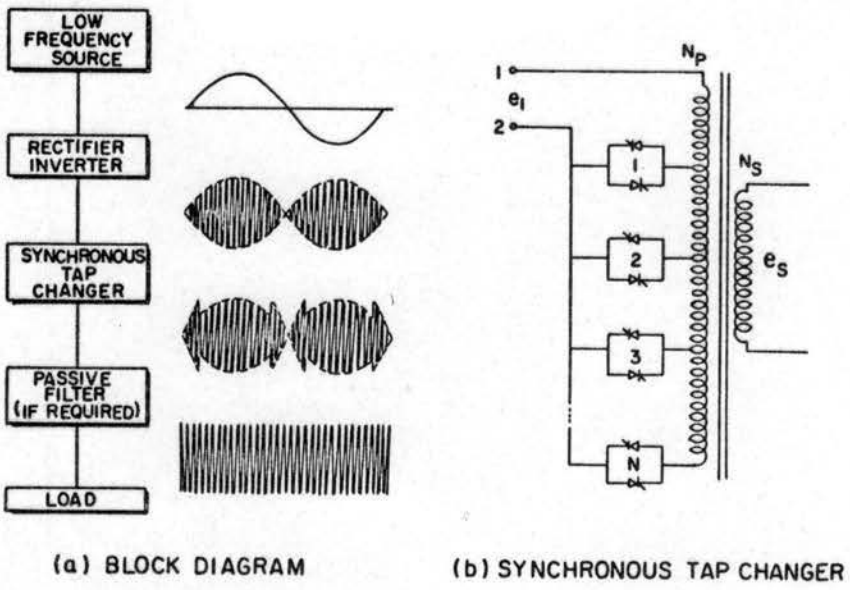


Figure 21. Step-up Cycloinverter With a Synchronous Tap Changer

considerations limit the number of taps.

The design and optimization of such systems are rather complex.

Mapham's High-Frequency Inverter Using a Single SCR

The basic circuit (in Figure 22) of this inverter is similar to the circuit shown in Figure 15(a) (22). The diode D1 serves as a path for reverse current of the capacitor C. The inductor L_2 simulates the primary inductance of an output transformer. At the cessation of diode current energy will still exist in L_2. It is transferred to capacitor C as a negative voltage with the period of $2\pi\sqrt{L_2C}$. The next time the SCR is triggered an increase in

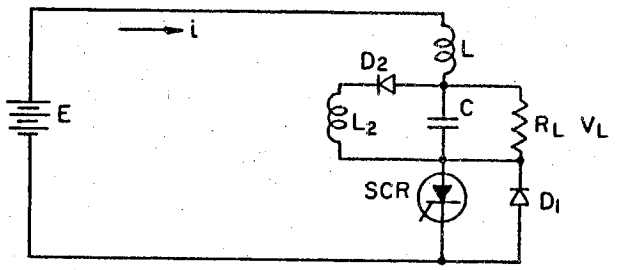


Figure 22. The Basic Circuit of the Single SCR Mapham's Inverter

the circuit current will be noticed, because the supply voltage has in effect been increased by the overshoot voltage. The currents and voltages will continue to increase each cycle until equilibrium is established. If the triggering period is made greater than $2\pi\sqrt{L_2C}$ the overshoot voltage will become of opposite direction to supply voltage, thus reducing the circuit current. In this case the output voltage would be a wavy line with a period of $\pi\sqrt{L_2C}$. The diode D_2 prevents that.

The analysis of this circuit is complicated, so it was made by using a computer.

This circuit has many advantages over previous inverters. A Mapham's inverter with two SCRs will be described and analyzed in much more detail. These two inverters have similar characteristics and calculations and conclusions for the next inverter which are also valid for this one. Of course, the inverter with two SCRs can handle with larger power than the inverter with only one SCR.

Mapham's High-Frequency Inverter Using Two SCRs

The Features of the Inverter

The good features of this inverter are (23):

1. Sine-wave output voltage.
2. Low switching losses in the SCRs.
3. Absence of misfiring because of the clean waveforms produced.
4. Ability to operate with light or no loads.
5. Having good load regulation; the load seeing a constant-voltage source.
6. Being little sensitve to reactive loads.
7. No requirements for very high-voltage SCRs when operating under heavy loads.
8. Losing of triggering pulses does not result in a short-circuit d-c voltage source.

The only shortcoming of this inverter is an increase in the SCRs required current-carrying capacity by roughly 50%.

The inverter can be used for all previously mentioned h-f generator applications at frequencies from about 1 kHz up to about 30 kHz.

Circuit Description

Figure 23 shows the circuit in its most elementary form, while Figure 24 and Figure 25 give typical circuit waveforms.

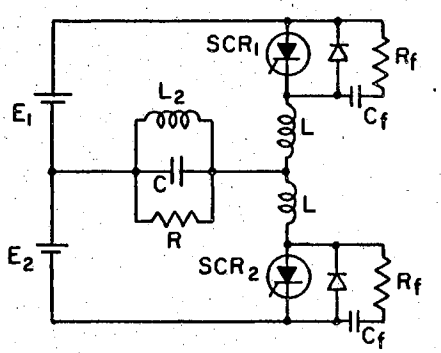


Figure 23. The Basic Circuit of the Mapham's Inverter With Two SCRs

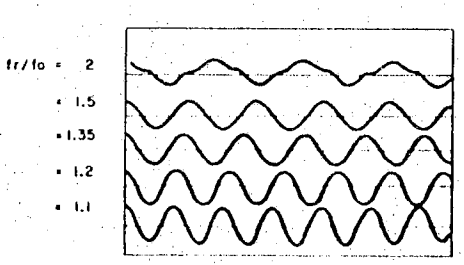


Figure 24. Output Voltage Waveforms for Different Ratios of Resonant to Triggering Frequency, f_r/f_o

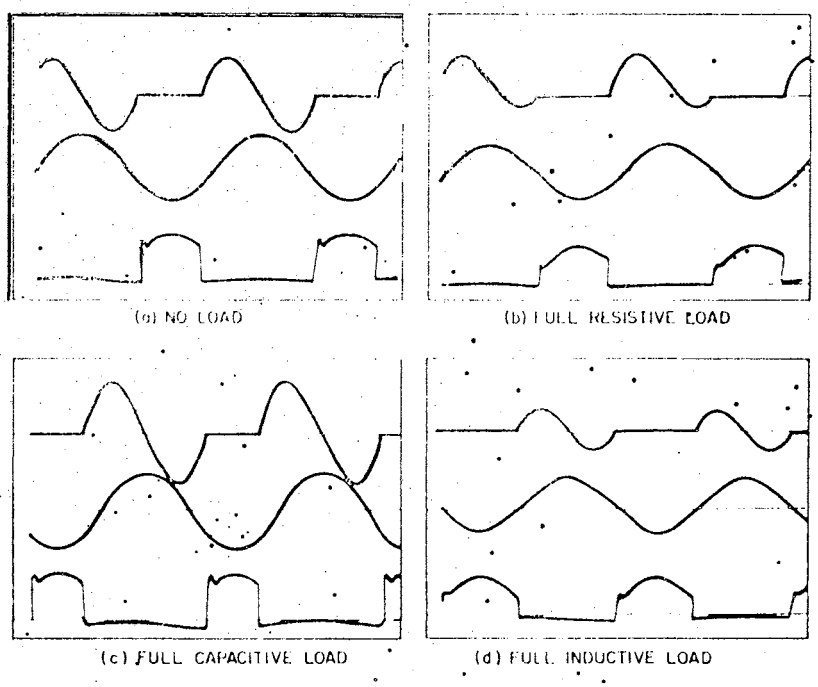


Figure 25. Circuit Waveforms of: SCR and Diode Current (top trace); Output Voltage (middle trace); and SCR Voltage (bottom trace)

The operation of the circuit is as follows. When SCR_1 is triggered, current flows from the supply E_1 charging up capacitor C to a voltage approaching $2E_1$. The current then reverses and flows back to the supply via diode D_1 and C discharges. During the reverse current flow, turn-off time is presented to SCR_1. SCR_2 is triggered next and a similar cycle occurs in the lower half of the circuit with a negative going pulse of voltage appearing across C. SCR_1 now triggered again and so the cycles repeat.

Figures 25(a) and (b) show the circuit waveforms with no load and full load, respectively. A comparison reveals

that the output voltage, and peak SCR voltage and current remain almost unchanged.

Figures 25(c) and (d) show the effect of a heavy capacitive and inductive load, respectively. Neither leading nor lagging zero power factor loads have any serious adverse effects on this inverter circuit.

Figure 23(b) shows the effect of varying the triggering frequency (f_o) on the output voltage (v_c) waveform while keeping the resonant frequency (f_r) of the LC circuit constant. Lowest distortion occurs at a ratio of $f_r/f_o = 1.35$.

As most practical applications of this inverter need an output transformer either for isolation or voltage transformation, the complete analysis ought to assume an inductance L_2, simulating the primary inductance of a transformer across the load R. Low relative values of L_2 drastically shorten the turn-off time during starting but otherwise do not have a very significant effect on the operation of the circuit.

If the inverter has a reactive load the resistive part of the load will be used as the load resistor R, while the reactive part should be combined with the capacitor C to give a new value of $C_{eq} = C \pm C''$. In Figure 26 is shown how a series resistive-inductive load was converted to an equivalent parallel circuit.

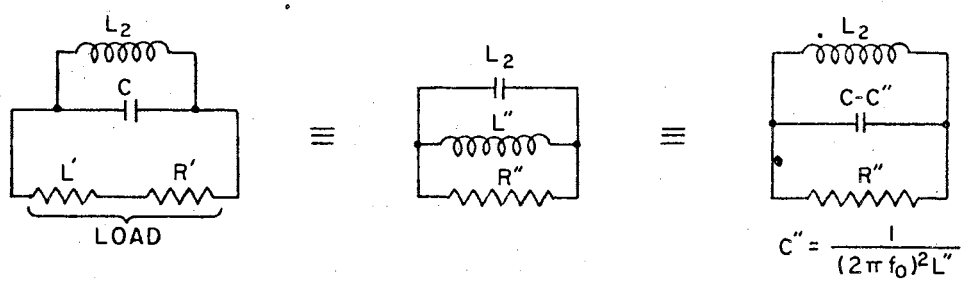


Figure 26. Conversion of Inductive Load to Equivalent Parallel Circuit

Circuit Analysis by Using the Computer Language BASIC

In the article (23) the inverter was analyzed by numerically solving the circuit with four differential equations by means of a General Electric 265 Time Sharing Computer. The opening and closing of the switches representing the SCRs and diodes were controlled by current zero-crossings. The following assumptions were made: 1. capacitors and inductors are pure and lossless; 2. SCRs and diodes turn on instantaneously, have zero voltage drop and there is no flow of reverse recovery current; 3. the power supply has zero impedance at all frequencies.

The solution is presented as a set of variables converted to normalized or dimensionless form; it enables the design data to be presented as a set of universally applicable tables with three variables: $R/\sqrt{L/C}$, f_r/f_o and L_2/L.

The following definitions of the parameters are:

I_S - peak steady-state SCR current,

I_D - peak steady-state diode current,

I_{DC} - average steady-state supply current,

V_C - peak steady-state capacitor and load voltage,

V_{Crms} - root-mean-square steady-state C and R voltage,

V_S - worst-case peak SCR forward and diode reverse voltage,

t_s - pulse-width (duty cycle) of steady-state SCR current,

t_D - pulse-width of steady-state diode current and steady-state circuit turn-off time (t_c),

t_{min} - worst-case t_c (in the first cycle of operation).

In designing an inverter one must know: the desired output power (S_o), the desired output frequency (f_o), the desired output waveform, load characteristics (phase angle, desired regulations, starting loads), the voltage of the power supply (E) and some less important characteristics.

Design Procedure

1. Choosing f_r/f_o (Figure 24): lower values of f_r/f_o give shorter t_c and higher V_S.
2. Choosing L_2/L: very low values of L_2/L (f. ex. 10) require a low-cost transformer, but t_c is shorter.
3. Choosing full-load $R/\sqrt{L/C}$: too low value of full-load $R/\sqrt{L/C}$ will economize in circulating current, but at the expense of t_c and load-regulation performance.
4. Finding I_{DC}: knowing S_o and E and assuming the efficiency of the inverter ($\eta \cong 0.9$), I_{DC} may be found from $I_{DC} = S_o/2E\eta$ amps.

5. Finding $\sqrt{L/C}$: having chosen f_r/f_o, L_2/L, and $R/\sqrt{L/C}$ the value of $I_{DC}\sqrt{L/C}/E$ may be read off from the table. As I_{DC} and E are known, $\sqrt{L/C}$ can be found.
6. Voltage and current relations: knowing $\sqrt{L/C}$ and E, the following can be found by multiplying the table values of current and voltages ratios by $E/\sqrt{L/C}$ and E, respectively: I_S, I_D, V_C and V_{Crms}.
7. Finding $\pi\sqrt{LC}$: knowing f_o, the half period of the LC circuit may be found from

$$\pi\sqrt{LC} = \frac{10^6}{2f_o \cdot f_r/f_o} \ \mu s \ (\mu H,\ \mu F \text{ and Hz units}) \ .$$

8. Time relations: as $\pi\sqrt{LC}$ is known, one may obtain t_s, t_D, and t_{min} by multiplying the table value by $\pi\sqrt{LC}$.
9. Resonant frequency: $f_r = f_o \cdot f_r/f_o$ Hz.
10. Component values: knowning $\sqrt{L/C}$ and f_r, R, L, L_2 and C are

$$R = \frac{R}{\sqrt{L/C}} \cdot \sqrt{L/C}\ \Omega \ , \qquad L = \frac{\sqrt{L/C} \cdot 10^6}{2\pi f_r} \ \mu H \ ,$$

$$L_2 = \frac{L_2}{L} \cdot L \ \mu H \ , \qquad C = \frac{10^6}{2\pi f_r \sqrt{L/C}} \ \mu F \ .$$

11. Choosing the SCR: the SCR may be specified by taking into account the values of V_S, I_S, f_o, t_s, t_{min}. The only unknown parameter dv/dt depends on the value of the $R_f C_f$ circuit in parallel with the SCR which is needed to damp out the ringing in the inductor L.
12. Choosing the diode: the diodes work hardest when the circuit is lightly loaded, hence I_D should be

calculated using the highest, possible in practice, value of $R/\sqrt{L/C}$, along with V_S, f_o and t_D. The diodes should be of the fast recovery type in order to reduce the turn-off loss, the high peak transient voltage across diodes and the radio frequency interference problem (11).

If the load momentarily presents a virtual short circuit to the inverter (rectifiers with C-input filters, incandescent lamps, and a-c motors) an additional capacitor should be connected in series with the load.

Besides the described center-tapped-supply configuration, there, also, exist center-tapped load and bridge (with four SCRs) configurations of this inverter.

Conventional Method of Circuit Analysis Assuming $L_2 \longrightarrow$ Infinity

Since a reasonably high L_2 does not have any significant effect on the operation of the circuit, in order to simplify the analysis one may assume $L_2 \longrightarrow$ infinity.

Before the circuit reaches a steady-state mode of operation, there exists a transient period which lasts a few cycles. The same equations are valid for both modes of operation but during the transient period the same intervals have different initial conditions.

Looking at the circuit shown in Figure 23, one can see that, after starting, there exist five different intervals of the operation of the circuit. These are shown in

Figure 27. For figures 4^i and 5^i the resistor and capacitor were reversed with respect to the locations of figures 2^i and 3^i. This was done to show that the same loop equations were applicable in both cases. After the 5^i, the sequence of the following intervals are again: 2^i, 3^i, 4^i, 5^i, 2^i, 3^i, ... Only the 1^i will not repeat again.

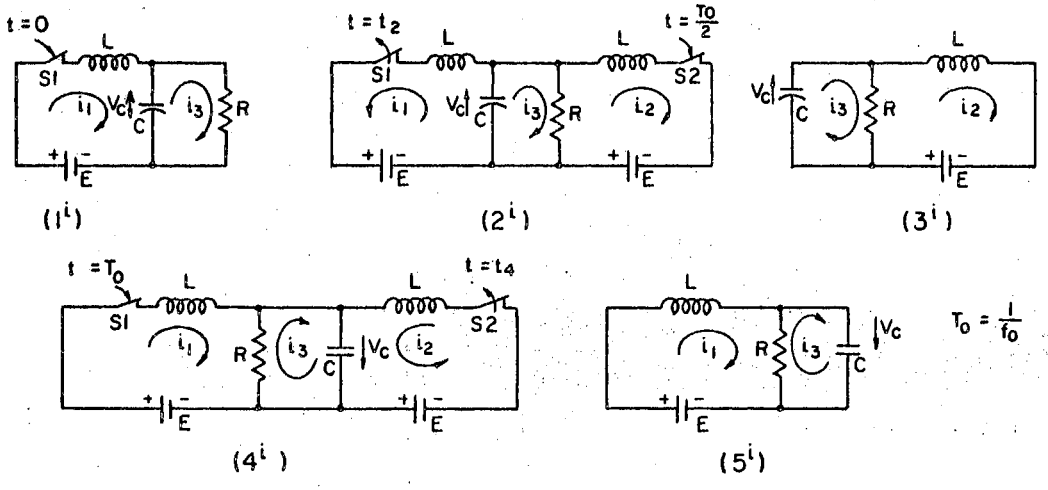


Figure 27. Five Operation Invervals of the Inverter

During the transient period the next intervals have different initial conditions from the corresponding previous intervals, but in the steady-state operation the initial conditions are the same. The same assumptions were made as well as for the analysis by using the computer language BASIC (23). The closing of the switches S1 and S2 represents,

in fact, the ceasing of the diode currents $i_1(t)$ and $i_2(t)$, respectively. The output voltage $v_c(t)$ is the voltage across the capacitor or the load.

The first interval begins with triggering SCR1 ($t_o = 0$) and lasts until SCR2 is fired ($t_1 = T_o/2$). The equations for the 1^i are:

$$L\frac{di_1}{dt} + \frac{1}{C}\int i_1 dt - \frac{1}{C}\int i_3 dt = E \ , \ i_1(0) = 0, \left(\frac{di_1}{dt}\right)_{t=0} = \frac{E}{L} \qquad (4\text{-}1)$$

$$-\frac{1}{C}\int i_1 dt + \frac{1}{C}\int i_3 dt + Ri_3 = 0 \ , \ i_3(0) = 0 \qquad (4\text{-}2)$$

$$v_c = Ri_3 \ . \qquad (4\text{-}3)$$

Solving these equations, if $R > \frac{1}{2}\sqrt{L/C}$, one may obtain:

$$i_1(t) = \frac{E}{L\omega_{r1}} \exp(-\alpha t)\sin \omega_r t + \frac{E}{R}\left[1 - \frac{1}{\sqrt{1-\xi_1}} \exp(-\alpha t) \cdot \sin(\omega_{r1} t + \theta_1)\right] \qquad (4\text{-}4)$$

$$v_c(t) = E\left[1 - \frac{1}{\sqrt{1-\xi_1^2}} \exp(-\alpha t)\sin(\omega_{r1} + \theta_1)\right] \qquad (4\text{-}5)$$

where

$\omega_{r1} = 2\pi f_{r1} = \sqrt{1/LC - (1/2RC)^2}$ is the corner resonant frequency

$\alpha = \frac{1}{2RC}$ is the damping constant

$\xi_1 = \frac{1}{2R}\sqrt{L/C}$ is the damping ratio

$\theta_1 = \cos^{-1} \xi_1$.

The initial values $i_1^o = i_1(0)$ and $v_c^o = v_c(0)$ for the next interval one can obtain putting $t = T_o/2$ in the equations (4-4) and (4-5). Thus, for the 2^i the initial conditions are: $i_1^o = i_1(T_o/2)$ and $v_c^o = v_c(T_o/2)$.

The second interval begins with triggering SCR2($t_1=T_o/2$) and lasts until $i_1(t)$ ceases (t_2). The equations for the 2^i are:

$$L\frac{di_1}{dt} + \frac{1}{C}\int i_1 dt + \frac{1}{C}\int i_3 dt = v_c^o - E \quad ,$$

$$i_1(0) = i_1^o \quad , \quad \left(\frac{di_1}{dt}\right)_{t=0} = \frac{v_c^o - E}{L} \tag{4-6}$$

$$\frac{1}{C}\int i_1 dt + \frac{1}{C}\int i_3 dt + Ri_3 - Ri_2 = v_c^o \quad ,$$

$$i_3(0) = \frac{v_c^o}{R} \quad , \quad i_2(0) = 0 \tag{4-7}$$

$$-Ri_3 + Ri_2 + L\frac{di_2}{dt} = E \tag{4-8}$$

$$v_c = R(i_3 - i_2) \quad . \tag{4-9}$$

The solution of these equations in the case that $R > \frac{1}{2}\sqrt{L/2C}$ and concerning the variables of interest, only, yields:

$$i_2(t) = \frac{(E+v_c^o)}{L\omega_{r2}}\exp(-\alpha t)\sin\omega_{r2}t - \frac{(E-Ri_1^o)}{2R\sqrt{1-\xi_2^2}}\exp(-\alpha t)\cdot$$

$$\sin(\omega_{r2}t+\theta_2) - \frac{1}{2}i_1^o + \frac{E}{L}t + \frac{E}{L\omega_{r2}}\exp(-\alpha t)\sin(\omega_{r2}t+2\theta_2) \tag{4-10}$$

$$i_1(t) = \frac{i_1^o}{2} - \frac{E}{L}t + \left(\frac{v_c^o - E}{L\omega_{r2}} + \frac{2\xi_2 i_1^o}{\sqrt{1-\xi_2^2}}\right)\exp(-\alpha t)\sin\omega_{r2}t$$

$$-\frac{i_1^o}{\sqrt{1-\xi_2^2}}\exp(-\alpha t)\sin(\omega_{r2}t-\theta_2) - \frac{(i_1^o R-E)}{2R\sqrt{1-\xi_2^2}}\exp(-\alpha t)\cdot$$

$$\sin(\omega_{r2}t+\theta_2) - \frac{E}{L\omega_{r2}}\exp(-\alpha t)\sin(\omega_{r2}t+2\theta_2) \tag{4-11}$$

$$v_c(t) = - \exp(-\alpha t) \left[\frac{v_c^o}{\sqrt{1-\xi_2^2}} \sin(\omega_{r2} t - \theta_2) + \right.$$

$$\left. + \frac{2\xi_2 R i_1^o}{\sqrt{1-\xi_2^2}} \sin\omega_{r2} t \right] \qquad (4-12)$$

where

$$\omega_{r2} = \sqrt{2/LC - (1/2RC)^2}$$

$$\xi_2 = \frac{\sqrt{2}}{4R}\sqrt{L/C} \quad \text{and} \quad \theta_2 = \cos^{-1} \xi_2 \ .$$

Since the frequency of $i_1(t)$ changes at the point $t = T_o/2$ from f_{r1} to f_{r2}, the end of the second interval (t_2) cannot be found in simple manner. One may find t_2 from the equation (4-11) putting $i_1(t_2) = 0$; by using the equations (4-10) and (4-12) the initial values for the third interval are:

$$i_2^o = i_2(t_2) \qquad \text{and} \qquad v_c^o = v_c(t_2) \ .$$

The third interval begins when $i_1(t)$ ceases (t_2) and lasts until the SCR1 is fired, again ($t_3 = T_o$). The equations which govern 3^i are:

$$L \frac{di_2}{dt} + Ri_2 - Ri_3 = E \ , \qquad i_2(0) = i_2^o \qquad (4-13)$$

$$-Ri_2 + Ri_3 + \frac{1}{C} \int i_3 dt = v_c^o \ , \ i_3(0) = \frac{v_c^o}{R} + i_2^o \qquad (4-14)$$

$$v_c = R(i_3 - i_2) \ . \qquad (4-15)$$

The solution of these equations, in the case that $R > \frac{1}{2}\sqrt{L/C}$ and concerning the variables of interest, only, yields:

$$i_2(t) = \frac{-i_2^o}{\sqrt{1-\xi_1^2}} \exp(-\alpha t)\sin(\omega_{r1}t-\theta_1) + \left(\frac{E+v_c^o}{L\omega_{r1}} + \frac{2\xi_1 i_2^o}{\sqrt{1-\xi_1^2}}\right)\exp(-\alpha t)\sin\omega_{r1}t$$

$$+ \frac{E}{R}\left[1 - \frac{1}{\sqrt{1-\xi_1^2}}\exp(-\alpha t)\sin(\omega_{r1}t+\theta_1)\right] \qquad (4-16)$$

$$v_c(t) = -E + \frac{(E+v_c^o)}{\sqrt{1-\xi_1^2}}\exp(-\alpha t)\sin(\omega_{r1}t+\theta_1) - \frac{2\xi_1(v_c^o+Ri_2^o)}{\sqrt{1-\xi_1^2}}\exp(-\alpha t)\sin\omega_{r1}t. \qquad (4-17)$$

The initial values i_2^o and v_c^o for the next interval one may obtain putting $t = T_o$ in the equations (4-16) and (4-17).

From the Figure 27 it is obvious that for the 4^i and 5^i valid the same equations derived for the 2^i and 3^i, respectively, if one replace i_1 by i_2 and vice versa and reverse the polarity of $v_c(t)$ and (v_c^o) thus considering the upper end of the circuit as the lower and vice versa.

After several cycles the circuit will reach its steady state of operation.

In order to design the inverter by using the conventional circuit analysis one should, for the given requirements (d-c voltage supply E, output power and frequency and load resistance — in the case of reactive loads, the load reactance should be added to the value of C) choose $R/\sqrt{L/C}$ and f_r/f_o, and from these conditions find L and C of the circuit. Then by using the derived equations one should determine when the steady-state operation is reached. From the steady-state equation (4-17) one may obtain V_{Crms} and

V_C (from $dv_c/dt = 0$). The values I_S, I_D can be found from the steady-state equations (4-10), (4-11) and (4-16) and the value of V_S by adding E to V_C (in fact the worst case V_S may happen during one of the transient cycles; so one must take it into account). The circuit turn-off time $t_c = t_D$ one may obtain from the steady-state equations (4-16) and (4-11), but the worst case $t_c = t_{min}$ one should evaluate from the equations (4-4) and (4-11) for the 1^i and 2^i. The duty cycle t_s of the SCRs can be found from the steady-state equations (4-10) and (4-16).

As it is obvious the analysis is rather complex, even assuming $L_2 \longrightarrow$ infinity.

The typical waveforms for the circuit with a resistive load with the operation intervals are shown in Figure 28.

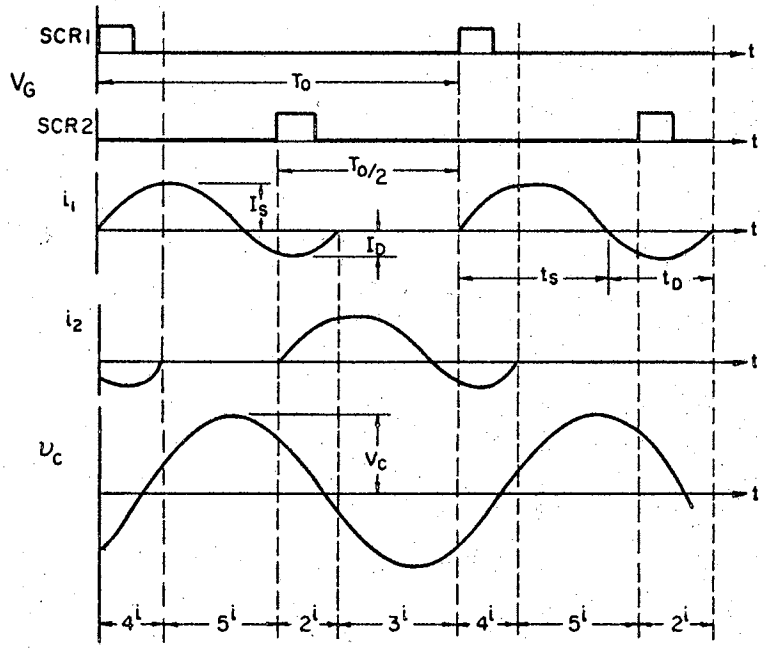


Figure 28. Waveforms for Circuits of Figure 27.

Circuit Analysis by Using the IBM System/360 Continuous System Modeling Program (S/360 CSMP)

S/360 CSMP is a problem-oriented program designed to faciliate the digital simulation of continuous process on large-scale digital machines (24). The program provides an application-oriented language that allows these problems to be prepared directly and simply from either a block-diagram representation or a set of ordinary differential equations. Simplicity and flexibility are characteristics of this language, which was designed for use specifically by the engineer or scientist who is familiar with analog computer simulations. S/360 CSMP requires only a minimum knowledge of computer programming and operation.

As is well known, an analog computer simulation of the system allows system parameters to be varied at will, and provides a relatively quick and inexpensive way of optimizing the system parameters for a given application. The author suggests the use of S/360 CSMP for an analysis of SCR inverter circuits. All operation intervals of the Mapham's inverter can be represented by their block diagrams; then using S/360 CSMP programs for each operation interval and defined E, R, L, C one may obtain the graphical solutions of the equations describing corresponding intervals. It is an easy task to find, from these plots, the important values of the inverter: I_S, I_D, V_C, t_D, t_s and from V_C to calculate V_S and V_{Crms} taking into account that for the ratios

$f_r/f_o = 1.5,\ 1.35,\ 1.2,\ V_C/V_{Crms} \cong 1.44,\ 1.40,\ 1.36,$ respectively.

Of course, as well as for the conventional method of analysis, one should consider the intervals until the circuit reaches its steady-state operation. The initial conditions for every next interval should be picked up from the corresponding previous interval.

After little rearrangements of the equations (4-1, 2, 3, 6, 7, 8, 9, 13, 14, 15) one may draw the block diagrams and write the programs for each interval. For example: $T_o = 100\mu s$, $E = 75V$, $R = 12.5\Omega$, $L = 30\mu H$, $C = 4.7\mu F$. (Note all summers and integrators are non-inverters with gain = 1.)

1^i

$$\frac{d^2 i_1}{dt^2} = -\frac{1}{LC} i_1 + \frac{1}{LC} i_3 \qquad i_1(0) = 0,\ \left(\frac{di}{dt}\right)_{t=0} = \frac{E}{L} \qquad (4\text{-}18)$$

$$\frac{di_3}{dt} = -\frac{1}{CR} i_3 + \frac{1}{CR} i_1 \qquad i_3(0) = 0 \qquad (4\text{-}19)$$

$$v_c = Ri_3 \,. \qquad (4\text{-}20)$$

Let $i_1 = C1$, $i_3 = C3$, $v_c = C4$, $di_1/dt = X1$, $di_3/dt = X3$, $d^2i_1/dt^2 = X4$, $i_1(0) = IC1$, $i_3(0) = IC3$, $(di_1/dt)_{t=0} = IC4$, $1/CR = K1$, $1/LC = K2$, $R = K3$.

The block diagram for 1^i is shown in Figure 29.

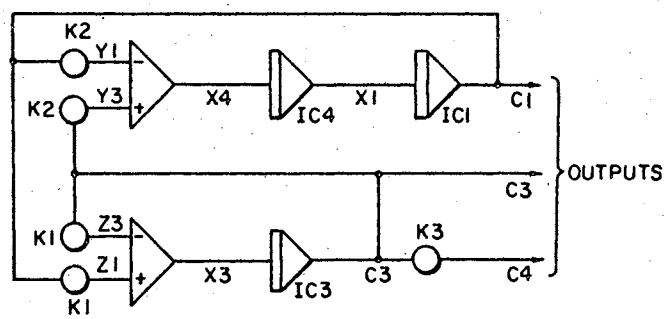


Figure 29. Block Diagram for the First Interval

$\underline{2^i}$

$$\frac{d^2 i_1}{dt^2} = -\frac{1}{LC} i_1 - \frac{1}{LC} i_3, \quad i_1(0) = i_1^o, \quad \left(\frac{di_1}{dt}\right)_{t=0} = \frac{v_c^o - E}{L} \tag{4-21}$$

$$\frac{di_3}{dt} = -\frac{1}{RC} i_3 - \frac{1}{RC} i_1 + \frac{di_2}{dt}, \quad i_3(0) = \frac{v_c^o}{R} \tag{4-22}$$

$$\frac{di_2}{dt} = -\frac{R}{L} i_2 + \frac{R}{L} i_3 + \frac{E}{L}, \quad i_2(0) = 0 \tag{4-23}$$

$$v_c = R(i_3 - i_2) . \tag{4-24}$$

Let $i_1 = C1$, $i_2 = C2$, $i_3 = C3$, $v_c = C4$, $di_1/dt = X1$, $di_2/dt = X2$, $di_3/dt = X3$, $d^2i_1/dt^2 = X4$, $i_1(0) = IC1$, $i_2(0) = IC2$, $i_3(0) = IC3$, $(di_1/dt)_{t=0} = IC4$, $1/CR = K1$, $1/LC = K2$, $R = K3$, $R/L = K4$, $E/L = K5$.

The block diagram for 2^i is shown in Figure 30.

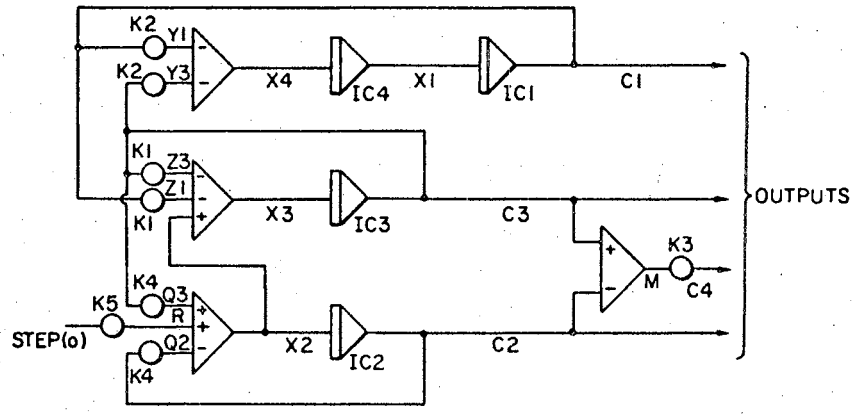


Figure 30. Block Diagram for the Second Interval

3^i

$$\frac{di_2}{dt} = -\frac{R}{L} i_2 + \frac{R}{L} i_3 + \frac{E}{L}, \quad i_2(0) = i_2^o \tag{4-25}$$

$$\frac{di_3}{dt} = -\frac{1}{RC} i_3 + \frac{di_2}{dt}, \quad i_3(0) = i_3^o = \frac{v_c^o}{R} + i_2^o \tag{4-26}$$

$$v_c = R(i_3 - i_2) . \tag{4-27}$$

Let $i_2 = C2$, $i_3 = C2$, $v_c = C4$, $di_2/dt = X2$, $di_3/dt = X3$, $i_2(0) = IC2$, $i_3(0) = IC3$, $1/CR = K1$, $R = K3$, $R/L = K4$, $E/L = K5$.

The block diagram for 3^i is shown in Figure 31.

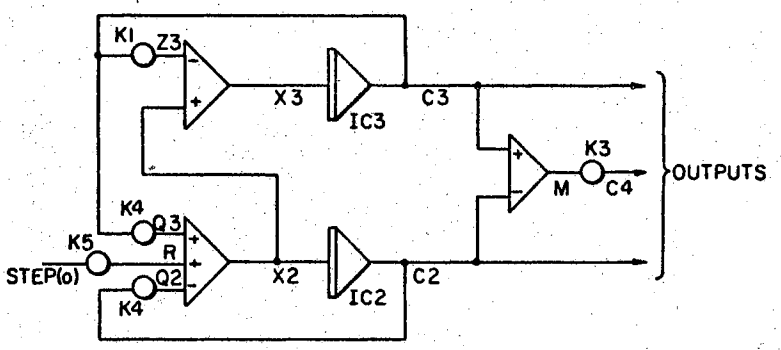


Figure 31. Block Diagram for the Third Interval

The programs are given in Table I for the seven intervals. As well as in the case of the conventional method of analysis the 4^i and 5^i are similar to 2^i and 3^i, respectively. One should substitute i_1 for i_2 and i_2 for i_1 and take into account that for 4^i $i_3^o = i_2(T_o) - i_3(T_o) = -v_c(T_o)/R$ and $v_c = -R(i_3-i_1)$. It is obvious that similar SCR inverter circuits may also be analyzed by using the S/360 CSMP in the manner described.

Trigger Circuits for h-f SCR Generators

In order to decrease the turn-on switching losses there are special requirements for trigger circuits, which are specified by manufacturers. For example, for the "General Electric" high-frequency SCRs C140 and C141 the characteristics of a gate supply should be: 20 volts open circuit, 20 ohms, square wave pulse with a minimum width of 1.5 μsec and a maximum rise time of 0.1 μsec.

TABLE I

S/360 CSMP PROGRAMS FOR THE OPERATION INTERVALS

```
****CONTINUOUS SYSTEM MODELING PROGRAM****

***PROBLEM INPUT STATEMENTS***

TITLE  HIGH-FREQUENCY SCR GENERATOR. FIRST INTERVAL

  INITIAL
  CONST  K1=17000.,K2=7092.E+06,K3=12.5
  INCON  IC1=0.,IC3=0.,IC4=25.E+05

  DYNAMIC
         X4=Y3-Y1
         X3=Z1-Z3
         X1=INTGRL(IC4,X4)
         C1=INTGRL(IC1,X1)
         C3=INTGRL(IC3,X3)
         C4=K3*C3
         Y1=K2*C1
         Y3=K2*C3
         Z1=K1*C1
         Z3=K1*C3
  TERMINAL
    TIMER DELT=5.E-08,FINTIM=55.E-06,PRDEL=5.E-07,OUTDEL=5.E-07
    PRTPL C1,C3,C4
    PRINT C1,C3,C4
         METHOD RKSFX
         END
         STOP

TITLE  HIGH-FREQUENCY SCR GENERATOR. SECOND INTERVAL

  INITIAL
  CONST  K1=17000.,K2=7092.E+06,K3=12.5,K4=416667.,K5=25.E+05
  INCON  IC1=8.6,IC2=0.,IC3=8.2,IC4=89.E+04

  DYNAMIC
         X4=-Y1-Y3
         X3=X2-Z1-Z3
         X2=R-Q2+Q3
         X1=INTGRL(IC4,X4)
         C1=INTGRL(IC1,X1)
         C2=INTGRL(IC2,X2)
         C3=INTGRL(IC3,X3)
         C4=K3*M
         R=K5*STEP(0)
         Y1=K2*C1
         Y3=K2*C3
         Z1=K1*C1
         Z3=K1*C3
         Q2=K4*C2
         Q3=K4*C3
         M=C3-C2
  TERMINAL
    TIMER DELT=5.E-08,FINTIM=55.E-06,PRDEL=5.E-07,OUTDEL=5.E-07
    PRINT C1, C2, C3, C4
    PRTPL C1, C2, C3, C4
         METHOD RKSFX
         END
         STOP

TITLE  HIGH-FREQUENCY SCR GENERATOR. THIRD INTERVAL

  INITIAL
  CONST  K1=17000.,K3=12.5,K4=416667.,K5=25.E+05
  INCON  IC2=52.3,IC3=51.78

  DYNAMIC
         X3=X2-Z3
         X2=R-Q2+Q3
         C2=INTGRL(IC2,X2)
         C3=INTGRL(IC3,X3)
         C4=K3*M
         R=K5*STEP(0)
         Z3=K1*C3
         Q2=K4*C2
         Q3=K4*C3
         M=C3-C2
  TERMINAL
    TIMER DELT=5.E-08,FINTIM=55.E-06,PRDEL=5.E-07,OUTDEL=5.E-07
    PRINT C2, C3, C4
    PRTPL C2, C3, C4
         METHOD RKSFX
         END
         STOP
```

TABLE I (Continued)

```
TITLE  HIGH-FREQUENCY SCR GENERATOR. FOURTH INTERVAL

      INITIAL
      CONST  K1=17000.,K2=7092.E+06,K3=12.5,K4=415557.,K5=25.E+05
      INCON  IC1=0.,IC2=28.42,IC3=9.67,IC4=153.E+04

      DYNAMIC
             X4=-Y2-Y3
             X3=K1-Z2-Z3
             X1=R-Q1+Q3
             X2=INTGRL(IC4,X4)
             C1=INTGRL(IC1,X1)
             C2=INTGRL(IC2,X2)
             C3=INTGRL(IC3,X3)
             C4=K3*M
             R=K5*STEP(0)
             Y2=K2*C2
             Y3=K2*C3
             Z2=K1*C2
             Z3=K1*C3
             Q1=K4*C1
             Q3=K4*C3
             M=C1-C3
      TERMINAL
        TIMER DELT=5.E-08,FINTIM=55.E-06,PRDEL=5.E-07,OUTDEL=5.E-07
        PRINT C1, C2, C3, C4
        PRTPL C1, C2, C3, C4
             METHOD RKSFX
             END
             STOP

TITLE  HIGH-FREQUENCY SCR GENERATOR. FIFTH INTERVAL

      INITIAL
      CONST  K1=17000.,K3=12.5,K4=416667.,K5=25.E+05
      INCON  IC1=50.67,IC3=44.01

      DYNAMIC
             X3=K1-Z3
             X1=R-Q1+Q3
             C1=INTGRL(IC1,X1)
             C3=INTGRL(IC3,X3)
             C4=K3*M
             R=K5*STEP(0)
             Z3=K1*C3
             Q1=K4*C1
             Q3=K4*C3
             M=C1-C3
      TERMINAL
        TIMER DELT=5.E-08,FINTIM=55.E-06,PRDEL=5.E-07,OUTDEL=5.E-07
        PRINT C1, C3, C4
        PRTPL C1, C3, C4
             METHOD RKSFX
             END
             STOP

TITLE  HIGH-FREQUENCY SCR GENERATOR. SIXTH INTERVAL

      INITIAL
      INCON  IC1=25.74,IC2=0.,IC3=7.48,IC4=62.E+04
      CONST  K1=17000.,K2=7092.E+06,K3=12.5,K4=416667.,K5=25.E+05

      DYNAMIC
             X4=-Y1-Y3
             X3=X2-Z1-Z3
             X2=R-Q2+Q3
             X1=INTGRL(IC4,X4)
             C1=INTGRL(IC1,X1)
             C2=INTGRL(IC2,X2)
             C3=INTGRL(IC3,X3)
             C4=K3*M
             R=K5*STEP(0)
             Y1=K2*C1
             Y3=K2*C3
             Z1=K1*C1
             Z3=K1*C3
             Q2=K4*C2
             Q3=K4*C3
             M=C3-C2
      TERMINAL
        TIMER DELT=5.E-08,FINTIM=55.E-06,PRDEL=5.E-07,OUTDEL=5.E-07
        PRINT C1, C2, C3, C4
        PRTPL C1, C2, C3, C4
             METHOD RKSFX
             END
             STOP

TITLE  HIGH-FREQUENCY SCR GENERATOR. SEVENTH INTERVAL

      INITIAL
      CONST  K1=17000.,K3=12.5,K4=416667.,K5=25.E+05
      INCON  IC2=45.11,IC3=40.76

      DYNAMIC
             X3=X2-Z3
             X2=R-Q2+Q3
             C2=INTGRL(IC2,X2)
             C3=INTGRL(IC3,X3)
             C4=K3*M
             R=K5*STEP(0)
             Z3=K1*C3
             Q2=K4*C2
             Q3=K4*C3
             M=C3-C2
      TERMINAL
        TIMER DELT=5.E-08,FINTIM=55.E-06,PRDEL=5.E-07,OUTDEL=5.E-07
        PRINT C2, C3, C4
        PRTPL C2, C3, C4
             METHOD RKSFX
             END
             STOP
```

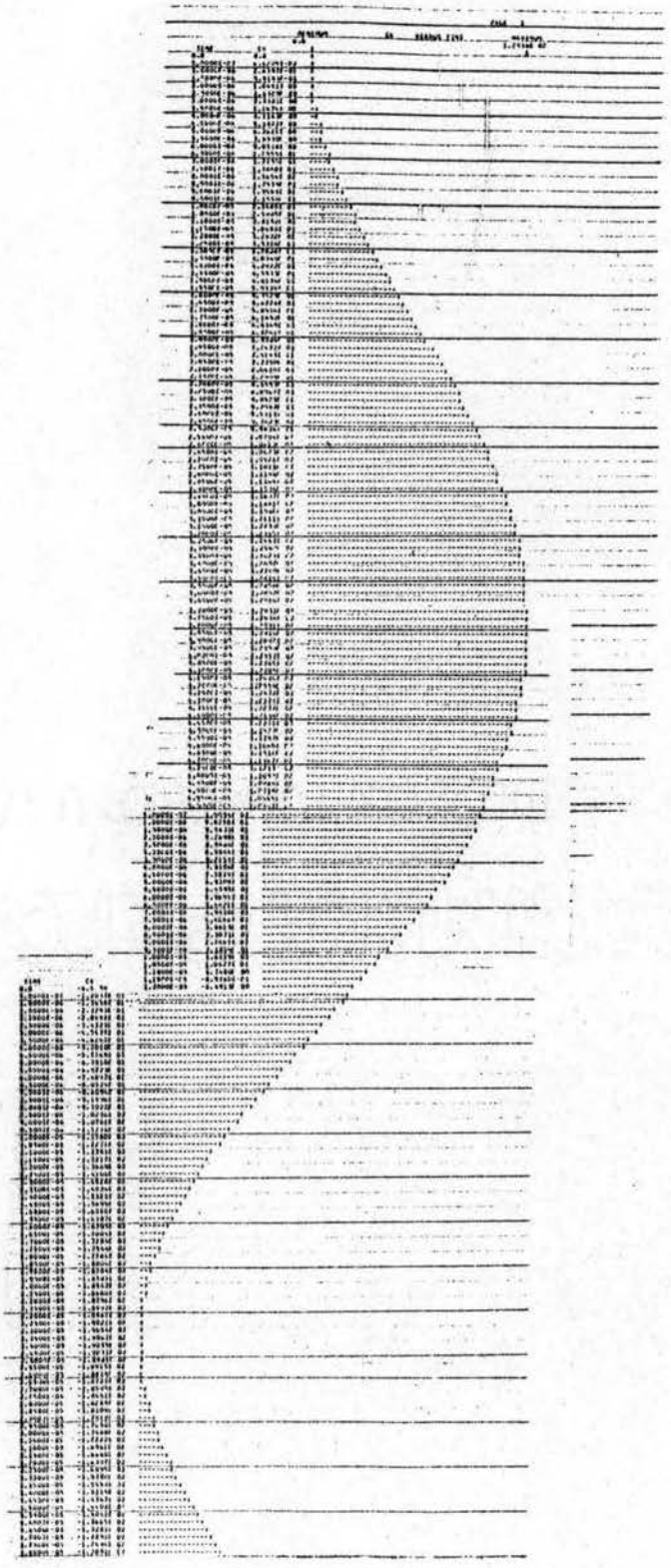


Figure 32. CSMP Plot of the Inverter's Output Voltage

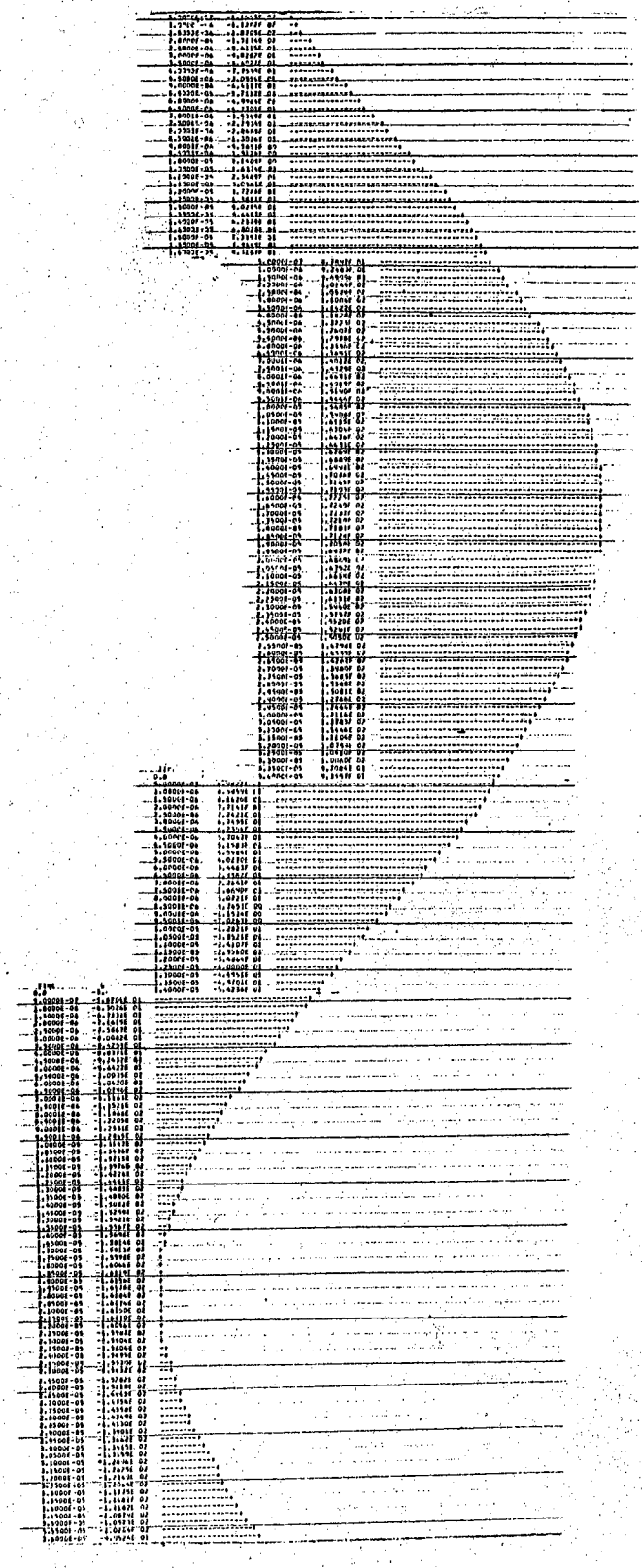


Figure 32. (Continued)

A simple variable-frequency trigger circuit with a unijunction transistor for triggering of a single SCR (in Figure 33(a)) can be used up to about 3 kHz, because the timing circuit RC has its limitations: 1. $R \geq 3.2$ K ohms is needed for the operating of a unijunction transistor oscillator, and 2. $C \geq 0.1$ μF since a lower value of capacitance cannot provide enough current for a gate of a medium- or high-current SCR.

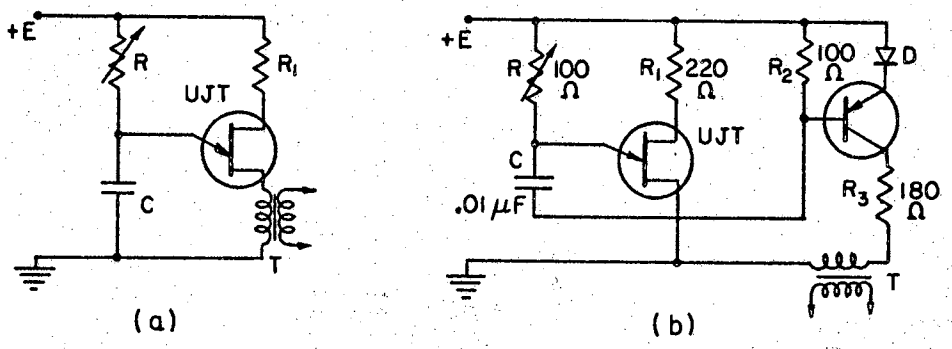


Figure 33. UJT Oscillator Trigger Circuits for SCRs

In Figure 33(b) is shown a modified UJT oscillator trigger circuit for variable high-frequency (about 20 kHz) triggering of a single SCR (25).

However, high-frequency inverters usually have two (or four) SCRs and, thus, they require a dual-pulse trigger circuit with two outputs, having the 180° phase relationship between their corresponding pulses. Several dual-pulse

trigger circuits using conventional transistors have been developed (4) (16). Some of them have blocking oscillators on their outputs, thus providing fast rising output pulses suitable for high-frequency SCR inverters.

A simple SCR trigger circuit is shown in Figure 34 (26). The frequency of the output pulses is defined by the expression

$$f = \frac{(V_{be} + i_b R_b) \cdot 10^8}{4 B_m A N_b}$$

where V_{be} is the base to emitter voltage of the transistors in volts; i_b is the base current of the transistors in amps; B_m is the maximum flux density in gauss; A is the core area in cm^2; and N_b is the number of turns.

Because V_{be} is relatively insensitive to oscillator d-c input voltage E and load current, the frequency of the output pulses f is independent of E and the load. However, by varying the value of the resistor of R the frequency variation can be achieved from 10 kHz to 20 kHz. Also, the frequency variation or precise frequency control may be obtained by using a voltage-regulating transistor instead of the $R_b C_b$ circuit.

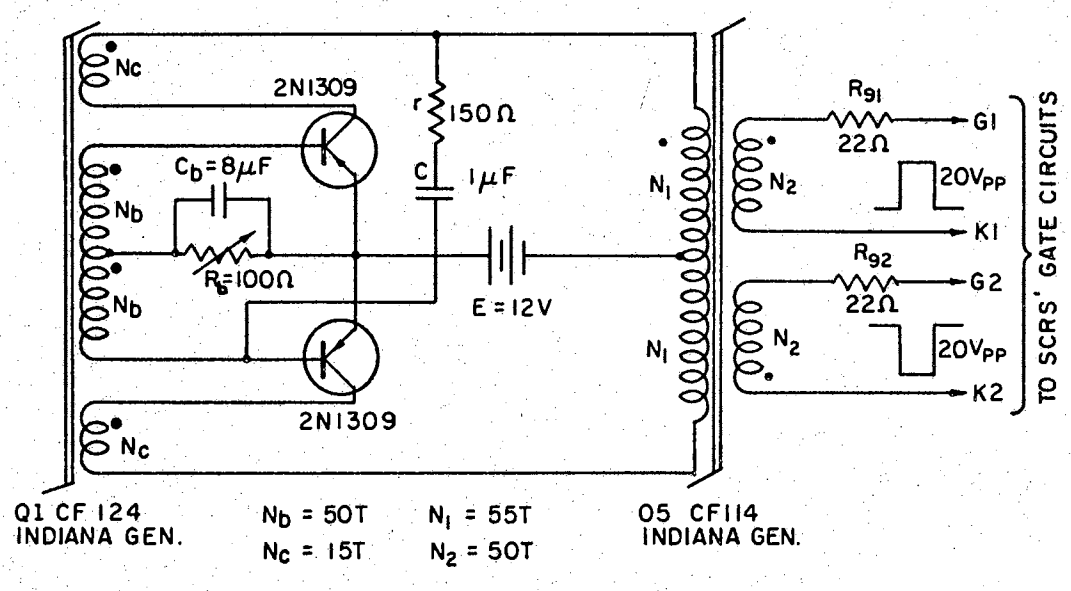


Figure 34. Simple Trigger Circuit for h-f SCR inverters

CHAPTER V

SUMMARY AND CONCLUSIONS

High-frequency operation of silicon controlled rectifiers has become important in industrial applications of power semiconductors. For such purposes special high-frequency SCRs should be used with high-frequency performance curves which take into account all dynamic parameters which affect the operation of the SCR at high-frequencies.

Several h-f SCR generators have been developed. Some of them are useful for one kind of application but not for others. Mapham's SCR inverter with two SCRs seems to be the most versatile and universal h-f generator for applications where a h-f voltage source with good regulation and sine-wave is required.

At present, there is no published complete study covering all of the problems associated with the h-f operation of SCRs. The author has presented a theoretical study of this field and has provided the reader with main references for further and deeper investigations of particular problems in the area of the production of h-f SCRs, as well as in the area of their industrial applications. Thus, the author hopes that this work may serve as a basic theory of h-f operation of SCRs. In addition, the author has

developed and presented a technique for relatively simple analysis of some SCR inverter circuits which uses the computer language S/360 CSMP which, it is believed, sometimes has advantages over a conventional method of analysis and an analysis by using pure digital computer languages.

The main problems in future investigations would be the practical realization of h-f SCR generators for ultrasonic applications such as ultrasonic welding, cutting, drilling, soldering and cleaning equipment. Such applications impose special load requirements such as: self-tuning, impedance matching, etc., on h-f generators. Most of such problems have not been properly solved, even for tube generators.

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