TIME SHARE TESTING OF NO. 1 ELECTRONIC SWITCHING SYSTEM CONTROL FRAMES

By

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TIME SHARE TESTING OF NO. 1

ELECTRONIC SWITCHING SYSTEM

CONTROL FRAMES

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PREFACE

This project involved the development of a computer-controlled test set for Western Electric's No. 1 Electronic Switching System. The prime objective was to develop a versatile time-sharing system to replace the dedicated test set, thereby reducing the time needed for systems testing.

The author wishes to take this opportunity to express his appreciation to his thesis adviser, Professor Paul McCollum, for his guidance and helpful suggestions during the preparation of this thesis. Also, a note of thanks is extended to the other members of the committee, Dr. Ed Shreve and Dr. James Rowland.

The author extends a note of acknowledgement to Dr. Richard Cummins for his assistance and advice throughout the course of study.

Thanks and appreciation go to Mr. Bob Sloan, Department Chief, Electronic Apparatus Testing, Western Electric Oklahoma City Works. Also, thanks are extended to fellow engineers for their helpful comments.

Special acknowledgement is especially due to my wife, Jo, for her understanding and constant encouragement, which were a great source of strength to me. She skillfully assisted me by making valuable suggestions in regard to the grammatical construction and proper thesis format. She sacrificed many long hours diligently typing the early drafts and the final preparation of this manuscript.

Finally, special gratitude goes to my dedicated wife, Jo, our son, Mike, and our twins, Kit and Kim, who often sacrificed their "family-time" in order that I could pursue my graduate studies, in addition to my work at Western Electric.

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NOMENCLATURE

ARO	Accumulator Register Matcher 0
AR1	Accumulator Register Matcher 1
ASCII	American Standard Code for Information Interchange
AUBO	Automatic Bus 0 Enable
AUR	Auxiliary Register
BCD	Binary Coded Decimal
BOWD	Buffer Order Word Decoder
BOWR	Buffer Order Word Register
BR	Buffer Register
CC	Central Control
CCAT	Central Control Automatic Test Program
CCDT	Central Control Data Transfer Program
CH	Homogeneity Flip-Flop
CRT	Cathode Ray Tube
CS	Sign Flip-Flop
DAC	Digital-to-Analog Converter
DEC	Digital Equipment Corporation
DRO	Data Register Matcher 0
DR1	Data Register Matcher 1
DTL	Diode Transistor Logic
ESS	Electronic Switching System
FR	First One Register
IAOR	Index Adder Output Register

IOT	Input-Output Transfer
LR	Logic Register
MAD	Memory Address Decoder
MB	Masked Bus
MM1	Match Mode One
MM2	Match Mode Two
MM3	Match Mode Three
PAR	Program Store Address Register
PDP 8/I	Programmed Data Processor 8/I
PSBO	Program Store Bus 0 Enable
PU	Peripheral Units
PUAT	Peripheral Units Address Translator
SP	Signal Processor
SPAT	Signal Processor Automatic Test Program
SPDT	Signal Processor Data Transfer Program
SR	Switch Register
TI	Texas Instruments Incorporated
TTL	Transistor Transistor Logic
TXT	Text Transfer Program
UB	Unmasked Bus

CHAPTER I

INTRODUCTION

In April of 1970 the author went to Chicago, Illinois, to make an evaluation of a Central Control-Signal Processor test set designed by an engineer at Western Electric's Hawthorne Works. The test set was designed using Integrated Circuit logic, a CRT display, and a Bright Industries magnetic tape reader for test data information. At this time the prototype had been in prove-in for five months.

Later many questions remained. Because the test set could not be completed in time for testing to start on the frames, the shipping date would be delayed. Therefore, it was decided that a test system could be designed incorporating features from the author's Central Control test set (SID 324959-1-1; also referred to as system 959) and the Hawthorne Works' set resulting in more versatility. In addition, the Hawthorne set would be used to fulfill our testing needs.

The proposed system will use a magnetic tape as this provided the test set with the ability to rapidly process large quantities of test information. It will utilize the system 959 switches and cabinets plus the redesign of the discrete component DTL logic to TTL logic for speed and space saving of the IC chips.

As it turned out, the decision to build a test system proved to be the best solution. The Hawthorne set could not be completed and proved-in by the end of 1970, which was the shipping date for the

first frame. The test system designed at the Oklahoma City Works fulfilled immediate needs, so the Hawthorne set was sent to the Dallas Works as they also needed a test set. They got it working after replacing the magnetic tape reader with a paper tape reader. Now another test set would be needed to meet testing requirements. The first test set designed at the Oklahoma City Works was the SID 324975-1-1 (also referred to as system 975-1); the second one which is explained in this paper was the SID 324975-2-1 (also referred to as system 975-2). The system 975-2 is a modification of the system 975-1. The system 975-2 changes the 975-1 from a single position test set to a time-sharing test set.

CHAPTER II

DESCRIPTION OF CENTRAL CONTROL AND SIGNAL PROCESSOR FRAMES

The SID 324975-1-1 is a computer controlled test set presently used to test the J1A037 A and B frame (Central Control) and the J1A049 A and B frames (Signal Processor). The Central Control can be described as a 44 bit general purpose computer used to control and maintain a No. 1 Electronic Switching System central office. The Signal Processor is a 24 bit highly specialized frame used during busy-hour calling to do the repetitive routine of call processing handled by the Central Control during low-traffic periods. In an ESS No. 1 office two Central Controls are required; one is the on line control unit, the other is standing by and if a problem develops, the units switch so as to have continuous service.

The Signal Processor handles the simple highly repetitive and time consuming supervisory and nonsupervisory scanning function of the system. By relieving the Central Control of this work, it greatly increases the over-all capacity of the system. The Signal Processor controls the line, trunk, and junctor scanners for supervision and the Signal Distributors for trunk and junctor control. It can perform functions to operate the Central Pulse Distributor and also make directed scans. The Signal Processor has its own Call Store which stores the supervisory data along with call information such as counts of dialed digits and numbers to be

outpulsed. When the Signal Processor reaches a point on a particular call which requires Central Control to take over processing, it enters the proper information in a buffer register which is interrogated periodically by the Central Control. Similarly, the Central Control can stop the Signal Processor and enter requests that certain tasks be performed.

ESS No. 1 is DTL, discrete component, + 24 volts D.C. and + 4.5 volts D.C. logic mounted on printed wiring boards. The circuit packs have 28 pins on a single side and are inserted into the 905A connector. The 905A connector is the test access to the frame. The test points used for frame control and monitoring are the outputs of gates or flip-flops. The inputs to the Central Control is the Buffer Order Word Register which is decoded to give the operational instructions. These inputs go into an A-11 circuit pack. The A-11 will receive a clear and then a 0.125 microsecond low going pulse which will set the A-11.

The Central Control on the ESS No. 1 is a three-phase, 5.5 microsecond cycle time computer with instructions that can be from one to four cycles in length. The block diagram of the Central Control is similar to a computer with additional registers. The Central Control has a complete arithmetic and logic unit, a 20 bit program counter, 23 registers used for maintainence of the ESS office, and other special registers such as: First One, J,K,X,Y,Z, Rotate and Shift.

The Signal Processor has a block diagram similar to the Central Control except it has no maintainence register and fewer special registers. The Signal Processor has a logic register but no program counter, as it has two registers controlled by the Central Control for communication between the two frames. The input to the Signal Processor is the

24 bit Instruction Register which under operating conditions receives inputs from the Central Control.

The first design work the author performed was to lay out a printed wiring board to access the input points on the two frames. The boards were fitted with coaxial cables with noise reducing capacitors and TI SN7416Ns which are hex inverter buffers/drivers with open collector high-voltage outputs. The pull up resistor is part of the DTL logic on the frames.

CHAPTER III

DESCRIPTION OF THE COMPUTER CONTROLLED TEST SET

A. Block Diagram Description

Figure 1 is a block diagram, as originally conceived, of the system 975-1 as used on the first test set. The binary decks were the special IBM cards used which contained the test information for the Central Control and the Signal Processor. Figure 2 shows a Central Control and a Signal Processor card (note that the test information was stored in binary on each row of the card). The test information was read from the cards using an IBM model 519 card reader. The test data is rearranged and then stored on dectape. The way the test information was stored is given in Table I and Table II. Table I is the dectape block storage map for the Central Control, and Table II is the dectape block storage map for the Signal Processor. The tables show that each frame has different length blocks on the dectape. This was handled by writing two additional programs needed to format the tape and thus get our test information from IBM cards to dectape.

The card reader PDP 8/I interface was designed using Digital Equipment Corporation (DEC) M series logic. It performs the necessary logic functions and buffering needed to interface the IBM card reader with the PDP 8/I computer. The biggest problem was the interface of the plus 40 volts of the card reader with the 5 volt logic of the computer. This was accomplished by using a voltage divider circuit and then

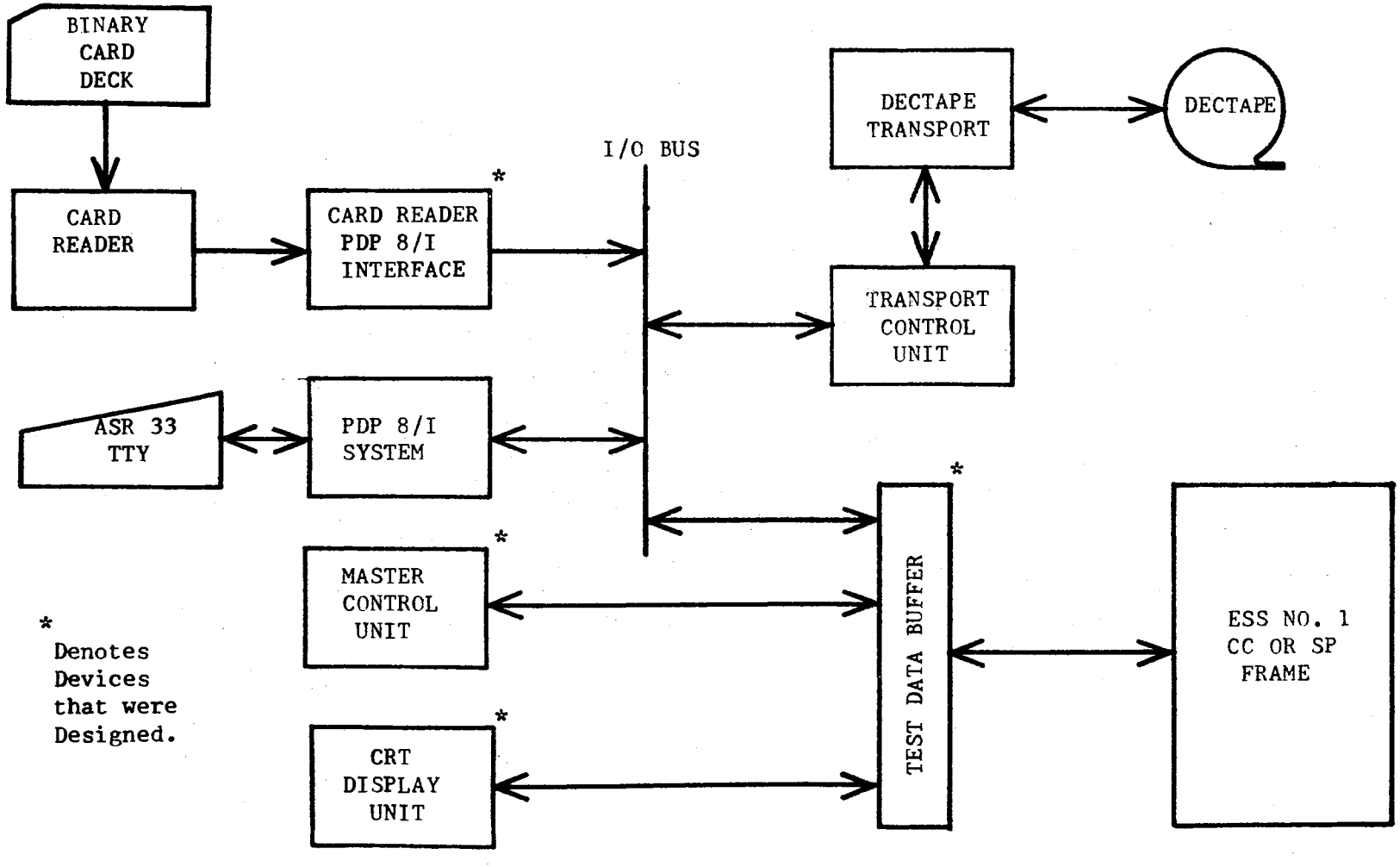

Figure 1. Block Diagram of System 975-1

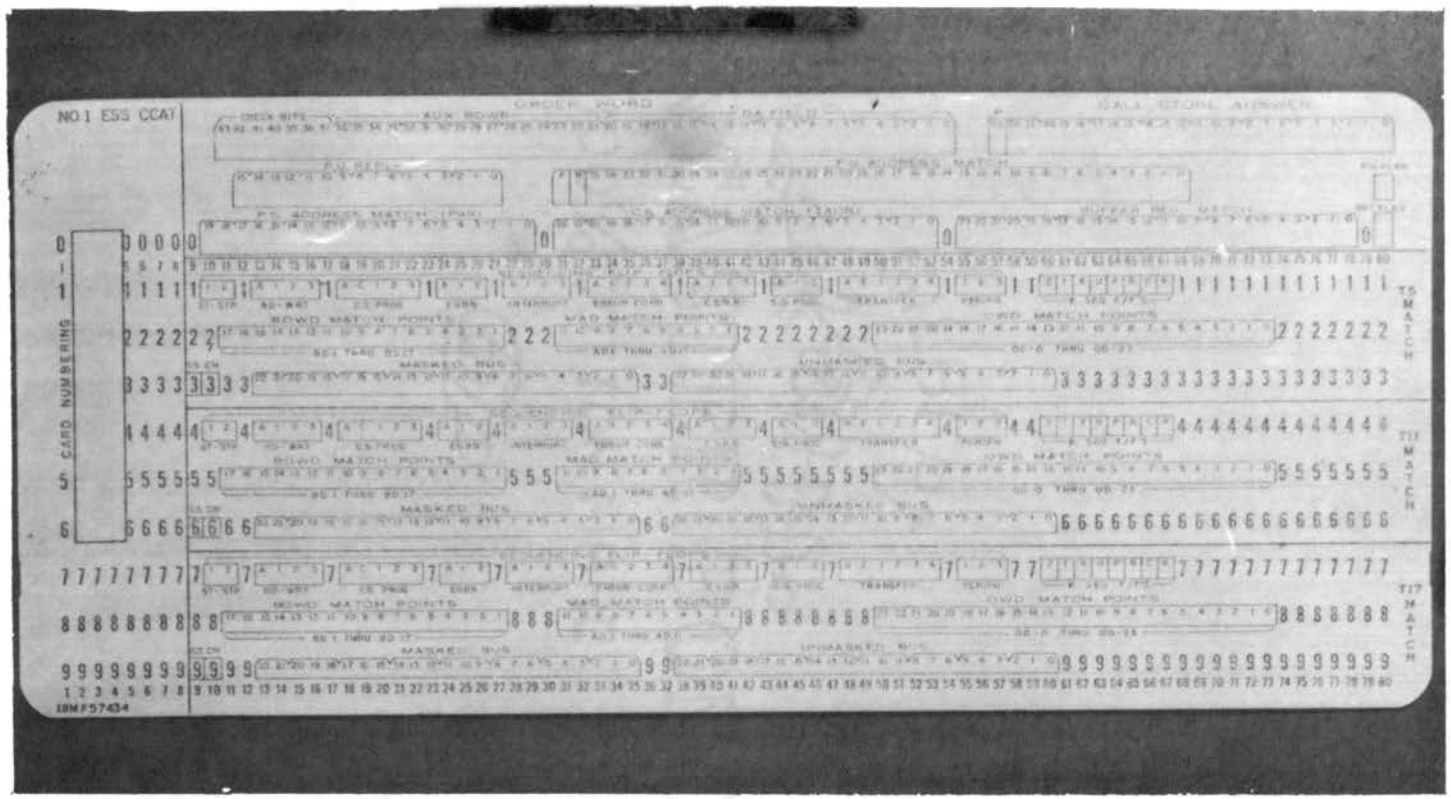

Figure 2(a). CCAT Card Used for Central Control Testing

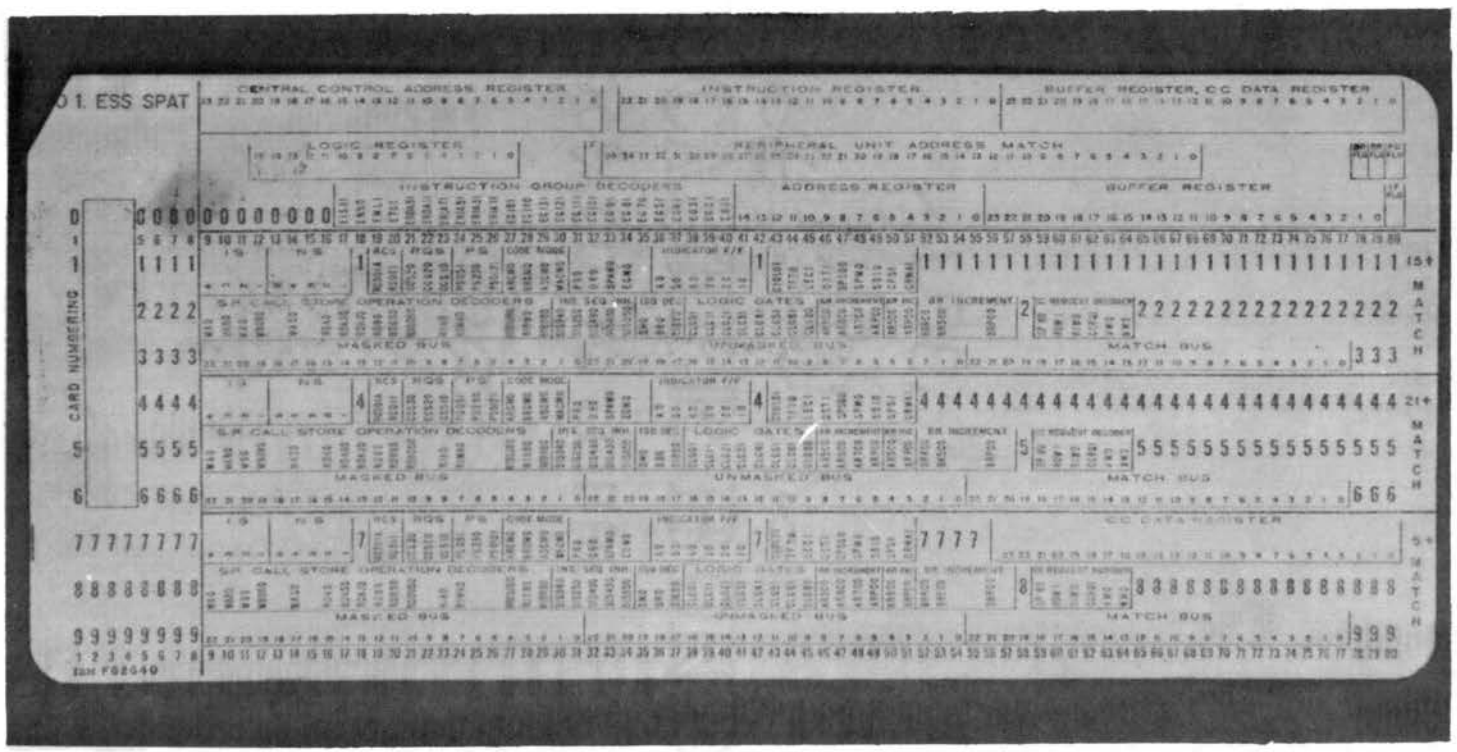

Figure 2(b). SPAT Card Used for Signal Processor Testing

TABLE I

DECTAPE BLOCK STORAGE MAP OF THE CC

Word	Information Stored
ØØ	Deck Number (ASCII)
Ø1	Deck Number (ASCII)
Ø2	Sequence Number (Packed ASCII)
Ø3	Sequence Number (Packed ASCII)
Ø4	Card Number (Packed ASCII)
Ø5	Card Number (Packed ASCII)
Ø6	BOWR 43-32
Ø7	BOWR 31-23, 3 Spares
1Ø	1 Spare, BOWR 22-12
11	BOWR 11-ØØ
12	CS ANS 23-12
13	CS ANS 11-ØØ
14	LR 15-Ø4
15	LR Ø3-ØØ, 8 Spares
16	1 Spare, F, R, PUAT 35-27
17	PUAT 26-15
2Ø	PUAT 14-Ø3
21	PUAT Ø2-ØØ, 9 Spares
22	1 Spare, PAR 19-Ø9
23	PAR Ø8-ØØ, 3 Spares
24	1 Spare, IAOR 22-12
25	IAOR 11-ØØ
26	BR 23-12
27	BR 11-ØØ
3Ø	EGBN A,1,2 - RDWRT A,1,2,3 - CS PROG A,C,1,2,3
31	K SEQ F/F2,1,X,U,P,R,C,K, 4 Spares
32	SIG PROC A,1,2 - INTERRUPTA,1,2,3 - ERROR COR A,1,2,3,4
33	ST - STP 1,2 - TRANSF A,E,1,2,3,4 - 4 Spares
34	PERIPH 1,2,3 - CSRR A,1,2,3 - T5 - T11 - T17, 2 Spares
35	1 Spare, BOWD 17-Ø7
36	BOWD Ø6-Ø1, 6 Spares
37	1 Spare, MAD 11-Ø1
4Ø	OWD 23-12
41	OWD 11-ØØ
42	CH, MB 22-12
43	MB 11-ØØ
44	CS, UB 22-12
45	UB 11-ØØ

TABLE I (Continued)

Word	Information Stored
46-63	(Format same as 3Ø-45)
64-1Ø1	(Format same as 3Ø-45)
1Ø2	FLAGS: PU, INIT, Col 61 - Row 9 (From previous card) 9 Spares
1Ø3	ØØØØ
1Ø4	ØØØØ

Number of Words (Decimal) = 69

2526_{10} Blocks/Tape

4736_{8} Blocks/Tape

TABLE II

DECTAPE BLOCK STORAGE MAP OF THE SP

Word	Information Stored
ØØ	Deck Number
Ø1	Deck Number
Ø2	Card Number (ASCII)
Ø3	Card Number (ASCII)
Ø4	Card Number (ASCII)
Ø5	Card Number (ASCII)
Ø6	AR23 - AR12
Ø7	AR11 - AR00
1Ø	I22 - I11
11	I10 - I00, 1 Spare
12	CCBR/DR23 - CCBR/DR12
13	CCBR/DR11 - CCBR/DR00
14	LR15 - LR04
15	LR03 - LR00, 8 Spares
16	2 Spares, FCG0, PUAT (35-27)
17	PUAT (26-15)
2Ø	PUAT (14-03)
21	PUAT (02-00), 9 Spares
22	INSTR GRP DCD E1SA1 - EG140
23	INSTR GRP DCD EG131 - EG11
24	9 Spares, AR14 - AR12
25	AR11 - AR00
26	BR23 - BR12
27	BR11 - BR00
3Ø	RC301, RC011, CCS30, CCS20, CCS10, IS4-IS1, NS5-NS3
31	NS2, NS1, C10L01-CRMA1, 1 Spare
32	KR5C0, KRPC0, PS051-WACM0, IF/FA0-IF/F40
33	IF/F30-IF/F10, CLG01-CLG80, 1 Spare
34	2 Spares, SM0-C16X0,PR0-ECM0, 1 Spare, S1S940, S1S250
35	S1S490-S1S850, RDB0-R1BRB0, 1 Spare
36	2 Spares, BR4C0-BRPC0, AR5C0-ARPC0, SP60-R1W0
37	1 Spare, WA0 - RDAJ0, CCR01 - NM0
4Ø	1 Spare, MB22 - MB12
41	MB11 - MB00
42	1 Spare, UB22 - UB12
43	UB11 - UB00
44	1 Spare, MAB22 - MAB12
45	MAB11 - MAB00
46	ØØØØ
47	ØØØØ

TABLE II (Continued)

Word	Information Stored
5Ø-67	(Format same as 30-47)
7Ø-1Ø7	(Format same as 30-47)
11Ø	CCDR23 - CCDR12
111	CCDR11 - CCDRØØ
112	FLAGS: DR, BR, PU, IF, 8 Spares
113	ØØØØ

Number of Words (Decimal) - 75

2358_{10} Blocks/Tape

4466_{8} Blocks/Tape

buffering it so that its output would be in the four to five volt range. The interface was only used on this first test set as now a small card reader has been purchased for another PDP 8/I. Although this card reader does not have the mass reading ability of the IBM model 519 it will be adequate to make any minor changes in test data that may result from modification to the Central Control or Signal Processor frames.

Figure 3 shows the System 975-1 as it is now being used at the Oklahoma City Works. The ASR33 teletypewriter is the method of communication between the tester and the computer. On the left is the two dectape transports; one has the test data tape, while the other has the diagnostic information tape. In the center is the PDP 8/I computer and above it is two drawers containing the DEC logic both for the card reader interface and some of the control and buffer logic. On the right is the CRT display unit and below it is the master control panel. Below the control panel and behind the black panels are three Auget planes of logic used for control and transmit. On the back side of the test set directly behind the black panels are two more Auget planes of logic used for the CRT display. Directly behind the CRT display is a specially designed double-sided printed wiring board containing the master clock, character generator and D to A convertors used for the CRT.

Taking each item in order, a brief description of its function within the system 975-1 will be given. The dectape transport and reader was purchased from DEC ready to interface directly with the PDP 8/I computer. The PDP 8/I computer was purchased from DEC and is a 12 bit mini-computer. It has 8K of core memory, and it came supplied with a

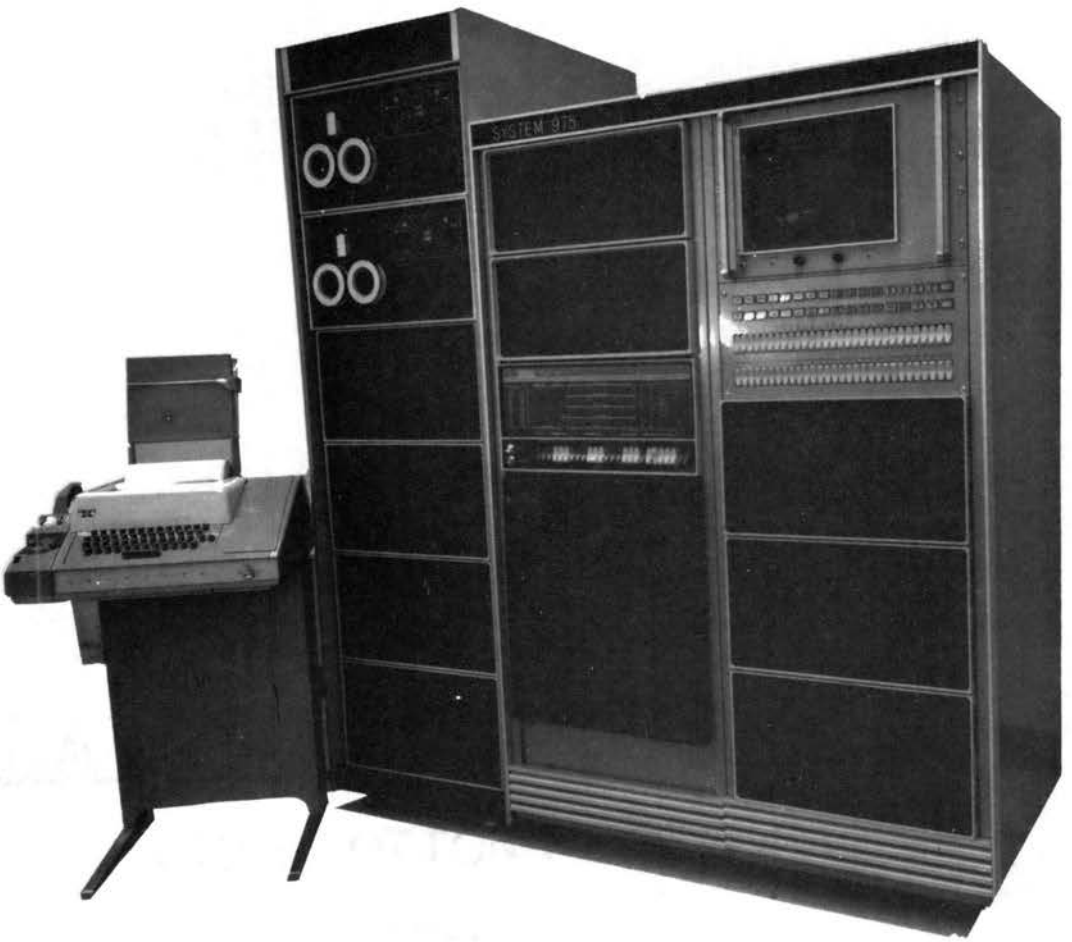

Figure 3. System 975-1

complete software package for using it as a standard computer.

The DEC drawers were wired by DEC to desired specifications from a wiring list made from the logic diagrams. The M series logic also came from DEC, and the drawers had to be proved in to verify that the logic diagram would work and that also no wiring errors were made in the drawers.

B. Control Panel and Logic

From this point on the logic and hardware design can be compared with the old dedicated test sets used to test either the Central Control or the Signal Processor. The control logic for most of the testing is very similar; except the system 975 uses TI TTL logic where the old test sets used A packs as used in the ESS No. 1 system. The switches used are Master Speciality with either a locking switch or a holding coil which is used for interlocking the switches electrically. R-C networks were used to remove noise or contact bounce in order to use the TTL chips. These switches replace the old mechanical interlocking switches and rotary type switches. Another improvement was to replace rows of binary switches used as input conditions to the frame with a set of octal coded switches used to load shift registers. The shift register is enabled by selecting the correct switch. The switches are labeled Word 1, Word 2, Word 3, Word 4, Buffer Register, Logic Register, CC Data Register, CC Instruction Register, and External Match Register. The Words 1, 2, 3, and 4 are used to load the shift registers in order to have the necessary number of cycles needed to complete any instruction. As mentioned before the Central Control instructions could take from one to four cycles to complete. When the tester has

to troubleshoot a problem he wants to be able to repeat the instruction that fails over and over until he finds the trouble.

These shift registers are tied in serial form except for the first SN7495 which is used in parallel load from the octal key and is then shifted three places by the local oscillator when the key is released. The three bit octal code is loaded and then shifted by what might be called a local oscillator built from a Motorola M 832P which is a four input expander gate. There are two gates on each chip. All the inputs except one are tied to the five volts. The exception is the output of a flip-flop. The outputs have a 1,000 pf capacitor between them and the expander gate on the other chip as shown in Figure 4. The change in the enable lead starts the oscillator and is disabled by the output from the J-K counter. This circuit allows three shift pulses to be generated and then is turned off. After the key is released a clear pulse resets the J-K flip-flops and the enable flip-flop which is used to trigger the local oscillator.

There are four strings of shift registers with 44 outputs for the four-word registers on the Central Control. The Buffer Register, CC Data Register, Instruction Register, and External Match Register have 24 outputs on their string of shift registers. The Logic Register is a short one as it has only 16 outputs on its string of SN7495s. Some of the other keys and switches on the panel are used for frame control. The set of switches marked monitor, cycle, or phase is used to control the mode of the frame.

In monitor the frame is under its own clock and can run at system speed. In cycle the frame can only perform one complete cycle for each clock advance pulse given from the test set. In phase the frame can

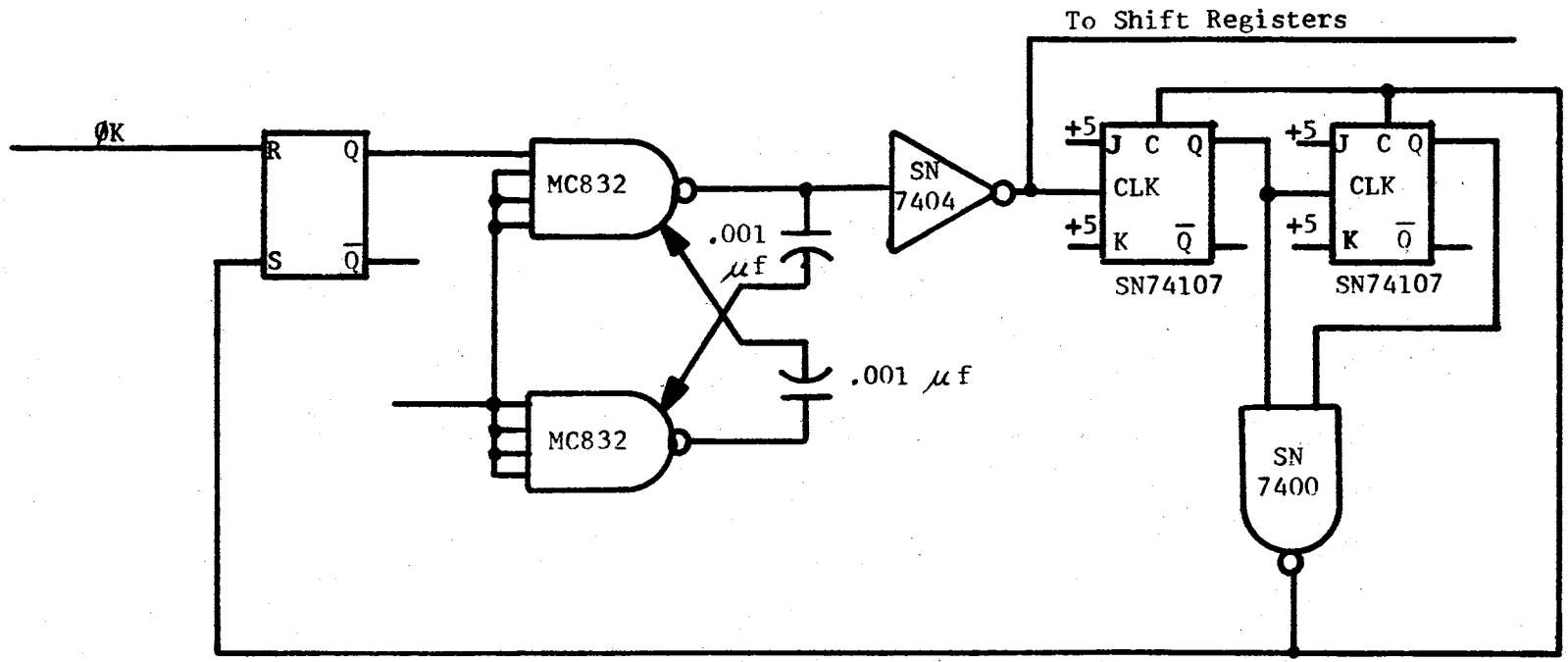

Figure 4. Local Oscillator

only perform each phase of a cycle with a clock advance pulse from the test set. The four switches for Cycle Select Word One to Cycle Select Word Four allow for cycling the necessary number of words used in troubleshooting the frame. If only a single cycle was needed to be repeated, then Cycle Select Word One is chosen. However, if three cycles were needed, then Cycle Select Word Three would be chosen and three instructions would be repeated in order so that the tester could locate the trouble. There is four other switches used with these and they are the Sync Select Word One to Sync Select Word Four. These are tied to an external connector so that the tester's oscilloscope can be triggered on the correct cycle when he is trying to locate trouble.

There are two more switches for control, one marked Central Control, the other marked Signal Processor. These are used in the logic to enables leads. The Central Control switch operates the make contacts of a power relay which gives power to the ICs on the CC cords. The Signal Processor cords get their power from the break contacts of the relay. The two switches used on the CRT will be discussed when explaining the CRT display. The other two rows are keys, some special purpose and some general. The first group includes Manual Clock Advance, AUBO (Automatic Bus 0 Enable), Forced Parity, Word Generator Reset, Inhibit Word Generator Advance, Octal keys 0 to 7, and the Load key. The second row is the 30 Flip-Flop Control keys used only on the Central Control.

The Manual Clock Advance is used to advance the frame clock one position. The AUBO is a control lead to the frame and is used only under manual testing. The Forced Parity is used when starting to test the frame. Once some degree of sanity is obtained, the Forced Parity

is released which unlocks the parity generator circuit of the frame. The Word Generator Reset merely resets the word generator to Word One while the Inhibit Word Generator holds the word generator at the same word when this key is operated. The Octal keys are used to load the registers while the Load key is used to load the information in the selected registor to the frame.

In the old CC test set the Flip-Flop Controls were a switch that grounded the output of a flip-flop in the frame and the switch would be set up by the tester after he had run the initialization part of the test deck. This circuit was designed so that either the computer or the tester using the key could control the frame flip-flops. When running a test, at the end of the initialization the computer sets the appropriate flip-flops for that deck and continues testing without interruption. The circuit is simple using cross-tied nand gates as an R-S flip-flop and the inputs for setting or resetting is a nand circuit of the computer IOT pulse or the output of the key. There are two decks of the Central Control; during testing some of the control flip-flops have to be changed. By using this method the procedure for testing is greatly simplified.

C. Test Cord Problem

Due to the card reader interface there was not enough room in the drawers to be able to give each input lead from the received cords individual gates. It was decided that the CC and SP receive cords would be wired together and the tester could remove the test cords not being used, as wired OR in TTL does not work.

The idea was conceived that the TTL would work in a wired OR if

the power and ground were removed from one of the chips. That is, either the Central Control receiver cords or the Signal Processor cords would have power. None of the engineers in the department could definitely say what would happen in this case, so the author went to the Engineering Laboratory and investigated this solution. The circuit shown in Figure 5 was used and the following procedures were followed.

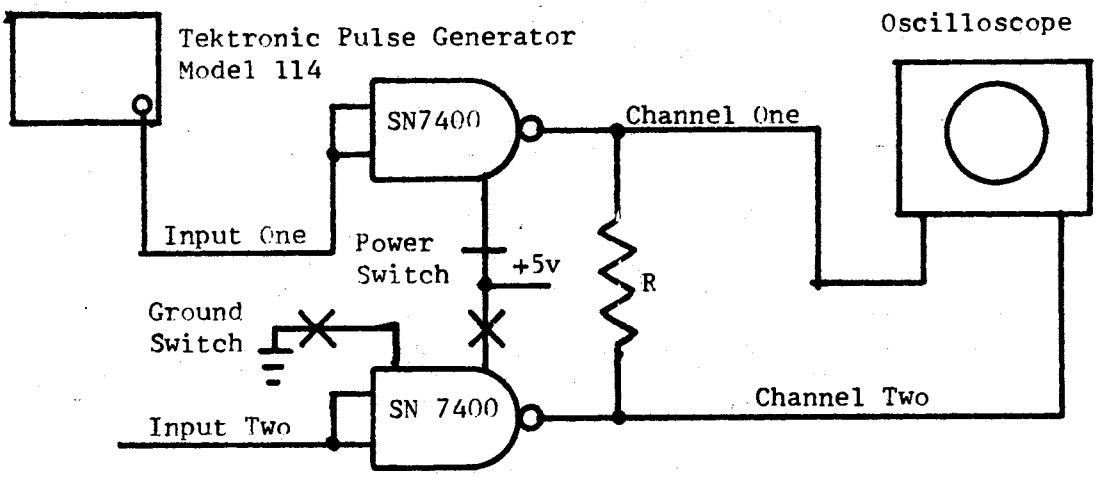

Figure 5. Circuit for Investigation of Wired OR

A tektronic pulse generator was used with a pulse width of 100 nanoseconds and period of 1.0 microsecond with amplitude of 4 volts. When applying this to input of the gate with the power switch and the ground switch in the normal state some distortion could be observed on channel two of the oscilloscope. Upon operating the ground switch to the make position, the distortion disappeared from channel two of the oscilloscope. Then switching the pulse generator to input two and changing the power switch from normal to make the output was the same as before.

After observing this method of removing power from the unused gate the wired OR would work. The next step was to remove the resistor and wire OR the output of the two gates. Performing the same tests there was no change from the previous results. This circuit was ran for several hours and then changing inputs and power ran the circuit for the rest of the day and by evening the gates were checked and it was found that there had been no damage to either chip and the responses were correct and as expected.

D. CRT Display Description

After discussing the CRT display, the hardware portion of the test set will have been completely covered. The CRT display is a Hewlett Packard Model 1300A X-Y Display. The screen is used as a 64 x 32 major matrix with each point in the major matrix being a 5 x 7 dot matrix which is called the minor matrix. There are four formats for the screen; two are for the Central Control and two are for the Signal Processor. The first eight columns of each row is for ASCII characters except for the last two rows. They are all ASCII characters thus any message up to 64 characters can be displayed in these bottom two rows. However, only four ASCII characters can be displayed as every other column is blanked. In most cases only two or three characters are needed to identify the register or group of test points as acronymns are widely used by the testers. This would be the case where BR is the Buffer Register and LR the Logic Register. The rest of the rows have been divided into 24 displayable characters using a blank between each column and every seventh character is blanked to give an octal field to each register. Figure 6 is a picture of one page of the binary

display. Note the octal grouping. Figure 7 is a picture of one page of the octal display.

The starting point of the display would be the master clock which is cross-tied monostable multivibrators (SN74121N) with a 3.3 megacycle speed. It is used to drive a set of dual J-K edge triggered flip-flops (SN74103N) tied together to form a binary counter. The first six outputs are decoded in (SN7442N) BCD to 10 line decoders and the output of the SN7442N are used as column pulses. The last five outputs of the register are decoded by an SN7442N for the row pulses. The blanking is done by nand gates, then nor gates, then nand gates, in order to get a string of pulses which are enabled by the rows. The output is the column pulses occurring at the correct row time. These outputs are ran through nand gates to give the desired format for that page of display.

The display is selected using the Central Control or Signal Processor switch with the Display 1/Display 2 switch. These enable the correct format to be displayed. Another switch is the Request Display which signals the computer that another display has been selected, thus refreshing the display to the currently selected format. The third switch associated with the CRT display is the Binary/Octal which enables the registers displayed to be either in binary or octal. The Octal Loading switches were chosen because the tester's instructions are given in octal, thus the tester can load the shift register, gate the instruction to the frame, request a display and verify that the octal instruction was loaded to the frame correctly.

The heart of the CRT display is the circulating memory. This is used to refresh the screen with each sweep and is composed to TI's

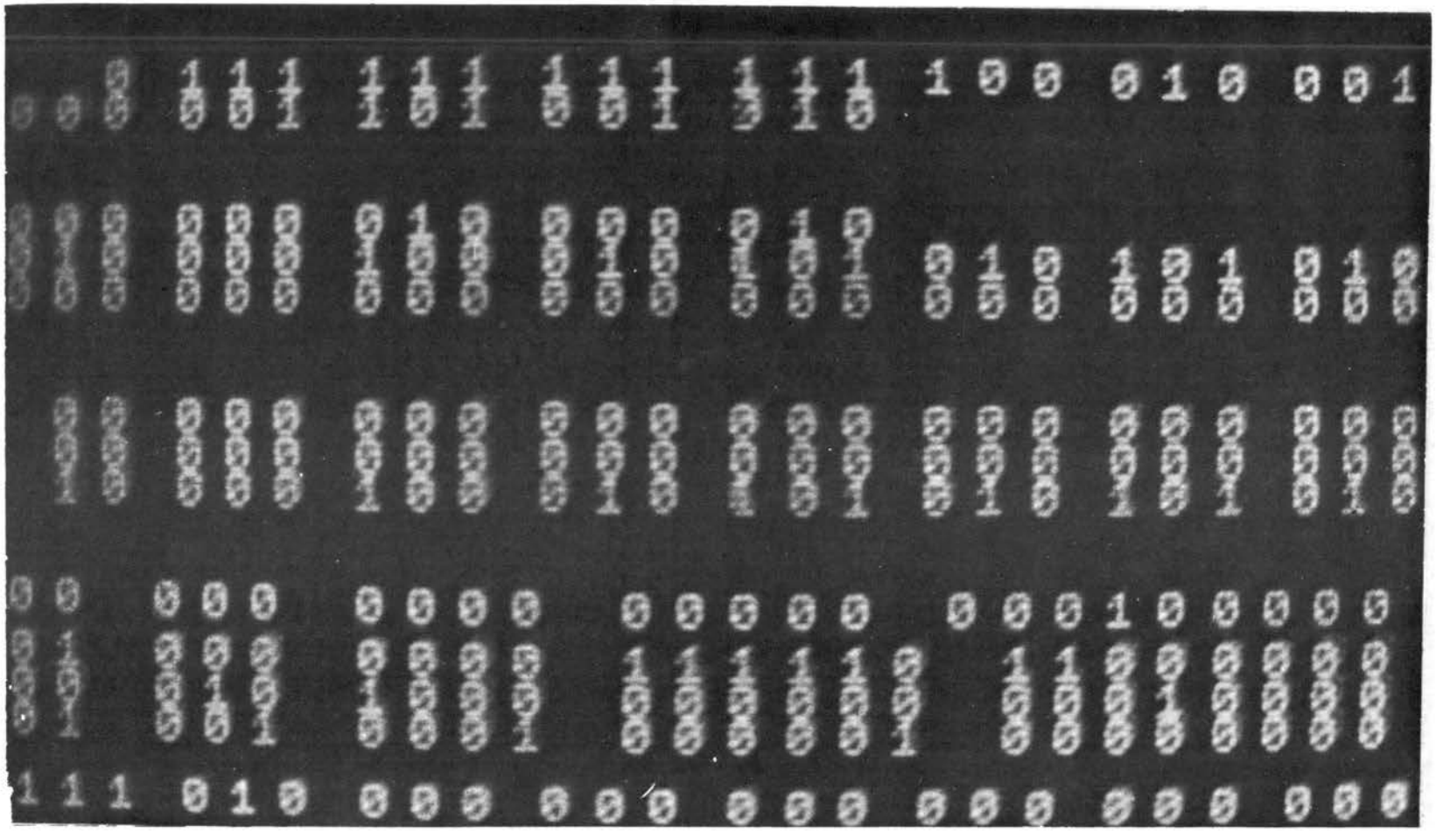

Figure 6. CRT Binary Display

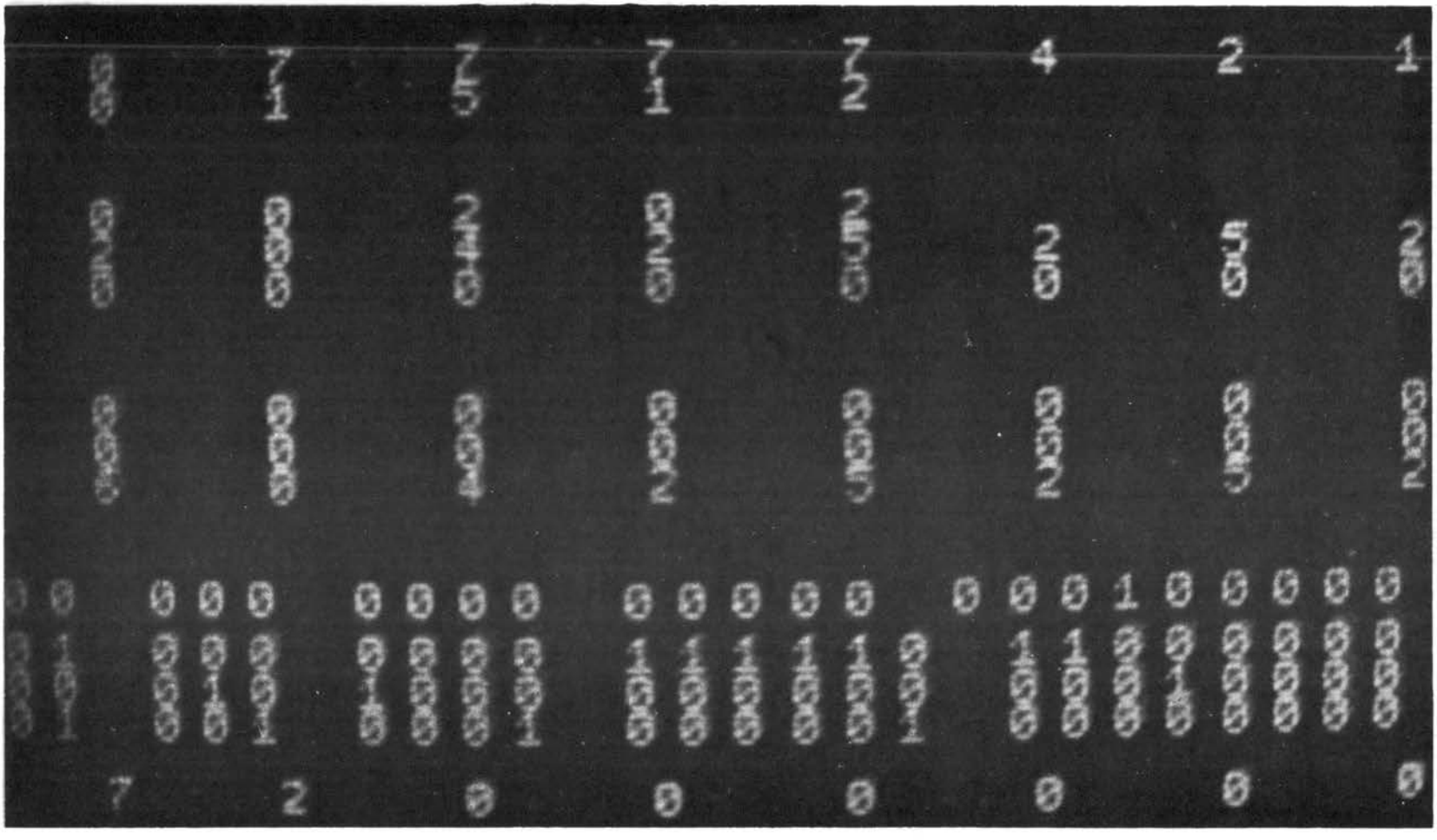

Figure 7. CRT Octal Display

TMS 3003 LR which are dual 100-bit shift registers. Figure 8 is one of the typical circuits of the 12 bit string, as they are all the same.

The information bit is brought in from the computer and stored in the shift register. When all 100 bits have been stored, a recirculate pulse is given by the computer, and the information is continually circulated through the shift register. The recirculate enable is the output of a flip-flop. One side will receive a memory interrup IOT pulse while the other side will receive the recirculate IOT pulse from the computer.

The biggest problems in this circuit was the phase clock pulses and the 28 volt interface with the 5 volt logic. The TMS 3003 LR needs a 28 volt change in the phase clocks. This was accomplished by using the circuit shown in Figure 9. The input PC1 is from a SN74121 with an external R-C network for a 0.4 microsecond pulse and used to trigger another SN74121 with the same R-C network. The output of the second SN74121 in turn triggers the third SN74121 with same R-C network and the output is PC2. PC2 is the input to a second circuit (same as Figure 9) to be used as $\emptyset_2$ to make up the two phase clock. The TMS 3003 LR shift registers have as circuit specification that the $\emptyset_1$ and $\emptyset_2$ be a minimum of 0.4 microseconds and thus the shift registers had to be carefully selected as some were too slow to work in this circuit.

From the memory the signals went into either an ASCII coder or a binary-octal coder depending on the column and row pulses. The ASCII coder sets up bits 6 and 7 for the TMS 4103 which is our character generator. The binary or octal coder is used for the information display and is controlled by the Binary/Octal key on the control panel.

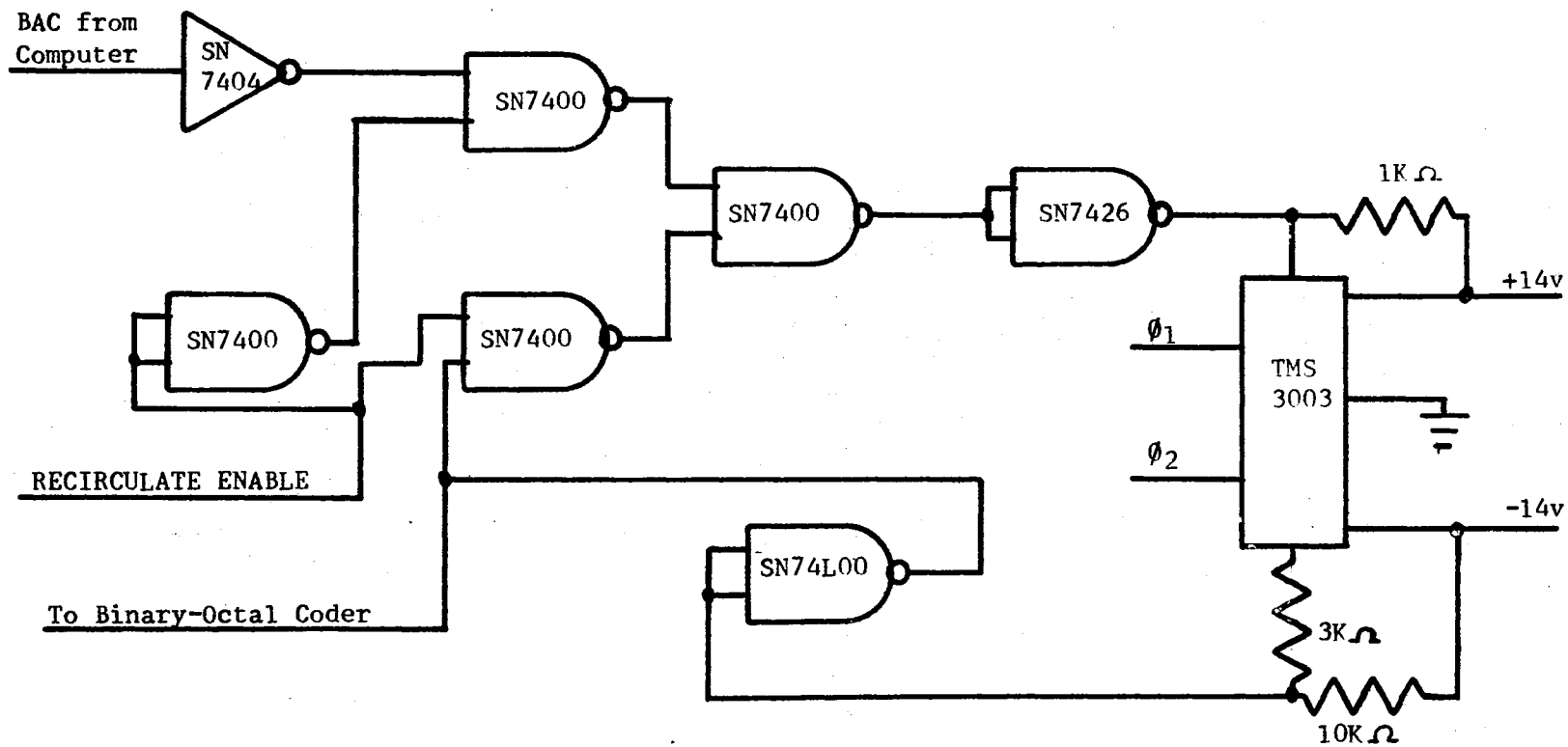

Figure 8. MOS Shift Registers Interface

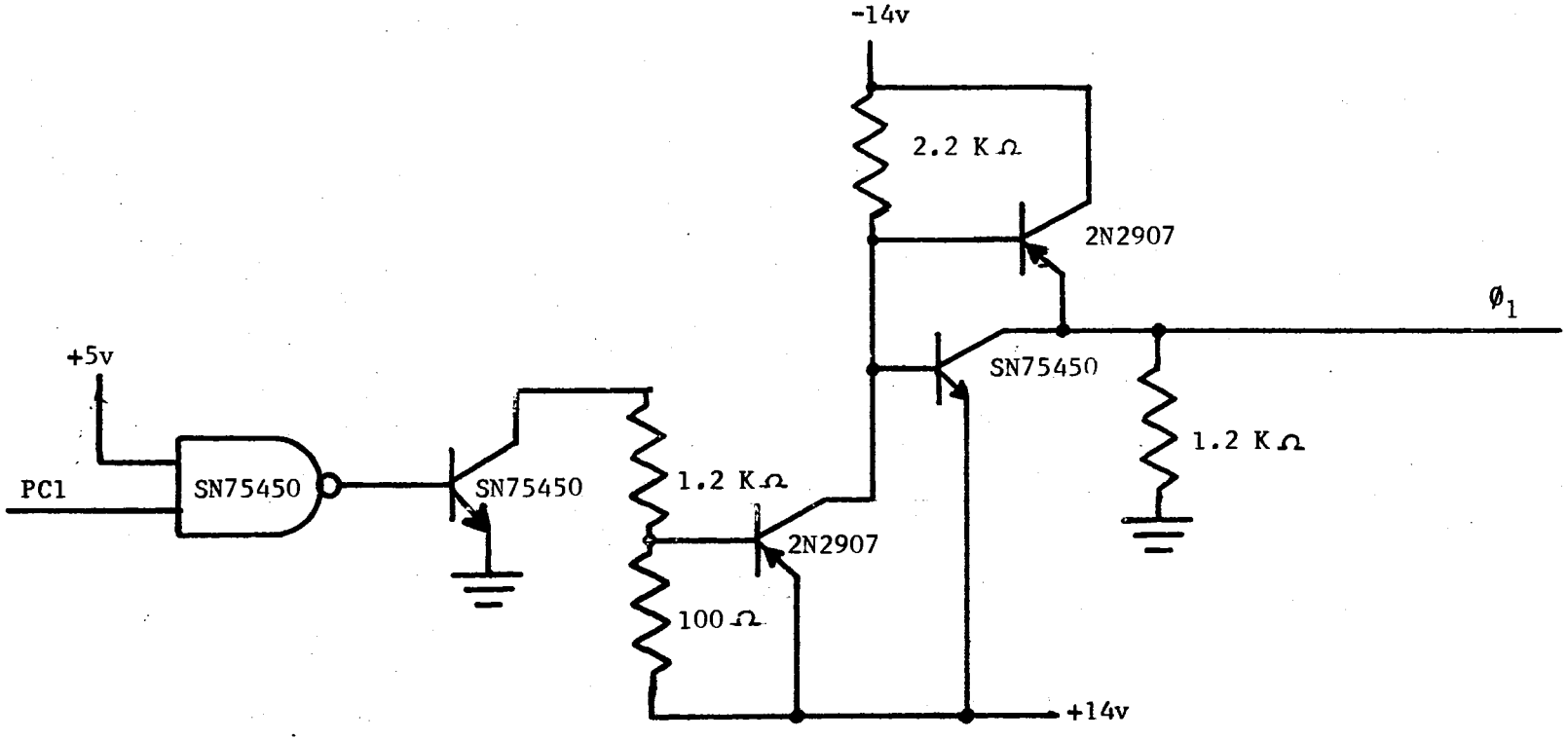

Figure 9. Phase Clock 5 Volt to 28 Volt Interface

In this case bits 6 and 7 are not used. The outputs of the coders are anded and ored to give the desired ASCII character or data bit wanted for display.

The TMS 4103 is a 28 volt MOS chip used to generate a 5 x 7 dot matrix that has been referred to earlier as the minor matrix. The interface of the 5 volt TTL with the 28 volt MOS is achieved in the same manner as with the circulating memory. This was shown in Figure 8. The signals then go into the digital format encoder where the character generator and the format blanking are anded before being sent to the digital-to-analog (DAC) convertors.

The 10 bit DAC was taken from the SP test set used at the Western Electric Hawthorne Works in Chicago. This test set uses a paper tape system for test data information, hard wired logic for test circuits, and a CRT to display the status of points being monitored by the test set. Their CRT has no memory and thus must be only one page in size. System 975-1 has two pages with a memory and is loaded from the computer which also allows the display of test data that was read off of the magnetic tape and stored in the computer's core memory. There is an X-DAC and a Y-DAC for the input to the CRT and the Z input is used for row blanking.

CHAPTER IV

SOFTWARE SUPPORT PROGRAMS

The hardware in the system has been briefly discussed. The next part consists of a brief description of the software. A lot of detail will not be given. Each program and how it was written to handle some of the unique processes will be explained.

There are five major programs for the 975 System. They are: CCAT, SPAT, CCDT, SPDT, and TXT(X), where (X) is a letter A to G used to distinguish between the seven text programs. The CCAT is the Central Control Automatic Test program. The SPAT is the Signal Processor Automatic Test program. The CCDT is the Central Control DATA Transfer program. The SPDT is the Signal Processor Data Transfer program. The seven TXT(X) programs are used to make the diagnostics tape with TXTA and TXTB used for the Signal Processor, while TXTC to TXTG are used for the Central Control.

Since the CCDT and SPDT are somewhat similar only a brief description of the CCDT shall be given. Basically, the CCDT is used to transfer the information from special IBM cards onto magnetic tape. The operation of the program is to use a formated magnetic tape of 105_8 word blocks for the CCDT and 113_8 word blocks for the SPDT. The programs are saved on the master tape as a system program and a call for either CCDT or SPDT will start the program.

The first response of the program is to type on the teletypewriter

STARTING BLK: which will be the block on magnetic tape where the first card read will be stored. As many digits as desired may be typed in, but the program will only recognize the last four. This method eliminates the necessity of starting over if a typing error is made.

The program response to the carriage return will be DECK: which is the test deck number of the cards to be processed. A two digit decimal number or the last two digits before the carriage return will be used as deck number and the program will respond with CARDS:. Type, in response to cards, the octal number of the cards in the deck to be processed. If there are more cards than indicated, the extra will be left in the card reader hopper. If there are fewer cards than indicated the program simply halts.

Upon the carriage return the program responds with LOAD SR (Ø=WRITE, 1=VERIFY). The switch register is either cleared to write the cards on magnetic tape or a bit is set to 1 for verification then Continue is pressed. A cleared switch register will cause the program to read a card, manipulate the bits and store the information onto every other block of the magnetic tape, according to the format as shown in Tables I and II. A one in the switch register will cause the card to be read, bits manipulated, the corresponding block on magnetic tape to be read into core, and then the card and tape information compared. If both are identical, another card is selected. If they are not identical, the program responds with VERIFICATION ERROR: printed and the program halts.

When a verification error occurs the information that is in error can be found at the following core location. Location 3466 is the octal number of the card that failed in verification. Location 3467 is the

present block number of the magnetic tape. Location 3470 is the word number of the block that failed and exact information of the card can be found in either Table I or Table II. Pressing Continue will cause the program to start over again.

When a deck has been run and the first question asked, the contents of location 17Ø is displayed in the accumulator. This represents the last block number used on the tape. This display can be used as a handy check to see whether the correct number of cards was read and that the correct starting block for the next deck is selected. The program also halts if it cannot pick up a card or the hopper of the card reader is empty. This was used for decks too large for the hopper or if a card should stick in the hopper. Clearing the problem and pressing Continue, the program will then finish processing the cards.

The TXTA to TXTG programs are used to prepare what we call the diagnostic tape. These programs create on tape a large file of text statements which contain the information that the tester uses to trouble-shoot a problem. Each block on the diagnostic tape contains 12 text statements each associated with the specific bit of that word being checked for a mismatch. The text statement is composed of the signal name, frame location, and schematic diagram location. An example from the CC would be block 37 bit 3; the text statement would be UBØ9 22Ø-19-Ø1 B 176. This would tell the tester than an error had occurred on the Unmasked Bus, bit 9, as the signal name was UBØ9.

The location on the frame is 22Ø-19-Ø1. The 22Ø would be the bay and plate location in the frame. This example would be bay 2, plate 20. In the CC it has four bays so the number would be between zero and three. In the SP it has three bays so the number would be

between zero and two. The plate number for each bay would be between 0 and 36. The connector location on the plate is given as the second number and will be between 0 and 48. The third part of the frame location information is the pin number of the specific connector and must be between 0 and 27.

The third part of the text statement gives the location in the schematic diagrams. In this example the lead could be found on the B sheets, page 176. There exists two other text statements. One is ILLEGAL MISMATCH TRY AGAIN which is assigned to the spare bits of a word. The other statement is, for example, EXTRA WIRE ON 326-14-Ø2. This is a spare pin on the test connector and should never change the state of the word received from the frame. Thus should a mismatch occur at this point, then a wire has been placed on the wrong pin or connector; therefore, the printout tells the tester what needs repaired.

CHAPTER V

SOFTWARE OF TEST PROGRAM

Now a more detailed description will be given on the CCAT and the SPAT programs. First, a brief description of the function of the program will be given and then a very short description of the subroutines. The best method is to describe the CCAT version one, and compare it with the SPAT version two, only when they differ. The CCAT version two and the SPAT version three will be used with the executive program for time-share testing.

The program is started by communication with the switch register. During normal operation the computer control switches are inoperative; however, when power is turned on the tester has one free "load address" and "start". The tester begins the program by pressing System Power switch and loading 42ØØ into the switch register. By pressing Load Address and then Start the program is started. After the program is entered, it will not halt except for one specific malfunction, which will be explained in the description of TRANSF; otherwise, control is maintained by use of the teletypewriter and switch register.

The first response from the program will be on the teletypewriter. The CCAT version one and SPAT version two ask two questions. The first is START, to which the tester will respond with a string of four numbers representing the starting block number, then a dash and four more numbers for the ending block number. The tester now has to give either a

carriage return or a semi-colon. The carriage return will start the program in the subroutine that checks for legal block numbers. The semi-colon is a flag to stop processing the test deck at the sequence number typed, or at the end of the initialization part of the deck if an I was typed. This feature is needed in CCAT to either inhibit or uninhibit circuits during a test sequence. The carriage return then starts the program.

The second question is asked when the program determines that the block numbers are legal; it responds with MODE. The tester answers by typing in the number of the desired mode of operation. A carriage return will now start the program to perform the tests and will continue until either a mismatch is detected, or the last block has been processed. Table III lists the six legal modes of the SP and six major modes of the CC. Table IV lists the eight minor modes for the CC.

TABLE III

CC AND SP MAJOR MODES OF OPERATION

Mode Number	Mode Operation	Code
14ØX	Manual/Manual/Cycle	M/M/C
24ØX	Manual/Automatic/Cycle	M/A/C
44ØX	Automatic/Automatic/Cycle	A/A/C
11ØX	Manual/Manual/Phase	M/M/P
21ØX	Manual/Automatic/Phase	M/A/P
41ØX	Automatic/Automatic/Phase	A/A/P

For the SP the (X) is a zero while for the CC it defines the minor modes as listed in Table IV. The major mode defines the status of the

TABLE IV

CC MINOR MODES OF OPERATION

(X)	Mode Operation	Code
Ø	NORMAL	Same as Major Mode
1	MATCH MODE ONE	MM1
2	MATCH MODE TWO	MM2
3	MATCH MODE THREE	MM3
4	MATCH MODE ONE-TWO	MM12
5	MATCH MODE ONE-THREE	MM13
6	MATCH MODE TWO-THREE	MM23
7	MATCH MODE ONE-TWO-THREE	MM123

test set and the frame, and is coded in a test set/clock/frame operation. The automatic or manual in the test set position means that the test set is running either automatically or must be advanced manually. The clock in automatic means the test advances the clock automatically while in manual the manual clock advance key on the control panel must be operated. The phase or cycle lets the frame be advanced either a single phase at a time or three phases at a time in cycle.

The 41ØX is the automatic testing mode while 21ØX is the most commonly used mode for troubleshooting problems. The 41ØX mode allows the block selection and advancing of the frame clock to be completely automatic. The clock is advanced under program control and each phase

is matched. The block selection continues until a mismatch is detected or until the end of the deck (also referred to as the selected block). The 21ØX performs the same function as 41ØX except each block of magnetic tape must be manually selected. After the tester runs the first block and advances the frame clock, the CRT display is updated. The matching is still performed during each time slot, but the next block of information must be manually selected by using the PROCESS NEXT RECORD option on the switch register.

The 11ØX mode allows the tester to cycle the frame through one phase at a time. The clock must be advanced manually from the test set control panel and the test data selected as in 21ØX. In this mode there is no matching, however, the tester can visually check the card against the CRT display for each phase. The three cycle modes run in the same manner as the three phase modes except for the matching. In a cycle mode the matching is performed only for the first phase and then the clock is advanced to the start of the next cycle. There also exists a mode of troubleshooting not listed in Table III. It is called monitor. In monitor the clock control is released from the control of the test set, and the frame runs on its own clock. The only function the test set can perform in monitor is to load the instruction at the start of every cycle. Here some differences exist between the CC and SP. As previously mentioned, the CC has an instruction of one to four cycles in length, while the SP is of a single cycle length. Thus, the SP recycles on the same instruction, while the CC uses the word generator circuit to load one instruction and increment so that on the start of the next cycle the next instruction can be loaded. When the word generator reaches the number of cycles for the instruction,

the word generator is reset and starts the instruction sequence over again. Thus, monitor is used for dynamic troubleshooting of gating pulses.

Now all the major modes of the CC and all the modes of the SP have been covered. The remaining minor modes of the CC will now be explained. The match mode (X), where (X) can be any possible combination of one, two, or three, is used to get more test information on the same CCAT card. For the CC testing three roving registers are used to access different registers associated with the frame. When testing in match mode (X) the program will match the one or more registers with the appropriate test data on the cards. Thus, when testing in match mode one, Register One is matched with the test data punched in the Unmasked Bus on the card. Match mode two, Register Two is matched with the Masked Bus while in match mode three, Register Three is matched with the OWD (Order Word Decoder) Match Points.

The program handles the matching in the same method as in the normal mode, except the IOT number is for the register under test instead of the card assigned match point. The exclusive OR is then performed as in the normal mode. This enables us to test all the registers in the CC that are used for maintainence and operating data. The difference here between the CC and SP is that the SP registers can be written into and read out into the CC Data Register where the matching can be performed. Some of the CC registers are read-write, some are read only, some are write only, while others are neither read nor write, but are the interrupt type. These various types can also be only one bit in a register as some CC registers contain all four types of flip-flops. These interrupt flip-flops can only be cleared when

the CC has placed out of service that piece of equipment which it monitors.

Also mentioned before was the user options. The program is written so that the interface between tester and test set has been simplified as much as possible. The tester needs only to give the program two strings of numbers and then has seven possible user options. These options can be exercised by depressing the appropriate switch on the computer switch register. Figure 10 is a sketch of the switch register with the user options.

The Display Original Card causes the program to continually update the CRT display with the information from the card which is stored in core. This information was read from the last block of the magnetic tape and represents the desired state of each test point. This option can be used with the Refresh CRT and the bit or bits changing state are the ones in error. The tester uses this option to determine the correct state of a test point before starting his troubleshooting.

The Refresh Display causes the program to display the information which represents the states of the test points in the frame. If the switch is left depressed, the display will be continually updated. Also, when this option is selected, the clock control is under control of the test set control panel. Without selection of Refresh Display the clock is under program control.

The three Continue Processing options are tester aids in testing the frames. The Continue Processing (Same Record) is very useful on the SP as it repeats the test using the last block of test data. This is especially helpful when a missing wire or wrong termination is found to be the defect. When the defect is repaired the tester can repeat

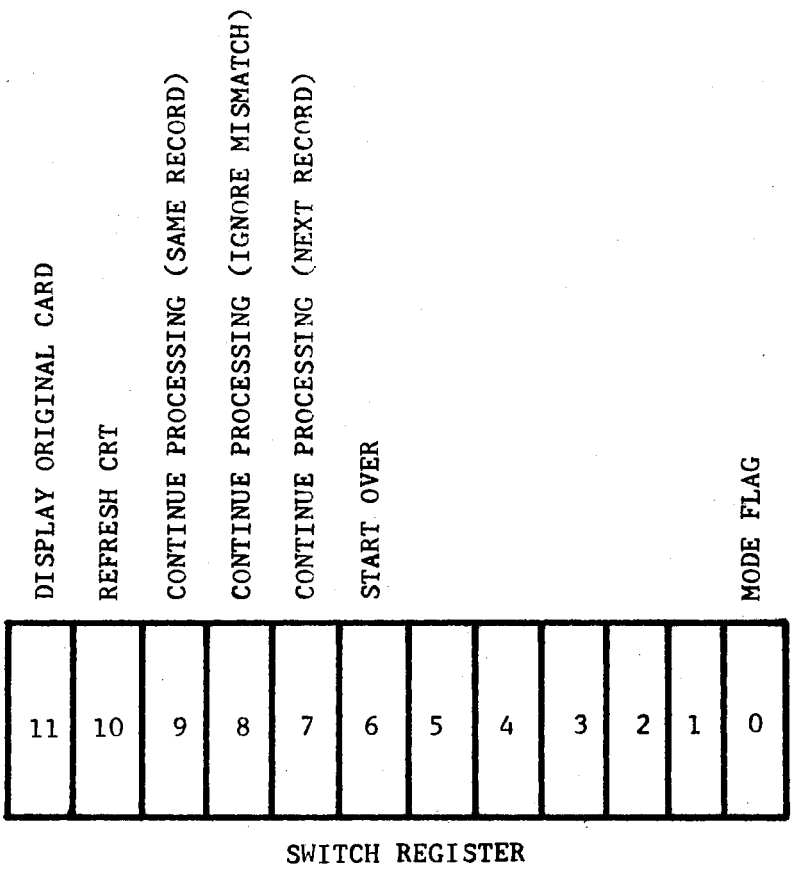

Figure 10. Switch Register Options

the last block and continue testing if the error was removed. Thus, it eliminates the need for restarting the entire deck. There also exists one condition for using this option and that is when the frame clock has been advanced to the start of the cycle. This option cannot be used on the CC as the PAR (Program Store Address Register), which is the same as a program counter in a computer, cannot be decremented the number of times this option might have been used.

However, the other two Continue Processing options can be used on both the CC and the SP. The Continue Processing (Ignore Mismatch) causes the program to be re-entered as though no mismatch had occurred. One reason for this option was that while troubleshooting, testers sometime ground points to inhibit circuits and then started over without removing the ground. When this occurs the tester can remove the ground and press Continue Processing (Ignore Mismatch). Thus, the testing can continue without restarting the test procedure.

The Continue Processing (Next Record) option ignores the mismatch and proceeds to process the next record provided the clock has been advanced to the start of the next cycle. This option was given to aid the tester in determining his problem. This was used to determine whether the test point was to change states as one level to another or pulse; in other words, to set and reset during this cycle.

The Start Over option will send the program back to the beginning and the starting information will be asked for. The five blank switches are available for additional user options.

The Mode Flag is used by the tester as a program interrupt as this is the only way the tester can stop a test that he has started. Otherwise, he must wait until the test has been completed or a mismatch has

occurred. The Mode Flag can be used anytime, while the Start Over is only available at a mismatch, error, or during the starting cycle. The other options can only be used after a mismatch, error, or the end of the deck. The Start Over is called by the program at the end of a deck.

The only other interface between the tester and the program is the error messages he receives on the teletypewriter. There are only three types of error messages. One is a mismatch error, one is a timing error, and the last is a magnetic tape reading error--the only fatal one.

When there is a mismatch the program prints the record block number, the card number, the point or points in error and also the page number in the schematic diagrams where the errors can be found. The errors are also identified by signal names and locations on the frame. A typical mismatch printout would be as follows:

```
CARD PROCESSED: 2583
RECORD BLOCK NUMBER: 4464
MISMATCH   LOCATION    SD
  UBØ9     22Ø-19-Ø1   B176
```

There also exist two more types of printouts for mismatch errors and they are as follows:

```
ILLEGAL MISMATCH TRY AGAIN:
EXTRA WIRE ON (XXX-XX-XX)
```

These indicate two specific problems. The first has had a point matched with a spare bit as shown in Table I or II. The second has a wire on what should be an unwired test connector pin.

The timing error is a message that tells the tester he has tried to start the program while the frame was stopped on either the second or third phase of a cycle. The printout looks like the following:

TIMING ERROR: FRAME NOT AT T5

This error message also will appear during normal cycling of the frame if the program is not able to advance the clock.

The third message is the only fatal error and is as follows:

UNABLE TO PROCESS MAG TAPE DATA

When a new block is selected, the program sends the tape transport into motion looking for the desired block number. When it is found, the program transfers the test information into core. If there has been any reading errors, bit zero of the B register of the transport control unit is a one. After each data transfer, bit zero is checked. If it is a zero, the program continues as usual. If bit zero is a one, the tape transport backs up and reads the block again. This can happen twice. Upon the third try if bit zero is still a one, the error message is printed; the program then comes to a fatal halt. When this happens there is nothing the tester can do but call an engineer to either fix the problem or get the DEC repairman to repair the transport. However, the system has been running for over a year, and to date this problem

has not been experienced.

The messages are typed using a routine called MESAGE. Using the text pseudo-op the ASCII characters are trimmed to six bits and packed, two per core memory location. Upon entry to MESAGE the address of the first trimmed and packed ASCII code is decremented by one and deposited in the autoindex register 1Ø. The TYPECH routine will type the characters until a six bit data word is reached which contains all zeros. This is the end-of-message code and the program jumps to a loop awaiting the tester's response.

At this time rather than referring to a fifteen page flow chart on the CCAT program, it would serve better purpose to give a brief description of the operations the program performs. Its first function after the tester's reply is to verify that the information is valid. After the program has confirmed the starting data, the mode is checked. Then the sequence flip-flop in the frame is checked for a timing error. If the timing is correct, then the PSBO (Program Store Bus 0 Enable) is checked to be sure that the frame can accept an input. If all checks are all right, the program looks for the first block of test data on the magnetic tape.

When the block is found it is read into core. The program then resets all the Control Flip-Flops. The next function is to check the flags. If the initialization flag is set, the program gates the input to the frame, then advances the clock to the start of the next cycle. In the initialization of the deck no matching is performed. The next flag checked is the Control Flip-Flop Flag that is listed in Table I under word 102 called the column 61-Row-9 flag. When a flag has been detected the Control Flip-Flops are then set according to Table V.

TABLE V

PROGRAM CODES

Deck No.	Setup No.	Control F/F Setup	MM1	MM2	MM3
1-28	Ø1	Normal	-	-	-
29	Ø2	A=6 & 7	-	-	-
30	Ø1	Normal	-	-	-
31	Ø3	Normal	-	-	324-05
32	Ø4	Normal	328-43	314-44	324-05
33	Ø5	B=28	DRØ	ARØ	324-05
34	Ø6	B	DR1	AR1	324-05
35	Ø7	B	DR1	DRØ	-
36	1Ø	B	-	DRØ	328-43
37	Ø1	Normal	-	-	-
38	11	Normal	-	-	318-42
39	12	Normal	232-41	FR	-
40	Ø1	Normal	-	-	-
41	13	C=1-11 & 15-24	326-33	324-30	326-14
42	14	D=1-11,15-25 & 28	326-33	324-30	326-14
43-44	Ø1	Normal	-	-	-
45	15	Normal	124-35	FR	-
46	16	E=4,11,16,17 & 25	320-38	AUR	-
47	17	F=1-3,5-7,11,16-18,20,22-25	014-01	AUR	-
48-49	Ø1	Normal	-	-	-
50-51	2Ø	Normal	124-35	-	-
52-54	Ø1	Normal	-	-	-
55-56	2Ø	Normal	124-35	-	-
57	21	Normal	LR	-	-
58	22	Normal	ARØ	-	-
59-60	23	Normal	AR1	-	-
61-62	24	G=5,11,18-21,24,29	-	-	-
63	Ø1	Normal	-	-	-
64	25	Normal	014-01	-	-
65-70	Ø1	Normal	-	-	-

When the Control Flip-Flops have been set the next flag checked is the PU (Peripheral Units). If the PU Flag is set then the PUAT (Peripheral Unit Address Translator) and PU Reply (Peripheral Units Reply Bus) is matched, otherwise the PUAT and PU Reply match is skipped. Then the PAR (Program Store Address Register), IAOR (Index Adder Output Register), and the BR (Buffer Register) are matched.

The matching is performed by taking the frame status from the IOT input, masking if needed, then complementing and incrementing the accumulator and saving this information. Next the test data is placed in the accumulator and any masking is performed. Then the saved information is two's complement added to the accumulator. A skip on zero accumulator indicates if an error has occurred. If the accumulator is zero, the program starts the next match. If not, the program jumps off to a routine for finding the bit or bits in error and then an error message is printed.

Let us refer again to Figure 2. Once the program has matched row zero of the card, rows one, four, and seven, rows two, five and eight, rows three, six and nine are all respectively matched as the same points are checked during each phase. Row one is the status and sequence flip-flops. They are matched as before with each word composed as shown in Table I. The BOWD (Buffer Order Word Decoder) and the MAD (Memory Address Decoder) are matched next. The program now checks the mode to determine if it must match the OWD (Order Word Decoder) with the OWD on the frame or with Register Three. This decision is reached by checking the mode for MM3 (Match Mode Three). If MM3 is requested, Register Three will be matched with the OWD points on the card. Register Three will be located as shown in Table V.

Again, the mode in row three must be checked for MM1 and MM2. If MM2 is selected, the MB (Masked Bus) and CS (Sign Flip-Flop) is matched with Register Two. If MM2 has not been selected, the MB and CS are matched with these points in the frame. Then the mode is checked for MM1 and the UB (Unmasked Bus) and CH (Homogeneity Flip-Flop) are matched with either the points in the frame or Register One. Registers One and Two are located respectively for each deck according to Table V.

When row three has been matched, the program then advances the clock and repeats the previous three rows of testing and clock advancing twice more. After the clock has been advanced at the completion of row nine matching, the program starts checking for the next block to be read from the magnetic tape. The matching is repeated and block selection continues until either a mismatch is found or the final block is selected. Upon completing the matching for the block the appropriate message is printed out and the CRT Display is updated. When the test decks are completed there are a few manual tests to be performed, then the frame is sent to the shipping area to be crated and stored until the delivery date.

CHAPTER VI

CONCLUSIONS

The System 975-2 does not look much different than the System 975-1. The System 975-2 has two separate cabinets, each containing a CRT display, a control panel and a teletypewriter. The DEC tape units are the new version which have two tape drives per transport unit. Thus, in the same space we now have four magnetic tape readers. The computer and drawers are the same. The drawers have been rewired. The card reader interface has been replaced with M101 and M113 to perform the OR of our monitoring boards. The outputs are now controlled by the interlocking switches which were changed to a flip-flop which is under program control.

The System 975-2 is more versatile because it has two test sets with 200 points for inputs and 850 monitoring points. This will be a more than sufficient number to test any ESS No. 1 frame; it also can be used to test ESS No. 2 frames, two at a time. The cords for the inputs will work on any frame with the 905A connector. The monitor boards will also work in any 905A connectors. However, it is currently being used with a CC and SP frame.

The CC and SP test positions are ten feet apart, and the test set sits between them, with a CRT display and teletypewriter unit on each side of the computer cabinet. This way the interconnections between the computer and CRT display units are kept short. There were some

changes made in the control panel. These were made to make the panel more specialized for that specific test station and also make the tester's options handier for him. On the SP control panel the Control Flip-Flop switches are changed to an auxiliary switch register. While on the CC, the SP control switches are changed to the auxiliary switch register. This puts the user options at the test station instead of several feet away at the computer. These are all the hardware changes needed to design the System 975-2, using the System 975-1 as a basis for the test set.

The software part has been simplified a great deal by keeping in mind a time-share system at the time we designed and wrote the software for System 975-1. The CCAT version one was written, so just a few instructions needed to be added to prepare the time-share CCAT version two. This also was some of the reasons for writing SPAT version two and three. The author is considering the writing of another version for both the CCAT and SPAT, utilizing subroutines that can be written in the same manner. Some examples of the subroutines are: mode checking, block verification, messages, exclusive OR, and several other shorter subroutines. These would be used in the executive program making it somewhat larger but saving twice as much core due to removal from both the CCAT and the SPAT programs.

There are some problems in the executive program which need to be checked dynamically under extreme test conditions. The main concern, at this time, is that the characters being typed on the teletypewriter do not get missed. The teletypewriter is the slowest device in the system; it takes 100 milliseconds to type one character. This is very slow, even when comparing it with the next most time-consuming operation,

that of loading the CRT display memory. To perform the refreshing of the CRT memory requires 34 IOT, 34 deposits in core, 100 readouts from core, 100 loads to the shift registers, and finally a recirculate IOT. All these operations still take a little less than 700 microseconds. Thus, the refreshing of the CRT display will cause no difficulty. The message printout on the teletypewriter is controlled by the program.

The last problem to be proved-in is that of running both test stations simultaneously in automatic test. The program runs fine using the technique of storing test data for each deck in odd or even block numbers. While running only one test station at a time, the program can perform all the matching before the next block comes up to be read from the magnetic tape. The way the time-share program is written, it stores the test data in every fourth block. This will slow the testing procedure slightly, but not having to stop the tape transport is a tremendous time saver. This was verified in the SPAT version two. An example in version one would be deck 1. In version one the tape transport rocked; that is, was stopped, reversed, stopped, started forward to read one block, and then stopped while the matching was performed. The time required to run deck one was five minutes and twelve seconds. In version two the data was stored in every other block. The tape transport was started and not stopped until there was either a mismatch or the end of the deck was reached. Version two takes 15 seconds to run. Version three for the time-share system using every fourth block takes 28 seconds. This is nearly twice as long; however, it saves us from having to build another $75,000 test set. Theoretically, the time-sharing program will work using every third block, but it leaves only seven microseconds before the program

must start reading data. This will be tried when the system has been completed and is working using every fourth block with both test stations in automatic test. There will be very few times that this will happen because the largest amount of time is spent in manual test, which uses very little computer time. Another reason that both test stations will not be simultaneously in automatic test is that the SP has only 18 test decks, containing just over 3,000 cards. The CC on the other hand has 70 decks containing more than 14,000 cards. Therefore, it would not be probable that both test stations would be running in automatic test. However, the programs are written so that only one constant needs to be changed in each program to prepare and run the tapes using whatever block spacing desired. All four programs, CCAT, SPAT, CCDT, and SPDT uses the same constant name for computing the next block.

The System 975-2 not only reduces the number of test sets needed for testing the ESS No. 1 control frames (CC and SP), but also can be used on other frames in the ESS No. 1 system. It can easily be adapted to the ESS No. 2 control frames or other frames. It also gives greater value when the test set is scrapped as the computer (which represents a large portion of the expense of the test set) can be used either in some other testing or manufacturing system, or as a computer system for engineering study and/or design.

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