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THE SYNTHESIS AND ANALYSIS OF FLUID CONTROL NETWORKS

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THE SYNTHESIS AND ANALYSIS OF FLUID CONTROL NETWORKS

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This dissertation was done in partial fulfillment of the requirements for the doctor's degree at the University of Oklahoma. The idea for this study was conceived by the author in 1958. Since that time, a number of associates have shared the hope that fluid networks could be synthesized and analyzed analytically. Special recognition is given to Mr. Joseph M. Case, now with the General Electric Corporation for assisting the author in formulating the general requirements of this study.

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CHAPTER I

INTRODUCTION

This study is concerned with the synthesis and analysis of fluid power and fluid control systems of a digital nature in which logic methods serve to implement the requirements rather than intuition.

The term fluid power refers to a system in which a fluid medium is utilized for the force that it is capable of exerting. The fluid medium inferred includes both gas and liquid. A fluid power system can be controlled by manual, mechanical, electrical, or fluid means. The control systems can be classified broadly as either analog or digital. In analog systems, the variables to be controlled are physically characterized by parameters which may vary continuously over a limited range. The functional units comprising an analog system are operationally interconnected to provide continuous feedback information and error detection. A digital system on the other hand operates with data represented as a series or set of characters which attain only certain discrete values. The functional components of a digital system are capable of representing only a relatively few discrete conditions -- certainly not a continuous function.

Fluid power is not a new field; it can be traced back to 1785 when an Englishman, Joseph Bramah, built the first hydraulic press. After World War I, when serious seal problems were partially solved, fluid power became acceptable for numerous applications. Technical advancements during World War II fostered the fluid-servo era which satisfied the basic requirements of many control problems. It is apparent that the space age struggle has cultivated the need for fluid digital control systems to supplement and replace conventional electrical hardware in many areas. Sophisticated fluid control elements capable of being packaged 6000 per cubic inch, of withstanding 50,000 g's, and operating with frequencies of from 10-100 KC presently exist. Fluid digital computers or control systems using such elements would not be heat generators, would be immune to ionizing radiation, and would perform satisfactorily at extremely high or low temperatures.

It may be surmised that the continued increase in popularity of fluid power is largely due to the fact that a confined fluid is one of the most versatile means of modifying motion and transmitting power. The future of fluid power and control systems is limited only by our imagination and our technical abilities.

Although a major part of the fluid controls currently used are digital, no logical method for the synthesis and analysis of fluid circuits has been reported. Hence, fluid power digital control is presently in the same historical period that electrical controls were prior to World War II. The fluid circuit designer has been required to depend upon his ingenuity and perseverance to employ the intuitive method of circuit synthesis and analysis. There exist many reminders

of the defeat of fluid designers in the form of electro-hydraulic machines. Knowing that the electrical engineers could usually offer control solutions to their problems engendered a deplorable attitude among fluid circuit designers.

Engineers invested with the responsibility of the design and operation of fluid control systems need a logical method to assist them in performing their work. The most likely field in which to locate such a method is electrical switching circuit theory. The fluid designer cannot expect those versed in electrical theory to be cognizant of the problems inherent in fluid circuits; therefore, many investigations by fluid power engineers, comparable to this study, are necessary to exploit fully the vast wealth of knowledge available for interpretation. Such investigations will result in the establishment of a foundation for the evolution of digital fluid circuit theory. The mastery of the logical synthesis and analysis of fluid switching circuits will direct the way to operational fluid computers and sophisticated control networks.

CHAPTER II

PREVIOUS INVESTIGATIONS

The synthesis and analysis of fluid circuits have been accomplished by intuitive processes. For an experienced designer, these processes can be applied appropriately to develop effective solutions to simple circuits. As the complexity of the circuit problem increases, the intuitive method becomes strictly an iterative game of trial and error. Although the ingenuity of the designer is challenged, his plight becomes analogous to "looking for a needle in a haystack."

The problem encountered by an engineer attempting to design a circuit involving sequential operations can be demonstrated using a timing chart. A timing chart consists of vertical divisions representing sequential time (display of events). Each time division corresponds to a change of the input states. Consider a circuit specification in which two inputs, x_1 and x_2, and one output Z are involved. The sequential cycle is as follows: 1) no inputs or output, 2) input x_2 is energized, 3) inputs x_2 and x_1 are both energized, 4) input x_2 is on while x_1 is off, 5) inputs x_2 and x_1 are on and the output Z is actuated, 6) only x_2 is on, and 7) all inputs are off and no output. The timing chart for the above sequence is given in Fig. 2-1.

The solution to a circuit problem such as the one shown in

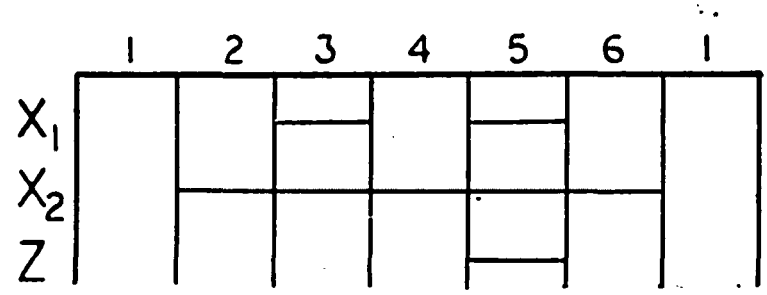


Fig. 2-1. Timing Chart for Sequential Cycle Example

Fig. 2-1 involves the establishment of unique conditions for each sequential division. In other words, the circuits must be capable of differentiating between time intervals having the same inpu states but different output conditions. Since the input states in this example do not create unique circuit conditions, a secondary circuit is required to provide the necessary distinguishing property. One solution to the example problem would be to have two secondaries emit signals as shown in Fig. 2-2. The uniqueness of the critical divisions on the timing chart are established, and the design of the network can be initiated.

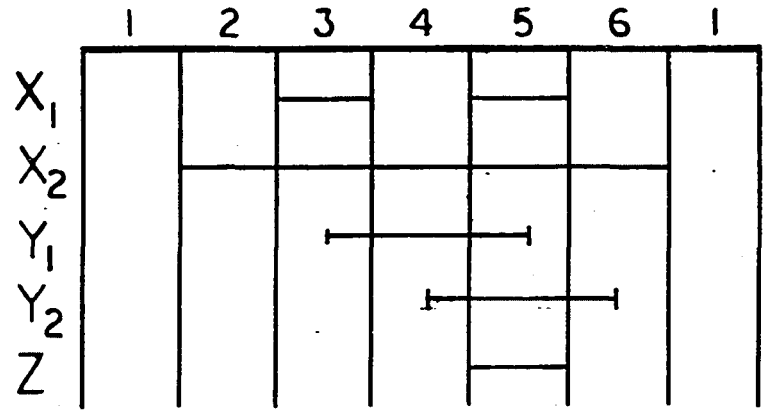


Fig. 2-2. Complete Timing Chart for Sequential Cycle Example

Although the need to have unique states can be recognized from the timing chart and the requirements for a particular secondary network can eventually be established, no assistance is received from the chart concerning the appropriate circuit configuration. The timing chart merely permits the development of the circuit specifications with no assurance given whether an optimum network will result.

A limited quantity of work has been reported on organizing and implementing the intuitive method. Mr. Paul Rolnick (1) published an extensive collection of basic circuits and proceeded to classify them according to purpose as an aid in synthesizing fluid circuits. Similar circuits, as well as more applied circuits, appear annually in the Fluid Power Index published by the Industrial Publishing Company, Cleveland, Ohio.

Several attempts have been made by the author to outline circuit synthesis methods for fluid designers. In Reference Manual for Hydraulic Circuits (2), a selected group of fluid components were introduced and classified; and special application circuits associated with agricultural mobile equipment were presented. Symbolic notation of the JIC (Joint Industry Conference) was used exclusively which resulted in the simplification of both design and analysis. These concepts were rigorously applied in Fluid Power and Control Systems (3) which covered all basic components and circuits. In addition, a conscientious attempt was made to reveal the nature of circuit design and present a criterion of design consistent with established practice. Although, considerable success was noted, the complicated memory circuits included were almost beyond intuitive reasoning. Logic functions

were presented to stimulate thought in the area, but no general use was exhibited.

An extensive literature survey conducted in conjunction with this study yielded 216 pertinent articles and revealed that Mr. H. R. Ronan (4) was the first reported person to attempt the transition from intuitive to logical design of fluid switching circuits. Although Mr Ronan's presentation must be recognized as a pioneer effort, the vaguely outlined scheme proposed had no practical value over intuitive methods. Since no work has been published on the logic design of hydraulic circuits subsequent to Mr. Ronan's paper, it can be assumed that fluid designers found the method impractical.

In preparation for this study, the author initiated and directed a number of research projects on fluid switching circuits which aided in establishing the requirements of this study. Mr. A. G. Comer (5) in 1957, conducted an experimental investigation on the switching circuit fluid network required to produce the intermittent feeding of a slave cylinder. In 1958, Mr. J. M. Case (6) conducted an experimental study on the digital positioning of a hydraulic cylinder. Also in 1958, Mr. W. R. Matthews (7) investigated the high speed cycling characteristics of hydraulic cylinders using fluid switching networks. Mr. J. F. Gormley (8) conducted a study in 1959 to compare the response characteristics of electro-hydraulic control with that of fluid switching circuit control.

Having the advantage of the results of the above mentioned research studies, the author initiated two concurrent investigations.

One study involved the electro-hydraulic analogy of switching circuits, and the second study pursued the application of Boolean algebra for synthesizing fluid networks. The first study conducted and reported with Mr. J. M. Case (9) attempted to bridge the gap between electrical circuits and fluid circuits by using appropriate analogies and a circuit reduction scheme. Although successfully accomplished and completely verified experimentally, the intuitive approach still prevailed to a large extent; and the method made the fluid designer completely dependent upon the attainment of the corresponding electrical circuit. Such a situation would not be a major improvement over the present condition. The second study was conducted by Mr. O'Neill Burchett (10) and resulted in an analytical demonstration of simple switching circuit design along the same lines of Mr. Ronan's. No basis was gained for future efforts, and a general feeling of discouragement prevailed.

No major attempt has been reported on the application of knowledge from other disciplines to the solution of fluid network problems. The significant progress made in the field of electrical engineering to establish a switching theory for electrical networks must be recognized. The modern theory of electrical switching circuits was initiated in 1938 by Claude E. Shannon (11) who introduced the use of algebraic logic in designing simple electrical relay circuits. A rigorous logical method for designing sequential circuits did not appear until 1954 when Mr. D. A. Huffman (12) presented his now famous flow table procedure to display sequential circuit behavior. The details involved in the evolution of switching theory must be accompanied by the characteristic nature of Boolean algebra; therefore Chapter IV will expound

the development of this theory.

The general status of fluid circuit synthesis and analysis as revealed in this chapter purports the obvious need for studies in this field. Since the requirements imposed on electrical switching circuits parallel those of fluid switching circuits, a possible solution to the fluid circuit design dilemma appears to be in electrical switching circuit theory. This is the direction pursued by the author in this investigation.

CHAPTER III

STATEMENT OF PROBLEM

The purpose of this investigation was to advance a logical method for the synthesis and analysis of fluid switching networks to replace the intuitive procedures currently being applied. The general plan of attack was to study the state of the art of electrical switching theory and to determine its possible application to fluid control circuits. An appropriate method has been deduced and will be demonstrated both analytically and experimentally.

CHAPTER IV

EVOLUTION OF SWITCHING CIRCUIT THEORY AND CONCEPTS

Switching circuit theory owes its existence to formal logic which was founded by Aristotle (400 B.C.) when he formalized his system of syllogisms. There are many reports throughout history of attempts by philosophers to find a manageable symbolism for the formalization of logic. Traditionally, the science of the philosopher, logic, has only been of interest to the mathematician in the past century or so. In 1854, an English mathematician, George Boole (1815-1864) presented the first practical system of logic in algebraic form. Boole's publications, the Mathematical Analysis of Logic (13) and The Laws of Thought (14), established a new mathematics called Boolean algebra whereby the problems in logic can be represented and solved in a manner similar to conventional algebra. Since the injection of algebraic logic by Boole, many mathematicians including Augustus DeMorgan, Gottlob Frege, and Russel and Whitehead have made major contributions to what is recognized and employed today as Modern Boolean Algebra.

Algebraic logic was conceived for the purpose of implementing the solution of logic problems concerned with the nature or form of the passage from evidence to conclusions. It was not invented with any technical application in mind. For eighty years, symbolic logic

was generally regarded as an interesting but useless concept with no practical application. In 1938, while still a graduate research assistant at M. I. T., Mr. Claude E. Shannon recognized that the logical structure of an electrical switching circuit was comparable to the structure of symbolic logic -- an instrument of exact thought both analytic and constructive. This logic structure was that Boolean algebra is a two-valued or binary algebra wherein every term has just two exemplary values with systematic rules for the use of three fundamental connectives, AND, OR, and NOT. Shannon's paper (11) demonstrated the application of classical Boolean algebra of symbolic logic by providing an orderly algebraic procedure for the treatment of relay contact networks and thus established him as being the initiator of modern switching theory.

Switching Equations

A Boolean switching equation completely describes the interconnection of switching elements and the required binary components. The variables associated with a Boolean equation are the various letters comprising the function. Each individual entry of an equation is termed a literal of the function. If the equation describes an electrical switching circuit, the literals represent individual switches A, B, C, etc. A literal can only possess two values, 0 and 1, in the same manner that a binary switch can be either off (0) or on (1).

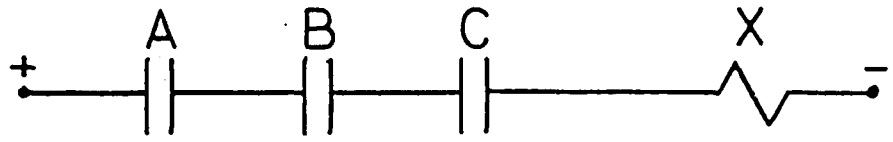
The fundamental connectives, AND, OR, and NOT, describe the interconnection of the literals or switches. These "connectives" are commonly referred to as logic functions and have the following customary

symbols: AND = · as in conventional multiplication, OR = + as in conventional addition, and NOT = $^{-}$ with the complementation sign above the indicated literal. Both the AND and OR connectives are binary operations whereas the NOT connective is a unary operation.

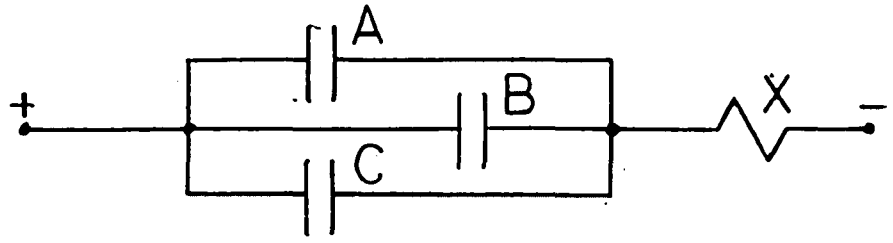
In a Boolean equation containing only literals and AND functions (such as ABC), the equation has a value of one if A = 1 AND B = 1 AND C = 1. Relating this concept to a switching circuit, an output is produced only when all of a given number of input signals are applied. Hence, A must be closed AND B must be closed AND C must be closed to obtain an output signal. The switching circuit representing the equation X = ABC is shown in Fig. 4-1 (a).

An OR logic equation (such as A + B + C) has a value of one if A = 1 OR B = 1 OR C = 1; therefore, to obtain an output from the inferred circuit, A must be closed OR B must be closed OR C must be closed. The electrical circuit describing the OR equation X = A + B + C is illustrated in Fig. 4-1 (b).

From Fig. 4-1, it can be surmised that the AND function describes series connected switches while the OR function describes parallel connected switches. In a Boolean equation consisting of only a complemented literal (such as $\bar{A}$), the equation has a value of one if A = 0 with the described electrical circuit having an output if A is NOT actuated as exhibited in Fig. 4-1 (c). Thus, an uncomplemented literal suggests a normally-open switch while a complemented literal is a normally-closed switch.



(a) Electrical Circuit for X = ABC



(b) Electrical Circuit for X = A + B + C

(c) Electrical Circuit for X = $\bar{A}$

Fig. 4-1. Circuit Configurations for Logic Functions

Application of Logic Processes

It has been demonstrated that a Boolean equation is a logic expression for a circuit configuration whereby the output is described in terms of the variables. Complete confidence must be established in the relationship between a logic expression and its corresponding circuit configuration. In order to promote this confidence, the circuit illustrated in Fig. 4-2 will be discussed.

It can be seen that the excitation of solenoid X in Fig. 4-2 is accomplished by exciting A AND either B OR NOT C or in another way by exciting C AND NOT B. The Boolean expression for the above logic

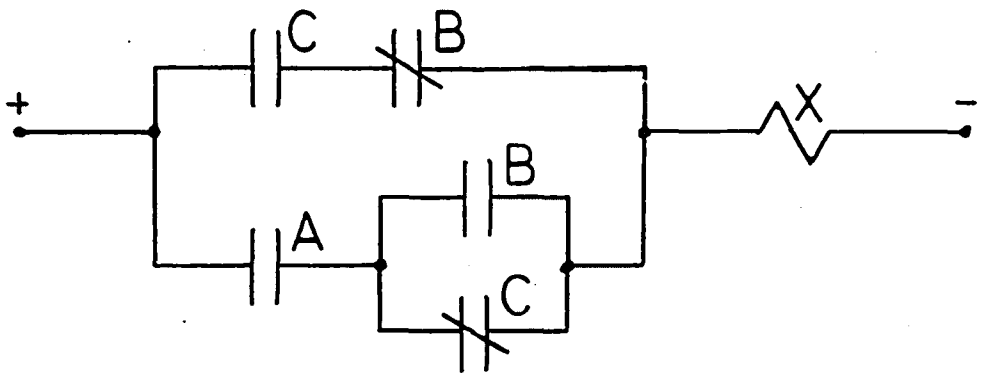


Fig. 4-2. Circuit for the Expression $X = A(B + \bar{C}) + C\bar{B}$

statement is

$$X = A(B + \bar{C}) + C\bar{B} \qquad 4\text{-}1$$

This circuit interpretation concept involving electrical contacts is both simple and fundamental and can be applied to electrical circuits in every case. However, the question arises whether the circuit represented by a given Boolean expression contains redundancies which could be eliminated to yield a simpler configuration. There are several procedures which can be employed to minimize circuit configurations. The procedures to be presented have been selected not only for their utility value in simplifying circuit equations but for demonstrating several basic concepts and relations of Boolean algebra.

The simplification of Eq. 4-1 can be achieved by employing the fundamental theorems of Boolean algebra presented in Appendix A. The theorems of Boolean algebra establish the fundamental rearrangements which are possible without affecting the equivalence of the equation or circuit. These theorems are often classified in terms of the number of variables involved; for example, single variable theorems,

two variable theorems, etc. Expanding Eq. 4-1 by the use of Theorem T-11 (a) results in

$$X = AB + A\bar{C} + C\bar{B} \qquad 4\text{-}2$$

Using Theorem T-14(a) gives the identity

$$A\bar{C} + C\bar{B} = A\bar{C} + C\bar{B} + A\bar{B} \qquad 4\text{-}3$$

Substituting the identity (Eq. 4-3) into Eq. 4-2, yields

$$X = AB + A\bar{C} + C\bar{B} + A\bar{B} \qquad 4\text{-}4$$

Applying Theorem T-11 (a) gives

$$X = A(B + \bar{B}) + A\bar{C} + C\bar{B} \qquad 4\text{-}5$$

The reduction of Eq. 4-5 can be accomplished by using Theorem T-4 (b) which produces

$$X = A + A\bar{C} + C\bar{B} \qquad 4\text{-}6$$

By employing Theorem T-7 (a), the final simplified equation becomes

$$X = A + C\bar{B} \qquad 4\text{-}7$$

Another method for achieving the simplification of a circuit equation as well as gaining an insight into the fundamental characteristics of Boolean algebra is the application of the truth table. A truth table is a display of all the possible combinations of values of the variables and the resulting effect of each combination on the output value. The specification for the operation of solenoid X in Fig. 4-2 is given by the circuit equation (Eq. 4-1). Since three variables (A, B and C) are involved, there are 2^3 or 8 combinations of values for the three binary variables. The truth table for Eq. 4-1 is shown in Table 4-1.

In the truth table shown in Table 4-1, the first three columns merely depict all the ways in which the two values 0 and 1 can be

assigned to the variables A, B, C. The fourth column shows the result of the particular values of the variables on the value of the output (X) as indicated by the circuit equation (Eq. 4-1). The Postulates of Boolean algebra as presented in Appendix A are required to evaluate the output condition (value of the equation) for prescribed

TABLE 4-1

TRUTH TABLE FOR $X = A(B + \bar{C}) + C\bar{B}$

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

inputs (values of the variables). For example, the value of X for input values of A = 0, B = 0, and C = 1 can be evaluated by substituting the values of the variables in the equation as follows:

$$X = A(B + \bar{C}) + C\bar{B} \qquad 4\text{-}1$$

$$X = 0(0 + 0) + 1(1)$$

Using Postulate P-2 (b), gives

$$X = 0(0) + 1(1)$$

Applying Postulates P-2 (a) and P-3 (a) yields

$$X = 0 + 1$$

Using Postulate P-4 (b) gives X = 1 which is recorded in the X column of the truth table opposite the corresponding input variable values.

The truth table shown in Table 4-1 reveals that the excitation of X is desired when any one of five input conditions is satisfied; hence, the following equation satisfies the truth table:

$$X = \bar{A}\,\bar{B}\,C + A\,\bar{B}\,\bar{C} + A\,\bar{B}\,C + A\,B\,\bar{C} + A\,B\,C \qquad 4\text{-}8$$

The simplification of Eq. 4-8 using the fundamental theorems of Boolean algebra can be accomplished as follows:

By the distributive law Theorem T-11 (a)

$$X = \bar{A}\,\bar{B}\,C + A\bar{B}(\bar{C} + C) + AB(\bar{C} + C) \qquad 4\text{-}9$$

Using theorem T-4 (b)

$$X = \bar{A}\,\bar{B}\,C + A\bar{B} + AB \qquad 4\text{-}10$$

Applying Theorems T-11 (a) and T-4 (b) again gives

$$X = \bar{A}\,\bar{B}\,C + A \qquad 4\text{-}11$$

Using Theorem T-8 (a) or Theorem T-13 (a) results in

$$X = A + \bar{B}C \qquad 4\text{-}7$$

The circuit described by Eq. 4-7 and shown in Fig. 4-3 represents the simplest form of the original equation (Eq. 4-1). It should be noted that the circuit possesses the same characteristics as the original circuit (Fig. 4-2).

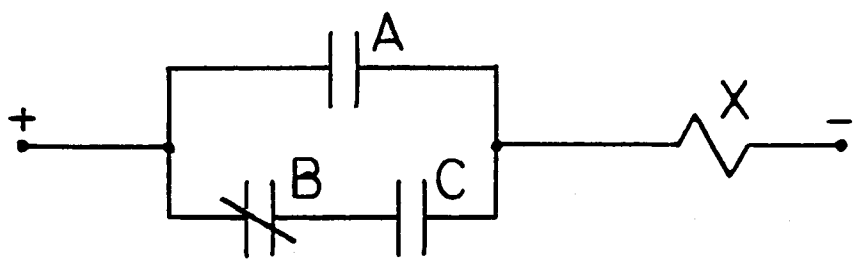


Fig. 4-3. Circuit for $X = A + \bar{B}C$

Graphical Simplification

There have been a number of methods proposed -- Quine (15, 16), McCluskey (17), and Veitch (18) -- for accomplishing the simplification of Boolean equations without resorting to the repeated application of Boolean theorems. It is not the purpose of this exposition to present and criticize such methods, but there is one particular method that is most useful and provides a basis for future considerations of concern to this study. This method is termed the Karnaugh Map Method and is based principally on Theorem T-9 (a), i.e., $XY + X\bar{Y} + X$. The Karnaugh map utilizes the reflected binary (Gray Code) ordering system for the rows and columns of the map rather than a straight binary ordering system. A Gray Code is a method of counting in a binary number system such that only one binary bit changes at a time. A comparison of the two code systems can be observed in Table 4-2.

TABLE 4-2

STRAIGHT AND REFLECTED BINARY CODES

	0 0 0		0 0 0
	0 0 1		0 0 1
	0 1 0	Reflected	0 1 1
Straight	0 1 1	Binary	0 1 0
Binary	1 0 0	or	1 1 0
Code	1 0 1	Gray	1 1 1
	1 1 0	Code	1 0 1
	1 1 1		1 0 0

Karnaugh maps represent circuit or Boolean expression in their fully expanded form much like truth tables. However, a map in contrast

to the truth table exhibits basic patterns which permit the simplest expression to be read directly. Using the procedures for developing the Karnaugh map as outlined in Appendix B, Eq. 4-8 can be expressed in map form as shown in Fig. 4-4.

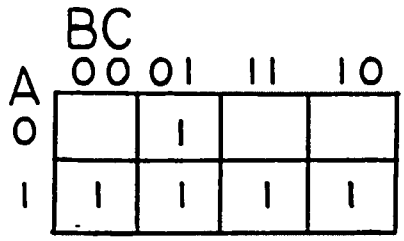


Fig. 4-4. Karnaugh Map for Eq. 4-8

Employing the reading technique presented in Appendix B, Eq. 4-7 can be read directly from the map by letting all entries in row 1 be represented by A and the entries in column 01 be represented by $\bar{B}C$. Furthermore, it can be seen that the original equation represented by Fig. 4-2 is not the simplest form because it was obtained by considering three separate group patterns on the map rather than two. The three patterns are: 1) row 1 -- columns 00 and 10; 2) row 1 -- columns 11 and 10, and 3) rows 0 and 1 -- column 01.

Although the Karnaugh map completely describes a Boolean equation in all of its forms, a reasonable amount of practice is required to appreciate its effectiveness. A Karnaugh map can be read very fast and proficiently for equations having four or less variables; but since the map doubles in size for each variable included, it becomes almost prohibitive above eight or ten variables.

From the discussion already presented on the characteristics and interpretation of Boolean equations, it should be apparent that it is

possible to manipulate a function into many different algebraic forms without changing the equivalence. Also, for every algebraic form of an expression, a correspondingly different circuit is obtained. Symbolic logic has, therefore, provided the means to achieve circuit uniqueness with logical identity.

Types of Circuits

The application of Boolean algebra to switching circuit design has been a major contributing factor to the successful synthesis of complex electrical control and computer systems. It became the instrument for increasing the reasoning power of design engineers and can be credited for many baffling devices in present day use. The phenomenal growth of many control areas such the electronic computer has resulted from the cascading of rather simple, module-type circuits to form complex machine networks.

Fortunately, the type circuitry needed to formulate many control systems of interest in the past has been of a type which could be cascaded and synthesized by a reasonable extension of binary algebraic theory. The type circuit referred to is designated as combinational circuits. Combinational logic is characterized by functional values which are dependent only on the existing values of the independent variables. This type circuit establishes a definite combination of output conditions for a given combination of input conditions regardless of input order; hence, the output is completely dependent upon present input conditions.

The synthesis of electrical combinational circuits has become a

mature field. Many detailed studies -- see (19, 20, 21, 22, 23) -- have been reported in the literature on the logical design of almost all classes of these circuits including series-parallel networks, multi-terminal contact networks, and non-series-parallel networks. Based on these studies, the design of many classes of combinational circuits has reached a point of being almost a routine procedure for switching circuit engineers. The technique used to develop the associated networks of combinational circuits involves the requirements for each output and the necessary inputs to achieve the desired output condition.

The initiation of a switching circuit design by intuitive or logical means requires a rigorous formulation of the conditions necessary to activate each output. Such a formulation means a firm set of specifications which is logically meaningful in a manner that is unambiguous and non-contradictory. Simple statements are needed covering every combination of logical conditions as to what is required, what is not required, and what is of no concern or importance. A proficient method for insuring that all possible combinations of states have been considered is to prepare a truth table or Karnaugh map whereby the desired output conditions can be considered for all combinations of input variables. Contradictory statements can also be discovered with such a logic tool and rectified in the formulative stage. Any table of combinations such as the truth table or Karnaugh map which contains each of the 2^n possible combinations of values of the variables will specify the Boolean functions needed to develop the prescribed network. Furthermore, such a table can always be satisfied

by a combinational circuit.

The synthesis of switching circuits presents two basic problems to the engineer. First, a circuit must be designed which will satisfy the specifications of the input-output relations. Second, the circuit should contain the most economical selection and arrangement of functional hardware. The accomplishment of the second problem has occupied the minds of many designers, and a substantial degree of success has been achieved through the recognition of basic circuit forms in combinational circuit equations. New and efficient techniques are constantly appearing in the literature for obtaining circuits containing a minimum number of binary elements. Although considerable work still remains to be accomplished on designing minimal networks, substantial contributions are already in evidence. A literature survey conducted for this study revealed that over 250 different people working with switching circuit theory have reported their findings. Adding to this total the many unknown investigators, results in a fabulous concentration of brains in one area which is developing beyond comprehension.

Combinational switching logic, although representing a very important type in electrical control systems, does not satisfy the requirements for circuits involving memory or sequential action. All switching circuits can be classifed as either combinational or sequential, and it is the latter type that has a great potential in other associated fields. Sequential logic is characterized by functions which depend not only on the immediate values of the variables but also on the values of variables at some previous time. Therefore, by

definition, a sequential circuit is one in which the output is related not only to the present inputs but also the past history of the inputs.

A sequential logic requirement presents a far more difficult problem to the engineer than one which can be satisfied by combinational logic. Prior to 1954, there was no method which was universally applicable to sequential problems. D. A. Huffman (12) was the first to develop a method by which the past input conditions of a system could be recorded and become an integral part of the solution. He presented a chart, called a "flow table," that could be used to register the past input conditions and define the operation of the desired circuitry. The horizontal rows of a flow table represent the internal states of a system whereas the vertical columns represent all possible input conditions. The entries in the flow table are the various states of the system which are implied by the circuit specification. The flow table is systematically transformed into Karnaugh maps which describe the memory and output circuits which can be read in terms of individual combinational circuit expressions.

Concurrently and independently of Mr. Huffman, E. A. Moore (25) studied the properties of sequential machines and developed a theory which parallels many aspects of the Huffman Method. Another noteworthy publication having a pioneer influence on sequential logic methods is that of George H. Mealy (26). Mealy's extensive report was directed more along the lines required in telephone switching circuits, but he clarifies several aspects on reduction techniques of concern in the Huffman-Moore Model.

Since the principal objective of this dissertation is the analysis

and synthesis of hydraulic sequential circuits, a detailed discussion of sequential logic as applicable to hydraulic circuits is contained in the next chapter. The concepts of electrical sequential logic theory as purported by the above cited references and others (26, 27) have been instrumental in providing the basis for the hydraulic circuit synthesis and analysis methods to be presented. Without this basis, an unpredictable and almost insurmountable amount of work would have been added to this investigation.

CHAPTER V

CIRCUIT SYNTHESIS FOR FLUID DIGITAL NETWORKS

Synthesis is the process of putting together to form a whole and is the opposite of analysis. In relation to this study, the process consists of finding a network that satisfies a prescribed set of requirements. The utilization of logic techniques capable of producing complete descriptions of complex fluid networks will require a significant extension of ordinary fluid signal system concepts. A demand for fluid power systems to be controlled by secondary signal networks is expressed. Such power systems must be responsive to control by fluid signals and must report their output conditions in the form of fluid signals. The above requirements are not necessarily incongruent with the current general philosophy of fluid system design because automatic and semi-automatic electrical-controlled, fluid-powered machines receive and emit electrical signals.

In order to provide a basis for the further discussion of fluid signal control, an example of a fluid-powered system exhibiting fluid signal admittance and emittance characteristics is shown in Fig. 5-1. and the corresponding electrical-controlled system in Fig. 5-2. Both motor systems have provisions for generating signals to report load and position information and possess appropriate transmission valves

for directing the motor. The hydraulic circuit symbols of the ASA (American Standards Association) will be used for all fluid circuit illustrations.

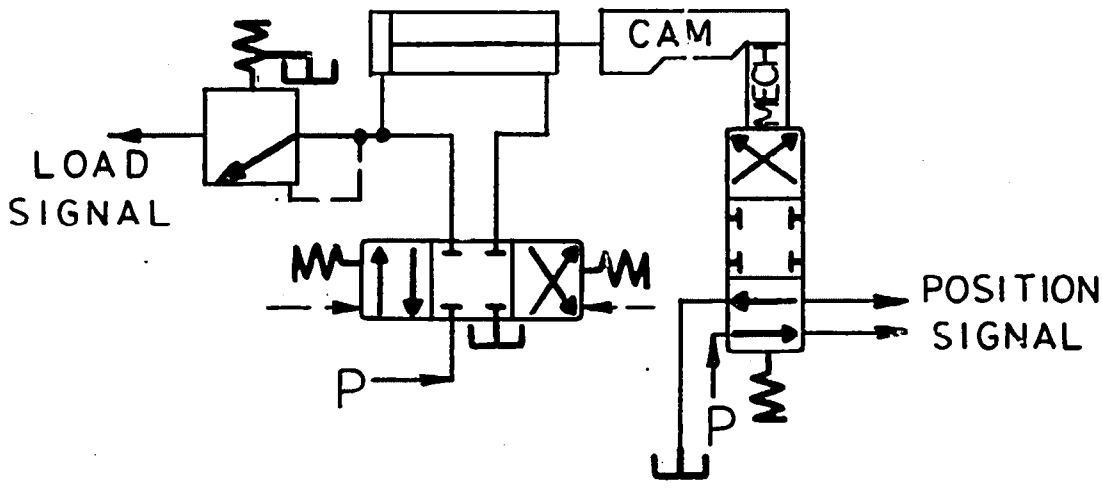


Fig. 5-1. A Fluid-Powered Fluid-Controlled Motor System.

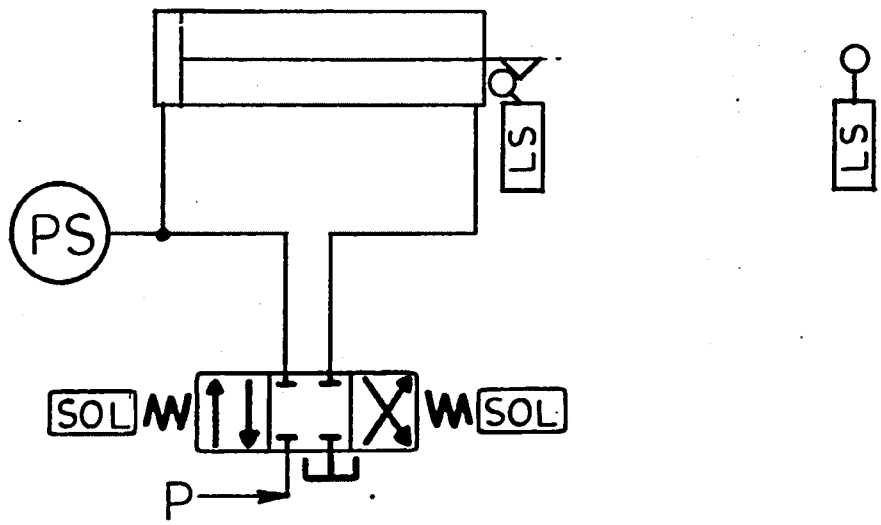


Fig. 5-2. A Fluid-Powered Electrical-Controlled Motor System

A fluid system may require the use of several fluid motor systems with various input-output characteristics to accomplish the objectives of the machine. To implement specific operational requirements, many different valve configurations are available and considered standard components. Reference is made particularly to two-position, three- and four-way valves, also to three-position, four-way (block center, open center, center bypass, etc.) valves. The power valves in Figs. 5-1 and 5-2 are three-position, block-centered, spring-centered, four-way valves.

Establishing the specific types of fluid powered motor systems for a machine enables the operational specification to be defined. A firm set of specifications must contain precise statements as to the desired output for each and every combination of input-output condition. The formulation of such a specification is undoubtedly one of the most difficult problems in control network synthesis. However, if the designer can obtain a decision on the necessary output for each (2^n) combination of inputs, plus information of a sequential nature on the order of events, a logical synthesis process can be initiated.

A letter symbol is assigned to each output from the fluid motor system (an input to the control network) and to each input required by the motor system (an output of the control network). It is conventional to assign network inputs as x_1, x_2, etc., and network outputs as Z_1, Z_2, etc. In relation to network outputs, the motor power valve can be incorporated into the control network with Z_1 and Z_2 becoming the transmission lines to actuate the fluid motor instead of signal fluid.

The output from a valve could have three distinct transmission conditions: 1) connected to pressure, 2) connected to tank, and 3) blocked to pressure and tank. To implement this study, valves possessing block port characteristics will not be considered as suitable control network elements. No major limitation is inferred by this restriction which makes possible the criteria that the binary value 1 means open or pressurized while 0 means a tanked condition.

One important aspect which must be recognized is termed the stability characteristics of a valve. This characteristic refers to the excitation and transmission of a valve. A time delay always exists between the time a valve is signalled to operate (excited) and the time when transmission is actually accomplished. A valve is considered to be in a stable condition during the period when a signal is applied and when transmission occurs. The stable condition occurs when the transmission function agrees with the excitation. This concept of stability can also be extended to control network operation -- the time delay between network excitation and network transmission. In a network, the time delay of several valves may be involved which gives rise to network instability.

Fluid Circuit Description

The fluid circuit synthesis technique which will be discussed is based on the flow table method originated by Huffman (14). The technique establishes a general approach to the logical synthesis of fluid networks and does not require intuitive reasoning. It has application to the broad class of fluid switching circuits involving memory and

possesses the necessary characteristics to effect a comprehensive understanding of the system.

The procedure used to synthesize fluid circuits involves a number of steps which require various describing charts to develop a solution. The complexity of the technique is such that a written presentation becomes almost meaningless without the simultaneous demonstration of the rules; therefore, a specific problem will be considered throughout the discourse to illustrate the procedure. Let it be assumed that a fluid network is required to control the two-cylinder motor circuit shown in Fig. 5-3. The desired operation of the cylinders is: cylinder A cycles once (A,$\underline{A}$); cylinder B extends (B); cylinder A cycles again (A,$\underline{A}$); and cylinder B retracts ($\underline{B}$). The shorthand circuit operation is then A,$\underline{A}$,B,A,$\underline{A}$,$\underline{B}$. The detent valves have mechanical spring locks to hold the last position of the valve until a fluid signal overcomes the detent force and repositions the valve's actuating element. The network to be designed will receive two inputs (x_1, x_2) and excrete two outputs (Z_1, Z_2) as indicated by the diagram.

The network synthesis is initiated by the development of a primitive flow table which depicts the various states the network must satisfy for the specified input and outputs. The primitive flow table is constructed from the word statement of the problem and exhibits the desired operational sequence in accordance with both input and output conditions. The primitive flow table reveals any contradictory or incomplete specifications, and the acceptance of its implications becomes irrevocable beyond this point.

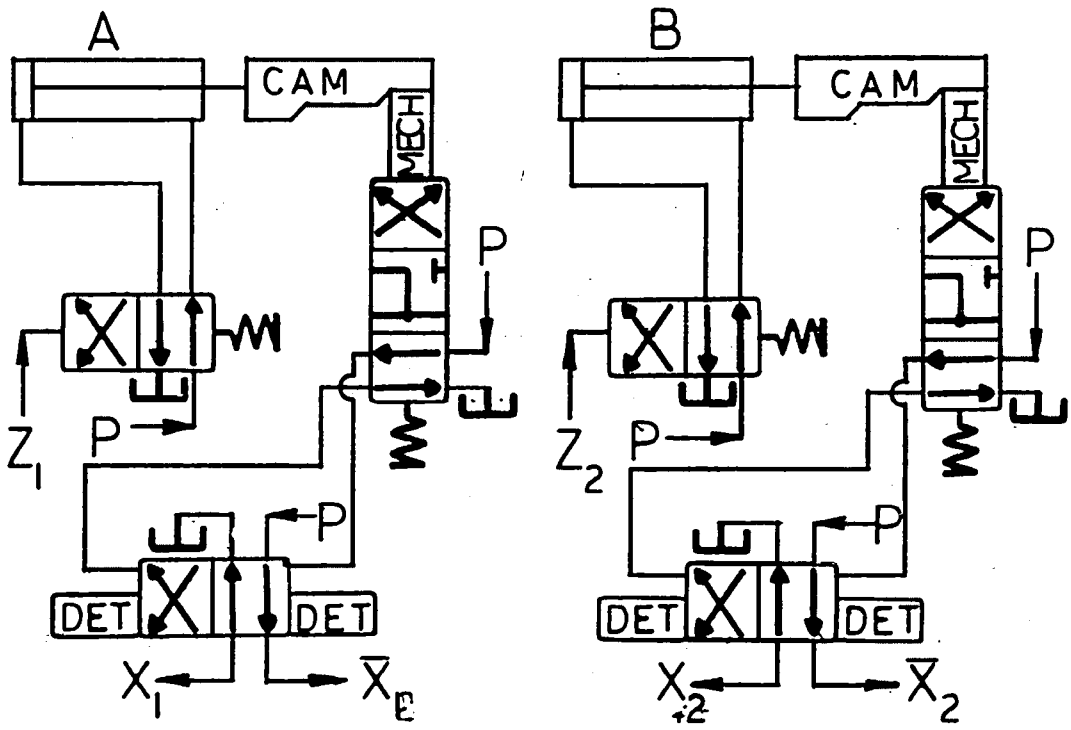


Fig. 5-3. Two-Cylinder System with Operation A,A,B,A,A,B

The flow table is comprised of rows and columns. The combinations of all inputs are represented in Gray code form and are the headings for the basic columns. The rows can be considered as representing the secondary states of the network. The state positions (operational events) both stable and unstable become entries in the table. The output conditions corresponding to each state entered in the table are listed in a special column on the right in the appropriate row. The stable states are circled with only one stable state assigned to a row. It will be evident that a change in an input condition represented on the flow table results in a state change in another secondary. In other words, when an input change occurs, the network moves from a stable state to an unstable state in the same row and then transfers

to a stable state in another row.

To initiate the recording of the operational description of the circuit action, a starting point must be selected. It is convenient for the cited example problem to assume that the cylinders have just arrived in the position shown in Fig. 5-3. At this point, the network input is $x_1 = 0$ and $x_2 = 0$, and the output of the network must be $Z_1 = 1$ and $Z_2 = 0$ to extend cylinder A. After cylinder A extends, the input changes to $x_1 = 1$ and $x_2 = 0$; and the output changes to $Z_1 = 0$ and $Z_2 = 0$. This process of reasoning continues until the full operational specification has been described as shown in Table 5-1.

TABLE 5-1

PRIMITIVE FLOW TABLE FOR 2-CYLINDER PROBLEM

Row	x_1 x_2 Inputs 00	01	11	10	Outputs Z_1 Z_2
1	①			2	10
2	3			②	00
3	③	4			01
4		④	5		11
5		6	⑤		01
6	1	⑥			00

Flow Table Reduction

The second step in a network synthesis problem is the reduction of the primitive flow table. Flow table simplification is an important phase of network synthesis because the design evolves from this table. Since the rows of a flow table represent the various internal

states required within the control network, it is worthwhile to apply methods that will minimize the number of rows. One method which should be applied is the check for redundant states. Such states are duplications and have their equivalence already represented on the table. Establishing the equivalence of two stable states results in the elimination of one row from the flow table. Three requirements must be satisfied before an equivalence exists between two stable states:

1. They are in the same column
2. They have the same output state
3. The states in each column of both rows must be the same or equivalent

Since the blanks in the primitive flow table represent unspecified entries or optional states, it is permissible to utilize their optional behavior to establish an equivalence whenever possible. No redundancies are evident in the flow table for the two-cylinder circuit example. This can be recognized because two stable states having the same output conditions do not exist in the same column.

Another means for achieving flow table simplification is termed merging. The merging process does not reduce the number of stable states in the table but eliminates some of the rows. This is accomplished by having more than one stable state assigned to a row as originally established by the flow table. Merging the rows of a primitive flow table to form a merged flow table is not dependent upon the output states. The rules for merging two rows of a flow table are:

1. The state numbers in both rows within each column must coincide, or

2. A state number in one row coincides with an optional term or blank space in the same column, or

3. Optional terms (blank spaces) are contained in both rows within corresponding columns.

Applying the above rules for merging the rows of a primitive flow table to the problem example, it can be observed that row 1 could merge with any one of rows 4, 5, or 6. Likewise, row 2 could merge with rows 3, 4, or 5; row 3 with row 4; and row 5 with row 6. In most instances, there are several ways to accomplish a merger; but for component and circuit economy, an optimum merger is desirable. In order to achieve such a merger, it is helpful to prepare a table of possible mergers and finally a merger diagram. A table of possible mergers for the example problem is shown in Table 5-2.

TABLE 5-2

TABLE OF POSSIBLE MERGERS FOR 2-CYLINDER PROBLEM

ROW	WITH	ROW
1		4
1		5
1		6
2		3
2		4
2		5
3		4
5		6

Using the table of possible mergers, a diagram can be drawn which graphically displays the merging characteristics of the rows. The merger diagram consists of a circular array of circled numbers -- each number representing a row or stable state number on the primitive flow table. For each possible merger between two rows, a connecting

line is drawn on the diagram between the appropriate numbers. Applying this procedure to the example problem yields a merger diagram as shown in Fig. 5-4.

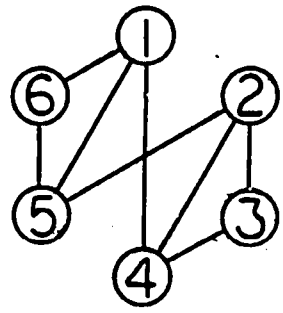


Fig. 5-4. Merger Diagram for 2-Cylinder Problem

The primary purpose for merging is to achieve an optimum configuration which generally can be interpreted to mean a minimum number of rows in the final merged flow table. To obtain this minimal value requires that the merger diagram be studied and manipulated to derive the most appropriate combinations of row mergers. The merger diagram aids in the identification of "clustered" and interconnected points. A merged combination is adequate when each number comprising the combination is linked with each and every other number in the combination. In many instances, there are more than one combination which would yield a minimum row merger. When such a situation exists and it is important to achieve the most economical circuit, all minimum row combinations should be explored. The most optimum merged groups for the 2-cylinder problem are rows 1, 5, and 6 and rows 2, 3, and 4. Using these two groups, the merged flow table for the example problem is as illustrated in Table 5-3.

TABLE 5-3

MERGED FLOW TABLE FOR 2-CYLINDER PROBLEM

	$x_1 x_2$ 00	01	11	10
a	①	⑥	⑤	2
b	③	④	5	②

The output column of the primitive flow table does not appear in the merged flow table because the outputs are associated with the stable states and not with the rows. The specified outputs have not been changed during the merger; however, they can no longer be exhibited on the flow table.

If the primitive flow table can be reduced to a merged flow table containing only one row, the desired output of the circuit is a function of only the input conditions and therefore becomes a combinational type circuit. When more than one row exists in the merged flow table, it indicates that the desired outputs are a function of not only the input conditions but also of the secondary states of the circuit. In such a situation, the circuitry must possess memory elements and be of the sequential logic type. Each row of the merged flow table must be represented by a different secondary state in the same manner as the columns of the flow table are uniquely specified. Two rows require one secondary specification ($y = 0$ and $y = 1$); whereas three or four rows require two secondaries ($y_1 = 0$ and 1 and $y_2 = 0$ and 1). In the case of an odd number of rows greater than one, a secondary state is provided -- one row containing only blank entries. In essence, the

existence of secondary rows in the merged flow table means that the circuit logic is such that the outputs cannot be described by simply the input functions, and that an internal circuit is required to generate "pseudo inputs" to perform the memory action.

The Operational Flow Table

Possessing the merged flow table and having established the number of secondaries required, it is necessary to label the rows appropriately in order to obtain the operational flow table. This process is termed "making secondary assignments." No secondary assignment problem exists with a two row merged flow table because only one secondary is required which means that one row is labeled 0 and the other 1. This is the situation with the 2-cylinder example under consideration; therefore, the corresponding flow table with secondary assignments is as shown in Table 5-4. In accordance with the inferences of Table 5-4, the logic action of the 2-cylinder problem can be accomplished with one binary-secondary circuit.

TABLE 5-4

OPERATIONAL FLOW TABLE FOR 2-CYLINDER PROBLEM

	x_1 x_2			
y	00	01	11	10
0	①	⑥	⑤	2
1	③	④	5	②

Merged flow tables having three or more rows generally present a problem in labeling the rows. The problem stems from the need to obtain

the "next state" by a unary action of the secondary. In other words, a necessary transition from one row to another should be accomplished by a single change in the secondary. Since the order or arrangement of the rows is arbitrary in the merged flow table, any reshuffling of row positions is permissible to accomplish proper circuit action. The transition problem can be illustrated by the use of the hypothetical merged flow table shown in Table 5-5.

TABLE 5-5

MERGED FLOW TABLE FOR A HYPOTHETICAL ACTION

	$x_1 x_2$ 00	01	11	10
a	①	2	⑤	6
b	⑦	8	③	4
c	7	②	3	⑥
d	1	⑧	5	④

By the inspection of Table 5-5, it can be seen that a number of transitions exist between non-adjacent rows; for example, in the transition from unstable state 2 to stable state 2, row "b" must be "jumped" and similarly for state 6. Such a "jump" would necessitate the internal state of two secondaries to change simultaneously. An action which is dependent upon the simultaneous response of two circuits is unpredictable and should not be considered. To avoid this transition problem, the rows of the flow table should be arranged so that "jumping" is unnecessary. The proper arrangement can be discovered with the aid

of a transition map. Such a map consists of columns and rows describing the required combinations of secondary states together with map entries representing the row numbers or letters. The initiation of row entries into the transition map is made by arbitrarily assigning row "a" to the "all-zero" position. Subsequent row designations are entered in the map to accomplish proper adjacent relations -- no diagonal transitions on the map. The transition map for the merged flow table shown in Table 5-5 is exhibited in Fig. 5-5.

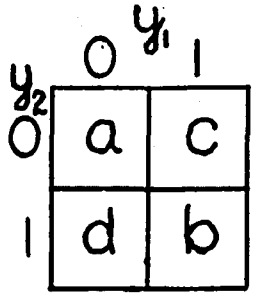


Fig. 5-5. Transition Map for Hypothetical Problem

Employing the transition map shown in Fig. 5-5 to arrange and label the rows of the flow table in Table 5-5, yields a properly assigned secondary. The operational flow table for the hypothetical problem with indicated secondary assignments is shown in Table 5-6. This flow table satisfies all adjacency requirements which means that all row-to-row excursions for a given state can be achieved by the change of only one secondary variable. It should be pointed out that the top and bottom rows are, by the definition above, adjacent rows.

TABLE 5-6

OPERATIONAL FLOW TABLE FOR HYPOTHETICAL PROBLEM

$y_1\ y_2$ \ $x_1\ x_2$	00	01	11	10
00	①	2	⑤	6
01	1	⑧	5	4
11	⑦	8	③	4
10	7	②	3	⑥

The Secondary Network

The operational flow table containing secondary states with assigned values becomes the basis for obtaining the logic circuit equations. Two types of circuits are involved in a sequential system -- secondary circuits and output circuits. In order to derive the equations for the secondary circuit, an excitation map must be obtained. This map is equivalent to the operational flow table except that the map entries are the desired secondary states for the appropriate map locations. The entries for the excitation map are designated as follows:

1. The entry for a stable state position indicated on the operational flow table is the same as the existing secondary state (operational event).

2. The entry for a given unstable state is the same as the next desired secondary state.

Applying the above procedure for making map entries to form the excitation map results in a completely specified binary valued map. The excitation map shown in Fig. 5-6, for the 2-cylinder problem

example was obtained from Table 5-4, and the excitation map for the hypothetical problem, exhibited in Fig. 5-7, was derived from Table 5-6.

y \ x_1x_2	00	01	11	10
0	0	0	0	1
1	1	1	0	1

Fig. 5-6. Excitation Map for 2-Cylinder Problem

y_1y_2 \ x_1x_2	00	01	11	10
00	00	10	00	10
01	00	01	00	01
11	11	01	11	01
10	11	10	11	10

Fig. 5-7. Excitation Map for Hypothetical Problem

The excitation map represents the secondary states which must exist to satisfy the sequence specification of a circuit; therefore, the Boolean expressions deduced from the map are the circuit equations of the secondary excitation network. Using the Karnaugh Map technique for obtaining the Boolean equations (see Appendix B), the equation of the secondary circuit for the 2-cylinder problem is

$$Y = y\bar{x}_1 = x_1\bar{x}_2 \qquad 5\text{-}1$$

The interpretation of this circuit equation in terms of fluid components is reserved for the next chapter.

Excitation maps containing more than one entry in a map location are difficult to read. To overcome this difficulty, individual excitation maps for each secondary can be drawn to simplify the map reading. The individual excitation maps for the hypothetical problem are shown in Fig. 5-8.

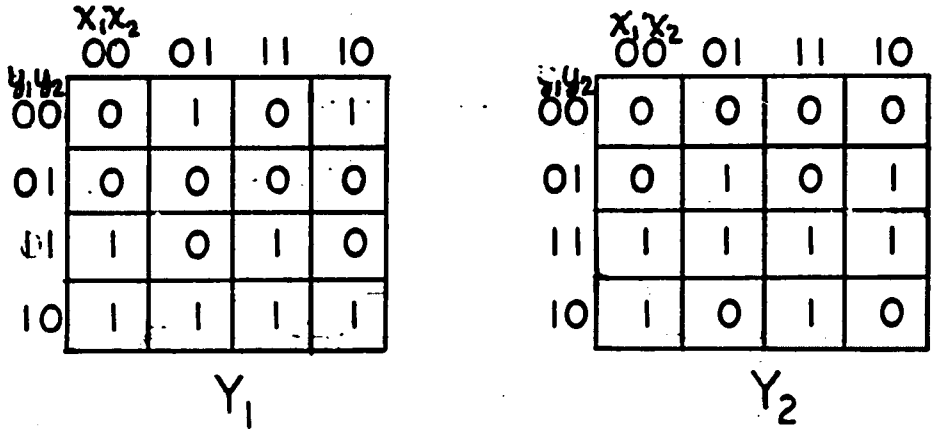


Fig. 5-8. Individual Excitation Maps for Hypothetical Problem

There are many different equations which can represent the entry patterns of a Karnaugh Map. In circuit synthesis, each minimal equation satisfying the map should be considered. The individual excitation maps for the hypothetical problem emphasize the various combinations which could be written to represent the entries of the map. A specific equation satisfying the Y_1 excitation map in Fig. 5-8 is

$$Y_1 = y_1\bar{x}_1\bar{x}_2 + \bar{y}_2\bar{x}_1x_2 + y_1x_1x_2 + \bar{y}_2x_1\bar{x}_2 \qquad 5\text{-}2$$

An expression for the Y_2 excitation circuit is

$$Y_2 = y_1\bar{x}_1\bar{x}_2 + y_2\bar{x}_1x_2 + y_1x_1x_2 + y_2x_1\bar{x}_2 \qquad 5\text{-}3$$

The Output Network

The Boolean equations for the output circuits are derived in a similar manner as the secondary circuit equations. The operational flow table is again utilized, but the map entries are the desired output states instead of the desired secondary states. Since the desired output states of a circuit are recorded in the primitive flow table for each stable and unstable state designated, this table is employed for making the entries in the output map. As in the operational flow table, the columns of the output map are the input states and the rows are the secondary states. The rules for making entries in the output map are as follows:

1. Enter the output state associated with each stable state shown on the primitive flow table in the location of the corresponding stable state on the operational flow table.

2. Between two stable states having the same output states, all unstable states involved in the transition must be assigned the same corresponding output state.

3. The output state corresponding to an unstable state is optional when the output state is changed between two stable states. A dash is entered in the map location to represent the optional output state.

The completed output map describes the conditions under which the prescribed outputs will occur. Applying the rules given above to formulate the output map for the 2-cylinder problem results in a map as shown in Fig. 5-9. Although the output Boolean circuit equations can be deduced directly from the composite output map, individual output maps for the two outputs (Z_1 and Z_2) simplify the map reading. The individual output maps for the 2-cylinder problem are shown in Fig. 5-10. The output map for the hypothetical problem cannot be formulated

because the output states are unknown -- the primitive flow table was not presented.

y \ x_1x_2	00	01	11	10
0	10	00	01	-0
1	01	11	-1	00

Fig. 5-9. Composite Output Map for 2-Cylinder Problem

y \ x_1x_2	00	01	11	10
0	1	0	0	-
1	0	1	-	0

Z_1

y \ x_1x_2	00	01	11	10
0	0	0	1	0
1	1	1	1	0

Z_2

Fig. 5-10. Individual Output Maps for 2-Cylinder Problem

In a combinational logic circuit, the output equations are functions of only the input states; whereas for sequential logic circuits, the output equations are always functions of the secondary states and generally certain existing input states. The Boolean equations for the output circuits of the 2-cylinder problem obtained from the individual output maps are as follows:

$$Z_1 = \bar{y}\,\bar{x}_2 + y\,x_2 \qquad 5\text{-}4$$

$$Z_2 = x_1x_2 + y\,\bar{x}_1 \qquad 5\text{-}5$$

The contribution of the secondary circuit output is an integral part

of the output equations. Neglecting the hardware aspects of the system, the logic requirements of the 2-cylinder control circuit have been satisfied by the three circuit equations (5-1, 5-4, and 5-5). These equations require further study before they are ready for hardware interpretation as will be pointed out in the remaining part of this chapter.

Logical Complications

There are some inherent pitfalls in the synthesis technique that must be recognized and avoided when they restrict or otherwise jeopardize the successful operation of the circuit. An experienced designer having a comprehensive understanding of machine cycle problems and the non-ideal characteristics of circuit components would be cognizant of the "practical" limitations of pure logic interpretations. It is important, however, to be able to recognize the application problems of the logic method as they appear in the synthesis procedure and in a form not requiring a vast amount of experience to correct. The five basic characteristics to be discussed should be recognized in the logic design of circuits. These characteristics are called 1) lockups, 2) oscillations, 3) cycles, 4) races, and 5) hazards.

Lockups

A lockup can be recognized on the flow table by a row which has not been provided with an accessible unstable state. It results in a situation where some state cannot be obtained more than once without a complete interruption of the power. The solution for such a problem is the proper rearrangement of the state entries to insure an unstable

state escape route from the locked-up row or rows. The problem will never occur in a properly developed primitive flow table. Two simplified flow tables are presented in Fig. 5-11 to illustrate a single row lockup and a multi-row lockup.

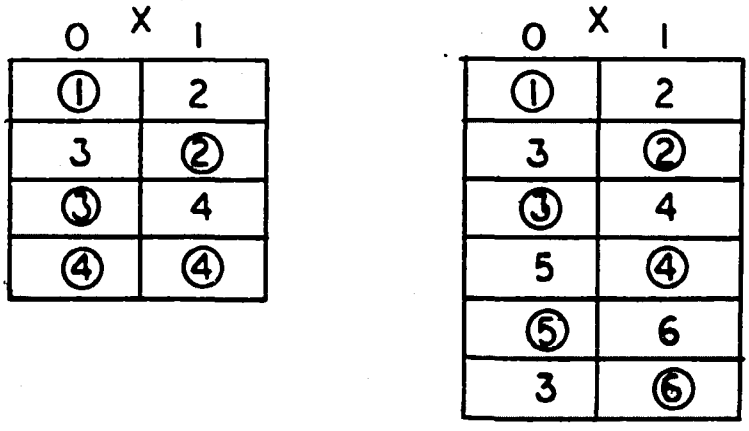


Fig. 5-11. Examples of Single and Multi-Row Lockup Conditions

Oscillations

An oscillation in a circuit stems from an input which makes an unstable state seek a non-existent stable state. Such a condition initiates a row-to-row excursion which cannot be stopped except by another input change. Input changes effect column shifts while unstable states provide the mechanism to cause row excursions. An oscillation can be detected on a flow table by locating an accessible column consisting of only unstable states. Oscillations, as with lockups, result from improperly constructed primitive flow tables. An example of a flow table yielding an oscillation is given in Fig. 5-12.

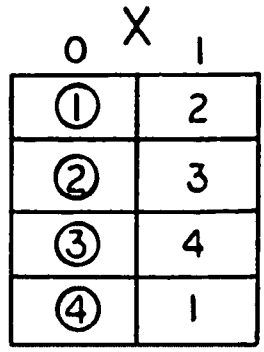


Fig. 5-12. A Circuit Oscillation Example

Cycles

A cycle refers to a cyclic secondary action such as described for an oscillation. An oscillation is a continuous type cycle which usually has a parasitic nature, but it could have some practical value in the production of output pulses or signals. A self-terminating cycle is one in which an unstable state initiates an excursion past more than one row but terminates at a stable state. A cycle of this type is often introduced intentionally to produce time delays for obtaining a prescribed circuit action.

An unstable state is one in which the entry in the excitation map does not agree in value with the designated row value. The unstable state is ordered to react by the appropriate input combination, and it seeks to satisfy its state value; hence, it will move to the row whose labeled value agrees with the unstable state value. A self-terminating cycle is a succession of secondary state designations that generates a cyclic action. Such a cycle can be illustrated as shown in Fig. 5-12 using a simplified flow table and excitation map. The cycle shown in

Fig. 5-13 is a good example of an intentional time delay inclusion in a circuit.

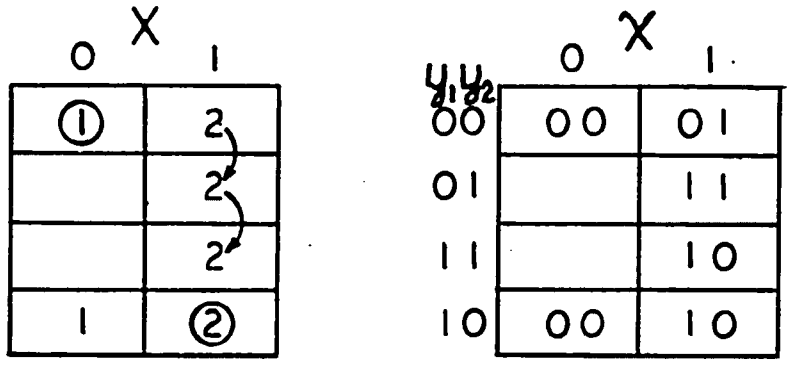


Fig. 5-13. A Self-Terminating Cycle Example

Races

The distinguishing feature of a race is a secondary transition which requires the simultaneous change of two or more secondary states. There are essentially two types of races -- the critical type and the non-critical type. A critical type race can terminate in any of two or more different stable states; hence, a situation exists where an undesired operation may result. It is important to be able to recognize and avoid critical race conditions during the synthesis process because the outcome is not predictable. A race condition exists whenever the value of a map entry representing an unstable state disagrees with the value of the row by more than one binary digit. A critical race exists when the results of the race between the two or more secondary variables cannot be predicted. The characteristics of a critical race are demonstrated in Fig. 5-14. The operation depicted in the illustration indicates that after the input (x) changes from 0 to 1,

stable state 11 is desired; however, both secondaries must change simultaneously to accomplish the proper shift.

y_1y_2	X = 0	X = 1
00	00	11
01	01	10
11	01	11
10	00	10

Fig. 5-14. A Critical Race Condition

The critical race problem can always be solved by the proper application of the transition map during the synthesis process. In certain cases, extra secondary states must be added to avoid transitions which would result in critical races. However, in many cases a cycle can be established that will terminate the secondary excursion on the desired row or on a row where the row value differs from the desired row value by only one binary digit. An example of the use of a cycle to avoid a critical race is given in Fig. 5-15. Several situations are exhibited in the illustration for preventing a critical race. Two useful cycles were inserted starting at row 11 to obtain row 00 in columns 00 and 10. A third cycle was introduced between rows 01 and 10 in column 11. These cycles directed the secondary to the desired position when a two variable change in the secondary was required.

A non-critical race is a predictable event. No matter which variable wins the race, the outcome is the same. A non-critical race

Y_1Y_2 \ X_1X_2	00	01	11	10
00	00	01	00	00
01	00	01	11	00
11	01	11	10	01
10	10	11	10	10

Fig. 5-15. Critical Races Eliminated with Cycles

condition is established when the unstable counterpart of the desired state or an equivalent substitute is entered in the map locations where the race could finish. A non-critical race is indicated in Fig. 5-16 in column 00 between row 11 and 00. The winner of the 01 and 10 race will still yield the desired result. Non-critical races are not detrimental to the operation of the circuit because they have a predictable destination, and they tend to shorten the transition time of the secondaries.

Y_1Y_2 \ X_1X_2	00	01	11	10
00	00	01	10	00
01	00	01	10	—
11	00	11	10	—
10	00	11	10	—

Fig. 5-16. A Non-Critical Race

The discussion of races so far has been restricted to those

affecting row-to-row or secondary operation. A second class of races could be considered for the input characteristics in certain problems. Such races may develop when simultaneous operations are desired which could yield a two variable input change. An example of a column race would be when the initial inputs are 00 and the next input condition is theoretically 11. In this case, unstable states existing in columns 01 or 10 could initiate a row-to-row excursion before the second input signal is registered, and a conceivable state of circuit confusion could result. Column races can be avoided through proper recognition and rearrangement of the flow table logic. The proper interpretation of the basic circuit specifications can usually resolve the problems associated with column races.

Hazards

Static hazards in circuits are somewhat similar to races because they arise due to the imperfect timing that accompanies non-ideal components. However, hazards refer to the operational problems encountered in parallel circuits. Consider the circuit represented by the Boolean equation

$$Y = \bar{x}_1 x_2 + x_1 y \qquad 5\text{-}6$$

The equation implies that if x_2 and y are both actuated (equal to 1), then the circuit should transmit regardless of the state of the valve x_1. But since valve x_1 is not a perfect switching element, during the period of time that x_1 shifts or changes its state, it would be possible for the circuit to lose transmission momentarily. Any unplanned interruption of circuit transmission constitutes a potential hazard

which could affect the entire intended logic of the system.

The excitation map represented by Eq. 5-6 is shown in Fig. 5-17. Each parallel branch of the circuit is identified on the map, in accordance with Appendix B, as a subcube. The two subcubes that constitute the given circuit are both functions of the same variable (x_1 and $\bar{x}_1$). This condition is one of the describing features of a potential hazard. The transmission of a circuit must always be independent of the variable undergoing a change.

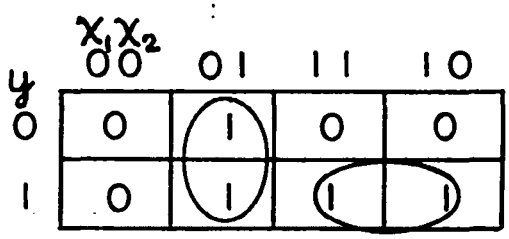


Fig. 5-17. Excitation Map Illustrating Potential Hazard.

To eliminate a potential static hazard, the circuit equation must possess terms that make the transmission independent of a changing variable. Although Eq. 5-6 accurately describes the logic conditions implied by the map in Fig. 5-17, an alternate route (parallel path) must be provided to maintain transmission during the period when the dependent variable changes. This route or path is termed the "hazard subcube," and it connects the subcubes required by the logic conditions of the problem. The hazard subcube which eliminates the hazard in Fig. 5-17 is shown dashed in Fig. 5-18 and modifies the circuit equation as follows:

$$Y = \bar{x}_1 x_2 + x_1 y + x_2 y \qquad 5\text{-}7$$

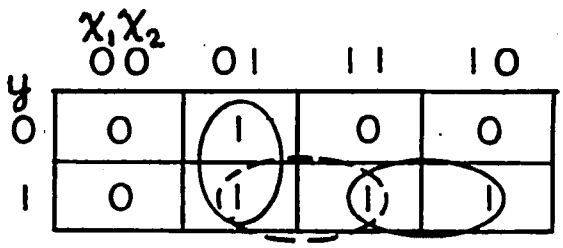


Fig. 5-18. Hazard Subcube for Eliminating Potential Hazards

Employing the concept of hazard subcubes to eliminate potential hazards in the excitation maps for the hypothetical problem shown in Fig. 5-8 results in a subcube for Y_1 of the entire (10) row and for Y_2 of the entire (11) row. The subcubes for this problem are shown in Fig. 5-19. The excitation equations previously derived must be modified to include the hazard subcube terms as follows:

$$Y_1 = y_1\bar{x}_1\bar{x}_2 + \bar{y}_2\bar{x}_1x_2 + y_1x_1x_2 + \bar{y}_2x_1\bar{x}_2 + y_1\bar{y}_2 \qquad 5\text{-}8$$

$$Y_2 = y_1\bar{x}_1\bar{x}_2 + y_2\bar{x}_1x_2 + y_1x_1x_2 + y_2x_1\bar{x}_2 + y_1y_2 \qquad 5\text{-}9$$

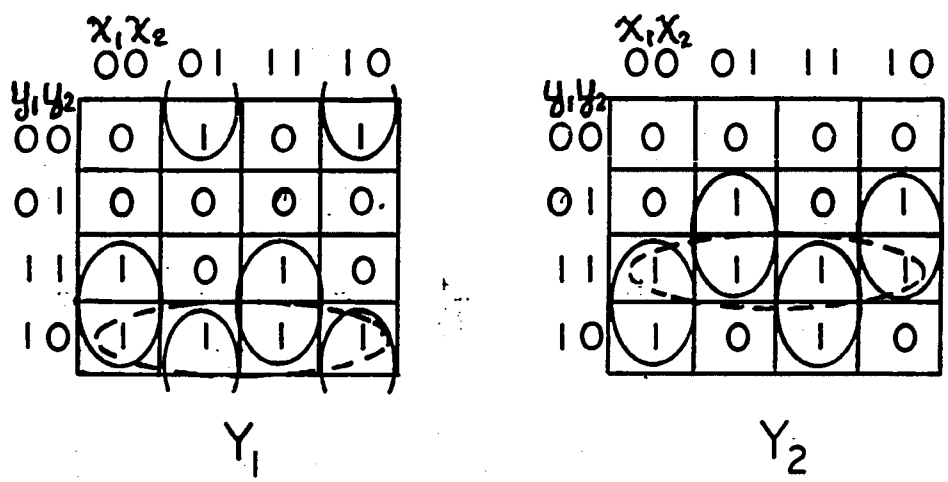


Fig. 5-19. Hazard Subcubes for Hypothetical Problem

The excitation map for the 2-cylinder problem (Fig. 5-6) contains a potential hazard which can be eliminated by the subcube $y\bar{x}_2$ which is shown in Fig. 5-20. Adding the hazard subcube term to Eq. 5-1, gives as the final secondary circuit equation, the following:

$$Y = y\bar{x}_1 + x_1\bar{x}_2 + y\bar{x}_2 \qquad 5\text{-}10$$

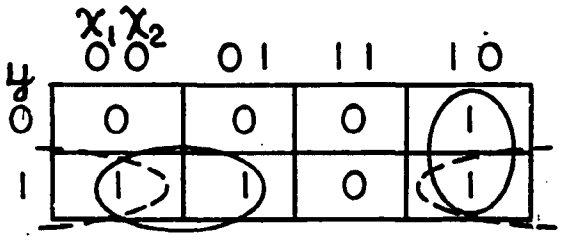


Fig. 5-20. Hazard Subcube for 2-Cylinder Problem

The output maps for the 2-cylinder problem shown in Fig. 5-10 also indicate potential hazards. The hazard for Z_2 can be eliminated by adding the subcube term yx_2 to Eq. 5-5 giving an operational output equation in the form

$$Z_2 = x_1x_2 + y\bar{x}_1 + yx_2 \qquad 5\text{-}11$$

The potential hazard in the Z_1 output map cannot be eliminated by a subcube because of the peculiar alternating characteristic of the map entries. If a hazard actually exists in the Z_1 output circuit, a different flow table merger combination is required and a new set of equations derived. Since the merger selected was the most optimum, a different combination will necessitate the use of a second secondary circuit. Before such "drastic" action is initiated, the circuit operation should be studied to determine whether a change in the variable

is expected during the cycle which would result in a hazard.

Analyzing Eq. 5-4 shows that a hazard would be encountered in the Z_1 output circuit if, during the operational sequence, it is necessary to transfer from a condition $\bar{y}\,\bar{x}_2$ directly to a condition yx_2. Using Table 5-4, an operational table can be written for the two variables in question to determine their logic behavior in the system as shown in Table 5-7. Table 5-7 indicates that the system does not require $\bar{y}\,\bar{x}_2$ to change immediately to yx_2; therefore, no hazard could result in using the circuit. The output equation for Z_1 is acceptable in the form shown in Eq. 5-4 which eliminates the need for redesigning the system.

TABLE 5-7

OPERATIONAL TABLE FOR 2-CYLINDER PROBLEM

Operation	x_2	y
1 s	0	0
2 u	0	0
2 s	0	1
3 s	0	1
4 s	1	1
5 u	1	1
5 s	1	0
6 s	1	0

The methods and procedures discussed in this chapter are complete enough to serve as a basis for the synthesis of both combinational and sequential type fluid circuitry. Although the example illustrations employed to demonstrate the synthesis process were simple, the important aspects of the subject were emphasized. One of the purposes of this chapter was to provide some insight into the orderly method of

synthesizing fluid sequential circuits by logic means. The implementation of this method of fluid switching circuit design into general practice can offer a useful and powerful tool for the fluid power engineer.

CHAPTER VI

FLUID LOGIC INTERPRETATION

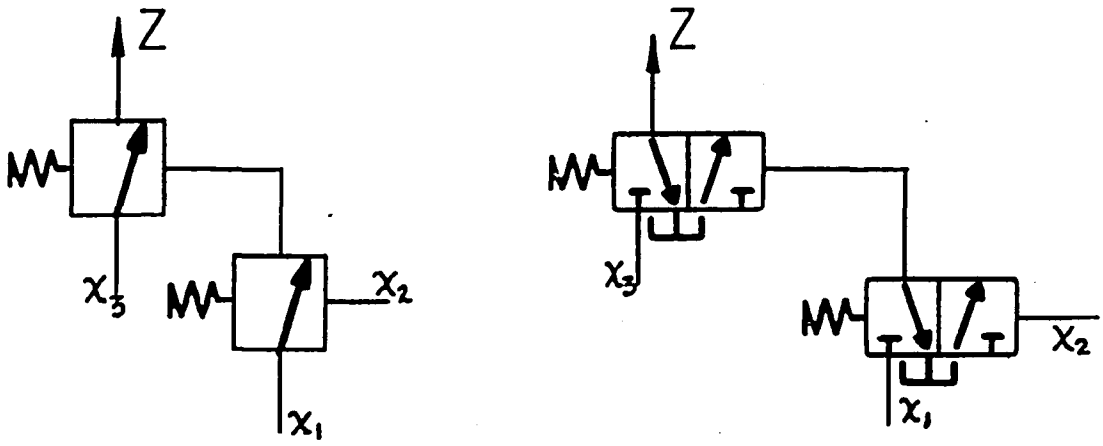
The interpretation of logic expressions in terms of fluid switching hardware presents a complex problem to the engineer. The obscure solution to the problem has undoubtedly contributed to the general acceptance that intuitive methods of circuit synthesis are mandatory. Based on the extensive literature survey conducted as part of this study, no rigorous interpretive method for fluid logic networks exists. The basic characteristics of fluid components and the physical behavior of fluid power systems are sufficiently different from their electrical counterparts that a simple solution to the interpretation problem is impossible. However, a method will be presented in this chapter which yields an orderly approach to the establishment of appropriate hardware for a fluid circuit. A by-product of the method is a composite operational chart that provides a complete insight into the logic implications of the circuit.

In order to appreciate the interpretation problem involved in developing an operational fluid switching network from a Boolean logic equation, an understanding must be gained of the demands imposed by such systems. In electrical contact circuits, an uncomplemented literal means that the contact transmits when energized while a complemented

literal means that the contact transmits until it is energized. This concept, although quite suitable for electrical applications, is not realistic for fluid control systems. In order to apply a binary logic system to fluid networks, the logic element must maintain fluid transmission in both the energized and non-energized states. The above statement means that an uncomplemented literal for a fluid system is transmitting to tank before energization and transmitting pressure afterwards. Likewise, an element represented by a complemented literal is transmitting pressure before actuation and to tank afterwards.

The fluid transmission concept must be adhered to throughout the logic synthesis and interpretive process. The importance of maintaining fluid transmission can be illustrated in Fig. 6-1 (a). The desired output (Z), described by the equation $Z = X_1X_2X_3$, is accomplished for the first actuation of the AND Circuit. However, no provision has been made to tank the fluid in the locked line between the two valves which results in Z being a function of only X_3. The binary valves used in Fig. 6-1 (a) do not satisfy the transmission criteria; because in the complemented condition, transmission is blocked with no tank transmission. The transmission concept for fluid logic circuits requires a configuration such as shown in Fig. 6-1 (b) to accomplish the necessary AND circuit action.

The logic expressed by a given Boolean equation can usually be satisfied by a number of component and circuit configurations. The exact class or type of fluid valve or valves to be used in a given circuit should reflect the general philosophy of the individual designer or company. In this respect, the components discussed and employed in



(a) (b)

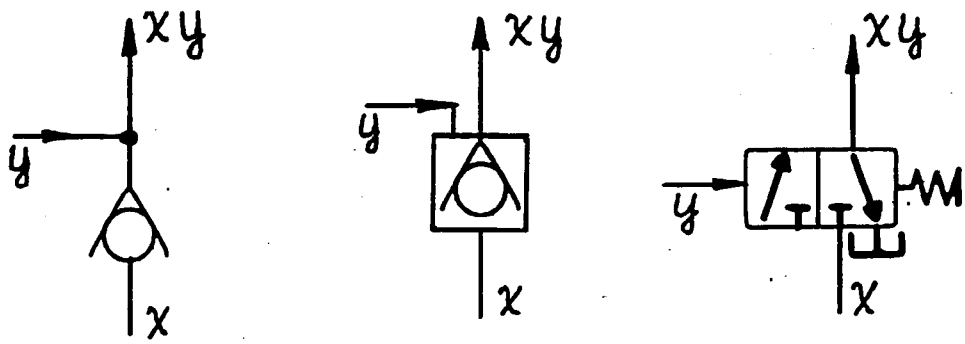
Fig. 6-1. Illustration of Fluid Transmission Concepts

this study have been selected for the purpose of demonstrating principles and not for advocating any particular hardware configurations. In order to use a given type valve in a fluid logic circuit, the logic characteristics of the valve must be recognized in a form compatible with the circuit equation. An appropriate group of valves are presented to demonstrate the interpretive process of circuit synthesis and to exhibit examples of describing characteristics of valves.

Fluid Logic Elements

The AND and OR logic functions are fundamental in circuit equations and need appropriate interpretation in fluid systems. Three types of fluid AND circuits are shown in Fig. 6-2 with different degrees of simplicity. In general, the simplest circuit configuration has the greatest operational limitation and is demonstrated by the circuits in Fig. 6-2. Circuit (a) can only be used as an AND circuit if the tanking

of signal y through x does not occur when signal y is needed elsewhere in the circuit. Similarly, circuit (b) can be used only when the tanking transmission for xy is coordinated with the tanking of x. Circuit (c) requires a higher valued switching element than circuits (a) or (b), but it is a perfect AND logic element. Considering the economic factor, circuit (a) should be used whenever possible while circuit (c) is the last resort. It should be realized that the actual selection of the type AND circuit to be used in the circuit must follow a thorough analysis of the operational characteristics of the system.

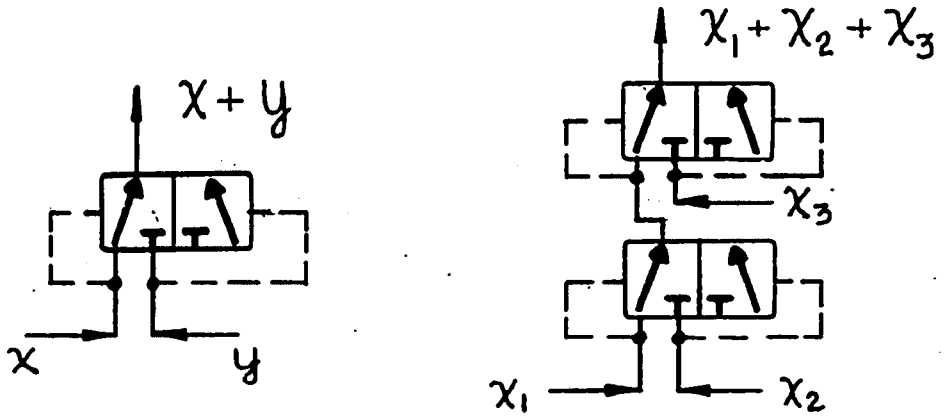


(a) check type (b) pilot check type (c) 3-way type

Fig. 6-2. Fluid AND Circuits

The OR function presents a difficult problem in fluid circuit interpretation. Although under special conditions various valve configurations can be employed to satisfy an OR circuit requirement, simple configurations are not generally feasible. However, a perfect OR function for a fluid circuit exists in the form shown in Fig. 6-3.

A combinational AND-OR circuit worthy of consideration is shown in Fig. 6-4. This circuit places certain restrictions on the system



(a) two-signal type (b) three-signal type

Fig. 6-3. Fluid OR Circuits

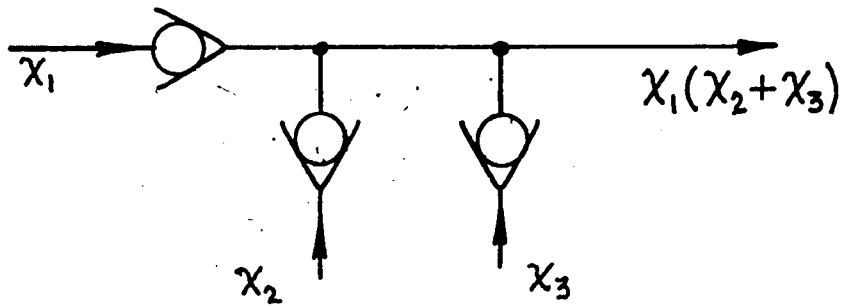


Fig. 6-4. A Combinational AND-OR Circuit

but offers enough simplicity that its possible use should always be investigated.

Fluid Flip Flops

A memory element such as a flip flop gives a circuit the power to remember decisions even though the information on which these were based is no longer available. A flip flop is a device which will assume one of two possible output states when actuated by an appropriate signal. Once the output state is established, the flip flop remains

fixed until a second input is applied to produce the second output state. Numerous valve configurations are possible to accomplish a flip flop action in fluid circuits. Some types are classical examples of perfect flip flop characteristics while others require interpretation.

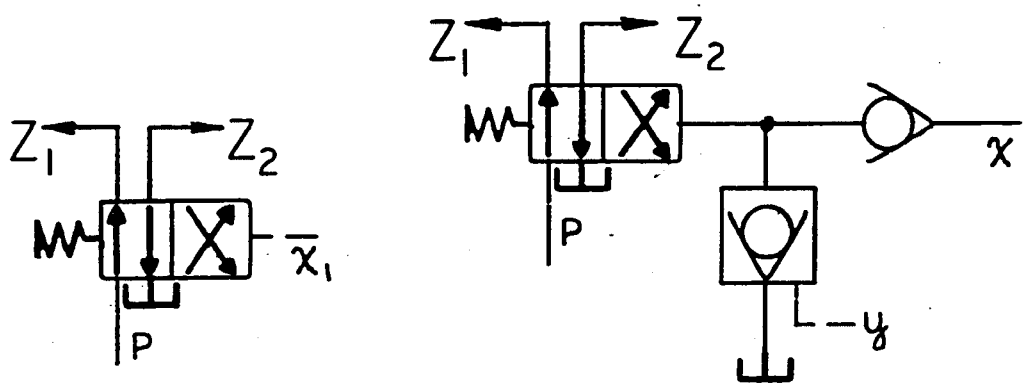
Consider the pilot-operated, spring offset, four-way valve as a flip flop element -- see Fig. 6-5. The output Z_1 in (a) is described by the relation $Z_1 = \bar{x}_1$ while the output Z_2 is $Z_2 = x_1$. Therefore, the classical complementation as presented in Appendix A, of one output gives the second output or $Z_1 = \bar{Z}_2$. Even in the full flip flop form, Fig. 6-5 (b), the classical complement gives the tanking transmission equation as follows:

$$Z_1 = Z_1 \bar{x} + y \qquad 6\text{-}1$$

$$\bar{Z}_1 = (\bar{Z}_1 + x)\bar{y} \qquad 6\text{-}2$$

$$Z_2 = Z_2\bar{y} + x\bar{y} = (Z_2 + x)\bar{y} \qquad 6\text{-}3$$

Letting $\bar{Z}_1 = Z_2$, in Eq. 6-2, gives Eq. 6-3 which demonstrates the classical behavior of this type valve.



(a) valve bnly (b) flip flop

Fig. 6-5. Spring Offset Type Memory Element

Significant deviations from classical valve behavior exist in many forms, and the recognition of these differences is very important in utilizing their characteristics. A simple example of the failure of classical complementation can be demonstrated by referring to the pilot-operated, four-way valve shown in Fig. 6-6. The output equations and their respective complements are

$$Z_1 = x_1\bar{x}_2 \qquad 6\text{-}4$$

$$\bar{Z}_1 = \bar{x}_1 + x_2 \qquad 6\text{-}5$$

$$Z_2 = x_2\bar{x}_1 \qquad 6\text{-}6$$

$$\bar{Z}_2 = \bar{x}_2 + x_1 \qquad 6\text{-}7$$

If the classical complement were valid, then $\bar{Z}_1 = Z_2$ and $\bar{Z}_2 = Z_1$. The significance of this complementing characteristics is that Eq. 6-5 does not describe how the output Z_1 can transmit to tank -- this is described by the Z_2 output equation. Thus, the classical complement of a function is not necessarily the operational or tanking function. An appropriate solution to the problem can be obtained by defining a term called the "fluid complement." The fluid complement of a function is always the tanking function without regard to the classical complement. This concept has implemented the general interpretation technique and has no apparent limitations.

The usefulness of the fluid complement concept can be appreciated when consideration is given to the perfect fluid flip flop -- a pilot-operated, detent held, four-way valve -- illustrated in Fig. 6-7. The

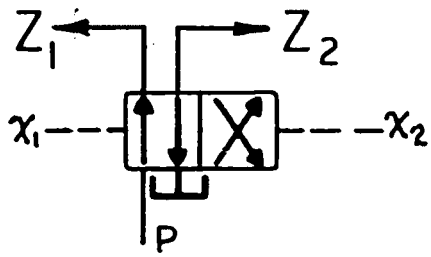


Fig. 6-6. Pilot-Operated Valve

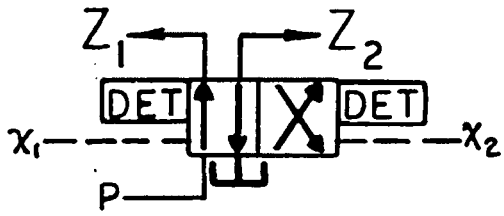


Fig. 6-7. The Perfect Fluid Flip-Flop

output equations are

$$Z_1 = x_1\bar{x}_2 + Z_1\bar{x}_2 \qquad 6\text{-}8$$

$$Z_2 = x_2\bar{x}_1 + Z_2\bar{x}_1 \qquad 6\text{-}9$$

The fluid complement of the output Z_1 is equal to the output equation for Z_2; however, the classical complement of Z_1 is

$$\bar{Z}_1 = (\bar{x}_1 + x_2)(\bar{Z}_1 + x_2)$$

or, by T-11(b) $$\bar{Z}_1 = x_2 + \bar{x}_1\bar{Z}_1 \qquad 6\text{-}10$$

Equation 6-10 represents an incorrect description of the tanking transmission for Z_1. The complementing characteristics of a valve can be checked easily and should be done before it is employed in a circuit.

No detrimental effects have been exhibited by the use of the fluid complement, and its continued use is recommended.

A detent equation, such as Eq. 6-8, can be readily recognized because the value of the equation under certain conditions is dependent upon the most recent value of the equation. In other words, a detent equation is, in part, a function of itself; for example, in Eq. 6-8, the equation value, Z_1, appears as a variable in the equation and modifies an AND term. The AND term such as $\bar{x}_2$ in Eq. 6-8, modified by the equation value is referred to as the detent part of the equation. The interpretation of a detent equation in terms of fluid hardware can be rigorously expressed by applying the unmodified part of the equation to one side of a detent valve and applying the classical complement of the detent part of the equation to the opposite side. This concept can be demonstrated by considering a detent equation having the following form:

$$W_1 = x_1 \bar{x}_2 \bar{w}_2 y_3 + w_1(\bar{x}_2 + \bar{w}_2 + y_2 + y_3) \qquad 6\text{-}11$$

The classical complement of the detent part of Eq. 6-11 is $x_2 w_2 \bar{y}_2 \bar{y}_3$. Using a detent valve, Eq. 6-11 is completely satisfied by the application of signals as shown in Fig. 6-8. Since the detent element displays the flip flop memory characteristic, its appearance is common in secondary circuit equations.

A final illustration shown in Fig. 6-9 will suffice to demonstrate valve interpretation and fluid complementation. The pilot check valve has an output equation of the form

$$Z = x_1 x_2 \qquad 6\text{-}12$$

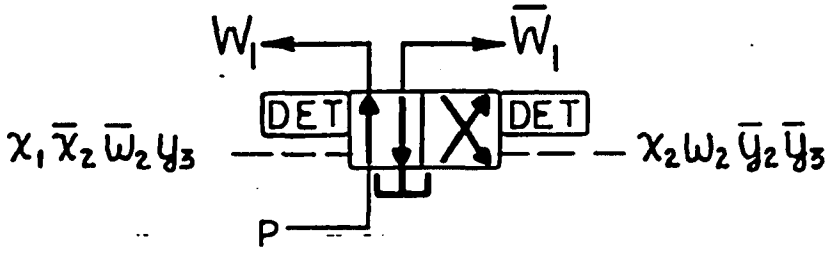


Fig. 6-8. The Detent Equation Interpretation

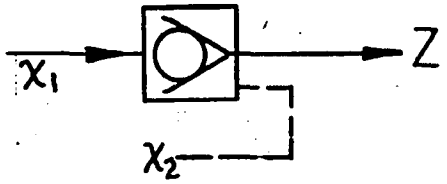


Fig. 6-9. Pilot Check Valve

Classically complementing this equation gives an erroneous tanking transmission function of

$$\bar{Z} = \bar{x}_1 + \bar{x}_2 \qquad 6\text{-}13$$

The fluid complement is the true tanking function and is

$$\bar{Z} = \bar{x}_1 \qquad 6\text{-}14$$

The Composite Operational Chart

The interpretation of the logic specifications described by the synthesis equations in terms of a fluid circuit requires a complete knowledge of the operational behavior of the system. An insight into the sequential characteristics of the circuit can be obtained by listing the order in which each part of the circuit equations contributes toward accomplishing the over-all system logic. Such an orderly record

of the system operation is termed the composite operational chart.

The composite operational chart consists of appropriate columns for the various input, secondary, and output states as well as columns for recording the contributions of the secondary and output equations. The rows of the chart describe the sequential behavior of the network with a row being assigned for each input-secondary-output combination. An example of a composite operational chart is shown in Table 6-1 which represents the operation of the two-cylinder problem developed in Chapter V. This chart was formed from information obtained from Table 5-1, Fig. 5-6, Fig. 5-9, Eq. 5-10, Eq. 5-4, and Eq. 5-11.

TABLE 6-1

COMPOSITE OPERATIONAL CHART FOR 2-CYLINDER PROBLEM

Operation		Inputs	Secondary	Outputs	Equation Contributions		
		x_1x_2	Y	Z_1Z_2	Y	Z_1	Z_2
1	A	0 0	0	1 0		$\bar{y}\,\bar{x}_2$	
2	<u>A</u>	1 0	1	0 0	$x_1\bar{x}_2$	$\bar{Z}_1=y$	
3	B	0 0	1	0 1	$y\bar{x}_1+y\bar{x}_2$		$y\bar{x}_1$
4	A	0 1	1	1 1	$y\bar{x}_1$	yx_2	$y\bar{x}_1+yx_2$
5	<u>A</u>	1 1	0	0 1	$\bar{Y}=x_1$	$\bar{Z}_1=\bar{y}$	x_1x_2
6	<u>B</u>	0 1	0	0 0			$\bar{Z}_2=\bar{x}_1$

The excitation equation for the two-cylinder problem can be written in the form

$$Y = x_1\bar{x}_2 + y(\bar{x}_1 + \bar{x}_2) \qquad 6\text{-}15$$

Performing the classical complement on the detent part of the equation results in a signal application as shown in Fig. 6-10. A second valve is needed to transform the basic input signals into appropriate combinations required in Fig. 6-10. The final secondary circuit is shown in Fig. 6-11.

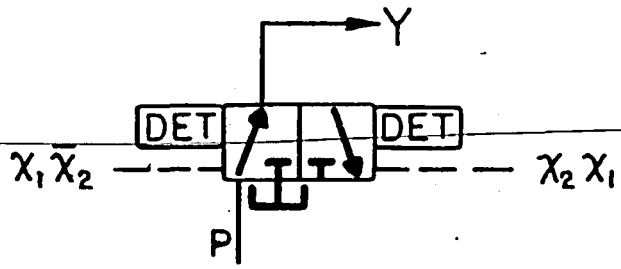


Fig. 6-10. Two-Cylinder Secondary Valve

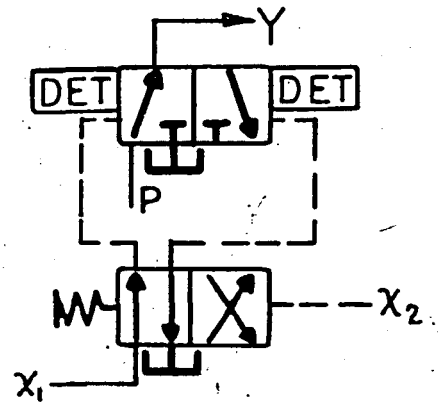


Fig. 6-11. Two-Cylinder Secondary Circuit

The first output equation for the two-cylinder problem is given by the equation

$$Z_1 = \bar{y}\,\bar{x}_2 + yx_2 \qquad 5\text{-}4$$

The output equation describes a circuit in which two signals must be either tanked or energized to give a transmission. One appropriate interpretation of the output equation requires two valves in series as

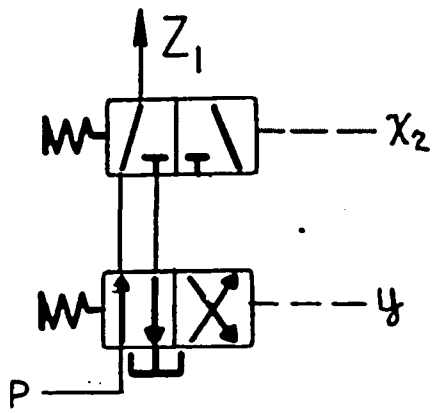


Fig. 6-12. First Output Circuit for 2-Cylinder Problem

shown in Fig. 6-12.

The second output equation for the two-cylinder problem is given by the equation

$$Z_2 = x_1x_2 + y\bar{x}_1 + yx_2 \qquad 5\text{-}11$$

Without employing a composite operational chart, the interpretation of this equation in terms of fluid hardware would be a major problem. A circuit which will always provide the appropriate pressure and tanking transmission can be developed with the aid of Table 6-1. Using pure binary valves, the pressure transmission can be accomplished by the circuit shown in Fig. 6-13 less the check valve. By referring to the composite operational chart, the tanking of Z_2 must not be initiated until the x_1 signal is de-energized; therefore, the tanking of Z_2 through x_2 must be prevented by the use of a check valve as indicated in Fig. 6-13.

Two valves in a circuit having the same output and input signals can usually be combined. This is the case of the x_1 valves in Fig. 6-13. The final circuit describing the second output equation for the

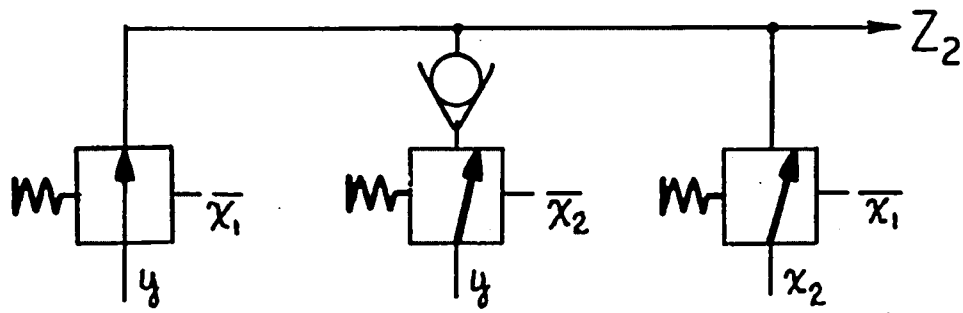


Fig. 6-13. Second Output Circuit (Binary) for 2-Cylinder Problem

two-cylinder problem is shown in Fig. 6-14.

The control network for the two-cylinder problem can now be synthesized by combining Figs. 6-11, 6-12, and 6-14. The final network shown in Fig. 6-15 will accept the signals generated in the power circuit of Fig. 5-3 and produce output signals to control the sequential order for the two cylinders as originally specified. The signals $\bar{x}_1$ and $\bar{x}_2$ shown in Fig. 5-3 were not needed in the final control network to simplify the circuit; therefore, these valve ports could be plugged or a three-way valve substituted.

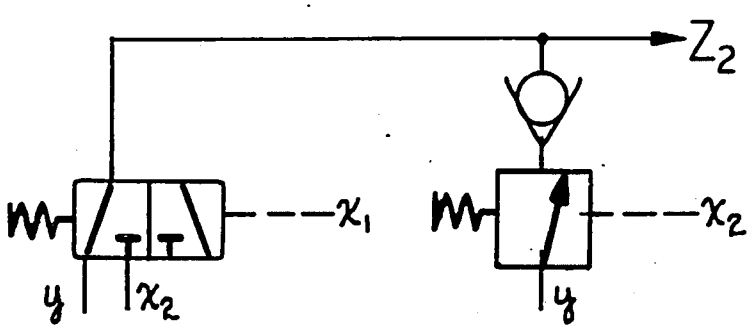


Fig. 6-14. Second Output Circuit for 2-Cylinder Problem

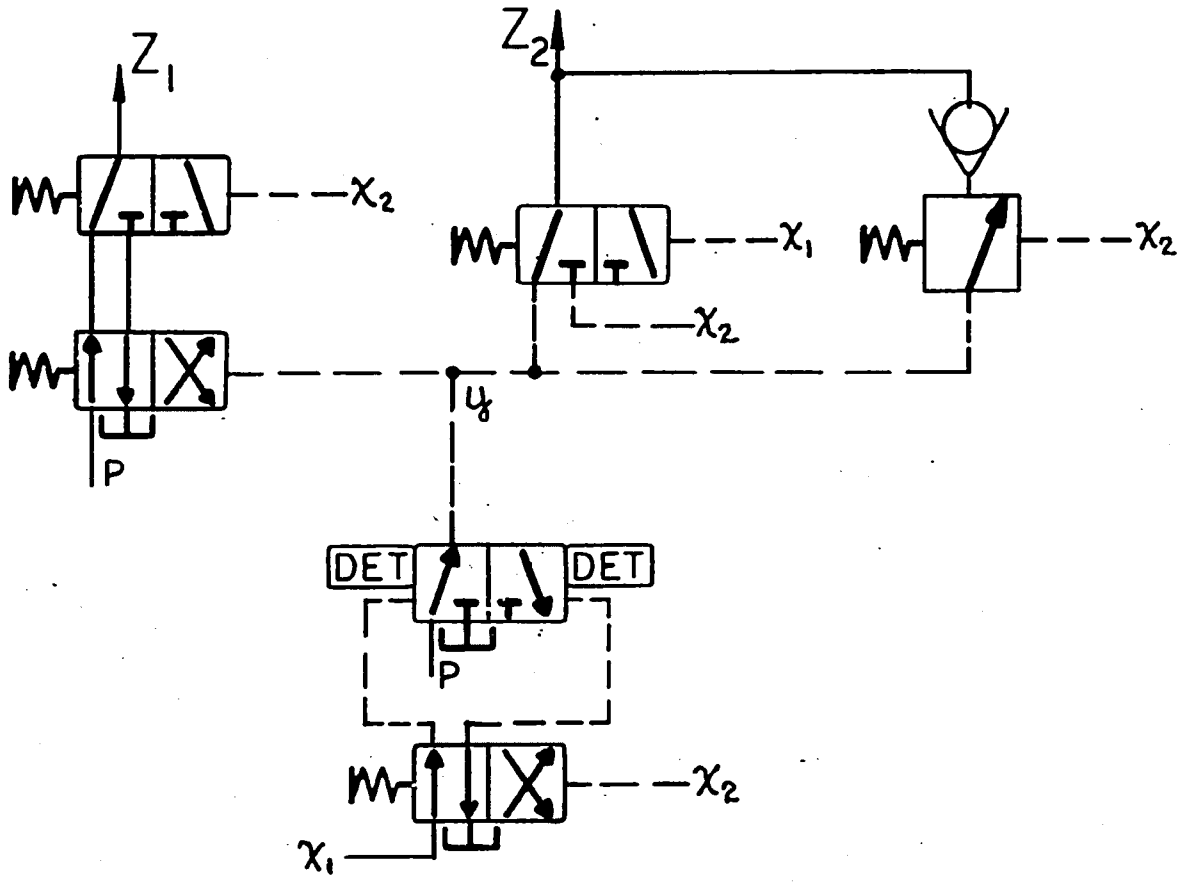


Fig. 6-15. Fluid Control Network for 2-Cylinder Problem

The interpretation of logic expressions in terms of fluid components presents a different situation for each problem considered. Recognizing the logic characteristics of valves permits their utilization in fluid networks. The reduction of circuit configurations can be implemented by the use of the composite operational chart. The chart exhibits the sequential order of signal states and displays the contributions of the circuit equations in achieving the specified logic. In synthesis problems involving complex equations, the operational chart is almost a necessity.

CHAPTER VII

FLUID NETWORK ANALYSIS

The analysis of fluid switching networks is the process of determining the operational logic of a system by deriving the characteristic algebraic equations of the circuit. In analysis, an existing circuit is available, and the transmission functions are unknown. The purpose of a network analysis is to discover the logic implications and the inherent limitations of the system. Such information is needed for the appropriate selection of circuit components, trouble-shooting, and circuit modifications (network reduction and changing or enlarging the control capability).

Control networks which have been intuitively designed are entirely satisfactory if they operate and require no changes; however, such ideal situations are the exception rather than the rule. Since the logic synthesis of fluid circuits has not been introduced and practiced, a need will be recognized for obtaining the algebraic expressions of existing circuits. It is the objective of this chapter to demonstrate a means by which such circuits can be analyzed and the appropriate synthesis maps obtained. In order to accomplish this goal, an example problem will be studied and discussed.

Selection of a Network

Considerable attention has been given to the selection of a suitable network that would exemplify a complex system of sufficient rigor to indicate whether the analysis method would hold for any conceivable application. It is difficult to single out a given circuit for reference because such a selection would be arbitrary and subject to the influence of personal opinion. The need for demonstrating the analysis technique for fluid networks, however, made such a choice necessary. The circuit to be considered in this chapter was intuitively designed and experimentally tested to secure a known operational circuit configuration possessing a typical random logic characteristic. A conscientious effort was made to achieve maximum network simplification for the eventual comparison of intuitive versus logic design methods.

The final circuit configuration as experimentally tested is shown in Fig. 7-1. It consists of two cylinders controlled by three-position, spring centered, power control valves. The cylinders, by means of appropriately designed cams, actuated signal valves which emitted position information type fluid signals to a control network. The control network utilized these signals to control the sequential behavior of the cylinders. The operational characteristics of the cylinders can be described by the shorthand sequential cylinder notation discussed in Chapter V as A, B, $\underline{B}$, $\underline{A}$, B, A, $\underline{A}$, $\underline{B}$. This sequential pattern established the need for memory elements because operation B does not always follow operation A and $\underline{A}$ does not always follow $\underline{B}$, etc.

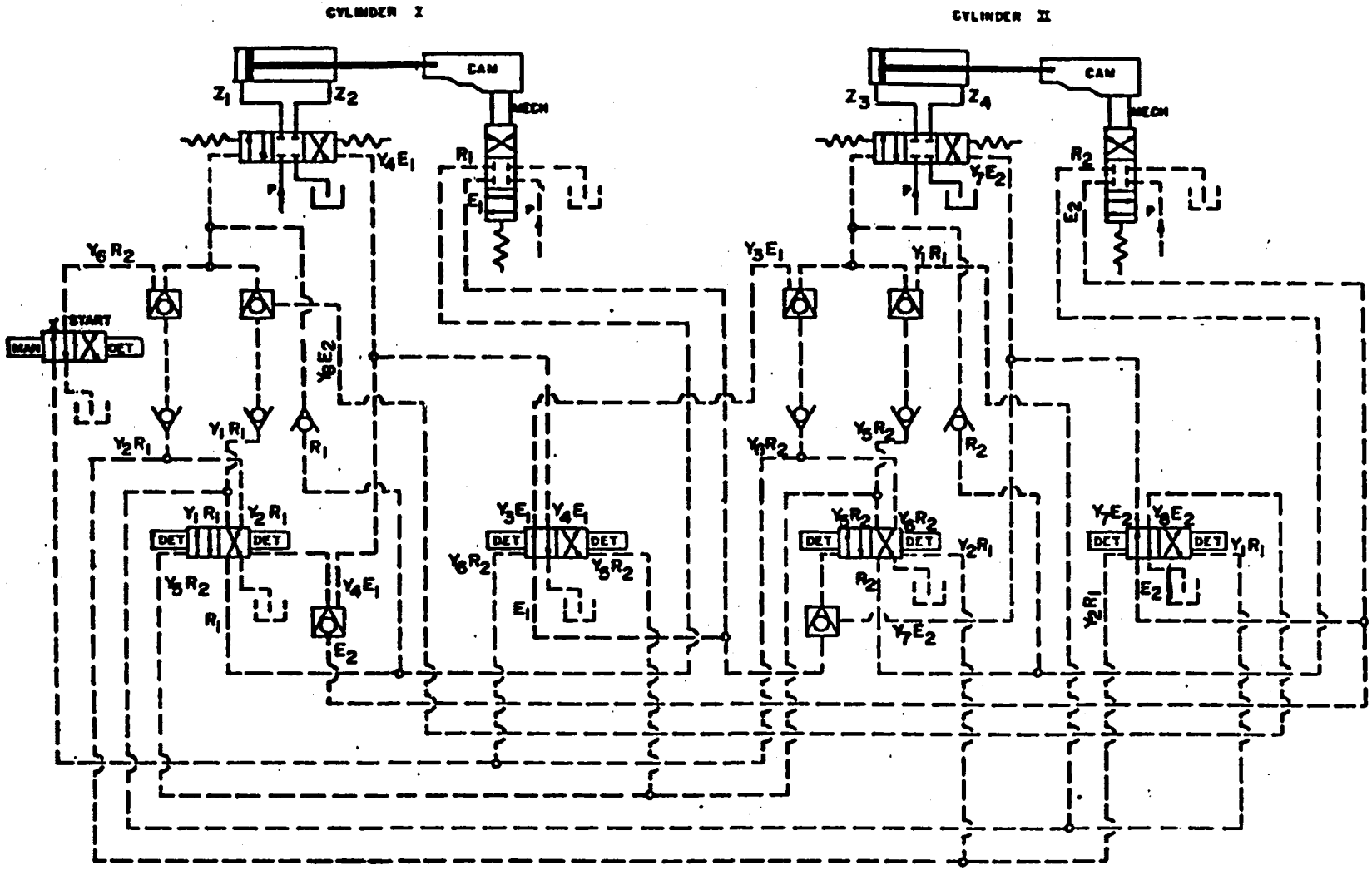


Fig. 7-1. Intuitively Designed Circuit Giving -- A, B, $\underline{B}$, $\underline{A}$, B, A, $\underline{A}$, $\underline{B}$.

General Circuit Equations

The logical analysis of an existing fluid network is initiated by labeling the signals emitted by each control valve. The origin of all signals actuating the control valves must be determined and appropriately identified at each valve. The technique of labeling and identifying fluid signals is exhibited on the intuitive circuit diagram in Fig. 7-1. The signals E_1 and E_2 refer to the extension signals for cylinders 1 and 2, respectively; likewise, signals R_1 and R_2 are concerned with the associated retraction signals. The Y signals are assigned to all valves which could be considered as secondary circuit elements. The output signals to the cylinders are labeled using the conventional Z designations.

After all lines are labeled and identified, general logic expressions are written to describe the conditions under which each valve output will be obtained. Such equations can be derived by circuit inspection if the operational characteristics of the valves are known. Sufficient background was presented in Chapter VI to write these equations. The general logic expressions for the intuitive circuit are as follows:

$$Z_1 = R_1(\bar{y}_4 + \bar{E}_1)(y_6R_2y_2R_1 + y_1R_1y_8E_2) \qquad 7\text{-}1$$

$$Z_2 = y_4E_1\bar{R}_1(\bar{y}_6 + \bar{R}_2 + \bar{y}_2 + \bar{R}_1)(\bar{y}_8 + \bar{E}_2 + \bar{y}_1 + \bar{R}_1) \qquad 7\text{-}2$$

$$Z_3 = R_2(\bar{y}_7 + \bar{E}_2)(y_3E_1y_6R_2 + y_1R_1y_5R_2) \qquad 7\text{-}3$$

$$Z_4 = y_7E_2\bar{R}_2(\bar{y}_3 + \bar{E}_1 + \bar{y}_6 + \bar{R}_2)(\bar{y}_1 + \bar{R}_1 + \bar{y}_5 + \bar{R}_2) \qquad 7\text{-}4$$

$$Y_1 = y_5 R_2 \bar{E}_2 + y_1 \bar{E}_2 \quad , \qquad 7\text{-}5$$

$$Y_2 = y_4 E_1 E_2 (\bar{y}_5 + \bar{R}_2) + y_2 (\bar{y}_5 + \bar{R}_2) \qquad 7\text{-}6$$

$$Y_3 = y_6 R_2 (\bar{y}_5 + \bar{R}_2) + y_3 (\bar{y}_5 + \bar{R}_2) \qquad 7\text{-}7$$

$$Y_4 = y_5 R_2 (\bar{y}_6 + \bar{R}_2) + y_4 (\bar{y}_6 + \bar{R}_2) \qquad 7\text{-}8$$

$$Y_5 = y_7 E_2 E_1 (\bar{y}_2 + \bar{R}_1) + y_5 (\bar{y}_2 + \bar{R}_1) \qquad 7\text{-}9$$

$$Y_6 = y_2 R_1 \bar{E}_1 + y_6 \bar{E}_1 \qquad 7\text{-}10$$

$$Y_7 = y_2 R_1 (\bar{R}_1 + \bar{y}_1) + y_7 (\bar{R}_1 + \bar{y}_1) \qquad 7\text{-}11$$

$$Y_8 = y_1 R_1 (\bar{y}_2 + \bar{R}_1) + y_8 (\bar{y}_2 + \bar{R}_1) \qquad 7\text{-}12$$

Having obtained the general logic expressions for the circuit, every means should be employed to reduce the number of variables and literals in the equations. An obvious way of achieving this goal is through the complementary characteristics of the flip flops or four-way valves. In other words, if a component possesses a dual transmission characteristic whereby one output is pressurized while the other is tanked, a literal and its complement can represent the associated outputs. For the circuit in Fig. 7-1, the following complementary relations are established:

$$w_1 = E_1 \bar{R}_1 \quad \text{and} \quad \bar{w}_1 = \bar{E}_1 R_1$$

$$w_2 = E_2 \bar{R}_2 \quad \text{and} \quad \bar{w}_2 = \bar{E}_2 R_2$$

$$y_2 = \bar{y}_1 \quad \text{and} \quad \bar{y}_2 = y_1$$

$$y_3 = \bar{y}_4 \quad \text{and} \quad \bar{y}_3 = y_4$$

$$y_5 = \bar{y}_6 \quad \text{and} \quad \bar{y}_5 = y_6$$

$$y_7 = \bar{y}_8 \quad \text{and} \quad \bar{y}_7 = y_8$$

The complementary relations are substituted in the general circuit equations to reduce the number of variables and permit the general simplification of the equations. The simplification process and the resulting logic relations for the secondary and output circuits of the example problem are as follows:

$$Z_1 = \bar{w}_1(y_3 + \bar{w}_1)(\bar{y}_5\bar{w}_2y_2\bar{w}_1 + \bar{y}_2\bar{w}_1\bar{y}_7w_2)$$

$$Z_1 = (\bar{w}_1y_3 + \bar{w}_1)(\bar{y}_5\bar{w}_2y_2 + \bar{y}_2\bar{y}_7w_2)$$

$$Z_1 = \bar{w}_1(\bar{y}_5\bar{w}_2y_2 + \bar{y}_2\bar{y}_7w_2)$$

$$Z_1 = y_2\bar{y}_5\bar{w}_1\bar{w}_2 + \bar{y}_2\bar{y}_7\bar{w}_1w_2 \qquad 7\text{-}13$$

$$Z_2 = \bar{y}_3w_1w_1(\bar{y}_5 + w_2 + \bar{y}_2 + w_1)(y_7 + \bar{w}_2 + y_2 + w_1)$$

since the term $\bar{y}_3w_1$ satisfies the equation,

$$Z_2 = \bar{y}_3w_1 \qquad 7\text{-}14$$

$$Z_3 = \bar{w}_2(\bar{y}_7 + \bar{w}_2)(y_3w_1\bar{y}_5\bar{w}_2 + \bar{y}_2\bar{w}_1y_5\bar{w}_2)$$

$$Z_3 = (\bar{w}_2\bar{y}_7 + \bar{w}_2)(y_3w_1\bar{y}_5 + \bar{y}_2\bar{w}_1y_5)$$

$$Z_3 = \bar{w}_2(y_3w_1\bar{y}_5 + \bar{y}_2\bar{w}_1y_5)$$

$$Z_3 = y_3\bar{y}_5w_1\bar{w}_2 + \bar{y}_2y_5\bar{w}_1\bar{w}_2 \qquad 7\text{-}15$$

$$Z_4 = y_7w_2w_2(\bar{y}_3 + \bar{w}_1 + y_5 + w_2)(y_2 + \bar{w}_1 + \bar{y}_5 + w_2)$$

since the term y_7w_2 satisfies the equation,

$$Z_4 = y_7w_2 \qquad 7\text{-}16$$

$$Y_2 = \bar{y}_3 w_1 w_2(\bar{y}_5 + w_2) + y_2(\bar{y}_5 + w_2)$$

$$Y_2 = \bar{y}_3 w_1 w_2 \bar{y}_5 + \bar{y}_3 w_1 w_2 + y_2(\bar{y}_5 + w_2)$$

$$Y_2 = \bar{y}_3 w_1 w_2 + y_2(\bar{y}_5 + w_2) \qquad 7\text{-}17$$

$$Y_3 = \bar{y}_5 \bar{w}_2(\bar{y}_5 + w_2) + y_3(\bar{y}_5 + w_2)$$

$$Y_3 = \bar{y}_5 \bar{w}_2 + y_3(\bar{y}_5 + w_2)$$

$$Y_3 = \bar{y}_5 \bar{w}_2 + y_3 w_2 + y_3 \bar{y}_5 \qquad 7\text{-}18$$

$$Y_5 = y_7 w_2 w_1(\bar{y}_2 + w_1) + y_5(\bar{y}_2 + w_1)$$

$$Y_5 = y_7 \bar{y}_2 w_2 w_1 + y_7 w_2 w_1 + y_5(\bar{y}_2 + w_1)$$

$$Y_5 = y_7 w_2 w_1 + y_5 \bar{y}_2 + y_5 w_1 \qquad 7\text{-}19$$

$$Y_7 = y_2 \bar{w}_1(w_1 + y_2) + y_7(w_1 + y_2)$$

$$Y_7 = y_2 \bar{w}_1 + y_7(w_1 + y_2)$$

$$Y_7 = y_2 \bar{w}_1 + y_7 w_1 + y_2 y_7 \qquad 7\text{-}20$$

Analysis Diagrams

The general specifications of the circuit are sufficient to establish the primitive flow table for the system. The logic implied by this flow table must be satisfied regardless of the method used to synthesize the circuit. The primitive flow table for the intuitive circuit is shown in Table 7-1.

TABLE 7-1

PRIMITIVE FLOW TABLE FOR INTUITIVELY DESIGNED CIRCUIT

Operation		$w_1 w_2$ 00	01	11	10	$Z_1 Z_2 Z_3 Z_4$
1	A	①			2	1 0 0 0
2	B			3	②	0 0 1 0
3	B			③	4	0 0 0 1
4	A	5			④	0 1 0 0
5	B	⑤	6			0 0 1 0
6	A		⑥	7		1 0 0 0
7	A		8	⑦		0 1 0 0
8	B	1	⑧			0 0 0 1

The secondary state values needed in conjunction with the indicated input states to produce the desired output states shown on the primitive flow table must be evaluated. The secondary states corresponding to the stable states are determined with the aid of the general output equations already derived. The actual procedure can be demonstrated by considering a given output requirement exhibited on the primitive flow table and examine the appropriate output equations to establish the necessary secondary values. By referring to the primitive flow table (Table 7-1), operation 1 (extension stroke of A) requires that $Z_1 = 1$; therefore, it can be seen from the Z_1 equation (Eq. 7-13) that since $w_1 = 0$ and $w_2 = 0$ then $y_2 = 1$ and $y_6 = 0$ before $Z_1 = 1$. Similarly, for operation 2 (extension of B) to occur, $Z_3 = 1$ and Eq.

7-15 must be satisfied; therefore, since $w_1 = 1$ and $w_2 = 0$, then $y_3 = 1$ and $y_5 = 0$. This evaluation process can be repeated until the conditions for each operation have been determined. The results of this process are recorded on an intermediate sequence table as illustrated in Table 7-2.

TABLE 7-2

INTERMEDIATE SEQUENCE TABLE FOR INTUITIVE CIRCUIT

Operation		Inputs		Secondary				Outputs			
		w_1	w_2	Y_2	Y_3	Y_5	Y_7	Z_1	Z_2	Z_3	Z_4
1	A	0	0	1		0		1	0	0	0
2	B	1	0		1	0		0	0	1	0
3	B	1	1				1	0	0	0	1
4	A	1	0		0			0	1	0	0
5	B	0	0	0		1		0	0	1	0
6	A	0	1	0			0	1	0	0	0
7	A	1	1		0			0	1	0	0
8	B	0	1				1	0	0	0	1

The binary values of the secondary states that are missing in the intermediate sequence table are determined by evaluating each secondary circuit equation. For example, it can be confirmed by Eq. 7-17 that $Y_2 = 1$ in operation 2 because y_2 was transmitting in the previous operation and $Y_5 = 0$. Similarly, in operation 3, $Y_2 = 1$ because $w_2 = 1$ and y_2 was transmitting in the previous operation. However, in

operation 4, the value of y_5 must be determined before a decision can be made concerning the value of y_2 because only $y_5 = 0$ can continue the y_2 transmission with the existing input states. The determination of the missing secondary state values by evaluating the general circuit equations is a critical phase of the circuit analysis and can be deduced by the application of the above procedure. After the values have been determined, they are entered in their corresponding locations in the intermediate sequence table to form the final sequence table for the circuit. The final sequence table for the intuitive circuit is shown in Table 7-3.

TABLE 7-3

FINAL SEQUENCE TABLE FOR INTUITIVE CIRCUIT

Operation		Inputs		Secondary				Outputs			
		w_1	w_2	Y_2	Y_3	Y_5	Y_7	Z_1	Z_2	Z_3	Z_4
1	A	0	0	1	1	0	1	1	0	0	0
2	B	1	0	1	1	0	1	0	0	1	0
3	B	1	1	1	1	1	1	0	0	0	1
4	A	1	0	0	0	1	1	0	1	0	0
5	B	0	0	0	0	1	0	0	0	1	0
6	A	0	1	0	0	1	0	1	0	0	0
7	A	1	1	1	0	1	0	0	1	0	0
8	B	0	1	1	0	0	1	0	0	0	1

Based on the input and secondary state information contained in

the final sequence table, an excitation map for the circuit can be drawn. The excitation map for the intuitively designed circuit must be a six variable type because of the four secondary and two input variables. The composite excitation map is illustrated in Fig. 7-2. The stable and unstable operational numbers are entered with their corresponding excitation entry to provide continuity.

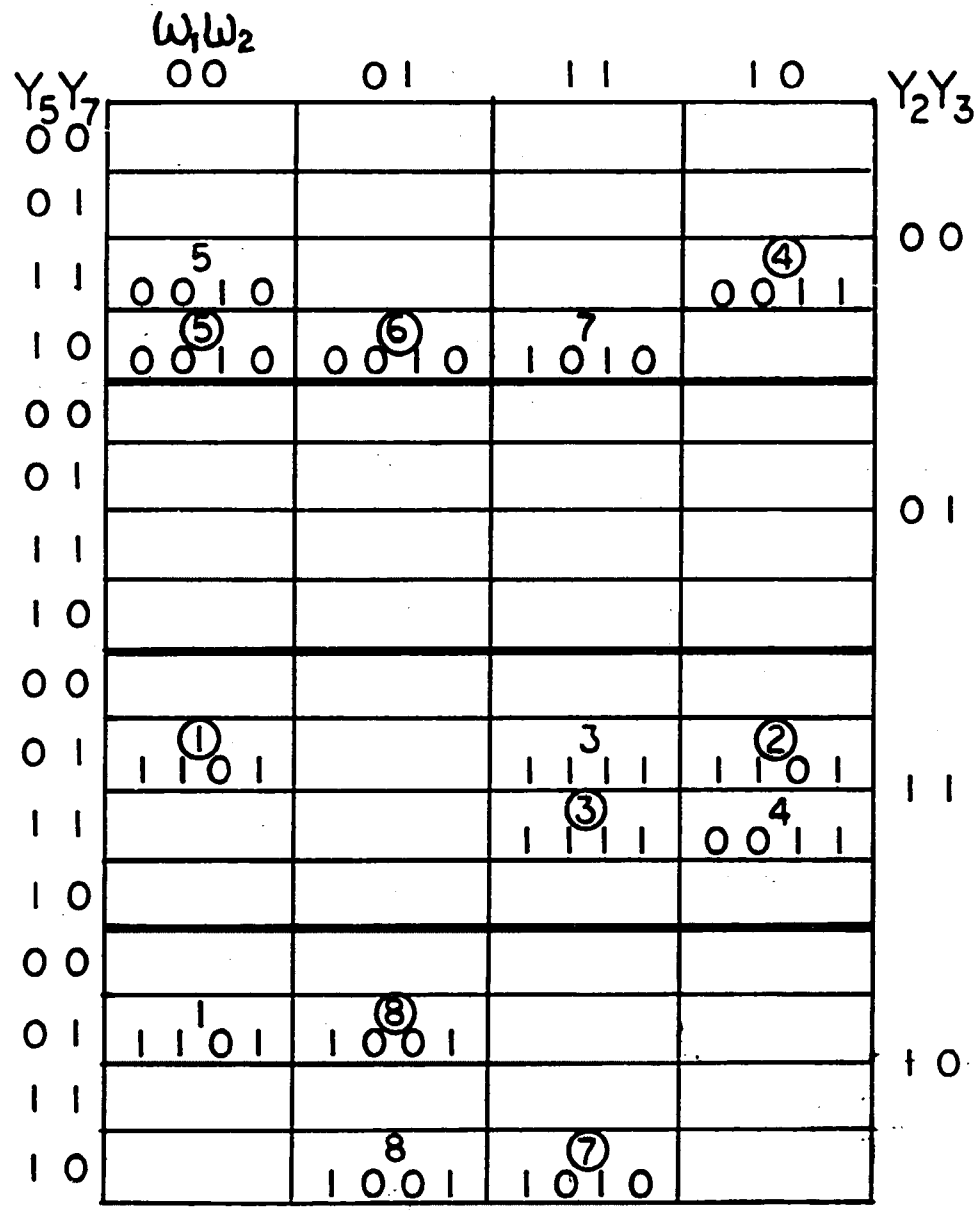


Fig. 7-2. Excitation Map for Intuitively Designed Circuit.

Possessing the excitation map for the intuitively designed circuit permits the simplest secondary circuit expressions to be determined. It should be emphasized that any simplification of equations obtained from the excitation map, which is derived from the analysis method being discussed, is completely dependent upon the existing operational pattern displayed on the map. In the logic synthesis method, the map pattern is optimized by the merging technique described in Chapter V. The simplest map equations for the secondary circuits can be written using the Karnaugh technique described in Appendix B. For the excitation map shown in Fig. 7-2, the simplest expressions are identical to the secondary equations already derived except for Y_2. The map indicates that the simplest Y_2 equation is

$$Y_2 = \bar{y}_5 + w_1 w_2 + y_2 w_2 \qquad 7\text{-}21$$

and not the expression given by Eq. 7-17. However, the simplest equation does not always yield the simplest circuit. In the case of Eq. 7-21, a four-way, pilot-operated, detent valve is still required as shown in Fig. 7-3.

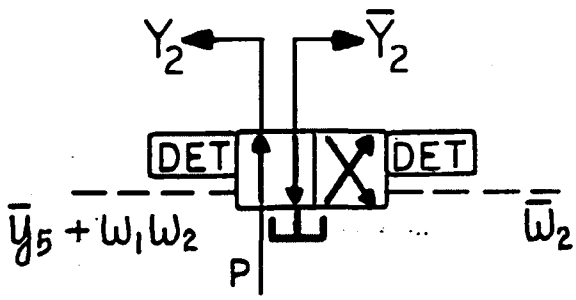


Fig. 7-3. Circuit Required to Satisfy Eq. 7-21.

It can be shown that the circuit configurations required to produce

the signal $\bar{y}_6 + w_1w_2$ in Fig. 7-3 is comparable to that originally employed to give the signals $y_6\bar{w}_2$ and $w_2\bar{y}_3$; therefore, the secondary circuit analysis did not reveal any profitable modifications in the secondary circuit. A better understanding of the operation of the circuit is provided, however, because of the insight given by the excitation map. For example, the term $y_3\bar{y}_6$ in the Y_3 equation (Eq. 7-18) and the term y_2y_7 in the Y_7 relation (Eq. 7-20) are hazard eliminating factors. The need for these factors was intuitively recognized without realizing their actual logic significance. In the event the circuit had not performed experimentally, this analysis would have provided the answer for hazard elimination and also a thorough evaluation whether the desired logic specifications were satisfied.

The final step in the analysis is to develop the output map for the system. Such a map can be formed from the information contained in the final sequence table. Again the stable and unstable operational numbers are entered in the map with their corresponding output state values. The output state values associated with a given stable state are fixed; however, the values corresponding to the unstable states usually contain optional terms. For example, referring to the primitive flow table (Table 7-1) consider the operation involved in shifting to stable state 3 from stable state 2. The values of Z_1 and Z_2 remain fixed while the values of Z_3 and Z_4 are changed; therefore, the actual values of Z_3 and Z_4 are arbitrary at unstable state 3. The arbitrary or optional values are marked on the output map in order to permit simplification of the output equations. The composite output map for the intuitively designed circuit is shown in Fig. 7-4.

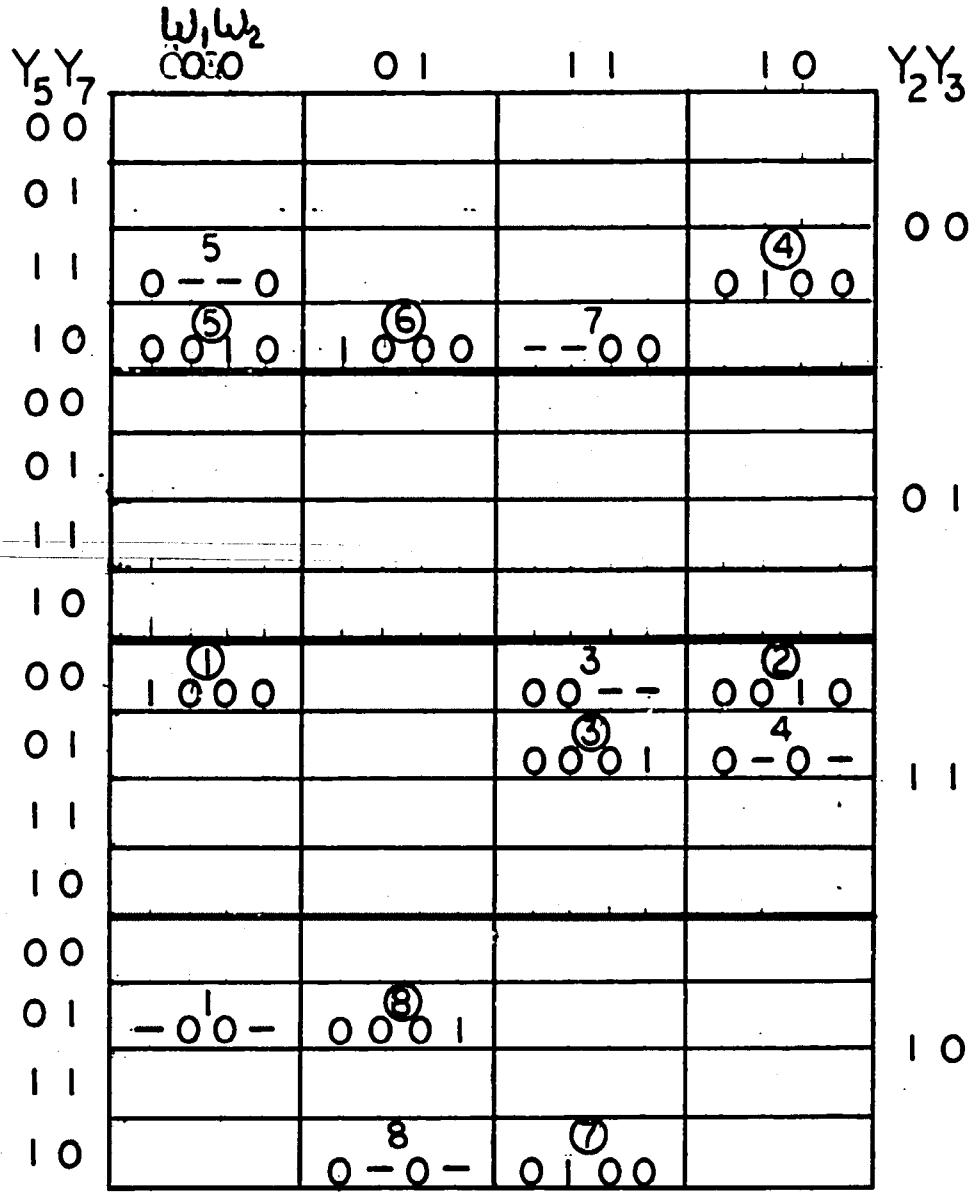


Fig. 7-4. Composite Output Map for Intuitively Designed Circuit

An examination of the output map (Fig. 7-4) for the intuitively designed circuit indicates that no hazards are involved in the output circuit equations. The equations for Z_2 and Z_4 are optimum for the output map configuration. According to the output map, the simplest

Z_1 equation is

$$Z_1 = w_2\bar{y}_2 + \bar{w}_1 y_3 \qquad 7\text{-}22$$

This equation contains half the number of literals involved in the original equation (Eq. 7-13) and represents a significant reduction. However, an inspection of the signals generated by the existing secondary circuit reveals that a major change of the entire circuit would be required to implement Eq. 7-22 with some reservations as to the over-all economy. The simplest Z_3 equation which can be deduced from the output map is

$$Z_3 = w_1\bar{y}_6 + \bar{w}_1\bar{w}_2\bar{y}_2 + \bar{w}_2\bar{y}_7 \qquad 7\text{-}23$$

This equation contains only one less literal than the original Z_3 equation (Eq. 7-15) and adds an extra OR term ($\bar{w}_2\bar{y}_7$) to eliminate a potential hazard. No apparent advantage is gained by using this equation in preference to the original circuit equation.

The analysis of the intuitively designed circuit has shown that the circuit is free of hazards and would be an operational configuration. The experimental verification of this circuit revealed that the circuit would operate over the full capacity range of the fluid power stand (variable up to a maximum pressure and flow rate of 1500 psi and 20 gpm, respectively). Every effort was made during the experimental testing to confuse the incorporated logic of the system by stopping and starting the circuit at various points in its cycle, but the circuit would always continue the proper action even when left idle for long periods of time. The physical arrangement of the circuit components is shown in Fig. 7-5.

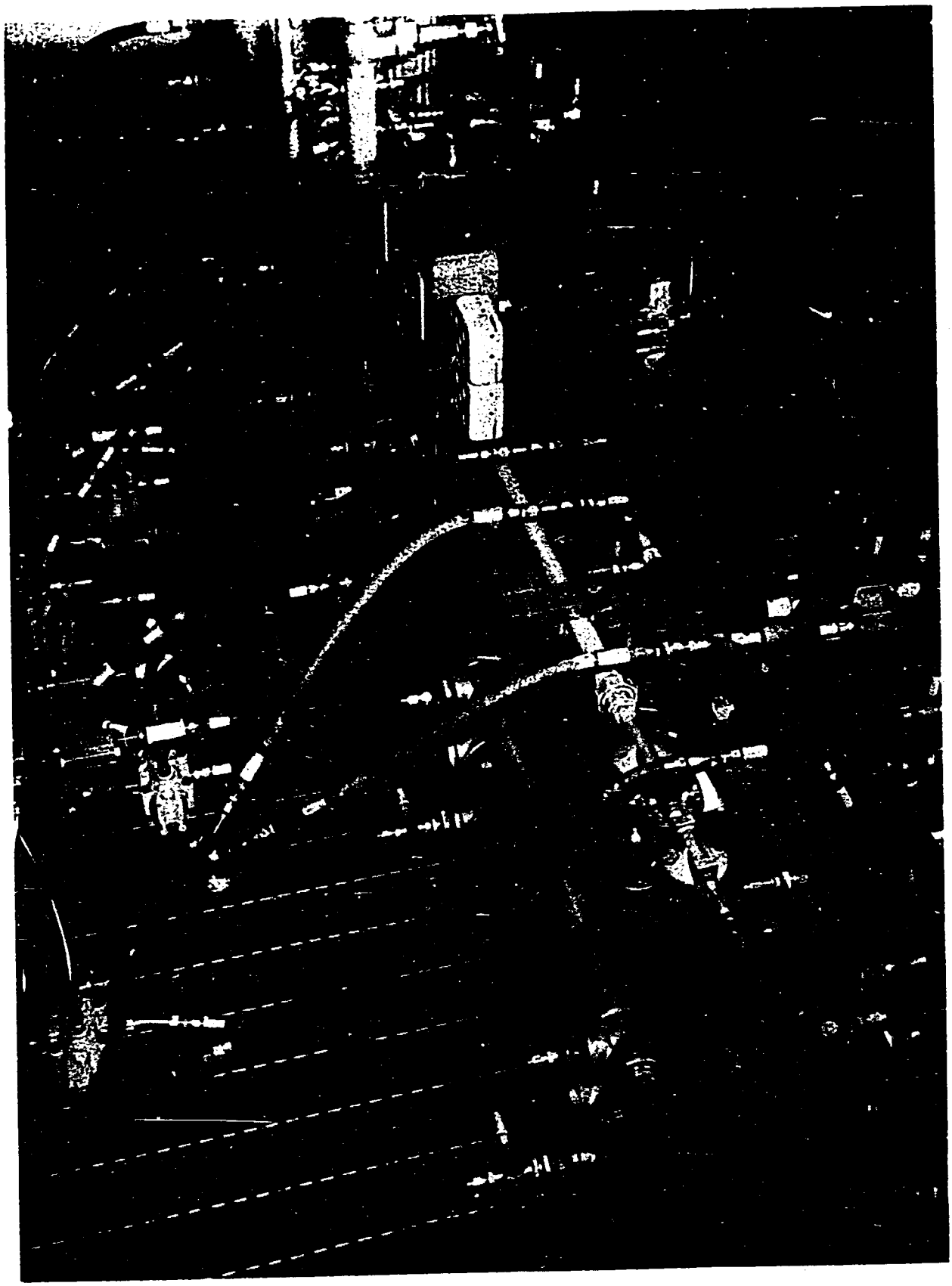


Fig. 7-5. Physical Arrangement of Intuitively Designed Circuit.

CHAPTER VIII

VERIFICATION OF SYNTHESIS METHOD

The logic synthesis method for fluid control networks presented in this thesis offers a means of extending the normal reasoning power of an engineer. It enables the designer to pursue a synthesis problem in a logical and orderly manner with a minimum amount of dependence on creativity. These claims are open for criticism unless a rigorous demonstration can be evidenced of the power and practicality of this method. It is the purpose of this chapter to justify these claims and permit the general appraisal of the method.

Engineers who have designed complicated fluid systems can appreciate the problems involved in the synthesis of sequential type circuits. The design of these circuits poses a tremendous challenge that is not always accepted by fluid power engineers. It is therefore important that the demonstration of the synthesis method presented herein be of a sequential logic type. Since the logic implications of the intuitively designed circuit presented in Chapter VII satisfies all major requirements of a complex sequential circuit, this two-cylinder system will be synthesized and studied.

An additional benefit can be realized by employing the logic specifications of the intuitively designed circuit in a synthesis study

because a comparison can be drawn of the final network configurations. It was mentioned in Chapter VII that considerable attention was given to the simplification of the circuit for the purpose of obtaining the most optimum circuit which could be intuitively designed. A direct comparison between the intuitively designed circuit and the logically designed circuit should reveal some measure of the degree of optimization achieved.

Circuit Synthesis Initiation

The specifications for the sequential circuit to be synthesized are established by the primitive flow table in Table 7-1. Using the synthesis technique presented in Chapter V, the circuit equations for the operational network will be derived. No redundant states are evident in the flow table because two stable states having the same output conditions do not exist in the same column. Based on the rules for merging two rows of a flow table, a table of possible mergers can be completed as shown in Table 8-1.

A merger diagram can be drawn based on the table of possible mergers and the procedure given in Chapter V. This diagram which displays graphically the merging characteristics of the rows of the primitive flow table permits a visual recognition of the appropriate row combinations. The merger diagram for the sequential problem is an array of eight numbers and is illustrated in Fig. 8-1.

A merger combination must comprise numbers in the merger diagram which are linked with each and every other number in the combination. The diagram shown in Fig. 8-1, displays a pattern that requires a

TABLE 8-1

TABLE OF POSSIBLE MERGERS FOR SEQUENTIAL PROBLEM

ROW	WITH	ROW
1		2
1		6
1		7
1		8
2		5
2		8
3		4
3		5
3		8
4		5
4		6
4		7
5		6
7		8

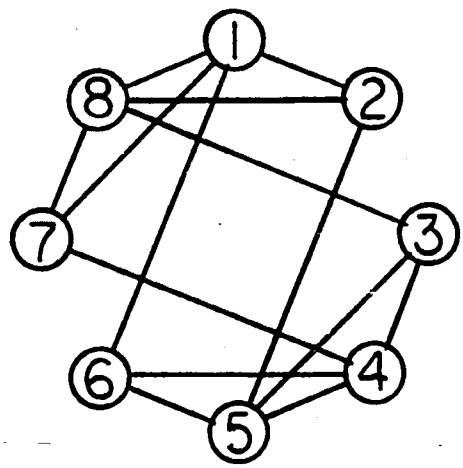


Fig. 8-1. Merger Diagram for the Sequential Problem

minimum of four rows in the merged flow table. There are eight different merging combinations possible to achieve the four row table. These combinations are shown in Table 8-2. In order to obtain the optimum circuit from a four row merged flow table, each possible combination which would produce such a table requires consideration. The circuit

TABLE 8-2

TABLE OF MERGERS FOR SEQUENTIAL PROBLEM

1.	1 - 2	3 - 4	5 - 6	7 - 8
2.	1 - 7	2 - 8	3 - 4	5 - 6
3.	1 - 7	2 - 8	3 - 5	4 - 6
4.	1 - 6	2 - 8	3 - 5	4 - 7
5.	1 - 6	2 - 5	3 - 8	4 - 7
6.	1 - 7 - 8	2	3 - 4 - 5	6
7.	1 - 2 - 8	3	4 - 5 - 6	7
8.	1 - 7 - 8	2	3	4 - 5 - 6

equations which are derived from the synthesis diagrams are different for each merged combination. An analysis will be presented for each possible merging combination to obtain the most optimum circuit configuration. Also, an appraisal method will be introduced for the purpose of comparing the circuit equations for determining the relative complexity of the various circuits.

Merger No. 1

The merged flow table for the first combination of row mergers given in Table 8-2 is shown in Table 8-3. From Table 8-3, it can be observed that no non-adjacent row transitions occur; therefore, using the procedure given in Chapter V, an excitation map can be drawn as shown in Fig. 8-2. The output map for the first merger, presented in Fig. 8-3, is based on the secondary assignments of Fig. 8-2 and the

TABLE 8-3

MERGED FLOW TABLE NO. 1 FOR SEQUENTIAL PROBLEM

	$w_1 w_2$ = 00	01	11	10
a	(1)		3	(2)
b	5		(3)	(4)
c	(5)	(6)	7	
d	1	(8)	(7)	

$y_1 y_2$	$w_1 w_2$ = 00	01	11	10
00	00		01	00
01	11		01	01
11	11	11	10	
10	00	10	10	

Fig. 8-2. Excitation Map No. 1 for Sequential Problem

$y_1 y_2$	$w_1 w_2$ = 00	01	11	10
00	1000		00--	0010
01	0--0		0001	0100
11	0010	1000	--00	
10	-00-	0001	0100	

Fig. 8-3. Composite Output Map No. 1 for Sequential Problem

output states given in Table 7-1 for the corresponding stable state numbers.

The secondary and output circuit equations are obtained from Figs. 8-2 and 8-3, respectively, using the Karnaugh map reading technique presented in Appendix B. The following equations are the network relations in factored form and contain the appropriate hazard eliminating terms.

$$Y_1 = y_2\bar{w}_1 + y_1w_2 \qquad 8\text{-}1$$

$$Y_2 = \bar{y}_1w_2 + y_2(\bar{w}_1 + \bar{y}_1) \qquad 8\text{-}2$$

$$Z_1 = \bar{w}_1(\bar{y}_2\bar{w}_2 + y_2w_2 + \bar{y}_1w_2) \qquad 8\text{-}3$$

$$Z_2 = w_1(y_1 + y_2\bar{w}_2) \qquad 8\text{-}4$$

$$Z_3 = \bar{w}_2(y_1\bar{y}_2 + y_2w_1 + y_1w_1) \qquad 8\text{-}5$$

$$Z_4 = w_2(\bar{y}_2\bar{w}_1 + \bar{y}_1y_2 + \bar{y}_1\bar{w}_1) \qquad 8\text{-}6$$

The diagrams and equations for the remaining merger combinations are obtained in the same manner as given for Merger No. 1. Therefore, no further detailed explanation is given concerning the resulting diagrams and equations.

Merger No. 2

y_1y_2 \ w_1w_2	0 0	0 1	1 1	1 0
0 0	0 0	0 1	0 0	0 1
0 1	0 0	0 1	1 1	0 1
1 1	1 0		1 1	1 1
1 0	1 0	1 0	0 0	

Fig. 8-4. Excitation Map No. 2 for Sequential Problem

TABLE 804

MERGED FLOW TABLE NO. 2 FOR SEQUENTIAL PROBLEM

	$w_1 w_2$ 00	01	11	10
a	(1)	8	(7)	2
b	1	(8)	3	(2)
c	5		(3)	(4)
d	(5)	(6)	7	

$y_1 y_2$	$w_1 w_2$ 00	01	11	10
00	1000	0-0-	0100	-0-0
01	-00-	0001	00--	0010
11	0--0		0001	0100
10	0010	1000	--00	

Fig. 8-5. Composite Output Map No. 2 for Sequential Problem

$$Y_1 = y_2 w_1 w_2 + y_1(\bar{w}_1 + y_2) \qquad 8\text{-}7$$

$$Y_2 = w_1 \bar{w}_2 + \bar{y}_1 \bar{w}_1 w_2 + y_2(w_1 + \bar{w}_2) \qquad 8\text{-}8$$

$$Z_1 = \bar{y}_1 \bar{y}_2 \bar{w}_2 + y_1 \bar{y}_2 w_2 + y_1 \bar{y}_2 w_1 + \bar{y}_2 w_1 \bar{w}_2 \qquad 8\text{-}9$$

$$Z_2 = y_1 y_2 \bar{w}_2 + w_1 w_2 \bar{y}_2 + y_1 \bar{y}_2 w_1 + y_1 w_1 \bar{w}_2 \qquad 8\text{-}10$$

$$Z_3 = \bar{w}_2(y_1 \bar{y}_2 + \bar{y}_1 w_1 + \bar{y}_2 w_1) \qquad 8\text{-}11$$

$$Z_4 = y_2 w_2 \qquad 8\text{-}12$$

Merger No. 3

TABLE 8-5

MERGED FLOW TABLE NO. 3 FOR SEQUENTIAL PROBLEM

	$w_1 w_2$ 00	01	11	10
a	(1)	8	(7)	2
b	1	(8)	3	(2)
c	(5)	6	(3)	4
d	5	(6)	7	(4)

$y_1 y_2$ \ $w_1 w_2$	00	01	11	10
00	00	01	00	01
01	00	01	11	01
11	11	10	11	10
10	11	10	00	10

Fig. 8-6. Excitation Map No. 3 for Sequential Problem

$y_1 y_2$ \ $w_1 w_2$	00	01	11	10
00	1000	0-0-	0100	-0-0
01	-00-	0001	00--	0010
11	0010	-0-0	0001	0-0-
10	0--0	1000	--00	0100

Fig. 8-7. Composite Output Map No. 3 for Sequential Problem

$$Y_1 = y_2w_1w_2 + y_1(\bar{w}_1 + w_1\bar{w}_2 + y_2) \qquad 8\text{-}13$$

$$Y_2 = \text{cannot eliminate hazard} \qquad 8\text{-}14$$

$$Z_1 = \text{cannot eliminate hazard} \qquad 8\text{-}15$$

$$Z_2 = w_1(\bar{y}_2w_2 + y_1\bar{y}_2) \qquad 8\text{-}16$$

$$Z_3 = \bar{w}_2(y_1y_2 + y_2w_1) \qquad 8\text{-}17$$

$$Z_4 = w_2(\bar{y}_1y_2 + y_2w_1) \qquad 8\text{-}18$$

Merger No. 4.

TABLE 8-6

MERGED FLOW TABLE NO. 4 FOR SEQUENTIAL PROBLEM

	w_1w_2 = 00	01	11	10
a	(1)	(6)	7	2
b	1	(8)	3	(2)
c	(5)	6	(3)	4
d	5	8	(7)	(4)

An inspection of Table 8-6 reveals that two transitions occur between non-adjacent rows. Also, no arrangement of the rows can be made to eliminate the transitions. Therefore, this merger combination would not yield an appropriate solution to the sequential problem and will not be further considered.

Merger No. 5

TABLE 8-7

MERGED FLOW TABLE NO. 5 FOR SEQUENTIAL PROBLEM

	$w_1 w_2$ 00	01	11	10
a	(1)	(6)	7	2
b	(5)	6	3	(2)
c	1	(8)	(3)	4
d	5	8	(7)	(4)

Merger No. 5 is discarded for the same transition problem existing in Merger No. 4. No suitable rearrangement of rows is possible.

Merger No. 6

TABLE 8-8

MERGED FLOW TABLE NO. 6 FOR SEQUENTIAL PROBLEM

	$w_1 w_2$ 00	01	11	10
a	(1)	(8)	(7)	2
b			3	(2)
c	(5)	6	(3)	(4)
d		(6)	7	

$$Y_1 = y_2 w_2 + y_1(y_2 + \bar{w}_1) \qquad 8\text{-}19$$

$$Y_2 = w_1 \bar{w}_2 + y_2(w_1 + \bar{w}_2) \qquad 8\text{-}20$$

$$Z_1 = \bar{w}_1(y_1\bar{y}_2 + \bar{y}_2\bar{w}_2) \qquad 8\text{-}21$$

$$Z_2 = w_1(\bar{y}_2 w_2 + y_1\bar{w}_2 + y_1 y_2) \qquad 8\text{-}22$$

$$Z_3 = \bar{w}_2(\bar{y}_1 y_2 + y_2\bar{w}_1) \qquad 8\text{-}23$$

$$Z_4 = w_2(\bar{y}_1\bar{w}_1 + y_2 w_1 + \bar{y}_1 y_2) \qquad 8\text{-}24$$

$y_1 y_2$ \ $w_1 w_2$	00	01	11	10
00	00	00	00	01
01			11	01
11	11	10	11	11
10		10	00	

Fig. 8-8. Excitation Map No. 6 for Sequential Problem

$y_1 y_2$ \ $w_1 w_2$	00	01	11	10
00	1000	0001	0100	-0-0
01			00--	0010
11	0010	-0-0	0001	0100
10		1000	--00	

Fig. 8-9. Composite Output Map No. 6 for Sequential Problem

Merger No. 7

TABLE 8-9

MERGED FLOW TABLE NO. 7 FOR SEQUENTIAL PROBLEM

	$w_1 w_2$ 00	01	11	10
a	(1)	(8)	(7)	2
b			3	(2)
c			(3)	4
d	(5)	(6)	7	(4)

$y_1 y_2$	$w_1 w_2$ 00	01	11	10
00	00	00	00	01
01			11	01
11			11	10
10	10	10	00	10

Fig. 8-10. Excitation Map No. 7 for Sequential Problem

$y_1 y_2$	$w_1 w_2$ 00	01	11	10
00	1000	0001	0100	-0-0
01			00--	0010
11			0001	0-0-
10	0010	1000	--00	0100

Fig. 8-11. Composite Output Map No. 7 for Sequential Problem

$$Y_1 = y_2w_2 + y_1(\bar{w}_1 + \bar{w}_2) \qquad 8\text{-}25$$

$$Y_2 = \bar{y}_1w_1\bar{w}_2 + y_2(w_2 + \bar{y}_1) \qquad 8\text{-}26$$

$$Z_1 = \bar{w}_1(w_2y_1 + \bar{w}_2\bar{y}_1 + y_2) \qquad 8\text{-}27$$

$$Z_2 = w_1(w_2\bar{y}_2 + y_1\bar{y}_2) \qquad 8\text{-}28$$

$$Z_3 = \bar{w}_2(\bar{y}_1y_2 + y_1\bar{w}_1 + y_2\bar{w}_1) \qquad 8\text{-}29$$

$$Z_4 = w_2(y_2 + \bar{y}_1\bar{w}_1) \qquad 8\text{-}30$$

Merger No. 8

TABLE 8-10

MERGED FLOW TABLE NO. 8 FOR SEQUENTIAL PROBLEM

w_1w_2	00	01	11	10
a	(1)	(8)	3	(2)
b			(3)	4
c	(5)	(6)	7	(4)
d		8	(7)	

y_1y_2	00	01	11	10
00	00	00	01	00
01			01	11
11	11	11	10	11
10		00	10	

Fig. 8-12. Excitation Map No. 8 for Sequential Problem

$y_1 y_2$ \ $w_1 w_2$	00	01	11	10
00	1000	0001	00--	0010
01			0001	0-0-
11	0010	1000	--00	0100
10		0-0-	0100	

Fig. 8-13. Composite Output Map No. 8 for Sequential Problem

$$Y_1 = y_2\bar{w}_2 + y_1(y_2 + w_1) \qquad 8\text{-}31$$

$$Y_2 = \bar{y}_1 w_1 w_2 + y_2(\bar{w}_2 + \bar{w}_1 + \bar{y}_1) \qquad 8\text{-}32$$

$$Z_1 = \bar{w}_1(y_2 w_2 + \bar{y}_1\bar{w}_2 + \bar{y}_1 y_2) \qquad 8\text{-}33$$

$$Z_2 = w_1 y_1 \qquad 8\text{-}34$$

$$Z_3 = \bar{w}_2(y_1\bar{w}_1 + \bar{y}_2 w_1 + y_1\bar{y}_2) \qquad 8\text{-}35$$

$$Z_4 = w_2\bar{y}_1 \qquad 8\text{-}36$$

Appraisal of Circuit Equations

In order to appraise the relative complexity of the circuits represented by the various combinations of equations, a criteria must be established that would reflect the resulting circuit complexity. The form of the secondary equations for each merging combination is characteristic of a detent valve; therefore, two four-way, detent valves are needed to satisfy the secondary memory action in each combination. The Z_1 and Z_2 output equations as well as the Z_3 and Z_4 equations for each combination are implemented by three-position, four-way, spring-centered,

block-centered, pilot-operated valves. Therefore, the most probable basis for appraising the circuit equations would be on the number of AND and OR valves required to generate the proper signals to operate the secondary and output valves.

Since the relative cost of an AND function component is comparable to that of the OR function component, no consideration need be given to the frequency of occurrence of one over the other. Furthermore, it can be rightfully assumed that each indication in the circuit equation of an AND or OR function requires the use of only one valve. In other words, no advantage can be given to operational patterns in the equations. The validity of this statement can be demonstrated by considering the following equation:

$$T = a_1(a_2b_1 + a_3b_2c_1 + a_2c_2) \qquad 8\text{-}37$$

Equation 8-37 describes a circuit having seven logic operations -- either AND or OR. This equation can be illustrated by function blocks as shown in Fig. 8-14. Since the perfect fluid logic elements are binary -- a function of only two signals -- a logic block is required for each operation.

The concept of needing a logic block or valve for each operation indicated in a circuit equation can be used to establish a quantitative basis for appraising the complexity of an equation. Thus, Eq. 8-37 would have a complexity value of seven. It is important in comparing two equations on the complexity value basis that both equations have equivalent forms (non-factored, uni-factored, or multi-factored forms). Special consideration was given to the form of the equations derived

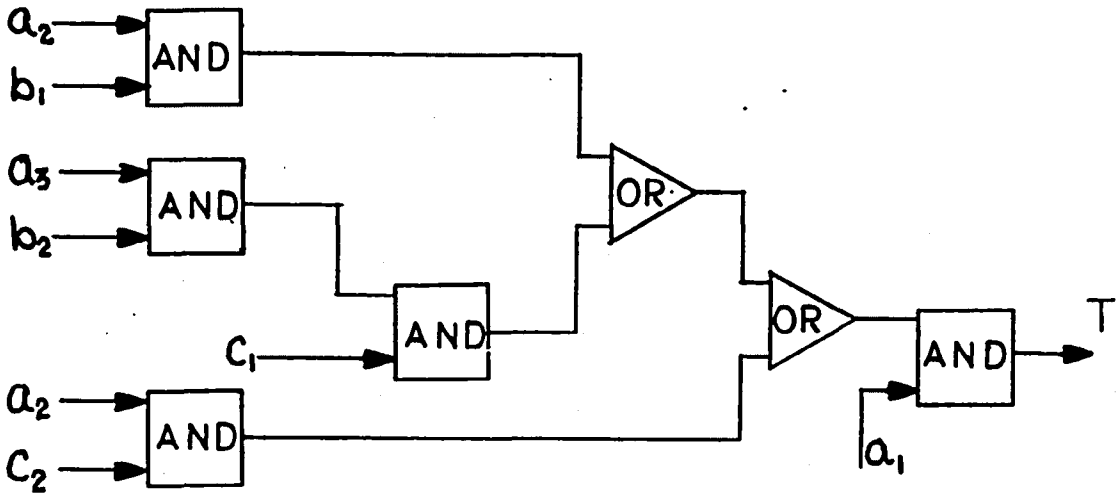


Fig. 8-14. Logic Representation for Eq. 8-37

for the sequential circuit problem in order that a direct comparison for each group of equations could be made. An examination of the secondary and output equations for each merger reveals the following complexity values for the sequential circuit problem:

$$CV_1 = 3 + 4 + 6 + 3 + 6 + 6 = 28$$

$$CV_2 = 5 + 7 + 11 + 11 + 6 + 1 = 41$$

$$CV_3 = \text{hazard}$$

$$CV_4 = \text{transitions}$$

$$CV_5 = \text{transitions}$$

$$CV_6 = 4 + 4 + 4 + 6 + 4 + 6 = 28$$

$$CV_7 = 3 + 5 + 5 + 4 + 6 + 3 = 26$$

$$CV = 4 + 6 + 6 + 1 + 6 + 1 = 24$$

It should be recognized that the complexity value of a network represents the number of AND and OR operations required to implement the logic of the system. Each AND and OR operation indicated in the

network equations means that a valve must be used. Therefore, in order to obtain the simplest network of switching valves, the circuit combination having the lowest complexity value is the best. To further emphasize this concept, an inspection of the complexity values for the various merger combinations reveals some remarkable differences. The second merger combination has a network complexity value of 41 which infers that 41 AND and OR valves are required to provide the appropriate signals to the output and secondary systems. In comparison, the eighth merger combination only requires 24 AND and OR valves to facilitate the proper signal emissions. The circuit configuration for Merger No. 8 is shown in Fig. 8-15.

The complexity value must be considered as representing the maximum number of AND and OR components required to implement the network. In many cases, a significant reduction of the circuit components can be accomplished by employing valve interpretation techniques and taking the maximum advantage of multiple signal requirements. An example of valve interpretation for simplification purposes can be seen in Fig. 8-15 where two spring-offset valves are employed in the secondary signal circuit. The use of these valves eliminated four AND valves from the system and provided an independent tanking line for the secondary valves. The multiple use of a generated signal for simplifying a circuit can be observed in the Y_2 secondary signal circuit. According to the characteristics of detent valves presented in Chapter VI, the Y_2 relation (Eq. 8-32) is interpreted as shown in Fig. 8-16. Thus, the signal w_1w_2 is needed to actuate both ends of the valve. By eliminating duplication of this signal, the circuit is reduced by one AND valve.

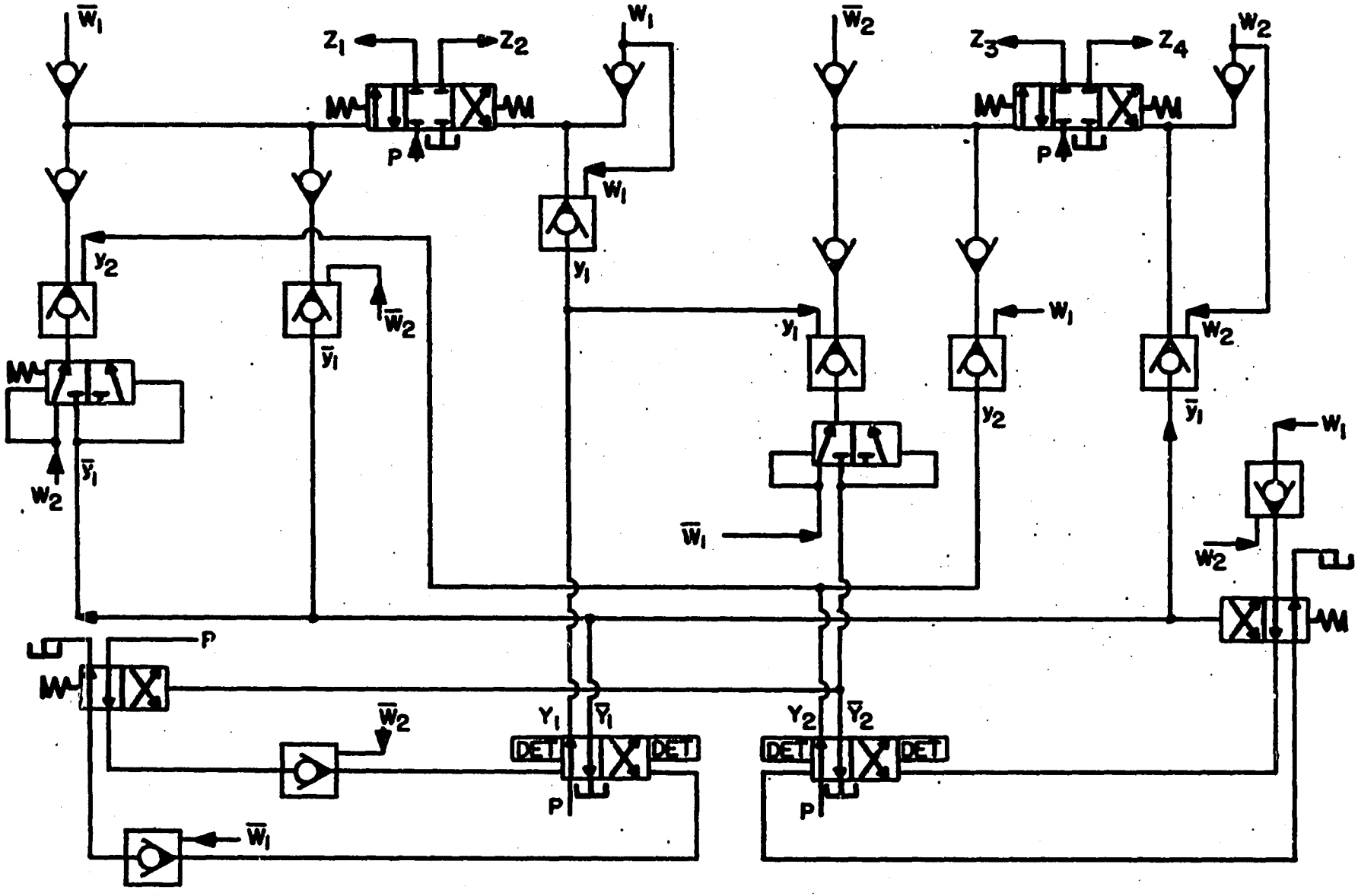


Fig. 8-15. Circuit Configuration for Merger No. 8 Sequential Problem.

There are undoubtedly several places in the circuit (Fig. 8-15) where network reduction could be achieved; however, the complete optimization of the logic circuit was not the objective of this presentation.

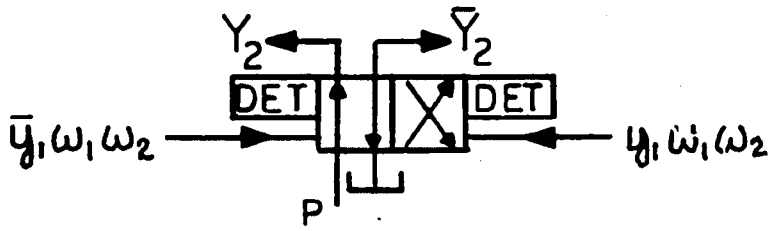


Fig. 8-16. The Y_2 Secondary Circuit for Merger No. 8

Since the circuit equations for the intuitively designed problem analyzed in Chapter VII are presented in the same form as the sequential circuit equations, the complexity value of the equations should be of interest. The complexity value of Eqs. 7-13, 7-14, 7-15, 7-16, 7-17, 7-18, 7-19, and 7-20 is

$$CV = 7 + 1 + 7 + 1 + 6 + 5 + 6 + 5 = 38$$

Based on the complexity values of the intuitively and logically designed circuit equations, a respectable simplification of the control network can be realized. Comparing the circuit configuration for Merger No. 8 (Fig. 8-15) with that for the intuitively designed circuit (Fig. 7-1) does not indicate any major difference in simplicity. It should be recognized, however, that Fig. 7-1 represents a highly optimized circuit in which maximum advantage was taken of all signals (note that pump pressure is not applied to the secondary and output signal circuits). In contrast, Fig. 8-15 represents a circuit that was

obtained directly from the logic synthesis and interpretation method. It is highly probable that the circuit in Fig. 8-15 can be reduced substantially whereas it is highly unlikely that the initutively designed circuit can be reduced in any fashion.

It should be emphasized that this chapter has demonstrated that a complicated sequential circuit can be synthesized logically and in its basic form can be expected to compare favorably with an intuitively designed circuit. Another aspect which has not been emphasized is the time element involved in the design procedure. Several weeks are sometimes required to intuitively design sequential fluid circuits whereas equivalent circuits can be logically synthesized in a few hours. Furthermore, a logic solution can consider all possible problems which may create operational difficulties and eliminate their effects before the circuit is fabricated.

Experimental Verification

The circuit shown in Fig. 3-15, together with the cylinders and signal systems illustrated in Fig. 7-1, was fabricated and the logic and operational characteristics experimentally verified. The physical arrangement of the circuit is shown in Fig. 8-17. Back-pressure load valves were installed in the cylinder power lines to simulate fully loaded cylinder rod conditions. System pressure was varied to a maximum of 1600 psi, and the flow rate ranged from 2 gpm to 18 gpm. The logic network performed perfectly from the start and continued to coordinate the movements of the cylinder rods properly throughout the test program. No external action could confuse the incorporated logic of the circuit short of blocking signal lines.

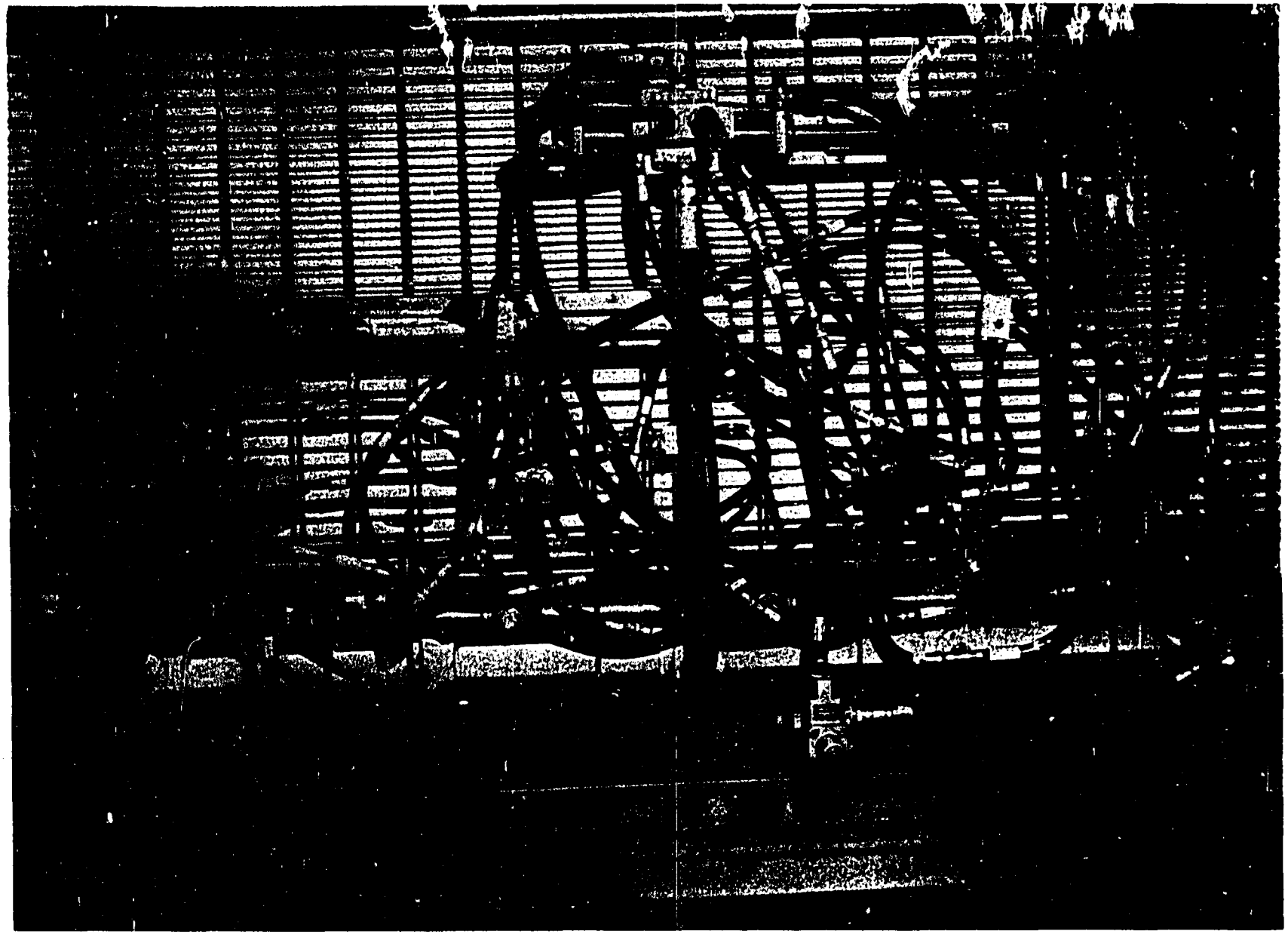


Fig. 8-17. Physical Arrangement of Fabricated Sequential Circuit.

CHAPTER IX

CONCLUSIONS

The control of machines by fluid power systems has become an important facet of modern control technology. The field of fluid servomechanisms has been one of the most rapidly growing fields of controls engineering and has already achieved a high degree of sophistication. In contrast, the design and analysis of fluid switching networks has not experienced any major growth; and its present application is still dependent upon the ingenuity of the engineer. This dissertation is concerned with an investigation of logic methods for fluid switching circuit synthesis and analysis which should help alleviate the recognized inadequacy of current intuitive procedures.

Fluid control networks incorporating fluid switching circuits have been universally applied in many machine areas such as mobile equipment, machine tools, and automatic transfer machines. New applications for digital fluid circuits are constantly being reported. The recent interjection of fluid amplifiers as potential logic elements in fluid networks has created industry-wide interest in fluid digital systems and fluid computer applications.

The primary goal in the selection of a specific control system is to achieve many of the advantages inherent to fluid systems. Some of

these advantages are as follows:

1. Component reliability and long life
2. Low heat generation
3. High signal amplification
4. Insensitivity to vibrational effects
5. Insensitivity to extremes of temperature
6. Versatile output power and motion.

In order to realize the advantages offered by fluid systems involving fluid switching circuits, a non-intuitive method must be advanced for their synthesis and analysis. Such a method has not been reported, and its absence is evidenced by the relatively simple networks currently in use. A general logic method would permit the synthesis of complex fluid networks possessing "decision-making" ability and would provide the means of extending the reasoning power of the design engineer.

This dissertation presents a logic method for the synthesis and analysis of fluid switching networks which satisfies the requirements of a universal design method. The contributions to the fluid power engineering field resulting from this study are as follows:

1. Recognition of the logic analogy existing between electrical switching elements and fluid switching elements.
2. A fluid transmission concept was introduced which provided the means needed to establish a practical correlation between electrical and fluid switching theory.
3. A concept of fluid complementation was proposed which provided the means of recognizing and describing the fundamental logic characteristics of non-classical fluid components.

4. A fundamental basis was established and demonstrated for interpreting all types of fluid switching components.

5. A composite operational chart was developed to verify the logic and operational behavior of fluid networks by revealing the contributions of each part of the circuit equations.

6. An analysis method was developed which would yield the logic equations and the characteristic synthesis maps for an existing network.

7. An appraisal method was introduced to give a quantitative comparison of equivalent circuit simplicity.

To the author's knowledge, this dissertation has demonstrated for the first time that a fluid network involving sequential operations could be synthesized and analyzed logically. The method proposed for analytically interpreting and implementing network equations has satisfied the requirements of a general design method.

The objectives of this investigation have been fulfilled to a degree far exceeding the initial expectations of the author. It is firmly believed that this study will incite fluid power engineers to pursue the logic synthesis of fluid circuits in many advanced areas. Such action will guarantee the introduction of many novel devices in the near future.

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APPENDIX A

POSTULATES AND THEOREMS OF BOOLEAN ALGEBRA

The Postulates of Boolean algebra are simple, independent, and consistent statements which relate the concepts of binary algebraic logic. They can be listed as follows:

P-1	(a) $X = 0$ if $X = 1$	(b) $X = 1$ if $X \neq 0$
P-2	(a) $1 \cdot 1 = 1$	(b) $0 + 0 = 0$
P-3	(a) $0 \cdot 0 = 0$	(b) $1 + 1 = 1$
P-4	(a) $0 \cdot 1 = 1 \cdot 0 = 0$	(b) $1 + 0 = 0 + 1 = 1$
P-5	(a) $\bar{1} = 0$	(b) $\bar{0} = 1$

The theorems of Boolean algebra are deduced from the postulates and show the relationships among the concepts. The theorems establish the general rules for equivalent expressions involving variables. The theorems are listed in groups of the number of variables involved.

Single Variable Theorems

T-1	(a) $0 \cdot X = 0$	(b) $1 + X = 1$
T-2	(a) $1 \cdot X = X$	(b) $0 + X = X$
T-3	(a) $XX = X$	(b) $X + X = X$
T-4	(a) $X\bar{X} = 0$	(b) $\bar{X} + X = 1$
T-5	(a) $\overline{(X)} = \bar{X}$	(b) $\overline{(\bar{X})} = X$

Two Variable Theorems

T-6	(a) $XY + YX$	(b)	$X + Y = Y + X$
T-7	(a) $X + XY = X$	(b)	$X(X + Y) = X$
T-8	(a) $X + \bar{X}Y = X + Y$	(b)	$X(\bar{X} + Y) = XY$
T-9	(a) $XY + X\bar{Y} = X$	(b)	$(X + Y)\,(X + \bar{Y}) = X$

Three Variable Theorems

T-10	(a) $XYZ = X(YZ) = (XY)Z$	(b)	$X+Y+Z = X+(Y+Z) = (X+Y)+Z$
T-11	(a) $XY + XZ = X(Y+Z)$	(b)	$(X+Y)(X+Z) = X + YZ$
T-12	(a) $\overline{XYZ} = \bar{X} + \bar{Y} + \bar{Z}$	(b)	$\overline{X+Y+Z} = \bar{X}\,\bar{Y}\,\bar{Z}$
T-13	(a) $XZ + \bar{X}YZ = XZ + YZ$	(b)	$(X+Z)(\bar{X}+Y+Z) = (X+Z)(Y+Z)$
T-14	(a) $XY + YZ + \bar{X}Z = XY + \bar{X}Z$	(b)	$(X+Y)(Y+Z)(\bar{X}+Z) = (X+Y)(\bar{X}+Z)$
T-15	(a) $XY + \bar{X}Z = (X+Z)(\bar{X}+Y)$	(b)	$(X+Y)(\bar{X}+Z) = XZ + \bar{X}Y$

The postulates and theorems which have been presented were listed as dual relations; in other words, Theorem T-6 (b) is the dual of Theorem T-6 (a). The dual of a Boolean expression is obtained by changing all AND's to OR's, changing all 0's to 1's and vice versa. Another form of a Boolean expression is the complementary expression. The complement of a Boolean expression always equals one when the expression equals zero. The complement is obtained in the same manner as the dual except that each literal is complemented; for example, consider the expression $X\bar{Y} + XY\bar{Z}$. The dual is $(\bar{X}+\bar{Y})(X+Y+\bar{Z})$; whereas its complement is $(\bar{X}+Y)(\bar{X}+\bar{Y}+Z)$.

The theorems of Boolean algebra can be proved from the postulates by using the method of "perfect induction." This method consists of listing all combination of values the variables of the theorem could

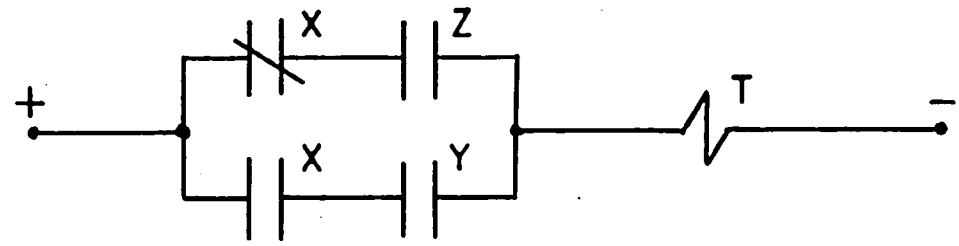
possess and making substitutions of these values in both sides of the relation. If the value of both sides is the same after each substitution, then the theorem is valid. An example of the method is illustrated in Table A-1 using Theorem T-15 (a).

TABLE A-1

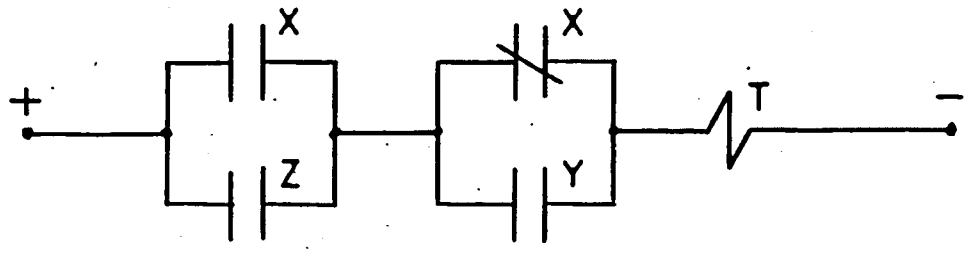
PROOF OF THEOREM T-15 (a)

Variables			Left Side	Right Side
X	Y	Z	XY+XZ	$(X+Z)(\bar{X}+Y)$
0	0	0	0·0 + 1·0 = 0	(0+0)(1+0) = 0
0	0	1	0·0 + 1·1 = 1	(0+1)(1+0) = 1
0	1	0	0·1 + 1·0 = 0	(0+0)(1+1) = 0
0	1	1	0·1 + 1·1 = 1	(0+1)(1+1) = 1
1	0	0	1·0 + 0·0 = 0	(1+0)(0+0) = 0
1	0	1	1·0 + 0·1 = 0	(1+1)(0+0) = 0
1	1	0	1·1 + 0·0 = 1	(1+0)(0+1) = 1
1	1	1	1·1 + 0·1 = 1	(1+1)(0+1) = 1

The validity of a proposed equivalence, including theorems, can be ascertained by circuit reasoning. To illustrate this process, the circuits described by both sides of the expression of Theorem T-15 (a) are developed as shown in Fig. A-1. Since the operating characteristics of both circuits are identical, the validity of the theorem can be accepted.



(a) Left Side of Expression



(b) Right Side of Expression

Fig. A-1. Circuit Configuration for Theorem T-15 (a)

APPENDIX B

THE KARNAUGH MAP

The Karnaugh map technique, developed by Karnaugh (28), provides a means of representing and simplifying switching circuit functions by applying elementary geometrical concepts which are related to the algebraic properties of the equations. This simple and rapid technique minimizes the number of appearances of algebraic variables in the associated equation. Although the theorems of Boolean algebra can be rigorously applied to simplify binary relations, it is a tedious procedure for all but the most trivial cases.

The Karnaugh Map technique for generating near-minimal forms of algebraic equations depends upon the recognition of certain basic patterns of map entries. The map, itself, must contain a sufficient number of rows and columns to provide appropriately a map location for each of the 2^n possible combinations of variable values. A distinguishing feature of this map is the use of the reflected binary (Gray code) code for labeling the rows and columns. The blocks composing the map created by the intersections of the rows and columns are called "cells." The basic patterns displayed by cells containing entries are called "subcubes." More specifically, a subcube is a set of cells possessing an adjacency relation. Such a relation can only occur when one or more of

the variables defining the cells of the subcube have constant values.

A Karnaugh map is concerned basically with algebraic equations having a two-stage form (the sum of products). A given equation is satisfied (equal to 1) when the values of the variables comply with the requirements of any product (AND) group in the equation. A specific entry in a cell of the map prescribes the combination of variables required to give one solution to the equation. Hence, a (1) is entered in a cell that describes the proper values of the variables needed by a particular product group to yield a solution.

The technique of making map entries can be demonstrated by considering the equation (T-14a) given by

$$A = XY + YZ + \bar{X}Z \qquad \text{B-1}$$

This equation is satisfied by the variable combination X AND Y, OR Y AND Z, OR NOT X AND Z. Three variables are involved; therefore, the Karnaugh map can be illustrated as shown in Fig. B-1. A (1) is entered in the cell or cells describing each product term. Therefore, for the term XY, a (1) is entered in the cell or cells of row X = 1 where Y = 1. The appropriate entries for the terms YZ and $\bar{X}Z$ are also inserted to complete the map.

X \ YZ	00	01	11	10
0		1	1	
1			1	1

Fig. B-1. Karnaugh Map for Eq. B-1

Interpreting the Karnaugh map to obtain near-minimal expressions requires the recognition of optimum subcube patterns. The simplest equations are normally obtained by using the largest subcubes. The expression required to locate a single cell involves every variable on the map; whereas a two-cell subcube eliminates one of the variables. Likewise, a four-cell subcube reduces the describing variables by two. and an eight-cell eliminates the three variables. This subcube concept for eliminating the number of describing variables can be demonstrated by Fig. B-2. The equation representing the map requires a four variable, a three variable, and a two variable product term to include the single cell, the two-cell subcube, and the four-cell subcube, respectively. The equation exhibited by Fig. B-2 is

$$Y = ab\bar{c}\bar{d} + a\bar{b}c + \bar{a}d \qquad \text{B-2}$$

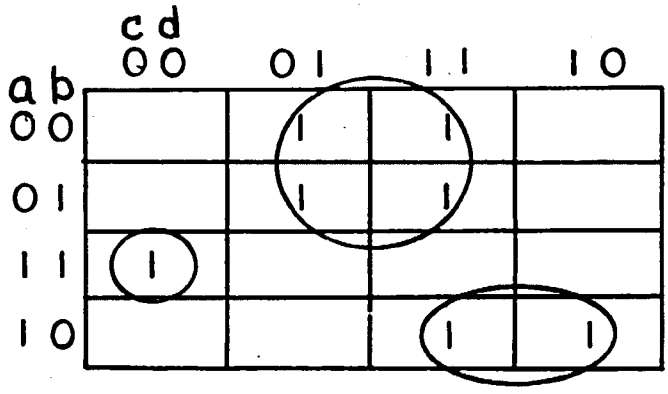


Fig. B-2. Karnaugh Map for Eq. B-2

The map in Fig. B-1 contains two subcubes which can be described by the equation

$$A = XY + \bar{X}Z \qquad \text{B-3}$$

This equation is a simpler relation than Eq. B-1, and its equivalence

can be verified by Theorem T-14 (a). The subcubes used to obtain Eq. B-3 satisfy the requirement that it is necessary to include a given cell only once. The three (2-cell) subcubes used for Eq. B-1 contain the redundant subcube YZ.

The properties of adjacency patterns which establish subcubes can be illustrated by the maps in Fig. B-3. The four maps display cell patterns of the same type -- a four-cell subcube described by two variables. The subcubes can be represented as follows: 1) map (a) - $\bar{W}\,\bar{X}$, 2) map (b) - $\bar{W}Y$, 3) map (c) - $X\bar{Z}$, and 4) map (d) - $\bar{X}\,\bar{Z}$. The characteristics of peripheral cells to combine with cells on the opposite side should be noted.

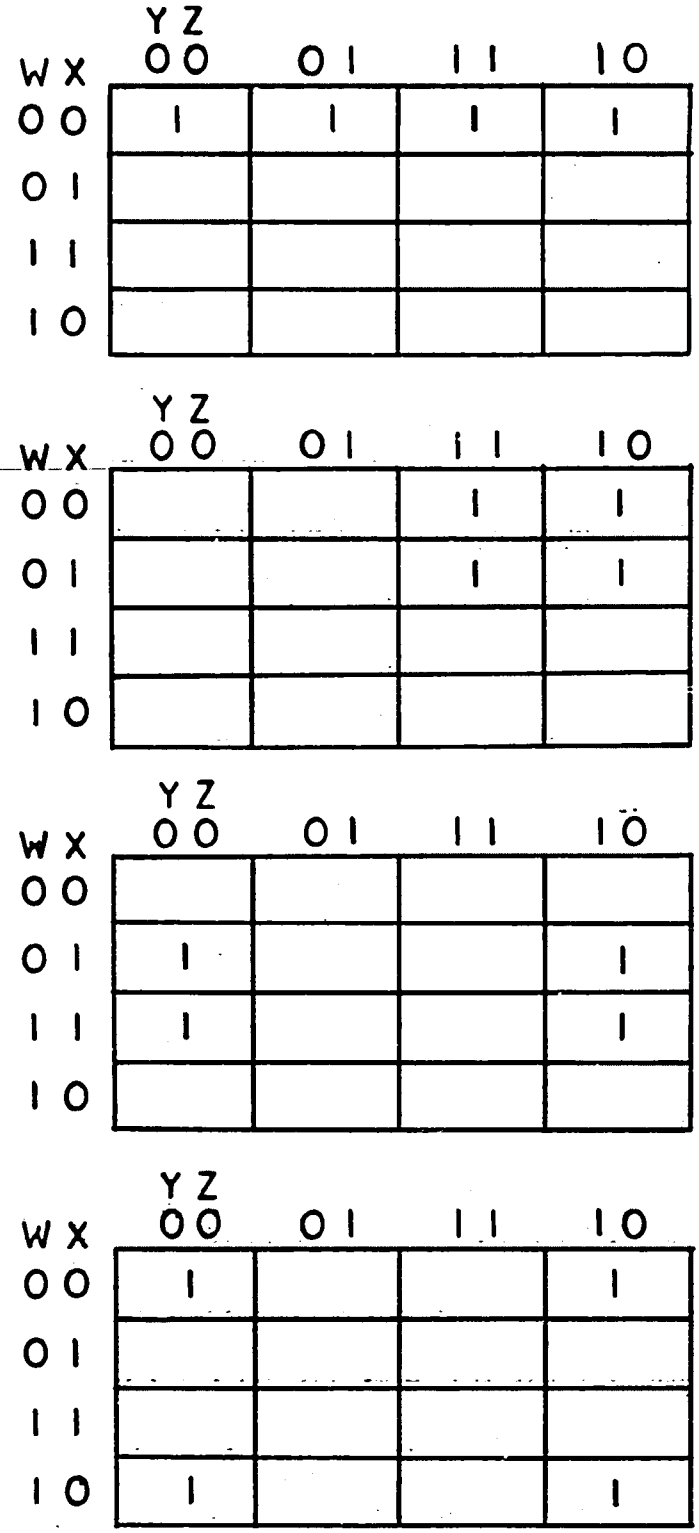


Fig. B-3. Properties of Adjacency Patterns.