TEST PROCEDURE FOR ERASABLE PROGRAMMABLE LOGIC DEVICES

By

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1985

Submitted to the Faculty of the
Graduate College of the
Oklahoma State University
in partial fulfillment of
the requirements for
the Degree of
MASTER OF SCIENCE
May, 1987

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PROGRAMMABLE LOGIC

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PREFACE

This study was begun to fulfill part of contract number 01-3374 with Sandia National Laboratories in Sandia, New Mexico. I am indebted to Dr. David Soldan, formerly of Oklahoma State University, for including me in the research project. A report of the entire project entitled "Sandia Sea Lance Telemetry Testing" was submitted to Sandia National Laboratories in January, 1987.

I wish to express my sincere gratitude to my original advisory committee members, Dr. David Soldan, Dr. Randy Reininger, and Dr. Richard Cummins. Thanks is especially due to Dr. David Soldan for remaining on my committee after moving away from Stillwater, Oklahoma to Wichita, Kansas. Without his advice and direction, this thesis would never have been completed. Special thanks is also due to Dr. Ramachandra Ramakumar for joining my committee after Dr. Reininger moved away. Dr. Ramakumar has been a great help in proof-reading and answering the many questions I could not ask Dr. Soldan without a long distance phone bill.

I appreciate the exceptional job my brother Dan Jones has done on the figures. He and the rest of my family have been excellent support. I would also like to thank the Electrical Engineering Technology Department and Dr. Perry McNeil for the teaching job on campus which has helped me pay the bills while completing the requirements for my degree.

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CHAPTER I

INTRODUCTION

The production of electronic circuitry is a highly competitive industry. Electronic systems must be manufactured and assembled in the most cost effective way possible. Additionally, the reliability of devices, components, and systems must be continually improved to stay competitive. Improvements in cost and reliability can be obtained at several levels of the manufacturing process: a) component level, b) circuit board level, c) subsystem level, and d) systems level. Component manufacturers are attempting to optimize the construction processes to produce high reliability components. Circuit designers are working to create the most efficient circuit board layouts possible. Automatic manufacturing techniques are being introduced to improve the yield of manufacturing processes. Testing is being used to achieve cost efficient reliability at the board, subsystem, and systems levels.

Electronic circuit testing is being conducted at many stages of the manufacturing process. Incoming devices are tested by manufacturing quality assurance, circuit boards are subject to in-circuit testing and functional testing[1], and functional systems test is used as a final check before shipping a complete product.

Programmable devices however, need an extra testing stage. After programming, the devices should be tested to assure that the desired function has been stored in each component. Frequently used

programmable devices now include Programmable Logic Arrays (PLAs), Read Only Memories (ROMs), and Erasable Programmable Read Only Memories (EPROMs). Another recently introduced programmable device is the Erasable Programmable Logic Device (EPLD). Several companies are now producing EPLDs.

The EPLD is similar to a Programmable Logic Array (PLA) in that it has the programmable sum of products matrix. In addition, the EPLD has the capability of sequential operation. Each sum of products term has a flip-flop on the output which can be used or bypassed. There are also selectable modes on each sum of products which can be used to provide feedback. Other additional features included in some EPLD's are varied numbers of product terms on each OR, shared AND terms on adjacent OR's, and buried register for more complicated logic functions[2].

CHAPTER II

PLA TESTING

Though the EPLD has many similarities to a PLA, the variations described above make testing a much more complex task. One must consider the optional feedback, registers, shared terms, clocking, and selectable I/O. The addition of sequential operation alone multiplies the number of possible tests by the total number of states. There is also the problem of getting the device to the desired state before each test. Clearly, the differences between PLAs and EPLDs make the PLA test techniques insufficient to test an EPLD. However, PLA techniques can be used with restrictions or modifications, because most of the EPLD architecture is identical to that of a PLA.

2.1 Logic Circuit Testing

All testing of circuits consisting of logic functions is conducted by some sort of test generation routine or program. The program is based on an algorithm to generate sets of inputs for the circuit which produce known outputs for the function. The sets of inputs or test patterns will test for all faults which would result in the circuit having a different output from the fault free circuit. The object of the test generation routine is then to generate a set of test patterns which will test for all or nearly all possible faults that may occur in the circuit.

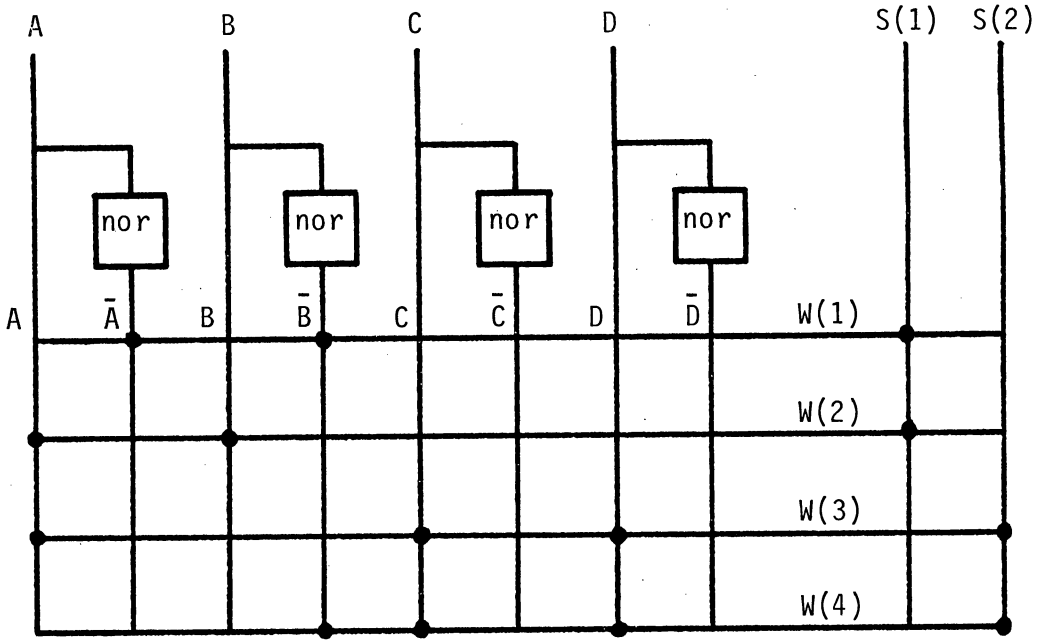
The most complete set of test patterns is the exhaustive test set. This consists of all possible combinations of the inputs. For a purely combinational circuit with n inputs 2^n test patterns would be required. If the circuit were sequential, then the outputs would not only depend on the current inputs but also on the current state of the clocked devices, most commonly flip-flops. With m flip-flops added to the above combinational circuit, there are now 2^n times 2^m total tests for exhaustive testing[3]. To give this emphasis consider the case where a combinational circuit has twelve inputs requiring 2^{12} or 4096 tests. Then, if only ten flip-flops were added, the number of tests would increase to 2^{12} times 2^{10} or 4,194,304. Clearly, the addition of flip-flops, like the ones present in EPLDs, makes testing a much larger task than the purely combinational PLA. This also shows how exhaustive testing can become a nearly impossible task.

There is more strategy involved in testing than the simple generation of an exhaustive test set. One only needs to test for each fault once. For this reason, models have been devised to describe the kinds of possible faults. These models are used to define all the possible faults first, then tests are generated to detect all the faults with the fewest number of test patterns possible. For a PLA with 16 inputs, 48 product terms, and 8 outputs, it has been shown[4] that with one set of fault models, the test set can be limited to a maximum of 1920 tests as opposed to the 2^{16} or some 65,000 tests for exhaustive testing. The actual test set used is often realistically only one quarter of this limit for a common PLA circuit[4].

2.2 Fault Models

All current test techniques have some way of modeling expected faults in the test generation routine. In PLA testing there are three single fault models in common use. They are the stuck-at model, the crosspoint model, and the short model. All three models are ways of looking at the possible failures in any given device. These faults could have been caused by a number of different factors, but the tester initially only wants to detect the presence of such a fault. The models are classifications of types of defects common to PLAs. None of these models are mutually exclusive, but tests generated for each model result in many redundant tests. For that reason, a large part of any test generation routine is to remove these unnecessary tests and to reduce the time it takes to test each device. To reduce the number of tests needed to completely test the device, it is necessary to use test patterns that detect the largest number of faults. These are all considerations in PLA testing based on fault models[4-14].

The stuck-at model looks at device faults in terms of the way they look to the rest of the circuit. The concept is that many missing connections or shorts appear to be lines stuck at a logical 1 or a logical 0 (a high or low voltage). This kind of fault prevents the inputs from having any effect on the affected line. So, for all practical purposes the line is stuck. Various kinds of failures in chip construction result in different stuck-at values in different manufacturing processes. One example of a test set for all stuck-at faults for a simple PLA circuit is shown in Figure 1. The first column shows the inputs A, B, C, and D. The second column gives the output for a fault free circuit with the given inputs. The third column gives the



ABCD	S(1)	S(2)	Stuck Fault Detected
0111	1	1	$\bar{A}$W(1),BW(2)
1000	1	1	$\bar{B}$W(1),AW(2),AW(3),$\bar{B}$W(4)
0110	1	1	CW(3),CW(4)
0101	1	1	DW(3),DW(4)
1111	0	1	S(1)W(1)
0000	0	0	S(1)W(2),S(2)W(3)
1100	0	0	S(2)W(4)

T = {0111,1000,0110,0101,1111,0000,1100} is the set of tests that detects all the single stuck faults.

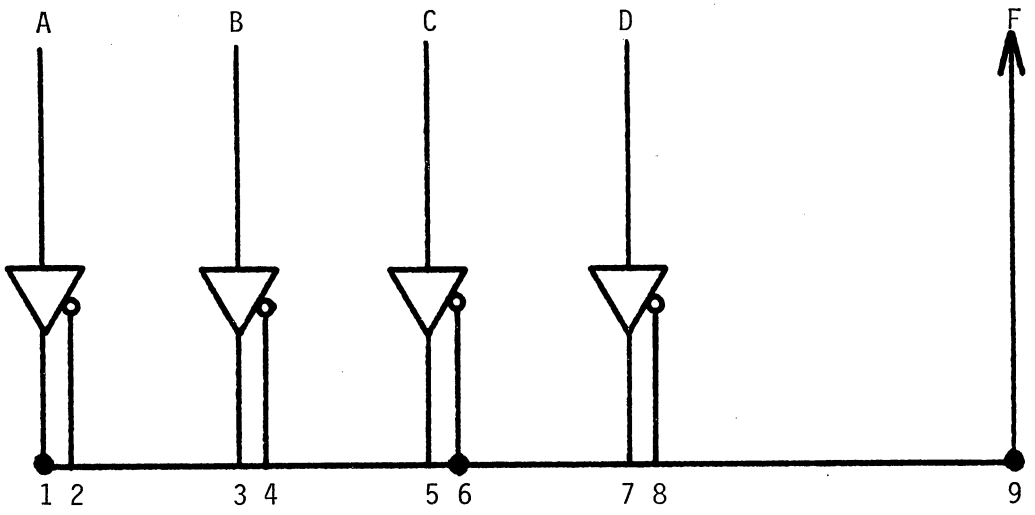
SOURCE NO. 14

Figure 1. Tests for Stuck-at Faults

faults tested and the W line used to pass the fault to the output. This example is based on the description of a PLA as a NOR-NOR combination which is identical in function to an AND-OR arrangement. The function can be understood by considering the W lines to have the value of a NOR of all those inputs connected to them with the dots. The S lines have the value of a NOR of the W lines similarly connected[14].

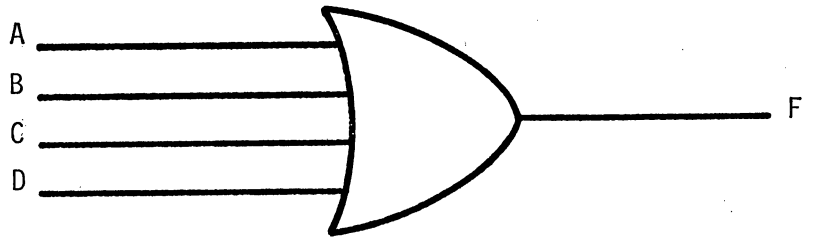
The crosspoint model covers a larger set of faults than the stuck-at model. This model looks at the presence and absence of a connection at the programmable crosspoints in the AND and OR arrays. The tests generated on the crosspoint model check that the connections in the arrays are present at only the correct places. A sample test set for a four input single output portion of a PLA is shown in Figure 2. The one assumption is that an open line appears to be stuck at a logical 1. Note that all eight possible crosspoint faults can be tested with only four tests. The crosspoints which are meant to be connected, denoted by the dots, are tested to see if the crosspoint is not present, while the crosspoints which are not desired are tested to see if they are erroneously connected[14].

The short model tests faults which are the results of more severe manufacturing failures. These faults are most often detected by the manufacturing quality analysis tests. The faults described by this model are actual shorts between neighboring circuit paths. These may be between two metal lines, two diffusion lines, two polysilicon lines, or any combination of two different lines. In most processes the result of this kind of fault is a wired-AND between the two lines. This causes the two lines to have the same value. Figure 3 shows an example of a short fault using a simple four input OR gate. The assumption is that a

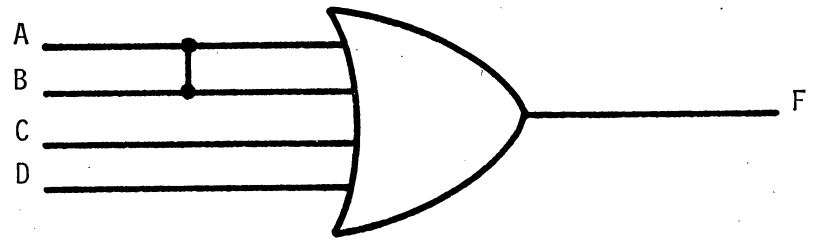


A B C D	F	Crosspoints Tested
1 0 1 0	1	1
0 0 0 0	1	6
0 1 1 1	0	2,3,5,7,9
0 0 1 0	0	2,4,5,8,9

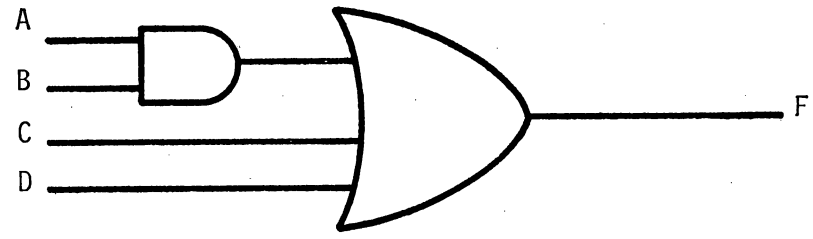
Figure 2. Crosspoint Fault Tests



(a) Desired Circuit



(b) Faulty Circuit



(c) Faulty Circuit Equivalent

Test Pattern:

ABCD	F
1000	1

if Faulty F=0

Figure 3. Short Fault Test Sample

short results in an AND of the two connected lines[3]. For the given sample test pattern it is clear to see that the fault free output would be a 1, but when A and B are connected the value for F is now 0. In a PLA or EPLD there are many parallel lines which can produce this kind of fault if there happens to be an electrical connection.

All of these models are based on the assumption that there is only one fault or a number of faults that do not mask each other. This assumption is true in most cases, but there are still some failures which are not detected as a result of the few instances it is not true. For this reason, some test routines also include a multiple-fault model which attempts to detect a fault in the presence of other faults[9,10].

2.3 Test Generation Routines

Though the fault models are similar, there are still many strategies to developing the optimum test generation routine. Some algorithms approach the task of testing from the function the circuit represents. Often called functional level testing, the tester checks to make sure the programmed device exercised the desired function[11]. Less attention is paid to the device hardware while attention is focused on the outputs presenting the intended function of the inputs. Many articles have been written on similar ways to generate tests for PLAs and complex combinational circuits. The test generation routines differ in the way the PLA structure is described, the order of the fault model covered first, and the fault models themselves. Each routine places a different emphasis on program size, memory conservation, test set minimization, and program each of use[4-11,14].

One approach, taken by Charles W. Cha[14], looks at the fact that the three single fault models contain many redundant tests. One fault is often tested by many test patterns. To prevent the waste of time to generate and then delete or run the extra tests, Cha shows that most stuck-at faults and short faults are tested for using the test set for all crosspoint faults. For this reason, Cha proposes that the tests for all crosspoint faults be generated first, and then the select classes of stuck-at faults and short faults be generated to complete the set.

CHAPTER III

EPLD TESTING

As stated earlier, an EPLD is similar in architecture to a PLA. Figure 4 is a simplified diagram of a standard PLA. An EPLD contains an entire PLA structure with the addition of a must more complex structure on each output line. Each output structure along with its combinational PLA-like function is called a macrocell. A general output cell is shown in Figure 5. The two blocks containing open connections are programmable with the crosspoints of the PLA portion of the device. The enable on the output is often a programmable function of the inputs. The enable and the feedback make it possible to use the output line as an alternate input. Thus, it is labeled as an I/O line instead of just the output.

Testing EPLDs is different than testing PLAs because of the EPLD's capability for both combinational and sequential operation. For a purely combinational circuit, such as a PLA, the output is a function only of the current inputs. For sequential circuits, the output may depend not only on the inputs to the circuit but also on the current state of the circuit. As a result, it is important to control not only the inputs but also the state of the circuit when testing EPLDs.

The ease of testing an EPLD circuit depends on the output scheme of the programmed circuit. An EPLD that realizes a purely combinational circuit without feedback can be tested using techniques developed for

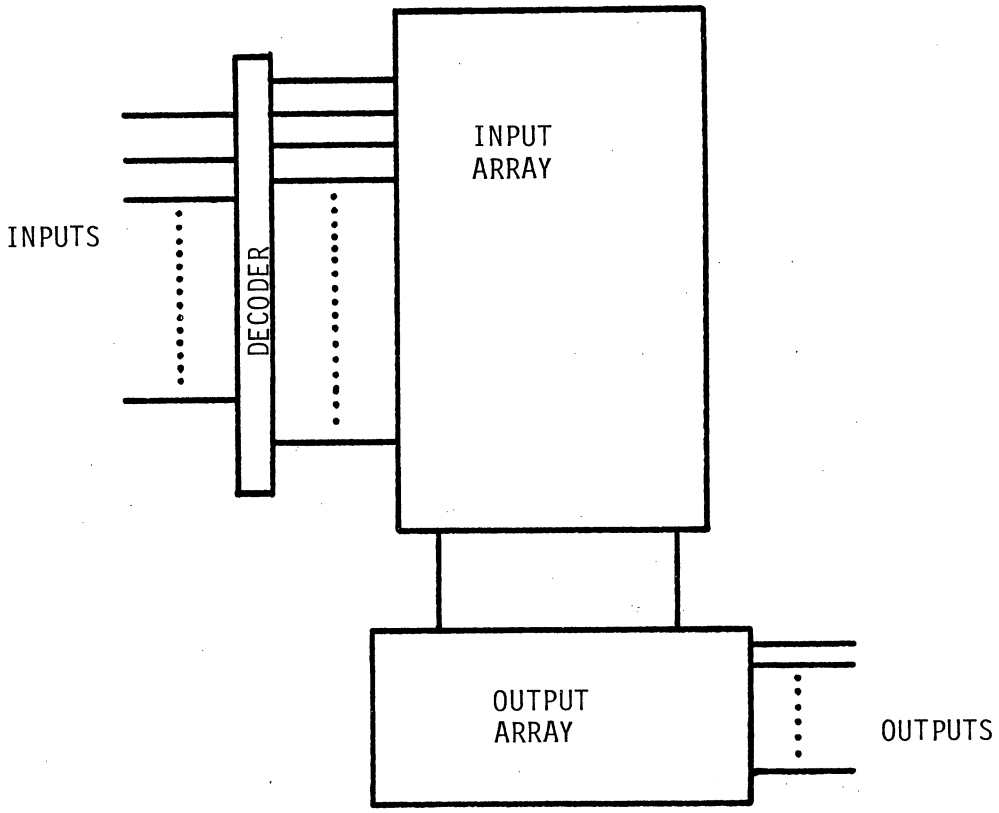


Figure 4. A Typical PLA

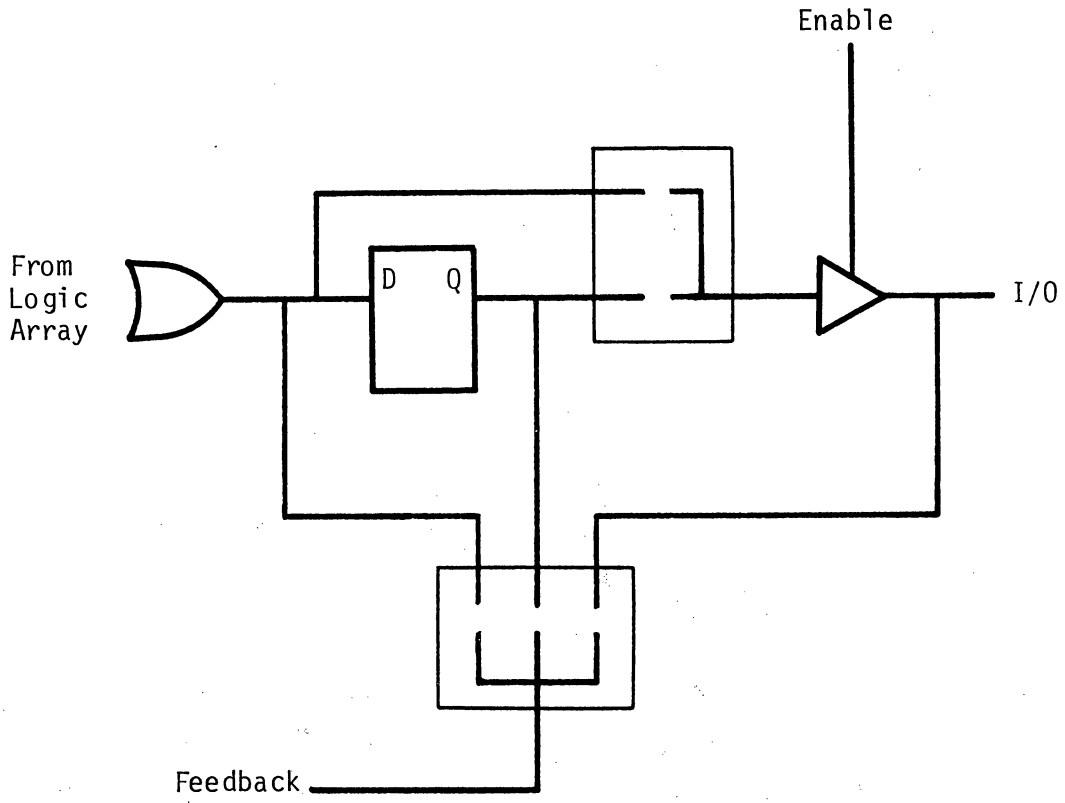


Figure 5. General Output Cell

PLAs. However, when flip-flops are included on the output or there is feedback, the flip-flop value or the feedback value needs to be known or present before each test.

In this discussion the word feedback will be used to describe any output value routed into the input of some other portion of the EPLD, not necessarily back into the same macrocell. If true feedback is meant, it will be stated as feedback into the same macrocell.

For testing purposes it is important to have flip-flops that can be preset to the desired value. This capability is very helpful when the flip-flop output value is fed back into some part of the circuit. The feedback value may not be the flip-flop value, but the sum of products value which would require the inputs set for the desired output for feedback and also for the test on the next portion of the circuit. This condition places so many requirements on the inputs that it is often not possible to find inputs to meet them all. Thus, some configurations prevent testing for all possible faults.

A similar problem is the programmable tri-state output enable. To read the output of a test the enable must be active or the value of the output stored in the flip-flop and then the tri-state enabled. If the input pattern required to enable the tri-state contradicts the test inputs then it may be necessary to use the I/O line which is the normal output for the circuit as the input for the feedback value. Then the tri-state can be enabled after the test to read the test output if the feedback was to the same macrocell.

3.1 Output Configuration

The options on the output need to be looked at individually to

present a complete testing procedure. Each of the output configurations is presented and then each one is discussed for testing purposes afterwards. The general output cell shown in Figure 5 was used as the guide. Figures 6 through 11 show the output configurations for each of the six possible selections. Figures 12 and 13 show the output configurations if an input latch is added to the input path for the I/O line.

Figure 6 shows the case of sequential output with combinational feedback. The output must be clocked through the flip-flop and the output enabled for the function value to be observed at the I/O pin. The combinational result is fed back immediately without the need of a clock pulse.

The second case, shown in Figure 7 has sequential output and sequential feedback. The output can be seen as in the previous case when the input is set followed by a clock pulse and the output enabled. The only difference in this structure is the position of the feedback. The value fed back is now the output of the flip-flop.

Sequential output with output feedback is shown in Figure 8. In this case the output is seen in the same way as in the previous two cases, but now the feedback is from the I/O line itself. The feedback path could be used for just that, or it could be used for an input, depending on the state of the enable.

Figure 9 shows the case of combinational output with combinational feedback. In this case the output can only be seen if the tri-state output is enabled while the inputs for the test are still valid. As in some of the previous cases, the requirement that the tri-state be enabled restricts the allowable inputs. Like the earlier combinational

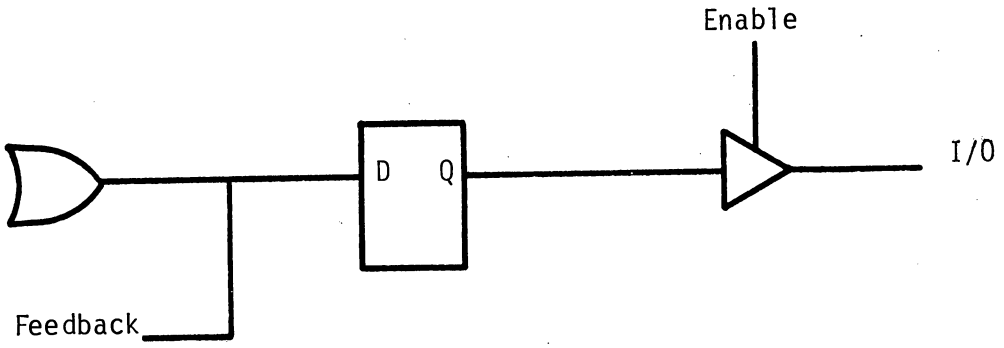


Figure 6. Sequential Output, Combinational Feedback

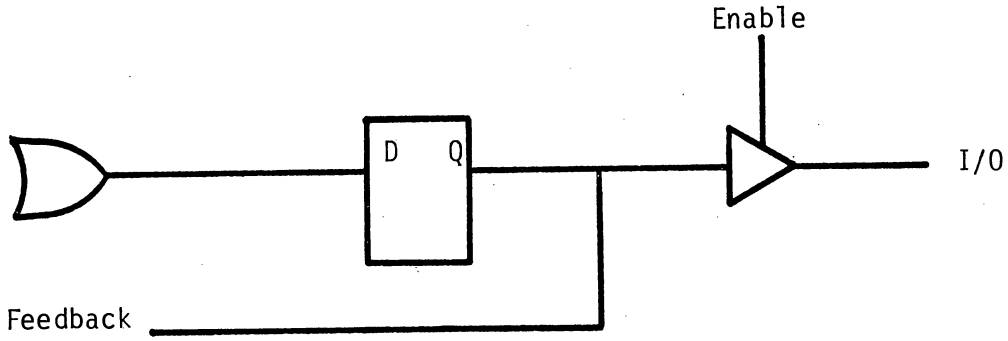


Figure 7. Sequential Output, Sequential Feedback

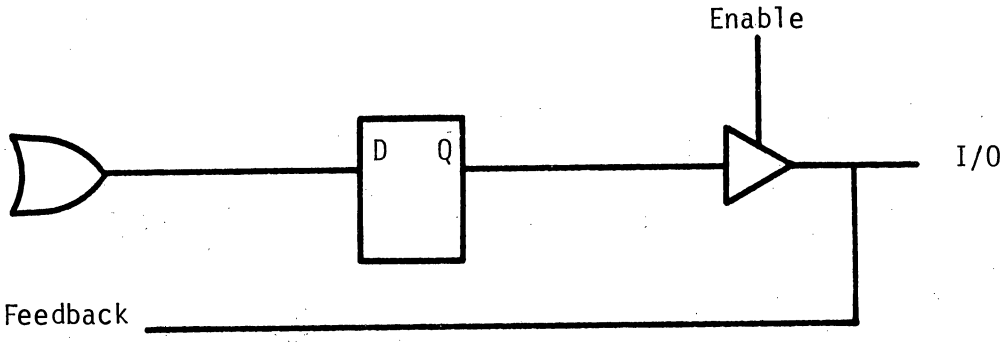


Figure 8. Sequential Output, Output Feedback

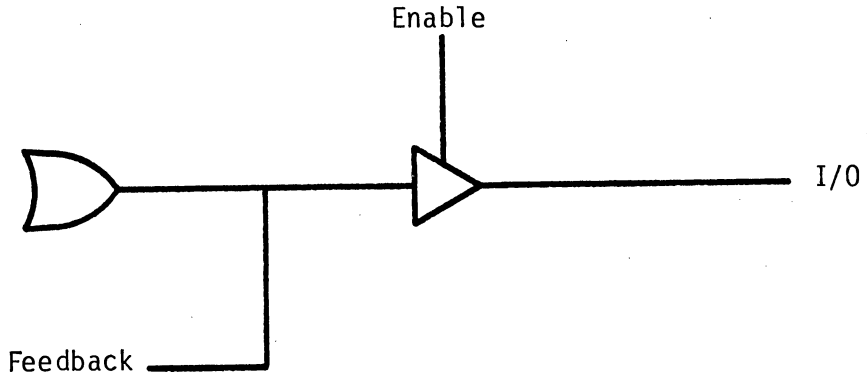


Figure 9. Combinational Output, Combination Feedback

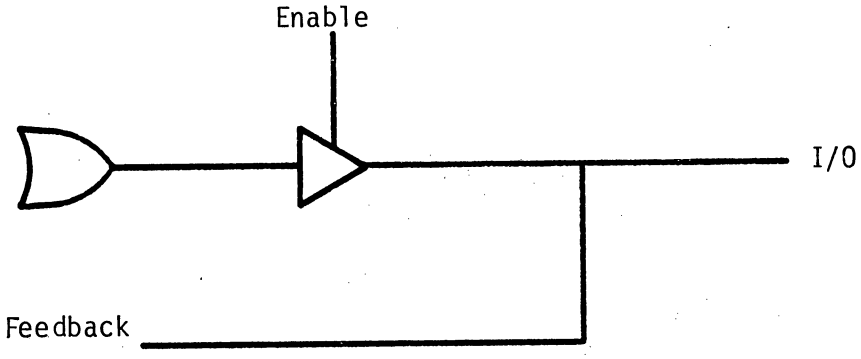


Figure 10. Combinational Output, Output Feedback

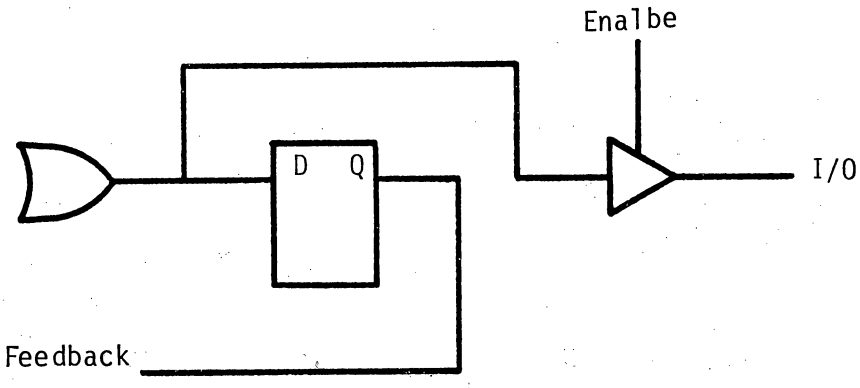


Figure 11. Combinational Output, Sequential Feedback

feedback case, the feedback value is the output of the sum of products array.

The output configuration shown in Figure 10 has a combinational output with output feedback. In this case the output is identical to that in Figure 9. however, the feedback is different. The feedback is once again from the macrocell output. Therefore, the feedback path could be used as another input instead of using the macrocell for output.

Figure 11 shows the case of combinational output with sequential feedback. The output can be seen as in the previous two configurations. The feedback is the output of the flip-flop even though the flip-flop is not used for the macrocell output. For this configuration, the clock pulse is only needed to propagate the combinational function result through the flip-flop for feedback.

Figure 12 is identical to Figure 10 with the addition of an input latch in the feedback path. The output is not affected by the change, but the latch must now be enabled to validate the feedback value. Unlike the flip-flops used for sequential operation, the latch requires the desired feedback value to be present at the input of the latch at all times that the latch is enabled. This requirement may or may not be a consideration but is merely presented as the difference in the previous cases and this one.

Figure 13 is identical to Figure 8 except for the added input latch. Once again the output path is not changed, but the input latch must be enabled for the feedback value to be validated.

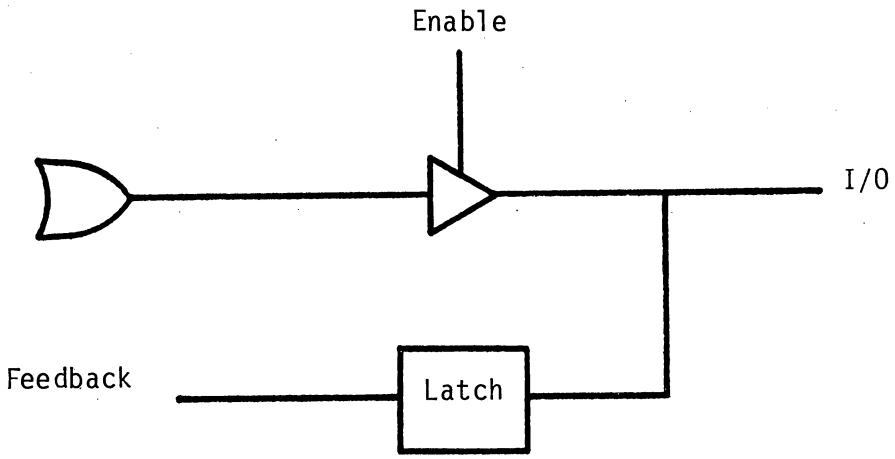


Figure 12. Combinational Output, Latched Feedback

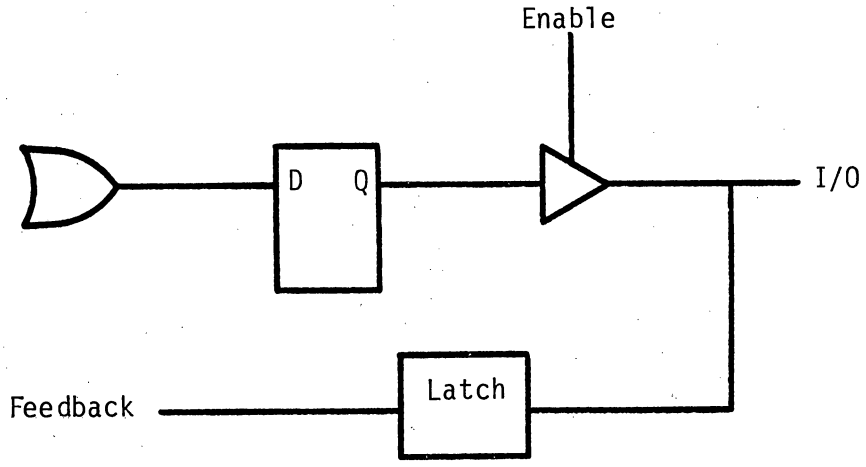


Figure 13. Sequential Output, Latched Feedback

3.2 PLA Test Modifications

As discussed in many other papers[4-11,14], the efficient testing of array patterns requires a close look at the circuit layout. Because of the similarities between PLAs and EPLDs, the most efficient approach to EPLD testing procedures is to begin with a PLA test generation algorithm and detail the changes required to make an EPLD test program. Each of the different output configurations described earlier presents a different set of problems. They are discussed separately in the same order used before.

The case of sequential output with combinational feedback was shown in Figure 6. If true feedback is present (the feedback value is used as an input in the same macrocell), then the feedback value is always equal to the combinational result. If the normal combinational logic is used, meaning the combinational logic can be described as a NOR-NOR two level circuit, then crosspoints meant to be connected which are activated by a 0 on the feedback path cannot be tested. The crosspoint cannot be tested because testing for the absence of the crosspoint requires the crosspoint to be activated. Placing a logical 1 on the crosspoint produces a 1 on the combinational output (given the line as the only one activated so its effect can be seen at the output). This value is different than the feedback value needed to activate the crosspoint, so an unstable condition is present and the test output cannot be held for observation. A similar condition is present for circuits using an inverted combinational circuit which could be described by a two level NOR-OR combination. The difference is that crosspoints to be made which are activated by a 1 on the feedback path cannot be tested. In both cases the feedback value is not the same as the output it produces. If

true feedback is not present then the tests for a similar PLA combinational circuit will test all possible faults in the EPLD.

In all cases the test generation routine must be free to set each input to a macrocell to the desired inputs for each test. If an input to one macrocell is the output from another macrocell then the output used must be first set to the desired value along with the other inputs for the test. In some cases the inputs required to set the value received from the other macrocell will contradict those needed for the test. For example, consider the situation where to macrocells with sequential output and combinational feedback are interconnected. Each one has the same logic function except for one input. The first macrocell used all primary inputs while the second macrocell uses the feedback from the first macrocell as one of its inputs. If the inputs required to set the output value on the first macrocell for the desired value to be used in the test of the second macrocell contradict in even one input required for the remainder of the second macrocell test then the test is not possible. So, in EPLD tests the restriction is present that not all tests may be possible because of contradictory inputs needed. From here on this requirement will be understood as a given restriction.

The case of sequential output with combinational feedback also has another possible complication. If the inputs required for the test do not contradict the output being enabled then the test can be run as follows. First, the test inputs are set to the desired values. Second, the clock must be pulsed to validate the output of the flip-flop. Third, the value of the output may be compared to the fault-free output desired. If the enable requires inputs not compatible with the test

inputs, then the inputs must be changed to those needed to enable the output, and finally, the output may be observed.

Sequential output with sequential feedback shown in Figure 7 has much fewer problems in testing. If true feedback is present then the flip-flop output Q can be preset to the feedback value desired. If the preset is not used, then the feedback value could be set by setting up the appropriate inputs to give the desired output, and the value clocked to the Q on the flip-flop. Then the inputs may be set for the test. At this point all the inputs are valid, and the output from the combinational part of the circuit is at the input to the flip-flop. Then the clock must be pulsed to validate the output through the flip-flop. Now, the value of the feedback does not matter because the output from the test is stored and the combinational circuit is not longer important for the test. Then, if the inputs required for the enable are not compatible with those of the test then the inputs must be changed to enable the output. Otherwise, the output is already valid for the test pattern just used. If true feedback is not used, the test procedure is the same as with true feedback without the need to preset Q.

The output configuration in Figure 8, sequential output with output feedback, requires many more considerations. If true feedback is used, there are three ways to set the feedback. If the output can be enabled with the test inputs set, then the Q may be preset to the desired feedback value. If the output can be enabled with the test inputs set and the Q is not preset, then the inputs may first be set to give the feedback value as the output, and the clock pulsed to set Q. If the enable cannot be set at the same time that the test inputs are set, then the only way to set the feedback value is to use the I/O pin as an input

for the value desired. For the first case (Q preset), the test inputs must be set and then the clock pulsed to allow the test output to be observed. In the second case, the Q must be loaded first, the test inputs set, the clock pulsed, and then the test output may be observed. In the third case, where the output is not enabled while the test inputs are valid, the test procedure is a little longer. First, the test inputs must be set. Then, the I/O pin must be set to the desired feedback value. Third, the clock must be pulsed to save the combinational circuit output. Then the I/O pin must be freed from input by removing the controlled feedback value. Fifth, the inputs may be changed to enable the output, and last, the output may be observed. if true feedback is not present, the only problem is the output enable. If the output is not enabled during the test, then the inputs must be changed after the test result has been clocked into the Q of the flip-flop. If the output is enabled during the test, then the test output need only be clocked to the output of the flip-flop to be observed.

Figure 9 shows one of the most restrictive output configurations for feedback; combinational output with combinational feedback. If true feedback is used, then only those tests which produce the same output as the feedback value needed for input may be run. The reason is that the only way to set the feedback value is through the combinational circuit output of the macrocell. If true feedback is used, then one must again look at the output enable. If the output is enabled during the test, then the output may be observed. However, if the output cannot be enabled during the test then there is no way to observe the output from the test. There is no way to hold the output while the output is enabled. So, for this configuration with true feedback, the only possible

tests are those with the same valued output and feedback with the output enabled while the test inputs are set. If true feedback is not used, then the only restriction is the requirement that the output be enabled during the test. If the output cannot be enabled while the test inputs are valid, then the test output cannot be seen.

The case of combinational output with output feedback, shown in Figure 10, is a little less restrictive. If true feedback is used the same restrictions are present as those discussed for the case of combinational output and combinational feedback. The requirements for observable tests are those with output equal to the feedback value used, with the output enabled while the test inputs are valid. If true feedback is not used then the only tests possible are still those which can have the output enabled during the test. The advantage of this configuration over the last one is that the feedback value can be set by using the I/O line as an input if the feedback value is used by another macrocell and the output can be disabled during the test. If the test inputs for another macrocell using the feedback from this cell cause the output to be enabled, the only way to assign a value to the feedback is to set the inputs to give the desired feedback value on the output. If the test inputs on the other macrocell cannot be set at the same time as the inputs are set for the feedback value, then the test is impossible.

The output configuration shown in Figure 11, combinational output with sequential feedback, only uses the flip-flop for feedback. If true feedback is used, then the feedback value may be set by presetting the Q to the desired value. If the preset is not used, then the inputs must be set to produce the same output value as the feedback value needed, and the result clocked through the flip-flop to load Q. With the

feedback value set, the only test restriction, a result of the output not being saved, is that the only observable test results are those which can enable the output while the test inputs are valid. Since the output is combinational, the clock need not be pulsed to propagate the output. So, to test with true feedback, the feedback value must be set by one of the two methods mentioned, and then the inputs set to the test values. If true feedback is not used then again only those tests which can allow the output to be enabled while the test inputs are set may be observed.

Figure 12 shows the same output configuration as Figure 10, with the added latch on the feedback path. This case of combinational output with latched feedback removes one of the restrictions of the case where there was only output feedback. The test output is not required to be the same as the desired feedback value. Using true feedback, the feedback value may be set by disabling the output, setting the I/O pin to the value of the feedback, pulsing the latch enable, and removing the I/O value. Then the other test inputs may be set for the desired test. There is still the requirement that the output must be enabled during the test, or the test result cannot be observed. This restriction is also true for the case where true feedback is not present.

Sequential output with latched feedback, shown in Figure 13, removes some of the restrictions experienced for the case of sequential output with output feedback, shown in Figure 8. In this case, the feedback value may be set by disabling the output, setting the I/O value to the feedback desired, and pulsing the latch enable. Otherwise, the Q must be set by preset, or clocking through a value, the output enabled, and then the latch enable pulsed. All other considerations are the same

as those discussed with reference to Figure 8.

CHAPTER IV

SUMMARY AND CONCLUSIONS

The EPLD testing problems are a result of the conflicts in the necessary input values to conduct the tests. The most frequent problem is the conflict between the combinational tri-state output enable and the sum-of-products test patterns. If the enable logic were done using mutually exclusive inputs from the inputs used in the rest of the EPLD then the conflicts would be eliminated. The other major problem is combinational feedback. The requirements to set the inputs for one sum-of-products to produce the feedback value used for another or the same macrocell is too much to allow adequate coverage of possible faults with the nonconflicting input combinations remaining. The only possible efficient test would look at the four level logic function resulting from the combination of macrocells connected by combinational feedback links. Then, one must deal with the increase of untestable faults as a result of the higher order function. Most other problems are a result of the inconvenience of having to clock values through at the appropriate time. With the control of the feedback path the EPLD can be tested with the same test patterns used for testing a similar PLA.

4.1 ALTERA EP300, EP1200

This paper was written with the ALTERA EPLDs in mind. The output configurations discussed are all the possible geometries of the ALTERA

EP300 and EP1200. The data sheets for the two devices are included in Appendix A and Appendix B respectively. The input latches are only present in the EP1200 when the proper clocking schemes are selected. The EP1200 also does not have as many options for the basic output configuration. It does not have purely combinational feedback, but only combinational feedback through the output path.

The greatest problems in testing the ALTERA EP300 and EP1200 are in the EP1200 geometry. The shared product terms create a different consideration when generating test patterns. If one macrocell using the shared term combinationally feeds the second macrocell, then that whole shared term may only have one value if it is required to set the feedback. The other problem is the buried registers. The values in the buried registers must be set to the desired values by the preset or the appropriate input combination and the flip-flop clocked to lock in the value. Because of the clocking of values in other flip-flops for testing, the value of the buried register may need to be stored for each test. Other conflicts could arise if the inputs for more than one feedback value conflict. Then the tests would be limited to those that did not contradict each other, resulting in possible faults not being tested.

4.2 Recommendations

To make the EPLD circuits as testable as possible, a few objectives should be kept in mind. If at all possible, the enable should be activated using its own input or inputs not dependent on those used in the rest of the device. The use of combinational feedback should be avoided. If combinational feedback is necessary, it does help to use

output feedback so that the feedback value could be set using the output pin as an input. Macrocells with presettable flip-flops should be used over buried registers which are hidden from the device outputs. Other extra functions like shared terms may or may not prevent testing, but they do make testing more complicated for the most part. All of the recommendations if followed, may still not yield a completely testable EPLD design. However, they will help meet one of testing's chief aims, achieving the maximum fault coverage.

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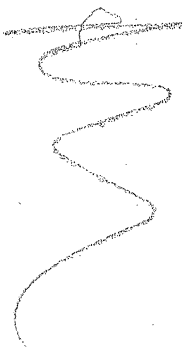
APPENDIXES



APPENDIX A

ALTERA EP300

EP300

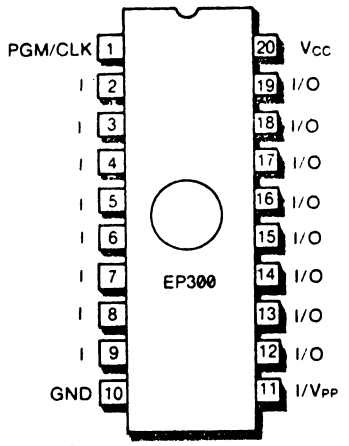
ERASABLE PROGRAMMABLE LOGIC DEVICE

FEATURES

- Programmable replacement for conventional fixed logic.
- EPROM technology allows reprogrammability, ensures high programming yield and ease of use.
- Second generation programmable logic architecture allows up to 18 inputs and 8 outputs.
- Each output is *User Programmable* for combinatorial or registered operation, in active high or low mode.
- Each output also has an independently *User Programmable* feedback path.
- Extra product terms provide a logical synchronous Preset and asynchronous Reset capability to all registers.
- Preload for more complete testability.
- Design Protection feature protects proprietary designs from competitors and protects the user from inadvertant programming.
- CMOS for low power, high reliability operation.
- Packaged in space saving (300 mil) 20 pin package.

CONNECTION DIAGRAM

FIG. 1

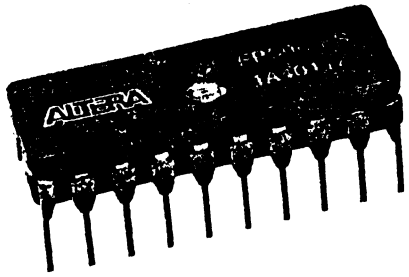


GENERAL DESCRIPTION

The ALTERA EP300 combines the power flexibility, and density advantages of CMOS, EPROM technology with second generation programmable logic array architecture. This combination defines a new capability in electrically programmable logic. The EP300 utilizes the familiar sum-of-products architecture which allows users to program complex custom logic functions quickly and easily. Up to 18 inputs and 8 outputs are provided, with eight product terms and a separate Output Enable term for each output.

A unique feature of the EP300 is the ability to program each output architecture on an individual basis. This gives the user the flexibility to assign either combinatorial or registered output, in either active high or active low mode, to each output pin. In addition, the feedback path can be programmed independently of the output to be either combinatorial, registered, or I/O.

The ALTERA EP300 features a Synchronous Preset and Asynchronous Reset capability to all output registers, along with automatic power-up reset. Another unique feature of the EP300 is the ability to preload output registers to any desired state. This capability is essential to permit full logical verification during testing.



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REV. 3.1

ALTERA EP300 ERASABLE PROGRAMMABLE LOGIC DEVICE

FUNCTIONAL DESCRIPTION

A block diagram of the EP300, along with logic diagrams of the I/O Architecture Control function and the Logic Array Macrocell are shown in figures 2 through 6. The EP300 is organized in the familiar sum-of-products format with a total of 74 product terms and 36 input lines.

At each intersecting point in the logic array, there exists an EPROM type programmable connection. Initially, all connections are made. This means that both the true and complement of all inputs are connected to each product term. Connections are opened during the programming process. Therefore any product term can be connected to the true or complement of any input. When both the true and complement connections of any input are left intact, a logical false results on the output of the AND gate. If both the true and complement connections of any input are programmed open, then a logical "don't care" results for that input. If all inputs for a product term are programmed open, then a logical true results on the output of the AND gate.

A dramatic improvement in the flexibility of programmable logic is achieved in the ALTERA EP300 through programmable I/O architecture. Each output can be combinatorial (i.e. direct output of the OR gate) or registered (i.e. output through a D type flip-flop). Both types of output can also be inverted. Independent of the output mode, the feedback can be programmed to be combinatorial, registered, I/O (i.e. directly from the pin), or none. These features enable the user to optimize the device for precise application requirements.

To improve functionality, the ALTERA EP300 has additional Synchronous Preset and Asynchronous Reset product terms. These terms are connected to all D-type Flip-Flops. When the Synchronous Preset product term is asserted (HIGH), the output register will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset product term is asserted (HIGH), the output register will immediately be loaded with a LOW (independent of the clock). An Asynchronous Reset overrides a Synchronous Preset request. On power-up, the EP300 performs the Reset function automatically.

The EP300 is manufactured using a CMOS EPROM process. This advanced process, along with built in test features, allows 100% pre-test of each programmable connection at the factory.

Using EPROM technology provides a logic chip concept which up until now was unheard of — *Reprogrammable* Custom Logic. In the past, regardless of whether the user chose full custom, standard cell, gate array, PROM's, FPLA's, or fuse programmable logic devices, once the custom pattern was integrated into a chip, it was not alterable. In contrast when using the EP300 the same chip can be erased and reprogrammed to correct programming mistakes, updates, or design changes.

FIG. 2 LOGIC ARRAY MACROCELL

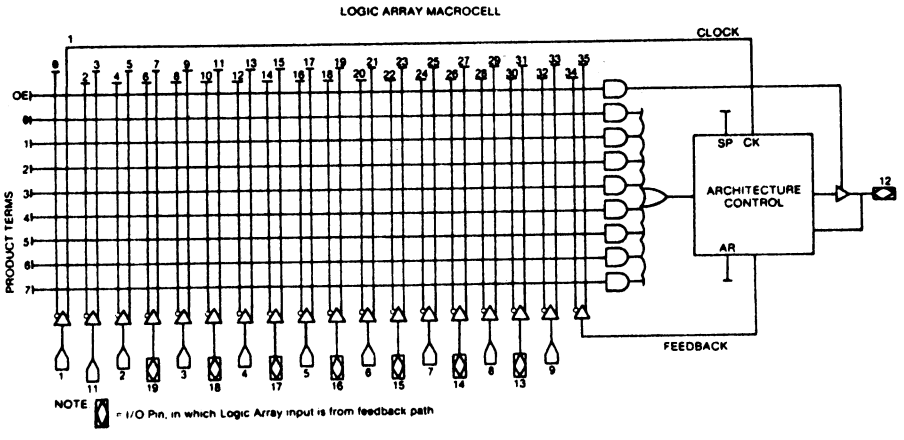
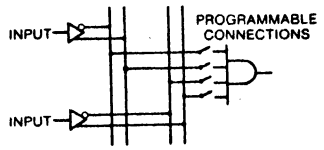
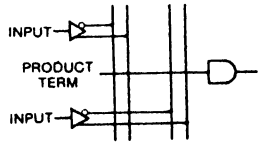


FIG. 3 KEY TO LOGIC ARRAY MACROCELL DIAGRAM



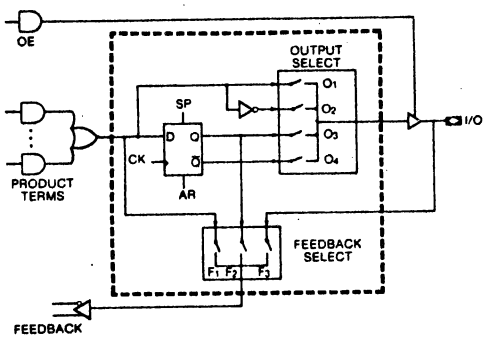
Equivalent Logic Diagram



Logic Array Representation

NOTE: All programmable connections are CLOSED after UV erase

FIG. 4 I/O ARCHITECTURE CONTROL



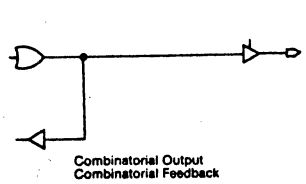
O_1	O_2	O_3	O_4	F_1	F_2	F_3	OUTPUT	FEEDBACK
I	O	O	O	I	O	O	Combinatorial/High	Combinatorial ★
I	O	O	O	O	I	O	Combinatorial/High	Registered ★
I	O	O	O	O	O	I	Combinatorial/High	I/O
O	I	O	O	I	O	O	Combinatorial/Low	Combinatorial
O	I	O	O	O	I	O	Combinatorial/Low	Registered
O	I	O	O	O	O	I	Combinatorial/Low	I/O ★
O	O	I	O	I	O	O	Registered/High	Combinatorial
O	O	I	O	O	I	O	Registered/High	Registered ★
O	O	I	O	O	O	I	Registered/High	I/O ★
O	O	O	I	I	O	O	Registered/Low	Combinatorial ★
O	O	O	I	O	I	O	Registered/Low	Registered
O	O	O	I	O	O	I	Registered/Low	I/O
n	n	n	n	O	O	O	any of above	none
O	O	O	O	m	m	m	none	any of above

I = Connection Closed
O = Connection Open
nnnn = Any Legal Output Configuration
mmm = Any Legal Feedback Configuration

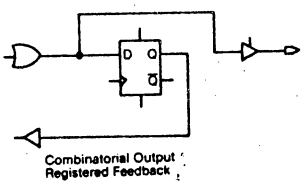
★ Configurations shown in fig. 5

NOTE: All programmable architecture connections are OPEN after UV erase

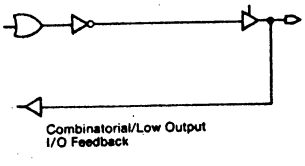
FIG. 5 EXAMPLE I/O CONFIGURATIONS



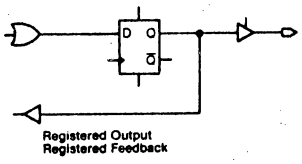
Combinatorial Output
Combinatorial Feedback



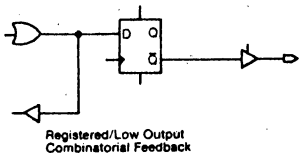
Combinatorial Output
Registered Feedback



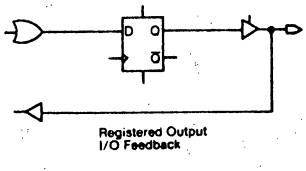
Combinatorial/Low Output
I/O Feedback



Registered Output
Registered Feedback

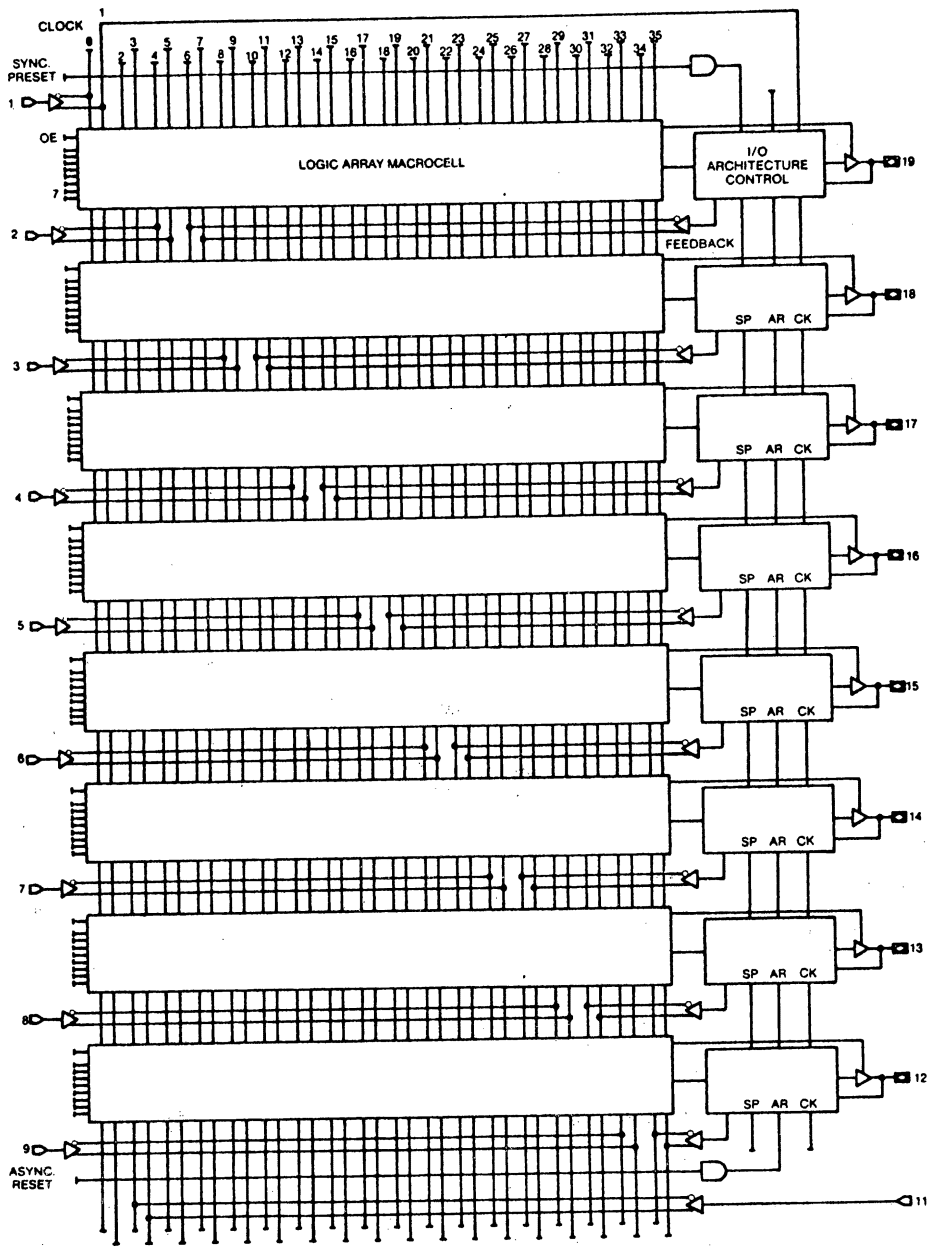


Registered/Low Output
Combinatorial Feedback



Registered Output
I/O Feedback

FIG. 6 EP300 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS — EP300, EP300-1, EP300-2, EP300-3

SYMBOL	PARAMETER	CONDITIONS	LIMITS	UNITS
V_{CC}	Supply voltage	With respect to GND	-0.3 to 6	V
V_{PP}	Supply voltage		-0.3 to 22	V
V_I	Input voltage		-0.3 to 6	V
V_O	Output voltage		-0.3 to 6	V
T_{stg}	Storage temperature		-55 to +125	°C

DC OPERATING CHARACTERISTICS — EP300, EP300-1, EP300-2

(T_A = 0°C to 70°C, V_{CC} = 5V±5%) note (1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input leakage current	V_{IN} = V_{CC} or GND	-10		10	µA
I_{OZ}	Output leakage current	V_{OUT} = V_{CC} or GND	-10		10	µA
I_{CC1}	V_{CC} supply current (standby)	V_{IN} = V_{CC} or GND		25	35	mA
V_{IL}	Input LOW voltage		-0.3		0.8	V
V_{IH}	Input HIGH voltage		2.2		V_{CC}+ 0.3	V
V_{OL}	Output LOW voltage	I_{OL} = +4.0mA			0.45	V
V_{OH}	Output HIGH voltage	I_{OH} = -4.0mA	2.4			V

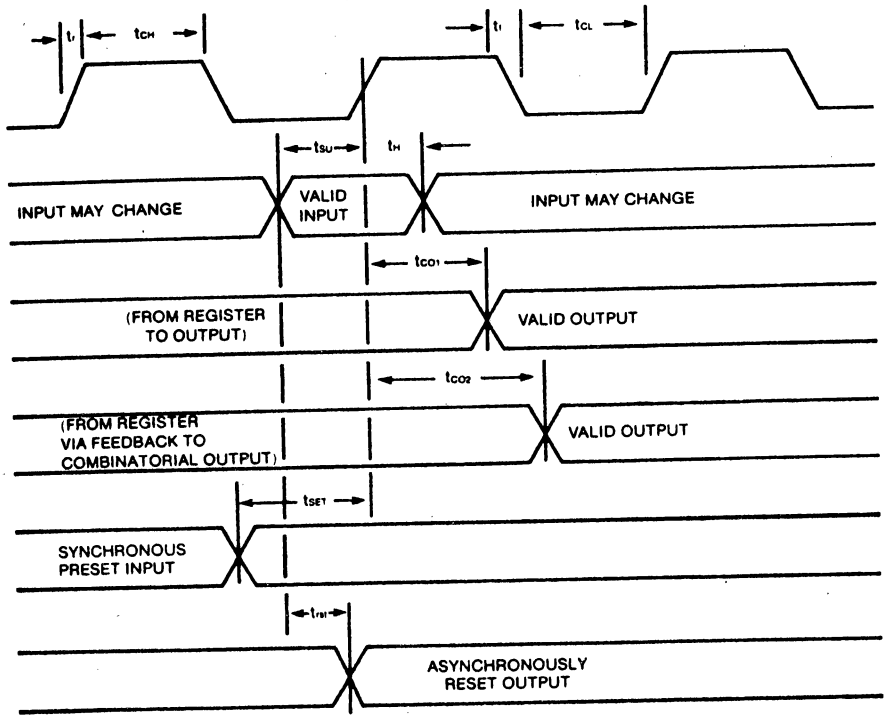
AC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V±5%) note (1)

			EP300-1			EP300-2			EP300			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{PD}	Input or I/O input to non-registered output	fig 9			35			65	25	60	90	ns
t_{pzx}	Input or I/O input to output enable	C_1 = 30pF			35			65		60	90	ns
t_{pxz}	Input or I/O input to output disable	fig 9 C_1 = 5pF note 2			35			65		60	90	ns
t_{SU}	Input or I/O input setup time		28			47			62	45		ns
t_H	Input or I/O input hold time		0	-15		0	-15		0	-15		ns
t_{CH}	Clock high time		20			25			30	20		ns
t_{CL}	Clock low time		20			25			30	20		ns
t_{CO1}	Clock to output delay time	fig 9			22			33		25	38	ns
t_{P1}	Minimum clock period (register output feedback to register input via internal path)				30			55		50	75	ns
f_1	Maximum frequency ($1/t_{P1}$)	C_1 = 30pF	33.3			18.2			13.3	20.0		MHz
t_{P2}	Minimum clock period ($tSU + tCO_1$)				50			80		70	100	ns
f_2	Maximum frequency ($1/t_{P2}$)		20.0			12.5			10.0	15.0		MHz
t_{set}	Synchronous preset input set-up time		28			47			62	45		ns
t_{rst}	Asynchronous output reset time delay				35			65	20	45	90	ns
t_{CO2}	Registered feedback through PLA to output. Relative to external clock				45			75		70	100	ns
I_{CC2}	V_{CC} supply current (active)	No load. f = 10MHz			50			40		25	40	mA

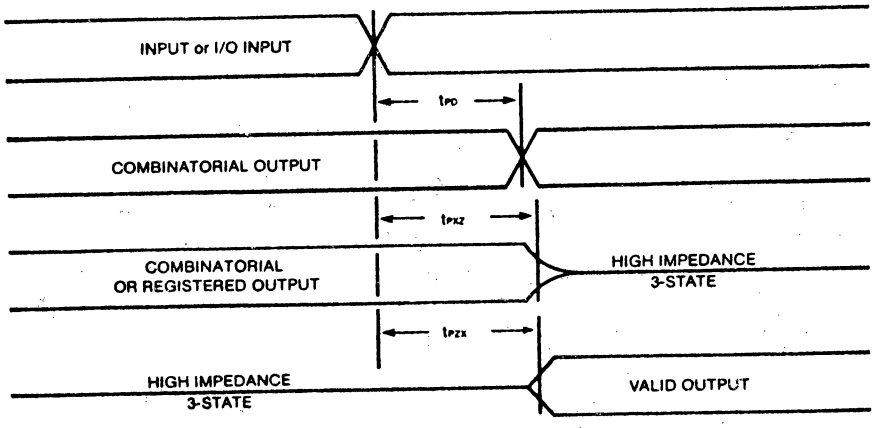
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only, for an output change of 500mV.

FIG. 7 SWITCHING WAVEFORMS



NOTES: t_r & t_f = 6ns
t_{CL} & t_{CH} measured at 0.3v & 2.7v
all other timing at 1.3v

FIG. 8 SWITCHING WAVEFORMS



LOW VOLTAGE OPERATION

DC OPERATING CHARACTERISTICS EP300-3

(T_A = 0°C to 70°C, V_{CC} = 3.0 to 4.5v) note (1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input leakage current	V_{IN} = V_{CC} or GND	-10		10	µA
I_{OZ}	Output leakage current	V_{OUT} = V_{CC} or GND	-10		10	µA
I_{CC1}	V_{CC} supply current (standby)	V_{IN} = V_{CC} or GND		10		mA
V_{IL}	Input LOW voltage		-0.3		$0.15V_{CC}$	V
V_{IH}	Input HIGH voltage		$0.75V_{CC}$		V_{CC}+ 0.3	V
V_{OL}	Output LOW voltage	I_{OL} = +100µA			0.1	V
V_{OH}	Output HIGH voltage	I_{OH} = -100µA	V_{CC}-0.1			V

AC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 3.0 to 4.5v) note (1)

			EP300-3			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Input or I/O input to non-registered output	fig 10			300	ns
t_{pzx}	Input or I/O input to output enable	C_1 = 30pF			300	ns
t_{pxz}	Input or I/O input to output disable	note 2 fig 10 C_1 = 5pF			300	ns
t_{SU}	Input or I/O input setup time		200			ns
t_H	Input or I/O input hold time		0			ns
t_{CH}	Clock high time		100			ns
t_{CL}	Clock low time		100			ns
tCO	Clock to output delay time	fig 10			150	ns
t_{P1}	Minimum clock period (register output feedback to register input via internal path)	C_1 = 30pF			250	ns
f_1	Maximum frequency ($1/t_{P1}$)		4.0			MHz
t_{P2}	Minimum clock period (tSU + tCO_1)				350	ns
f_2	Maximum frequency ($1/t_{P2}$)		2.8			MHz
t_{set}	Synchronous preset input set-up time		200			ns
t_{rst}	Asynchronous output reset time delay				250	ns
t_{CO2}	Registered feedback through PLA to output. Relative to external clock				350	ns
I_{CC2}	V_{CC} supply current (active)	No load. f = 1MHz		15	30	mA

1. Typical values are for T_A = 25°C, V_{CC} = 3V
2. Sample tested only, for an output change of 500mV

FIG. 9 AC TEST CONDITIONS

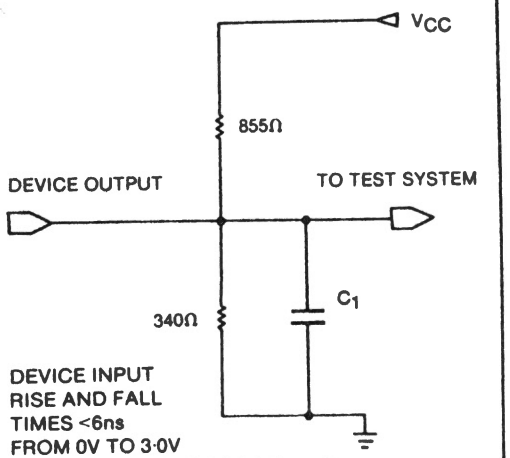
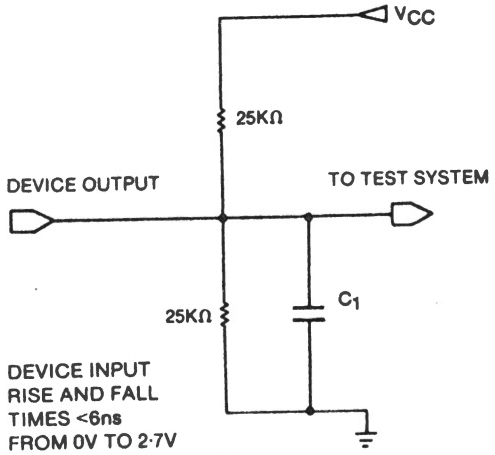


FIG. 10 AC TEST CONDITIONS



PROGRAM ERASURE

The erasure characteristics of the EP300 are such that erasure of the programmed connections begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms. It is important to note that sunlight and certain fluorescent lighting could erase a programmed EP300 since they have wavelengths in the range of 3000 to 4000 Angstroms. Extrapolated results suggest that constant exposure to room level fluorescent lighting could erase an EP300 in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. As a consequence if the EP300 is to be exposed to these types of lighting conditions for extended periods of time then opaque labels should be placed over the EP300 window to prevent unintentional erasure.

The recommended erasure procedure for the EP300 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms. The integrated exposure dose for erasure should be a minimum of 15 W sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EP300 should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated exposure dose that an EP300 can be exposed to without damage is 7000 Wsec/cm^2. This is approximately one week at 12000 μW/cm^2. Exposure of the EP300 to high intensity UV light for long periods may cause permanent damage.

FUNCTIONAL TESTING

The EP300 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements.

As a result traditional problems associated with the programming yield of fusible programmable logic circuits are avoided.

Additionally, to assist rapid testing of the EP300, a special test pre-conditioning mode is available.

This mode is entered by raising pin 9 to V_{HH} and controlling data pre-conditioning with pin 1 (see figure 11). The pre-conditioning mode permits any of the states that the EP300 could attain to be reached directly without the need for extensive input sequences to attain the desired state.

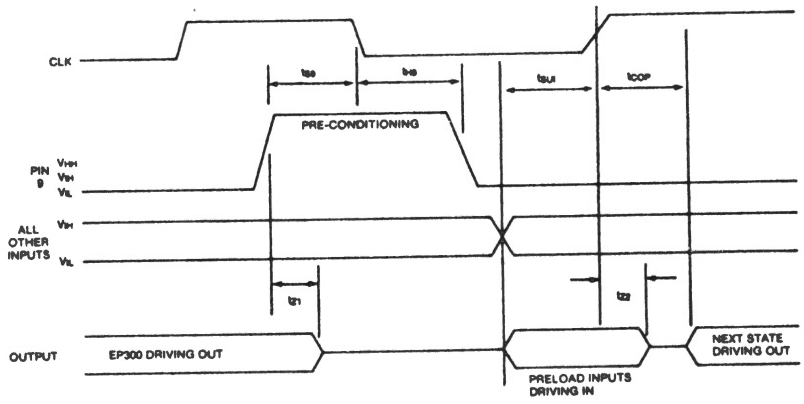
PRECONDITIONING MODE

A.C. CHARACTERISTICS

(T_A = 0° C to 70° C, V_{CC} = 5V±5%) V_{HH} = 21V ± 0·5V)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{S9}	Setup time of Pin 9 going to V_{HH} with respect to Clock falling edge			100		ns
t_{H9}	Hold time of Pin 9 (going from V_{HH} to V_{IL} or V_{IH}) with respect to Clock falling edge			0		ns
t_{SUI}	Setup time of all preload inputs with respect to Clock rising edge			100		ns
t_{COP}	Output delay time (Register to output) after Clock rising edge			100		ns
t_{Z1}	Output 3-state delay time after assertion of Pre-load (Pin 9 = V_{HH})			200		ns
t_{Z2}	3-state delay time of external device driving in after clock rising edge			15		ns

FIG. 11 PRECONDITIONING WAVEFORM



DESIGN SECURITY

The EP300 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used a proprietary design implemented in the device cannot be copied nor retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

PROGRAMMING DEVELOPMENT TOOLS

The EP300 is supported by an advanced programming development system that facilitates accurate and rapid product development.

The software system, known as A+PLUS, is the Altera Programmable Logic User System which supports multiple design entry techniques that include:

- Schematic diagram entry . . . PC-CAPS, DASH-2
- Interactive netlist entry . . . NetMap
- Boolean equation entry . . . NetMap

The typical development environment used for this software would be an IBM Personal Computer and equivalent machines with the following configuration:

- Dual floppy disk drive or hard disk drive
- MS-DOS operating system version 2.0 or later release
- 384K memory
- Altera device programming card and unit

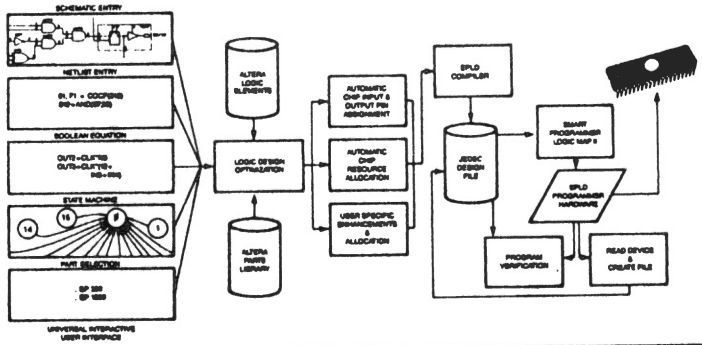
The output of A+PLUS is a data file in a standard JEDEC format. The EP300 can then be programmed using the programming card.

DESIGN RECOMMENDATIONS

Operation of devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating condition for extended periods may affect device reliability. These devices contain circuitry to protect the input against damage to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that input and output pins be constrained to the range GND ≤ (Vin or Vout) ≤ Vcc. Unused inputs must always be tied to an appropriate logic level (e.g. either Vcc or GND).

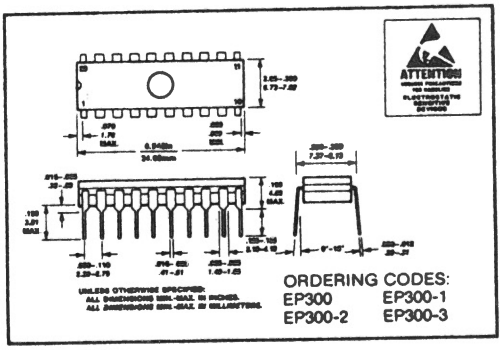
For optimum DC and AC performance all unused product terms should be programmed with all AND connections open excepting (any) two inputs and their associated complements.

FIG. 12



The EP300 is also supported by ABEL (Advanced Boolean Expression Language) which is available from DATA I/0 and by CUPL (Compiler for Universal Programmable Logic) from Assisted Technology. All of these development programs produce standard JEDEC data files that are compatible with a variety of programming hardware including ALTERA LogicMap; Stag Microsystem's PPZ and ZL30 products and DATA I/O's LogicPak with programming/test adapter 303A-009.

PACKAGE OUTLINE



ORDERING CODES:
EP300 EP300-1
EP300-2 EP300-3

ALTERA DISTRIBUTORS

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Address	City	State	Zip	Telephone
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840 Fairport Park	Fairport	NY	14450	716 381 7070
1551 Carmen Drive	Elk Grove Village	IL	60007	312 437 9680
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1806 Vestal Parkway East	Vestal	NY	13850	607 748 8211
13485 Stamford	Livonia	MI	48150	313 525 1800
5853 Point West Drive	Houston	TX	77036	713 988 5555
1207 Putnam Drive NW	Huntsville	AL	35805	205 837 9300
221 North Lake Blvd.	Altamonte Springs	FL	32701	305 834 9090
13710 Omega Road	Dallas	TX	75244	214 386 7300
261 Gilbralter Road	Horsham	PA	19044	215 674 4000
10203 Bren Road East	Minnetonka	MN	55343	612 935 5444
1500 Northwest 62nd Street	Fort Lauderdale	FL	33309	305 771 7520
9901 Burnet Road	Austin	TX	78758	512 835 4000
6408 Castleplace Drive	Indianapolis	IN	46250	317 849 7300
44 Hartwell Avenue	Lexington	MA	02173	617 861 9200
259 Kappa Drive	Pittsburg	PA	15238	412 782 2300
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60 Crossways Park West	Woodbury	NY	11797	516 921 8700

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Jericho Turnpike	Westbury	NY	11590	516 334 7474
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3 Town Line Circle	Rochester	NY	14623	716 424 2222
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21139 Victory Blvd.	Canoga Park	CA	91303	818 999 4702
1000 R.I.D.C. Plaza Suite 203	Pittsburgh	PA	15238	412 782 1600
90 E. Tasman Dr.	San Jose	CA	95134	408 946 7171
11049 N. 23rd Drive Suite 100	Phoenix	AZ	85029	602 997 4874
25 Wiggins Ave.	Bedford	MA	01730	617 275 5100
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18 Madson Road	Fairfield	NJ	07006	201 227 7880
9330 Gaither Road	Gaithersburg	MD	20877	301 840 5900
4202 Beltway Drive	Dallas	TX	75234	214 661 5010
6750 Nancy Ridge Dr. Suite D & E, Bldg. 7	San Diego	CA	92121	619 450 0454
150 South Sunnyslope Road	Brookfield	WI	53005	414 784 9020
10300 W. 103rd Street Suite 200	Overland Park	KS	66214	913 492 2922
1771 Tribute Road Suite B	Sacramento	CA	95815	916 929 9732
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4815 South Sheridan Fountain Plaza Suite 109	Tulsa	OK	74145	918 622 8000
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1959 South 4130 West	Salt Lake City	UT	84104	801 974 9953
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237 Hymus Blvd. Pointe-Claire, Quebec, Canada	H9R 5C7	514 694 7710
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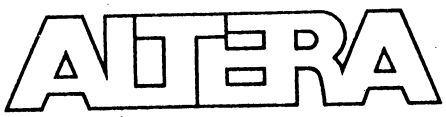

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APPENDIX B

ALTERA EP1200

EP1200 ERASABLE PROGRAMMABLE LOGIC DEVICE

FEATURES

- EPROM technology programmable LSI replacement for conventional fixed logic.
- Programmable Macrocell & I/O architecture: up to 36 inputs or 24 outputs, 28 Macrocells including 4 buried state registers.
- All inputs are latchable with a programmable latch feature.
- Low power: 15mW typical standby dissipation.
- Typical usable equivalent gate count of 1200 2-input NAND gates.
- Advanced architecture features including programmable output type (active high/active low), register by-pass and reset controls.
- Programmable clock system for input latches and output registers.
- Product-term sharing and local bus architecture for optimized array performance.
- Compatible with LS TTL and 74HC CMOS logic.
- Register pre-load and erasable array for 100% generic testing.

GENERAL DESCRIPTION

The Altera EP1200 is an LSI logic circuit that can be programmed to provide logic replacement for conventional SSI and MSI logic circuits.

The EP1200 contains CMOS EPROM (floating-gate) elements that control the logical operation of the device. The device can typically provide equivalent performance to 1200 gates of SSI and MSI logic. The EPROM technology enables the logic designer to rapidly program the device and make design changes after erasing for just a few minutes. The same technology also permits 100% factory testing of all elements within the device.

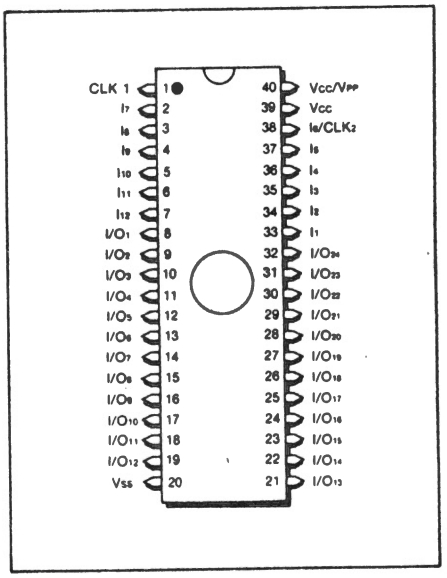
The CMOS technology reduces power consumption to less than 10% of equivalent bipolar devices without sacrificing speed performance.

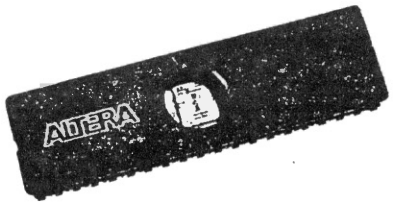
To implement general purpose logic the EP1200 contains the familiar sum-of-product PLA structure with a programmable AND and fixed OR array. The design uses a range of OR gate widths to accommodate logical functions without the overhead of unnecessary product-terms nor the speed penalties of programmable OR structures.

A segmented PLA design that provides local and global connectivity also optimizes the performance of the EP1200.

The EP1200 contains innovative architectural features that provide significant I/O flexibility and maximize performance within a conventional dual-in-line package.

CONNECTION DIAGRAM





PRELIMINARY DATA

NOTICE: THIS IS NOT A FINAL SPECIFICATION. SOME PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

ALTERA EP1200

ERASABLE PROGRAMMABLE LOGIC DEVICE

REV 1.1

FUNCTIONAL DESCRIPTION

The EP1200 is an LSI erasable programmable logic device (EPLD) which uses EPROM technology to configure connections within a programmable logic array. The device has a programmable I/O architecture that provides options to change inputs, outputs and logical function of the device.

The internal architecture is based on 28 Macrocells each of which contains a PLA and a programmable I/O block that can be programmed to create many different logic structures. This powerful I/O architecture can be configured to support both active-high, active-low, 3-state, open-drain and bi-directional data ports or act as an input, all on a 4-bit wide basis.

All inputs to the circuit may be latched, including the 12 dedicated input pins.

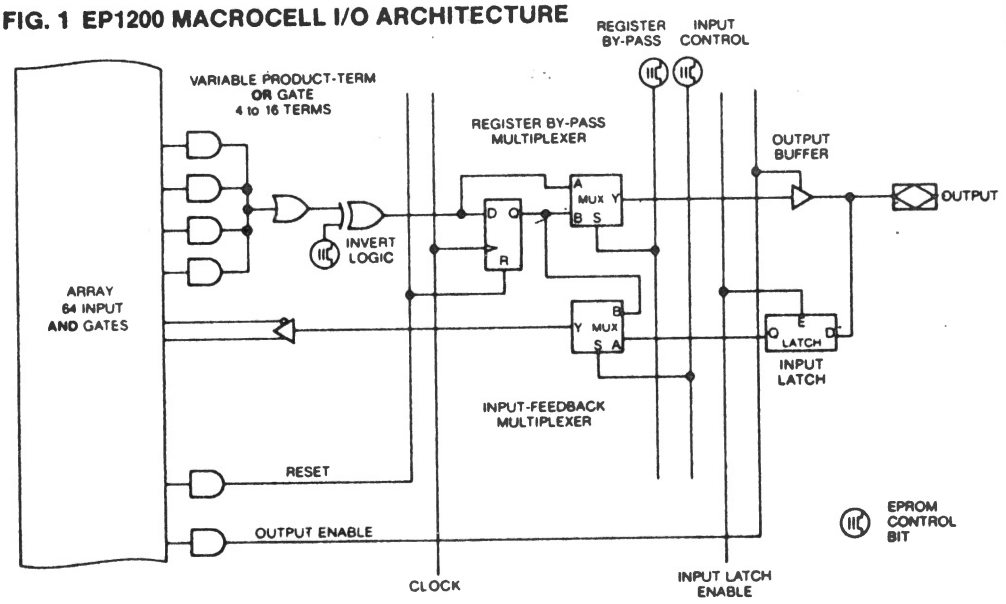
The Macrocells share a common programmable clock system that controls clocking of all registers and input latches. The device contains 8 modes of clock operation that allow logic transition to take place on either rising or falling edges of the clock signals.

The primary logic array of the EP1200 is segmented into two symmetrical halves that communicate via global bus signals. The main arrays contain some 15104 programmable elements representing 236 product terms each containing 64 input signals.

Macrocells in each half of the circuit are grouped together for architecture programming. These banks of four Macrocells can be further programmed on an individual Macrocell basis to generate active high or active low outputs of the logic function from the PLA.

The circuit further contains four Macrocells whose outputs are only fed back into the array to create buried-state functions. The feedback path may be either the registered or combinatorial result of the PLA output. The use of buried state Macrocells provides maximum equivalent logic density without demanding higher pin-count packages which consume valuable board space.

FIG. 1 EP1200 MACROCELL I/O ARCHITECTURE



I/O ARCHITECTURE

The Input/Output architecture of the EP1200 Macrocells can be programmed using both static and dynamic controls. The static controls remain fixed after the device is programmed whereas the dynamic controls may change state as a result of the signals applied to the device.

The static controls set the inversion logic, register by-pass and input feedback multiplexers. In the latter two cases these controls operate on four Macrocells as a bank. The buried-state registers have simpler controls which determine if the feedback is to be registered or combinatorial.

The dynamic controls consist of a programmable input latch-enable, as well as reset and output-enable product terms. The latch-enable function is

common throughout the EP1200 and is programmed by the clock control block but may also be driven by input signals applied to pin 1 (see clock modes Table 1). The reset and output-enable controls are logically controlled by single product terms (the logic AND of programmed variables in the array). These terms have control over banks of four Macrocells.

The output-enable control may be used to generate architecture types that include bi-directional, 3-state, open-drain or input only structures.

BUS STRUCTURE

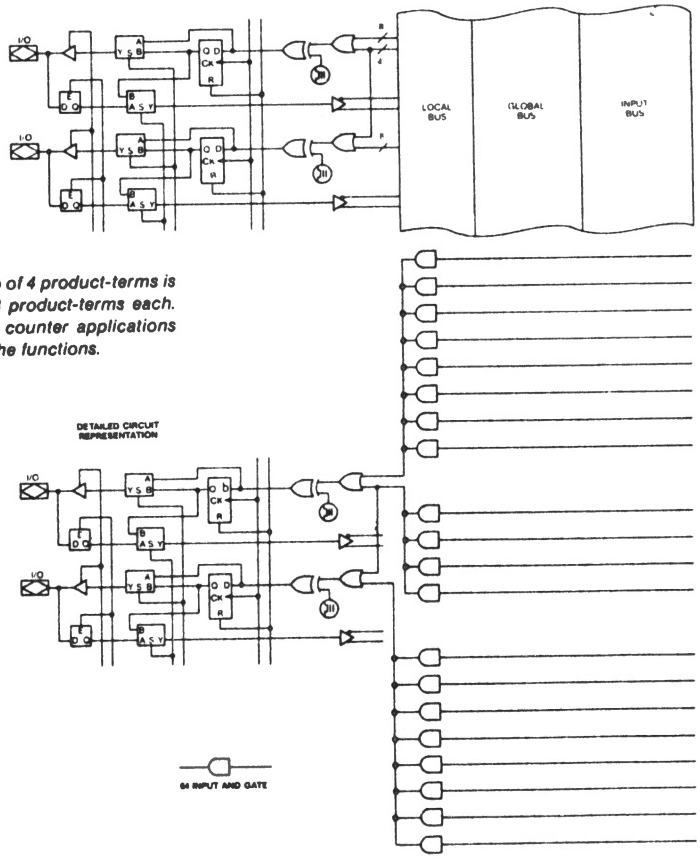
The two identical halves of the EP1200 communicate via a series of busses. The local bus structure that is used for communication within each half of the chip contains 16 conductors that carry the TRUE and COMPLEMENT of 8 local Macrocells.

The global bus is comprised of 48 conductors that span the entire chip which carry the TRUE and COMPLEMENT of primary inputs (pins 2 through 7 and 33 through 38), signals from 4 Buried Registers, as well as the global outputs of 8 Macrocells in groups A-3 and B-3.

SHARED PRODUCT TERMS

Macrocells 9, 10, 11, 12, 17, 18, 19 and 20 have the facility to share a total of 16 additional product terms. The sharing takes place between pairs of adjacent macrocells. This capability enables, for example, Macrocells 9 and 10 to expand to 16 and 8 effective product terms respectively and for Macrocells 11 and 12 both to expand to 12 effective product terms. Figure 2 shows this sharing technique in detail. This facility is primarily of use in state machine and counter applications where common product-terms are frequently required among output functions.

FIG. 2 SHARED PRODUCT-TERM CIRCUITS



In this illustration a small group of 4 product-terms is shared by groups containing 8 product-terms each. This feature is most useful in counter applications where common terms exist in the functions.

MACROCELL — BUS INTERFACE

The Macrocells within an EP1200 are interconnected to other Macrocells and inputs to the device via three internal data buses.

The product-terms span the entire bus structure that is adjacent to their Macrocell so that they may produce a logical AND of any of the variables (or their complements) that are present on the buses.

Macrocells all have the ability to return data to the local or global bus. Feedback data may originate from the output of the Macrocell or from the I/O pin. Feedback to the global bus communicates throughout the part. Macrocells that feedback to the local bus communicate to only half the EP1200. Connections to and from the signal busses are made with EPROM switches that provide the reprogrammable logic capability of the circuit.

Macrocells in groups A-3 and B-3 and the buried registers all have global bus connections while Macrocells in groups A-1, A-2, and B-1, B-2 have local bus connections. Figure 3 illustrates the local and global bus connections. Advanced features of the ALTERA development system will, if desired, automatically select an appropriate Macrocell to meet both the logic requirements and the connection to an appropriate signal bus to achieve the interconnection to other Macrocells.

FIG. 3 MACROCELL BUS STRUCTURE

At each intersecting point in the logic array there exists an EPROM-type programmable connection. Initially, all connections are complete. This means that both the true and complement of all inputs are connected to each product-term. Connections are opened during the programming process. Therefore any product term can be connected to the true or complement of any input. When both the true and complement connections of any input are left intact, a logical false results on the output of the AND gate. If both the true and complement connections of any input are programmed open, then a logical "don't care" results for that input. If all inputs for a product term are programmed open, then a logical true results on the output of the AND gate.

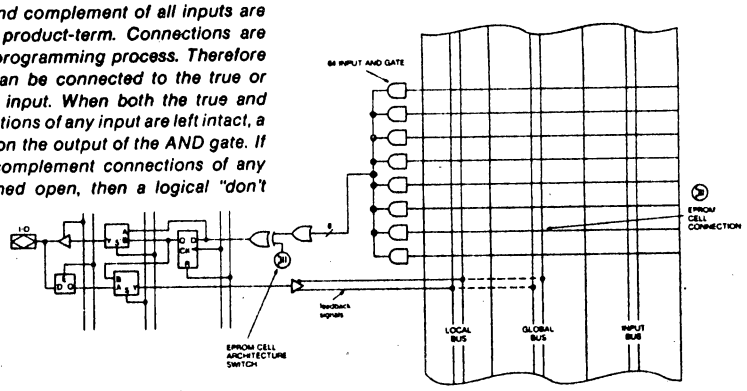
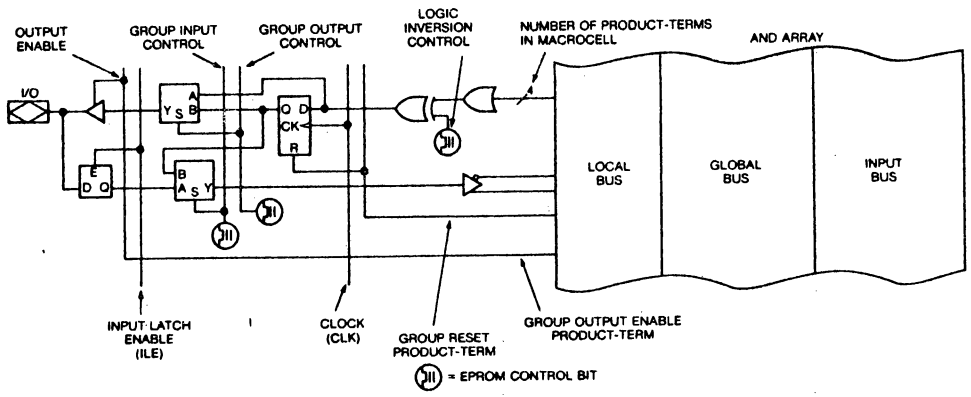


FIG. 4



CLOCK MODE CONTROL

The EP1200 contains two internal clock data paths that drive the input latches (transparent 7475 type) and the output registers. These clocks may be programmed into one of 8 operating modes. Figure 4 shows a typical Macrocell which is driven by the master clock signal CLK and the input latch-enable signal ILE.

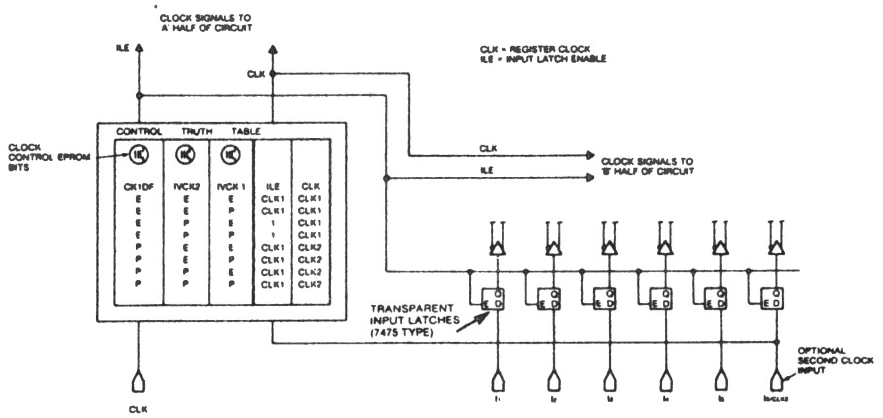
The master clock signal is input via pin 1. In programmed modes 4, 5, 6 and 7 a second clock is required which is input via pin 38. Table 1 shows the operation of each programming mode.

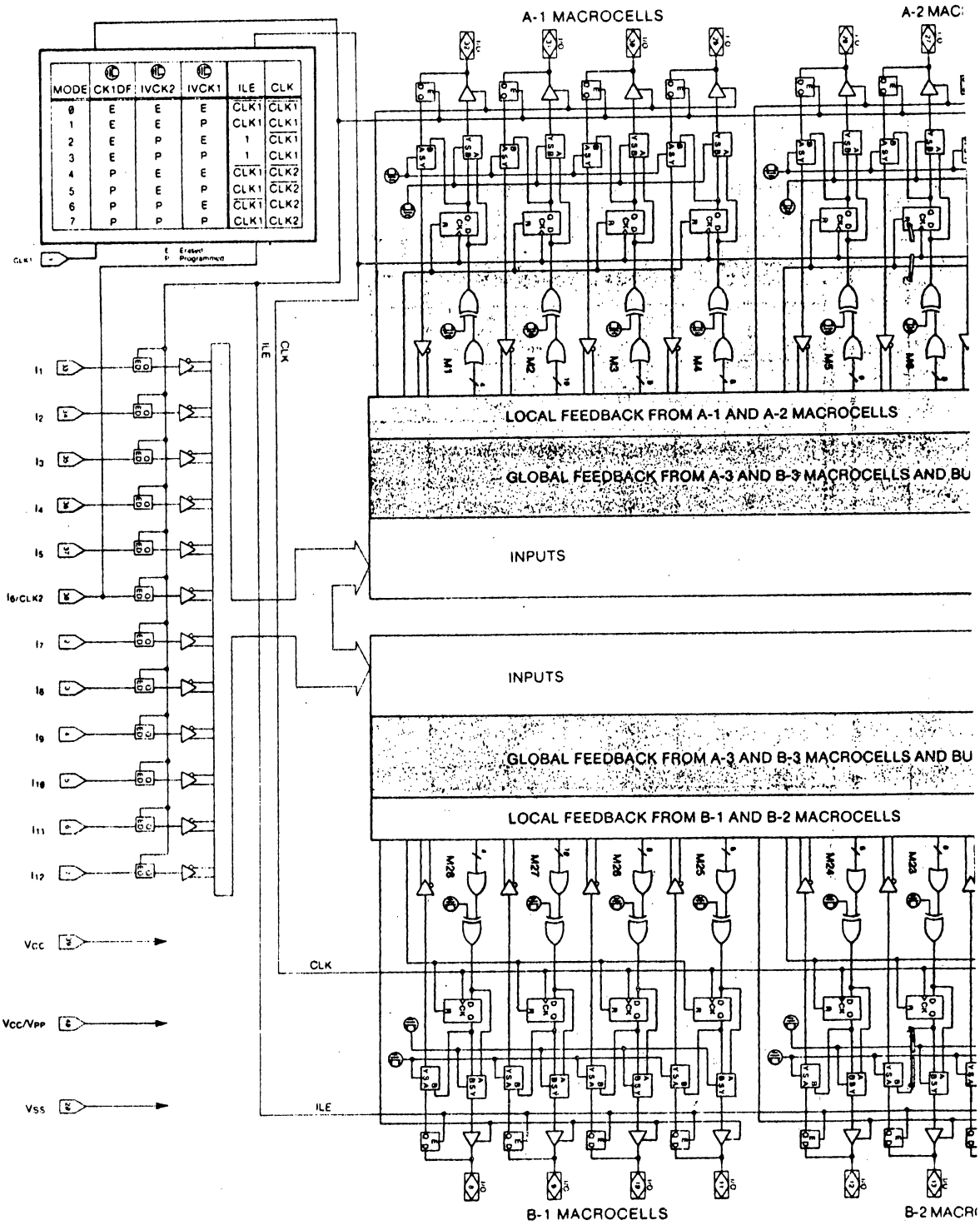
Care is required when using any of the two-clock modes to ensure that timing hazards are not created.

TABLE 1 CLOCK PROGRAMMING

PROGRAMMED MODE	INPUT SIGNALS ARE LATCHED WHEN:	OUTPUT REGISTERS CHANGE STATE WHEN:	CLOCK CONFIGURATION
0	CLK1 (PIN1)	CLK1 (PIN1)	1 CLOCK
1	CLK1 (PIN1)	CLK1 (PIN1)	1 CLOCK
2	INPUTS NOT LATCHED	CLK1 (PIN1)	1 CLOCK
3	INPUTS NOT LATCHED	CLK1 (PIN1)	1 CLOCK
4	CLK1 (PIN1)	CLK2 (PIN38)	2 CLOCKS
5	CLK1 (PIN1)	CLK2 (PIN38)	2 CLOCKS
6	CLK1 (PIN1)	CLK2 (PIN38)	2 CLOCKS
7	CLK1 (PIN1)	CLK2 (PIN38)	2 CLOCKS

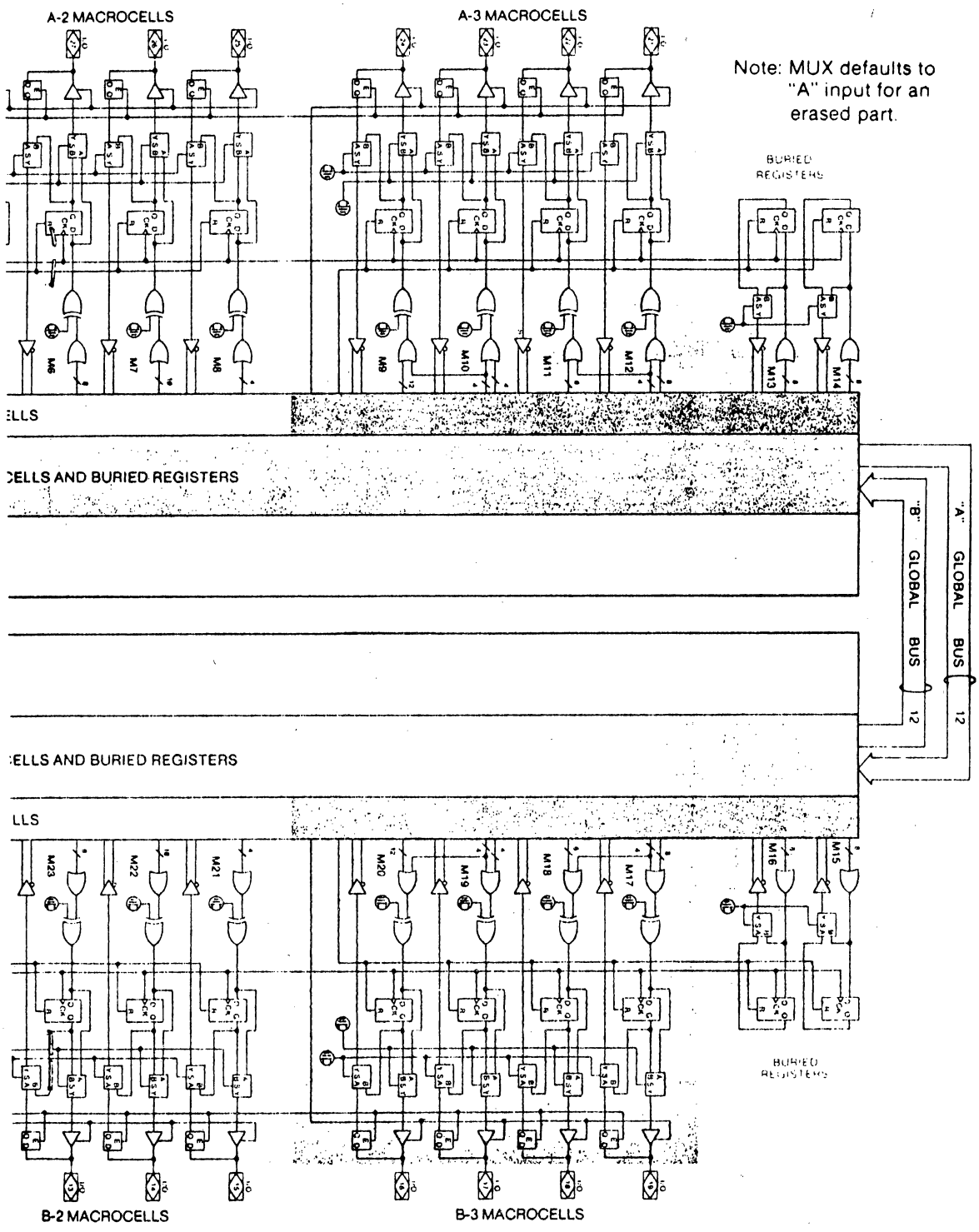
FIG. 5 PROGRAMMABLE CLOCK CONTROL SYSTEM





MODE	CK1DF	IVCK2	IVCK1	ILE	CLK
0	E	E	E	$\overline{CLK1}$	$\overline{CLK1}$
1	E	E	P	CLK1	CLK1
2	E	P	E	1	$\overline{CLK1}$
3	E	P	P	1	CLK1
4	P	E	E	$\overline{CLK1}$	$\overline{CLK2}$
5	P	E	P	CLK1	$\overline{CLK2}$
6	P	P	E	$\overline{CLK1}$	CLK2
7	P	P	P	CLK1	CLK2

E Erasure
P Programmed


A-2 MACROCELLS
A-3 MACROCELLS
Note: MUX defaults to "A" input for an erased part.
BURIED REGISTERS
M6
M7
M8
M9
M10
M11
M12
M13
M14
ELLS
CELLS AND BURIED REGISTERS
"A" GLOBAL BUS
"B" GLOBAL BUS
12
12
ELLS AND BURIED REGISTERS
LLS
M23
M22
M21
M20
M19
M18
M17
M16
M15
BURIED REGISTERS
B-2 MACROCELLS
B-3 MACROCELLS

ABSOLUTE MAXIMUM RATINGS

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{CC}	Supply voltage	With respect to GND	-0.5	6.0	V
V_{PP}	Programming supply voltage		-0.5	20.0	V
V_I	DC INPUT voltage		-0.5	V_{CC}+0.5	V
I_{CC}	DC V_{CC} current			+100.0	mA
T_{STG}	Storage temperature		-40	+125	°C
T_{AMB}	Ambient temperature	Under bias	-10	+85	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{CC}	Supply voltage		4.75	5.25	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature		0	70	°C
T_R	INPUT rise time			500	nS
T_F	INPUT fall time			500	nS

DC OPERATING CHARACTERISTICS

T_A = 0° to 70°C, V_{CC} = 5.0V±5%

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.2		V_{CC}+0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level output voltage	I_O = -4.0mA DC	2.4			V
V_{OL}	LOW level output voltage	I_O = 4.0mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND			±10.0	µA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND			±10.0	µA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND I_O = 0		3.0		mA
I_{CC2}	V_{CC} supply current (active)	No load f = 10 MHz		50		mA

AC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V±5%) Note (1)

Symbol	Parameter	Conditions	EP1200-1			EP1200-2			EP1200			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PD}	Non-registered input or I/O input to non-registered output	Fig. 8		55			70			95		ns
t_{PZX}	Non-registered input or I/O input to output enable	C_1 = 30pf		55			70			95		ns
t_{PXZ}	Non-registered input or I/O input to output disable	Note (2), Fig. 8 C_1 = 5pf		55			70			95		ns
t_{SU}	Non-registered input or I/O input to output register set-up	Fig. 8 C_1 = 30pf		40			50			65		ns
t_H	Non-registered input or I/O input to output register hold			0			0			0		ns
t_{CH}	Clock high time			25			30			35		ns
t_{CL}	Clock low time			25			30			35		ns
t_{CO1}	Clock to output delay			25			30			35		ns
t_{P1}	Minimum clock period (register ouput feedback to register input — internal path)			50			60			80		ns
f_1	Maximum frequency ($1/t_{P1}$)			20			16.6			12.5		MHz
t_{P2}	Minimum clock period (t_{SU} + t_{CO1})			65			80			100		ns
f_2	Maximum frequency ($1/t_{P2}$)			15.5			12.5			10		MHz
t_{RST}	Asynchronous reset time			55			70			95		ns
t_{CO2}	Registered feedback through PLA to output. Relative to external clock			70			85			105		ns
t_{ILS}	Set up time for latching inputs			0			0			0		ns
t_{ILH}	Hold time for latching inputs			15			20			25		ns
t_{C1C2}	Minimum clock 1 to Clock 2 delay			40			50			65		ns
t_{ILDFS}	Input latch to D-FF setup time	Mode 0, 1		40			50			65		ns
t_{DFILS}	D-FF to input latch setup time			25			30			35		ns
t_{P3}	Minimum period for a 2-clock system (t_{C1C2} + t_{CO1})			65			85			100		ns
f_3	Maximum frequency ($1/t_{P3}$)			15.5			12			10		MHz

1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500 mV

FIG. 6 SWITCHING WAVEFORMS

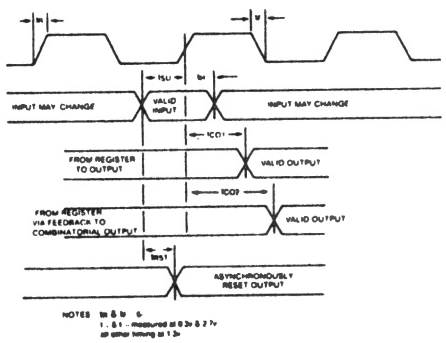


FIG. 7 SWITCHING WAVEFORMS

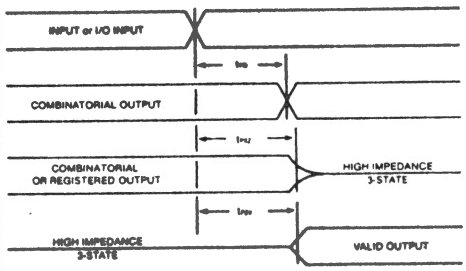
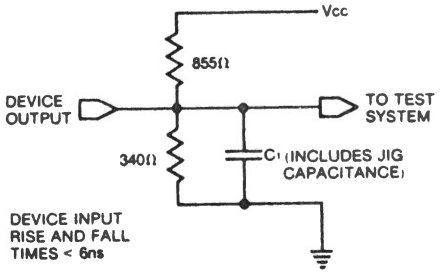


FIG. 8 AC TEST CONDITIONS



PROGRAM ERASURE

The erasure characteristics of the EP1200 are such that erasure of the programmed connections begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms. It is important to note that sunlight and certain fluorescent lighting could erase a programmed EP1200 since they have wavelengths in the range of 3000 to 4000 Angstroms. Extrapolated results suggest that constant exposure to room level fluorescent lighting could erase an EP1200 in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. As a consequence, if the EP1200 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the EP1200 window to prevent unintentional erasure.

The recommended erasure procedure for the EP1200 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms. The integrated exposure dose for erasure should be a minimum of 15Wsec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 1200 μW/cm² power rating. The EP1200 should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated exposure dose for an EP1200 without damage is 7000 Wsec/cm². This is approximately one week at 12000 μW/cm². Exposure of the EP1200 to high intensity UV light for long periods may cause permanent damage.

The EP1200 may be erased and re-programmed as many times as needed using the recommended erasure exposure levels.

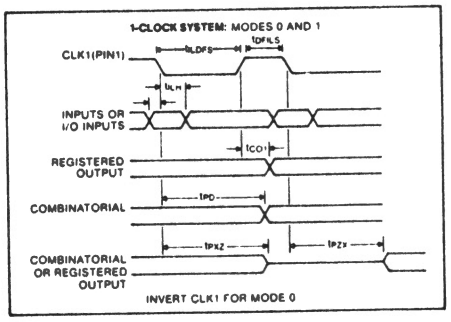
FUNCTIONAL TESTING

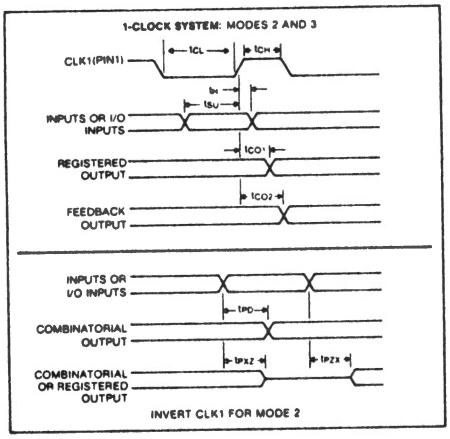
The EP1200 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements including buried state registers.

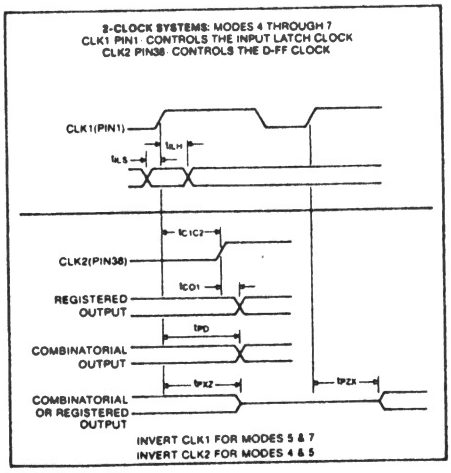
As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP1200 allows test program patterns to be used and then erased. This facility to use application-independent, general purpose tests is called generic testing and is unique among user-defined LSI logic devices.

To enable functional evaluation of counter and state-machine applications, the EP1200 contains register pre-load circuitry. This can be activated by interrupting the normal clocked sequence and applying V_{HH} on pin 2 to engage the pre-load state. Under these conditions the flip-flops in the EP1200 can be set to any logical condition and then return to normal operation. This process simplifies the input sequences necessary to evaluate counter and state-machine operations.

FIG. 9 SWITCHING WAVEFORMS





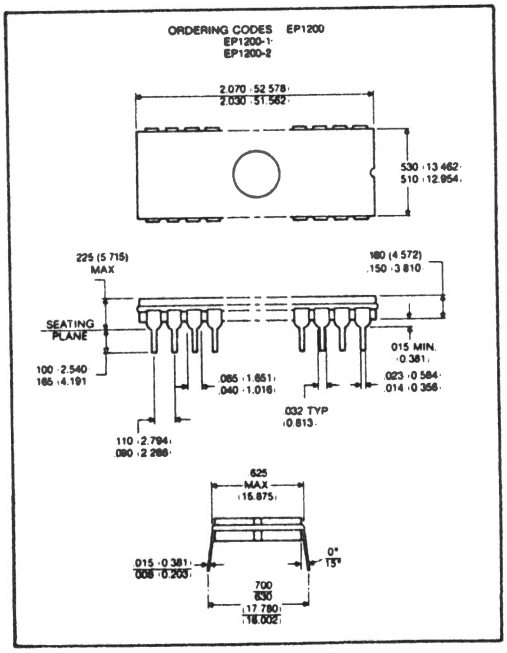


DESIGN RECOMMENDATIONS

If operated with stresses above those listed under "Absolute Maximum Ratings" the device may be permanently damaged. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating condition for extended periods may affect device reliability. These devices contain circuitry to protect,the input against damage to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that input and output pins be constrained to the range GND ≤ (Vin or Vout) ≤ Vcc. Unused inputs must always be tied to an appropriate logic level (e.g., either Vcc or GND).

In normal operation Vcc/Vpp (pin 40) should be connected directly to Vcc (pin 39).

PACKAGE OUTLINE



PROGRAMMING DEVELOPMENT TOOLS

The EP1200 is supported by an advanced programming development system that facilitates accurate and rapid product development.

The software system, known as A+PLUS, is the Altera Programmable Logic User System which supports multiple design entry techniques that include:

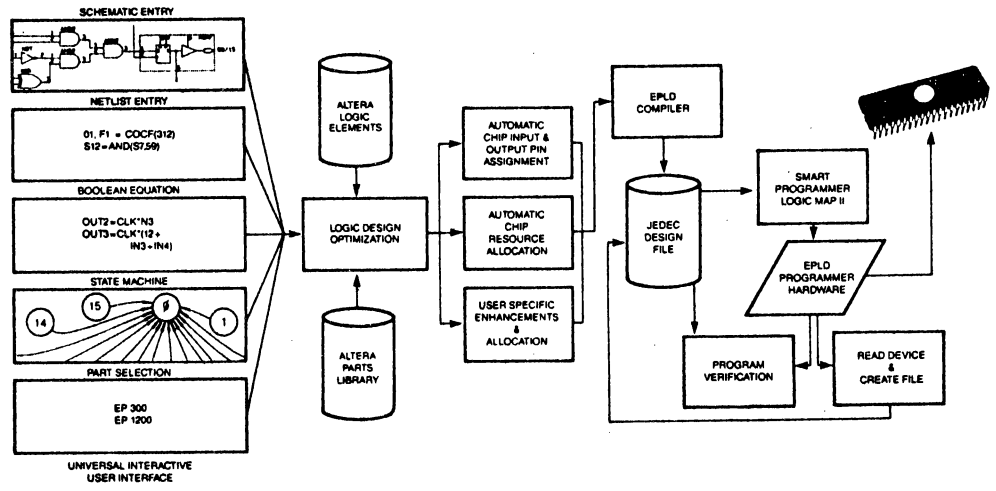
- Schematic diagram entry ..... PCCAPS
- Interactive netlist entry ..... NetMap
- Boolean equation entry .. Altera Design File

The typical development environment used for this software would be an IBM Personal Computer and equivalent machines with the following configuration:

- Dual floppy disk drive or hard disk drive
- MS-DOS operating system version 2.0 or later release
- 384K memory
- Altera device programming card and unit

The output of A+PLUS is a data file in a standard JEDEC format. The EP1200 can then be programmed using the programming card.

ALTERA PROGRAMMABLE LOGIC USER SYSTEM



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