DESIGN AND FABRICATION OF 256X1 SINGLE TRANSISTOR DYNAMIC RAM

By

MKM NASIM UDDIN

Bachelor of Science

Bangladesh University of

Engineering & Technology

Dhaka, Bangladesh

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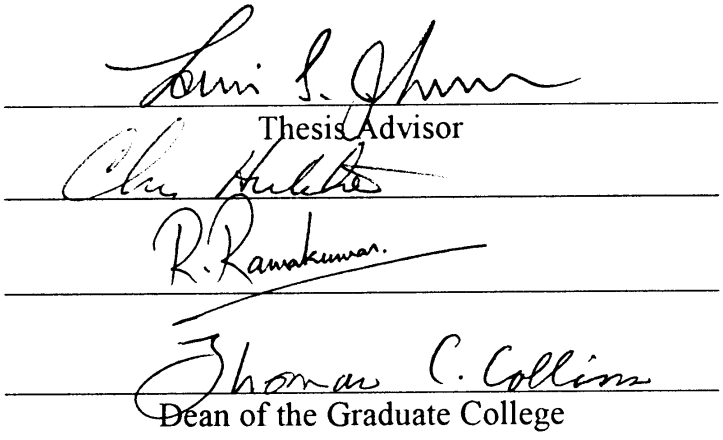
Thesis Approved:



Thesis Advisor

Dean of the Graduate College

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TABLE OF CONTENTS

LIST OF FIGURES

CHAPTER I

INTRODUCTION

In the electronics industry, random access read/write memory devices are referred to as a RAMs. The storage locations in RAM can be accessed in a random order. Unlike ROM, the data stored in RAM are not permanent in nature; that is, they can be altered. We are able to both write new data into a location in RAM for storage and read data back out for use in processing. Because of its versatile read and write features, RAM finds wide use in applications where data change frequently [4].

The dynamic RAM is the cheapest and consequently the most popular, RAM for large microcomputer systems [5].

The basic memory cell, which consists of a single transistor and a capacitor, is small and a very dense array can be made. The cell area can be minimized by overlapping poly1 and poly2 by one lambda. Because the major cost of a semiconductor memory is usually in the cost of the wafer, the more chips on a wafer, the lower the cost of a single chip. Therefore Dynamic RAMS have a lower cost per bit than memories with less compact arrays. Because the Dynamic RAMs consume only a.c. current, the power dissipation is quite low. Dynamic RAMs are also fast for a system to access giving them a high performance rating [5].

A dynamic RAM is a MOS memory which stores a bit of information as a charge on a capacitor. Since this charge decays away in a finite length of time (milliseconds) a periodic refresh is needed to restore the charge so that the Dynamic RAM retains its memory [5].

SINGLE TRANSISTOR DYNAMIC RAM CELL:

The basic memory cell, which consists of a single transistor and a capacitor, is small and a very dense array can be made. This cell is shown in fig. 1.1(a) and its cross-sectional view is shown in fig. 1.1(b).

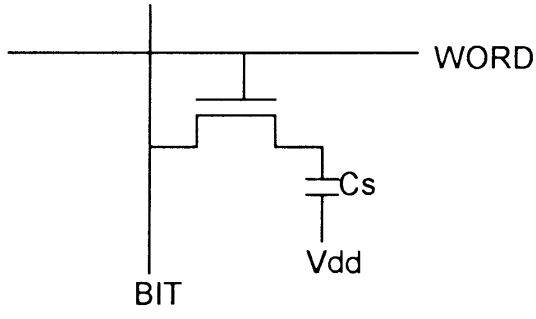

Fig 1.1(a): Single Transistor dynamic RAM cell

The information is stored in capacitance Cs, which is built using poly2. Building this cell poly 1 is overlapped by poly2 to make the cell compact. The gate acts to insulate the stored charge except during read/write operations. To write, the BIT line is charged to the desired level, and the word line is driven high, which charges up Cs via the transistor. To read, the word line is again selected, the bit line is tristated, and the charge in Cs is put in the bit line and is detected by a specially designed sense amplifier. The reading is destructive; after reading, the information must be immediately restored. This is done by using a refresh cycle. The same bit line is used for both read and write operations, but the direction of

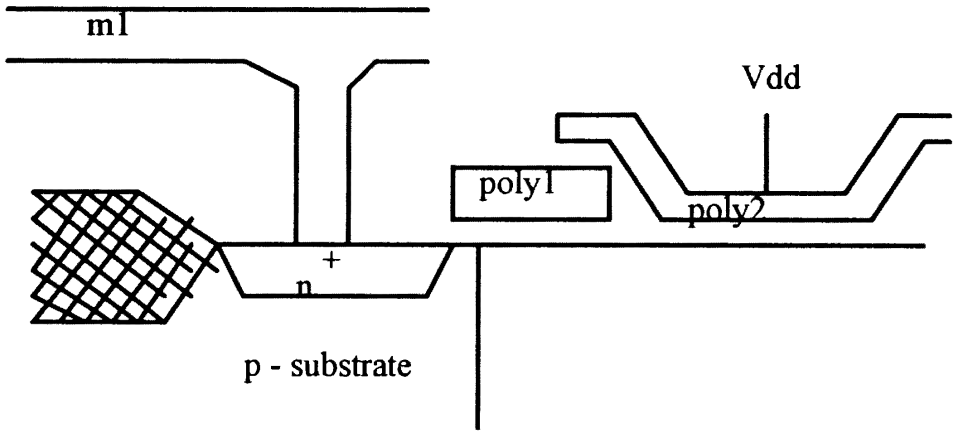

Fig. 1.1(b) : Cross sectional view of memory cell

current is reversed [5].

The storage node has to have a capacitance big enough to maintain an adequate difference between a sensed '1' and a sensed '0' on the bit line. Here with a fixed supply voltage the sense signal Vout is proportional to $C_s/(C_s+C_{bit})$ [1].

ROW DECODER:

A very simple row decoder is shown in Fig. 1.2. This uses a precharged domino AND gate [3].

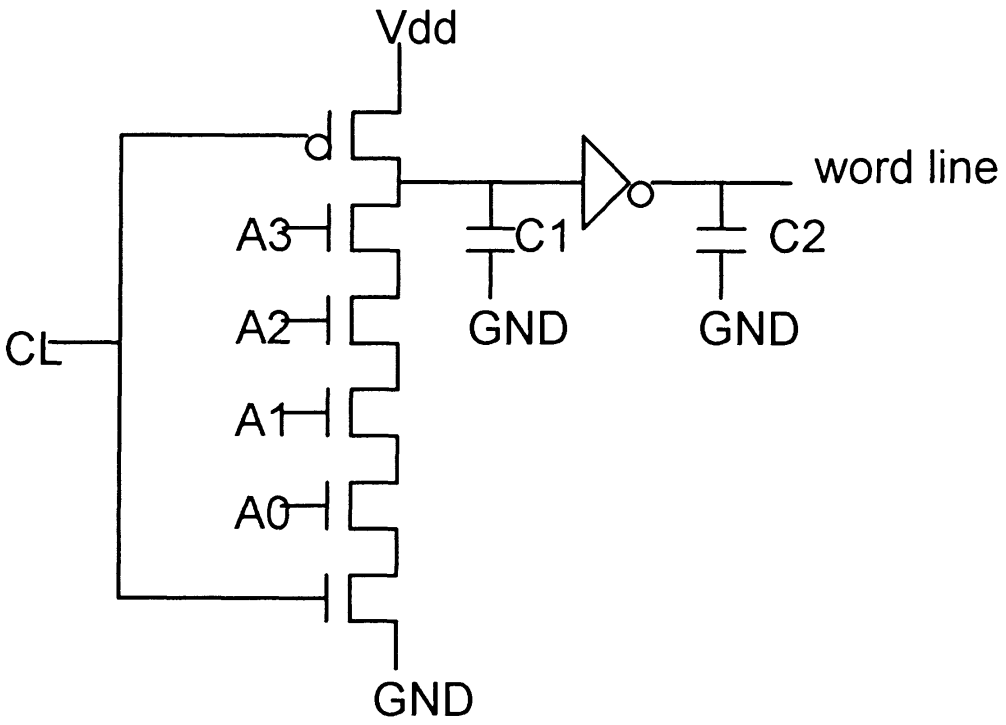

Fig.1.2 Domino AND row decoder

When CL=0 the capacitors C1 and C2 are precharged to 1 and 0 respectively. When CL=1 and A0=A1=A2=A3=1 then word line=1.

The precharge technique has the advantage that it avoids the use of the pull

up network, at the expense of one p-transistor and one additional n-transistor. This leads to almost a 50% savings in silicon area for larger circuits and reduction of the output capacitance, resulting in higher speed. Further more, the pull down circuit does not have to sink the pull-up current (as in the case of the pseudo nmos circuit), which also results in higher speed [3].

COLUMN DECODER :

A column decoder is shown in fig. 1.3. In this design, a NOR gate switches a single transmission gate [7].

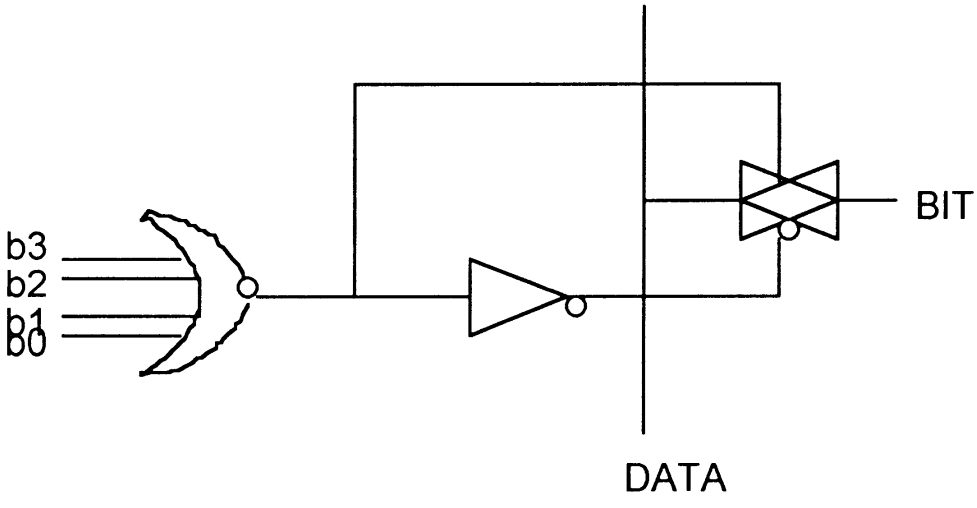

Fig. 1.3 : NOR Column decoder

READ / WRITE AND REFRESH CIRCUIT:

Read /Write and Refresh circuit of a dynamic RAM is shown in fig. 1.4. To write information into the cell the $\overline{R/W}$ line is set to logic 0 and data is applied at the DATA IN line. The desired row and column lines are selected to select a particular cell. The BIT line is precharged to approximately Vdd/2 by setting the $\overline{READ}$ control signal to high. To read stored information the $\overline{R/W}$ line is set to logic 1. Stored charge in the cell is detected by the sense amplifier. Details of this circuit are discussed in later chapter.

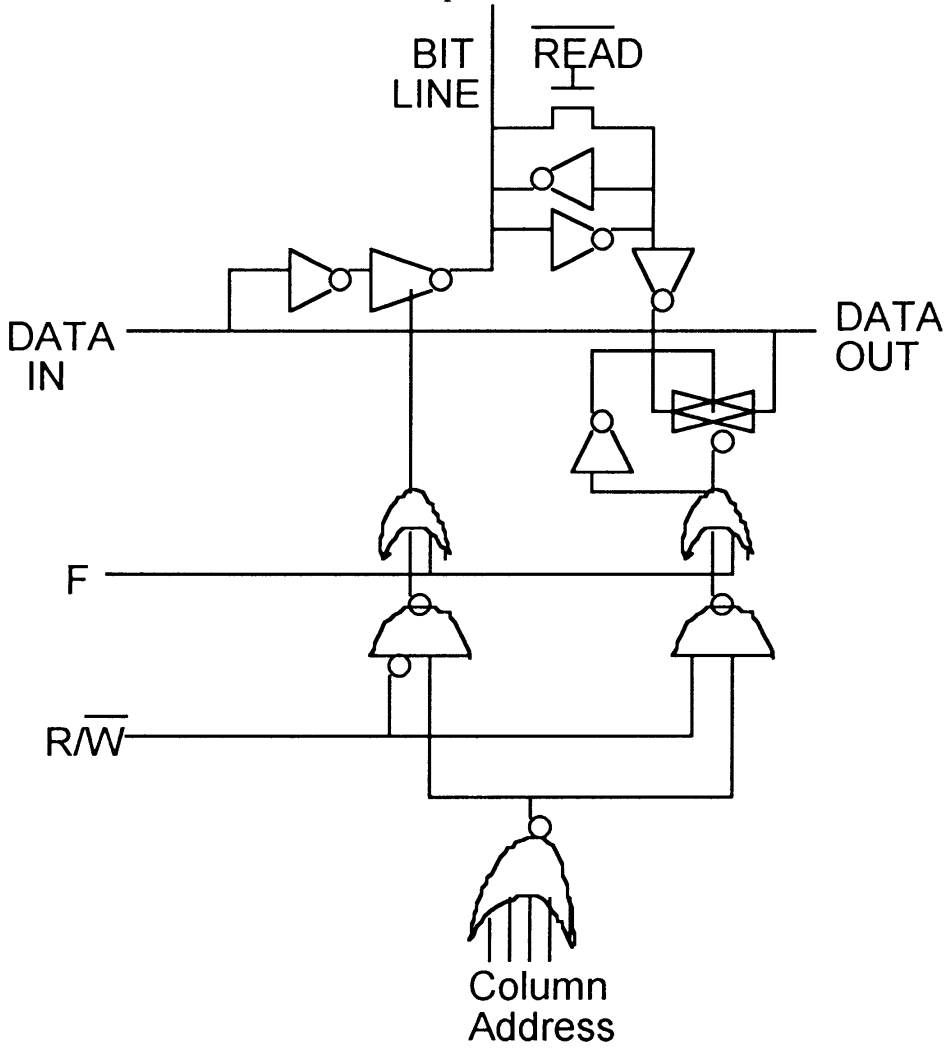

Fig. 1.4 : Read / Write & Refresh Circuitry

READ / WRITE DIAGRAM CONVENTION OF DYNAMIC RAM:

Fig.1.5, 1.6, 1.7, 1.8 shows a sample Read / Write operation diagram of Dynamic RAM. During Read or Write operation the desired word (row) and column line are set at high. After Write '0' or Write '1' operation the bit line is precharged to approximately Vdd/2.

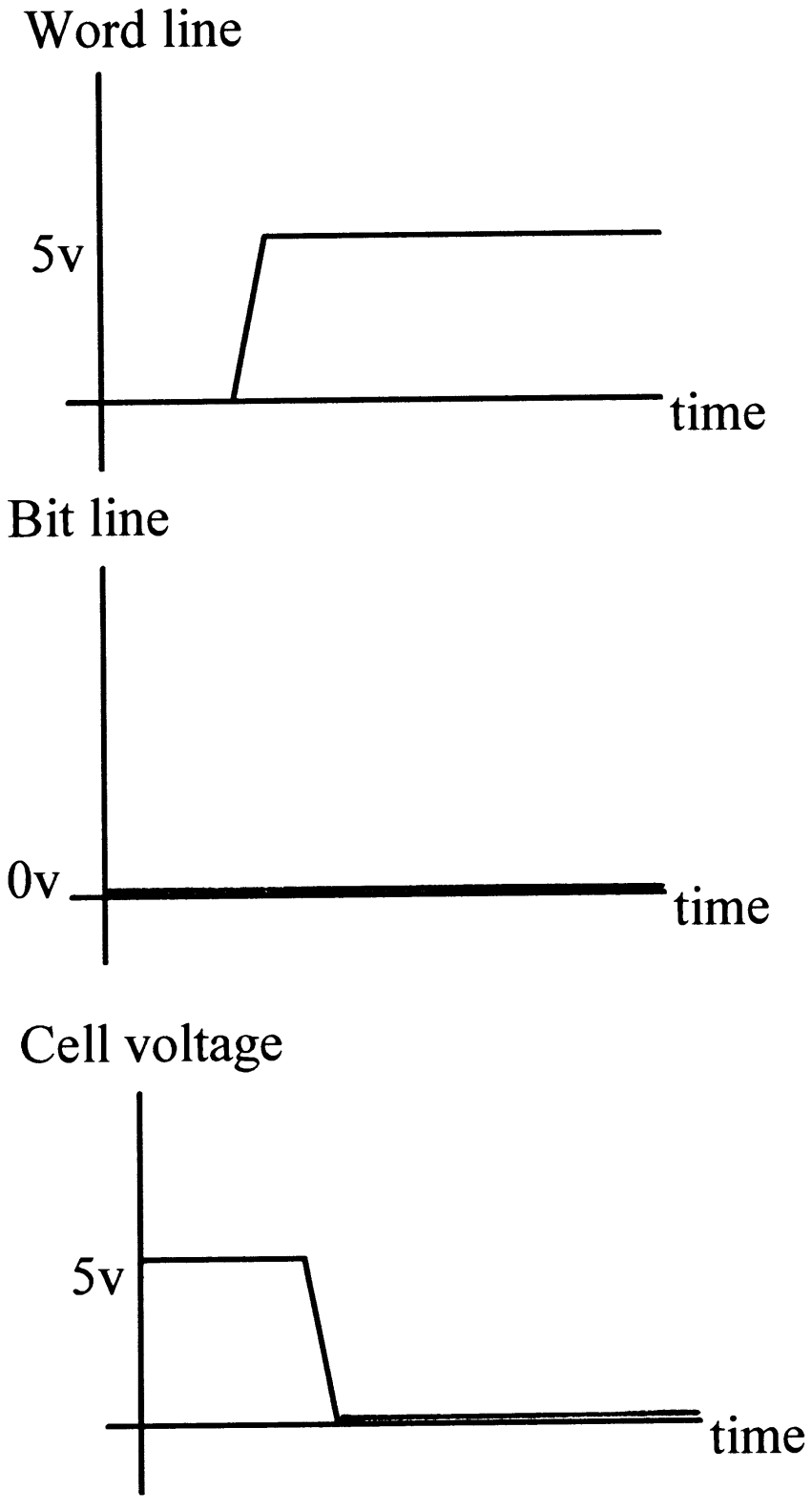

Fig. 1.5: Plot of Write '0' operation of DRAM

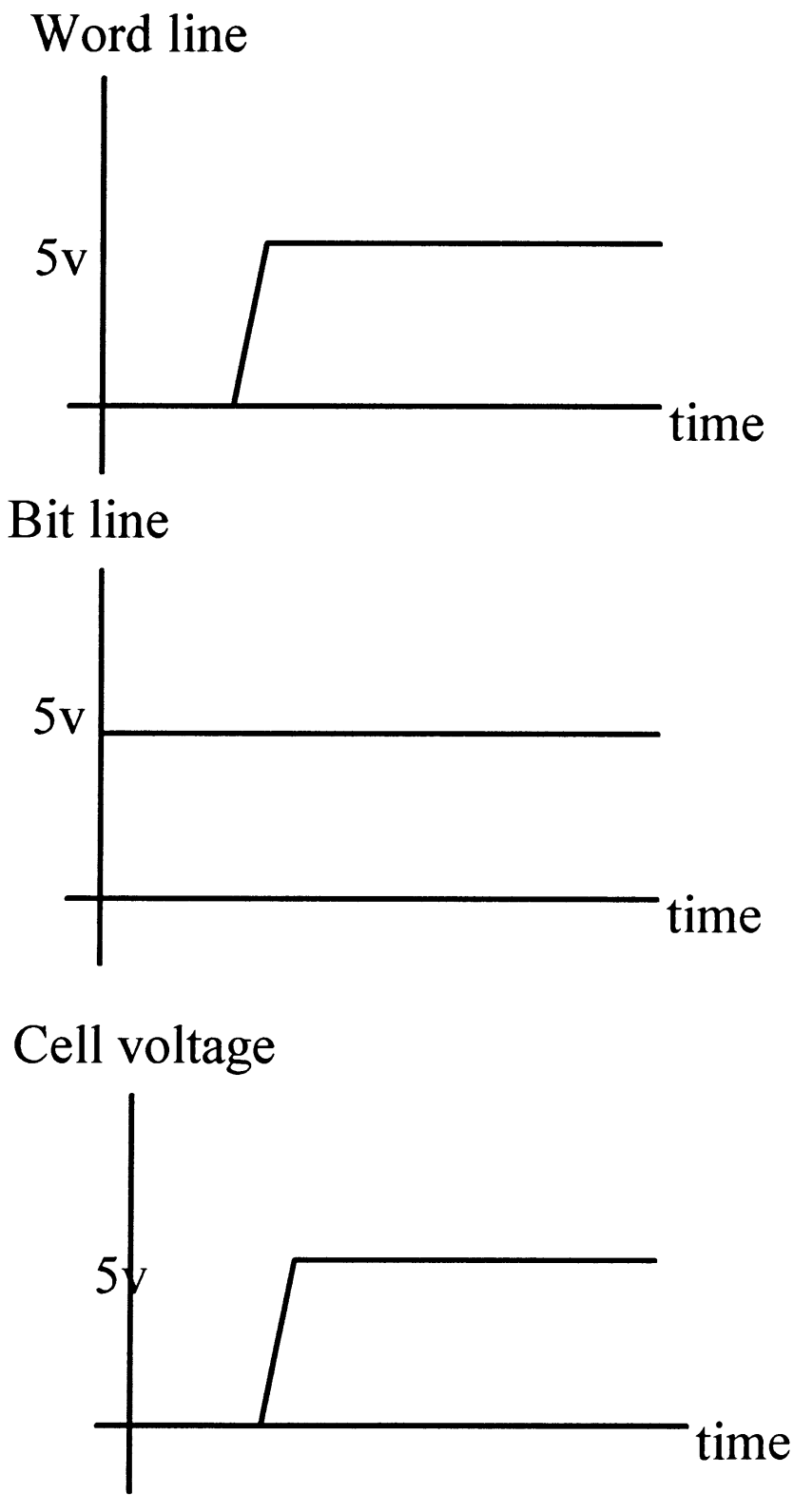

Fig. 1.6: Plot of Write '1' operation of DRAM

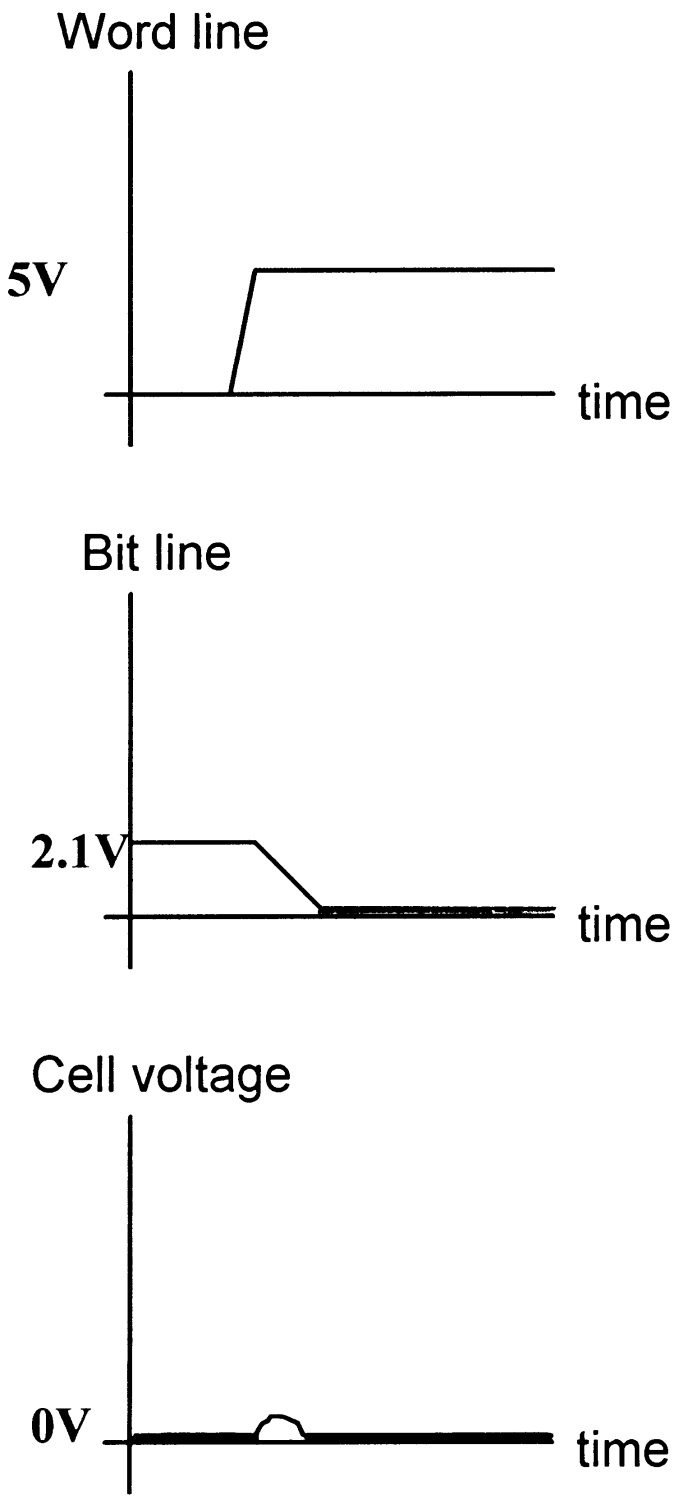

Fig.1.7: Plot of read '0' operation of DRAM

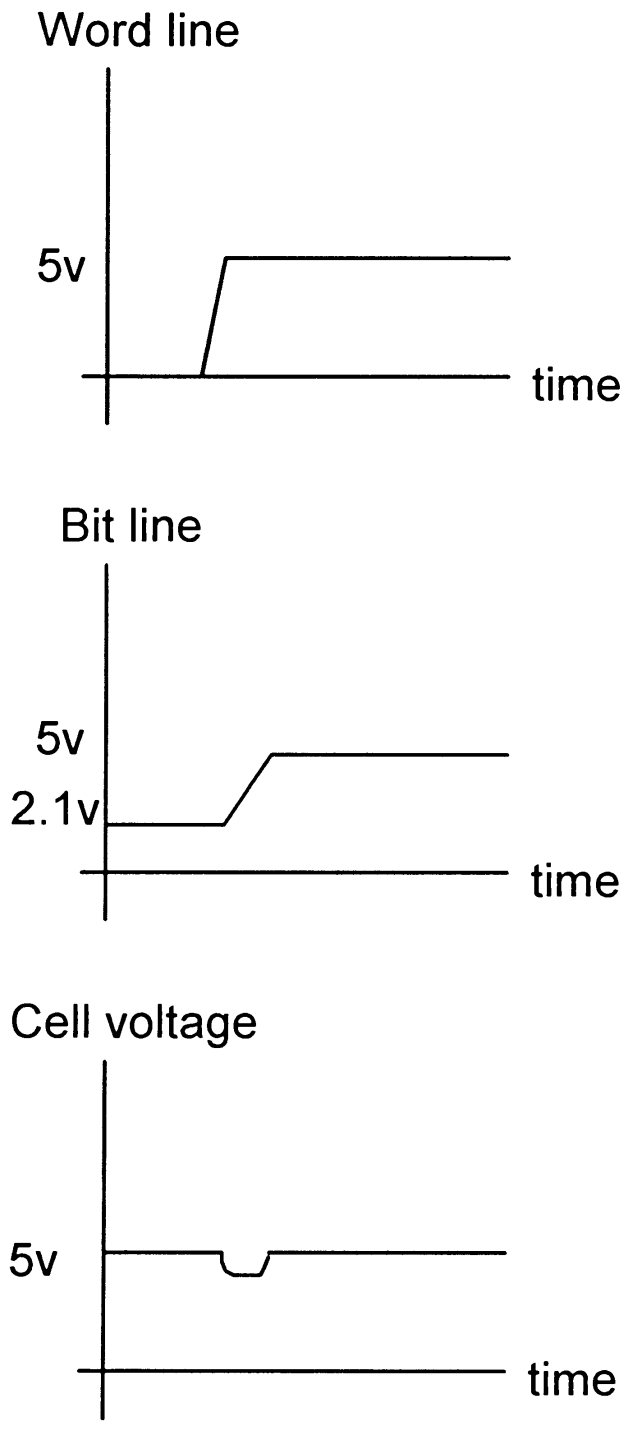

Fig. 1.8: Plot of Read '1' operation of DRAM

CHAPTER II

256X1 SINGLE TRANSISTOR DYNAMIC RAM

RAM ARCHITECTURE

The block diagram of the Dynamic RAM is shown in fig.2.1 The architecture shown has basic parts: row address buffer, row decoder, memory array, sense amplifier, read / write and refresh circuitry, column mux, column decoder, column address buffer, input and output buffer.

The floor plan of 256x1 Single Transistor Dynamic RAM is shown in fig.2.2 and its layout is shown in fig.2.3 & 2.4 . For row decoding a precharged domino AND gate is used (layout is shown in fig.2.5). The output of the AND gate selects one of the 16 word line when the row address strobe is low. NOR gates are used for column decoding (layout is shown in fig.2.6). The output of these gates switch a single transmission gate.

The memory array is a special group of circuits that store data within RAM. This array consists of one storage element (cell) for each bit of data the memory must store. These cells are organized in orderly matrix pattern. The floor plan of memory array is shown in fig.2.7 and its layout is shown in fig. 2.8. This array consists of 256 cells arranged 16 rows and 16 columns.

Read/Write/Refresh circuitry is used (as shown in fig.1.4) to read, write and refresh the cell. The column address strobe is used to control the column address, F control line is used to control refreshing cycle, $R/\overline{W}$ to control read/write operations, $\overline{read}$ to precharge the bit line. Other basic cells are also shown (From Fig. 2.9 to 2.14).

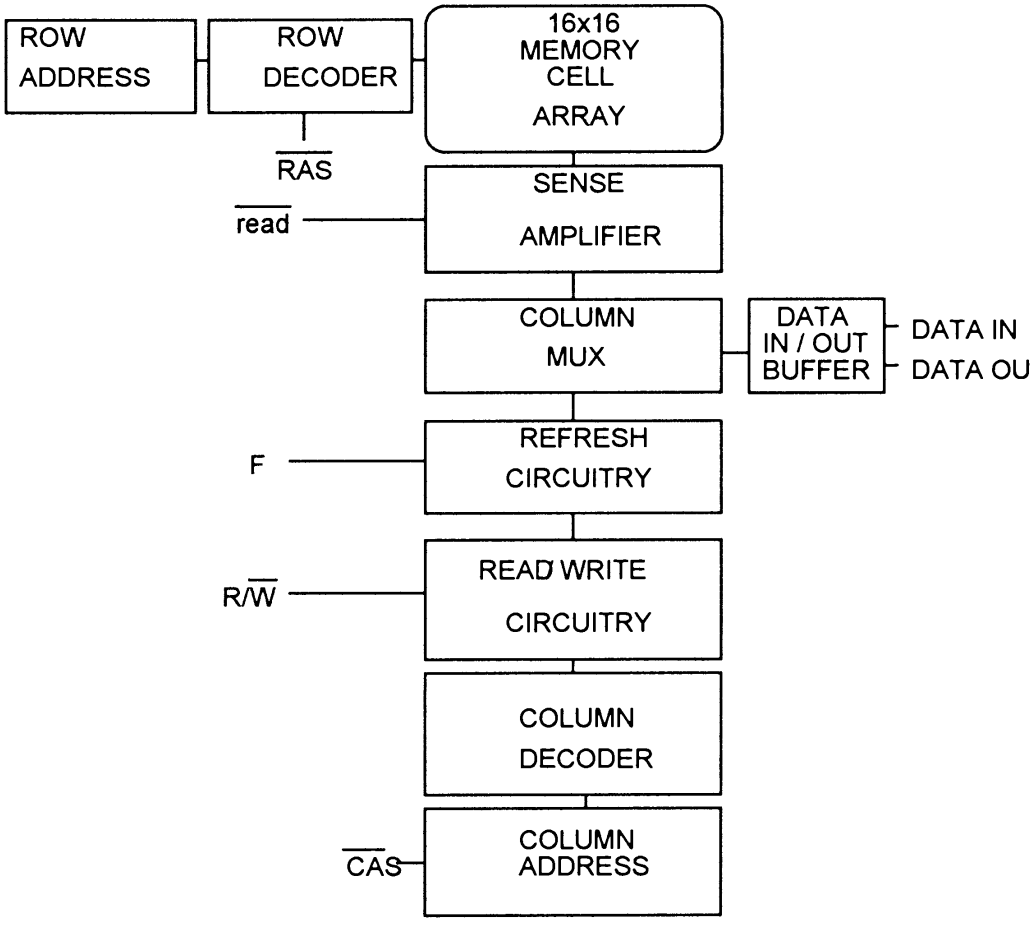

Fig. 2.1 : BLOCK DIAGRAM OF 256x1 DYNAMIC RAM

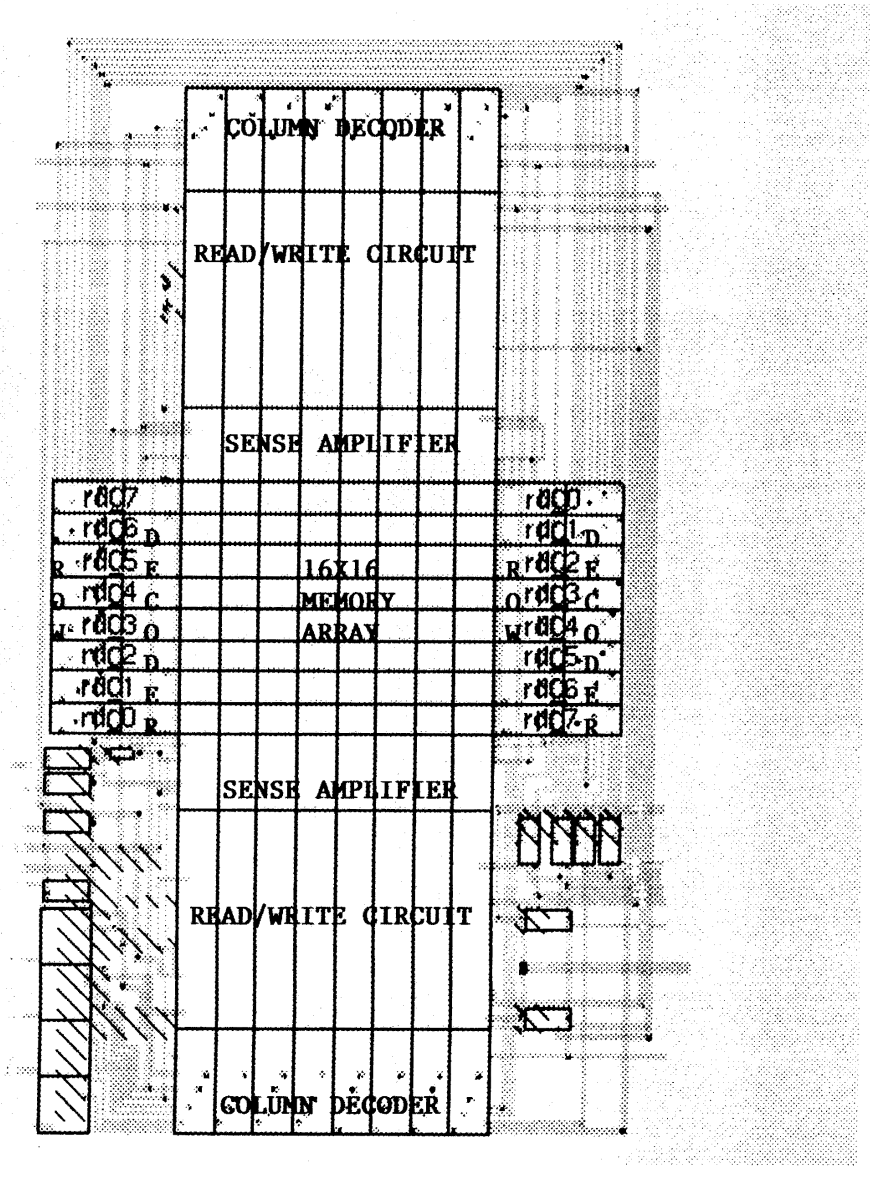

Fig. 2.2: Floor plan of 256x1 Single Transistor Dynamic RAM

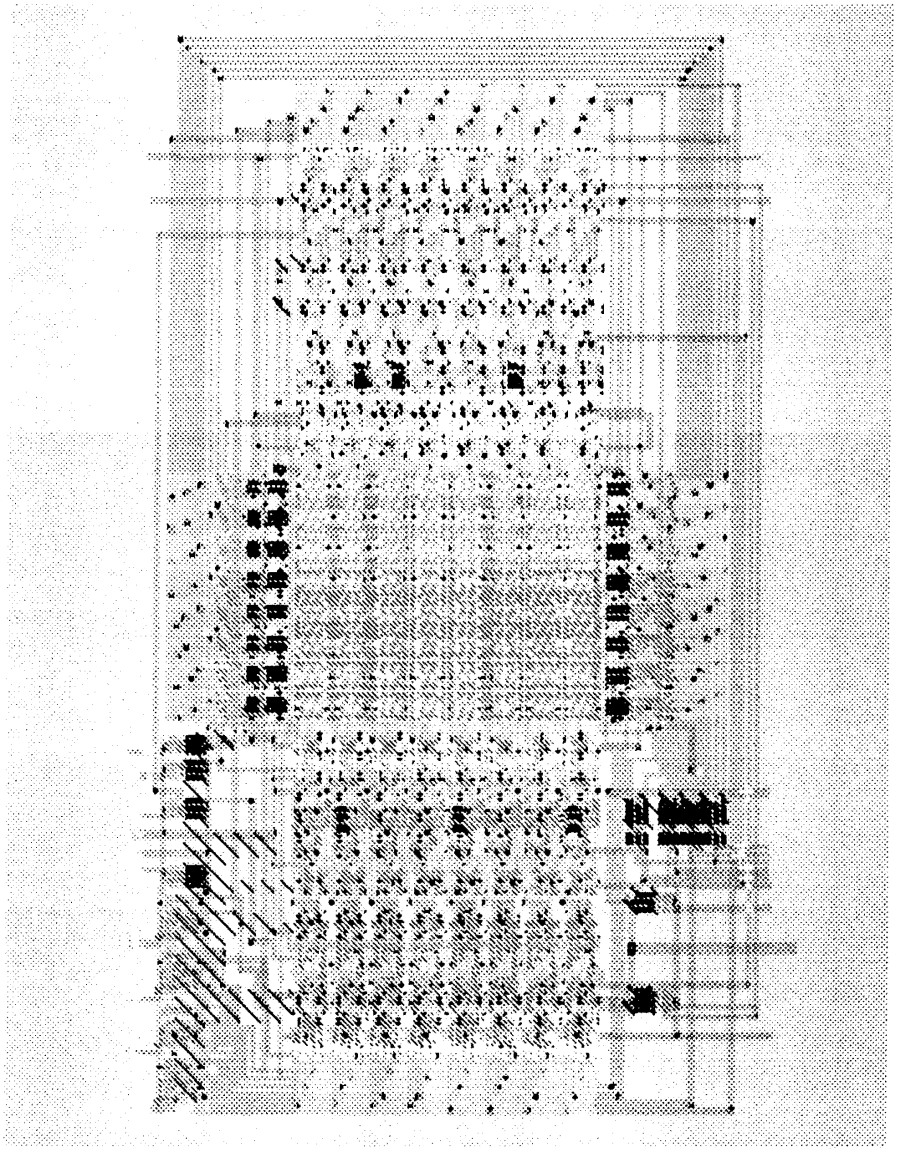

Fig. 2.3: Circuit layout of 256x1 Single Transistor Dynamic RAM

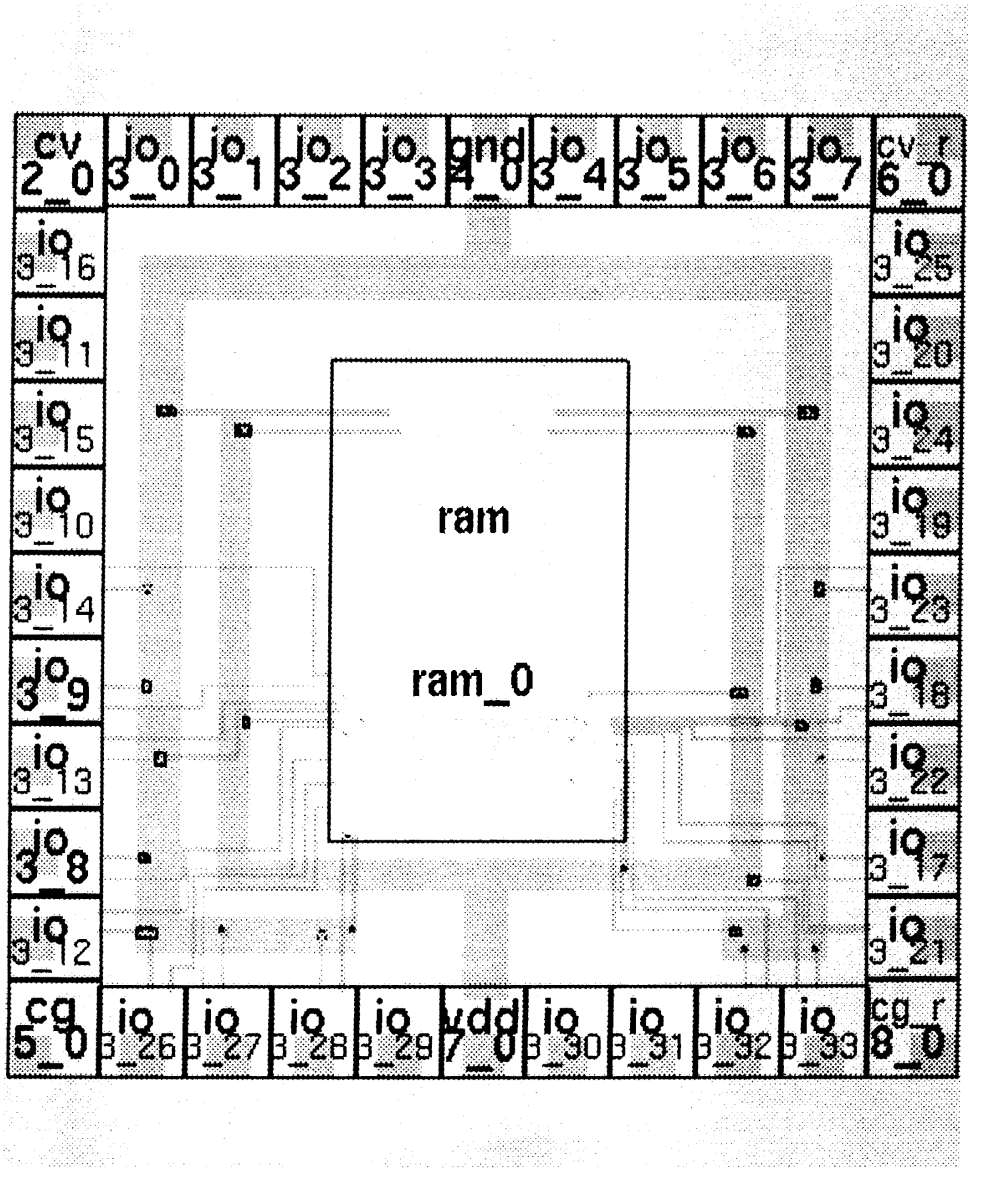

Fig. 2.4: 256x1 Single Transistor Dynamic RAM with pad

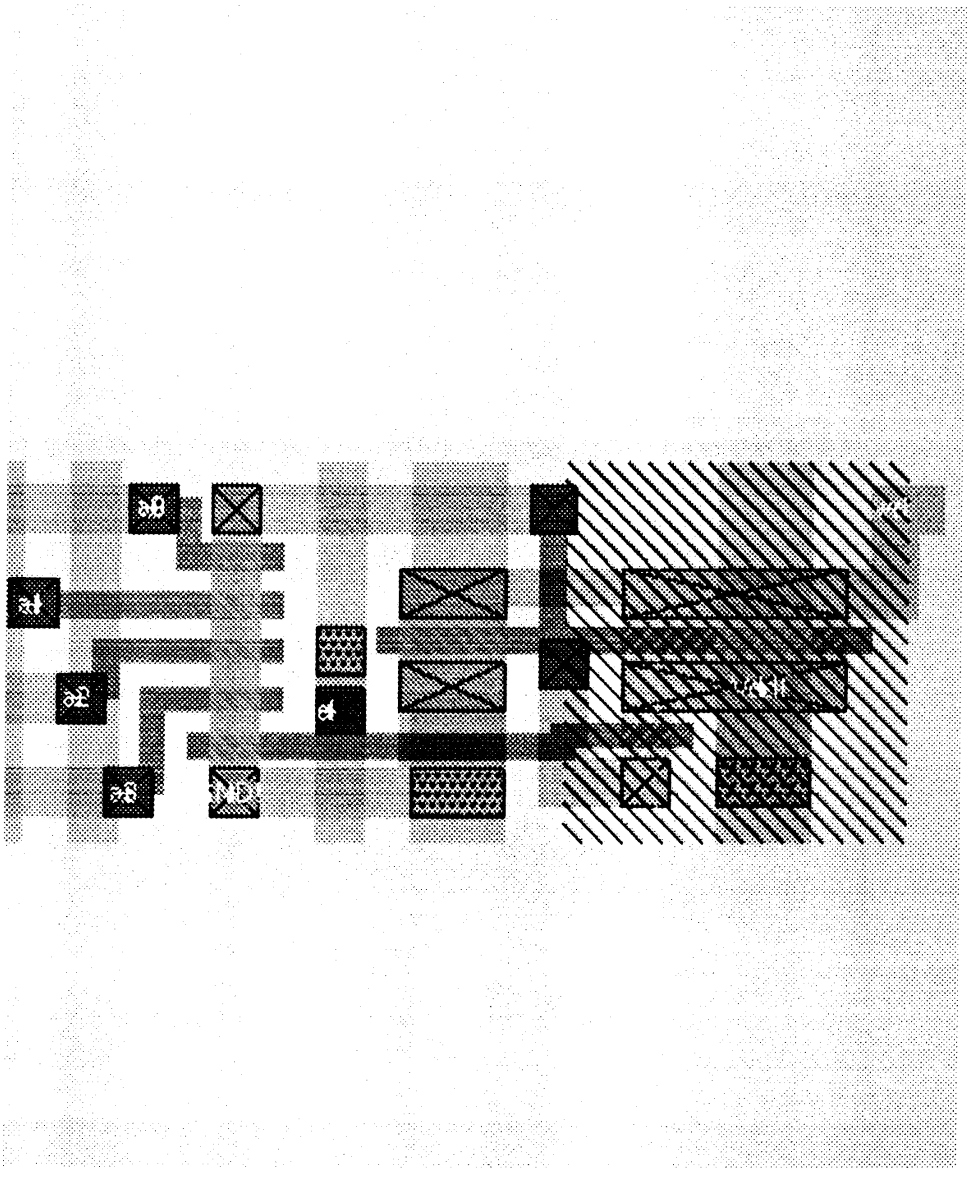

Fig. 2.5: Circuit layout of row decoder

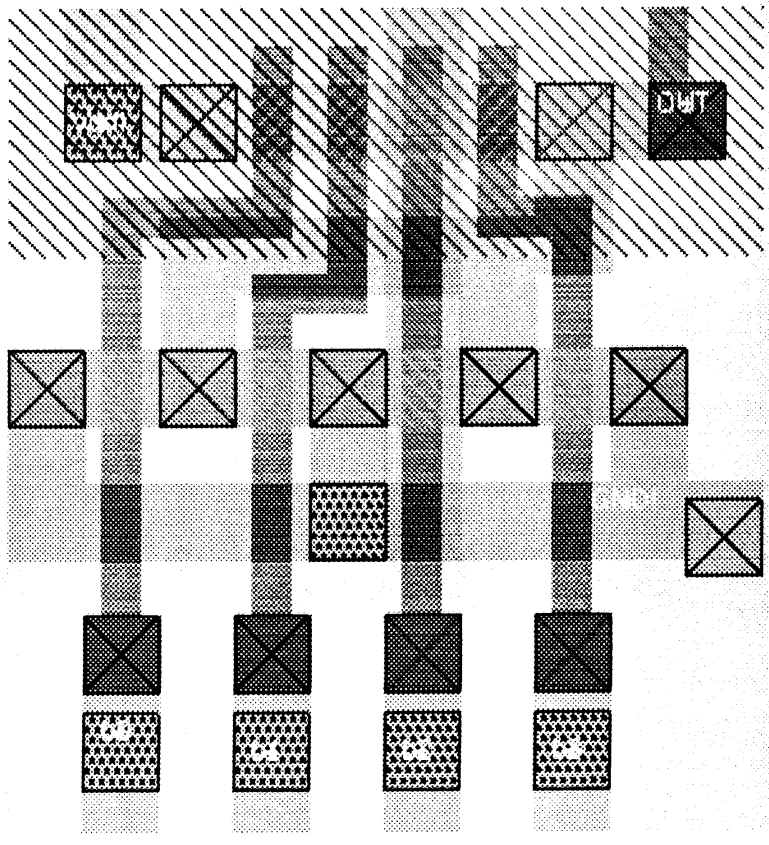

Fig. 2.6: Circuit layout of column decoder

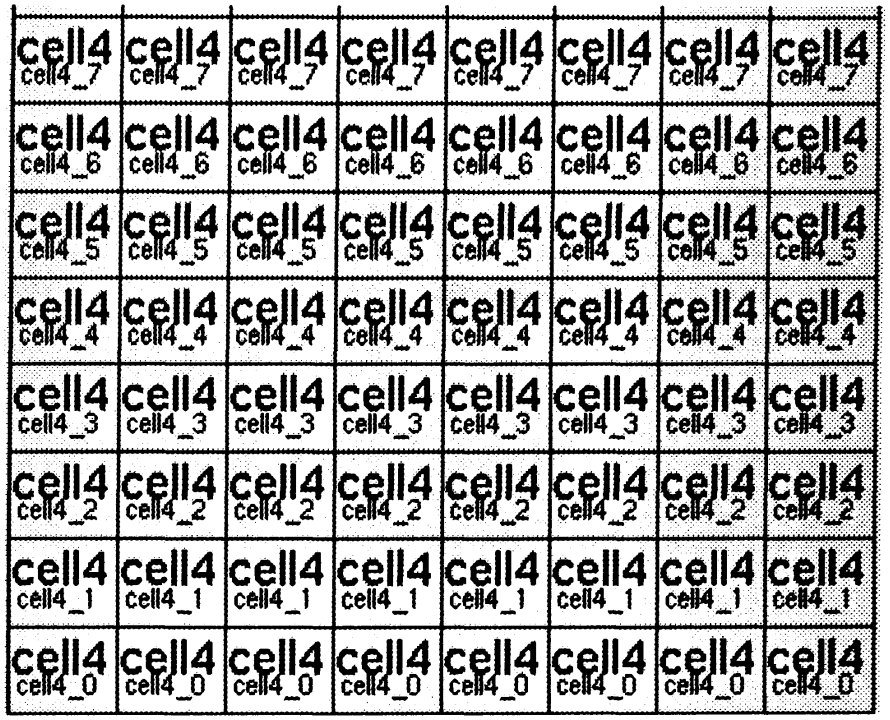

Fig. 2.7: Floor plan of 16x16 memory cell array

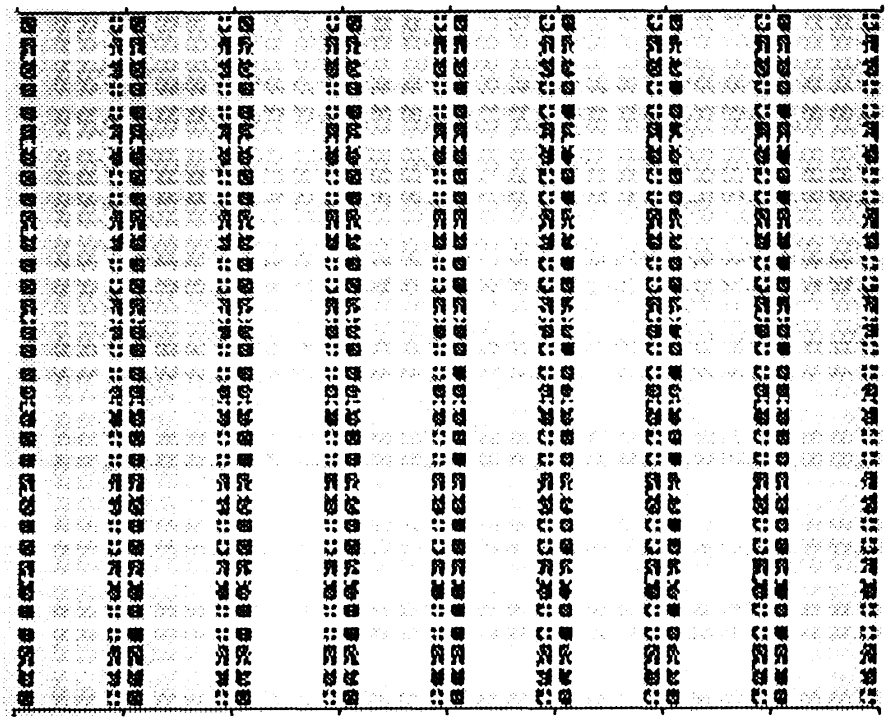

Fig. 2.8: Circuit layout of 16x16 memory cell array

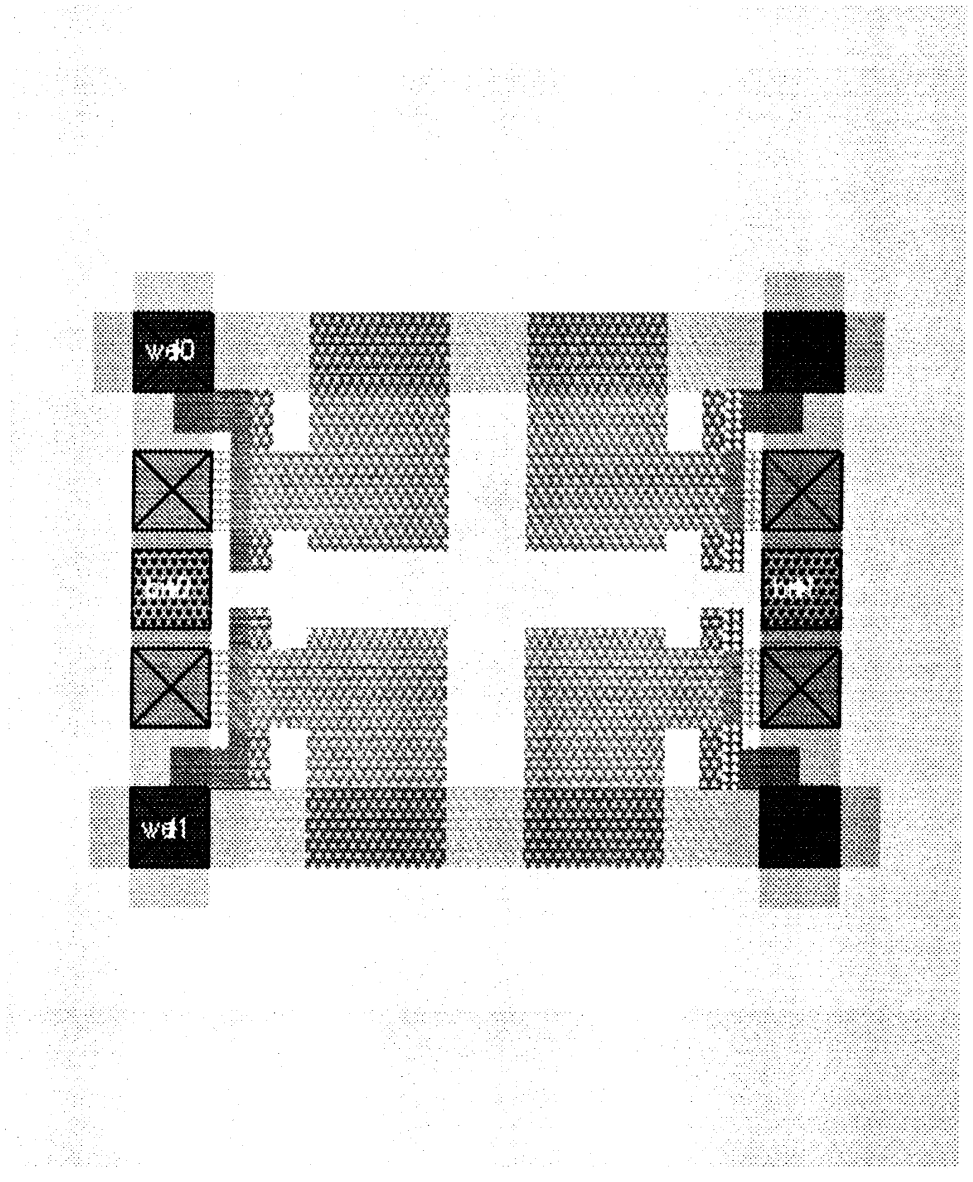

Fig. 2.9: Circuit layout of 4 basic memory cells. Design rule error occurs due to overlaping of poly1 and poly2.

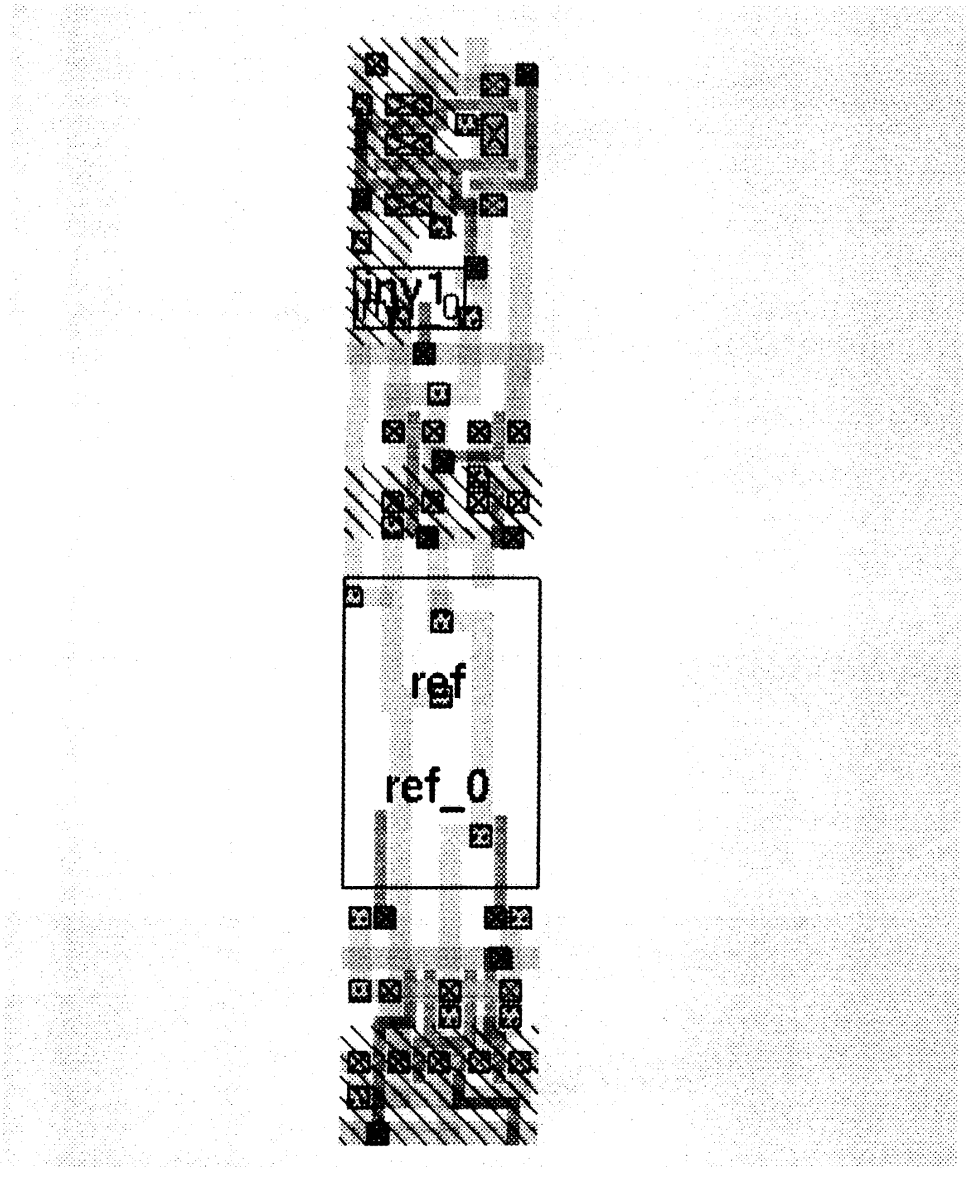

Fig. 2.10: Circuit layout of read/write and refresh circuitry

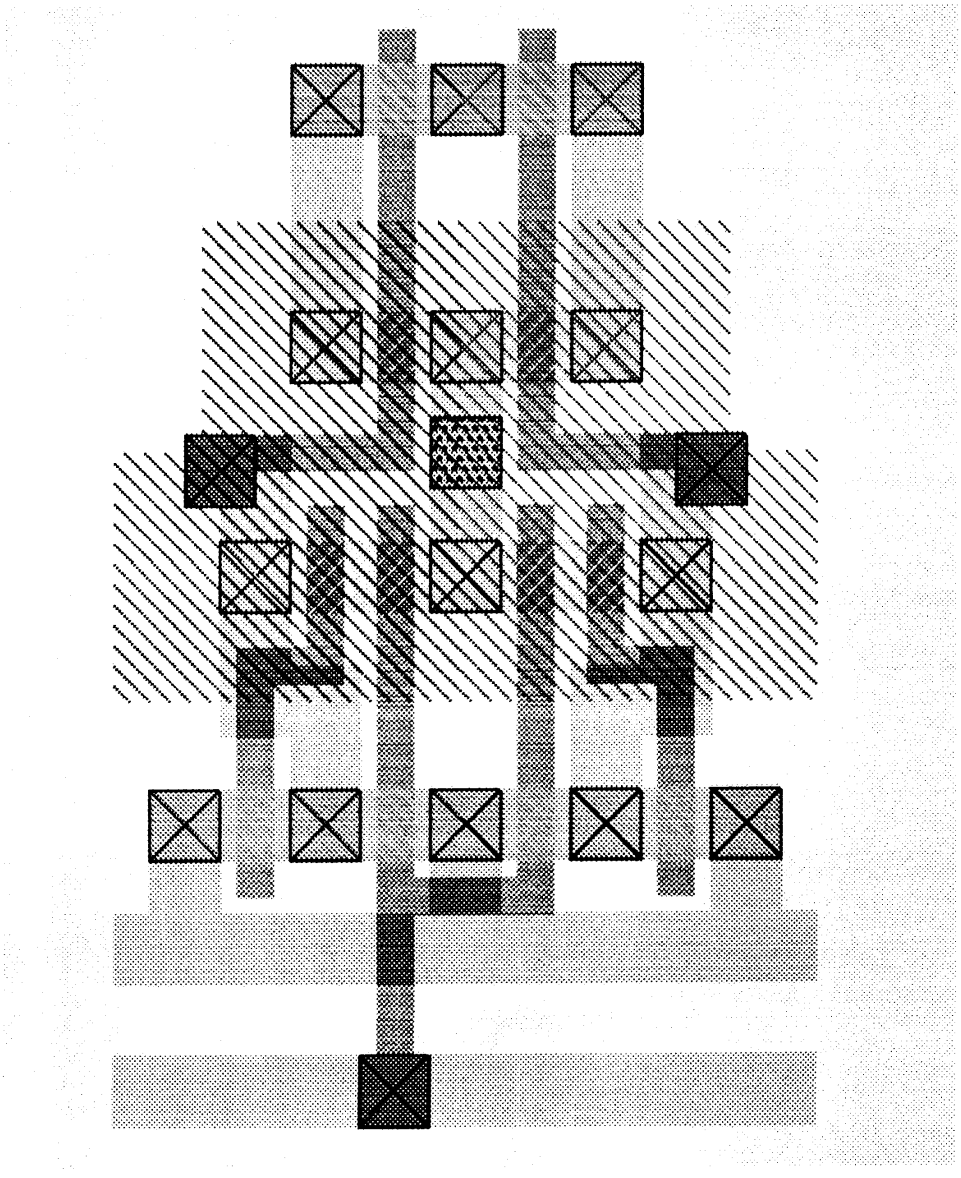

Fig. 2.11: Circuit layout of refresh control

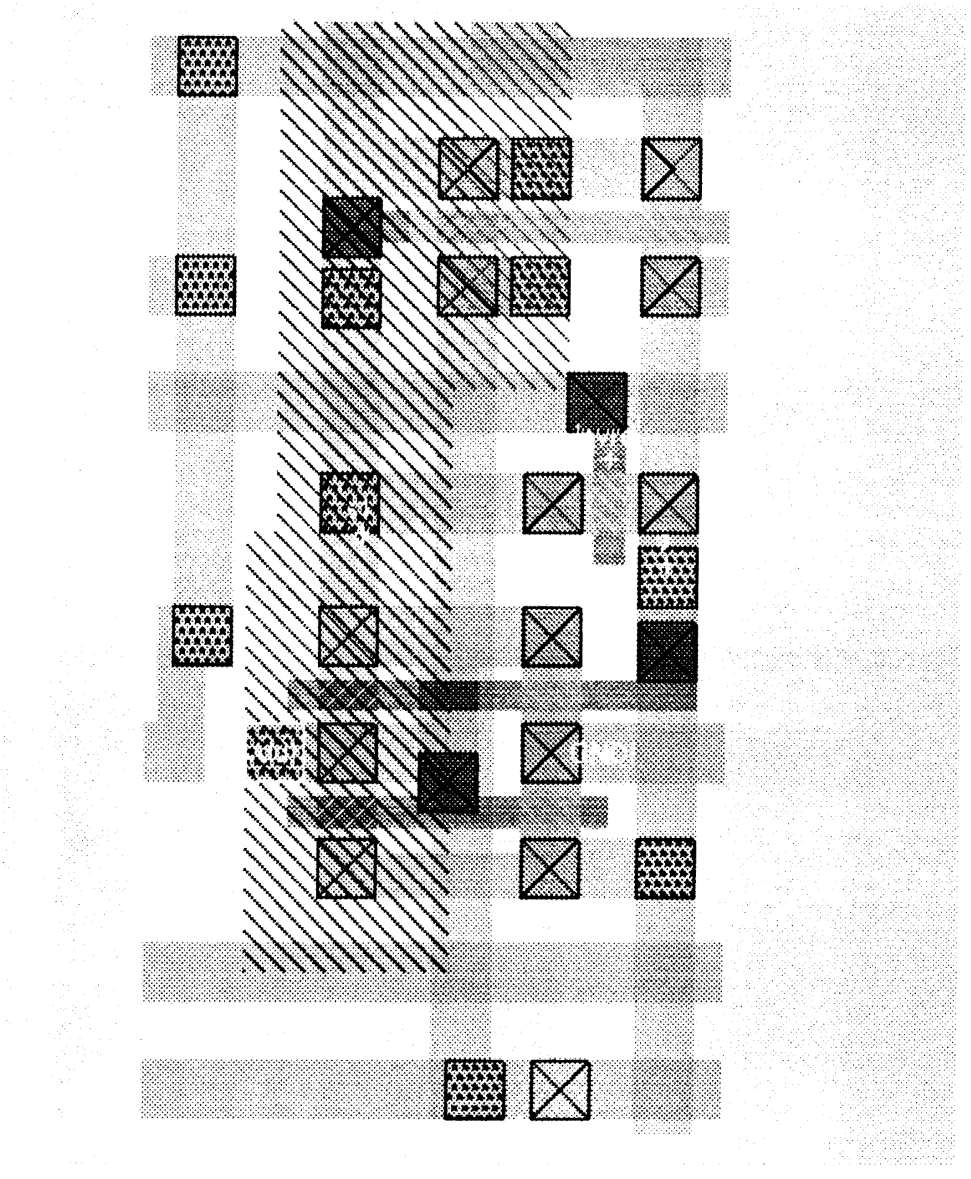

Fig. 2.12: Circuit layout of precharge control and sense amplifier

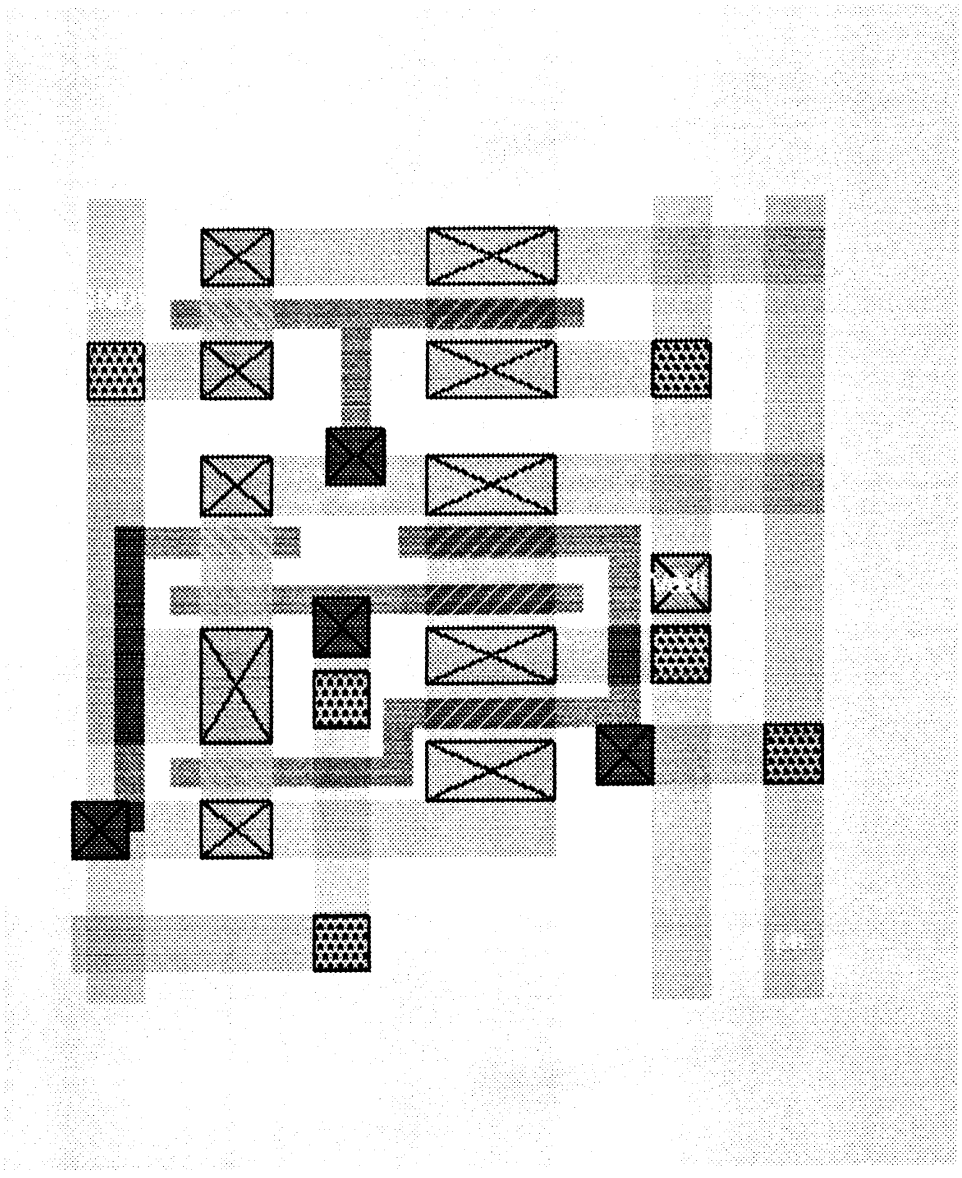

Fig. 2.13: Circuit layout of tri state switch

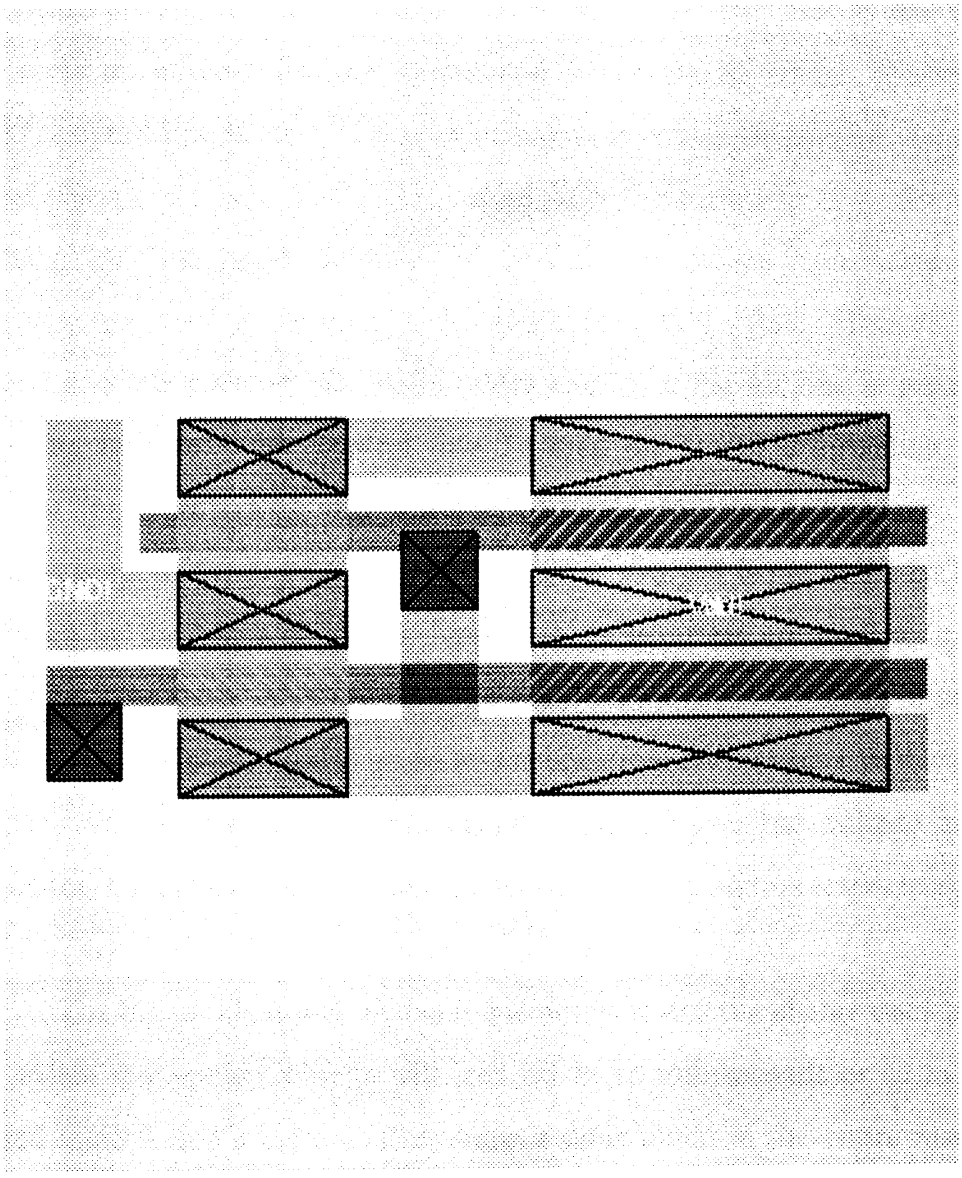

Fig. 2.14: Circuit layout of buffer

INPUT / OUTPUT OPERATIONS:

First, the $\overline{RAS}$ control line is set to high to precharge the row decoder . Then $\overline{RAS}$ and $\overline{CAS}$ control lines are turned low and desired row and column addresses are applied to select a particular cell. The $\overline{read}$ line is also set to low. To write an information, the information is applied at **DATA IN** line and the **R/**$\overline{W}$ control line is set to low with selecting desired word and bit line. All of the input signals are held stable for a short time. This permits the address control signals, and data input to propagate through the circuits with RAM. After the interval, the word is selected at the address location. Thus information will be stored into the selected cell. After Write operation the bit line is precharged by applying high to $\overline{read}$ control line To read the stored information the R/$\overline{W}$ control line is set to high with selecting particular row and column line. This time no data is applied to **DATA IN** line. The stored charged is put in the bit line and is detected by the sense amplifier. Back to back inverters are used to make sense amplifier. The sense amplifier senses a small differences of voltage in the bit line. The voltage difference ΔV is given by the equation, $\Delta V = (Vbit - Vs)Cs/(Cs+Cbit)$. Where, Vbit is the bit line precharge voltage, Vs is the voltage across cell capacitor, Cs and Cbit are the capacitances of cell and bit line respectively.

The big problem with dynamic memories is that the charge does leak off, to the extent that enough charge will leak off in 10 milliseconds or so to convert a stored logic 0 into a logic 1. If nothing is done about it, the entire memory will

revert to the discharged state, where all bits will be read as 1's. The reading is also destructive; after reading the information must be immediately stored. So, after writing a 0 into a cell or reading from a cell, the cell must be refreshed by applying high to the refresh control line **(F).** During the refresh cycle the memory can not be read or written into [6].

CHAPTER III

CIRCUIT ANALYSIS AND RESULTS

The RAM circuit contains storage capacitor. So it can not be simulated by using irsim simulator. Again, there are lot of transistors in the circuit, so the whole circuit can not be simulated by using spice. Therefore, a part of the circuit is chosen to be simulated (as shown in fig. 3.1) by using spice.

Fig. 3.2(a) and 3.2(b) show the precharging of bit line by applying logic high to the $\overline{\text{READ}}$ and **F** control line. It is shown that bit line is precharged to 2.1volts. The bit line is precharged after writing '0' or '1. It takes almost 7 ns to precharge the bit line.

Fig. 3.3(a) shows the **write '0'** operation. Write '0' operation is performed by setting the $\text{R}/\overline{\text{W}}$ control line at low, the $\overline{\text{READ}}$ at low, the **F** at low and applying low signal input to **DATA IN** line and selecting desired row and column line. It takes about 2.5 ns to write '0' into the cell.

Fig. 3.3(b) shows the write '1' operation. This is done by setting the $\text{R}/\overline{\text{W}}$ control line at low, the $\overline{\text{READ}}$ at low, the **F** at low and applying high signal input to **DATA IN** line and selecting desired row and column line It takes about 3 ns to write '1' into the cell.

Fig. 3.4(a) shows the **read '0'** operation. Read '0' operation is performed by setting the $\overline{R/W}$ line high, the $\overline{READ}$ low, the **F** at low and selecting row and column line. This makes a change in voltage in the bit line and the stored charge in the cell is sensed at the **DATA OUT** line by the sense amplifier. It takes about 6 ns to read '0'.

Fig. 3.4(b) shows the **read '1'** operation. Read '1' operation is performed by setting the $\overline{R/W}$ line high, the $\overline{READ}$ low, the **F** at low and selecting row and column line. The stored charge is sensed at **DATA OUT** line by the sense amplifier. It takes about 6 ns to read '1'.

When there is no read/write operation the F control is set to logic high. So, if there is any voltage change in the bit line it will refresh the memory cell. The refreshing occurs every few milliseconds.

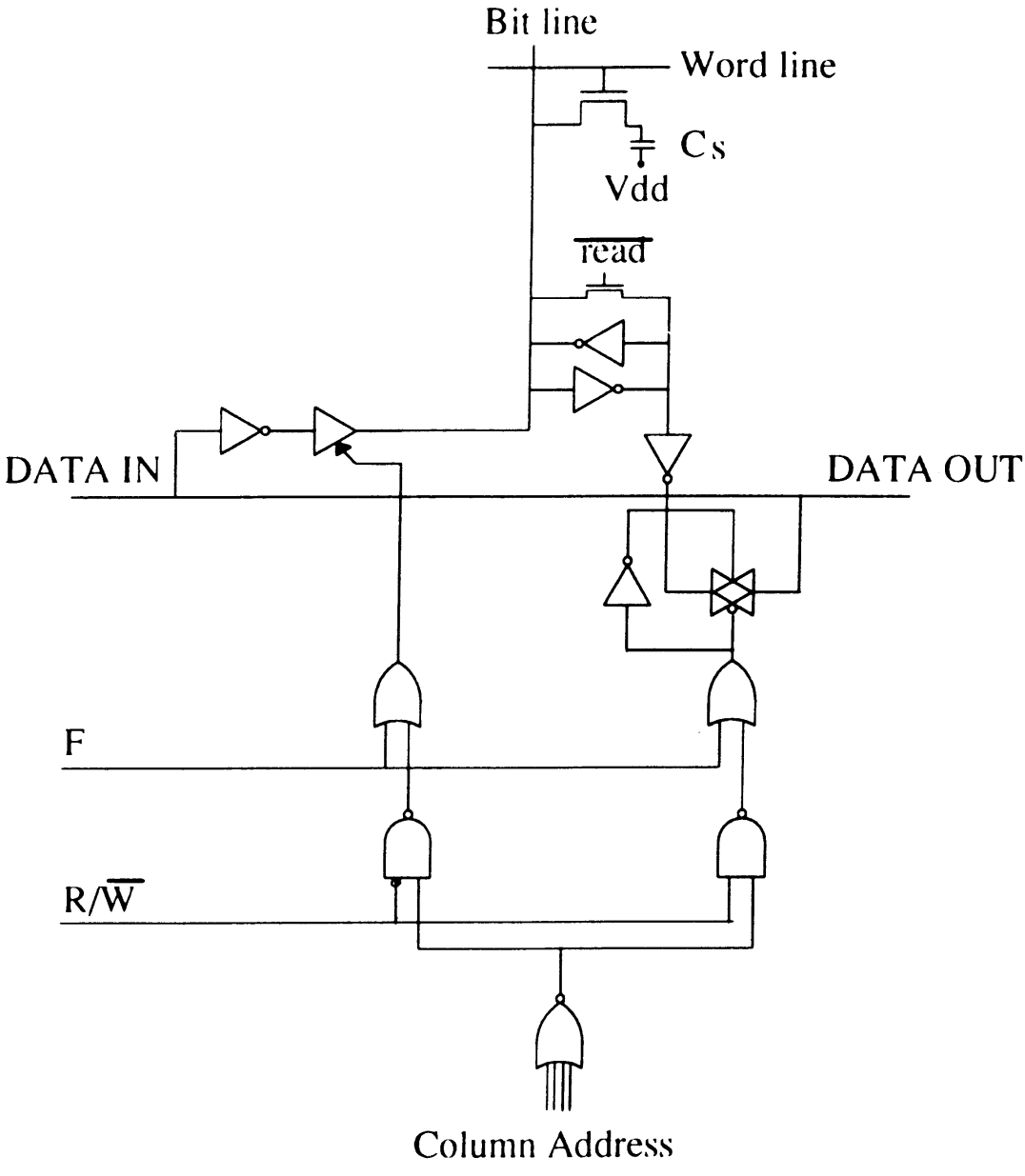

Fig. 3.1: Read/Write and Refresh circuitry with single memory cell

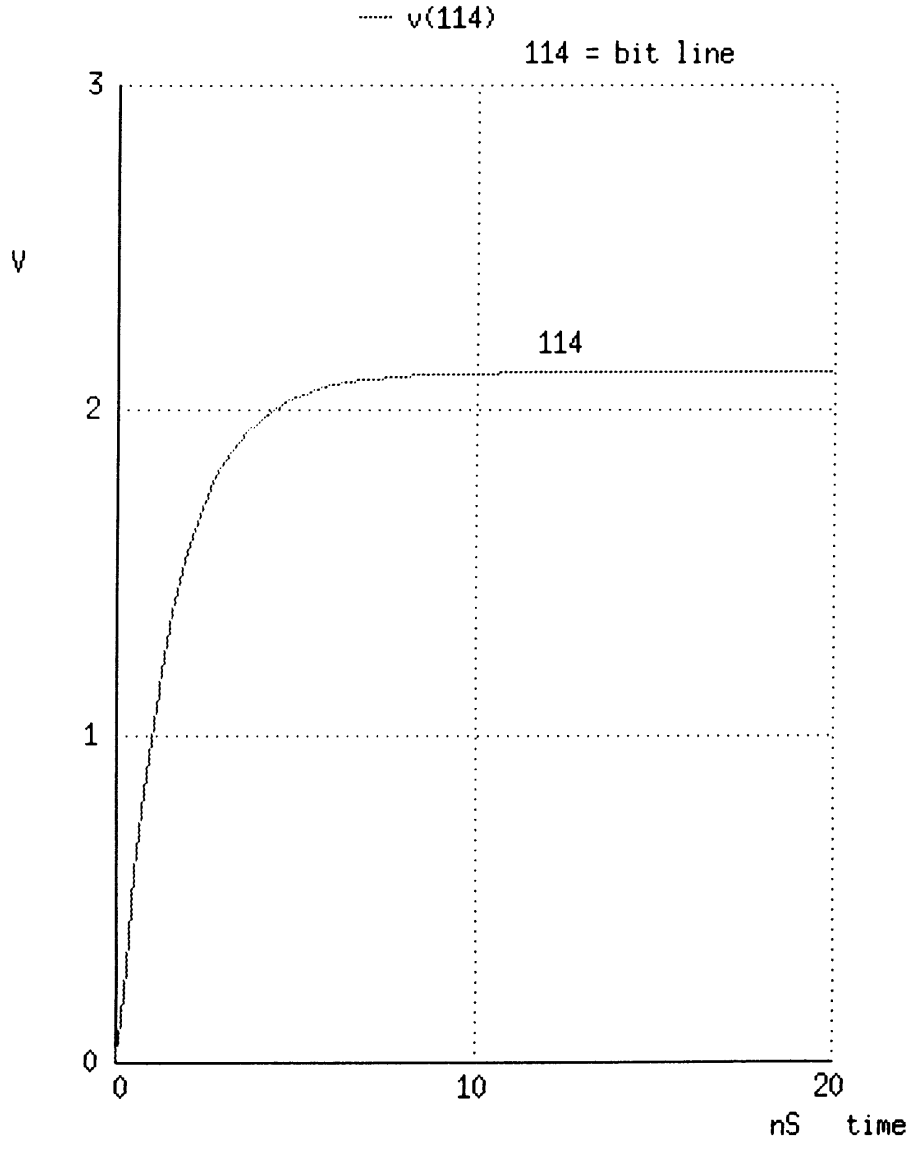

Fig. 3.2(a): Plot of precharging the bit line after writing '0'

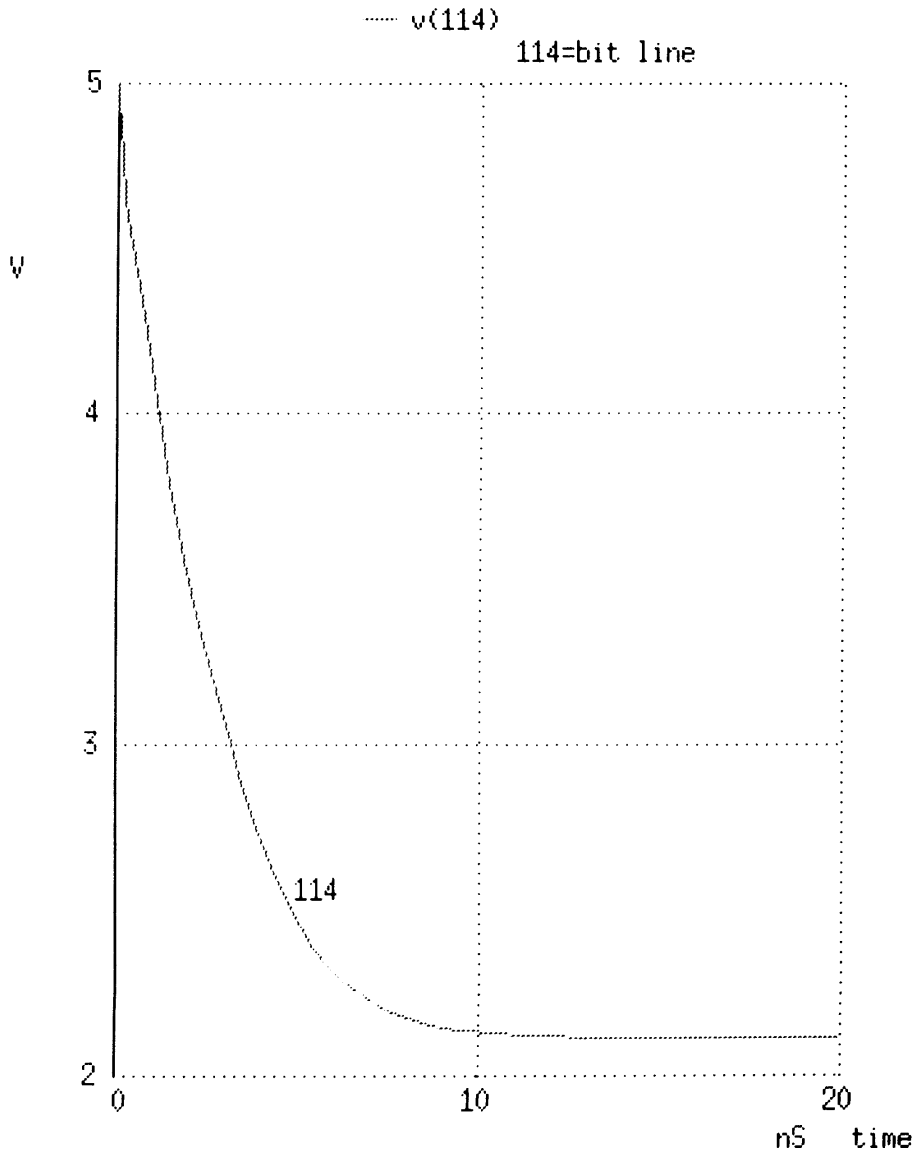

Fig. 3.2(b): Plot of precharging the bit line after writing '1'

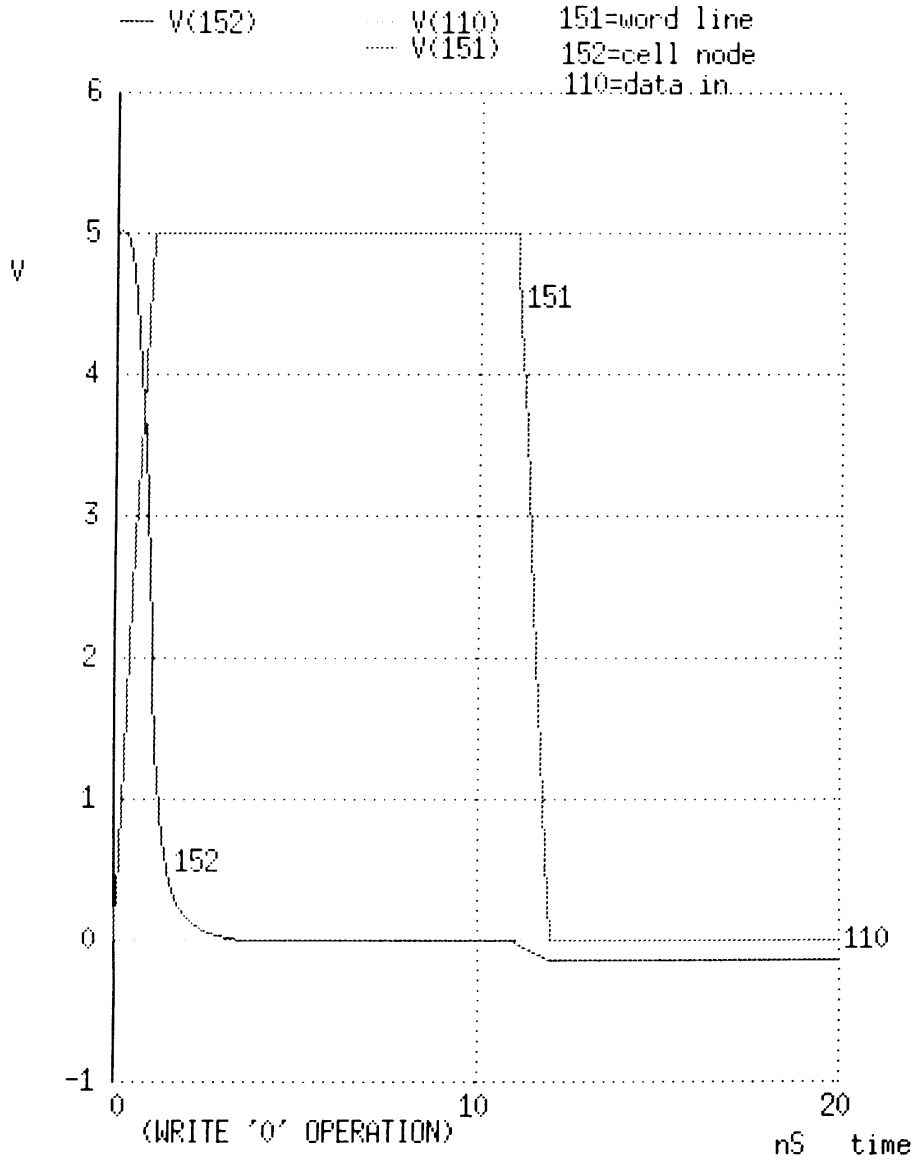

Fig. 3.3(a): Plot of Write '0' operation of RAM

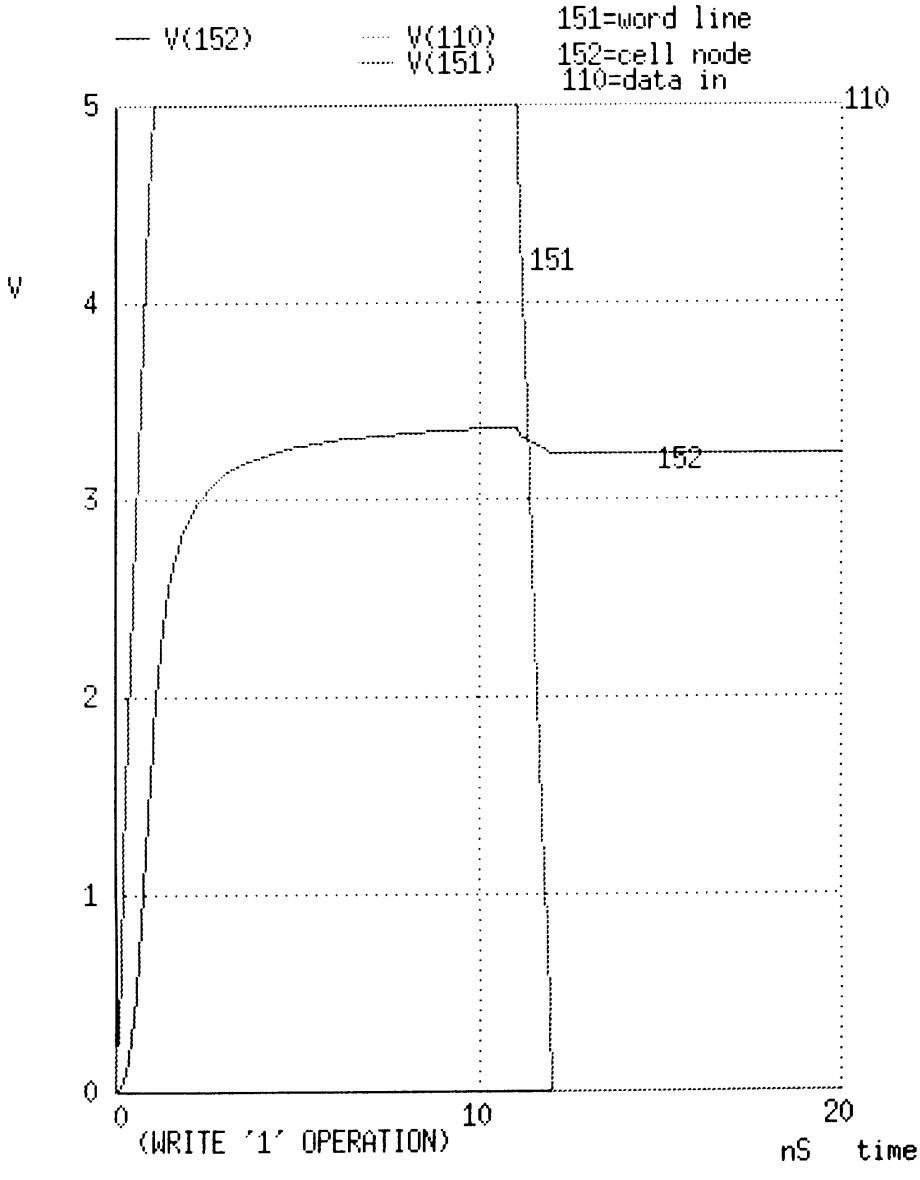

Fig. 3.3(b): Plot of Write '1' operation of RAM

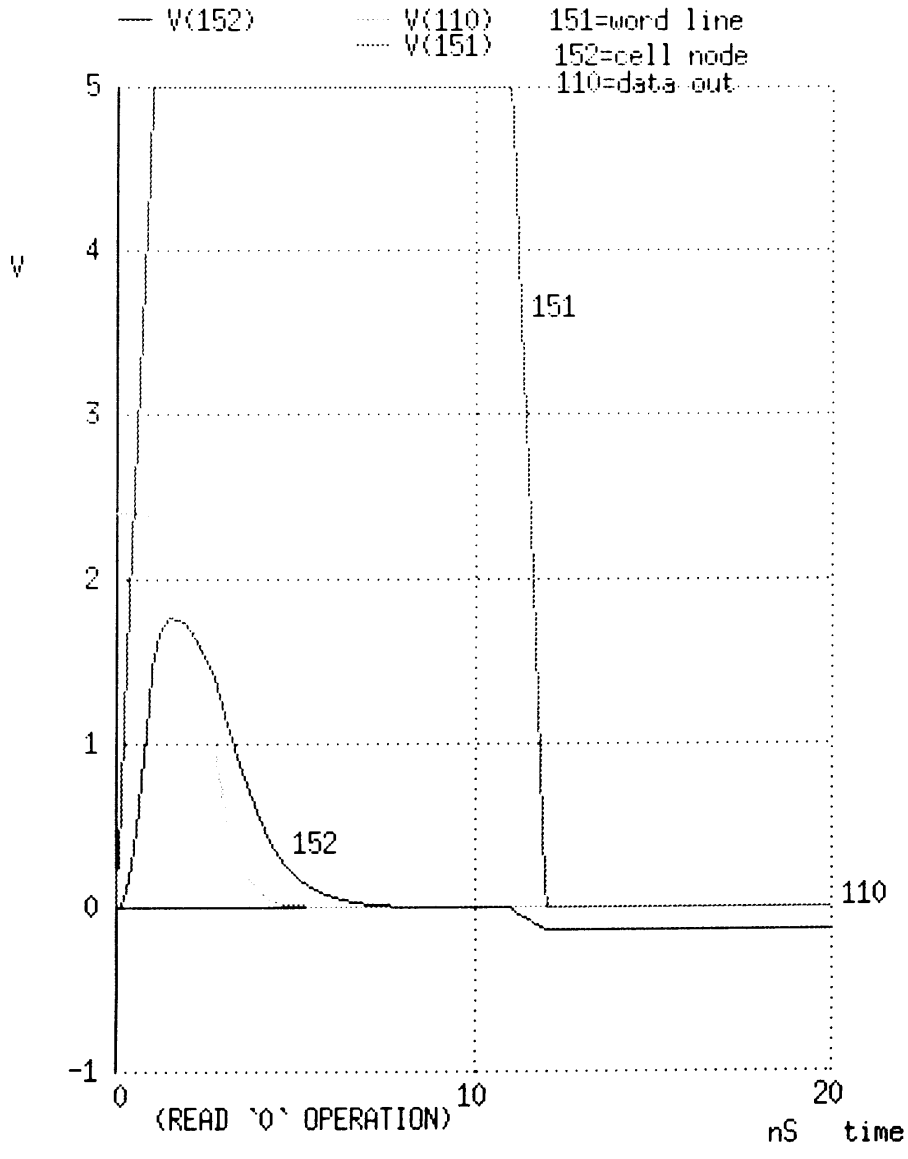

Fig. 3.4(a): Plot of Read '0' operation of RAM

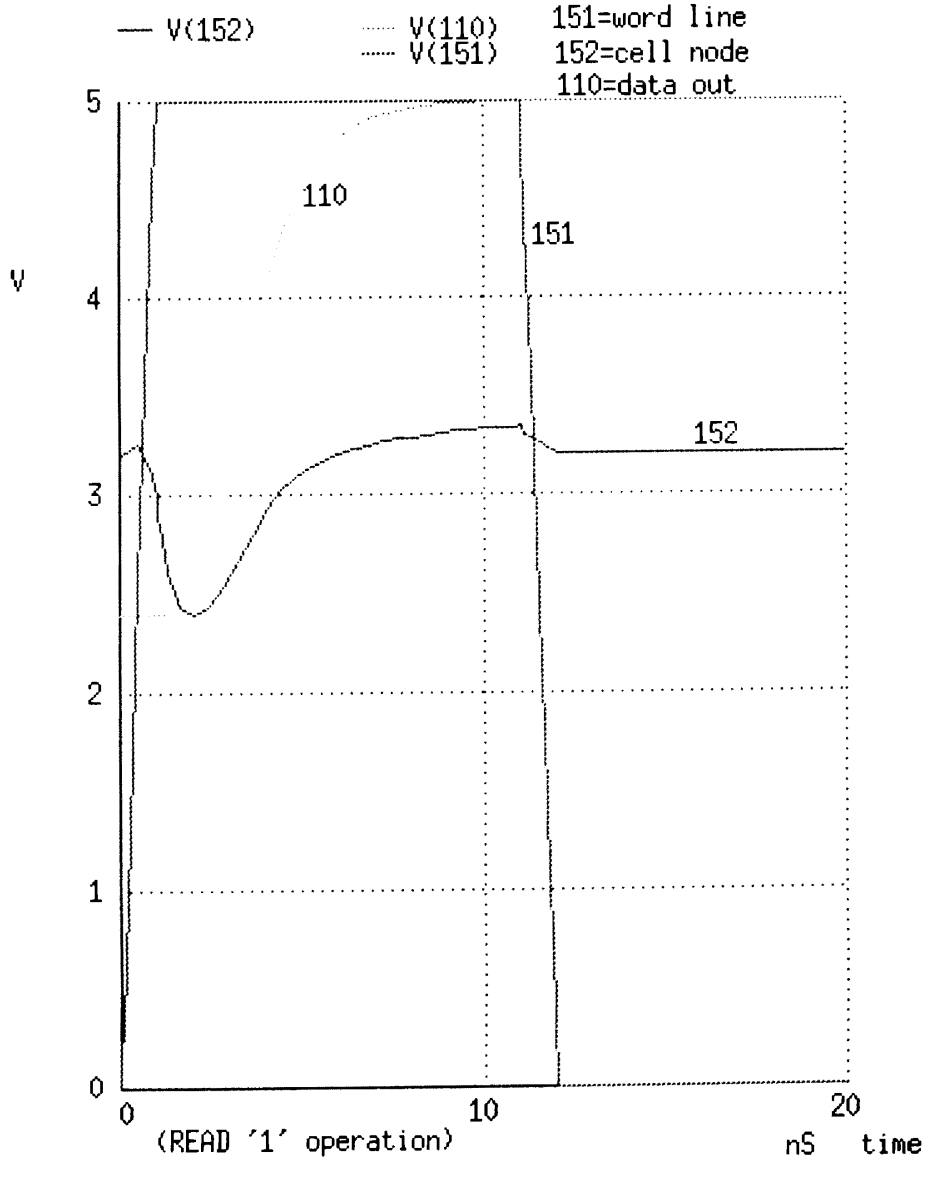

Fig. 3.4(b): Plot of Read '1' operation of RAM

CHIP TEST AND RESULTS

The top view of the chip is shown below:

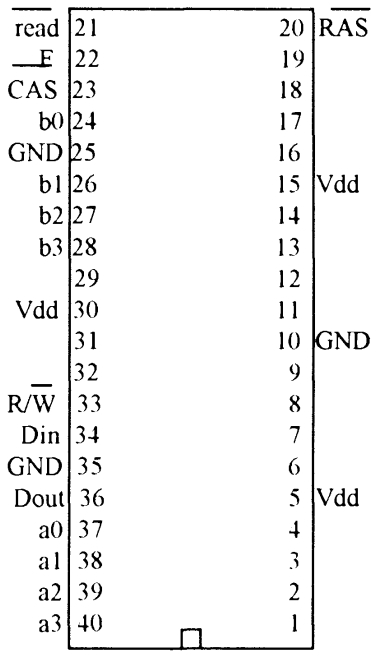

Fig. 35: Top view of the chip (256x1 single transistor dynamic RAM)

a0, a1, a2, a3 are row addresses and b0, b1, b2, b3 are column addresses.the $\overline{RAS}$ and the $\overline{CAS}$ are used to control the row and column addresses respectively,the F control line to control refresh operation, the $\overline{read}$ control line to precharge the bit line, the $\overline{R/W}$ to control write and read operation,the Din line to applied data input and the Dout to read the stored data out.

The chip was tested using VLSI tester II. The chip pin numbers and the corresponding ZIF socket numbers are shown below:

Chip pin #	ZIF socket #	Chip pin #	ZIF socket #
1	1	21	29
2	2	22	30
3	3	23	31
4	4	24	32
5	5	25	33
6	6	26	34
7	7	27	35
8	8	28	36
9	9	29	37
10	10	30	38
11	11	31	39
12	12	32	40
13	13	33	41
14	14	34	42
15	15	35	43
16	16	36	44
17	17	37	45
18	18	38	46
19	19	39	47
20	20	40	48

The following are the chip test data file, output response file and output error file. Data file for one single cell test is shown. Tests were done for all the cells. No errors were found.

```
DATA FILE FOR READ/WRITE OPERATION TEST
---------------------------------------

45 1
46 2
47 3
48 4
32 5
34 6
35 7
36 8
20 9
29 10
30 11
31 12
41 13
42 14
44 15

d 0000 0000 0 0 0 0 0 0 1
t 0011 0011 0 0 0 0 0 1 1
t 0011 0011 0 1 1 0 1 1 1
t 0011 0011 0 0 0 0 1 1 1
t 0011 0011 0 0 0 0 0 0 0
t 0011 0011 0 1 1 0 1 0 0
t 0011 0011 0 0 0 0 1 0 0
```

OUTPUT RESPONSE FILE FOR READ/WRITE OPERATION

```
4
4
4
3
3
3
3
2
2
3
3
4
4
4

d
t 0011 0011 0 0 0 0 0 1 1
t 0011 0011 0 1 1 0 1 1 1
t 0011 0011 0 0 0 0 1 1 1
t 0011 0011 0 0 0 0 0 0 0
t 0011 0011 0 1 1 0 1 0 0
t 0011 0011 0 0 0 0 1 0 0
```

OUTPUT ERROR FILE FOR READ/WRITE OPERATION

```
4
4
4
3
3
3
3
2
2
3
3
4
4
4

d
t 0000 0000 0 0 0 0 0 0 0
t 0000 0000 0 0 0 0 0 0 0
t 0000 0000 0 0 0 0 0 0 0
t 0000 0000 0 0 0 0 0 0 0
t 0000 0000 0 0 0 0 0 0 0
t 0000 0000 0 0 0 0 0 0 0
```

CONCLUSIONS

In order to maximize the number of bits that can be memorized in a certain chip area, the basic cell must be as simple as possible. The basic cell of single transistor dynamic RAM is small and a very dense array can be made. Therefore, single transistor dynamic RAMs have a lower cost per bit than memories with less compact arrays.

The design was compact. The ratio of bit line capacitance to memory cell capacitance was such that the size of the memory array could be made about ten times bigger than the existing one.

The chip was tested using VLSI digital tester II and no errors were found. Therefore, it can be concluded that in designing memory cell the poly1 and poly2 can be overlapped by one lambda to save area.

But the chip test results might be wrong due to the fact that the data input and output lines were shorted. So, during read operation data input might influence the data output. This drawback of the design could be overcome by passing the data input through a tri-state switch. So, during read operation the data input would not affect the data output.

REFERENCES

1. Randel, B. and Treleaven. VLSI Architecture. University of Bristol, 1982. p 44-53.
2. Einspruch, Norman G. VLSI HANDBOOK. 1985. p 151-159.
3. Mukherjee, Amar. Introduction to nMOS & CMOS VLSI systems design. 1986. p 100-104, 262-277.
4. Triebel, Walter A. and Chu, Alfred E. Handbook of Semiconductor and Bubble Memories. Prentice-Hall, INC. 1982. p 111-167.
5. Price, Betty and Due-Gundersen, Gunnar. Semiconductor Memories. 1983. A wiley-Interscience Publication. p 48-75.
6. Williams, Gerald E. Digital Technology. Third edition. 1986. Science research associates, Inc. p 451-465.
7. Weste, Neil H. E. and Eshraghian, Kamran. Principles of CMOS VLSI Design. Addison-wesley Publishing Company. p 348-363.
8. Joshi, P. C. and Krupanidhi, S. B. Journal of Applied Physics. 73Jun1 1993. p 7627-34.'
9. Sydnor, Alvin G. Radio Electronics. v.61 Dec. 1990. p 89.
10. Denning, Peter J. American Scientist. v.74 March/April 1986. p 126-7
11. Robinson, Arthur L. Science. v.224 May 11 1984. p 590-2.
12. Bywater, R. E. H. Hardware / Software Design of Digital Systems. 1981. Prentice Hall international, Inc. p 96-104.
13. Mazumder, Pinaki. IEEE Journal of Solid State Circuits. v 23 Aug. 1988. p 933-41.

14. Lydic, John W. Jr. EDN. v.32 oct. 15, 1987. p 198+

VITA

MKM NASIM UDDIN

Candidate for the degree of

Master of Science

Thesis: **DESIGN AND FABRICATION OF 256X1 SINGLE TRANSISTOR DYNAMIC RAM**

Major Field: Electrical Engineering

Biographical:

Personal Data: Born in Bhola, Bangladesh, on November 15, 1966, the son of AKM Ali Hossain and Khadija Khatun.

Education: Graduated from Mirzapur Cadet College, Bangladesh, in September 1984; received Bachelor of Science degree in Electrical & Electronic Engineering from Bangladesh University of Engineering & Technology, Dhaka, Bangladesh in May 1991. Completed the requirements for the Master of Science degree with a major in Electrical Engineering at Oklahoma State University in July 1994.

Experience: Teaching Assistant, Department of Electrical & Computer Engineering, Oklahoma State University, August 1993 to May 1994.

Professional Membership: Institute of Electrical & Electronics Engineers (IEEE).