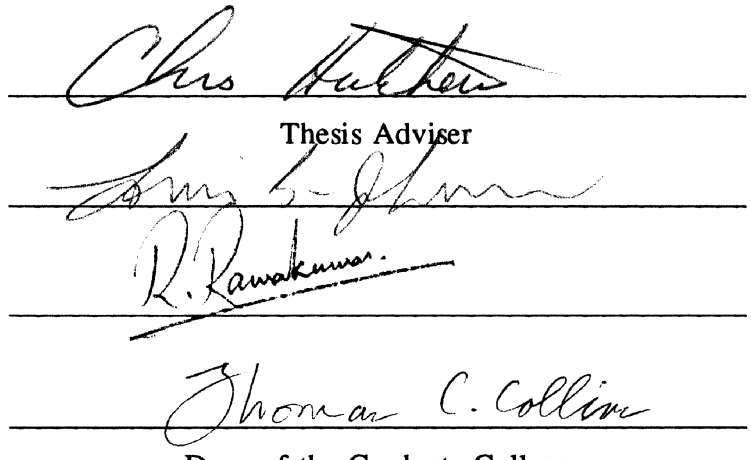
A PROPOSED ARCHITECTURE FOR A HALL

EFFECT BASED NONVOLATILE MEMORY

BASED ON THINFILM SOS

Thesis Approved:



Thesis Adviser

Dean of the Graduate College

PREFACE

Non-volatile memory has many desirable features. Demand for these features inspired us to develop a new kind of non-volatile memory i.e. Magneto Hall effect Random Access Memory (MHRAM) which should have the advantages of magnetic core memory, high density, high speed and anticipated low cost. This thesis implements the building blocks required for the realization of the read and write paths including memory using Thin Film Silicon On Sapphire (TFSOS) technology. A novel layout approach to minimize the offset voltage was also implemented. All the building blocks were designed and verified by simulating on Honeywell SPICE (HSPICE) and fabricated on TFSOS. Testing of all these blocks was completed with the result indicating that this memory has a potential future use if slight modifications in the design are completed.

First and foremost I would like to express my sincere gratitude to my major advisor, Dr. Chriswell Hutchens for his invaluable inspiration, guidance and constant encouragement which kept me motivated throughout the course of the project. I am again thankful to him for providing me with this research opportunity and exposing me to NRaD facilities at San Diego. The practical experience I gained at NRaD, San Diego was invaluable.

I would like to thank Tom Schmitt for his valuable guidance and support

during my stay in San Diego. I thank the office of NRaD, San Diego for the computing resources and financial support provided by them for this project.

I express my sincere appreciation to Dr. Louis Johnson for his advice in the field of VLSI and constant encouragement. I also thank Dr. R. Ramakumar for serving on my supervisory committee.

I thank all my colleagues in research group and friends who have helped me to complete this work. Finally, I owe deep sense of gratitude to my parents Prakash Shah and Dipika Shah, my brother Nimish, my sister in law Manisha and my wife Jigna without whose moral support and affection this work could not have been a success.

TABLE OF CONTENTS

Chapter Page

LIST OF TABLES

LIST OF FIGURES

NOMENCLATURE

EEPROM	electrically erasable programmable read only memory
SNOS	silicon nitride oxide semiconductor
FRAM	ferro-electric random access memory
MRAM	magneto-resistive random access memory
MHRAM	magnetic hall-effect random access memory
NDRO	non-destructive readout
DDP	double differential pair
ΔR	fractional change in resistance
R	Resistance
μ	mobility
B	B magnetic field
V_H	hall voltage
VH	hall voltage
V_{mag}	magneto-resistive voltage
I	current
TSOS	thinfilm silicon on sapphire
e	magnitude of the charge on the carriedr
υ	draft speed

$\mathcal{E}$	electric field
w	distance between two tapped points VHA and VHB
J	current density
ρ	charge density
t	thickness of inversion layer
R_H	hall coeffiecient
ΔV	overdrive voltage
ΔI	difference of current in two arms
V_{INM}	difference in input
r_{out}	output resistance
C_{out}	output capacitance
GBP	gain bandwidth product
BW	bandwidth
H	drive field
C	circumference of toroid
V_{OS}	offset voltage

CHAPTER I

INTRODUCTION

Non-Volatile Memory

Non-volatile memory is used for a wide range of military and commercial applications. Not a single non-volatile memory has achieved universal application without tradeoffs, in either power, density, performance or radiation hardness [1]. Non-volatile memory is essential because data can be lost in the event of a power failure or due to radiation exposure (high flux charged particles).

In this section different types of non-volatile memories are introduced and compared. This is followed by the rationale for choosing hall-effect based non-volatile memory from several potential memories.

Comparison of Non-volatile memory

A complete list of non-volatile memory includes Magnetic core memory, EEPROM (Electrically erasable programmable read only memories), Flash EEPROM, SNOS (Silicon-nitride-oxide-semiconductor), FRAM (Ferroelectric random access memory), MRAM (Magneto-Resistive RAM) and MHRAM (Magnetic Hall effect RAM). In the following section , the advantages, disadvantages and areas of applications will be presented in an outline format.

Magnetic Core Memory:

Advantages: Non-volatility,unlimited read/write cycle and inherent resistance to radiation.

Limitations: Low density, low speed, high cost and power hungry for modern systems.

Applications: It is widely used for all kinds of applications including shipboard and airborne computers.

EEPROM:

Advantages: 5-V programmability with no need for erasure before programming, byte and page mode write operations, low power, moderate density, data protection lockout and non-volatility under the severe military temperatures specifications.

Limitations: Low write speed, moderate access time, moderate endurance, density limitations, radiation hardness, low component yield due to complicated manufacturing and hence the high cost.

Applications: Many areas of data recording including reprogrammable program memory and storage of pointers and processors information prior to losing system power. It is used where the need for storing data under the extreme conditions of mechanical shock and temperature are present.

Flash EEPROM:

Advantages: Low cost, high density, high yield, reasonably high endurance and incircuit eraser and reprogrammability.

Limitations: Erase/Reprogrammability process, separate erase/reprogram voltage, moderate access time and limited radiation hardness.

Applications: Replacing EEPROM's depending upon the requirements.

SNOS (Silicon-nitride-oxide-semiconductor):

Advantages: 5 V only operation, extremely high endurance (wear out is related to power ON/OFF cycles), high speed access, low power and radiation hardness.

Limitations: High cost and density.

Applications: Program memory, data recording, replacing core memory and also is used for wide range of applications that utilize battery backed SRAM, however SNOS requires a reliable means for long term storage.

Ferro-Electric RAM:

Advantages: High density, access and write time are comparable with advanced processors speed and has superior radiation hardness.

Limitations: Durability and retention.

Applications: Data recording, bulk storage, replacing core memory depending upon requirements, wide range of applications in space and nuclear environment.

Magneto-Resistive RAM:

Advantages: Fast write time, Non-destructive readout (NDRO) method, radiation hardness, durability, retention and ease of integration.

Limitations: Low sense level of signal resulting in either long access time or large

areas.

Applications: Radiation hardened related applications.

Hall-Effect RAM:

Advantages: Fast write time, Non-destructive readout (NDRO) method, radiation hardness.

Limitations: Low sense level of signal voltages resulting in either long access time or large areas. Manufacturing process is difficult for hall sensors.

Applications: Radiation hardened related applications.

Both ferro-electric memory and magneto-resistive memory require further material development. The ferro-electric material must overcome fatigue, while MRAM must overcome the associated problem with a small sense signal. In the Table 1 [1] key characteristics of non-volatile memory are listed in tabular form. The potential candidates for our applications selected from the table are MHRAM and MRAM. The reasons fot their selection are they are faster then magnetic core memory, radiation hardened and the cost is potentially low. Ultimately the ideal non volatile RAM would have the density and cost of dynamic RAM, the access time of SRAM and the non-volatility and endurance of magnetic core memory.

Hall-effect based non-volatile memory

We have been constrained to the use of thin film silicon on sapphire (TSOS) for the development of a non-volatile memory system by NRaD. This memory should have the advantages of core memory with anticipated reduced cost, high density and high speed. There were two potential available options which fill the opportunity.

Non-Volatile Memory	SPEED (Access time)	Write time	Endurance	Radiation Hardness	Limitations	Cost
EEPROM	150 nS	10 mS byte / page	10^4 - 10^5 write cycles	Low - Moderate	Write Speed, Endurance	Moderate
FLASH EEPROM	120 nS	High	10^4 write cycles	Low - Moderate	Write Speed, Endurance	Low
SNOS	35 nS	SRAM write 35nS, download 11 mS	10^5 power cycles	Moderate	Density	Moderate to high
FRAM	100 nS	200 nS	10^{10} read/write	High	Endurance, Bit removal phenomena	Potentially Low
MRAM	Density depend 0.2-2 µS	100-200 nS	No known limitations	High	Read Speed and Endurance	Potentially Low
CORE	350 nS	900 nS	No limits	Moderate to High	Speed, Density and Power	High
MHRAM	Density depend 0.1-1 µS	50-100 nS	No known limitations	High	Read Speed and Endurance	Potentially Low

Table 1 Key Characteristics of Non-volatile Memory [1]

1. Magneto-Resistive RAM (MRAM).

2. Magneto-Hall Effect RAM (MHRAM).

The functions and advantages of the two would be discussed below. Magnetoresistive memory is dependent on change of resistance. This change of resistance is a function of the mobility and B-field as shown by Equation 1.

$$\frac{\Delta R}{R} \equiv (\mu B)^2 \tag{1}$$

where

$\Delta R/R$ is the fractional change in resistance per resistance,

μ is the mobility and

B is the B magnetic field.

An MHRAM is based on the principle of hall-effect which will be explained in greater detail in section 2.1. The hall voltage V_H is dependent on mobility and B field as shown in Equation 2

$$V_H \alpha B\mu \tag{2}$$

The magnetoresistive voltage is written as,

$$V_{mag} = \Delta R I \tag{3}$$

where

I is the current flowing through the magnetoresistive resistance.

From Equation 1 and 3 we have,

$$V_{mag} = R(\mu B)^2 I \tag{4}$$

and from Equation 2 and 4 we have,

$$\frac{V_H}{V_{mag}} \alpha \frac{1}{\mu B R I} \tag{5}$$

If the ratio in Equation 5 is greater than 1, MHRAM should be selected while for the values of Equation 5 less than 1, a MRAM should be the solution, for reasonable values of R, I, μ and B. For practical field strengths and easily achieveable geometries and mobility, MHRAM should be much more sensitive then MRAM resulting in better read access time. In addition, Hall effect offers better performance in terms of simpler circuits and a stronger read signal. For these reasons the hall approach was selected over the magneto resistive approach.

The limitation of the hall approach is low speed due to low signal levels. But it provides better performance than MRAM in read/write currents, read signal strength and density. We can partially compensate for the speed loss by using multistage amplifiers. The gain of the amplifier is selected to provide minimum delay and optimal bandwidth. The approach and functionality of sensing MHRAM signals is presented in the following sections. For the MHRAM design n-type hall sensors were selected using a planar technology on the TSOS CMOS process.

Proper measures were taken to compensate the expected problems due to small sense voltage and the expected differential offset voltage. A pair of matched hall

devices were used to overcome the offset voltage due to tapping of points in hall sensor to measure an hall voltage. A novel layout approach was used to minimize the offset voltage in the first amplification stage and a two stage feedforward autozero comparator was used to minimize the offset of the first stage amplifier. These circuits will be discussed in greater detail in chapter 2.

Overview and Objective

Overview

The Magnet Hall-effect Random Access Memory (MHRAM) test chip developed here uses the hall effect principle, which in the presence of a magnetic field generates a voltage to determine the direction of the stored magnetic field which represents the storage of a logical "1" or "0", in a manner analogous to a core memory.

The magnetic field is generated by passing a current over a thin film magnet. Depending on the direction of current over the magnet a logical "1" or "0" is stored. Write logic is included to select a cell to be written and pass a current over the magnet of that particular cell, whose direction depends upon the data to be stored. Various analog and digital cells along with the write reference circuits are used to design complete write path. Reading from the cell is done by selecting the cell, introducing read current in that particular cell and sensing the magnetic field using the principle of hall effect. The hall voltage generated is than amplified using various analog, digital and reference circuits to read the stored data. The read path is the most

critical part of the design since the signal obtained from the hall sensor is of a very low magnitude.

Two versions of MHRAM were developed. One based on silicon hall sensor and the other based on indium antinomide hall sensor. All circuits were designed using TSOS CMOS process. The MHRAM was designed to operate on a single 5 V supply. The use of a programmable magnet allows for the Non Destructive Read Out (NDRO) for environment which requires fail safe operations.

The MHRAM chip test chip is a four memory element organization in an array of two row by two column matrix. This design uses two sets of power supplies (VDD and GND), which provide isolation between a. c. signals in analog circuit with clocking circuits in digital circuits. The basic building blocks which are used along with 2 X 2 MHRAM arrangement are shown in figure 1. Two output pins were used, one for each column. Also the basic building blocks and read path and write path were fabricated separately on another test chip to allow individual testing of their performance and functionality.

Objective

The objective was to design building blocks and complete a 2 X 2 MHRAM, to check for their functionality independent of the availability of a hall sensor signal. This provided a means to determine minimum value of the signal that can be read correctly with the designed read path. The design of the hall cell, an memory element which stores the data is to be provided by JPL.

If this design is successful, then the approach will be used in future designs to

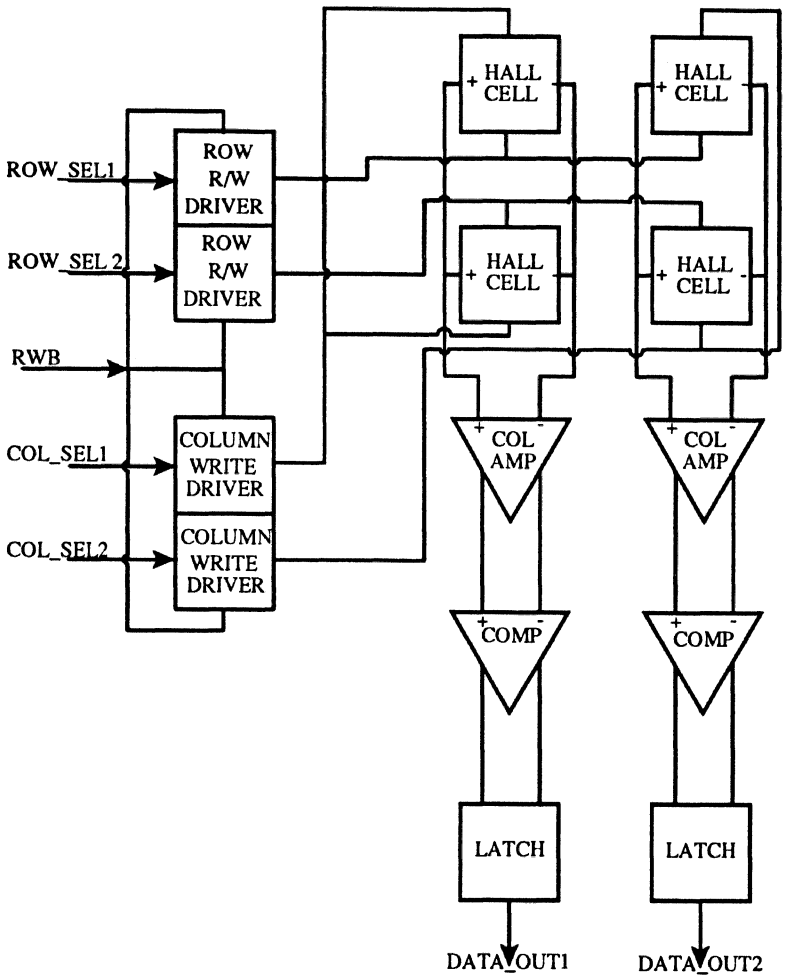


Figure 1 MHRAM Functional Overview

make a larger array with some modifications if needed.

The content of this thesis is presented in five chapters. Chapter 2 discusses in detail the hall effect, MOS hall sensors for sensing the magnetic field using the hall effect principle, magnetic memory concept, offset voltage considerations during the design and methods to reduce it. Autozeroing techniques which cancel the offset voltage in a two stage feedforward comparator is discussed in brief. Chapter 3 describes the basic building blocks for the read and write path along with its simulation and test results. Chapter 4 discusses the system level realization along with the explanation of its functionality. Simulation results are also included in this chapter. Chapter 5 offers conclusions based on these results. Suggestions for further work along with future prospects of this design are also offered.

CHAPTER II

LITERATURE REVIEW

This chapter presents in detail the hall effect principle, the silicon based hall sensor, followed by the magnetic memory concepts. In the remaining sections expected offset problems and methods for minimizing these problems are discussed.

Hall Effect

The hall effect is a direct result of the Lorentz force on moving charge carriers constrained to move in a given direction and subjected to a transverse magnetic flux density. The hall-effect plays an important role in the study of charge carrier conduction and hence occupies an important position among the methods for studying the transport properties of conductors.

The physics involved in understanding the hall-effect can be best understood from figure 2. If a current of I ampere is flowing through a specimen (metal or semi-conductor) of length l, width w and thickness t, placing this specimen in a transverse magnetic field B, an electric field ε is induced in the direction perpendicular to both I and B. If I is in the positive X-direction, B is in the positive Z-direction, then a force will be exerted in the negative Y-direction on the current carriers, which results in a potential V_H called hall voltage between terminals VHA and VHB.

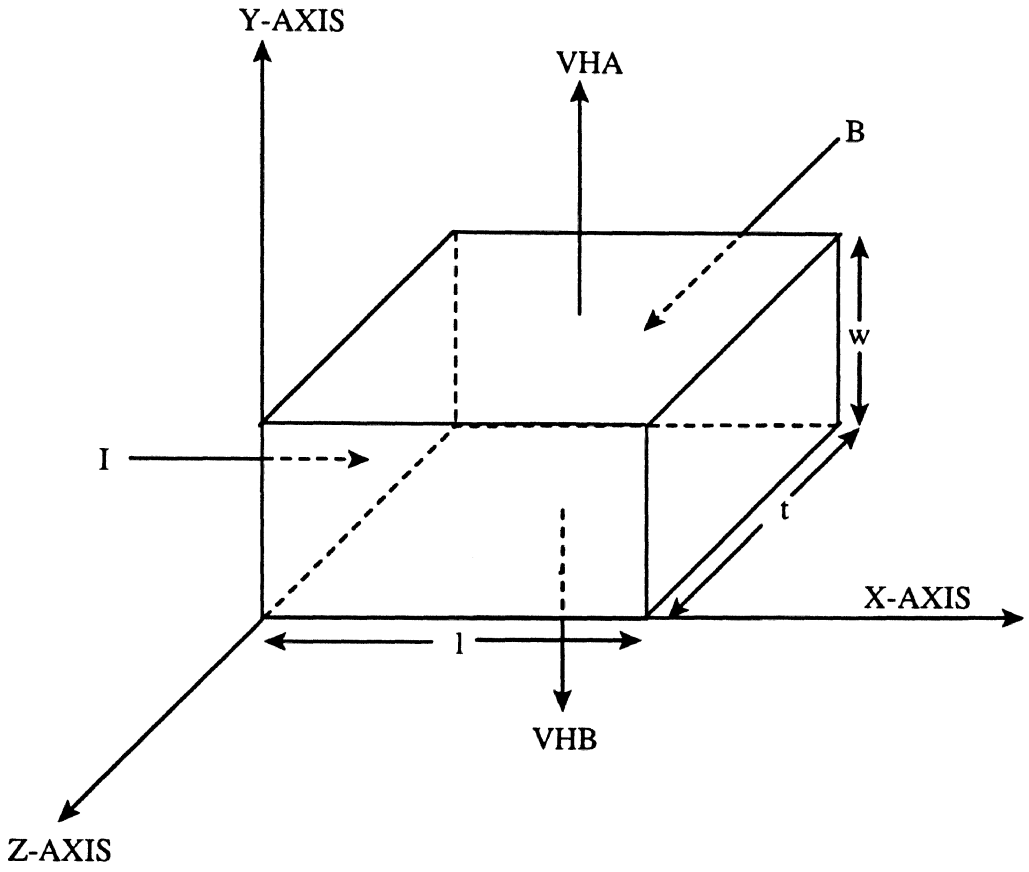


Figure 2 Hall effect

In an equilibrium state, the electric field ε due to hall-effect must counter the force on the carrier to balance the magnetic force.

Hence,

$$e\varepsilon = Bev \tag{6}$$

where,

e is the magnitude of the charge on the carrier,

υ is the drift speed and

ε is the electric field.

Also,

$$\varepsilon = \frac{V_H}{w} \tag{7}$$

where,

w is the distance between surface VHA and VHB.

From Equation 6 and 7 we have,

$$V_H = Bvw \tag{8}$$

Current density J is defined as,

$$J = \rho v = \frac{I}{tw} \tag{9}$$

where,

ρ is the charge density and

t is the thickness of the specimen in direction of the magnetic field.

From Equation 8 and 9 we have,

$$V_H = \frac{BI}{\rho t} \tag{10}$$

If B, I, V_H and t are known or measured, ρ can be determined. Hence, the hall coefficient R_H is defined by

$$R_H = \frac{1}{\rho} \tag{11}$$

From Equation 10 and 11 we have,

$$R_H = \frac{V_H t}{BI} \tag{12}$$

Since it is desirous that we have as large a hall voltage as possible, and we anticipate a small magnetic field strength. Also we desire to have small values of I and t is fixed. It is desirable to select a material with as large a R_H as possible. Hall Sensors based on the principle is the focus in the next section.

Hall Sensors

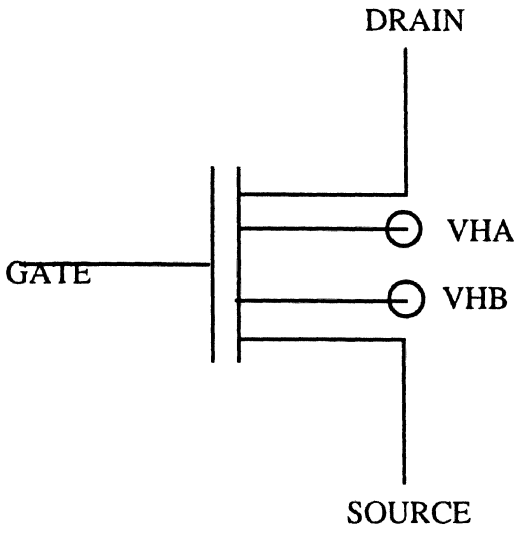
A hall device, as a magnetic field sensor, is an input transducer, which converts magnetic field H into an useful electronic signal. Semiconductor hall sensors fabricated of silicon, indium antinomide and gallium arsenide are widely used for precise motor control in the design of video tape recorder, the vending machine etc. CMOS compatible sensors for detection of magnetic fields parallel and perpendicular to the chip surface are well suited for the integration of the sensors with the analog

and digital circuitry on the same chip. When integrating monolithically hall elements with other circuitry, a high impedance MOS transistor is well suited to amplify the hall voltage output to the respectable level.

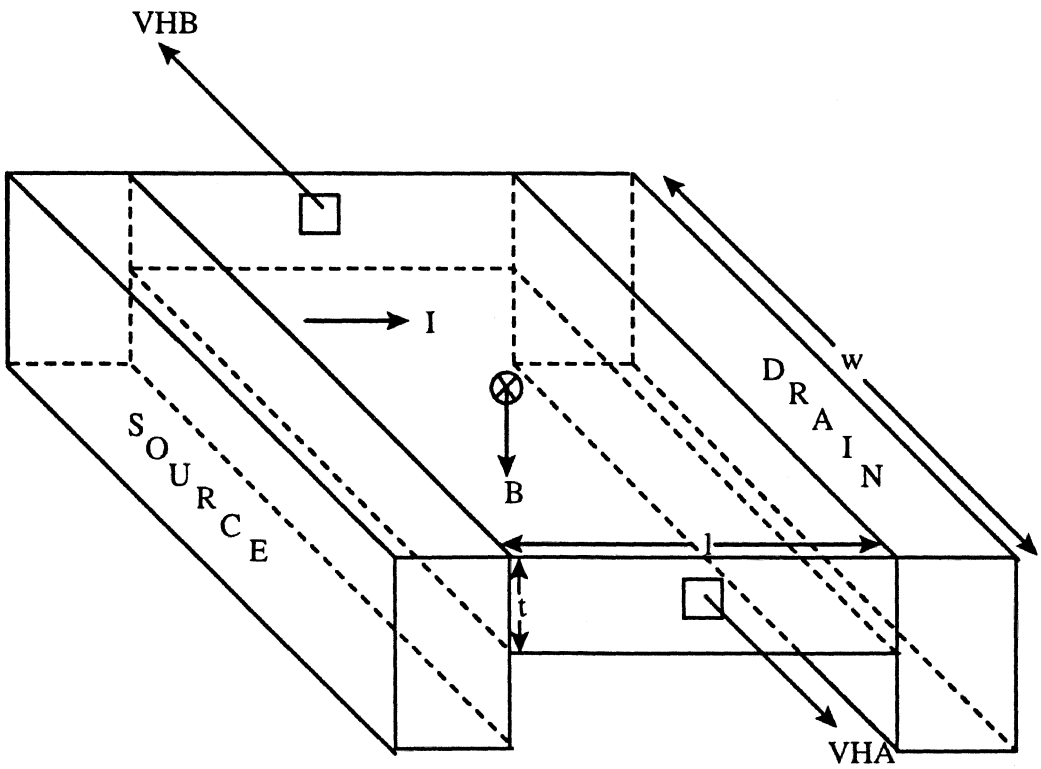
A CMOS compatible MOS hall sensor is shown in figure 3. Figure 3(a) shows MOS hall sensor symbol with floating body and figure 3(b) shows the cross-section of a silicon based MOS hall sensor. On applying a gate voltage to an MOS hall sensor, an inversion layer is formed. A drain current will flow on the application of a drain to source voltage. This MOS hall sensor is placed in a magnetic field, with the field orthogonal to drain to source voltage in order to measure the magnetic field. The hall voltage is generated due to the hall effect which is tapped by two hall contacts VHA and VHB. The resulting hall voltage V_H is given by Equation 10, where t is the thickness of the inversion layer.

The resulting hall voltage is a function of the device drain to source voltage, gate to source voltage, geometric length to width ratio (As mentioned previously the hall voltage is directly proportional to drain current and drain current is dependent on drain to source voltage, gate to source voltage and device geometric, length to width ratio), magnetic field strength, thickness of the inversion layer and the electron mobility.

The hall voltage which is directly proportional to the drain to source current will saturate as MOS hall sensor enters into the saturation region. Hence there will be two modes of operation linear or saturation just as a classical MOS transistor. High hall voltage with low drain to source currents thus are conflicting requirements.



(A) Symbol with floating body



(B) Cross-section

Figure 3 Silicon based MOS hall sensor

Therefore, a compromise must be made between the obtainable hall voltage and achievable drain current for a properly sized MOS hall sensor. The transconductance curve in the subthreshold region of MOS device shows that as the gate to source voltage is increased above the threshold voltage, drain to source current increases exponentially, but at the same time thickness of the inversion layer also increases. However, the hall voltage V_H is directly proportional to drain to source current and inversely proportional to thickness of the inversion layer, the two effects then tend to offset each other. Hence an appreciably higher hall voltage is achievable if the device is operated at currents near pinch-off voltage. The hall voltage is directly proportional to the magnetic field.

Lippman and Kuhrt[34] have shown that a geometric factor G(L/W , θ) relates the normalized hall voltage to the length to width ratio for different hall angles θ [4]. Hall elements requires L/W of 2 or more while length to width ratio of MOS transistor should be less than or equal to 0.05. V_H is directly proportional to mobility and hence any effort to increase the mobility will improve V_H.

Hence one obvious choice to obtain a higher hall voltage is to fabricate an n-channel rather then p-channel MOS sensors resulting in a factor of 2 improvement in the hall voltage. The other choice would be to select a sensor fabricated in depletion mode rather than the enhancement mode. The reason being higher achievable V_H in mv/kg in depletion mode. Also, it is preferrable to operate the sensor at currents near pinch-off voltage. And finally, the value of I and B should be selected such that a desirable hall voltage V_H is achievable under constraints mentioned previously.

Two variants of hall sensors are to be used in the proposed MHRAM design, a indium antinomide version and a silicon version. Indium antinomide has a higher sensitivity than silicon hall sensor, since the mobility of indium antinomide is 9 times that of silicon. The estimated hall voltage for the silicon based sensor designed by NRaD is expected to be 1 mv while that of indium antinomide based sensor is approximately 10 mv. One problem with indium antinomide is that it is not suitable for high temperature operation, because of the dependence of the input resistance on temperature [5]. The silicon sensor used in the MHRAM design is based on a fully depleted n-type MOSFET without a bulk terminal. This sensor can be thought of as an five terminal device (two hall voltage tabs and the classical MOSFET drain, gate and source terminals.

The magnetic field sensed by a hall sensor is actually the data (logic "0" or logic "1") which is stored in a ferromagnet. In the next section, the magnetic storage concepts are examined.

Magnetic Memory Concept

Thin film of magnetic materials have some very desirable properties for memory applications. Unlimited read and write cycles, infinite data retention, compatibility with integrated circuits, intrinsic radiation hardness, and material stability are all very useful properties for memory applications.

There are two possible configuration for magnetic memory cells. In the first configuration the plane of magnetic cell is perpendicular to the plane of substrate

while in the second configuration the plane of magnetic cell is parallel to the plane of substrate. In the parallel configuration, the entire magnetic toroid can be deposited in a single processing step and hence is easier to fabricate compared to the perpendicular configuration. The perpendicular configuration has tighter coupling and hence for a given signal less current drive is required. For the proposed design of the MHRAM we will be using a planar technology. Now limitations and proposed methods to store the data in the ferromagnet using planar technology are described.

The magnetic concepts essential for the storage of the data, are examined below. The drive field H is related to the driving current I and circumference C of the toroid by Ampere's law.

$$I=HC \tag{13}$$

For magnetization the drive field H has to reach the minimum H-field known as the coercive force Hc. This coercive force can be reached earlier for the perpendicular toroid with a smaller toroid circumference due to tighter coupling. There are three important levels in the B-H curve as shown in figure 4. They are knee field, coercive force and saturation field, and are referred to as the Hk, Hc and Hs respectively. When the current through magnet is such that drive field is less than knee field Hk, magnetization will not be affected by removal of drive current. For changing polarity of magnetization, drive field should be greater than Hc or equal to saturation field Hs. Hc can be compared to various loss mechanism such as eddy currents because the polarity of the magnetization can only change if the applied field exceeds Hc. Hence for NDRO, in the read mode, drive current applied should be such

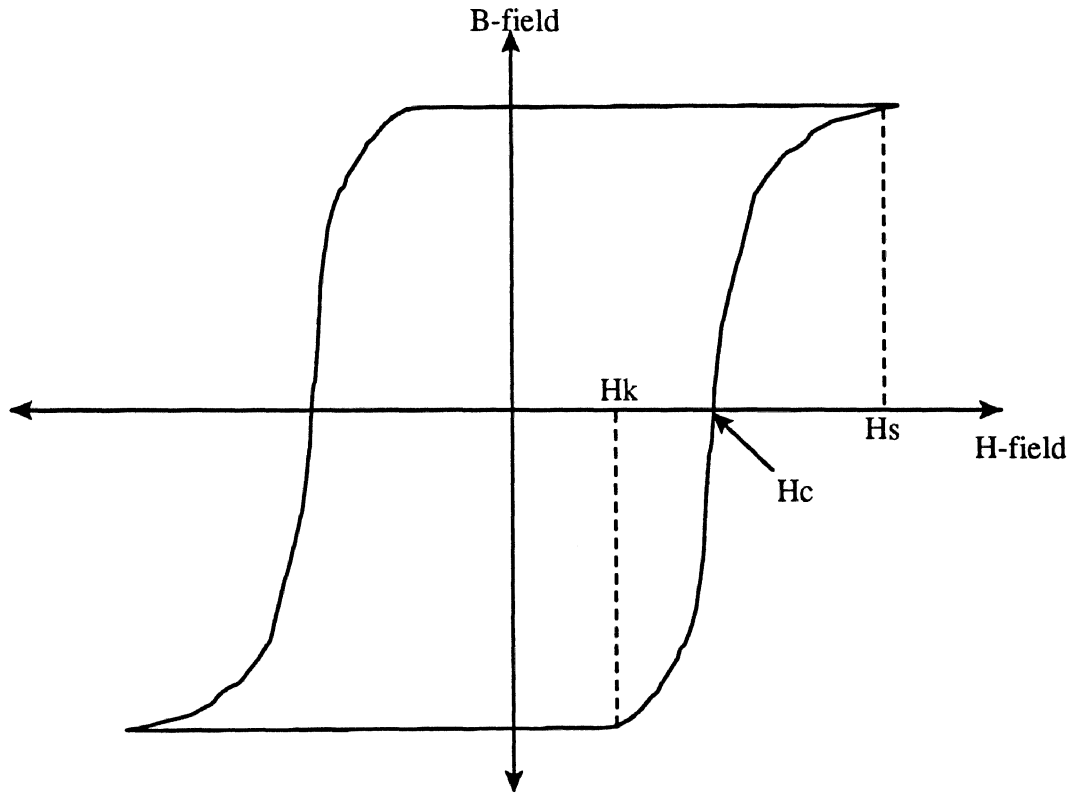


Figure 4 Hysterisis loop of a ferromagnet

that drive field produced should be less than Hk. In write mode drive current applied should be such that drive field produced should be greater than Hc.

The magnetic memory cell used for the proposed MHRAM is a ferromagnet design using planar technology. A bi-directional current flows over this magnet allowing binary data to be stored. Direction changes in current flowing over the ferromagnet, modifies the B-field direction as shown in figure 5. During the write mode current passes over a magnet in one of two directions depending on the data to be stored. During read mode, magnetic field due to the ferromagnet is sensed using MOS hall sensor as described previously. The resulting signal is amplified providing the desired output.

The hall cell which is the core of the MHRAM, consists of three parts, hall sensor, ferromagnet and differential amplifier pair. The next section describes the hall cell in detail along with its function.

Hall Cell

Hall cell can be broken into two key elements, Hall sensor and ferromagnet. In previous sections both hall sensor and ferromagnet has been described. The hall cell is shown in figure 6. It has three terminals VHD, VHS and VHG which controls the current flowing through MOS hall sensor, two terminals VH+ and VH- between which the sensed hall voltage is tapped and two more teminals IW_COL and IW_ROW for input and output of write current which passes over the layer of magnet in MOS hall sensor to magnetize it. A side view of hall cell is also shown in figure 7, to provide

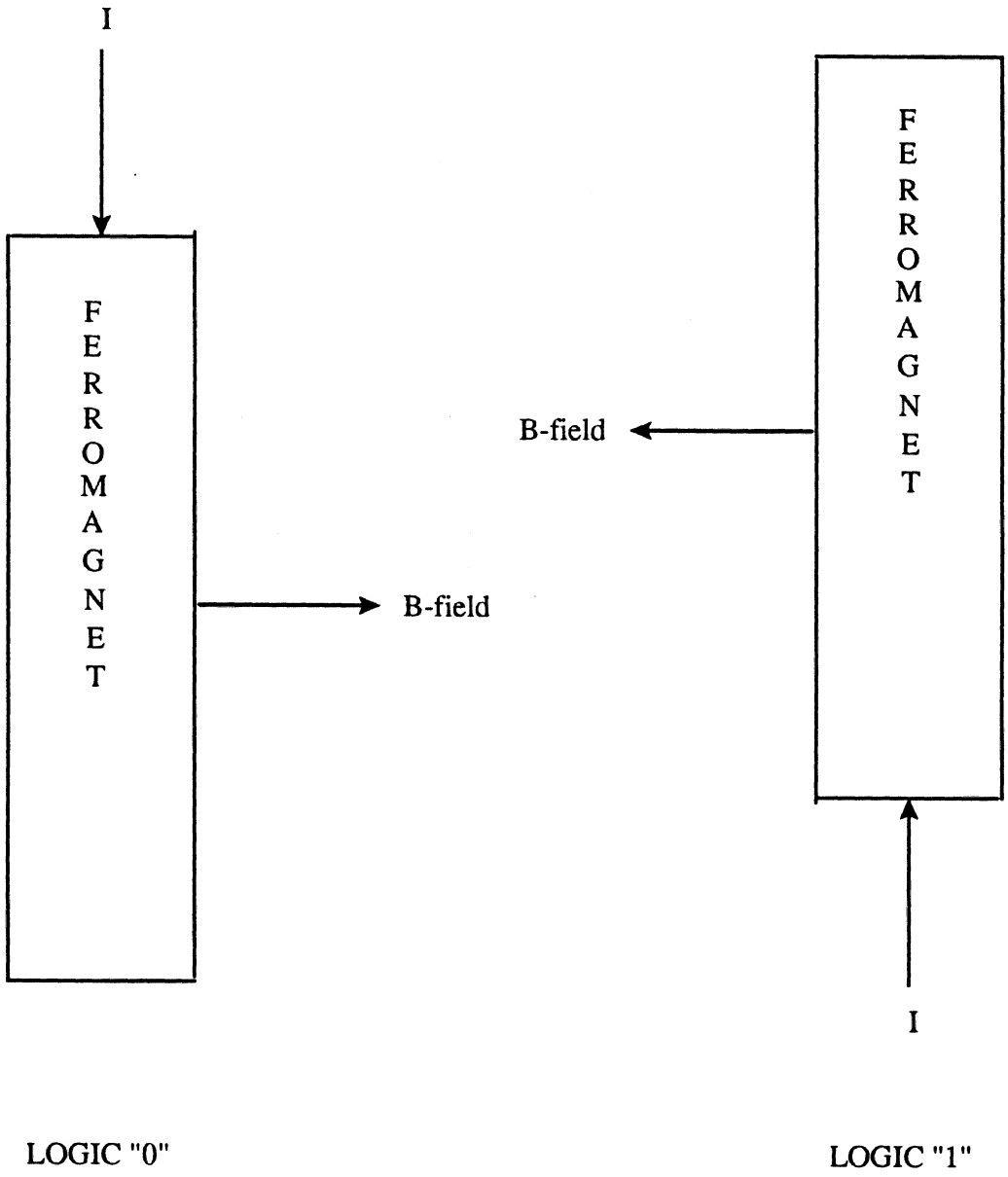


Figure 5 Bidirectional current relation to binary logic data

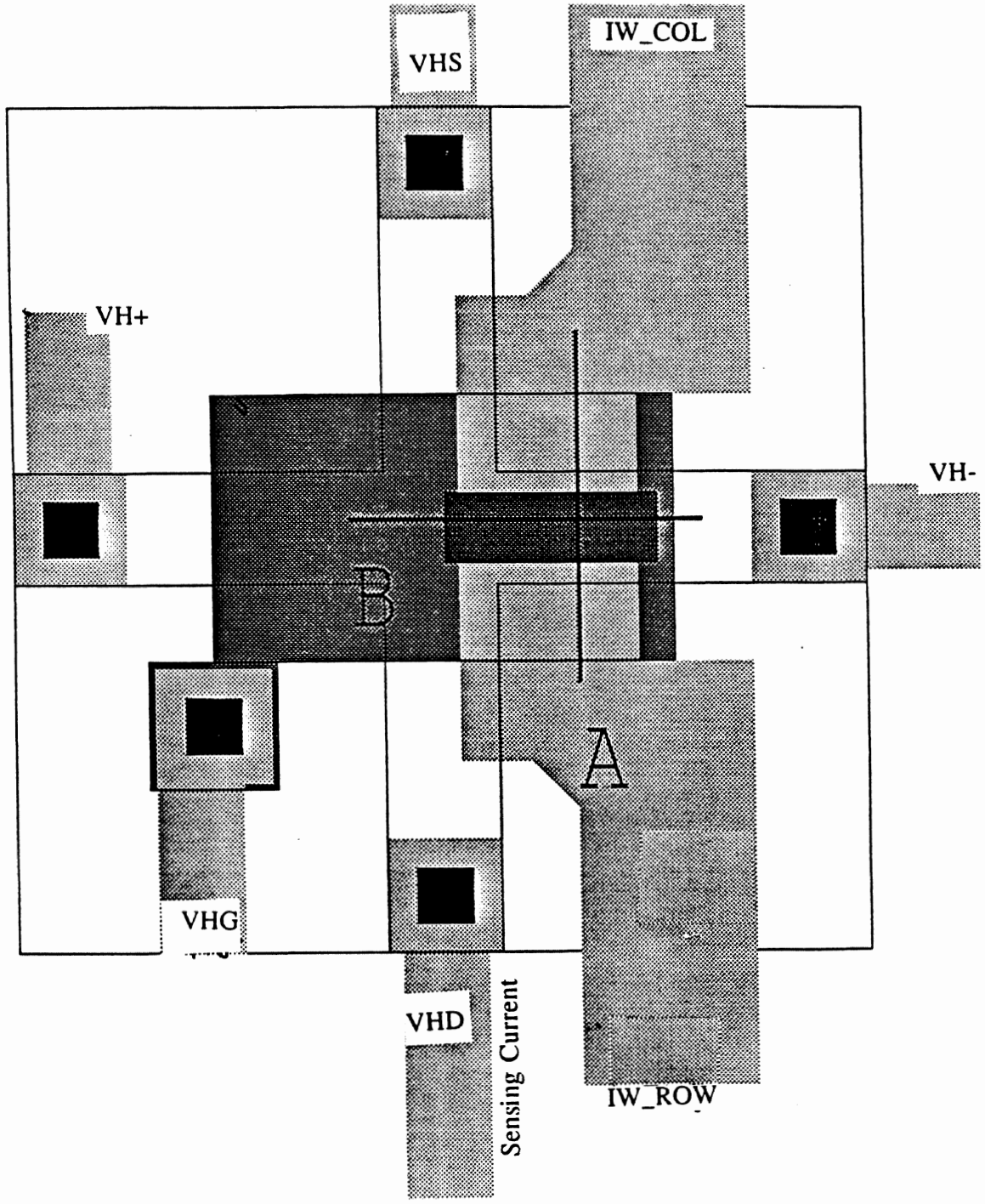


Figure 6 Hall cell

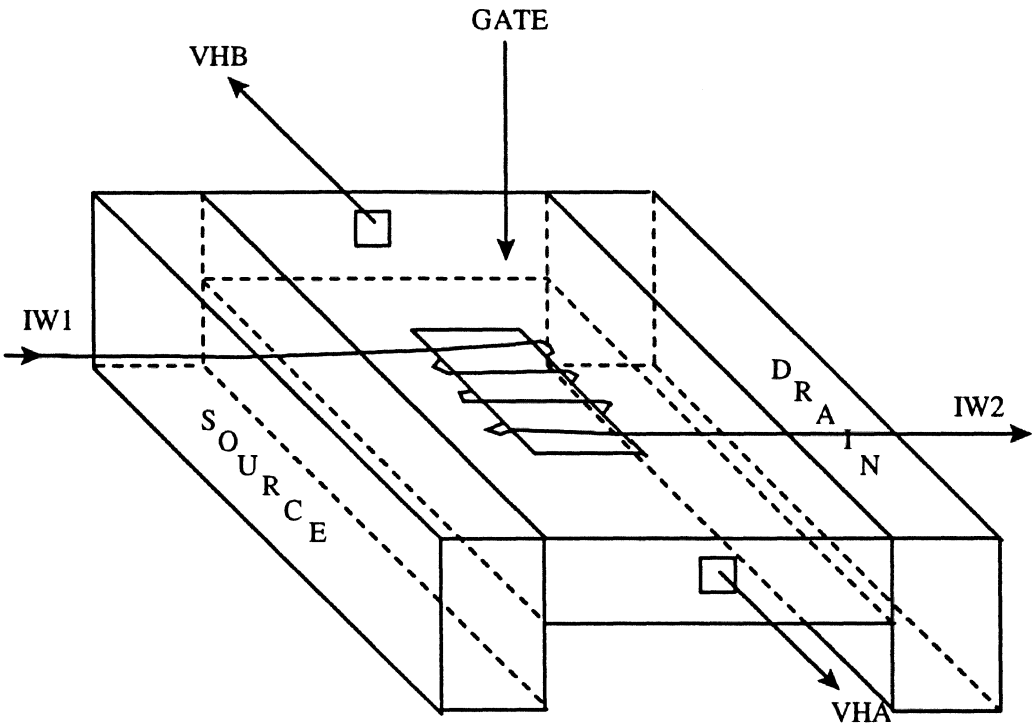


Figure 7 Sideview of hall cell

an improved perspective for the reader.

Working of Hall cell

The hall cell acts as the memory element in the MHRAM system. The drain, source and gate are biased to a particular voltage depending upon the required mode of operation as explained in section 2.2. Upon passing a write current over a magnet, the magnetic field orthogonal to drain to source current in MOS hall sensor is generated. This magnetic field induces resultant hall voltage which is measured at taps VHA and VHB. The polarity level of VHA w.r.t. VHB will depend on the direction of the write current over a magnet as shown in figure 8.

The voltage level senses by the silicon MOS hall sensor is expected to be in the range of 1 mv. The coercive current for writing the data in the magnet is expected to be 25 mA and is provided by the write path.

Offset Cancellation in Hall cell

To measure the hall voltage two points are tapped in hall sensor. If the MOS hall sensor is placed in a magnetic field so that the field is orthogonal to the drain current, then a maximum hall voltage is generated in the inversion layers. Using planar technology and photolithographic techniques, the dimensions and placement of tapped areas may be very accurately defined. Geometrically, two points tapped can be accurately aligned to within 0.0003 inch of each other [4]. This results in an offset voltage, which is the function of geometry, doping and alignment tolerance. If the offset voltage is larger then 1 mV then it becomes difficult to measure V_H reliably.

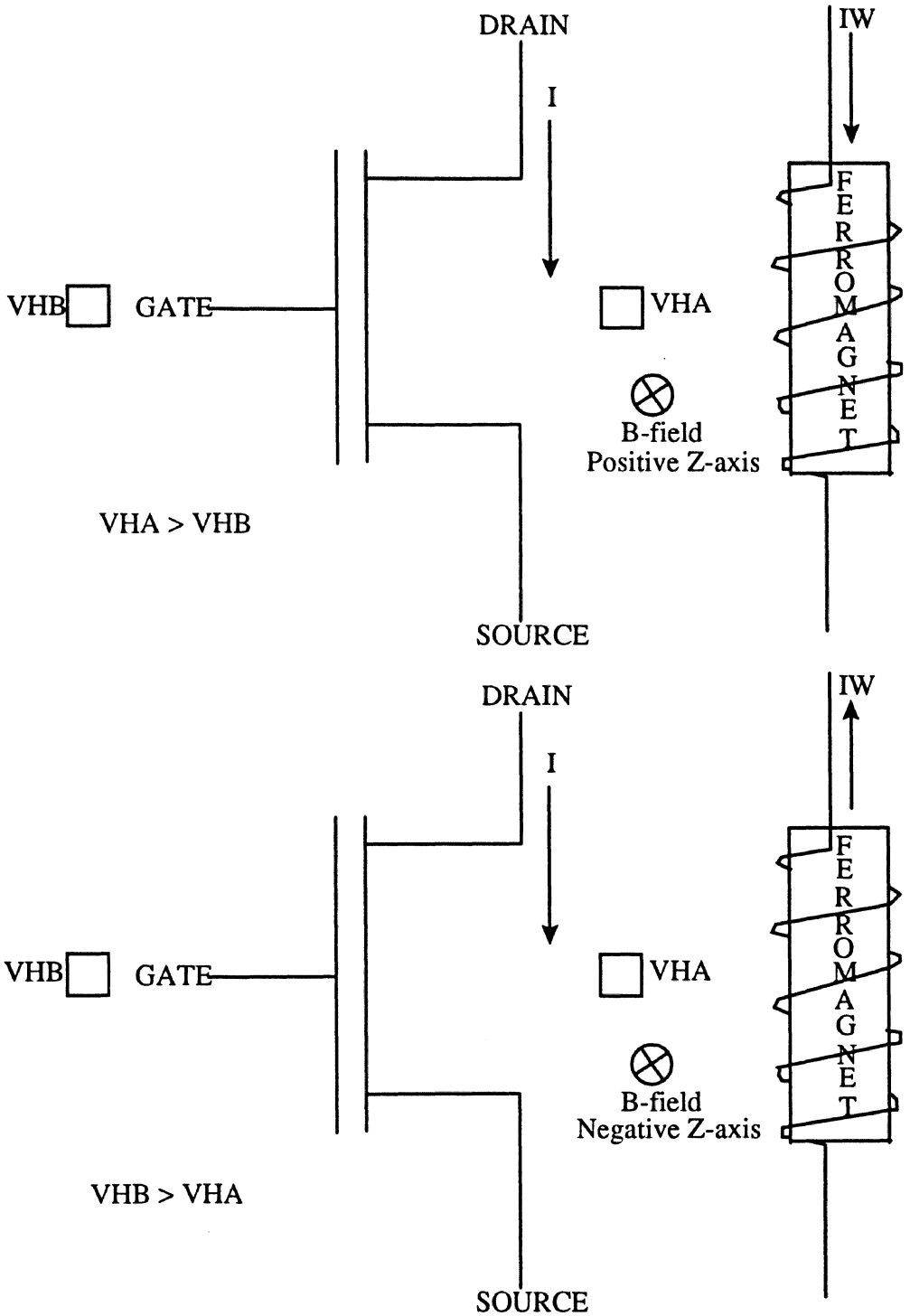


Figure 8 Dependence of Hall voltage on write current

Hence to overcome the offset voltage due to geometry, doping and accuracy tolerance, two hall cells are arranged in parallel.

This arrangement (assuming systematic offset) would result in offset cancellations. The arrangement for this set up is shown in figure 9. The two hall cells are arranged vertically, and mirrored across the vertical axis. The drain, source and gate of cell 1 is shorted to the drain, source and gate of cell 2 respectively. Since both the hall cells are a vertical mirror image, the write current is flowing in one direction only for both the hall cells. This arrangement will help cancelling the systematic offset, since the sensing current (the current flowing through the individual hall cell on application of drain, source and gate voltage) will be in opposing directions. And the hall voltage generated in each hall cell will have a different polarities from the other cell. Since at least part the offset is systematic induced while the hall voltages are of opposite polarity between the two cells as shown in figure 10 reduces error. By connecting the hall voltage terminals to the double differential pair amplifier as shown in figure 11, systematic offset voltage will be cancelled. The functionality of this arrangement is explained below.

Since the write current is flowing in one direction only for both the cells, while the sensing current of the MOS hall sensor is flowing in opposite directions for both the hall cells, results in V_{HA1} and V_{HB2} being at same potential and V_{HA2} and V_{HB1} at same potential (for figure 9). Figure 10 shows the polarity for each hall cell including hall voltage and systematic offset voltage.

Thus the hall voltage of each hall sensor including the offset voltage will be

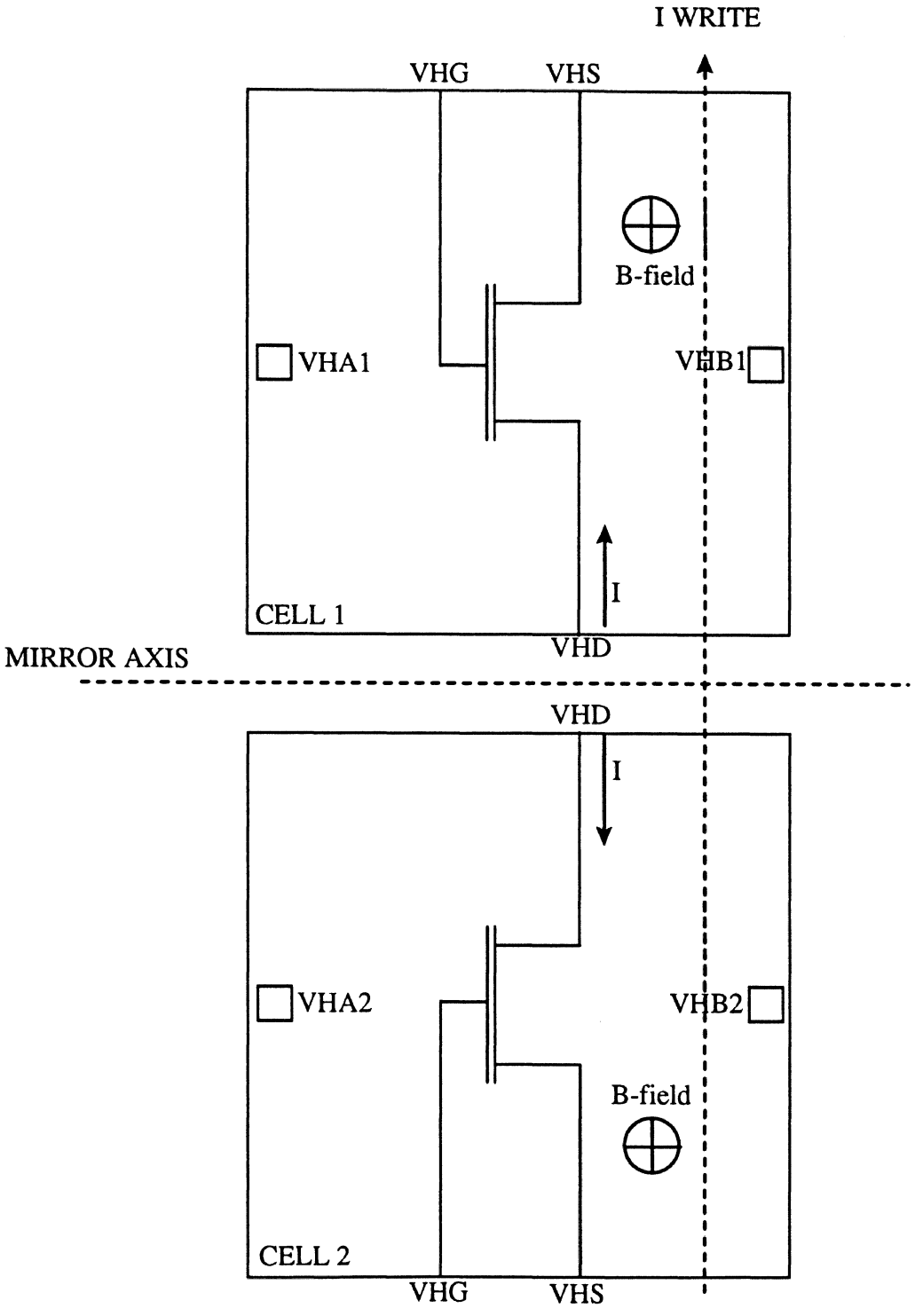


Figure 9 Setup for a hall cell in parallel

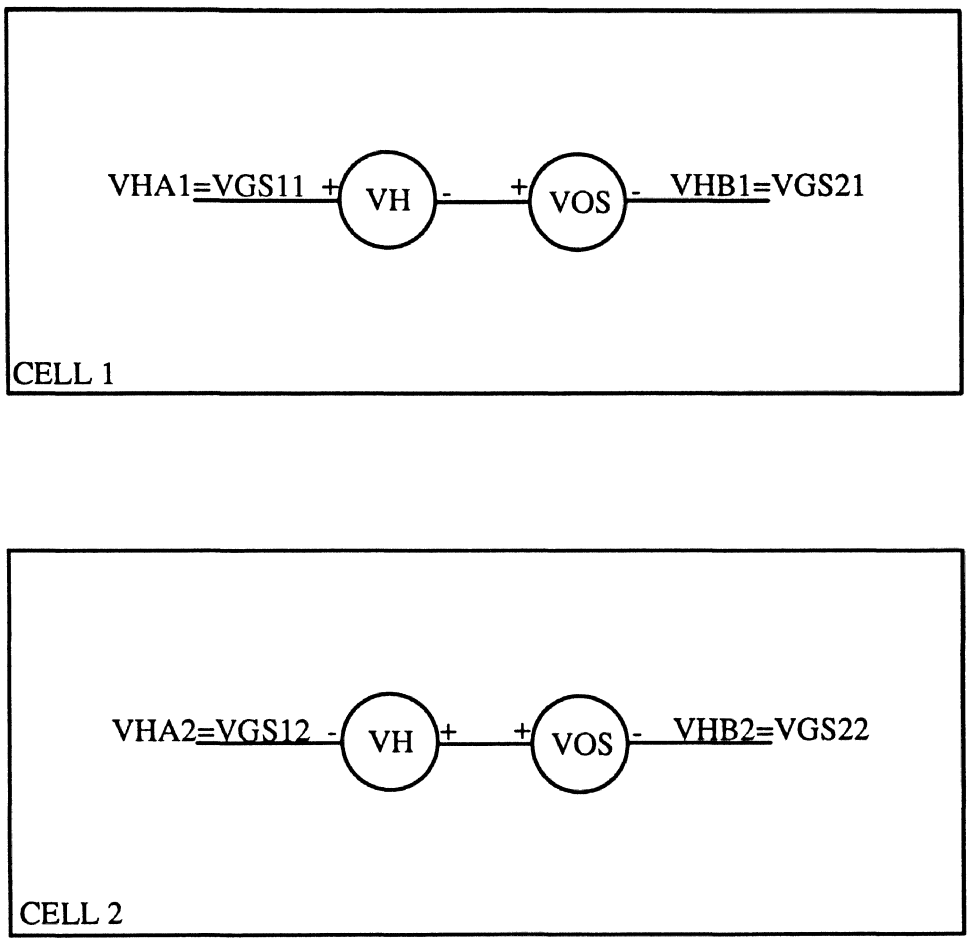


Figure 10 Actual hall voltage at the input of DDP

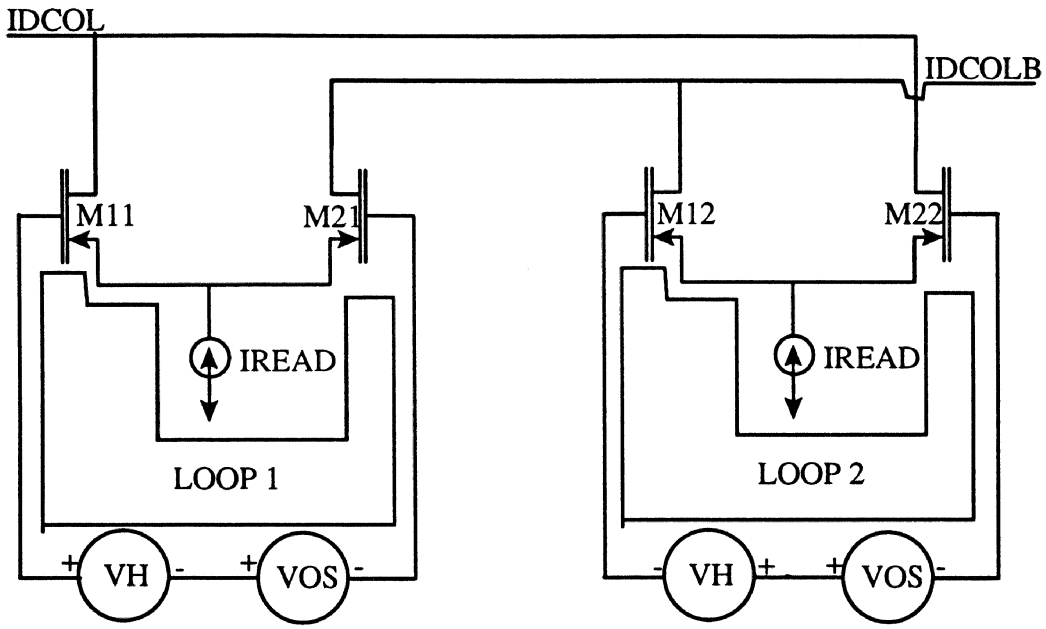


Figure 11 Hall voltage at the input of DDP

connected to the gates of two differential pairs whose drains are tied as shown in figure 11 to form double differential pair (DDP) voltage to current amplifier. This amplifier is the first input stage for the read path. The source of this differential pair is provided with the read current during the read mode of an MHRAM cell. The DDP along with column amplifier (current to voltage amplifier) will form an differential pair column amplifier. Voltage appearing at the gate of two differential pair amplifier is shown in figure 11.

The drain of the transistors in the DDP whose gate are connected to V_{HA1} and V_{HB2} which are at same polarity are connected together to form one output of the DDP and drain of the transistors whose gates are connected to V_{HB1} and V_{HA2} which are at the opposite potential are connected together to form other output of DDP. Below it is shown that with this arrangement of the DDP and two hall sensors, the resulting current at the output of voltage to current amplifier results in systematic offset voltage cancellation. From figure 11,

From loop 1 we have,

$$V_H + V_{OS} + V_{GS21} - V_{GS11} = 0 \tag{14}$$

$$\therefore V_H + V_{OS} = V_{GS11} - V_{GS21} \tag{15}$$

Similarly, from loop 2 we have,

$$V_H - V_{OS} = V_{GS22} - V_{GS12} \tag{16}$$

Now, assuming $g_m = g_{m1} = g_{m2}$, $V_{GS11} = V_{GS12} = V_{GS1}$, $V_{GS21} = V_{GS22} = V_{GS2}$ and $V_{GS11} = V_{GS22}$ are at higher potential (for calculation purpose) w.r t. $V_{GS21} = V_{GS12}$, the

analysis will proceed as follows. The column current difference can be written by noting the node current I_{DCOL} and I_{DCOLB} as follows,

$$\therefore I_{DCOL} = -g_m(V_H + V_{OS} + V_{GS21}) - g_m(V_H - V_{OS} - V_{GS12}) \quad (17)$$

$$\therefore I_{DCOL} = -g_m(2V_H) \quad (18)$$

Similarly we have,

$$I_{DCOLB} = g_m(2V_H) \quad (19)$$

From equation 18 and 19 we can see that systematic offset voltages are cancelled.

Offset voltages in the differential pair transistors of the DDP can loss the signal also. This differential offset can be reduced by the use of a common centroid layout of the differential transistor pairs. The next section describes our common centroid layout method with some test results demonstrating that systematic offsets can be minimized by proper transistor layout.

Common Centroid

There are two sources of error in the elements of MOS integrated circuits. They are

Systematic error : This type of error affects adjacent elements having similar geometries.

Random error : This kind of error varies from transistor to transistor and cannot be improved by matching techniques.

In this section it is demonstrated that systematic error can be reduced by laying out transistors in a common centroid manner. However, also, general overall circuit performance can be improved by the application of central limit theorem, hence the use of multiple stripes. The use of multiple stripes results in better estimate of the parameter means i.e. V_{TO}.

Theory

The offset voltage in the transistor sets the lower limitation for which an analog amplifier is able to sense a small d.c. voltage correctly. Offset or effective V_{TO} mismatches are a function of several parameters i.e. oxide thickness, doping, width, length etc. The effective offset voltage (V_{OS}) which lumps all parameter variations is determined as follows. From figure 12.

We know that,

$$\Delta I = g_m V_{INM} \tag{20}$$

provided $\Delta V >> V_{OS}$.

where,

ΔV = V_{GS} - V_{TO} (overdrive voltage)

ΔI = I_A - I_B (difference of current in two arms)

V_{INM} = V_{GSA} - V_{GSB} (difference in input)

and,

$$g_m = \beta(\Delta V)_M \tag{21}$$

also,

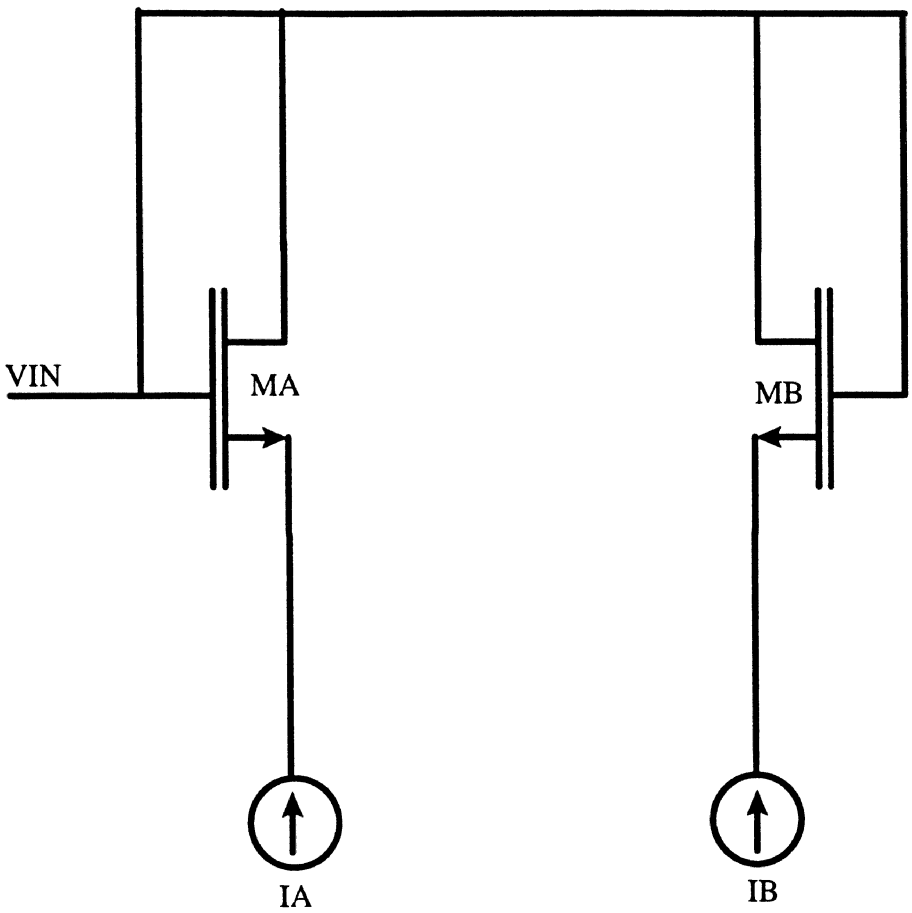


Figure 12 VOS measurement circuit

$$\beta = \frac{2I_M}{(\Delta V)_M^2} \tag{22}$$

where

$(\Delta V)_M = [(V_{GSA} - V_{TO}) + (V_{GSB} - V_{TO})]/2$ and

$I_M = (I_A + I_B)/2$

From equation 20, 21 and 22 we have,

$$V_{OS} = V_{INM} = \frac{\Delta I (\Delta V)_M}{2I_M} \tag{23}$$

In the above equation the average values of I and ΔV are used for calculations of g_m and β of a differential pair of transistor. The reason being, in reality g_m and β would not be the same, even though they are designed to have same g_m and β. The value of g_m and β would be different due to parameter variations.

Layout Technique

Two different arrangements for layout of differential pairs of transistors in common centroid are explained in this section. One of the method is to layout transistor in normal common centroid format as shown in figure 13. In this method each transistor has two stripes which are diagonally placed. The second method which is mentioned is the one used for the layout of DDP. We will refer to this as a comquad centroiding. The comquad centroid is a new way to layout differential pair transistors. In this method each transistor has eight stripes and are arranged as shown in figure 14. Figure 14 reflects the positioning of transistor in actual layout. From

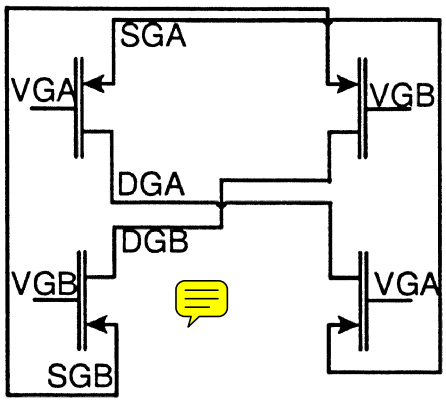


Figure 13 Common centroid arrangement

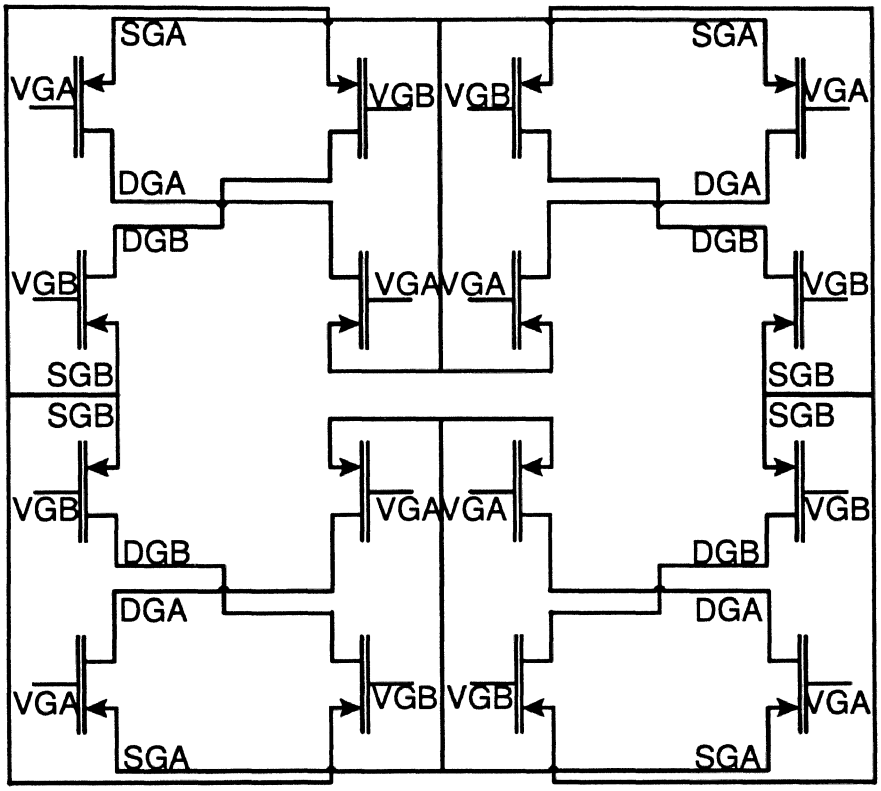


Figure 14 Comquad centroid arrangememt for differential pair

figure 14 we can see that comquad centroid is a common centroid of common centroid layouts and hence the name comquad centroid.

We believe that comquad centroid will provide improve offset voltage, since there will be improvement in the reliability of parameters due to application of the central limit theorem and common centroiding. Transistors, in both arrangements were layout and fabricated. Next section shows the results of both methods.

Test Results

Testing for the common centroid layout and comquad centroid layout was done using a 4145A semiconductor parameter analyzer. First of all the V_T for transistors were determined by plotting an square-root of I_D as a function of V_{GS}, and the point where the slope is maximum is found. X-intercept from that point is V_T. For plotting this curve both the drain and the gate of the transistors are tied together and connected to one SMU channel and varied from 0 V to 5 V. The source is tied to 0 V.

Offset voltages for differential pair of transistors layout in common centroid and comquad centroid manner were determined by shorting DGA to VGA and DGB to VGB in figures 13 and 14. VGA is connected to one of the SMU channel and is varied from $1.5V_T$ - 20 mV to $1.5V_T$ + 20 mV. VGB is held constant at 1.5 V_T. SGA and SGB both were held constant at 0 V or 5 V for n or p channel devices respectively. Offset voltage is the difference in gate voltage (VGA - VGB) when current flowing through arms DGA and DGB is equal.

Threshold voltage for n and p channel device were found to be 0.696 V and -0.99 V respectively. Offset voltage for n and p channel differential pair laid in

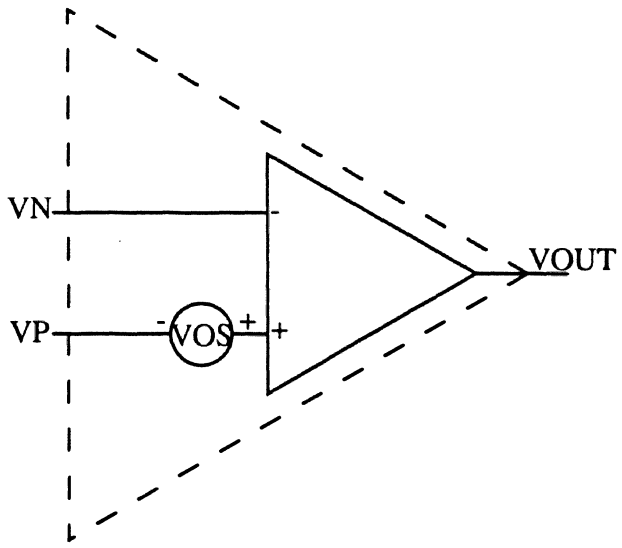
common centroid format with geometries of 2 X 5/2 and 2 X 7/3 respectively for each differential pair transistor were measured. The n and p channel devices laid in common centroid format were found to have a mean of 6.42 mV and 3.01 mV and a standard deviation of 4.28 mV and 3.07 mV respectively. P-channel differential pair laid out in comquad centroid format with geometries of 8 X 7/3 showed very good results with a mean offset voltage of 0.36 mV and a standard deviation of 0.40 mV.

The test results shows that the offset voltage can indeed be reduced by systematic layout technique. Also comquad centroid technique showed a very good results which makes possible for us to measure the signal of as low as 1 mV.

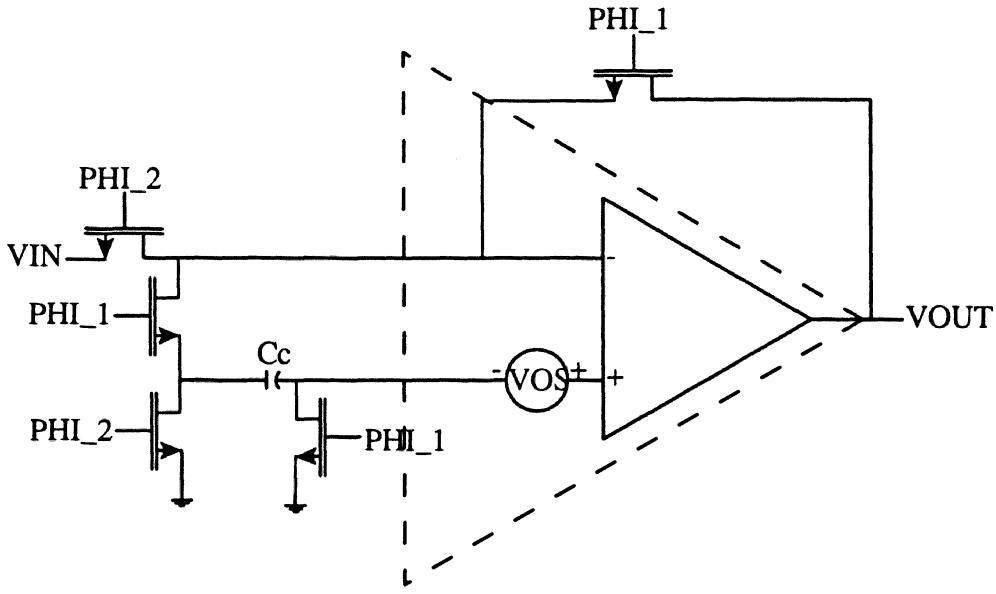
Autozeroing

Autozeroing is a process by which the input offset voltage is stored on a series coupling capacitor and is summed with the input to cancel the effect of the offset voltage. The proposed circuit is shown in figures 15 and 16. Clever design techniques and careful layout can reduce offset voltage but cannot eliminate them. The offset voltage is typically a small voltage (d.c.) from 1 mv to 20 mv. In the design of MHRAM, the input of the comparator will vary from 8 mv to 60 mv. If the offset voltage is larger than the value of the signal, the signal would be lost. Hence, autozeroing plays an important role in this design.

This technique of autozeroing works well with CMOS because of the high input resistance of the MOS devices and readily availability of capacitors. Conceptually offset reduction is limited by the willingness to compromise speed and

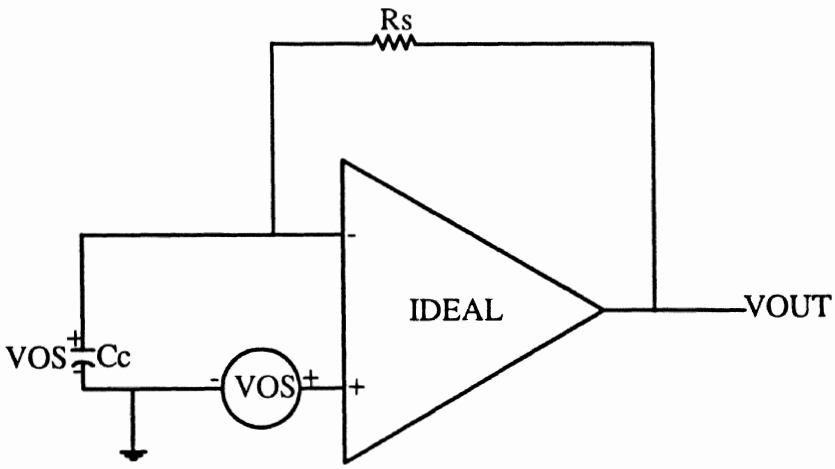


(A) Ideal comparator

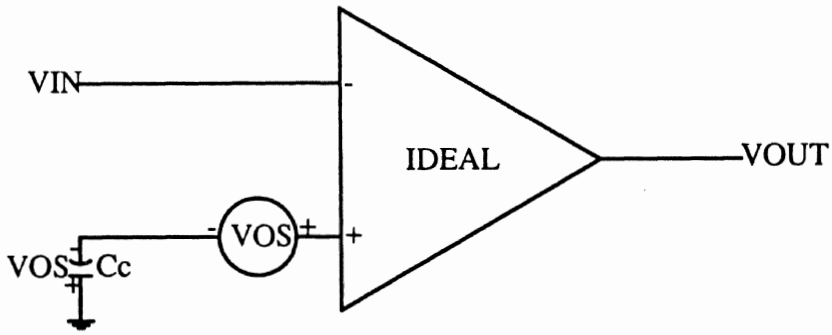


(B) Setup for the autozero circuit

Figure 15 Autozero setup



(A) Comparator during PHI_1 autozero state



(B) Comparator during PHI_2 state

Figure 16 Autozero operation

area by increasing the value of C_C [19].

Figure 15 illustrates a practical implementation of autozeroing. The comparator shown is an ideal comparator with an external offset voltage. A polarity is assigned arbitrarily for convenience. It is also assumed that comparator autozeroing works on two non-overlapping clocks, PHI_1 and PHI_2. When PHI_1 is ON, the arrangement is as shown in figure 16. In this mode the offset is measured and stored on the capacitor. During PHI_2 the offset voltage which is stored on capacitor is connected addatively to cancel the offset voltage.

The time required for the input signal to settle after the autozero switch is closed is calculated as follows.

$$\tau_{settling} = \frac{kR_S C_C}{A_{VOL}} \qquad (24)$$

where,

k = number of time constants which depends upon the desired accuracy [9].

Although it would appear that autozeroing is perfect solution for offset problems. Autozero has limitation that don't eliminate V_{OS} effects completely but add errors by the following mechanism.

The opening and closeing of MOS switches injects or removes charge due to clock signal applied at the gate of switches. Capacitor C_{AZ} will also loose some of its charges during PHI_2 due to switch leakage. If offset is completely cancelled ($\tau = \infty$) during common mode value of VP and VN during PHI_1, it may not cancel during

PHI_2 due to different common mode value of VP and VN which may have different value of offset voltage. Non uniform common mode gain also induces an error equivalent to V_{OS}.

Additionally gain consideration demand that a differential signal should be transmitted unattenuated via C_C. Therefore C_C should be made much greater than C_{amp} + C_{SW}, where C_{amp} is the parasitic capacitance of the input stages and C_{SW} is the parasitic capacitance of the autozeroing switch. Attempts should be made to keep C_C 10 times C_{amp}. Keeping C_C large also improves the charge injection errors. However, all of this comes at an expense of speed or selling performance.

CHAPTER III

READ/WRITE LOGIC BUILDING BLOCKS

The MHRAM consists of many small analog and digital blocks. These blocks will be described in detail in this chapter and will be used to design the complete MHRAM in the second phase. From an architectural point of view the MHRAM is similar to that of a standard SRAM address and data format. However, there are substantial differences in the internal read and write functions. The different building blocks explained in the following sections individually are Read/Write Row Driver, Write Column Driver, Differential Paired Column Amplifier, Two Stage Feedforward Comparator, Analog Latch, Biasing circuits and Digital circuitry (Refer to figure 1).

Row Read/Write Driver and Column Write Driver

Each row and column of the memory array has a row and a column driver. The row driver operates in read mode and write mode, while column driver operates only in write mode. Chapter 4 explains how the row and column driver together provide write current and read current during the write and read mode respectively, which is helpful for performing write and read functions in the memory.

Figure 17 shows the row read/write driver. The row read/write driver has three external control pins DATA_IN, ROW_SEL, and RWB, three biasing pins VB13W,

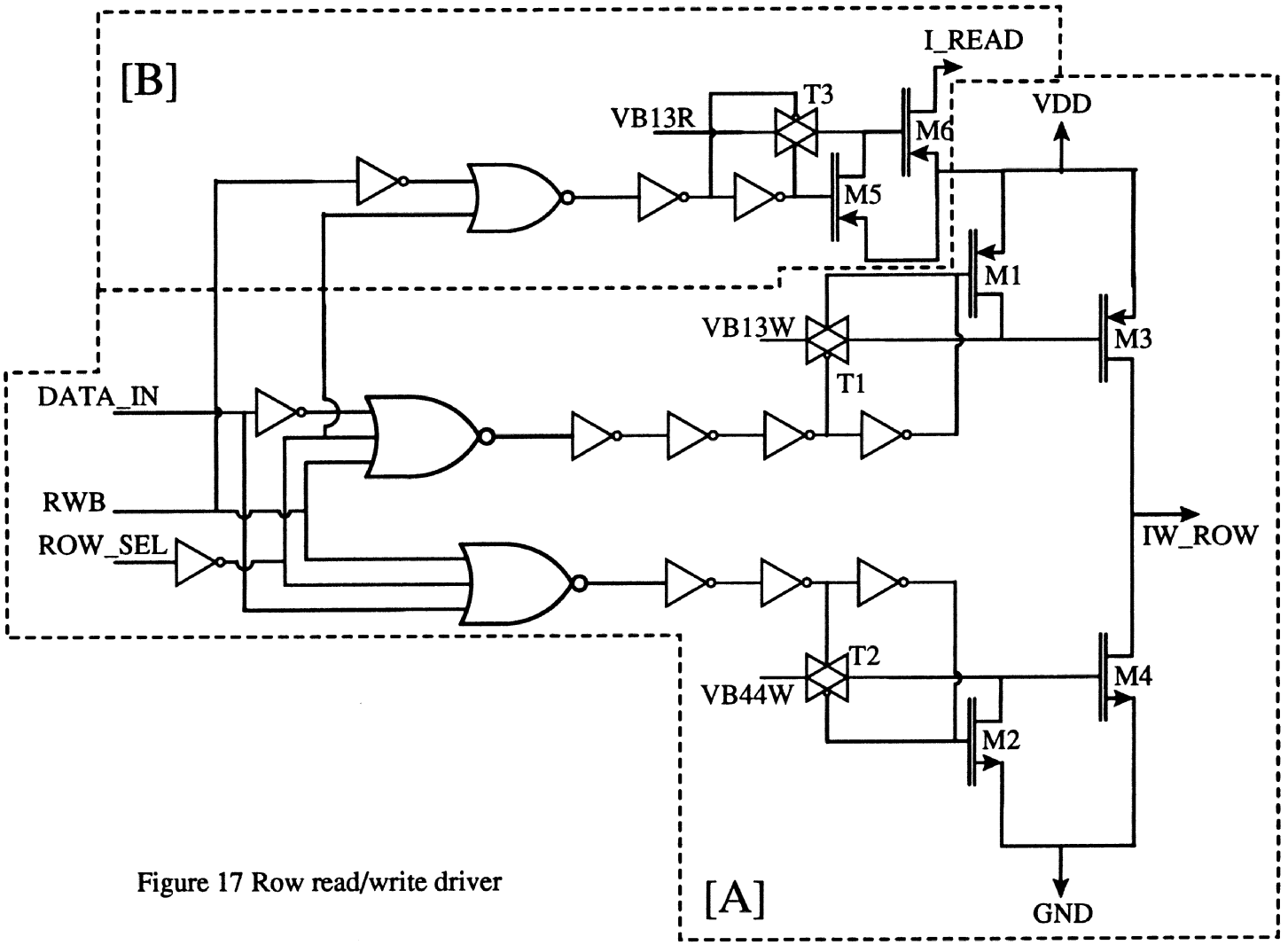


Figure 17 Row read/write driver

VB44W and VB13R which comes from the biasing circuit (see section 3.5), and output pins IW_ROW and I_READ. IW_ROW and I_READ represents write and read current respectively.

The operational mode of row read/write driver depends on the status of the pin RWB, low write and high read. ROW_SEL activates on being high or deactivates on being low the particular driver. For simplicity figure 17 is divided into two sections. Section A is activated during write mode while section B is activated during the read mode.

In write mode IW_ROW sinks (DATA_IN active low) or sources (DATA_IN active high) current depending upon the status of the pin DATA_IN. Transistors M3 and M4 whose gates are supplied via biasing voltages VB13W and VB44W respectively acts as current mirror with the write biasing circuit (see section 3.5). The write biasing circuit has 2.5 mA of current flowing through its arm. Therefore geometries of transistor M3 and M4 are kept ten times that of the mirroring transistors in the write biasing circuit. This results in capability of IW_ROW to source or sink current of 25 mA, the current which is required to program an magnet in memory cell.

In read mode, I_READ sources current. Transistor M6 whose gate is supplied via biasing voltage VB13R acts as a current mirror with the read biasing circuit (see section 3.5). The read biasing circuit has 40 μA of current flowing through its arm. Therefore geometry of transistor M6 is kept four times that of mirroring transistor in the read biasing circuit. This results in capability of I_READ to source current of 160 μA, the required read current for the design.

Column write driver is shown in figure 18. The column write driver has three external control pins DATA_IN, COL_SEL and RWB, two biasing pins VB13W and VB44W which comes from the biasing circuit (see section 3.5) and output pin IW_COL. IW_COL represents write current.

The write column driver operates only in write mode (RWB is active low). It has the functionality similar to that of row read/write driver during write mode. The only difference is the way in which the logic circuitry is determined i.e. IW_COL sinks (DATA_IN active high) or sources (DATA_IN active low) current depending upon the status of the pin DATA_IN.

As explained above the drivers are designed such that, when row read /write driver acts as a current source column write driver will act as a current sink and vice versa.

Simulation

The Spice simulation results for row read/write driver and column write driver are shown in Table 2. They were designed to source and sink 25 mA of current via IW_ROW and IW_COL during the write mode and source 160 μA of current via I_READ during the read mode. All the biasing voltages to these circuit were applied using the biasing circuits (see section 3.5). The write and read current were simulated by applying different logic levels to the control pins RWB, DATA_IN and ROW_SEL , resulting in selection of mode of operation of a driver and resultant current at the output pins IW_ROW, IW_COL and I_READ as shown Table 2.

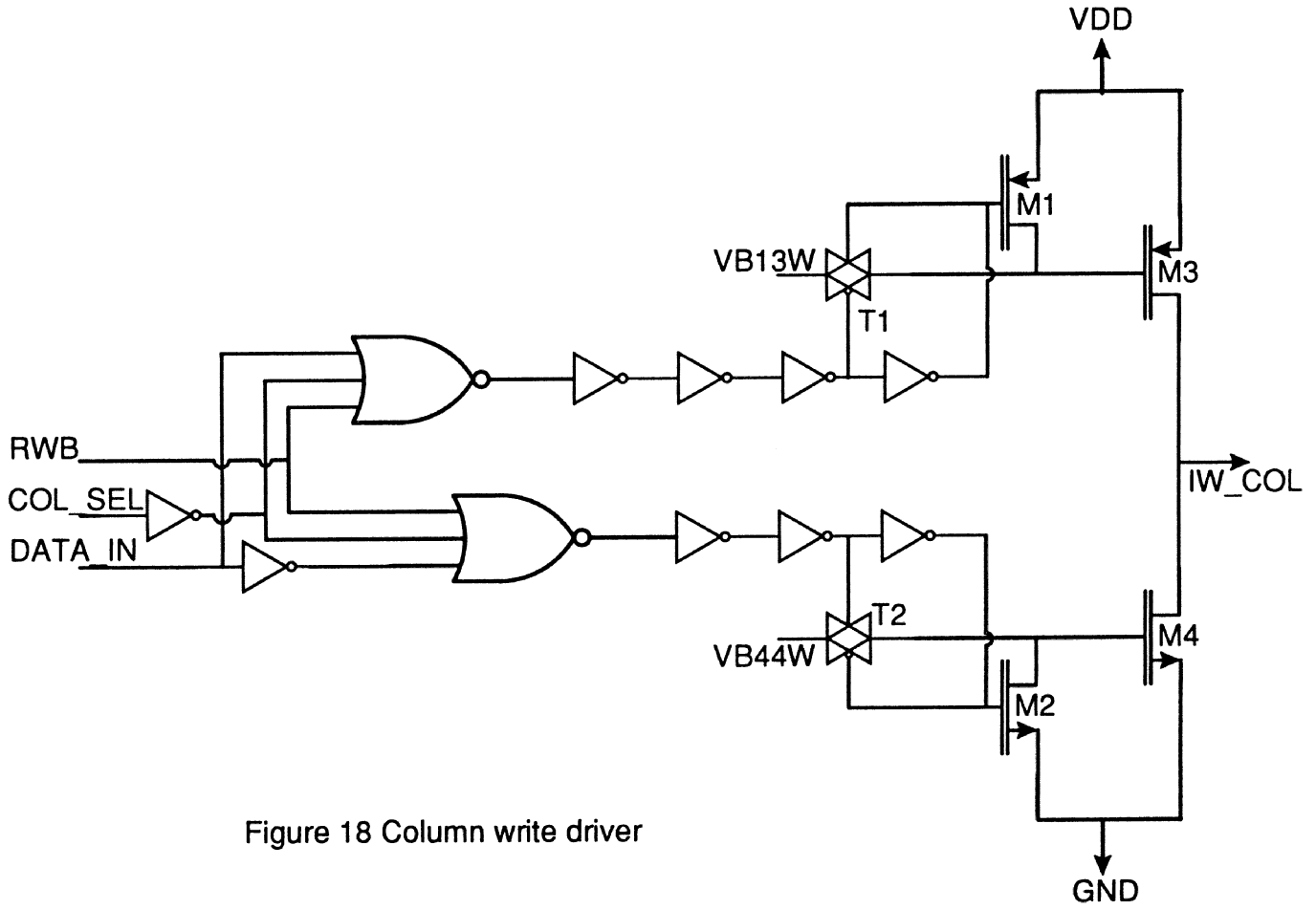


Figure 18 Column write driver

ROW_SEL	COL_SEL	RWB	DATA_IN	IW_COL	IW_ROW	I_READ
0 V	0 V	0 V	0 V	Leakage Current	Leakage Current	Leakage Current
0 V	0 V	0 V	5 V	Leakage Current	Leakage Current	Leakage Current
0 V	0 V	5 V	0 V	Leakage Current	Leakage Current	Leakage Current
0 V	0 V	5 V	5 V	Leakage Current	Leakage Current	Leakage Current
5 V	5 V	0 V	0 V	Sources 25 mA	Sinks 25 mA	Leakage Current
5 V	5 V	0 V	5 V	Sinks 25 mA	Sources 25 mA	Leakage Current
5 V	5 V	5 V	0 V	Leakage Current	Leakage Current	Sources 160 μA
5 V	5 V	5 V	5 V	Leakage Current	Leakage Current	Sources 160 μA

Table 2 Simulation results for Row read/write driver and Column write driver.

Test Results

The row read/write driver and column write driver were tested using a 4145A semiconductor parameter analyzer. Reference biasing circuits which provide the bias voltages for these drivers were also laid out next to the drivers. The reference current of 40μA and 2.5 mA were supplied by two SMU pins on 4145A for the read and the write biasing circuits respectively. Logic levels for control pins RWB, ROW_SEL, COL_SEL and DATA_IN were supplied by external generators. The read and the write current for the row driver, and write current for the column driver were monitored. The test results are shown in Table 3.

On comparing the test results and the simulation results it can be observed that row and column drivers supplies write current as expected +/- 15%. The read current measured on testing is found to be 220μA (simulation result 170 μA). The read current was measured at 0 Volts (Potential at I_READ = 0 V), instead of the design value of 3.78 V. The high read current is due to the transistor reaching the avalanche point (i. e. applying V_{DS} = 5 V instead of V_{DS} = 1.22 V to M6).

Differential Paired Column Amplifier

The differential pair column amplifier, an cascade amplifier is the first stage of the three stages involved in the amplification of the hall sensed signal during the read mode of the MHRAM. Cascade amplifier is used to provide higher output impedance and reduce the effect of the miller capacitance [2].

The differential pair column amplifier is shown in figure 19. It has three

ROW_SEL	COL_SEL	RWB	DATA_IN	IW_COL	IW_ROW	I_READ
0 V	0 V	0 V	0 V	Leakage Current	Leakage Current	Leakage Current
0 V	0 V	0 V	5 V	Leakage Current	Leakage Current	Leakage Current
0 V	0 V	5 V	0 V	Leakage Current	Leakage Current	Leakage Current
0 V	0 V	5 V	5 V	Leakage Current	Leakage Current	Leakage Current
5 V	5 V	0 V	0 V	Sources 29 mA	Sinks 28 mA	Leakage Current
5 V	5 V	0 V	5 V	Sinks 29 mA	Sources 28 mA	Leakage Current
5 V	5 V	5 V	0 V	Leakage Current	Leakage Current	Sources 220 µA
5 V	5 V	5 V	5 V	Leakage Current	Leakage Current	Sources 220 µA

Table 3 Test results for Row read/write driver and Column write driver.

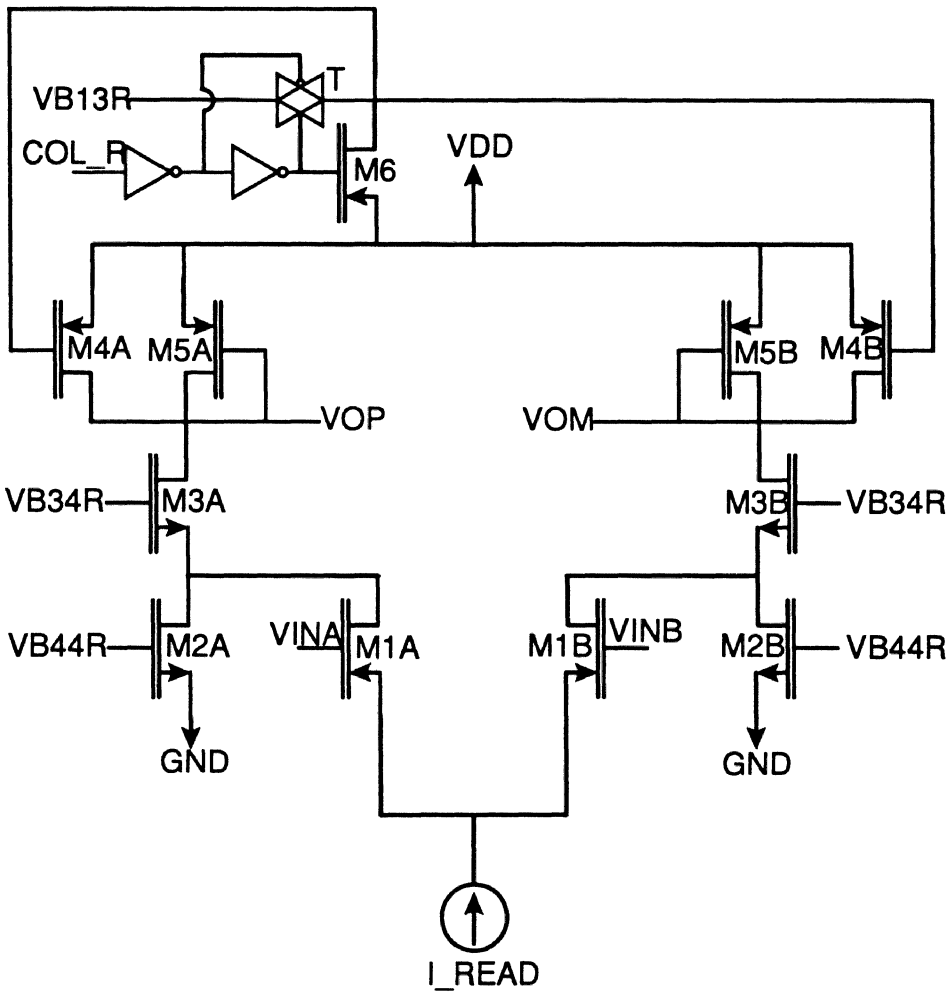


Figure 19 Differential pair column amplifier

biasing pins VB13R, VB34R and VB44R which comes from the biasing circuit (see section 3.5), two differential input pins VINA and VINB which is the output of the memory hall cell (see section 2.4), one control pin COL_R which comes from column select amplifier (see section 3.6), one current reference pin I_READ which comes from row read/write driver (see section 3.1), and two output pins VOP and VOM. This amplifier is placed, one per each column of the MHRAM, and is selected when COL_R pin is active high.

The expected output of memory hall cell was 1 mV. Therefore, transistors M1A and M1B were laid out in comquad fashion (see section 2.5), to minimize the offset voltage. Transistors M5A and M5B are active diode loads. Transistors M4A and M4B are current sources. The gates of transistors M2A, M2B, M3A, M3B, M4A and M4B are supplied by biasing voltages. The output VOP and VOM will be feeded to the next amplification stage i.e. two stage feed forward comparator for further amplification.

Small Signal Analysis

The small signal analysis of a differential pair column amplifier which is connected to the output of the memory hall cell is shown below. A simplified model of differential pair column amplifier is shown in figure 20. A valid assumption has been made in this model that both sides of the differential pair column amplifier are perfectly matched. Hence the node at which M1A and M1B are shorted can be considered as a.c. ground. Also different capacitance in this circuits are (the capacitance are listed considering the facts that for TSOS process $C_{ds} = 0$ and $C_{gs} >>$

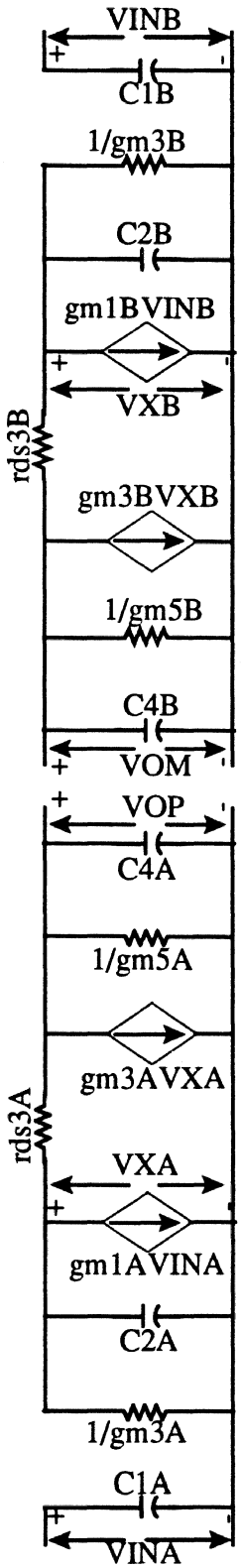


Figure 20 Small signal model for differential pair column amplifier

C_{dg}).

$$C_{1A} = C_{gs1A}$$

$$C_{2A} = C_{gs3A} + C_{ds2A} + C_{dg2A} + C_{ds1A} \equiv C_{gs3A}$$

$$C_{3A} = C_{ds3} \equiv 0$$

$$C_{4A} = C_{ds4A} + C_{ds5A} + C_{dg4A} + C_{dg3A} + C_{gs5A} \equiv C_{gs5A}$$

C_{dg1A} being very small is neglected. Also $g_{m5A} >> g_{ds4A}$, $g_{m3A} >> g_{ds2A}$, $g_{m3A} >> g_{ds1A}$. Same considerations are made for the other half matched circuit.

Therefore, differential voltage transfer function can be written as [2].

$$\frac{V_{OM}(S) - V_{OP}(S)}{V_{INB}(S) - V_{INA}(S)} = \frac{V_{OUT}(S)}{V_{ID}(S)} = -\frac{g_{m1}}{g_{m5}} \frac{1}{[1+\tau_5 S][1+\tau_3 S]} \tag{25}$$

where,

$$\tau_5 = \frac{C_{gs5}}{g_{m5}}, \tau_3 = \frac{C_{gs3}}{g_{m3}} \tag{26}$$

Thus, the first order analysis of frequency response of differential pair column amplifier has two poles at τ_3 and τ_5.

The output resistance and capacitance were found to be [2].

$$r_{out} = \frac{1}{g_{m5}} \tag{27}$$

and

$$C_{out} = C_{gs5} \tag{28}$$

The bandwidth of the circuit is

$$BW = \frac{1}{r_{out} C_{out}} = \frac{g_{m5}}{C_{gs5}} \tag{29}$$

The gain bandwidth product of the circuit is

$$GBP = \frac{g_{m1}}{C_{gs5}} \tag{30}$$

Gain, bandwidth and gain bandwidth product equations derived above describes the performance of the circuit.

Simulation

The spice simulation of the DC transfer characteristic of the differential column amplifier is shown in figure 21. This simulation was done by ramping one of the differential input from 2.49 volts to 2.51 volts, while keeping the other input steady at 2.5 volts. The reference voltage was applied via the biasing circuit. The read current comes via read driver and the selection is made by COL_R (active high). The output voltage is almost linear for this range and a DC gain of 16 is achieved.

Test Results

The differential pair column amplifier was tested using a 4145A semiconductor parameter analyzer. Reference biasing circuit which provide the bias voltages for these amplifier is also laid out next to the differential pair column amplifier. The reference current of 40 μA is supplied to the read biasing circuit by one of the SMU pin. One of the differential input which is varied from 2.49 V to 2.51 V is also supplied via SMU pin. The other differential input which is held at 2.5 V is supplied

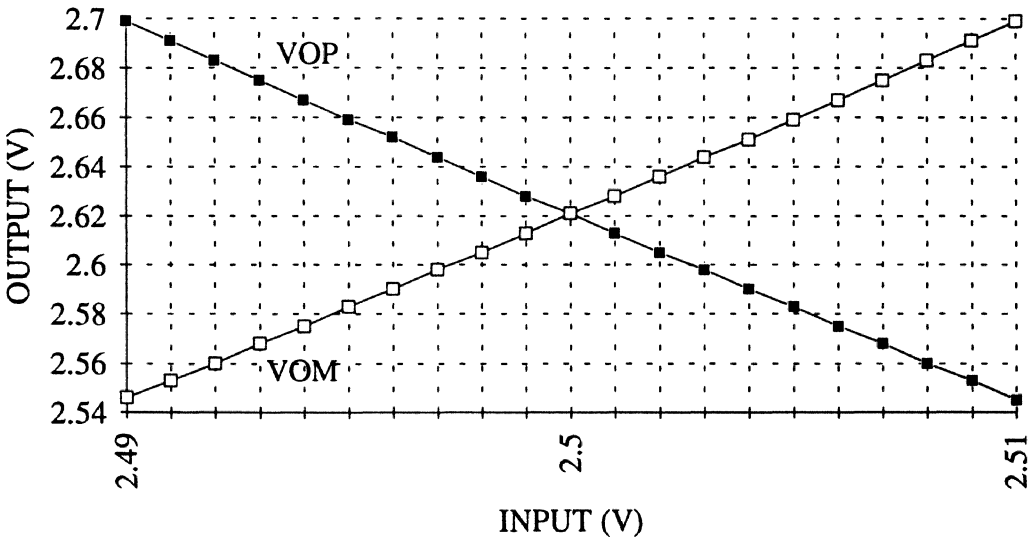


Figure 21 DC transfer characteristic of differential pair column amplifier obtained by simulation

via constant voltage source. Logic COL_R is supplied by external generator. I_READ is supplied by one of the SMU pins, which is held at the value measured in section 3.1.

Finally the output voltage VOP and VOM is monitored using two of the monitor pins on 4145A. The average gain of 18 was achieved with an average offset voltage of 1.5 mV. The output voltage is almost linear for this range. Test results for differential pair column amplifier are shown in figure 22 and figure 23. Figure 23 shows resultant gain with input offset of 1.4 mV and figure 22 shows resultant gain with input offset of 0.1 mV.

On comparing the test results and the simulation results it can be observed that the resultant gain is as expected + 10%. The offset voltage has to be improved by 1 mV. Since the transistors M1A and M1B are laid out in comquad fashion (see section 2.5), which has mean offset voltage of 0.36 mV (see section 2.5), the resultant offset voltage is due to the current mismatch in the drain of M1A and M1B. This error can be eliminated by layout consideration from the transistor M1A and M1B (DDP) to the drain of M2A and M2B. Also proper layout technique (i.e. common centroid) for cascade and load transistor in column amplifier will improve the offset voltage. Once the offset voltage is brought down to less than 0.5 mV in this stage it is feasible to measure an 1 mV of signal.

Comparator

The two stage feedforward comparator is the second and third stage of the

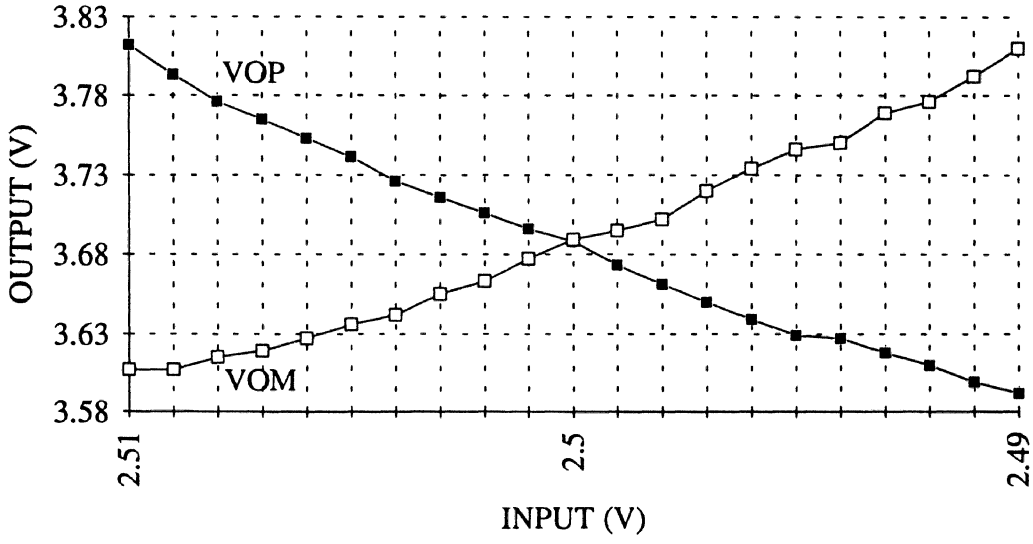


Figure 22 DC transfer characteristic of differential pair column amplifier

obtained by testing (V_{os} = 0.1 mV)

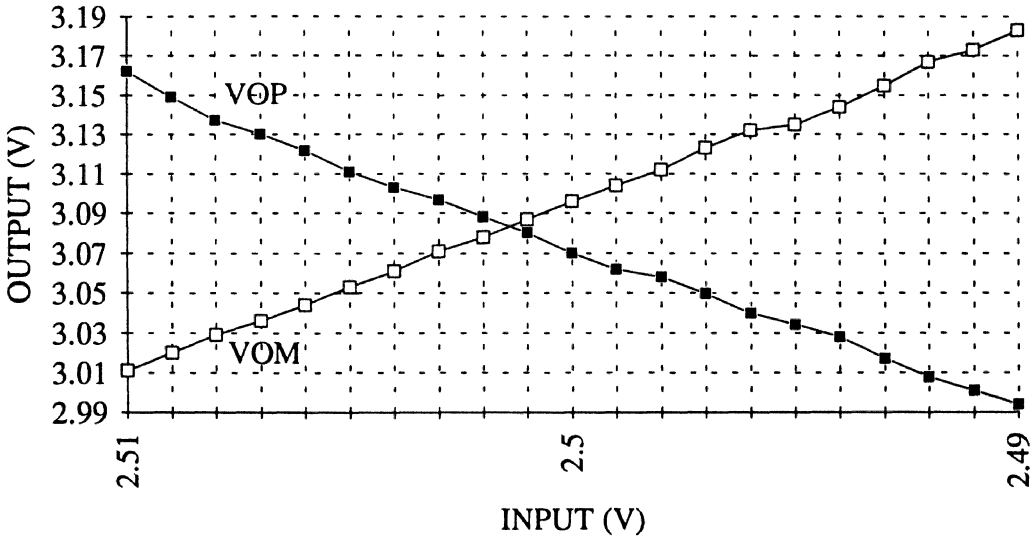


Figure 23 DC transfer characteristic of differential pair column amplifier obtained by testing (V_{os} = 1.4 mV)

three stages involved in the amplification of the hall sensed signal during the read mode of the MHRAM. Single stage comparator is the basic building block for an two stage feedforward comparator. A novel all NMOS differential comparator is used. It is same as conventional CMOS comparator, except that the active loads are realized using NMOS transistors.

The single stage comparator is shown in figure 24. It has two reference biasing pins VB1 and VB2 which comes from comparator biasing circuit (see section 3.5), two differential input pins VIN1 and VIN2, and two output pins VOUT1 and VOUT2. Transistors M1A and M1B are differential input pair of comparator. Transistors M2A and M2B are active resistor loads. Transistors M3A and M3B are current sources. Gates of M3A, M3B and M4 are supplied by the biasing voltages. The small signal analysis of differential in / differential out comparator can be referred in [19].

The gain of the comparator is given as

$$\frac{V_{OUT2}(S)-V_{OUT1}(S)}{V_{IN1}(S)-V_{IN2}(S)}=\frac{V_{OUT}(S)}{V_{id}(S)}=\frac{g_{m1}}{g_{m2}}\frac{\omega_1}{(S+\omega_1)} \tag{31}$$

where

$$\omega_1=\frac{g_{m2}}{C_{gs2}} \tag{32}$$

The bandwidth is given as

$$BW=\frac{g_{m2}}{C_{gs2}} \tag{33}$$

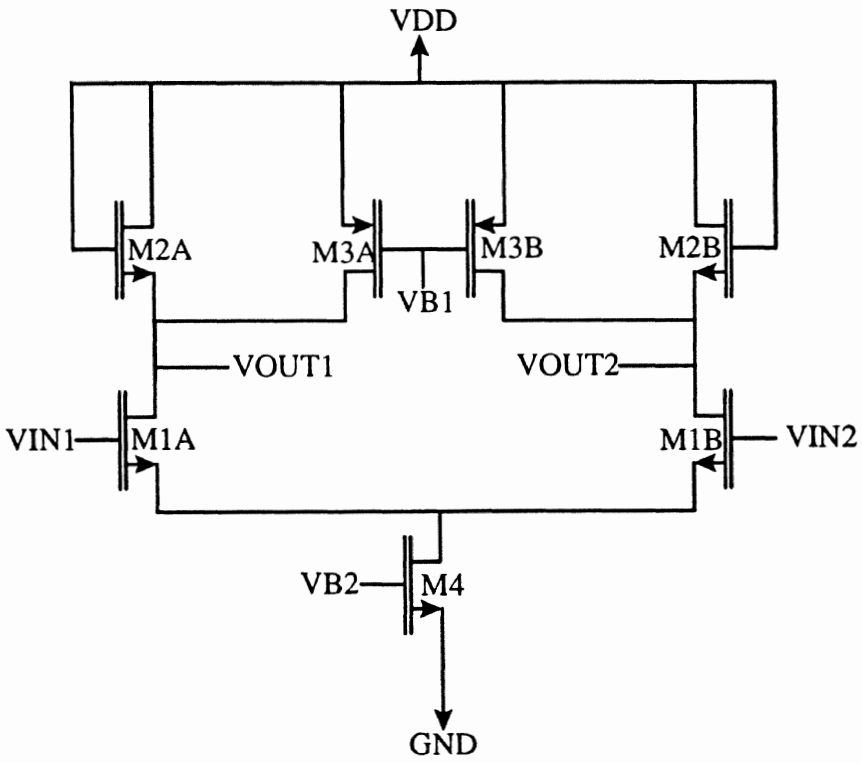


Figure 24 Single stage comparator

From equations 31 and 33,

$$GBP = \frac{g_{m1}}{C_{gs2}} \tag{34}$$

Thus the following gain, gain bandwidth product and bandwidth equations describe the performance of the single stage comparator.

Two stage feedforward comparator is shown in figure 25. It is expected to have a gain near 70. The drop in the gain is due to the ratio of the input capacitance to autozero capacitor. This two stage feedforward comparator is controlled by three clock signals PHI_0, PHI_1 and PHI_2 supplied externally. Three inverter in series are used to generate PHI_0BAR. VOP and VOM are the differential input to the autozero comparator which is fed by the differential pair column amplifier (see section 3.2). VAZ, an autozero reference voltage which comes from autozero biasing circuit (see section 3.5) is designed to have a value which is equal to the magnitude of a DC bias point of the differential pair column amplifier. This increases the autozeroing efficiency by decreasing the settling time.

Autozeroing is accomplished by applying VAZ, while shorting the output and input of the single stage comparator i.e. operating in unity gain (PHI_1 and PHI_2 active high). Starting at the first stage and working forward to the second stage via the PHI_1 and PHI_2 clocks, the bypass transistors are opened. Once the autozeroing phase is completed PHI_0 transition down applying signal from differential pair column amplifier to the two stage comparator. VOUT1 and VOUT2 are the final amplified output, which are then fed to analog regenerative latch. This analog

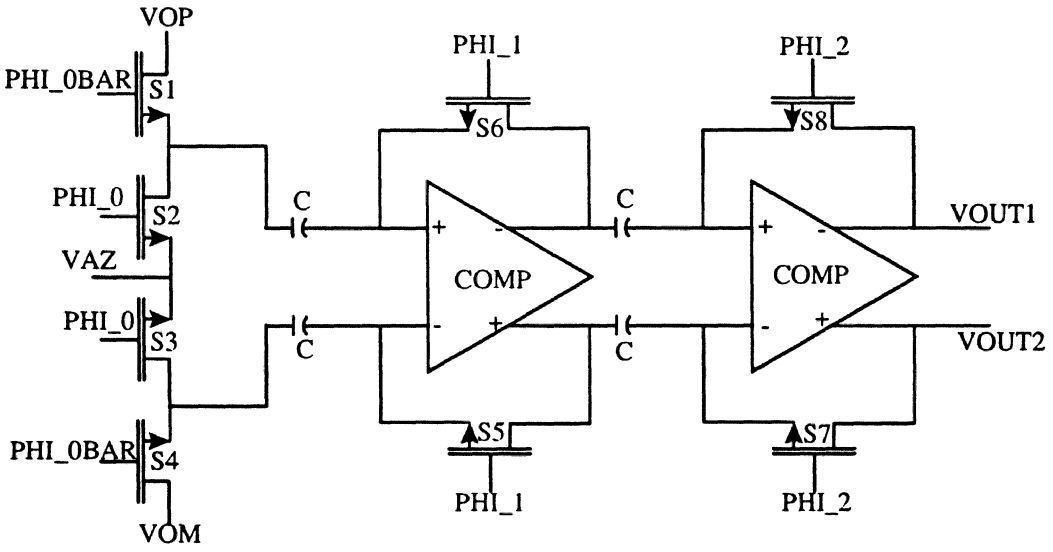


Figure 25 Two stage feedforward comparator

regenerative latch is explained in next section, which flips the output of two stage feedforward comparator to one of the digital logic level.

Simulation

The spice simulation of the DC transfer characteristic of the single stage comparator is shown in figure 26. This simulation was done by ramping one of the input from 2.25 V to 2.75 V, while keeping the other input steady at 2.5 V. The reference voltage was applied via the biasing circuit. The output voltage is almost linear for the input varying from 2.4 V to 2.6 V and DC gain of 10 is achieved in this region. If the input falls outside this range then the gain may increase or decrease depending upon the position of operating point. Combining the two stages of comparator we expect the gain to be somewhere in the region of 70 to 100.

Test Results

The single stage comparator was tested using a 4145A semiconductor parameter analyzer. Comparator biasing circuit which provide the bias voltages for these comparator was also laid out next to single stage comparator. The reference current of -40μA for the comparator biasing circuit was supplied through one of the SMU pins. One of the differential input which is varied from 2.45 V to 2.55 V is also supplied via SMU pins. Other differential input which is kept steady at 2.5 Volts is supplied by Vs (voltage source) pin. Finally the output voltages is monitored using the monitor pins on 4145A. The output voltage is almost linear in this region. The DC gain of 8 was achieved with a mean offset voltage of 5.3 mV. Figure 27 and

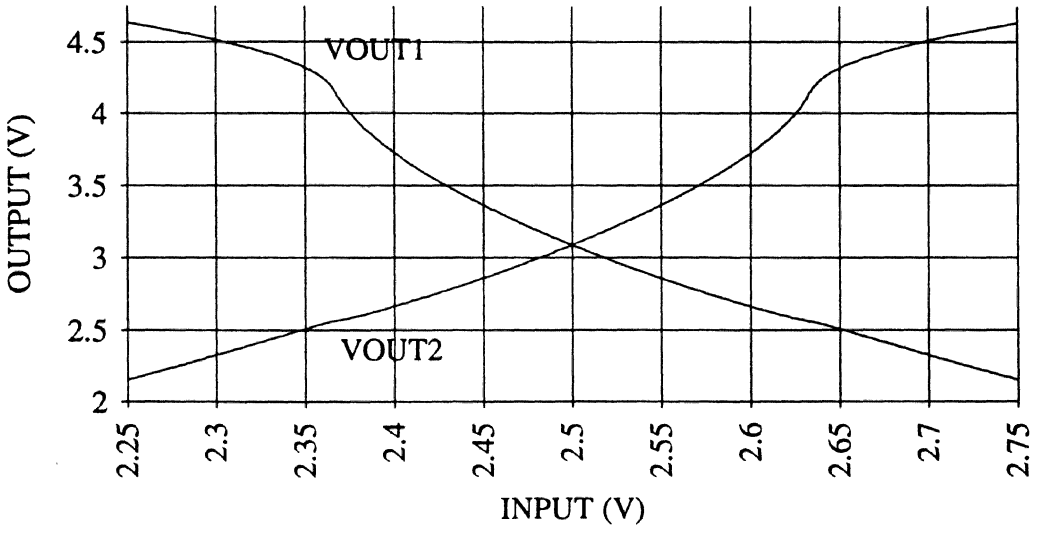


Figure 26 DC transfer characteristic of single stage comparator

obtained by simulation

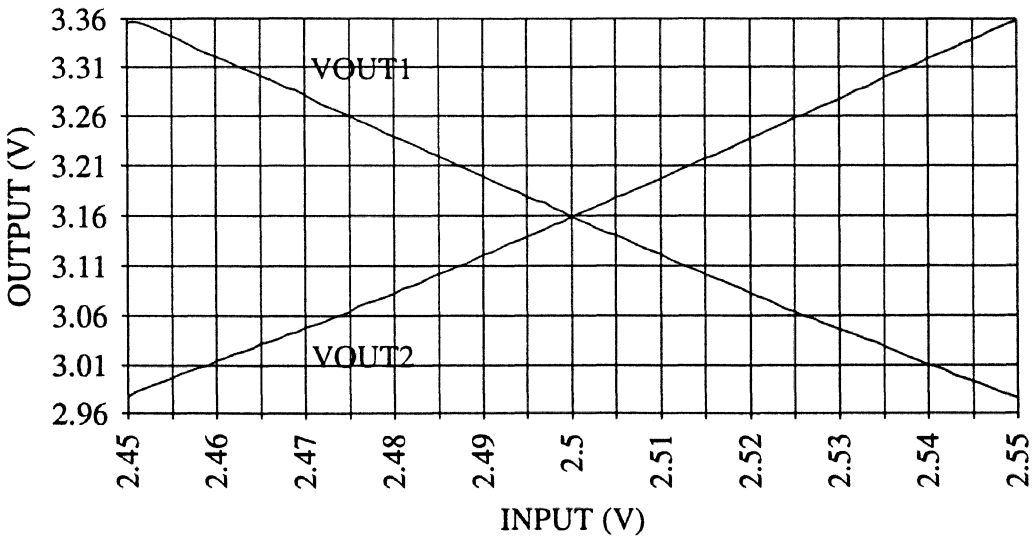


Figure 27 DC transfer characteristic of single stage comparator

obtained by testing (V_{os} = 0 mV)

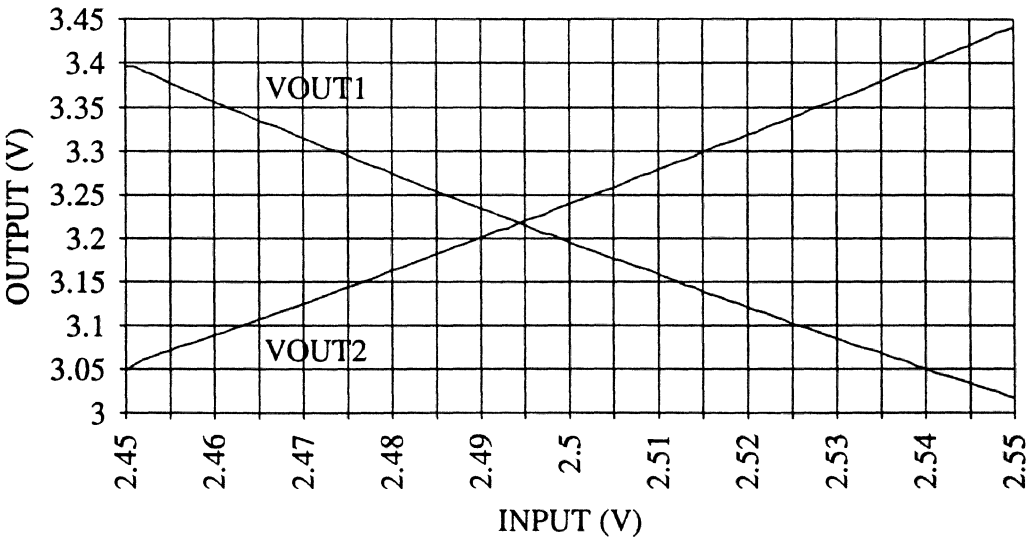


Figure 28 DC transfer characteristic of single stage comparator

obtained by testing (V_{os} = 5.5 mV)

figure 28 shows the test results for single stage comparator. Figure 28 shows the output with a gain of 8 and input offset of 5.5 mV and figure 27 shows the output with a gain of 8 and input offset of 0 mV.

On comparing the test result and simulation result it is seen that the output of the single stage comparator has a gain as expected -20%.

The single stage comparator seemed to work satisfactorily and so the test set up for the autozero was set up as shown in figure 29. The first stage of the single stage comparator was used as the buffering unit for testing the autozeroing of the second stage of the two stage feed forward comparator. Since we expect the signal of 1 mV and the column amplifier has the average gain of 18, we decided to test the autozeroing for the second stage of comparator using 20 mV differential signal at the input of the buffering stage. The one input was held constant at 2.5 V through external generator. The second input was supplied by 2.5 V DC supply plus 20 mV peak-to-peak sinusoidal signal. The PHI_1 was made active low, to make first stage as the buffering unit. The PHI_2 which was generated via clock generator with 20 nS rise and fall time, was supplied using high speed board specially designed for this purpose.

Finally, the outputs were measured, one at a time using the picoprobe, on a 11402 digitizing oscilloscope. Figures 30 and 31 show the autozeroing of the second stage of the two stage feedforward comparator, with the total gain of 46 and 72, when the clocks are switched from 0 V to 5 V and -4.25 V to 4.25 V respectively. Also, the offset voltage is approximately equal to 5 mV when clocks are switched from 0 V

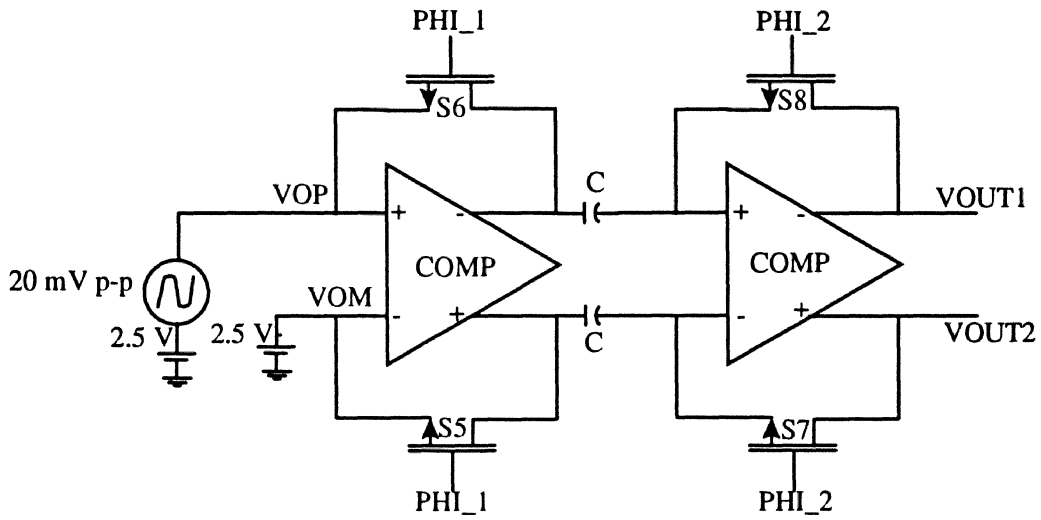
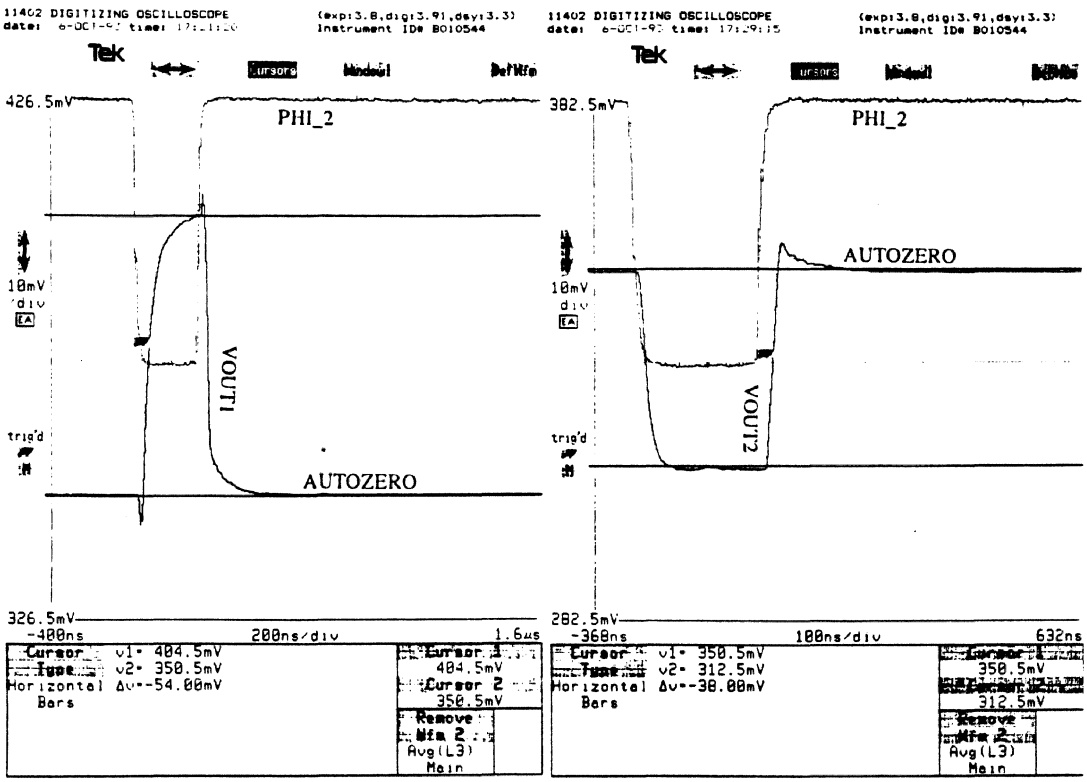
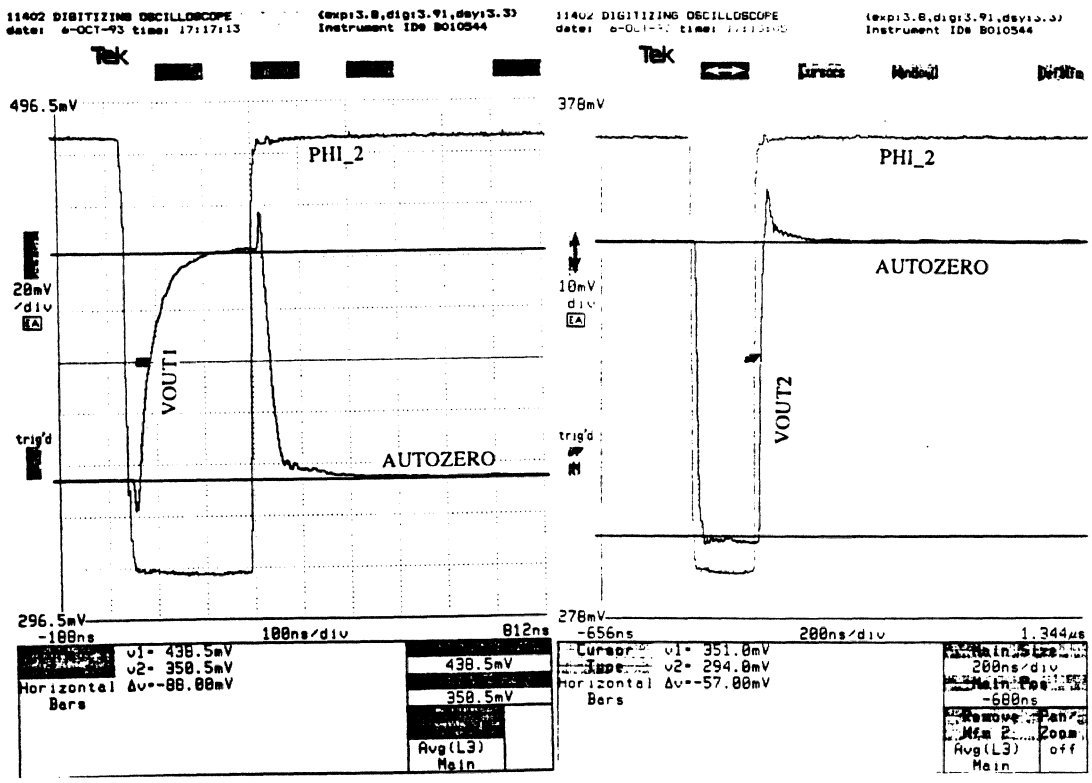


Figure 29 Test setup for autozeroing



V_{os} = VOUT2 - VOUT1 during autozero phase ≈ 5 mV

Figure 30 Output of two stage comparator where second stage is autozeroed with clock varying from 0 V to 5 V



V_{os} = VOUT2 - VOUT1 during autozero phase ≈ 0 mV

Figure 31 Output of two stage comparator where second stage is autozeroed with clock varying from -4.25 V to 4.25 V

to 5 V and is approximately equal to 0 mV when the clocks are switched from -4.25 V and 4.25 V, showing that autozero works satisfactorily when the n-switches are held at negative potential. Hence, we determine that n-switches are leaky. It is difficult to measure the offset voltage accurately due to noisy supply lines. If low noise lines are used then offset after autozeroing could be measured perfectly.

The output shown in the figures 30 and 31 are on 10:1 scale. Clocks which have a different scale, not shown in the figures, helps to determine the starting and ending of the autozeroing.

Latch

Analog regenerative latch is the final stage of the read path. Once the hall sensed signal is amplified by all the three amplification stage, it is then fed to the analog regenerative latch. This latch converts the differential input to one of the digital data logic levels.

The analog regenerative latch is shown in figure 32. It has one reference biasing pin VREFLATCH which comes from latch biasing circuit (see section 3.5), two differential input which comes from two stage feedforward comparator (see section 3.3), one clock PHI_X which controls the latch is supplied externally through clock generator and an output pin OUT. Transistor M2A and M2B are the differential input to the latch. M1A and M1B are the cross coupled transistor which results in regenerativeness. Transistor M3 acts as a switch. Transistor M4-M5 and M6-M7 acts as a level shifter circuit.

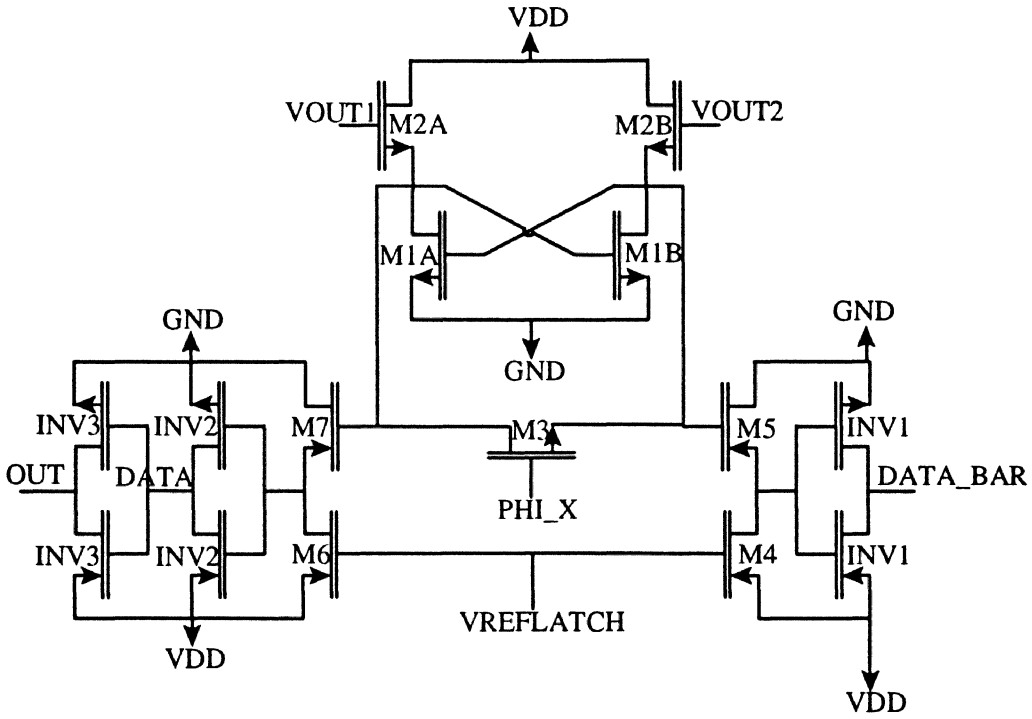


Figure 32 Analog Regenerative Latch

Analog latch is designed to have an high output as long as PHI_X is active high. On applying the differential input signal, when the PHI_X transits to active low, the regenerative cycle will start, resulting in one of the digital level data output, depending upon the value of differential input signal.

Simulation

The spice simulation of the transient characteristic for a analog regenerative latch is shown in figure 33 with an response time of 12 nSec. Both the inputs of the latch are held at constant voltages of 2.3 V and 2.7 V respectively. The reference voltage is supplied by the latch biasing circuit. Initially PHI_X is kept active high and hence output constantly remains high for any change in the input. On PHI_X going active low the input is reflected at the output and a valid digital signal is achieved at the output. It was simulated for different differential inputs varying from 0.3 V to 1.2 V with good results.

Test Results

The analog regenerative latch was tested using a 4145A semiconductor parameter analyzer. Latch biasing circuit which provided the bias voltage for these latch was also laid out next to analog regenerative latch. The latch reference current of 40 μA was supplied through one of the SMU pin. Clock PHI_X was supplied via external generator. This test was done to see the working of the latch rather than the transient response and the result is shown in figure 34. The two differential inputs which are held at constant voltages of 2.3 V and 2.7 V, are supplied via constant

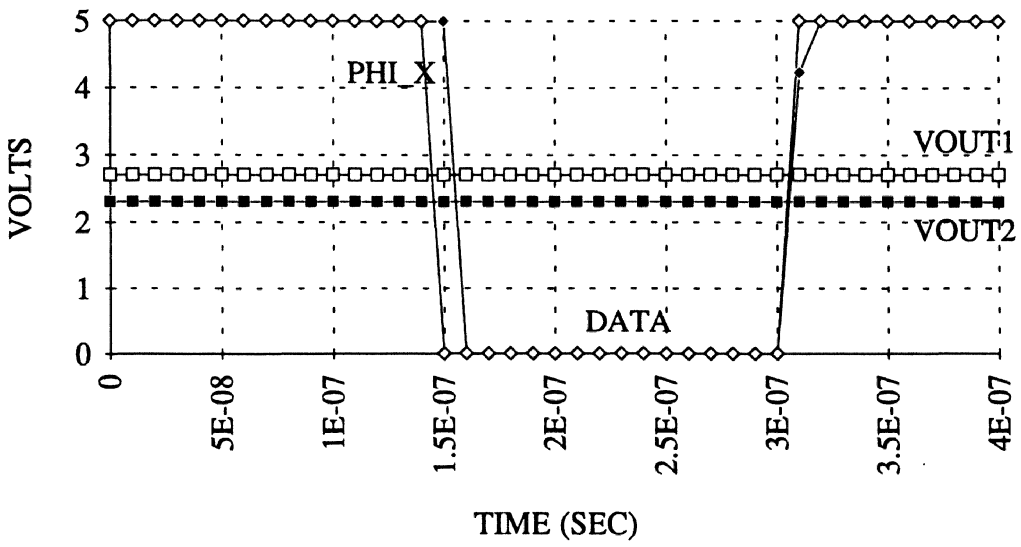


Figure 33 Transient characteristic of analog regenerative latch obtained by simulation

voltage sources Vs pins. The output OUT was monitored using the Vm pin on 4145A.

First the clock PHI_X is turned ON to active high. After some time PHI_X is switched to 0 V by hand and the latch condition is noted for the current value. This test sequence was repeated with different differential input voltage varying from 1.4 V to 0.2 V. Results of this test are shown in Table 4.

On comparing the test and the simulation results we can determine that the analog regenerative latch works satisfactorily. Sensitivity of analog regenerative latch can be improved by an order of magnitude with some modifications in the circuit. Sensitivity for this latch was low because the n-type devices were leaky and regenerative circuit for this latch consists of n-transistors.

Reference Biasing Circuits

Reference biasing circuits plays an important role in the design of the analog circuits. In the design of the MHRAM five biasing circuits were used, each providing different biasing voltages and mirroring current. This biasing circuits are Write biasing circuit, Read biasing circuit, Autozero biasing circuit, Comparator biasing circuit and Latch biasing circuit and are explained in the following section.

Write biasing circuit :

The write biasing circuit is shown in figure 35. It has one input reference current pin IWREF supplied externally and two output bias voltage pins VB13W and VB44W. IWREF for the MHRAM is derived to be 2.5 mA. Transistor M1 and M2 forms an current mirror circuit. Transistor M1 and M4 forms a current mirror circuit

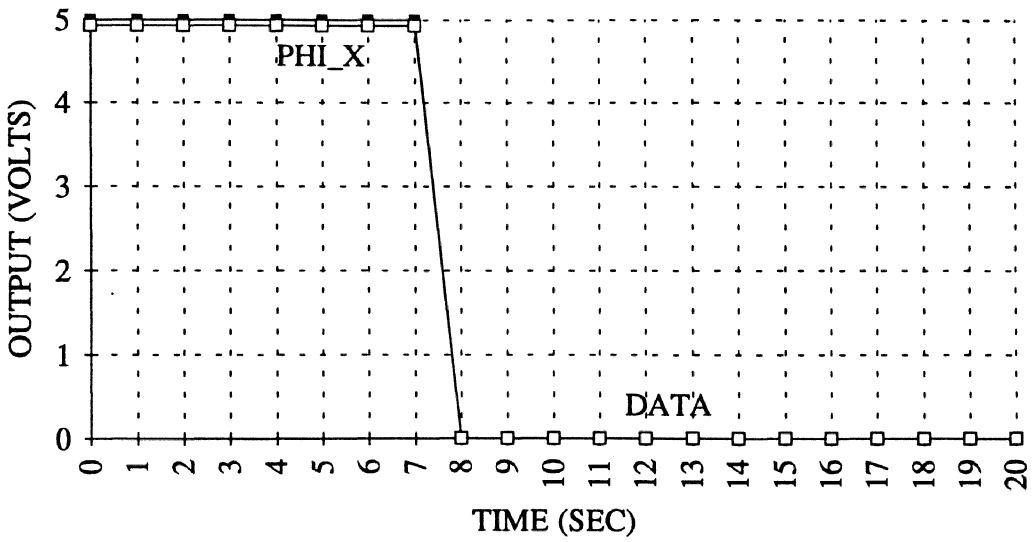


Figure 34 Working of analog regenerative latch obtained by testing

VOUT1	VOUT2	ΔVIN	Test For Level DATA	Pass/Fail
3.3 V	1.9 V	1.4 V	High	Pass
3.1 V	2.1 V	1.0 V	High	Pass
3.0 V	2.2 V	0.8 V	High	Pass
2.9 V	2.3 V	0.6 V	High	Pass
2.8 V	2.4 V	0.4 V	High	Pass
2.7 V	2.5 V	0.2 V	High	Pass
2.5 V	2.7 V	-0.2 V	Low	Pass
2.4 V	2.8 V	-0.4 V	Low	Pass
2.3 V	2.9 V	-0.6 V	Low	Pass
2.2 V	3.0 V	-0.8 V	Low	Pass
2.1 V	3.1 V	-1.0 V	Low	Pass
1.9 V	3.3 V	-1.4 V	Low	Pass

Table 4 Test results for Analog Regenerative Latch

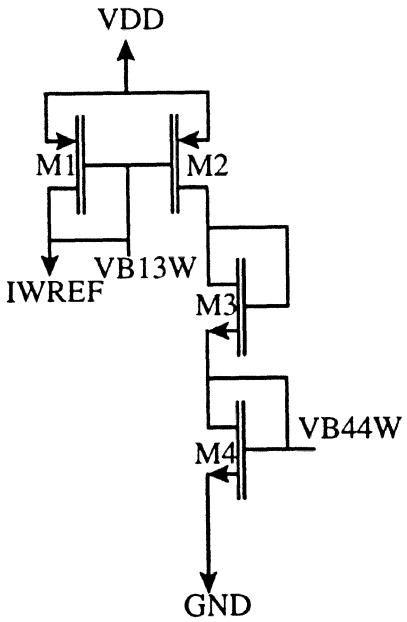


Figure 25 Write reference circuit

with transistors (provided there source are at same potential) whose gates are connected to bias pins VB13W and VB44W respectively. This circuit provides bias voltages for the row and column drivers (see section 3.1).

Read biasing circuit :

The read biasing circuit is shown in figure 36[A]. It has one input reference current pin IRREF supplied externally and three output bias voltage pins VB13R, VB34R and VB44R. IRREF for the MHRAM is derived to be 40 μA. Transistor M1 and M2 forms an current mirror circuit. Transistors M1, M3 and M4 forms a current mirror circuit with transistors (provided there sources are at same potential) whose gates are connected to VB13R, VB34R and VB44R respectively. This circuit provides bias voltages for row driver (see section 3.1), differential pair column amplifier (see section 3.2) and autozero biasing circuit (see section 3.5).

Autozero biasing circuit :

The autozero biasing circuit is shown in figure 36[B]. It has two input pins VB34R and VB44R which comes from read biasing circuit (see section 3.5) and one output pin VAZ. Transistor M3A and M4A forms an current mirror with M3 and M4 (read biasing circuit) respectively. This circuit provides bias voltage to two stage feedforward comparator (see section 3.3).

Latch biasing circuit :

Latch biasing circuit is shown in figure 37. It has one input reference current pin IFFREF supplied externally and one output pin VREFLATCH. IFFREF for the MHRAM is derived to be 40 μA. This circuit is similar to the read biasing circuit, the

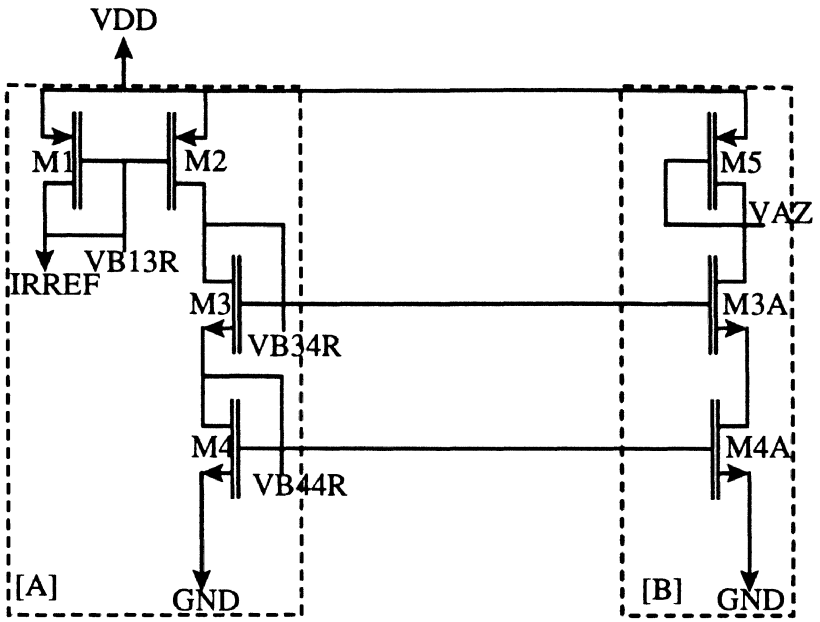


Figure 36 [A] Read biasing circuit

Figure 36 [B] Autozero biasing circuit

Figure 36 Biasing circuit

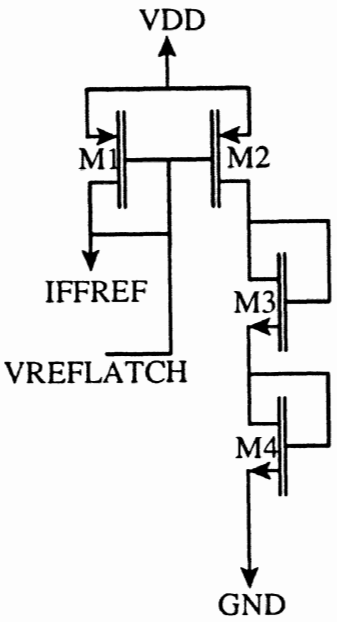


Figure 37 Latch biasing circuit

only difference being different transistor geometries. This circuit provide bias voltage for the analog regenerative latch (see section 3.4).

Comparator biasing circuit :

Comparator biasing circuit is shown in figure 38. It has one input reference current pin ICOMPREF supplied externally and two output pins VB1 and VB2. ICOMPREF for the MHRAM is derived to be -40 μA. Transistor M1A-M1B and M2A-M2B forms the current mirror. M2A and M3 forms current mirror circuit with transistors (provided there sources are at the same potential) whose gates are connected to VB1 and VB2 respectively. This circuit provide bias voltages to single stage comparator and two stage feedforward comparator (see section 3.3).

Simulation

The spice simulation of the biasing circuits for write, read, autozero, comparator and latch was carried out. Reference current of 40 μA was supplied for read biasing circuit which in turn will also be supplied to autozero biasing circuit. Reference current of 2.5 mA, 40 μA and -40 μA was supplied for write, latch and comparator biasing circuits respectively. Simulation results are shown in Table 5.

Test Results

The test for biasing circuits were carried out on a 4145A semiconductor parameter analyzer. For each biasing circuit there respective reference current were supplied via SMU pins, and the bias voltages were monitored using SMU and Vm pins on 4145A. The measured reference voltages are shown in Table 5.

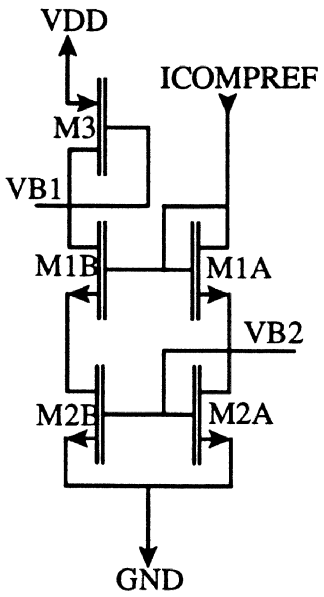


Figure 38 Comparator biasing circuit

Biasing Circuits	Simualtion Results	Test Results
Write Biasing Circuit		
VB13W	2.99 V	2.94 V
VB44W	1.62 V	1.39 V
Read Biasing Circuit		
VB13R	3.28 V	3.34 V
VB34R	2.49 V	2.23 V
VB44R	1.35 V	1.20 V
Autozero Biasing Circuit		
VAZ	2.91 V	3.17 V
Comparator Biasing Circuit		
VB13	3.16 V	3.17 V
VB44	1.52 V	1.30 V
Latch Biasing Circuit		
VREFLATCH	3.43 V	3.40 V

Table 5 Simulation and Test results of Biasing Circuits.

On comparing the test and the simulation results it is seen that the biasing circuits works as designed. Since, n-threshold was lower by 0.2 V then expected, few bias voltages which were dependent on n-transistor were lower than expected.

Logic Circuits

Designing of complete 2X2 MHRAM, requires designing of various logic circuits for the control of the input/output pins and also for the selection of a particular cell in an array using few address lines. Inverter, NAND and NOR gates which are the basic building blocks for the logic circuits are explained in this section. Also, column select amplifier which activates particular differential pair column amplifier (see section 3.1) is explained in brief.

Column Select Amplifier

Column select amplifier is shown in figure 39. It is basically a OR gate. It has two input pins RWB and COL_SEL supplied externally and one output pin COL_R. When both the inputs are active high then COL_R will be activated, resulting in a selection of differential pair column amplifier in a particular column.

Simulation :

The spice simulation was carried out for column select amplifier. It was checked for all the possible conditions and its results are shown in form of the truth table in Table 6.

Test Result :

Testing of column select amplifier was done using 4145A semiconductor

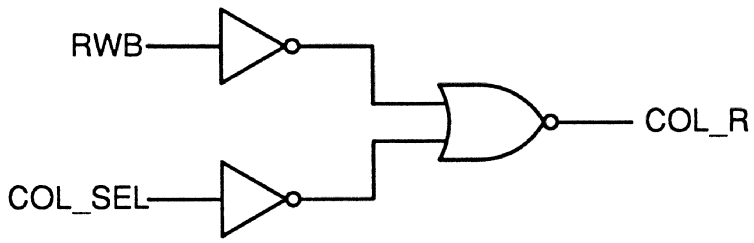


Figure 39 Column select amplifier

RWB	COL_SEL	COL_R
0 V	0 V	0 V
0 V	5 V	0 V
5 V	0 V	0 V
5 V	5 V	5 V

Table 6 Simulation and Test results for Column Select Amplifier

parameter analyzer. Both the inputs were supplied by using constant voltage pins Vs. The output was measured using channel Vm for all the possible combination of inputs. The test results were found to be same as that of simulations.

Inverter

The inverter shown in figure 40 was tested using 4145A semiconductor parameter analyzer. Its input was varied from 0 V to 5 V via SMU pin. The output was monitored using channel Vm. The resultant gain and the noise margin are shown in Table 7A. Since, we want to have an equal noise margin for inverter, and from Table 7A we can see that the high noise margin (HNM) is not equal to the low noise margin (LNM). Hence, the width of the p-channel transistor was changed to 34.4 μm from 30 μm and the new noise margin is shown in Table 7B.

NAND

Four input NAND gate shown in figure 41 was tested using a 4145A semiconductor parameter analyzer. First one of the input was varied from 0 V to 5 V via SMU pin, and the remaining inputs were supplied 5 V via external generator. The output is monitored using Vm channel and respective gain and the noise margins are noted. Then two inputs are varied simultaneously from 0 V to 5 V, with the other two inputs being held at 5 V and the output is noted. Similarly the readings for three inputs and four inputs varying simultaneously from 0 V to 5 V were noted down. This readings are as shown in Table 8. The HNM and LNM were found to be almost equal and greater then 20% of the supply, hence no modification were made in this

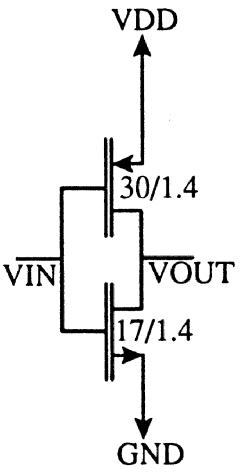


Figure 40 Inverter

P-transistor of 30/1.4	High Noise Margin	Low Noise Margin	Gain
N-transistor of 17.6/1.4	2.1 V	1.95 V	15.8

(A) Test results

P-transistor of 34/1.4	High Noise Margin	Low Noise Margin
N-transistor of 17.6/1.4	1.95 V	1.97 V

(B) Simulation results after modification.

Table 7 Results of Inverter

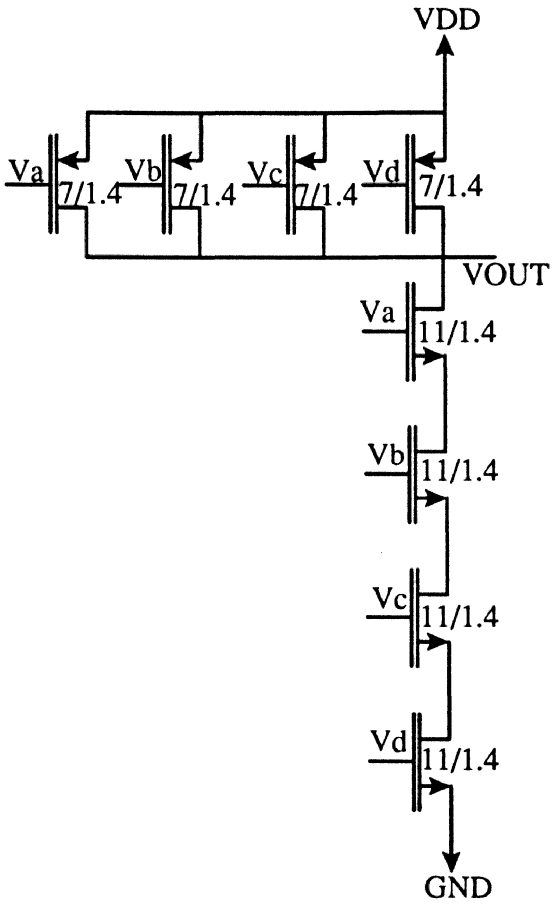


Figure 41 Four input NAND

Number of Inputs simultaneously varying from 0 V to 5 V for P-transistor of 7/1.4 N-transistor of 11/1.4	High Noise Margin	Low Noise Margin	Gain
One	2.51 V	1.28 V	15.74
Two	1.62 V	2.24 V	21.40
Three	1.32 V	2.60 V	24.26
Four	1.20 V	2.84 V	24.94

Worst-case High Noise Margin = 1.20 V

Worst-case Low Noise Margin = 1.28 V

Table 8 Test results for four input NAND.

circuit.

NOR

Four input NOR gate shown in figure 42 was tested using a 4145A semiconductor parameter analyzer. First one of the input was varied from 0 V to 5 V via SMU pin, and the remaining inputs were supplied 0 V via external generator. The output is monitored using Vm channel and respective gain and the noise margins are noted. Then two inputs are varied simultaneously from 0 V to 5 V, with the other two inputs being held at 0 V and the output is noted. Similarly the readings for three inputs and four inputs varying simultaneously from 0 V to 5 V were noted down. This readings are as shown in Table 9A. The HNM is 40% of the supply and LNM is 15% of the supply and hence the modifications in circuit geometries were done. The new width of the n-channel and p-channel transistors are 4 μm and 29μm respectively. The simulation results for modified geometry with LNM of 20% of the supply and HNM of 30% of the supply is shown in Table 9B.

XNOR

XNOR was tested for its functionality using 4145A semiconductor parameter analyzer. Two of its inputs were supplied using voltage source Vs and the output was monitored using Vm. Result showed that XNOR works satisfactorily for supply ranges of 5 V and 3.3 V.

Multiplexer

4:1 multiplexer was tested for its working using 4145A semiconductor

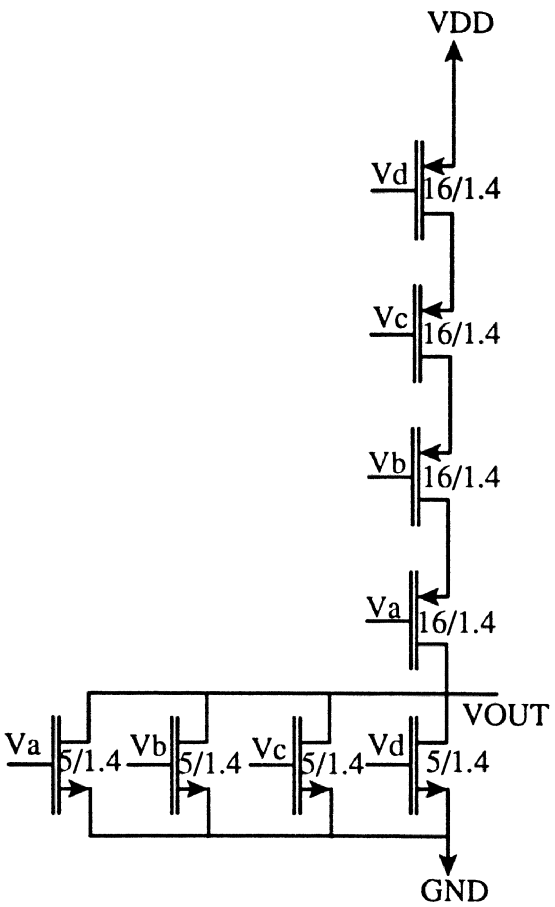


Figure 42 Four input NOR

Number of Inputs simultaneously varying from 0 V to 5 V for P-transistor of 16/1.4 N-transistor of 5/1.4	High Noise Margin	Low Noise Margin	Gain
One	2.02 V	1.84 V	15.38
Two	2.60 V	1.11 V	14.70
Three	3.00 V	0.82 V	17.22
Four	3.24 V	0.72 V	18.96

Worst-case High Noise Margin = 2.02 V

Worst-case Low Noise Margin = 0.72 V

(A) Test results.

Modified Four input NOR P-transistor of 29/1.4 N-transistor of 5/1.4	High Noise Margin	Low Noise Margin
	1.47 V	1.01 V

(B) Simulation results after modification.

Table 9 Results for four input NOR

parameter analyzer. Four of its inputs were connected using SMU pins. The selection lines were supplied via Vs pins and the output was monitored using Vm pin. Results showed that 4:1 mux works satisfactorily.

All the logic gates which have been designed are to be used in the second phase of the MHRAM design. Next chapter explains the complete read and write path along with its simulation results.

CHAPTER IV

2 X 2 MHRAM

The goal was to design building blocks for MHRAM, which when combined will work as complete MHRAM. All the building blocks and the memory cell have been discussed in the previous chapter. This chapter focuses on the read and write path implementation using the building blocks. Writing to a hall sensor based memory cell involves passing a current over the top of a magnet in one of the two directions depending on the logic state to be stored. This is accomplished with a bi-directional write current through the selected memory cell. The RWB pin determines which mode the row and column driver would be operating in.

The read operation involves biasing the gate of the MOS hall sensor to the desired DC voltage and applying a drain to source voltage to MOS hall sensor. In the presence of the magnetic field, with the current passing from drain to source of the MOS hall sensor, results in a hall voltage across the hall MOSFET channel tabs points. It is the resulting differential voltage signal which is amplified to develop the data signal.

Figure 43 shows the architectural view of complete 2X2 MHRAM (4-bit MHRAM) , an twenty-three pin package. The twenty-three pin package includes

* Two seperate VDD and GND pairs for analog and digital circuits

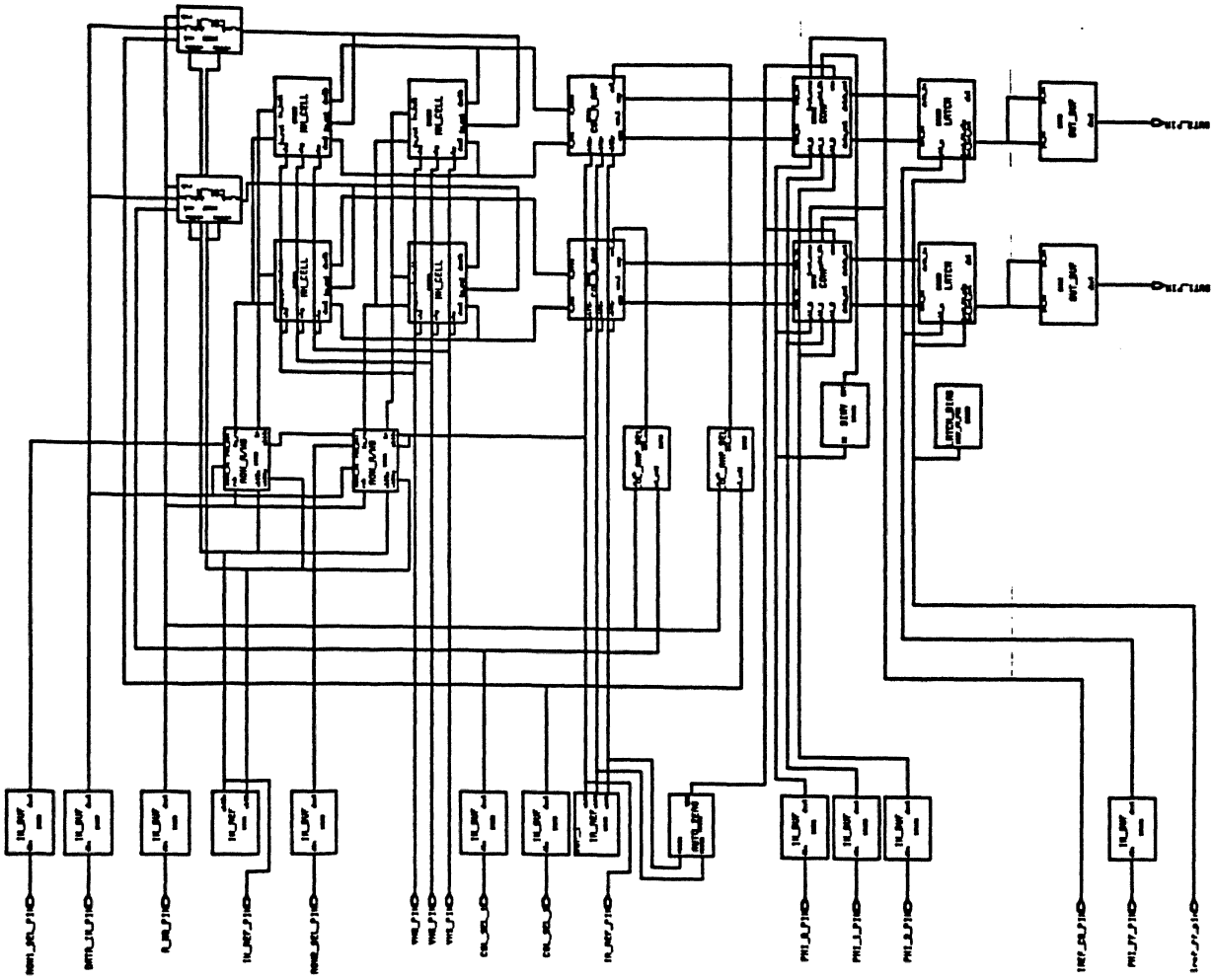


Figure 43 Arrangement of 2 X 2 MHRAM

* Four current bias supply (one each for the write, read, latch and comparator biasing circuits)
* Four clock signals (three clocks used for autozeroing of two stage feedforward comparator and one clock for the analog regenerative latch)
* Two column select pins (to select a particular column)
* Two row select pins (to select a particular row)
* Three pins VHG, VHD and VHS (to bias the MOS hall sensor for generation of a hall voltage)
* One RWB pin (which decides the read/write mode of operation)
* One DATA_IN pin (which determines the data to be written)
* Two output pins (one per each column)

This pins controls the complete memory. For large memory array decoding and encoding circuits along with few other digital circuits may have to be included. Now in the following part of this chapter complete working of read and write path is discussed.

Write Path

Figure 44 shows the block diagram of the complete write path which includes row read/write driver, column write driver, memory cell and write biasing circuit. Setting pin RWB active low activates the driver in write mode. In write mode row and column driver together selects one memory cell via its row and column select pins ROW_SEL and COL_SEL. Bias voltages for drivers are provided by write biasing

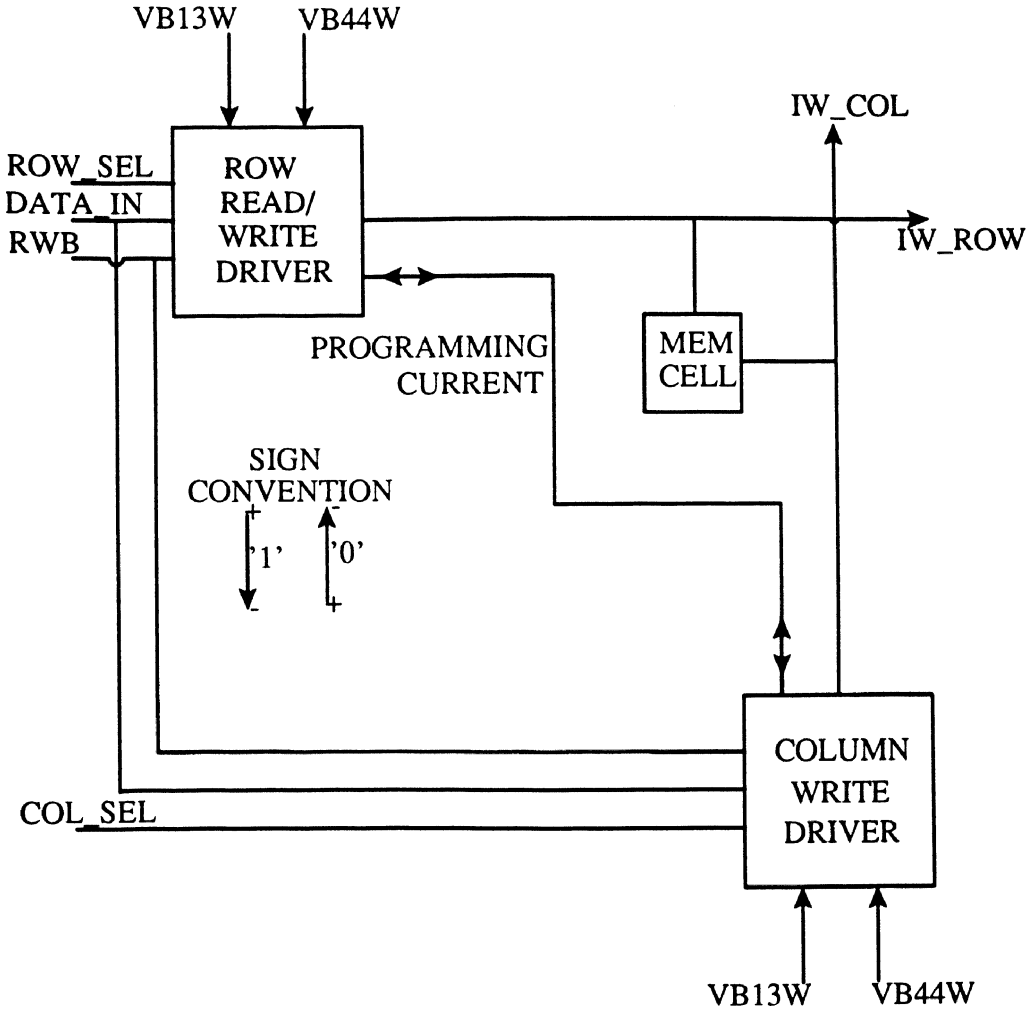


Figure 44 Write current path and sign convention

circuit. Depending upon the logic level of DATA_IN, row and column driver will sink and source current through its pins IW_ROW and IW_COL, to program an magnet. Programmed value depends on the direction of the write current. Figure 44 also shows the sign convention (i.e. direction of current for the particular data to be stored in the hall sensor).

Read Path

Figure 45 shows the complete read path which includes a memory cell having two hall cell in parallel (see section 2.4), differential paired column amplifier, two stage feedforward comparator and analog regenerative latch. In read mode one particular memory cell is selected via row and column select pins ROW_SEL and COL_SEL. Setting RWB pin active high activates the selected row driver in read mode, hence providing read current to the DDP of the selected memory cell. Also, RWB and COL_SEL together will activate one of the differential pair column amplifier.

The output of the hall cell would be a small differential signal. Analog design methods are critical when handling small differential signals and encompasses both circuit design and layout technique. Hence the two hall cells are used in parallel to cancel the systematic offset (see section 2.4) of the hall cell and the DDP of differential pair column amplifier is laid in a comquad arrangement (see section 2.5) to minimize the input offset voltage of the first amplification stage.

The output of the hall sensor cell is fed to the differential pair column

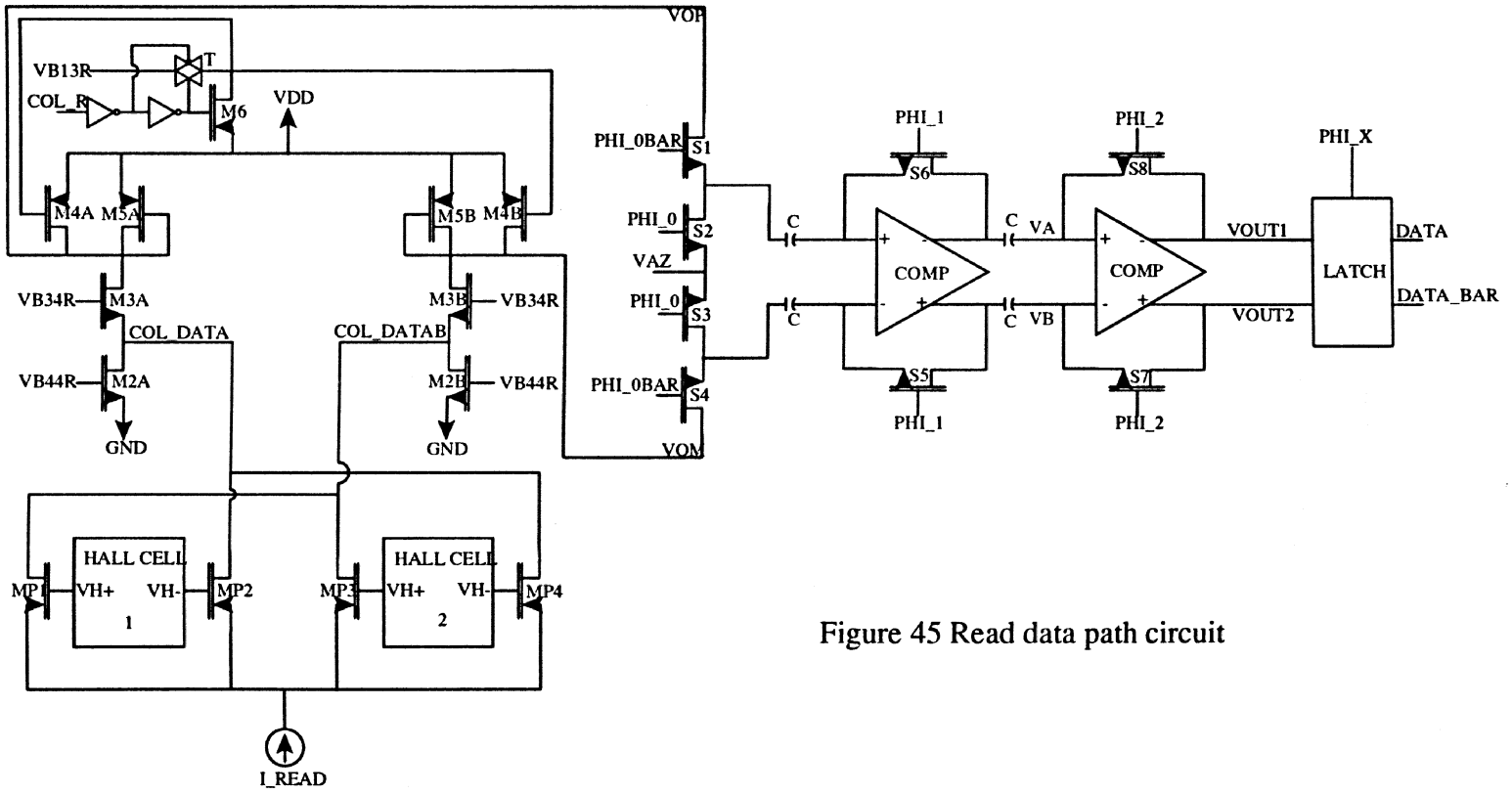


Figure 45 Read data path circuit

amplifier. The output of this column amplifier is fed to the two stage feedforward comparator. The feedforward comparator design uses two single stage comparator (section 3.3), each stage with the gain of eight. Autozeroing is accomplished by applying VAZ (autozero reference voltage) while shorting the output and input of the comparator i.e. unity gain (PHI_1 and PHI_2 are active high). Starting at the first stage and working forward to the second stage via the PHI_1 and PHI_2 clocks, the bypass transistors are opened. The autozero reference voltage was selected to be equal in magnitude to the DC bias point of the column amplifier, this increases the efficiency of autozeroing by decreasing the settling time.

Once the autozeroing phase is completed PHI_0 transitions down applying signal from differential pair column amplifier to the autozeroing comparator. At this point read signal must have been amplified by 800 times. This signal is impressed at the latch input, which is equalized by PHI_X. When PHI_X transits down equalization ends and valid data appears at the output data pin. The output is valid as long as the PHI_X is active low. The latch has enough gain to set the digital signal. Read access time consists of decode (row and column select), autozeroing, evaluation and latched valid data. The transition of clock signals and data is shown in figure 46. In the following part of this chapter simulations of read and write paths are discussed.

Simulation

The spice simulation was done for the write path by connecting a small resistance of 200Ω between the row and the column driver. Then the input signals

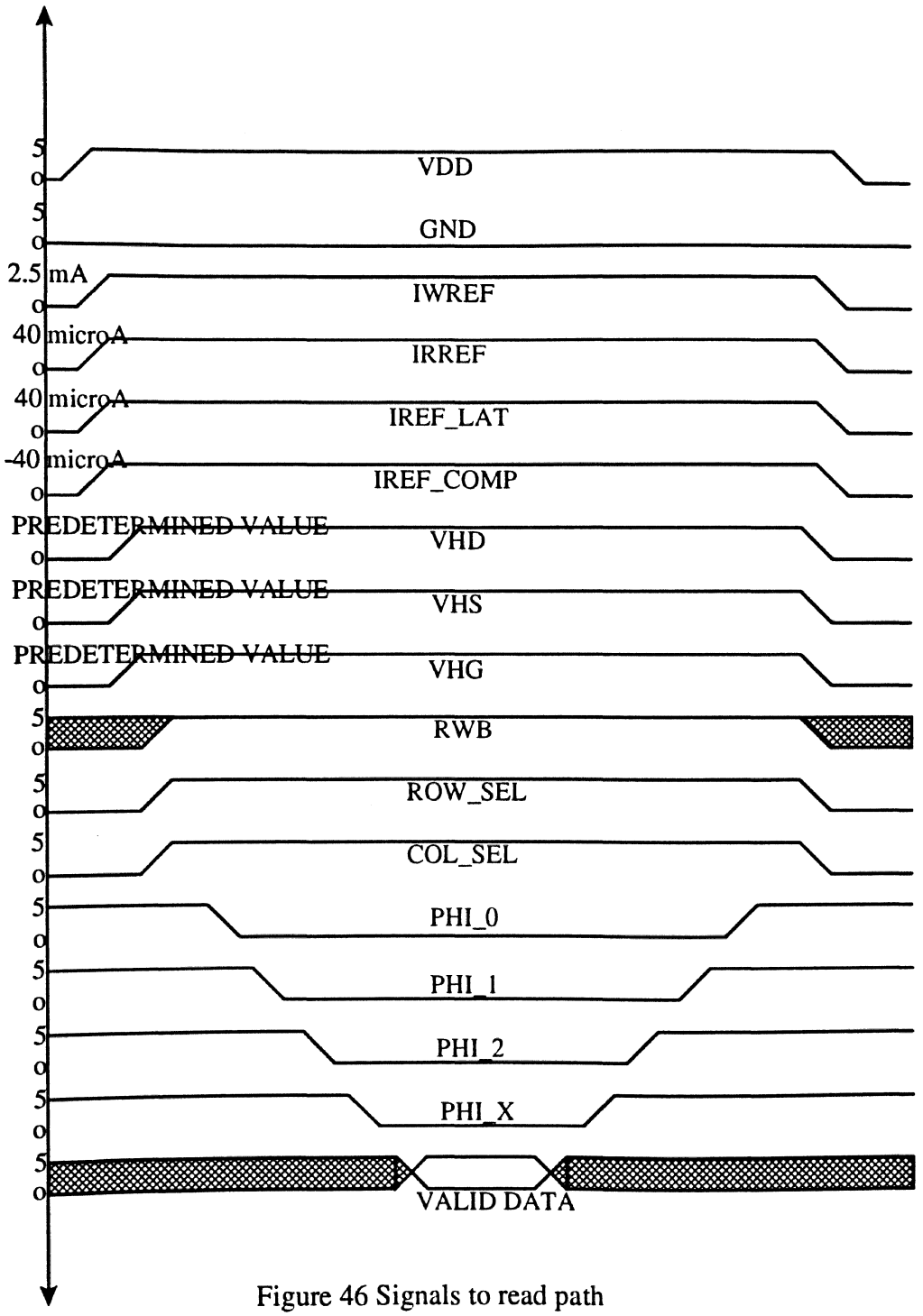


Figure 46 Signals to read path

COL_SEL, ROW_SEL, DATA_IN and RWB were supplied along with the bias voltages from the write biasing circuit. The simulated sinking and sourcing current were found to be same as one shown in Table 3 (see section 3.1).

The spice simulation for the transient analysis of read path was done and the result is shown in figure 47 to figure 55. The differential signal of 1 mV was applied at the input of the differential pair column amplifier. All the bias voltages were supplied using biasing circuits. Clocks were used with the rise time and fall time of 10 nS. Output after each stage of amplification is shown along with the final output in figures 47 to 55. An access time of approx. 100 nS is predicted from address setup to latch output.

Result of all the basic building blocks is already known from the previous chapters. It could be seen that 1 mV signal can be read, but proper measures has to be taken to minimize the offset voltage. The following chapter includes conclusions and recommendations for the next phase of design.

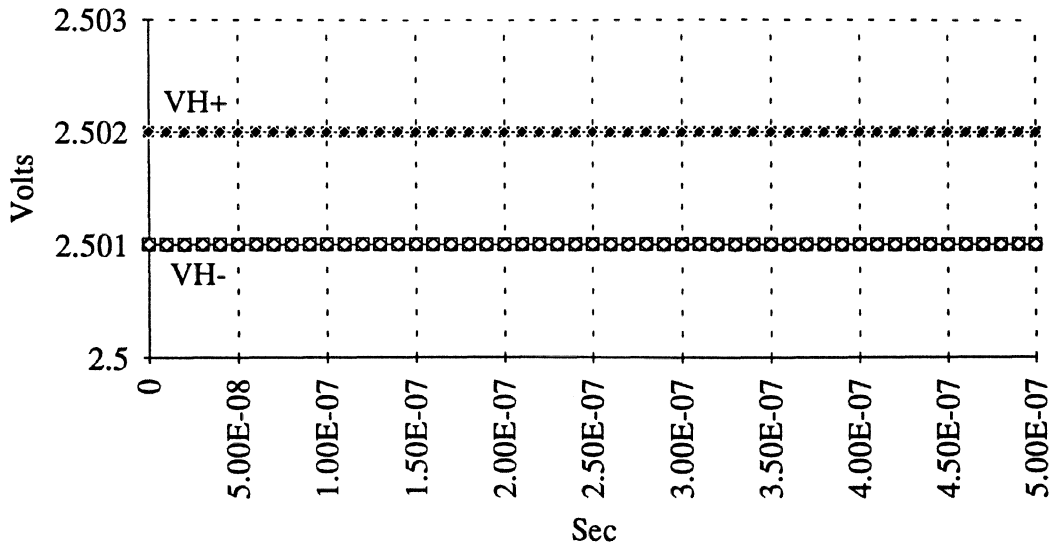


Figure 47 Input to the differential pair column amplifier (VH+ > VH-)

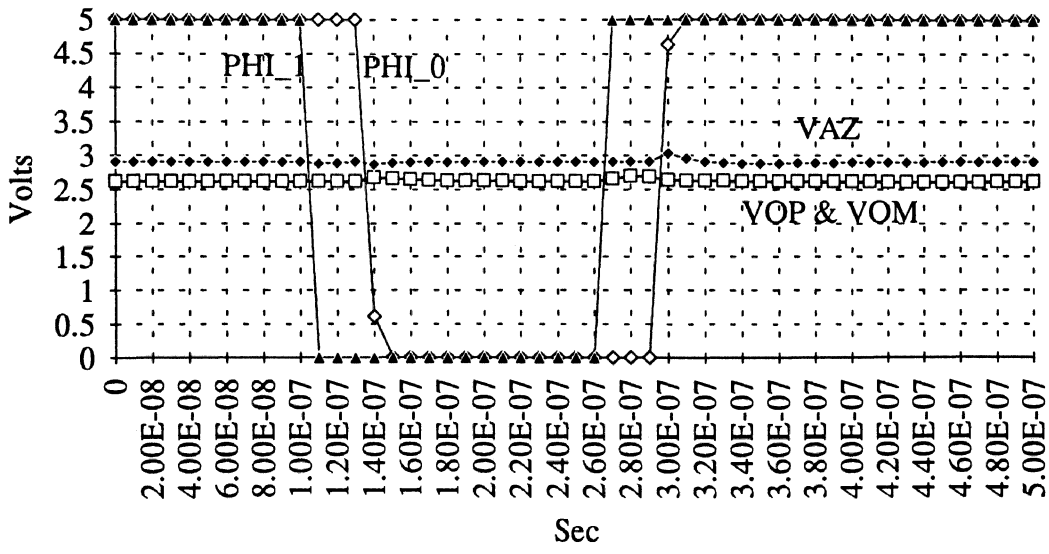


Figure 48 Output of differential pair column amplifier along with autozero voltage (VH+ > VH-)

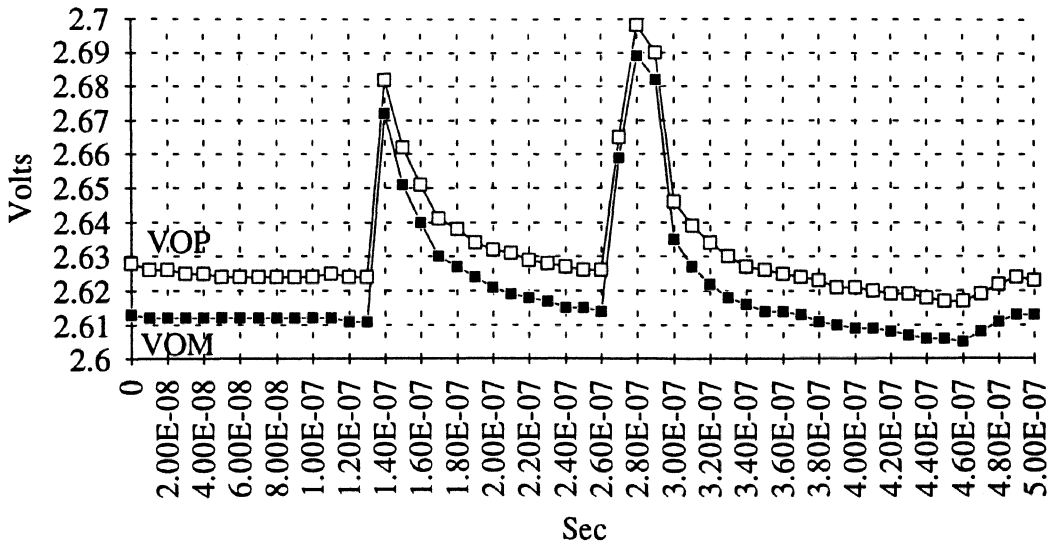


Figure 49 Zoomed output of differential pair column amplifier

(VH+ > VH-)

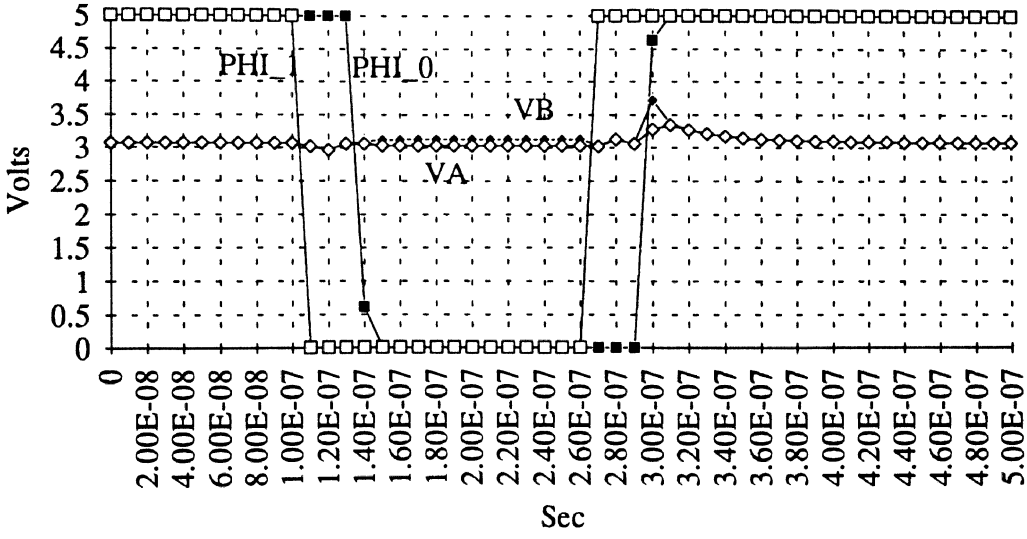


Figure 50 Output of first stage comparator along with clocks

(VH+ > VH-)

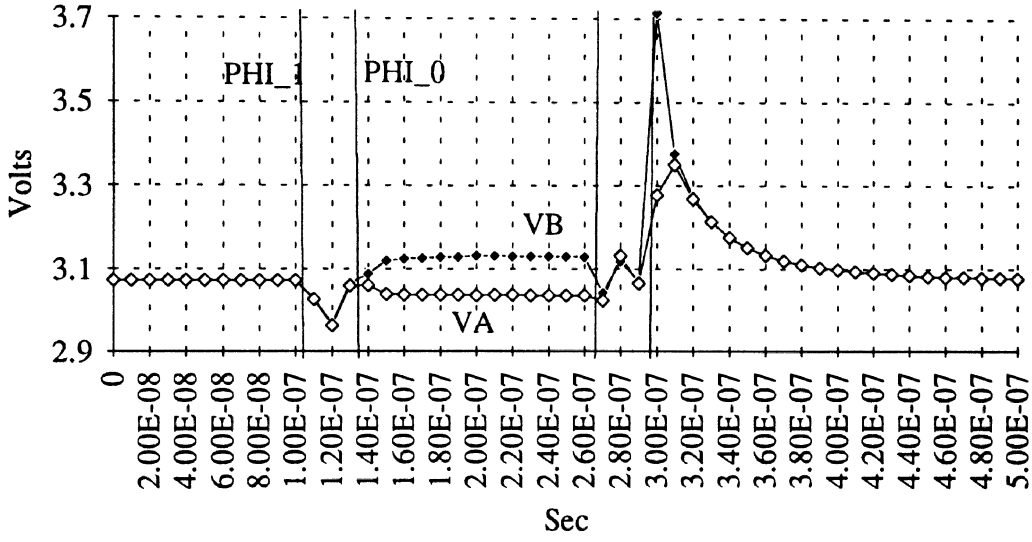


Figure 51 Zoomed output of first stage comparator (VH+ > VH-)

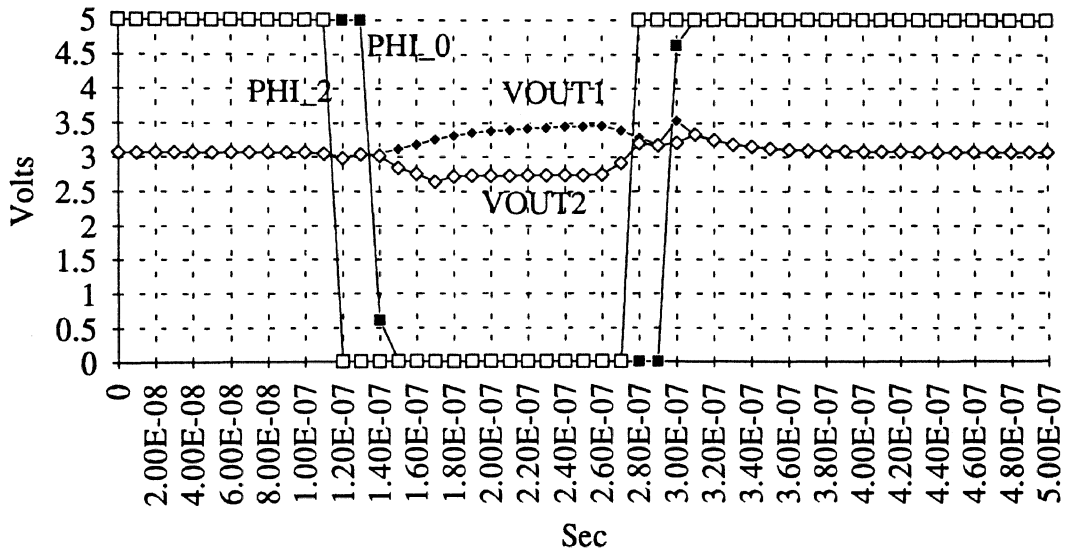


Figure 52 Output of second stage comparator along with clocks

(VH+ > VH-)

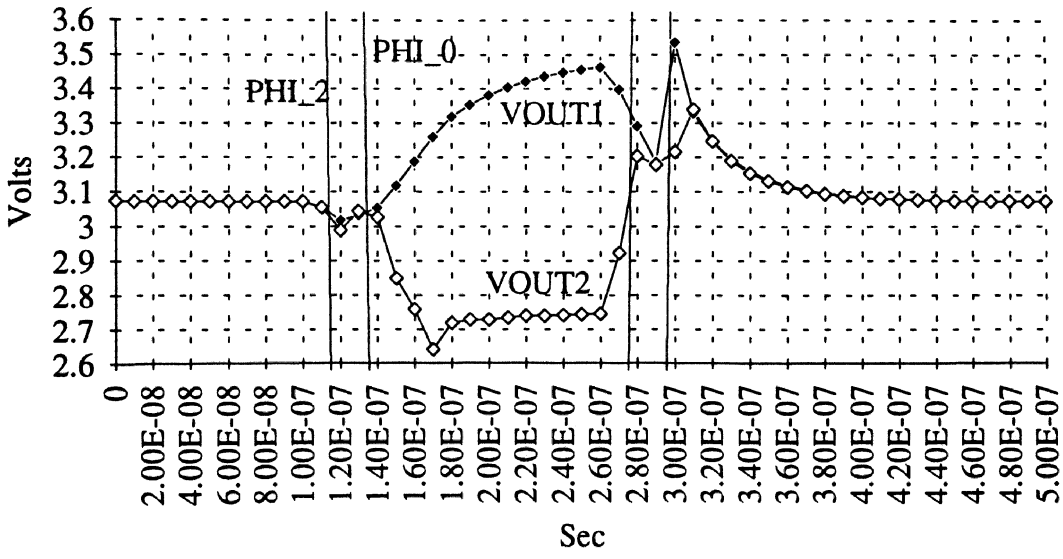


Figure 53 Zoomed output of second stage comparator (VH+ > VH-)

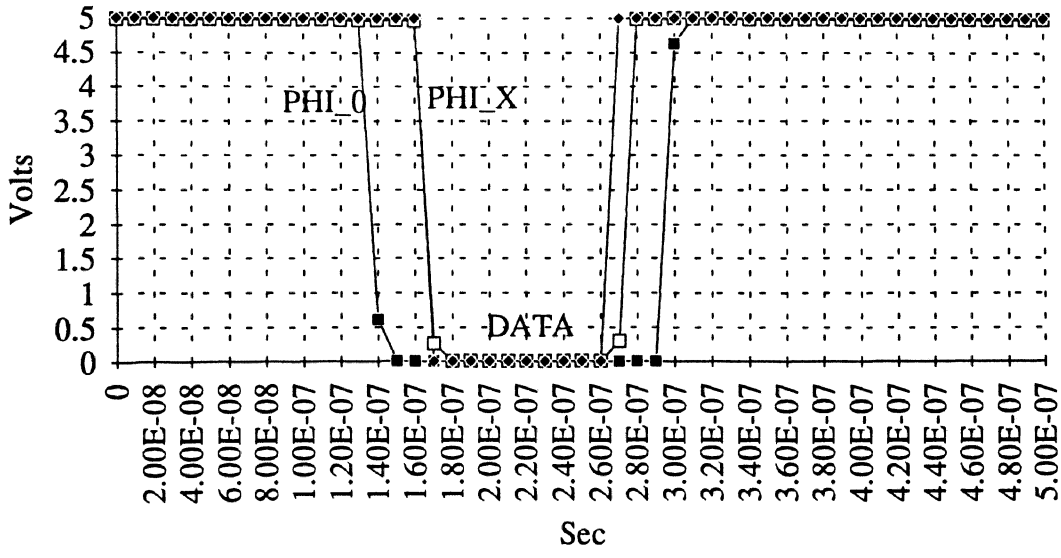


Figure 54 DATA output of Analog regenerative latch (VH+ > VH-)

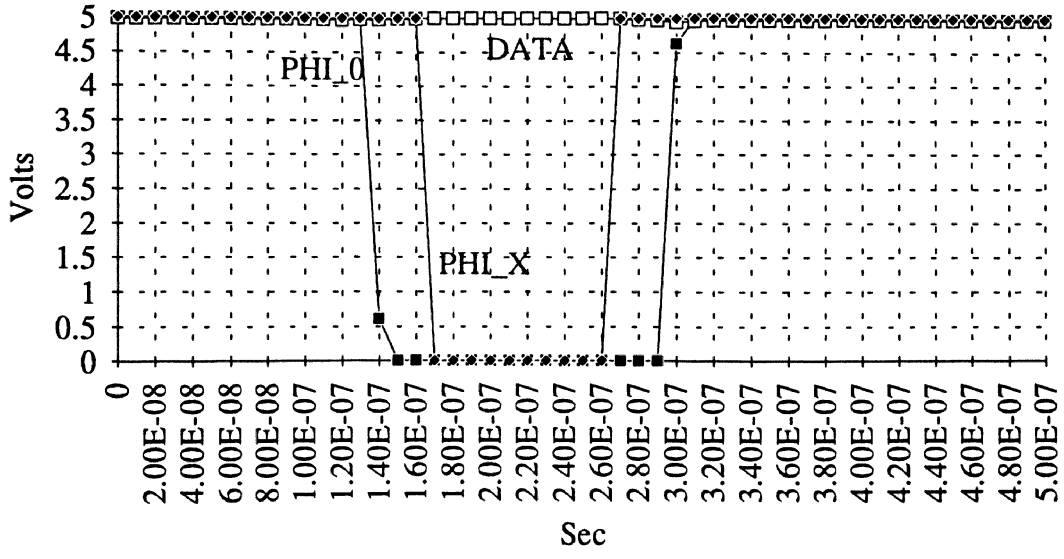


Figure 55 DATA ouput of analog regenerative latch (VH+ < VH-)

CHAPTER V

RESULTS AND CONCLUSIONS

Building blocks for 2X2 MHRAM were designed, simulated and tested. Results show that this memory is feasible given a valid hall cell. A new layout technique refered to as a comquad centroid was successful and demonstrated that offset voltages could be maintained below 0.5 mV.

The differential pair column amplifier works reliably except for its input offset voltage with a mean of 1.5 mV. This input offset voltage is due to current mismatch at the output of DDP and should be less then 0.5 mV. This current mismatch will be reduced by autozeroing the differential pair column amplifier, at the output of DDP. This will take some ingenuity but multiple approaches exist to minimize the offset voltage. Also proper layout technique (i.e. common centroid) for cascade and load transistor in column amplifier will improve the offset voltage. Also since only one layer metal was available for layout, the task was difficult but with two layers of metal now available, improvements in layout will minimize the offset. The gain of the column amplifier will also be reduced to 10. The gain was higher since we decided to include one more hall cell in parallel to the existing one to cancel the systematic offset of the hall cell. This doubled the geometry of the differential pair input of the differential pair column amplifier.

Two stage feedforward comparator works correctly along with its autozeroing. We need not autozero the comparator in modified read path for the redesign of this memory. Systematic offset of the comparator will be further reduced by common centroid layout.

The performance of the latch was found to be satisfactory. However, the sensitivity of the latch could be improved by an order of magnitude. The performance of the biasing circuits and logic circuits were found satisfactory. Logic circuits can be improved to enhance the performance as suggested.

It was found that n-devices are leaky and hence n-switches will be replaced by p-switches or improvement in the process should be made to overcome this drawback. The threshold for n-devices was lower by 0.2 V as compared to the expected value.

Simulation of the read path and write path as explained in chapter 4 shows that it is possible to write in memory as well as to sense a signal of 1 mV during the read mode. And from the test results it is found that slight modification in the differential pair column amplifier could make this memory a success. An access time of 100 nS is expected from address setup to latch output.

The final conclusion is that it is feasible to make this memory with minor modification to the column amplifier. Figure 56 shows the complete modified read path. Autozeroing of column amplifier at the point shown in figure 56 will balance the current and hence minimize the offset voltage. Once this offset is reduced the MHRAM would overcome the present drawback.

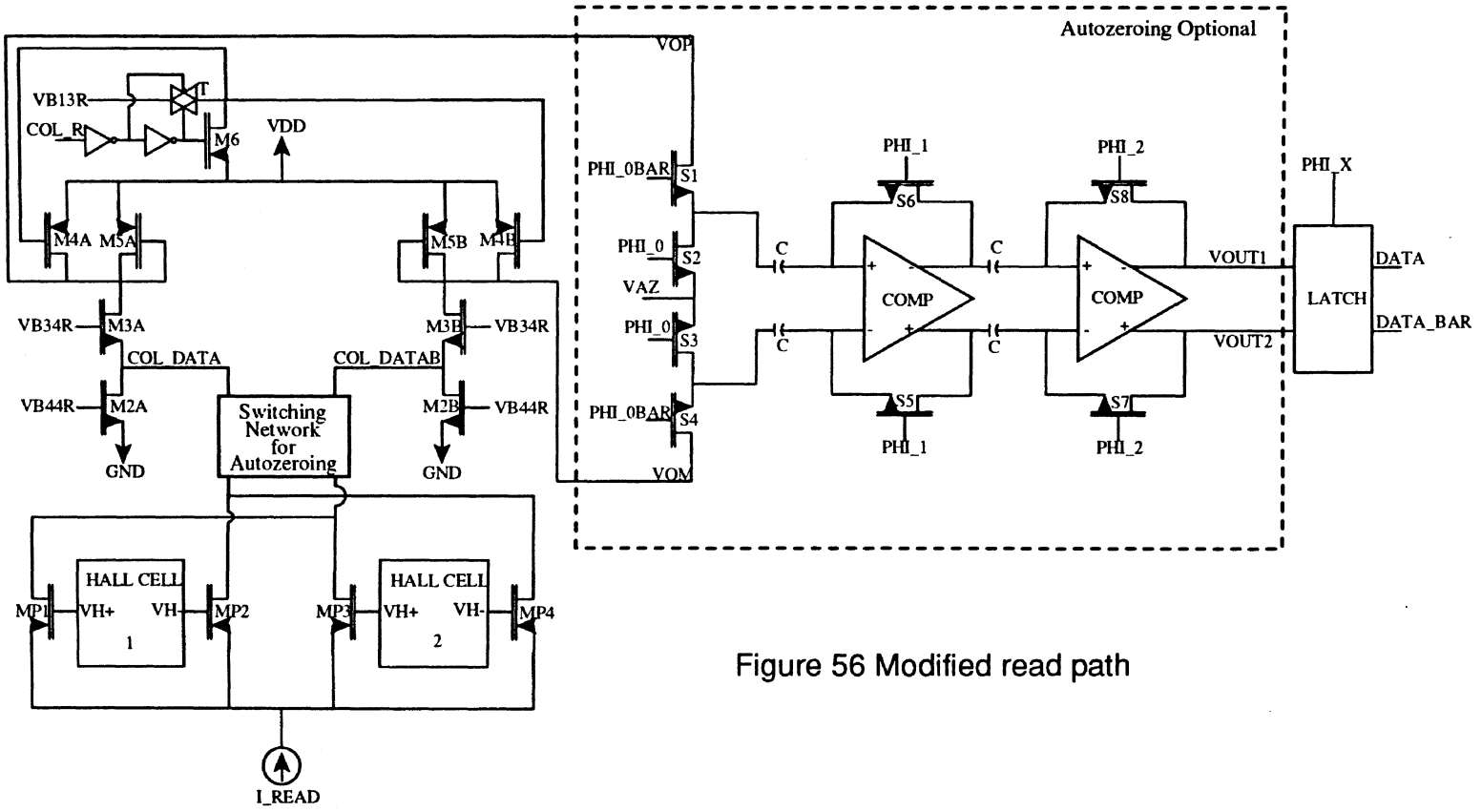


Figure 56 Modified read path

BIBLIOGRAPHY

1. Bob Peteras., "Non-Volatile Memory Technologies Hold Promise For Today and Tomorrow," Defense Electronics., pp. 82-84., October 1991.
2. Allen, P. E., and Holberg, D. R., CMOS Analog Integrated Circuit Design, HRW Inc., 1987.
3. Weste, N., and Eshraghian, k., Principles of CMOS VLSI Design, Addison-Wesley Publishing Company., 1988.
4. Gallagher, R. C. , and Corak, W. S. , "A Metal -Oxide Semiconductor (MOS) Hall Element," Solid - State Electronics, Pergamon Press, vol. 9, pp. 571-580.
5. Atsuo Yagi, and Shuichi Sato, "Magnetic and Electrical Properties of N-Channel MOS Hall Effect Device, " Japanese Journal of Applied Physics, Vol. 15, No. 4, April, 1976.
6. Daughton, J. M., "Magnetoresistive Memories - Analogies with Ferroelectrics," Ferroelectrics, vol. 116, pp. 175-194, 1991.
7. Popovic, R. S., "The Vertical Hall - Effect Device," IEEE Electron Devices Letters, Vol. EDL - 5, No. 9, September 1984.
8. Behzad Razavi, and Bruce. A. Wooley, "Design Techniques for High - Speed, High -Resolution Comparators, IEEE Journal of Solid - State Circuits, Vol. 27, No. 12, December 1992.

9. Daughton, J. M. "Magnetoresistive Memory Technology," Thin Solid Films, Vol. 216, No. 1, pp. 162 - 168, August 1992.

10. Paranjape, M., and Ristic, Lj., "Multi - Dimensional Detection of Magnetic Fields Using CMOS Integrated Sensors," IEEE Transactions on Magnetics, Vol. 27, No. 6, November 1991.

11. Sugiyama, Y., Takeuchi, Y., and Tacano, M., "Highly - Sensitive 2deg - Hall Device made of Pseudomorphic $In_{0.52}AI_{0.48}As$ / $In_{0.8}$ $Ga_{0.2}$ as Hetrostructure," International Conference on Solid - State Sensors and Actuators, 1991.

12. Nathan, A., Kung, B., and Manku, T., "Silicon Nanotesla Magnetoresistors - Temperature Coefficient of Resolution," International Conference on Solid - State Sensors and Actuators, 1991.

13. Zhang, M., and Mishra, D., "A Novel 3 - D Field Sensor in Standard CMOS Technology," International Conference on Solid - State sensors and Actuators, 1991.

14. Mccreary, J. L., and Gray, P. R., "All - MOS Charge Redistribution Analog - to - Digital Conversion Techniques - Part I," IEEE Journal of Solid - State Circuits, Vol. SC - 10, No. 6, pp. 371 - 379, December 1975.

15. Shyu, J. B., Temes, G. C., and Krummenacher, F., "Random Error Effects in Matched MOS Capacitors and Current Sources," IEEE Journal of Solid - State circuits, Vol. SC - 19, pp. 948 - 955, December 1984.

16. Gottfried, R. G., Zimmer, G., and Mokwa, W., " CMOS - Compatible Magnetic Field Sensors Fabricated in Standard and in Silicon on Insulator Technologies,"

Sensors and Actuators, A25 - A27, pp. 753-757, 1991.

17. Chovet, A., Roumenin, Ch. S., Dimopoulos, G., and Mathieu, N., " Comparison of Noise Properties of Different Magnetic - Field Semiconductor Integrated Sensors," Sensors and Actuators, A21 - A23, pp. 790 - 794, 1990.

18. Turvey, K., and Dignan, J. J., " Optimum Rectangular Geometry for Hall Effect Devices and Their Applications in Determining Properties of Electrons in Silicon," American Journal of Physics, Vol. 60, No. 7, pp. 608 - 615, July 1992.

19. Deepak, S., A Proposal for An 8 - Bit Radiation Hardened Flash A/D Converter, Masters Thesis, Oklahoma State University, Stillwater, 1992.

20. Schee, L., and Fedorak, R., " Ferroelectric Memory Real or Imaginary," 1988 Gomac Conference Digest, p. 25, 1988.

21. Tebble, R. S., and Craik, D. J., "Magnetic Materials," Wiley - Interscience, N. Y. NY p.680, 1969

22. Sze, S. M., Physics of Semiconductor Devices, Wiley - Interscience, N. Y. NY, p. 46, 1969.

23. Kittel, C., " Theory of the Stucture of Ferromagnetic Domains in Films ans Small Particles," Phys. Rev., 70, 965, 1946.

24. Tebble, R. S., and Craik, D. J., " Magnetic Materials, " Wiley - Interscience, N. Y. NY p. 375. 1969.

25. Quinn, H. F., " Advanced Memory Techniques," Digital Applications of Magnetic Devices, p. 438.

26. Schillman, E., " Technischen Rundschau," Vol. 42, p. 9, 1957.

27. Phillips, A. B., IEEE Spectrum 1, p. 83, 1964.

28. Lofgren, L., Journal of Applied Physics, Vol. 29, p. 158, 1958.

29. Sah. C. T., Institution of Radio Engineers, ED9, p.94, 1962.

30. Mengali. O. J., and Shilliday, T. S., Solid - State Electron, Vol. 7, p. 379, 1964.

31. Leistiko, O. Jr., Grove, A. S., and Sah, C. T., IEEE ED 12, p.248 1965.

32. White, M. H., and Gallegher, R. C., IEEE Vol. 53, p.314, 1965.

33. Cricchi, J. R., and White, M. H., Transistor Reasearch and Development Program. Final Report, Part II - Development of Stable Complementary MOS Field Effect Transistors NAS5 - 3758 by Westing House Aerospace Divicon for NASA Goddard Space Flight Center, November 1965.

34. Lippman, H. J., and Kuhrt, F., Z.Naturforshung Vol. 13a, p.474, 1958.

35. Becke, H., Hall, R., and White, J., Solid - State Electron, Vol. 8, p.813, 1965

36. Fowler, A. B., Fang, F., and Hochberg, IBM Research Development Vol. 8, p. 427, 1964.

VITA 2

RUCHIR P. SHAH

Candidate for the Degree of

Master of Science

Thesis: A PROPOSED ARCHITECTURE FOR A HALL EFFECT BASED NONVOLATILE MEMORY BASED ON THINFILM SOS

Major Field: Electrical Engineering.

Biographical:

Personal Data: Born in Bombay, India, On August 14, 1970, the son of Prakash and Dipika Shah.

Education: Graduated from Children's Acadamy High School, University of Bombay, India, 1985; received Bachelor of Engineering in Electronics Engineering from University of Bombay, India in July 1991. Completed the requirements for the Master of Science degree with a major in Electrical Engineering at Oklahoma State University in May 1994.

Experience: Research Assistant (Jan 1993 - Present), Department of Electrical and Computer Engineering, Oklahoma State University; worked at NRaD, San Diego, California on Master's thesis.
Reasearch Assistant (Sept 1990 - May 1991), Prompt Computers Pvt. Ltd, Bombay, India.

Professional Memberships: Tau Beta Pi, IEEE.