A PROPOSED 10-BIT 1 GHZ TWO-STEP ANALOG TO DIGITAL CONVERTER FOR IMPLEMENTATION IN TFSOI

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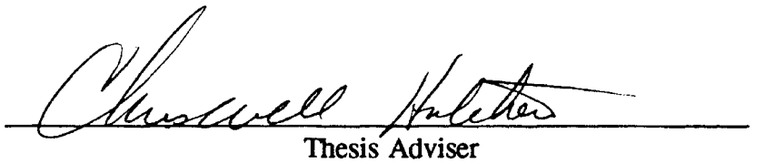

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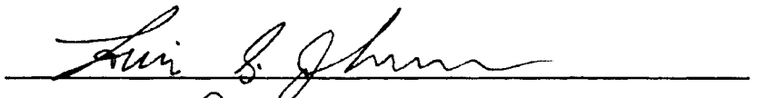

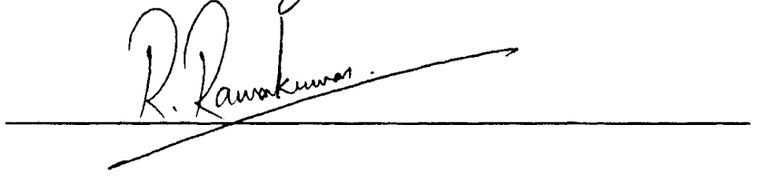

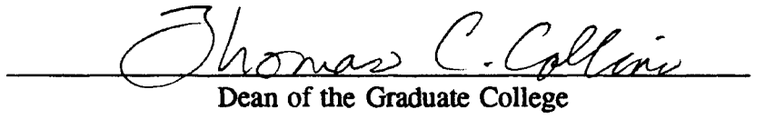

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PREFACE

This thesis reviews the state of art in 10 bit two-step Analog-to-Digital Converter (ADC) and proposed an architecture suitable for implementation in thin-film 0.25 μm Silicon on Insulator (TFSOI) process. Designed and simulated key building blocks of the proposed architecture. The building blocks were laid out using MAGIC and submitted for fabrication.

I wish to express my gratitude to the individuals who assisted me in this thesis and during the years of my coursework at Oklahoma State University. First and foremost, I must thank Dr. Chriswell Hutchens, my thesis adviser, for providing me an excellent opportunity of conducting this research. His guidance has been invaluable. I deeply appreciate his efforts, patience and support throughout the duration of this work.

Secondly, I must express extreme gratitude to the members of my graduate committee, Dr. Louis Johnson and Dr. R. Ramakumar, for serving in my committee. Their cooperation and time will always be greatly appreciated.

I would also like to thank my fellow research colleagues, graduate students and well-wishers for their manifest and continuing support throughout this process.

And to my family members who have graciously given their unconditional love, encouragement and devotion, I wish to convey my deepest sentiments of appreciation.

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NOMENCLATURE

β_x	Gain factor of MOSFET x
ΔV_T	Variation in threshold voltage
ΔV_x	Gate overdrive voltage of MOSFET x
ω_T	Unity gain frequency
C_B	Bootstrap capacitor
C_{DSx}	Drain to source capacitance of MOSFET x
C_{GDx}	Gate to drain capacitance of MOSFET x
C_{GSx}	Gate to source capacitance of MOSFET x
C_{inj}	Injector capacitor
EEPROM	Electrically erasable programmable read only memory
GBP_A	Analog gain bandwidth product
GBP_D	Digital gain bandwidth product
GBP_U	Unity gain bandwidth product
g_{DSx}	Small signal drain to source transconductance of MOSFET x
g_{mx}	Small signal channel transconductance of MOSFET x
GSPS	Giga samples/sec
I_{DSx}	Saturation current of MOSFET x
k	Boltzmann's constant
K_x	Transconductance factor of MOSFET x

LSB	Least significant bit
m	Number of bits of the coarse stage
M_x	Subscripted MOSFET
MSB	Most significant bit
n	Total number of bits
N	Number of stages
R_{SUM}	Summing resistor
TFSOI	Thin-film Silicon on Insulator
T_x	Conversion time of x
V_{DD}	Positive supply voltage
V_{DSx}	Drain to source voltage of MOSFET x
V_{FS}	Full scale voltage
V_{GSx}	Gate to source voltage of MOSFET x
V_{OH}	High output logic level
V_{OL}	Low output logic level
V_{OS}	Offset voltage
V_{PGM}	Programming voltage
V_{SS}	Negative supply voltage
V_{Tx}	Threshold voltage of MOSFET x
V_{tun}	Tunneling voltage
$(W/L)_x$	Channel width to length ratio of MOSFET x

CHAPTER I

INTRODUCTION

The demand has increased for video bandwidth converters at resolution greater than 8 bits for the application of high-speed speed measuring equipment, medical engineering systems and HDTV system [1,2]. Traditional designs of video rate analog to digital converters (ADC) have used flash architectures and bipolar technologies to obtain 8 bit resolution. For resolution above 8 bits, flash ADC suffers from severe disadvantages. Not only the large area and high power dissipation but also performance limitations due to high nonlinear input capacitance or signal distribution problems stimulated the development of multistage ADCs [1]. BICMOS technologies have also been used to build high speed multistage ADCs because they provide both high conversion rates and the required sample and hold capability [3]. The cost of these ADCs however, is increased by the more complex process technology and the power dissipation is relatively large. Thus, reducing the cost and power dissipation with the same or even better performance in CMOS technologies is an important objective. The following section reviews 10 bit two-step ADCs literature in brief.

1.1 Previous Work on 10 Bit Two-Step ADCs

A pipelined or multistep ADC employs a partial/serial approach with two or more stages

depending on the number of bits resolved per stage. Each stage consists of a flash ADC, a digital to analog converter (DAC) and a residual amplifier. The primary advantage of a pipelined architecture is its high throughput rate due to concurrent operation of the stages and proportional reduction in the area and power consumption. However, the exact interstage gain in the multistep or pipelined architecture is critical and many gain correction techniques have been developed to obtain high resolution [4,5]. To achieve high-speed conversion and to avoid interstage gain error, the number of stages will be restricted to two in two step architectures.

Earlier the 10 bit converter was bipolar and only 8 bits were attained in CMOS technology. A 10 bit CMOS two-step flash ADC was first reported by Joey Doernberg et al. [6]. This architecture consists of a Sample/Hold circuit (S/H), MSB ADC, LSB ADC, two DACs and an incrementer. The first ADC converts the MSBs. Its output is fed directly to one DAC and the output of it is used as the first voltage reference to determine LSBs. The MSBs output also goes to an incrementer and then to a second DAC whose output is the second voltage reference for the LSB ADC. Since the digital inputs to the two DACs differ by 1 LSB of the MSB ADC, the two DAC outputs will encompass the unknown input. Both of these references are a subset of the voltages used as a reference to the MSB ADC (hence this architecture is also referred to as subranging ADC). This architecture achieves the conversion rate of 5 Msample/s.

Bang-Sup Song et al. [7] proposed 10 bit recycling two-step ADC with a conversion rate of 15 MHz. The architecture uses the same capacitor array multiplying digital to analog converter as S/H amplifier, DAC and residual amplifier. As a result, the linearity of a DAC is improved. Digital error correction is used to correct the errors occurring in the coarse stage.

Behzad Razavi et al. [8] reported the design of a 12-bit 5 Msample/s two-step ADC. The converter performs a 7-bit coarse flash conversion followed by 6-bit fine flash conversion. The circuit uses interstage capacitor DAC and subtractor to achieve high-speed. The first stage

comparators are designed for high speed and only moderate resolution. One bit of overlap was used between the two stages to accommodate the errors in the coarse stage conversion. Digital error corrections were also used to achieve the overall accuracy.

There are different topologies in two-step architecture based on the way the inter stage process has been carried out.

1.2 Objective

The objective of the thesis was to carry out the literature survey of 10 bit two-step architectures and propose an architecture of conversion rate of 2.5 GHz with 10 bit resolution and ± 0.5 V full scale voltage.

In this thesis, maximum conversion rates and constraints are obtained for three different topologies and based on the relative performance, a subranging ADC with partial residual scaling has been proposed. This architecture makes use of current mode summing to generate the residual signal and to scale it by four times. A current steering DAC is used to achieve high speed when converting the digital signal of the first stage to current signal. Unlike in a conventional 10 bit architectures where they make use of analog and digital error correction to achieve the required resolution, in the present case floating-gate injector trimming (Fowler-Nordheim trimming) is used to achieve the accuracy. The 0.25 μm thin-film Silicon on Insulator (TFSOI) technology is selected as it offers the highest silicon speed performance.

All the building blocks were designed and verified using SOISPICE. Two versions of coarse comparator and fine comparator with and without floating gate injectors were submitted for fabrication. The folded cascode amplifier to be used as a building block of the buffer chain was also submitted for fabrication.

Chapter II reviews the factors which limit the accuracy of conversion and how they can be minimized. The guidelines to prevent the noisy interaction of the analog and digital sections in the ADC are reviewed. It also focuses on different types of analog memories available and the floating gate memory characteristics that make it suitable for trimming offsets of analog circuits. The different amplification techniques that can be obtained in a comparator are also reviewed. Finally the possible high speed two-step architectures are studied, and the maximum conversion rate for a given process is derived. On the basis of relative performance, subranging with partial residual scaling ADC is proposed.

Chapter III presents the design analysis and simulation results of the building blocks coarse comparator, DAC, buffer and fine comparator.

Finally Chapter IV offers the conclusions and suggest focus points for future efforts based on the results obtained.

CHAPTER II

LITERATURE REVIEW

This chapter presents, in detail, the factors limiting accuracy, theory and performance issues of analog memory followed by the comparator amplification techniques and layout considerations for mixed signal circuits. The last section presents the comparison of three high-speed ADC architectures. The maximum conversion rates are obtained for three different high-speed two-step architectures. On the basis of relative performance, a subranging ADC approach with partial residual scaling is proposed.

2.1 Factors Limiting Accuracy

This section describes the primary sources of ADC errors such as static offset voltage of comparators and amplifiers, dynamic offset error or charge injection/redistribution and noise. These errors degrade the ADC performance unless care is taken to minimize their effect during the design and layout. The critical design equations, parameters affecting these sources of errors and the guidelines to minimize the errors are presented and discussed.

2.1.1 Offset Voltage of the Comparator

All differential and current mirror pairs exhibit an input offset voltage due to the transistor mismatch i.e., variations in threshold voltage and geometry etc. This input offset voltage is referred to as static offset voltage which is given by [9]:

$$V_{OS} = \left[\pm 2\Delta V_T \pm \left(\frac{\Delta\beta}{\beta}\right)\Delta V \pm 2\Delta V_T\left(\frac{\Delta\beta}{\beta}\right)\right]\sqrt{N_p} \qquad (1)$$

where N_p is the number of transistor pairs, ΔV is the gate overdrive voltage, and V_T and β take on their standard notation. ΔV_T and $\Delta\beta$ represent the variations in threshold voltage and gain factor respectively. These mismatches are due to variations in the fabrication process. Variations in the gain factor can be minimized by using large devices and variations in threshold voltage is minimized by biasing the device at high gate to source voltage. Matching of two transistors is also affected by the orientation of two devices in the layout. Finally, with careful layout technique and device size selection, the static offset voltage can be kept to a minimum. Furthermore, to minimize the static offset voltage to the desired accuracy, either autozeroing techniques or Fowler-Nordheim trimming can be used [10].

2.1.2 Dynamic Offset Errors

Charge injection resulting from channel inversion and clock feedthrough introduces offset voltages referred to as dynamic offset errors. Due to mismatch in their dimensions, parasitic mismatch and threshold voltages, two nominally identical MOS devices carry slightly different

charges in their inversion layers. This difference results in a charge injection mismatch when the two switches turn off and a charge absorption mismatch when they turn on. This charge mismatch creates an offset voltage and is referred to as dynamic offset voltage. The redistribution of this charge is a function of terminal impedance on both ends of the switch. Hence any mismatch in terminating impedance and capacitance results in an input referred offset voltage even in a fully differential environment. Charge injection error also can result due to clock feedthrough. Since the clock signal makes very large transitions, it can couple from gate to source or drain through C_{GS} and C_{GD}. The charge injection error can be minimized by using the following guidelines [9]:

- Make the load capacitance larger than the switch area. This will significantly reduce clock feedthrough but at the expense of a reduction in settling and sampling bandwidth.
- Design for as large V_{GS} as possible. Even though large value of V_{GS} results in larger absolute clock feedthrough voltage, it becomes a small percentage of the total gate to source voltage. A large value of V_{GS} also has the added advantage of minimizing threshold voltage mismatch, but at the expense of increased power dissipation.
- Reduction in the clock voltage swing to the point where the switch just turns on and off reduces the excess clock voltage coupling.
- Make use of fully differential circuit configurations. The clock feedthrough voltage appears, to the first order, as a common mode signal and is therefore rejected. Hence circuits with a good common mode rejection ratio is highly recommended.

However, in high-performance applications, fully differential signal processing alone does not guarantee the complete elimination of charge injection error due to the mismatch in switches, switch terminal impedances and clock edges. The charge injection error or dynamic offset can be kept at its minimum by the use of fully asynchronous designs i.e., no clocking and switching.

2.1.3 Noise

The thermal noise is generated from channel resistance due to random thermal motion of carriers. The mean-square input-referred thermal noise is given by [9]:

$$Noise\ power \approx \frac{8KT\Delta f}{3g_m} \tag{2}$$

where Δf is the noise bandwidth, K is the Boltzmann's constant and T is the absolute temperature. Due to the random nature of thermal noise, it cannot be canceled by using any of the offset reduction techniques. Hence the thermal noise must be kept below 1/2 LSB. Taking the required signal to noise ratio into consideration, the constraints on g_m and C_L of a given transistor or a circuit can be determined from equation (2) as follows:

$$g_m \geq \left[\frac{8KT\Delta f}{3}\right] \frac{(2^{n+1})^2}{V_{FS}^2} \tag{3}$$

where Δf equal to the gain bandwidth product or $g_m/2\pi C_L$ and C_L is given by:

$$C_L \geq \left[\frac{4KT}{3\pi}\right] \frac{(2^{n+1})^2}{V_{FS}^2} \tag{4}$$

where $(V_{FS}/2^{n+1})^2$ represent 1/2 LSB power with n being the total number of bits and V_{FS} being

a full scale voltage of the ADC. K is the Boltzmann's constant. Note C_L must be scaled up to reflect the number of equivalent noise sources at the input.

Among the error sources presented in this section, only the static offset voltage of the comparator can be cancelled using autozero techniques or Fowler-Nordheim trimming. The worst case error that can be tolerated is ±1/2 LSB for 10 bit resolution. Since dynamic offset voltage and noise cannot be cancelled, it must be kept below 1/2 LSB of the ADC by good design technique, proper layout and trimming. Dynamic V_{OS} must be less than 0.49 mV for a 10 bit subranging ADC with V_{FS} equal to 1 V. The charge injection errors and noise can be minimized by using a fully differential architecture and large capacitances along with small switch sizes. However, the later results in an increased settling time. Since the settling time cannot be sacrificed due to ω_T limitations of the process, the residual signals (the difference of input signal and reconverted analog signal of the first stage of ADC) have been partially scaled to reduce the dynamic offset constraints and Fowler-Nordheim trimming is selected as a method to eliminate the static offset errors. This in turn eliminates the switches and capacitors used for autozeroing which contribute to the dynamic offset errors associated with the fine comparators (FC). Due to this, we recommend a fully asynchronous design which employs Fowler-Nordheim trimming to eliminate the static offset voltage.

2.2 Analog Memory

A non-volatile semiconductor device originally developed for digital memory is exploited as a non-volatile analog memory device. In particular, an analog electrical erasable programmable ROM (EEPROM) is proposed to be used to trim the offset in the opamp, comparator, current DAC and to set the trip point of the coarse ADC comparators. Offsets are generally in the range

of -10 mV to +10 mV when good design and layout practice is followed and no offset reduction techniques are utilized. With trimming, offsets can be reduced in the range of -100 μV to +100 μV, an improvement of two orders of magnitude [11].

This section reviews the different types of analog memories, in particular floating-gate memory, Fowler-Nordheim tunneling mechanism and finally the characteristics suitable for trimming the offset voltage.

The EEPROM devices are classified as:

- A charge trapping device
- A floating-gate device

2.2.1 A Charge-Trapping Device

This device stores the charge in the "traps" at the interface of the multi-layer insulator gate structure and/or in the insulator bulk. Different charge trapping device structures have been proposed. They are: (1) MNOS (metal nitride oxide silicon), (2) MAOS (metal alumina silicon dioxide semiconductor) and (3) MAS (metal alumina semiconductor) and so on. Among these, the MNOS device is the most attractive as an analog memory and is utilized in some analog applications [12].

A typical n-channel MNOS FET structure is as shown in the Figure 1. The thin (50 Å) silicon dioxide layer allows charge to tunnel through, by the Fowler-Nordheim tunneling mechanism (discussed later in this section), when a voltage in the range of +25 V to +35 V range is applied to the gate [13]. This charge is then trapped in the silicon/dioxide silicon nitride interface. It remains trapped there since both the materials are high quality insulators. As a result, threshold voltage V_T increases. On the other hand, in order to lower V_T, electrons are driven

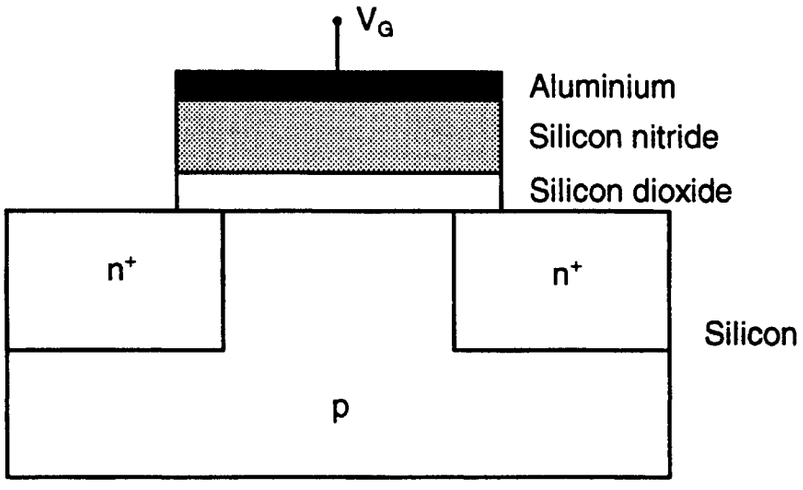

Figure 1. A typical n-channel MNOS structure.

out from the nitride to the substrate by applying a negative high voltage at the gate. The threshold voltage shift ΔV_T is proportional to the change of the stored charge near the oxide-nitride interface ΔQ_{in} and is given by [14]:

$$\Delta V_T = - \frac{t_{nd} \Delta Q_\epsilon}{K_{nd} \epsilon} \tag{5}$$

where t_{nd} and $k_{nd}\varepsilon$ are the thickness and dielectric constant of Si_3N_4, respectively. Consequently, the transconductance of the device will be altered and the memory value can be determined by measuring the drain current.

The MNOS technology has the disadvantage of requiring the silicon nitride material in addition to the standard MOS materials.

2.2.2 Floating-Gate Device

Unlike charge-trapping devices, the floating-gate device has the charge stored in a conducting or semiconducting floating layer sandwiched between insulators. Three different types of floating-gate devices have been proposed:

- Avalanche injection floating-gate device
- Thin-tunneling-oxide floating-gate device
- Thick-oxide floating-gate device

The first type is distinguished from the other two types by the charge injection mechanism to the floating-gate.

2.2.2.1 Avalanche Injection Floating-Gate Device

One-well known example of this type is FAMOS (floating-gate avalanche-injection MOS). A typical structure of FAMOS is as shown in Figure 2 [12]. FAMOS utilizes charge transport to the floating-gate by avalanche injection of electrons from the p-n junction. For p-channel FAMOS, a reverse p-n junction voltage in excess of -30 V will cause the onset of the injection of high energy electrons from the p-n junction avalanche region to the floating gate. As a result, the electrons will be accumulated on the floating gate. The amount of injected charge is a function of amplitude and duration of the junction voltage. Because of the relatively thick-oxide layers, this device can retain the stored charge for an extremely long time. However, it is difficult to discharge or erase the stored charge on the floating gate. Furthermore, the injecting process is insufficient because only a small fraction of the avalanche current is injected into the floating gate. Moreover FAMOS is a two terminal device, and hence has limited use in circuit design.

2.2.2.2 Thin-Tunneling-Oxide Floating-Gate Device

To overcome the above problems, thin-tunneling-oxide floating-gate structures were proposed. Most of these devices utilize relatively thin-oxide, but not as thin as that in the MNOS device, to charge and discharge the floating gate through the tunneling mechanism. As an example, FLOTOX (Floating-gate tunnel oxide) device structure is as shown in Figure 3. In order to shift V_T higher, a positive voltage pulse is applied to the top gate, while the source, drain and substrate are grounded. As a result, electrons tunnel from the drain to the floating gate through the thin oxide and charge the floating gate negatively. A positive high voltage pulse at the drain will remove the electrons from the floating gate while the source is floating and both the top gate

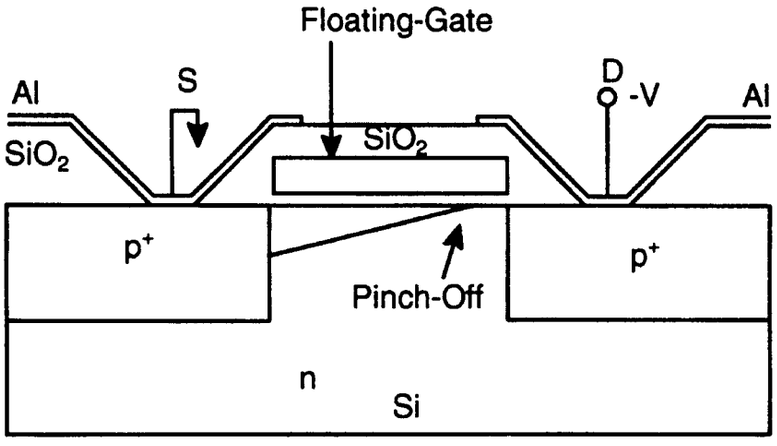

Figure 2. A typical p-channel FAMOS structure.

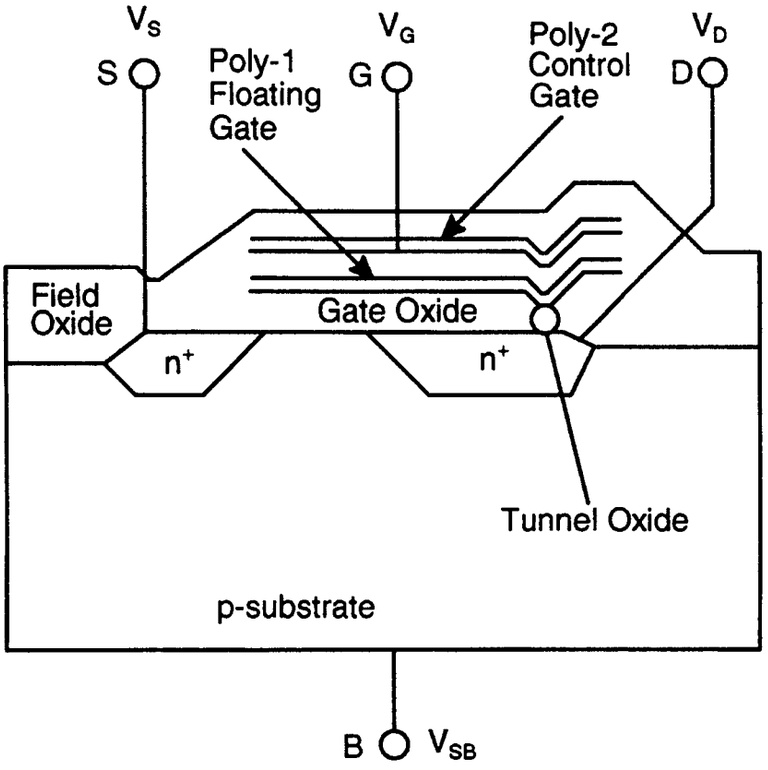

Figure 3. The FLOTOX device structure.

and the substrate are grounded. Tunneling is achieved directly from the drain without the conductive channel formation on the substrate. Consequently, V_T is lowered. The threshold voltage shift is given by [15]:

$$\Delta V_T = - \frac{\Delta Q}{C_{pp}} \tag{6}$$

where ΔQ is the change of the stored charge on the floating gate and C_{pp} is the capacitance between the control gate and the floating gate. The amount of stored charge in the floating gate can be sensed by the drain current.

2.2.2.3 Thick-Oxide Floating-Gate Device

To fabricate the above mentioned thin-oxide floating gate devices, special fabrication techniques like ultra-thin tunneling oxides are required. Furthermore, the very thin tunneling area degrades the retention characteristics. To overcome these drawbacks, the floating gate devices fabricated in standard CMOS process with thick-oxide have been proposed by using a geometric trick to enhance the field strength at SiO_2 interface. It is also desirable to avoid the use of the drain of the transistor for programming of the floating gate. An example of this type, a charge injector structure as proposed by Carley [10], is shown in Figure 4. A test device was fabricated in 2 μm p-well CMOS process with a gate-oxide thickness of 400 Å. Since the polysilicon rectangle ends in the middle of an n^+ diffusion, the electric field at the corners of the poly rectangle is increased by an enhancement factor of 2 to 4.

Several different types of floating gate devices with thick-oxide are available in the

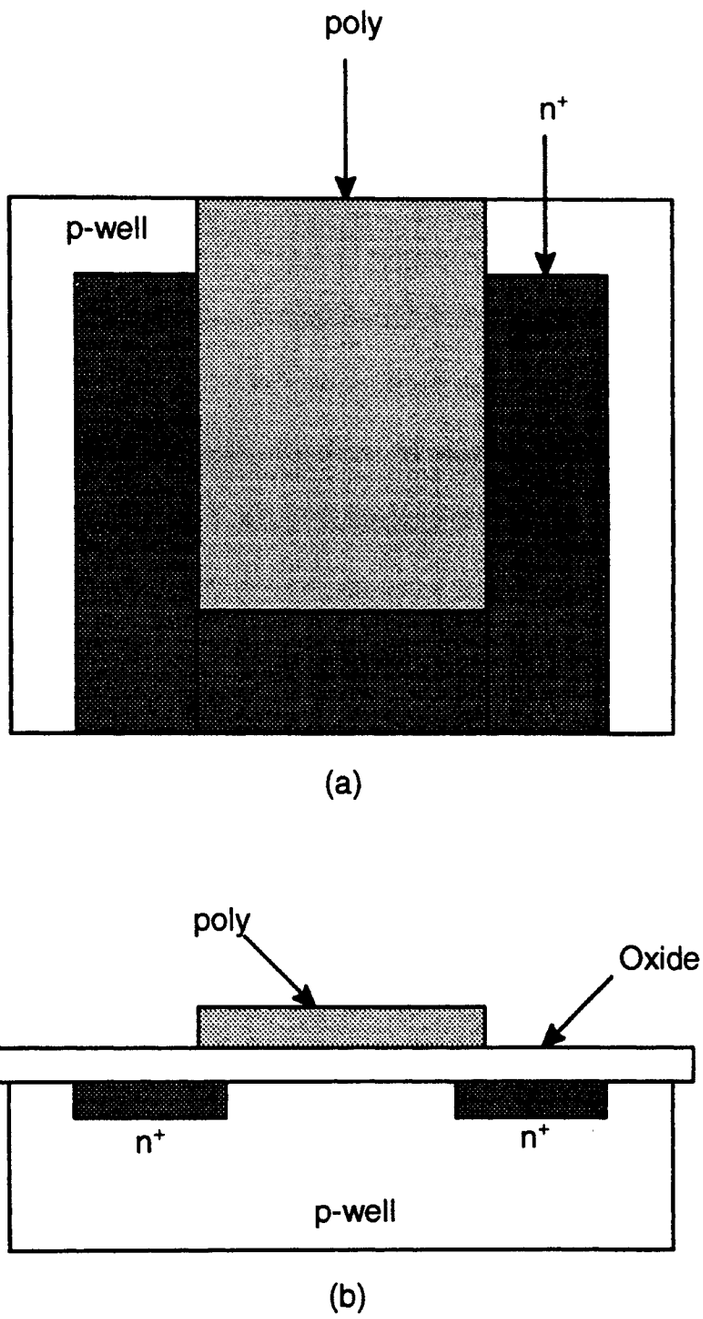

Figure 4. A charge-injector strucrure floating-gate device.
(a) Top view
(b) Cross section

literature. Depending on the process and the application, several suitable type devices have been proposed.

2.2.3 Fowler-Nordheim Tunneling Mechanism

The Fowler-Nordheim tunneling mechanism can be explained as follows [10]; there exists an energy barrier of approximately 3.2 eV that prevents electrons in the silicon or polysilicon from entering SiO_2. At room temperature, the electrons can only tunnel through an oxide barrier of 50 Å thickness. If the potential within a 50 Å range of Si/SiO_2 interface is below 3.2 eV, the electrons that tunnel into the SiO_2 will always return to the Si and no current will flow. However, if the electric field in the SiO_2 is strong enough (6.4×10^8 V/m), then the few electrons that tunnel into the SiO_2 will be carried away by the electric field and there will a small current away from the Si surface. Increasing the electric field increases the electron flow and thus the electron current. It takes a gate to diffusion voltage of approximately 25 V to remove electrons from the gate given an oxide thickness of 400 Å. This voltage should be well below the gate oxide breakdown voltage for the given process.

2.2.4 Characteristics of the Floating-Gate Memory

When the floating gate devices are used for digital memory, they are optimized for small area, high writing speed and low failure rate. In applications like circuit trimming, other requirements like accurate control of the floating gate charge and good charge retention properties are important. Typically this requires moderate size injectors to maintain matching accuracy and high storage capacitor to injector ratio.

There are several important properties of the memory device which must be considered during the design of an analog trim memory circuit. In the following section aging characteristics, short term drift characteristics, endurance characteristics, resolution and speed are considered.

Aging characteristics

The charge retention of an analog memory circuit depends on the thickness of the gate oxide. Thicker the gate oxide, better the retention characteristics. Although a thin oxide (< 200 Å) floating gate device needs a thin-tunnel oxide in order to achieve the electrically erasable property similar to the MNOS device, this tunnel oxide need not be as thin as in MNOS device (< 50 Å). Therefore, charge will be retained longer in a floating gate device than MNOS device. The textured-poly floating gate devices have even thicker oxides so that they have better retention characteristics [12]. The floating gate devices with standard (thick) gate oxide (400 Å) charge loss would be less than 0.1% in 10 years at operating temperature 100 °C [10]. Therefore precise analog trim voltages may be stored for the lifetime of the many products. Preliminary work by researchers at Oklahoma State University have confirmed the suggested retention rates, composed of a dielectric absorption component and thermal component.

Short term drift characteristics

The time degradation of the retention of the floating gate device is an exponential function of the time. For the thin oxide floating gate device, an initial drift lasting several hours was observed by Sackinger et al [16]. Furthermore, Carley [10] reported that after inducing a voltage change at the floating gate, the gate tends to move back towards its original voltage over a period

of several minutes. The short term drift is believed to be due to traps sites with long time constants near SiO_2 interface settling to a new equilibrium. The rate of change of this short term drift can be greatly reduced by slowing down the trimming process. These short term drifts have been observed to be in the order of 0.04% per day at 130 ℃ [10].

Endurance characteristics

The decrease in the charging and discharging current with repeated cycling which occurs in EEPROMs does not present problem for the analog applications for the following two reasons:

- The trimming voltage is typically set to one value and subsequent trimming operations if any cause small changes in that value.
- By applying a small charging or discharging current for a longer time, the same voltage can be generated at the floating gate with less stress on the oxide.

In many trimming applications, the duration of the trimming procedure is not a major set back as only a few trims have to be performed and in many cases, quite often they can all be performed in parallel.

Resolution

The resolution is theoretically very high because the minimum injection charge could be a single electron. However, it is difficult to control the amount of charge injected during trimming, because it depends on temperature, charge concentration condition and the individual devices. The smallest changes will be limited by the ability of external circuit to detect the change. For example, 250 million electrons injected to the floating gate will cause a 2 V change

in V_T [17]. To date, the best resolution is approximately 8-10 bits [12].

Speed

In order to control the memory value precisely, either low voltage or short duration pulses should be used. The low amplitude pulse needs a long pulse duration, while many short duration pulses should be applied to achieve a wide dynamic alteration of the memorized value. The program speed for most analog application will not be a problem since as stated earlier in trimming applications there are only few trims to be performed and in many cases, they can all be performed in parallel.

From the above discussion, it is clear that, theoretically it is possible to accurately control the injection or removal of electrons using good design circuit. Although a lot remain to be understood regarding Fowler-Nordheim injection be they become procedural analog solutions. As analog memory circuits can be programmed bidirectionally due to temperature and age variations, the circuit can be recalibrated to maintain the desired accuracy. However trim rates are often quite slow (somewhat related to accuracy), typically 1-10 mV/sec change in floating gate voltage. In both opamps and comparators, as they are inherently amplifiers, it is easy to generate the decision logic as to which direction to drive the floating gate during the trimming process. Hence we intend to use Fowler-Nordheim trimming to trim the offset voltage of the fine comparators, amplifiers, to trim the current sources of DAC and to vary the trip points of the coarse comparators. This eliminates the settling time associated with autozeroing process (see equation (12)). All proposed trimming will maintain the opamp in the feedback loop and require direct comparison to a reference. The opamp in the feedback loop will either be part of the system circuitry or temporary switched in for the trim process.

2.3 Comparator Amplification Techniques

The basic function of a comparator is to provide amplification sufficient to ensure that digital output levels can be generated in response to small differences in input signal levels. This amplification need not be linear, nor continuous in time, consequently it can be realized using non-linear gain stages and the total amplification can be distributed along a cascade of pipelined stages [5].

The following are three general approaches to obtain the amplification in a comparator:

- Single stage amplifier (SPA)
- Multistage amplifier (MA)
- Regenerative amplifier (RA)

Figure 5 shows small signal models representation of each of these approaches. In the figure g_m represents the transconductance of the amplifier stage and C_L represents the capacitance of the corresponding output node.

2.3.1 Single Stage Amplifier (SPA)

It is assumed that a step waveform is applied at the input because linear amplification is not required in comparison applications, the output need not settle close to steady state value at the time the comparison takes place. Thus the amplification A for this circuit is defined as the ratio of output V_O to the input step amplitude V_i after an amplification time T_a if the MOSFET output conductances are neglected. The relationship between T_a and A is given by:

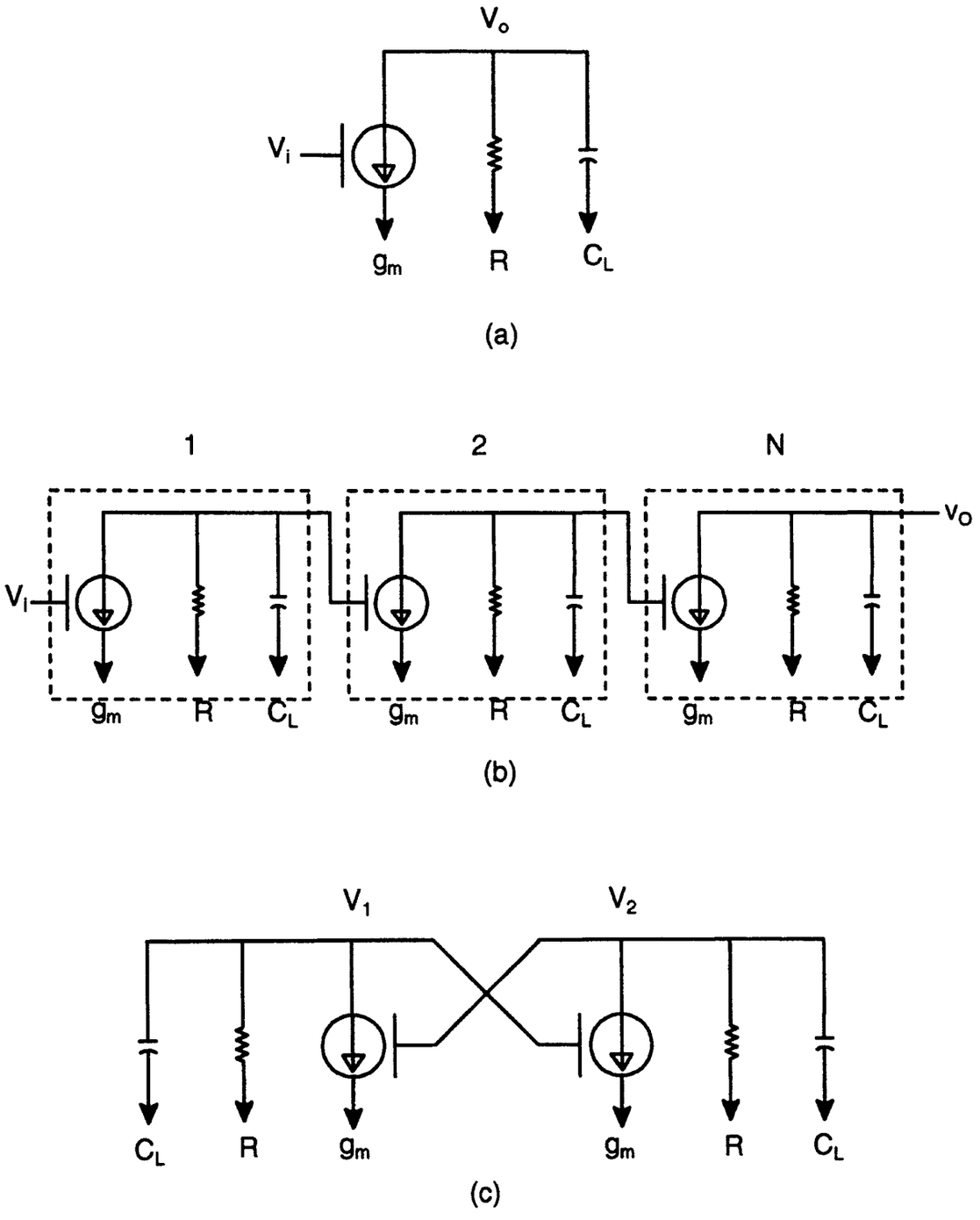

Figure 5. General approaches to obtain amplification in comparators.

(a) Single-stage amplifier (SA).

(b) Multistage amplifier (MA).

(c) Regenerative amplifier (RA).

$$T_a = \frac{C_L}{g_m} \times A \tag{7}$$

Gain A is the small signal gain and depends on process parameters and circuit geometries and equals $g_m R_O$.

2.3.2 Multistage Amplifier (MA)

It consists of cascade of a identical SPAs. The relationship between total gain A and T_a is given by:

$$T_a = \frac{C_L}{g_m} \times (A \times M)^{\frac{1}{N}} \tag{8}$$

For MA, there exists an optimum number of stages N_{op}, for which T_a is minimized. The relationship between N_{op} and ln A is nearly linear and is given by [18]:

$$N_{op} \approx 1.1 \times \ln(A) + 0.79 \tag{9}$$

for A < 1000.

2.3.3 Regenerative Amplifier (RA)

Regenerative amplifier can also be used as a nonlinear gain stage. The equivalent

amplification A of such a stage is defined as the ratio of the differential output $V_1(t) - V_2(t)$, to the initial unbalance, $V_1(0) - V_2(0)$, after a regeneration time period of T_a. Again neglecting the MOSFET output conductance, the amplification time T_a is related to A by:

$$T_a = \frac{C_L}{g_m} \times \ln A \tag{10}$$

In a SA and MA configurations, amplifier gain is limited by the low frequency gain of a stage, whereas gain in an RA in theory is limited only by dc bias conditions and the supply voltage. Thus by observing the equations (7), (8) and (10) it is obvious that area efficient amplification can be best obtained by regeneration. Furthermore, from the above equations, it is seen that in an RA, the amplification is proportional to natural log of gain and hence the amplification time required to generate digital levels is small. Based on these results, regenerative approach is used in the second stage where it has to resolve small voltages in the range of 2 mV. The multistage approach is used in the first level of ADC to conserve power and due to the relatively large voltages. As the input signal to the first stage is quite large, the settling time will become competitive with regenerative approach.

2.4 Layout Considerations For Mixed Signal Circuits

Due to continued scaling of VLSI technology, high speed digital circuits and high performance analog circuits can be integrated on the same chip. As a result of the demands for higher clock rates and greater analog precision, switching noise has become a serious concern in the design of high-speed ADCs. In such mixed-signal systems, fast switching transients produced

in the digital circuits will couple into sensitive analog components, limiting the analog precision.

The main sources of the noisy interaction of analog and digital circuits are [9]:

- Capacitive coupling (direct and through the substrate).
- Noise injection through the power supply lines.

Lateral coupling occurs, when two metal lines run parallel for a given path. This type of coupling occurs when an analog and a digital signal run in a close proximity. The usual way of reducing the problem is to place the lines carrying analog signals reasonably far away from the lines carrying digital signals. Moreover, ground-signal-ground (GSG) arrangement achieves lateral shielding. Separate ground lines for analog and digital circuit must be used and should be merged off chip. With this arrangement, any switching noise generated in the signal line will be terminated on the ground line. But in some topologies, GSG shielding is not possible due to unavoidable crossings built into them. In such a case, when two signals have to cross but cannot couple capacitively, a shield layer biased to ground can be used.

The noise in the substrate is produced by two mechanisms, the capacitive coupling of digital nodes with the substrate and the impact ionization effect responsible for substrate current. A straightforward method to overcome capacitive coupling is to reduce the parasitic capacitance at the drain node of digital circuit. This can be achieved by keeping the drain contact as small as possible, then as the area of the drain to substrate node is small, the coupling with the substrate is reduced.

In case of bulk devices, if analog and digital circuits are separated by four times the effective thickness of the epitaxial layer, cross talk between digital circuit blocks and sensitive analog circuits occur primarily because of bulk, but further increase in the physical separation will not reduce substrate cross talk. In an n-well process, p^+ guard rings can partially shield sensitive analog circuits from noise in the bulk if the rings are placed very close to the analog circuits. The

current induced in the substrate by the digital signals will then be collected by the guard ring and will not enter the analog portion of the die. Reducing the inductance in the substrate bias was found to be the most effective way of minimizing the substrate noise [19]. Due to the lack of a conducting substrate in TFSOI, the guard ring must be replaced by ground ring around the analog circuit.

Another important source of noise is disturbances in the analog sections through the power supply lines. The lines that bring power to analog cell can also couple signals from other portions of the chip onto signal nodes within the cell. The most significant source of coupling signals is from the digital circuits, which tend to generate current spikes at switching times, onto sensitive analog signal nodes. A standard approach to avoid coupling between digital and analog circuit is to have separate analog and digital power supplies, which are merged off chip.

The parasitic inductance due to the power supply connection between pad and frame also cause spikes to occur, especially when output drivers have to control large capacitive loads. These spikes can be reduced by limiting the value of inductance (parallelizing bonding wires) and/or the time derivative of digital current. This typically means placing several band wires in parallel and the pads close to the frame.

It is especially important to follow the above discussed rules particularly, in case of an ADC, consisting of analog circuits (amplifiers and comparators) and digital circuits (DAC and encoders).

2.5 Comparison of High-Speed Architectures

Conceptually the multistage ADC has two or more stages where each stage does a coarse analog to digital conversion using comparators, referred in this thesis as the coarse comparators

(CC), followed by a finer grained comparison (the second step). The digital output of the coarse comparator is immediately reconverted into an analog signal using a DAC. The analog output of the first stage is subtracted from the held input signal, and finally the (optionally amplified) residual difference voltage is applied to a second stage ADC composed of fine comparators (FC). The performance requirement of the fine grained comparators is always more stringent.

Following are the three proposed two-stage ADC architectures, presented as possible 10 bit 2.5 GHz solutions:

- Subranging
- Two-Step with Residual Scaling
- Subranging with Partial Residual Scaling

Subranging

The subranging architecture is as shown in Figure 6. Conversion is done in two stages. In the first stage, the 'm' most significant bits (MSB) are determined using 2^m-1 coarse comparators. The output of the first stage determines the range in which the second or residual processing stage input lies. The digital output of the first ADC stage is converted into an analog signal using a DAC and it's subtraction from the input signal results in the residual signal. The residual signal is then compared using the range of reference voltages set, selected, or computed by the first stage DAC depending on the implementation approach. The second set of comparators referred to as the fine comparator resolves the remaining 2^{n-m} least significant bits. Static and dynamic offset voltage (as a result of device mismatching), charge injection error and noise are critical to the fine comparator stage operation as it must resolve finer granule input signals. Offset voltage can be minimized using autozeroing techniques (AZ) and floating gate injector trimming

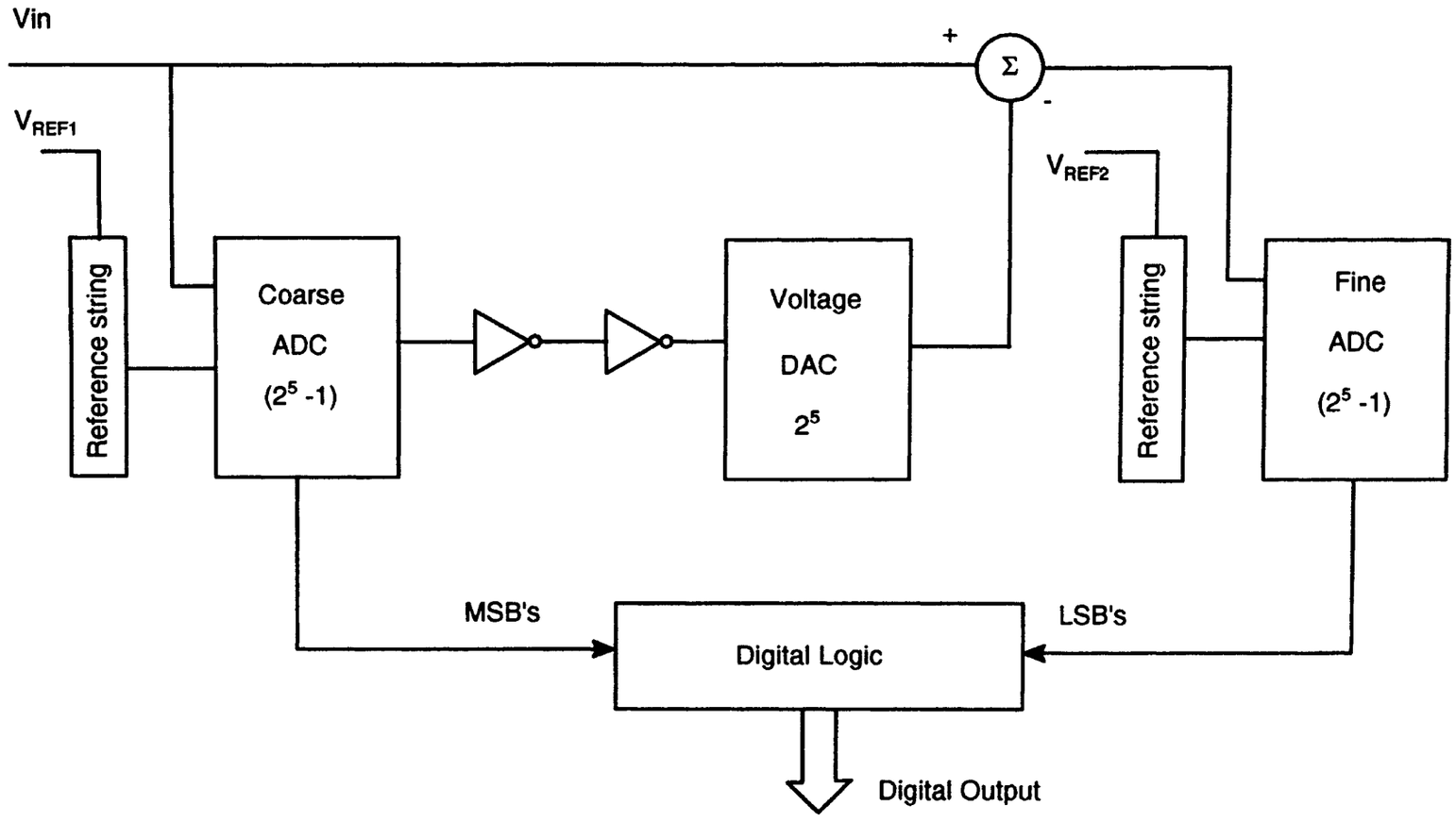

Figure 6. 10 bit Subranging A/D converter block diagram.

(Fowler-Nordheim trimming). The limitation of this architecture lies with the difficulty of designing fine comparators whose noise floor, charge injection/redistribution, and static errors are maintained below 1/2 LSB. This limitation can be mitigated by the use of a residual amplifier at the cost of an increased settling time associated with the linear amplifier as in the following two step architecture.

Two-Step with Residual Scaling

A two step residual scaling architecture is shown in Figure 7. Again conversion takes place in two steps. In the first step, the MSBs are resolved using 2^m-1 coarse comparators. The digital signal is then converted into an analog signal for use in calculating the residual signal. The residual signal is obtained by subtracting the reconstructed analog signal from the input signal and amplifying it 2^m times. The same set of reference string and comparators can optionally be used in the second step to resolve the LSBs. This eliminates matching requirements between stages but not without a resultant loss in settling speed and an increase in complexity. As the input signal can be quite large for both stages, comparators need not be autozeroed or trimmed. However the larger settling time associated with the residual scaling amplifier makes this method less attractive.

Subranging with Partial Scaling

A proposed two step subranging ADC architecture with partial residual scaling is shown in Figure 8. The first stage uses 2^m-1 comparators to implement the coarse ADC generating the MSBs and passes this result onto a switched current DAC. The DAC generates a negative current

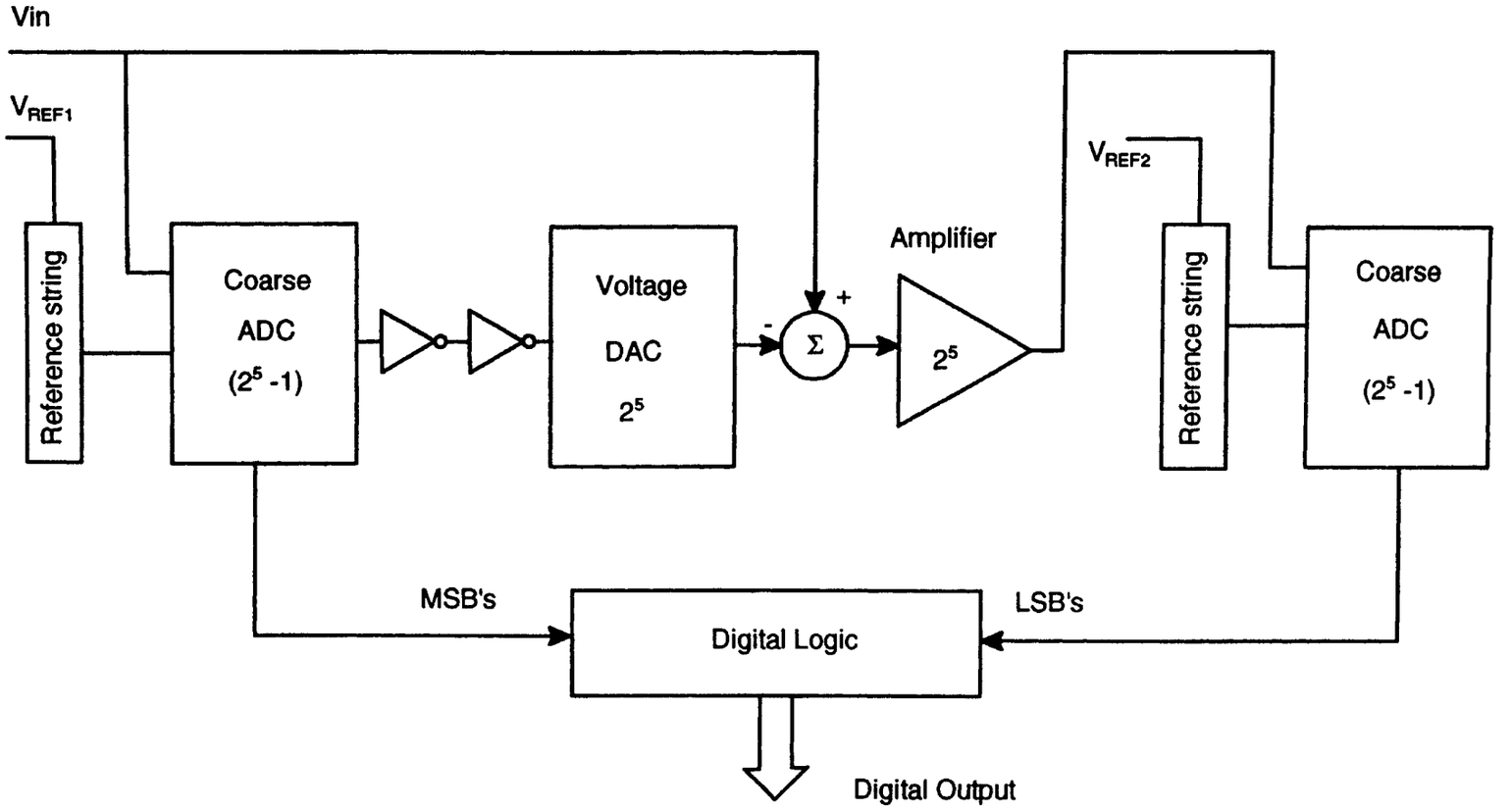

Figure 7. 10 bit Residual scaling A/D converter block diagram.

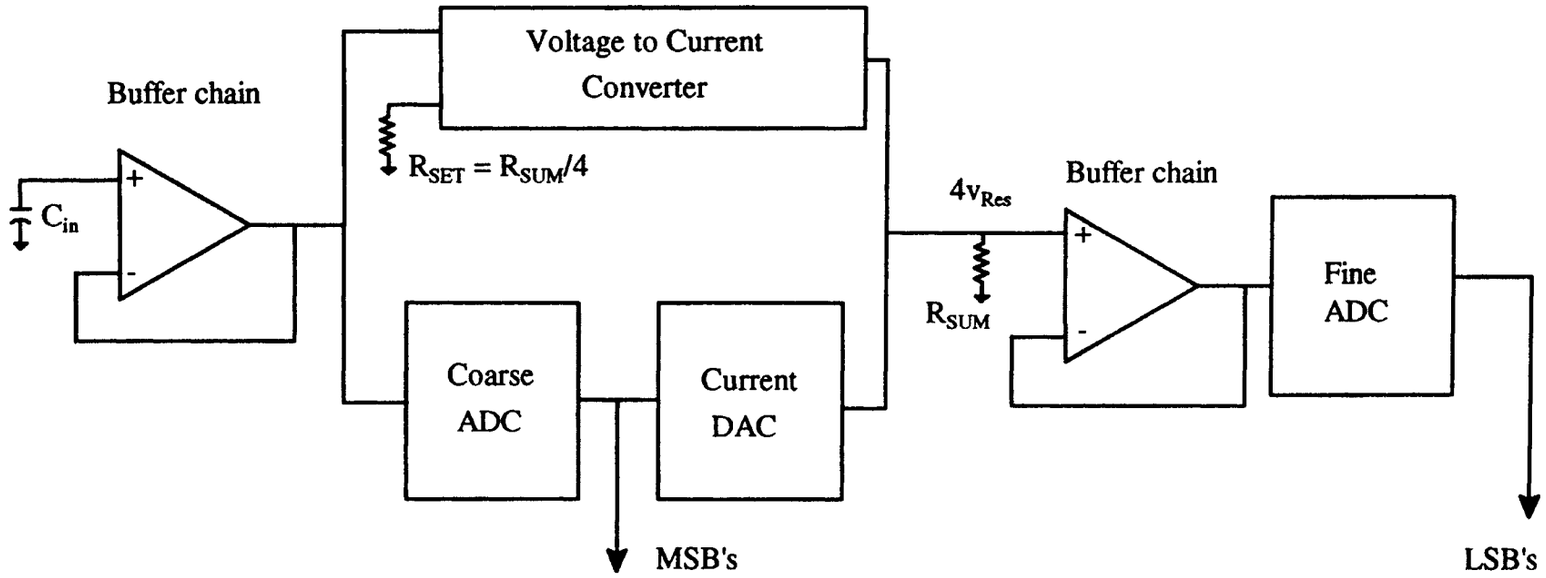

Figure 8. 10 bit Subranging with partial residual scaling A/D converter block diagram.

representation of the coarse signal estimate using the MSBs from the coarse ADC. Current mode summing is then applied to obtain the residual signal, this approach potentially reduces the conversion speed by reducing the parasitic capacitances and provides a potential means to control the time constant when selecting the summing node resistor R_{SUM}. Voltage to current conversion of the input is required to convert the input voltage signal to its current equivalent before summing across R_{SUM} in developing the residual voltage signal. This residual signal is scaled (in this case up by a factor of four times) to ease the accuracy and noise requirements of the fine comparators and then buffered to reduce the parasitic capacitance (or settling time) of the summing node. The use of 4x scaling means the fine comparators are required to resolve only 2 mV differences. This method offers a means to overcome the large amplifier settling time associated with fully residual scaling by: (1) partial scaling of the residual signal, (2) buffering to ease the settling time of the summing node through the distributed parasitic capacitance. This in turn ease the performance requirements of the fine comparators. As previously noted, partial residual scaling makes the fine comparator less vulnerable to noise, static offset, and charge injection errors. The drawback of this approach is the requirement of an accurate high speed voltage to current converter.

2.5.1 Building Blocks

The proposed architectures share many of the building blocks in common, namely the coarse comparator, fine comparator and DAC. This section deals with the review of the performance constraints on these building blocks. The settling time equations for each building block are presented and discussed for completeness.

2.5.1.1 Coarse Comparator

The design of both coarse and fine comparators plays a crucial role in the overall system performance. Their input offset voltage and delay directly influence the resolution and the speed of the coarse stage. The first stage has 2^m-1 coarse comparators. The coarse comparators estimate the 'm' MSB bits of the input signal. Either a regenerative type or simple multistage inverter circuit can be used as a coarse comparator. A multistage inverter approach (see Figure 5(b)) has been selected here to minimize power consumption. Also, due to the large input signal amplitude, the settling time of a multistage comparator settling will be very time competitive with a regenerative solution. The Fowler-Nordheim trimming mechanism is proposed to electrically program positive and negative reference voltages (threshold adjustments) on the floating gate. This shifts the trip point of the inverter by modifying the effective threshold voltage of each transistor of the inverter. This eliminates the large settling time associated with any autozero requirement.

The performance of a multistage coarse comparator is governed by the following constraint equations.

- $Z_{in} = (2^m-1)(C_{in})$ should be much greater than 5000 ohms to minimize reflection co-efficient error where 2^m-1 is the total number of comparators in the first stage and C_{in} is the capacitance of a comparator.
- C_{in} should be greater than or equal to 15 ffd to minimize thermal noise effects.
- The time required to settle to 1/2 LSB accuracy is given by:

$$T_{CC} = \frac{1}{GBP_U} (A \times M)^{\frac{1}{N}} \ln\left[V_{OH} \frac{2^{m+1}}{V_{FS}}\right] \quad (11)$$

where GBP_U is the unity gain bandwidth and equals g_m/C_{GS}. V_{OH} is the output logic level and A is the gain. N is the optimum number of stages as given by equation (9) (see section 2.3.2 for more details).

2.5.1.2 Fine Comparator

Second stage performance is determined primarily by the fine comparator, which resolves the LSBs of the input signal. The fine comparator must be designed to resolve inputs as small as 1/2 LSB of a 10 bit ADC in the subranging approach. The errors reviewed in the section 2.1 are more critical to fine comparator performance. Static offset voltage can be cancelled using a autozero technique (see [20] for details) or Fowler-Nordheim trimming.

- The time required for autozeroing the fine comparators is given by:

$$T_{AZ} = \frac{10}{GBP_U} \ln\left[V_{OS} \frac{2^{n+1}}{V_{FS}}\right] \quad (12)$$

where GBP_U is the Unity GBP and equals $g_m/C_{GS(FC)}$, g_m is the transconductance of the fine comparator. The autozeroing capacitor C_{AZ} is chosen much greater (10x) than $C_{GS(FC)}$ (the fine comparator input capacitance) in order not to attenuate the signal presented to the fine comparator.

Unfortunately, C_{AZ} typically increases the settling time by a factor of at least 10 over the potential process settling time. This will result in a prohibitive delay for the given performance

objective and the ω_T limitations. Therefore an alternative approach must be used to eliminate the static offset voltage. It is our intent to utilize Fowler-Nordheim trimming to eliminate static offset voltage of the regenerative comparators. Thermal noise as a error function can only be eliminated by the appropriate choice of C_L (see equation (4)). To minimize settling time given the signal levels in stage two, the fine comparator must be regenerative in nature (see section 2.3.2).

- The time required to settle to 1/2 LSB accuracy is given by:

$$T_{FC} = \frac{1}{GBP_A} \ln\left[\frac{V_{OH}\, 2^{n+1}}{V_{FS}}\right] \tag{13}$$

- With 4x scaling of the residual scaling, T_{FC} is given by:

$$T_{FC} = \frac{1}{GBP_A} \ln\left[\frac{V_{OH}\, 2^{n-1}}{V_{FS}}\right] \tag{14}$$

where V_{OH} is the output logic swing and GBP_A is the analog GBP and equals g_m/C_O. g_m represent transconductance and C_O represent the output capacitance of the regenerative amplifier. Comparator performance is most severely constrained by dynamic and mismatch dependent offset.

2.5.1.3 DAC

All two-step ADCs require the intermediate reconversion of the MSB to an analog equivalent by a DAC. In two-step ADCs, the coarse conversion typically provides a thermometer

code output, which suggests the use of a linear or segmented capacitor array [8] (see Figure 9) or 2^m reference currents for the DAC (see Figure 14) since both can be driven directly by the outputs of the first stage comparators. This DAC has several advantages over binary weighted DACs [8]. First, it avoids the need for thermometer binary code conversion in the critical path of the ADC, thereby improving the conversion speed. Second, the transfer characteristics of both the DACs is guaranteed to be monotonic and third, the DAC lends itself to simple layout and routing because each capacitor or required reference current can be included with its corresponding comparator. The linear settling of the output, the charge injection error and dynamic offset associated with the switches and capacitances put an upper limit on the settling performance of the capacitor array DAC while only the switches in the current steering DAC limit the settling performance. For this reason, we have chosen to use a current steering DAC along with current summing to calculate the residual voltage of the first stage conversion. However, Fowler-Nordheim trimming of currents will be required. DAC Performance is governed by the following constraints and equations.

For a capacitor array DAC,

- C_{DAC} should be greater than C_O (the total capacitance at the output node) in order not to attenuate the signal given to the subtractor or the amplifier (see Figure 6 and 7).
- The time required to settle to 1/2 LSB is given by:

$$T_{DAC} = \frac{K}{GBP_D} \ln\left[\frac{V_{MSB}\, 2^{n+1}}{V_{FS}}\right] \qquad (15)$$

where 'n' is the total number of bits and GBP_D is the digital GBP equals $g_{m(Sw)}/C_{DAC}$ and $g_{m(Sw)}$ is the transconductance of the switch. K varies between 2 to 10 and depends on the process

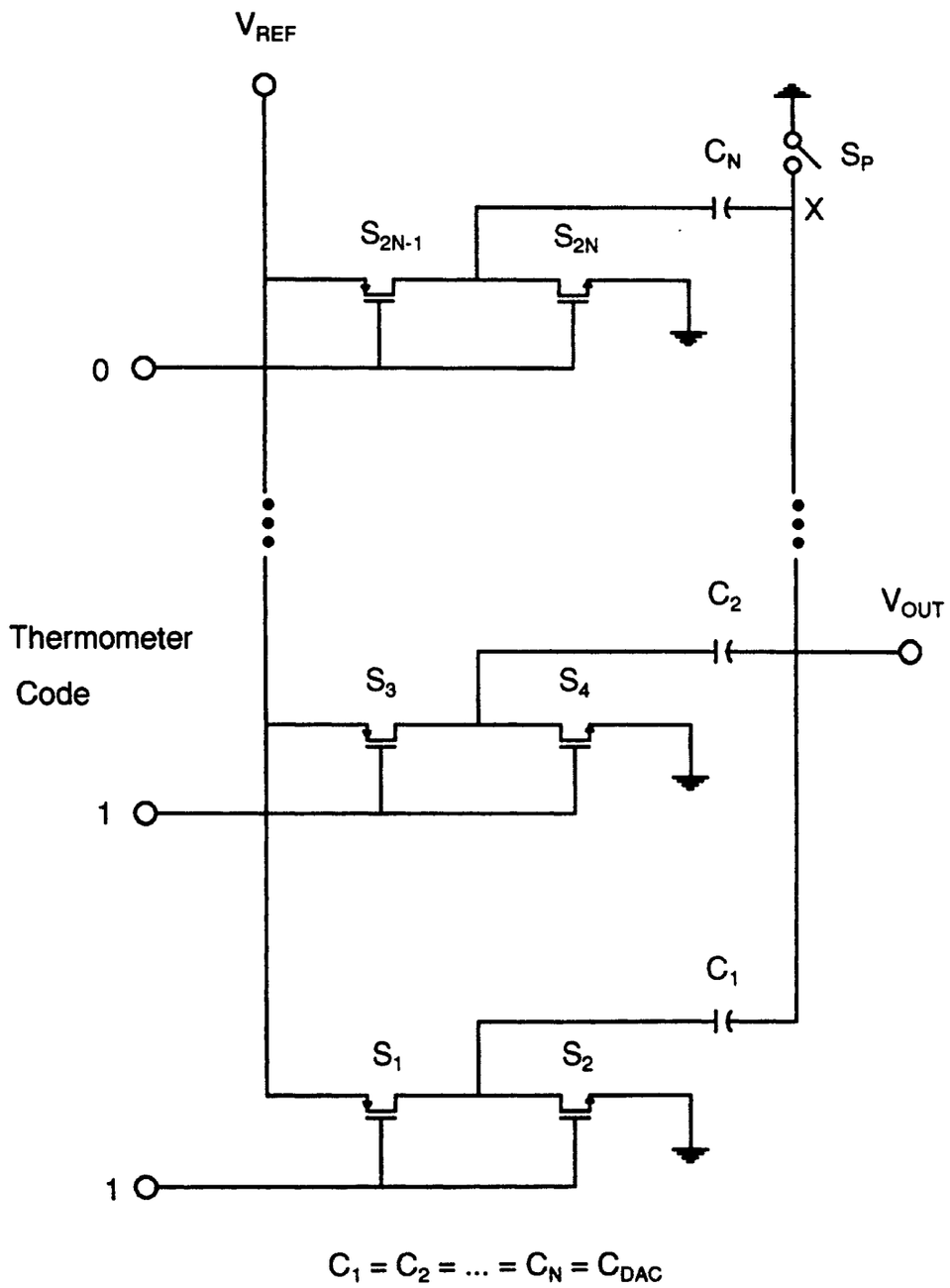

Figure 9. Linear-array capacitor DAC.

parameters. V_{MSB} is the reconverted analog signal of the first stage.

The current steering approach is governed by the following settling equations.

- The time required to settle to 1/2 LSB accuracy is given by:

$$T_{IDAC} \approx \frac{2}{GBP_D} + C_L R_{SUM} \ln[2^{n+1}] \qquad (16)$$

where the first term is the delay of the settling switch. GBP_D is the digital gain bandwidth product and equals $g_{m(Sw)}/C_{GS(Sw)}$. C_L represent the total capacitance at the summing node and R_{SUM} is the summing resistor used to provide voltage scaling (see Figure 8).

In the following sections, total ADC system delay performance (delay is easily converted to the sample rate) constraints will be developed for the three approaches using the building blocks presented previously.

2.5.2 Subranging ADC

The system performance of the subranging architecture, including the constraint equations for the subtractor and the total conversion time are presented in this section.

In the first stage, the coarse comparator estimates the 'm' MSB bits of the input signal and sets the reference voltages for the second stage. The interstage processing is carried out by the DAC in conjunction with a subtractor. A linear array capacitor DAC is used to allow voltage processing to convert the ADC estimate generated by the first stage to an analog signal. The subtractor develops the residual signal by combining the DAC output with the held input signal. The second stage digitizes the residual output of the subtractor to encode the LSBs.

2.5.2.1 Subtractor

The subtractor (Sb) is configured for a closed loop gain of unity to achieve maximum speed and linearity. The subtractor circuit is as shown in Figure 10 [8]. If the subtractor is implemented as a fully differential circuit, the offset is primarily the result of charge injection mismatch between switches and the offset voltage of opamp. As the subtractor offset voltage appears as an offset voltage in the overall characteristics of the ADC, either it must be autozeroed, trimmed or kept low enough so as not to drive the input of the second stage out of its linear range. Subtractor performance is governed by the following constraints and equations.

- $C_{GS(Sb)}$ should be greater than $C_O/2$ to maintain the stability of the circuit. C_O is the output capacitance of the subtractor (i.e., the input capacitance of the fine comparator and the inherent capacitance of the subtractor) and is given by $(2^m-1)(C_{GS(FC)})$ in subranging ADC architecture.
- The time required to settle to 1/2 LSB accuracy is given by:

$$T_{Sb} = \frac{5}{GBP_A} \ln\left[\frac{V_{Res}\, 2^{n+1}}{V_{FS}}\right] \qquad (17)$$

It is assumed that $g_{m(Sw)}$ (the transconductance of the switch) is greater than g_m (the transconductance of the subtractor) and GBP_A is the analog GBP equals $g_{m(Sb)}/C_O$. C_O is the output capacitance of the subtractor. V_{Res} is the residual analog signal making up the LSB bits.

- Thermal noise must be less than 1/2 LSB power. (see section 2.1.3).

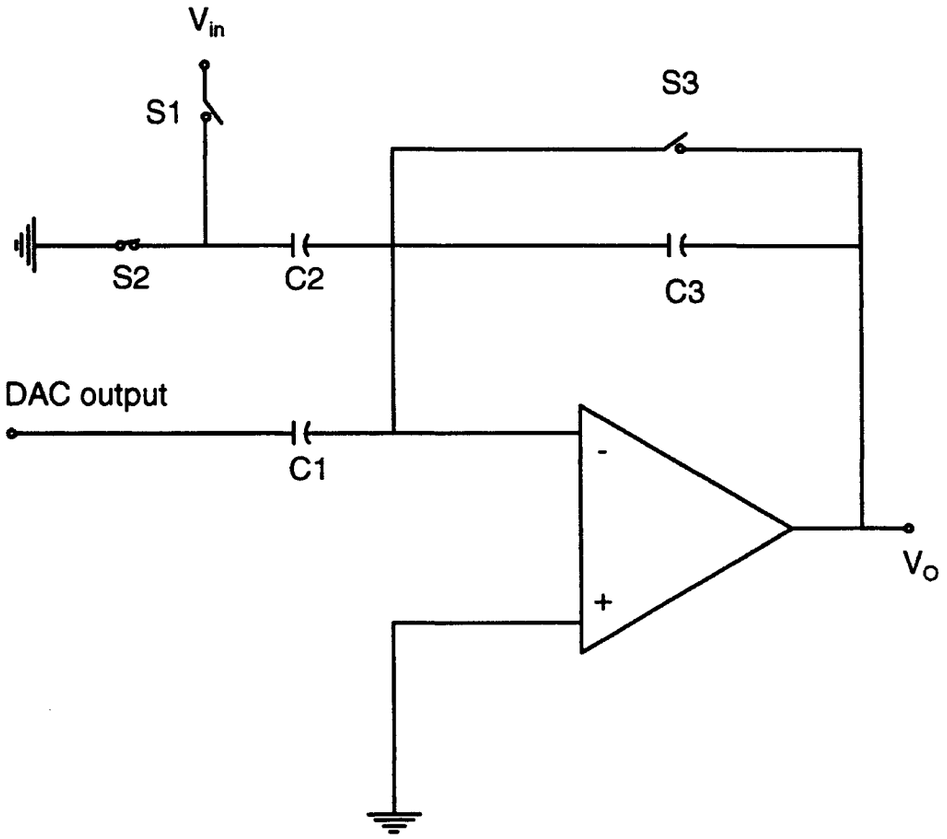

Figure 10. Subtractor circuit.

2.5.2.2 Total Conversion Time

For a subranging ADC, the total conversion or settling time is obtained by simply summing the settling time's of each block in the worst case serial path (see Figure 6) of the system. It is assumed that the settling time of the input is small when compared with total conversion time. Then, from equations (11), (15), (17) and (13), the total time taken for an analog to digital conversion by the subranging architecture is given by:

$$T_{Con} = \frac{1}{GBP_U}(A \times M)^{\frac{1}{N}} \ln\left[V_{OH}\frac{2^{m+1}}{V_{FS}}\right] + \frac{K}{GBP_D}\ln\left[\frac{V_{MSB}\,2^{n+1}}{V_{FS}}\right]$$

$$+ \frac{5}{GBP_A}\ln\left[\frac{V_{Res}\,2^{n+1}}{V_{FS}}\right] + \frac{1}{GBP_A}\ln\left[\frac{V_{OH}\,2^{n+1}}{V_{FS}}\right] \qquad (18)$$

where $GBP_U = 2\ GBP_D = 5\ GBP_A$, by substituting A = 343, N = 3, V_{OH} = 1.5 V, K = 2, V_{MSB} = 1 V, V_{FS} = 1 V, V_{Res} = 124 mV we get,

$$T_{Con} \approx \frac{47}{GBP_A} \qquad (19)$$

2.5.3 Residual Scaling ADC

The residual scaling ADC works on a somewhat different principle than the subranging architecture. The residual signal is scaled up by 2^m times between the stages. Hence both stages

are identical allowing for the potential use of same comparator to compute both the MSBs and LSBs. The performance of the coarse comparator, DAC and fine comparator were explained in section 2.5.1. For this reason, only the overall system operation, the performance and constraint relations of the residual amplifier and the total conversion time of the residual scaling ADC are presented here.

In the first stage, the coarse comparator estimates the 'm' MSB bits of the input signal. In the intermediate stage, a capacitor array DAC reconstructs the analog signal of the first stage and an interstage amplifier scales up the residual signal by 2^m for LSB determination.

2.5.3.1 Residual Amplifier (Amp)

A differential amplifier circuit is used to subtract the reconverted 'm' bit analog signal of the first stage from the input and scales up this residual signal by 2^m times. We refer to the subtractor circuit (Figure 10) as residual amplifier if the ratio of C_2 to C_3 is 2^m. Performance of the residual amplifier is governed by the following equations.

- $C_{GS(Amp)}$ should be greater than $C_O/2$ to maintain the stability of the circuit. $C_{GS(Amp)}$ is the input capacitance of the residual amplifier. C_O is the output capacitance of the amplifier (i.e., the input capacitance of the second stage comparator) and is given by $(2^m-1)(C_{GS(Sec)})$ in the two-step architecture with residual scaling. 2^m-1 represent the total number of comparators in the second stage. $C_{GS(Sec)}$ is the input capacitance of the second stage amplifier.
- The time required to settle to 1/2 LSB accuracy is given by:

$$T_{Amp} = 4 \frac{2^m}{GBP_A} \ln[2^{m+1}] \tag{20}$$

where GBP_A is analog gain bandwidth and equals g_m/C_O. g_m represent the transconductance of the amplifier.

2.5.3.2 Total Conversion Time

If the noted settling constraints for the coarse comparator, DAC and residual amplifier are combined, from equations (11), (15) and (20), the total conversion or settling time is given by the following equation,

$$T_{Con} = 2 \frac{1}{GBP_U} (A \times M)^{\frac{1}{N}} \ln\left[V_{OH} \frac{2^{m+1}}{V_{FS}}\right] + \frac{K}{GBP_D} \ln\left[\frac{V_{MSB}\, 2^{n+1}}{V_{FS}}\right]$$

$$+ 4 \frac{2^m}{GBP_A} \ln[2^{m+1}] \tag{21}$$

where $GBP_U = 2\ GBP_D = 5\ GBP_A$, by substituting m = 5 and all other terms are as defined in the section 2.5.2.2, we get,

$$T_{Con} \approx \frac{556}{GBP_A} \tag{22}$$

2.5.4 Subranging ADC with Partial Residual Scaling

This architecture attempts to capture the advantages of both the architectures presented previously and combine them to overcome some of the limitations of both. Partial scaling is a hybrid approach similar to residual scaling except that the residual signal is amplified by only four times to avoid the large settling time of the scaling amplifier, while at the same time making the fine comparators less sensitive to noise, charge injection error and dynamic offset. The performance of the coarse comparator, current steering DAC and fine comparator were summarized in section 2.5.1. This section provides an system overview, the performance and the constraint equations for the voltage to current converter and the total ADC conversion time for partial scaling.

In the first stage, the coarse comparators estimate the 'm' MSB bits. The residual signal is formed using a V-I current conveyor to minimize the delay in conjunction with a current steering DAC. Both the V-I converter and current steering DAC utilizes Fowler-Nordheim trimming to eliminate V_{OS} error and static transistor mismatching. Summing of the DAC current and current conveyor current across an accurate summing resistor R_{SUM} provides voltage scaling for the residual signal.

2.5.4.1 Voltage to Current Converter

The input voltage signal is converted into its current equivalent to permit the subtraction of the first stage reconverted analog current signal (DAC output). This approach of summing current signals is potentially faster, but requires accurate resistor matching and a very fast and accurate V-I converter. The accuracy of conversion depends on the accuracy of R_{SET} of the V-I

converter and should be 1 part in 2^{n+1}.

Voltage to current converter performance is governed by the following equations

- For minimum delay, C_L R_{SET} should be less than $1/GBP_U$.

where R_{SET} scales the current magnitude

- The time required to settle to 1/2 LSB accuracy is given by:

$$T_{V\text{-}I} = \frac{2}{GBP_U} \ln[2^{n+1}] \qquad (23)$$

where GBP_U equals g_m/C_{GS}. g_m is the transconductance and C_{GS} is the input capacitance of V-I converter.

The residual error signal is scaled up by four times to ease the accuracy and settling requirements of fine comparator. This requires R_{SUM} to be equal to four times of R_{SET}. The required accuracy of R_{SUM} is also 1 part in 2^{n-1}. In addition, to ensure maximum bandwidth $R_{SUM}C_L$ should be maintained much less than $1/GBP_D$ while g_m of the current conveyor and unit current sources be sufficiently large enough to drive the parallel $R_{SUM}C_L$ impedance, where C_L is the input capacitance of the fine comparator buffer.

2.5.4.2 Total Conversion Time

Assuming that the settling time of V-I converter is less than combined conversion time required for coarse stage and DAC, the total conversion time is given by summing up the settling time's of the coarse comparator, DAC, sumnode and fine comparator (see Figure 8). From the equations (11), (16) and (14),

$$T_{Con} = \frac{1}{GBP_U}(A \times M)^{\frac{1}{N}} \ln\left[V_{OH}\frac{2^{m+1}}{V_{FS}}\right] + \frac{2}{GBP_D} + C_L R_{SUM} \ln[2^{n+1}]$$

$$+ \frac{1}{GBP_A} \ln\left[\frac{V_{OH}\, 2^{n-1}}{V_{FS}}\right] \quad (24)$$

where $GBP_U = 2\ GBP_D = 5\ GBP_A$, by substituting for A, N, V_{OH} as defined in section 2.5.2.2, we get,

$$T_{Con} \approx \frac{17}{GBP_A} + 7.6\ C_L R_{SUM} \quad (25)$$

2.5.5 Summary

For a given process, constraints and maximum conversion rates have been obtained for the three ADC architectures specifically, subranging, residual scaling and subranging with partial residual scaling. These simplified assumptions may lead to an error of 30% to 50% in the estimated performance. However this offers an excellent means of ranking the relative performance of each approach. Finally an improved version for a two step ADC based on a partial residual scaling architecture has been presented, which when combined with Fowler-Nordheim trimming offers the potential to perform the classical two-step 10 bit ADC architecture. In this section, we summarize how the proposed architecture outperforms the other two architectures.

The three architectures differ based on the way the interstage process has been carried out.

From the equations (19), (22) and (25) it is seen that subranging architecture is relatively faster. However the drawback of subranging architecture lies with designing a high-speed fine comparator which has a noise floor and offset voltage less than 490 μV (represents 1/2 LSB of the second stage of ADC). This is difficult to achieve with the MOS devices. The stringent requirements of the fine comparator can be relaxed by amplifying the residual signal 2^m times as in case of two-step with residual scaling architecture. But from the equation (22) it is seen that, this approach is 12 times slower than the subranging architecture. This is due to the large settling time associated with the amplifier. Hence to overcome the drawbacks associated with these two architectures we proposed the subranging architecture with partial residual scaling. This architecture can be made to run as fast as subranging architecture by employing the following techniques

- Current mode summing is used in conjunction with V-I converter and DAC to generate the residual signal. This potentially increases the frequency of operation due to lower impedance of current node and reduced full scale swing.
- The residual signal has been scaled up by four times by setting the sum node resistor four times that of the R_{SET} of V-I converter. This makes the fine comparator less sensitive to noise and avoids the use of an amplifier in the critical path.
- Distributed buffers are used to ease the settling time associated with the sumnode. This will greatly reduce the settling time at the sumnode (second term of the equation (25)).
- Fowler-Nordheim trimming is employed instead of classical autozero technique to reduce the offset voltage. The trimming guarantees a fully asynchronous operation unlike the autozero technique, this in turn eliminate the charge injection error and the settling time associated with autozeroed process. As floating-gate devices can be fabricated with thick-oxide, charge can be stored for life time of the product.

Key to the success of this architecture are accurate resistors (1:1000+), understanding of the available tunneling structures (Is it true Fowler-Nordheim tunneling) and a fast accurate V-I converter. The implementation of some of the building blocks of subranging ADC with partial residual scaling are discussed in detail in the next chapter.

CHAPTER III

SYSTEM BUILDING BLOCKS

This section describes the implementation of the building blocks for the proposed architecture of a subranging ADC with partial residual scaling in thin-film silicon on insulator (TFSOI) technology. The functional description and the constraints were covered in brief in section 2.5.4. The design analysis and simulation results of coarse comparator, DAC, buffer and fine comparator are presented. The design of V-I converter is beyond the scope of this thesis. However by making the assumption that the conversion time of the V-I converter is less than that of the conversion time required for the coarse stage and DAC combined, the total conversion time of the proposed ADC can be estimated.

3.1 Coarse Comparator

This section presents the design considerations for multistage approach, analysis of the first stage with floating gate injectors and the concept of trip point control using Fowler-Nordheim trimming.

The coarse stage resolves the five MSBs of the input signal. To determine all of the possible quantization levels of an n/2 coarse stage, $2^{n/2}$-1 (in the present case 31 comparators) are required. A reference decision level for each comparator is typically generated by each voltage

division of a reference. The comparator generates thermometer coded outputs. Suitable digital logic can then be used to generate a MSB digital word equivalent to the value of the detected quantization level. At the same time, the digital thermometer coded signal will be converted to the analog signal by DAC to generate the residual signal.

As one of the transistor is always off when the inverter circuit is in either high or low state, there is no dc path from V_{DD} to V_{SS}, the resultant quiescent current and hence the power dissipation is zero. However, there will be dynamic power dissipation during transition from either 0 to 1 or 1 to 0, as both transistors are on for a short period of time. The dynamic power dissipation during switching is given by [21]:

$$P_d = C_L (V_{DD} - V_{SS})^2 f_p \tag{26}$$

Thus the average power dissipation is proportional to output capacitive load, power supply voltages and switching frequency. Since the circuits are operated at ± 1.5 V and the C_L (the input capacitance of the following stage) is relatively small for short channel TFSOI devices, the dynamic power consumption is relatively small.

In a conventional ac coupled inverter amplifier, the reference voltage is stored on a capacitor and during the amplification mode the comparator amplifies the difference between input and reference, generating a decision bit. Where as in present case, corresponding to various reference voltages, the trip points are set by programming an effective threshold. This is achieved by varying the threshold voltages of either M1 or M2 of the first stage using Fowler-Nordheim

trimming. This approach allows the continuous operation of the coarse comparator resulting in high-speed conversion.

3.1.1 Design Considerations

A multistage comparator circuit is as shown in Figure 11. Three stages were selected in this design since higher net gain results in greater speed. The choice of three stages is a compromise between the optimal gain per stage and the required logic level to drive the DAC and the minimum allowable gain. In a multistage approach, average propagation delay of each comparator is smaller than delay of each stage as the input signal is amplified in the stages within the comparator, the succeeding stages are driven by stronger signal and thus switching speed is increased [22]. The gain of each stage is given by:

$$A = \frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}} \tag{27}$$

The switching delay of each stage is given by:

$$t_1 \approx \frac{C_{GS3} + C_{GS4}}{g_{m1} + g_{m2}} \tag{28}$$

where g_{m1}, g_{m2} and g_{DS1}, g_{DS2} represents transconductance and output conductance of the first stage respectively. C_{GS3} and C_{GS4} represents the input capacitance of the next stage transistors. For low frequency operation, typical 0.25 μm TFSOI parameters $g_{m1} + g_{m2}$ and $g_{DS1} + g_{DS2}$ equals 3.1 mmho

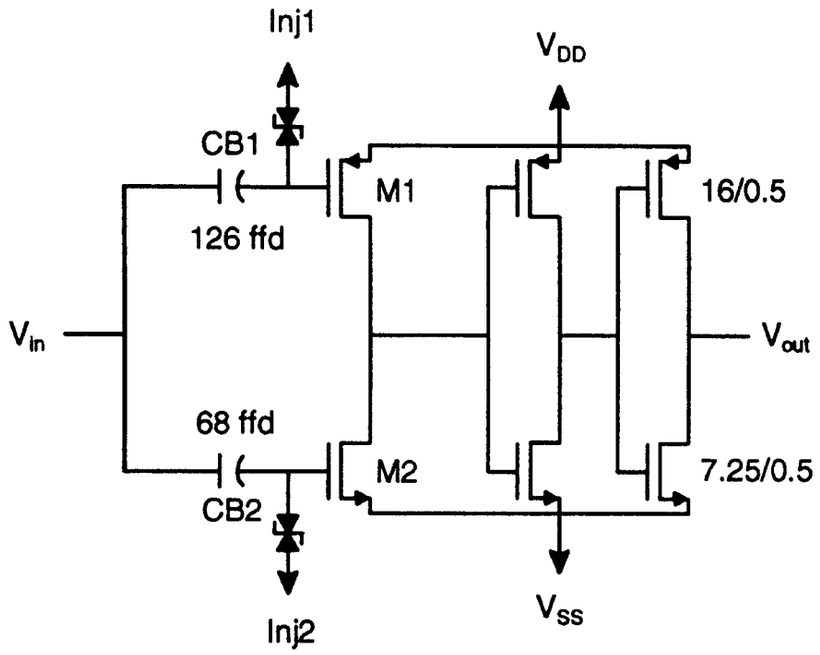

Figure 11. Multistage comparator.

and 0.26 mmho respectively results in a small signal low frequency voltage gain of approximately 12. It is expected that the actual gain of the process may be as low as 7 or 8. Figure 12 shows the simulated transient response of a the multistage comparator with the input voltage of 16 mV (1/2 LSB of the coarse stage). The performance of the circuit with and without injectors is expected to be nearly identical. With a β ratio of one and taking into account the mismatch from transistor widths M1 and M2 equal to 16 μm and 7.25 μm and lengths of 0.5 μm is chosen. The projected delay for the coarse stage from simulation is 250 ps. Theoretical delay from equation (8) is 115 ps with process f_T of 20 GHz, total gain A equal to 512 (gain per stage equal to 8) and N equal to 3.

3.1.2 Analysis of the First Stage

The first stage of a coarse comparator consists of: (1) current injectors pair C_{inj1} and C_{inj2} for injecting and removing electrons to and from the floating gate, (2) a bootstrap capacitors C_{B1} and C_{B2}, to allow external control and programming of the floating gate voltages without actually having an electrical connection between programming and floating gate and finally (3) the inverter consisting of M1 and M2 with these floating gates.

The percentage of the programming voltage that appears across the floating depends on the capacitive coupling ratio K. It is given by [15]:

$$K \approx \frac{1}{1 + \frac{C_{GS}}{C_B}} \tag{29}$$

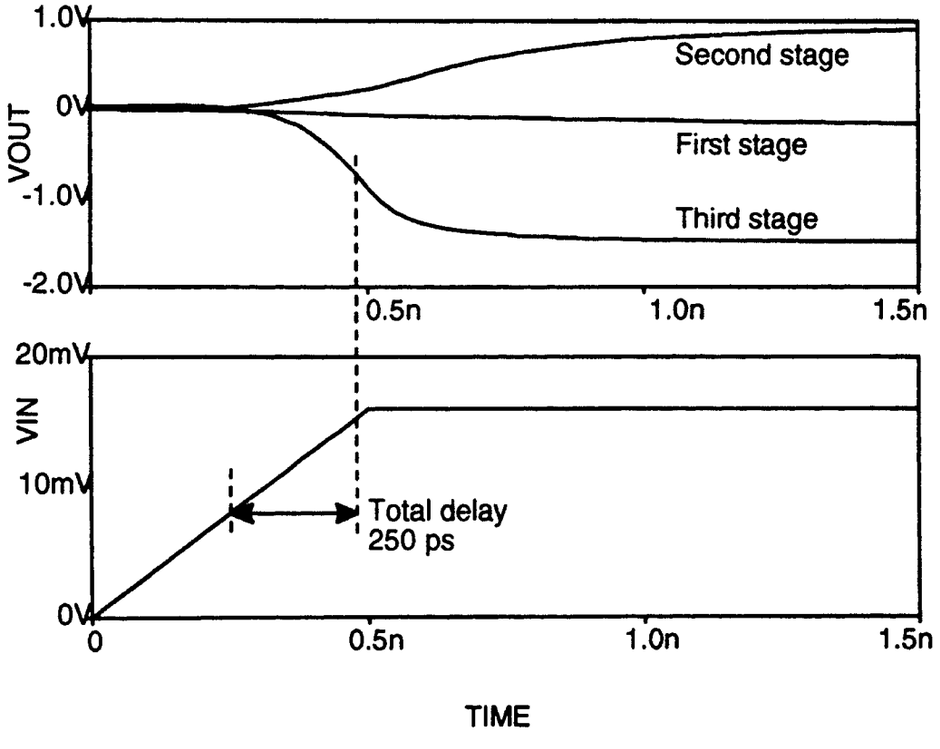

Figure 12. Transient response of multistage comparator.

where C_B is the bootstrap capacitor between the floating gate and the control gate across the source and drain shorted, C_{GS} is the floating gate to source capacitance. C_{GD} (the capacitance between floating gate and drain) and C_{inj} (injector capacitance across the gate oxide) are assumed to be relatively small.

The programming voltage required tunneling is given by:

$$V_{PGM} = \frac{V_{tun}}{K} \tag{30}$$

where V_{tun} is the tunneling voltage. Thus for the given tunneling voltages, tighter coupling minimizes the required programming voltages V_{PGM}. For this reason, the bootstrap capacitor should be at least one order of magnitude larger than C_{GS}. Taking into account the circuit area, proper trade offs between the size of the bootstrap capacitor and the programming voltage should be made. The approximate bootstrap coupling ratio in this design is 9/10.

The working principle of the floating gate injector and Fowler-Nordheim mechanism was covered in detail in section 2.2. The injector structure symbolically shown in Figure 11 is similar to the one explained in the section 2.2.2.3. To inject electrons on to the floating gate, the V_{PGM} should be kept negative and positive voltage applied at V_B. For bootstrap ratio of 9/10, a tunneling voltage on the order of 6 to 7 V [10] should result changing the threshold voltage as given by the equation (6). Similarly electrons can be removed from the floating gate by keeping V_{PGM} positive and V_B negative.

3.1.3 Transfer Characteristics of Coarse Comparators

The narrow range where both transistors are in the saturation is exploited for use in analog comparison. The saturation currents for two transistors including the q_T component (injected charge on the floating gate), are given by:

$$I_{DS1} = -\frac{\beta_p}{2}\left(V_{in} \pm \frac{q_T}{C_{GS} + C_B} - V_{DD} - V_{Tp}\right)^2 \tag{31}$$

$$I_{DS2} = \frac{\beta_n}{2}\left(V_{in} \pm \frac{q_T}{C_{GS} + C_B} - V_{SS} - V_{Tn}\right)^2 \tag{32}$$

with I_{DS1} equal to I_{DS2}

$$V_{in} = \frac{V_{DD} + V_{Tp} + \left(V_{SS} + V_{Tn}\right)\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \pm \frac{q_T}{C_{GS}+C_B} \tag{33}$$

where β_n, β_p, V_{Tn} and V_{Tp} take on their standard notations. V_{in} is the applied input voltage.

Since both transistors are in saturation, they act as current sources so that the equivalent circuit in this region is two current sources in series between V_{DD} and V_{SS} with the output voltage coming from their common point. The region is inherently unstable due to its high gain nature

and the changeover from one logic level to the other is rapid. Thus a small input voltage has a large effect at the output. If β_n equals β_p and V_{DD} equals negative V_{SS}, then from equation (33) the trip point can be derived as,

$$V_{in} = V_{Trip} = \frac{V_{Tn} + V_{Tp}}{2} \pm \frac{q_T}{C_B} \tag{34}$$

This implies that the changeover between logic levels is symmetrically placed about the point at which V_{in} equals V_{out}. This point is referred to as trip point. For equal threshold voltages (with q_T equal to 0), the trip point is zero.

In the coarse comparator stage, 31 comparators should trip at 31 uniformly spaced voltages. From equation (34), it is seen that by varying the threshold voltages (by injecting a charge q_T on the floating gate), the trip point can be varied. This implies that for positive trip point, effective V_{Tn} (effective threshold voltage is the threshold voltage after programming the device) should be greater than effective $|V_{Tp}|$ and for negative trip point, effective V_{Tn} should be less than effective $|V_{Tp}|$. With V_{ref} equal to 1, n being equal to 5 in the coarse stage, the trip points should be set from ±32 mV (correspond to LSB) to ±0.5 V (correspond to MSB) in steps of 32 mV. The shift in the trip point by 1 LSB is achieved by adding 1 LSB to each of the threshold voltages of n and p channel transistors (see equation (34)). The Figure 13 shows the transfer characteristics obtained for comparators with different trip points by simulation. As noted previously the floating-gate devices with thick-oxide have good retention characteristics and hence the threshold voltage is expected to remain constant for a typical product life of 10 years.

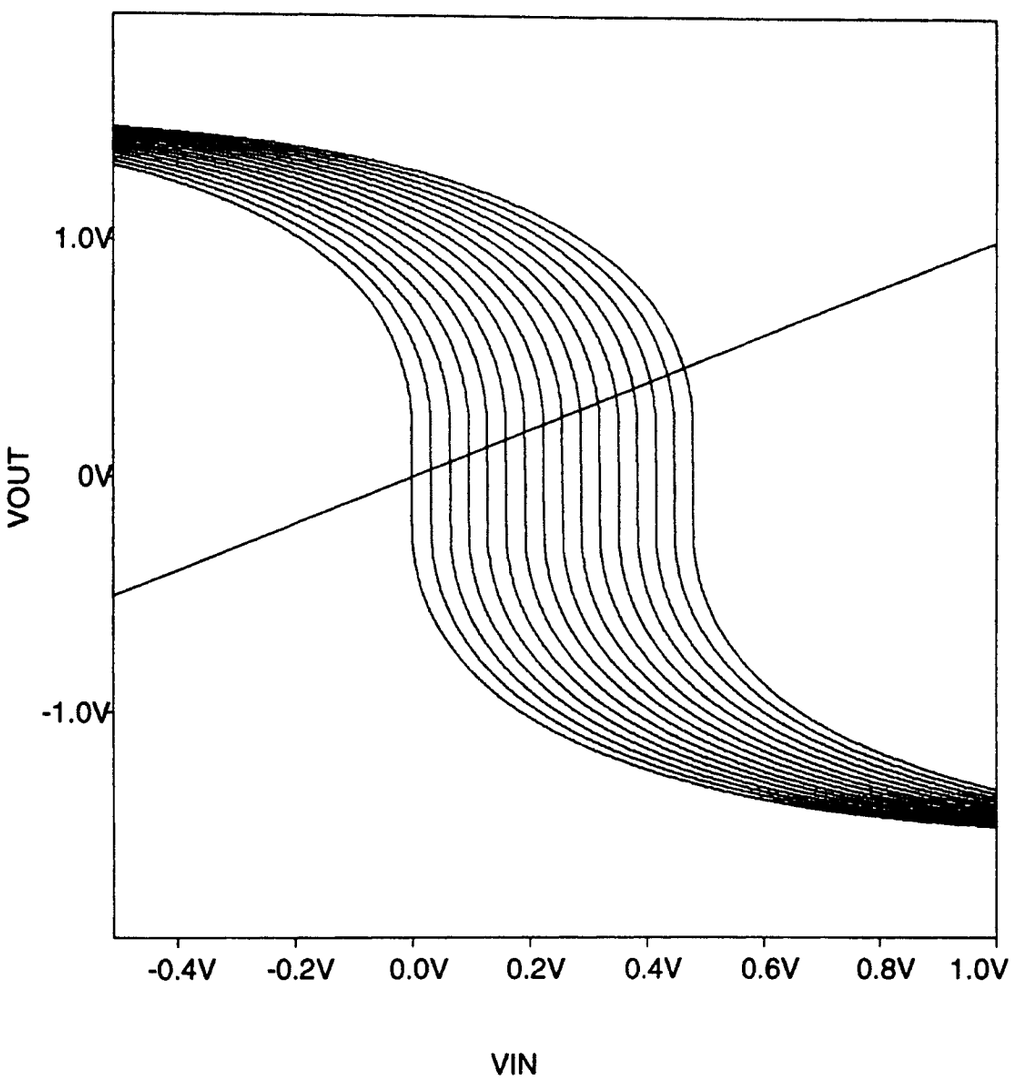

Figure 13. Transfer characteristics of comparators with different trip points.

3.2 Current Steering DAC

The circuit diagram for the current steering DAC is as shown in Figure 14. In order to meet a high conversion rate demand, the current steering DAC approach which makes use of unit current sources is used. A current mode converter has the advantage that voltage swings in the circuit are minimized, which in turn reduces the sensitivity for parasitic capacitances and enhances the conversion speed as well as accuracy.

The DAC consists of 31 units current sources along with the differential current switch (see Figure 15), to route the current either to the output node (R_{SUM}) or ground. All the switches are operated by the thermometer output code of the coarse stage with each comparator routing one current source. This in turn eliminates the decoding delay. The total current at the output node obtained by adding the unit current sources improves the relative accuracy of the sum current with a factor of $\sqrt{N}$, where N is the total number of unit current sources, provided that original matching properties are uncorrelated [23]. The same unit current source structure can be duplicated for every unit current. This allows optimal design of the circuit for high speed. This also ensures low glitch operation that can result due to unequal delays [24].

3.2.1 Design Considerations

To achieve the best possible current matching between current sources, the device must have both a high output resistance and good device matching characteristics. To improve the device output resistance, long channel length devices must be used. To improve the device matching, both the channel length and the channel width must be significantly larger than minimum geometry. Consequently, to achieve good accuracy, large devices must be used. This

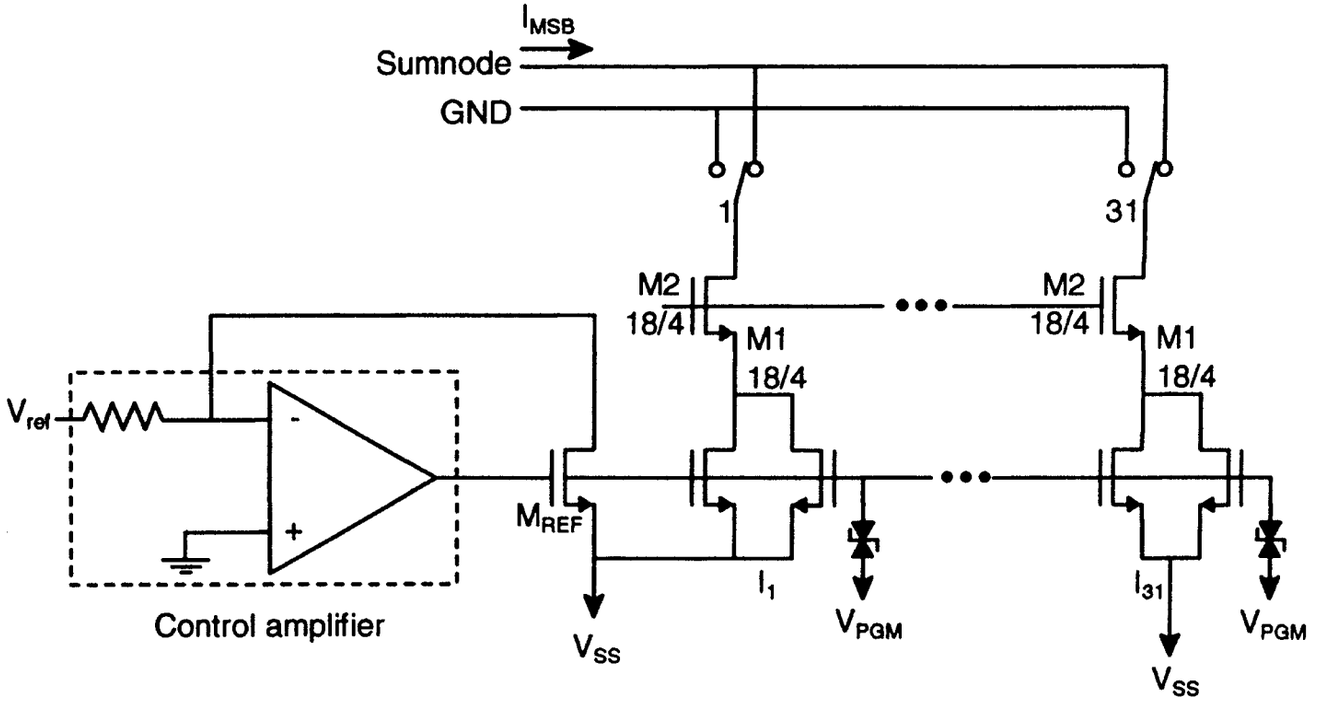

Figure 14. 5 bit Current steering DAC.

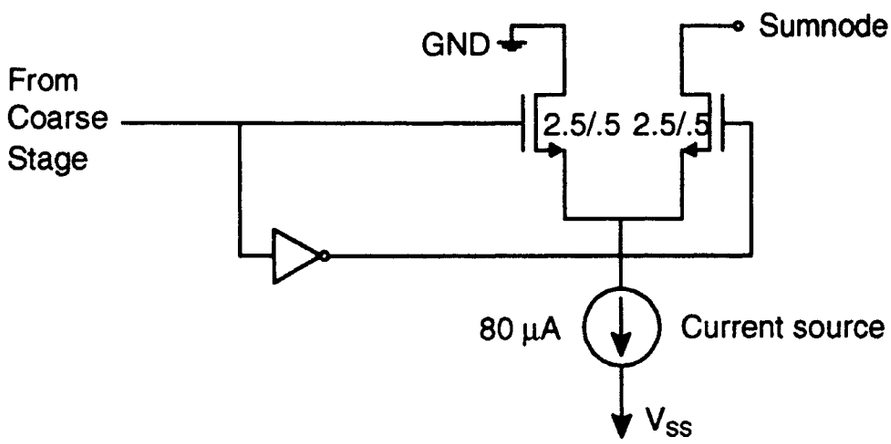

Figure 15. Differential current switch.

has the added benefit of reducing thermal noise. Although increasing the device size reduces the device mismatches, the mismatches cannot be eliminated completely. Even if a sufficiently high output resistance can be obtained, the device mismatches will limit the converter accuracy. These mismatches lead to a relative error current given by [9]:

$$\frac{\Delta I}{I_{REF}} = \frac{\Delta \beta}{\beta} \pm \frac{2\Delta V_T}{\Delta V} \tag{35}$$

where I_{REF} is the reference current and all other terms take on their standard notations. The error of the DAC should be kept below 1/2 LSB with 10 bit resolution. The desired accuracy can be achieved by trimming the current sources by Fowler-Nordheim trimming. With 4x scaling of the residual signal, the voltage at the sum node equivalent to 1 LSB of fine stage will be 4 mV. To reduce the large settling time associated with the sum node, the resistor R_{SUM} was set equal to 50 Ω. Hence the unit current source will be 80 μA. The reference transistor M_{REF} is used in a current mirror configuration to set the currents in the unit current sources. Placing M_{REF} in a closed loop with the control amplifier compensates for systematic variations in threshold voltage of the current source transistors due to time and temperature [24]. The folded cascode amplifier with high open loop gain can be used as a control amplifier.

To achieve greater resolutions, the effect of the V_T mismatch should be kept to minimum by operating the current sources with the highest possible overdrive voltage. As the threshold voltage of TFSOI devices is in the range of 0.2 V, the current sources are designed to operate at an overdrive voltage of 2.5 V_T or approximately 500 mV. Devices with 4 μm channel length are

chosen to have greater output impedance. With I equal to 80 μA, K equal to 150 $\mu A/V^2$ and ΔV of 500 mV, the widths of M1 and M2 equal to 18 μm is chosen ($L_{effective}$ = 0.25 μm).

The parasitic capacitance at the common source node of the switch should be small to minimize the recovery time of the voltage at this node during the switching transition. This can be achieved by using small sized transistors for the current switch [25]. Hence minimum size with W equal to 2.5 μm and L equal to 0.5 μm are chosen.

The conversion rate of the DAC is equal to the delay of the switch and settling time associated with the residual signal at the sumnode as given by the equation (16). The delay associated with the switch is 11 ps by simulation. Theoretical delay of the switch from the first term of the equation (16) is approximately 15 ps. By substituting C_L (the capacitance at the sumnode) equal to 64 ffd (see section 3.3), R_{SUM} equal to 50 Ω, n equal to 10 in the second term of the equation (16), the settling time associated with the signal will be 24 ps. Hence DAC conversion time is approximately 35 ps (from simulation). The theoretical conversion time is 39 ps. It has been assumed that the conversion time of the V-I converter can be designed such that it is less than the combined conversion time associated with the coarse stage and DAC.

3.3 Distributed Buffer Chain

Distributed buffers are used to ease the settling time associated with the sumnode. The settling time associated with the sumnode without buffers would be R_{Sum} $C_{GS(FC)}$. As the $C_{GS(FC)}$ in present case is quiet high (approximately 1 pf), the settling time associated with the sumnode would be excessively high. The impact of the input capacitance of the fine comparator on the sumnode is reduced by connecting a tree structure of buffers between the sumnode and fine comparators in the second level ADC is as shown in Figure 16. Each buffer in the buffer chain

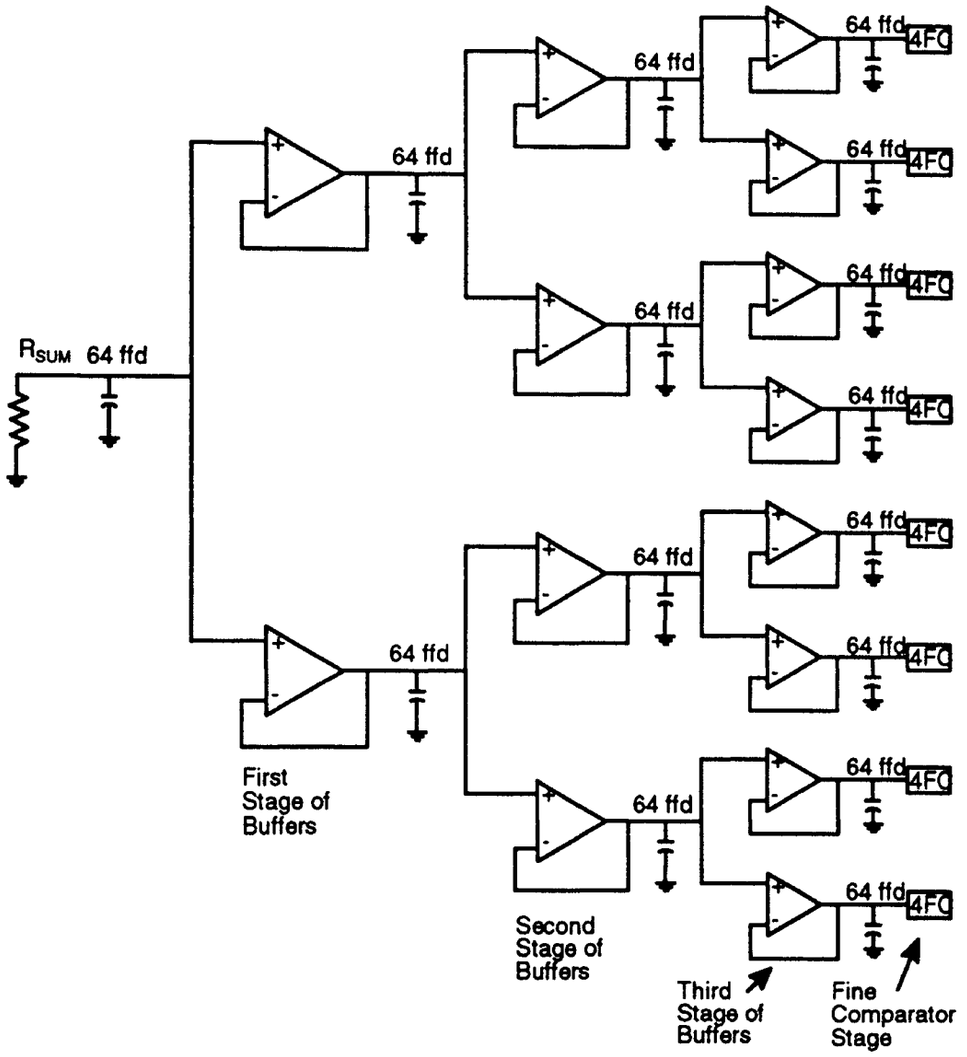

Figure 16. Distributed buffer chain.

is a simple folded cascode amplifier configured for a closed loop gain of a unity. The size of the buffer is ultimately determined by maintaining the ratio of output to input capacitance of the buffer equal to three in order to maintain the stability of the circuit. The buffer in each stage will drive the twice of its input capacitance along with its own input capacitance.

As a trade off between area and delay, for a given input capacitance of fine ADC stage, three stages of buffers were used. The total delay will be only the delay along any one of the parallel paths. All buffers in the buffer chain are identical.

Due to stability and self compensating characteristics and minimum area requirements, the folded cascode opamp was selected as a buffer (see Figure 17). The open loop gain and phase response of the opamp is as shown in Figure 18. The circuit is designed for 33 dB of open loop gain and unity gain frequency of 1.8 GHz. The phase margin with 3 times of its input capacitance load is 47°. The total delay starting from the sumnode, through the buffer along one of the parallel path is given by equation (8). The closed loop gain A is equal to 1 and N number of stages equal to 3. Hence the total propagation delay associated with the buffer from simulation is approximately equal to 161 ps (with f_T of 1.8 GHz). The theoretical propagation delay is approximately 86 ps.

3.4 Fine Comparator

The fine comparator circuit is as shown in the Figure 19. It consists of bias circuit, preamplifier, cross coupled latch and inverters. Preamplifier operates using ±1.5 V supplies while latch uses 1.5 V supply. The preamplifier consists of a differential pair M1 and M2 with current source pair M3 and M4 acting as active loads. The latch is composed of cross coupled p-channel pair M6 and M7 and n-channel pair M8 and M9 with n-channel switch MSw to provide a reset

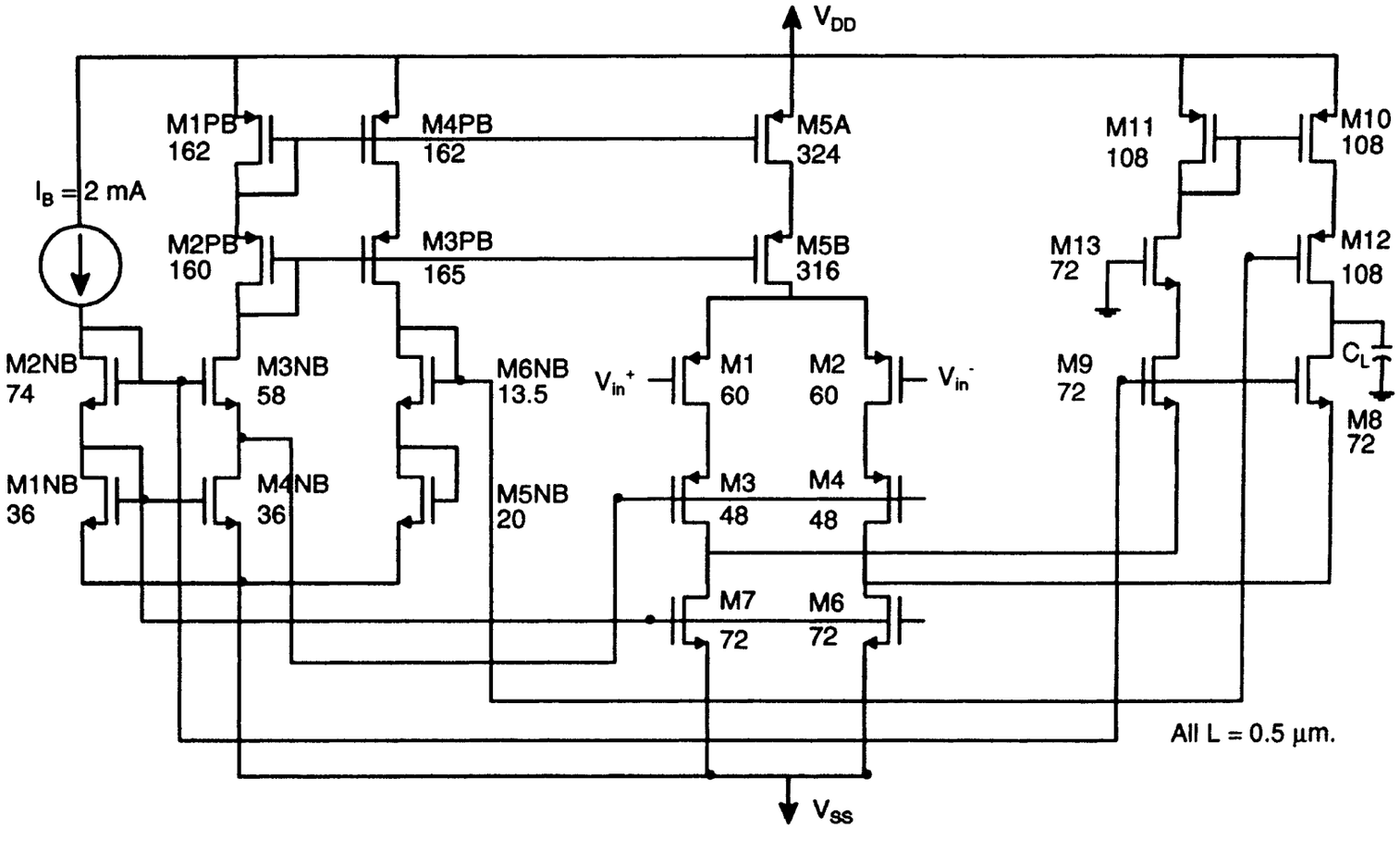

Figure 17. Folded cascode amplifier with bias string.

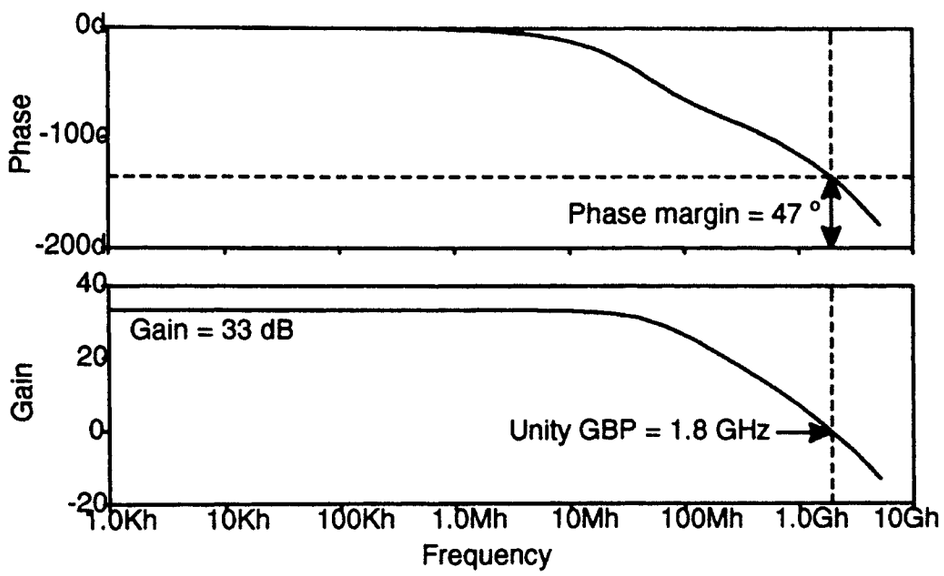

Figure 18. Open loop gain and phase response of folded cascode amplifier.

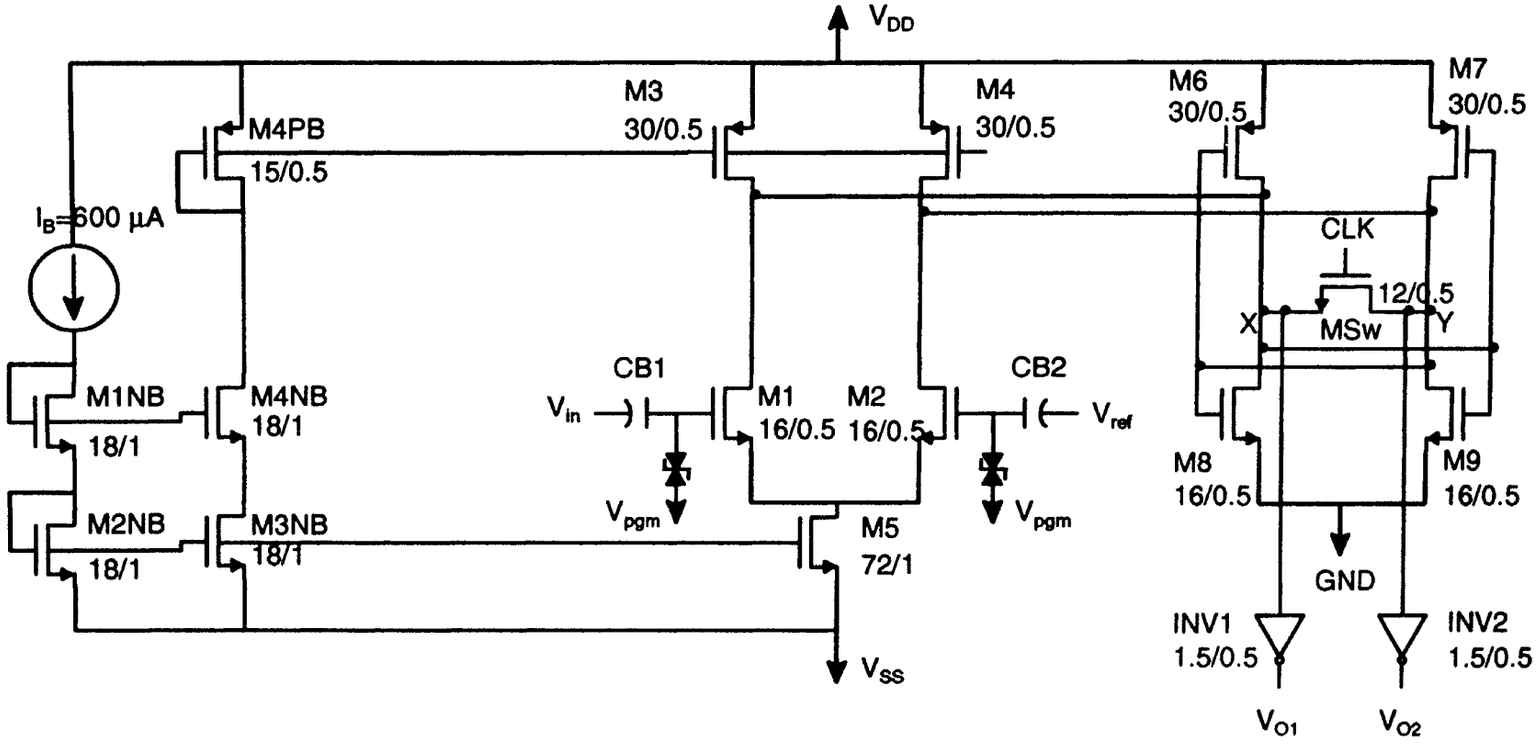

Figure 19. Dual differential regenerative comparator.

function. Inverters MI1, MI2 and MI3, MI4 are used to obtain the final logic levels and to protect the parasitic sensitive nodes of latch from external loading effects.

The dynamic operation of the circuit is divided into a reset time interval and regenerative time interval as shown in timing diagram of Figure 20. The two time intervals are between T1 and T2 and between T2 and T3 respectively. During the reset interval, the comparator is in the reset mode and current flows through the closed resetting switch MSw, which forces the previous two logic states to be equalized. After the preamplifier settles, a voltage proportional to the input voltage difference is established between nodes X and Y. This voltage will act as the initial imbalance for the regeneration time interval. The regeneration period is started by the opening of switch MSw. The p-channel cross pair M6 and M7 together with n-channel pair M8 and M9 regenerate the voltage differences between nodes X and Y to a voltage swing nearly equal to the power supply voltage.

3.4.1 Operating Analysis and Design Considerations

When the switch is on, the differential amplifier senses the input voltage difference and corresponding voltage difference is established between nodes X and Y. The bias circuit is used to set up the reference voltages for current source/sink and fix the reference current in the differential amplifier. As our goal is to design a comparator that has optimum comparison speed and high accuracy, the dimensions of all the transistors are chosen according to the constraints derived in the following sections.

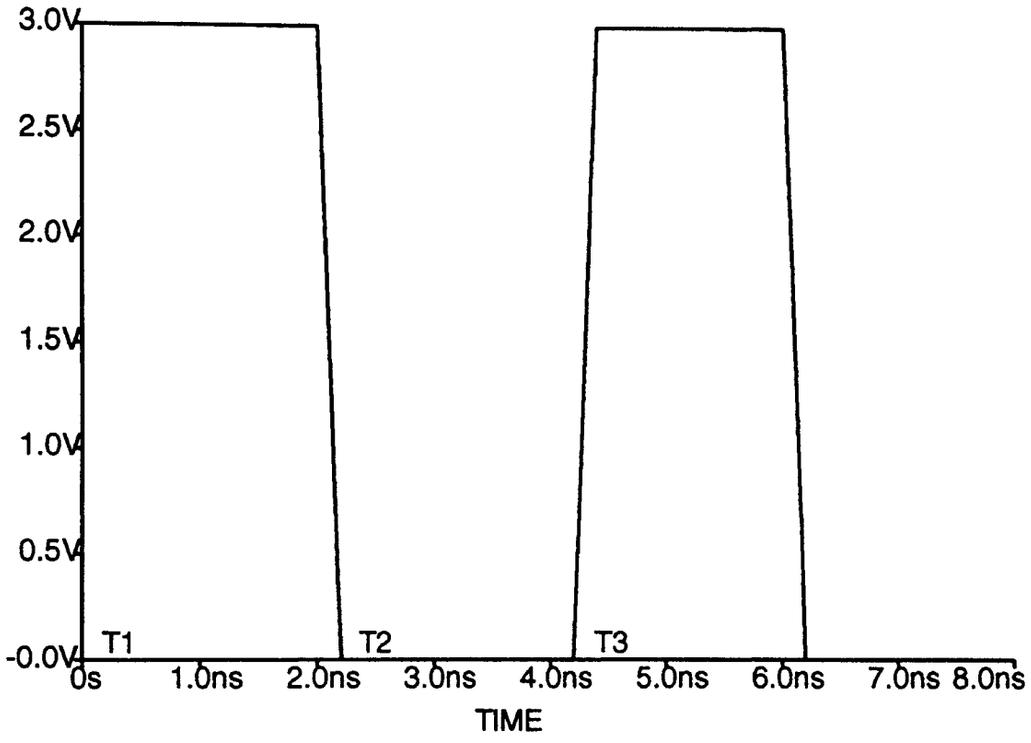

Figure 20. Timing diagram.

3.4.1.1 Resetting Process and Speed

The initial voltage difference, $V_x(0)$-$V_y(0)$ is very important in the decision of the regenerative direction. Imperfect resetting will cause hysterisis. The geometry of the switch should be carefully chosen to ensure the optimum resetting speed. As an example, assume that node X is at a high-voltage level before reset. As soon as the switch is closed, the voltage difference between nodes X and Y reduces very quickly but later the reduction slows down. It will have a local minimum at some instant if the current through switch MSw is equal to the current through M9, while M8 just reaches the edge of conduction, which should be avoided in high speed applications [26]. To ensure sufficient current to charge node Y, current through MSw should be greater than current through M9.

Hence,

$$I_{sw} > I_9 \tag{36}$$

As an example, assume that $V_x = 0.8$ V, $V_y = 0.7$ V, $V_{T(sw)} = 0.2$ V, $V_{clock} = 3$ V, $V_{T(M9)} = 0.17$ V, $V_{ss} = 0$ V, then MSw will be in linear region and M9 will be in saturation region, as given by:

$$\frac{K_n W_{sw}}{L}\left[\left(V_{clock} - V_y - V_{T(sw)}(V_x - V_y)\right) - 0.5(V_x - V_y)^2\right]$$

$$> \frac{K_n W_9}{2L}\left[V_x - V_{ss} - V_{T(M9)}\right]^2 \tag{37}$$

By substituting these values, we have,

$$W_{sw} > 0.7\ W_0 \tag{38}$$

The resetting speed can be derived using the small signal model as shown in Figure 21. In this equivalent circuit g_{mx} and g_{my} represent the total transconductance of M6 and M7 and M8 and M9 respectively. C_x and C_y represents the total capacitance at the nodes X and Y, this includes gate to source and drain to source capacitances of M6, M7, M8 and M9, gate to source and drain to source capacitances of MSw and drain to source capacitances of M3 and M4 and M1 and M2 and the gate to source capacitance of buffer inverters. The node equations at X and Y are given by:

$$C_x \frac{dV_x}{dt} + g_{mx}V_y + (V_x - V_y)\, g_{m(sw)} = 0 \tag{39}$$

$$C_y \frac{dV_y}{dt} + g_{my}V_x + (V_y - V_x)\, g_{m(sw)} = 0 \tag{40}$$

Assuming, $g_{mx} = g_{my} = g_m$, $C_x = C_y = C_o$,

Solving equations (39) and (40), we get, the reset time t_s,

$$t_s = \frac{C_o}{(g_m - 2g_{sw})} \ln \frac{V_x(t) - V_y(t)}{V_x(0) - V_y(0)} \tag{41}$$

$V_x(0)$-$V_y(0)$ is the initial voltage difference before resetting process starts and equal to 1.5 V and $V_x(t)$-$V_y(t)$ at the end of the process will be equal to $g_m/(g_{mx} + 2g_{m(Sw)})$ times of the input voltage difference. Equation (41) indicates that if $2g_{sw}$ is smaller than g_m it is impossible to reset the comparator. Hence the width of switch should be selected such that,

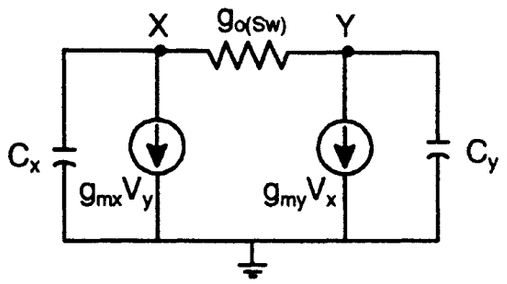

Figure 21. Small-signal model of the comparator.

$$g_{sw} > \frac{g_m}{2} \tag{42}$$

3.4.1.2 Regeneration Speed

While the clock starts falling, the conductance of switch decreases and the regeneration process begins when the transconductance of the switch becomes smaller than half of the transconductance of g_m. When the switch is off, g_{Sw} is zero, and the regeneration time t_r from the equation (41) is given by:

$$t_r = \frac{C_o}{g_m} \ln \frac{V_x(t) - V_y(t)}{V_x(0) - V_y(0)} \tag{43}$$

where $V_x(0)$-$V_y(0)$ is the initial voltage difference before regeneration process starts and equal to $g_{ml}/(g_{mx}+2g_{m(Sw)})$ of the input voltage difference. $V_x(t)$-$V_y(t)$ at the end of the process will be equal to the power supply voltage or approximately equal to 1.5 V.

3.4.2 Optimization Results

It is clear from the equation (43) that by making the switch small, regeneration time can be made faster while the upper limit is set by the constraints given by the equations (38) and (42). Hence W equal to 12 μm is chosen as an optimal choice between regeneration and reset speed. W/L ratios of the n-channel and p-channel transistors of latch are sized for equal pull-up and pull-down capability. Taking into account the load effect from the inverters and the mismatch from

transistor widths, W8 and W9 equal to 16 μm and W6 and W7 equal to 30 μm are chosen. The widths of inverter transistors are 1.5 μm.

Taking into account, the mismatch due to transistor widths, M1 and M2 are selected equal to 16 μm. I_B was chosen to have the overdrive voltage of differential pair equal to 0.6 V. Since drain to source capacitance of M3 and M4 contribute to the capacitance at X and Y, for a given I_B and node voltages at X and Y of $V_{DD}/2$ equal to 0.75 V during reset, the minimum widths of 30 μm for M3 and M4 are chosen to keep them in saturation. The choice of overdrive voltage is a trade off between maximum headroom, breakdown voltage and maximum g_m. The bias current can be increased to some extent to raise the comparison speed at the expense of power dissipation.

For the above dimensions the total parasitic capacitance and total transconductance at node X will be approximately equal to 150 ffd and 5.6 mmho respectively (from simulations). Assuming that regeneration time and reset time are equal, the total time taken for the conversion is equal to approximately 465 ps from equation (43). The theoretical conversion time is equal to 360 ps (see equation (14), it is assumed that process f_T is lowered by approximately 3 times due to the additional parasitic capacitances).

3.4.3 Simulation Results

The circuit shown in Figure 21 was simulated using fully depleted thin-film SOI MOSFET models in SOISPICE. The SPICE simulations of the transient characteristic are shown in Figure 22. When clock goes high at t equal to 2 ns, the preamplifier senses the analog input and amplifies the difference, thus generating a differential voltage at X and Y. At t equal to 4 ns, clock goes low to strobe the latch, thereby regeneratively amplifying the small difference at V_x

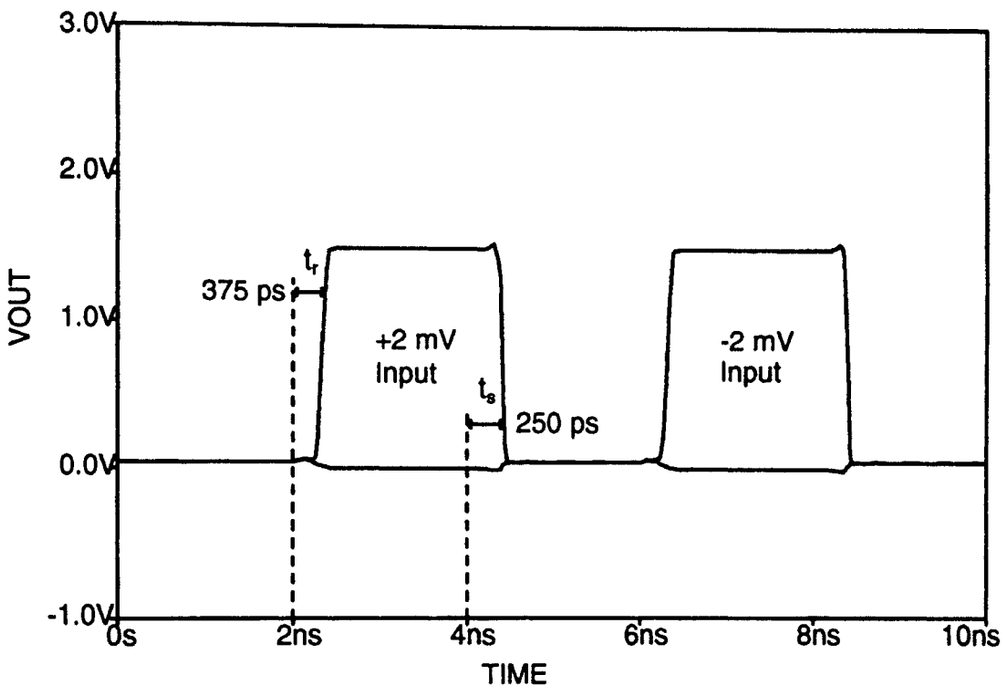

Figure 22. Transient response of the regenerative comparator.

and V_y to a level approaching the power supply voltage. From simulation the regeneration time was found to be 375 ps and reset time was found to be 250 ps with the clock of 0.2 ns rise and fall time. The response corresponds to input voltage of 2 mV (1/2 LSB). Approximately 625 ps is required to achieve the comparison.

3.4.4 Layout Considerations

Any mismatch between M1 and M2, M3 and M4, M8 and M9 and M10 and M11 (across X and Y nodes of the latch) may result in a false output. Hence latch should be symmetrical. Therefore the layout process should be carried out very very carefully to preserve the matching properties of the devices and to minimize the parasitic capacitances. The most common ways in which layout influences matching are through device proximity and device orientation. Matching of components is degraded by placing them apart. Therefore two devices intended to match should be placed in close proximity, decreasing their mismatch.

One technique for improving the matching devices is called the "common centriod" layout style. Both differential pair and the p-channel and n-channel pair of latch are laid out using this technique, each transistor has been divided into eight fingers and grouped into transistors of four fingers each, and then laid out in a common centriod fashion. Dividing transistors into eight diminish the sensitivity of mismatch to quadratic spatial variations in the process parameters [9].

Any sufficiently large parasitic capacitance mismatch between nodes X and Y of the latch leads to an erroneous result due to charge injection and clock feedthrough error of switch MSw. To guarantee that two parts of the symmetric circuit match all the wires on each side must contain the same length at each wiring layer and have the same exact crossings with other devices or wires. The whole latch structure is laid out symmetrically, the left part of the latch circuit is just

the mirror image of the right part (see Figure 23). This eliminates the dynamic offset errors.

It is also necessary to pay extreme attention to prevent the noisy interaction of analog circuit (preamplifier) and digital circuit (latch). Since the gate of the switch in the comparator is driven by the digital signal (clock) while the source and drain are connected to analog nodes. The steps taken to prevent the interaction of analog and digital circuits were discussed in detail in section 2.4.

Despite all the precautions taken in designing and laying out the circuit, the comparator will still have the offset voltage due to the parametric mismatch in the transconductance, parasitic capacitance, threshold voltage caused by imperfections in the process and due to the random errors. Small imbalances in the charge injection error and clock feedthrough error or any noise would lead to an input referred offset voltage. As the latch is very sensitive to the imbalance, the offset voltage has to be trimmed for static offset voltage in order to prevent the circuit to amplify the input signal in the wrong direction. Hence the circuits are trimmed using Fowler-Nordheim trimming method to eliminate static mismatch. The trimming removes the static offset of both the latch and the effective offset associated with the buffer chain.

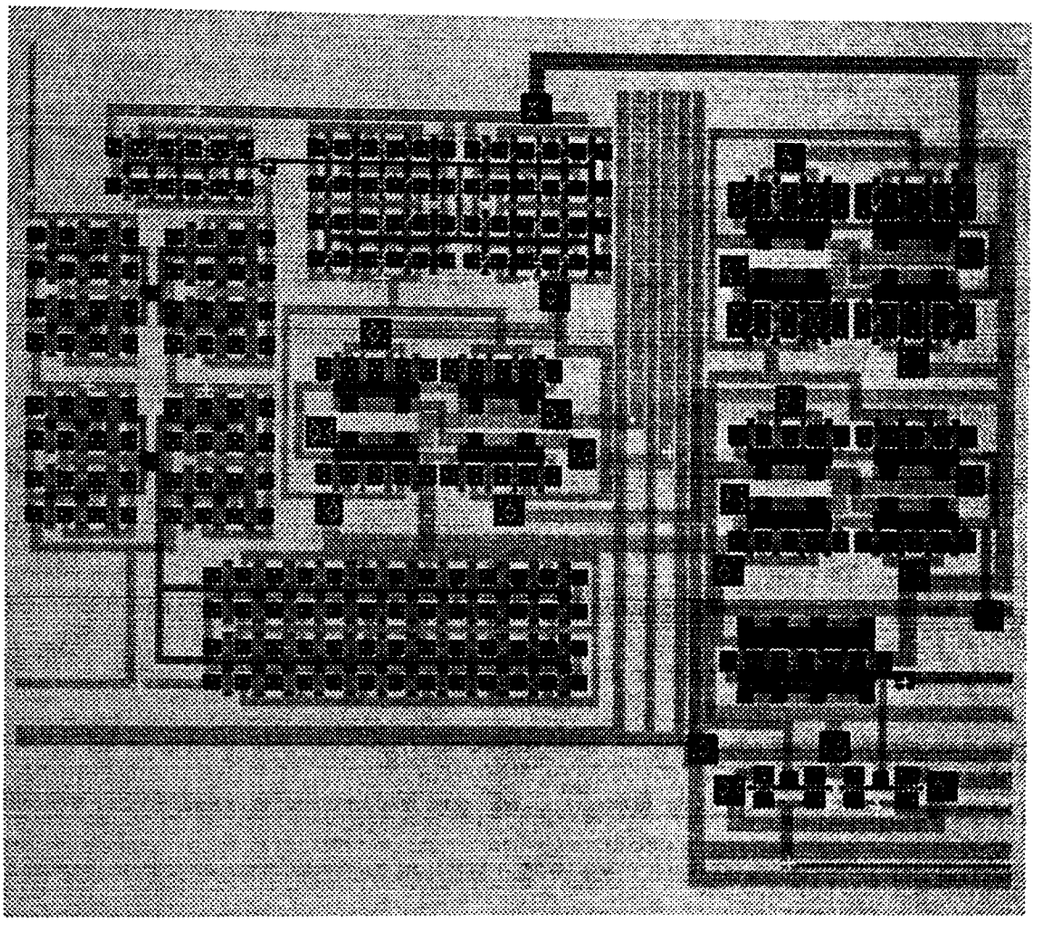

Figure 23. Layout of the regenerative comparator.

CHAPTER IV

RESULTS AND CONCLUSIONS

Three possible 10 bit high-speed two-step ADC architectures were studied and the total conversion time for each architecture was derived for a given process as a function of gain bandwidth product. The comparison shows that high speed with greater accuracy can be achieved by using subranging architecture with partial residual scaling. The new architecture was developed as necessary to achieve the goal of 10 bit 2.5 GHz conversion rate. The simulated and theoretical (ignoring C_{DS} and C_{GD}) conversion time required for each of the building blocks are tabulated in Table I. The tabulation of the above time delays from coarse comparator to residual summing node, through the cascode buffer chain and finally the settling of the fine comparator results in a projected delay from simulation is 1071 ps or an effective ADC conversion rate less than 1 GHz compared to a theoretical delay of 2 GHz. However, by pipelining the two stages the effective throughput can be increased to 1 GHz suggested as future work. All simulation results are based on the models supplied by IBM which are 1.5 times slower than original proposed models. However, theoretical calculations using f_T equal to 20 GHz and ignoring C_{DS} shows that a conversion rate of 2 GHz can be achieved (see Table I). This suggests that better SOI devices are required to achieve our objective. Table II shows the performance summary of the proposed ADC architecture.

By reevaluating the theoretical performance of Table I and including C_{DS} approximately equal to $C_{GS}/2$ (obtained from SOISPICE output file) in the performance equations (8) and (14), the observed shortcomings are accounted for in the following manner;

• Coarse comparator delay becomes 230 ps.

• Buffer chain non dominant pole (g_m/C_p) is 3.5 ω_T where C_p is the parasitic capacitance at the source of the cascoded transistor rather than predicted differential to single-sided mirror. Delay now becomes 150 ps.

• Fine comparator performance becomes 360 ps where reset time has been assumed to be equal to regeneration time.

The preceding discussion serves to point out that for SOI processes in general the relative values of C_{DS} to C_{GS} can be a significant factor in high performance considerations. In the future the success or failure of the winning TFSOI process i.e., BESOI, SIMOX and SOS must include considerations for C_{DS} as well as f_T, self gain μ, C_{GD} and thermal effects. Although C_{GD} is not taken into consideration, it is not negligible and can also contribute appreciably to the performance delay.

The success of our proposed architecture as explained previously depends on the availability of accurate resistors R_{SET} and R_{SUM}. The concept of floating memory for analog applications, in particular for trimming the offsets is relatively new and needs further studies. Fowler-Nordheim mechanism is poorly understood; it is believed that there is another mechanism which is responsible for injection and removal of electrons [6]. The improvement of floating gate process with respect to trap density should be made to reduce the initial and long term drift. The initial degradation of the retention characteristics due to the trapped charge in the interface of Si-Sio_2 of the floating gate memory for digital applications is not a serious problem where only logic levels are required, however for analog applications, the resolution will be directly affected by the

initial and long term drift [12]. Hence future development in floating gate analog memories have to be followed closely to be adopted for our design.

The following suggestions provide the future scope that will help in realizing the complete ADC architecture.

• A wide band and fast Sample/Hold circuit has to be developed. In addition, the circuit should have high noise immunity and low offset voltage.

• The multistage comparator was designed for β ratio of one; i.e., width of p device is approximately twice that of n device. This in turn increases layout area and dynamic power dissipation. Since the delay response of an inverter pair for β ratio of one and equal sized p and n transistors is similar, it is preferable to use equal sized p and n channel transistors when similar structures are cascoded [21]. The widths of transistors are three times larger than minimum size. These transistors can be made smaller. This in turn reduces C_{DS} and improves the performance slightly.

• The current DAC design has to be verified using simulation and fabricated.

• A fast V-I Converter has to be designed which has a conversion time of less than the combined conversion time of coarse stage and the DAC.

• A folded cascode amplifier used as an integral part of the buffer chain should be redesigned with the input capacitance of 32 ffd and an open loop gain greater than or equal to 46 dB to keep the errors at its minimum.

• A method should be investigated to pipeline two stages of conversion process.

Even with the above modifications the keys to success 10-bit 2.5 GHz ADC are: accurate Fowler-Nordheim trimming, improved SOI devices and a fast S/H circuit.

TABLE I

Performance summary of the building blocks of the proposed ADC

Building blocks	Conversion time (ps) (Simulation)	Conversion time (ps) (Theoretical with f_T = 20 GHz)
Coarse comparator	250	115
DAC	35	39
Buffer chain	161	86
Fine comparator	625	360
Total conversion time	1071	600

TABLE II

Proposed ADC features

Summary	
Technology	0.25 μm CMOS/TFSOI
Power supply	± 1.5 V
Resolution	10 bits
Linearity	± 1/2 LSB
Conversion time	1 Gsamples/s

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