DEVELOPMENT OF HIGH PERFORMANCE CMOS AMPLIFIERS USING SHORT CHANNEL THIN FILM SILICON ON INSULATOR DEVICES

By

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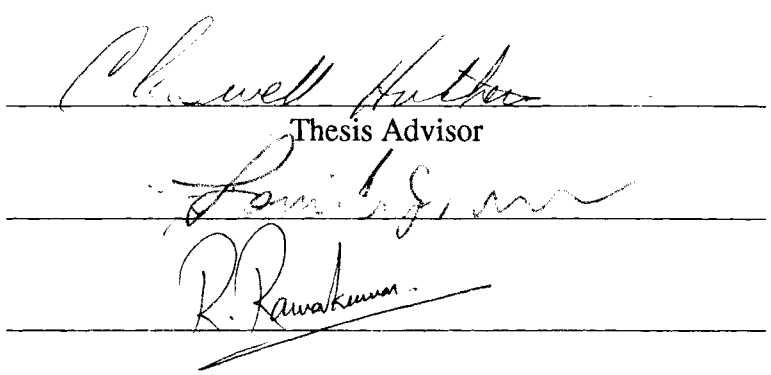

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PREFACE

Fully differential topologies offer good performance in signal processing due to the cancellation of common mode signals such as clock feedthrough and power supply noises etc. This work specifically aimed at developing fully differential high performance amplifiers to be used in high frequency, high resolution Analog to Digital Converters. Combining a novel circuit design approach with the extension of previously reported circuit design techniques has resulted in high performance amplifiers with unprecented figures of merit. Simplification of existing circuit analysis techniques has been another accomplishment of this work. Major performance gain has come from technology advancement but it must be properly exploited with appropriate circuit design methods as documented in this thesis.

I wish to express my sincere appreciation to my major advisor, Dr. Chriswell Hutchens for his intelligent supervision, constructive guidance and sporting attitude. My appreciation extends to my other committee members Dr. R. Ramakumar and Dr. L.G. Johnson. I sincerely thank the Naval Ocean Surveillance Command (NOSC), San Diego for providing financial support to this project and excellent work experience.

I also would like to express my gratitude to my colleagues at Oklahoma State University and my old EE and TX pals from IIT Delhi for fond memories.

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NOMENCLATURE

SOI	Silicon on Insulator
f_T, ω_u	Unity Gain Frequency
L_{eff}	Effective Channel Length of the Transistor
μ	Transistor Self Gain
g_m	Transistor transconductance
r, r_{ds}, r_o	Transistor output resistance (unless noted otherwise)
C_{gs}	Gate to Source Capacitance of the Transistor
C_{gd}	Gate to Drain Capacitance of the Transistor
ADC	Analog to Digital Converter
PSRG	Power Supply Ripple Gain
A_v	DC Gain
R_D	Drain Resistance of the transistor
R_S	Source Resistance of the transistor
V_{DD}	Drain Power Supply Voltage
V_{SS}	Source Power Supply Voltage
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio

GBP	Gain Bandwidth Product
SOISPICE	A Circuit Simulator for SOI Circuits
GSPS	Giga Samples Per Second
KSPS	Kilo Samples Per Second
R_g	Gate Resistance
C_g	Gate Capacitance
A_{VOL}	Open Loop DC Gain
UGBP	Unity Gain Bandwidth Product
V_{os}	Offset Voltage
W/L	Width to Length Ratio for the Transistor
V_{bi}	Bias Voltages
V_{GS}	Gate to Source Voltage for the Transistor
V_{DS}	Drain to Source Voltage for the Transistor

CHAPTER 1

INTRODUCTION

Recent advances in the fabrication technology of thin film short channel Silicon on Insulator (SOI) devices, prompted by the fundamental advantages of dielectric isolation along with very high frequency unity gain frequencies have stimulated an interest in the development of high performance CMOS circuits which can operate in the microwave range. These devices with L_{eff} = 0.25μm, typically have an f_T in excess of 30 GHz. These SOI MOSFETs are different from conventional bulk MOSFETs because the *body is thin and floating,* and the underlying (substrate) oxide is thin enough to enable an *effective back gate.* These differences make SOI device behave in a different way which calls for a different design approach. The most important being the "kink" effect which occurs at high drain to source voltages, V_{DS}. Also, due to a very short channel length the intrinsic self gain of the transistor, μ, of the transistor is very small (of the order of 20-25dB only) as compared to 40-50dB in a long channel bulk MOSFET. This calls for use of gain enhancement techniques in the deign of short channel MOS circuits. The "kink" effect suppression calls

for a low voltage operation and finally high frequency operation is possible if the additional parasitics in the circuit are kept to a minimum. This is accomplished by elimination of the common mode feedback circuitry in the fully differential opamp configurations. A very important advantage of these devices is the elimination of junction capacitances at the source and drain of the transistor because there is no semi-conducting substrate. Thus, this work aims at developing high performance amplifiers which make use of the advantages of these devices and at the same time using novel design approaches to overcome the problems faced by short channel MOS design. New circuit design techniques preserve the advantages of the previously reported works and eliminate the disadvantages to give an opamp with a very high differential mode gain and a very low common mode gain and a very high unity gain frequency and low power supply ripple gain. These amplifiers drive large loads due to low noise floor required by the A/D conversion applications for which they are designed. Also, dynamic biasing and subthreshold operation techniques are used to develop an amplifier with a very low quiescent power dissipation. Some previously published analyses has been presented in a simplified form and important issues are brought to the attention of the interested reader. To ensure best matching in the fabricated devices and ensure high frequency operation, the layout techniques used form an important part of this work.

The rest of this thesis is organized as follows: In chapter 2, characteristics of thin film short channel devices are presented. In chapter 3, various design techniques developed and used for design of high performance amplifiers are discussed. Chapters 4 and 5 describe the architecture and performance of the amplifiers. Finally, Chapter 6 discusses the accomplishments of this work and makes suggestions for future research.

CHAPTER 2

CHARACTERISTICS OF SHORT CHANNEL THIN FILM SOI DEVICES

In this chapter, the unique characteristics of short channel thin film, fully depleted SOI devices are presented and analyzed briefly. These characteristics include the charge coupling between the front and the back gate of the SOI MOSFET and it's impact on threshold voltage. Further, effects of small geometry on device performance such as drain induced conductivity enhancement, charge sharing, back surface charge modulation etc. are presented. Then the very important "kink" feature of thin film SOI devices is discussed, and using a charge based representation, I-V characteristics are derived for a SOI MOSFET. This chapter is just a brief overview of the detailed analysis carried out in [1] through [7].

2.1 **Threshold voltage analysis**

Fig. 2.1 shows a thin film SOI MOSFET. Because SOI films are thin, the electrical properties of MOSFET's fabricated in them are typically influenced by the charge coupling between the front and back gates. The (front gate) threshold voltage differs considerably from that of its bulk counterpart and depends on the bias and the properties of the back gate.

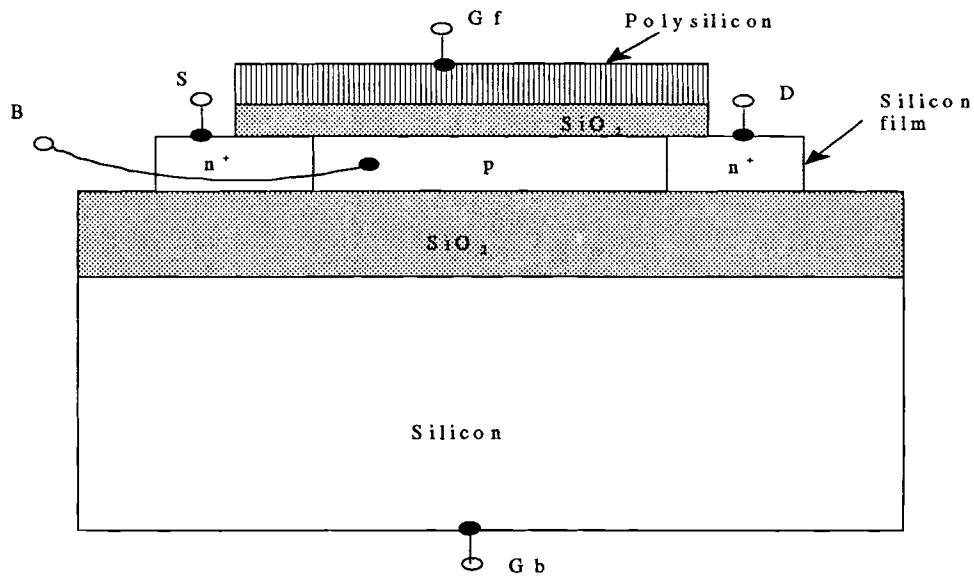

Fig 2.1 Cross sectional view of a generic n-channel SOI MOSFET

The front Ψ_{sf} and the back Ψ_{sb} surface potentials are the band bending potentials from a hypothetical neutral film body to the respective surface. The electrostatic potential at this point, if the source is grounded, is just the built in potential of the source body film junction. Thus, we can write

$$V_{Gf} = \Psi_{sf} + \Psi_{of} + \Phi^{f}_{MS} \tag{1}$$

and

$$V_{Gb} = \Psi_{sb} + \Psi_{ob} + \Phi^{b}_{MS} \tag{2}$$

where V_{Gf} and V_{Gb} are the front and back gate voltages, Ψ_{of} and Ψ_{ob} are the potential drops across the front and back gate oxides, and Φ^f_{MS} and Φ^f_{MS} are the front and back gate body work function differences. Solving the Poisson's equation across the film and applying Gauss's Law to the front and back surfaces the following expressions can be derived.

$$V_{Gf} = V^f_{FB} + (1 + \frac{C_b}{C_{of}})\Psi_{sf} - \frac{C_b}{C_{of}}\Psi_{sb} - \frac{Q_b/2 + Q_{cf}}{C_{of}} \qquad (3)$$

where $V^f_{FB} = \Phi^f_{MS} - Q_{ff}/C_{of}$ is the front gate (bulk MOSFET) flatband voltage, $C_b = \epsilon_s/t_b$ is the depletion capacitance, and $Q_b = -qN_At_b$ is the depletion region area charge density. Similarly,

$$V_{Gb} = V^b_{FB} - \frac{C_b}{C_{ob}}\Psi_{sf} + (1 + \frac{C_b + C_{sb}}{C_{ob}})\Psi_{sb} - \frac{Q_b/2 + Q_{cb}}{c_{ob}} \qquad (4)$$

where $V^f_{FB} = \Psi^f_{MS} - Q_{ff}/C_{ob}$ is the back gate (bulk MOSFET) flatband voltage. Q_{cf} and Q_{cb} are the charges associated with front and back gate oxides. Equations (3) and (4) are the key relations that describe the charge coupling between the front and the back gates when the film body is completely depleted. Combining them leads to the description of the (front gate) threshold voltage in terms of the back gate bias V_{Gb} and device parameters.

When the back surface is depleted, Ψ_{sb} is strongly dependent on V_{Gb} ; its value ranges from about zero to $2\Phi_B$ between the onset of accumulation and inversion respectively. The values of V_{Gb} (V^A_{Gb} and V^I_{Gb}) corresponding to this onset when the front surface is inverted ($\Psi_{sf} \simeq 2\Phi_B$) are defined as :

$$V_{Gb}^{I} \simeq V_{FB}^{b} + \left(1 + \frac{C_{sb}}{C_{ob}}\right) 2\Phi_B - \frac{Q_b}{2C_{ob}} \tag{5}$$

$$V_{Gb}^{A} \simeq V_{FB}^{f} - \frac{C_b}{C_{ob}} 2\Phi_B - \frac{Q_b}{2C_{ob}} \tag{6}$$

The dependence of V_{Tf} on V_{Gb} for $V^{A}_{Gb} < V_{Gb} < V^{I}_{Gb}$ is obtained as in [1]:

$$V_{Tf} \simeq V_{Tf}^{A} - \frac{C_b C_{ob}}{C_{of}\,(C_b + C_{ob} + C_{sb})}\,(V_{Gb} - V_{Gb}^{A}) \tag{7a}$$

$$\simeq V_{Tf}^{I} - \frac{C_b C_{ob}}{C_{of}\,(C_b + C_{ob} + C_{sb})}\,(V_{Gb} - V_{Gb}^{I}) \tag{7b}$$

where,

$$V_{Tf}^{I} = V_{FB}^{f} + 2\Phi_B - \frac{Q_b}{2C_{of}} \tag{8}$$

$$V_{Tf}^{A} = V_{FB}^{f} + \left(1 + \frac{C_b}{C_{of}}\right) 2\Phi_B - \frac{Q_b}{2C_{of}} \tag{9}$$

Thus, as V_{Gb} increases from V^{A}_{Gb} to V^{I}_{Gb} (an increase of $2\Phi_B(1 + (C_b + C_{sb})/(C_{ob})$), V_{Tf} decreases linearly with V_{Gb} from V^{A}_{Tf} to V^{I}_{Tf} (a decrease of $2\Phi_B(C_b/C_{of})$).

2. 2 Short Channel Effects

2.2.1 *Charge Sharing*

The (front channel) threshold voltage V_{Tf}, defined for low drain voltage - source voltage V_{DS}, is reduced in short channel MOSFET's because some of the depletion charge under the gate is shared by the source and the drain. In the SOI devices this sharing is influenced by the coupling between the front and back gates.

In strong inversion, the film is assumed to be completely depleted, except for sheets of surface charge, Q_{cf0} and Q_{cb0}, at the front and front and back gate surfaces respectively. (The subscripts f and b refer to the front and back surfaces respectively, and the subscript 0 refers to the solution for $V_{DS} = 0$). The potential of the front surface Ψ_{sf0} is approximately constant between the source and the drain and is given by $\Psi_I \sim 2\Phi_B$, where Φ_B is the Fermi potential of the neutral film, to which all the potentials are referenced.)

The depletion charge may be regionally divided into three portions as shown in Fig. 2.2 , associated with the gate, source and drain.

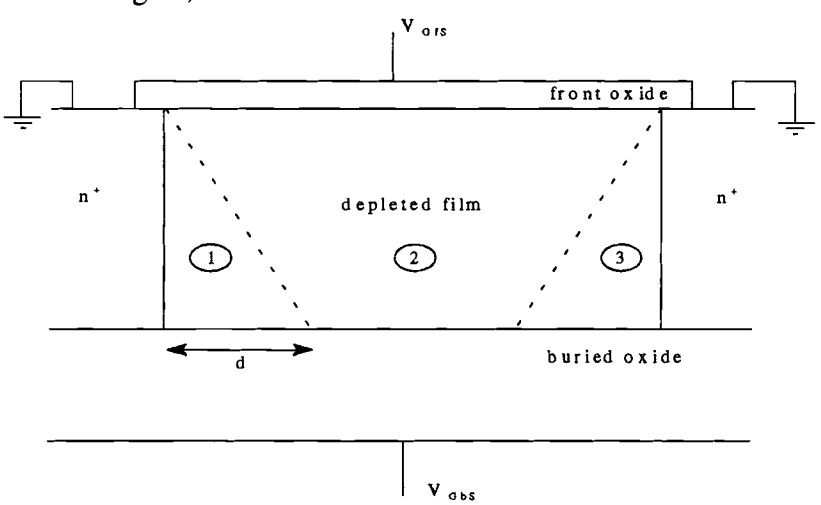

Fig. 2.2 A simple charge sharing model for thin film SOI MOSFET. The portions 1, 2 and 3 "controlled" by the gates, source and drain.

The portion 1, which is controlled by the front and back gates, is defined approximately by a trapezoid, and hence the depletion charge per unit area controlled by the gates is

$$Q_{b(eff)} = -qN_A t_b\left(1 - \frac{d}{L}\right) \triangleq Q_b\left(1 - \frac{d}{L}\right) \tag{10}$$

where t_b is the film thickness and L is the channel length of the MOSFET. The one dimensional Poisson's equation can be then solved to give:

$$Q_{cf0} = -C_{of}\left[V_{GfS} - V_{FB}^{f} - \left(1 + \frac{C_b}{C_{ob}}\right)\Psi_{sfo} + \frac{C_b}{C_{of}}\Psi_{sbo} + \frac{Q_{b(eff)}}{2C_{of}}\right] \tag{11}$$

and

$$Q_{cb0} = -C_{ob}\left[V_{GbS} - V_{Fb}^{f} - \left(1 + \frac{C_b}{C_{ob}}\right)\Psi_{sb0} + \frac{C_b}{C_{ob}}\Psi_{sf0} + \frac{Q_{b(eff)}}{2C_{ob}}\right] \tag{12}$$

where $C_b = \epsilon_s / t_b$, $C_{of} = \epsilon_{ox} / t_{of}$, and $C_{ob} = \epsilon_{ox} / t_{ob}$ are the front and back (buried) oxide capacitances per unit area, and V^f_{FB} and V^f_{FB} are the front- and back gate flatband voltages. (The quantities t_{of} and t_{ob} are the thicknesses of the front and back oxides.)

To characterize V_{Tf} , the distance d must be analytically approximated. This is done by following analysis to account for the two dimensional electric field near the back surface in portions 2 and 3. The effective lateral component of the electric field , $E_{b(eff)}$, at the back interface is approximated as

$$E_{b(eff)} = \sqrt{\frac{qN_A(V_{bi} - \Psi_{sb0})}{2\epsilon_s}} + f_\alpha \frac{\epsilon_{ox}}{\epsilon_s} \frac{V_{GbS} - V_{FB}^b - \Psi_{sb0}}{t_{ob}} + f_\beta \frac{\epsilon_{ox}}{\epsilon_s} \frac{V_{bi} - V_{GbS} + V_{FB}^b}{t_{ob}} \qquad (13)$$

where the first term is due to the depletion charge and the second and third terms are due to fringing fields from portion 1 and the source to the back gate. f_α and f_β , are empirical factors between 0 and 1 and can be obtained by curve fitting the V_{Tf} data.

Now,

$$d \simeq \frac{(V_{bi} - \Psi_{sb0})}{E_{b(eff)}} \qquad (14)$$

When the back gate is biased to accumulate the back surface, $Q_{cb0} > 0$ and $\Psi_{sbo}=V_{BS}$, the body to source voltage. Then in strong inversion, with $\Psi_{sf0} = \Psi_I$, combining (10) through (14) yields

$$Q_{cf0} = - C_{of} (V_{GfS} - V_{Tf}) \qquad (15)$$

where V_{Tf} depends on L as well as V_{BS} and V_{GbS} as derived earlier. The back surface accumulation charge Q_{cb0} is also simultaneously defined by (10) through (14).

When V_{GbS} is set to deplete the back surface, $Q_{cb0} = 0$ and $\Psi_{sb0} > V_{BS}$ is unknown. In this case (10) through (14) give a polynomial equation which must be solved to determine Ψ_{sb0} , which when inserted into (11), defines Q_{cf0} and V_{Tf} . In the model, Ψ_{sb0} is determined by a simple iterative scheme: (i) assuming no charge sharing, calculate Ψ_{sb0} from (12); (ii) use that value successively in (13), (14) and (10) to determine $Q_{b(eff)}$; (iii) use (12) to

determine a modified value for Ψ_{sb0}. Steps (i), (ii) and (iii) are repeated until the solution converges, which in fact, occurs only in few iterations [6].

2.2.2 *Drain Induced Conductivity Enhancement*

When a large (positive) drain voltage V_{DS}, is applied to a short N channel MOSFET, the channel charge is modulated indirectly through the two dimensional electric field in the film, as well as directly through the induced gradient in the surface potential ψ_{sf} along the channel. In [2], the charge at the source end of the channel is expressed as

$$Q_{cf}(0) = -C_{of}\left(V_{GfS} - V_{Tf} + \beta\frac{\epsilon}{C_{of}}\frac{t_b}{L^2}V_{DS}\right) \tag{16a}$$

$$\approx -C_{of}\left(V_{GfS} - V_{T(eff)}\right) \tag{16b}$$

where $\beta = 1$ or $1 + C_b/(C_b+C_{ob})$, depending upon whether the back surface is accumulated or depleted. $C_{ob} = \epsilon_s/t_b$ is defined as the body capacitance, and $V_{T(eff)}$ is defined as an effective threshold voltage. For a given drain bias, the difference between V_{TF} and $V_{T(eff)}$ is a measure of the modulation of the charge at source due to the two dimensional electric field in the film i.e. due to DICE. We note, therefore, from (16) that the characterization of the channel charge and hence the device conductance deviate from the gradual channel approximation as β increases, or as back surface goes from accumulation to depletion. Also, it is obvious from (16) that two dimensional DICE effect is diminished as t_b decreases.

2.2.3 *Carrier Velocity-Field model*

In the saturation region of operation of a MOSFET, the drain current $I_{DS(sat)}$ and the incremental drain conductance $g_{DS(sat)}$ depend on the manner in which the carrier velocity saturates. This velocity saturation and the channel length modulation it produces are important in short channel devices because the channel charge that remains near the drain in the saturation region is proportional to $I_{DS(sat)}$, which varies inversely with L. For SOI MOSFETs, there are additional dependences on the back surface charge condition and on film thickness, t_b. Due to high transverse electric filed in the thin SOI film, as well as high longitudinal electric field in the short channel, there can be considerable non linearity in the carrier velocity and in the carrier velocity field characteristic. For an increasing longitudinal field $|E_y| \equiv d\Psi_{sf}/dy$ in the channel, the velocity tends to saturate (at $v_{sat} \approx 10^7$ cm/s) [6]. A piece wise continuous model for velocity saturation is used.

$$v(y) = \frac{\mu_{eff}\,|E_y|}{1 + \dfrac{\mu_{eff}\,|E_y|}{2v_{sat}}} \qquad (17)$$

$$= v_{sat}, \quad \text{if } v(y) > v_{sat}$$

Thus, we have

$$\mu_{eff} = \frac{\mu_{n0}}{1 + \theta\, E_x(y)} \qquad (18)$$

where μ_{eff} is the low-(longitudinal)-field mobility. This dependence along the channel is modeled in terms of the average $E_x(y)$ in the channel. θ is an empirical constant. From $V_{DS} = 0$ solution and the DICE analysis, the average transverse field in the channel is expressed as in [1]

$$E_x(y) = \frac{C_{of}}{2\epsilon_s}\left[V_{GfS} - V_{Tf} - \frac{Q_{b(eff)}}{C_{of}} + 2\frac{C_{ob}}{C_{of}}(\Psi_I - \Psi_{sb0}) + \beta\frac{C_b}{C_{of}}\left[\frac{t_b}{L}\right]^2 V_{DS} - (1 - \alpha)\Delta\Psi_{sf}(y)\right] \quad (19)$$

Thus, we can write

$$\mu_{eff} = \frac{\mu}{1 - B\,\Delta\Psi_{sf}(y)} \quad (20)$$

where newly defined parameters μ and B are bias dependent but spatially constant [1].

2.3 Back Surface Charge Modulation

In all the previous analysis, it has been assumed that back surface charge condition depends only on the applied biases V_{BS} and V_{GbS}. However, in general the back surface charge condition is also dependent on L. It is possible with $_{fixed,\ VBS}$ and V_{GbS} for a back surface accumulation layer present in a long channel SOI MOSFET to be partially or completely depleted away by a sufficient reduction in L. This depletion charge sharing effect occurs exclusively in SOI MOSFETs and is discussed in greater detail in [2]. Similarly, any accumulation layer present as the back surface, for a given device, can be partially or fully depleted away by a non zero V_{DS}. This effect is present in long channel

devices also but is more pronounced in short channel devices due to two dimensional field distribution.

2.4 Triode Region Current

The steady state channel current is

$$I_{DS} = - W\, Q_{cf}(y)\, v(y) \tag{21}$$

Using the models in section 2.2 and carrying out required mathematics the voltage dependence of I_{DS} is derived to be (as in [6])

$$I_{DS} = \frac{W\, \mu_{eff} \left(Q_{cf}^2(0) - Q_{cf}^2(L) \right)}{2C_{of}\,(1 + \alpha)\, L \left(1 + \left(\frac{\mu_{eff}}{2\, v_{sat} L} \right) V_{DS} \right)} \tag{22}$$

where μ_{eff} is defined as:

$$\mu_{eff} \triangleq \frac{\mu}{1 - f_B\, BV_{DS}} \tag{23}$$

where f_B is an empirical constant.

2.4 Saturation Region Current

In the saturation region operation of the MOSFET, a high longitudinal electric field

occurs near the drain, causing the carrier velocity to saturate at v_{sat}. Thus, the channel current can be expressed as

$$I_{DS(sat)} = - W Q_{cf} (L_e) v_{sat} \quad (24)$$

where $L_e \leq L$ due to channel length modulation. For long channel devices, it implies that $Q_{cf}(L) \approx 0$, which is the basis for pinch off model for saturation characteristics.

2.4.1 *Saturated drain Current*

In the saturation region, the channel maybe divided into a portion (adjacent to the source) in which the carrier velocity is field-dependent and another (near drain) in which the velocity is saturated. At the boundary between the two portions, $y = L_e$, we can define $V_{DS(eff)} \triangleq \Delta\Psi_{sf}(L_e)$ ($\leq V_{DS}$). At the onset of operation in the saturation region, $L_e = L$ and $V_{DS(eff)} = V_{DS(sat)}$, where $V_{DS(sat)}$ is the actual drain saturation voltage.

In the region $0 \leq y \leq L_e$ with L and V_{DS} replaced by L_e and $V_{DS(seff)}$, (24) expresses $I_{DS(sat)}$. This expression equated to (22) gives $V_{DS(eff)}$ as a function of L_e. Then $I_{DS(sat)}$ is fully characterized by (22) or (24) except for the description of L_e which is derived in the next section.

2.4.2 *Channel Length Modulation*

Channel length modulation, which is reflected by finite output conductance in the saturation region, is quantitatively defined as $L_d \triangleq L - L_e$, the length of the portion of the

channel in which the carrier velocity is saturated. In the region $0 \le y \le L_e$ with L and V_{DS} replaced by L_e and $V_{DS(eff)}$, (24) expresses $I_{DS(sat)}$. This expression equated to (22) gives $V_{DS(eff)}$ as function of L_e.

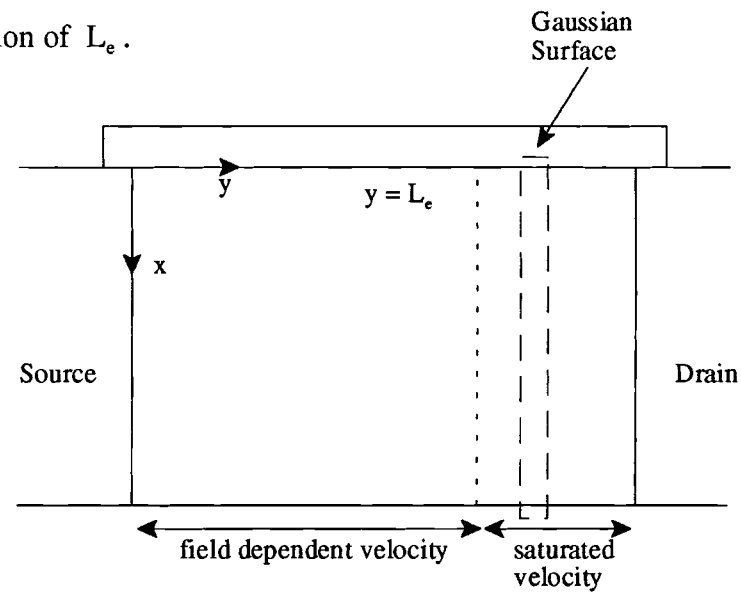

Fig. 2.3 Schematic cross section along the length of the channel when the SOI MOSFET is in saturation, showing the field-dependent and saturated-velocity regions.

Fig. 2.3 shows a cross section of the high field region near the drain of an SOI MOSFET in saturation. Since, the carrier velocity in the region is saturated, the continuity of current in steady state implies that $Q_{cf}(y)$ is spatially constant in the region. To derive a differential equation in $\Delta\Psi_{sf}(y)$, Gauss's law is applied to a narrow strip in the region as shown in the figure:

$$\epsilon_s \frac{d^2}{dy^2}\left[\int_0^{t_b} \Delta\Psi\, dx\right] = C_{of}\,\Delta\Psi_{sf} + C_{ob}\,\Delta\Psi_{sb} - \Delta Q_{of} - \Delta Q_{ob} \qquad (26)$$

Following the quasi two-dimensional DICE analysis earlier and using the conditions that $\Delta Q_{cb} = 0$ when the back surface is depleted or $\Delta \Psi_{sb} = 0$ when the back surface is accumulated a differential equation in $\Delta \Psi_{sf}$ (y) is obtained which can be solved with the appropriate boundary conditions to yield

$$L - L_e = L_d \sim l_c \sinh^{-1} \left[\frac{\mu_{eff} \left(V_{DS} - V_{DS(eff)} \right)}{2 v_{sat} \, l_c} \right] \tag{27}$$

where

$$l_c \Delta t_b \sqrt{\frac{C_b \, \beta}{2 C_{of} \, (1 + \alpha)}} \tag{28}$$

The combination of (22), (24) and (27) gives a transcendental equation for L_e that can be solved numerically in a few iterations.

2.5 Impact Ionization Current

The flow of electrons through the high field region near drain which generates holes that flow into the MOSFET body and electrons that flow out of drain. This generation current for weak impact ionization can be expressed as

$$I_{Gi} = (M - 1) \, I_{DS(sat)} \tag{28}$$

where the factor (M-1) is given by the integral of the field dependent ionization coefficient

over the high field region:

$$(M - 1) = \int_{L_e}^{L} \alpha_0 \, e^{-\frac{\beta_0}{|E_y|}} \, dy \tag{29}$$

The solution of above equation using the longitudinal electric field expressed as

$$E_y \simeq E_0 \cosh\left(\frac{y - l_e}{l_c}\right) = \sqrt{E_o^2 + \frac{\left(\Delta\Psi_{sf} - V_{DS(eff)}^2\right)}{l_c^2}} \tag{30}$$

yields

$$(M - 1) \simeq \frac{\alpha_0}{\beta_0} \left(V_{DS} - V_{DS(eff)}\right) e^{\left(\frac{-\beta_0 l_c}{V_{DS} - V_{DS(eff)}}\right)} \tag{31}$$

The impact-ionization current when incorporated in the model physically accounts for the floating body effects, for example the " kink effect", but only empirically simulates the drain junction breakdown which may involve the parasitic bipolar transistor. Figures 2.4(a) and 2.4(b) show the input and output characteristics of an SOI MOSFET operating in the velocity saturation region. Note the "kink" at large values of V_{DS}. Thus, one of the important considerations in the design of short channel SOI circuits is to keep V_{DS} small so as to avoid the onset of this "kink". Also, note the velocity saturation effects in the input characteristics because current increases linearly with V_{GS} instead of following the long channel square law.

To summarize, the operational model of the SOI MOSFET is described by the equations (22) and (24) in the triode and saturation region of operation respectively.

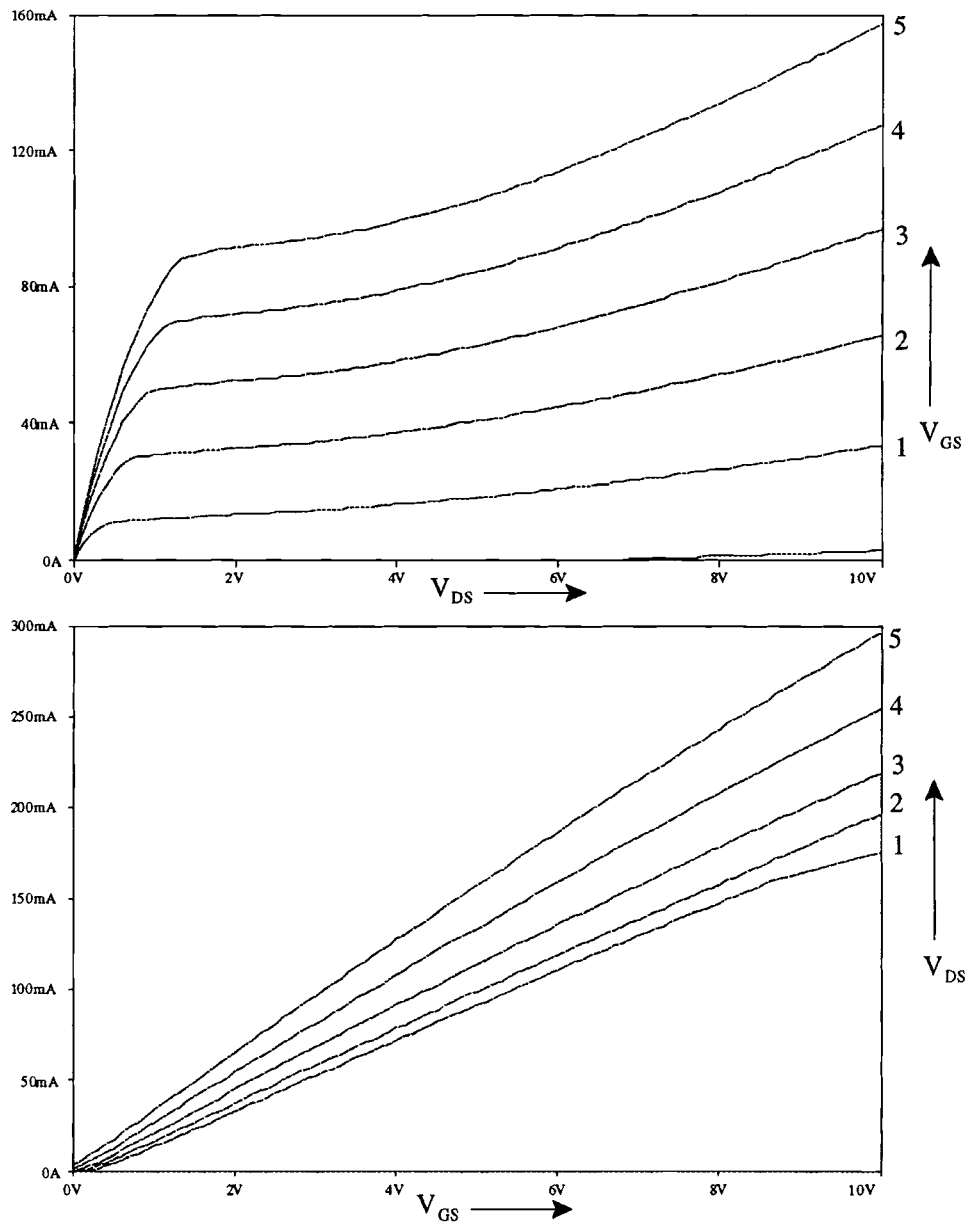

Fig. 2.4 Output and Input Characterisctics of a Short Channel SOI NMOS

CHAPTER 3

DESIGN TECHNIQUES FOR FULLY DIFFERENTIAL AMPLIFIERS WITH INHERENT COMMON MODE REJECTION

This chapter describes the techniques used in the design of the amplifiers presented in this thesis. Some previously published techniques such as gain enhancement and cross coupled mirror loads are described briefly. These are used further to develop the novel differential only boosting concept. Also, a simple transistor topology with a source resistance is analyzed and is used to arrive at the tail boosting technique for reducing the common mode gain. Then a simplified analysis of Power Supply Ripple Gain (PSRG) is presented which brings out the superior power supply rejection performance of the cross coupled mirror amplifier. Finally, these techniques are applied to develop a differential only boosted fully differential amplifier and the amplifier performance equations and results are presented.

3.1 Gain Boosting

The principle of using negative feedback to improve the output impedance forms the heart of the gain boosting technique as described by Bult and Gleen in [8]. It is a very innovative extension of negative feedback principle used in cascoding which was developed by Hostica et al [9]. It simply increases the cascoding effect of the cascoding transistor by addition of a local feedback gain stage as shown in Fig 3.1(a).

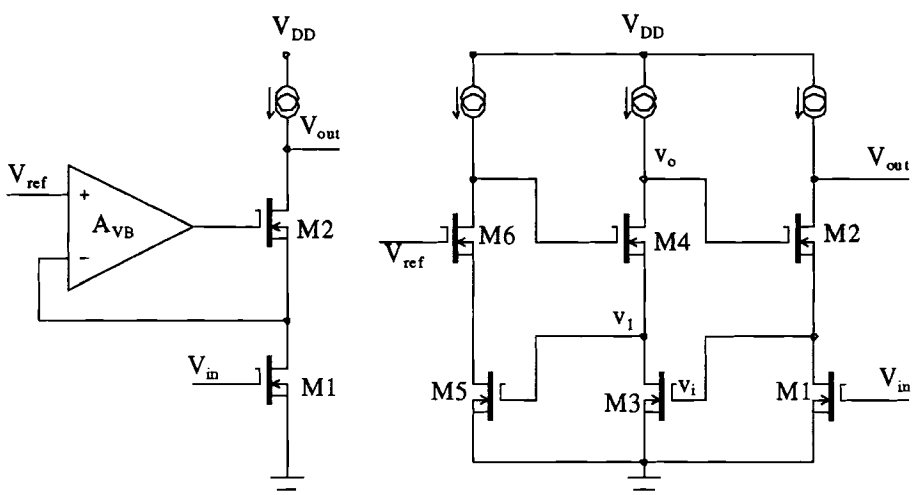

Fig. 3.1 (a) Principle of Gain Boosting (b) Recursive Gain Boosting

This increases the output impedance of the circuit by the gain of the local gain stage A_{VB}. In this manner the output impedance and gain can be increased by several orders of magnitude as follows:

$$r_o \approx g_{m2}\, r_{o2}\, A_{VB}\, r_{o1} \qquad (1)$$

Therefore,

$$A_V \approx g_{m2}\, r_{o2}\, g_{m1}\, r_{o1}\, A_{VB} \qquad (2)$$

If the additional gain stage is implemented as a cascode stage, this gain boosting technique can in turn be applied to this boosting cascode stage. In this manner a recursive implementation of gain boosting can be obtained as shown in fig. 3.1(b). This boosting stage can also be implemented as a folded cascode and as shown later this results in novel differential only boosting. Voltage gain in the boosted stages is limited by factors such as leakage currents, avalanching, thermal feedback and area/geometry or scaling limitations.

For understanding the high frequency behavior of the boosted amplifier, following equivalent circuit of a composite cascode amplifier with a boosting transconductance amplifier is analyzed (For example, M1 and M2 of fig. 3.1(b) forming the main amplifier and M3 as the boosting transconductance amplifier. All transistors assumed to be identical)

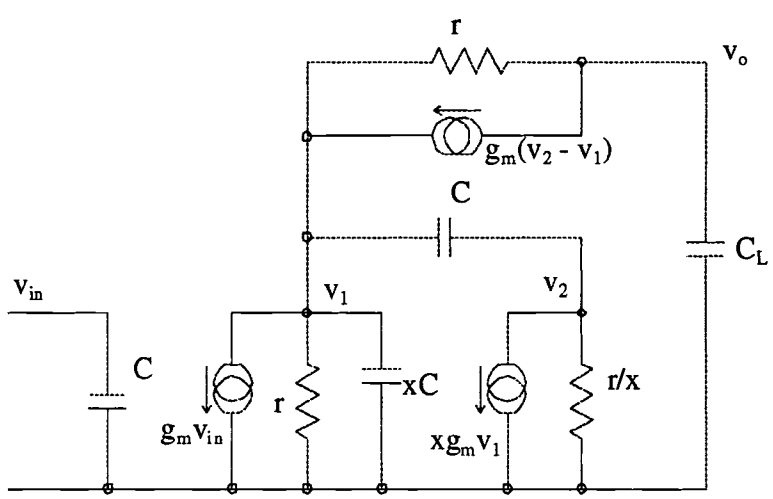

Fig. 3.2 Equivalent Circuit of the Boosted Cascode Amplifier

In the above equivalent circuit, C is the C_{gs} (C_{gd} is assumed to be negligible) and x is the factor by which the second stage is scaled down. It should be noted that C_{db} and C_{sb} have not been used in the analysis as they are assumed to be negligible in a thin film process. To maintain the same transistor self gain, μ, both the width and the current in the

transconductor should be scaled. Assuming a square law device, which is an oversimplification for short channel devices, the transconductance of the boosting amplifier is scaled down by x only which results in a scaled bandwidth. Thus, we can write the following equations for the analysis of this scaled stage:

At node v_1 , we have,

$$g_m v_{in} + \frac{v_1}{r} + v_1 x sC = g_m (v_2 - v_1) + (v_2 - v_1) sC + \frac{(v_o - v_1)}{r} \tag{3}$$

At node v_2, we have

$$x g_m v_1 + \frac{v_2 x}{r} + sC (v_2 - v_1) = 0 \tag{4}$$

At node v_o , we can write

$$g_m (v_2 - v_1) + \frac{v_o}{r} + v_o C_L = 0 \tag{5}$$

Assuming $\mu = g_m r >> 1$, we have the following transfer function

$$\frac{v_o}{v_i} = \frac{\mu^2 (\mu+1)}{s^3 C^2 C_L r^3 + \mu s^2 C C_L r^2 + \mu^2 s C_L r + 2} \tag{6}$$

Solving for the poles of (6) we have,

$$p_1 = \frac{2}{\mu^2 r C_L} \quad p_2 \text{ and } p_3 = \frac{\mu}{r C} = \frac{g_m}{C} \tag{7}$$

Also, from (3), (4) and (5) we can solve for the transfer function of the boosting amplifier as:

$$\frac{v_2}{v_1} = \frac{r(x g_m - C)}{(x + rC)} \tag{8}$$

Solving for poles and zeroes of (8), we have,

$$p_1 = \frac{x g_m}{C} \qquad z_1 = \frac{x g_m}{C} \tag{9}$$

Now, (6) through (9) provide us with vital information about pole zero placement to obtain a single pole roll off and fast settling response.

In [8] it is discussed that the composite amplifier will have a single pole roll off as long as ω_{3dB} of the boosting amplifier is greater than the ω_{3dB} of the composite amplifier. This is equivalent to the fact that ω_{unity} of the boosting amplifier be greater than ω_{3dB} of the main amplifier. Thus, boosting stage need not be as fast as main stage.

Also, we note from (8), that there is a pole zero doublet at the unity gain frequency of the boosting amplifier. Since, it is a well known fact that a doublet degrades the settling behavior of amplifier due to a slow settling component [12], it should be further away from bandwidth of the amplifier. Since, the composite amplifier would be used in a closed loop configuration and maximum closed loop bandwidth is the unity gain frequency of the main amplifier, we have, ω_{unity} of the boosting amplifier > ω_{unity} of the main amplifier. This now implies

$$\frac{xg_m}{C} > \frac{g_m}{C_L} \qquad or \quad x > \frac{C}{C_L} \tag{10}$$

Thus, the load capacitor decides the scaling factor and because of the double pole at the non dominant pole location, scaling factor should be greater than C/C_L to have a safe phase margin. Fast settling response depends also on the phase margin and the relationship between phase margin and minumum settling time has been discussed in [21]. It should be noted that analysis carried out in this section is oversimplified because of the assumptions. However, it gives a fair idea of the critical issues involved in the design of the boost amplifier.

3.2 Cross Coupled Active Loads

In this section, we analyze the difference in the common mode and differential mode behavior of a cross coupled mirror and use it to develop the novel differential only boosted impedance stack. Fig. 3.3 shows a cross coupled current Mirror. [10]

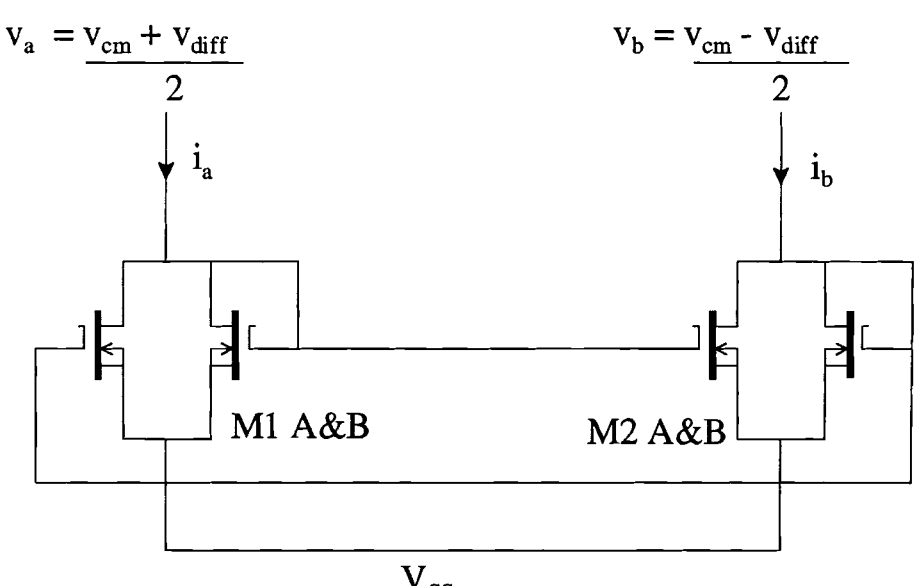

Fig. 3.3 A Cross Coupled Current Mirror

Using the conventional definitions of differential and common mode signals:

$$v_a = \frac{v_{cm} + v_{diff}}{2} \tag{11}$$

$$v_b = \frac{v_{cm} - v_{diff}}{2} \tag{12}$$

Similar notation is used for differential and common mode currents. To understand the difference in the common mode and differential mode behavior, we can analyze the following equivalent circuit shown in Fig. 3.4. Of specific interest are the differential and common mode impdedances of this circuit.

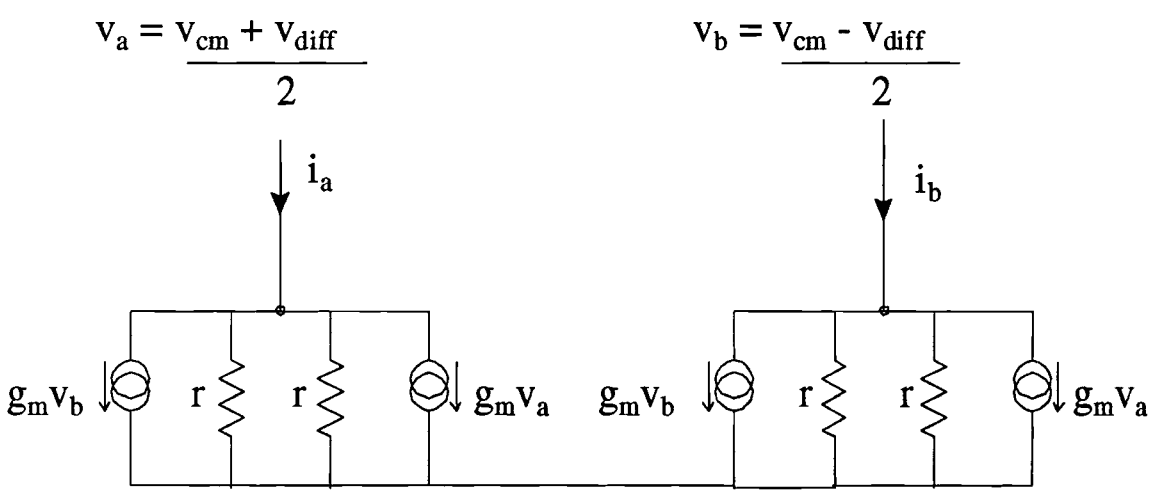

Fig. 3.4 Equivalent Circuit for the Cross Coupled Current Mirror

Thus, we have

$$i_a = \frac{i_{cm} + i_{diff}}{2} = g_m v_{cm} + \frac{v_{cm} + v_{diff}}{r} \quad (13)$$

$$i_b = \frac{i_{cm} - i_{diff}}{2} = g_m v_{cm} + \frac{v_{cm} - v_{diff}}{r} \quad (14)$$

Therefore,

$$i_{diff} = \frac{2 v_{diff}}{r} \quad (15)$$

$$i_{cm} = 2 g_m v_{cm} \quad (16)$$

Hence, we see that,

$$r_{odiff} = \frac{v_{diff}}{i_{diff}} = \frac{r}{2} \quad (17)$$

$$r_{ocm} = \frac{v_{cm}}{i_{cm}} = \frac{1}{2 g_m} \quad (18)$$

Also, for a transconductance amplifier we have,

$A_V = g_{meff} \cdot r_{oeff}$ (19)

where, g_{meff} is the effective output transconductance and r_{oeff} is the effective output impedance. Thus,

$$A_{vcm} = g_{mcm} \cdot r_{ocm} \tag{20}$$

From equation (20), we see that a low common mode impdance results in a low common mode gain and this forms the basis of design of fully differential amplifiers with inherent common mode rejection. Also, we observe from equations (13) and (14), that common mode signals need to be subtracted to give a low common mode impedance. This powerful observation now leads to the concept of cross coupled differential amplifiers which is presented in fig. 3.5 for illustrative purpose only. v_a and v_b have earlier been defined in equations (11) and (12).

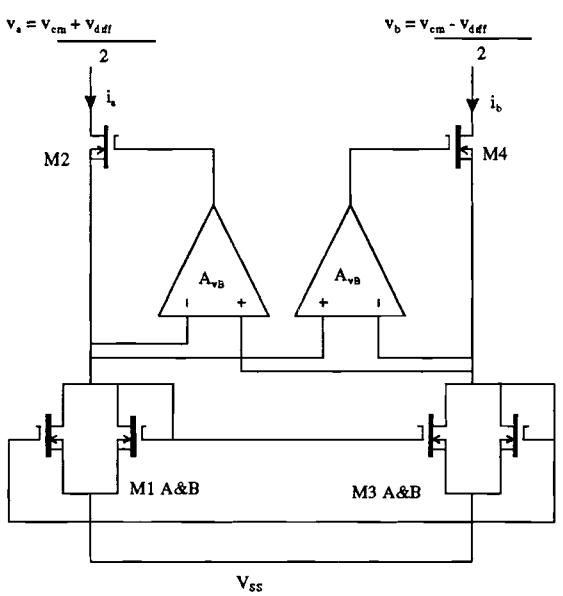

Fig. 3.5 Concept of Cross Coupled Differential Amplifiers

From the schematic in the fig 3.5 it is clear that for common mode signals, there is no gain at the gate of the cascode and this results in the output impedance of this stack being

equal to that of a single transistor only. This absence of feedback now results in a reduction of the common mode impdedance. Thus, we see that

$$r_{odiff} = r_{o1} A_{vB} g_{m2} r_{o2} \quad (22)$$

$$r_{ocm} = r_{o2} \quad (23)$$

Now, the concept of combining the two amplifiers into a single fully differential amplifier is straight forward and this results in the novel differential only boosting architecture. It is called so, because there is no boosting of the common mode gain and the only the differential mode signal is boosted. Thus, we have a differential only boosted impedance stack which is shown in Fig. 3.6. The differential and common mode impedances of this stack are same as in equations (22) and (23) respectively.

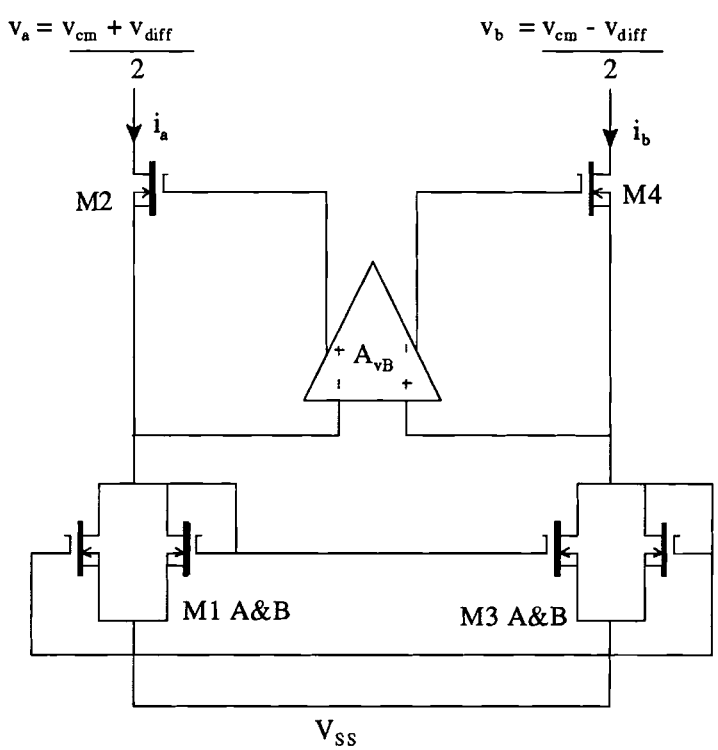

Fig. 3.6 A Differential Only Boosted Impedance Stack

3.3 Common Mode Gain Reduction and Tail Impedance Boosting

Fig. 3.7 shows the schematic of a fully differential folded cascode amplifier.

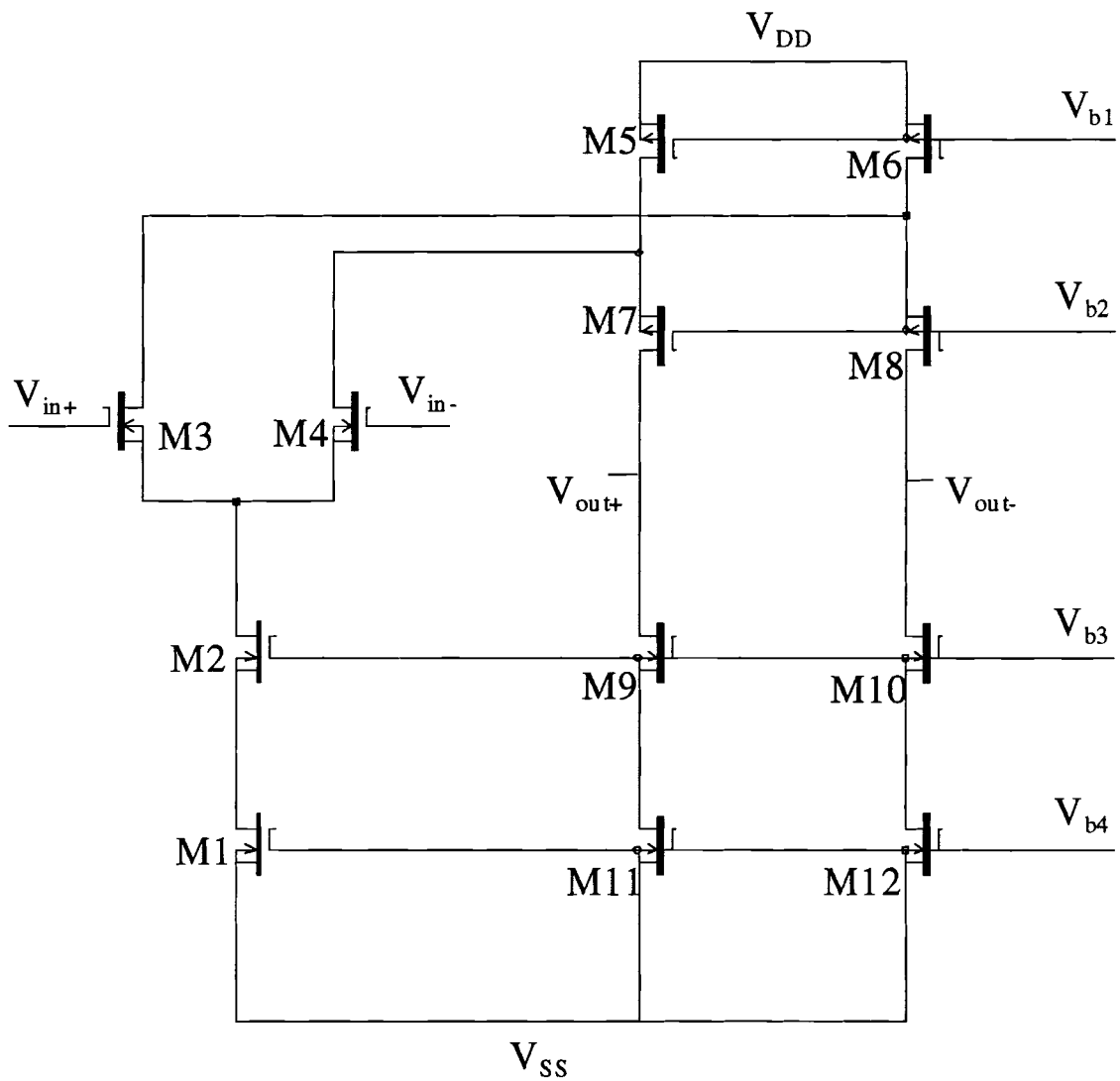

Fig. 3.7 A Fully Differential Folded Cascode Amplifier

We can draw the simplified common mode half circuit of this amplifier as shown in fig. 3.8.

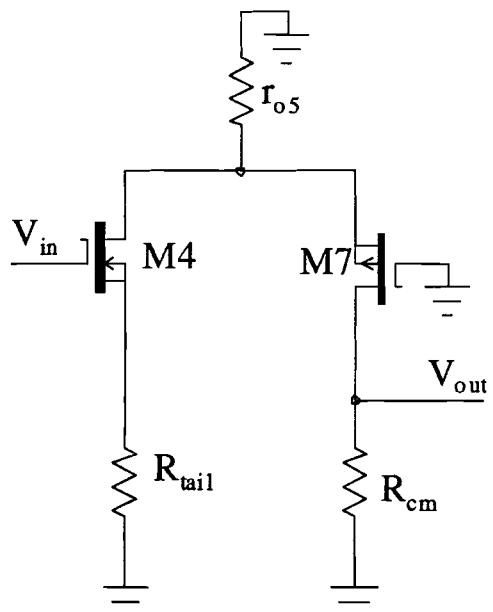

Fig. 3.8 Common Mode Half Circuit for A_{cm} Calculation

For analysis, we can draw the equivalent circuit as shown in fig. 3.9

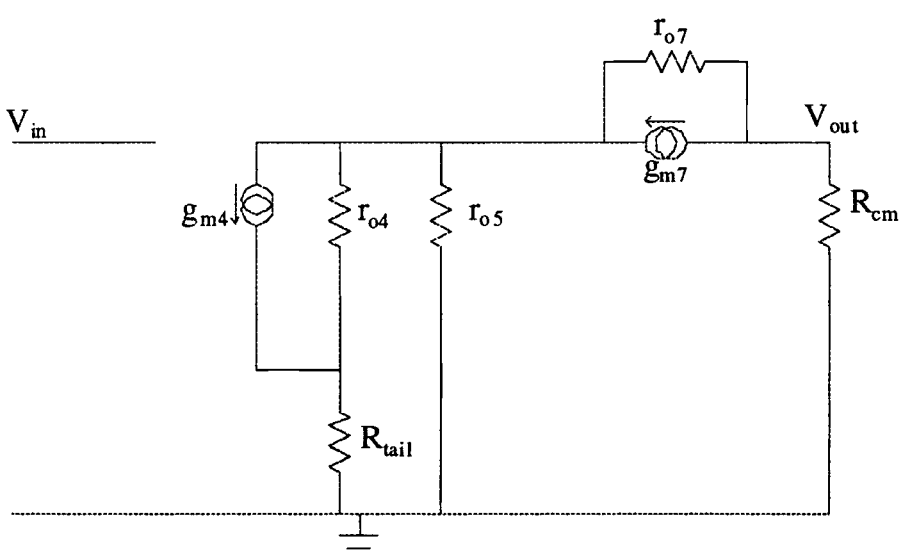

Fig. 3.9 Equivalent Circuit for A_{cm} Calculation

From the equivalent circuit of fig. 3.9, we can write following equations

$$g_{meff} = \frac{g_{m3}}{g_{m3} R_{tail} + 1} \approx \frac{1}{R_{tail}} \qquad (for \quad g_{m3} R_{tail} \gg 1) \tag{24}$$

$$r_{oeff} = R_{cm} \parallel \left[\left[\left[(\mu_3 + 1) R_{tail} + r_3 \right] \parallel r_5 \right] (\mu_7 + 1) + r_7 \right] \tag{25a}$$

$$\approx R_{cm} \qquad (\text{for small } R_{cm}) \tag{25b}$$

Thus, we have

$$A_{cm(eff)} = g_{meff} \cdot r_{oeff} \approx \frac{R_{cm}}{R_{tail}} \tag{26}$$

We have earlier described (see section 3.2, Fig 3.6), the technique used to design a load stack with a low common mode impedance and a high differential mode impedance. Thus, to reduce the common mode gain further, R_{tail} has to be increased. This task is readily accomplished by boosting the tail impedance of the differential pair by using the gain boosting principle of sec. 3.1. It is to be noted that this idea is also a novel contribution of this research work since tail boosting has never been used to reduce common mode gain in fully differential amplifiers before, to the best of author's knowledge. Now, the common mode gain is limited by the gain limitation of the boosted cascodes and the differential pair device mismatch.

3.4 Power Supply Ripple Gain Analysis

Now, we present a simplified analysis of power supply ripple gain which has been previously presented in the literature in a rather complicated manner[20]. For this, the transistor circuit of fig. 3.10(a) is analyzed.

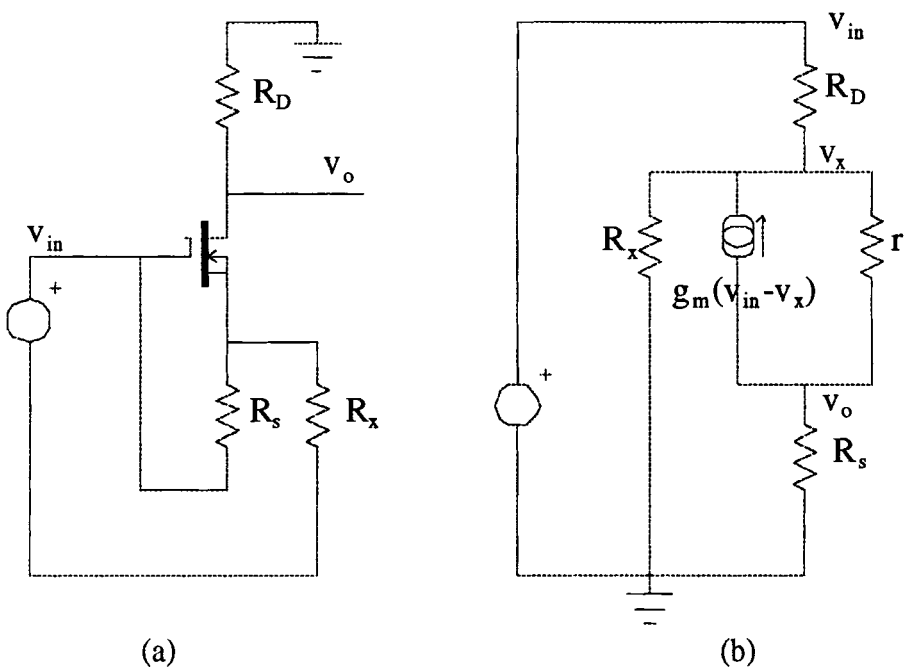

Fig. 3.10 (a) Transistor Circuit for PSRG Analysis. (b) Equivalent Circuit

We can now write following node equations for the equivalent circuit of fig. 3.10(b). Thus, we have, for nodes v_x and v_o, respectively

$$\frac{v_{in} - v_x}{R_s} = \frac{v_x}{R_x} + \frac{v_x - v_o}{r} - g_m (v_{in} - v_x) \tag{27}$$

$$\frac{v_x - v_o}{r} - g_m (v_{in} - v_x) = \frac{v_o}{R_D} \tag{28}$$

From equations (27) and (28) we can solve for the transfer function as

$$\frac{v_o}{v_{in}} = \frac{-R_D(\mu R_s - R_x)}{(\mu+1)R_s R_x + (R_D + r)(R_s + R_x)} \tag{29}$$

A case of special interest is for R_x very large compared to R_s i.e. $R_x/R_s \to \infty$. For this particular case which is normally the situation, as we'll see later,

$$\frac{v_o}{v_{in}} = \frac{R_D}{(\mu+1)R_s + R_D + r} \tag{30}$$

As an example, we can calculate PSRG for the Lu Wu amplifier [10] shown in fig. 3.11

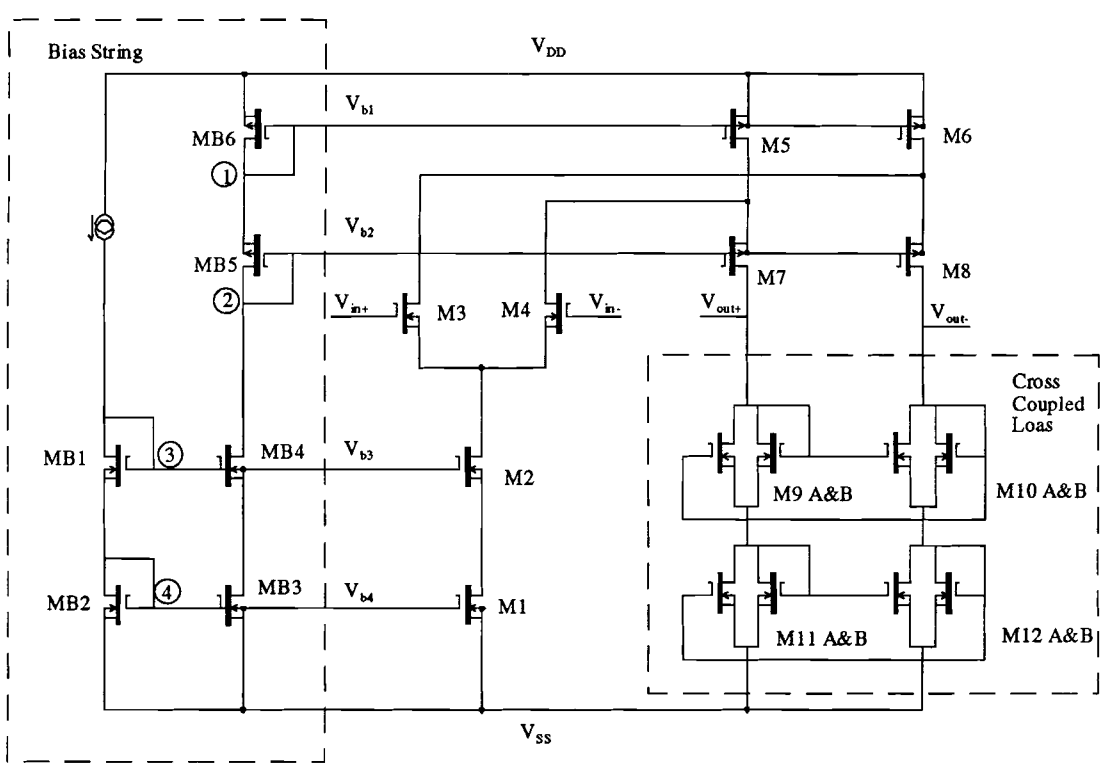

Fig. 3.11 The Lu Wu Amplifier with Cross Coupled Loads

It is to be noted that ac ripple on the supply side makes it's way to the gates of the cascode transistors through to the low impdedance path provided by the diode connected transistors in the bias string which effectively act as "short circuit" to the power supply they are connected to. Thus, nodes 1&2 are shorted to V_{DD} and 3&4 are shorted to V_{SS}. The nodes marked V_{DD} are excited when ripple is supplied through V_{DD} side and nodes marked V_{SS} are excited when the ripple is supplied through V_{SS} side. Thus, marked nodes can be connected to the voltage source or ground depending on the supply they are connected to. Also, biasing transistors M5 & M6 are equivalent to a simple resistor (equal to r_{DS}) since the gate and the source are connected to the same supply and this results in zero transconductance current. Thus, M4 represents the differential pair, M2 is the cascode transistor in the tail, M7 is the cascode transistor and the load resistance is $2/g_m$ as calculated in [10]. Thus, the simplified circuit looks like

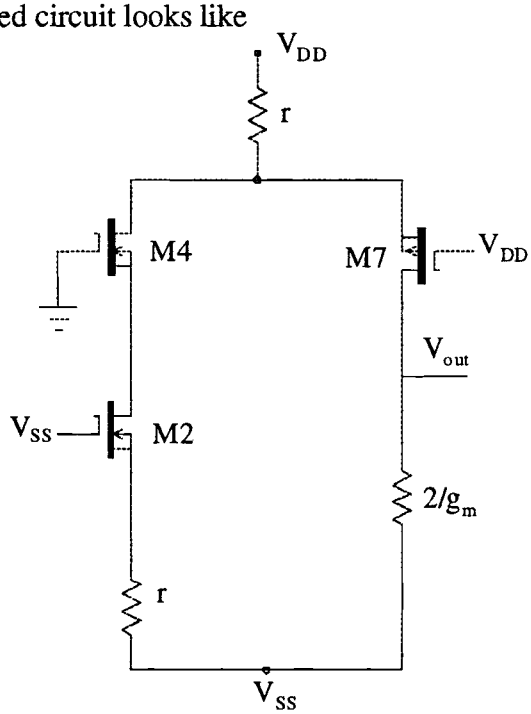

Fig. 3.12 Simplified Half Circuit for PSRG Calculations for the Lu Wu Amplifier

For this circuit with the AC excitation on the V_{DD} side, we have

$R_D \approx 2/g_m$

$R_S \approx r$

$R_x \approx \mu^3 r$

$\therefore \mu_{eff} \approx 2/\mu^2$, using (29). μ_{eff} is the effective gain.

Similarly, we can calculate PSRG on the V_{SS} side. Since there are two paths for ac ripple to get to the output, we can analyze the circuit using the superposition principle. For ac excitation in the tail current cascode M2, we have

$R_D \approx 2/g_m$

$R_S \approx r$

$R_x = \infty$

$\therefore \mu_{eff} \approx 2/\mu^2$ (using (29))

For ac excitation only at the current sink load resistor, we have

$R_D \approx \mu r$

$R_S \approx 2/g_m$, $\mu = 0$, $r = 0$ ($\because$ there is no transistor on this side)

$R_x = \infty$

$\therefore \mu_{eff} \approx 1$ (using (29))

Thus, we have $A_{vss} \approx 2/\mu^2 + 1 \approx 1$

Note that, for simplicity, this analysis assumes the same value of transistor self gain, μ for both n and p transistors, same transconductance and output impdedance, which is rarely the case for any actual process. However, this is much simpler (compared to the more

accurate analysis technique followed in [20]) and easily followed for the purpose of hand estimates. Capacitances can be added at proper nodes to the circuit to obtain a complete PSRG frequency response. The results of this analysis show excellent agreement with simulations shown in Fig. 3.13

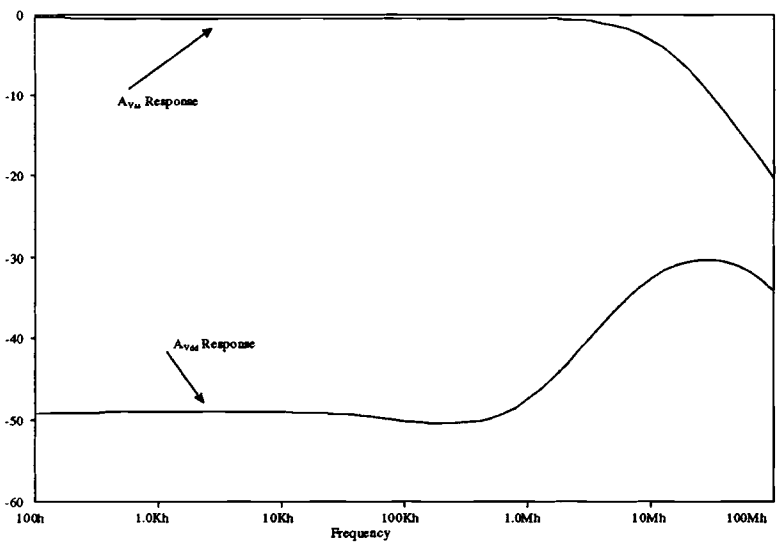

Fig. 3.13 PSRG Response of the Lu Wu Amplifier

Also, with the results presented in this section, it is worthwhile stressing that it is the low common mode gain that makes the circuit stable. A high CMRR which might be misleading because of high differential gain only. That is why the circuit of Fig 3.8 cannot be stable without the addition of common mode feedback circuit to reduce common mode gain. Also, consistent with this philosophy, high PSRR alone can be again misleading if the differential gain is high. For example, a circuit with a common mode gain of 20dB and a differential mode gain of 170dB will have a CMRR of 150dB but cannot be DC stable without some kind of common mode feedback to reduce the common mode gain to less than 1.

3.4 Thermal Noise

The thermal noise is generated from channel resistance due to random thermal motion of carriers. The mean-square input-referred thermal noise is given by [15]:

$$Noise\ power \approx \frac{8KT\Delta f}{3g_m} \tag{31}$$

where Δf is the noise bandwidth, K is the Boltzmann's constant and T is the absolute temperature. Due to the random nature of thermal noise, it cannot be canceled by using any of the offset reduction techniques. Hence the thermal noise must be kept below 1/2 LSB. Taking the required signal to noise ratio into consideration, the constraints on g_m and C_L for a given transistor or circuit can be determined according to the following equations:

$$g_m \geq \left[\frac{8KT\Delta f}{3}\right] \frac{(2^{n+1})^2}{V_{FS}^{\ 2}} \tag{32}$$

where Δf equal to the gain bandwidth product or $g_m/2\pi C_L$, and C_L is given by:

$$C_L \geq \left[\frac{4KT}{3\pi}\right] \frac{(2^{n+1})^2}{V_{FS}^{\ 2}} \qquad (33)$$

where $(V_{FS}/2^{n+1})^2$ represent 1/2 LSB power with n being the total number of bits and V_{FS} being a full scale voltage of the ADC. K is the Boltzmann's constant. Note C_L must be scaled up to reflect the number of equivalent noise sources at the input. Thus, greater the resolution of the A/D converter, lower the required noise floor and thus, high resolution A/D converters must drive large capacitive loads.

3.5 A fully differential differential only boosted folded cascode amplifier with Inherent Common Mode Rejection

In this section, the design techniques described in sections 3.1 through 3.3 are applied to develop and analyze a differential only boosted amplifier. The simulation results show excellent agreement with the predictions of the simplified analysis and success of differential only boosting and tail boosting. The analyses include the ac response of the differential and common mode gain, power supply ripple gain on both V_{dd} and V_{ss} side. Also, the transient step response of the amplifier is presented to confirm the single pole settling behaviour which shows that the pole zero doublet is placed beyond the frequency of interest (GBP of the main amplifier).

Fig. 3.13. shows the schematic of the boosting amplifier used for boosting the n type cascodes. The p type boosting amplifier is simply the electrical complement of the n type i.e.

NMOS's replaced by PMOS's and vice versa.

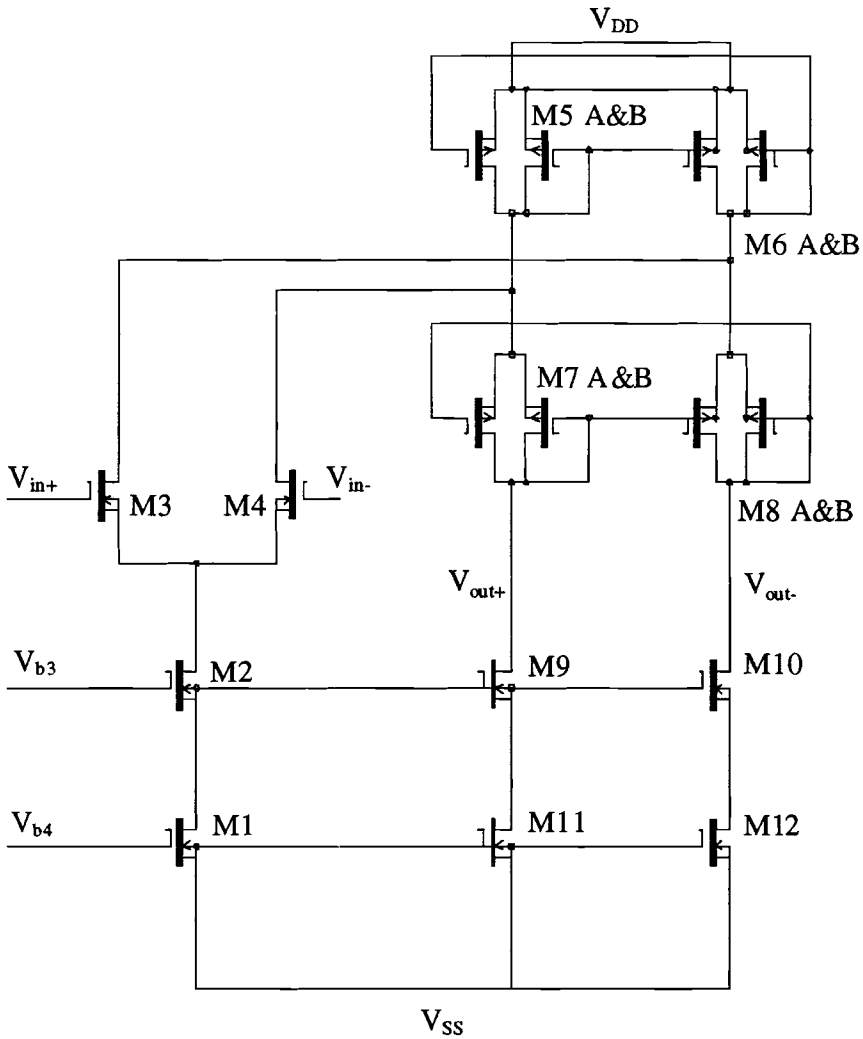

Fig. 3.11 The Modified Lu Wu Amplifier used as Nch Boosting Amplifier

Performance of this modified Lu Wu amplifier, which is again an original contribution of this work, is summarized in following equations.

1) $A_{vdiff} = \mu^2/4$ (34)

2) $A_{cm} = 2/(3\mu^2)$ (35)

3) $GBP = g_{m1} / C_L$ (36)

4) $Av_{dd} = 1$ (37)

5) $Av_{ss} = 3/(2\mu^2)$ (38)

Note that for the complement version, A_{Vdd} and A_{Vss} will be simply interchanged others performance parameters remaining the same.

Now, combining all the design ideas presented so far, we apply them to develop the fully differential differential only boosted amplifier which achieves very low common mode gain without using extra common mode feedback circuits. Fig. 3.15 shows the schematic of the amplifier.

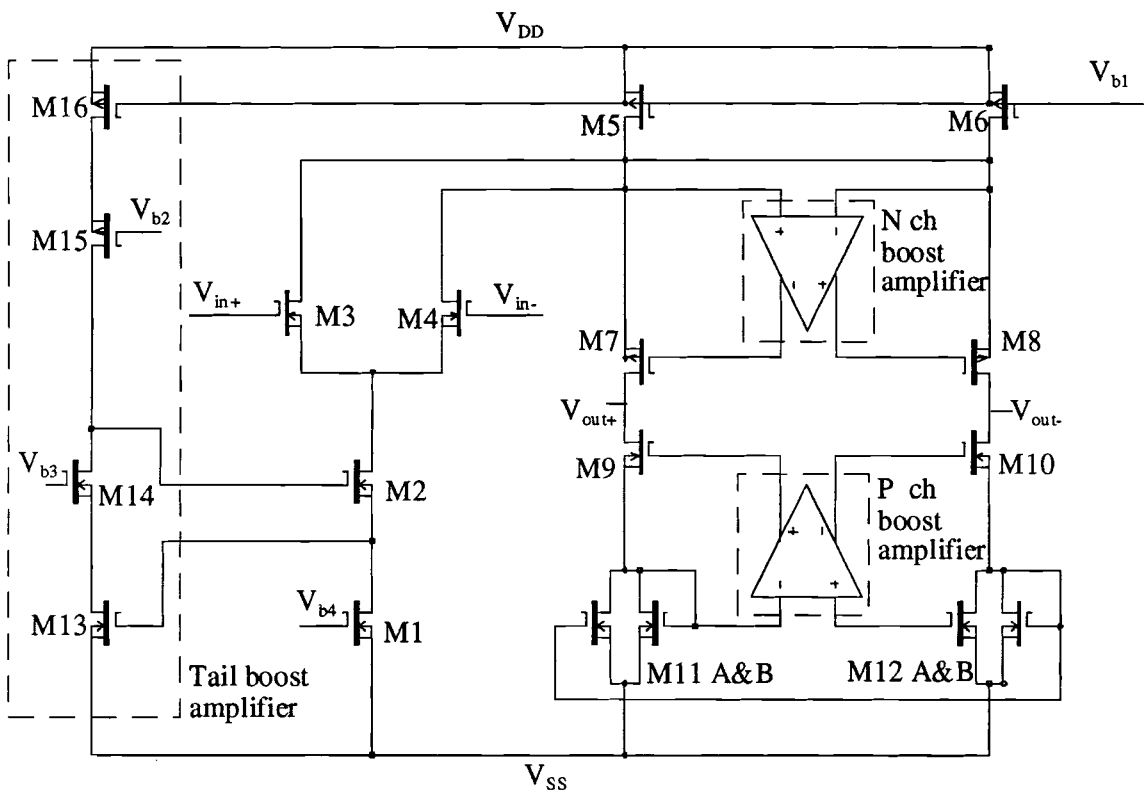

Fig. 3.15 The Fully Differential Differential Only Boosted Amplifier

The following expressions can be derived for the performance of this amplifier.

$$A_{vdiff} \approx (\frac{\mu^2}{4})^2 \tag{39}$$

$$A_{vcm} \approx \frac{2}{\mu^3} \tag{40}$$

$$\omega_u \approx \frac{g_m}{C_L} \tag{41}$$

Fig. 3.16 shows the DC response of the Lu Wu amplifier and this amplifier. Note the clipping of the output voltage in the case of Lu Wu amplifier which occurs due to the series connected "diodes" sinks as the V_{GS} is limited by the current in that branch. Also, note that the swing limitation has been eliminated by the use of a single cross coupling instead of double as now V_{DS} can increase while current remains constant.

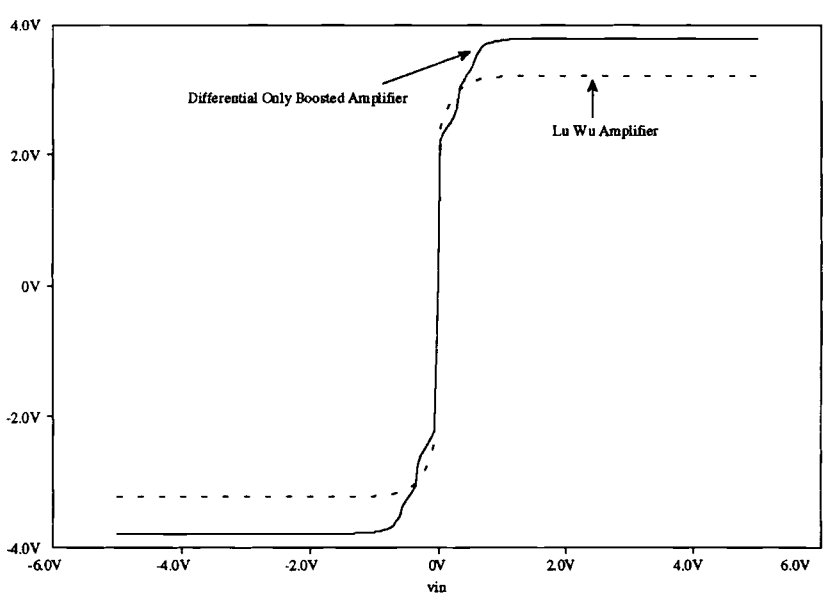

Fig. 3.16 Comparison of DC Response of the Differential Only Boosted Amplifier and the Lu Wu Amplifier.

Fig. 3.17 shows the AC response of the amplifier. As expected the differential gain of the main amplifier is boosted by that of the additional boosting amplifier. Also, common mode gain response is shown with and without tail boosting. The remarkable difference in the common mode gain brings out the importance of tail boosting which is one of the key ideas in this design.

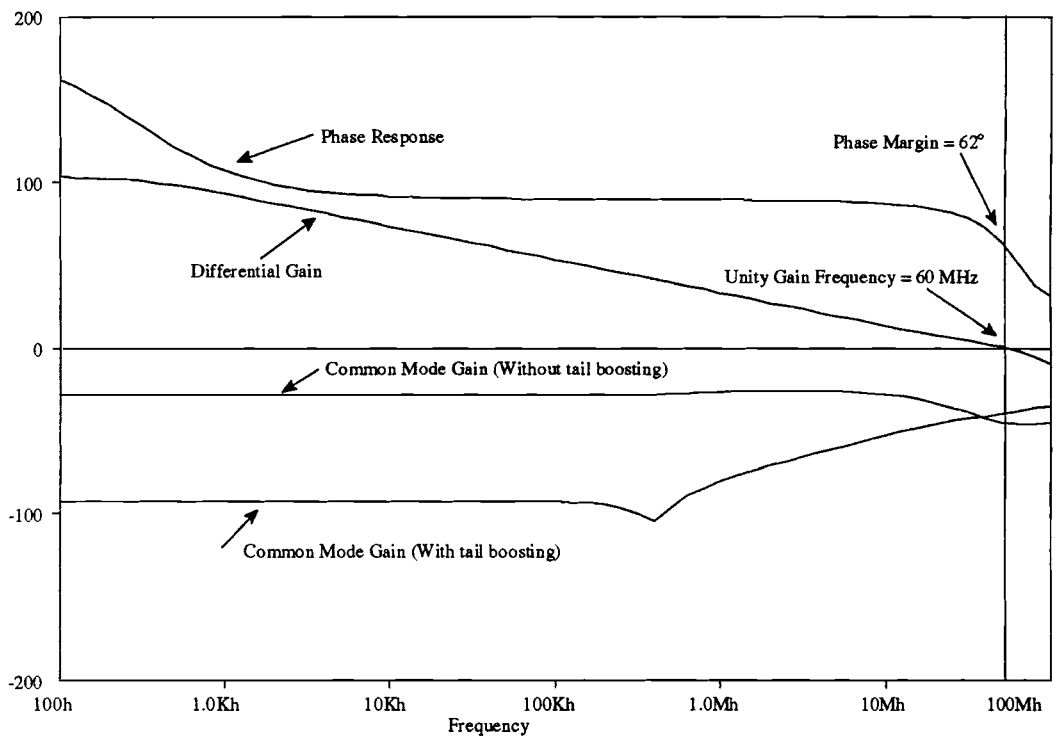

Fig. 3.17 Open Loop Frequency Response of the Differential Only Boosted Amplifier

The transient response of the amplifier to a step input is shown in fig. 3.18, which demonstrates the stability of the described architecture. Single pole settling behavior is observed indicating that there are no slow settling components in the pass band of the amplifier. Also, transient voltages at the gates of the cascode transistors are shown to bring out the stability of the boosting amplifiers and their fast settling response.

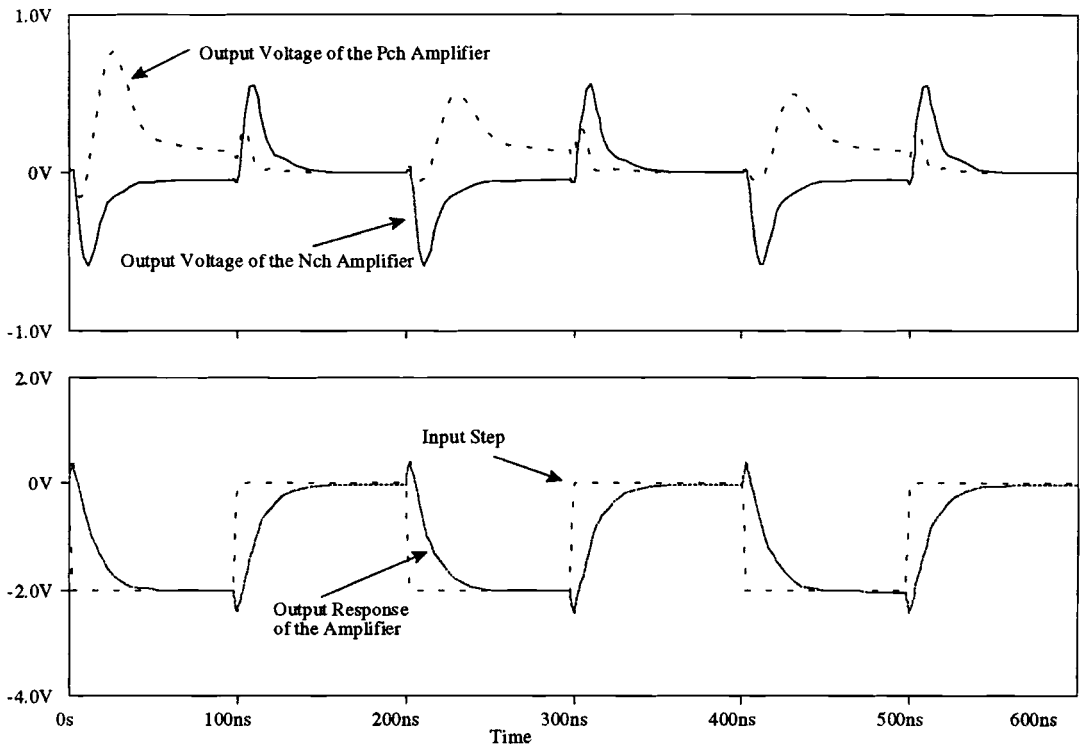

Fig. 3.18 Closed Loop Unity Gain Transient Response of the Boosted Amplifier

Now, following the analysis used in section 3.4, we can calculate the PSRG for the differential only boosted amplifier. From equation (32) we see that the power supply ripple makes it's way directly to the output from the supply to which cross coupled loads are connected. It can be shown that same is the case for the modified Lu Wu amplifier (see fig. 3.14) which is used as the boosting amplifier. Thus, it is clear that the power supply ripple makes it's way to the gate of the cascodes of the main amplifier. The tail boosting amplifier also contributes to the PSRG. To understand the contribution of each block, we can analyze the simplified half circuit for the boosted amplifier as shown in fig. 3.19

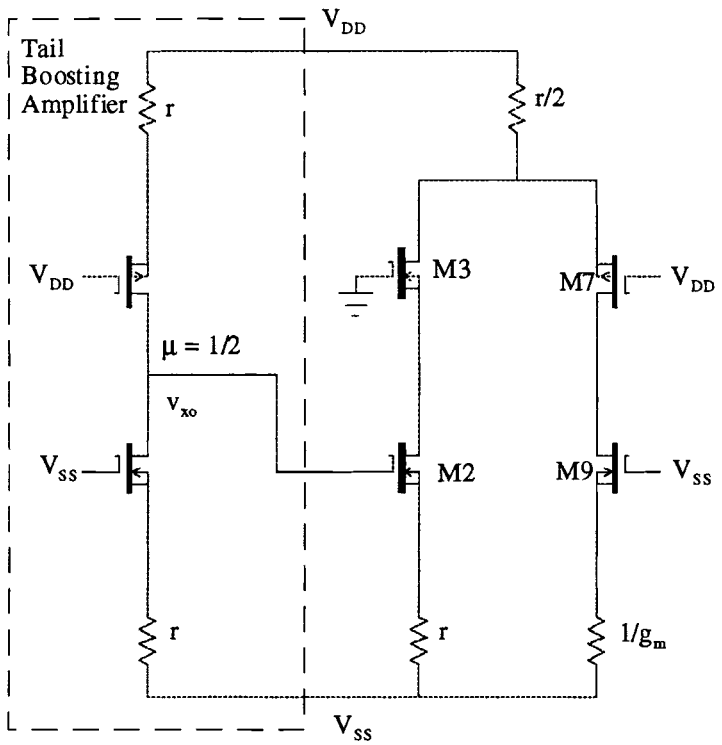

Fig. 3.19 Simplifier Half Circuit for Boosted Amplifier PSRG Analysis

To further simplify the analysis, the contribution of the tail boosting amplifier is analyzed first. It is obvious from fig. 3.19, that the tail boosting amplifier behaves in an identical fashion for the ripple on both V_{dd} and V_{ss}, sides as the circuit is symmetrical. So, we can calculate Av_{xx} (xx=dd or ss)for the tail boosting amplifier. Thus, at node v_{xo}

$R_s = r$

$R_D = \mu r$

$R_x = \infty$

$\therefore A_{vxx} = 1/2$ (using 29) (42)

Now, we can use superposition to calculate A_{VDD} for the boosted amplifier. For excitation only in the cascode device, M7,

$R_s = r$

$R_x = \mu^3/r$

$R_D = \mu \,.\, 1/g_m = r$

$\therefore A_{veff} = 1/\mu$ (from 29) A_{veff} being the effective AC gain.

For excitation in the cascode of the tail boosting amplifier,

$R_s = r$

$R_x = \infty$

$R_D = r$

$\therefore A_{veff} = 1/2\mu$ (from 29 and using the fact that Av_{xx} for boosting amplifier is 1/2)

Thus, total A_{VDD} for the boosted amplifier = $3/\mu$. Similarly, we can analyze A_{Vss} for this amplifier using the superposition principle.

For excitation in the cascode of the tail boosting amplifier,

$R_s = r$

$R_x = \infty$

$R_D = r$

$\therefore A_{veff} = 1/2\mu$ (from 29 and 42)

For excitation only in the cascode device, M9

$R_s = 1/g_m$

$R_x = \infty$

$R_D = \mu r$

$\therefore A_{veff} \approx 1$ (from 29)

Thus, total A_{Vss} for the boosted amplifier = 1. We can summarize the PSRG

performance of the boosted amplifier in following equations,

$$Av_{dd} = 3/\mu \quad (43)$$

$$Av_{ss} = 1. \quad (44)$$

Fig. 3.20 shows the PSRG response for the differential only boosted amplifier. From this analysis, we note that the PSRG depends on the common mode impedance of the amplifier. The lower the common mode impedance, the lower the PSRG on the supply opposite to which low impedance loads are connected to. This observation implies that cross coupled amplifiers are best suited for single supply operation and the cross coupled side should be connected to ground for best PSRG performance.

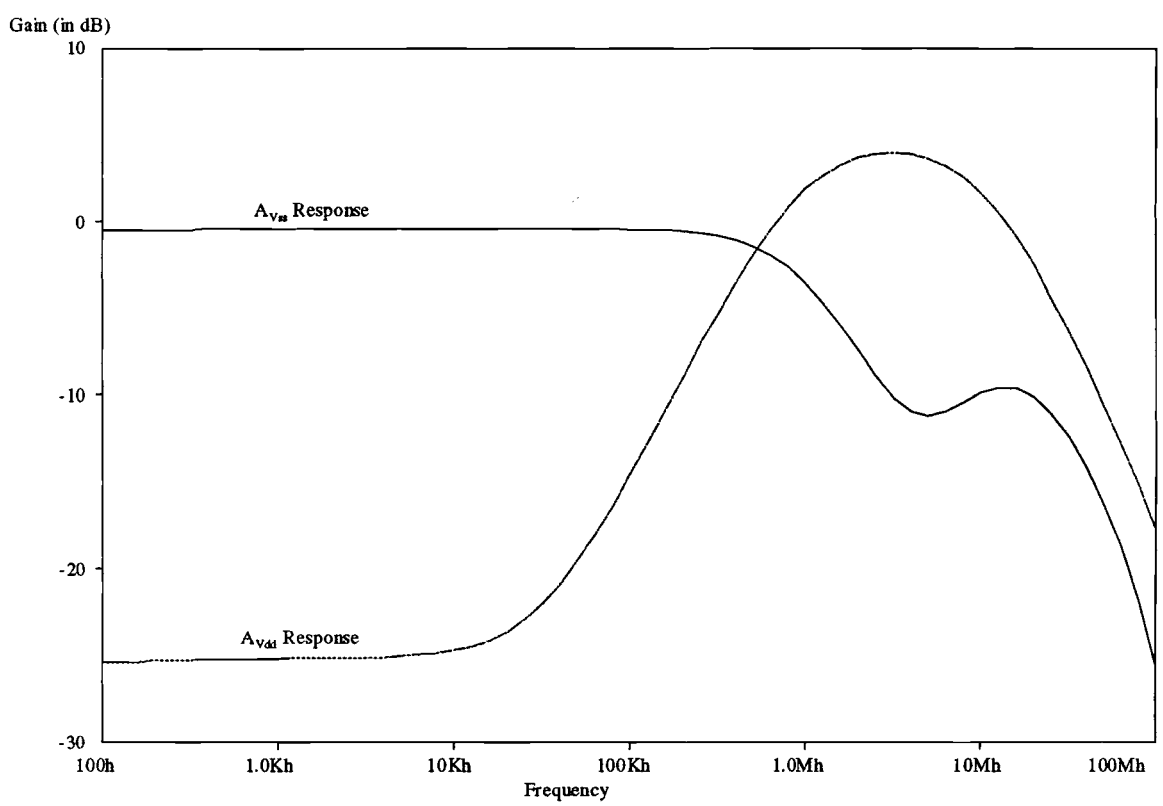

Fig. 3.20 PSRG Response of the Boosted Amplifier

CHAPTER 4

A MICROWAVE BANDWIDTH, HIGH DC GAIN AMPLIFIER

This chapter describes the design and development of the first ever CMOS amplifier projected to operate in microwave frequency range. The amplifier is intended to be used in a 2.5 GSPS over sampled A/D converter with a resolution of 16 bits. The required unity gain frequency is 5 GHz with an open loop differential gain of about 96 dB. A fast and accurate settling amplifier leads to contradictory demands of wide bandwidth and high DC gain. Wide bandwidth calls for short channel devices biased at large current levels and high gain requires long channel devices biased at low current levels. However, by using the differential only boosting technique described in chapter 3, (section 3.3) this task has been achieved in the new IBM SOI 0.25μm process in which the devices have an f_T in the range of 25-40 GHz and self gains of about 20-25dB.

Since there are no simple design equations as yet for design of SOI circuits, the design presented here is heavily simulation aided. Also, since SOISPICE does not converge for gain boosting topologies, the architecture used has been validated with Pspice simulations for level 2 SOI MOSFET parameters. However, the simulator does converge

for only one stage of the amplifier and that has been used to project the behavior for the amplifier by changing the widths in the same deck and changing the loads accordingly.

4.1 Amplifier Specifications

To keep the thermal noise generated in the transistor channel below the required level of 1/2 LSB of the A/D converter (section 3.5, eqn 39) , this amplifier must drive a load capacitor of 30pf. Thus, we can summarize the amplifier specifications as follows:

A_{Vdiff} = 96 dB (1)

GBP = 5 Ghz (2)

C_L = 30pF (3)

Input referred noise = 5 $\mu V/\sqrt{Hz}$ (4)

$V_{o\,(swing)}$ = Within 1V of the supplies (5)

4.2 Recursive Differential Only Folded Cascode Boosting

To achieve a high DC gain this amplifier uses the novel concept of recursive differential only folded cascode boosting which is a combination of the recursive cascode gain boosting and differential only boosting schemes described in sections 3.1 and 3.2 as shown in fig 4.1. In this implementation, the cascode transistors of the boosting amplifiers are also boosted by boosting amplifiers. Note that this technique is extremely useful in fully differential configurations where differential only boosting is more easily implemented. The

lower levels of boosting amplifiers are scaled in accordance with the scaling principle developed in section 3.1. Thus, returns in the DC gain are more than the required increase in area as boosting amplifiers take lesser area at lower levels. Recursive differential only folded cascode boosting, however, degrades the frequency response slightly but preserves the low common mode gain response of the boosting amplifiers while boosting the differential gain.

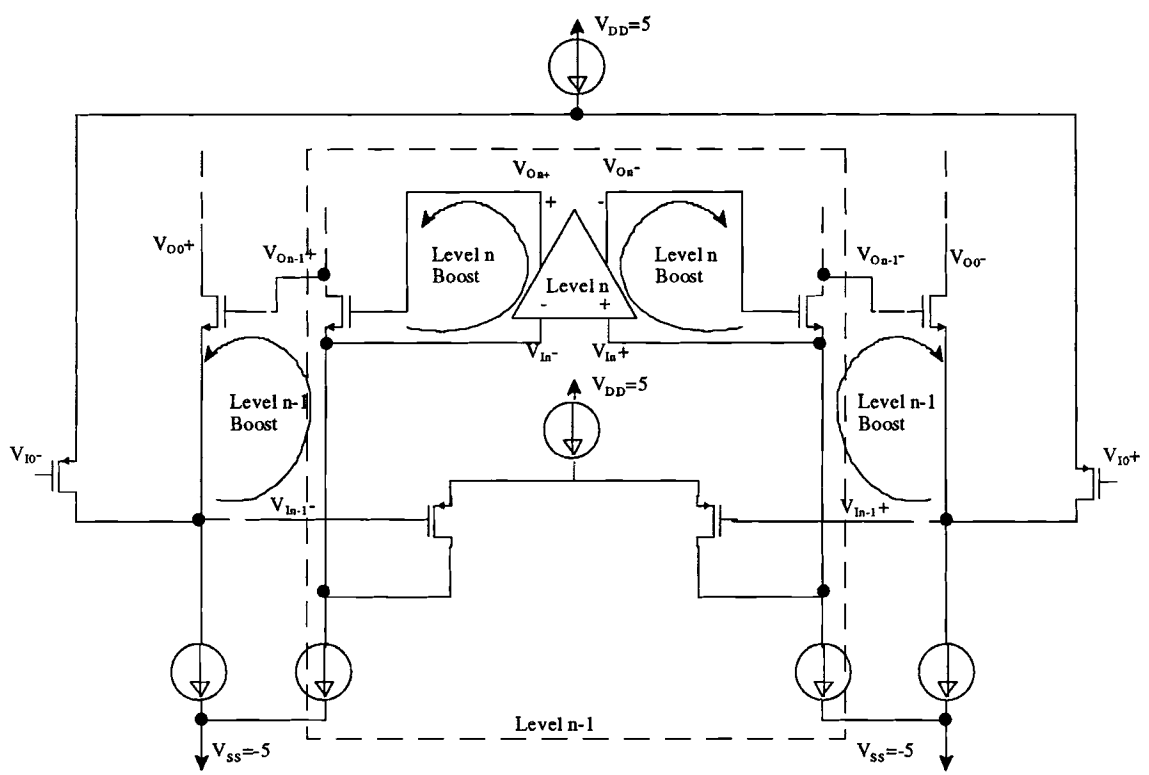

Fig. 4.1 Recursive Differential Only Folded Cascode Boosting

4.3 Circuit Topology and Projected Performance

Fig. 4.2 shows the schematic of the high performance amplifier. The Nch and Pch boost amplifiers are differential only boosted amplifiers (see fig. 3.15). Thus, the dc gain achieved by the amplifier is combined gain of six transistors corresponding to two levels of boosting.

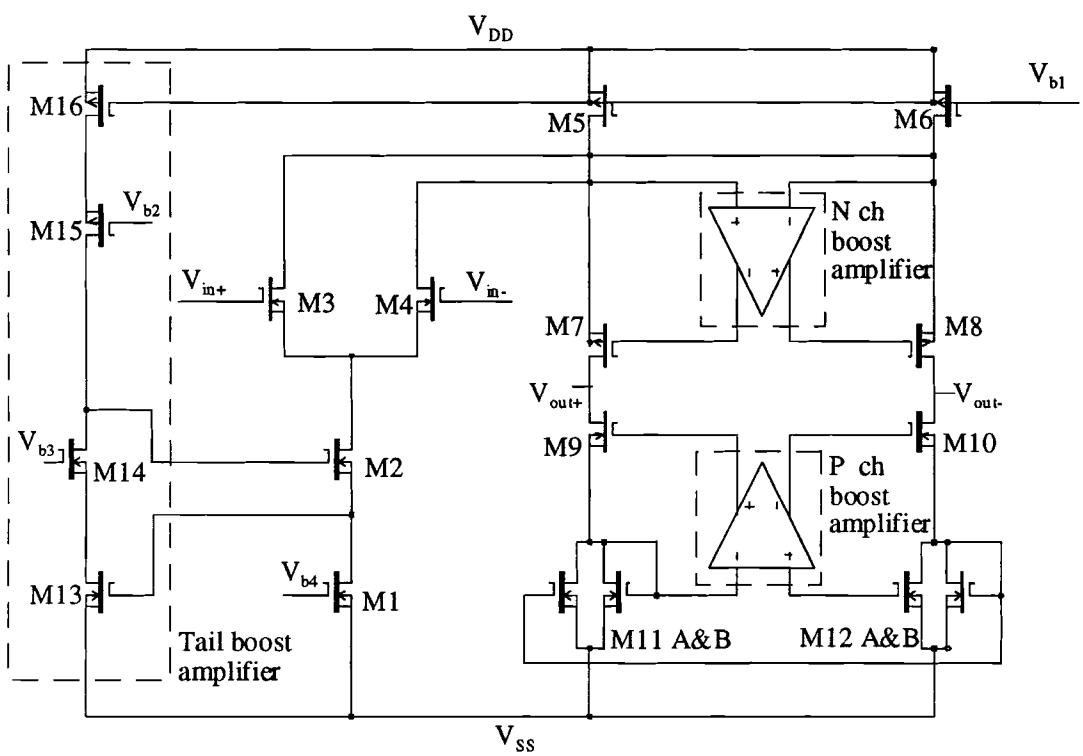

Fig. 4.2 Schematic of the High Performance Amplifier

The circuit operation is similar to that of the differential only boosted amplifier of section 3.6 and the boosting stages can be analyzed separately with proper feedback capacitors as in section 3.1. Special concerns in SOI circuit design are presented in the following sections.

4.3.1 DC Behavior

To extract an effective transconductance (g_{meff}) of about one Siemen from a transistor, it must conduct current in miliamperes as well as require a large width to length ratio. Wide devices with minimum channel length are used to maintain the practical "overdrive" voltage (about 1.0 V) on the transistor is an additional constraint because short channel devices cannot operate with large V_{DS}. This is due to the avalanching problem which occurs at large V_{DS} across the transistor. Thus, $V_{DS,}$ in addition to V_{GS}, in these short channel transistors has to be limited to about 1.5V or so otherwise the avalanche multiplication results in the "kink effect" (see section 2.5) in the I_{DS} V_{DS} curves which reduces the r_{DS} drastically thereby reducing the intrinsic gain of the transistor. Also, increasing V_{GS} further doesn't increase g_m but can result in tunneling through the thin gate oxide in these devices. This means that amplifier must be operated with low voltage supplies.

This amplifier preserves the advantage of large swing at the output due to single cross coupling in the load transistors.

4.3.2 AC Behavior

This amplifier is designed to have a unity gain frequency of approximately 5 Ghz. Fig. 4.3 shows the ac response of the main stage only. The dc gain of one stage as simulated is 37 dB. This implies that the dc gain for double boosted amplifier will be 117 dB when measured differentially. The differentially measured bandwidth will also be twice i.e. 6.5 GHz. From the simulation, the common mode gain for one stage is -25dB. By boosting the tail impedance once, the common mode gain is further reduced to about -60dB but then the differential pair mismatch places a practical limit on the common mode performance.

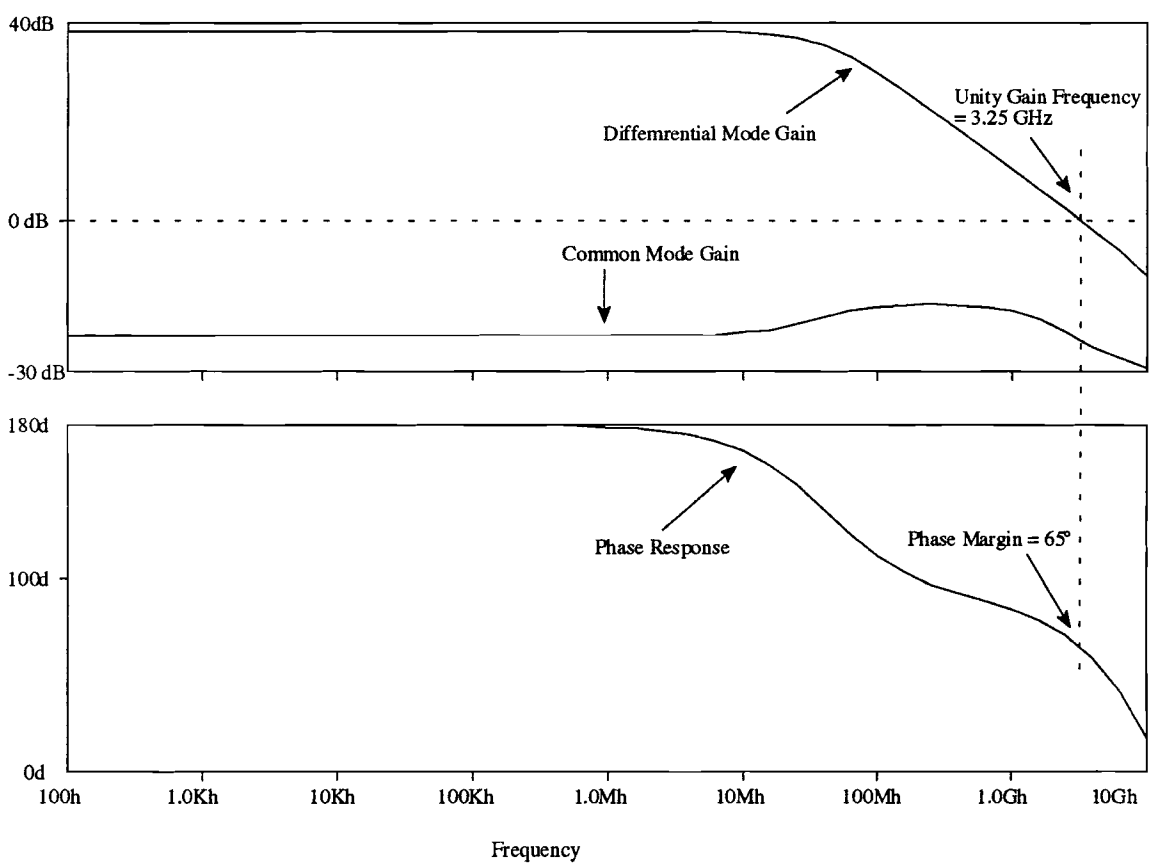

Fig. 4.3 Open Loop AC Response of the High Performance Amplifier

From fig 4.3, we see that there is only one pole below the unity gain frequency. This point might be somewhat misleading here since, this isn't the exact frequency response. The single pole frequency response would be unaffected below the unity gain frequency with addition of boosting amplifiers since the poles and zeroes of the boosting amplifiers are designed to be beyond the unity gain frequency of the main amplifier. Also, phase response would be altered by the addition of boosting amplifiers. But this simulation does give us a fair idea of the non dominant pole location and thereby the phase margin.

Amplifier performance can be summarized by the following equations

$$A_{vdiff} = (\mu^2/4)^3 \quad (6)$$

$$A_{vcm} = 2/\mu^3 \quad (7)$$

$$CMRR = \mu^9/64 \quad (8)$$

$$\omega_{unity} = g_m / C_L \quad (9)$$

4.4 Layout Considerations

Layout of a circuit which is operating in microwave range is a separate problem in itself. A lot of care must be taken to ensure that circuit is not slowed down by the added parasitics associated with the interconnects. The Following problems have to be addressed in such a layout task.

The whole circuit size is dictated by wavelength constraint which implies that circuit dimensions must be less than $\lambda/8$, (λ is the wavelength associated with the maximum projected operating frequency) on each side to the setting up of a microwave resonator by

the power bus or the ground ring. This problem is more severe in GHz range where oscillations can result more readily because of a small wavelength involved. To minimize this problem, wires are laid out in a ground-signal-ground fashion and are overlapped with different level metal to provide a low impedance path for field lines termination. Also, to provide a low impedance path for field termination a ground ring is put around the circuit.

The next problem faced is the source impdedance of the transistors. From analysis in chapter 3 (section 3.4, equation 24), we have the following equation for a transistor with a non neglectable source resistance, R_S

$$g_{meff} \approx \frac{g_m}{g_m R_S + 1}$$

Thus, we see that greater the source resistance, lower the effective transconductance of the transistor. This is known as "source degradation" in MOS circuits. This problem is most severe in the differential pair of the main stage amplifier where required transconductance is about 1S. Thus, to satisfy the requirement $g_m R_S << 1$, R_s must be less than about 0.05 ohm for a 5% transconductance degradation. This forces the metal connections to the sources of the equivalent transistors to be very wide.

The gate RC time constant is another problem which has to be tackled to make fast circuits. To reduce the RC delay in the gate of the transistors, special poly to metal1 contacts are laid out on the gate of the transistors and they are connected by metal1 to reduce the series resistance of the gate, R_g such that $R_g C_g >> \omega_u$ of the amplifier. Also, on the

process side, T-gates can be fabricated which further reduce the time constant of the gate.

To ensure matching in the transistor pairs, all the transistors have been laid out using fingers of smaller transistors which helps avoid large variation of parameters among different transistors by statistically averaging all the parameter variations in the units of a single large transistor. For example, the differential pair in the high performance amplifier contains about 1000 fingers. At this point in time, insufficient data is available to determine the effects of global mismatch on the circuit performance. Also, laying out transistors in fingers helps ease the R_gC_g constraint, since $R_g \propto W$ for wide transistors not laid out as fingers.

4.5 Testing Approach

These wide bandwidth, high DC gain amplifiers have to be put in special configurations on chip itself to measure the open loop gain and the frequency response of the amplifier. Special high frequency probe cards have to be used for on chip testing. These probe cards have pads laid out in ground-signal-ground fashion to provide low impedance path for field lines termination. The testing objectives are to measure the open loop gain of the amplifiers, measure the GBP & settling time and characterize the transistors and test circuits by s-parameter tests. Following sections describe the test structure and the procedure to measure the performance of these amplifiers and other test cells such as the boosting amplifiers.

4.5.1 Open Loop Gain Measurement

The opamp is placed in a unity gain feedback configuration using feedback capacitors as shown in Fig. 4.4.

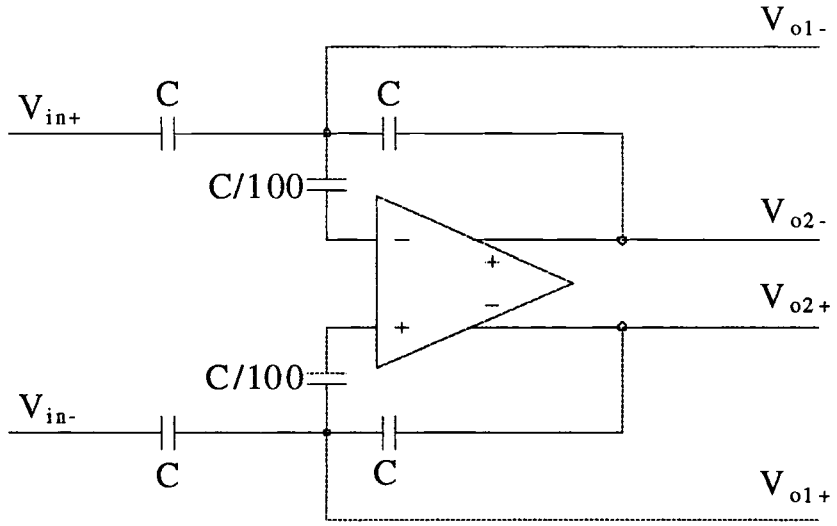

Fig. 4.4 A_{VOL} Frame for High Performance Amplifier

For this configuration, the open loop gain of the amplifier is given as:

$$A_{VOL} \approx 100 \frac{V_{o2+} - V_{o2-}}{V_{o1+} - V_{o1-}} \tag{10}$$

Thus, we see that a capacitive voltage divider is formed at the input of the amplifier which amplifies the voltage at the input of the amplifier by a fixed capacitor ratio before it goes to the output pad. The ratio of 100 was selected since there is a limit to the lowest value capacitor that can be reliably fabricated. The inherent gate to source capacitance of the input transistors dictates the size of this small capacitor. The measurement points must be buffered to prevent the input impedance of the amplifier from degrading. Thus, the signal

amplitude at the input of the amplifier is multiplied by a factor of 100 before it goes off chip, thus, simplifying the measurement procedure. Also, the terminals of feedback capacitors are connected by switched which are used to discharge the capacitors.

4.5.2 Unity Gain Frequency Measurement

For measurement of the unity gain frequency of the amplifier, again the amplifier is put in a unity gain feedback configuration as shown in fig. 4.5.

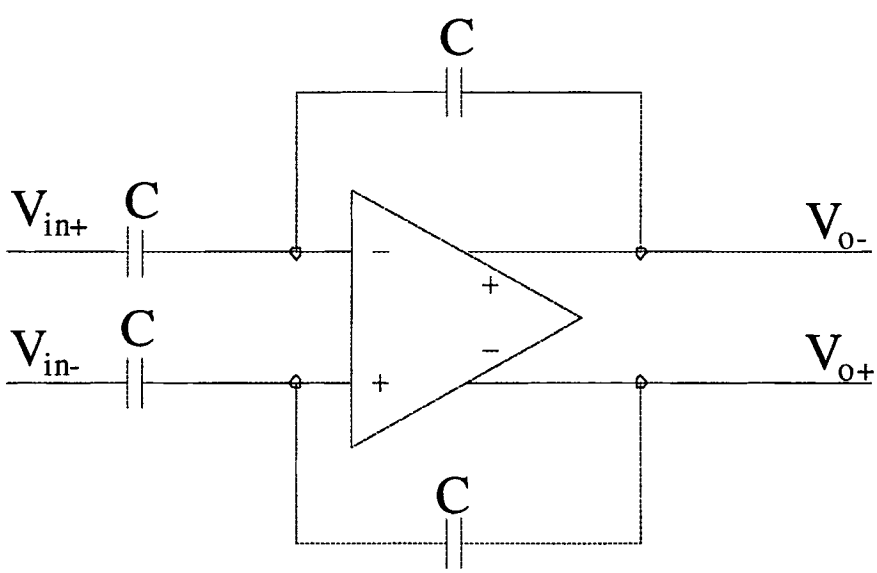

Fig. 4.5 UGBP Frame for High Performance Amplifier

A step input is applied to the amplifier and the settling behavior of the opamp is measured to calculate the gain bandwidth product of the amplifier. This arrangement serves the dual purpose of measurement of V_{offset} and unity gain bandwidth of the amplifier. Assuming single pole settling, following equation can be derived for the output response to

a step input.

$$V_o = V_{in} (1 - \exp (-\omega_u t)) \quad (11)$$

Using equation(6) , the time taken to settle with in a desired accuracy can give a measure of the bandwidth of the amplifier. For example, to settle within 0.1% of the final value, the time taken is , $t = 6.91/\acute{\omega}_u$. In addition, the open loop gain (assuming perfectly matched capacitors) determines the accuracy to which output can settle. Fig. 4.7 shows the unity gain transient response of the main stage of the high performance amplifier without boosting. It is the not the exact response of total amplifier. However, it can give a fair idea of the bandwidth of the amplifier with reduced settling accuracy because of the low DC gain of a single stage without boosting.

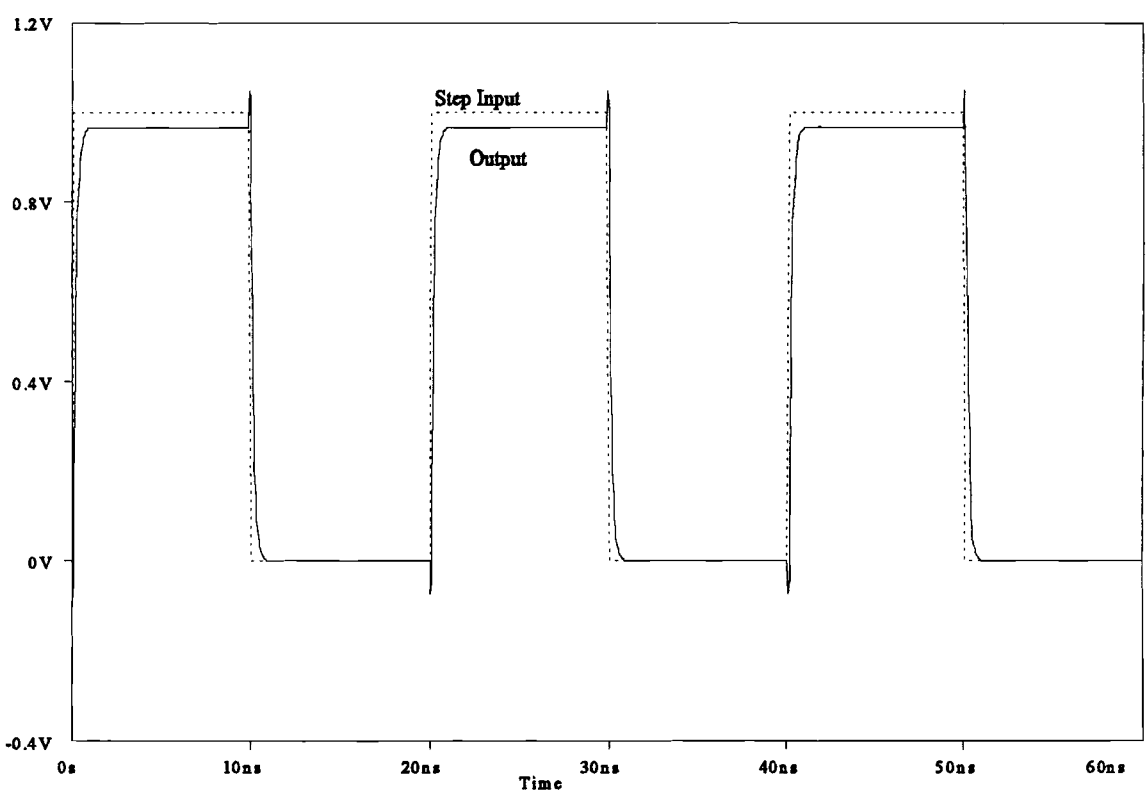

Fig. 4.7 Closed Loop Unity Gain Transient Response of the High Performance Amplifier

4.5.3 S-Parameter Testing

Also, as a further test, high performance opamp has been put in s-parameter frame which can be used to measure the effective forward and reverse transconductance and input as well as the output impedance in 1-10 GHz range. It is to be noted that for all these test structures except A_{VOL} measurements, high speed probe cards are required which can measure signal frequencies in GHz range.

4.5.4 Tests for Lower Level Cells (Boosting Amplifiers)

The boosting amplifiers :

1) Nch level1 : N differential pait, single boosted amplifier. (Fig. 3.15)

2) N ch level2: N differential pair, modified Lu Wu amplifier (Fig. 3.14)

3) Pch level1 : P differential pair, single boosted amplifier (Fig. 3.15)

4) P ch level2 : P differential pair, modfied Lu Wu amplifier (Fig. 3.14)

have been connected in an open loop configuration on a dc test frame because the open loop gain on these circuits is smaller than that of the main amplifier. So, specially configured structures are not required. To determine the ac response of these boosting amplifiers are again connected in a unity gain feedback configuration (as shown in fig. 4.6) and placed in a high speed probe pad frame where settling response can to be measured to calculate the bandwidth of these amplifiers as described in section 4.5.2

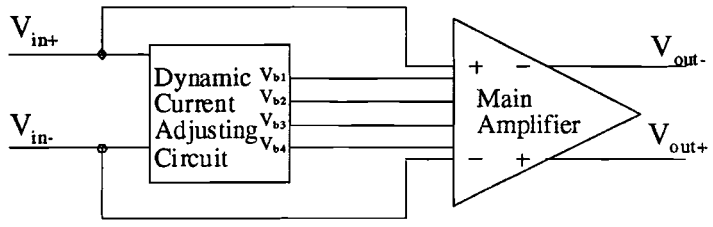

Fig. 5.1 The Low Power Amplifier

5.1 Amplifier Specifications

To keep the thermal noise generated in the transistor channel below the required level of 1/2 LSB of the A/D converter (see section 3.5), this amplifier must drive a load of 350pF. Thus, we can summarize the amplifier specifications as follows:

$A_{vdiff} = 108dB$ (1)

$\omega_{unity} = 2$ Mhz (2)

$C_L = 350pF$ (3)

Input referred noise = 1.25 $\mu V/\sqrt{Hz}$ (4)

5.2 Amplifier Design Approach and Archtitecture

The main feature of this amplifier is the dynamic current adjust circuit which changes the input bias current to the amplifier depending upon the input signal amplitude [22]. The main amplifier is simply a differential only boosted amplifier which has been described in section 3.6. Fig. 5.1 shows the block diagram for the low power amplifier.

5.2.1 The Dynamic Current Adjust Circuit

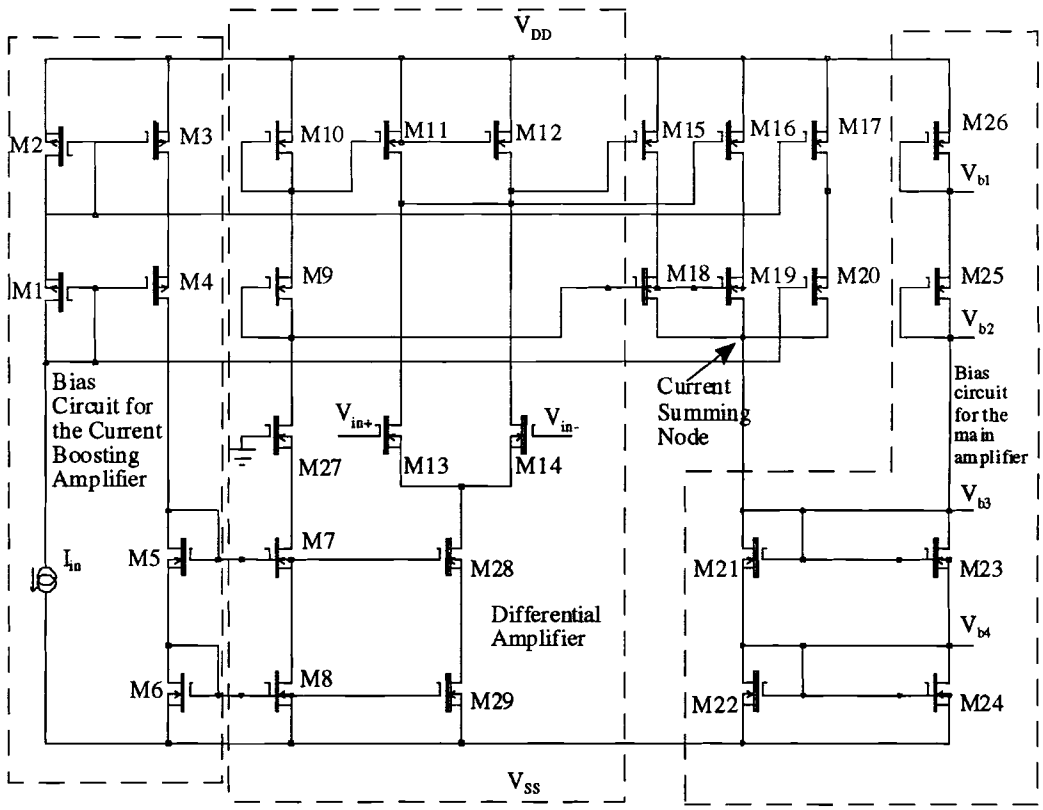

Fig. 5.2 The Dynamic Current Adjust Circuit

The dynamic current adjust circuit of Fig 5.2 forms the heart of the "low power" amplifier. It monitors the signal amplitude at the input of the differential pair and when the signal rises above a "dead band" of approximately 80mV, it increases the biasing current supplied to the main amplifier. All devices in the current adjust circuit are very long channel devices. This is due to the fact that the input quiescent bias current must be very small to minimize overhead power consumption and an overdrive voltage of about 250mV is required to ensure overdrive voltage matching which is very critical for subthreshold operation.. This results in very small W/L ratios for these transistors. The detailed

operation of this circuit is as follows. This circuit can be further divided into two blocks: an absolute value sensing circuit and a bias circuit for the main amplifier. The absolute value sensing circuit is simply a differential amplifier whose outputs act as biasing voltages for current boost transistors M15 & M16 and a current summing node (CSN) which sums the current from the current boost transistors M15 & M16 and the mirroring transistor M17. Thus, this circuit dynamically adjusts the bias current to the main amplifier depending on the signal amplitude. Transistors M1 through M6 form the bias string for the absolute value sensing circuit. These are very long channel devices as described previously. Transistor M27 keeps the voltage variations matched in the legs of the differential pair and the output transistors. Transistors M11 and M12 are the loads for the differential amplifier and these initially are biased to operate in triode region so that the voltage at the output of the amplifier is close to V_{DD} and the current boost transistors M15 & M16 are OFF. This means that the current being supplied to the main amplifiier is just the quiescent bias current which is mirrored by M17. Transistors M13 & M14 form the differential pair. When the differential signal at the input of this circuit rises above the "dead band" the differential pair potentially switches all the current into one leg. The load transistor in that leg is then pulled down into saturation. This lowers the output voltage of the differential amplifier which in turn causes the corresponding current boosting transistor to conduct more current. The current boosting transistor is designed to give a current boost of about 60dB with a 210mV change in V_{GS} along the subthreshold input transconductance slope which is about 70mV/decade . This change in V_{GS} supplies a boosted current which is summed at the CSN. Transistors M21 through M24 mirror that current into the main amplifier by adjusting the

bias voltages V_{b1} through V_{b4} which control the bias current in the main amplifier. The pulling down of the output voltage of the amplifier is accomplished as follows. Transistors M11 & M12 are identical but they are both made slightly narrower than required to mirror exactly twice the current flowing in M10 and wider than M10 so that when the current flowing in these transistors is equal to M10 or less, they are pulled up into the triode region of operation. Since, V_{GS} is constant for these transistor and current is small, V_{DS} must decrease to maintain the reduced current flow (see eqn 22, chapter 2). But when the all the current in the tail of the differential pair flows into a single transistor, the restriction on V_{DS} to be small no longer holds and V_{DS} increases which brings the output voltage down for the amplifier thus, increasing V_{GS} for the boosting transistors. This in turn boosts the current depending on the subthreshold I-V characteristic slope. The current from the quiescent current mirror, M17 and the current boosting transistors M15 & M16 is summed at the summing node to form the bias current for the main amplifier. Transistors M21 through M26 form a conventional cascode bias string for the main amplifier. In summary, this design approach simply changes the input bias current to the main amplifier depending on the absolute value of the input signal amplitude.

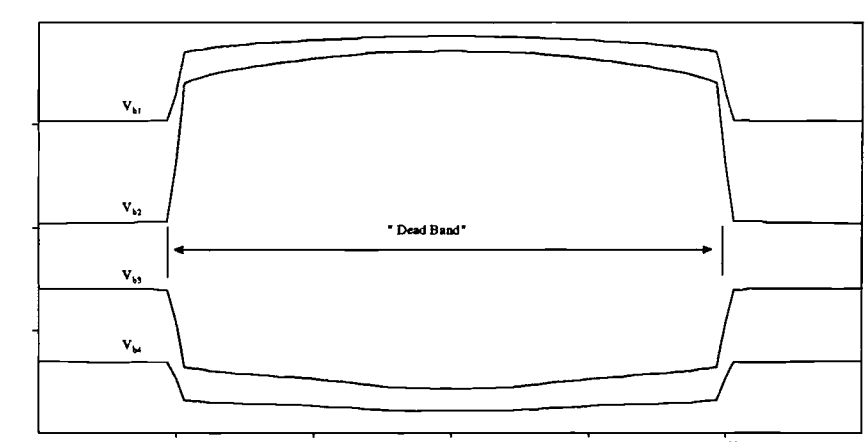

Fig. 5.3 DC Response of the Dynamic Current Adjust Circuit

Fig. 5.3 shows the dc transfer characteristics of the dynamic current adjusting circuit. Notice the dead band extends to about 80mV and the bias voltages then adjust according to the change in the bias current.

5.2.2 Main Amplifier Circuit

The main amplifier circuit is similar to the boosted amplifier presented in chapter 3. One of the characteristics of this amplifier is the longer channel length on all the devices. This is done to help ensure "overdrive matching" on all the devices. All the devices operate in subthreshold region and this is done to achieve a very high dc gain. This amplifier is projected to achieve a dc gain of 120dB. The bandwidth requirement on this amplifier are not very stringent. The required bandwidth to achieve the desired settling time is about 2MHz which is easily attainable. But the load capacitance ,which is very large (about 350pF) to reduce the noise floor, is required due to very high desired Signal to Noise Ratio (SNR). As described earlier the current increase in the differential pair increases the output transconductance of the amplifier and achieves the required bandwidth when the signal amplitude rises above the "dead band". Nch and Pch boost amplifiers are modified Lu Wu amplifiers as shown in Fig 3.4. Single cross coupling as discussed in chapter 3, avoids swing limitation. Typical DC and AC response of this architecture has already been analyzed in chapter 3 and 4. Transient response is of special interest since the amplifier has a variable bandwidth depending on the input signal amplitude but a detailed analysis of the transient response is beyond the scope of this work. Fig. 5.4 shows the main amplifier.

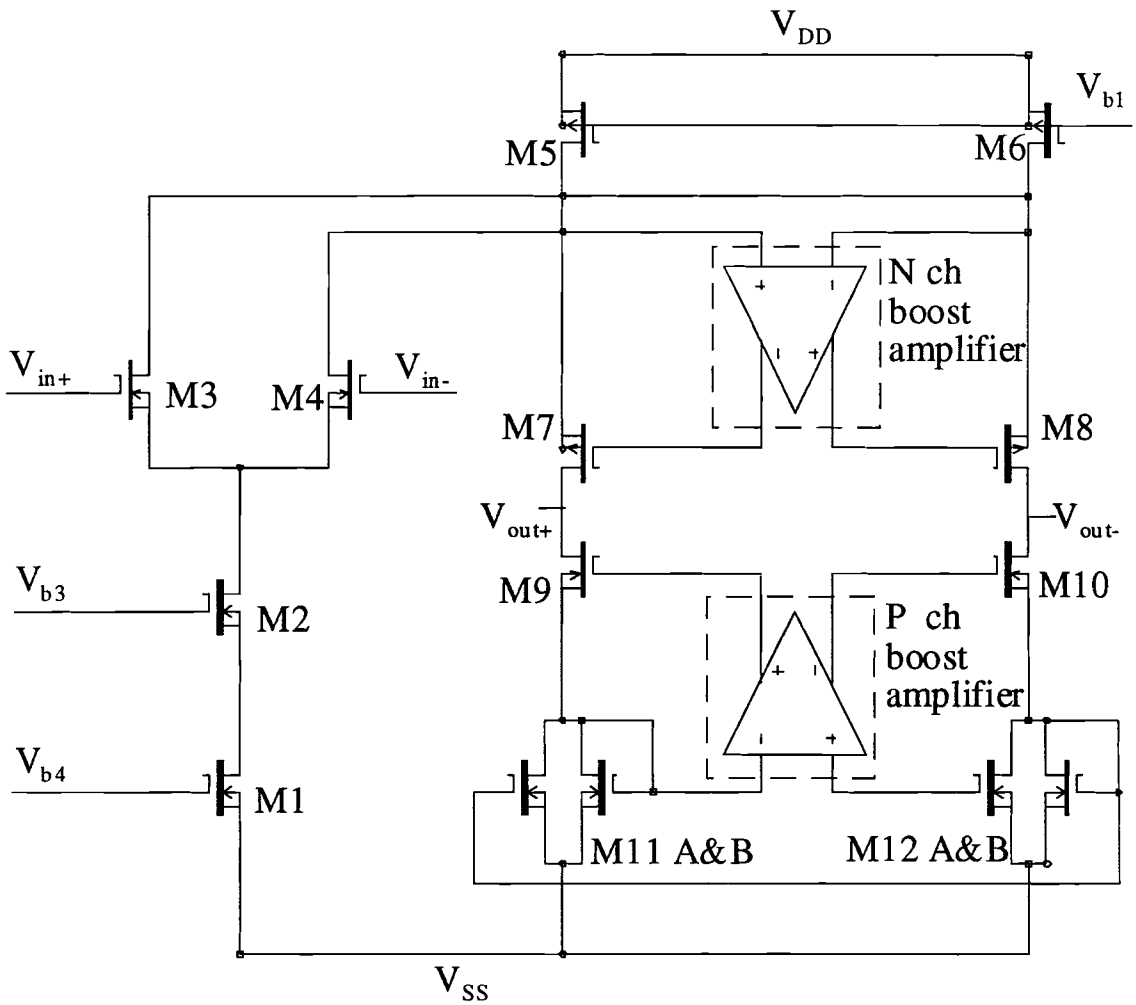

Fig. 5.4 Main Amplifier

Amplifier performance can be summarized in following equations

$A_{vdiff} = (\mu^2/4)^2$ (5)

$A_{vcm} = (2/\mu)$ (6)

$CMRR = (\mu^5/32)$ (7)

$$\omega_{unity} = g_m/C_L \quad (8)$$

5.3 Layout Considerations

The most important consideration in this type of a circuit operating in subthreshold region, is the pairwise device matching. Therefore, laying out matched devices is one of the very important feature of this circuit, since, geometry and layout are the only options at the designer's disposal. Transistors are laid out using fingers as described earlier in chapter 4 and further interdigitizing and multi common centroiding is used to ensure best matching among critical transistor pairs. Fig. 5.5 shows a multi common centroid interdigitized transistor pair layout with a common source.

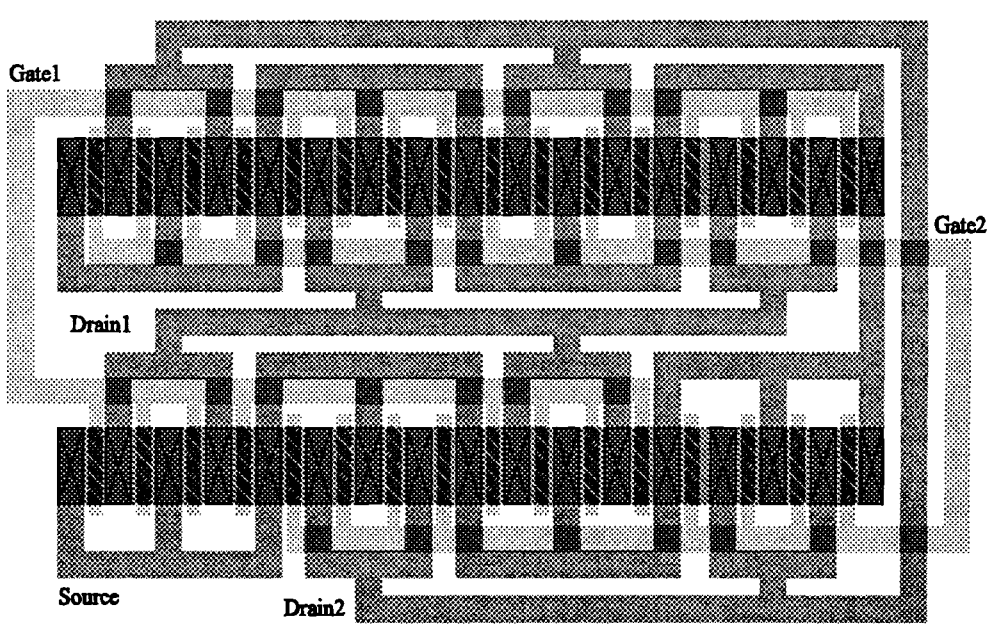

Fig. 5.5 An Interdigitized Multi Common Centroid Transistor Pair

5.4 Testing Approach

High DC gain amplifiers have to be put in special configurations on chip itself to measure the open loop gain and the frequency response of the amplifier. Following sections describe the test structures and the procedures to measure the performance of the low power amplifier and the lower level test cells such as the dynamic current adjust circuit and the boosting amplifiers.

5.4.1 Open Loop Gain Measurement

The opamp is placed in a unity gain feedback configuration using feedback capacitors as shown in Fig. 5.6.

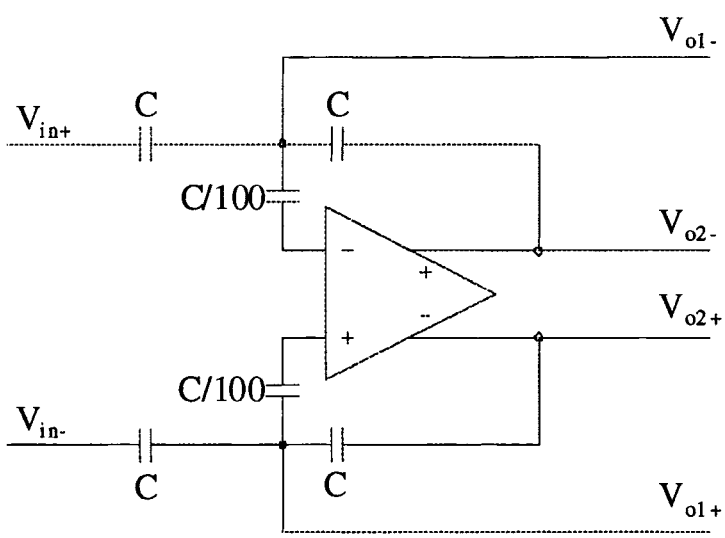

Fig. 5.6 A_{VOL} Frame for Low Power Amplifier

The analysis of this configuration has already been discussed in section 4.5.1

5.4.2 Unity Gain Frequency Measurement

For measurement of the unity gain frequency of the amplifier, the amplifier is again put in a unity gain feedback configuration as shown in fig. 5.7.

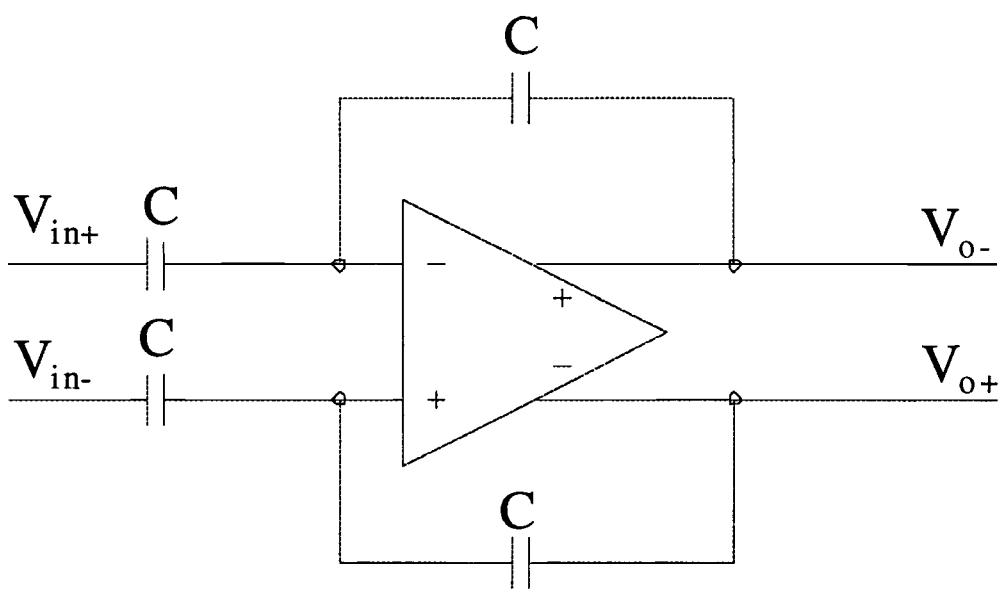

Fig. 5.7 UGBP Frame for the Low Power Amplifier

A step input is applied to the amplifier and the settling behavior of the opamp is measured to calculate the gain bandwidth product of the amplifier. The relation between the settling behavior and performance parameters has already been discussed in section 4.5.2 However, in this case the transient response is affected by variable bandwidth of the amplifier. Note, the kink in the output response just when the bias voltages switch to boost

the current in the main amplifier. As stated earlier, this variable bandwidth response is not properly understood at present and needs a further detailed analysis. Fig. 5.8 shows the unity gain transient response of the main stage of the low power amplifier(without boosting). It is the not the exact response of total amplifier, however, it can give a fair idea of the bandwidth of the amplifier with reduced settling accuracy because of the low DC gain of a single stage without boosting.

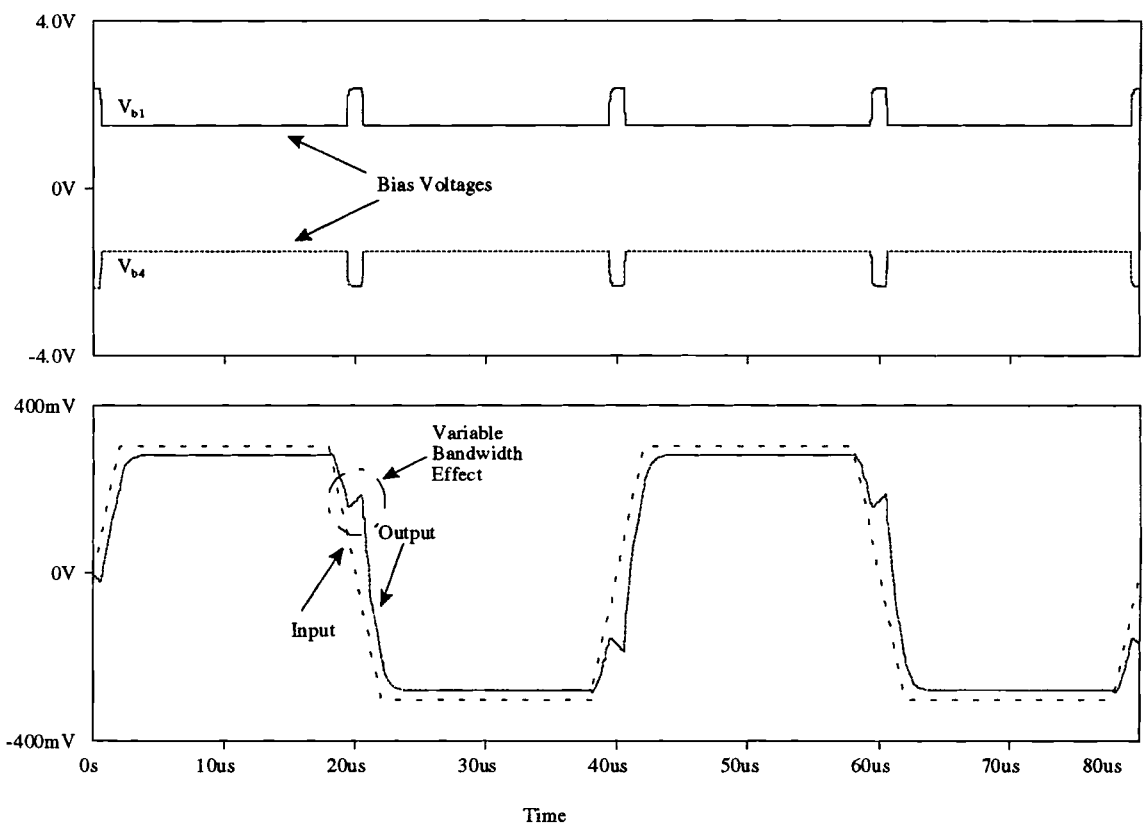

Fig. 5.8 Transient Response of the Variable Bandwidth Low Power Amplifier

5.4.3 Tests for Lower Level Cells

The boosting amplifiers have been connected in an open loop configuration on a dc test frame because the open loop gain on these circuits is smaller than that of the main amplifier. So, specially configured structures are not required. For ac response of these amplifier they are again connected in a unity gain feedback configuration (as shown in fig. 5.7) settling response has to be measured to calculate the bandwidth of these amplifiers as described in section 4.5.2.

The dynamic current adjust circuit is simply connected a dc pad frame in which all the test outputs such as the output bias voltages v_{b1}, v_{b2}, v_{b3} and v_{b4} are connected to the pads. A dc sweep is applied to the input of the circuit and the output bias voltages are observed and thus, the "dead band" can be calculated as shown in the dc response of this circuit in fig. 5.3

CHAPTER 6

CONCLUSION AND SUGGESTIONS FOR FUTURE WORK

The work presented in this thesis holds great promise for future high performance microwave CMOS circuits which will become a reality due of the advances in technology and innovative design techniques. Most important, during the course of this project, the focus was on developing blocks which would be used in a system later on. Therefore, the most obvious direction to go from here is to use these blocks to build high performance systems and verify the promises offered by this work. The most important application for the amplifiers which have been presented in this work lie in the domain of switched capacitor circuits. SC circuits such as A/D converters and filters have wide ranging applications in front end signal processing. A wide band, high DC gain amplifier which employs a fully differential configuration is a critical building block of SC circuits. The amplifiers presented here go a step further in combining many the advantages of the various circuit techniques that have been developed so far with some novel contributions from the authors. With this in mind these amplifiers have achieved very respectable performance figures as far as DC gain, bandwidth and common mode gain. Simulations do indicate this

performance but actual circuits on the chip are yet to be tested. One of the major concerns is that technology also hasn't matured to guarantee performance as predicted by the models used in the simulations. The process is still in the research stages and the design can definitely be improved further which should result in a better performance. For example, in the modified Lu Wu amplifier which has been used as a differential only boosting amplifier, there is a bandwidth reduction due to more load at the source of the cascode transistor compared to the actual Lu Wu amplifier. This point has been made by the authors and an alternate technique has been implemented which does not reduce the bandwidth. Similarly, there is a vast ocean of knowledge which is required to make a folded cascode to operate at $f_T/2.2$ with a 60° phase margin which is the ideal GBP for this amplifier. Boosting introduces poles and zeroes and doublets and the actual effect of all the poles and zeroes combined can be predicted by a simplified analysis but has not been analyzed in detail yet. The analysis being very tedious would require a symbolic simulator and a very careful and a knowledgeable analyst. As is the case all the time, the technology does promise a lot but it will be limited by the laws of physics but only imagination limits the design. Future performance gains will come more from the design approach rather than technological advances. This trend is already visible in the microprocessor segment of the VLSI market where reorganized chip architecture has resulted in much faster processors. Therefore, efforts put in design will reap more dividends because it will be easier to implement them in existing commercialized processes.

The authors have lately discovered literature which discussed cross coupling in one or more different fashions [23], [24] and [25], but Lu Wu [10] are the only one who

specifically point out the importance of cross coupling in reducing the common mode gain. Cross coupling of the mirrors to eliminate common mode feedback has been one of the essential component of the design presented in this thesis. Klass Bult [8] developed cascode gain boosting which is the other key idea in this design. And Fossum et al. [1] through [6], are to be commended for the first comprehensive analysis of short channel SOI MOSFETs and contributing SOISPICE2.21. All these efforts have helped considerably in the development of high performance circuits presented in this thesis.

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