A PROPOSED 10-BIT HIGH-SPEED TWO-STEP NEURAL-BASED ANALOG-TO-DIGITAL CONVERTER

By

JIE ZHENG

Bachelor of Science

University of Science and Technology of China

Hefei, China

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This study was conducted to propose a new architecture for high-speed (2.5-GHz) and high-resolution (10-bit) A/D converter. The key functional blocks of the proposed architecture were designed, simulated and laid-out for fabrication. The 4-bit flash ADC system were tested.

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NOMENCLATURE

I_D	Drain Current
V_S	Source Potential
V_T	Threshold Voltage
V_{TN}	NMOS Threshold Voltage
V_{TP}	PMOS Threshold Voltage
k	Boltzmans Constant
T	Temperature in Degree Kelvin
f	Frequency
R	Resistance
C	Capacitance
LSB	Least Significant Bit
MSB	Most Significant Bit
C_L	Load Capacitance
V_{DD}	Positive Power Supply
V_{SS}	Negative Power Supply
g_m	Transconductance Parameter
R_O	Output Impedance

g_{ds} Drain to Source Transconductance Parameter

V_{IN} Input Voltage

V_{OUT} Output Voltage

V_{REF} Reference Voltage

C_{gs} Gate to Source Capacitance

C_{gd} Gate to Drain Capacitance

C_{ds} Drain to Source Capacitance

CLK Clock Signal

ΔV Gate Overdrive Voltage of MOSFET

ω_T Unity Gain Frequency

τ_X Time Constant of X

t_d Delay Time

GBP Gain Bandwidth Product

V_{OS} Offset Voltage

W/L Width to Length Ratio for the Transistor

μ Transistor Self Gain

V_{FS} Full Scale Voltage

HADC Hopfield Neural Network Analog-to-Digital Converter

V/I Voltage-to-Current Converter

DEM Dynamic Element Matching

CMOTA Current Mirror with OTA

CHAPTER 1

INTRODUCTION

Analog-to-digital (A/D) converters provide the interface between the analog signal domain and the binary digital computational domain. The development of digital signal processor (DSP) technology has increased the use and importance of the A/D converter. A 10 bit A/D converter with a high conversion frequency of over 2.5 GHz is needed for the applications of digital signal processing in telecommunication, networks, image processing, medical engineering system and consumer products. However, the maximum conversion frequency of the existing 10 bit A/D converter still remains in the order of 50-200 MHz [1][2][3].

Without doubt, the flash A/D converter (full parallel converter) gives the best conversion frequency performance. The negative attributes of this converter type are the large die size, high power dissipation and large input capacitance. Flash converter uses 2^n-1 comparators and 2^n matched resistors for n-bit resolution. Thus, the 1023 comparators, which are needed for a 10 bit application, result in large area, high power consumption as well as large input capacitance. Moreover, the input bandwidth is limited if the input is to be driven by a 50Ω signal due to the large buffer needed to drive the ADC's large number of comparators. Even with state-of-the-art technologies the flash architecture is clearly not an acceptable approach for a 10 bit 2.5 GHz A/D converter.

Two-step flash architectures are an effective means of realizing high speed, high resolution A/D converters. With conversion rates approaching half those of fully parallel A/D converter's, this type of architecture provides a relatively small input capacitance together with low power dissipation due to the reduced number of comparators required to achieve the high resolution. A two-step architecture uses a sample and hold circuit together with a high speed A/D – D/A coarse quantizer subtraction circuit. As a part of the effort it was determined that the sample and hold circuit requires a 1590 GHz process bandwidth for 10-bit 2.5GHz application. Such a high-performance sample and hold function is clearly not feasible with existing CMOS technology and is beyond the scope of this effort.

The folding and interpolation architecture, successfully used in high speed and high resolution bipolar A/D converter [1][4], employs considerable fewer comparators than a fully parallel converter and in addition does not require a sample and hold. The result is a high speed, low power dissipation converter with small die area. While incorporating the folding and interpolation scheme with MOS devices, this type converter suffers from an inherent limitation associated with the linearity of velocity saturated MOS devices. The folding factor number is as small as two due to the soft non-linearity of MOSFET differential pair transfer function (see Appendix A). This restriction results in folding CMOS architecture have a large number of comparators and large power consumption as well as matching difficulties. It was also found that the required 2.5GHz bandwidth for a folding architecture with MOS devices is also well beyond the reach of any current process.

Neural networks behave essentially like analog nonlinear circuits. Interconnections between neurons (the elementary processing units) permits one to obtain high parallel computational capabilities, which potentially ensure high speed conversion. The Hopfield neural network is one of the most popular networks for electronic neural computing due to the simplicity of the network architecture and quick convergence in the time domain. Hopfield neural-based A/D converters have several advantages over conventional A/D converters. For a 10 bit Hopfield A/D converter only 45 neurons and 10 voltage to current converters are required. Thus, this architecture has a significantly smaller area than the fully flash A/D converter which employs 1023 comparators in the 10 bit case. By adjusting the contribution values between the amplifiers with a learning rule, the adaptive A/D converter with linear A/D conversion performance can be made. The adaptability of a neural-based A/D converter can be useful to compensate for initial device mismatches or long-term characteristic drifts. However, the conversion rate performance is constrained by the worst case delay of LSB (Least Significant Bit) when neural-based architecture applies to 8 ~ 10 bit resolution. The worst case delay happens when the variation of input signal causes the digital output to be changed from 100...00 to 011...11, or from 011...11 to 100...00. Moreover, the great size differences (up to 64 ~ 256) between neurons used in 8 ~ 10 bit application makes their matching very difficult to meet the resolution requirements. Therefore, the neural-based converter is suitable for the 4 ~ 5 bit resolution application and as previously noted has many advantages over the 4-5 bit flash A/D converter.

1.1 Objective

The objective of this thesis is to investigate and propose a new type A/D converter architecture for high speed and high resolution application and has resulted in a two-step neural network-based A/D converter. This research presented here is based on a review of two-step flash A/D converters, analysis of the folding and interpolation scheme, and Hopfield neural network A/D converters. The analysis and testing results of 4-bit flash A/D converter cells are also used to support this proposal.

Incorporating the Hopfield neural network architecture into the two-step combines the advantages of both neural and two-step ADC. It is potentially a solution and currently the best choice for a 10 bit 2.5 GHz A/D converter although a high speed track and hold circuit is still needed for this architecture.

1.2 Organization

Chapter 1 has introduced the background and the purposes for this study.

Chapter 2 reviews the architectures of high-speed and high-resolution A/D converters: flash ADC, two-step ADC, folding and interpolation ADC, and neural-based ADC. The critical block functions of A/D converter, i.e., comparators, D/A converters, are also reviewed. The factors limiting accuracy are presented in this chapter.

Chapter 3 includes one architecture of 4-bit flash A/D converter system. The analysis, circuit simulations and test results have shown that high speed performance could be reached with proper laid-out and fabrication. The testing results of this 4-bit

ADC system and six functional testing subcells, which were fabricated on the IBM 0.1μm SOI/SOS process, are also presented.

Chapter 4 presents a Hopfield neural network A/D converter. The conversion rate, which is correlative with worst case delay of LSB, is calculated and confirmed by simulation. Three kinds of voltage-to-current converters, the key function block used in Hopfield neural network A/D converter, are analyzed. Based on the above work, the two-step neural-based A/D converter is proposed and its performance is estimated.

Chapter 5 summarizes the results of the study, conclusions, and recommendations.

Appendix A includes the analysis of a folding and interpolation architecture for velocity saturated CMOS process. The simulations support the result that the limitation of soft non-linearity of MOSFET differential pair restricts the maximum folding number while applying MOS devices to this architecture. For each of three stages: folding, buffer, and comparator, the requirements of matching and offset are described. The bandwidth requirement of process is analyzed and power dissipation of comparators is discussed.

CHAPTER 2

LITERATURE REVIEW

Traditional analog-to-digital converter designs have used a flash architecture to obtain high conversion rate and a sigma-delta architecture to obtain the high resolution. For the resolutions greater than 8 bits, the fully flash A/D converter suffers from severe disadvantages. Not only the large area (exponential growth) and power dissipation but also the performance limitations due to a highly nonlinear input capacitance and reference mismatching problems have stimulated the development of multistage A/D converters, folding and interpolation A/D converters, and neural network-based A/D converters.

The first section of this chapter reviews the flash A/D converter followed by three different kinds of architectures for realizing high-speed and high-resolution analog-to-digital converters: two-step, folding and interpolation, and the Hopfield neural network. The second section reviews the factors limiting the accuracy of ADC systems. The third section presents three kind of comparators as well as their performances and limitations. The digital-to-analog converter, an essential block function for multistage ADC, is reviewed in the last section.

2.1 High-Speed ADC Architectures

In this section, we will see a brief overview of four commonly used high-speed A/D converters, i.e., flash, multi-step, folding and interpolation and Hopfield neural network, as well as their performances. The best-known flash architecture shows a excellent speed performance. However, this architecture requires 2^N -1 comparators to achieve an N-bit resolution. The alternatives to a full-flash architecture are the multi-step, folding and interpolation, and neural network A/D conversion principles. These architectures are capable of achieving a large analog bandwidth and high resolutions without incurring the power and area penalties associated with the flash architectures.

2.1.1 Flash A/D Converter

Flash converters are the standard approach for realizing very-high-speed converters, as seen in some publications [15][16][17]. The input signal in a flash converter is fed to 2^n-1 comparators in parallel, as shown in Figure 2.1. Each comparator is also connected to a different node of the resistor string. Any comparator connected to a resistor string node where V_{REF} is larger than V_{IN} will have a '1' output while those connected to nodes with V_{REF} less than V_{IN} will have a '0' outputs. Such an output code word is commonly referred to as a thermometer code since it looks quite similar to the mercury bar in a thermometer. Note that the top and bottom resistors in the resistor string have been chosen to create the 0.5 LSB offset in an A/D converter.

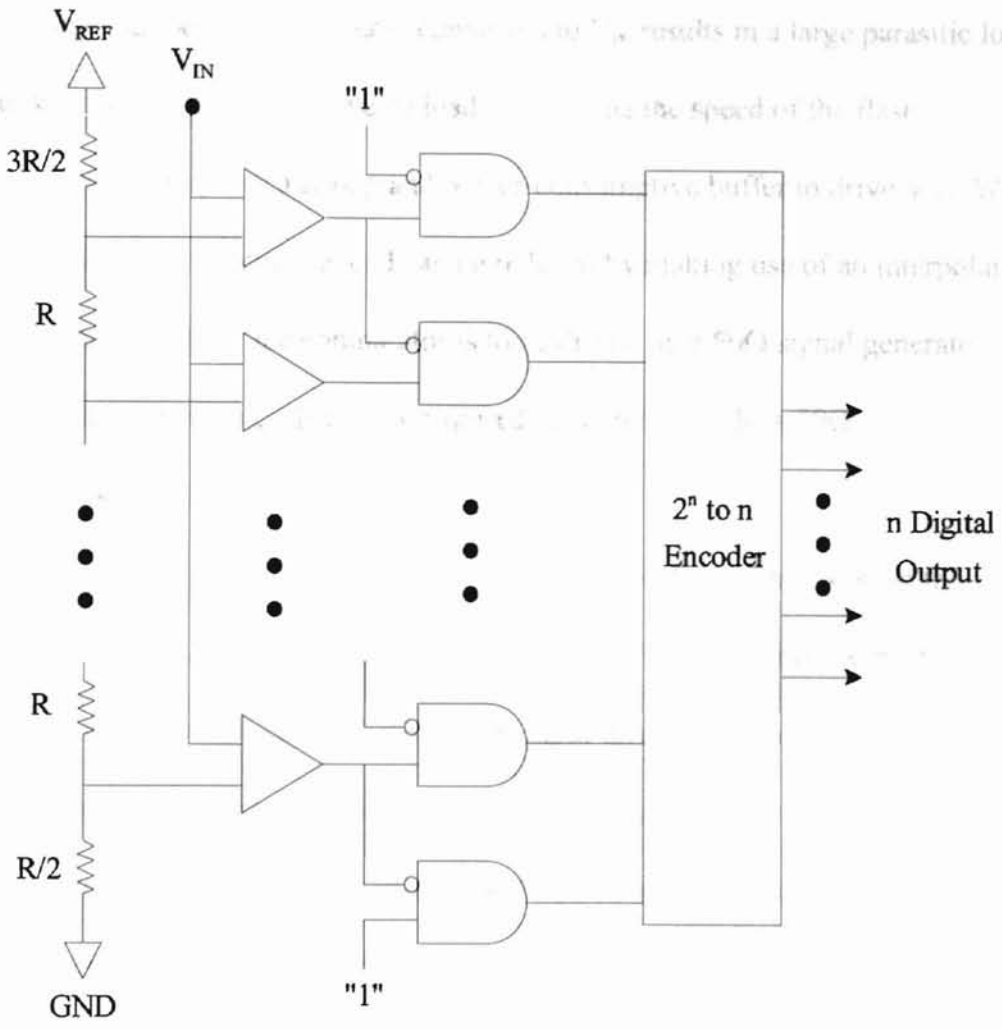


Figure 2.1 A Typical Flash A/D Converter System Diagram

Some of the important design issues that should be addressed when building high-speed flash A/D converters are outlined as follows.

• Input Capacitance Load

The large number of comparators connected to V_{IN} results in a large parasitic load at the node V_{IN}. Such a large capacitance load often limits the speed of the flash converter and usually requires a strong and power-consumptive buffer to drive V_{IN}. We shall see that this large capacitance load can be reduced by making use of an interpolation architecture. Specifically, if the comparator is to be driven by a 50Ω signal generator, C_{IN} should be less than $1/(2\pi R\omega)$, where ω is required bandwidth and R is 50Ω.

• Reference Resistor String Nonideality

A primary factor determining the basic DC linearity of any flash ADC is the matching that is obtained in the elements of the resistor divider. Uniform reference levels must be established without being affected by the input drive requirements of the bipolar inputs or the setup time of the capacitor levels during the autozero interval. Matching of the resistor ladder elements depends partially on the patterning techniques that are used in the fabrication process. It is also dependent on geometry, which is dictated by the layout and the particular process. The accuracy of reference resistor string is limited to 5-6 bit [31].

• Sampling Clock Jitter

The sampling clock jitter, a function of the sample/hold (S/H) circuit noise, is critical in determining the maximum frequency that can be converted by an ADC system. Therefore, it must be designed to be very small. Internally, a small rise or fall time of the

sampling clock avoids additional jitter caused by noise of the clock amplifier circuits. This requires large geometry transistors to be used in the amplifier circuits to control thermal or kT/C noise ($\Delta t = \frac{\sqrt{kT/C}}{\pi f_{CLK} V_{FS}}$, or for comparator switches at 1GHz, $\Delta t = 0.09$ps). Furthermore, crosstalk with the other circuits in the vicinity must be minimized to avoid modulation of the sampling clock.

• Clock Skew and Input Signal

Even very small differences in the arrival of clock or input signals at the different comparators can cause errors. For a high speed input signal, it would only take very small time to change through 1 LSB ($\Delta t < \frac{1}{\pi f_B 2^{n+1}}$, or at 1GHz, $\Delta t < 5$ps and 0.16ps for 5 bit and 10 bit respectively). If there is a clock skew between comparators greater than 1 LSB, the converter will then produce a false logic function. One means of easing this problem is to precede the converter by a sample-and-hold circuit. However, accurate high-speed sample-and-hold circuits can be more difficult to realize than the flash converter itself. It should also be noted that the delay differences may not be caused just by the routing differences of clock and V_{IN} signals, but could also be caused by process variation of drives, switches and capacitance loading.

2.1.2 Multi-Step A/D Converter

To avoid some of the problems encountered with a full-flash converter the multi-step architecture was developed [21-24]. Multi-step A/D converters employ much fewer

comparators than the flash ADC with insignificant sacrifice of conversion rate. Since three or more stages have the difficulties of complex sample and hold circuits with little additional reduction in area, the two step has become the prevalent solution for high speed A/D converter with a resolution of 8-10 bits. Specifically, two-step converters require less silicon area, dissipate less power, have less input capacitance load, and the voltage which the comparators need to resolve are less stringent than for flash equivalents. However, two-step converters do have a larger latency delay, although their throughput approaches that of flash converters. The general block diagram for a two-step converter is shown in Figure 2.2.

The operation of this two-step converter is as follows. The m-bit MSB A/D determines the first m MSBs of n bit digital output. To determine the remaining LSBs, the quantization error is found by reconverting the m-bit digital signal to an analog value using the m-bit D/A and subtracting that value from the input signal. With this approach, rather than requiring 1023 comparators as in a 10-bit flash converter, only 62 ($2^m+2^{n-m}-2$, here m=5, n=10) comparators are required for a two-step A/D converter. However, this straightforward approach would require all the components to be at least 10-bit accurate. Furthermore, two-step converters require accurate DAC conversion and a summing circuit.

Based on the different approaches to process the residual signal, the two-step flash A/D converter is categorized into three kinds of architectures: subranging, two step with residual scaling and subranging with partial scaling. These architectures, as well as their performances and limitations, are presented as follows [30].

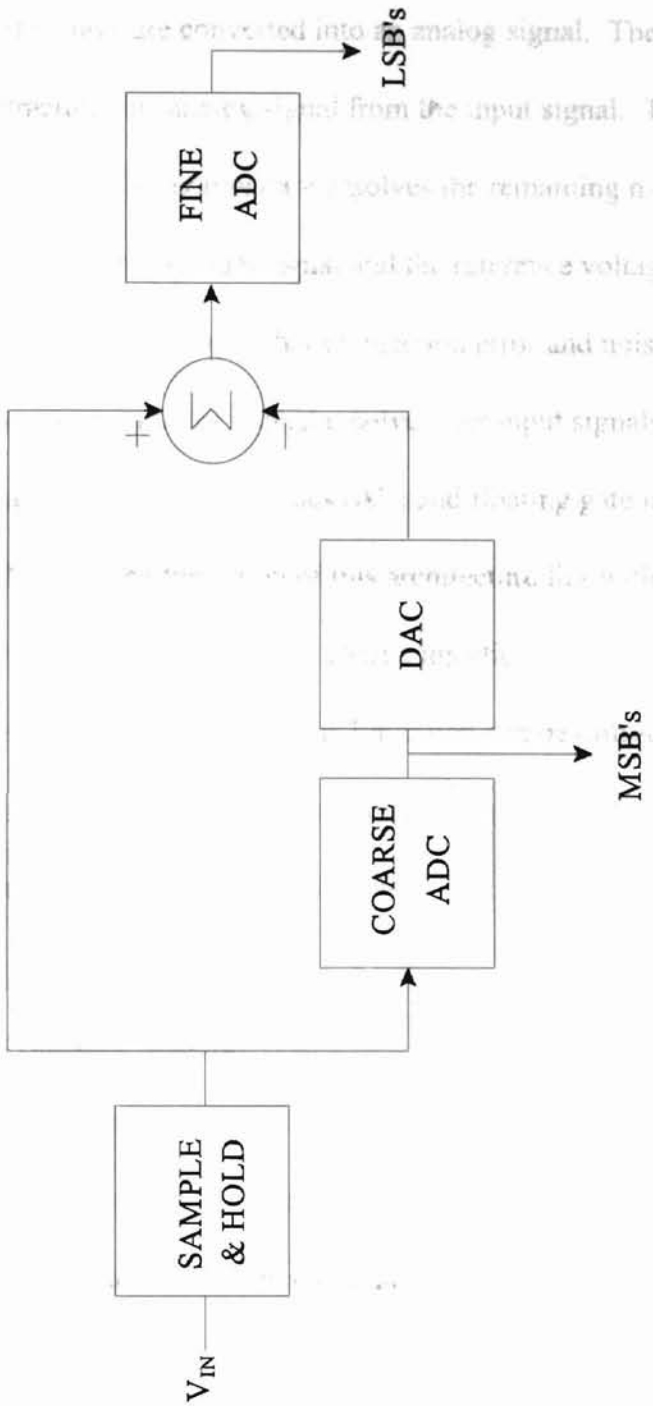


Figure 2.2 Two-Step A/D Converter System Block Diagram

2.1.2.1 Subranging Architecture

The subranging architecture is shown in Figure 2.3 [30]. The m-bit digital outputs of the first A/D converter stage are converted into an analog signal. The residual signal is then computed by subtracting this analog signal from the input signal. The second set of comparators referred to as the fine comparator resolves the remaining n-m least significant bits by comparing the residual signal and the reference voltages of the second stage. Static and dynamic offset voltage, charge injection error and noise are critical to the fine comparator stage operation, as it must resolve finer input signals. Offset voltage can be minimized using autozeroing techniques (AZ) and floating gate injector trimming (Fowler tunneling) [12][29]. The limitation of this architecture lies with the difficulty of designing fine comparators whose noise floor, charge injection/redistribution, and static errors must be maintained below 1/2 LSB. This limitation can be mitigated by the use of a residual amplifier at the cost of an increase in settling time associated with the linear gain amplifier as in the following two step architecture.

2.1.2.2 Two-Step with Residual Scaling

A two-step residual scaling architecture is shown in Figure 2.4 [30]. The residual signal is obtained by subtracting the reconstructed analog signal from the input signal and amplifying it 2^m times. The same set of reference strings and comparators can optionally be used in the second stage to resolve the fine bits. This approach eliminates matching requirements between them but increases settling speed and complexity. As the input signal can be quite large for both stages and comparators often need not be autozeroed.

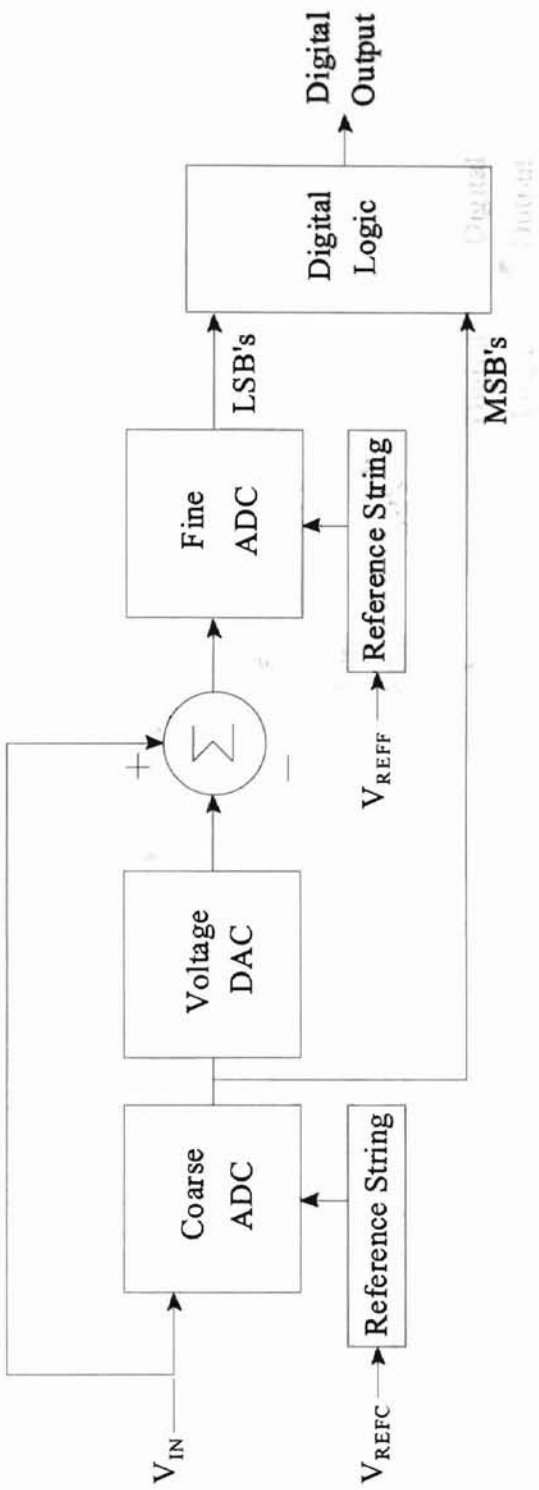


Figure 2.3 Two-Step Subranging A/D Converter System Block Diagram

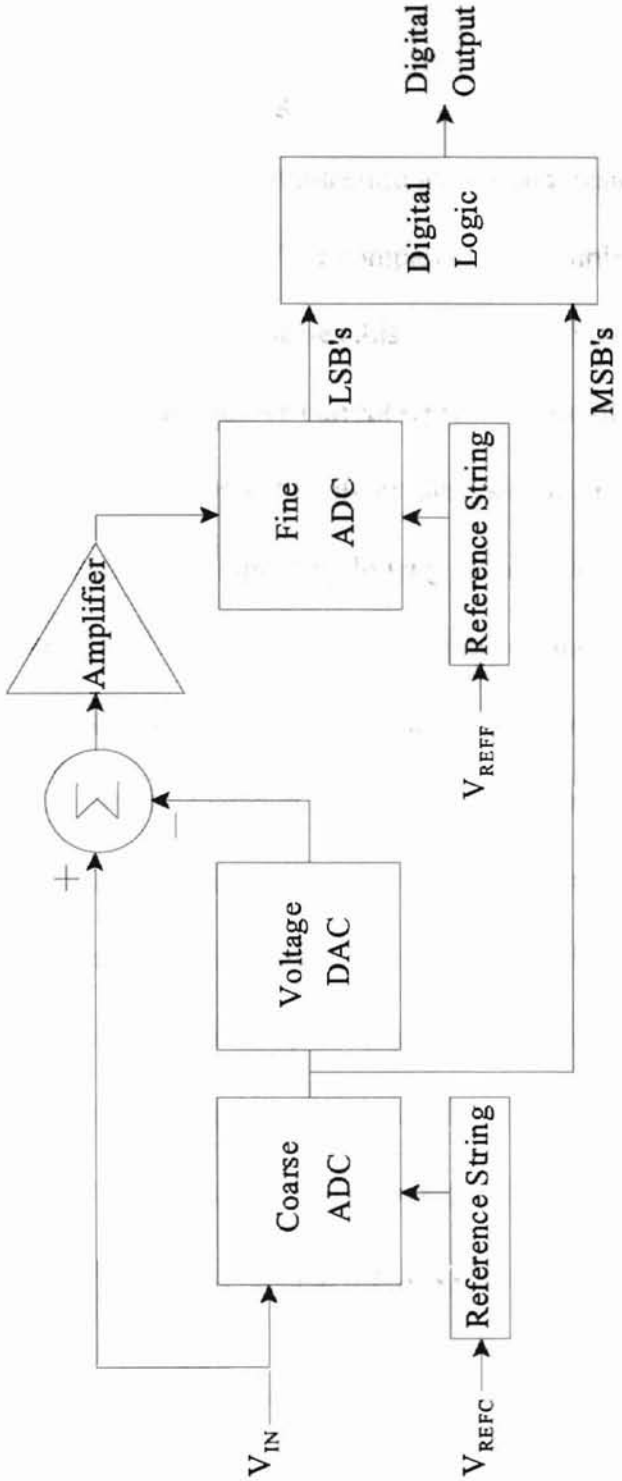


Figure 2.4 Two-Step with Residual Scaling A/D Converter System Block Diagram

However, a longer settling time associated with the residual scaling amplifier makes it less attractive, since a high conversion speed is our main objective.

2.1.2.3 Subranging with Partial Scaling

A two-step subranging ADC architecture with partial residual scaling is shown in Figure 2.5 [30]. The first stage uses 2^m - 1 comparators for implementing the coarse A/D converter to generate the MSB's and passes this result on to the switched current DAC. Note that the DAC generates a negative current representation of the coarse signal. Current mode summing is then applied to obtain the residual signal. This approach potentially reduces the conversion speed by lowing the parasitic capacitance while providing a means to control the time constant by selecting the summing node resistor R_{SUM}. This comes with a high price in area and power to maintain accurate high bandwidth voltage to current conversion. Voltage to current converter (VIC) is required to convert the input voltage signal to its current equivalence before summing across R_{SUM} in developing the residual voltage signal. This residual signal is scaled as much as m times to ease the accuracy and noise requirements of the fine comparators and then buffered to reduce the parasitic capacitance (or settling time) of the summing node. The use of m scaling means the fine comparators are required to resolve only m times the 0.5mV differences ($m\frac{V_{FS}}{2^{n+1}}$). This method offers a means to overcome the large amplifier settling time associated with the fully residual scaling by: (1) partial scaling of the residual signal, and (2) buffering to ease the settling time of the summing node due to the distributed parasitic capacitance. As previously noted partial residual scaling also

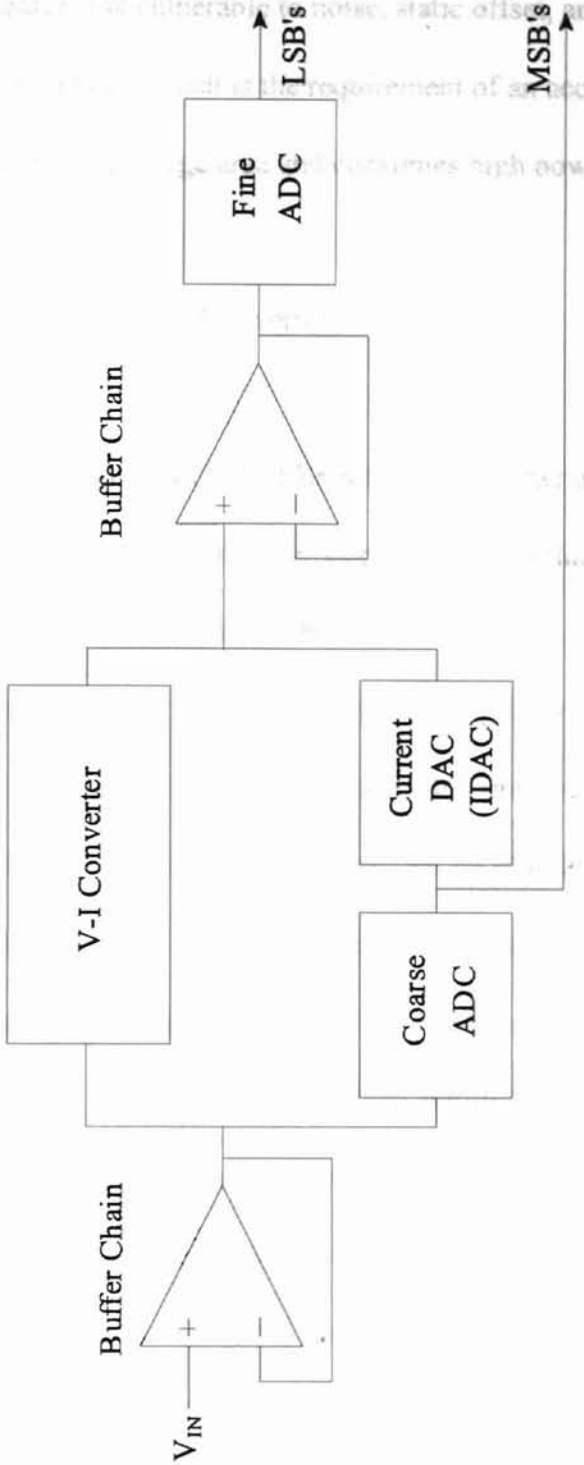
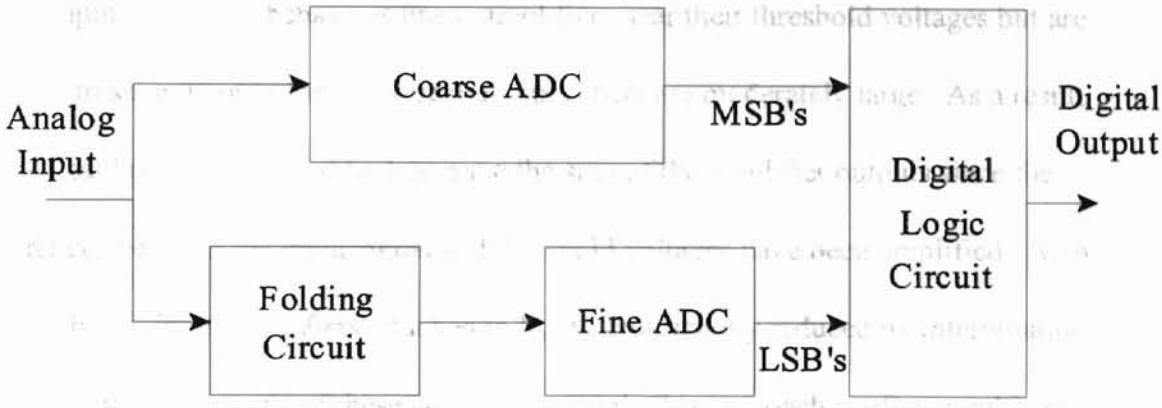


Figure 2.5 Subranging with Residual Scaling A/D Converter System Block Diagram

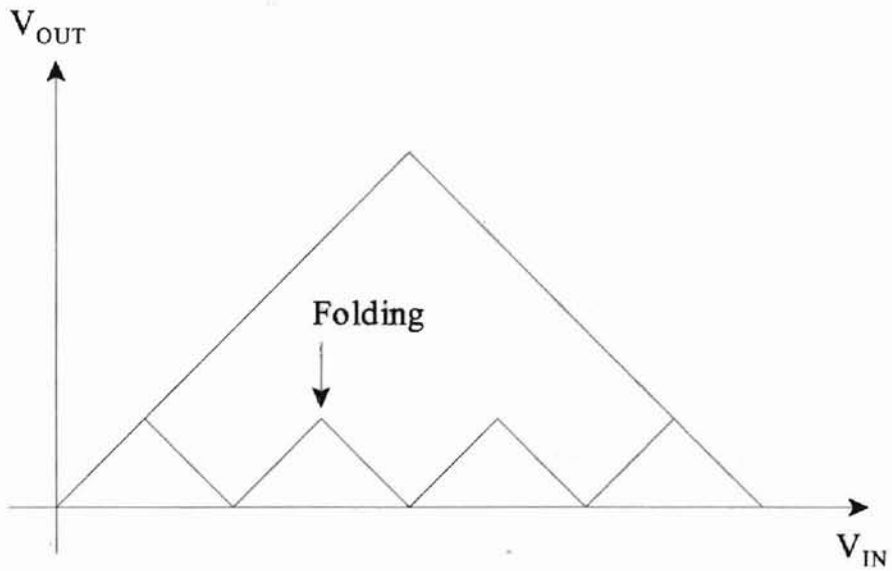
makes the fine comparator less vulnerable to noise, static offset, and charge injection errors. The weakness of this approach is the requirement of an accurate high speed V/I converter which takes up a very large area and consumes high power.

2.1.3 Folding and Interpolation A/D Converter

Folding and interpolation are two different A/D converter architectures. A folding A/D converter is similar in operation to a two-step converter in that a group of LSBs are found separately from a group of MSBs, as shown in Figure 2.6. However, while a two-step converter requires an accurate D/A converter, a folding converter determines the LSB set more directly through the use of nonlinear analog preprocessing and simultaneously determines the MSB set. Also note that no sample-and-hold is required in this system implementation[6][20]. The architecture uses analog preprocessing to transform the input signal into a repetitive (the folding in time) output signal to be applied to the fine converter. In this system the most significant bits are determined by the coarse quantizer, which determines the number of times a signal is folded. The fine bits are determined by the fine quantizer which converts the preprocessed "folded" signal into the fine code. In this way, it is possible to obtain an 10-bit resolution with only 62 comparators (5-bit coarse and 5-bit fine). Furthermore, the sampling of the analog signal at the same clock edge does not require the need for a sample-and-hold amplifier. The low component count results in a small die area and a reduction in power. One drawback, however, is the higher repetition rate of the folded input signals that can result in rounding-off the tips of the folded signal [28]. This rounding-off problem can result in a



(a) A typical folding system diagram



(b) Folding circuit: output signal as a function of input signal

Figure 2.6 A Folding ADC Architecture

loss of resolution at the high-frequency end of the input spectrum in the conversion process.

The interpolation converters make use of input amplifiers, as shown in Figure 2.7. These input amplifiers behave as linear amplifiers near their threshold voltages but are allowed to saturate once their differential inputs become moderately large. As a result, noncritical latches only need to determine the sign of the amplifier outputs since the differences between the input signal and threshold voltages have been amplified. Also, the number of input amplifiers attached to V_{IN} is significantly reduced by interpolation between adjacent outputs of these amplifiers. While this approach is often combined with a folding architecture [6][28], the interpolation architecture has also been used quite successfully by itself [4].

Incorporating the interpolation technique into the folding topology, the folding and interpolation architecture has the advantage of both folding and interpolation. The advantage is that the large number of comparators can be significantly reduced through creating only a small number of folding signals and deriving the remaining folding signals by the resistive interpolation between the outputs of two adjacent signals. A linear interpolation between the two adjacent signals with an accuracy less than 0.5 LSB of the interpolated system is required. In this case, the 32 folding signals necessary for the 5 least significant bits are derived from a four times interpolation between eight output signals of the folding encoder. Thus, this architecture is very suitable for high-resolution converters which require a large analog bandwidth.

The folding and interpolation architecture has been successfully used in bipolar process [4][5][6]. Nevertheless, as stated in the Appendix A, the inherent limitation of

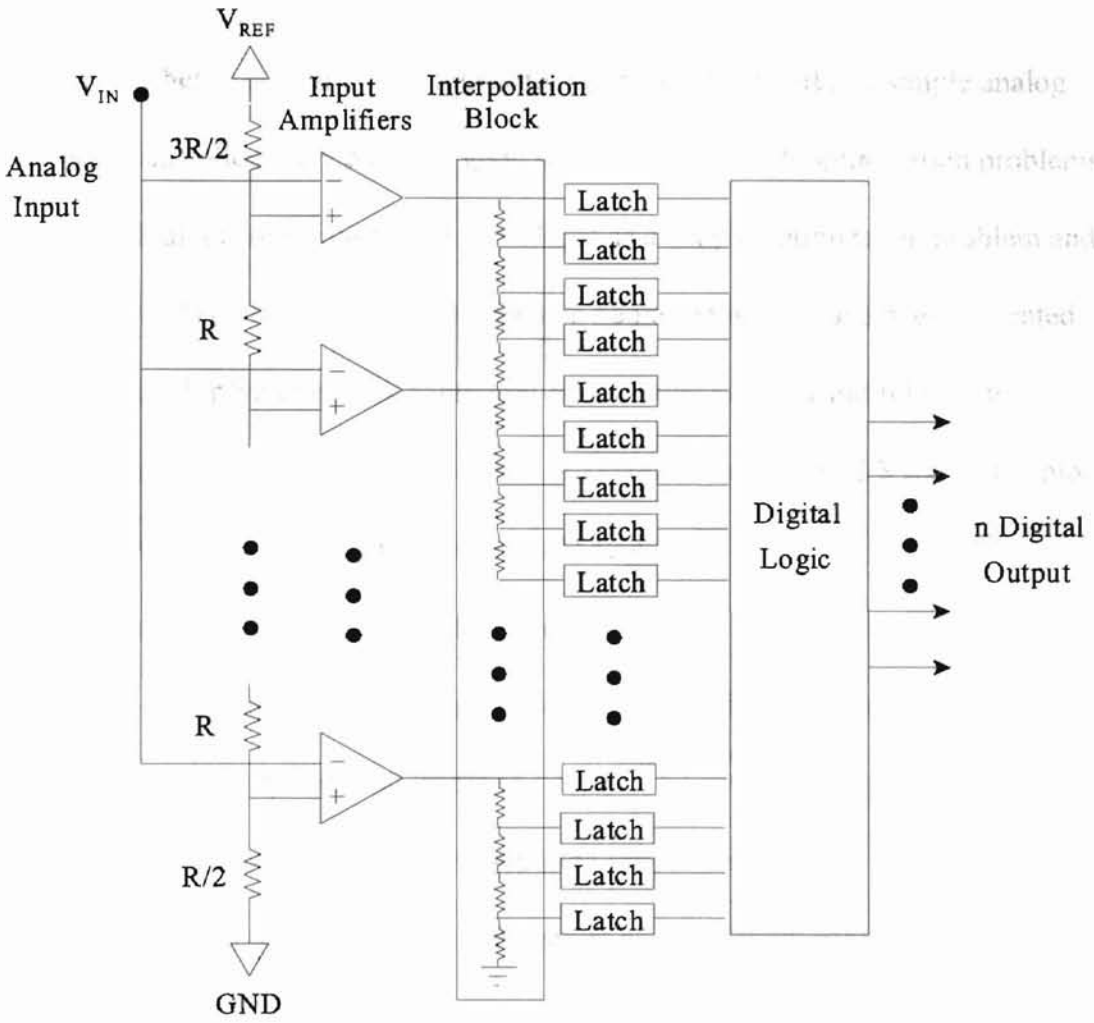


Figure 2.7 An Interpolation ADC Architecture

soft non-linearity of MOSFET differential pairs restricts its potential application to the subthreshold MOS processes.

2.1.4 Neural Network A/D Converter

It has been shown [8] how highly interconnected networks of simple analog processors can collectively compute good solutions to difficult optimization problems. Analog-to-digital conversion can be considered as a simple optimization problem and thus several A/D conversion systems based on neural-networks have been presented [8][9][10]. A Hopfield network composed of one-layer neurons and fully connected feedback resistors can be used to realize an A/D converter. Figure 2.8 shows the block diagram of typical Hopfield neural-based A/D converter.

In this Hopfield network, simple decision-making amplifiers and a resistive network are used. Each noninverting amplifier has a sufficient voltage gain to function as a comparator with output digital levels of 1 or -1. The amplifier outputs are fed back to the amplifier inputs with the densely connected resistive network.

Due to the inherently simple architecture and massively parallel processing capability, the neural-based circuits will potentially play an important role in the next-generation A/D converter systems.

The high-speed ADC architectures, fully flash, multi-step, folding and interpolation, and neural network, are summarized as follows.

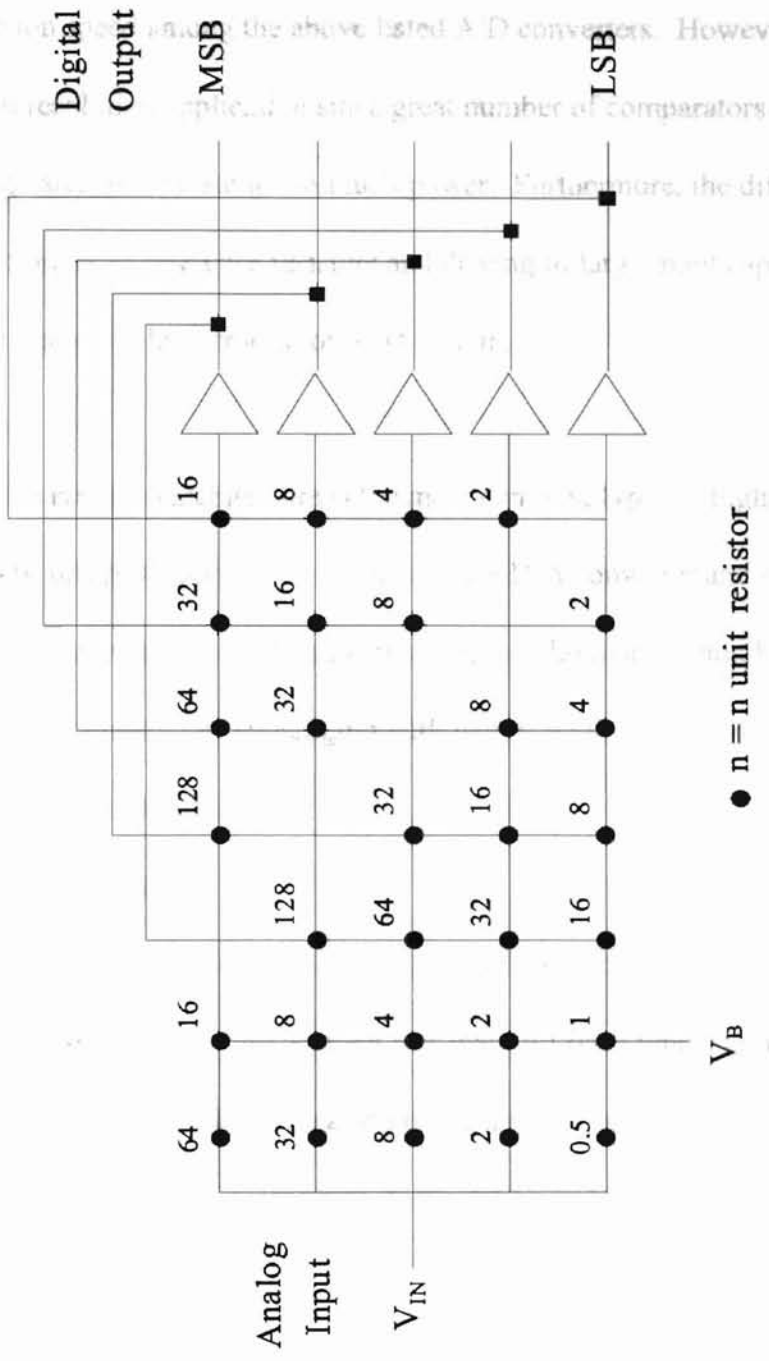


Figure 2.8 A Typical Hopfield Neural Network ADC Architecture

• Flash ADC

This architecture is very suitable for 4-5 bit resolution application because it has the highest conversion speed among the above listed A/D converters. However, it cannot be used for 8-10 bit resolution application since great number of comparators employed result in a very large area and consume too much power. Furthermore, the difficulties in matching of great number of reference resistors and driving of large input capacitance also restrict its application in high resolution A/D system.

• Multi-Step ADC

Currently, the two-step architecture is the most common type for high-speed and high-resolution (8-10 bit) ADC application. An accurate D/A converter and summing circuit are needed in this architecture. Moreover, it requires high-speed and high-resolution sample/hold circuit. The subranging with partial scaling type requires high accurate V/I converter additionally.

• Folding and Interpolation ADC

It has been successfully used for A/D converter in bipolar process. The number of comparators needed in this architecture is much less than full flash type and no sample/hold circuit is needed. Both the area and power are much smaller than that of flash ADC. Nevertheless, this architecture has its limitation in MOS process due to the soft non-linearity of MOSFET (see Appendix A).

• Neural Network ADC

This architecture is potentially an important implementation for high-speed ADC since its simplicity in circuit and fast conversion process. In theory, neural network ADC

offer an on-board trim to eliminate the requirement for high accuracy component matching. The worse case delay in LSB restricts its application for 8-10 bit resolution ADC. In Chapter 4, a new two-step neural-based ADC will be proposed to achieve high-speed and high-resolution performances, which incorporates neural-based ADC into a two-step ADC.

2.2 Factors limiting accuracy

Among the sources of A/D converter errors, the static offset voltage, dynamic offset voltage, and thermal noise are three major sources affecting the system accuracy. This section presents and discusses these major sources of error as well as the critical design issues and parameters. The DAC error sources as well as reference errors will then be discussed in this section.

2.2.1 Static Offset Voltage

Input amplifiers, output amplifiers, and comparators in practical circuits inherently have a built-in offset voltage. This offset voltage is caused by the finite matching of components primarily and is referred to as the static offset voltage, which is given by [11]

$$V_{os} = [\pm\Delta V_T \pm \frac{1}{2}\cdot(\frac{\Delta\beta}{\beta})\cdot\Delta V \pm \frac{1}{2}\cdot\frac{\Delta\beta}{\beta}\cdot\Delta V_T]\cdot\sqrt{N_p} \qquad (2.1)$$

where V_T and β represent the threshold voltage and transconductance respectively, ΔV_T and $\Delta\beta$ are the variations in the threshold voltage and transconductance respectively, and N_p is the number of transistor pairs, i.e., differential pairs and current mirrors.

The static offset voltage is very important for system DC performances. Note that Fowler trimming or an autozero procedure [12] can be used to remove the static offset in a system. Furthermore, care must be taken during the layout of the circuit. The static offset voltage can be minimized by using common centroid geometry and multiple transistor fingers layout scheme in conjunction with inter-digitation.

2.2.2 Dynamic Offset Voltage

The charge injection mismatch resulting from channel inversion and clock feedthrough creates an offset voltage referred to as dynamic offset voltage. The charge injection mismatch due to channel inversion is caused by the redistribution of charge. When a switch is closed, the switching transistor is made conductive by mobile carriers that are attracted into the channel by the gate voltage. For charge equilibrium, the total charge of the mobile carriers in the channel must be equal to the total charge stored in the gate. The redistributed charge on the gate in strong inversion is given by:

$$Q = C_{gs} (V_{gs} - V_T) \tag{2.2}$$

The redistribution of this charge is a function of terminal impedance on both ends of the switch. Therefore, any mismatching in switch transistor dimensions, input or output

impedance, parasitic capacitance and threshold voltages can result in what is referred to as dynamic offset voltage.

The clock feedthrough error is caused by the mismatch charge absorption when autozeroing technique is used in comparators. This error voltage is given by:

$$V_{os} = \frac{\Delta Q}{C_{AZ}} \cdot \frac{(g_{mc} + g_{ml})}{g_{mi}} \tag{2.3}$$

where ΔQ is the channel charge mismatch of switches, C_{AZ} is the input sampling or autozero storage capacitor, and g_{mc}, g_{ml}, g_{mi} are the transconductance value of the comparator, load, and input circuit, respectively (see Figure 2.9).

The dynamic offset voltage must be kept below 1/2 LSB of the A/D system by proper design and layout. Several guidelines can be used to minimize the dynamic offset voltage [11]. First, the large load capacitance will significantly reduce the clock feedthrough but at the expense of slowing down the setting time and reducing the bandwidth. Second, the large V_{GS} will minimize the threshold voltage mismatch but at the expense of increased power consumption due to decreased headroom. Third, small clock voltage swing to the point where the switch just turns on and off reduces the clock voltage coupling effect. Fourth, a good common mode rejection ratio of fully differential pairs with good matching reduces the clock feedthrough voltage since clock signal appears, to the first order, as a common mode signal.

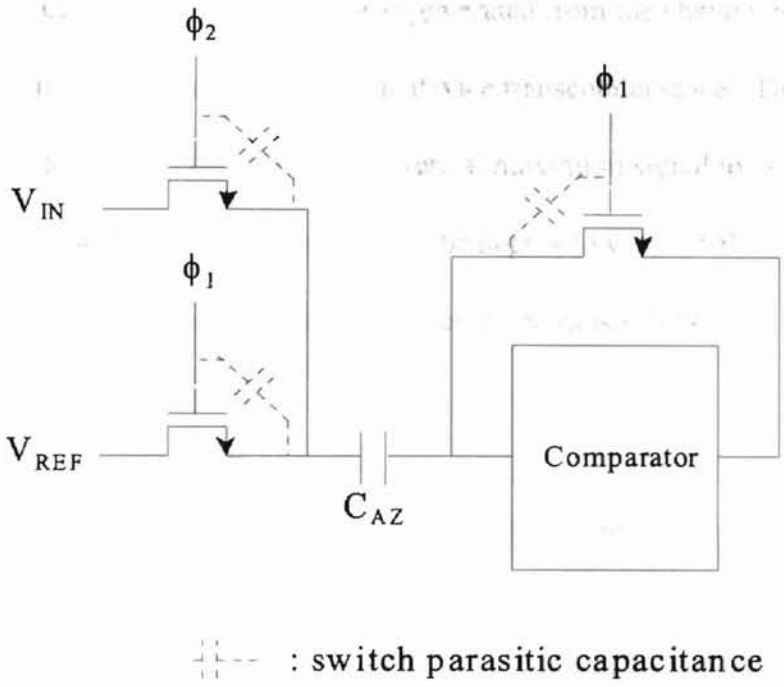


Figure 2.9 Comparator with Autozeroing Technique

2.2.3 Noise

Noise of current sources, amplifiers, resistors, and so on, add to the A/D system errors. Among the noise sources in CMOS devices, the thermal noise is the most significant one since the MOS transistors exhibit small flicker noise and shot noise [11]. The thermal noise in an MOS transistor is generated from the channel resistance, and its magnitude is inversely proportional to the device transconductance. The thermal noise exhibits itself as a deviation from the theoretical maximum signal to noise ratio that an ideal converter can have. Therefore, it must be kept below 1/2 LSB. The mean-square noise values of the thermal noise sources in an MOS transistor is

$$\text{Noise Power} = \frac{8kT\Delta f}{3g_m} \tag{2.4}$$

where k is the Boltzmann's constant, T is the absolute temperature, and Δf is the noise bandwidth. Taking both bandwidth and signal to noise ratio requirements into consideration, the constrains on g_m and C_L can be determined based on the following equations:

$$g_m > \left(\frac{8kT\Delta f}{3}\right) \cdot \frac{(2^{n+1})^2}{V_{FS}^2} \tag{2.5}$$

and

$$C_L > \left(\frac{16kT}{3\pi}\right) \cdot \frac{(2^{n+1})^2}{V_{FS}^2} \tag{2.6}$$

where V_{FS} is the full scale voltage of the A/D system.

Among the error sources presented in this section, only the static offset voltage of the comparator can be cancelled using autozero techniques or Fowler trimming. Since the dynamic offset voltage and thermal noise can not be canceled, they must be kept below an LSB of the A/D system by proper design, layout and trimming. Dynamic offset voltage can be minimized by using the fully differential circuit and large load capacitor while the thermal noise can be mitigated by large capacitor. However, a large capacitor will result in the large size and large power consumption as well as and increased settling time for the system.

2.2.4 DAC Errors

DAC is a critical component in two-step ADC architecture and its errors will greatly affect the ADC system performances. In the actual DAC circuit, the mismatch in reference resistors, reference capacitors, and reference current, introduces the static offset. Furthermore, the clock feedthrough of the analog switch causes the dynamic offset voltage. The thermal noise in reference resistors and reference current sources also contributes its error to the DAC and must be kept 1 to 1.5 LSB below the signal.

A special dynamic element matching (DEM) technique can be used in DAC to increase signal-to-noise ratio and this technique will be discussed in Chapter 4.

2.3 Comparators Amplification Techniques

This section reviews the comparator amplification techniques and their applications in the coarse and fine comparators. Functionally, the comparator needs to ensure that digital output levels can be generated based on small differences of two input signal levels. Therefore, amplification is the basic function of comparator. Since the comparator amplification need not be linear, it can be implemented by using nonlinear gain stages.

The comparator amplification techniques can be categorized into three generic approaches. A single-pole amplifier (SPA) is the simplest form of comparator. A multistage amplifier (MA), comprised of a cascade of N identical SPA's, provides higher gain than SPA. A regenerative amplifier (RA), implemented using positive feedback, has the best speed performance among these approaches[13]. Figure 2.10 shows the small signal equivalent circuit for each of these amplification techniques.

2.3.1 Single pole amplifier (SPA)

Assumed that a step waveform is applied at the input of comparator. The equivalent amplification factor A for this circuit is defined as the ratio of the output V_O to the input step amplitude V_i (see Figure 2.10(a)) after an amplification time T_a. If the MOSFET output impedance are quite large, the relationships between T_a and A for the SPA is simply

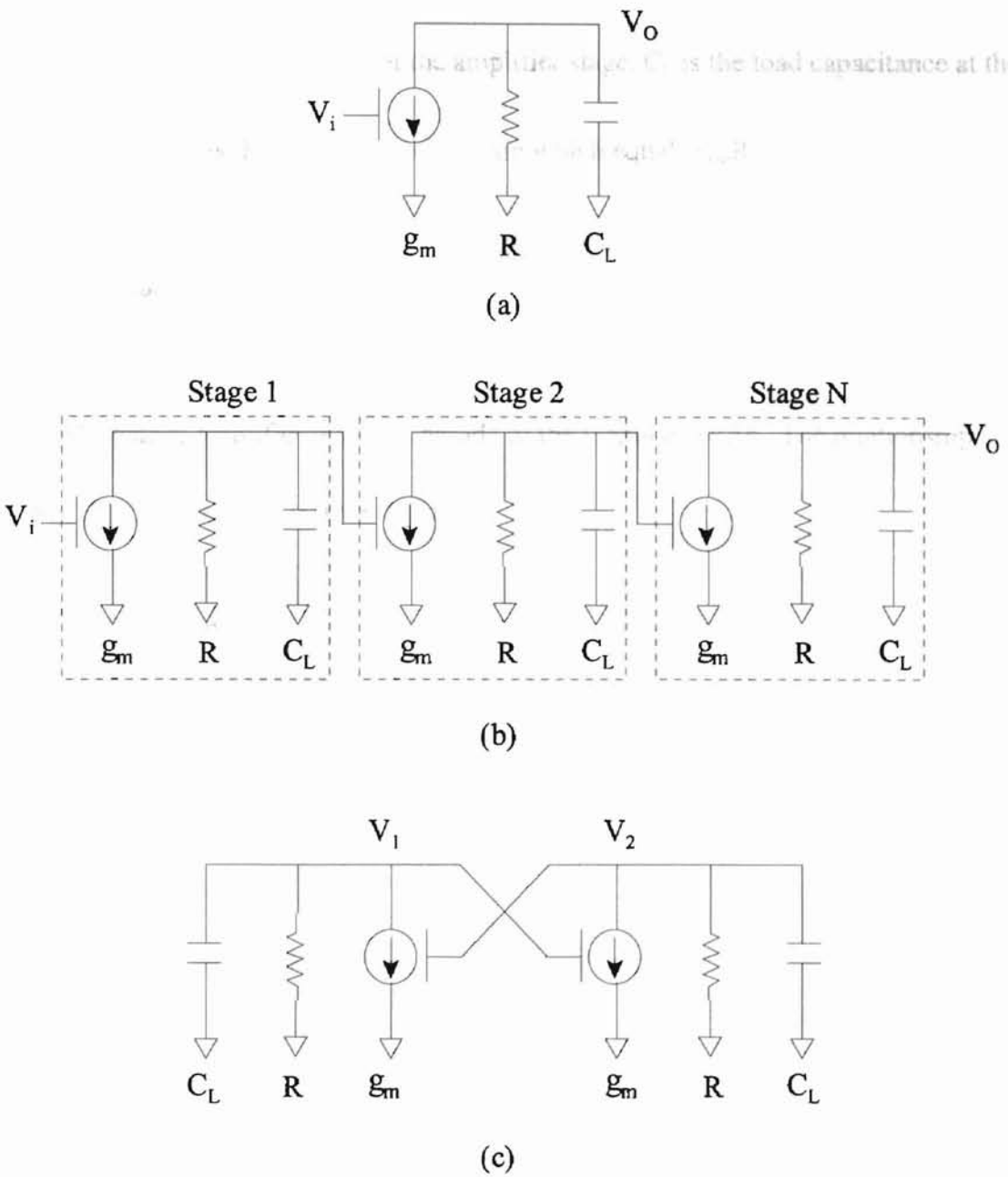


Figure 2.10 General Approaches to Obtain Amplification in Comparators

(a) Single pole amplifier (SPA)

(b) Multistage amplifier (MA)

(c) Regenerative amplifier (RA)

$$T_a = \frac{C_L}{g_m} \cdot A \tag{2.7}$$

where g_m is the transconductance of the amplifier stage, C_L is the load capacitance at the output node, and A is the small signal DC gain which equals $g_m R_O$.

2.3.2 Multistage amplifier (MA)

Multistage amplifier is just a cascade of the identical SPAs. The relationship between T_a and A for MA is given by[13]:

$$T_a = \frac{C_L}{g_m} \cdot (A \cdot N!)^{\frac{1}{N}} \tag{2.8}$$

where N is the number of the amplifier stages. For the MA, there exists an optimum number of stages N_{op}, for which T_a is minimized. The relationship between N_{op} and A is approximated by [13]

$$N_{op} \approx 1.1 \cdot \ln(A) + 0.79 \tag{2.9}$$

for $A < 1000$.

2.3.3 Regenerative amplifier (RA)

As stated previously, a positive feedback amplifier can also be used as a comparator. The equivalent amplification factor A of such a amplifier is defined as the ratio of the differential output, $V_1(t)$-$V_2(t)$, to the initial differences, $V_1(0)$-$V_2(0)$, after a

regeneration time period of T_a. Again assume the MOSFET output impedance is very large, the amplification time T_a is then related to A by

$$T_a = \frac{C_L}{g_m} \cdot \ln(A) \tag{2.10}$$

For the SPA and MA configurations, the amplification gain is limited by the low frequency gain of the individual SPA stages. However for RA, the gain A is limited only by the noise floor and the power supply voltage. From the above equations (2.7),(2.8), and (2.10), it can be seen that the amplification time T_a in a comparator is best obtained by means of regeneration technique. However, for a practical implementation this may be difficult to accomplish as in case of MOS comparators due to the relatively large offsets within the sense amplifier. Therefore, the regenerative amplifier is generally preceded by a preamplifier [14]. The preamplifier also eliminates the "kick back" voltage which introduce error source into reference resistor chain.

The previous discussions in this section described three comparator amplification techniques. In two-step A/D architectures, the SPA and MA are generally used in the first level of the ADC to conserve power, whereas the RA is used in the second stage where it has to resolve small voltages in the range of 0.5mV to 2mV. In general, the RA is used in high-speed ADCs to achieve the fastest speed performance.

2.4 Digital-to-Analog Converter (DAC)

All two step A/D architectures require the intermediate re-conversion of the MSBs to an analog equivalent by a DAC. The typical digital-to-analog converter consists of three major elements: (1) some type of resistor or capacitor network, (2) a means of switching either a reference voltage or current to the proper input terminals of the network as a function of the digital value of each digital input bit, and (3) a reference voltage or current. For high-speed applications in a two-step A/D converter system, the most commonly used DACs can be categorized into three types: resistor network DAC, capacitor network or charge redistributed DAC, and current reference source DAC. Figure 2.11 shows these three kinds of DAC.

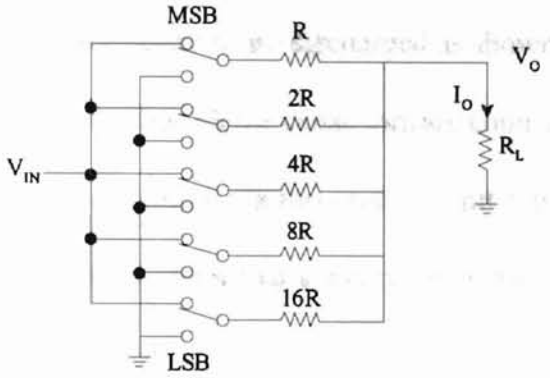
• Resistor Network DAC

Figure 2.11(a) shows a 5-bit DAC using a weighted-resistor network. The size of each resistor is inversely proportional to the weighted value of the particular digital bit that it converts.

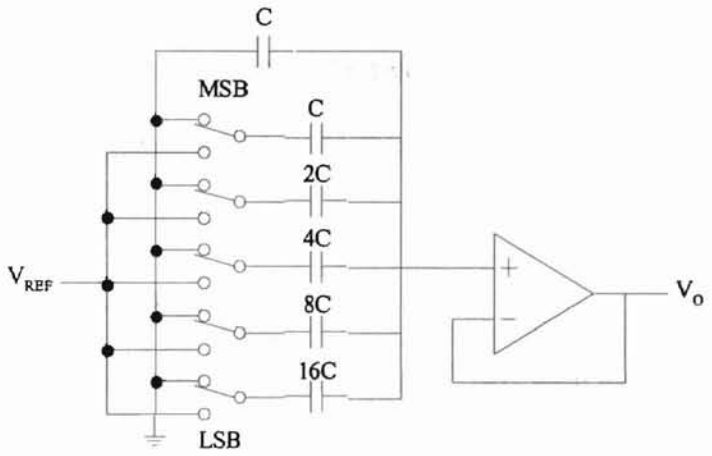
Since delay of the DAC is proportional to the resistance of R, the R must be small enough to decrease the RC time constant. Nevertheless, it is difficult to obtain matching resistors for 10 bit accuracy [31] at low resistance value in a CMOS process. This disadvantage limits its application in high speed A/D systems.

• Capacitor Network DAC

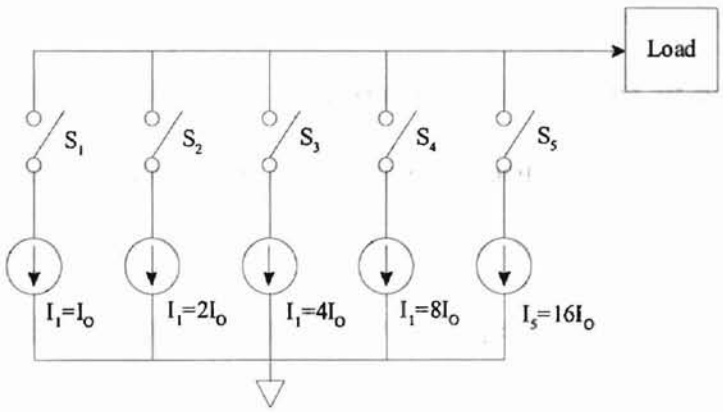
In Figure 2.11(b) an example of a binary weighted capacitor D/A converter system is shown. The system consists of n binary weighted capacitors, an additional



(a) a 5-bit DAC using a weighted-resistor network



(b) a 5-bit DAC using a weighted-capacitor network



(c) a 5-bit DAC using reference current sources network

Figure 2.11 Three Kinds of Most Commonly Used DAC

capacitor with the unit capacitance, an operational amplifier used as a follower, and a set of switches that connect the weighted capacitors to the reference voltage V_{ref}. At the beginning of the conversion all capacitors are discharged as shown in the switch configuration of Figure 2.11(b). Then all the capacitors are connected to the reference voltage to perform a precharge condition. In this case the unit capacitor C is still short-circuited to ground. When the conversion starts, every capacitor, depending on the digital input information, is connected to ground or remains in the reference position. During the conversion, the charge is redistributed over the capacitors and a binary-weighted D/A conversion is obtained for the generated output voltage. The accuracy of this type DAC can be 10-bit [31]. The limitation of this DAC is that it requires the precharge process, which slows down the conversion speed.

• Current Reference Source DAC

Sometimes it is necessary to obtain a current DAC with high accuracy in an A/D converter system. Figure 2.11(c) shows a example of binary-weighted current reference source DAC. The digital input code is applied at the control end of switch. Each reference current source I_i is switched to the output node I_{out} by the bit switches $S_1 \sim S_5$. Since current reference source can be implemented by using high accuracy current mirror (OTA type), its accuracy can be 10-bit [31]. Therefore, this kind of DAC can be employed in the high-speed and high-resolution A/D system, as stated later.

Among the three different kinds of DAC described previously in this section, the resistor network DAC has the simplest form but it suffers from resistor matching

difficulty when applied in high resolution application in a CMOS process. The capacitor network DAC needs an accurate and high-speed OTA to achieve high resolution and speed performances. The current reference source DAC is the best choice in this proposal due to its achievable high accuracy as well as high speed performances although it has larger area than the previous two DACs. This kind of DAC, along with current mirror with OTA technique, will be discussed in Chapter 4.

The dynamic element matching (DEM) DAC is very suitable for high accuracy application [25][26]. By reducing the correlation among successive error sources, DEM DAC can achieve high signal-to-noise ratio performance up to 12 bit [25]. The DEM DAC will be discussed in Chapter 4.

CHAPTER 3

4-BIT FLASH A/D CONVERTER

IMPLEMENTATION AND TESTING RESULTS

The parallel A/D architecture, commonly referred to as flash A/D conversion, provides the fastest possible approach to quantizing an analog signal. All of the possible quantization levels are simultaneously compared to the analog input signal. Figure 2.1 represents the architecture of a generic flash A/D converter.

In order for an analog signal to be quantized, its voltage level must be within the end points of the reference voltage divider. Comparators for which the analog input level is greater than the respective reference levels will output digital logic '1'. Likewise, the comparators that have reference levels that are greater than the analog input will output logic '0' as a result of the comparison process. The appearance of the 2^N-1 bit digital word that results from the simultaneous comparisons gives rise to the thermometer analogy. A continuous string of 1's should appear up to the quantization level that is nearest to the input level. Beyond this point, a continuous string of zeros results. The height of the string of 1's can be read, as the mercury in a thermometer, to yield the quantized measurement of the analog input. In actual implementation, digital logic, referred to as bubble detector or thermometer decoder, is used to evaluate the results of adjacent comparators in order to find the '1'/'0' boundary condition. The bubble detector

will produce only one output that is true, thus providing a unique digital code to the 2^N:N encoder in the last stage. The active signal acts as an address line to the encoder which enables the output of a single N-bit word equivalent to the value of the detected quantization level.

In this chapter, the first section will present the schematics of five functionality blocks, i.e., comparator, bubble detector, encoder, input buffer, and output buffer. The SPICE simulations are also presented. The testing results will be included in section two. The characteristic curves of P transistor and N transistor reveals the performances of IBM 0.1μm process. The DC screen and AC response testing results of five functional blocks on the wafers are displayed later. Finally, the future design considerations are shown in section three based on the practical testing results.

3.1 4-Bit Flash ADC System Building Blocks

The block diagram of practical 4-bit flash A/D converter in this study is shown in Figure 3.1. An input buffer is employed to drive the large input capacitance of 15 comparators while an output pad driver is used for the 4-bit system to drive the output pads.

3.1.1 Comparator

The function of the comparator is a crucial, and often a limiting component in the

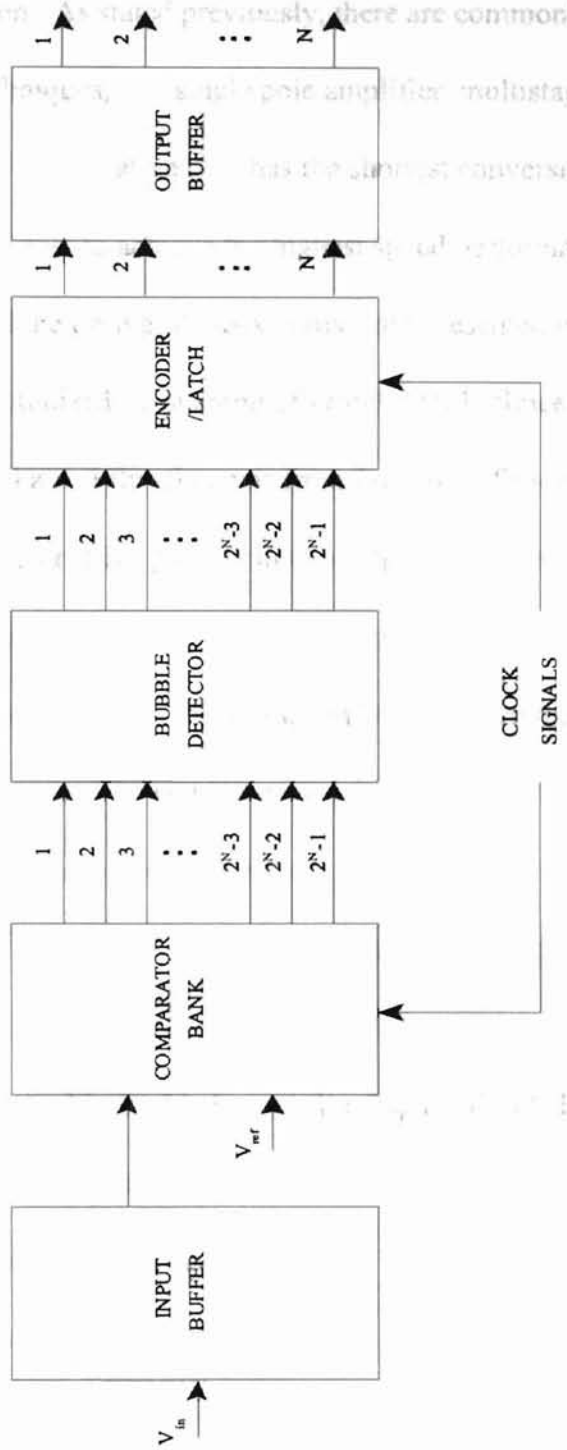


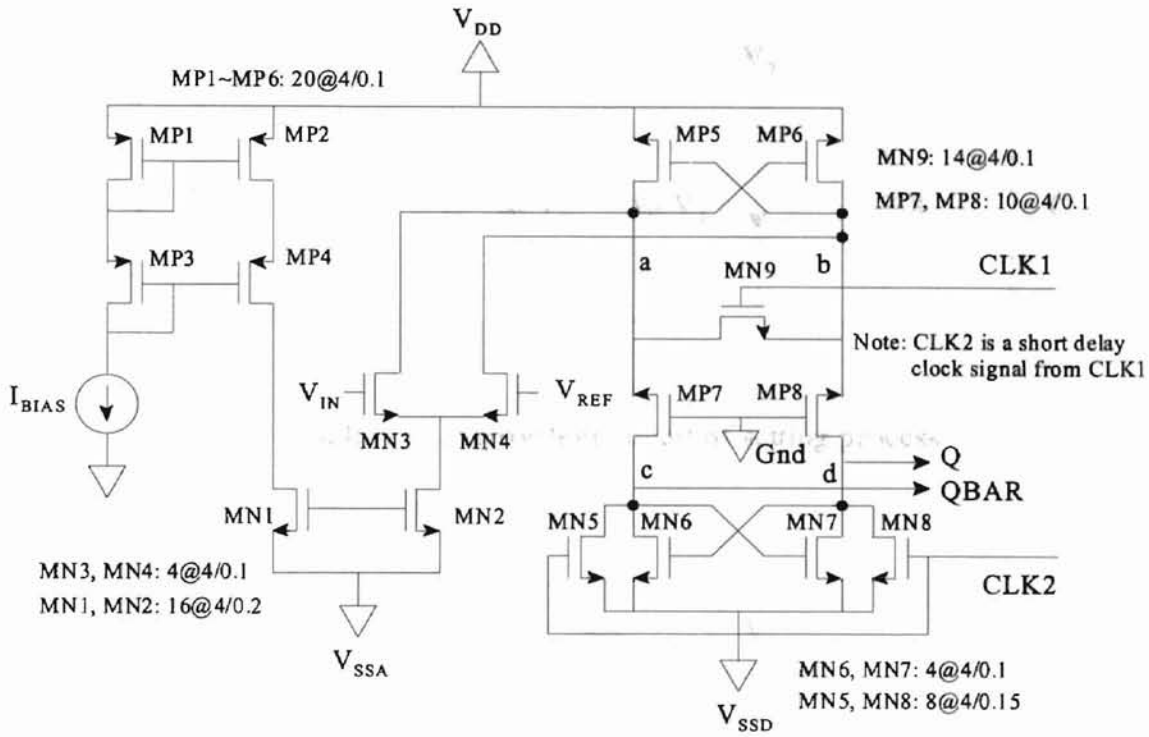
Figure 3.1 4-Bit Flash A/D Converter System Block Diagram

design of high-speed A/D conversion systems due to its finite accuracy, comparison speed, and power consumption. As stated previously, there are commonly three comparator amplification techniques, i.e., single pole amplifier, multistage amplifier, and regenerative amplifier. Since regenerative type has the shortest conversion time, it was employed in this 4-bit A/D system to achieve the highest speed performance. The schematics of comparator and the timing of clock signals are presented in Figure 3.2 [19].

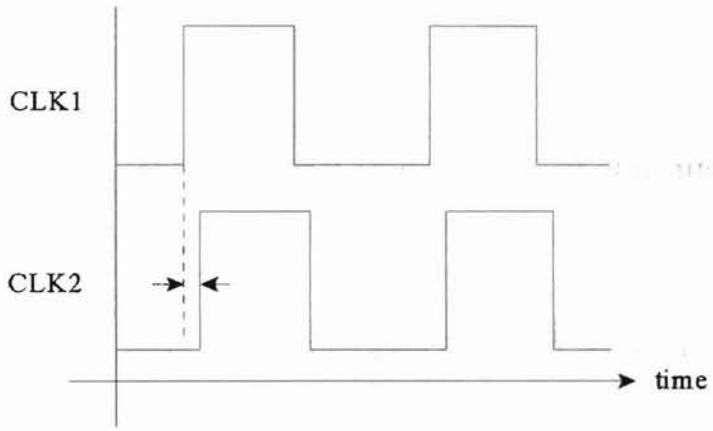
The regeneration is initialized by opening of switch MN9. Since the transistor MP7 and MP8 isolate the N-channel flip-flop pair from P-channel flip-flop pair, the use of two clocks performs the regenerative process in two steps. The first step of regeneration is within the short time slot between CLK1 getting high and CLK2 getting high. The P-channel flip-flop regenerates the voltage differences between nodes a and b. The second regeneration step starts when CLK2 getting high. The voltage differences between node c and d is quickly amplified to a voltage swing equal to the logic levels.

The first regeneration step is very important, not only in raising the regeneration speed but in reducing the total input offset voltage. The differential errors caused by the mismatches in MP7 and MP8, and in the N-channel flip-flop are divided by the amplification gain in the first regeneration step, when referred to the input as an equivalent offset voltage. Therefore, their contribution to the total equivalent input offset voltage can be neglected for sufficiently high gain.

The comparison mechanism has to be closely explored in order to optimize speed and accuracy. For each step regeneration, the small signal equivalent circuits of the setting and resetting processes are shown in Figure 3.3. For the setting process, the following two differential equations are derived as follows:



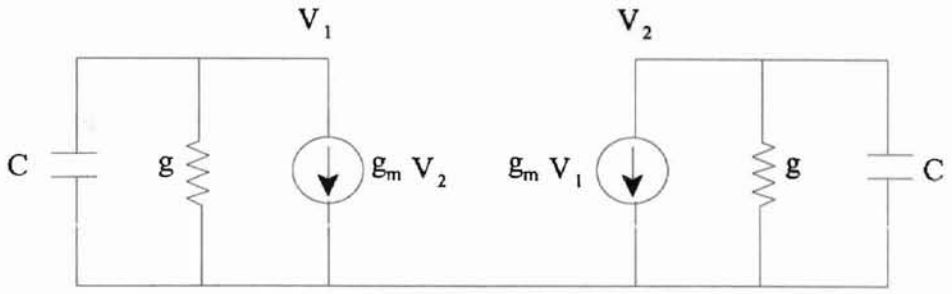
(a) Schematic of regenerative comparator



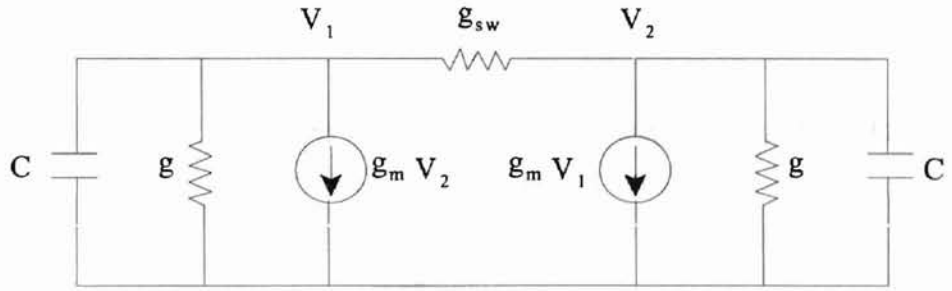
(b) Timing of CLK1 and CLK2

Figure 3.2 (a) Schematics of Regenerative Comparator

(b) Timing of Clock Signals CLK1 and CLK2



(a) Small signal equivalent circuit of setting process



(b) Small signal equivalent circuit of resetting process

Figure 3.3 Small Signal Equivalent Circuit of Setting and Resetting Process for Each Step Regeneration

(a) Setting process (b) Resetting process

$$g_m v_2 + g v_1 + C\frac{dv_1}{dt} = 0 \tag{3.1}$$

$$g_m v_1 + g v_2 + C\frac{dv_2}{dt} = 0 \tag{3.2}$$

Solving (3.1) together with (3.2) gives

$$v_1 - v_2 = v_{IC} \cdot e^{\frac{g_m - g}{C} \cdot t} \tag{3.3}$$

where v_{IC} is initial voltage difference of v_1 and v_2, and should be less than 1/2 LSB. By assuming $g_m >> g$, this equation can be simplified as follows.

$$v_1 - v_2 = v_{IC} \cdot e^{\frac{g_m}{C} \cdot t} \tag{3.4}$$

This equation is applicable for both first step and second step regeneration. Thus, for the first step regeneration, we have

$$v_{O1} = v_{IC1} \cdot e^{\frac{g_{mp5}}{C} \cdot t} \approx v_{IC1} \cdot e^{\frac{t}{\tau_p}} \tag{3.5}$$

where v_{O1} is the first step regeneration output voltage, τ_p is the time constant of first step regeneration (P transistor pair). For the second step regeneration, its initial voltage is the voltage v_{O1} of the first step regeneration. Thus, we have

$$v_{O2} = v_{O1} \cdot e^{\frac{g_{mn6}}{C} \cdot t} \approx v_{IC1} \cdot e^{\frac{t}{\tau_p}} \cdot e^{\frac{t}{\tau_n}} = v_{IC1} \cdot e^{\frac{t}{\tau_p} + \frac{t}{\tau_n}} \tag{3.6}$$

where τ_n is the time constant of second step regeneration (N transistor pair). V_{O2} is the output voltage of second step regeneration and also is the output voltage of this comparator circuit. When $t = t_{set}$, V_{O2} equals to V_{OH}, which is the logic high level voltage. Then, t_{set} can be derived as follows.

$$t_{set} = \frac{1}{\frac{1}{\tau_p} + \frac{1}{\tau_n}} \cdot \ln \frac{V_{OH}}{V_{IC1}} \tag{3.7}$$

Based on the P and N transistor characteristics testing data, we can assume that $\tau_p = 1.5\ \tau_n$. Then, equation (3.7) can be simplified as follows.

$$t_{set} = \frac{3}{5} \cdot \tau_n \cdot \ln \frac{V_{OH}}{V_{IC1}} \tag{3.8}$$

For the resetting process, we can derive the following two differential equations.

$$g_m V_2 + g V_1 + C\frac{dV_1}{dt} + (V_1 - V_2) \cdot g_{sw} = 0 \tag{3.9}$$

$$g_m V_1 + g V_2 + C\frac{dV_2}{dt} + (V_2 - V_1) \cdot g_{sw} = 0 \tag{3.10}$$

Solving these two equations gives

$$V_1 - V_2 = V_{OH} \cdot e^{\frac{g_m - g - 2 \cdot g_{sw}}{C} \cdot t} \tag{3.11}$$

where V_{OH} is the initial voltage difference of V_1 and V_2 for resetting process. When $t = t_{reset}$, $V_1 - V_2$ should be reset to less than V_{IC1}. By assuming $g_m >> g$, t_{reset} can be derived as follows:

$$t_{reset} = \frac{C}{g_m - 2 \cdot g_{sw}} \cdot \ln \frac{V_{IC}}{V_{OH}} = \frac{C}{2 \cdot g_{sw} - g_m} \cdot \ln \frac{V_{OH}}{V_{IC}} \tag{3.12}$$

Then the total delay of this comparator is determined by adding t_{set} and t_{reset},

$$t_d = t_{set} + t_{reset} = \frac{3}{5} \cdot \frac{C}{g_{mn6}} \cdot \ln \frac{V_{OH}}{V_{IC1}} + \frac{C}{2 \cdot g_{sw} - g_{mn6}} \cdot \ln \frac{V_{OH}}{V_{IC1}}$$

$$= \frac{2}{5} \frac{C}{g_{mn6}} \cdot \ln \frac{V_{OH}}{V_{IC1}} \cdot \frac{3 \cdot \frac{g_{sw}}{g_{mn6}} + 1}{2 \cdot \frac{g_{sw}}{g_{mn6}} - 1} \tag{3.13}$$

where C and g_{mn6} are shown below,

$$C = W_{n6} \cdot L \cdot C_{OX} + \frac{W_{sw} \cdot L \cdot C_{OX}}{2} \tag{3.14}$$

$$g_m = \frac{W_{n6} \cdot \Delta V \cdot \mu_{sat} \cdot C_{OX}}{L} \tag{3.15}$$

Define k and k_w as follows,

$$k = \frac{\mu_{sat}}{\mu_{sw}} \tag{3.16}$$

$$k_w = \frac{g_{sw}}{g_{mn6}} = \frac{W_{sw}}{W_{n6}} \cdot \frac{\mu_{sw}}{\mu_{sat}} = \frac{W_{sw}}{W_{n6}} \cdot \frac{1}{k} \tag{3.17}$$

Solving equations (3.13), (3.14), (3.15), (3.16) and (3.17) gives

$$t_d = \frac{2}{5} \cdot \frac{L^2}{\mu_{sat} \cdot \Delta V} \cdot \ln \frac{V_{OH}}{V_{IC}} \cdot (1 + \frac{k_w \cdot k}{2}) \cdot \frac{3 \cdot k_w + 1}{2 \cdot k_w - 1}$$

$$= \frac{2}{5} \cdot \frac{L^2}{\mu_{sat} \cdot \Delta V} \cdot \ln \frac{V_{OH}}{V_{IC}} \cdot \frac{(2 + k_w \cdot k)(3 \cdot k_w + 1)}{2(2 \cdot k_w - 1)} \cdot \tag{3.18}$$

The optimized comparator delay is approached by

$$\frac{dt_d}{dk_w} = 0$$

Thus, the equation for k_w is derived as follows.

$$6 \cdot k_w^{\,2} \cdot k - 6 \cdot k_w \cdot k - k - 10 = 0 \tag{3.19}$$

If

$$k = \frac{\mu_{sat}}{\mu_{sw}} = 0.7 \tag{3.20}$$

From equations (3.19) and (3.20), we have $k_w = 2.17$ and

$$\frac{W_{sw}}{W_{n6}} = k_w \cdot k = 1.52 \tag{3.21}$$

The simulation results of this comparator is shown in Figure 3.4.

3.1.2 Bubble Detector

The digital output of the comparators should represent a thermometer code, as described previously. The boundary between the '1's and '0's must be detected in order to establish the segment of the quantization range in which the input lies. Figure 3.5 illustrates the schematics of the bubble detector. Exclusive-or gate is used here to detect the '1'/'0' boundary condition. The bubble detector geometry is three times large than the encoder to achieve the best speed performance.

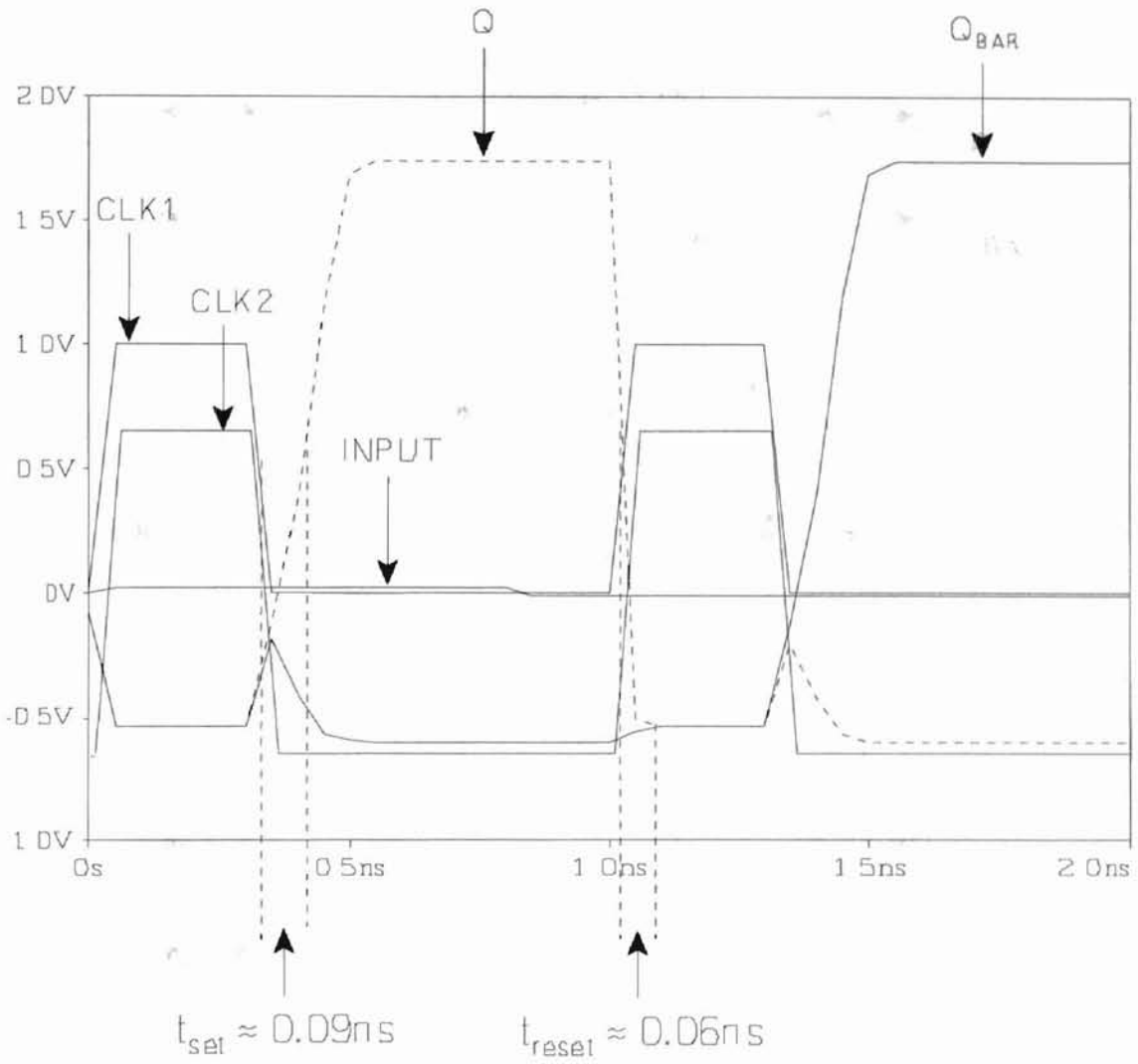
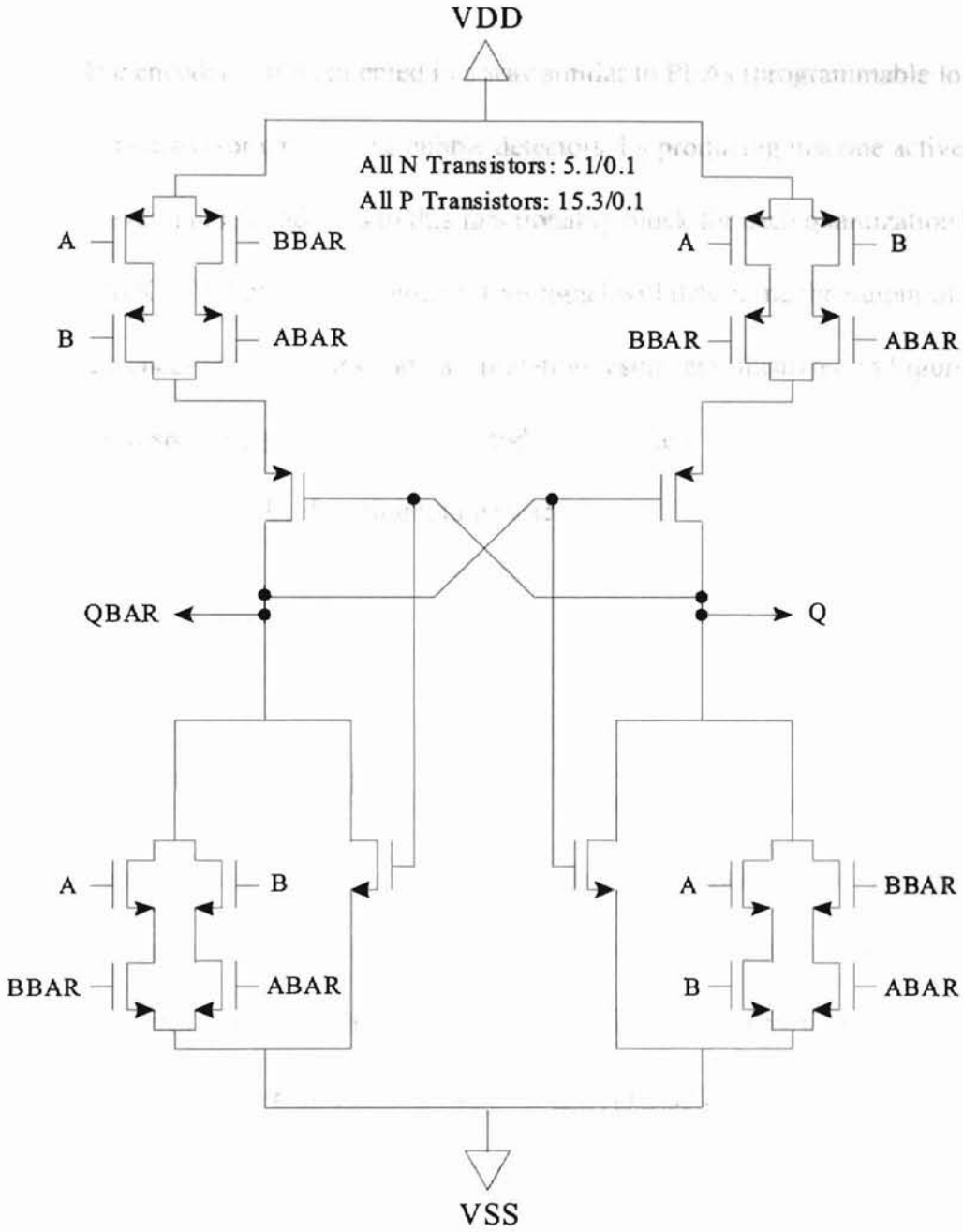


Figure 3.4 Simulation Result of Regenerative Comparator



Q = A XOR B

Figure 3.5 Schematic of Bubble Detector

3.1.3 Encoder

The encoder is implemented in a way similar to PLAs (programmable logic array) [7]. The exclusive-or gates in the bubble detectors, by producing just one active output signal, deliver a unique address to this functionality block for each quantization level of the flash ADC. Therefore, the unique active signal will determine the output of a digital word. The encoder schematics and its simulation results are illustrated in Figure 3.6 and Figure 3.7, respectively. To achieve the highest speed and bandwidth performance, the encoder is designed to be the minimum geometry.

3.1.4 Input Buffer and Output Buffer

At the output of the 4-bit ADC system, the minimum size transistors of encoder is not able to drive the output load, which usually has a large capacitance. The inverter chain, which also function as a buffer, is used in the 4-bit ADC system as a pad driver. At the other extreme, the width of bubble detector is scaled up by four times to keep the effect load of encoder small and maintain a maximum bandwidth. For the same reason, the comparator is scaled up by four time again with the added benefit of reducing the noise floor. Thus, in this 4-bit flash ADC system, input of the 15 comparators produce a very large capacitance, which could reduce the input bandwidth. To avoid bandwidth reduction, an input buffer must be employed to drive this large load. In this design solution, a source follower is used in the 4-bit ADC system. Figure 3.8 and Figure 3.9 display the schematics of input buffer and output buffer.

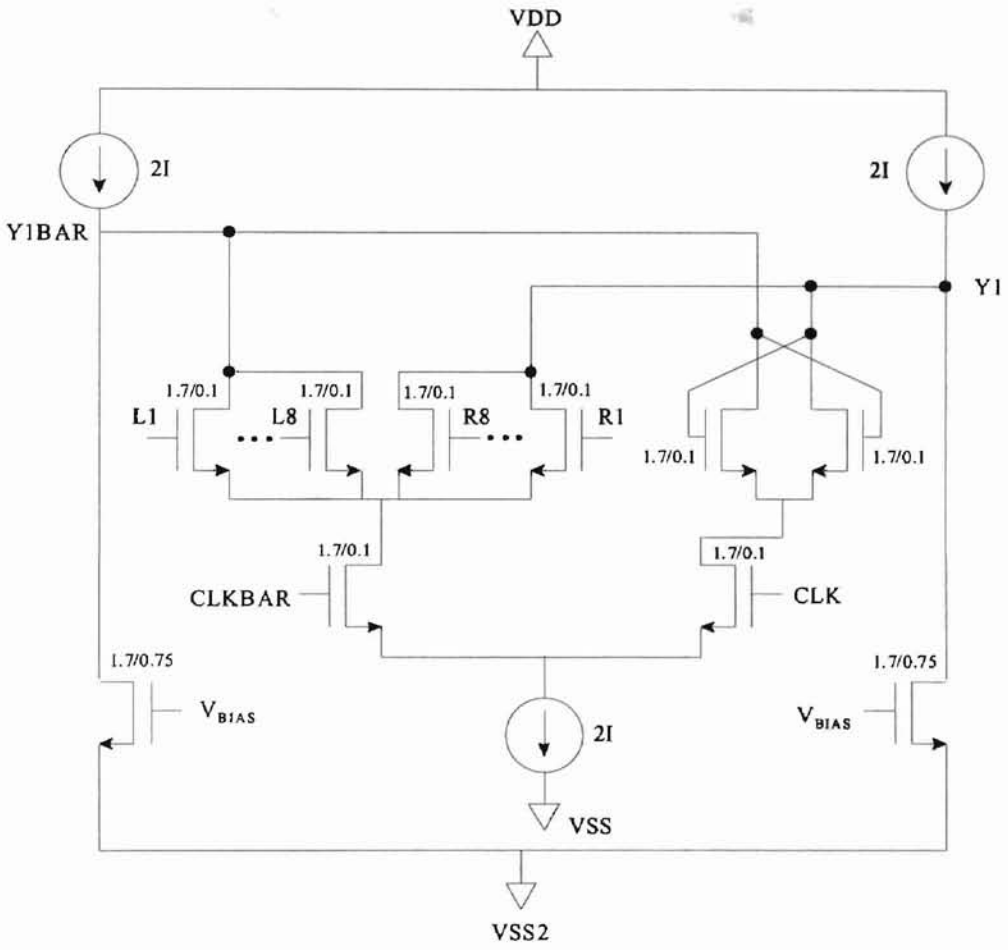


Figure 3.6 Schematic of Encoder

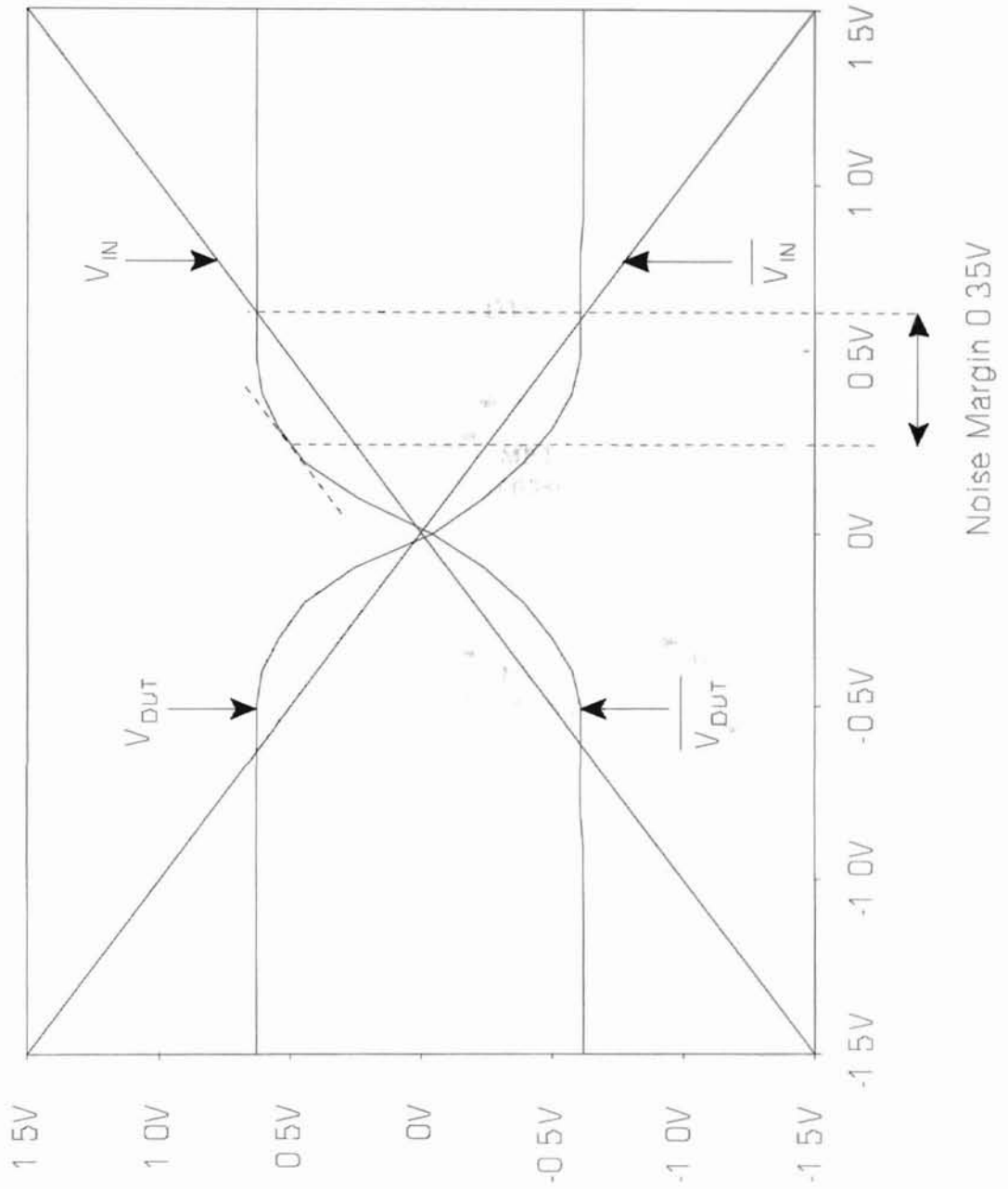


Figure 3.7 Simulation Result of Encoder

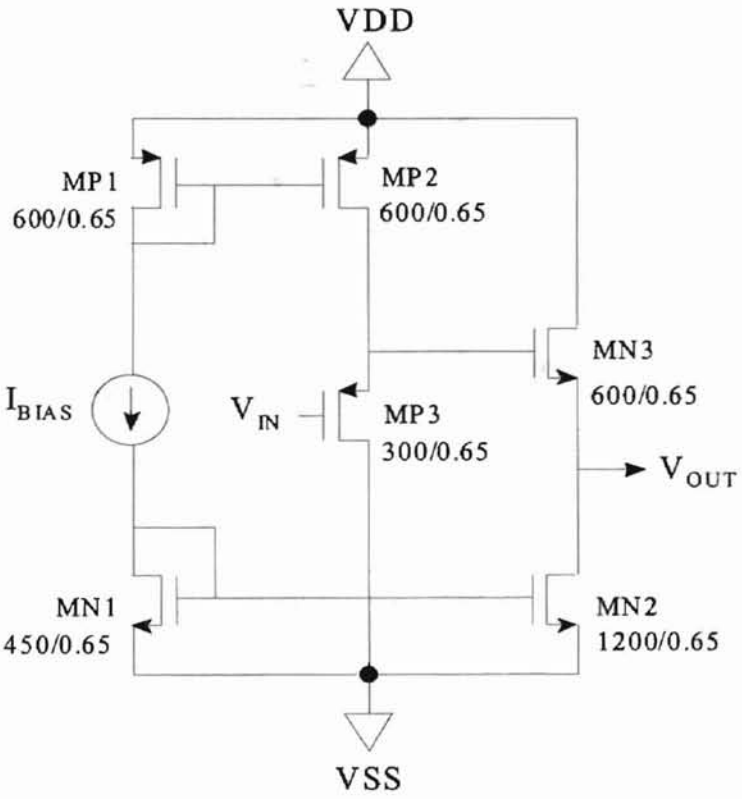


Figure 3.8 Schematic of Input Buffer

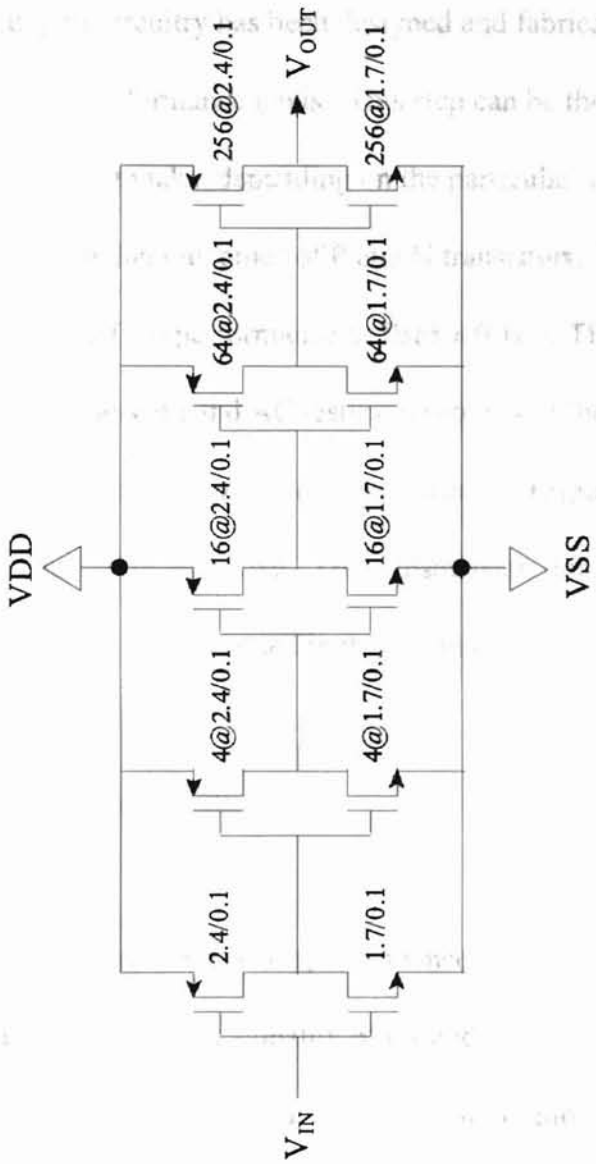


Figure 3.9 Schematic of Output Buffer

3.2 Testing Results

After a flash A/D system has been selected based on a thorough examination of specifications and the support circuitry has been designed and fabricated, the next step is to perform tests to verify the performance goals. This step can be the most difficult of all, and there are many approaches to take, depending on the particular testing objectives. This section first shows the testing outcomes of P and N transistors. The characteristics of P and N transistor will reveal the performance of IBM's 0.1μm TFSOI process. In the second part, DC screenings, transient and AC testing responses of the input buffer, output buffer, comparator, bubble detector, and encoder are illustrated respectively. The gate delay, rise/fall time and bandwidth are tested. The transmission line effect and load capacitance effect on testing are also included in this section.

3.2.1 P and N Transistors Testing Results

The transistor characteristics show the performances of process and allow one to determine the performances of each functionality block and 4-bit ADC system. Typical P and N transistor characteristics are shown in Figure 3.10 and Figure 3.11, respectively.

The testing results reveal that P transistor suffered from avalanche when V_{DS} goes beyond 1.1V. Thus, it limited the maximum power voltage which can safely be applied in the circuit. It also can be seen from the testing data that N transistor has a recognizable large leakage current when V_{GS} equals to 0. This means that the N transistor has a very

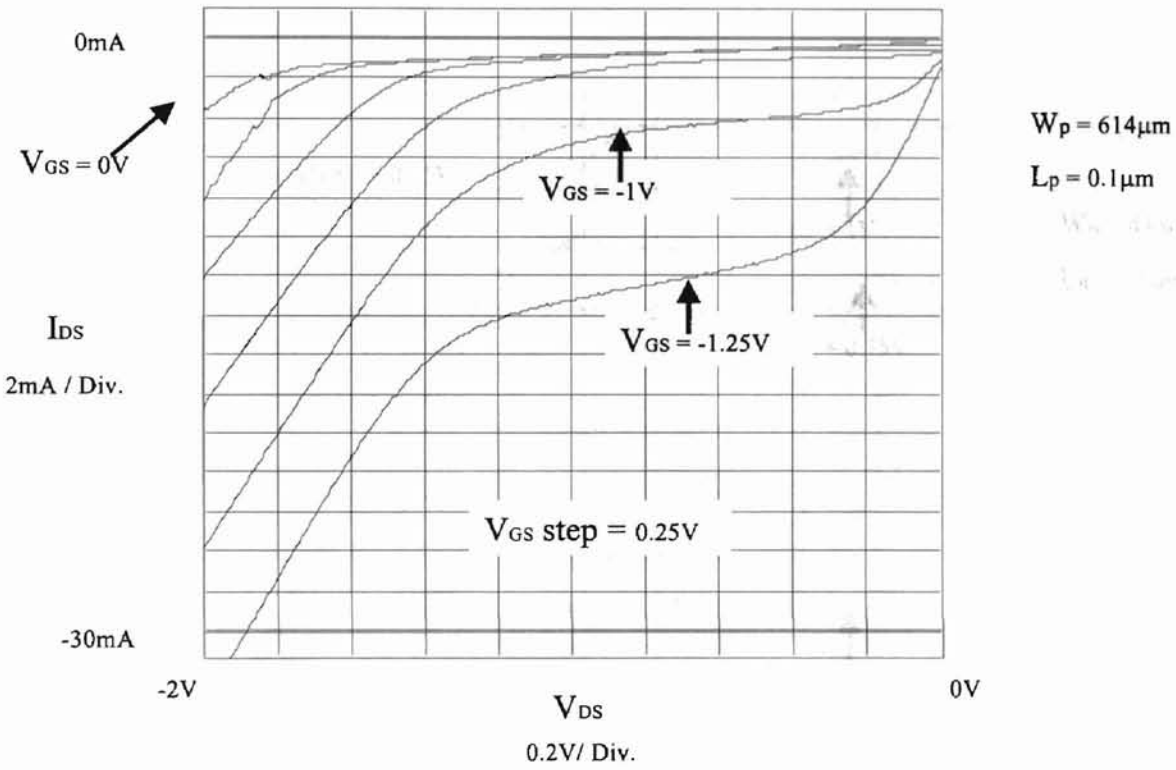


Figure 3.10 P Transistor Characteristics

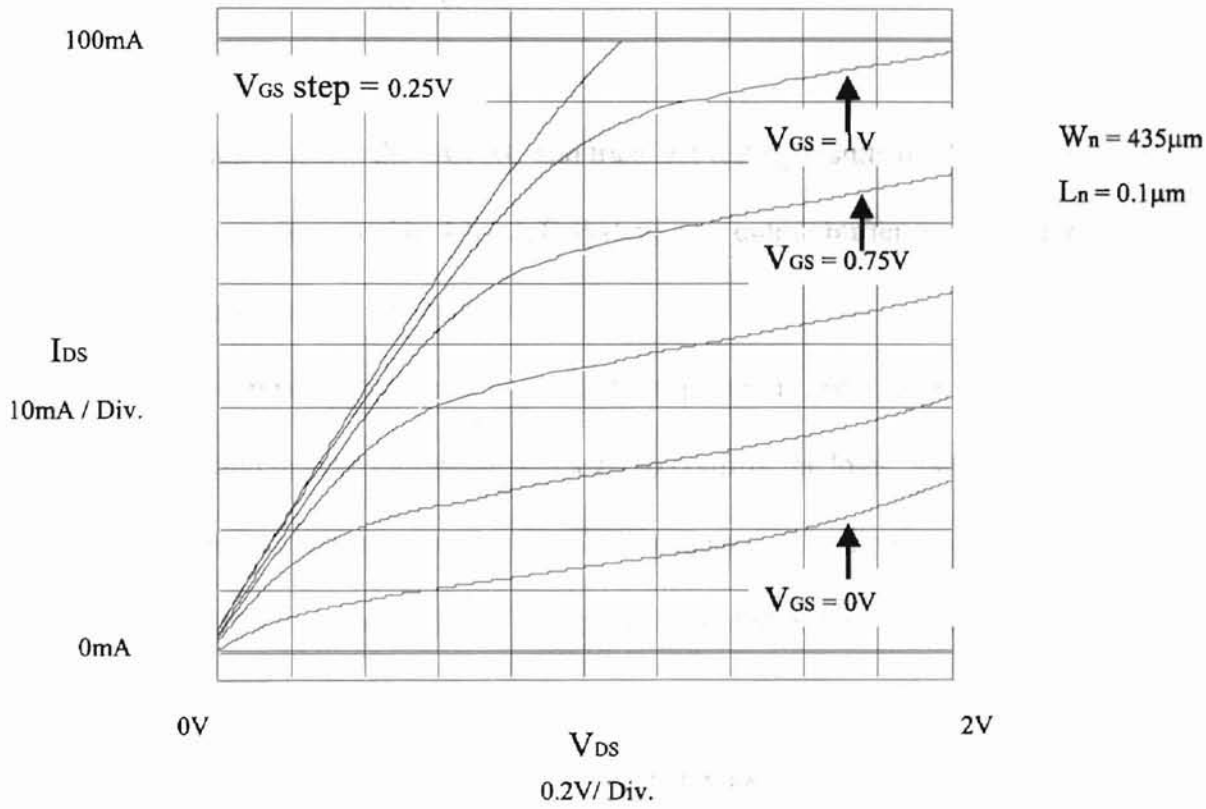


Figure 3.11 N Transistor Characteristics

low threshold voltage. Both P and N transistor fabrication defectives have restricted the anticipated system performances, primarily in the speed and bandwidth. Also, we determined that the self gain of the P and N transistors are approximately 6 and 8, respectively.

3.2.2 Functional Blocks Testing Results

This section displays the DC, AC and transient testing results of all the five functional blocks implemented in 4-bit A/D system, i.e., output buffer, input buffer, bubble detector, comparator and encoder.

For the DC function verification, the test setup uses an HP 4155A to sweep one of the input signals and test the output voltage level to confirm the logic, gain, offset, etc. For the pulse transient response testing, the high frequency pulse signal is applied to the input via a Model 10 high speed probe. The output is tested using a Model 34A or Model 10 probe. For AC response testing, the test setup is similar to that of the transient except for that the input signal applied is sinusoid rather than pulse. The following observations were made.

- **Output buffer**

First of all, the DC sweep testing results of the output buffer is illustrated in Figure 3.12. The DC transfer function of this output buffer showed that it can produce a logic function while it has two problems, a bad transfer curve in transition region and limited output voltage at a logic high. The first problem is due to the avalanche voltage

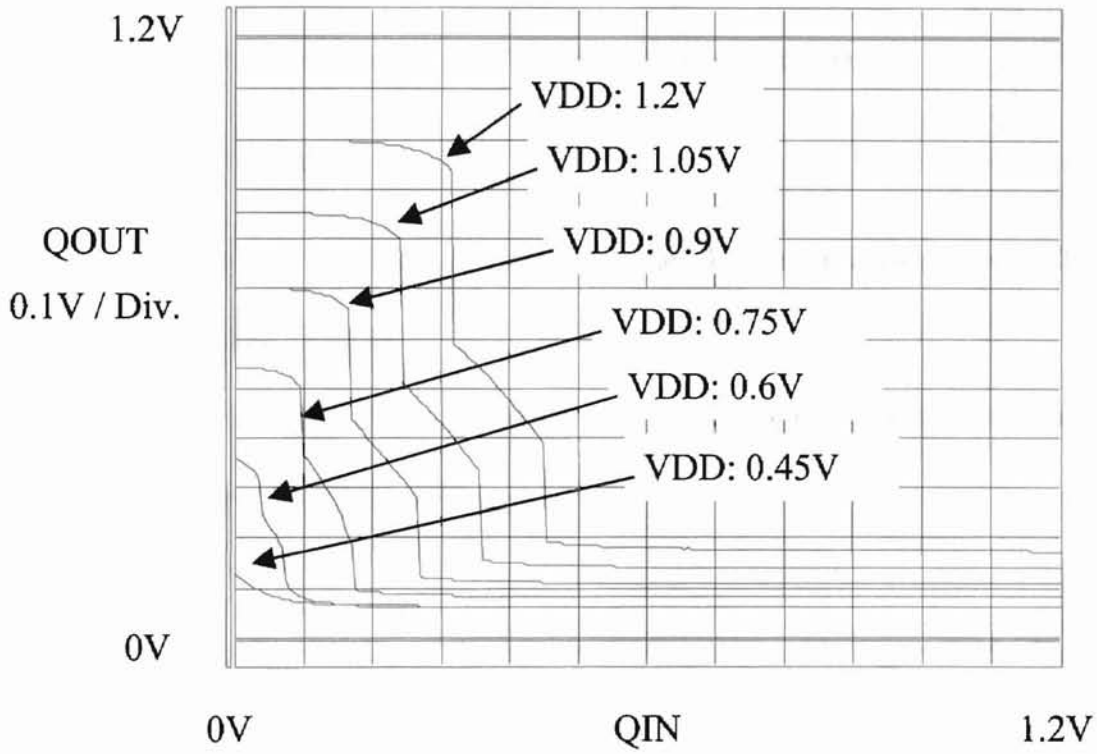


Figure 3.12 Output Buffer DC Sweep Response

of the P transistor and the second one comes from the leakage current of N transistor.

The pulse transient response of output buffer is shown in Figure 3.13. The testing data show that the delay for the first four stages of output buffer is 300ps and 260ps, for the rise and fall edge respectively. Therefore, the average delay per stage is given as

$$t_d = \frac{300ps + 244ps}{2 \cdot 4} = 68ps \tag{3.22}$$

Since the inverter chain is scale up by four, the effective gate delay is

$$t_d = \frac{68ps}{4} = 17ps$$

This is commonly referred to as gate delay per stage. This result is closed to the IBM testing data, which is 22ps [18].

The relationships between gate delay and power supply for output buffer are tested and illustrated in Figure 3.14.

• Input buffer

A typical DC screening of the input buffer is presented in Figure 3.15. The DC gain is limited to be 0.4 to 0.75. This performance can be verified by the analysis in the following. The DC gain of a source follower is given by:

$$A = \frac{g_m}{g_m + g} = \frac{1}{1 + \frac{g_p + g_n}{g_m}} \approx \frac{1}{1 + \frac{2 \cdot g_{ds}}{g_m}} = \frac{1}{1 + \frac{2}{\mu}} \tag{3.23}$$

where μ is the self gain of transistor. The total DC gain of the input buffer shown in Figure 3.8, which composed of two source followers, is given by

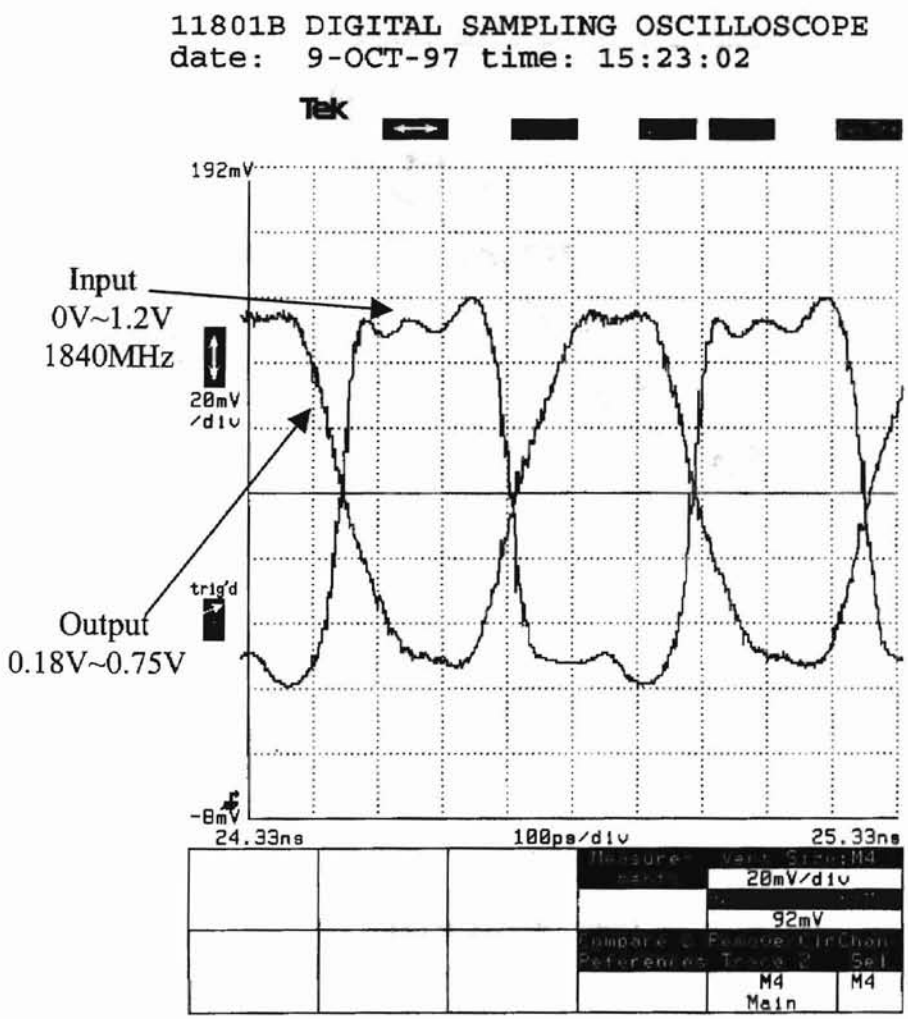


Figure 3.13 Pulse Transient Response of Output Buffer

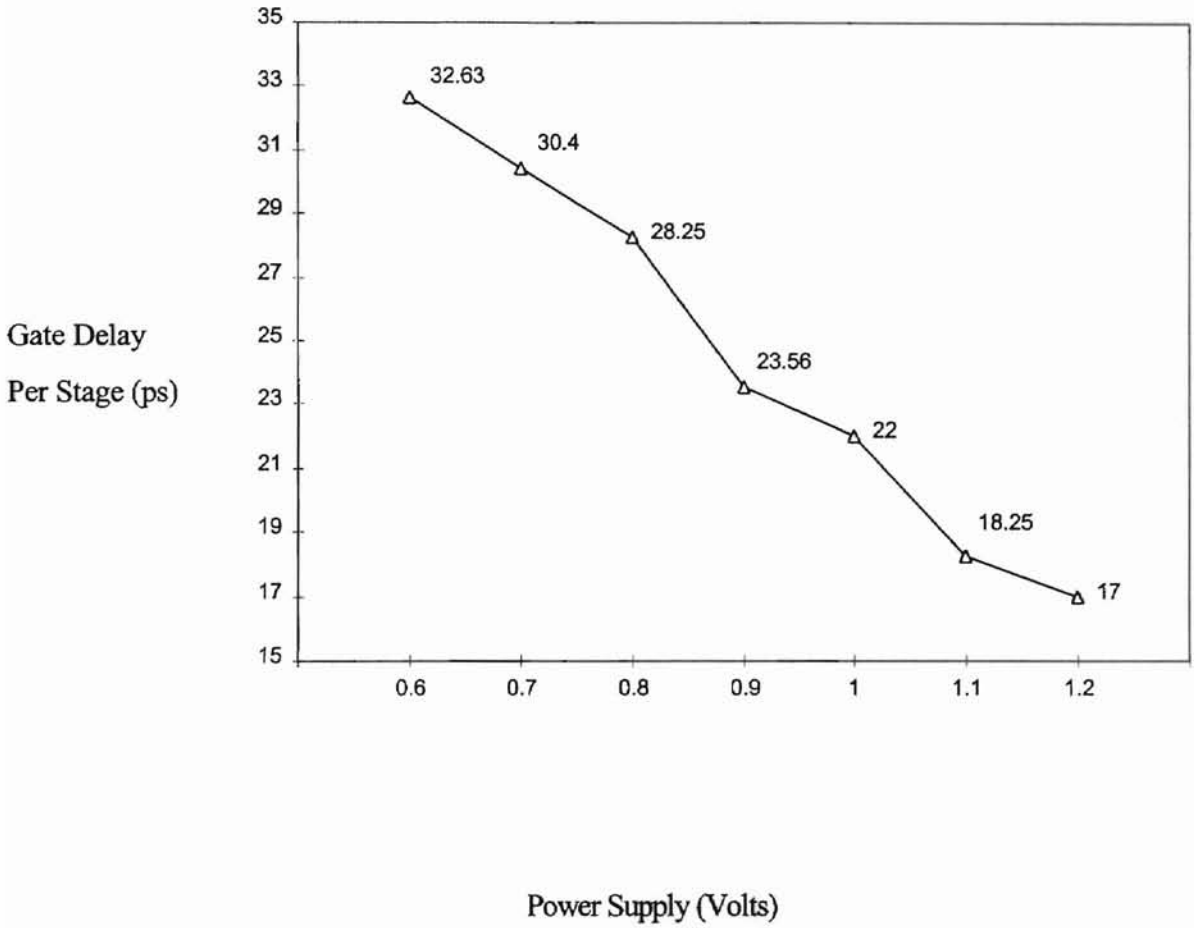


Figure 3.14 Gate Delay Per Stage Versus Power Supply

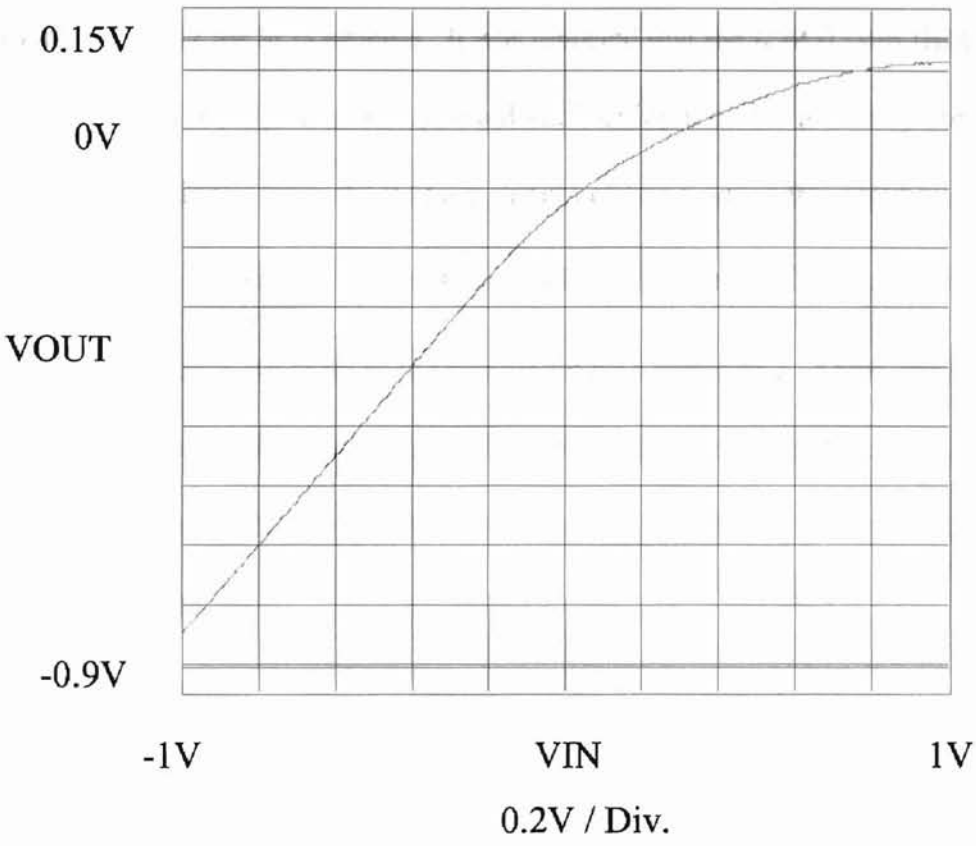


Figure 3.15 Input Buffer DC Sweep Response

$$A_T = A^2 = \frac{1}{(1+\frac{2}{\mu})^2} \tag{3.24}$$

When self gain μ is $6 \sim 8$, A_T is $0.56 \sim 0.64$. This analysis using the P and N transistor data agrees with the tested results of Figure 3.15. The pulse transient response of input buffer is presented in Figure 3.16.

The AC response testing of input buffer showed that the bandwidth of input buffer is around 0.75GHz for SOS process. It was reported that the f_T of 0.1μm IBM process P transistor is 67GHz [18]. The limited bandwidth of input buffer is mainly due to the following restrictions. First, the 0.65μm length of transistor in this input buffer, which is not the minimum length, reduces the bandwidth by a factor of 6.5. Second, the low g_m of P transistor (Figure 3.10) reduces the bandwidth by a factor of 2. Third, the load effect reduces the bandwidth by a factor of 2. The MOSFET source resistance could also contribute to the degradation of bandwidth. The input buffer is redesigned to achieve 5.6GHz bandwidth.

- **Bubble detector**

The basic function of bubble detector is the exclusive-or. To verify the DC function, we can connected one of A or B to ground and sweep the other one. The DC sweep test of the bubble detector is displayed in Figure 3.17. The DC function of bubble detector is confirmed by the testing. The problems that existed here are similar to that of output buffer since both of them are CMOS logic blocks. The P transistor's avalanche voltage causes a logic transition problem and the N transistor's leakage current results in a limited output voltage swing.

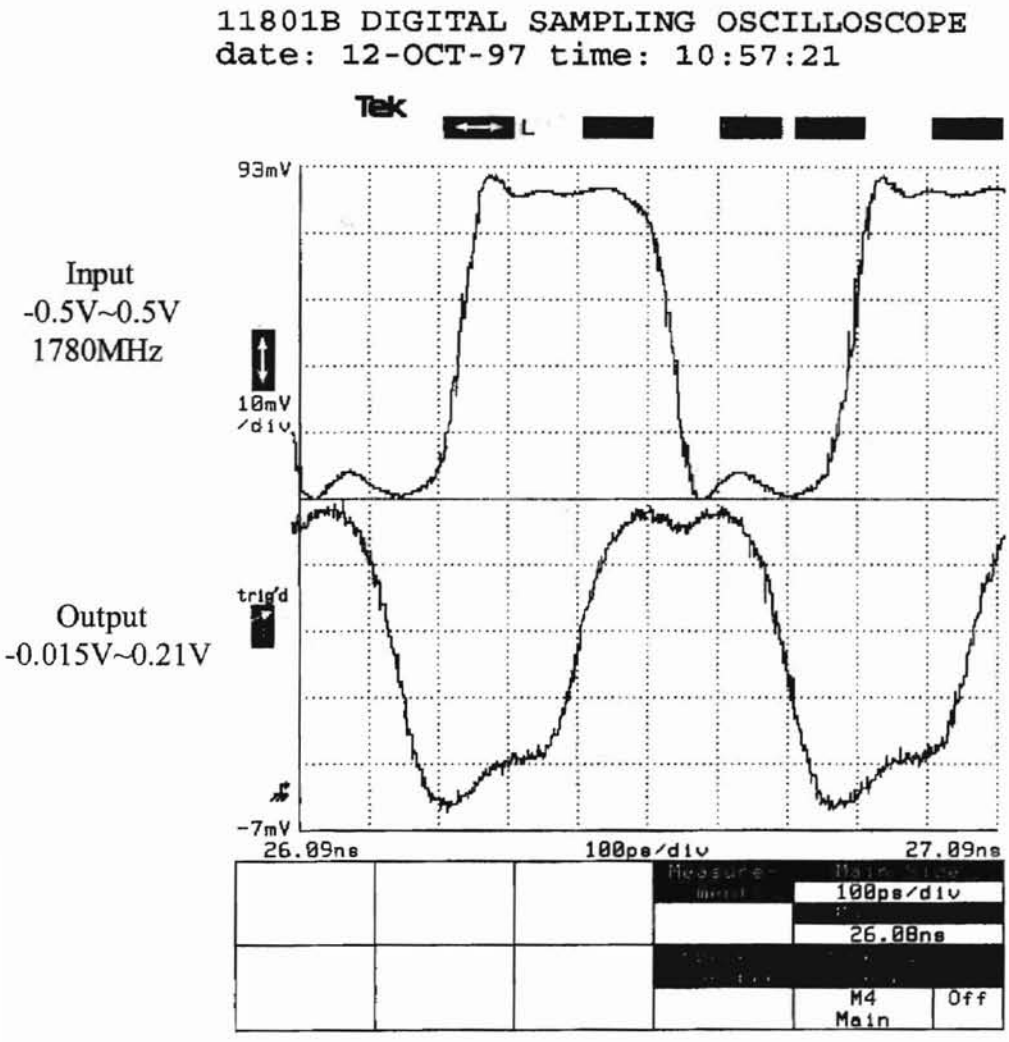


Figure 3.16 Pulse Transient Response of Input Buffer

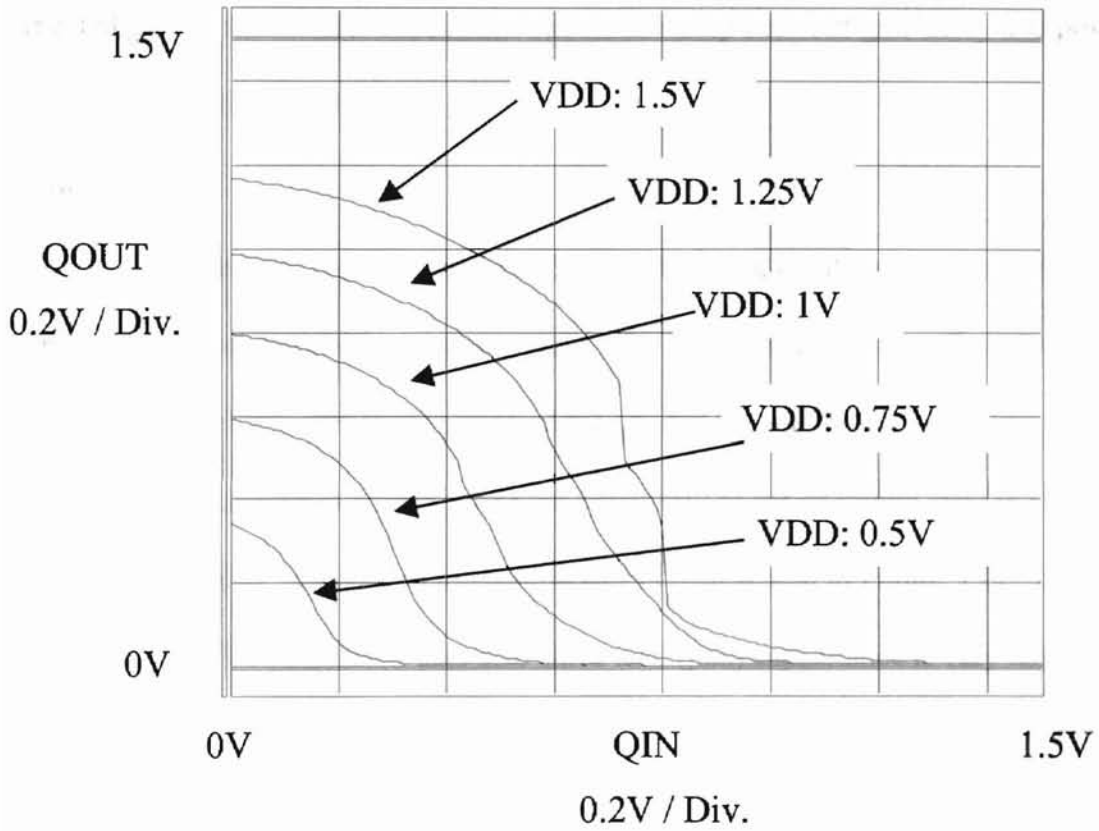


Figure 3.17 Bubble Detector DC Sweep Response

The pulse transient response of the bubble detector is shown in Figure 3.18. The rise time and fall time of the output are 1340ps and 1350ps, respectively. De-embedding (which will be discussed later in pad capacitance section) must be considered here due to the great difference between the gate capacitance of bubble detector and the load or pad capacitance. The effective gate delay is estimated to be 37ps based on a de-embedding factor 36:1, which includes a factor of three due to the series switched resistance. The expected gate delay is about 22ps [18]. The relationship between gate delay and power supply is shown in Figure 3.19.

• Comparator

The function of comparator is verified by sweeping input and applying the clock signals to the clock terminals simultaneously. The DC sweep response of comparator is shown in Figure 3.20. The testing verified the DC functionality of comparator. The offset voltage measured is 30 mV while the sensitivity of the changing state is 10 mV.

The transient response of the comparator is represented in Figure 3.21. De-embedding must be considered here also since load (pad) capacitance is very large while the transistors in comparator is very small. The de-embedding factor is 15:1. Therefore, the equivalent rise and fall time are 32ps and 30ps, respectively. The simulation demonstrated a rise and fall time of 60ps.

• Encoder

Each encoder has 16 inputs signals with half of them (8 inputs) on each side. In the single encoder testing layout, seven of eight inputs on each side had been tied to the negative power supply. Therefore, the basic function of this encoder testing circuit is

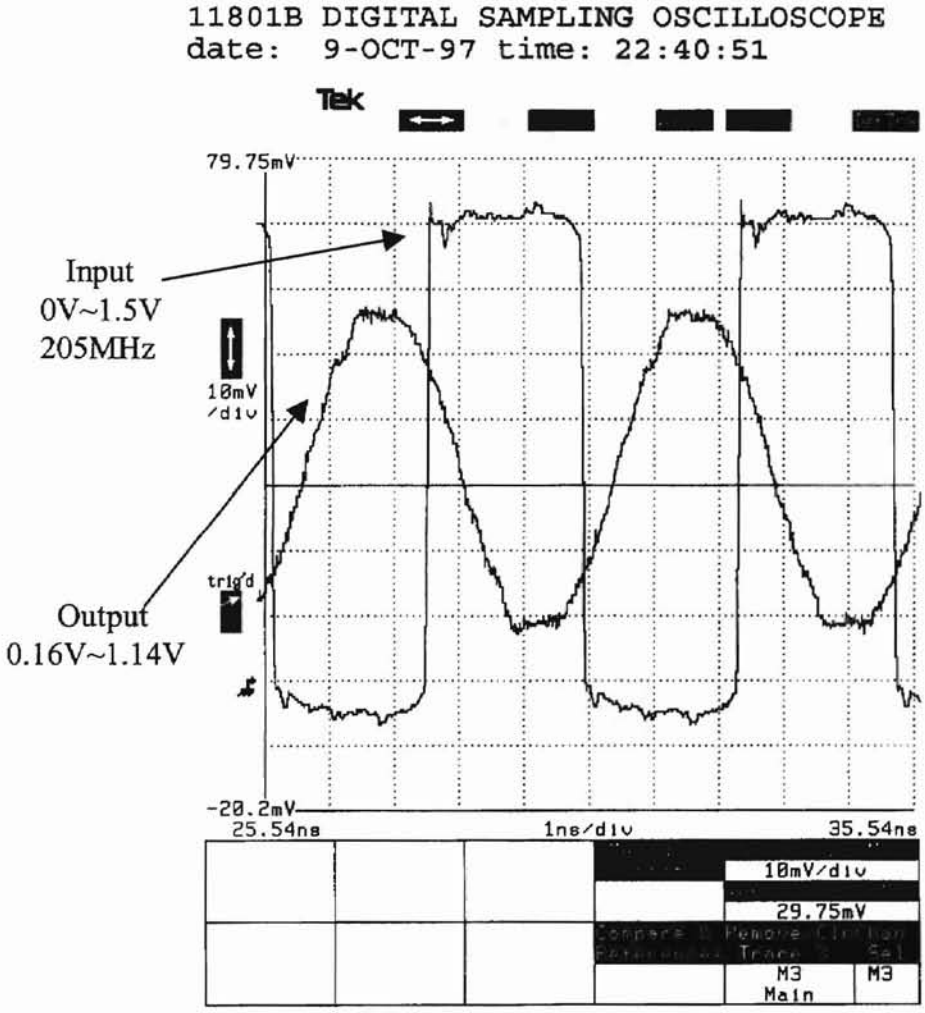


Figure 3.18 AC Response of Bubble Detector

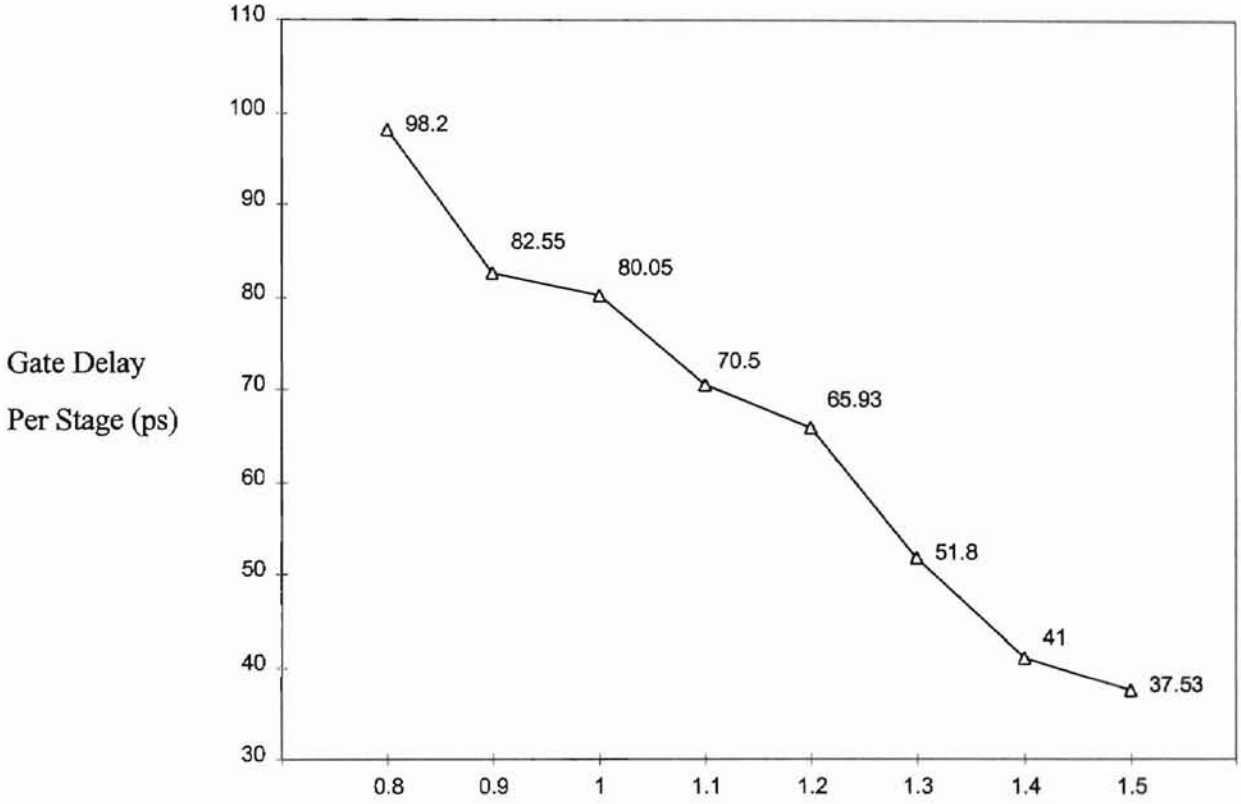


Figure 3.19 Gate Delay Versus Power Supply

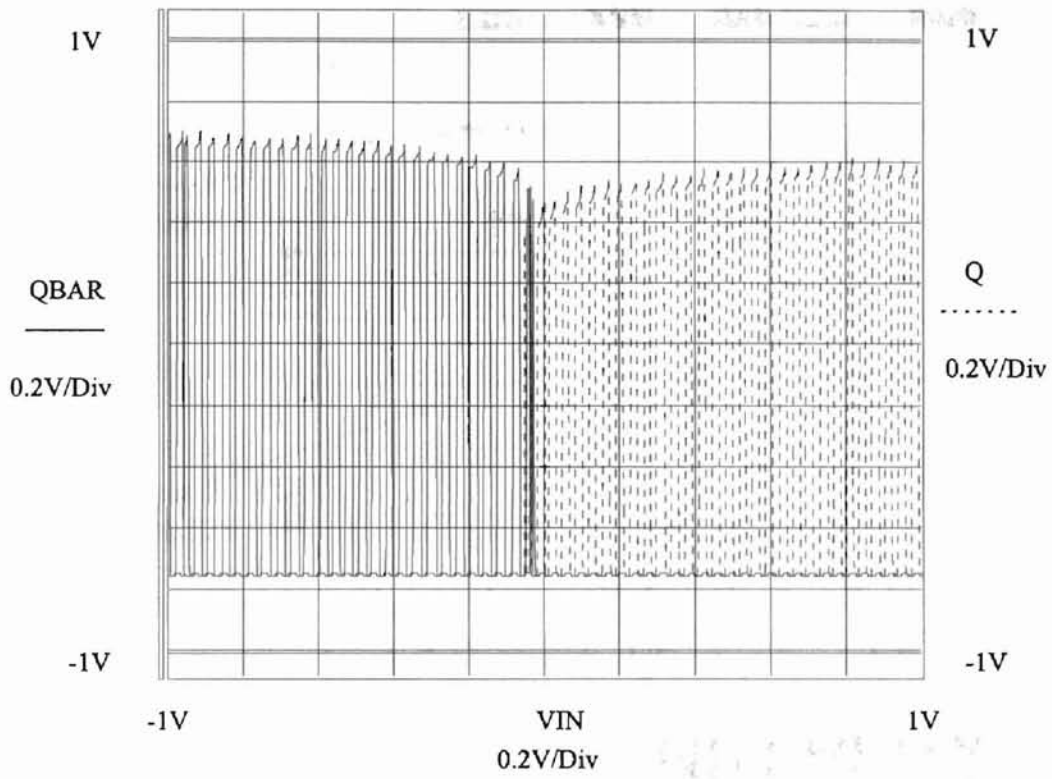


Figure 3.20 Comparator DC Sweep Response

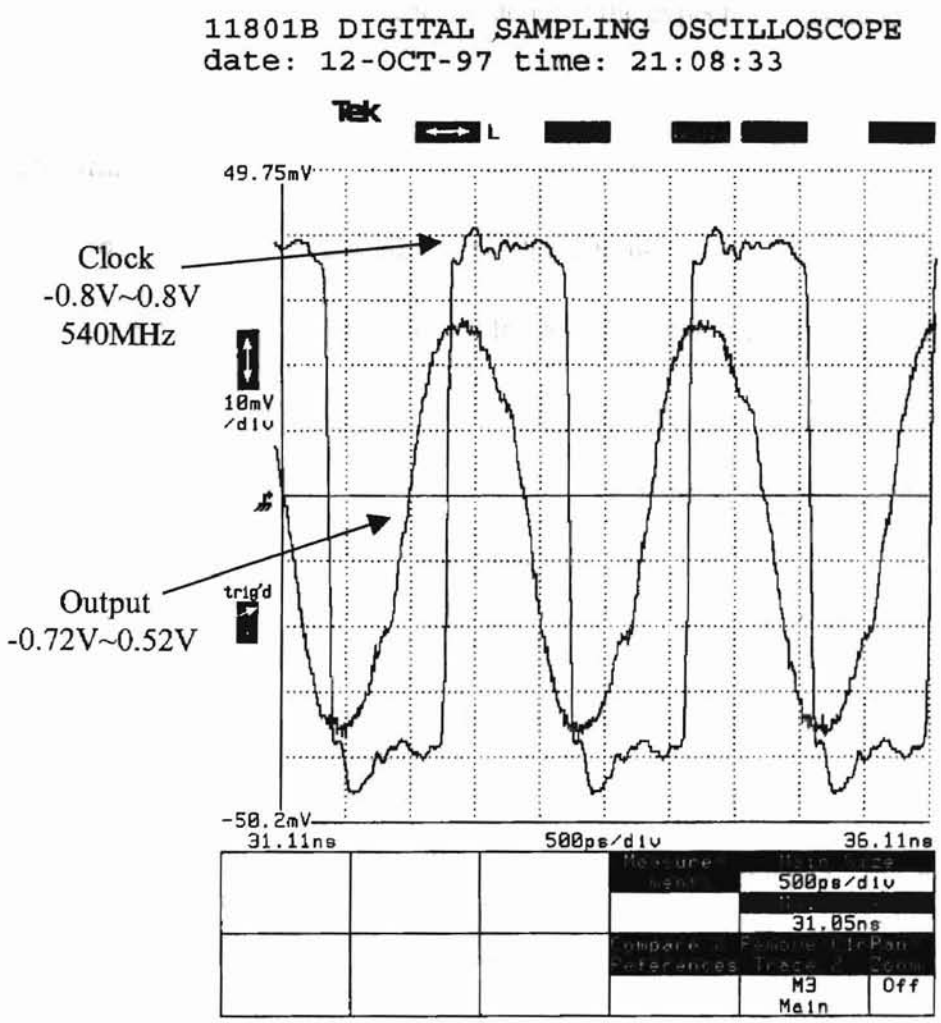


Figure 3.21 Clock Pulse Transient Response of Comparator

simply an inverter. The DC sweep testing of encoder is illustrated in Figure 3.22. The limited output logic high voltage is due to the N transistor leakage current.

The pulse transient response of encoder is displayed in Figure 3.23. The large pad capacitance limited its rise and fall time performance. The pad de-embedding factor is 87. The encoder was redesigned to achieve the expected 60ps delay performance.

- **Pad capacitance**

The pad capacitance measured was too large to be ignored. The 200μm by 200μm pad capacitance was measured at 0.07pF for the SOS process, 1.56pF for the SOI and 3.29pF for the BULK.

The driving or loading problem, which referred to as the de-embedding problem, arises when the small geometry circuit has a large load capacitance. Due to the large pad capacitance, the problem, exists in the small geometry test circuits, including the comparator, bubble detector and encoder. The large pad capacitance results in a slow rising time and a limited bandwidth. The de-embedding problem can be eased by inserting a buffer chain between the output of these circuits and the pad. The buffer would ensure the loading factor for each stage to be no more than approximately four.

- **Inductance**

The probe tip inductance plays an important role in the testing system when measurement frequency exceed a 1GHz or a rise time of 1-2ns. The pad capacitance and probe tip inductance together restrict the rise/fall time of the testing system and thus restrict the maximum bandwidth can be measured. From the testing of single 200μm by

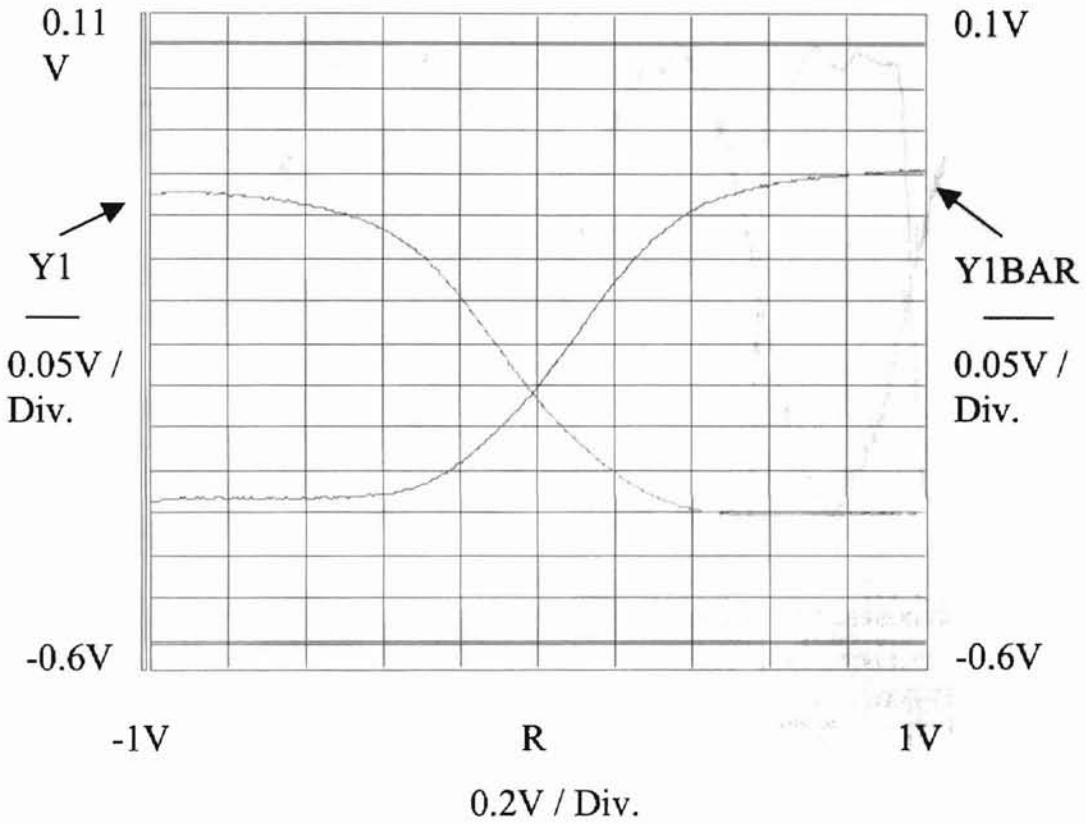


Figure 3.22 Encoder DC Sweep Response

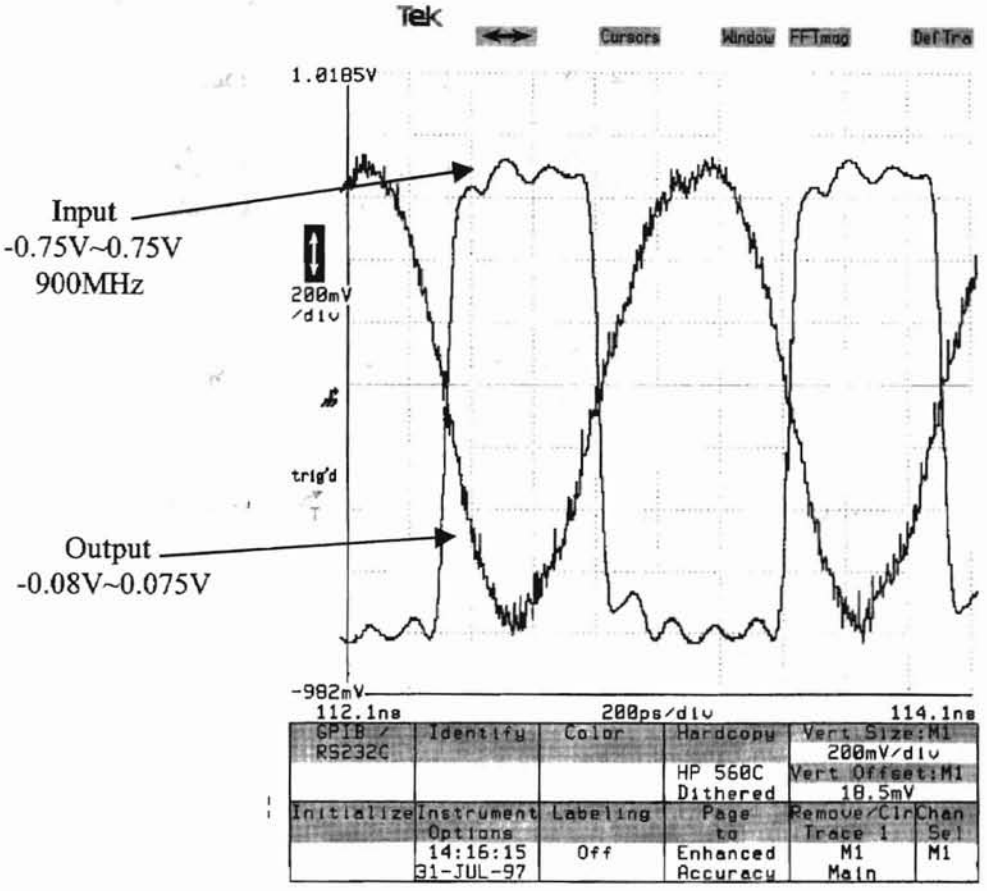


Figure 3.23 Pulse Transient Response of Encoder

200μm pad, it was determined that measure system rise/fall time is 160ps. Figure 3.24 (a) and (b) represent the model for SOS and SOI pad testing setup, respectively. The inductance of the tip can be derived from Figure 3.24 (a) as follows.

The impedance from point a to the load is

$$Z_L = sL + Z_0 \tag{3.25}$$

The reflection factor R and transfer factor T are

$$R = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{sL + Z_0 - Z_0}{sL + Z_0 + Z_0} = \frac{sL}{sL + 2Z_0} \tag{3.26}$$

$$T = 1 + R = 1 + \frac{sL}{sL + 2Z_0} = \frac{2sL + 2Z_0}{sL + 2Z_0} \tag{3.27}$$

When input is step unit signal, i.e., $V_{IN}(s) = \frac{1}{s}$, the output $V_{OUT}(s)$ is

$$V_{OUT}(s) = T \cdot V_{IN}(s) = \frac{2sL + 2Z_0}{sL + 2Z_0} \cdot \frac{1}{s} = \frac{1}{s} + \frac{1}{sL + 2Z_0} \tag{3.28}$$

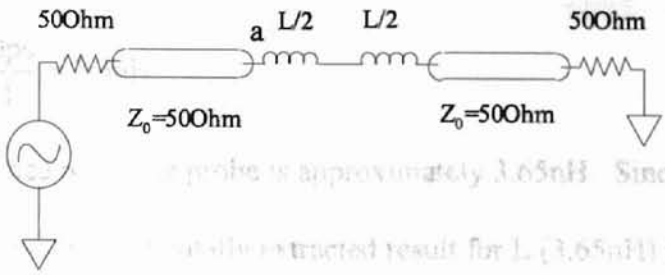
Time domain response of output signal is

$$v_{OUT} = (1 + e^{-\frac{2Z_0}{L}t})u(t)$$

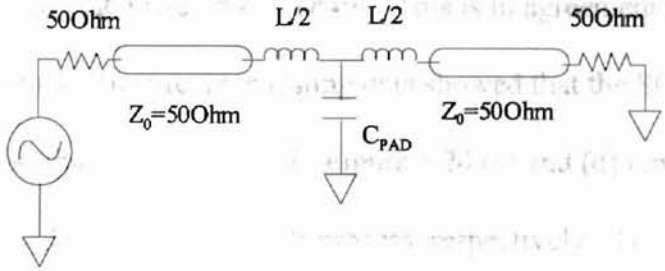
The time constant τ can be represented as

$$\tau = \frac{L}{2Z_0} \tag{3.29}$$

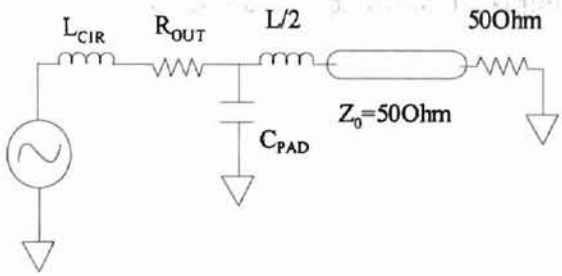
Since the t_{rise} measured is 160ps, the inductance can be derived as follows.



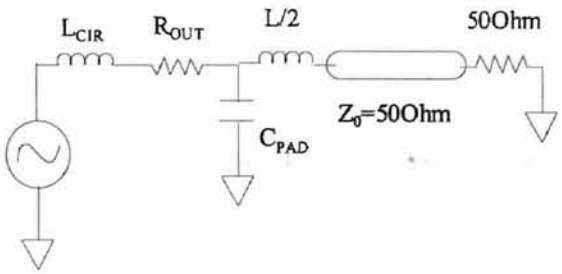
(a) SOS pad model



(b) SOI pad model



(c) SOS output buffer model



(d) SOI output buffer model

Figure 3.24 Output Pad Model for Analysis

$$L = 2Z_0\tau = 2Z_0\frac{t_R}{2.2} = Z_0\frac{t_R}{1.1}$$

$$= 50\Omega \cdot \frac{160ps}{1.1} = 7.3nH \qquad (3.30)$$

Therefore, the inductance of tip per probe is approximately 3.65nH. Since the probe tip length is about 3mm, this experimentally extracted result for L (3.65nH) is consistent with the general rule for inductance estimation, i.e., 1nH/mm. The simulation of circuit in Figure 3.24 (b) showed that a rise time is 184ps. This is in agreement with the measured data, 160~170ps. The previous testing data showed that the SOS pad capacitance is much less than that of the SOI. Figure 3.24 (c) and (d) represent the output buffer testing system model for SOS and SOI process, respectively. The measured rise time for the SOS output buffer was 162ps while the simulation result was 149ps. The testing rise time for the SOI output buffer was 252ps while the simulation data was 203ps.

Since all the measured data of all four cases in Figure 3.24 are in good agreement with the simulation results, the pad capacitance C and probe inductance L are to be used in the redesign of 4 bit ADC system.

• Measuring system limitation

The measuring system bandwidth is limited by pad capacitance, tip inductance, probe capacitance and instrument bandwidth. The total delay of measuring system is given by [35]:

$$t_{TOTAL} = \sqrt{t_{PAD}^{\ 2} + t_{TIP}^{\ 2} + t_{PROBE}^{\ 2} + t_{INST}^{\ 2}} \qquad (3.31)$$

where t_{PAD}, t_{TIP}, t_{PROBE}, and t_{INST} are the delay caused by pad, tip, probe, and measuring instrument, respectively. Based on the testing data, probe specifications and instrument specifications, the test setup rise time is estimated to be 120ps.

- **Ground bounce on the power supply**

The ground bounce is caused by the inductance of power supply when the circuit switches at the high frequency. The testing reveals that there exist a large ground bounce in both sides of power supplies, V_{DD} and V_{SS}. The measured amplitude of this noise was 360mV and 320mV for V_{DD} and V_{SS}, respectively, when V_{DD} is 1.2V and V_{SS} is 0V. The inductance can be estimated as follows. The ground bounce voltage is

$$V_{GB} = L\frac{di}{dt} = L\frac{\Delta V}{R \cdot \Delta t} \tag{3.32}$$

where ΔV is 1.2V, Δt is 68ps, which was shown earlier in this chapter, R is 180Ω and V_{GB} is 360mV. Then the inductance is estimated as 4nH.

The ground bounce effect can be eased by adding the sufficient decoupling capacitance for filtering out the interference.

3.3 Future Design Considerations

The testing results shown above reveal some problems existing in the design and layout. Several modifications will be made to overcome these problems and improve the performances.

• **Pad size**

The effect of pad capacitance increases the rise time and decreases the bandwidth. Therefore, pad size should be kept as small as possible. It is also required to use the small pad to lessen the driving problem. The pad size will be shrunk to diamond 100μm × 100μm on the diagonal. This modification will decrease the C_{PAD} to one-eighth of 200μm × 200μm, or 200fF, 400fF for SOI and BULK process, respectively.

• **Inductance**

To ease or avoid inductance effect on the power supplies, the ground layout should be properly arranged. The input ground should be connected directly to the output ground on the layout. For CMOS logic circuits such as the output buffer, bubble detector, V_{SS} should be tied to both the input and output grounds to eliminate ground loop inductance.

• **Decoupling capacitor**

The Decoupling capacitor must be much greater than load capacitance to filter out the switching interference. The following rule should be followed for SOS and SOI layouts at all times.

$$C_{DEC} \geq 8 \cdot C_{CH} \tag{3.33}$$

where C_{DEC} is decoupling capacitance, C_{CH} is the total worst case capacitance which will charge during the switch rise or fall time.

- **Pad driver**

Pad drivers should be added at the output of the comparator, bubble detector and encoder to avoid the de-embedding problem. The taper buffer [32], or inverter chain, can be used as pad driver.

CHAPTER 4

A PROPOSED TWO-STEP NEURAL-BASED A/D CONVERTER

The studies in the area of artificial neural networks have been revitalized due to advances in VLSI technologies. In particular the Hopfield neural network, composed of one-layer neurons fully connected by feedback resistors, is widely applicable in electronic computing [9][10]. The realization of an A/D converter is a specific problem of optimization for which a Hopfield neural network can be built [8][9][10].

The implementation of Hopfield A/D converter is not suitable for 10 bit resolution application due to the worse case delay in LSB. This chapter proposes a new architecture for high-speed and high-resolution application: a two-step neural-based A/D converter. This new ADC architecture incorporates the Hopfield A/D converter into the two-step technique. It will be shown later that this is the best choice for a high-speed and high-resolution ADC in the current MOS process.

This chapter is divided into sections as follows.

Section one describes the Hopfield neural network (HNN), with symmetric and non-symmetric interconnections. The worse case delay of the non-symmetric type network is thoroughly analyzed.

Section two presents the building blocks for a proposed neural-based A/D converter. The system diagrams of 5-bit coarse and 5-bit fine ADC, as well as their simulations, are also presented in this section.

In the Hopfield neural-based A/D converter (HADC) system, the basic function of the input stage, feedback stage and bias stage is that of voltage-to-current (V/I) conversion. For this reason, the V/I converters are the critical design issues in a HADC system. The resistor is the simplest form of V/I converter. The switch type V/I converter has higher accuracy than that of a resistor type at the expense of larger area. The current mirror with an OTA (CMOTA) type V/I converters can achieve the highest accuracy and bandwidth among V/Is but the drawback is its very large size and power consumption. Section three presents all three V/I converters and their performances.

The DAC is the essential block in a two-step A/D converter system, the speed and accuracy performances of the DAC have a great effect on the entire two-step ADC and must be n bit accurate. The dynamic element matching (DEM) technique, which improves signal-to-noise ratio, has been successfully applied in DAC [25][26]. The dynamic element matching DAC is described in section four.

Finally, the performances of the proposed two step neural-based 10-bit high-speed A/D converter are discussed and estimated in section five.

4.1 Hopfield neural network A/D converter

Hopfield network is one of the most common architectures used in the neural network application due to its simplicity and quick convergence. It can be used to

implement associative memories, pattern recognition, and optimization system [9]. A/D conversion is one of the successful applications of Hopfield networks. This section discusses two kinds of HADC: symmetric interconnections and non-symmetric interconnections.

4.1.1 HADC with symmetric interconnections

A symmetric type HADC is shown in Figure 2.8. Hopfield has shown [8] that the energy or Lyapunov function for this type architecture is

$$E = -\frac{1}{2}\sum_{j=0}^{n-1}\sum_{i\neq j}^{n-1} T_{ij}\, D_i\, D_j - \sum_{i=0}^{n-1} I_i\, D_i \qquad (4.1)$$

where

$$T_{ij} = -2^{(i+j)}$$

$$I_i = -2^{(2i-1)} + 2^i\, VN_{in}$$

and VN_{in} is normalized input voltage. The energy function of a symmetric Hopfield network has many local minima. Thus, the symmetric approach can not guarantee the correctness of the converged results and the convergence problem of symmetric type has limited its application in A/D converter.

4.1.2 HADC with non-symmetric interconnections

A non-symmetric type HADC is shown in Figure 4.1. It has been shown [27] that there is a unique global minima for such an A/D system energy function. For this reason

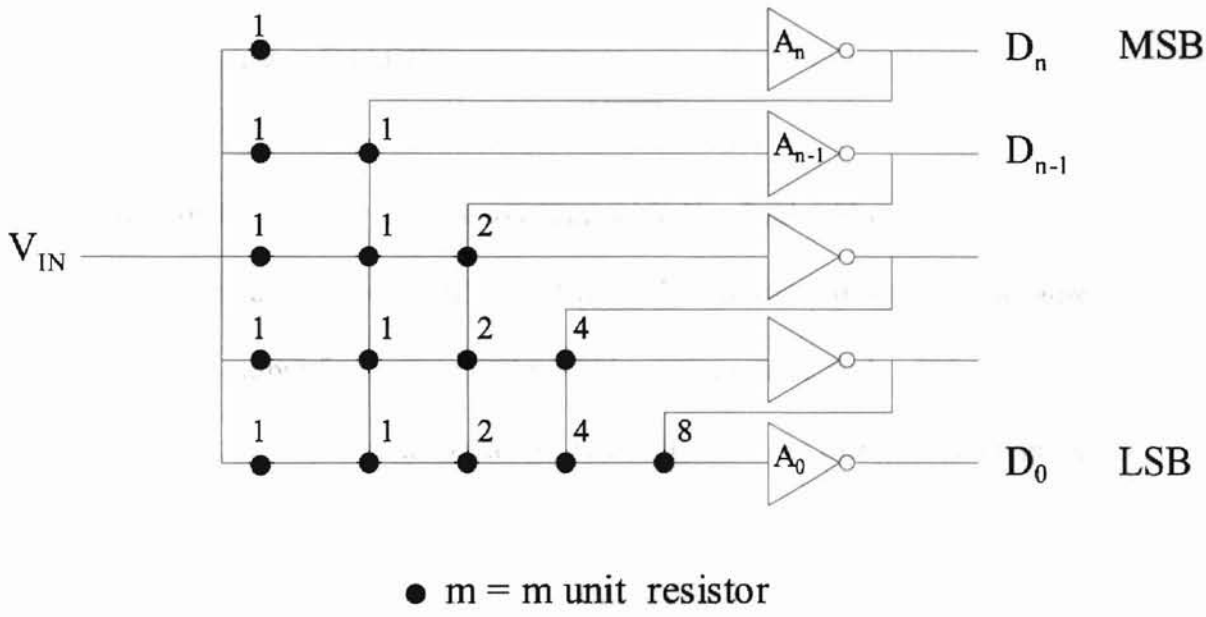


Figure 4.1 A 5-Bit Non-Symmetric Type Hopfield Neural-Based A/D Converter

it was selected to be used in the proposed implementation of a high speed, high resolution A/D converter and HADC referred to in this thesis will be the non-symmetric interconnections type. Moreover, it has a simpler form than the symmetric type. In other words, the non-symmetric type will result in a more compact design and will benefit from the improved matching and reduced power consumption.

4.1.3 Worst case delay of HADC

The worst case delay of n bit non-symmetric Hopfield A/D converter is the conversion time of an LSB of digital output when the variation of input signal causes the change of digital output from '100...00' to '011...11', or from '011...11' to '100...00'. To simplify the analysis, assume the delays of comparators are identical and represented by t_d. This assumption is readily achieved by proper selection of the geometry of each transistor used in the inverter chain, as shown in the final proposal.

For the MSB of the digital output, it takes only one t_d time to get the stable value of D_n, where D_n is the output of the MSB comparator. However, inverter chain A_{n-1} can not start the correct conversion until it get the stable value of D_n. Thus, an additional t_d is needed to achieve the correct and stable result of A_{n-1}. This conversion delay process also applies to the following inverter chain A_{n-2}, and so for the A_{n-3}, A_{n-4}, ..., A_0. Additionally, the input stage, which is V/I converter, also contributes to the conversion delay. Thus, the general expression of worst case delay can be written as follows.

$$T_{wc} = n \cdot t_d \tag{4.2}$$

where T_{wc} is the worst case delay of the n bit system and t_d is the delay of the comparators. To achieve 10 bit accuracy, each comparator should have at least four inverters due to the gain (6~8) of each inverter in velocity saturation. Therefore the minimum delay of each comparator is 4τ, where τ is the gate delay per stage. In the case of a 5 bit coarse and fine HADC system,

$$T_{wc} = 5 \cdot t_d = 20\tau \tag{4.3}$$

Then, the maximum conversion rate of the 5 bit non-symmetric Hopfield A/D converter is

$$f_{max} = \frac{1}{T_{wc}} = \frac{1}{20\tau} \tag{4.4}$$

Based on the testing data for gate delay per stage of the pad driver, which is 18ps, the maximum speed of a 5 bit HADC is

$$f_{max} = 2.8\text{GHz} \tag{4.5}$$

4.2 Two-Step Neural-Based A/D Converter Building Blocks

The new high-speed and high-resolution ADC architecture proposed in this study is a two-step neural-based ADC, which combines the HADC with the two-step technique. Figure 4.2 shows this new ADC architecture, which consists of a 5-bit coarse HADC, a 10-bit accuracy V-I converter, a dynamic element matching current DAC [25], and a 5-bit fine HADC. The 5 bit coarse A/D converter and 5 bit fine A/D converter are shown in Figure 4.3 and Figure 4.4, respectively. The simulation results for 5-bit neural-based ADC is shown in Figure 4.5. The V-I converter and dynamic element matching current

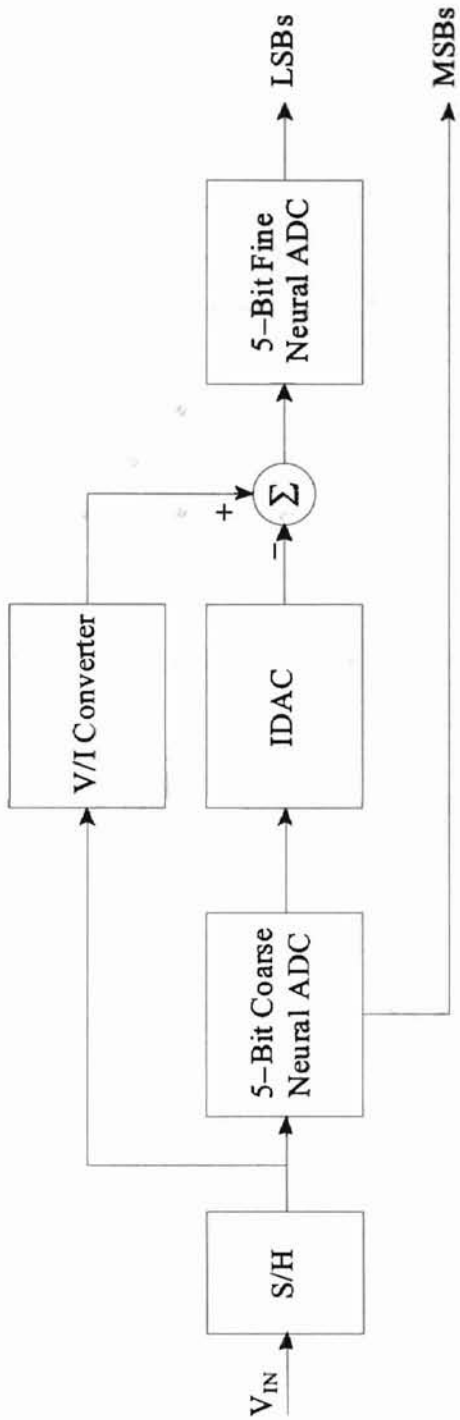
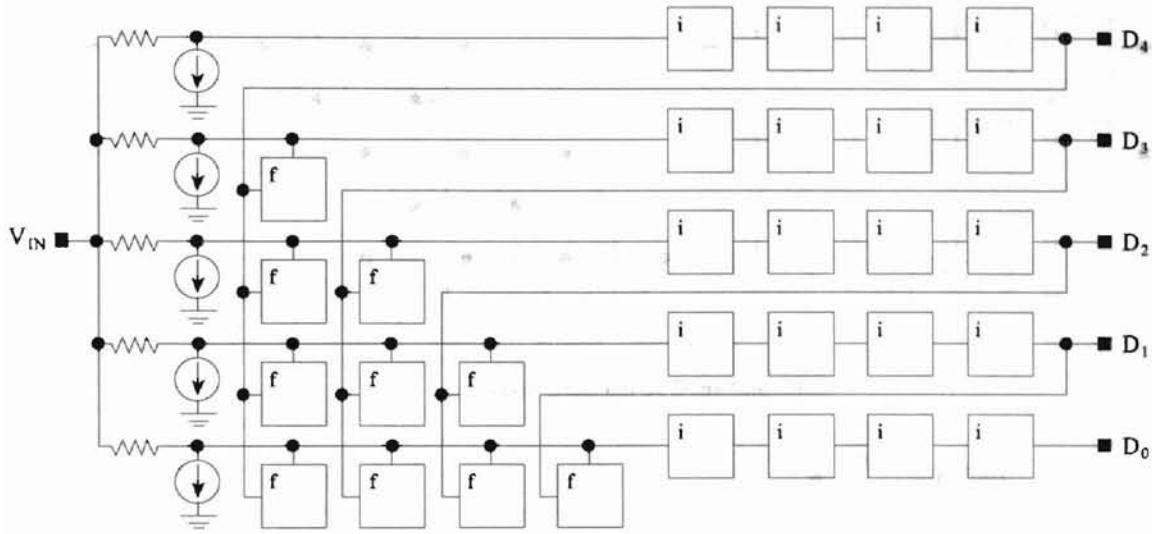
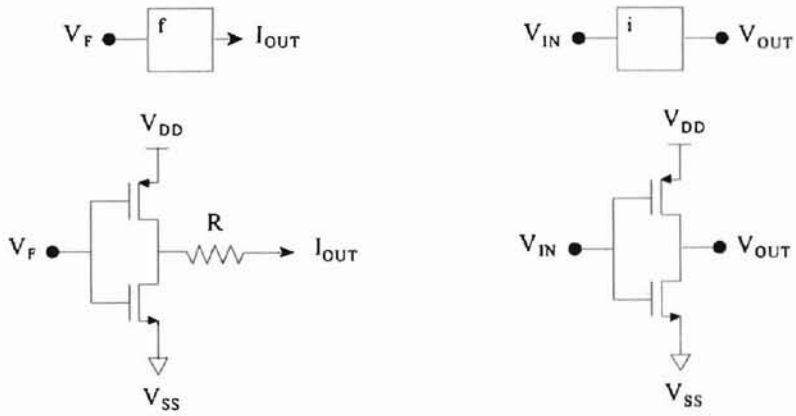


Figure 4.2 The Block Diagram of Proposed 10-Bit 2.5GHz Two-Step Neural-Based A/D Converter



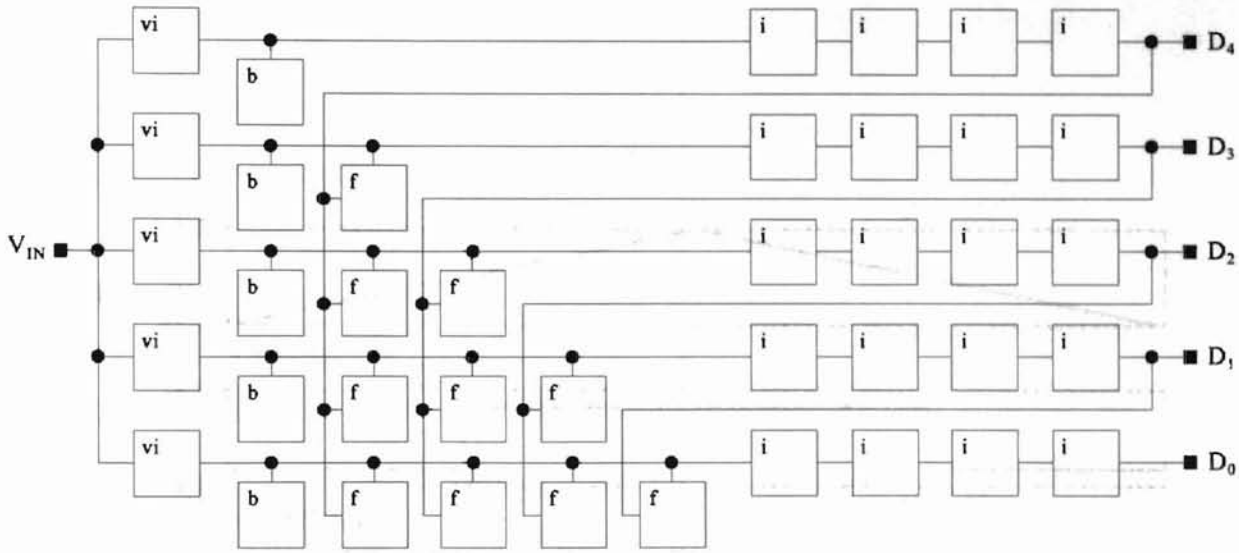
(a) block diagram of 5-bit coarse ADC



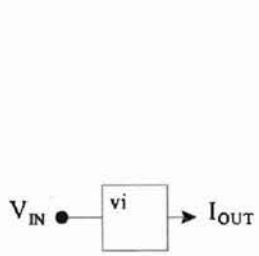
(b) feedback circuit

(c) inverter circuit

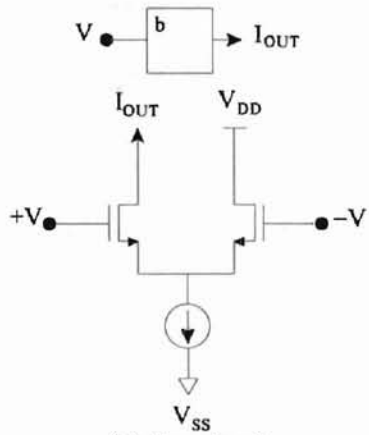
Figure 4.3 The 5-Bit Neural-Based Coarse A/D Converter



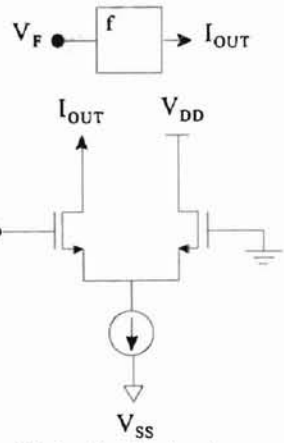
(a) block diagram of 5-bit fine ADC



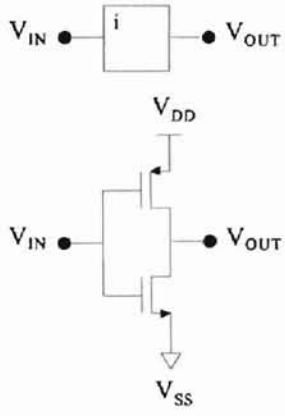
(b) voltage-current converter



(c) bias circuit



(d) feedback circuit



(e) inverter circuit

Figure 4.4 The 5-Bit Neural-Based Fine A/D Converter

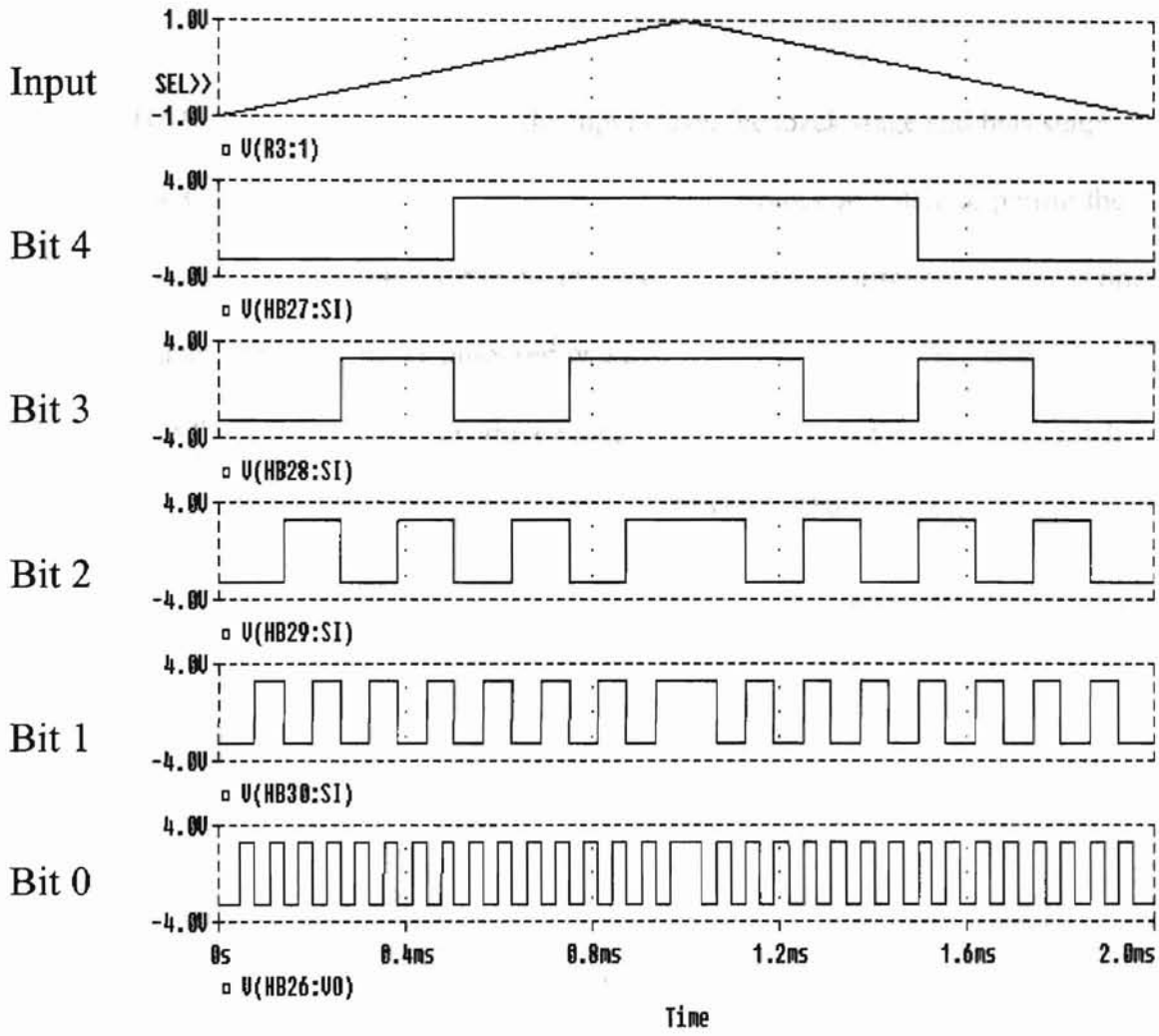


Figure 4.5 Functional Simulation Result of the 5-Bit Neural-Based Coarse and Fine ADC

DAC are discussed in the following sections.

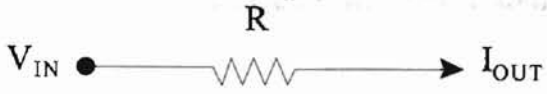
4.3 Voltage-to-Current Converter

In HADC, the voltage signal for the input stage, feedback stage and bias stage (see Figure 4.3 and Figure 4.4) are converted into their current equivalent to permit the addition at the input end of the inverter chains. Thus, voltage to current converter is one of the critical design issues in the proposed two step neural-based A/D converter. Depending on the required accuracy, three types of V/I converters, i.e., resistor, switch and CMOTA, can be chosen from to implement the HADC. The remainder of this section discusses V/I converters.

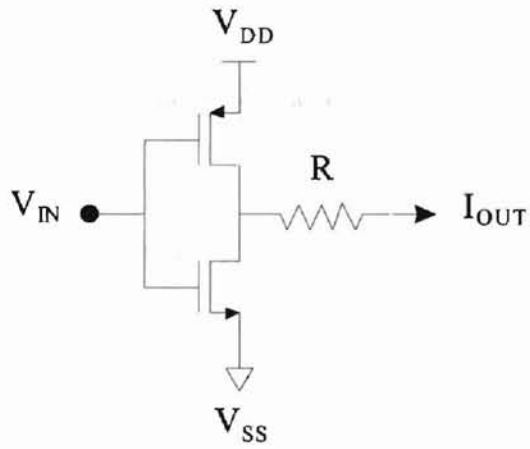
4.3.1 Resistor type

The fact is very obvious that the resistor is the simplest form of the voltage to current converter. Figure 4.6 shows the resistor type V/I converter.

Since the time constant of this V/I converter is proportional to the resistance, the small values of resistors are necessary to achieve the high speed. However, this leads to resistor matching difficulties in the MOS process [31]. For this reason, the resistor type is restricted to use in the coarse HADC, with a resolution of 5-bit, in the proposed ADC architecture. The resistor type V/I converter in Figure 4.6(a) can be used in input stage and bias stage. However, the resistor type V/I converter in Figure 4.6(b) is commonly used for feedback stage. This is due to that the input signal of a feedback stage is simply



(a) resistor



(b) resistor with inverter

Figure 4.6 Resistor Type Voltage-to-Current Converter

the digital signal from the output of HADC. Any voltage deviation in output digital signal (even though it is still logic "true") will result in a source of error for the following comparators(inverter chains) if the V/I converter in Figure 4.6(a) is used here. The V/I converter in Figure 4.6(b) eliminates this error from output digital signals.

Both the area and power consumption of resistor type V/I converter are smallest among the three different kinds of V/I converter while the resolution is limited to 5 ~ 6 bits in the MOS process.

4.3.2 Switch type

It is much easier to achieve a high accuracy current reference than a high accuracy resistor. A current source, which has 10 bit accuracy, is achievable in the existing process if proper design steps are taken. A high accuracy reference current can be generate by a current mirror with OTA (CMOTA), which will be discussed later in this chapter. Therefore, a switch type V/I converter is employed in the fine A/D converter with a resolution goal of 10 bits. Figure 4.7 shows the switch type of V/I converter.

Note that the bias stage and the feedback stage have different characteristic from the input stage. Functionally, the bias and feedback stage is similar to the switching circuit. Both of them have discrete input (voltage) and output (current) signals rather than continuous signals, which are in the input stage. Each transistor in the switch type is in either 'on' or 'off' state. Consequently, the non-linearity of switch type over the whole input range does not affect the accuracy of the states 'on' and 'off'. Under this circumstance, the accuracy of V/I converter is completely dependent on the accuracy of

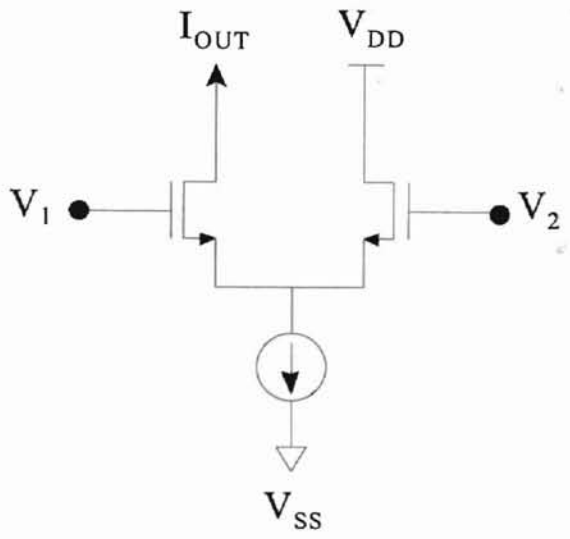


Figure 4.7 Switch Type Voltage-to-Current Converter

tail current source. The CMOTA architecture can be used to generate high accuracy current references. The speed of the V/I converter is dependent on the switch and the load. Thus, it can potentially achieve higher accuracy and faster settling time than the resistor type. The switch type is employed in the bias and feedback stage of the fine A/D converter.

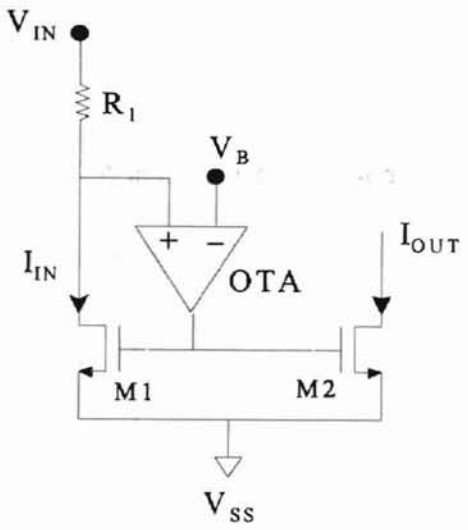
The disadvantage of this function is that it suffers from non-linearity problems, 10 bits of accuracy for whole input signal range is still difficult to achieve in the current MOS technology [33][34]. Therefore, this scheme can not be used as the input stage, which requires that 10 bit accuracy be maintained the whole range of input signal.

The switch type V/I converter has the modest area and power consumption. The 10-bit resolution can be achieved when it is used in the feedback stage.

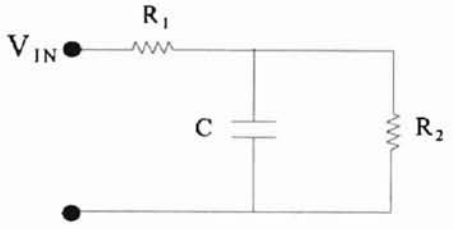
4.3.3 CMOTA type

Neither the resistor type nor switch type V/I converter can be used in the input stage of fine HADC due to their accuracy and linearity limitations. The bandwidth requirement makes it even more difficult to implement a high accuracy V/I converter in the input stage of fine HADC. The CMOTA type V/I converter is developed to be used in the input stage of fine HADC. Figure 4.8 shows the block diagram of the prototype and its small signal equivalent circuit. Note that R_1 must be trimmed here to achieve 10 bit accuracy.

As the simplified equivalent circuit shows, the input impedance of the voltage to current converter is



(a) basic circuit diagram



(b) equivalent small circuit

Figure 4.8 Current Mirror with OTA Type Voltage-to-Current Converter

$$Z_{in} = R_1 + \frac{R_2 \cdot \frac{1}{S \cdot C}}{R_2 + \frac{1}{S \cdot C}} \tag{4.6}$$

where C is the total input capacitance, R_2 is the input equivalent resistance exclusive of R_1 and can be represented by

$$R_2 = \frac{1}{A \cdot g_m} \tag{4.7}$$

where A is the gain of the OTA and g_m is the transconductance of transistor M_1. The input current I_{in} can be expressed by

$$I_{in} = \frac{V_{in}}{Z_{in}} = \frac{V_{in}}{R_1} \cdot \frac{S + \frac{1}{R_2 \cdot C}}{S + \frac{1}{(R_1 // R_2) \cdot C}} \tag{4.8}$$

Thus, the zero and pole of this transfer function is

$$S_{zero} = \frac{1}{R_2 \cdot C} \tag{4.9}$$

$$S_{pole} = \frac{1}{(R_1 // R_2) \cdot C} \tag{4.10}$$

If R_2 dominates over R_1, the bandwidth of the voltage to current converter at the input port is

$$\text{Bandwidth} \approx \frac{1}{R_2 \cdot C} \tag{4.11}$$

The accuracy, bandwidth and noise floor requirements for this block function are as follows.

(1) accuracy

$$R_1 > 2 \cdot 2^{10} \cdot R_2 = \frac{2048}{A \cdot g_m} \tag{4.12}$$

(2) bandwidth

$$\frac{A \cdot g_m}{C} > BW \tag{4.13}$$

where BW is the bandwidth requirement for CMOTA.

(3) noise floor

$$C > (\frac{16kT}{3\pi}) \frac{(2^{n+1})^2}{V_{FS}^{\ 2}} \tag{4.14}$$

where V_{FS} is the full scale range of input voltage of ADC.

Expression (4.12), (4.13) and (4.14) are the three critical issues for the design of OTA later on. From these equations, A and g_m can be determined. The delay of CMOTA can be estimated by the following.

$$t_{delay} = \frac{0.5}{BW} \tag{4.15}$$

The 10-bit accuracy can be achieved for the whole input range for CMOTA. However, the area and power consumption of the CMOTA are largest among the three different kinds of V/I converter due to the OTA.

The final 10-bit accurate V/I converter used in this design is shown in Figure 4.9. In order to achieve the required precision, the error due to the finite drain conductance, or channel-length modulation effect must be controlled. The cascode scheme is useful for reducing the current transfer ratio error, along with the OTA's which are employed in this design to keep drain-to-source voltages V_{DS} of source and mirror sides equal. This technique will greatly reduce the error caused by the lambda effect.

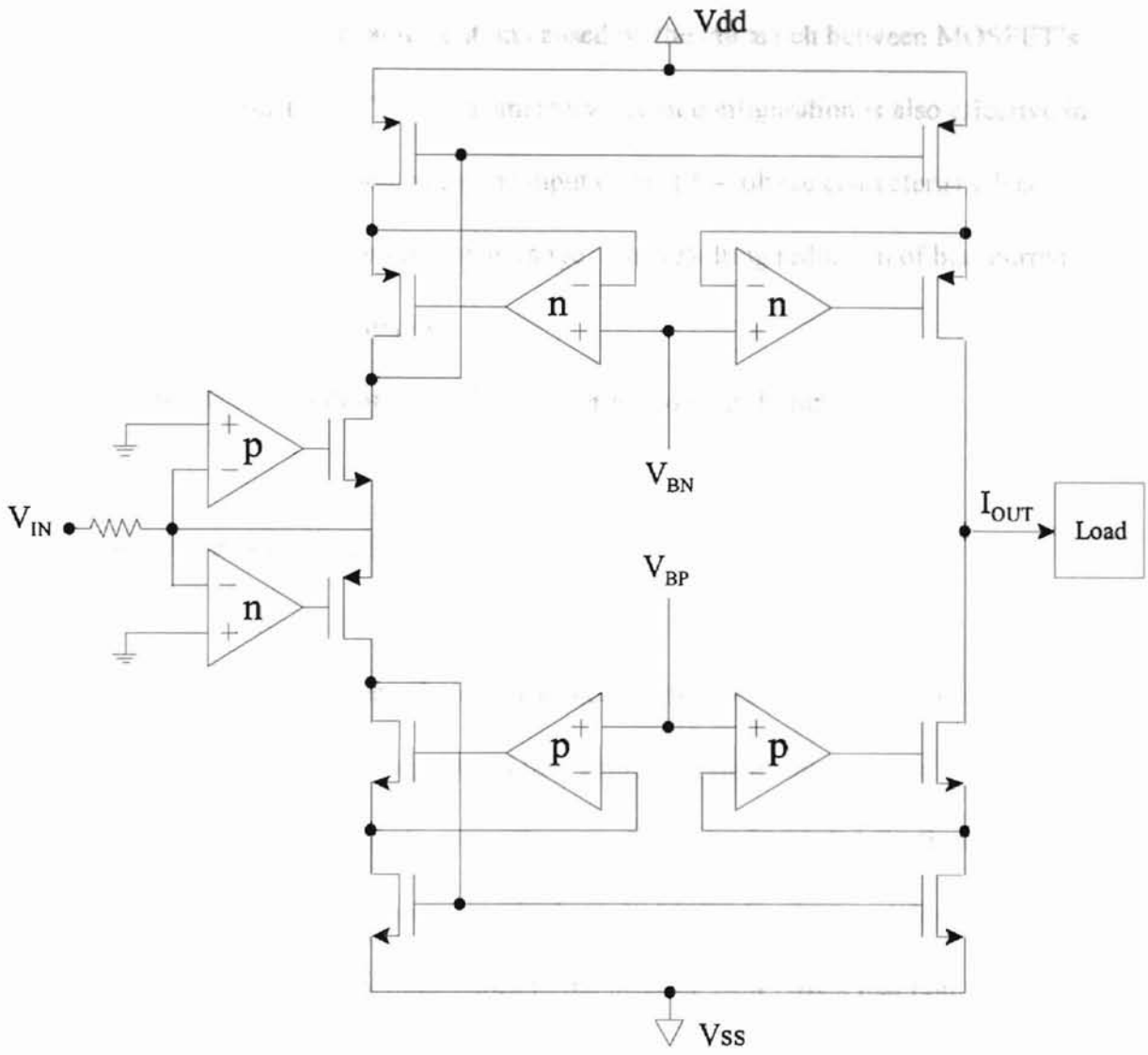


Figure 4.9 A 10-Bit Accuracy AB Class Type Voltage-to-Current Converter

The class AB configuration using both P-channel and N-channel current mirrors is used here to reduce the bias current relative to the signal current. This leads to the reduction in the offset current at the output caused by the mismatch between MOSFET's used for the current mirrors. The complementary circuit configuration is also effective in reducing the harmonic distortion, since the input current-to-voltage characteristic has quite good linearity for wide input current range. The resulting reduction of bias current also leads to lower power dissipation.

The simulation result of this V/I converter is shown in Figure 4.10.

4.4 Dynamic Element Matching (DEM) DAC

The DEM techniques have been introduced in the DAC system to decorrelate the conversion noise from the input signal and thus achieve high signal-to-noise ratio[25][26]. This kind of DAC involves the use of a bank of 1-bit DACs, the outputs of which are summed together to generate a single multi-bit DAC. For most digital input values, there are many possible input codes to the bank of 1-bit DACs that nominally yield the desired analog output value. Thus, the conversion noise arising from errors introduced by the 1-bit DACs can be "scrambled" by randomly selecting one of the appropriate codes for each digital input value.

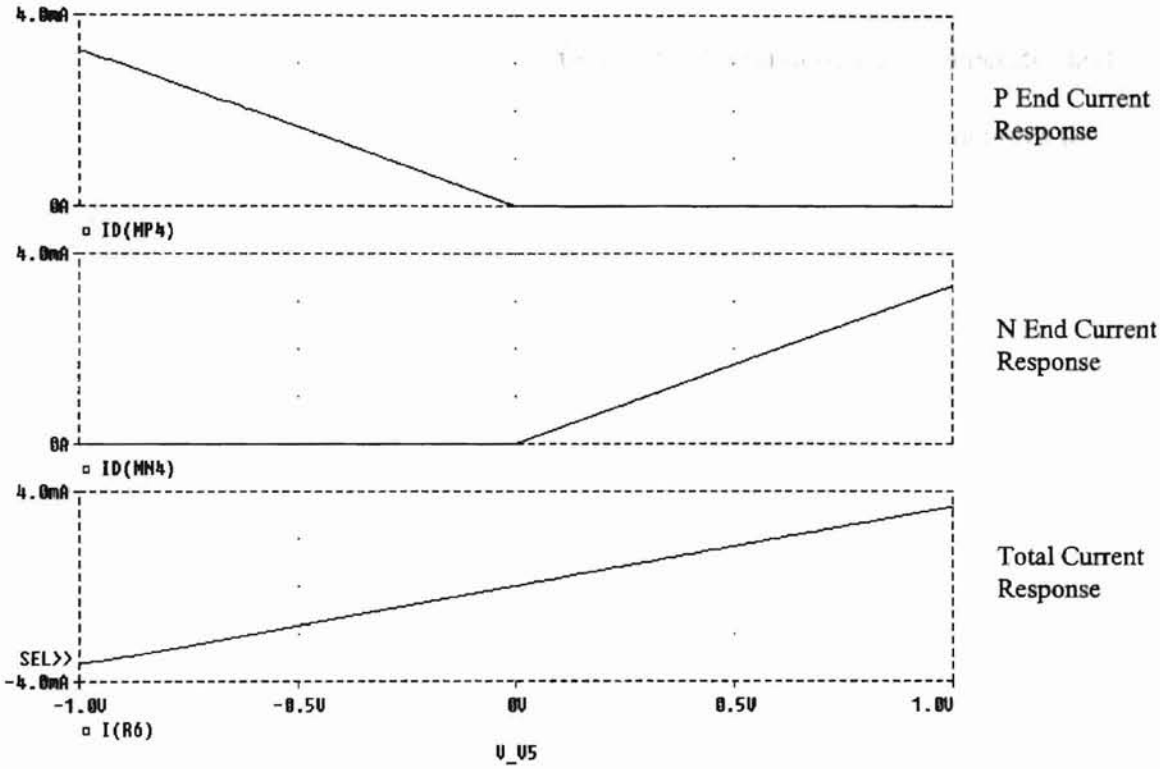


Figure 4.10 DC sweep simulation result of 10-Bit Accuracy AB Class Type V/I Converter

4.4.1 DEM DAC System Building Blocks

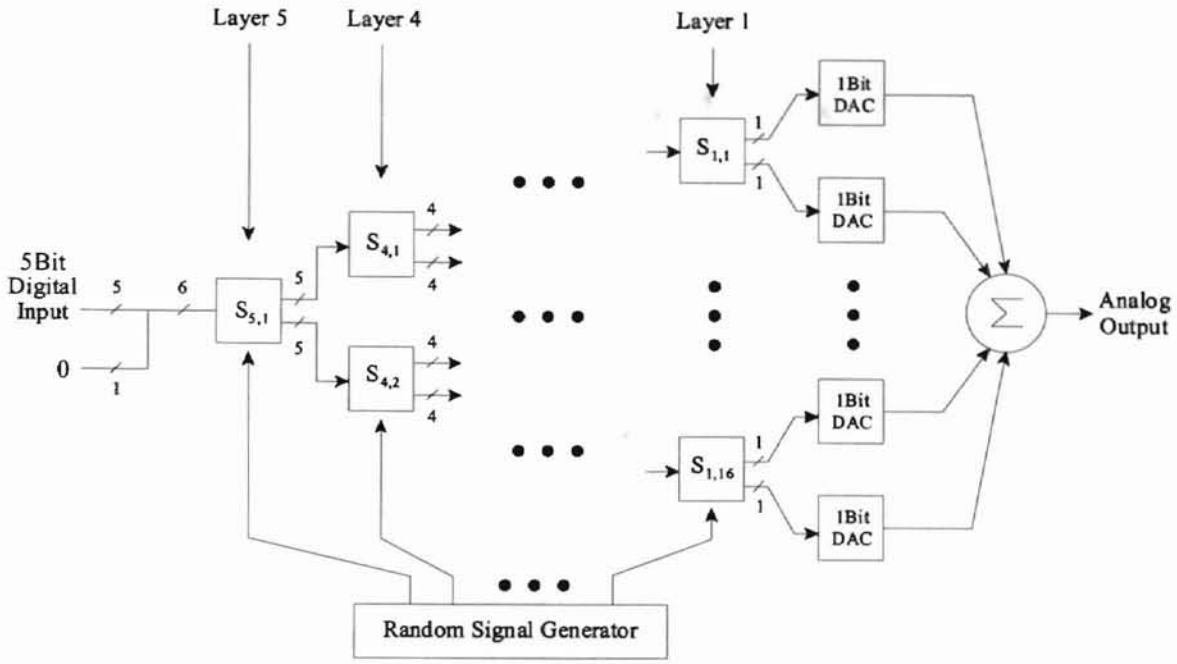
The DEM DAC architecture[25], which is used in this study, is shown in Figure 4.11. The 1-bit current DAC using an OTA topology is introduced in the next section. The tree-structured digital encoder consists of n layers of a random signal generator and switching blocks, each labeled $S_{k,r}$, where k denotes the layer number and r denotes the position of the switching block in the layer.

4.4.2 1-Bit DAC Bank

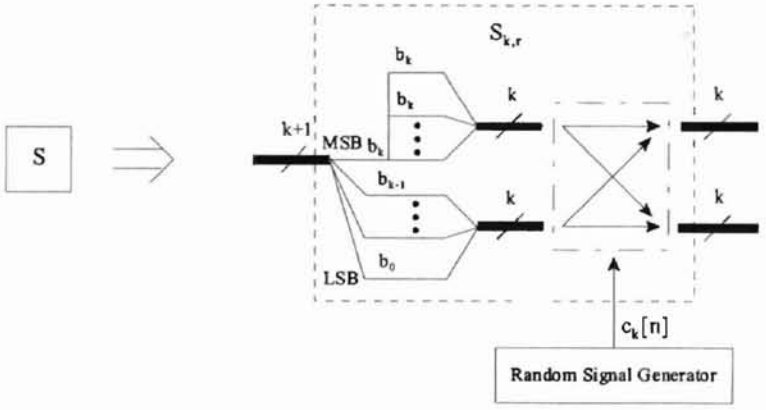
The block diagram of a 1-bit DAC bank is shown in Figure 4.12. The basic function of 1-bit DAC is that of V/I conversion except that the input is digital signal rather than analog signal. Therefore, the accuracy and bandwidth requirements for V/I converters discussed previously can be applied here. Since a high-resolution DAC is required in this design, the CMOTA is employed here to keep the 10-bit accuracy. Note that the CMOTA also provides a convenient way to implement the 1-bit DAC bank by just adding multiple mirror legs.

4.4.3 Switching Block

Figure 4.9 (b) shows the functional details of the switching block $S_{k,r}$. The switching block has one k+1-bit input, two k-bit outputs, and a random control bit input, $c_k[n]$. The random control bit is common to all the switching blocks within the k^{th} layer.



(a) block diagram of 5-bit DEM DAC architecture



(b) switching block $S_{k,r}$

(c) single switch implementation

Figure 4.11 A 5-Bit Version of the Proposed Dynamic Element Matching DAC

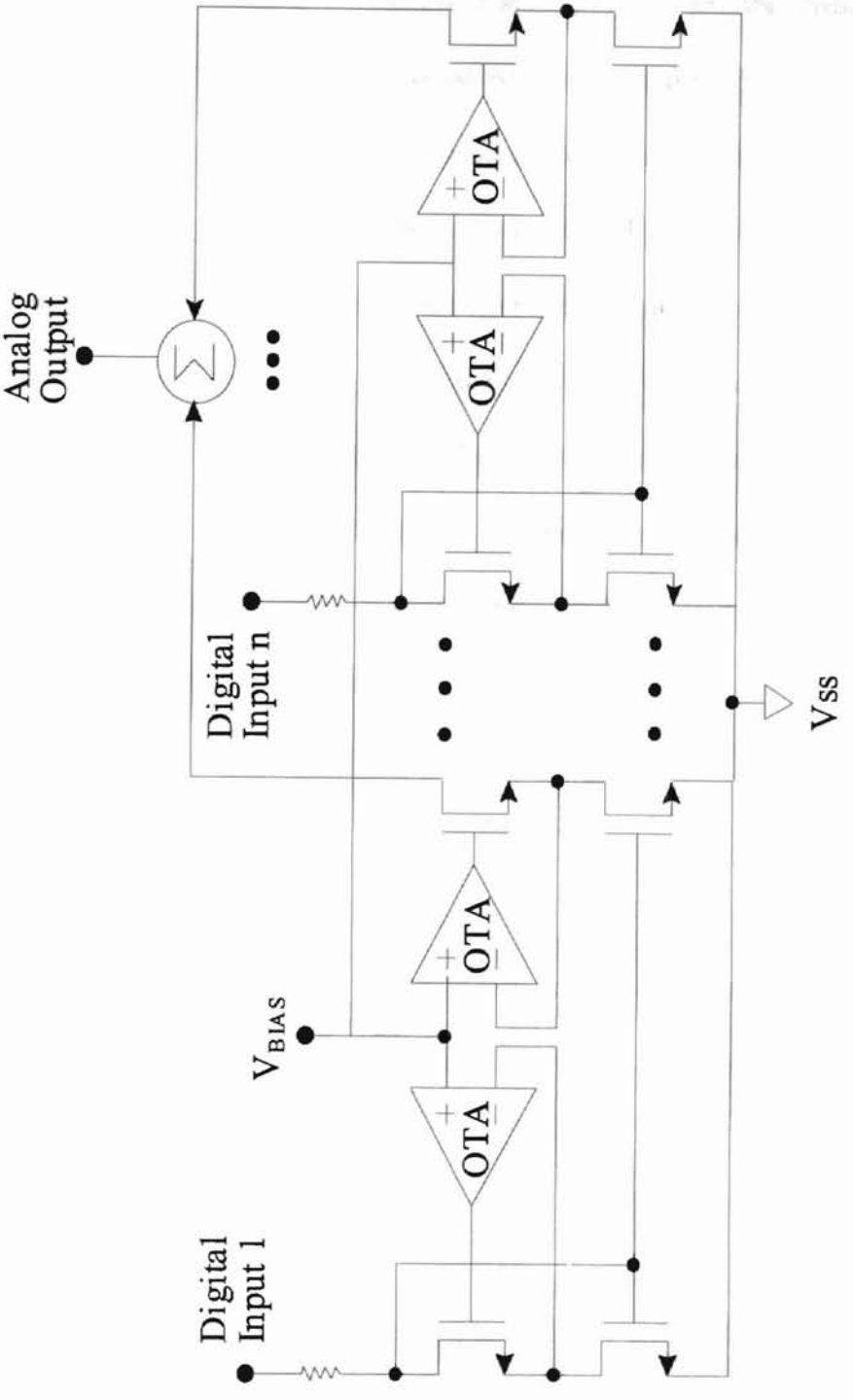


Figure 4.12 10-Bit Accuracy 1-Bit DAC Bank

The $S_{k,r}$ switching block operates such that when $c_k[n]$ is high, the most significant bit (MSB), b_k, of the input is mapped to all k bits of the top output, and the remaining k bits of the input are mapped directly to the k bits of the bottom output. When $c_k[n]$ is low, the situation is as above except that the mappings are interchanged. Thus, it follows that $S_{k,r}$ can be implemented using k binary switches, all controlled by $c_k[n]$. The process of randomly mapping the input to the outputs is referred to as random switching. At the outermost layer, i.e., k = 5, the DAC input is assigned to the $S_{5,1}$ input bits b_1 through b_5, and a zero is assigned to the input bit b_0, as indicated in Figure 4.9 (a). It is shown [25] that the digital encoder obtained by interconnecting the switching blocks of Figure 4.9 can achieve the 10-bit accuracy under the requirement of 7-bit accurate 1-bit DAC bank. This results in 3-bit (18dB) performance inprovement.

4.4.4 Random Signal Generator

Pseudo-random sequences are certain binary sequences of length $n = 2^m-1$. They have many useful properties, one of which is that their periodic autocorrelation function is given by

$$\rho(0) = 1 \qquad \rho(i) = -\frac{1}{n}, \qquad \text{for} \quad 1 \le i \le n-1 \tag{4.16}$$

These sequences have been known for a long time and they are used in scrambling, ranging-finding, fault detection, modulation, etc.

To construct a pseudo-random sequence of length $n = 2^m-1$, one needs a primitive polynomial h(x) of degree m. Since five layers are needed to be used in the DEM DAC,

the space between the adjacent control signals should be more than five to decorrelate them. Therefore, in this design, m is chosen to be $5 \times 5 = 25$ to meet the above requirements. The polynomial h(x) of degree m = 25 is defined below.

$$h(x) = x^{25} + x^3 + 1 \tag{4.17}$$

In a practical implementation this is a shift register consisting of 25 D flip-flops. Figure 4.13 shows the topology of m = 25 pseudo random signal generator.

4.5 Performances of proposed two step neural-based A/D converter

The block diagram of the 10 bit 2.5 GHz converter is shown in Figure 4.2. The functional simulation results of neural-based A/D converter and voltage-to-current converter have been shown in Figure 4.5 and Figure 4.10, respectively. In this section, the conversion rate of the neural-based ADC is fully discussed first. The performances of proposed 10-bit A/D converter system, resolution and speed, are estimated later.

4.5.1 Conversion rate

Expression (4.3) and (4.5) indicate the worst case delay and maximum speed of 5 bit neural A/D converter. The total delay of 10 bit A/D system consists of three major factors: the 5 bit coarse converter delay, DAC delay, and 5 bit fine converter delay. Then the worst case delay of the 10 bit system is

$$T_{WC} = T_{WC\_CADC} + T_{WC\_DAC} + T_{WC\_FADC} \tag{4.18}$$

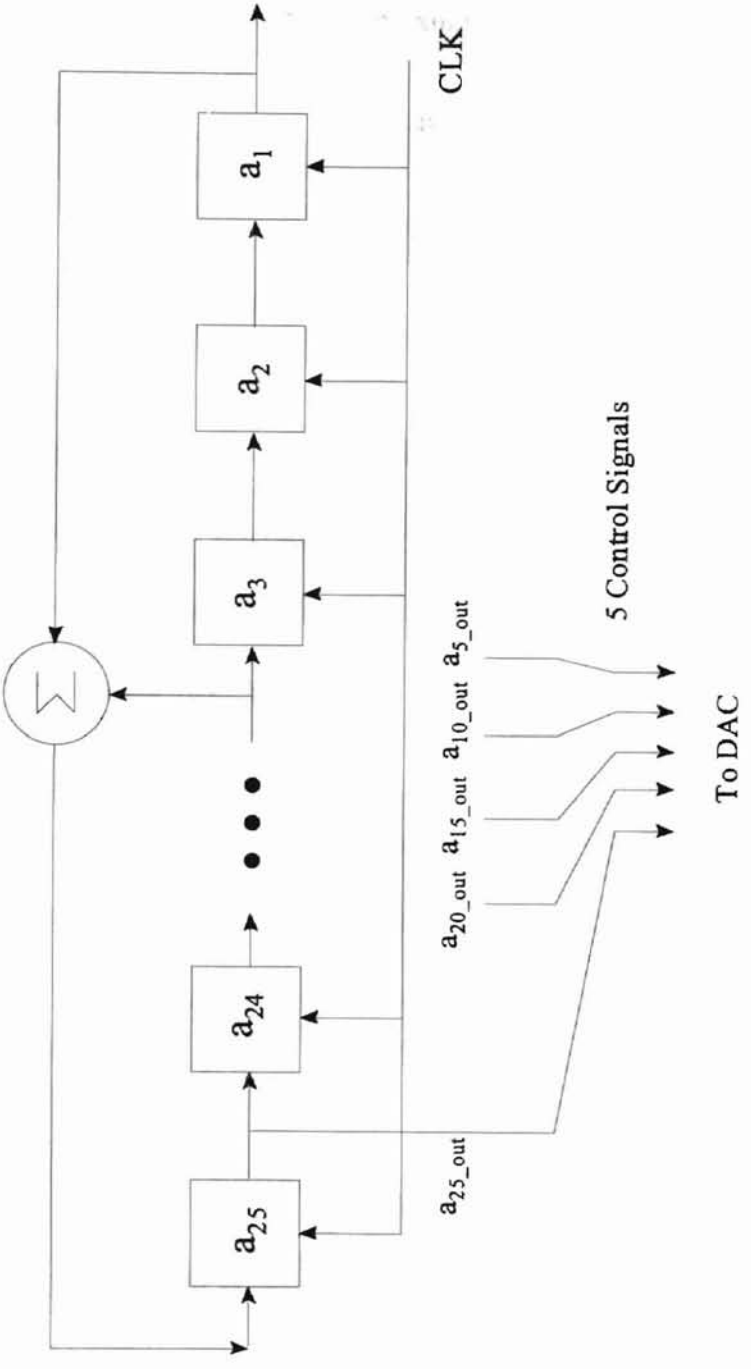


Figure 4.13 Pseudo Random Signal Generator

Assume that the DAC delay is 12τ, which can be achieved by design the switching blocks properly. Here τ is the gate delay per stage, i.e., 18ps based on the testing data in Chapter 3. Substitute equation (4.3) into (4.18), the maximum speed of the 10 bit system is

$$f_{max} = \frac{1}{T_{wc}} \cong \frac{1}{20\tau + 12\tau + 20\tau} = \frac{1}{52\tau} = 1.1\text{GHz} \tag{4.19}$$

4.5.2 Accuracy and bandwidth

Since it is feasible to achieve the high accuracy for the current reference, the accuracy and bandwidth of V/I converter used in the DAC and the fine ADC are then the critical issue to achieve the goal of 10 bit 2.5GHz two-step neural-based A/D converter. Therefore, the accuracy and bandwidth of the CMOTA V/I converter are now analyzed for the proposed 10 bit A/D system.

The schematic of this voltage-to-current converter is shown in Figure 4.9. The requirements of accuracy and bandwidth have been shown in (4.12) and (4.13). Assume the gain of OTA is 200, which is achievable even for a short channel length OTA. R_1 is chosen to be 500Ω. From (4.12),

$$g_m > \frac{2048}{A \cdot R_1} = \frac{2048}{200 \cdot 500} = 0.02048 \tag{4.20}$$

Then W_1 should be greater than 106μm.

W_1 is set to be 500μm here to make the design simple and compensate the design for geometric variations. Since the input capacitance of OTA decreases the bandwidth of the system, the width of the OTA transistors should be as small as possible. On the other

hand, the high accuracy requires large transistors, which lead to the small bandwidth. The compromise is

$$W_a = \frac{1}{3} \cdot W_1 = \frac{500\mu m}{3} \cong 166\mu m$$

W_a is set to be 150μm in this design.

From (4.13), the bandwidth of the voltage-to-current converter is now

$$BW = \frac{A \cdot g_m}{C} > \frac{200 \cdot 0.097}{(500+150) \cdot 10^{-12}} = 29.8 \text{ GHz} \qquad (4.21)$$

4.5.3 Area and power dissipation

Based on the existing layout of functional blocks in two-step neural-based ADC, the area of the proposed ADC, which includes 5-bit coarse HADC, DEM DAC, V/I converter, and 5-bit fine HADC, is estimated to be 59.6mm^2. The power dissipation is about 1 Watt.

4.5.4 Comparison between two-step neural-based ADC and two-step flash ADC

From the testing data in Chapter 3, we can estimate the performances of two-step flash ADC and list them as follows. The performances of two-step neural-based ADC are also listed below as comparison.

	Neural Type	Flash Type
1. Dynamic Range (R)	60dB (10bit)	60dB (10bit)
2. Maximum Conversion Speed (S)	1.1GHz	1.7GHz
3. Power Dissipation (P)	1Watt	3.6Watt
4. Area	59.6mm^2	205.6mm^2
5. Criterion Factor (R × S / P)	66	28

Item 5 is a comprehensive criterion factor which includes performances of dynamic range (resolution), speed relative to the power consumption. From this criterion factor, we can see that the two-step neural-based ADC is better than two-step flash ADC for high-speed, high-resolution per watt and a better choice for low-power applications.

CHAPTER 5

CONCLUSIONS AND SUGGESTIONS

The growth in the use of digital systems has increased the use of monolithic high speed and high resolution A/D converters as the interface for the acquisition and measurement of many signals that exist in the real world as spectrums of analog waveforms. To this end a 10 bit 2.5 GHz A/D converter has been designed and developed in this study.

The status of the art in A/D converters includes many different types of architecture, but for high speed and high resolution application the two step flash approach is the most common and desirable choice. Therefore, the reviews of three kinds of the two step flash types: subrange, two step with residual scaling and subrange with partial scaling, are presented following the introduction of this paper.

Folding and interpolation architecture was presented which has been implemented in the bipolar technology. This architecture employed much fewer comparators in the bipolar process than a fully parallel converter, so it has the advantages of small die area, lower power dissipation and easier matching. A very attractive characteristic is that no sample and hold circuit is required. To incorporate the MOSFET devices into this architecture, the complete analysis of folding with MOSFET was done. The analysis revealed two defects on the folding and interpolation architecture with MOSFET. The folding number is restricted to two due to the non-linearity of the MOSFET device. That

means this architecture with MOSFET device has no advantages over the fully flash because a large numbers of comparators are still needed. Thus, the problems of area, power consumption and matching make the implementation of folding and interpolation architecture with MOSFET impossible in current technology. Moreover, the bandwidth requirement of 234 GHz is beyond the current processes (see Appendix A).

The Neural network has shown its capability in the application of A/D converter since Hopfield presented a network (Hopfield neural network) as one implementation of A/D converter in 1984. The analysis in this study showed that the non-symmetric Hopfield neural network A/D converter has greater performances over the traditional flash type in the resolution range of 4-5 bits especially in matching, area and power consumption. To make the neural-based converter acceptable for 10 bit applications, a two-step technique is incorporated into the HADC to produce the proposed two-step neural-based ADC. Three different kinds of V/I converters were discussed. The resistor type could be used in the coarse HADC stages: input, bias and feedback. The switch type V/I has 10 bit resolution, but its linearity problem restricts its application to the coarse or fine HADC stages: biasing and feedback. The class AB CMOTA type can achieves 10 bit accuracy without sacrificing the linearity performance, so it can be used in the input stage of fine A/D converter. The price of its advantages is that it require more complex circuitry and thus larger area than the previous two types. Since high accuracy voltage-to-current converters are needed in the 10 bit two step neural-based A/D converter to achieve the best overall performance, the CMOTA is used in this study. The CMOTA architecture can also be employed in 1-bit bank of DEM DAC to achieve 10-bit accuracy

for 1-bit DAC. Dynamic element matching (DEM) technique is used to achieve high signal-to-noise ratio for DAC.

Conclusively, the two step neural-based A/D converter is the best solution to the high speed and high resolution with 10 bits A/D converter in the current available technology. The functional blocks of this kind of ADC system have been designed in this study. Several critical issues are needed to study in the future. First, a high speed and wide bandwidth sample and hold circuit must be designed. The circuit should have high noise immunity and low offset voltage. Second, the fast and accuracy DAC and V/I converter have to be verified by combining simulations with fabricated test data. The HADC has also to be confirmed for its conversion rate and resolution by the testing.

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APPENDIX A

FOLDING AND INTERPOLATION A/D CONVERTER

As stated previously, the full flash A/D converter suffers from large number of comparators, which leads to large area, high power consumption and large input capacitance in high resolution approach. Meanwhile, the two step flash A/D converter needs the high speed sample and hold function as well as subtraction function which are not feasible for current process. In this appendix an architecture using folding and interpolation techniques is investigated, which is capable of achieving a large analog bandwidth and high resolutions without incurring the power and area penalties associated with the flash architecture and using high speed sample and hold circuit associated with the two step converter. This architecture has been implemented in bipolar process successfully [4][5][6].

MOSFET is widely used in various VLSI systems. Nevertheless, as stated later, some limitations on MOSFET make it uneconomical to incorporate MOSFETs into the folding and interpolation architecture. The main limitation is caused by the inherent limitation of soft non-linearity of MOSFET differential pairs.

Since the design of a conversion system such as folding and interpolation converter begins with an analysis of the system, the requirements and restrictions (or limitations) of a folding and interpolation system are analyzed and summarized in this

appendix. The derived performance constrains will demonstrate the limit of a folding ADC system.

Four main issues, system and block transfer functions, general requirements, folding limitations and interpolation restriction, are included in the analysis of a proposed 10-bit folding and interpolation ADC.

The proposed folding and interpolation architecture with MOSFET is illustrated in Figure A.1.

A.1 Block transfer functions

The analysis of block transfer functions will reveal the zero-pole characteristics of each block and the system. Therefore, many system performances, such as gain, bandwidth, stability and accuracy, can be estimated from the transfer functions. In this section, gain and bandwidth requirements will be given out based on the analysis of transfer functions.

The transfer functions of buffer stage, source follower and folding stage are analyzed and then the system transfer function is introduced.

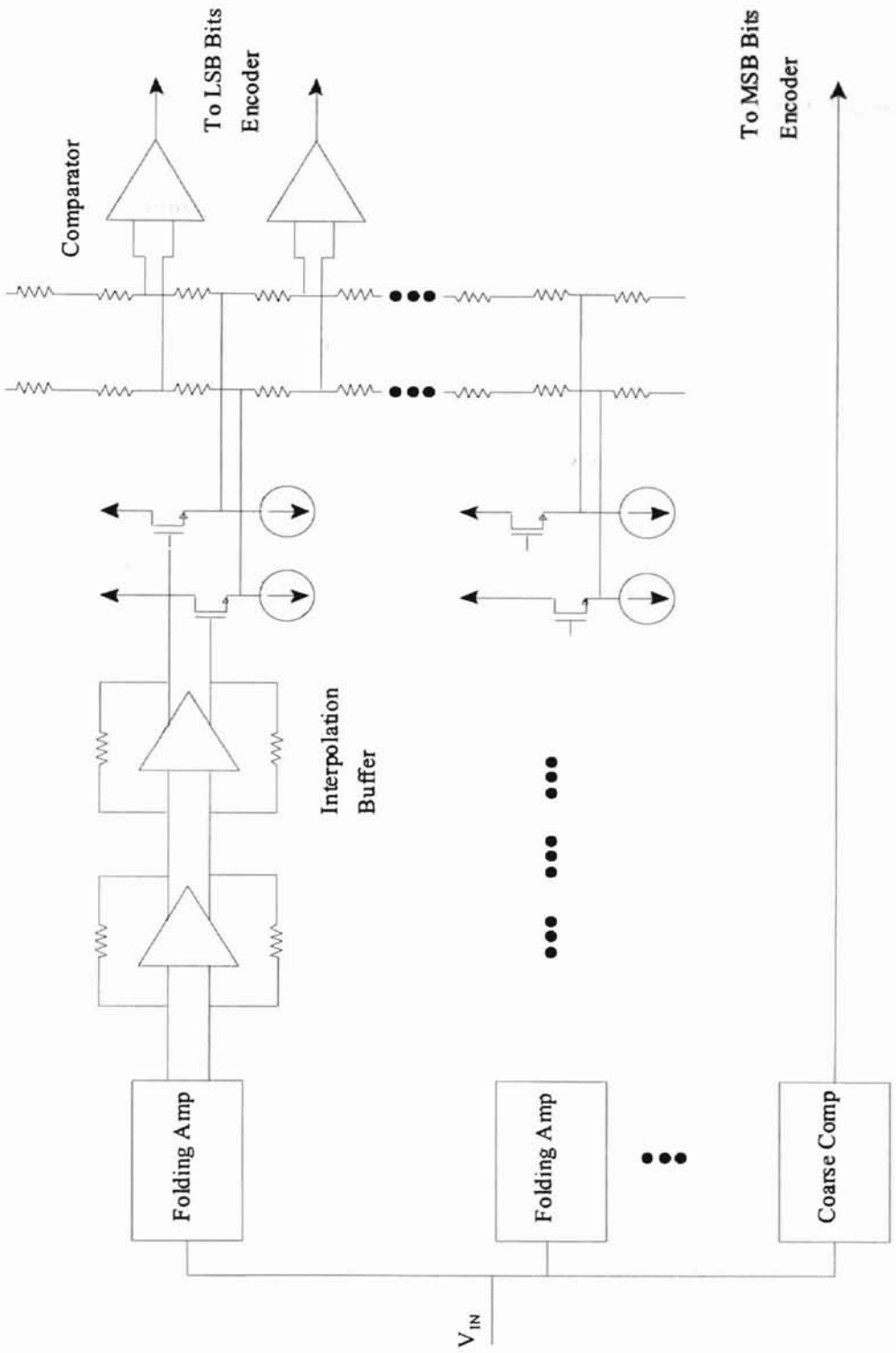


Figure A.1 10-bit 2.5 GSPS Folding and Interpolation ADC Block Diagram

A.1.1 Buffer stage

The buffer stage and its small signal equivalent circuit are shown in Figure A.2.

The transfer function of buffer stage is

$$A_{V2} = \frac{V_o}{V_i} = -\frac{g_{mb}}{sC_{outb} + g_{outb}} \tag{A.1}$$

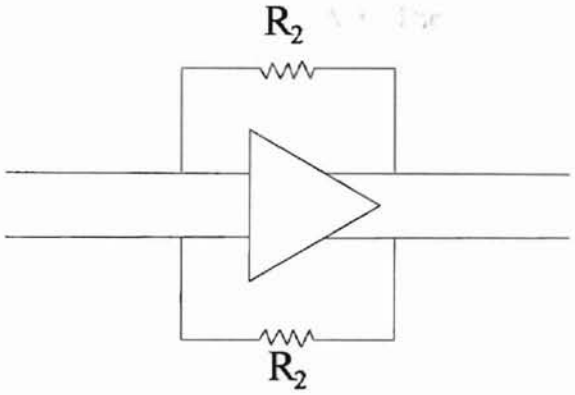
Where g_{mb} is the transconductance of OTA in buffer stage.

$$C_{outb} = C_{gss} \tag{A.2}$$

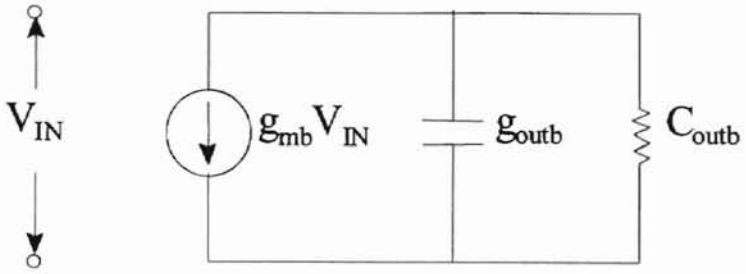
$$g_{outb} = g_{ob} + g_2 \tag{A.3}$$

$$g_2 = \frac{1}{R_2} \tag{A.4}$$

C_{gss} is the gate-source capacitance of source-follower and g_{ob} is the output conductance of buffer stage.



(a) Interpolation Buffer



(b) Small Signal Equivalent Circuit

Figure A.2 (a) Interpolation Buffer (b) Small Signal Equivalent Circuit

A.1.2 Source follower

The source follower is shown in Figure A.3. The transfer function of source follower is

$$A_{V3} = \frac{V_o}{V_i} = \frac{g_{ms}}{g_{ms} + 1/Z_o} \tag{A.5}$$

Where g_{ms} is the transconductance of source-follower and Z_O is the equivalent impedance of interpolation resistor strings and their parasitic capacitors.

From the transmission line theory, we have

$$Z_O = \sqrt{\frac{R}{j\omega C}} \tag{A.6}$$

From transfer function (A.5), we know that A_V approaches 1 and has 10 bit accuracy under the following condition.

$$g_{ms} > 2^{11} \cdot \frac{1}{Z_o} \tag{A.7}$$

The resistance R should be big enough to make to satisfy the above condition. However, large R affects the bandwidth since the bandwidth of the source follower is

$$BW = \frac{1}{2\pi(\frac{R}{R \cdot g_{ms} + 1})C} \tag{A.8}$$

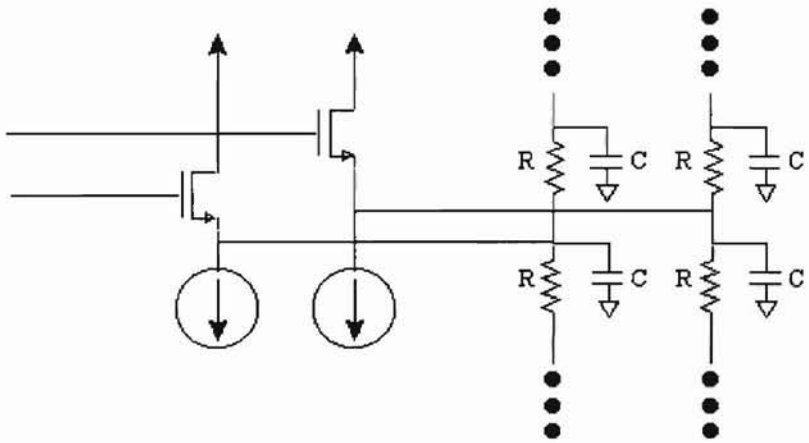


Figure A.3 Schematic of Source Follower

A.1.3 Folding stage

The folding stage and its small signal equivalent circuit are shown in Figure A.4.

Assume that input signal is

$$V_{IN} = V_{FS}\,SIN(2\pi\, f_{IN}) \tag{A.9}$$

After folding,

$$\Delta I = g_{mf}\frac{V_{FS}}{N_F}\,Sin(2\pi\, f_{IN}\, N_F\, \pi/2) \tag{A.10}$$

Where N_F is the folding factor and g_{mf} is the transconductance of folding amplifier. This ΔI, instead of V_{IN}, will be referred to as input signal in the analysis of transfer function.

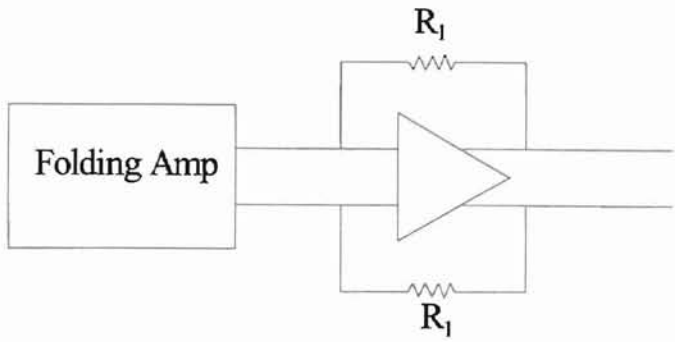
It is worth pointing out that the folded signal has a bandwidth of $N_F \cdot \pi/2$ of the full scale input signal bandwidth due to the nonlinear folding operation.

The transfer function of the folding stage is

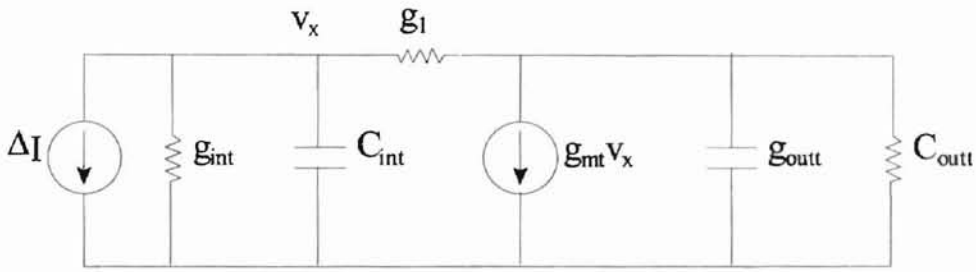
$$A_{ZI} = \frac{V_o}{\Delta I} = \frac{g_{mt} - g_1}{g_1(y_1 + y_2 + g_{mt}) + y_1 y_2} \tag{A.11}$$

Where g_{mt} is the transconductance of OTA.

$$y_1 = s\,C_{int} + g_{int} = s\,C_{gst} + (N_F+2)\,g_{of} \tag{A.12}$$



(a) Folding Stage



(b) Small Signal Equivalent Circuit

Figure A.4 (a) Folding Stage (b) Small Signal Equivalent Circuit

$$y_2 = s\,C_{outt} + g_{outt} = s\,C_{gsb} + g_{ot} \tag{A.13}$$

$$g_1 = \frac{1}{R_1} \tag{A.14}$$

C_{gst} and C_{gsb} are the gate-source capacitance of OTA and following buffer stage respectively. g_{of} and g_{ot} are the output conductance of folding amplifier and OTA respectively.

A.1.4 System transfer function

System transfer function is

$$A_Z = A_{Z1}\,A_{V2}\,A_{V3}$$

$$= -\frac{(g_{mt}-g_1)g_{mb}g_{ms}}{(g_1(y_1+y_2+g_{mt})+y_1y_2)(sC_{outb}+g_{outb})(g_{ms}+1/Z_o)} \tag{A.15}$$

DC transfer function is

$$A_Z(s=0) = -\frac{(g_{mt}-g_1)g_{mb}g_{ms}}{(g_1((N_F+2)g_{of}+g_{ot}+g_{mt})+(N_F+2)g_{of}g_{ot})g_{outb}g_{ms}}$$

Since $g_1 >> g_{ot}$,

$$A_Z(s=0) \approx -\frac{(g_{mt}-g_1)g_{mb}g_{ms}}{g_1((N_F+2)g_{of}+g_{ot}+g_{mt})g_{outb}g_{ms}} \tag{A.16}$$

A.1.5 Bandwidth and gain requirements

From equation (A.1), (A.5), (A.11) and (A.15), we can see that the system transfer function has four poles. There are two poles in folding stage and one pole in both of buffer stage and source follower. To simplify the analysis, we assume all of four poles are the same. In this case,

$$\omega_{3dB2} = 0.64\ \omega_{3dB1} \tag{A.17}$$

$$\omega_{3dB4} = 0.43\ \omega_{3dB1} \tag{A.18}$$

Where ω_{3dB1} is the bandwidth of single pole system, ω_{3dB2} is the bandwidth of two-pole system and ω_{3dB4} is the bandwidth of four-pole system. Therefore, the bandwidth requirement for buffer stage and source follower is

$$2.5\ \text{GHz}\ (N_F\ \pi/2)\ \frac{1}{0.43} = 18.27\ \text{GHz}\ .$$

Later in section A.3, we will see that folding factor N_F is restricted to 2 for a velocity saturation process. Thus, the bandwidth requirement for folding stage is

$$2.5\ \text{GHz}\ (N_F\ \pi/2)\ \frac{0.64}{0.43} = 11.69\ \text{GHz}\ .$$

where $N_F = 2$.

To maintain the 10-bit resolution, the voltage corresponding to one LSB at the inputs of comparators should be greater than the offset voltage of comparators. So the gain requirement for the system is

$$A_{min} = A_Z(S=0)\ \frac{g_{mf}}{N_F}$$

$$>> \frac{V_{oscomp}}{V_{FS} / 2^N}$$

The offset voltage of comparators is 10 mV. Then,

$$A_{min} >> \frac{10mV}{1V / 2^{10}} = 10 \qquad (A.19)$$

A.2 General requirements

The general requirements we discuss here are gain bandwidth product (GBP), matching (accuracy), and offset voltage.

A.2.1 Gain bandwidth product (GBP) and f_T

$$GBP = A\ \omega_{3dB} = A\ (N_F\ \pi/2)\ 2.5\ GHz$$

Using (A.19),

$$GBP \geq A_{min}\ (N_F\ \pi/2)\ 2.5\ GHz = 10\ (N_F\ \pi/2)\ 2.5\ GHz$$

$$GBP \geq 78\ GHz \tag{A.20}$$

So the process requirement is

$$f_T \geq 3\ GBP = 234\ GHz \tag{A.21}$$

A.2.2 Matching

To maintain the 10-bit accuracy, the sum of errors of ADC system is required to be smaller than half of one LSB.

$$\sqrt{\sum_i \left(\frac{\Delta m_i}{m_i}\right)^2} \leq \frac{0.5LSB}{V_{FS}} = 0.05\%$$

From (A.13),

$$\sqrt{\sum_i \left(\frac{\Delta m_i}{m_i}\right)^2} \approx \sqrt{\left(\frac{\Delta g_{mt}}{g_{mt}}\right)^2 + \left(\frac{\Delta g_{mb}}{g_{mb}}\right)^2 + \left(\frac{\Delta g_1}{g_1}\right)^2 + \left(\frac{\Delta g_2}{g_2}\right)^2}$$

Then,

$$\sqrt{\left(\frac{\Delta g_{mt}}{g_{mt}}\right)^2 + \left(\frac{\Delta g_{mb}}{g_{mb}}\right)^2 + \left(\frac{\Delta g_1}{g_1}\right)^2 + \left(\frac{\Delta g_2}{g_2}\right)^2} \leq 0.05\%$$

Now, by assuming all of the items contributing to the total errors are the same, it lead to

$$\frac{\Delta g_{mt}}{g_{mt}} = \frac{\Delta g_{mb}}{g_{mb}} = \frac{\Delta g_1}{g_1} = \frac{\Delta g_2}{g_2} = 0.025\% \tag{A.22}$$

A.2.3 Offset voltage

(1) folding stage

$$V_{osf} = \left| \pm 2\Delta V_T + \left(\frac{\Delta\beta}{\beta}\right) \Delta V \pm 2\Delta V_T \left(\frac{\Delta\beta}{\beta}\right) \right| \leq 0.5 \text{ LSB} = 0.5\text{mV} \qquad \text{(A.23)}$$

(2) buffer stage

$$V_{osb} = \left| \pm 2\Delta V_T + \left(\frac{\Delta\beta}{\beta}\right) \Delta V \pm 2\Delta V_T \left(\frac{\Delta\beta}{\beta}\right) \right| \leq 0.5 \text{ LSB } A_{VF} = 1.5\text{mV} \qquad \text{(A.24)}$$

where $A_{VF} \approx 3$.

(3) comparator stage

Each of 512 comparators in 10-bit folding / interpolation ADC architecture should satisfy the offset voltage requirement.

$$V_{osc} = \left| \pm 2\Delta V_T + \left(\frac{\Delta\beta}{\beta}\right) \Delta V \pm 2\Delta V_T \left(\frac{\Delta\beta}{\beta}\right) \right| \leq 0.5 \text{ LSB} \cdot A_V = 5\text{mV} \qquad \text{(A.25)}$$

where $A_V \approx 10$.

A.3 Folding limitations

The folding factor is the key to achieve an economical architecture and is greatly affected by the characteristics of differential pair type of BJT and MOSFET.

A.3.1 Differential pair performance

The transfer curves of BJT and MOSFET differential pairs are shown in Figure A.5. The linear region of BJT differential pair is

$$\Delta_{BL} = 4V_T = 4\times 25\ \text{mV} = 100\ \text{mV} \tag{A.26}$$

where V_T is the threshold voltage of bipolar transistors

The linear region of MOSFET differential pair is

$$\Delta_{ML} = 4V_{OD} = 4\times 250\ \text{mV} = 1\ \text{V} \tag{A.27}$$

where V_{OD} is the overdrive voltage of MOSFET transistors.

It is obvious from (A.26) and (A.27) that the linear region of BJT differential pair is much smaller than that of MOSFET differential pair.

A.3.2 Folding performance

The operation of the folding circuit is illustrated in Figure A.6.

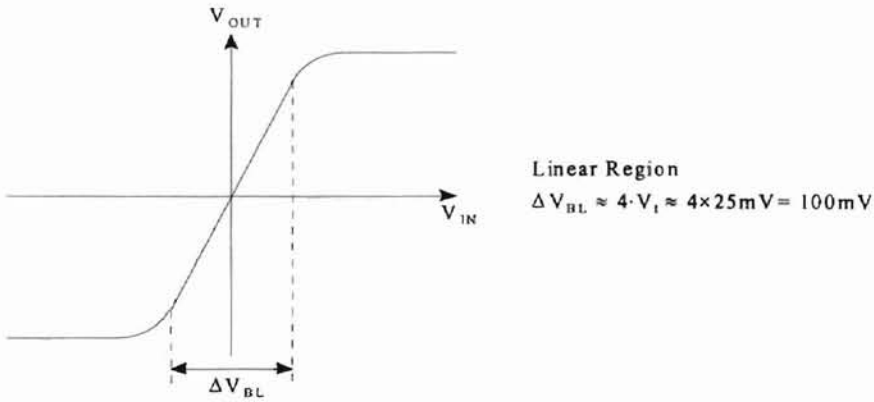
The maximum number of folding is

$$N_{MAX} = \frac{V_{FS}}{\Delta V} \tag{A.28}$$

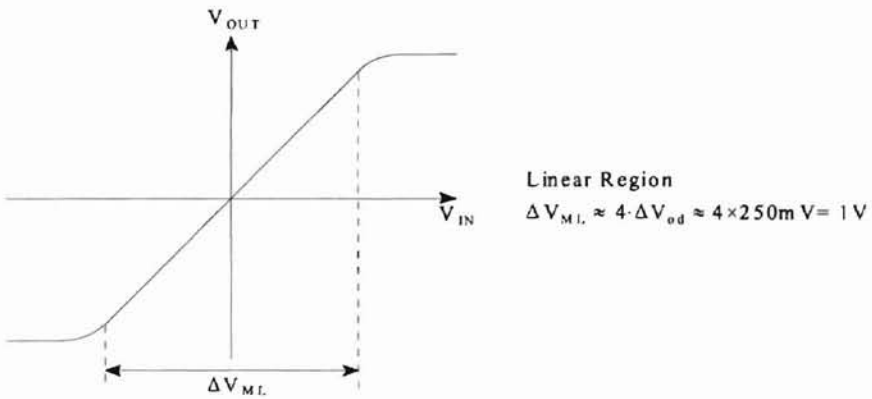
where V_{FS} is full scale voltage of input analog signal.

We can increase the folding number by 2 if using CDP (Coupled Differential pair) architecture. Then,

$$N_{MAX} = 2\frac{V_{FS}}{\Delta V} \tag{A.29}$$



(a) BJT Differential Pair Transfer Function



(b) MOSFET Differential Pair Transfer Function

Figure A.5 Differential Pair Transfer Function (a) BJT (b) MOSFET

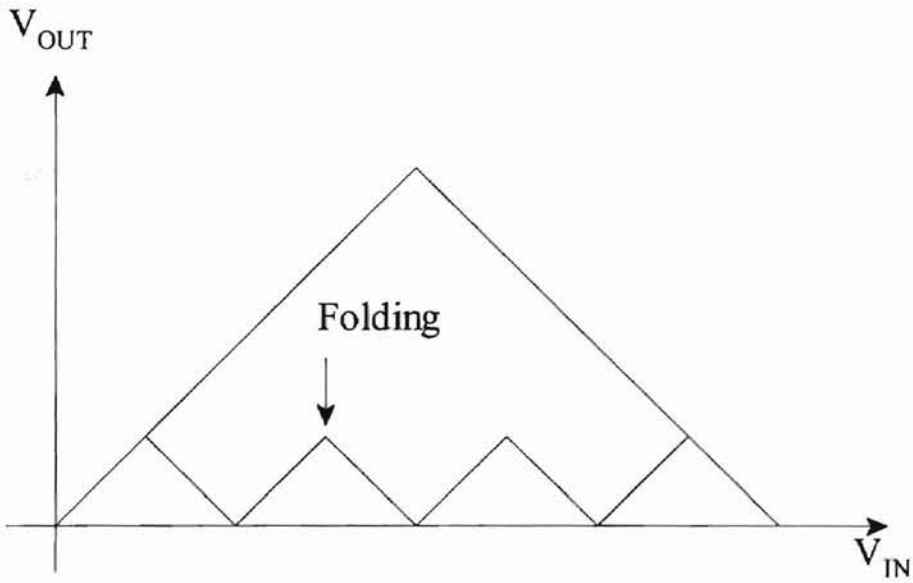


Figure A.6 Transfer Curve of Folding Circuit

If $V_{FS} = 1V$,

$$N_{MAX} = 2\left(\frac{1V}{100mV}\right) = 20, \qquad \text{for BJT,} \tag{A.30}$$

$$N_{MAX} = 2\left(\frac{1V}{1V}\right) = 2, \qquad \text{for MOSFET,} \tag{A.31}$$

The maximum number of folding for MOSFET is much less than BJT due to the soft non-linearity of MOSFET differential pair transfer function.

A.4 Interpolation restrictions

To maintain high resolution, a great number of interpolation resistors should be employed in the folding / interpolation ADC system with small folding number. If folding factor is 2, then 1024 (512×2) interpolation resistors and 512 comparators could be used to get 10-bit resolution. However, a great number of interpolation resistors and comparators will bring about the following problems.

A.4.1 Matching

The accuracy of interpolation resistors is required to be

$$\frac{\Delta R}{R} \le \frac{1}{2 \times 512} = 0.1\%, \qquad \text{for all of 1024 resistors} \tag{A.32}$$

This is a difficult requirement for IC layout and not readily achieved.

A.4.2 Power consumption

Assume C_L is the capacitance at the input end of comparators.

The noise floor requires

$$C_L \geq \frac{16kT}{3\pi}\left(\frac{2^{10+1}}{1V}\right)^2 = 88fF \qquad (A.33)$$

Since the C_{gs} of comparator is the major part of C_L, we can get the minimum width of comparators.

$$W_{comp} \geq \frac{88}{1.2}\mu m = 73\mu m$$

The current for each comparator is

$$I = k'W\Delta \approx 6.67mA$$

Then, the total power consumption of comparators is

$$P = V \cdot I \cdot N_{comp} = 3V \times 6.67mA \times 512 = 10.1W \qquad (A.34)$$

The source follower and folding circuit can be expected to consume 2 times more power. Therefore, such a large power consumed for only the comparators can not be tolerated.

A.5 Requirements for folding and interpolation architecture

Based on the above analysis of the folding / interpolation ADC, we conclude the following requirements for the folding and interpolation architecture.

(1) process $f_T > 234$ GHz

(2) mismatch of 1024 interpolation resistors < 0.1%

(3) mismatch of g_m for folding and buffer stage < 0.025%

(4) worst case offset voltage < 0.5mV (except comparators)

(5) comparator offset voltage < 10mV

(6) power consumption for comparators > 10.1W

Clearly these requirements make CMOS an unsuitable choice for a folding and interpolation ADC.

VITA

Jie Zheng

Candidate for the Degree of

Master of Science

Thesis: A PROPOSED 10-BIT HIGH-SPEED TWO-STEP NEURAL-BASED ANALOG-TO-DIGITAL CONVERTER

Major Field: Electrical Engineering

Biographical:

Personal Date: Born in Fuzhou, China, On January 5, 1964.

Education: Graduated from Affiliated High School of Fujian Normal University, Fuzhou, China in July 1980; received Bachelor of Science degree in Electrical Engineering form University of Science and Technology of China, Hefei, China in July 1985. Completed the requirements for the Master of Science degree with a major in Electrical Engineering at Oklahoma State University in December, 1997.

Experience: Raised in Fuzhou city, China; employed as an Engineer in Hitachi Fujian, Ltd., Fuzhou, China from August 1988 to December 1994; employed by Oklahoma State University, Department of Electrical and Computer Engineering as a graduate research assistant from January 1995 to present.