A 2KSPS 1mW LOW POWER MULTIBIT $\Delta\Sigma$ MODULATOR WITH 16-BIT DYNAMIC RANGE

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LIST OF SYMBOLS

AAF	Anti-aliasing filter
A_V	OTA open-loop gain
B	Number of bits in quantizer
b	Interpolative architecture's feedback gain
C_{fb}	Feedback capacitor in switched-capacitor Integrator
C_{gs}	MOSFET gate to source parasitic capacitance
C_L	Integrator load capacitance
C_{ox}	MOSFET oxide capacitance
C_{si}	Sampling capacitor in switched-capacitor integrator
DAC	Digital-to-analog converter
DR	Dynamic range
e	Quantization error introduced in ΣΔ loop
f_B	Frequency band-of-interest
FFT	Fast Fourier Transform
f_N	Nyquist frequency in hertz
f_S	Sampling frequency in hertz
g_{ds}	MOSFET drain to substrate admittance
k	Integer sample
KSPS	Kilosamples per second
L	ΣΔ modulator order
MOSFET	Metal on Substrate Field Effect Transistor
NTF	Noise transfer function
OSR	Oversampling ratio

OTA	Operational Transconductance Amplifier
P	Average noise power
S_{ee}	Output noise power
SNR	Signal-to-noise ratio or signal-to-quantization-noise ratio
STF	Signal transfer function
S_{xx}	Input signal power
t_f	MOSFET fall time from on to off state in seconds
t_s	Sampling period
V_{DAC}	DAC output voltage
V_{ds}	MOSFET drain to source voltage
V_{fs}	Full-scale voltage
V_g	MOSFET gate voltage
V_{gs}	MOSFET Gate to Source Voltage
V_{in}	Input signal of ΣΔ modulator
V_{ref}	DAC reference voltage
x	Input to the ΣΔ loop
y	Output signal of modulator

CHAPTER 1

INTRODUCTION

The demand for battery-powered applications is arousing immense interest in power efficient portable electronic devices. Meanwhile, integrated circuit (IC) densities and operating speeds have continued to climb. As chips get more complex, faster and larger, they are utilizing more power as well. In fact, with pleas for portability adding to the usual clamor for more features and faster operation, power consumption has in many cases become the limiting factor in meeting the demand of various applications today. This need has never gone unnoticed. Low power IC design has become a vibrant area of research and development, resulting in advances in low power fabrication processes, circuit techniques, dynamically programmable power supplies, and power efficient microprocessors and sophisticated mixed-mode devices.

As the demands for longer battery life on feature rich portable devices has become a multi-billion dollar industry, design of low power ICs is key to provide lengthened periods of usage without frequent recharge, this is especially true for remote unattended applications. Since the improvements of high demand long-life battery is

slow, design techniques, process selection and system architectures are critical to power efficient product design. Meanwhile, the above strong performance and cost incentives of VLSI technology have encouraged the design of analog-to-digital (A/D) and digital-to-analog (D/A) converters that are amenable to integration on the same silicon substrate with digital signal processing circuitry. Today's advanced thin-film SOI CMOS VLSI processes with lower parasitics and smaller feature sizes allow the transistors to operate at higher clock rates, in tens of gigahertz, making portable communication systems possible. However, the poor component matching and reduced power supply levels that accompany these technologies, has restricted a lot of high precision analog front-end and further revealed more difficult designs on the analog portion of the system-on-chip. Although many error correction techniques have been developed and used to implement precision Nyquist rate ADC's (NR-ADC), it is still very difficult to achieve more than 12-bit accuracy with moderate conversion rates (< 100MSPS) in wideband applications. Due to their requirements for large die size and critical component matching criteria, NR-ADCs are restricted to low-resolution, high-speed applications. Conversely, oversampled $\Delta\Sigma$ A/D converters are well suited for implementation in VLSI technology as they provide an efficient means of exchanging speed for resolution. In addition, they are very tolerant to component mismatches and circuit non-idealities. Since typically the largest component of these converters is the digital decimation filter, it directly benefits to use the enhanced circuit density and continued scaling of VLSI technology. Low-power, high-resolution in low and medium frequency wideband $\Delta\Sigma$ A/D converters have gained an unique role in cost effective mixed mode IC application in today's standard digital CMOS process. However, due to the down scaling of the power supply and high

demand for lower power consumption, the design and implementation of ΔΣ A/D converters is still an active research issue.

Thus, the motivation for this work was to design and implement a very low-power and high-resolution 2KSPS ΔΣ A/D converter for remote unattended data acquisition applications. The ΔΣ modulator was successfully designed and submitted for fabrication on silicon-on-insulator process as prototype, later measurement should reveal any improvement or modification if necessary. On the other hand, a lower power decimation filter is also being finalized at OSU AAVDC by Mr. C. M. Liu. The key blocks of the decimation filter were also fabricated on the same process with the modulator. With confidence, the system can be readily implemented and put out for second fabrication run shortly after measurements.

1.1 Organization

Following the background introduction of this work, various ΔΣ A/D converters are reviewed. Chapter 2 touches on different types of mainstream ΔΣ A/D converter, their fundamentals and performances.

In Chapter 3, the design work for the 2KSPS, 1mW, 16-bit single loop third order ΔΣ A/D modulator is covered. A full discussion of the A/D design is presented from the architectural to circuit designs along with some non-ideality effects.

In Chapter 4, at the end of preliminary design, the author concludes the project and gives some suggestions for future design works.

CHAPTER 2

Delta Sigma Modulators

Conventional high resolution A/D converters, such as successive approximation and flash type converters, operating at the Nyquist rate often do not make use of the exceptional high speeds achieved with a scaled CMOS VLSI technology. Moreover, these Nyquist rate converters require a complicated analog low pass filter or the anti-aliasing filter to limit the maximum frequency input to the A/D. On the other hand, $\Delta\Sigma$ A/D converters use a low resolution ADC (less than 5-bit quantizer, 1-bit typically), noise shaping, and a high oversampling rate to achieve high resolution through further digital decimation process.

A qualitative view of quantization noise power is shown in Figure 2.1 for each A/D conversion method. As opposed to the others, the noise shaping technique has effectively utilized today's high bandwidth processes to acquire higher resolution. The figure also demonstrates that the in-band noise power of an oversampling noise shaper is much lower than other techniques. The attenuation of the out-of-band noise power

requires digital post filtering. For the above reasons, ΔΣ ADCs are very suitable for implementation on the existing digital VLSI processes.

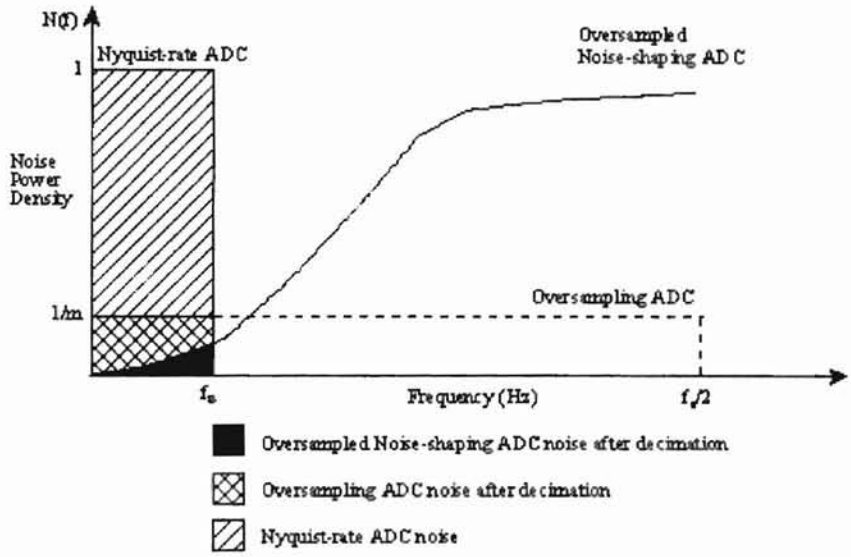

Fig 2.1 Comparison of Noise Spectrum of Different ADCs

2.1 General Interpolative ΔΣ Structure

A linear model of a general ΔΣ modulator is shown in Figure 2.1, which is also known as an interpolative structure. The output of the quantizer is fed back to the input of the opamp integrator, with transfer function H(z). At low frequencies, when the opamp's gain is high, the feedback reduces the difference between the input and the output. At high frequencies, since the opamp's gain is low, the noise is thus not reduced. In other words, the injected noise following the integrator is filtered at low frequencies.

From Figure 2.1, the signal and noise transfer functions can be derived as shown in (2.1) and (2.2). Equivalently in (2.3), the output Y(z) is a linear combination of the input signal and noise signal, with each being filtered by their corresponding transfer function, STF(z) and NTF(z) respectively.

$$STF(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1+H(z)} \tag{2.1}$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \tag{2.2}$$

$$Y(z) = NTF(z)E(z) + STF(z)U(z) \tag{2.3}$$

From the above observation, one can design H(z) with constant large magnitude from DC to f_B, the input signal bandwidth. The signal transfer function STF(z) is then

unity over the band of interest while NTF(z) is appreciably zero over this same band. Hence, with the use of additional post filtering, we remove the out-of-band quantization noise with little or no effect on the input signal.

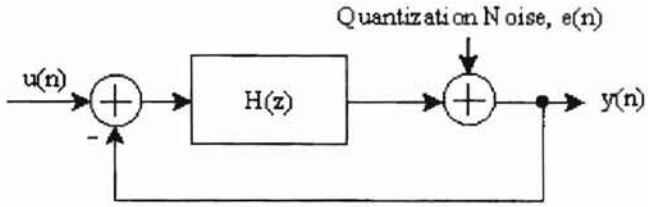

Fig 2.2 Linear Model of a General ΔΣ Modulator (Interpolative Structure)

Another useful observation is that when choosing a specific function for H(z), the maximum level of the in-band signal u(n), must remain within the maximum levels of the feedback signal, y(n). Otherwise the large gain of H(z) will cause the output signal of H(z) to saturate and overload the quantizer, eventually causing instability. This is especially true for 2-levels quantizers. On the other hand, multi-levels quantizers can significantly reduce this large quantization noise power although care must be taken to insure the multibit D/A in the feedback loop remains linear up to the ADC conversion resolution.

Further investigation of the above linear model, with the assumption that the signal to be quantized is uniformly distributed within each quantization step, results in a quantization noise q(n) power, which is represented by [26], [27]:

$$\sigma^2 = \frac{4 \cdot \Delta^2}{3 \cdot 2^{2N}} \tag{2.4}$$

where Δ is the quantization level or $\frac{V_{FS}}{2^N}$; N is the number of bits of the quantizer.

Thus, the associated quantization noise power spectral density is:

$$N_Q(f) = \frac{\Delta^2}{3 \cdot f_s} \cdot 2^{-2(N-1)} \tag{2.5}$$

where f_s is the oversampling frequency.

For $f_s >> f_B$ or the oversampling frequency much higher than the signal frequency, the shaped contribution for an L^{th}-order modulator output results in an in-band power given by [27]:

$$P_Q = \frac{4}{3} \frac{\Delta^2}{2^{2N}} \frac{\pi^{2L}}{2L+1} \left(\frac{2f_B}{f_s}\right)^{2L+1} \tag{2.6}$$

From (2.6), three pieces of valuable information on the effects of noise shaping are provided. It indicates that the quantization noise power decreases by (L+0.5) bit/octave of oversampling, or equivalently 3(2L+1) dB/octave. Secondly, each additional bit of resolution of the quantizer increases overall ADC's signal-to-noise ratio (SNR) by 6 dB.

Thirdly, for each additional bit increase in the quantizer, while maintaining the same SNR, the OSR is reduced by $\sqrt[(L+0.5)]{2^m - 1 / 2^{m1} - 1}$; where m1 and m are the original and desired number of bits of quantizer respectively. From all of the above, we are able to predict the required oversampling ratio of an L^{th}-order modulator for a specified SNR of an interpolative $\Delta\Sigma$ ADC.

Due to the reduced sensitivity of the typical interpolative structure, it is better suited to analog implementation than the error-feedback structure [5]. Thus, the error-feedback structure will not be discussed. Among the higher order modulators, several improved interpolative structures which make use of the resonators were also documented [1, 23-25]. These modified architectures have resulted in the placement of zeros in the NTF spread over the band-of-interest, this in return provides better dynamic range performance than placing all the zeros at DC, in addition to their improved component sensitivity.

2.2 Multi-Stage Cascaded ΔΣ Structure

Another approach for realizing ΔΣ modulators is to use a cascade type structure where the overall higher order modulator is constructed using a few lower orders. Theoretically, provided that the lower order single-bit modulators are stable, the overall higher order system is also stable. In addition, it also suffers fewer overtone problems than a first and second order modulator alone [27],[31].

An example of a second order modulator obtained by cascading two first order modulators is shown in Figure 2.3. The signal x[n] is input into the first modulator, and its quantization error $e_1[n]$ is treated as an input into the second modulator. The final digital output y[n] is the difference of the first stage's delayed output and second stage's differentiated output. To express quantitatively, we replace the DACs with unity gain, and the output is :

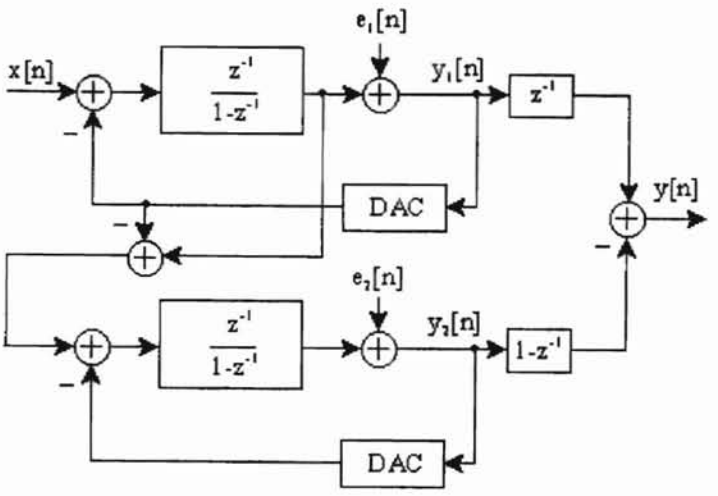

Fig 2.3 "1-1" Cascaded 2nd Order Modulator

$$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})Y_2(z) \tag{2.7}$$

where,

$$Y_1(z) = z^{-1}X(z) + (1 - z^{-1})E_1(z) \tag{2.8}$$

and

$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z) \tag{2.9}$$

Substituting (2.8) and (2.9) into (2.7), we can easily obtain

$$Y(z) = z^{-2}X(z) - (1 - z^{-1})^2 E_2(z) \tag{2.10}$$

Notice that an extra delay is experienced by the input signal, yet the modulator realizes the same output as the standard second order ΔΣ modulator. The advantage of using this cascaded structure is that the quantizer in either of the first order modulators will never overload for input signal bounded within ±V. One notorious drawback of the cascaded structures is that they require good matching between the analog and digital transfer functions as well as matching among the D/A output levels among various stages [2], [27]. Also, the integrator leakage and mismatch effects can lead to the propagation of poorly shaped noise from an earlier stage to the final outputs [29], [30], [40].

To illustrate its disadvantage, with use of Figure 2.3, if the integrator of the first stage is imperfect with a transfer function, and still the second stage is perfect,

$$H_{1x} = \frac{\alpha z^{-1}}{(1-\delta z^{-1})} \tag{2.11}$$

Manipulating (2.7)-(2.10) with substitution of (2.11), it yields Y(z) as

$$Y(z) = X(z)\frac{\alpha z^{-2}}{1-z^{-1}(\alpha-\delta)} + E_1(z)\frac{z^{-2}(1-\alpha)}{1-z^{-1}(\alpha-\delta)} + E_1(z)\frac{z^{-1}(\alpha-\delta)(1-z^{-1})}{1-z^{-1}(\alpha-\delta)} - (1-z^{-1})^2 E_2(z) \tag{2.12}$$

The first term which contains the input signal is no longer a simple delay but a potential ripple depending on (2.11). However, this transfer function can be designed to be flat at

lower baseband frequency if the oversampling ratio (OSR) is large [28]. The second term is the unshaped noise resulting from the first stage; third term is the first order shaped noise from the first stage and the last term is the desired second order shaped noise. The unshaped noise resulting from the imperfection of the integrator has the potential to dominate the overall noise performance. Thus, if more than two stages are cascaded, the cumulative effects of such quantization error leakage effect will yield diminishing returns in performance improvement [37]. Finally, some comparison of different multi-stage cascaded architectures, can be readily found in literatures [30, 32-34].

2.3 Parallel Structures

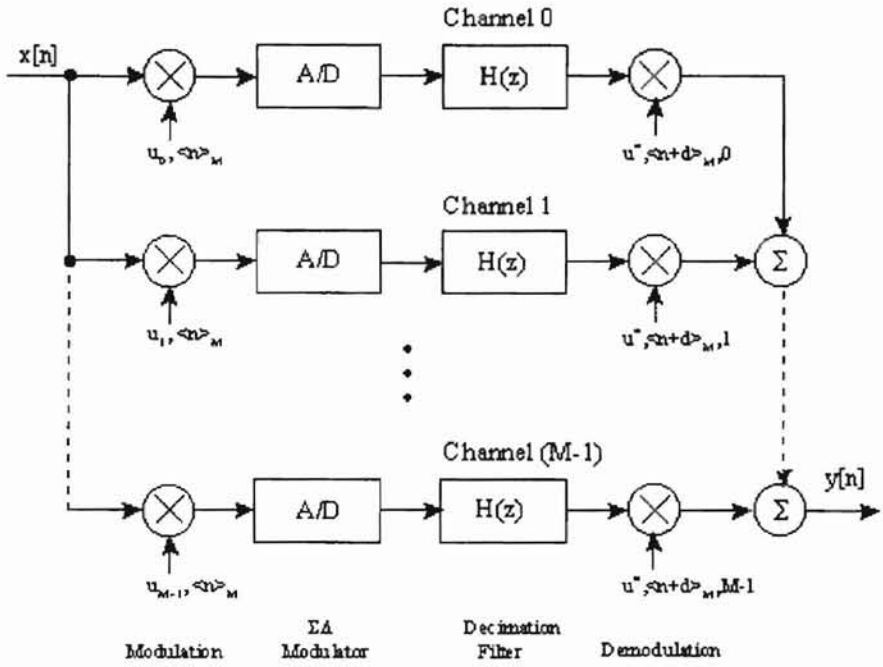

Fig 2.4 General Parallel ΔΣ Converters Architecture

Recently, a few approaches using parallelism have been presented to increase the bandwidth and/or resolution of the ΔΣ converters [42-45]. Two main approaches are time-interleaved and time-domain signal coding which is also known as ΠΔΣ. Although there are a few other approaches to parallel ΔΣ ADC, they are usually more complex to implement and thus are omitted in this review, e.g. frequency-band decomposition which uses different bandpass ΔΣ for decomposing the signal frequency band.

The general architecture was analyzed in [46] and only the results are shown for further comparison. Each channel of the parallel ΔΣ converter consists of an analog multiplier, ΔΣ modulator, digital filter and a digital multiplier, as shown in Figure 2.4. The outputs of each channel are added together to reconstruct the corresponding magnitude of the analog signal in digital domain. In Figure 2.4, the symbol <> represents a modulated (MOD) operation and the sequence $u[n]=u_{I,<n>M}$ is taken from elements of a unitary matrix (i.e. $UU^T=I$). As the input signal passes through the linear-modeled filter S(z) and the quantization noise passes through the filter with transfer function N(z), as explained in Figure 2.5. The noise paths through the parallel ΔΣ converter are shown in Figure 2.6. With multiplication of S(z) with N(z), yielding F(z), the output signal y[n] can be written as [46]:

$$y[n] = \sum_{k=0}^{\infty} f(k) \cdot x[n-k] \cdot \sum_{r=0}^{M-1} u_{r,} < n-k >_M \cdot u^{*} < n+d-k >_{M,r} \qquad (2.13)$$

where k is the delay through the signal path.

The reason for using a unitary matrix arises from recognizing the property $UU^T=I$. As the sequences $u_{i,j}$ is taken from the unitary matrix, the second summation in (2.13) is thus a comb sequence C_M. Further simplification yields

$$y[n] = \sum_{k=0}^{\infty} f(k) \cdot x[n-k] \cdot C_M(k-d) \qquad (2.14)$$

where f(k) is the Fourier Transform of F(z), i.e. the convolution of the signal filter and digital filter transfer functions in discrete time domain.

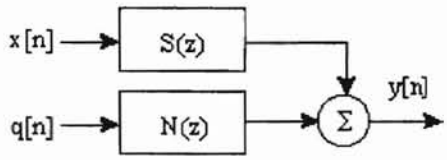

Fig 2.5 Linear ΔΣ A/D Model where q[n] is uniformly distributed white noise

This model illustrates that the modulator output of each channel is simply a delayed version of the input signal and the output of each channel is a digitally filtered version of the modulator output which is identical to the typical ΔΣ A/D converter. The comb sequence is a result of the modulation and demodulation on each signal path. The final output is then the summation of all available channels.

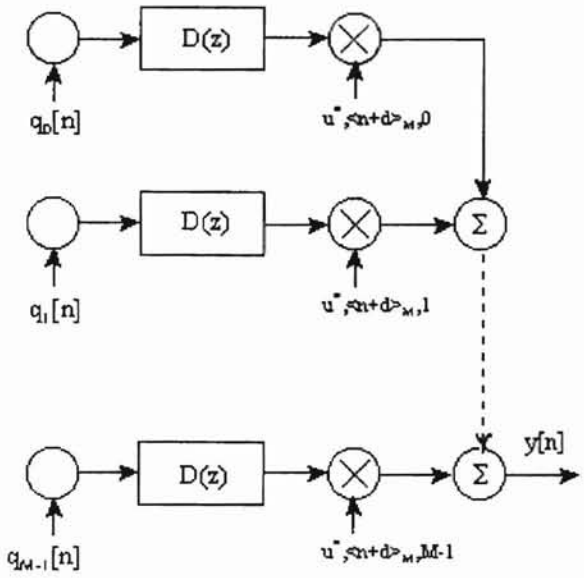

Fig 2.6 Noise Path through Parallel ΔΣ A/D Converter

Taking a look on the quantization noise path in the parallel ΔΣ A/D, in Figure 2.6, D(z) is the combination of N(z) and H(z). Assuming that the quantization is uncorrelated among all the ΔΣ A/D converters, the SNR of the system is written as [44], [46]:

$$SNR = 10 \cdot \log\left(\frac{\varepsilon(y[n]^2)}{\frac{\Delta^2}{12} \cdot d^T \cdot d}\right) \tag{2.15}$$

ε is a function of the unitary matrix, the filter used in each channel and the signal amplitude. Thus, a single channel ΔΣ A/D converter still provides an increase of L+ ½ bits for each doubling in OSR. The parallel ΔΣ A/D converter achieves an increase of

L-½ bits for each doubling the number of channels. Yet, an additional ½ bit improvement for every doubling the number of channels can be achieved by extending the dynamic range of the modulator in the parallel structure, i.e. L bit per doubling channel.

2.3.1 Time Interleaved ΔΣ ADC

The simplest unitary matrix is the identity matrix, which is used in the time-interleaved ΔΣ A/D Converter, shown in Figure 2.7. Generally, the ΔΣ modulator requirements are not relaxed because the input to each channel is sampled at 1/M the clock rate. Thus, each of the modulators operates at the full clock rate. (M is the number of channels) Hence, this architecture is sensitive to sampling clock jitter and channel mismatches. One advantage of this architecture is that each channel is identical and it simplifies the overall design. The main degradation in performance of the time-interleaved ADCs is due to sampling jitter. It is caused by the incorporation of the finite state machine which generate the sampling sequences [45]. The error power due to the sampling jitter for time-interleaved ΔΣ is:

$$\Psi = \frac{(\sigma \cdot \omega \cdot A)^2}{2 \cdot OSR} \tag{2.16}$$

where σ is the variance of time jitter with oversampling, A is the amplitude of input sine wave and ω is the input frequency of the sine-wave. From (2.16), to decrease the sampling jitter is one must increase the OSR of the system. However, increasing OSR is not always a feasible solution when constrained by the process bandwidth, hardware complexity and power consumption. A more attractive approach of using parallelism is $\Pi\Delta\Sigma$, in term of overall performance while utilizing additional area and power more efficiently.

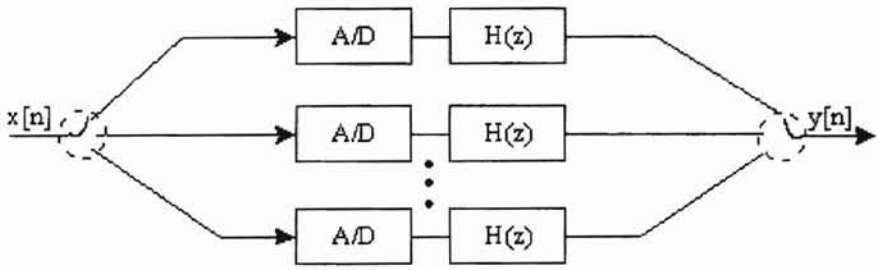

Figure 2.7 Time Interleaved $\Delta\Sigma$ A/D Converter

2.3.2 ΠΔΣ ADC

The ΠΔΣ architecture was originally presented as a Nyquist rate ADC architecture and it was extended by I. Galton *et al* [42-44] to allow for time-oversampling. In return, it provides reduced analog processing requirements and increased resolution. The architecture is identical to one shown in Figure 2.4 with the use of Hadamard sequences, as the unitary matrix, for its simplicity of circuit implementation in nature. It was reported that an M-channel ΠΔΣ ADC with oversampling f_s, has achieved a conversion performance close to that of a typical ΔΣ ADC with oversampling frequency M times f_s [47]. In other words, with the willingness to increase area, one can achieve the same resolution with lower OSR with space-oversampling. This allows the designer to trade off area for operating frequency with little change in power dissipation. This work was extensively published by I. Galton *et al* and thus covering of details is not necessary. A brief introduction of ΠΔΣ ADC is necessary because it possesses the potential of achieving higher resolution in high-performance applications with use of an existing processes which are limited by more traditional ΔΣ ADCs designs. In Figure 2.8, a primary comparison of the two main parallel ΔΣ ADCs are summarized.

Parallel Architecture	**Channel Mismatch**	**Offset**	**Sampling Jitter**	**Hardware Complexity**
Time Interleaved	High	High	High	Low
ΠΔΣ	Low	High	Medium	Low

Fig 2.8 Comparison of Two Parallel ΔΣ A/D Converters

CHAPTER 3

Modulator Design and Implementation

This chapter describes the circuit implementation of a switched-capacitor 3rd Order ΔΣ Modulator. The chosen architecture of the modulator was initially proposed by S. Nadeem and C. Sodini for a data acquisition system in kinestatic charge detection application [1]. In the first section, the architectural and system designs procedures are described. In the second section, the system building blocks are then covered with schematics and circuit analysis, the non-ideal effects are further considered as necessary. The building blocks of the modulator consist of three integrators, comparator, innovative serial feedback D/A converter, clock circuitry and level shifter. In the last section, an overall system design is re-evaluated.

3.1 Low Power Modulator Architecture

The modulator analysis is performed in the z-domain, as shown in Figure 3.1. From the transfer function of the modulator, the loop coefficients are determined. In the analysis, a stable modulator with a required signal-to-noise ratio in the baseband is the primarily parameter used to set the coefficients for the overall system design. The noise shaping of the modulator is determined by its NTF order with its placement of the poles and distributed zeros in the signal passband.

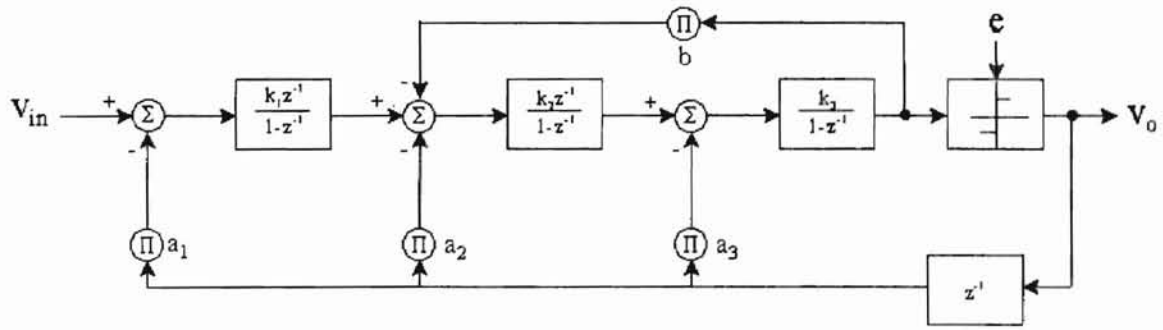

Fig 3.1 z-Domain Linear Analysis of the 3rd Order ΔΣ Modulator

To understand the system behavior, a linear approximation model of the modulator is implemented as follows, each of the integrators is replaced by its discrete time equivalence with gain k_i and the quantizer is modeled as a signal-independent

additive white noise source, e; the D/A converter is simply modeled as a delay. The output of the linear system, v_o, can be described as a combined response of both the input v_{in} and quantization noise e in (3.1).

$$v_o = H_x(z) \cdot v_{in} + H_e(z) \cdot e \tag{3.1}$$

Where $H_x(z)$, $H_e(z)$ are the signal(STF) and quantization noise(NTF) transfer functions, respectively. By writing the node equations in Figure 3.1, we may show that the output, v_o as in (3.2),

$$v_o = \frac{k1 \cdot k2 \cdot k3 \cdot z^{-2}}{\alpha} \cdot v_{in} + \frac{(1-z^{-1}) \cdot (1+(k2 \cdot k3 \cdot b - 2) \cdot z^{-1} + z^{-2})}{\alpha} \cdot e \tag{3.2}$$

where the denominator,

$$\alpha = 1 + A \cdot z^{-1} + B \cdot z^{-2} + C \cdot z^{-3} \tag{3.3}$$

and the coefficients of the polynomial α are given by:

$$A = k_2 \cdot k_3 \cdot b + k_3 \cdot a_3 - 3 \tag{3.4}$$

$$B = (k_2 \cdot k_3 \cdot (a_2 - b) - 2 \cdot k_3 \cdot a_3 + 3) \tag{3.5}$$

$$C = k_1 \cdot k_2 \cdot k_3 \cdot a_1 - k_2 \cdot k_3 \cdot a_2 + k_3 \cdot a_3 - 1 \tag{3.6}$$

From equation (3.2), the locations of the system zeros are a function of the resonator frequency which is only controlled by the integrator's feedback coefficient, b. While the system poles are determined by the coefficients a_i and b. An elliptical filter with a passband ripple of less than 0.5dB was chosen to locate the system poles and zeros in achieving the ADC specifications while maintaining the stability of the modulator loop. To insure loop stability, a heuristic approach of restricting the peak of NTF to be less than 4.5 was used, i.e. $\left|NTF(e^{j\omega t})\right| < 4.5$ [6]. Further investigation of the multibit quantization will be discussed.

By using the behavioral MATLAB® design toolbox iteratively developed here at OSU AAVDC by A. Tyagi [4], we show that with the placement of the distributed zeros in passband and elliptical poles of the modulator have achieved a signal-to-noise ratio of 99dB. In Figure 3.2, an oversampling ratio(OSR) of 64 was used for simulation with passband up to $1/128^{th}$ f_s, the signal bandwidth.

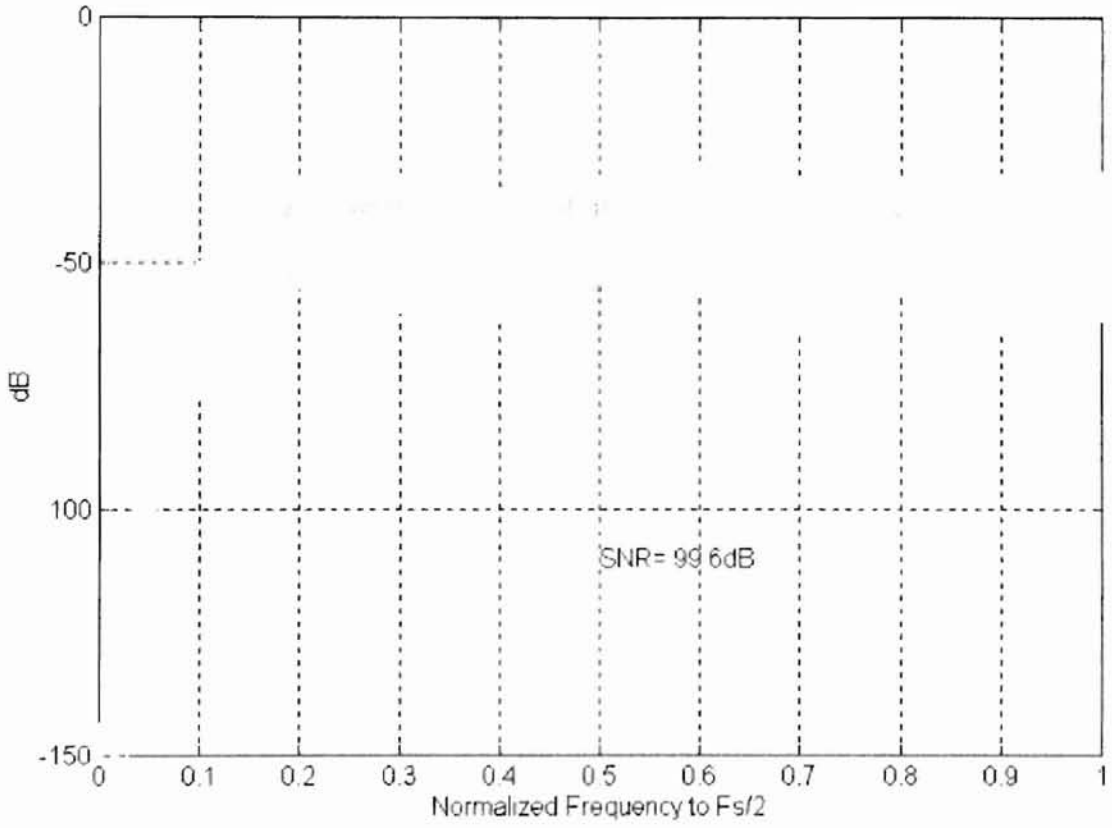

Fig 3.2 MATLAB® Simulated Output Spectrum of the Modulator

3.1.1 Coefficient Design and Dynamic Range Scaling

The loop coefficients were previously set based on the desired output spectrum for the noise shaping. In particular, when implementing an operating modulator, the voltage level on all the nodes may not have the same power level, which may introduce large noise gains from the nodes with small signal levels and result in unstable operation. Basically, the dynamic scaling is done by proportional scaling the gain of each integrator to avoid signal clipping, as well as power optimization by simulating the system. Through iterative runs for different integrator gains, the following integrator closed-loop gains were found as proper values:

$$K_1 = \frac{39}{40}; K_2 = \frac{39}{40}; K_3 = \frac{40}{40}$$

where K_i is the i^{th} integrator's closed-loop gain. The resulting outputs for each integrator and the final modulator output are respectively presented in Figure 3.2 for a couple of simulation cycles. These plots also exemplify how the interpolative $\Delta\Sigma$ modulator operates. Each consecutive integrator attempts to interpolate between its input waveform's values corresponding to the adjacent digital quantization steps in an analog fashion. This process coupled with oversampling consequently produces a quantizer output that interpolates between adjacent quantization levels. Thus, the modulator's output provides a more precise estimation of the modulator's input waveform. Note that

it is necessary to insure that, through the design process, there is no integrator clipping in the loop.

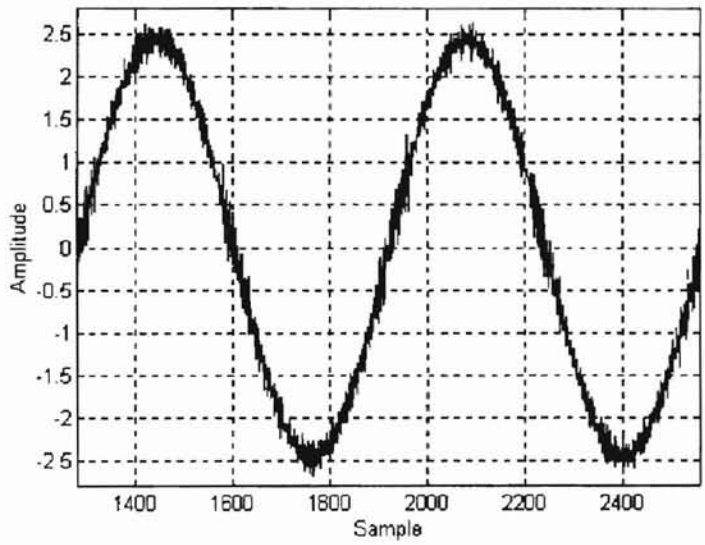

Figure 3.3(a) Output of 1st Integrator with 1V, 2 kHz Sine Modulator Input at f_s=1.28 MSPS and M=64.

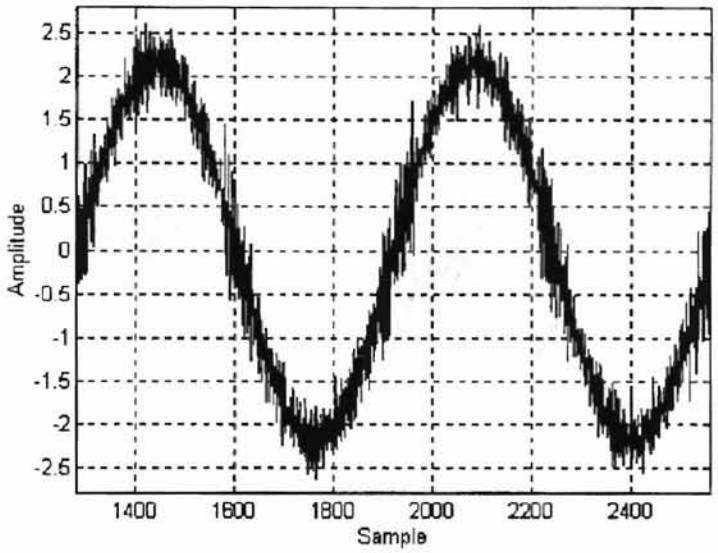

Figure 3.3(b) Output of 2nd Integrator with 1V, 2 kHz Sine Modulator Input at f_s=1.28 MSPS and M=64.

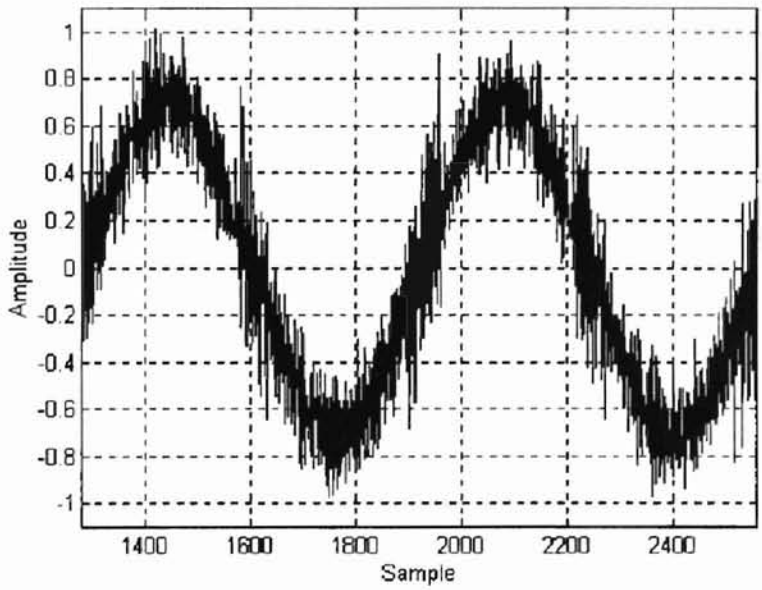

Figure 3.3(c) Output of 3rd Integrator of Interpolative ΣΔ Modulator with 1V., 2 kHz Sine Modulator Input at f_s=1.28 MSPS and M=64.

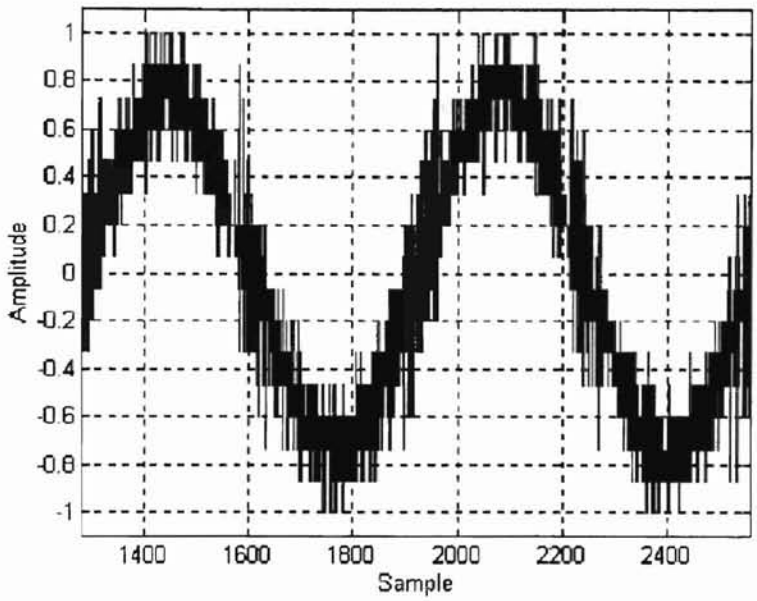

Figure 3.3(d) Output of Interpolative ΣΔ Modulator with 1V., 2 kHz Sine Modulator Input at f_s=1.28 MSPS and M=64.

3.1.2 Multibit Oversampling Converter Design

In order to increase the dynamic range (DR) and reduce the idle tones, a typical 1-bit quantizer in the ΔΣ modulator is usually replaced by a multibit quantizer. According to (3.7), an increase of 6 dB per additional quantizer bit is achievable for overall DR of ADC after decimation.

$$\Delta DR = 20 \cdot \log(2^N - 1) \text{ dB} \tag{3.7}$$

Where N is the resolution of the multibit quantizer. While modulators based on multibit quantization are tolerant of non-linearity in the quantizer because of the noise shaping, they do impose stringent linearity requirements on the D/A converter. The DAC non-linearity error thus enters the modulator as its input. Therefore, the modulator's resolution and linearity are limited by the D/A converter [10].

For higher order converters with a single bit quantizer, it has been shown [5] that $\left|NTF(e^{j\omega t})\right| < 2$ is necessary to insure stability. In practical application, $\left|NTF(e^{j\omega t})\right| < 1.5$ is usually used to provide a reasonable input range of about 80% of the range of the quantizer. The corresponding corner frequency of the noise transfer function, $NTF(e^{j\omega t})$ or $H_e(e^{j\omega t})$ is $0.06f_s$. It was also shown that as the number of the quantization levels is increased, the maximum allowable gain $\left|NTF(e^{j\omega t})\right|_{\max}$ is also increased as well [6]. In our case, for an input range set at 80% of the range of the quantizer, $\left|NTF(e^{j\omega t})\right|_{\max}$ can be set at 5.0 with a 4-bit quantizer, where the corresponding corner frequency is found to be $0.19f_s$.

The increase in corner frequencies corresponding to the increase in the maximum gain has the following effects. With the assumption of $f_c >> f_0$, the noise in the baseband falls well within 18dB/octave slope of a third-order filter transfer function. Taking into account both the increased gain and corner frequency of $H_e(z)$, implies that quantization

noise in the baseband is suppressed by an additional 24 dB for a converter with a 4-bit quantizer compared to one with a single bit quantizer. Therefore, the total reduction of the quantization noise in the baseband is approximately (4-1)bit * 6dB/bit + 24dB or 42dB.

3.1.3 Power Consumption of the Modulator

The power consumption of the modulator, as a function of signal baseband and resolution, is the primary factor behind this selected architecture. A simple model [1] is used to determine and minimize the power dissipation of the modulator while meeting the specifications.

For a given baseband, the signal-to-noise ratio can be calculated as a function of the clock frequency and the order of the modulator. The clock frequency of the ADC system further determines the settling requirement on the integrators which is a measure of the power consumption, provided the amplifier topology and mode of operation are known. The minimum current requirement in the integrator is a function of linear (or nearly) settling and slewing requirement. This is the dominant power contributor for integrators. Depending on the operating frequency and OTA devices, the power dissipation may be dominated by the switching logic or integrators as will be shown later.

To model the slewing requirements of the OTA, it is assumed the maximum output swing of the integrator is at five-sixth of the supply voltage, V_{supply}, but when m-bit quantizer is utilized, the required slew rate is reduced by 2^{m-1}. The maximum slewing time to be one-quarter of the clock period, t_s. Hence, the output current can be represented as follow,

$$I_{out} = SR \cdot C_L = \frac{\Delta v}{\Delta t} \cdot C_L = \frac{\frac{5}{6} \cdot V_{sup} \cdot C_L}{2^{m-1} \cdot \frac{1}{4} \cdot t_s} \approx \frac{3.3 \cdot C_L \cdot V_{sup}}{2^{m-1} \cdot t_s} \tag{3.8}$$

Equation (3.8) provides the upper limit on the bias current required in the output leg of a class A (or AB with small difference) amplifier to meet the slewing requirements with capacitive load C_L [38]. The sampling and integrating capacitors, C_s and C_I of the amplifier in the switched-capacitor approach with feedback, the feedback gain η can be found as

$$\eta = \frac{C_I + C_s}{C_I} \neq 1 \tag{3.9}$$

The fact that the feedback gain is not unity, reduces the effective settling bandwidth of the amplifier [38]. For the amplifier with its differential pair operating in saturation, the transconductance,

$$g_m = \frac{I_{TAIL}}{\Delta v} \tag{3.10}$$

where the overdrive voltage Δv is defined as V_{gs}-V_T, and I_{TAIL} is the tail current of the differential pair. Thus I_{TAIL} can be expressed as

$$I_{TAIL} = \frac{20 \cdot C_L \cdot f_s \cdot \eta \cdot \Delta v}{2^{m-1}} \tag{3.11}$$

where the sampling frequency f_s is defined as $1/t_s$; with the assumption of five time constants within one-quarter of the clock period to settle.

From (3.8) and (3.11) for I_{out} and I_{TAIL} requirements, we observe that the linear settling component is greater than the slewing criteria. We must then use the maximum current requirement dictated by the linear settling criteria to model the current of the integrator. In this case, class A and AB have the same constraints [5]. The total current in the amplifier can be then represented as αI_{TAIL}, where α is a function of the topology of the amplifier. For a third order modulator with three integrators in the loop, the total modulator power can be given by:

$$P_{\text{mod } 3} = \frac{60 \cdot \eta \cdot C_L \cdot f_s \cdot \alpha \cdot \Delta v \cdot V_{\text{sup}}}{2^{m-1}} \tag{3.12}$$

To suppress the thermal noise and maintain the signal-to-noise ratio of the ADC system, the required load capacitance has a minimum value of:

$$C_L = 10^{SNR/10} \cdot k \cdot T \cdot \frac{2 \cdot f}{f_s} \tag{3.13}$$

with the assumption of a full scale input signal of 1V with signal bandwidth f.

Substitute (3.13) into (3.12),

$$P_{\text{mod}3} = \frac{120 \cdot \eta \cdot 10^{SNR/10} \cdot k \cdot T \cdot f \cdot \alpha \cdot \Delta v \cdot V_{\text{sup}}}{2^{m-1}} \tag{3.14}$$

This provides us a fundamental limit on the third order modulator power dissipation as function of baseband (f), the resolution (SNR) and the power supply voltage (V_{sup}). Note that the power consumption of the switch-capacitor networks of the three integrators is insignificant, or nearly an order of magnitude lower when the integrators are operating in the saturation mode. As we will see later, for amplifiers operated in subthreshold, this is not necessary true.

So far, we have assumed that all the integrators in the loop are identical, yet to optimize the power consumption, the second and higher stages do not have to use the capacitor value dictated by the thermal noise floor. The loop coefficients of a higher order loop are determined by the ratio of the sampling to integrating capacitors and it place a lower limit on the integrating capacitors. If the second and higher stages use minimum capacitor values, the model can be easily modified and is given by:

$$P_{\text{mod}3} = \frac{40}{2^{m-1}} \cdot V_{\text{sup}} \cdot \alpha \cdot \eta (10^{SNR/10} \cdot k \cdot T \cdot f \cdot \Delta v + C_{\text{min}} \cdot f_s \cdot (N-1)) \tag{3.15a}$$

where the order of the modulator N is generalized.

Using (3.13), we may deduce the power consumed by the networks, P_{sw} in (3.15b), to illustrate its contributing factor to the power consumption of the modulator.

$$P_{sw} \approx 4 \cdot k \cdot T \cdot 10^{\frac{SNR}{10}} \cdot V^2 \cdot f + 2 \cdot (N-1) \cdot C_{\min} \cdot V^2 \cdot f_s \qquad (3.15b)$$

Conversely, for integrators operating in the subthreshold mode, the transconductance is $\frac{I_{TAIL}}{v_{thermal}}$, by replacing Δv in (3.10) with $v_{thermal}$, the slew rate requirement in (3.8) has now become the dominant factor in determining the power consumption of the amplifiers. Thus, the minimum current requirement is dictated by the slew rate process, as opposed to its linear settling counterpart as shown above. This is the opposite scenario to integrators operated in the saturation mode. More importantly however, the power consumption of the switch-capacitor networks is no longer negligible. The total power consumption of the modulator is thus the sum of both the integrators and the switched-capacitor networks. Reforming (3.15a) for the case of subthreshold operation, yields

$$P_{\mathrm{mod}\,3(sub)} = \frac{4}{2^{m-1}} \cdot V_{\sup}^2 \cdot f_s \cdot \left(\frac{10^{SNR/10} \cdot k \cdot T}{OSR} + C_{\min} \cdot (N-1)\right) + P_{sw} \qquad (3.15c)$$

3.1.4 Properties of the Modulator and Its Building Blocks

Figure 3.4, shows the switched-capacitor implementation of the third order single loop analog modulator. This is the single loop modulator architecture with distributed feedback where the output of the 4-bit quantizer is fed back to the input of each of the three integrators in the loop through the use of a parallel-to-serial D/A converter. The loop coefficients a_1 and b determine the pole location, as discussed previously. The coefficient b determines the complex zero pair location in the baseband, with one real zero at DC. This architecture does not require an active summing node at the input and has also been referred to as the 'cascade of resonators structure' [20]. The feedback around the second and the third integrator forms the resonator structure where the complex transmission zeros in the quantization transfer function can be designed by selecting the correct resonator frequency. This topology has superior high frequency settling properties because the integrators and resonators are connected without the delay-free loops and the worst case settling happens when two amplifiers settle in series [1]. Thus, the errors resulting from this worst case settling only disturb the relative positioning of the noise shaping transmission zeros for which the architecture is shown insensitive over a wide range [23]. The distributed nature of the quantized feedback improves the stability characteristics of the loop even more with the three additional bits of the quantizer, and as a result it is more stable. This architecture will be further investigated through measurements, and thus multiple reset switches were included for studies when implementing the system on silicon.

In the modulator, the same amplifier was used for all three of integrators for design simplicity. Although the second and third stages do not have the same stringent requirement on slew rate and gain requirement as the first stage, having the same amplifier design help shortening the design phase considerably. In addition, this choice has negligible effect on power consumption as confirmed by the analysis in previous section.

Due to the oxide thickness of the process, an analog floating gate memory reference is not suitable for implementation for the comparators [21], instead a resistor reference string was selected. Although this has increased the power consumption, the resolution, speed and function of the ADC system is more of a concern at this preliminary stage of design. The actual power dissipation of the reference can be easily extracted from the measurement if necessary.

The serial feedback DAC is a novel addition to the $\Delta\Sigma$ modulator and it is a full digital design. The serial DAC was easily implemented with care for its linearity performance. The DAC output is then used as control logic to steer the reference currents to achieve negative feedback to each of the integrators in the loop. Since the DAC is clocked at 16 or 2^4 times faster than the integrators, additional hardware was added to achieve both a fast and slow non-overlapping clock phases. The advantage is that the oversampling frequency for this design is much lower compared to a comparable existing single-bit design while the additional hardware and added power to drive the DAC is also minimal. This robust serial DAC approach is particularly valuable for higher

performance ΔΣ ADC since the analog integrators always run slower than the digital logic. Making use of the excess bandwidth, that is the under-utilized bandwidth in excess of the integrator and less than that of the process limit. To implement a serial multibit modulator design is thus an excellent choice for improving the DR of the ADC with low power demands. On the other hand, the associated switched-current references of the serial DAC was also selected to eliminate the need for linear dual poly capacitors in order to implement the system on a single poly process.

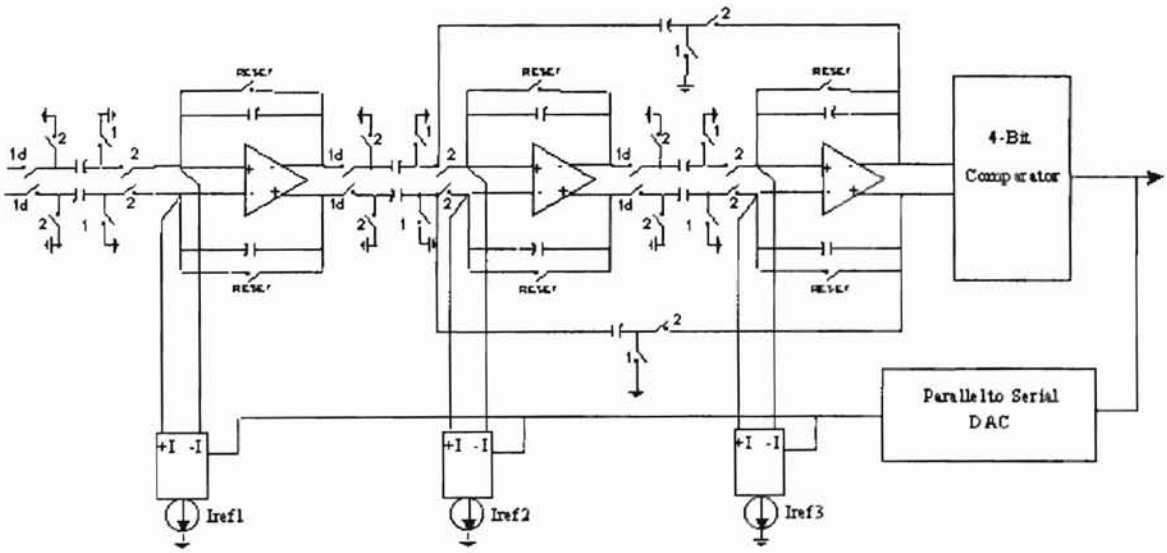

Fig 3.4 Switched-Capacitor Implementation of a 3rd Order ΔΣ Modulator

3.2 Integrator

The OTA is the most critical building block in the ΔΣ modulator. Incomplete settling of the integrator outputs is considered a gain error if the settling process is linear and thus the settling speed of OTA sets the maximum oversampling frequency of the ADC system [11], even if a complete settling is not required [12]. Note that slew rate limiting of the integrator, in any case, is non-linear behavior and must be avoided. From simulation, the outputs of the integrators are allowed to settle within one quarter of the clock cycle and thus four to five time constant of settling time are needed in this application. However, it can be shown that for an integrator with lower bandwidth than the sampling rate, and with correspondingly inaccurate settling will not impair the ΔΣ modulator performance, provided that the settling process is linear [11].

3.2.1 Operational Transconductance Amplifier Design

A fully differential architecture was used. Since the switched capacitor circuits are true sampling devices, small amounts of high frequency noise coupled through the power supplies or any data path will fold down in the baseband and cause distortion. Thus, the switches are sized to meet the requirement of 16-bit settling in one-quarter the clock period, i.e. the RC bandwidth of switch-capacitor networks. Moreover, all the odd harmonic distortions are eliminated, as the DC to DC transfer characteristics of a fully differential OTA is inherently symmetrical [3]. To increase the signal swing and power

supply rejection while reducing the clock feedthrough, a fully differential folded-cascode OTA design is again encouraged for the integrator as the need for relative fast settling with modest gain requirement to suppress the quantization leakage error and harmonic distortion, as compared to two-stage amplifier. The common mode voltage level is maintained in the fully differential circuit by using a common mode feedback circuit using a switched capacitor approach.

The chosen opamp topology is shown in Fig. 3.5. The fully differential input signal is applied to the input differential pair which operates in weak inversion. Instead of saturation region, a weak inversion was chosen for the differential pair due to the lower power consumption and higher gain available in weak inversion. To further illustrate, we may compare the transconductance to drain current ratio in both active and subthreshold for gain and power efficiency; In saturation, g_m is proportional to the square root of the applied drain current, while in weak inversion, it is directly proportional to its drain current to its first order. Hence, a smaller current is more efficiently utilized in weak inversion for higher transconductance and high gain as long as the bandwidth requirements can be achieved and offset tolerated. Moreover, speed is not a critical issue in our application, operating in weak inversion is thus a better choice for low power design. On the other hand, from behavioral simulation of the modulator, a reasonable gain of ($\approx$4000) is required to achieve good power supply, common mode rejection and linearity for the amplifier, a pair of cascode devices is used to further boost up the differential voltage gain. OTA current biasing was set by the square law operated transistors while all the other transistors were operated in subthreshold.

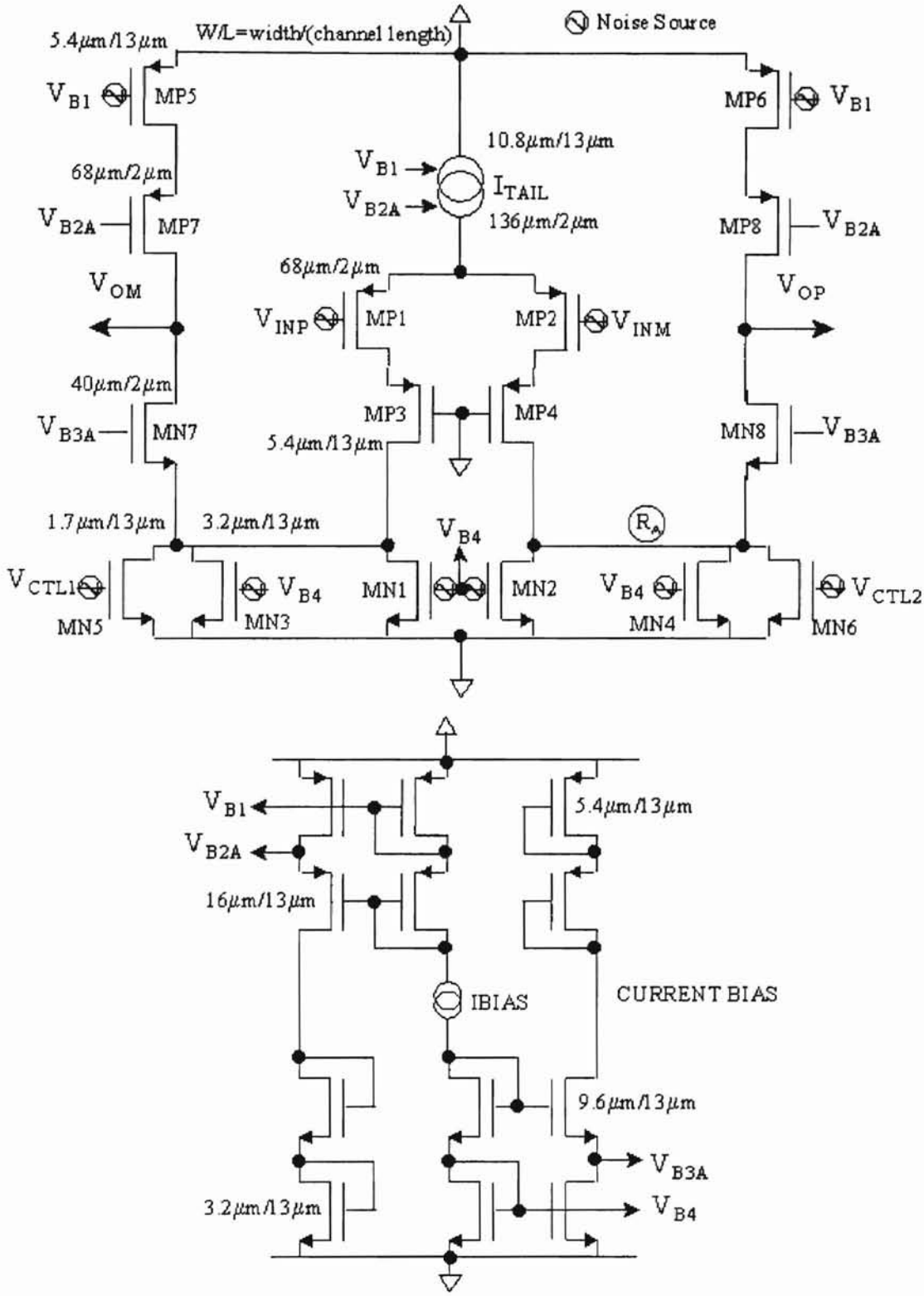

Fig 3.5 Folded Cascode OTA with Noise Sources

3.2.2 Noise Performance

Noise imposes a fundamental limitation for the performance of the CMOS amplifier, hence it is important to analyze the causes of noise and employ possible measure that can reduce it. In this amplifier circuit, each of the transistors have been modeled using an equivalent voltage noise source, $\widetilde{v}^2(f)$, as presented in Fig 3.5, with the assumption that all noise sources are statistically uncorrelated. In this analysis, we further assume that all the necessary transistors are matched. Note that, the noise source of the cascoded tail current is essentially a common mode signal and thus suppressed by the CMRR of the amplifier; it is therefore omitted in the analysis. Also, the cascoded transistors of the amplifier which consist of transistors MN7, MN8, MP7, MP8, MP3 and MP4 usually do not affect the total equivalent input-referred noise voltage and hence they will fall out in the final analysis. As a result, the input-referred noise voltage is mainly caused by the input differential pair and current sources of the amplifier. Since these noise sources are uncorrelated, the current mean-squared noise value at output node, can be represented as

$$\widetilde{i}_o^{\,2}(f) \approx \widetilde{v}_{p2}^{\,2}(f) \cdot g_{mp2}^{\,2} + \widetilde{v}_{p6}^{\,2}(f) \cdot g_{mp6}^{\,2} + \widetilde{v}_{ns}^{\,2}(f) \cdot g_{mns}^{\,2} \tag{3.16}$$

$$\text{where } \widetilde{v}_{ns}^{\,2}(f) \cdot g_{mns}^{\,2} = \sum_{i=2,4,6} (\widetilde{v}_{ni}(f) \cdot g_{mni})^2 \tag{3.17}$$

Equivalently, $\widetilde{v}_{ns}^{\,2}(f)$ is the noise term of collapsed current sources MN2, MN4 and MN6.

Since the effective transconductance of the OTA is $g_{mOTA} \approx g_{mp2}$ (3.18)

Dividing (3.16) by the OTA transconductance g_{mOTA} , the output noise can be related back to an equivalent input-referred noise value which results is expressed as:

$$\tilde{v}_{in}^{\,2}(f) = \frac{\tilde{i}_o^{\,2}(f)}{g_{mOTA}^{\,2}} \tag{3.19}$$

For OTA with differential pair operating in subthreshold,

$$g_{mOTA} \approx {I_{gmOTA}}/{v_{thermal}} \tag{3.20}$$

Thus, the equivalent input-referred noise is,

$$\tilde{v}_{in}^{\,2}(f) \approx \tilde{v}_{p2}^{\,2}(f) + \tilde{v}_{p6}^{\,2}(f) \cdot (\frac{g_{mp6}}{g_{mOTA}})^2 + \tilde{v}_{ns}^{\,2}(f) \cdot (\frac{g_{mns}}{g_{mOTA}})^2 \tag{3.21}$$

We thus realize that, from (3.21), MP1-MP2, MP5 and MP6 are the primary dominant noise sources as well as the current sources MN1-MN6 which also degrade the performance of the amplifier. Also note that the last two terms are much larger than that of MP1 and MP2. Before further pursuing the analysis, we need a model for both noise generators for the MOS devices.

For the MOS transistor, the thermal noise source can be modeled as [5] and its spectral density is represented,

$$\tilde{v}_{th}^{\,2}(f) = 4 \cdot (\frac{2}{3}) \cdot k \cdot T \cdot \frac{1}{g_m} \tag{3.22}$$

where k is Boltzmann's constant with a value of $1.38 \cdot 10^{-23}$ JK^{-1} , T is the absolute temperature in Kelvins and g_m is the transconductance of a MOS transistor operating in active region. From (3.22), the thermal noise is reduced by increasing the transconductance of the device or minimizing the operating low temperature.

The effect of 1/f or flicker noise of the MOS transistor, which normally dominates at the low frequency, can be modeled as [5],

$$\tilde{v}_f^{\,2}(f) = \frac{K^2}{W \cdot L \cdot C_{ox} \cdot f} \tag{3.23}$$

where the constant K is dependent on device characteristics and can vary widely for different devices in the same process. The variables W, L and C_{ox} represent the device's width, length and gate capacitance per unit area, respectively. From (3.23), we observe the device's area WL and $1/t_{ox}$ are inversely proportional to 1/f noise.

After reviewing both the thermal and flicker noises, we possess the knowledge to design each transistor in the amplifier to achieve the desired performance while bearing in mind their noise contribution, which could significantly limit the

resolution of the amplifier in reality. For the purpose of hand analysis and to ease the process of design, we only look at the contributing terms without actually calculating its values, primarily due to the lack of hard data for the selected process. Precaution should be taken to make sure such that the total equivalent noise should be at least 9dB below the SNR of the ADC system [8].

Deriving from (3.21) and (3.22), the input-referred noise, $\overline{v}_{in}^{\,2}(f)$, based on thermal noise terms, is proportional to the following factors:

$$\overline{v}_{in}^{\,2}(f) \propto \frac{T^2}{I_{dsp2}} \qquad of \qquad MP1\ \&\ MP2(subthreshold)$$

$$\overline{v}_{in}^{\,2}(f) \propto \frac{T^4 \cdot I_{ns} \cdot (W/L)_{ns}}{I_{dsp2}^{\,3}} = \frac{T^4 \cdot (W/L)_{ns}}{I^2} \qquad of \qquad MN1 - MN6(sq.Law)$$

$$\overline{v}_{in}^{\,2}(f) \propto \frac{T^4 \cdot I_{dsp6} \cdot (W/L)_{p6}}{I_{dsp2}^{\,3}} = \frac{T^4 \cdot (W/L)_{p6}}{I^2} \qquad of \qquad MP5\ \&\ MP6(sq.Law)$$

(3.24)

From (3.24), we may further draw a few observations for reducing thermal noise for this amplifier:

(1) Transistors MP1 and MP2, which are the input differential pair, should be made as large as possible or increase its transconductance g_m to suppress the noise.

(2) The larger geometry of transistor MN1-MN6 and MP5, MP6 have significant effect on the noise. Also, the noise is directly proportional to T^4 and thus this OTA is not suitable for operating in higher temperature range.

Turning to the effect of flicker noise, by substituting (3.23) into (3.21), the input-referred voltage of the flicker noise, $\widetilde{v}_{in}^{\,2}(f)$, is proportional to the following factors:

$$\widetilde{v}_{in}^{\,2}(f) \propto \frac{K_{p2}}{(W \cdot L)_{p2}}$$

$$\widetilde{v}_{in}^{\,2}(f) \propto \frac{K_{ns}}{(W \cdot L)_{ns}} \cdot \frac{(\frac{W}{L})_{ns} \cdot T^2}{I} = \frac{K_{ns} \cdot T^2}{L_{ns}^2 \cdot I} \tag{3.25}$$

$$\widetilde{v}_{in}^{\,2}(f) \propto \frac{K_{p6}}{(W \cdot L)_{p6}} \cdot \frac{(\frac{W}{L})_{p6} \cdot T^2}{I} = \frac{K_{p6} \cdot T^2}{L_{p6}^2 \cdot I}$$

With (3.25), in order to reduce 1/f noise, it suggests the use of longer channel length devices is highly desirable while not restricting the bandwidth of the OTA. Also, operating at higher current is helpful for decreasing the effect of flicker noise.

Since this OTA is used as switched-capacitor integrator in the modulator, the capacitor of the first stage integrator sets the noise floor of the ADC system, ($\widetilde{v}_{ADC}^{\,2} = \frac{k \cdot T}{OSR \cdot C}$) and thus the total input-referred noise of the OTA should be designed to be lower than the noise floor of the ΔΣADC by at least 9 dB [8]. If a higher dynamic range (>100 dB) is of design specification, special noise reduction techniques should be employed [39].

3.2.3 Dynamic Common Mode Feedback

The main drawback of a fully differential approach of the OTA is the need for CMFB circuit. The function of the common mode feedback (CMFB) circuit is to set and control the output common mode voltage and to control it to be at some desired voltage. The applied negative feedback of the OTA determines the differential signals does not affect the common mode voltage, and thus it is free to swing up and down. Besides requiring additional power and area, the CMFB circuit limits the output swing, increases noise and reduces the bandwidth of the OTA. Typically, the CMFB is used to control the current sources in the output stage to establish the common mode output level of the OTA. In the consideration of larger output signal swing, a switched capacitor CMFB is realized instead of a continuous time approach. The design was initially proposed by R. Castello and P. Gray in Fig 3.6 [38] is particularly suited for low-voltage and low-power applications. The reasons are two folds; This CMFB design requires very little additional power consumption, with the exception of the replica circuit that defines the proper value of V_{CNTL}, which can be shared by the OTA. Second, this additional circuit does not degrade the differential output swing since the level shift operation performed by the capacitors C_{1A} and C_{2A} is not limited by the supplied voltages. Although this CMFB circuit can supply large currents for a positive signal, a negative signal is limited to 2I, by the tail current. This can cause a slow negative common mode output transient, however by choosing appropriate device sizes, such that the p-type current-mirrors are faster than the n-type current-mirror with all common mode output transients are thus guaranteed to be at its positive polarity. Hence, the CMFB is insured to work at its maximum speed.

In Figure 3.6, the capacitors C_{1A} and C_{2A} are used to generate the average of the output voltages, which is used to create the control voltage for the OTA output current sources . The voltage across the capacitors C_{1A} and C_{2A} is determined by the capacitors C_{1B} and C_{2B}, during phase Φ_1 and hence establish the desired common mode output voltage periodically. Note that the capacitors C_{1B} and C_{2B} are switched in on the phase opposite that of associated with the input signal sampling. C_{1B} and C_{2B} are generally sized one-quarter to one-tenth the sizes of C_{1A} and C_{2A}, with the consideration of avoiding charge injection errors and not overloading the amplifier.

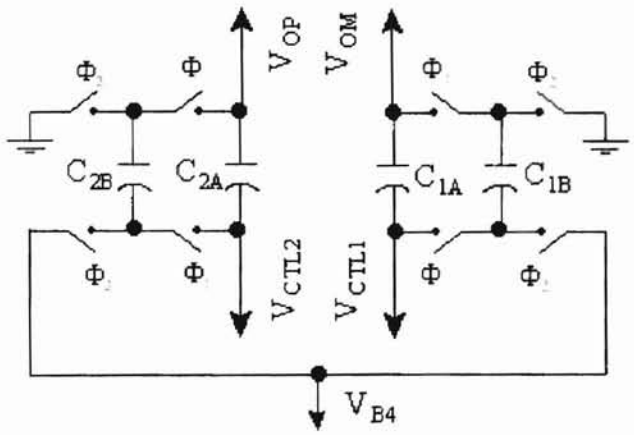

Fig 3.6 Switched-Capacitor Common Mode Feedback Circuit

The simulation of the OTA was done using SOISPICE 4.41 [17]. In Figure 3.7, an equivalent load capacitance of 30pF was used for the OTA in unity gain feedback configuration for its frequency response simulation, the –3dB exists at 210KHz with a phase margin of 115 degree, with a DC open-loop gain of 6000.

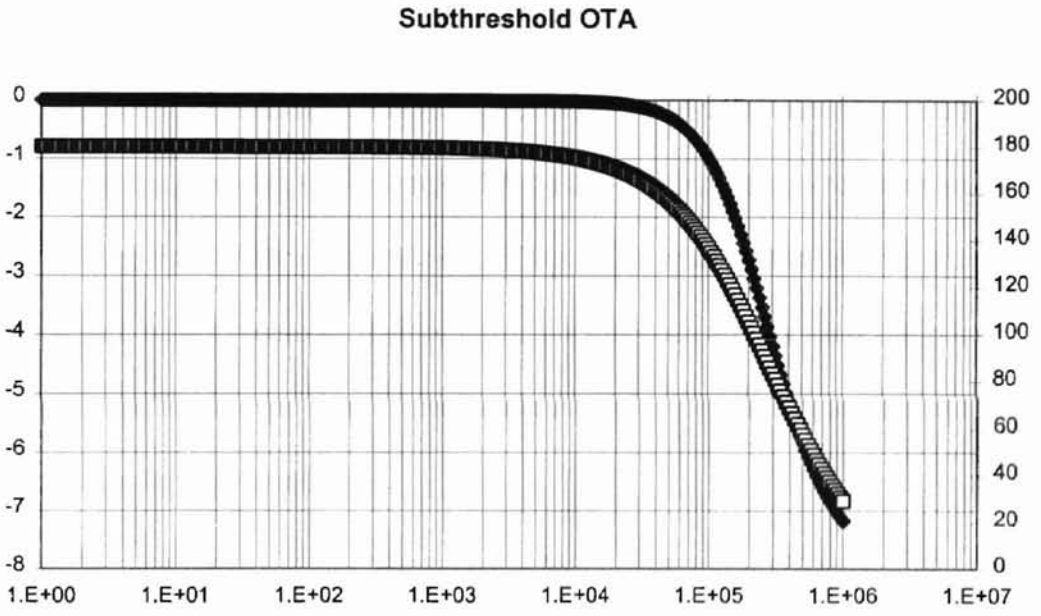

Fig 3.7 OTA Frequency Response; lower curve is the voltage gain in dB and the upper curve is the phase response in degree.

3.3 Quantizer

This comparator has a stage of preamplification followed by a track-and latch stage, shown in Figure 3.8. The preamplifier is used to obtain higher resolution and minimize the effects of kickback (charge transfer from the track-and-latch stage as it goes from the track mode to latch mode, resulting in glitches). A track-and-latched stage is used to amplify the preamplifier output signal and drive the subsequent digital logic circuitry. Note that the preamplifier is designed for some low gain of 4 to 10, otherwise the resulting large time constant will limit the speed of the comparator in the track mode. In the latch mode, the positive feedback of the track-and-latch stage regenerates the sampled analog signal into a full scale digital signal, as a result it minimizes the total number of gain stages required. This architecture has been widely used and proven in higher speed application for its reliability and simplicity [5]. The time constant in the latch phase can be also found as :

$$\tau_{latch} \approx K \cdot \tau_{inv} \cdot \ln(\frac{\Delta V_{\log ic}}{\Delta V_{IC}}) \tag{3.26}$$

Where K is the loading factor and τ_{inv} is the stage delay of a self-loaded inverter; ΔV_{logic} is the desired digital logic voltage; ΔV_{IC} is the initial voltage difference at the beginning of the latch phase, defined as $A_v \cdot \frac{V_{FS}}{2^m}$ where m is the number of bits of the quantizer.

The schematics of the preamplifier are presented in Figure 3.9, note that the DC gain is $\frac{g_{mN1}}{g_{mN3}}$, or the transconductance ratio of the transistor MN1 to MN3. The gain is easily set (4 to 10) with a small compromised in bandwidth, allowing fast settling to be maintained. The common mode voltage level is set by transistors MP1 and MP2 during resetting of the preamplifier stage. The simulation results of the comparator can be found in Figure 3.10 for the frequency response of the preamplifier stage and the transient response of the comparator is followed in Figure 3.11.

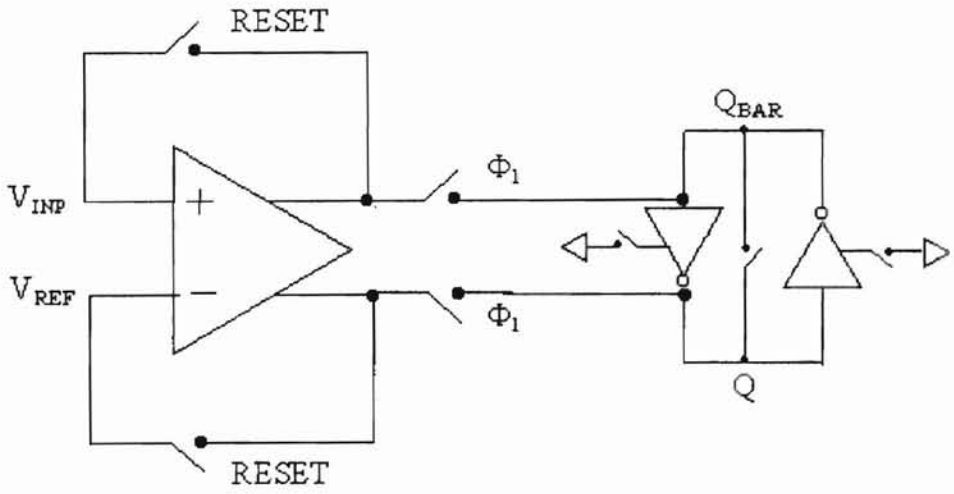

Fig 3.8 System Level Latched Comparator

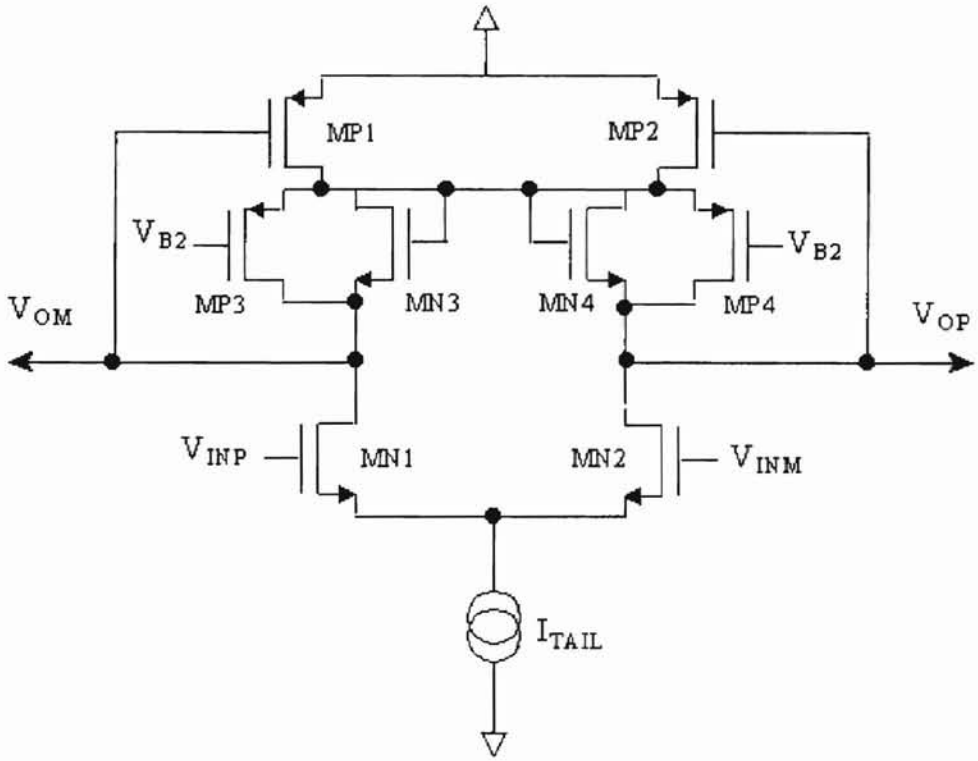

Fig 3.9 Preamplifier Stage of the Comparator

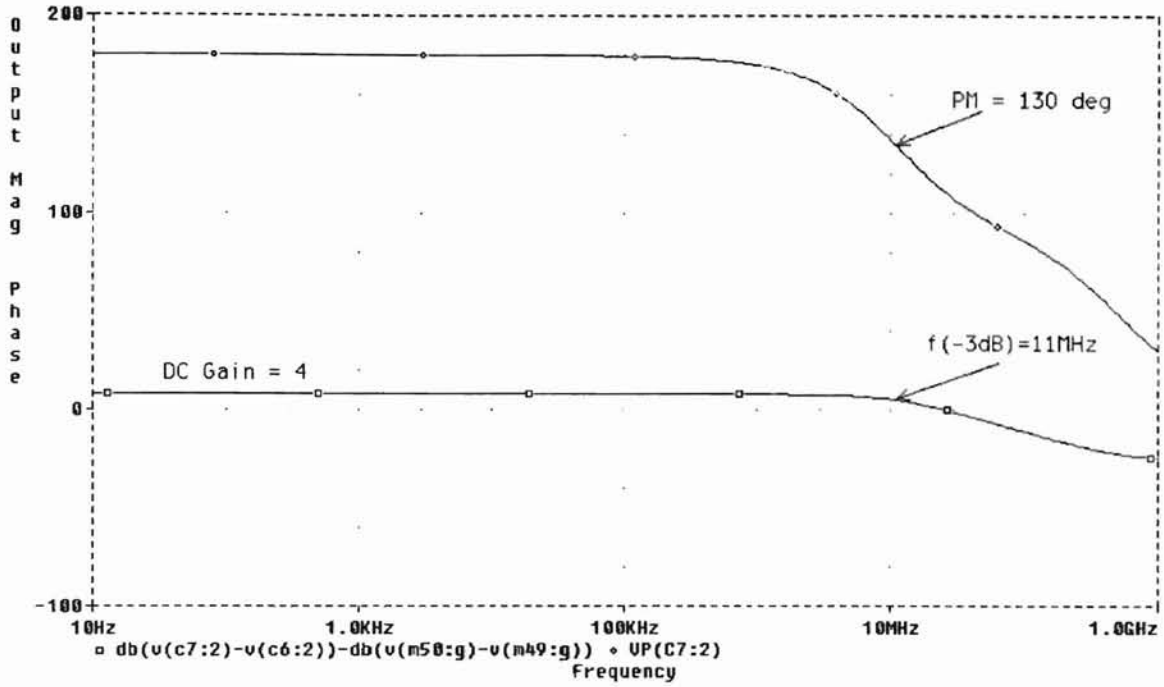

Fig 3.10 Frequency Response of the Preamplifier

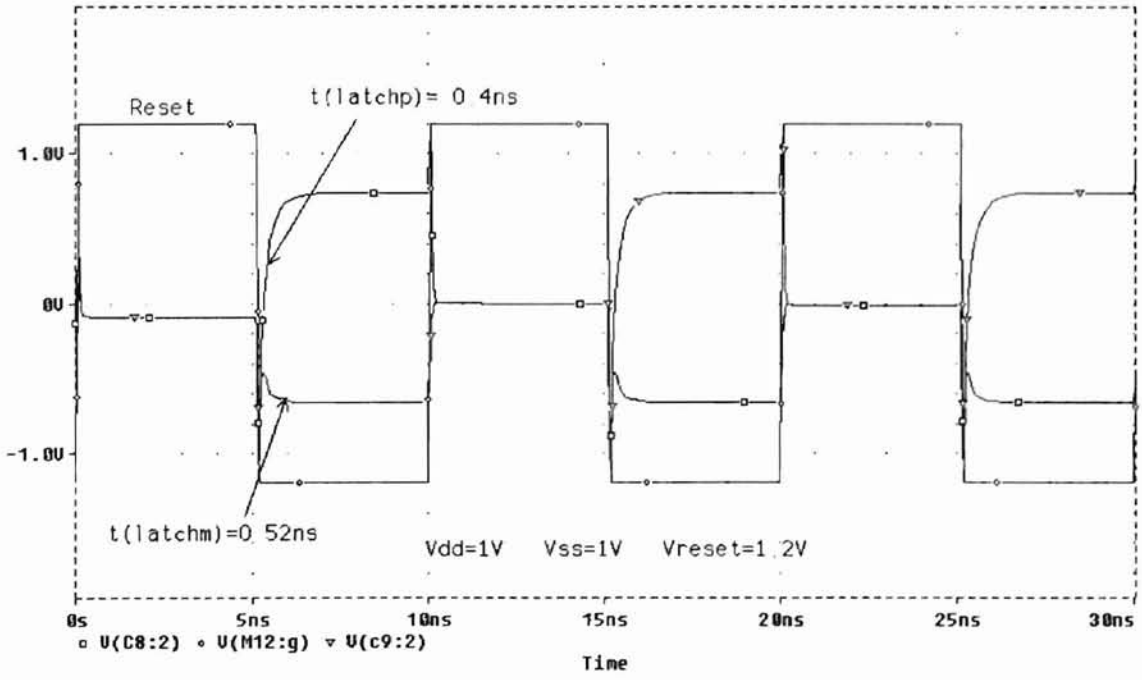

Fig 3.11 Transient Plot of the Comparator

3.4 Current Metered DAC

The output of the quantizer (encoder is not shown) is presented as a binary input to the decimation filter and the internal DAC is shown in Figure 3.12b. The DAC consists of a parallel-to-serial register, combinational logic and three switched current references. The serial output is clocked out by the DAC's clock (2^4 x f_s) at the start of the sampling phase. While the DAC output is high, I_{ref} is integrated onto each of the hold capacitors of the integrators, where the on time of the reference current is proportional to the quantizer output serially processed by the DAC. The equivalent voltage output of DAC can be expressed as follow:

$$V_{dac} = \frac{I_{ref} \cdot T}{C_H} \sum \frac{CNT_Q}{2^m - 1} \tag{3.27a}$$

Where CNT_Q is the number of 1's in thermometer code of the m bit quantizer and C_H is the hold capacitor of integrator; I_{ref} is the scaled reference current source which sets the feedback coefficient a_1 in (3.2) to (3.6). T is the on time of a DAC clock pulse.

From (3.27a), the accuracy of the DAC is thus a function of the clock resolution, which includes the rise time, fall time and jitter associated with the matching of the capacitors and the reference currents to each summing node. This particular DAC is charge-based and monotonic by design [8]; the analog output signal is directly proportional to the number of counts in the thermometer code from the quantizer.

In other words, the output of DAC is directly proportional to the number of digital inputs, hence monotonicity is guaranteed for the DAC. From simulation, Figure 3.12a, it is observed that the DAC is inherently monotonic. By definition, it will be better than ±½ LSB of the ADC if the DAC is allowed to fully settled and jitter is properly managed. From the worse case simulation, a low gain 30dB OTA was used for the integrator while the DAC was clocked at a relative high frequency of 50MHz, while output full settling was achieved.

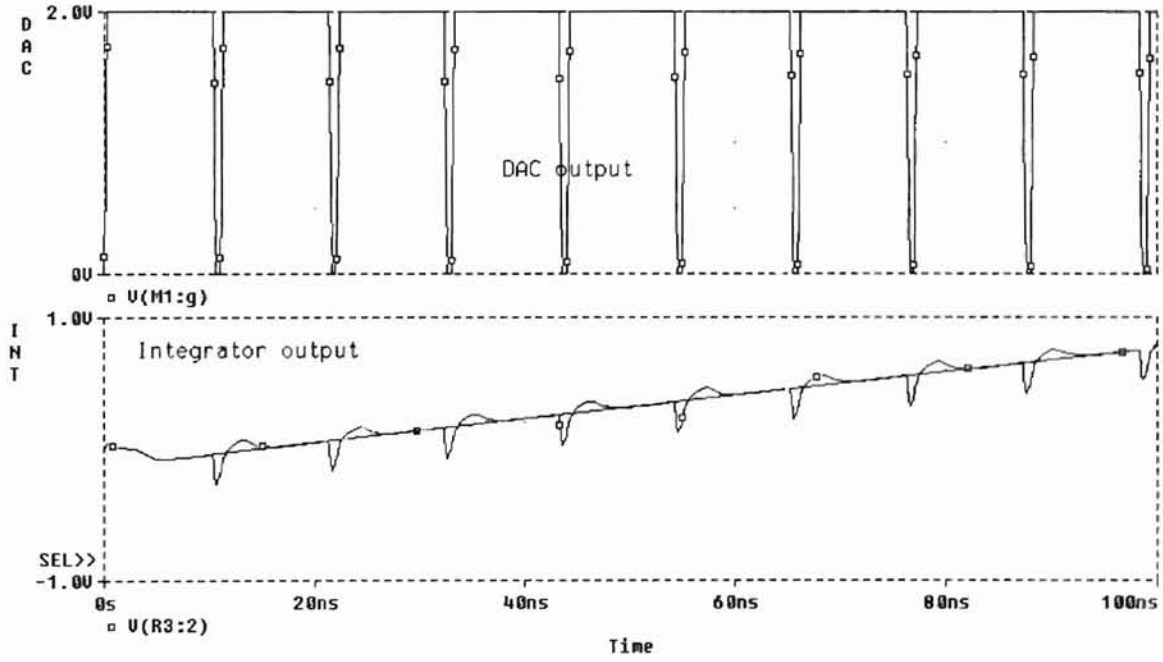

Fig 3.12a Output of Integrator (lower) with DAC feedback.

Two practical issues are of concern when designing the DAC, the linear scaling error and INL. Linear scaling error is caused by the finite matching of the reference current sources, capacitors and clock jitter. The total output error of DAC due to current mismatch and jitter , σ_{dac} is derived as (3.27b). It is obvious that the current mismatch dominates the DAC error. Since the switched current reference of the DAC scales the modulator feedback coefficients of the noise shaping transmission zeros, the shift in zero placement of modulator NTF will cause degradation of noise shaping. Hence, it requires fine calibration of current references to achieve desired noise shaping. The DAC error can be written as follows;

$$\sigma_{dac} = \sqrt{\frac{\sum_{i=1}^{CNT}(\frac{\Delta t_{cl}}{T})^2}{n} + (\frac{\Delta I_{ref}}{I_{ref}})^2} \qquad (3.27b)$$

where T is the total period of each clock pulse, Δt_{cl} is the uncertainty of the clock signal caused by the jitter, ΔI_{ref} represents the noise current of DAC and n is the number of pulses/samples to achieve each feedback, in our case n=16 or 2^4 maximum, or 8 on average.

On the other hand, the integral non-linearity (INL) of DAC must be constrained to ±½ LSB of the ADC objective, in order to realize its 16-bit accuracy [9]. By the use of the Central Limit Theorem, feedback with multiple constant pulses (instead of single long pulse) is advantageous because the white source jitter is reduced by factor of three to four times for a 4-bit system, as a result INL is further minimized. Note that, as long as the thermal noise is minimized, the jitter is of little concern as compared to the noise current

in the reference sources. Lastly, the modulator was designed in fully differential manner, it thus allows the use of one reference current per feedback coefficient, which ensures excellent DAC feedback accuracy and also optimal use of power. The use of switched-current feedback was selected for our design as the unavailability of linear double poly capacitor on process.

A small rise and fall time of the sampling clock has been designed to avoid additional jitter caused by white noise of the DAC and clock circuitry [41]. Applying the Central Limit Theorem, the jitter of the resulting clock signal, out of n samples, from DAC which is used to achieve charge-based feedback to the input of the integrators, can be represented as

$$t_{jitter(eq)} = \sqrt{\frac{\sum(\frac{\Delta t_{cl}}{T})^2}{n}} \tag{3.28}$$

To model the time uncertainty caused by the jitter, we assume that the clock signal (square wave) is generated by applying a sine wave signal V_{cl} with amplitude A, to the DAC [8]. The ideal DAC have thus a noise bandwidth proportional to the signal bandwidth (3.31). The total uncertainty of clock signal is

$$\Delta t_{cl} = \frac{e_n}{\pi \cdot A \cdot f_{cl}} \tag{3.29}$$

where A is the amplitude of the ideal sine wave used to generate the DAC clock, V_{dd} of DAC in this case, with frequency f_{cl}. And the thermal noise e_n is further defined in (3.30) as

$$e_n^2 = 4 \cdot k \cdot T \cdot R_n \cdot \Delta f \tag{3.30}$$

This gives the RMS noise value which corresponding to 1σ. 1σ is the normal distributed noise amplitude of 16% with 1rms value, equivalently equal to ½ LSB of the quantizer. R_n is the equivalent noise resistance of DAC.

For a first order system with system bandwidth of f_b, the noise bandwidth is

$$f_{noise} = \frac{\pi \cdot f_b}{2} \tag{3.31}$$

To a first order approximation, a CMOS digital circuit has a rise/fall time of,

$$t_{rise} \approx {}^{0.35}\!/_{f_b} \tag{3.32}$$

Substituing (3.30)-(3.32) into (3.29), we can easily acquire[8]:

$$\Delta t_{cl} = \frac{1}{A \cdot f_{cl}} \cdot \sqrt{\frac{0.7 \cdot k \cdot T \cdot R_n}{\pi \cdot t_{rise}}} \tag{3.33}$$

Substitute (3.33) into (3.28) and we may now estimate the time uncertainty caused by the jitter,

$$t_{jitter(eq)} = \sqrt{\frac{\sum(\frac{0.7 \cdot k \cdot T \cdot R_n}{\pi \cdot t_{rise} \cdot A^2})}{n}} \approx \frac{0.57}{V_{dd}} \sqrt{\frac{k \cdot T}{n \cdot C}} \tag{3.34}$$

From (3.34), in order to reduce the jitter, one can maximize the rise and fall time of the system clock or increase the number of samples and capacitance. In order to decrease the jitter by half, one can double V_{dd} or increase C by four times, however both increase the power consumption, $P_{dig} \propto C \cdot V_{dd}^2$. Alternatively, sizing up the output driver (transistor's length) of the DAC clock and the switches of the current steering circuit, Figure 3.12b, in order to minimize noise bandwidth while not significantly reducing the clock speed is the only solution which does not increase the power consumption significantly. Last but not least, the clock frequency was designed at 2^m times the oversampling frequency, the increase in digital power dissipation is only minimal as the gate count and area to drive the DAC is small.

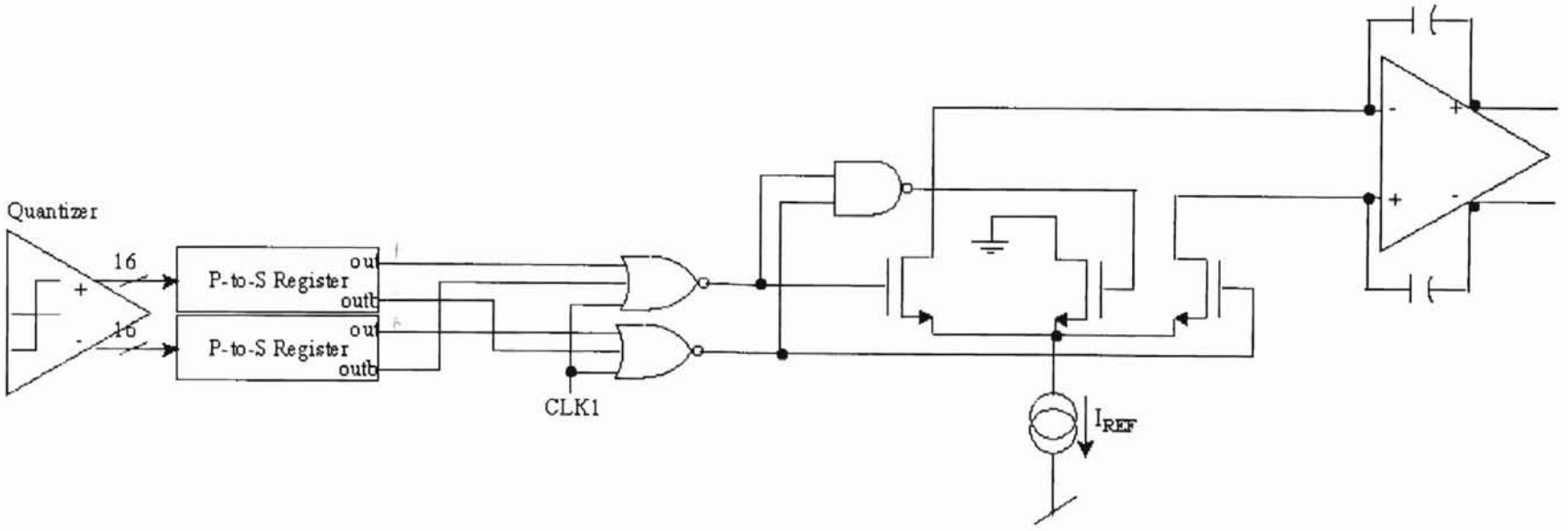

Fig 3.12b Current Metered Feedback DAC

3.5 Clock Circuitry

One simple method for generating non-overlapping clocks is shown in Fig 3.13. Here, delay blocks are used to insure that the clocks remain non-overlapping. These delays could be implemented as a cascade of an even number of inverters.

As the DAC is operating 2^4 times faster than the rest of the modulator, an additional set of non-overlapping clock signals is needed. These additional clock signals are thus 2^4 times faster than the modulator's. A 16 bit counter was then used to divide down the frequency, and its carry is made useful as a slower clock, the oversampling frequency of the modulator, as shown in Figure 3.14. The comparison of the clock phases are also presented in Figure 3.15.

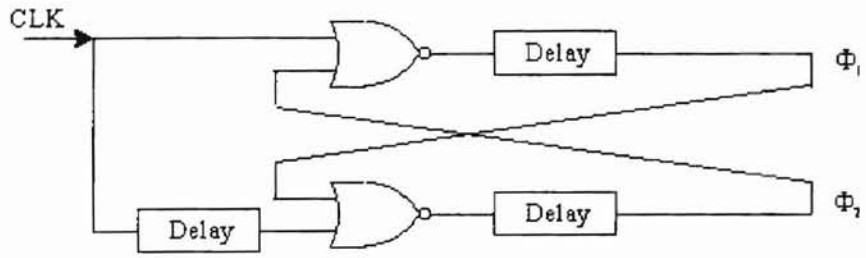

Fig 3.13 Non-Overlapping Two Phase Clock Generator

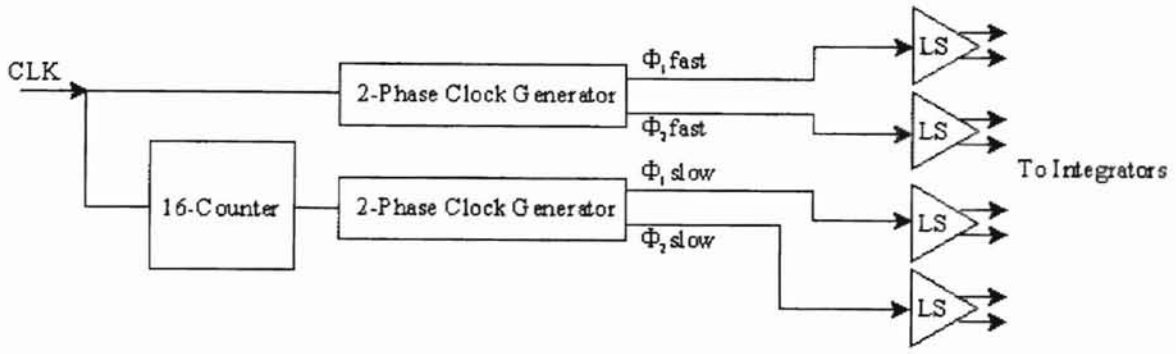

Fig 3.14 Two sets of Non-Overlapping Two Phase Clocks

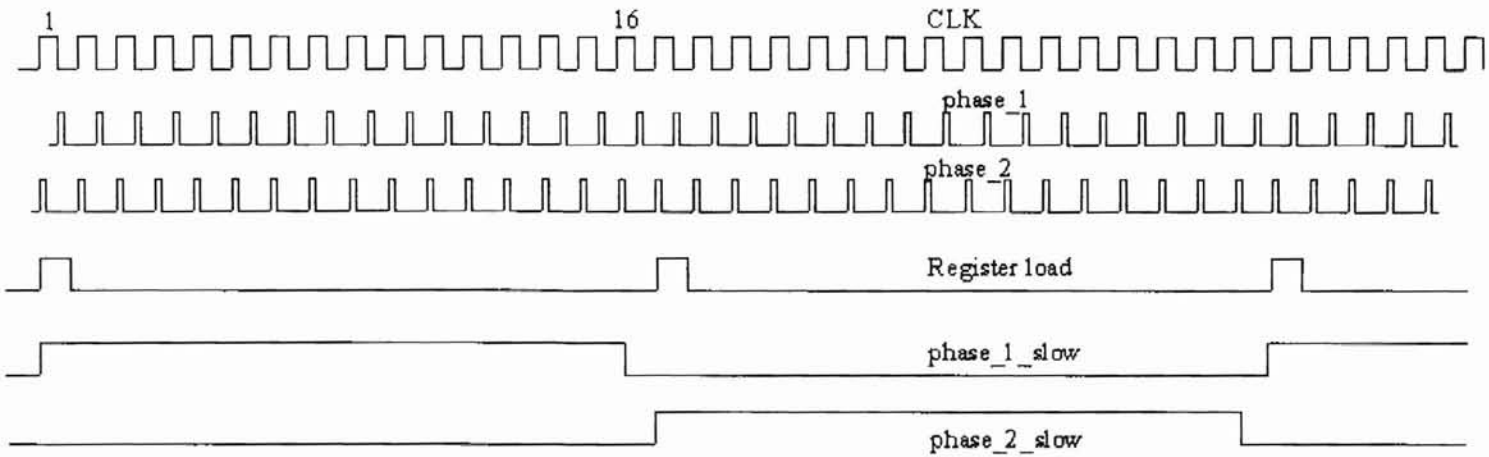

Fig 3.15 System Timing Diagram

3.6 Level Shifter

The level shifter is used in conjunction with the clock circuitry to drive the switches associated with the integrators and comparator. Since the clock circuitry is operating at a lower power supply to save digital power consumption, a step up on clock signal swing to drive the switches is required. The level shifter, as shown in Figure 3.16, take the differential inputs, and converts them to a higher voltage levels before feeding into scaled inverters to drive the switches. The reference voltages in the level shifter can be used for fine adjustment of the output edges. As the differential outputs are tracked, a relative accurate pair of clock signals is available to turn on and off different switches at the same instant at the far end. Since the output to input voltage level ratio is between 1.2 to 2, the regenerative time for the level shifter is approximately half of the stage delay of a single β–matched inverter. As a result, the total delay of the level shifter is about three times the regenerative time, which is quite short. The simulation results are shown in Figure 3.17. At layout of the modulator, the analog and digital circuits are well separated to insure isolation and a single clock path was routed from the clock generator and tree-distributed at the far end where it is applied to the integrators, so to minimize clock skew.

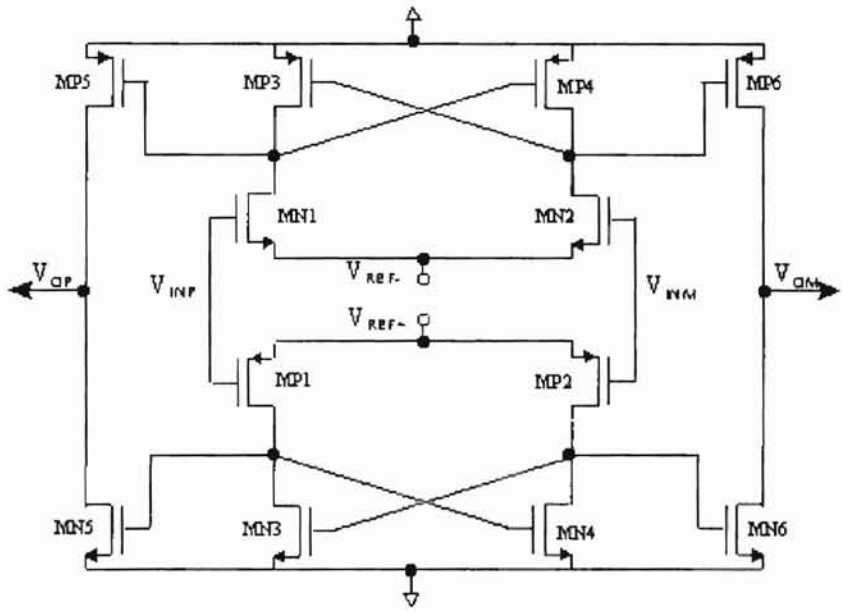

Fig 3.16 Complementary Regenerative Type Level Shifter

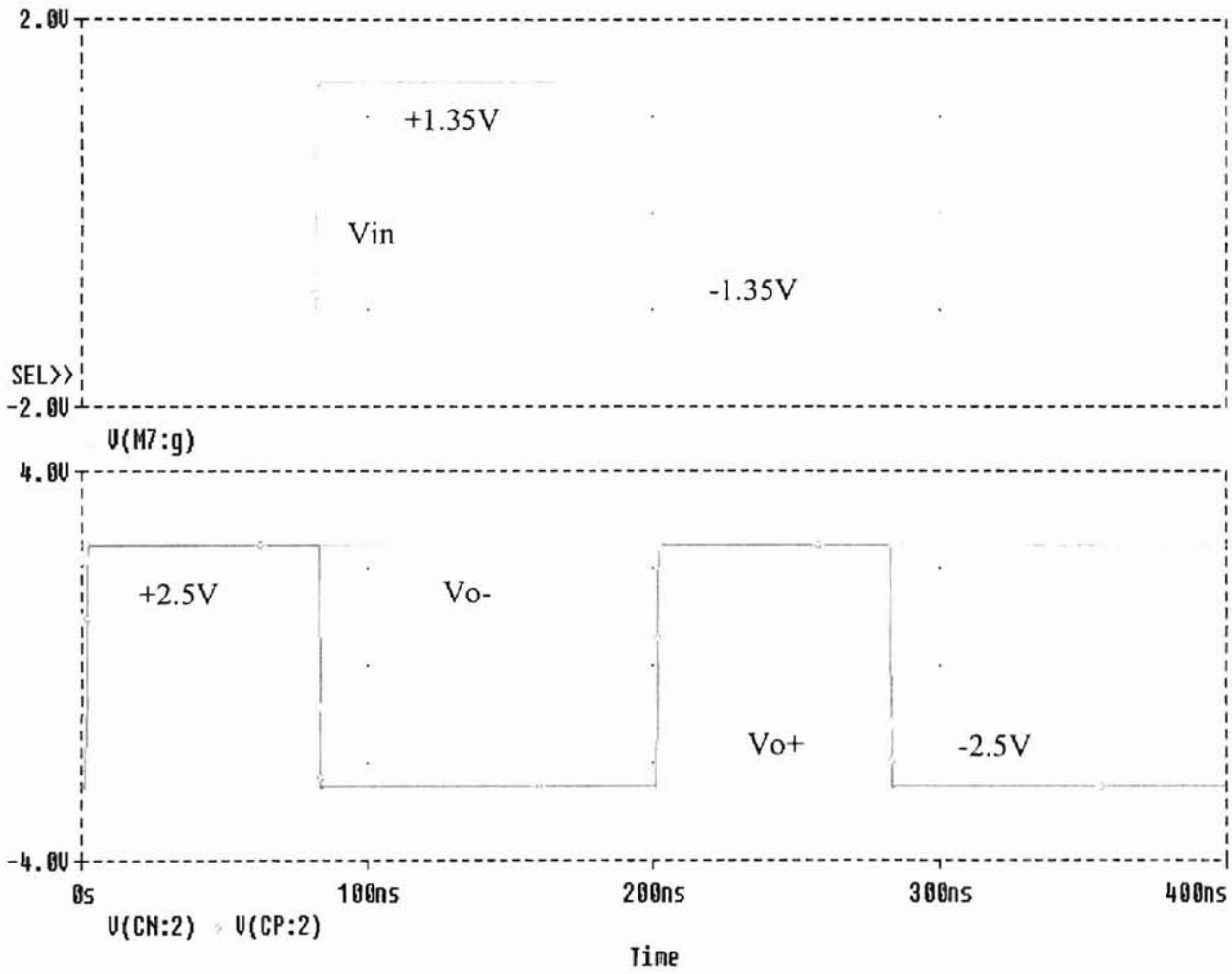

Fig 3.17 Level Shifter Transient Response

3.7 Non-Idealities on Performance Limitation

3.7.1 Leaky Integrator

In practice, the gain of the integrator is limited by circuit constraints, and thus is not infinite. The consequence of a leaky integrator is that only a fraction of β of the previous output of the integrator is added to each new input sample. The integrator transfer function is generally expressed as follows [49]:

$$H(z) = \frac{\alpha \cdot z^{-1}}{1 - \beta \cdot z^{-1}} \tag{3.35}$$

and its DC gain is then $H_0 = \frac{\alpha}{1-\beta}$. The limited gain at low frequency hence reduces the attenuation of the quantization noise in the baseband. Consequently, an increase of in-band quantization noise in the baseband, S_B, and is given by [11],

$$\frac{\Delta S_B}{S_B} = \frac{10}{3 \cdot \pi^2}\left(\frac{OSR}{H_0}\right)^2 + \frac{5}{\pi^4}\left(\frac{OSR}{H_0}\right)^4 \tag{3.36}$$

Thus, with an OSR comparable to the integrator gain H_0, the performance penalty incurred is on the order of 1.3 bits of overall ADC performance. As a result, the DC gain of the OTA should be designed to exceed the OSR by at least ten to twenty times.

3.7.2 Settling Error

Speed constraints are imposed by the OTA on the ΔΣ modulator. The GBP and slew rate (SR) are the two main parameters which characterize the amplifier dynamic performance in the linear and current limited operations respectively. The simultaneous effect of GBP and SR degradation leads to the loss of proportionality between the amplitude of the input samples and the settling error, causing an increase of the in-band noise power. To model the effect of settling error, it was assumed that it is uncorrelated from sample to sample and it is uniformly distributed in a range of $\pm\varepsilon_{max}$ as a worse case scenario, where ε_{max} is the maximum settling error [26]. It was calculated as,

$$\varepsilon(n) = SR \cdot \tau \cdot \exp(-\frac{t}{\tau} + \frac{G \cdot V_{step}}{SR \cdot \tau} - 1) \approx \Delta v \cdot \exp(^{G \cdot V_{step}}\!/_{\Delta v} - GBP \cdot t) \qquad (3.37)$$

provided that $SR\tau < GV_{step} < V_{step,max}$; τ is the time constant, defined as 1/GBP; G is the gain of integrator, defined as C_{in}/C_{fb}, usually equal to unity; V_{step} is the input step voltage resulting from both the input and the negative feedback, in steady state V_{step} is $V_{FS}/2^{m-1}$. Δv is the voltage mode of transistor, for device in saturation, it is defined as $(v_{gs}-v_T)$; for subthreshold mode, it is defined as kT/q or $v_{thermal}$.

The above model represents quite a good tradeoff between simplicity and accuracy. Using the assumptions above, the in-band settling error noise power at the output of the modulator can be then derived as [26]:

$$P_{SE} = \frac{K}{OSR} \cdot \exp\left(\frac{-g_m}{2 \cdot f_B \cdot OSR \cdot C_T}\right) \tag{3.37}$$

where

$$K = \frac{1}{3}\left(\frac{SR \cdot C_T}{g_m}\right)^2 (1+G)^2 \cdot \exp\left\{-2 \cdot \left(\frac{v_{in} \cdot G \cdot g_m}{SR \cdot C_T \cdot (1+G)} - 1\right)\right\} \tag{3.38}$$

In this case, maximum input step voltage of v_{in} or 2Δ was used for integrating time $T=f_s/4$. With the assumption that G=1, (3.37) can be approximated as follow:

$$P_{SE} \approx \frac{4 \cdot \Delta v^2}{3 \cdot OSR} \cdot \exp\left(2 - \frac{v_{in}}{\Delta v} - \frac{GBP}{f_s}\right) \tag{3.37b}$$

where Δv is v_{gs}-v_T for square law while $v_{thermal}$ for subthreshold operation.

From above equations for the in-band noise power due to settling error, a double dependency of OSR exists. The noise reduction error 1/OSR is provided by the increase in the sampling frequency and the exponential factor is due to the reduction of the settling time period, or equivalently due to the increased time percentage in the slew rate mode. It was noted that there exists an OSR value where the OTA never leaves the current-limited operation mode. Thus, for increasing values of slew rate, the improvement in the noise power saturates for large OSR value. Equation (3.37b) can be used as an insight for designing the integrators. It reveals that the gain-bandwidth product of the amplifier should be designed at least twice that of the oversampling frequency and with higher overdrive voltage in order to suppress the in-band noise power sufficiently.

3.7.3 Capacitor Linearity Issue

A highly linear double-poly capacitors is a critical element for mixed-signal IC design. The bottom plate of an interconnection layer has a capacitance to substrate whose value is similar to the capacitance value between layers, such large capacitor areas add large parasitics to the circuits and which, in turn often lead to an increase of power dissipation because of the need for increased current drive. On the other hand, a MOS capacitor formed between the gate and the shorted drain-source, has very compact area, but the non-linearity of the equivalent capacitance is often undesirable. It was claimed in [19] that switch-current $\Delta\Sigma$ ADC implementation may not require linear capacitors, in which complete system consists of transistors only. Yet for a switched capacitor implementation, linear capacitor is still desirable to the accuracy of ADC performance. Unfortunately, the available process to this project was not equipped with second layer of poly, a compromise of using oxide capacitor was thus selected on the test run.

3.7.4 Charge Injection in Switched-Capacitor Circuits

When appropriate switching is used, charge injection terms are signal independent, and the resulting injection error can be considered as constant offset and be readily corrected. Unfortunately, charge injection errors are very much signal-dependent for higher resolution ADC system. There are a few ways to reduce or cancel its effect, to reduce its limitation to the accuracy of the converter, several compensating methods are recommended: the use of dummy switch [5], autozeroing, correlated double sampling [39] and digital correction and cancellation. Most of the above circuit techniques fundamental, which deal with narrow band noise sources in general, were well presented by C. Enz and G. Temes in [39]. However, the above techniques should be employed if charge injection error becomes a performance limitation of ADC system.

3.8 Low Power System Design on Scalable CMOS Process

As technology advances, the constant scaling on CMOS process offers higher device speed and compact area. Generally, the benefits of constant scaling can be positively applied to digital systems (higher speed and lower power consumption), while regarding analog systems the constant scaling may not be always useful [18]. As processes shrinking into the deep sub-micron regime, the devices operate in the velocity saturation regime rather than the square-law mode. As a consequence, both operating modes are considered and compared in Figure 3.18 and Figure 3.19. A constant scaling factor s (>1), is used in all expressions to evaluate its effect on circuit performances [14].

The constant scaling on analog CMOS circuits is unfavorable for achieving high signal-to-noise ratio (SNR). When a process undergoes constant scaling, SNR is reduced by s^3, as indicated in (3.39). A figure of merit (FOM), which is defined in (3.40), also indicates an overall negative effect on analog circuits when operated or designed with more advanced scaled processes. The defined FOM is interpreted as the power consumption needed to maintaining a certain gain-bandwidth product (GBP) and SNR for analog circuit's performance for a process. As an additional indicator of the negative effect of scaling on analog CMOS is that the GBP-power ratio and SNR-GBP-power ratio are reduced by s^2 and s respectively in both square law and velocity saturation modes.

The effect of scaling on SNR is defined as:

$$SNR \propto \frac{V_{DD}^{2} \cdot C}{8 \cdot k \cdot T} = \frac{V_{DD}^{2} \cdot W \cdot L \cdot Cox}{8 \cdot k \cdot T} \alpha \frac{1}{s^{3}} \tag{3.39}$$

$$\frac{SNR\_GBP}{Power} \propto \left(\frac{V_{DD}^{2} \cdot C}{8 \cdot k \cdot T}\right)\frac{gm/C}{I \cdot V_{DD}} \alpha \frac{1}{\Delta V \cdot s} \tag{3.40}$$

In Figure 3.19, the FOM for digital circuits, delay-power product, is reduced by s^3 as CMOS under goes constant scaling. The only negative effect is the speed-thermal noise-power ratio which is reduced by s in the square law mode. This indicates an increase in jitter when scaling in the square law mode [14]. While operating in velocity saturation constant scaling is advantageous only for digital circuits, especially in sub-micron technology. In short, it is advantages to design digital circuits on advanced processes as it is faster and more power efficient as well, while analog circuits should be designed to operate in the longest channel length process which will achieve the bandwidth requirement. On the other hand, if operating in velocity saturation is inevitable, the overdrive voltage Δv should be no greater than required to achieve velocity saturation.

As a result of these observations, for a pure analog design to be optimal in terms of minimum power consumption per decibels of dynamic range, a suitable CMOS process must be chosen for the specific analog application by selecting the minimum channel length L which will achieve the minimum required GBP. This will insure the maximum power supply V_{DD} and in turn the maximum SNR and minimum GBP

required. In other words, it is always power efficient to have a larger power supply to maintain the maximum SNR, as shown in (3.39), as opposed to having larger capacitors to suppress the noise floor. Hence, using more advanced process than required will only power-penalize the design with no benefit, this is especially true for pure analog circuit design. In fact, on many mixed signal IC designs, especially ΔΣ ADC applications specific, the overall performance is usually bounded by the analog circuits and thus selecting an appropriate process based on analog circuit performance is obvious. A low power observation on velocity saturation design is presented. A detailed, but a different approach, of the limits to the low power circuit design is also considered by E. Vittoz, referenced in [16]. The author believes over time true mixed mode process will be utilized to provide designer with both analog and digital transistors.

F.O.M.	Square Law Devices	Velocity Saturation Devices
GBP	$gm/C = \frac{W/L \cdot \mu \cdot Cox \cdot \Delta V}{W \cdot L \cdot Cox} = \frac{\mu}{\Delta V \cdot L^2} \quad \alpha \quad \frac{s^2}{\Delta V}$	$gm/C = \frac{W \cdot Cox \cdot v_{sat}}{W \cdot L \cdot Cox} = \frac{v_{sat}}{L} \quad \alpha \quad s$
$\frac{GBP}{Power}$	$\frac{gm/C}{I \cdot V_{DD}} = \frac{1}{W \cdot L \cdot Cox \cdot \Delta V \cdot V_{DD}} \quad \alpha \quad \frac{s^2}{\Delta V}$	$\frac{gm/C}{I \cdot V_{DD}} = \frac{2}{W \cdot L \cdot Cox \cdot \Delta V \cdot V_{DD}} \quad \alpha \quad \frac{s^2}{\Delta V}$
SNR_GBP	$\frac{V_{DD}^2 \cdot C}{8 \cdot k \cdot T} \cdot \frac{W/L \cdot \mu \cdot Cox \cdot \Delta V}{C} = \frac{\frac{W \cdot V_{DD}^2}{L \cdot \Delta V} \cdot \mu \cdot Cox}{8 \cdot k \cdot T} \quad \alpha \quad \frac{1}{\Delta V \cdot s}$	$\frac{V_{DD}^2 \cdot C}{8 \cdot k \cdot T}\left(\frac{v_{sat} \cdot Cox \cdot W}{C}\right) = \frac{V_{DD}^2 \cdot W \cdot v_{sat} \cdot Cox}{8 \cdot k \cdot T} \quad \alpha \quad \frac{1}{s^2}$

Figure 3.18 Comparison of Devices Operate in Square Law and Velocity Saturation for Analog Circuits.

F.O.M.	Square Law Devices	Velocity Saturation Devices
Delay	$C \cdot \frac{V}{I_{DS}} = \frac{W \cdot L \cdot Cox \cdot V_{DD}}{\frac{W \cdot \mu \cdot Cox \cdot \Delta V_{DD}^2}{L}} \approx \frac{L^2}{\mu \cdot Cox \cdot \Delta V_{DD}}$ $\alpha \ \frac{1}{s}$	$C \cdot \frac{V}{I_{DS}} \approx \frac{W \cdot L \cdot Cox \cdot V_{DD}}{W \cdot v_{sat} \cdot Cox \cdot \Delta V_{DD}} \approx \frac{L}{v_{sat}}$ $\alpha \ \frac{1}{s}$
Power	$\frac{W}{2 \cdot L} \cdot \mu \cdot Cox \cdot \Delta V_{DD}^3 \ \alpha \ \frac{1}{s^2}$	$W \cdot v_{sat} \cdot Cox \cdot \Delta V_{DD}^2 \ \alpha \ \frac{1}{s^2}$
Power_Delay	$\frac{1}{s^3}$	$\frac{1}{s^3}$
$\frac{Speed}{Thermal\_Noise}$	$\frac{\frac{I}{CVkT}}{C} = \frac{\varepsilon ox}{TOX} \frac{W}{L} \frac{\mu \Delta V_{DD}^{\ 2}}{2VkT} \approx \frac{\varepsilon ox}{TOX} \frac{W}{L} \frac{\mu \Delta V_{DD}^{\ 2}}{2kT}$ $\alpha \ \frac{1}{s}$	$\frac{I}{CV v_{nT}^{\ 2}} \approx \frac{\varepsilon ox}{TOX} W \frac{v_{sat} \Delta V_{DD}}{2VkT}$ $\approx \frac{\varepsilon ox}{TOX} W \frac{v_{sat}}{2kT} \ \alpha \ 1$

Figure 3.19 Comparison of Devices Operate in Square Law and Velocity Saturation for Digital Circuits.

CHAPTER 4

CONCLUSIONS AND SUGGESTIONS

ΔΣ A/D converters, using noise-shaping techniques, have demonstrated their ability to achieve resolutions in excess of 16 to 20 bits at low power levels. The more successful approaches [1,2,3,4] have based the architecture on the robustness of the 1-bit quantizer. The ΔΣ feedback from the quantizer is required to be accurate to the same dynamic range as the ADC under design. Component matching limits of approximately 0.1% (10 bits without special trimming or calibrations methods [5]) have prohibited the use of multibit quantizer and DAC until now.

This restriction to a 1-bit quantizer requires higher oversampling ratios. A second and third order 1-bit ΔΣ ADCs require an OSR in excess of 128 to achieve 16-bit resolution and three times higher OSR for 20-bit systems. The high oversampling ratio results in excessive power dissipation due to both the high slew rate requirements of integrators and high clock rates of the digital systems. In general, the power consumption of the modulator can be divided into two related but different sources, both are linearly dependent on the oversampling frequency, f_s. Typical OTA and comparator tail currents

must be set to achieve the slewing requirements of the integrator settling which is directly dependent on f_s while logic power dissipation is set directly by the CV^2f_s component.

Efforts to achieve a significant reduction in power consumption which focuses on reducing the oversampling ratio, M, through the use of multibit quantizers has the benefit of reducing both the analog and digital power components of the modulator. In addition, multibit ΔΣ ADCs have been shown to exhibit more robust stability characteristics with lower slew rate, wider signal range, better immunity to idle tone problems and lower out of band noise [6,7,8,9]. However, a robust approach to accurate DAC design was demonstrated.

This design work was conducted on a multibit ΔΣ A/D quantizer which utilizes a clocked current metered DAC to maintain DAC accuracy well in excess of 16 bits. As a result of this new DAC approach, implemented on fully depleted TFSOI process, the power dissipation is reduced by a factor of three to four times approximately over existing single bit design on bulk processes.

On the other hand, higher order modulators require careful attention to the placement of appropriate zeros in the transfer function of the analog filter [1, 24, 25]. Moreover, when a higher order modulator is driven by a large input, the single-bit quantizer is overloaded, causing an increase in the quantization noise [25]. The increased quantization noise is amplified by the analog filter in the modulator leading to instabilities which is observed as a low frequency oscillations. Thus, a third or higher

order modulators based on the use of a single bit quantizer are potentially unstable [26] and may require circuitry to reset the integrators when large signals are detected in the integrator outputs [27]. Stable higher order modulators employing a single quantizer can be designed, provided that the number of levels in the modulator's quantizer is increased sufficiently to prevent the overload of the quantizer [10-12]. The use of a multibit quantizer thus has the additional benefit of reducing the power of the quantization noise introduced by the quantizer itself. In this design, a third order interpolative 4-bit $\Delta\Sigma$ modulator using this novel application in DAC design was hence encouraged.

The modulator was submitted for fabrication on IBM thin-film silicon-on-insulator (TFSOI) process. It is known that SOI has excellent capability as a low power technology. Dropping the voltage is very effective in reducing chip power. The ability of SOI as a low power source originates from the fact that SOI circuits can operate at low voltage with the same performance as a bulk technology at high voltage. At the same performance as bulk CMOS, SOI can reduce the chip power by 1.7-3X (depending on the switching factor of the devices). Further direct illustration from Figure 4.1, we observe the benefit of using of SOI devices is that the power consumption and power supply voltages is substantially reduced although the parasitic capacitance is only reduced by one-fifth, as opposed to bulk.

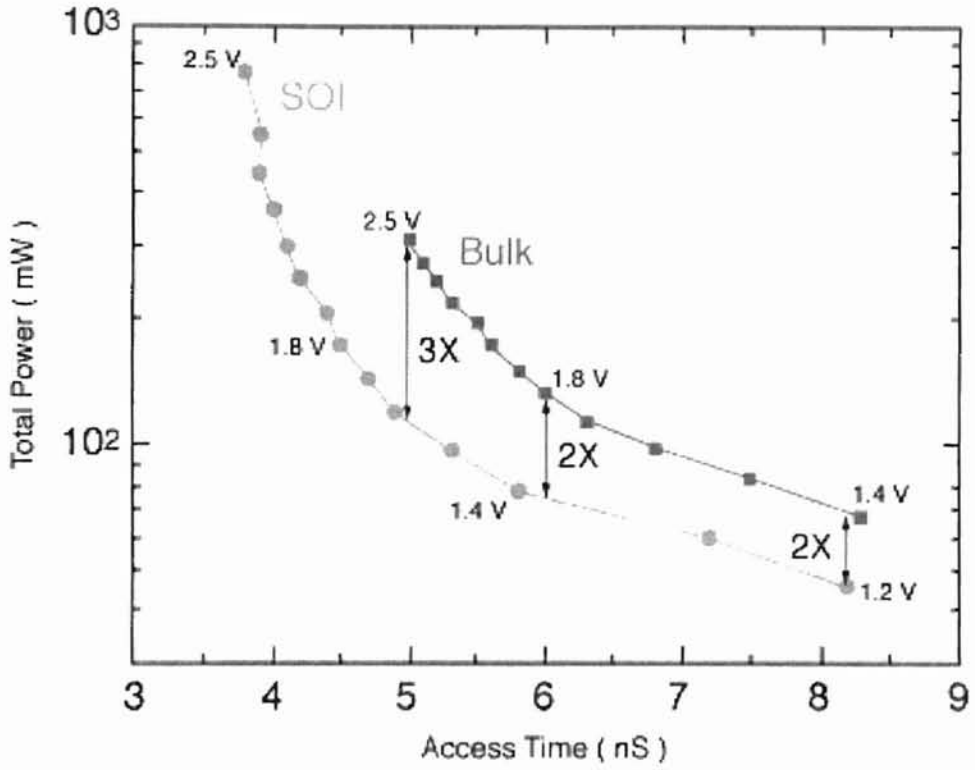

Fig 4.1 Comparison of Power Consumption for Both Bulk and SOI Devices

4.1 Testing of ΔΣ Modulator

Conventional histogram analysis is used to test the linearity, offset, DNL and missing code [54]. It is a good test, for linear ADC, yet requires a large number of samples from the input sine wave. For example, DNL test for 16-bit ADC to within 0.1% with 95% confidence will require more than 20M sample. Thus, FFT based tests are a more common test for high resolution non-linear ΔΣ ADC test.

FFT spectrum testing is used mainly to evaluate the noise floor, harmonic level and spurious free dynamic range (SFDR) of ADC. The noise floor reflects the quantization noise, aperture noise and missing codes. The harmonic distortion reflects the non-linearity which distorts the transfer function. A spurious free spectrum reflects the lack of interference signals such as parasitic oscillation and the intermodulation of this signal with the input [8]. Although FFT testing is intuitive, selection of the input frequency is critical. According to DFT theory, the data sequence is assumed to repeat itself with a period of NT (N is number of sample and T is the sampling period). Leakage will occur when the sampling frequency is not an integer multiple of the input frequency, i.e. $f_{samp} \neq kf_{in}$. As consequence of this discontinuity, a new frequency component is generated. On the other hand, if $f_{samp} = kf_{in}$, only several identical levels in the signal cycles are repeated sampled and thus many bins of ADCs are not tested. In short, the frequency leakage is inevitable for ADC testing. However, windowing functions can reduce leakage but reduce the frequency resolution as well. Proper choice

of input frequency and windowing function is thus very important for accurate and informative ADC test. Analytically, an input x_{in} to A/D has output y_{out}, which consisting of N samples has an integer number of whole cycles of the input sine wave [51]. And the SNR of a test frequency is derived in (4.5).

$$x_{in}(t) = A \cdot \cos(\omega t + \phi) \tag{4.1}$$

$$y_{out}(t) = s(n) + \varepsilon(n) \tag{4.2}$$

where ε is the noise component of output y.

If the desired frequency component ω be j-th element of $Y_{out}(k)$, the variance of the signal or also known as the signal power is [52]:

$$\sigma_s^2 = \frac{2}{N(N-1)}|Y(j)|^2 \tag{4.3}$$

An unbiased estimate of the in-band noise power is also given by:

$$\sigma_n^2 = \frac{2}{N(N-1)} \sum_{k=1}^{(M-1)/2} |Y(k)|^2 \qquad ,k \neq j \tag{4.4}$$

Hence, the SNR for the test frequency ω is derived as:

$$SNR = 10 \cdot \log\left(\frac{|Y(j)|^2}{\sum_{k=1}^{(M-1)/2} |Y(k)|^2} \right) \quad ,k \neq j \tag{4.5}$$

FFT based testing is widely used for characterizing ΔΣ ADC for its simplicity and unbiased accurate estimation of SNR. Modulator output data generated from testing is expected to be performed using the spectrum analysis in behavioral MATLAB® design toolbox developed at OSU.

All the key blocks are padded for both AC and DC testing along with the modulator. The following blocks will be characterized for their functionality and AC performance: amplifier(DC open-loop gain, GBP and phase margin), DAC(INL), comparator(settling time), clock circuitry and level shifter for functionality.

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