A 4-BIT 1GSPS LOW-POWER FLASH ANALOG-TO-DIGITAL CONVERTER WITH AN INHERENT REFERENCE STRING

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This study was conducted to propose a unique high-speed (1Gsps) low power 4-bit flash analog-to-digital converter (ADC). The complete ADC including the unique comparator bank was designed, simulated, laid-out, fabricated, and tested successfully.

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NOMENCLATURE

ADC	Analog-to-Digital Converter
C	Capacitance
C_{gs}	Gate to Source Capacitance
C_{IN}	Input Capacitance
C_L	Load Capacitance
C_T	Total Input Capacitance
DAC	Digital-to-Analog Converter
DR	Dynamic Range
f_B	Bandwidth
f_N	Nyquist Rate
f_t	Process Bandwidth
g_{ds}	Drain to Source Transconductance
g_m	Transconductance Parameter
I_D	Drain Current
I_{dd}	Power Supply Current
k	Boltzmans Constant
k	Transconductance
L	Transistor Channel Length
LSB	Least Significant Bit

MSB	Most Significant Bit
n	Number of Bits
OTA	Operational Transconductance Amplifier
R	Resistance
R_{IN}	Input Resistance
R_O	Output Resistance
Ron	Transistor On Resistance
R_S	Source Resistance
SiMOX	Separation by IMplantation of OXygen
SNR	Signal-to-Noise Ratio
SOI	Silicon On Insulator
SOS	Silicon On Sapphire
T	Absolute Temperature
T_{CLK}	Clock Period
t_d	Delay Time
T_S	Settling Time
V_{dd}	Positive Power Supply
V_{FS}	Full Scale Voltage
V_{IN}	Input Voltage
V_{OS}	Offset Voltage
V_{OUT}	Output Voltage
V_{pp}	Peak-to-peak Voltage
V_{REF}	Reference Voltage

V_S	Source voltage
V_{ss}	Negative Power Supply
VTC	Voltage Transfer Characteristic
V_{TN}	NMOS Threshold voltage
V_{TP}	PMOS Threshold voltage
V_{TRIP}	Inverter Trip Voltage
W	Transistor Channel Width
W/L	Transistor Width to Length Ratio
Z_{IN}	Input Impedance
Z_L	Load Impedance
Z_O	Transmission Line Impedance
Δq	Quantum
ΔV	Overdrive Voltage
ΔV_{TRIP}	Trip Voltage Difference Between Two Adjacent Inverters
β	Beta
μ	Transistor Self-Gain
τ_X	Time Constant

CHAPTER 1

INTRODUCTION

Analog-to-digital converters or ADCs digitize analog signals for use in digital signal processing (DSP). For example, noise elimination in audio and image signals using digital filters and fast algorithms have resulted in high quality radio and TV equipment. High performance ADCs on SOS/SiMOX are now essential in space, battery-operated, portable communication systems. Digitizing as close as possible to the antenna provides the system designer access to high yield, low cost DSP solution in combination of silicon and software.

High-speed ADCs are essential for accurate and fast conversion rates that are required for sophisticated real time data processing. There are many techniques that can be used to convert analog signals to digital. Among them the flash ADC is the fastest (see Chapter 2). The ultimate goal is to produce ADCs that are fast, accurate, low-power consuming, and take up less die area on chip.

1.1 Objective

This study will attempt to introduce and review the essential methods to achieve

the above goals. A flash ADC has been designed, simulated and tested that provides a 4-bit resolution and an estimated 1Gsps conversion rate. The uniqueness of the ADC lies in the fact that it has an inherent reference string embedded within the comparator bank (see Chapter 3). This eliminates the requirement for a resistor string present in flash ADCs.

1.2 Organization

Chapter 1 has introduced the background and the purpose behind this study.

Chapter 2 reviews flash ADCs. It discusses basic operation, advantages and disadvantages and design problems associated with flash ADCs (section 2.1). Then section 2.2 discusses ADC design considerations. Factors that limit ADC accuracy are then described in section 2.3. Section 2.4 discusses ADC specifications and lastly section 2.5 discusses test procedures that are useful in determining ADC performance.

Chapter 3 discusses the unique 4-bit flash ADC that has been developed. It includes functional description, circuits analysis (section 3.1), simulation (section 3.2), and test results (section 3.3).

Chapter 4 presents two applications of 4-bit flash ADC. The first application is a time-interleaved ADC using four flash ADCs described in this study arranged in parallel (section 4.1). The second application describes how a flash ADC is used in an automatic gain control system in a receiver (section 4.2).

Chapter 5 summarizes the results of this study, conclusions, and proposes some improvements.

CHAPTER 2

LITERATURE REVIEW

ADCs are an integral part of today's telecommunication hardware. As mentioned in the introduction, ADC design goals are to achieve higher dynamic range, faster conversion rates, and low-power operation while consuming less area on chip. These goals are achieved by using a number of circuit design and layout techniques that are discussed in this chapter. It is also important to take into consideration the basic analog-to-digital conversion techniques and the fabrication process when attempting to optimize performance. Achieving these goals aid in the overall quality of the product including efficiency, cost, and reliability.

This literature review discusses the flash ADC architecture in detail including its advantages and disadvantages over other types of ADCs. A brief discussion of ADC design considerations and factors that limit accuracy are presented. An overview of ADC specifications and test procedures that are used to measure performance are also included.

ADCs convert an input analog signal into a string of binary numbers where, each binary number represents a sampled input voltage level. This conversion can be accomplished in many ways. Depending on the conversion mechanism, ADCs are categorized into three types. The first type or type I is called the serial ADC. They

include the dual slope or integrating, delta-sigma (or sigma-delta), successive approximation, bit-serial pipelined, and algorithmic ADCs. The Type II is the parallel, or more commonly known as the flash ADC. Finally, the type III ADC is subranging ADC (two step and multiple step). In this chapter, our emphasis will lie in discussing the type II or flash ADC ([1] pp.1-21, [2] pp.54-59).

2.1 Flash ADC Architecture

A flash ADC digitizes a signal by simultaneously comparing a sample of the input signal with monotonically increasing quantization voltage levels. Each quantization level corresponds to a binary number from zero to full scale of the ADC. The result is a binary representation of the input signal. The flash ADC uses a "brute force" ([1] p.16) method that realizes the fastest possible means since the entire conversion is accomplished in one step.

A block diagram of a generic flash ADC is shown in Figure 2.1. The flash ADC can be divided into three subsystems. They are the comparator, the bubble detector, and the encoder stages.

2.1.1 Comparator Stage

The most critical circuit element of the flash ADC is the comparator. For a n-bit flash ADC, 2^n-1 number of comparators are required. A comparator compares the magnitude of one signal to another. In an ADC, one input of a comparator is connected to the input signal and the other input is connected to a unique quantization level (see Figure

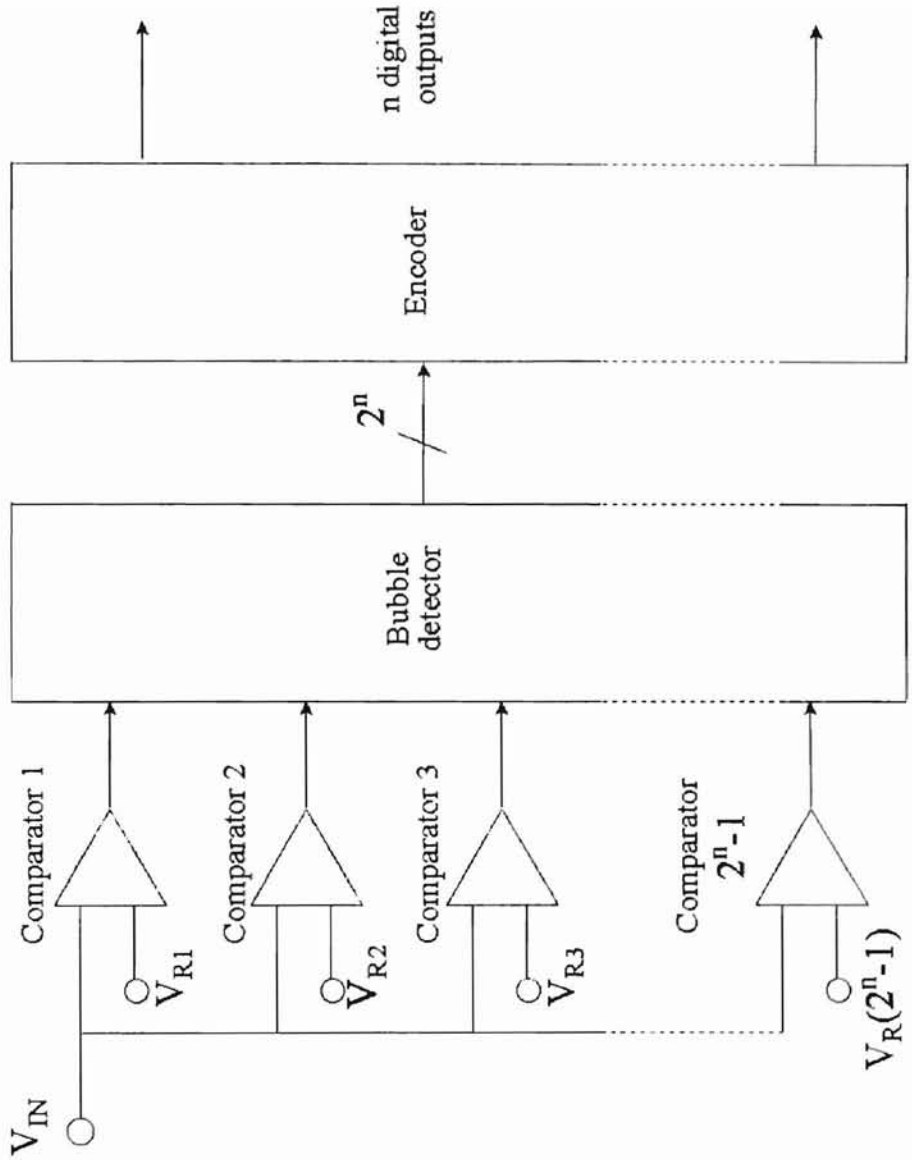


Figure 2.1 A generic flash ADC block diagram

2.1). Each comparator, compares the sampled input signal level to its specific quantization level (quantization levels are denoted by $V_{R(2^n-1)}$ in Figure 2.1). If the sampled input signal level is higher than the quantization level of a particular comparator, then the comparator output is a logic '1'. If the sampled input signal level is lower than the quantization level of a particular comparator, then the comparator output is a logic '0'.

The comparator bank output is a thermometer code. The outputs of the comparators with quantization levels below the sampled input voltage level, are logic '1's. Similarly, the outputs of the comparators with quantization levels above the input signal voltage are logic '0's. The transition point or boundary between the logic '1's and the logic '0's in the thermometer code represents the level of the input voltage. In addition, two more comparators can be added to indicate underflow and overflow (See Chapter 3).

Comparator amplification techniques are used to force the comparator outputs to valid logic levels of '0' or '1' as quickly as possible. Comparator circuits can come in many forms such as switch capacitor, differential pair, or inverter forms and categorized as single pole amplifier, multistage (feed forward) amplifier, and regenerative amplifier [3].

Until now quantization voltage levels have been produced by a resistor string ([1] p.16) or conversion ladder ([5] p.3). This resistor string provides the comparators with monotonically increasing voltages in increments of a quantization voltage (Δq). Problems with this reference string are power consumption and errors caused by mismatch and loading effect.

Recently, several new ideas, including the basis for this study, have eliminated the need for a resistor string. They incorporate an inherent reference string built into the comparators by using various techniques. Each comparator is an inverter having a different trip voltage. This simulates the quantization levels. In reference [12] and [13] the trip voltages for each inverter are realized by Focused-ion-beam implants to control the process locally resulting in multiple MOSFET threshold voltages. The technique used in this study also uses the inverter as a comparator. The only difference is that by varying the widths of the NMOS and PMOS devices of the inverter (see Chapter 3), a different trip voltage for each inverter is established.

The advantage of setting device geometry over the Focused-ion-beam implant is that it uses standard technology and doesn't require additional costly and special process steps. The Focused-ion-beam implant method requires time consuming process steps to locally control the transistor threshold voltages to set the inverter trip voltages.

2.1.2 Bubble Detector Stage

The above mentioned boundary between the '1's and '0's in the thermometer code must be detected in order for the digital encoder to produce the corresponding digital representation of the sampled input voltage. The bubble detector stage detects this boundary. One of the 2^n outputs of the bubble detector stage will have logic high representing the thermometer code boundary. The rest of the outputs are low. The bubble detector does this by using simple combinational logic in the form of NAND or NOR

gates. Since the thermometer code is not always perfect, error correction techniques described in [3] and [11] are frequently used in the bubble detector logic (see Chapter 3).

2.1.3 Encoder Stage

The bubble detector produces just one active high in 2^n output signals resulting in a unique address that can be applied to the encoder stage. The encoder codes 2^n logic signals to an n-bit binary word. This requires n number of encoders. Circuit implementation of encoders can be realized using ROM (read-only memory), PLA (programmable logic array) ([1] pp.32-35), or regeneration circuits [3] which is the fastest among the three [16].

The advantage of flash ADCs over other types is its high-speed conversion capabilities. But they suffer from high power dissipation from the resistor string and large number of high-speed comparators (the number of comparators doubles for every additional bit). Exponentially increasing numbers of comparators lead to larger and therefore expensive chip size and poor matching. The large input capacitance of the comparators needs to be driven by power consuming input buffers that are required to prevent bandwidth reduction. These problems and more discussed in detail in the next section limit the flash ADC resolution to not more than 8 bits.

2.2 Design Considerations for Flash ADC

In this section, some ADC design considerations are briefly discussed. They include the resistor string, charge injection, input capacitance and settling time, small signal bandwidth, slew rate limitation, and design for low-power and low-voltage.

2.2.1 Resistor String

The resistor string provides the quantization voltage levels to each comparator. The resistor string is the primary factor effecting the linearity of a flash ADC. The quantization voltage level applied to each comparator is in increments of $(1/2^n)V_{FS}$. Therefore the quantization error should be no greater than ½ LSB (1 LSB = $1/2^n$). The resistor string bow effect introduces error into the reference voltages and is discussed in section 2.3.3. Choosing proper geometry, low resistance metal, and an accurate process are ways to reduce errors introduced by resistor string mismatches.

The resistor string or ladder is also the primary source of ADC power dissipation. Eliminating the resistor string and its associated power consumption has been achieved for the flash ADC developed in this study (see Chapter 3). This has resulted in reducing the power consumption significantly.

2.2.2 Charge Injection

Analog CMOS switches develop undesired parasitic capacitance between their gate and source/drain terminals. If a MOS switch is turned off, channel charge dissipates producing a transient current. This in turn affects the linearity of the ADC by reducing

switched capacitor comparator circuit resolution. Charge injection occurs due to channel charge and clock feedthrough and is modeled in [22]. Reducing charge injection can be accomplished by isolating comparator inputs by proper timing of transmission gates, clock phase isolation, using fully differential and/or multi-stage comparators (usage very common [28]), adding larger switching capacitance (increases power consumption though) ([4] pp.312-314)[27], and using dummy switches (least effective method) [28].

2.2.3 Input Capacitance and Settling Time

The input capacitance limits the performance of a flash ADC affecting its bandwidth, settling time and slew rate. The input capacitance including the pad and gate oxide (C_{gs}) of comparators poses a loading problem for the signal buffer that drives the comparators. Figure 2.2 shows the equivalent circuit at the input of a high-speed ADC. The signal generator (V_S) having an output resistance of R_S (typically 50Ω) is connected by a transmission line having an impedance of Z_0 (50Ω) to the input of the ADC. R_{IN} and C_T represent the ADC input resistance and capacitance respectively. Note that C_{IN} is the input capacitance of a single comparator.

The input capacitance typically depends on the dynamic range of the ADC (higher the number if bits (n) required, the larger C_T becomes). However, large C_{IN} reduces the bandwidth of ADC. The maximum C_{IN} for a given frequency is given below,

$$C_{IN} << \frac{1}{2\pi f_B 2^n Z_0} \tag{2.1}$$

where f_B is the operation speed and n is the number of bits of the ADC. Substituting $f_B=2f_N$ were f_N is the nyquist frequency and as an example letting f_N=2GHz, n=4 bits, and

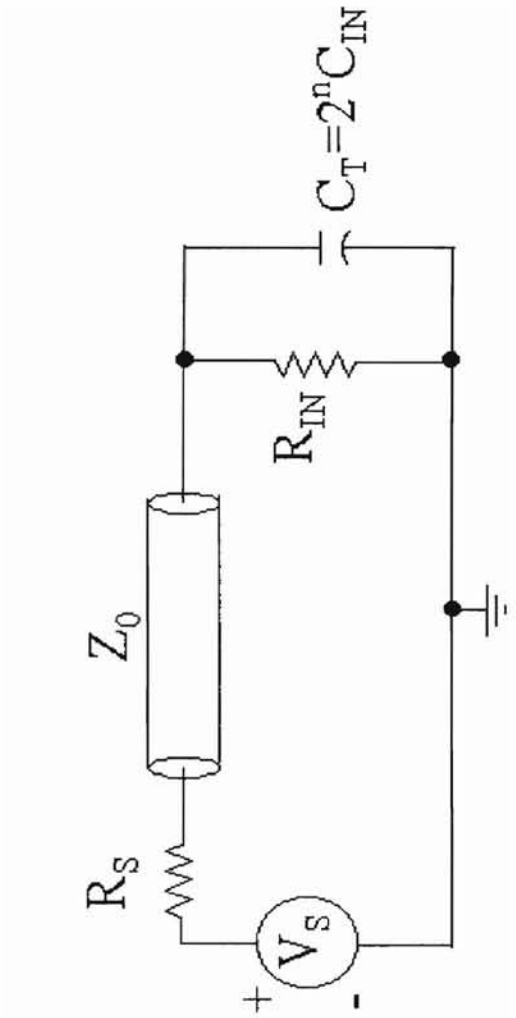


Figure 2.2 Equivalent circuit at ADC input

Z_0=50Ω, equation 2.1 sets a maximum limit on C_{IN} which is,

$$C_{IN} << 200fFd .$$

The above result clearly states that if the device is to operate at the given frequency, the input capacitance must be limited. Also note that an amount of 200fFd is difficult to achieve.

Let us further examine equation 2.1. It is re-written as,

$$f_N = \frac{1}{2^n \pi Z_0 C_{IN}} . \tag{2.2}$$

Using $C_{IN}=C_{gs}=2/3WL\mu C_{ox}$ and Z_0=50Ω,

$$f_N = \frac{3}{100\pi 2^n WL\mu C_{ox}} . \tag{2.3}$$

By substituting Peregrine UTSi 0.5μm process model parameters given in Table B.1, equation 2.3 is simplified to,

$$f_N = \frac{1.082\times 10^{12}}{W 2^n} . \tag{2.4}$$

Taking the natural logarithm of both sides of equation 2.4 gives,

$$\ln(f_N) = \ln\left(\frac{1.085\times 10^{12}}{W}\right) - n\ln(2) . \tag{2.5}$$

The plot of equation 2.5 for $\ln(f_N)$ versus n for values of W=4,8,40, and 80μm is shown in Figure 2.3. From this plot, it is seen that as the number of bits (n) increases, the natural log of the nyquist frequency decreases. Also as the widths of the comparators are increased, the speed performance recedes. Both phenomena occur due to the increase in input capacitance. To achieve high DR bandwidth a buffer (without distortion) must be utilized.

Another limitation at the input to ADC performance is reflections on the transmission line when not terminated properly [23][39]. To minimize reflection in the circuit of Figure 2.2, the impedance R_S, Z_0, and R_{IN} must be matched very close to each other [39]. At high speeds the line inductance associated with interconnect between the transmission line and the input (i.e. bond wire inductance) can further degrade ADC performance [3].

By way of an example let there be a mismatch between Z_0 and Z_L (ADC input impedance) of ε. The transmission function is,

$$T(\omega) = \frac{2Z_L}{Z_L + Z_0}. \tag{2.6}$$

Substituting for $Z_L = Z_0(1+\varepsilon)$ and simplifying gives,

$$T(\omega) = \frac{2[Z_0(1+\varepsilon)]}{Z_0(2+\varepsilon)} \approx (1+\varepsilon)\left(1-\frac{\varepsilon}{2}\right) = \left(1+\frac{\varepsilon}{2}-\frac{\varepsilon^2}{2}\right). \tag{2.7}$$

Assuming that the second order term in equation 2.7 is negligible,

$$T(\omega) \approx \left(1+\frac{\varepsilon}{2}\right).$$

The error (ε) introduced by mismatch must satisfy,

$$\left|1-\left(1+\frac{\varepsilon}{2}\right)\right| V_{IN} < \frac{V_{FS}}{2^{n+1}} \tag{2.8}$$

where, V_{FS} and V_{IN} are the ADC full scale and input voltage respectively. Satisfying the above condition keeps the ADC error less than ½ LSB, which is essential for accurate conversion (see section 2.4.1). Simplifying equation 2.8 to find n results in,

$$n < \frac{\ln\left(\frac{V_{FS}}{V_{IN}}\right) - \ln|\varepsilon|}{\ln 2}. \tag{2.9}$$

The plot of n versus ε of equation 2.9 for equality is shown in Figure 2.4 for V_{FS}/V_{IN} ratio values of 10, 4, 2, and 1. From this plot it is seen that as the mismatch increases, the dynamic range of the ADC decreases. For example from the graph, for a 10% mismatch, the maximum number of bits of the ADC is less than 4. This result implies that the external circuitry mismatches limit the ADC dynamic range.

Assuming R_{IN} is infinite and Z_0 is negligible in Figure 2.2, analysis shows ([1] p.51) the settling time T_S of an ADC is given by,

$$T_S = R_S \cdot C_T \cdot \ln(2^n) < T_{CLK} \,. \tag{2.10}$$

Note that C_T is set by the noise floor (kT/C). Equation 2.10 represents a fundamental limit for the speed-resolution of an autozeroed switched capacitor CMOS flash ADC ([1] p.51). Also note that the settling time at the input has to be less than the ADC sampling clock period (T_{CLK}). As an example, substituting values into equation 2.10 gives,

$$T_S = 50\Omega \cdot 200fF \cdot 2^4 \cdot \ln(2^4) = 0.444ns \,,$$

for n=4. This result limits the speed of a 4-bit ADC to less than 2.25GHz.

2.2.4 Small Signal Bandwidth

The performance of the input buffer is limited by the ADC input capacitance and the input driver output impedance. Equation 2.10 shows the effect of C_{IN} that needs to be kept as low as possible to prevent bandwidth reduction. This implies that the number of comparators be limited and thus limiting flash ADC resolution.

At high frequencies, the amplification will degrade and eventually ADC resolution will drop. The requirement from the comparator is for the output to have

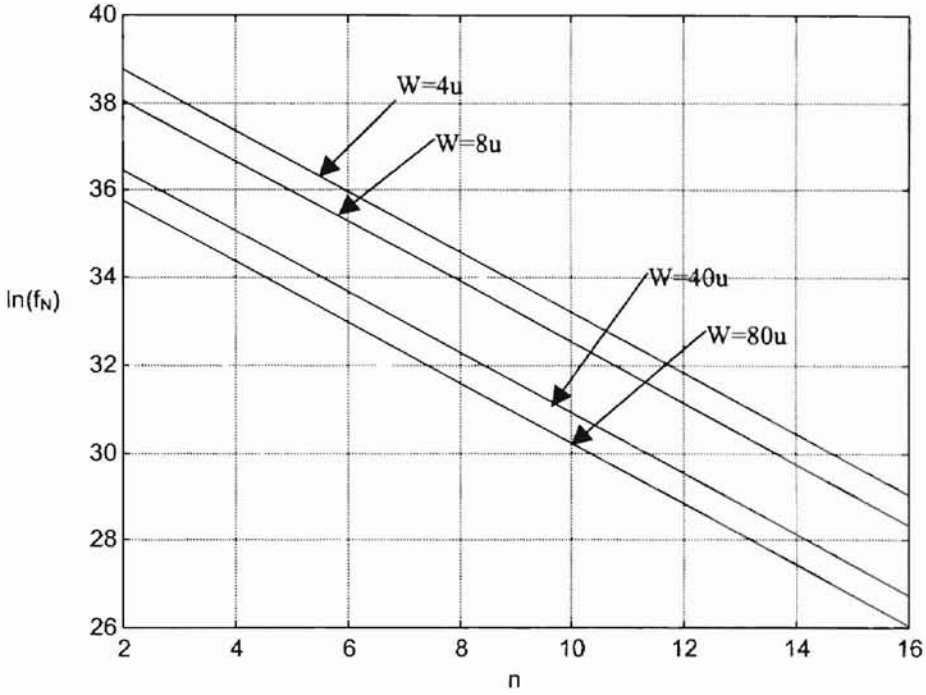


Figure 2.3 Graph of equation 2.5 for W=4,8,40, and 80μm

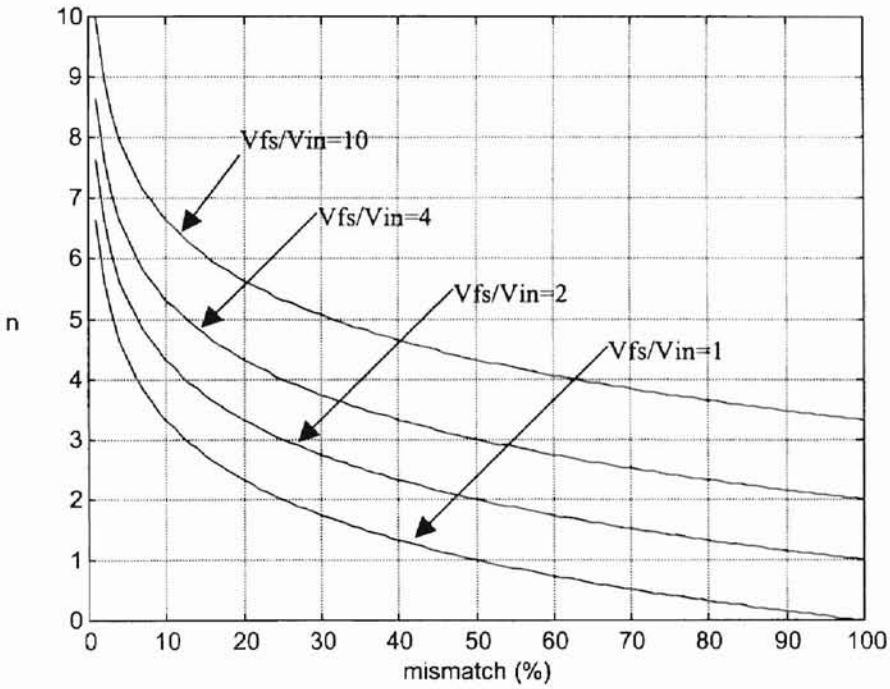


Figure 2.4 Graph of equation 2.9

sufficient drive capabilities to properly latch valid logic levels. Therefore, the 3dB point may not always need to be used and a higher frequency may be sufficient ([1] pp.59) and still have proper latching. This implies that the latch sensitivity and gain must to be taken into consideration when designing for bandwidth.

2.2.5 Slew Rate Limitation

The slew rate is defined as the maximum rate at which the output changes when input signals are large. Slew rate limitation of an OTA comparator is given by,

$$f_p < \frac{I}{2 \cdot \pi \cdot V_p \cdot C} \tag{2.11}$$

where, f_p is the maximum frequency, V_p is the sinusoidal peak amplitude, C is the OTA compensation capacitance or load capacitance, and I is the OTA tail current. The slew rate can therefore put a maximum limit on the comparator large signal bandwidth.

2.2.6 Low-Power and Low-Voltage Design

The principle power dissipating elements in an ADC are the comparators (large number, requires low offset and must operate at high-speed), interstage gain blocks (pipelined ADCs), and resistor string (see section 2.2.1). Reference [15] discusses methods to reduce power dissipation and utilize low voltage supplies in flash ADC design. Some of the techniques reviewed are: 1) power minimization in switched capacitor gain blocks by operating on lower supply voltages, 2) implementation of transmission gates at low voltage, and 3) capacitor scaling.

Scaling down the process results in reduced V_{DD} and thus minimizes power consumption. Scaling however, has negative effects on analog circuit performance. The effect of scaling on SNR, GBP, and delay are discussed in [30]. For example, SNR is inversely proportional to 1/3rd power of scaling. Therefore reducing power supply to minimize power consumption may not always be possible since the decrease in SNR will affect analog circuit performance. It is note worthy to mention that it is nearly always power efficient to have larger power supplies to maintain the maximum SNR as opposed to having larger capacitors to reduce the noise floor [30].

Taking the above mentioned when designing improves ADC performance. These design considerations are summarized below.

- Implementing sound layout techniques such as common centroid, fingers, interdigitation, dummy devices and concentrating on layout compactness can reduce offset voltages due to device mismatching.
- Using switched capacitor circuits can further reduce the offset voltage by at least an order of magnitude or more. But improperly applied can introduce charge injection errors.
- Charge injection errors can be limited by the proper timing of switches including clock phase isolation, implementing fully differential and multistage circuits and by using dummy switches.
- Lack of attention given to the effects of parasitic RLC of the driver pads and transmission lines when designing for high-speed performance can limit the bandwidth.

- Having a low input capacitance has a positive effect on the bandwidth, slew rate and settling time. Is also relaxes driving requirements of input buffers thus resulting in low-power consumption and higher bandwidth.
- Minimizing mismatches in the external circuit of the ADC will result in a high dynamic range.
- An advantage of using an SOI/SOS process over bulk process is reduced parasitic capacitance.
- Scaling has advantages for digital circuits since this results in faster and more power efficient circuits. On the other hand analog circuits should be designed to operate in the longest channel length process that will achieve the ADC bandwidth specification [30].

This concludes the discussion on ADC design considerations. The next section discusses the factors that affect ADC accuracy. These factors are directly related to the above ADC design considerations.

2.3 Factors Limiting Accuracy

Among the factors that limit the accuracy of a flash ADC are static offset voltage, dynamic offset voltage, resistor string bow effect, and noise. Keep in mind that these factors are directly or indirectly related to the ADC design considerations discussed above.

2.3.1 Static Offset Voltage

Amplifiers and comparators on chip have an inherent offset voltage. This offset voltage known as the static offset voltage occurs due to mismatching of components, geometry, and threshold variations of the process. The static offset voltage is essentially modeled as a DC voltage at the input of the circuit. An equation for the static offset voltage at the input of a differential pair is derived in [37] and further simplified in [3] to obtain,

$$V_{OS} = [\pm\Delta V_T \pm \frac{1}{2}\cdot(\frac{\Delta\beta}{\beta})\cdot\Delta V \pm \frac{1}{2}\cdot(\frac{\Delta\beta}{\beta})\cdot\Delta V_T]\sqrt{N_P} \qquad (2.12)$$

where, N_p is the number of transistor pairs, ΔV is the gate overdrive voltage, and V_T and β are the standard notation. Equation 2.12 shows the dependency of V_{OS} on the process parameters β and V_T. Autozeroing [14][27] or Fowler trimming ([34] pp.103), and careful layout techniques such as common centroid, multiple transistor finger, and inter-digitation layout schemes can be used to minimize static offset voltage.

2.3.2 Dynamic Offset Voltage

Dynamic offset voltage is produced by charge injection (section 2.2.2). As already mentioned, charge injection occurs during transistor switching. Due to transistor and capacitor mismatching, paracitics, and threshold voltages (process dependent), two identically laid-out MOS devices can have slightly different charges in their inversion layers. During switching a charge injection mismatch and charge absorption mismatch occurs.

A number of techniques are used to minimize dynamic offset voltage. To minimize charge injection, the load capacitance can be made larger than the switch area. This will be at the expense of affecting the frequency response. Using large V_{gs} can reduce the effect of the threshold voltage but at the expense of increasing the power consumption due to decreased headroom. Reducing the clock voltage swing so that the switches are just turned on and off can reduce the clock voltage coupling effect but will slow down circuit performance and reduce dynamic range. Using fully differential implementation to take advantage of common mode rejection can also reduce clock feedthrough.

2.3.3 Resistor String Bow Effect

The resistor string resistance must be kept low to supply adequate bias currents to the fast comparators, which require the voltage reference to source large currents. A low-ohmic resistor string is presented in [35]. The input exhibits a signal-dependent input impedance (non-linear input impedance). This can be modeled as a signal dependent capacitance. SPICE simulation presented in reference [32] shows the input capacitance model by a constant 10pF fixed and a diode capacitance in parallel. The input capacitance varies from 16pF to 12.5pF as the input is swept form 0V to full scale voltage. The bow effect is due to the above mentioned non-linear input impedance. The bow effect introduces an increasing error to the comparator reference voltages as you move towards the center node of the resistor string [4]. Appendix A presents a short analysis of the resister string bow effect and resulting error.

2.3.4 Noise

There are two types of noise. They are interference noise and inherent noise ([2] p.181). The first is a result of unwanted interaction between the circuit and the outside world or between different parts of the circuits. Examples are ground bounce, crosstalk, and signal reflection and are discussed in detail in [23]. Careful circuit wiring and layout (guard rings, decoupling capacitors) are techniques used to reduce the interference noise and are discussed in detail in [23][24][25][26].

The other type of noise, inherent noise, is due to fundamental properties of the circuit. This type of noise can never be eliminated but can be reduced by using proper circuit structure or by increasing the power supply that makes the noise floor insignificant. Examples of inherent noise are thermal, shot and flicker noise.

Two major sources of noise in MOSFET transistors are flicker and thermal noise. The flicker noise (a form of dynamic V_{OS}) can be neglected at high-speed since it is inversely proportional to the frequency. The thermal noise is due to the resistance of the channel. The mean square value of the thermal noise in a MOSFET is,

$$\text{Noise Power} = \frac{8kT\Delta f}{3g_m} \tag{2.13}$$

where, k is the Boltzman constant, T is the absolute temperature, and Δf is the noise bandwidth. The constraints on g_m and C_L are,

$$g_m > \frac{8kT\Delta f}{3} \cdot \left(\frac{2^{n+1}}{V_{FS}}\right)^2 \tag{2.14}$$

and,

$$C_L > (\frac{16kT}{3\pi}) \cdot (\frac{2^{n+1}}{V_{FS}})^2 \quad (2.15)$$

The thermal voltage must be maintained less than ½ LSB. A large capacitor can be used for this purpose but this degrades the settling time and increases power consumption.

Having discussed the factors that limit ADC accuracy above, the next section discusses ADC specifications and test procedure to determine ADC performance characteristics.

2.4 ADC Specifications

There are many ways to specify ADCs. In industry, the definition of these specifications may vary according to company or research community. This is due to the fact that there are few standard ways to specify ADCs. Among the specifications discussed are ADC quantization error, monotonicity, missing code, resolution, Differential nonlinearity error (DNLE), Integral nonlinearity error (INLE), offset error, gain error, signal to noise ratio (SNR), effective number of bits (ENOB), dynamic range, SFDR (Spurious Free Dynamic Range), conversion time, and input bandwidth.

2.4.1 Quantization error

The transfer function of a typical 4-bit ADC is shown in Figure 2.5. The straight line represents the transfer function of an infinite accuracy ADC while the step function represents the transfer function of an ideal ADC. For a certain range of analog input, the

output digital code is the same for the ideal ADC. This results in a quantization error. If the difference between the infinite and the ideal transfer functions are taken, the result is a sawtooth plot shown in Figure 2.6. Notice that the maximum quantization error is +/- ½ LSB. The quantization error is inherent in all finite accuracy ADCs.

2.4.2 Monotonicity

The slope of the ADC transfer function should always be increasing. This means that as the input analog signal increases, the digital output never decreases resulting in monotonicity.

2.4.3 Missing Code

A code is missing if a digital output does not occur for any analog input.

2.4.4 Resolution

The resolution of an ADC is defined as the number of quantization levels the input signal is split into. For example, a 4-bit ADC has a resolution of 2^4=16.

2.4.5 Differential Nonlinearity Error (DNLE)

The DNLE is a measure of how much the step size of the actual transfer function

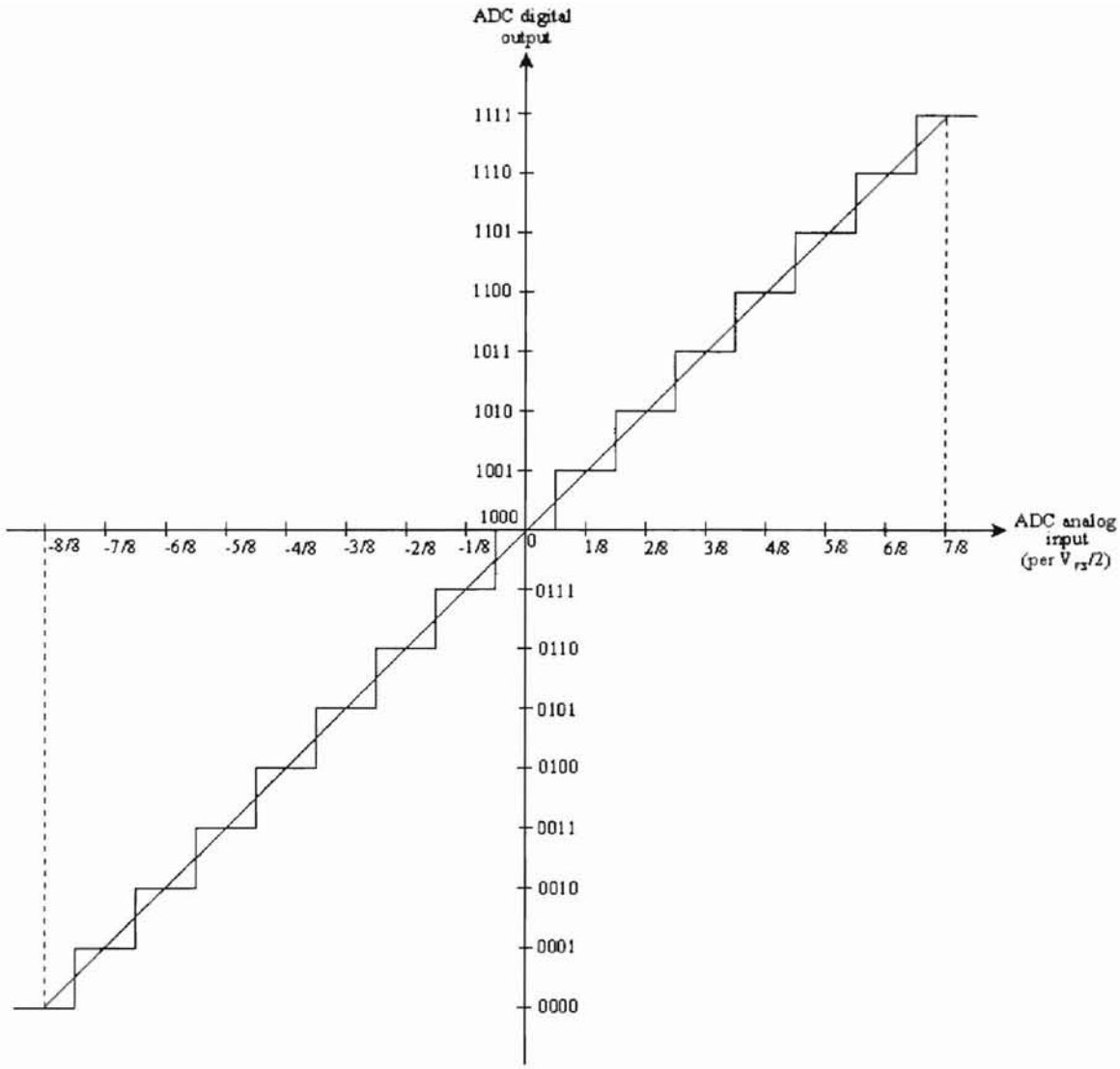


Figure 2.5 Transfer function (infinite accuracy and ideal) of a 4-bit ADC with bipolar power supply

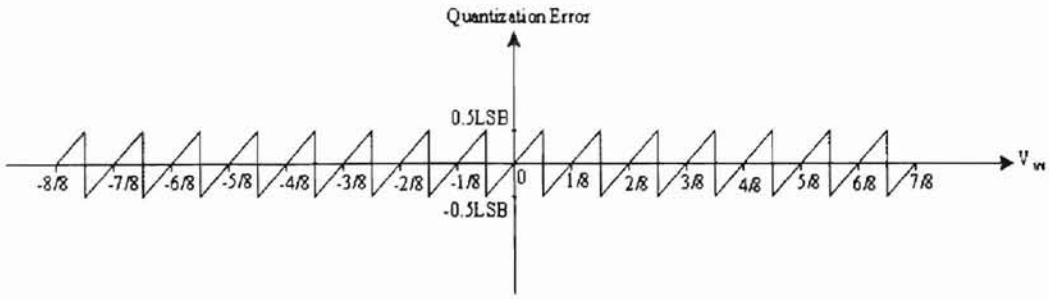


Figure 2.6 Quantization error of an ideal 4-bit ADC

deviates from the ideal transfer function. Each step of the actual transfer function is compared with the ideal step size. The difference is the DNLE.

$$\text{DNLE} = \text{Ideal code width} - \text{Actual code width} \tag{2.16}$$

The DNLE is also specified as the maximum of all the DNLEs of the codes. Figure 2.7 shows the DNL of a code. The ideal transfer function is the dash line while the actual transfer function is the solid line. Figure 2.8 shows how the quantization error is affected by DNL. The DNL produces an irregular saw tooth.

2.4.6 Integral Nonlinearity Error (INLE)

The INLE is the deviation of the midpoint of each step from the ideal location. Figure 2.7 shows the INLE given the ideal and actual transfer functions. Figure 2.8 shows the effect of INLE on the quantization error. The INLE can increase the quantization error by more than ½ LSB.

2.4.7 Offset Error

The offset error is the deviation of the first transition level of the actual transfer function from the ideal. Figure 2.9 illustrates this. If V_Z is the first transition level on the actual transfer function, and V_{ideal} is the first transition level for the ideal transfer function, the offset error is,

$$\text{Offset error} = V_Z - V_{ideal} \tag{2.17}$$

where, $V_{ideal} = 0.5\text{LSB}$.

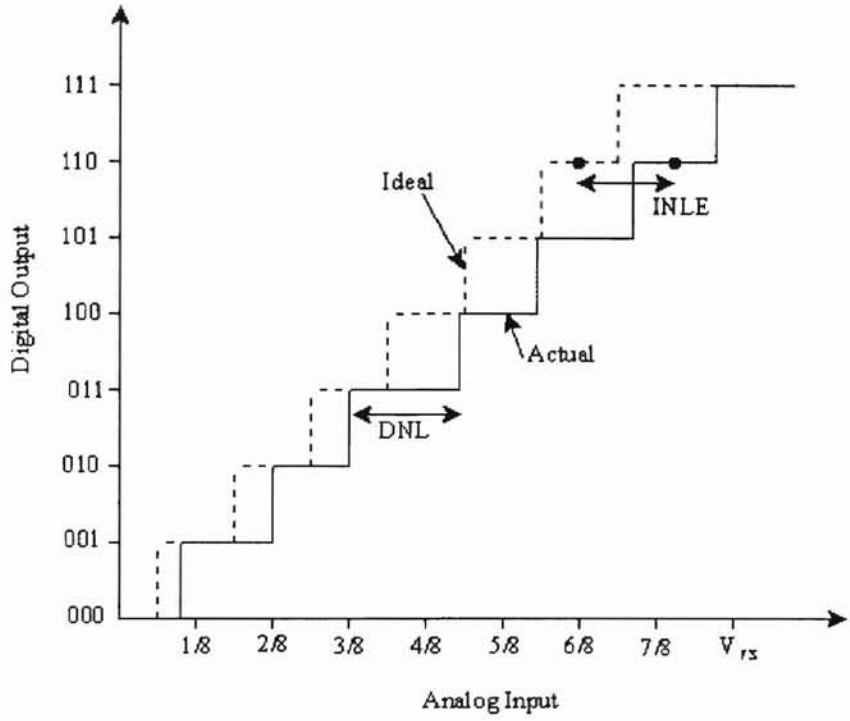


Figure 2.7 DNL and INL of an ADC

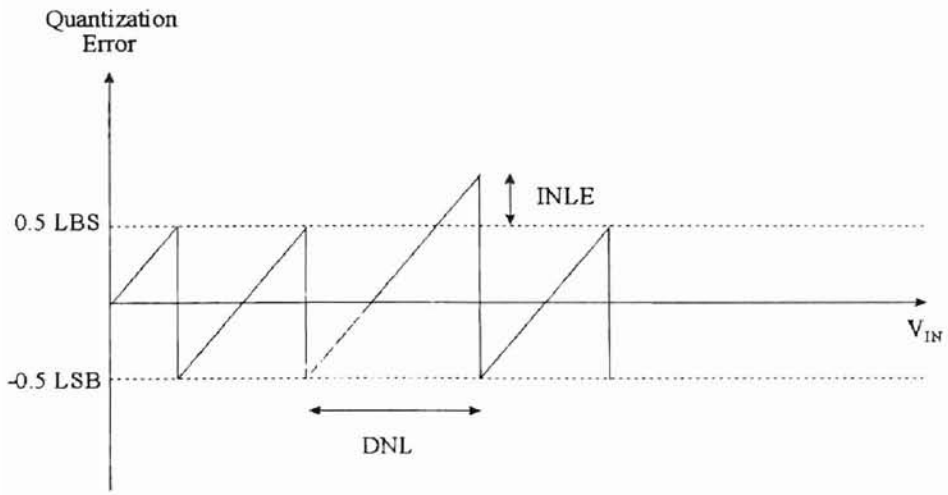


Figure 2.8 Effect of INL and DNL on the quantization error

2.4.8 Gain Error

The gain of an ADC is the slope of the transfer function. The gain error is the deviation of this slope to the ideal transfer function slope. The ideal slope is $V_{FS}/(2^n-1)$. There are various ways to define the slope of an ADC of which three are given below.

1) A best fit line through the code midpoints of the transfer function.
2) A straight line between the first and the last code midpoints.
3) Least error fit line.

The gain error is also specified by the deviation of the highest transition level on the transfer function (see Figure 2.10).

$$\text{Gain error} = V_f - V_{ideal} \tag{2.18}$$

where, V_f is the highest transition voltage and $V_{ideal} = V_R - 1.5LSB - \text{Offset error}$.

2.4.9 Signal to Noise Ratio (SNR)

The SNR is determined by taking a FFT of the output of the ADC for an input sinusoidal signal (see section 2.5). A pure sinusoidal input will undergo various changes as it propagates through the ADC. The distortion present at the output of an ADC with dynamic input, results from the inherent quantization error, DNL, INL, and noise. Distortion introduces extra frequencies into the output. SNR is the ratio of the magnitude of the fundamental frequency to the root mean square (RMS) of all other frequencies including harmonics. Due to quantization noise only, the SNR of an ideal N-bit ADC for a sinusoidal input is,

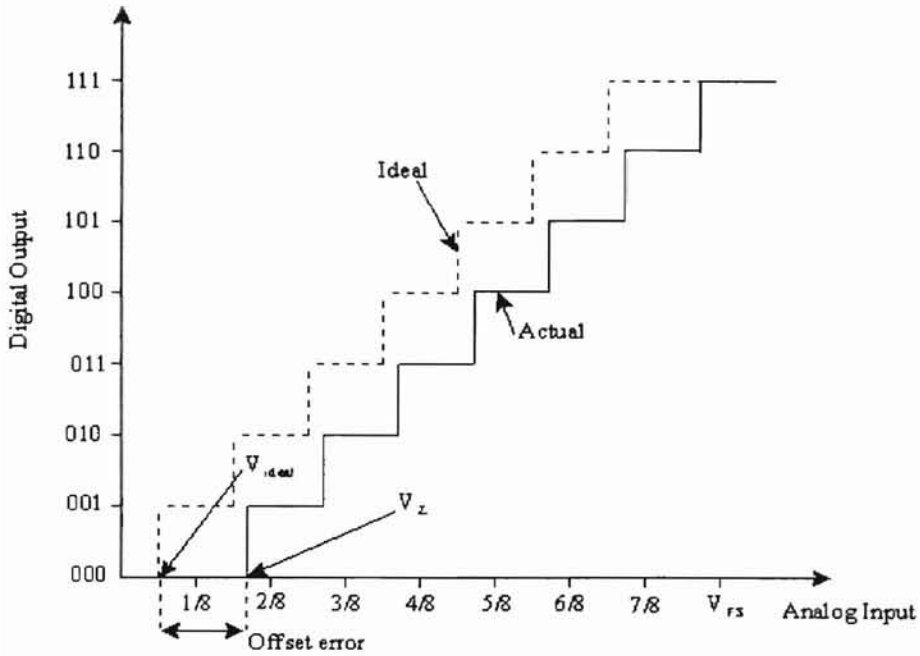


Figure 2.9 Offset error of an ADC

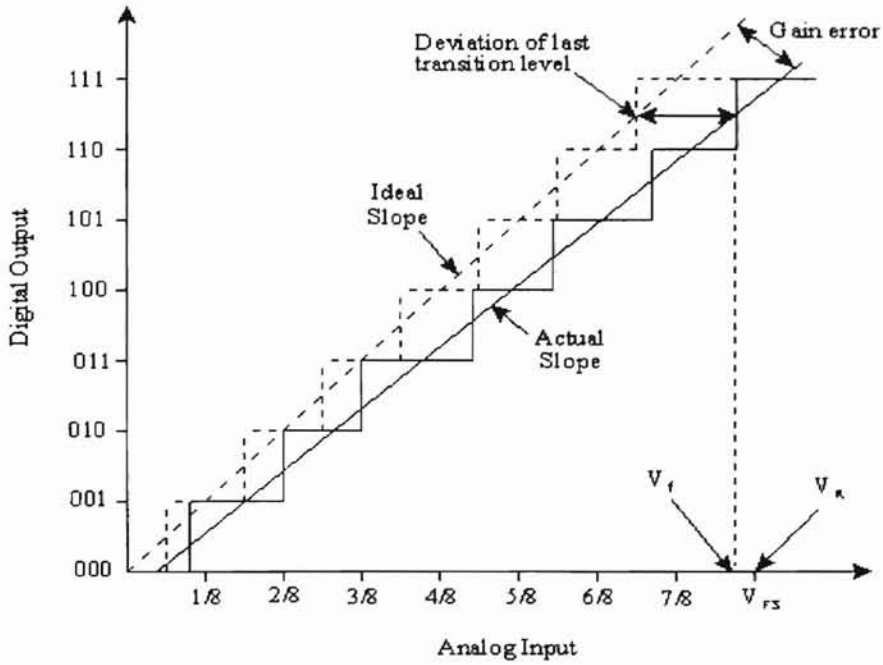


Figure 2.10 Gain error of an ADC

$$SNR = (6.02N + 1.76)dB. \tag{2.19}$$

2.4.10 Effective Number of Bits (ENOB)

The quantization noise is inherent in any ADC. Distortion caused by a non-linear transfer function can however reduce the theoretical SNR. An expression to calculate the ENOB which is N in equation 2.19 is,

$$ENOB = \frac{SNR(measured) - 1.76}{6.02}. \tag{2.20}$$

The ENOB is somewhat all-inclusive and includes the effects of both noise and distortion products [2][31].

2.4.11 Dynamic Range

The dynamic range of an ADC is specified as the ratio of the rms value of the full scale input sinusoidal signal to the rms output noise plus distortion measured [4]. Obtaining the RMS output noise plus distortion is obtained by taking a FFT of the output and eliminating the fundamental that represents the input signal frequency. The dynamic range is a function of the frequency of the input signal. This measurement is a good indication of an ADC dynamic performance.

2.4.12 SFDR (Spurious Free Dynamic Range)

The SFDR is the difference between the fundamental amplitude the largest

harmonic measured in dB ([31] pp.83-84). SFDR is shown in Figure 2.18(b). This measure is very important since it indicates ADC actual resolution over its operating frequency.

2.4.13 Conversion Time

The conversion time of an ADC is the time that a valid input takes to produce the corresponding digital word at the output. This is also known as the latency of the ADC.

2.4.14 Input Bandwidth

This specifies the highest input frequency of the analog input signal the ADC can convert while maintaining the specified performance characteristics.

Having introduced ADC specifications, the remainder of this chapter discusses test procedure to determine some of these specification and test procedures to characterize ADC performance.

2.5 Testing Procedures

This section discusses the testing of ADCs to determine some of the critical specifications mentioned in the previous section. It is important to note that the meaning of the specifications are closely related to how the test is performed and how the data is

extracted from the ADC. Testing procedures can be categorized as static and dynamic testing.

2.5.1 Static Testing

Applying a series of precision DC voltage levels is static testing. The ADC output is monitored. Static test can be used to determine the transition levels, DNLE, INLE, offset, and gain error of the ADC. The most common static test is the ramp test and is described below.

2.5.1.1 Ramp Test

The ramp test applies a high precision DC voltage that is usually produced by a DAC having a higher resolution than the device under test (DUT). The DC voltage is incremented in small steps at the input of the DUT. A block diagram of the test setup is shown in Figure 2.11. As the analog input is stepped through, the DUT will trip at a particular transition region between two adjacent output codes. This is repeated a number of times for the same transition region. When the DUT converts to the next code 50% of the time, the analog input voltage is recorded as transition level for that code [2]. Because of noise in the transition band (modeled in [33]), as the analog input is slowly incremented there is an increasing probability that the new code will be converted. Figure 2.12 shows results of such a test for two adjacent codes. In the plot shown, the vertical axis represents how often a code transition occurred for a particular analog input. The

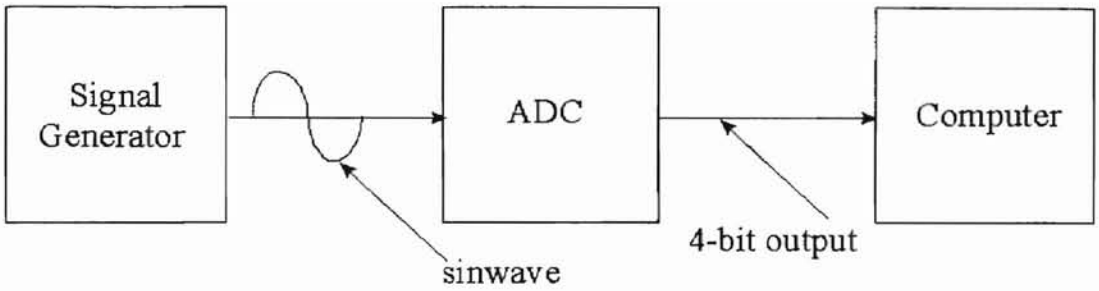


Figure 2.11 Block diagram of ramp test

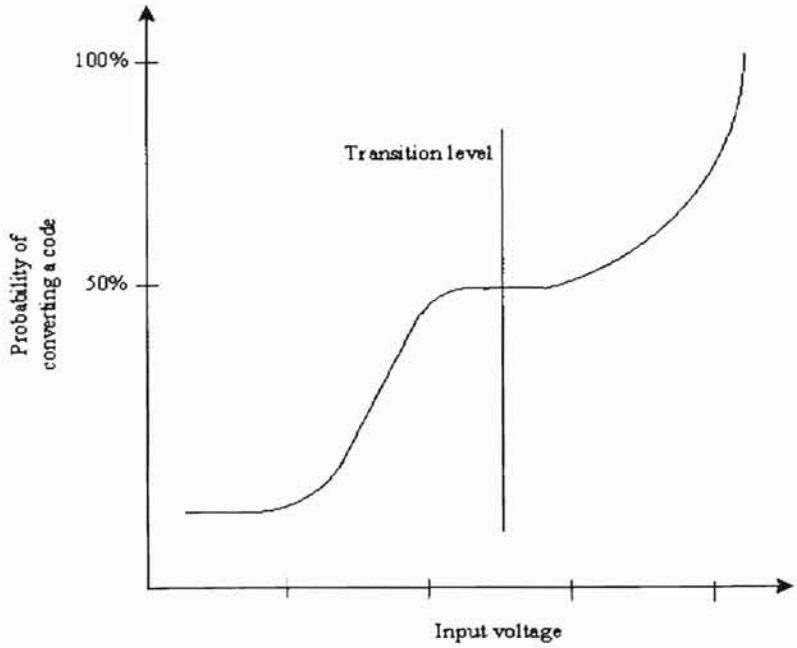


Figure 2.12 Ramp test results

width and shape of the curve depends on the noise when the input is near the transition level. Using this test, the transition level for each code can be determined. This data can now be used to generate a transfer function and thus determine DNLE, INLE, offset and gain error. Figure 2.13 shows the voltage transfer characteristic (VTC) of a 4-bit ADC that can be generated using the transition level data. The input voltage (Vin) is a ramp and the outputs D0 to D3 are the LSB to MSB respectively.

The static test described above is sufficient to determine DC performance. Another static test called the servo loop test is described in [1][2][7]. This test can provide for a high degree of accuracy and is readily automated.

Note that nonlinearities that are coupled into input signal bandwidth are not revealed by these tests. This is because the ADC may perform differently at different input signal frequencies, signal amplitudes, and sampling times. Dynamic tests take into consideration the above mentioned weaknesses of static testing.

2.5.2 Dynamic Testing

Dynamic testing [2][7][8] involves the use of periodic signals to determine ADC performance. Results from these types of tests give a better idea as to how the device would function under real conditions. In this section the histogram test and a test for determining spurious free dynamic range are discussed.

2.5.2.1 Histogram test

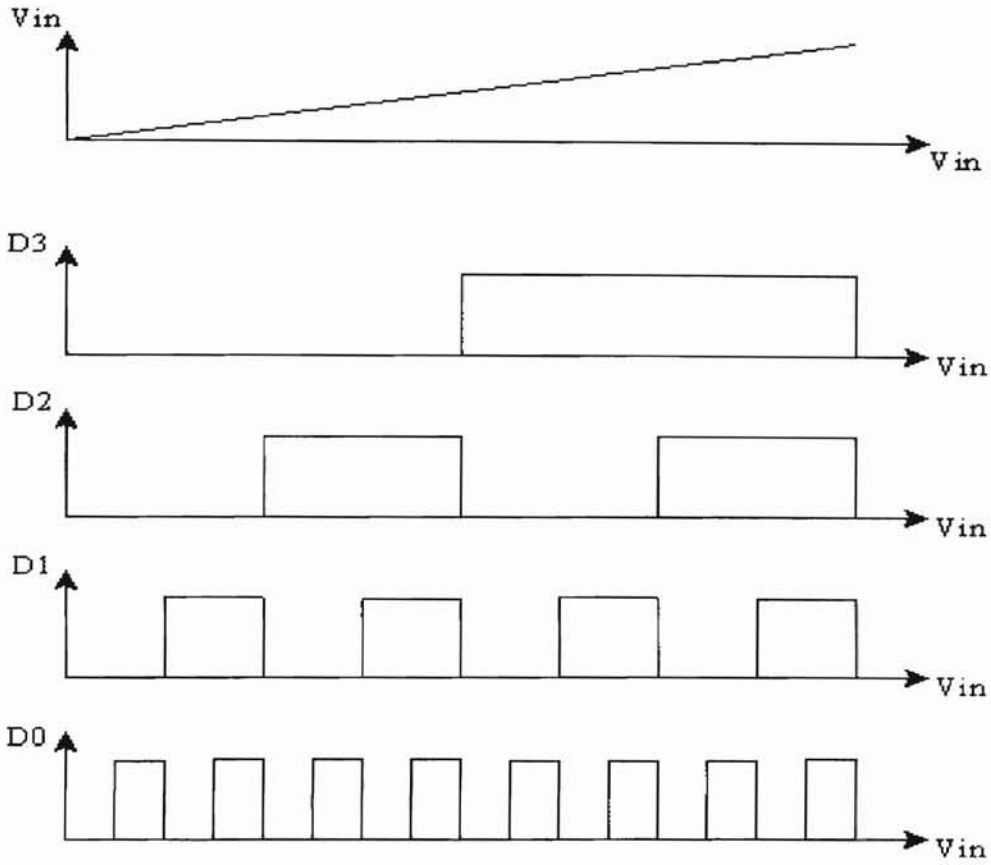


Figure 2.13 Voltage transfer characteristics (VTC) of a 4-bit ADC

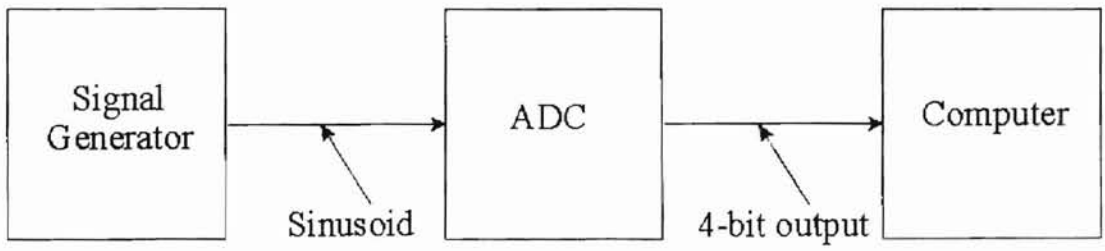


Figure 2.14 Histogram test setup

The histogram test [7][9] uses as input a full-scale sine wave with a specific frequency. This frequency must be non-coherent (see section 2.5.2.2) with the sampling rate of the ADC. The histogram software [7] counts the number of occurrences of a particular output code. A block diagram of the test setup is shown in Figure 2.14. A few things to take into consideration when executing this test are:

1) Since the input waveform must be predictable, it must not drift in amplitude, frequency or wave shape.
2) An integer number of periods should be sampled so that each code bin gets equal opportunity. It is recommended to collect at least 20,000 samples of data to insure measurement repeatability [7].
3) The input sine wave amplitude must exactly match the ADC input voltage range so that all codes are tested.

For each output code, a point is plotted whose height is proportional to total number of times the code occurred. For an ideal ADC, a sinusoidal input produces a cusp function [7] given by the following equation,

$$\Delta N_M = N_{per} \frac{f}{\pi f_S} \left[\sin^{-1}\left(\frac{m - 2^{n-1} + 1}{2^{n-1}} \right) - \sin^{-1}\left(\frac{m - 2^{n-1}}{2^{n-1}} \right) \right] \tag{2.21}$$

where, m is the ADC code bin number, ΔN_m is the number of occurrence of the code in the m^{th} bin, f is the input frequency, f_S is the sampling frequency, and N_{per} is the number of periods of data acquired. See Appendix C for the derivation of equation 2.21.

A sine wave changes more rapidly at its midpoint than at its high or low points. Therefore the input will spend a different amount of time at each code bin. This results in high counts for the high or low codes and low counts for codes at the middle. The

resulting plot of a histogram test for an ideal ADC is illustrated in Figure 2.15.

If the DUT has a missing code or a high DNLE, the resulting plot may look like the plot shown in Figure 2.16. For a missing code, there would be no count for that particular code and thus a zero count would result. If large spikes are present, this indicates large DNLE. The offset error can be detected by checking the symmetry of the curve about the ADC output code corresponding to mid scale. For a zero offset, it is symmetrical. Large gain errors can be detected by looking at the width of the histogram [7].

Also note that a triangular waveform can be used as the input. This will result in equal counts for all the codes since the time duration spent on each code bin is the same. The draw back with this method is that a triangular waveform cannot be made as spectrally pure unlike a sine wave.

2.5.2.2 Spurious Free Dynamic Range (SFDR) testing

The fast Fourier transform test [7][8] is very useful in determining ADC dynamic performance such as the SFDR. In this test a full-scale sinusoid with a particular frequency (single tone) is applied to the ADC input. Then the DFT (Digital Fourier Transform) of the resulting output is taken. If the number of output data points is a power of two, e.g. 1024, the FFT can be used to determine the DFT. Figure 2.17 illustrates a block diagram of the test setup.

The signal source generates a sine wave. The low pass filter is to ensure a spectrally pure sine wave is passed to the ADC input. The output of the 4-bit ADC is

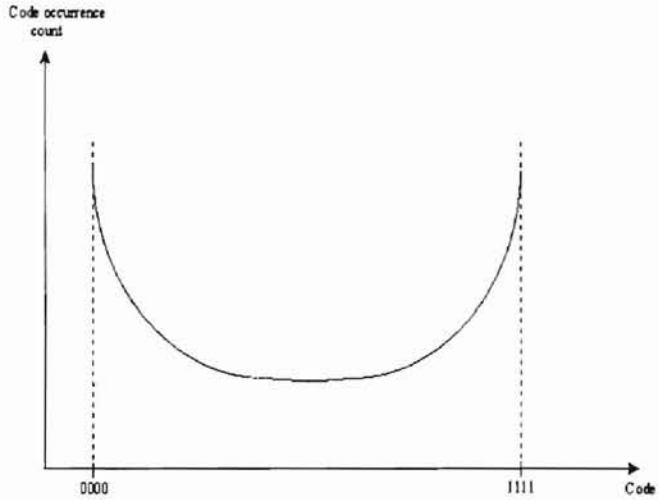


Figure 2.15 Histogram test result of an ideal ADC

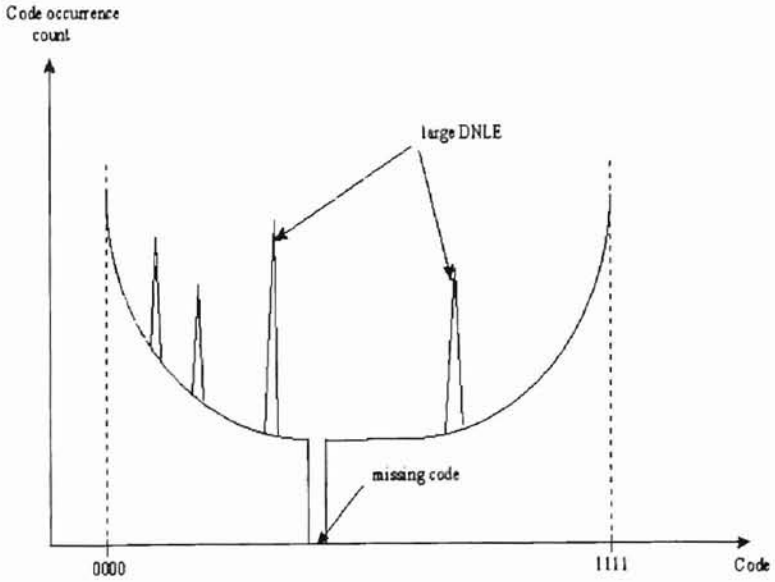


Figure 2.16 Histogram test result of an actual ADC

captured by the data acquisition system and then computer calculates the FFT. The computer should convert the 4-bit ADC output in to an analog signal or a higher precision DAC may be inserted between the 4-bit ADC and the computer in the test setup. Having acquired the data, the computer must pass it through a Hanning or Blackman window to minimize spectral leakage [7][10][33].

The FFT when plotted for an ideal ADC, the input frequency (fundamental) and noise due to quantization error will appear (Figure 2.18 (a)). If the ADC suffers from non-linearities, apart from the fundamental and quantization error, harmonics due to distortion also appear (Figure 2.18 (b)).

The signal to noise ratio can be calculated by,

$$\text{Signal to noise ratio} = 20\log\left(\frac{S}{N}\right) \tag{2.22}$$

where, S is the sum of the magnitudes of the spectral lines due to the fundamental and N is the sum of the magnitudes of the remaining spectral lines [7][20].

This test is very similar to the histogram test (2.5.2.1). The same precautions described for the histogram test must be taken for this test to be successful. In fact the same data obtained from the histogram test can be used. The input frequency is selected so that harmonics aliased into baseband, do not coincide with the fundamental [7]. As an example, values for input frequency may be 4.95MHz, 9.95MHz, or 14.95MHz if the sampling rate is 20MHz.

Apart from the above two dynamic tests, a few more tests such as the two (dual) tone, sine wave curve fitting, beat frequency, and the envelope tests are useful in determining ADC dynamic performance.

The dual tone test is identical to the single tone test described in section 2.5.2.2.

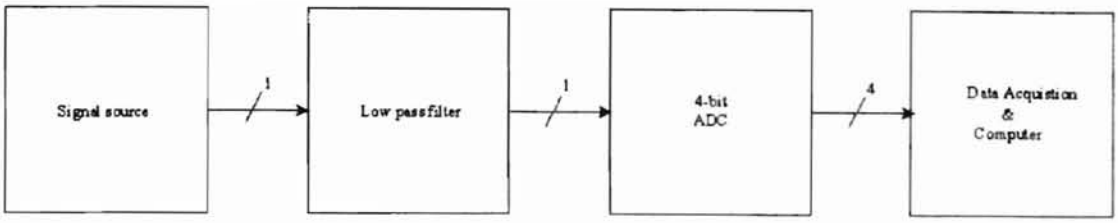


Figure 2.17 Block diagram of SFDR test setup

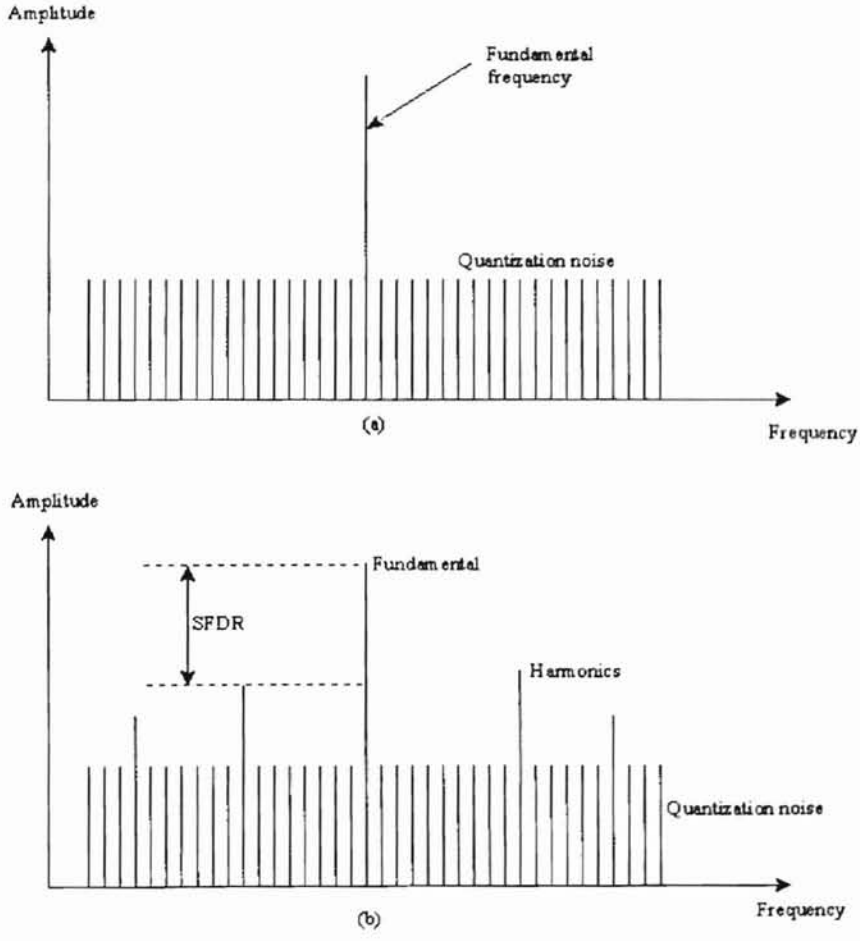


Figure 2.18 SPDR test (a) Output spectrum of an ideal ADC

(b) Output spectrum of an actual ADC

The only difference is that this test uses two input sinusoids instead of one. Both signals have equal amplitude but are at different frequencies. A single tone test for the latest high speed and high resolution ADCs becomes insufficient due to the need of a spectrally pure input that must always have a higher resolution than the DUT. This requires sophisticated and costly test and measurement instruments to implement the test. In addition a filter is required for each frequency used. Recently improved ADCs have exceeded measuring instrument's ability to test them. The two tone or dual tone test described in [18] and [19] can overcome the limitations of the single tone test that require high precision signal generators. Analysis show that the procedure used in [18] gives a more accurate ADC characterization than from a single tone test.

The sine wave curve fitting test can find the quantization error, DNLE, missing codes, INL, aperture uncertainty and noise of an ADC [7]. The beat frequency test is a qualitative test that can detect any gross problems with the ADC such as missing codes and DNLE [1][7]. The envelope test can be used as a qualitative measure of slewing ability and large signal bandwidth (section 2.2.5) in flash ADCs [1][7]. A good test plan to follow for characterizing an ADC using some of the tests described above is summarized below.

- The ramp test is useful to determine ADC specifications at DC. It is a good test to check ADC functionality. It has the added advantage of determining DNLE, INLE, offset, and gain error.
- Dynamic tests reveal ADC performance under real operational conditions.
- The histogram test is good to determine missing codes, DNLE, and offset error.
- The single tone and double tone tests are good to find the SFDR of the device under

test. This reveals the ADC ENOB, SNR, and resolution.

- The advantage of the dual tone test over the single tone test is that it doesn't require high precision measurement devices.
- Keep all test leads as short as possible to reduce ADC bandwidth limitation (see section 2.2.3). This will reduce the effect of transmission line impedance on the 3dB bandwidth.

This concludes our brief introduction into flash ADC architecture, design considerations, factors limiting accuracy, performance specifications, and testing procedures. The next chapter discusses the unique 4-bit flash ADC design features and steps taken to maximize performance.

CHAPTER 3

A 4-BIT FLASH ADC ARCHITECTURE WITH INHERENT REFERENCE STRING

This chapter introduces the 4-bit flash ADC design architecture. It includes discussion and analysis of all the sub-systems including unique design methods used to optimize ADC performance. Simulation results of the complete system using PSPICE are presented. Results from the testing of the 4-bit ADC design fabricated on MIT/LL 0.25μm, IBM 0.1μm, and Peregrine UTSi 0.5μm processes are also presented.

3.1 4-bit Flash ADC Architecture

The flash ADC is similar to that described in section 2.1. The design of each block is discussed in detail. They include the comparator bank, feed forward, bubble detector, encoders, and pad driver stages.

3.1.1 Comparator Bank Stage

The comparator bank is composed of inverters. The approach below describes a method for implementing an ADC comparator bank using geometry ratios to set each

individual comparator trip point. Thus the reference string is eliminated along with its associated power consumption. The fabrication of a bank of 2^n-1 of these comparators results in a classical n-bit flash ADC, which has an inherent embedded reference string. The inherent internal reference is set by properly scaling the inverter geometry. This approach is directly applicable for use in both multistage feed forward and regenerative comparator designs. We will however limit our discussion to feed forward comparator designs. As a direct result of the reference string elimination, the resulting ADC 1) operates on lower power, 2) avoids the distortion associated with the resistor string bow effects (section 2.3.3), and 3) no longer requires accurate resistor and/or capacitor elements. Quantization accuracy now depends to a first order on transistor area and local or side-by-side transistor matching to achieve monotonic voltage conversion. As a result of this and the low-power features of CMOS, analysis suggest fabrication of flash ADCs with 8-bit accuracy.

3.1.1.1 Geometrically Setting Inverter Trip Voltage

The quantization of the input signal is possible by geometrically setting inverter trip voltages. For an inverter operating in velocity saturation both N and PMOS currents are equal when the input voltage is at the trip voltage of that inverter. Now for $V_{TN}+V_{TP}=V_{OS}$, and $V_{SS} = -V_{DD}$ and solving for V_{TRIP},

$$V_{TRIP}= \left(V_{DD} - V_{TN}\right)\frac{\left(W_p k_p - W_n k_n\right)}{\left(W_p k_p + W_n k_n\right)} + \frac{V_{OS} W_p k_p}{\left(W_p k_p + W_n k_n\right)} \qquad (3.1)$$

where, k_n and k_p are the mobility constants or transconductance per mm for N and PMOS transistors in velocity saturation respectively, and W_P and W_N are the width of the N and PMOS transistors of the inverter respectively. The detailed derivation of equation 3.1 is found in Appendix D.

Failure of the sum of V_{TN} plus V_{TP} to not equal zero results in a DC offset V_{OS}. This ADC design approach takes advantage of the near linearity of the large signal output characteristics of CMOS transistors in velocity saturation, the low device area cost, and the low-power properties of CMOS inverters. Using equation 3.1 and solving for the trip voltage difference between two neighboring comparators, in code position,

$$\Delta V_{TRIP} = \frac{V_{FS}}{2^n} = 2K_R \frac{(V_{DD} - V_{TN} + V_{OS}/2)(W_{p_{m+1}} W_{n_m} - W_{p_m} W_{n_{m+1}})}{(K_R \cdot W_{p_m} + W_{n_m})(K_R \cdot W_{p_{m+1}} + W_{n_{m+1}})} \tag{3.2}$$

where, $K_R = k_p/k_n$ and V_{OS} is the equivalent offset of the inverter due to all mismatch error sources, V_{FS} is the full-scale input voltage of the ADC and m represents the mth comparator. See Appendix D for the derivation of equation 3.2.

The V_{OS} mismatch of moderate sized in area, side by side inverters, exclusive of the designed in threshold mismatch is typically less than 4-10mV. The key to controlling threshold mismatch is device area and maintaining devices in close proximity. It is noteworthy from equation 3.2 that V_{OS} and the overdrive bias V_{DD} - V_{TN} are both scaled to a first order with the changes in transistor geometry. From the above equations it is readily observed that both ΔV_{TRIP} and V_{TRIP} are controlled by transistor widths. Since the geometry is unique for each inverter, monotonicity can be guaranteed as long as side by side inverters in the thermometer code are physically maintained in close proximity at layout. This ensures device matching such that local mismatch does not exceed the

designed in or desired ΔV_{TRIP} derived from equation 3.2. Implicit in this is that to the degree one is willing to spend area as a resource affects the number of designed bits which can be achieved with a resulting increase in power consumption.

Figure 3.1 shows the PSPICE simulation of the voltage transfer characteristic or thermometer levels for the 4-bit ADC without encoding demonstrating the validity of the previous analysis. The individual comparators were sized using equation 3.1 and 3.2.

3.1.1.2 Power Consumption Advantage

Power dissipation is proportional to the input frequency and the number of quantization levels. For example if a sine wave is applied to the input of an n-bit comparator all 2^n-1 feed forward comparators will trip twice every cycle or

$$P \quad \alpha \quad f_B\left(2^n - 1\right)C_L V_{DD}^2 \tag{3.3}$$

where, f_B is the ADC bandwidth or half the Nyquist rate, C_L is the load capacitance, and V_{DD} is the power supply voltage. Power consumption is proportional to the reference voltage, input frequency, and grows exponentially with the desired resolution. It is important to note that power is directly proportional to the bandwidth of the applied signal and approaches zero with no input activity. This serves to further improve the overall ADC efficiency. The main improvement considering the power consumption is that there is no static power dissipation at the front end of the ADC but there does exist dynamic power dissipation. The advantage of this over a resistor string in now clear. Resistor strings have static as well as dynamic power dissipation.

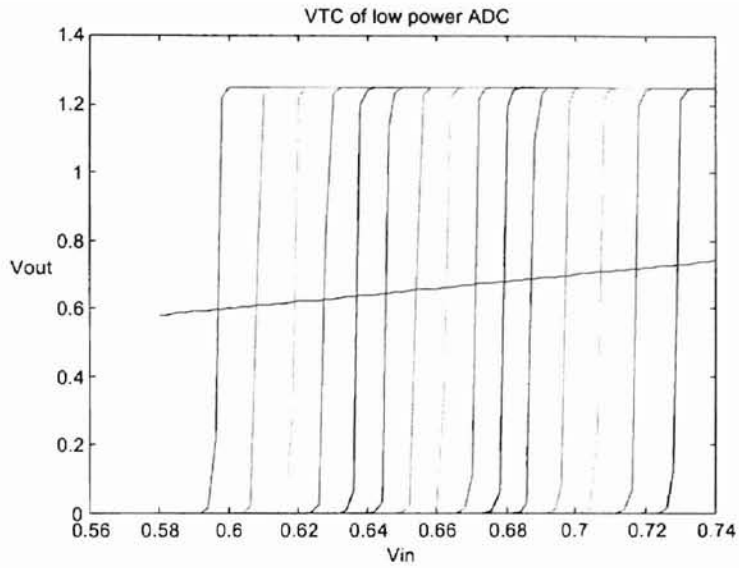


Figure 3.1 Comparator bank inverter VTCs

3.1.2 Feed Forward Stage

Each comparator with its unique trip point (based on specific required geometry differences) can be laid-out using 2 to 5 inverters in series resulting in a feed forward comparator with a unique trip point. The input inverter in each comparator is sized using the above equation 3.1 and 3.2 while the remainder are "beta" matched inverters with a trip voltage at $(V_{DD} + V_{SS})/2$ and are required to ensure sufficient comparator gain (see Figure 3.2). The total gain of the feed forward stage can be written as,

$$A_T = {V_{PP}}/{2^{n+1}} \approx \mu^S \tag{3.4}$$

where, V_{pp} is the peak to peak input voltage, s is the total number of inverter stages in series, μ is transistor self gain, and n is the number bits in the quantizer or ADC. This results in an n-bit quantizer ADC having 2^n-1 unique comparators.

The output of the comparators may not always have exact logic levels. A valid logic level has to be applied to the bubble detectors if the ADC is to function properly. The feed forward stage of the flash ADC amplifies the output of the comparators to obtain a valid logic level. The gain A_{inv} of a single inverter is given by,

$$A_{inv} = \frac{g_{m_n} + g_{m_p}}{g_{o_p} + g_{o_n}} \tag{3.5}$$

For the case of the MIT model, the above gain, A_{inv}=6. If the input to the feed forward stage is 30mV and we require an output from this stage of 1V, the overall gain is, 1V/30mV = 33. This requires $\ln 33 / \ln 6 \approx 2$ inverters in series in the feed forward stage. It has been shown ([4] pp.315-317) that the time constant through n inverters in series is,

$$\tau_{total} = 2 \cdot n \cdot A_v \cdot \tau_T \tag{3.6}$$

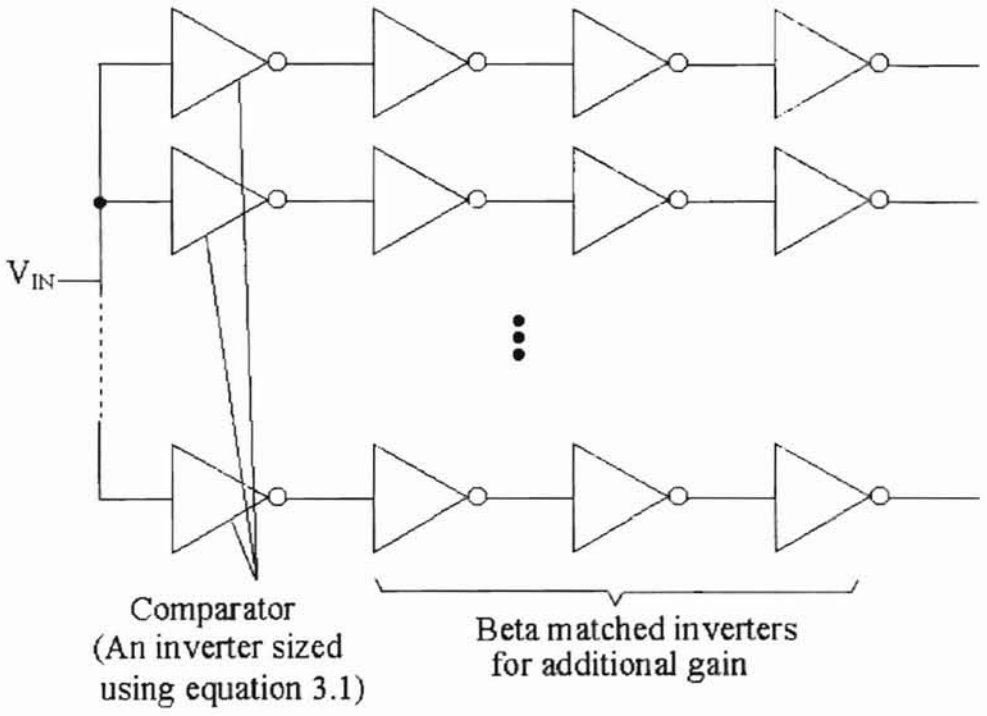


Figure 3.2 Comparator and feed forward stage of 4-bit ADC

where,

$$\tau_T = \frac{C_{gs}}{g_m}$$

with C_{gs} being the input gate capacitance of inverter and g_m the small-signal transconductance of the inverter. Let $g_m=g_{mn}+g_{mp}=160\mu S$, $C_{gs} = C_{gsn}+ C_{gsp}=2fF$, n=2 and $A_v=6$ then,

$$t_{delay} = 2.2 \cdot \tau_{total} = 0.66ns$$

Therefore the time required for the output of comparator stage to reach a valid logic level in worst case situation is 0.66ns. This can also be considered as the feed forward stage delay.

3.1.3 Bubble Detector

The bubble detector finds the boundary of the thermometer code output of the reference less comparator bank. This boundary is where the thermometer code changes from being all 1's to all 0's and it indicates the voltage level to be digitized. Let A_{n-1} be the top most output to have a logic '1' indicating the transition point. Let A_n be the next output above A_{n-1} and A_{n+1} be the next output above A_n. The truth table of the logic function for boundary detection is shown below.

A_{n+1}	A_n	A_{n-1}	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Table 3.1 Truth table for bubble detector with error correction

Looking at Table 3.1, the output Y is high only when $A_{n+1}A_nA_{n-1}$ = '001' thus indicating the thermometer code boundary. The other possible ideal cases are when $A_{n+1}A_nA_{n-1}$ = '000' or '111' in which case the boundary does not exist and '011' in which case the boundary exists but is at incorrect place for detection. For these cases the output Y is set to '0'. The rest of the cases are errors that can occur in the thermometer code. For all these non-ideal cases, the output Y is again set to ' 0'.

The resulting Boolean function is given by,

$$Y = A_{n-1}\overline{A}_n\overline{A}_{n+1}. \tag{3.7}$$

Further manipulation of equation 3.7 gives,

$$\overline{Y} = (A_{n-1}\overline{A}_n\overline{A}_{n+1})'. \tag{3.8}$$

The above Boolean simplification represents a three input NAND gate having inputs of A'_{n+1}, A'_n and A_{n-1}. Transistor level implementation of this circuit is shown in Figure 3.3. Note that an inverter is connected to the NAND gate output to obtain Y.

Although this circuit has error correction ability, increasing the number of inputs can further increase accuracy of boundary point detection at the expense of increasing load capacitance and delay. The advantage of using the NAND gate is that the pull up circuit is three PMOS devices in parallel that can compete with the pull down circuitry with minimum area consumed by the PMOS devices. Note the three NMOS devices in series increase the pull down time of the circuit and that means that the PMOS devices do not need to have large area to obtain the same speed.

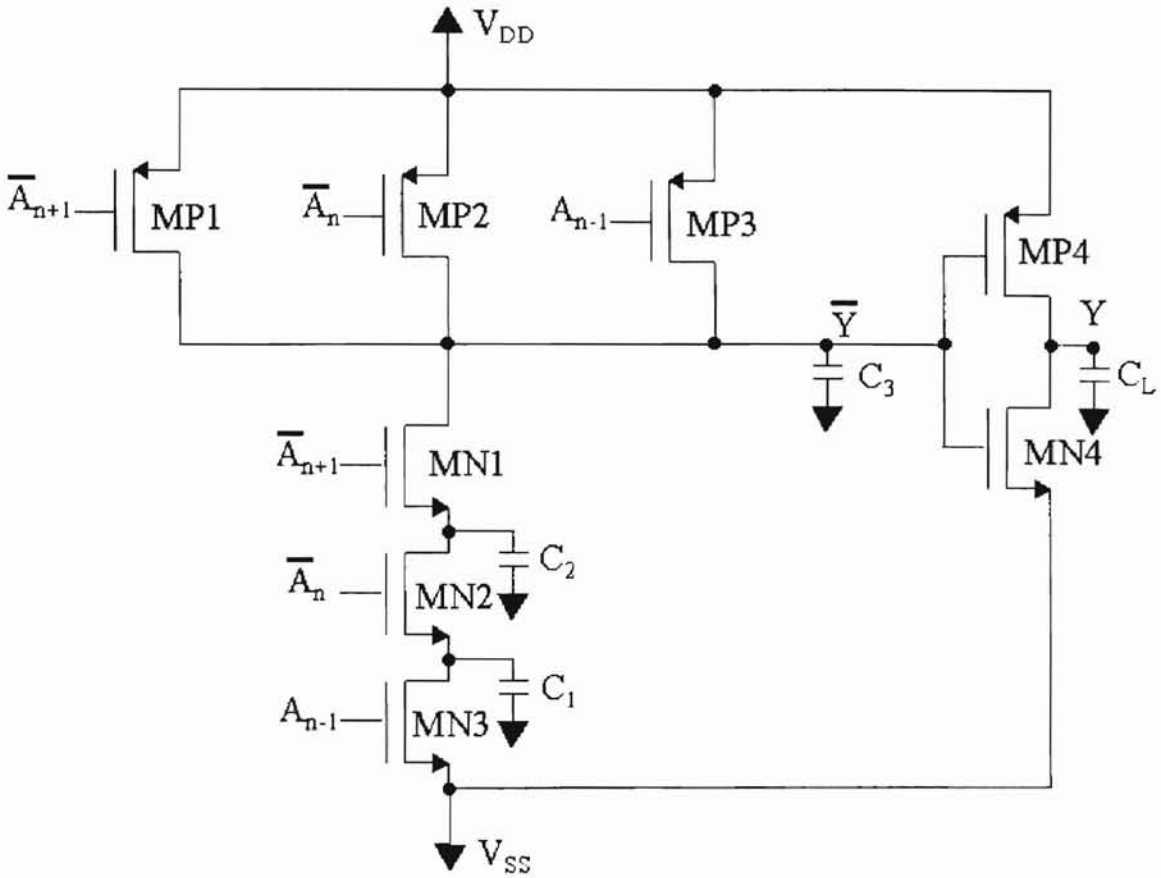


Fig 3.3 Bubbled detector boundary detection circuit

3.1.3.1 Bubble Detector Delay Analysis

The circuit shown in Figure 3.3 is now analyzed to determine its delay properties. The worst-case rise time delay occurs when the inputs $A_{n+1}A_nA_{n-1}$ changes from '000' to '001' respectively. Using the Elmore delay theorem [38], the rise time delay (t_{dr}) is,

$$t_{dr} = 2.2\left[R_{N1}C_3 + R_{N2}(C_2 + C_3) + R_{N3}(C_1 + C_2 + C_3) + R_{P4}C_L\right] \tag{3.9}$$

The worst-case fall time delay (t_{df}) occurs when the inputs $A_{n+1}A_nA_{n-1}$ change from '001' to '000' respectively. Using the Elmore delay theorem the fall time delay is,

$$t_{df} = 2.2\left[R_{P1}(C_1 + C_2 + C_3) + R_{N4} \cdot C_L\right] \tag{3.10}$$

where, R is the on-resistance of the transistor. The capacitance C_1, C_2, C_3 and C_L are the equivalent load capacitance at the nodes shown in Figure 3.3. The delay (t_d) can be found by using the equation,

$$t_d = \frac{t_{dr} + t_{df}}{2}. \tag{3.11}$$

Looking at equation 3.10, we see that MP1 must charge three capacitors. To further improve circuit performance, sizing MP1 larger than the other two PMOS will reduce its on-resistance and thus reduce the worst case rise time. This situation also applies for NM3 since it has to discharge three capacitors (see equation 3.9). A suggestion is to size the width of MP1 three times that of the other two PMOS devices and MN2 and MN3 twice and three times that of MN1 respectively, assuming C_1=C_2=C_3.

3.1.3.2 Detection of Overflow and Underflow

The block diagram of Figure 3.4 shows how the feed forward stage is connected to the bubble detector stage. Notice how Q and Qbar of each level of the feed forward stages are connected to A_n, A'_{n-1}, and A'_{n+1} inputs of the AND gate. Also note the two extra feed forward blocks at the extremes shown in dashed squares. These two blocks detect overflow and underflow. The overflow and underflow circuits result in the all bubble detector outputs going low, i.e. '000...0' if the input voltage moves out of the range of the supply voltage rails. The effect of this is to freeze the encoder outputs at its previous value.

3.1.4 Encoder Stage

A single encoder is a regenerative type circuit. Its advantage is high gain and fast operation due to regeneration. Figure 3.5 shows the circuit diagram of an encoder. For a 4-bit flash ADC four of these encoder circuits are arranged as shown in Figure 3.6 to obtain an output digital word. Each block contains an encoder circuit of Figure 3.5. In Figure 3.6, the top most encoder produces the LSB and the bottom most encoder produce the MSB. The way in which the the NMOS gates of the each encoder are connected define its binary weight. The bubble detector outputs are connected to the NMOS gates of each encoder as shown (black dot denotes a connection) in Figure 3.6. The bubble detector output generates a uniques address for each quantization level that when applied to the encoders produces a binary word. Consider the MSB encoder. The upper half of the bubble detector outputs are connected to 8 NMOS devices to the left side of an encoder. The lower half of the bubble detector outputs are connected to the other 8 NMOS devices to the right side of the encoder. In this configuration the MSB encoder

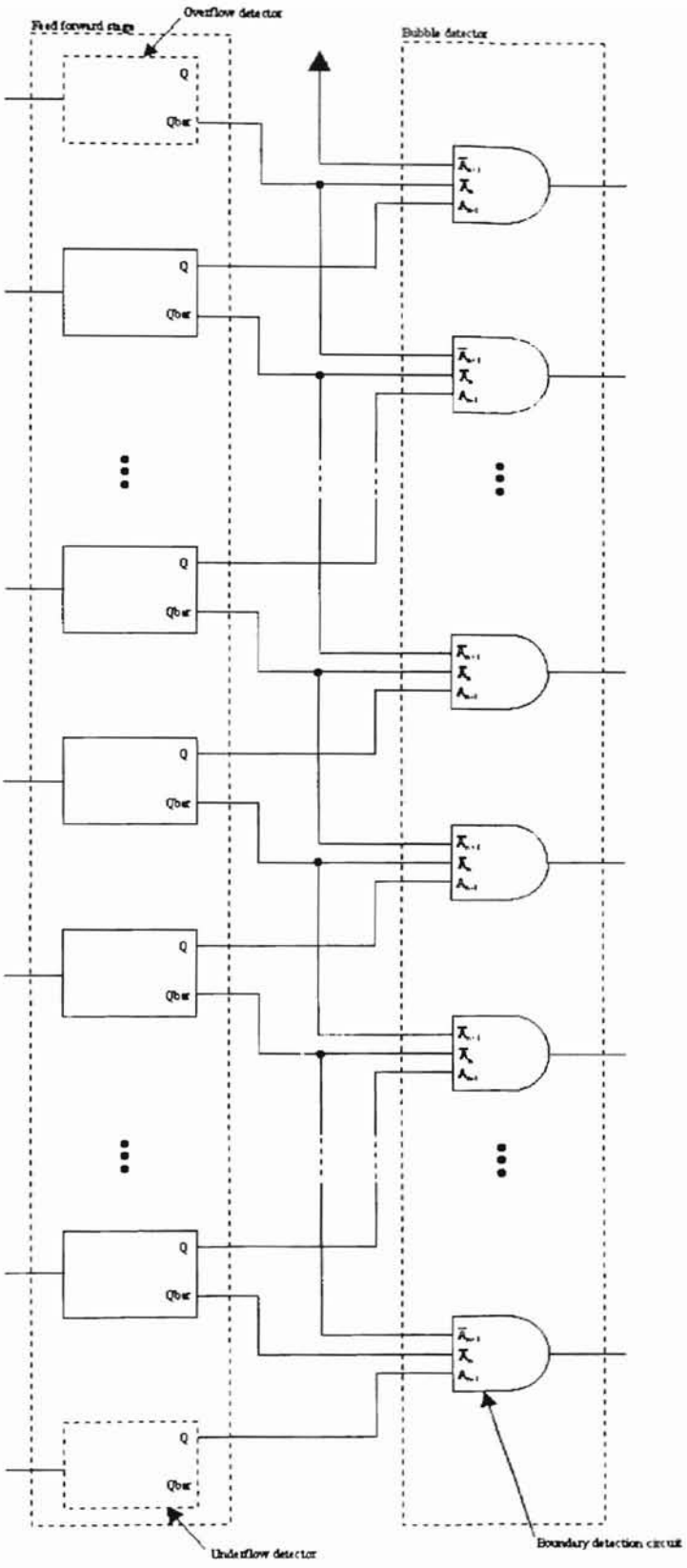


Figure 3.4. Overflow and underflow of 4-bit ADC

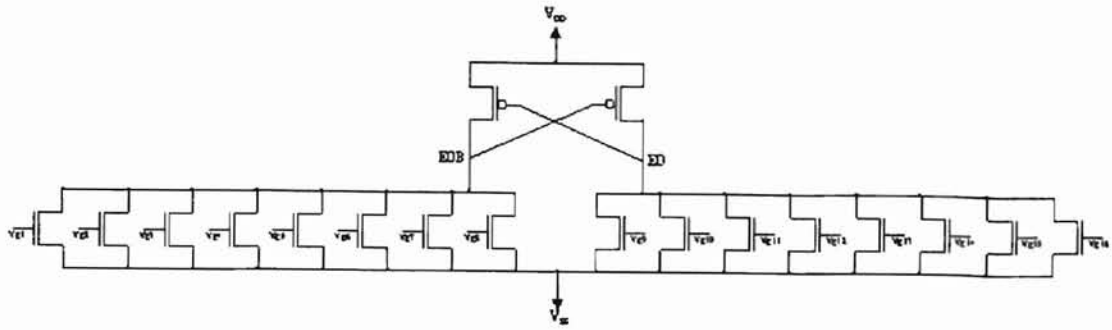


Figure 3.5 A single encoder

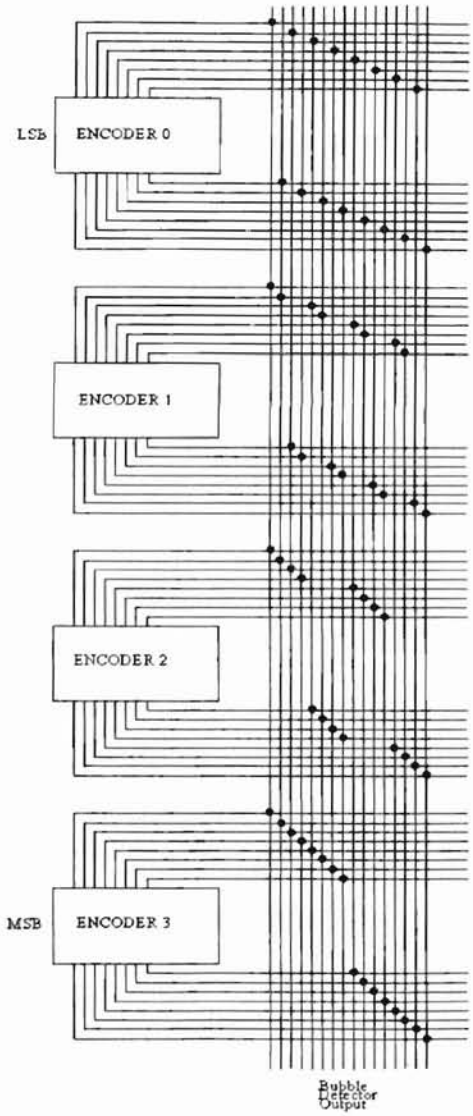


Figure 3.6 Encoder connections that produce a binary number

output is high only when one of the upper half of the bubble detector outputs is high. If a lower half bubble detector output is high, the MSB encoder output is low. This particular arrangenent in which the connections to the gates are made produce a 4-bit binary word. Depending on what side the output is taken, the non-inverted (EO) or an inverted output is available (EOB) (see Figure 3.5). Either one of these outputs or both can be used as the inputs to a pad driver.

Test results from the MIT/LL OSU chip 1998 concluded that the encoders leaked owing to short channel effects. In order for this problem to be minimized, two steps have been taken. 1) Increase channel length. This will reduce short channel effects such as leakage but at the expense of sacrificing speed. 2) Resize PMOS and NMOS in the encoder circuit. This counteracts the leakage through the NMOS devices. This will make the pull up stronger by charging the load capacitor more than the leaking NMOS transistor can discharge. This can prevent the load capacitance from eventually discharging completely and thus giving error values.

3.1.5 Pad Driver

The pad driver function is to drive the large pad capacitance and/or external circuitry. The encoder is incapable of performing this task since its driving ability is low. A tappered buffer design discussed in [36] is used having an optimized delay. The pad driver developed for our application has 6 stages. The pad driver circuit is shown in Figure 3.7.

It uses two inputs Vin and Vinb. These inputs are connected directly from an encoder (EO and EOB). Using two inputs instead of one to drive the pad driver reduces

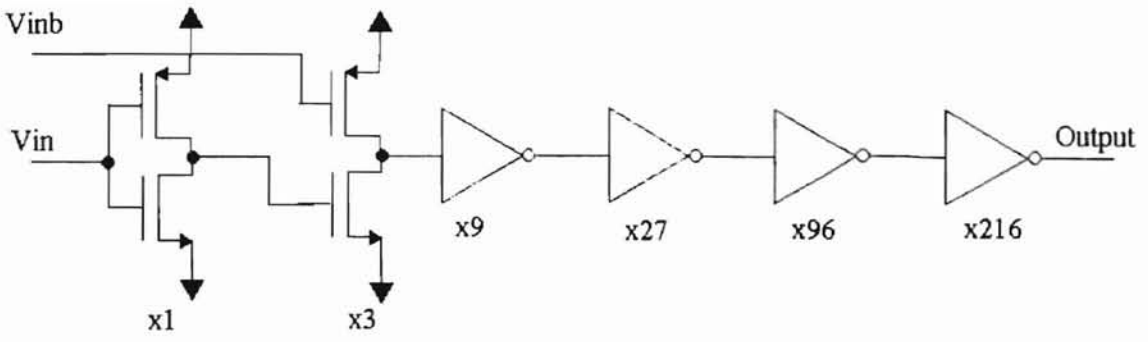


Figure 3.7 Six-stage pad driver

error and loading effects. Also shown in Figure 3.7 are the device scaling factors. For example, the 2nd stage is 3 times while the 5th stage is 96 times wider than the 1st stage respectively. The scaling factor of 3 (a_{opt}=2.718 [36]) is only used for the first four stages. A scaling factor of 4 was used for the last two stages, merely to obtain a good layout shape for the pad driver.

This concludes the detailed discussion of the 4-bit flash ADC sub systems. The next sections present simulation and test results of the ADC.

3.2 4-bit Flash ADC Simulation Results

The simulation results of the 4-bit flash ADC are presented below for DC and transient analysis. Peregrine UTSi 0.5μm process device model was used for the simulation. This process has a f_t of 18GHz.

3.2.1 DC Analysis

The VTC curves of the comparators (feed forward stage outputs) are shown in Figure 3.8. The supply voltages were V_{DD}=3.6V and V_{SS}=0V. Note that the input voltage ramp swing is approximately between 1.35V and 2.55V for all of the comparators to switch and the difference in voltage of two consecutive trip point is about 100mV (ΔV_{TRIP} in equation 3.2). Figure 3.9 shows the input DC voltage sweep of the 4-bit flash ADC. This confirms the functionality of the converter. Note that VD3 through VD0 are the MSB through LSB outputs respectively.

3.2.1 Transient Analysis

A transient simulation was done to establish the maximum operation speed of the ADC. Figure 3.10 shows this result. The input was a triangular waveform of period 38ns (f=26MHz) having a voltage swing between –0.47V and 0.79V. For this simulation, V_{DD} and V_{SS} were set at 1.8V and -1.8V respectively for all the stages including comparator bank and feed forward stages, bubble detector and encoder stages, and pad drivers. Some important ADC performance data obtained from simulation are summarized below.

- ΔV_{TRIP} = 78mV
- Total delay = 1.441ns
- Maximum operation speed = 694MHz
- Power consumption,

  without pad driver = 448mW @ 694MHZ

  with pad driver = 457mW @ 694MHZ

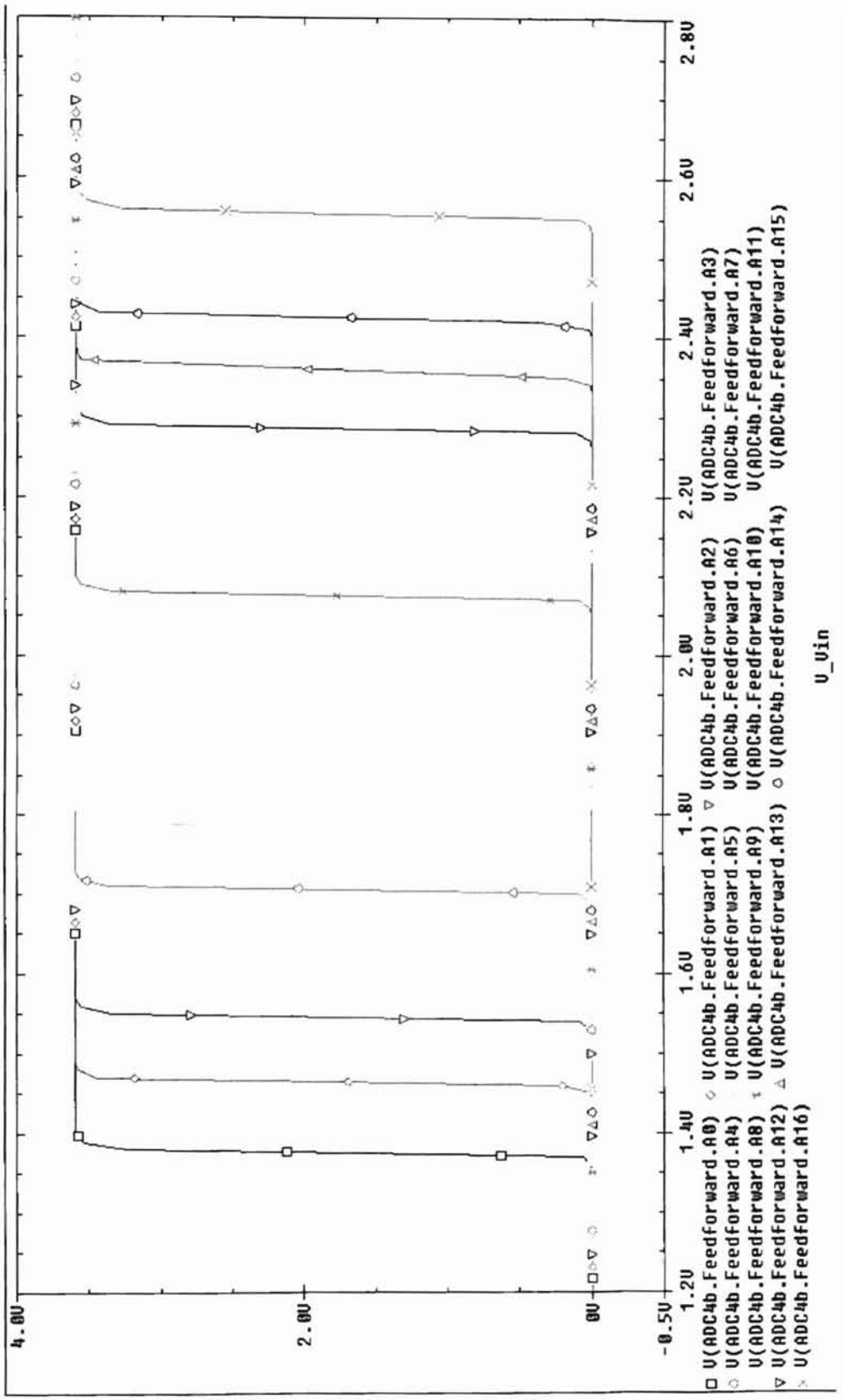


Figure 3.8 VTC curves of comparator bank inverters

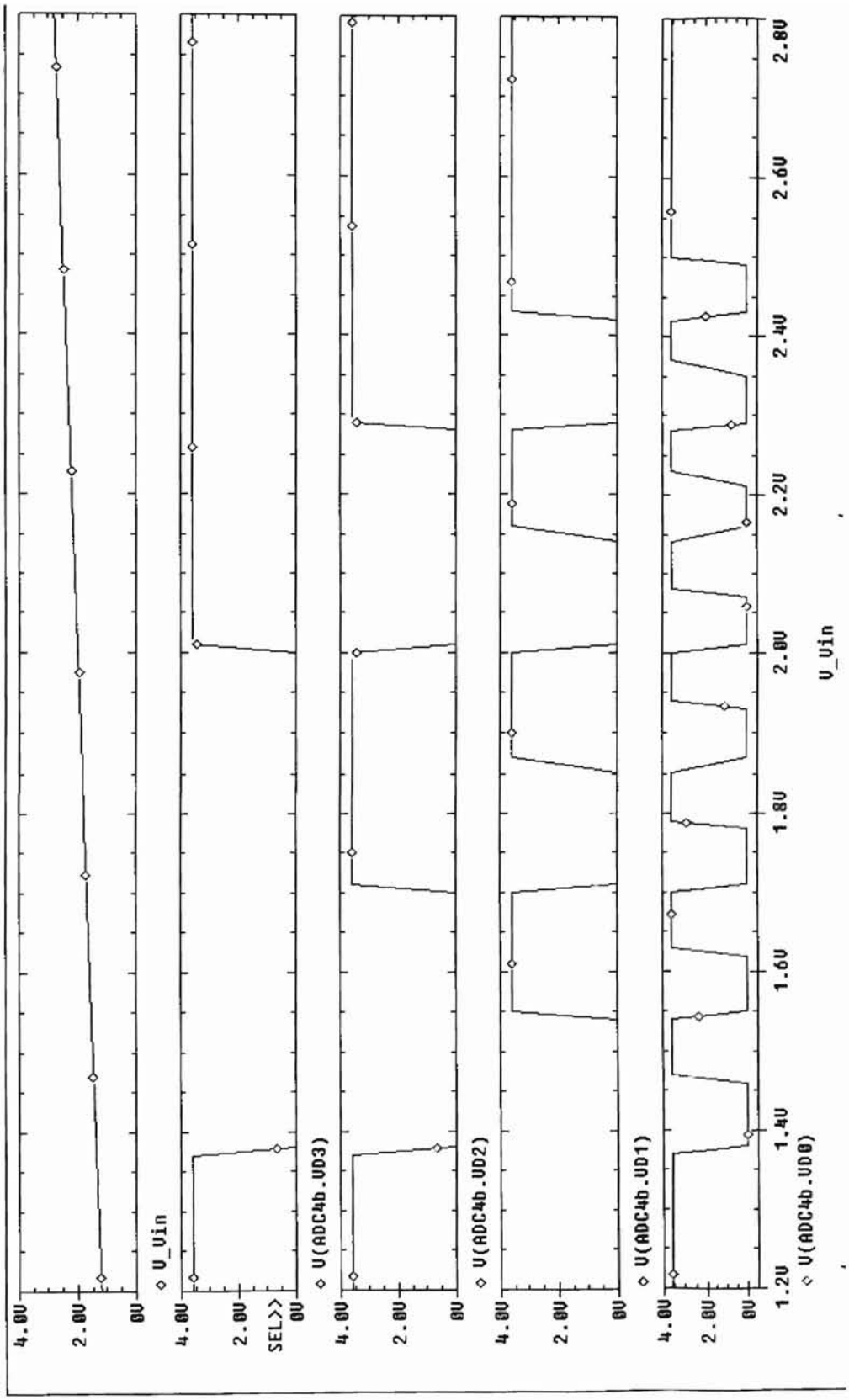


Figure 3.9 DC sweep of ADC

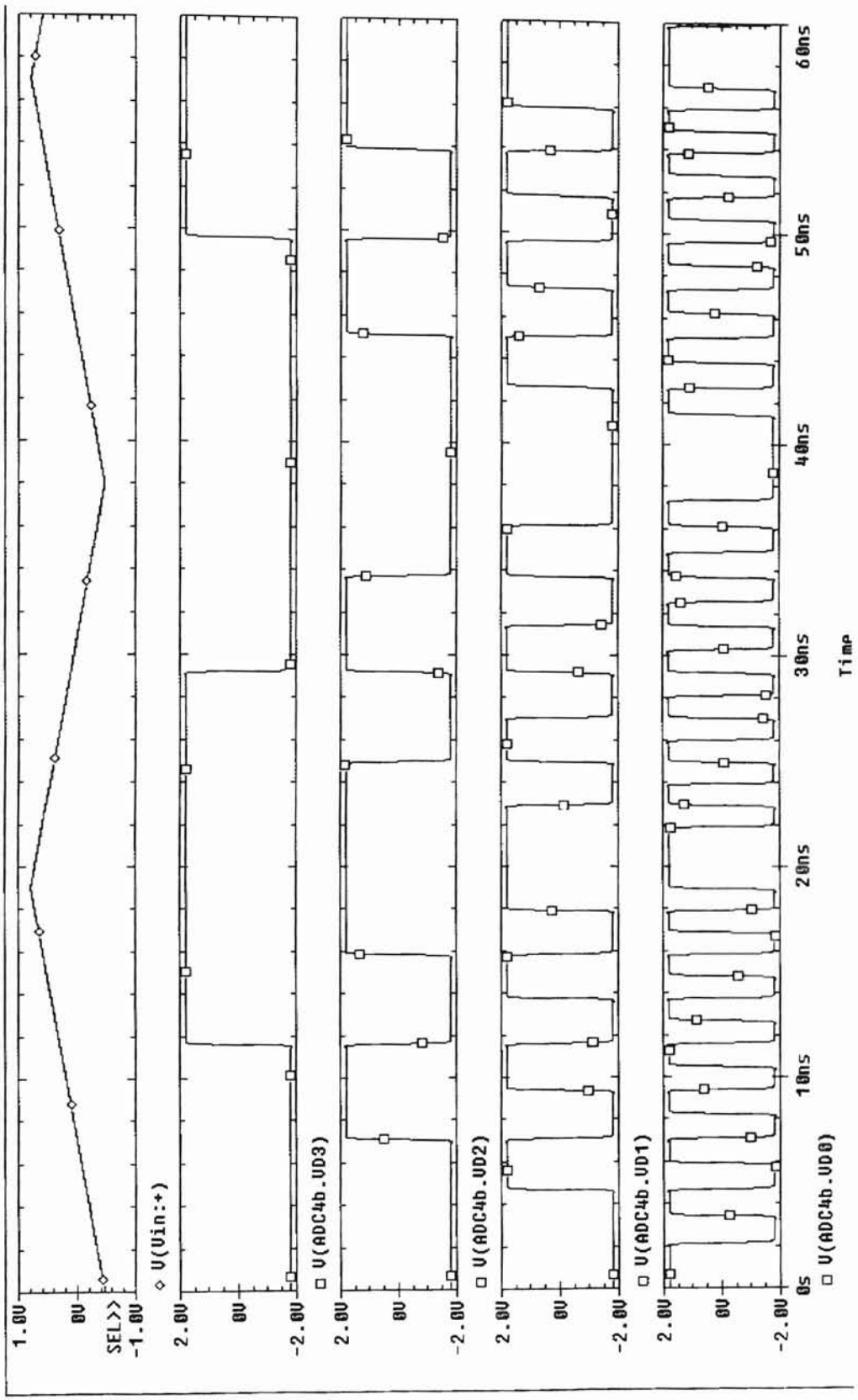


Figure 3.10 Transient simulation of ADC for a triangular input

3.3 Test Results

This section presents the test results from the MIT/LL 0.25μm, IBM 0.1μm, and Peregrine 0.5μm UTSi chips. Testing of the MIT/LL chip proved the comparator bank functionality while the IBM and Peregrine chips proved the full 4-bit ADC functionality.

3.3.1 MIT/LL 0.25μm Chip Test Results

The MIT/LL 0.25μm process chip was submitted for fabrication in late August 1998 and 12 die (dimensions 2.3mm x 2.3mm) where received in June 1999. Figure 3.11 shows the MIT/LL chip layout on Tanner L-Edit. The circuits in the chip include a 4-bit flash ADC, high-speed track and hold, 4-bit DAC, OTA, ring oscillator, and device characterization of transistors and inverters. Out of these circuits, the device characterization transistors and inverters, ring oscillator, and the 4-bit flash ADC were tested. The test results of these circuits are presented below.

3.3.1.1 Device Characteristics

Figure 3.12 shows the circuit layout of the MIT/LL 0.25μm process devices. The devices include,

1) N and PMOS transistors, each having two fingers of W=5μm and L=0.75μm (shown in magnified view in Figure 3.12).
2) Three large inverters,

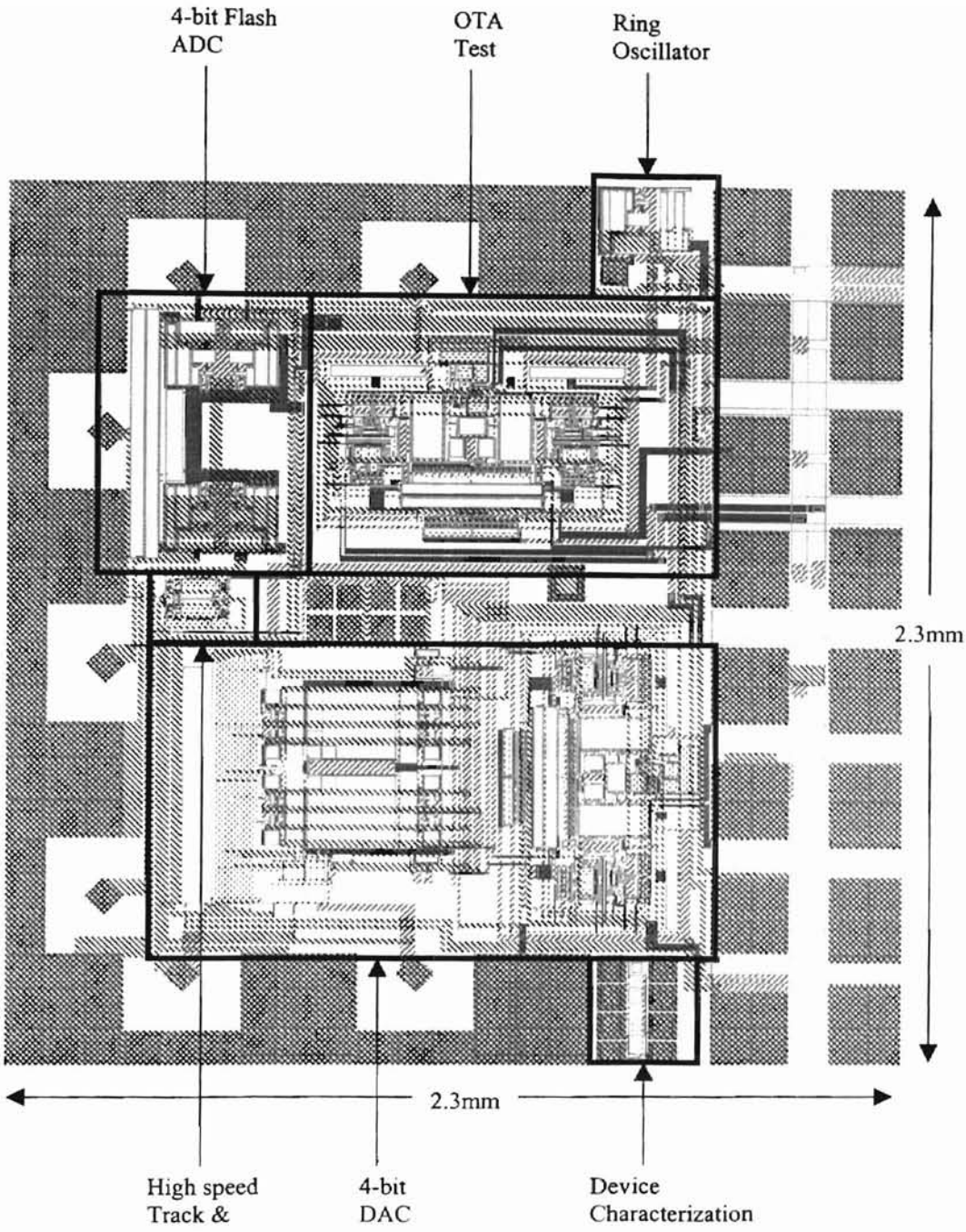


Figure 3.11 MIT/LL OSU 1998 chip layout

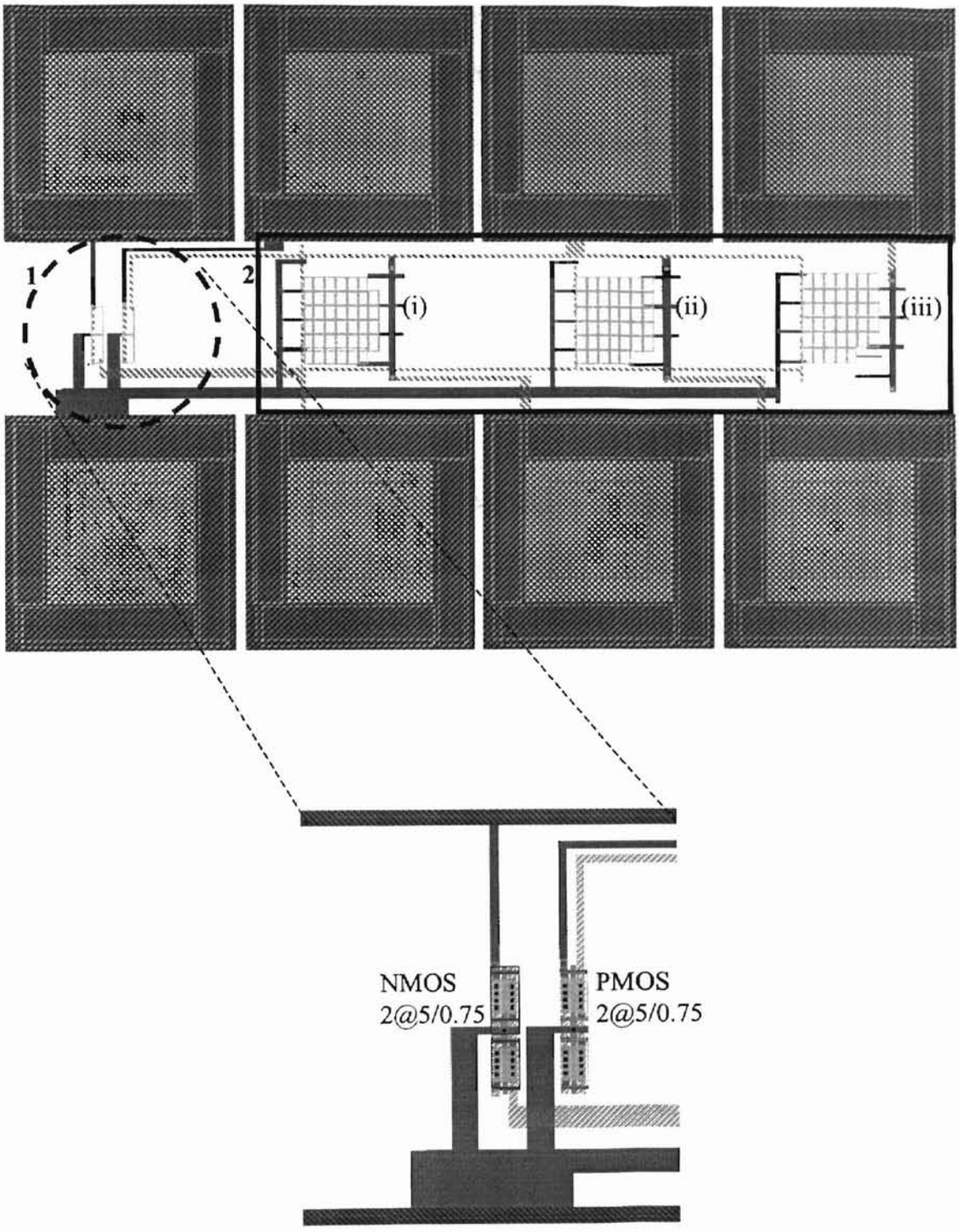


Figure 3.12 Device Characterization test circuit (top) and magnified view of large transistors (bottom)

(i) PMOS (W=20μm, L=0.25μm) NMOS (W=20μm, L=0.25μm)

(ii) PMOS (W=21μm, L=0.25μm) NMOS (W=19μm, L=0.25μm)

(iii) PMOS (W=28μm, L=0.25μm) NMOS (W=12μm, L=0.25μm)

The layout makes it possible to test the inverters and the individual transistors that comprise each inverter (see Figure 3.12).

Large Transistor Devices

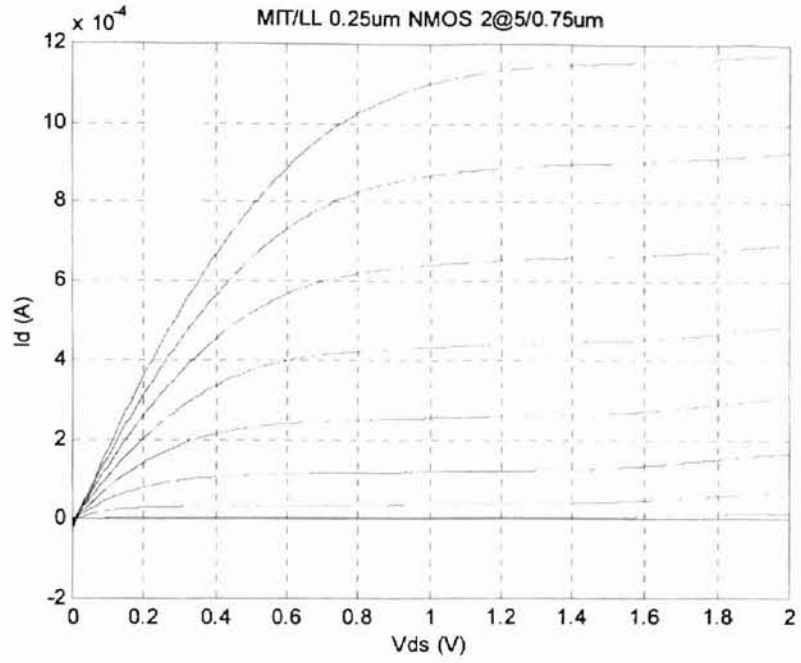
The NMOS device characteristics are shown in Figure 3.13(a). Vgs was swept from 0.0V to 1.8V with step increments of 0.2V. The measured quantities where, V_t=390mV, g_m= 1.10mS, and g_{ds} = 50.00uS. The PMOS device characteristics are shown in Figure 3.13(b). Vgs was swept from 0.0V to -1.8V with step increments of -0.2V. The measured quantities where, V_t=-393mV, g_m= 0.40mS, and g_{ds} = 16.70uS.

Large Inverter Individual Transistors

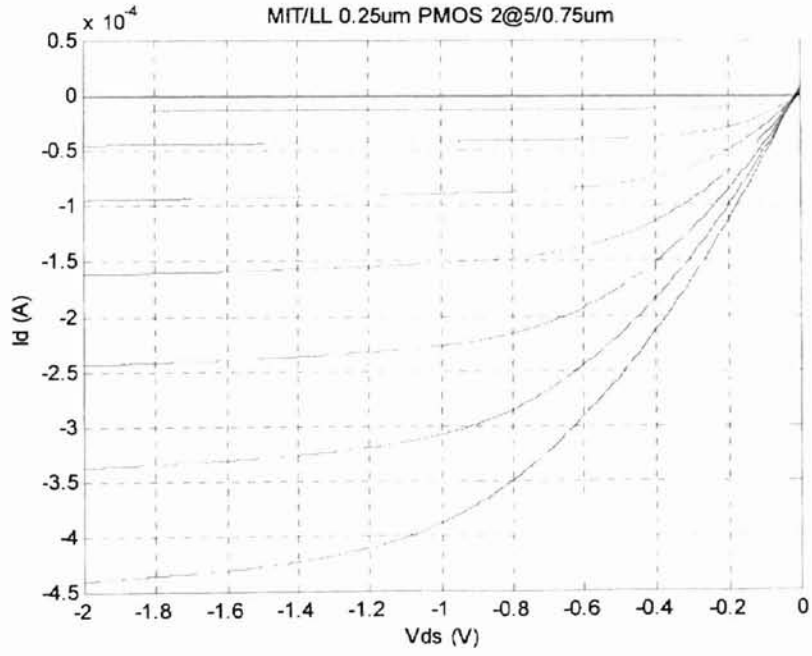
The NMOS and PMOS characteristic curves are shown in Figure 3.14. Vgs was swept from 0.0V to 1.6 V in steps of 0.2V for the NMOS devices and for the PMOS devices, Vgs was swept from 0.0V to -1.6 V in steps of –0.2V. Table 3.2 shows measured parameters of each device.

W_n(um)	V_t(mV)	g_m(mS)	g_o(mS)	W_p(um)	V_t(mV)	g_m(mS)	g_o(mS)
12	271	1.25	0.10	20	-210	1.125	0.10
19	276	1.75	0.10	21	-209	1.50	0.17
20	271	2.30	0.13	28	-200	1.575	0.20

Table 3.2 MIT/LL measured transistor parameters



(a)



(b)

Figure 3.13 Large transistor characteristics (a) NMOS (b) PMOS

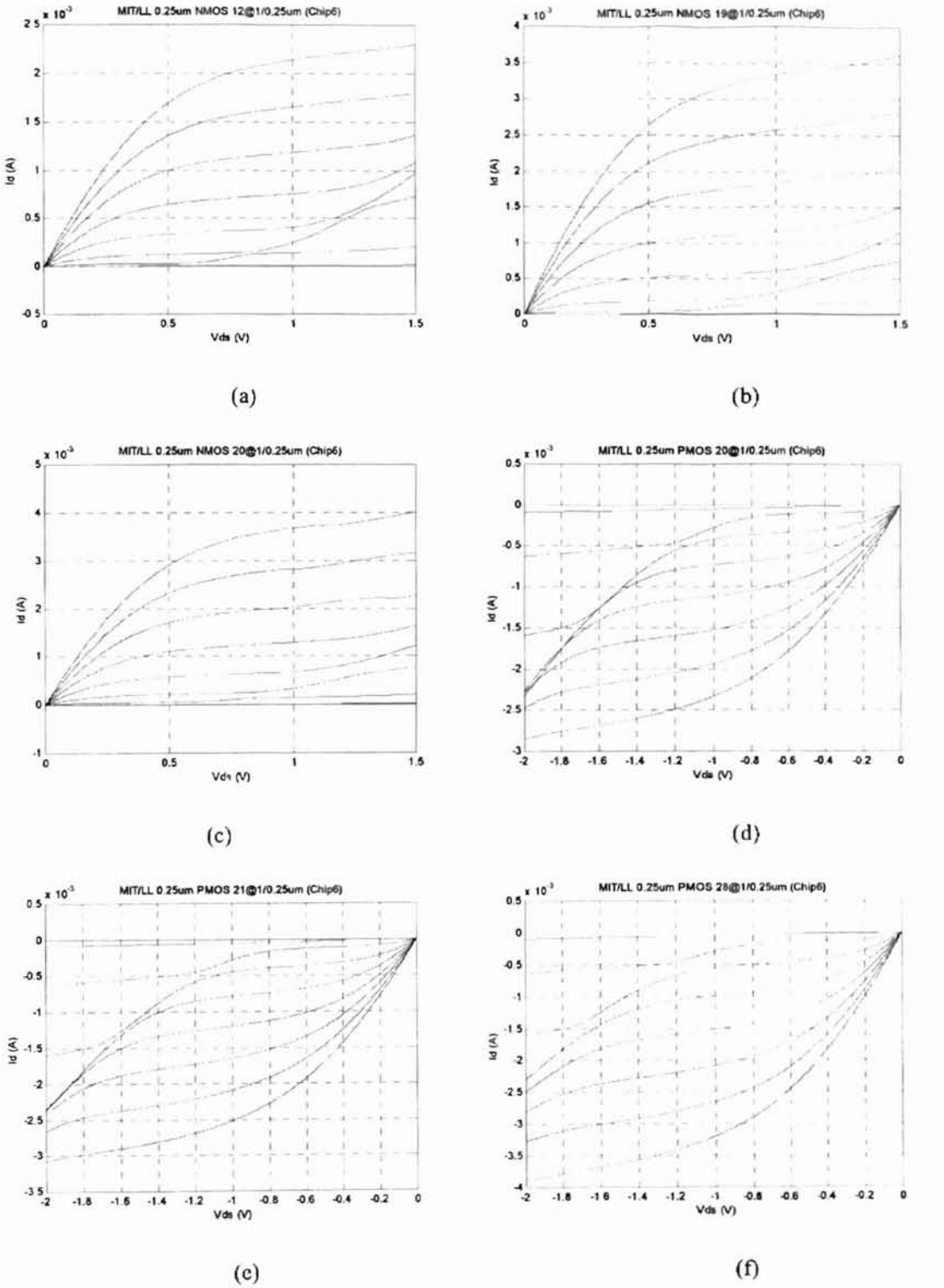


Figure 3.14 Large inverter transistor characteristics (a) Wn=12μm (b) Wn=19μm (c) Wn=20μm (d) Wp=20μm (e) Wp=21μm (f) Wp=28μm

Large Inverters

Figure 3.15 shows the inverter VTC for the three inverters. Voltage supply was Vdd= 0.5V and Vss= -0.5V. Table 3.3 shows the trip voltage of each inverter. Observe that as the Wp/Wn ratio increases, the trip voltages increase as expected. This proves that the theory described in Chapter 3 is accurate and quantization using this procedure is feasible. However a problem existed with the MIT devices. From Figure 3.15 we can see that curve 1 doesn't reach Vdd or Vss. This means that the middle transistor (Wn=Wp=20um) does not fully turn on or off and has considerably low gain compared with the other two inverters. The reason for this is explained by looking at the individual transistor characteristic curves in Figure 3.14. In the cutoff region we observe that at approximately Vds>0.8V the transistor current becomes significant. In other words, the transistors are said to leak which is a drawback in short channel devices. This may be the main reason that the 4-bit flash ADC did not work even in functionality testing. The encoder circuits would have been affected considerably by transistor leakage. This is because the circuit may find it difficult to regenerate due to insufficient gain if the either the P or the N devices leak current.

As a solution to this problem, the N device channel lengths in the encoders were increased to prevent leakage and the complete 4-bit ADC was resubmitted in the Peregrine 0.5μm process. The ability of the Peregrine process to support zero threshold voltage devices was used in designing the comparator bank inverters. Figure 3.16 depicts the comparator bank power supply current versus the input. The smooth appearance of the curve implies that at least most of the inverters trip at their geometrically set trip

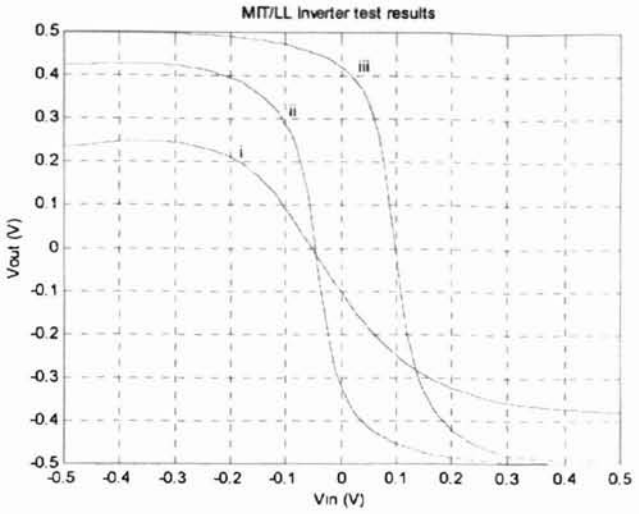


Figure 3.15 Inverters with geometrically set trip voltages

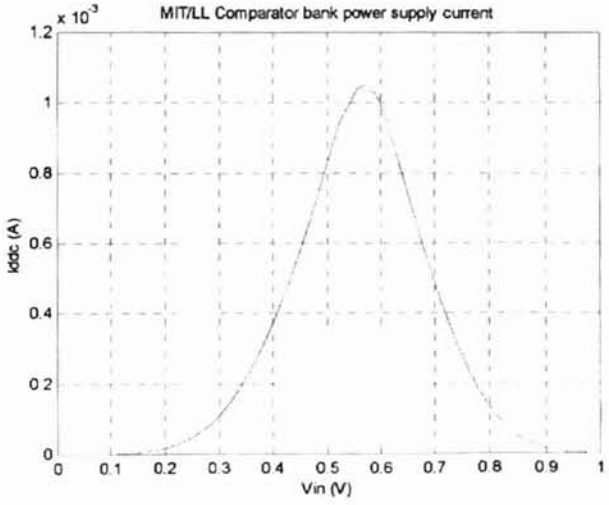


Figure 3.16 Characteristic comparator bank power supply current

Inverter	Offset voltage (mV)
i	-52*
ii	-46
iii	100

Table 3.3 Inverter trip voltage

voltages.

3.3.1.2 Ring Oscillator

Testing the ring oscilator is useful in determining process limitations. It consists of 65 inverters in series where Wn=Wp=4.0μm and L=0.25μm. A six-stage pad driver is used to drive the single output pad. Figure 3.17 shows the layout of the 65 inverter ring oscillator and pad driver on the MIT/LL chip. The test results are shown in Figure 3.18(a) and 3.18(b). It is important to note that the pad driver delay must be less than the ring oscillator delay if test measurements are to be that of the ring oscillator (see Appendix E for proof). Otherwise the test data will be limited by the pad driver.

3.3.2 IBM 0.1μm Chip Test Results

This chip was submitted in late December 1997 and the fabricated wafer arrived in January 2000. The results presented below are for an output buffer ring oscilator, NMOS characteristics, comparator bank and feed forwared stage, and the 4-bit ADC.

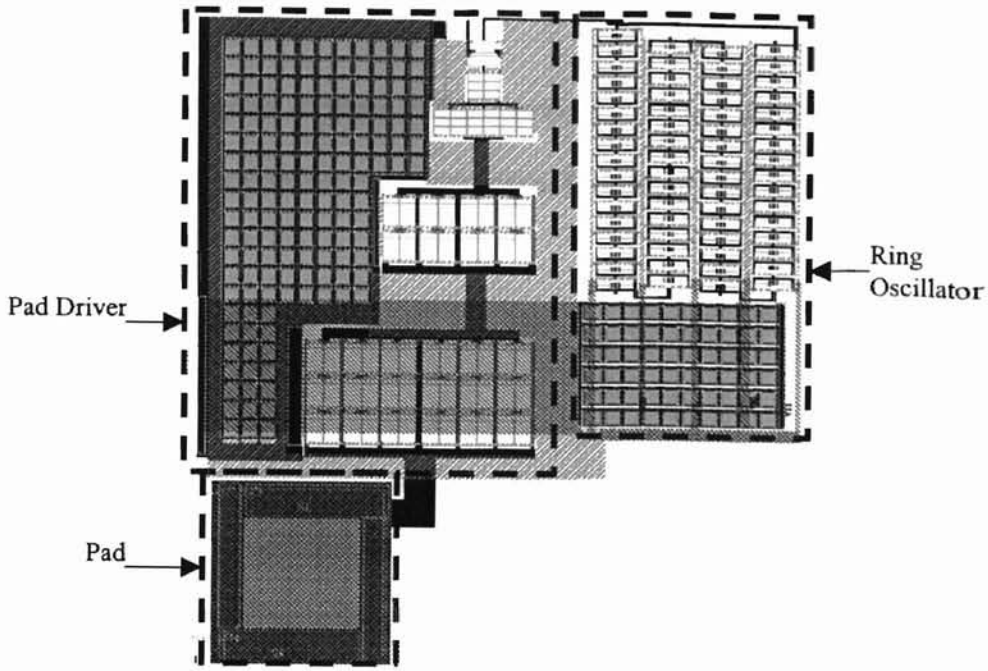
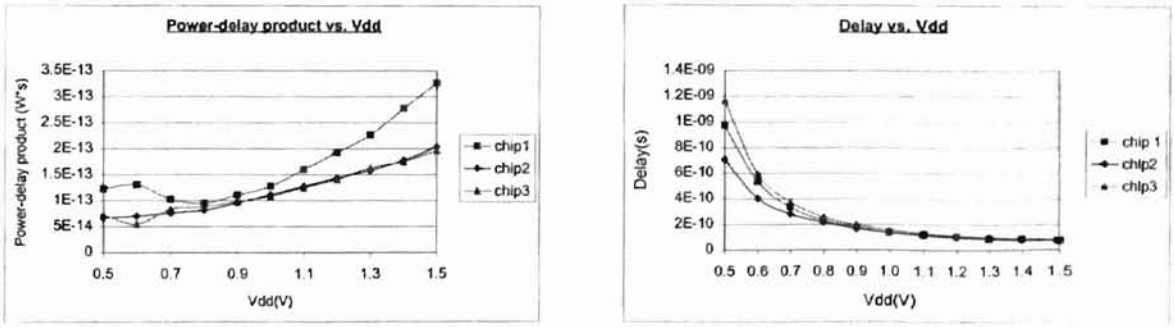


Figure 3.17 Ring oscillator of MIT/LL chip



(a) (b)

Figure 3.18 MIT/LL ring oscillator test results (a) Power-delay product vs. Vdd

(b) Delay vs. Vdd

3.3.2.1 Ring Oscillator

This circuit consists of three pad driver buffers connected in series and made into a ring oscillator. Each pad driver has 5 inverters. Test results are shown in Figure 3.19.

3.3.2.2 Device Characteristics

Although test setup for a minimum sized transistor was not included in the layout, NMOS characteristics were obtained indirectly from another circuit. The transistor curves are shown in Figure 3.20. Note that unlike in the MIT/LL process, the transistors do not leak.

3.3.2.3 Comparator Bank and Feed Forward Stage

Test results from the comparator bank and feed forward stage for selected comparators are shown in Figure 3.21. Note that the average trip voltage difference (ΔV_{TRIP}) between two consecutive comparators is 5mV. Table 3.4 shows the transistor sizes in fingers and their trip voltages (V_{TRIP}) corresponding to each output in Figure 3.21. Note that a size of a finger for both unit NMOS and PMOS was 1.7μm.

	Vout1	Vout6	Vout7	Vout8	Vout9	Vout14	Vout15
NMOS	19	14	13	12	11	6	5
PMOS	10	20	22	24	26	36	38
Wp/Wn	0.5	1.4	1.7	2	2.4	6	7.6
V_{TRIP} (V)	0.498	0.554	0.557	0.565	0.569	0.605	0.613

Table 3.4 Summary of comparator bank and feed forward stage trip voltages

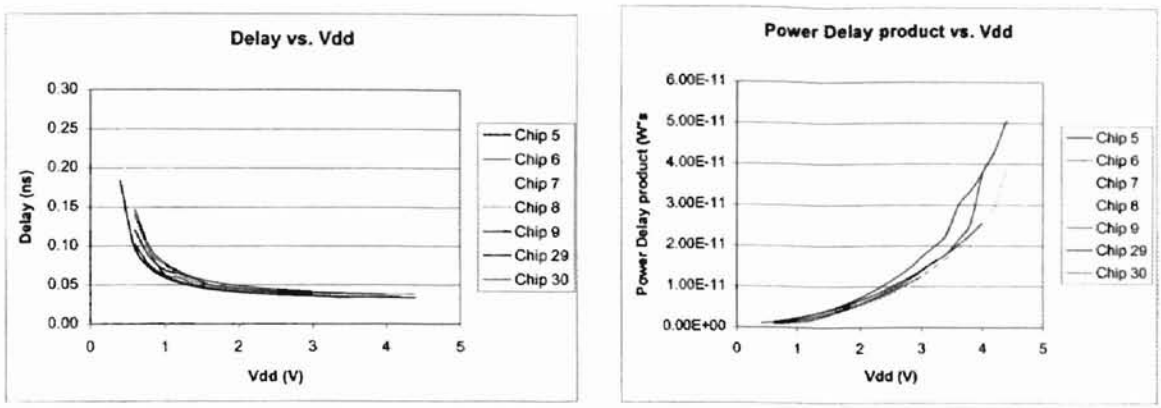


Figure 3.19 IBM chip output pad driver ring oscillator

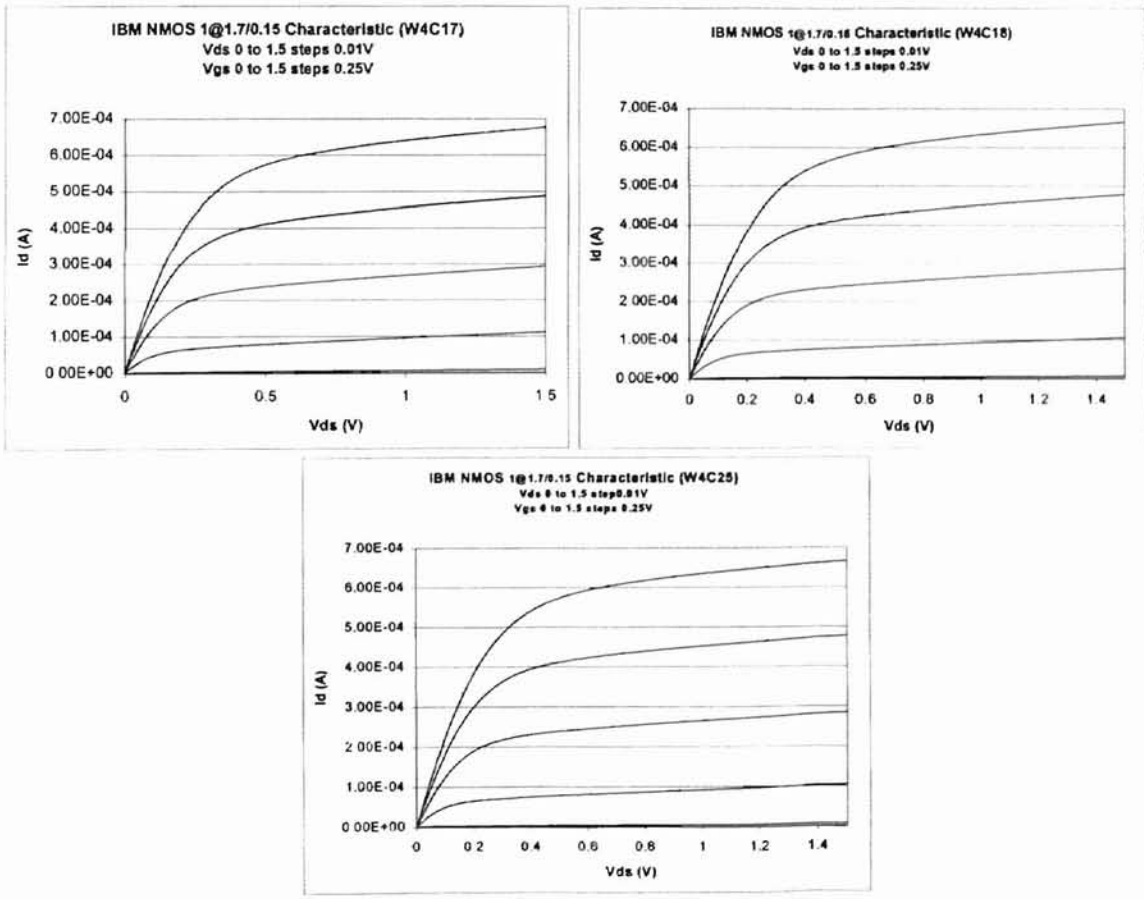


Figure 3.20 Transistor characteristics curves for a 1.7/0.15μm minimum geometry NMOS

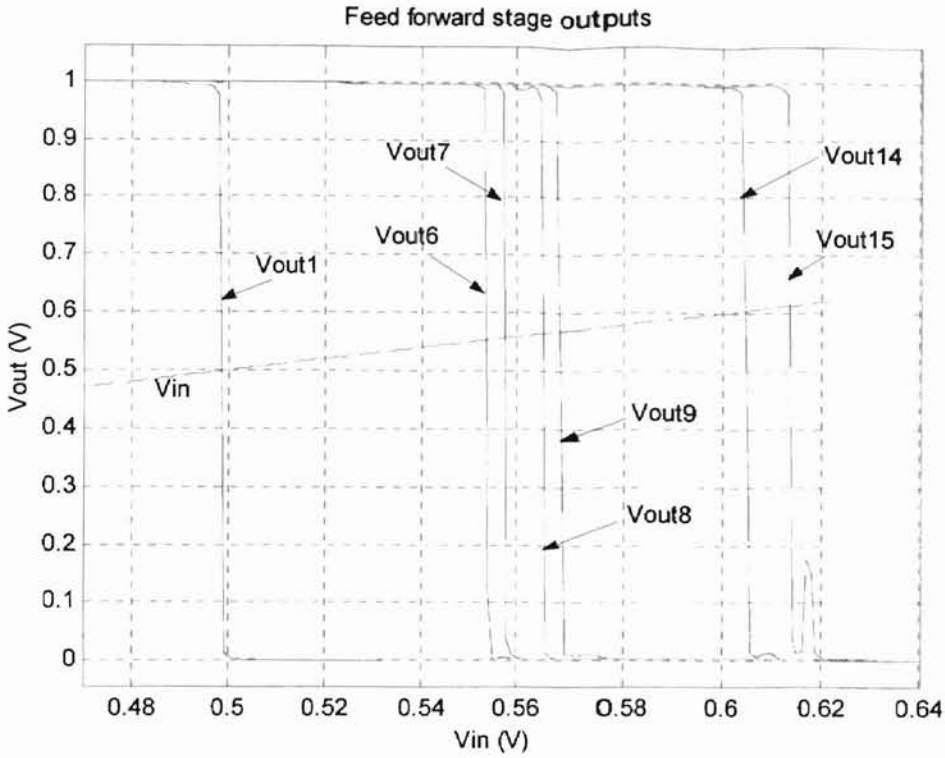


Figure 3.21 Comparator bank and feed forward stage outputs

3.3.2.4 Full 4-bit ADC Test

Figure 3.22 and 3.23 show the input and the four digital outputs obtained from a transient test of the full 4-bit ADC. The input frequency was a 2KHz triangular input having a peak to peak voltage of 0.38V and offset of 0.095V. The power supply voltages for the comparator bank and feed forward was at +/-0.70V, bubble detector and encoder at +/- 0.25V, and pad drivers at +/- 0.55V. The results show the 4-bit ADC is functional. The problems that exist with the design have been identified. These problems and proposed solutions are presented in section 3.4.4.

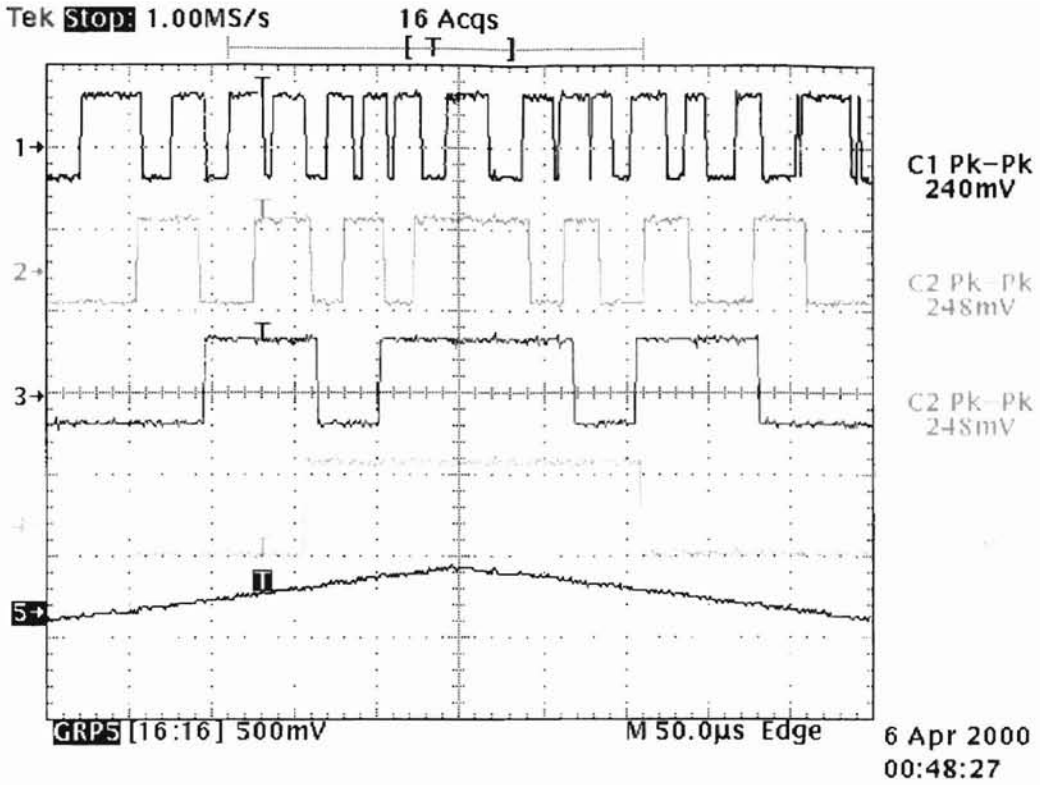


Figure 3.22 IBM 4-bit ADC transient

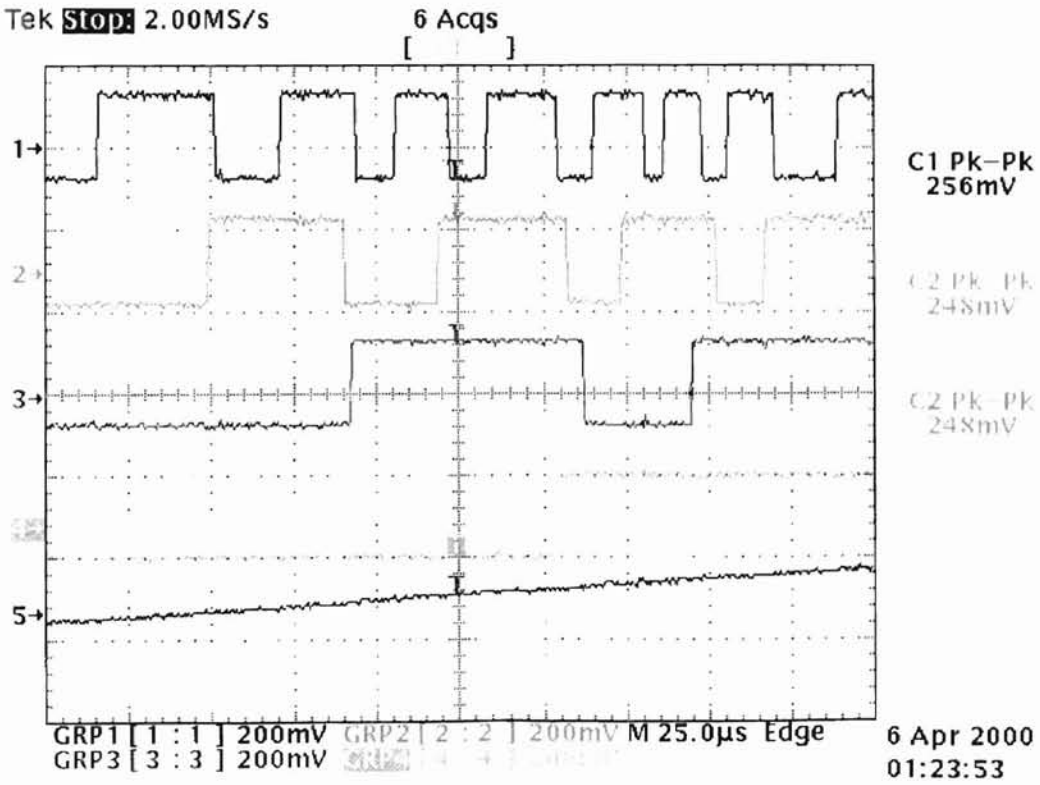


Figure 3.23 IBM 4-bit ADC transient zoomed

3.3.3 Peregrine UTSi 0.5μm Chip Test Results

The OSU peregrine chip was sent for fabrication in August 1999 and was received in late February 2000. Each six-inch diameter wafer consisted of 45 die and 5 wafers were provided. Test results include ring oscillator data and process performance comparison, device characteristics, comparator bank inverter VTC, and full 4-bit ADC test.

3.3.3.1 Ring Oscillator

A ring oscillator circuit consisting of 49 stages was tested in all five wafers to compare process and wafer performance. The results are shown below in Figure 3.24 (Stage delay vs. Vdd) and Figure 3.25 (Power delay product vs. Vdd). The results conclude that out of the 5 wafers, wafer number 11 (W11) had poor performance compared with the other wafers (W15, W14, W9, and W6).

3.3.3.2 Device Characteristics

The NMOS device had a minimum width of 2μm while the PMOS minimum width was 3μm. The length of both devices was 0.5μm. Figure 3.26 (a) and (b) show transistor characteristic curves. Figure 3.26 also compares the PSICE model with the test data for N and PMOS devices. Note that there is a difference between the PSIPCE model simulation and the actual test data. This difference may account for circuits not being

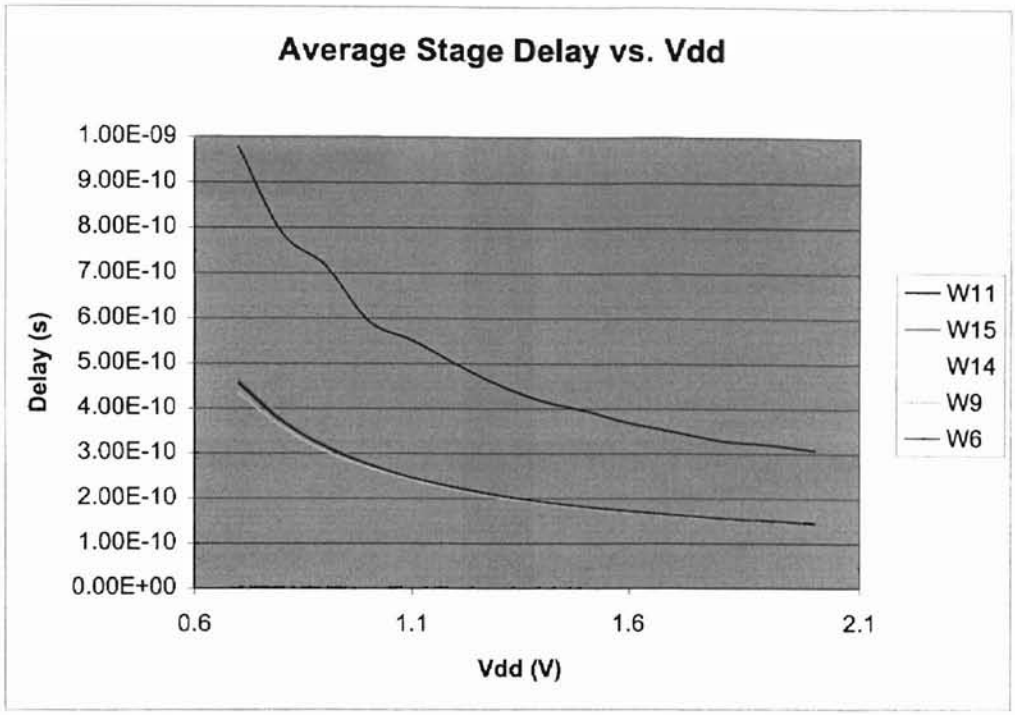


Figure 3.24 Average stage delay vs. Vdd

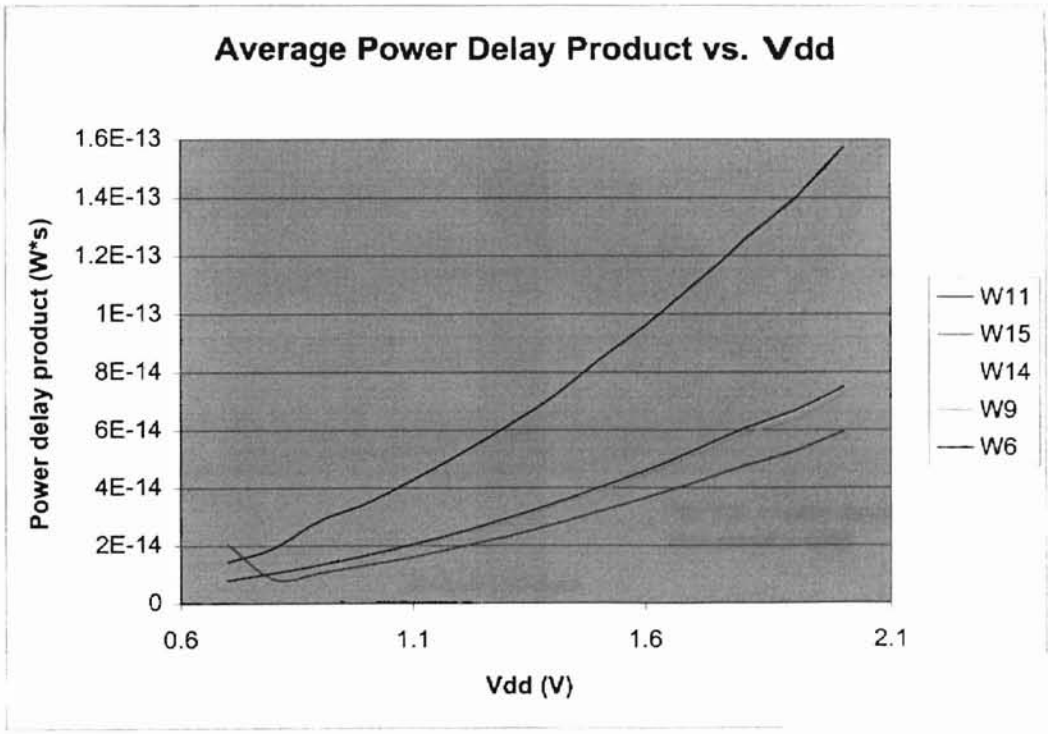
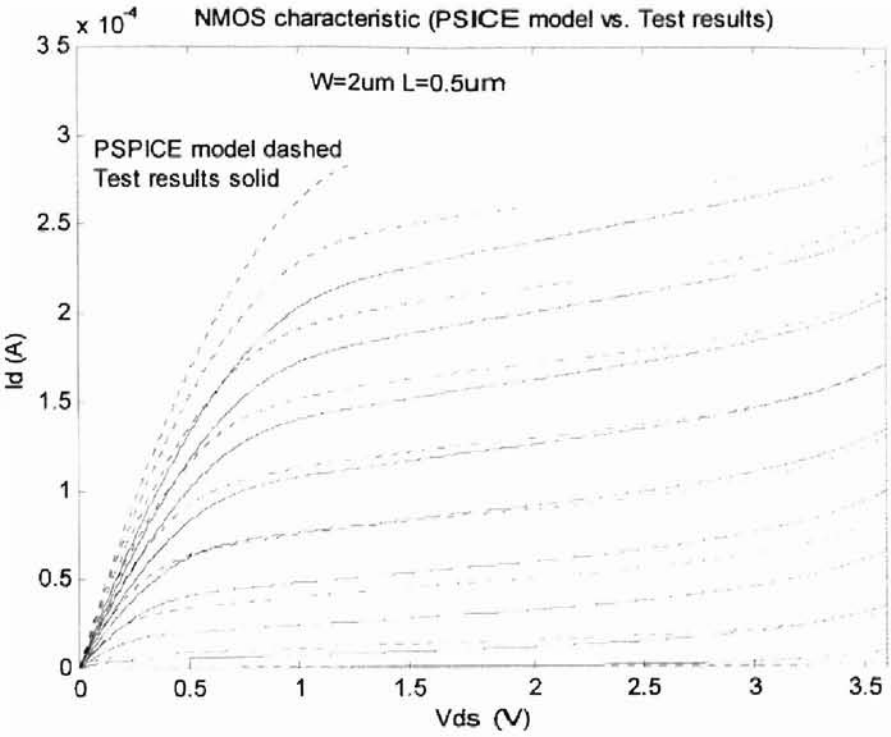
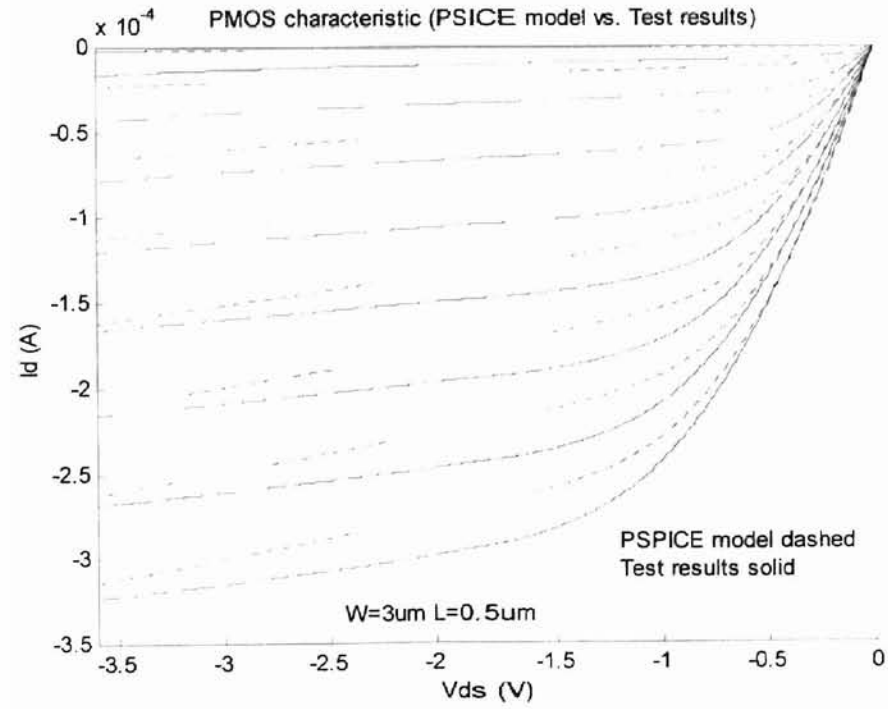


Figure 3.25 Average power delay product vs. Vdd



(a)



(b)

Figure 3.26 Comparison of PSPICE model with test data. (a) NMOS (b) PMOS

optimized properly during the design phase. Transistor measured parameters are shown below in Table 3.5.

	NMOS W=2μm L=0.5μm	PMOS W=3μm L=0.5μm
g_m	0.156mS	0.211mS
g_o	15.92μS	16.25μS
Ron	7883Ω	6284
V_T	229mV	-222mV

Table 3.5 Peregrine UTSi 0.5μm transistor measured parameters.

3.3.3.3 Comparator bank VTC

The test block of the comparator bank included all 17 comparators. The test results of VTC curves for all 17 inverters are shown in Figure 3.27. The results again indicate that geometrically setting inverters do indeed trip at different trip voltages. Looking at the plot, the difference between trip voltages (ΔV_{TRIP}) is not uniform. The trip voltage difference increases as you move towards the larger PMOS inverters. This can be attributed to process variation and offset voltages. The minimum ΔV_{TRIP} was 0.011V and maximum ΔV_{TRIP} was 0.325V. The average ΔV_{TRIP} was 0.018V. Also note that the comparators do not pull up to Vdd whilst they do pull down to Vss. It was observed that the NMOS devices were weaker in shutting off compared with the PMOS devices. This could explain the leakage phenomena.

3.3.3.4 Full 4-bit Flash ADC Test

Two versions of the 4-bit flash ADC were included in the chip. The difference

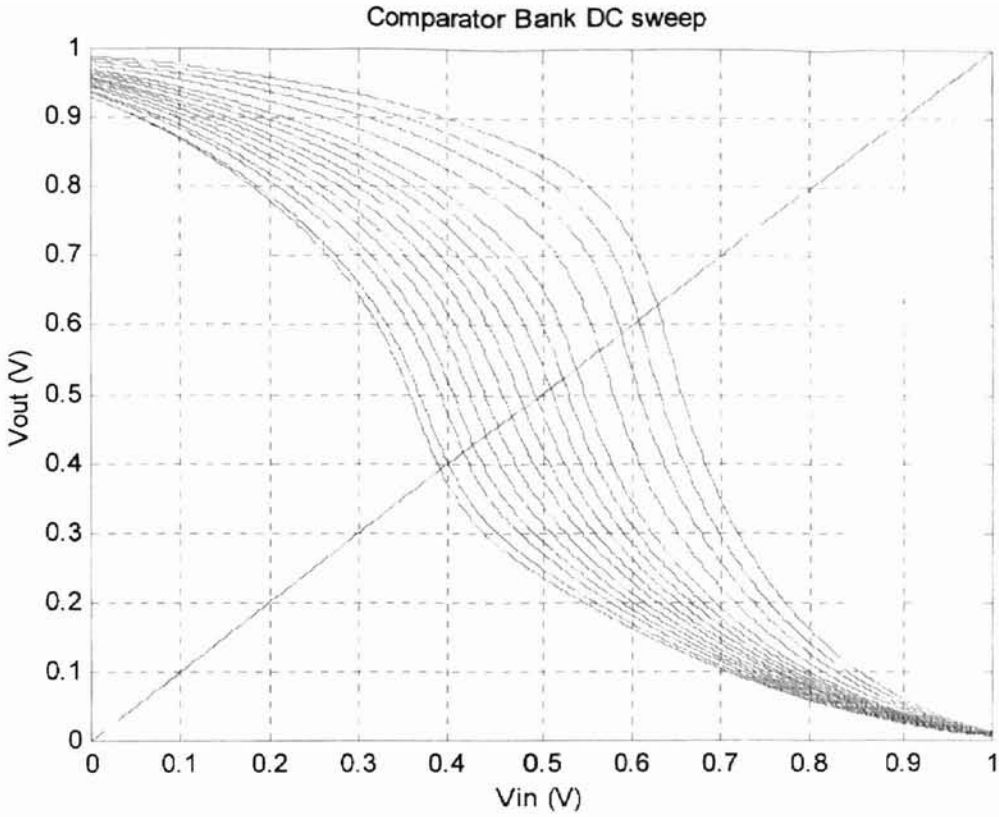


Figure 3.27 Comparator bank inverter VTC

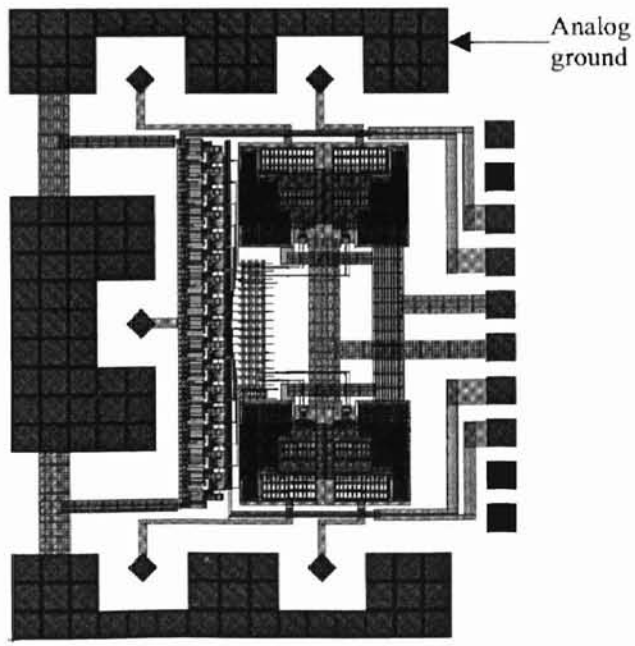


Figure 3.28 4-bit flash ADC layout for Peregrine UTSi 0.5μm process

was in the encoder NMOS channel length which was 0.5μm and 0.8μm. This was due to suspected leaking of the NMOS (see section 3.3.1.1). It happened that the ADC with L=0.5μm failed to work while L=0.8μm ADC was successful. Figure 3.28 shows the layout of the 4-bit flash ADC.

The results obtained confirm functionality of the ADC. Figure 3.29 shows the transient test result. Its is observed that the all the output codes are present as expected (see Figure 3.9 and 3.10). Any difference can be due to various reasons, limitaion by the measuring instruments including signal generator and oscilloscope resolution and accuracy. If some of the comparator bank ΔV_{TRIP} voltage are less than the resolution of the signal generator, some of the output codes will not be sampled and as a result missing codes are present. A major observation was that the LSB was not steady at all.

The speed performance was also very poor. The best die could operate at 4KHz and no more. Almost all dies operated at 1KHz. Figure 3.29 and 3.30 show ADC output for a triangular input of 1KHz. Looking at Figure 3.30 two problems with the ADC are now apparent. The fifth output code is weak and the outputs are not alligned properly. The fifth code being weak effects the DNL of the ADC. The output not being alligned properly adds errors to the output digital word.

Figure 3.31 shows the reconstructed output for a sinusiodal input of 0.38Vpp at 1KHz. The ouput seems to follow the input very well. The result of dynamic testing to find DNLE and SFDR of the ADC are presented in Figure 3.32 and 3.33. Figure 3.32 is the result of the histogram test. Note that the dashed line represents the ideal ADC (equation 2.21) while the solid line is for the actual DUT. The results obtained conclude that there are no missing codes. Figure 3.33 shows the DNLE using data obtained from

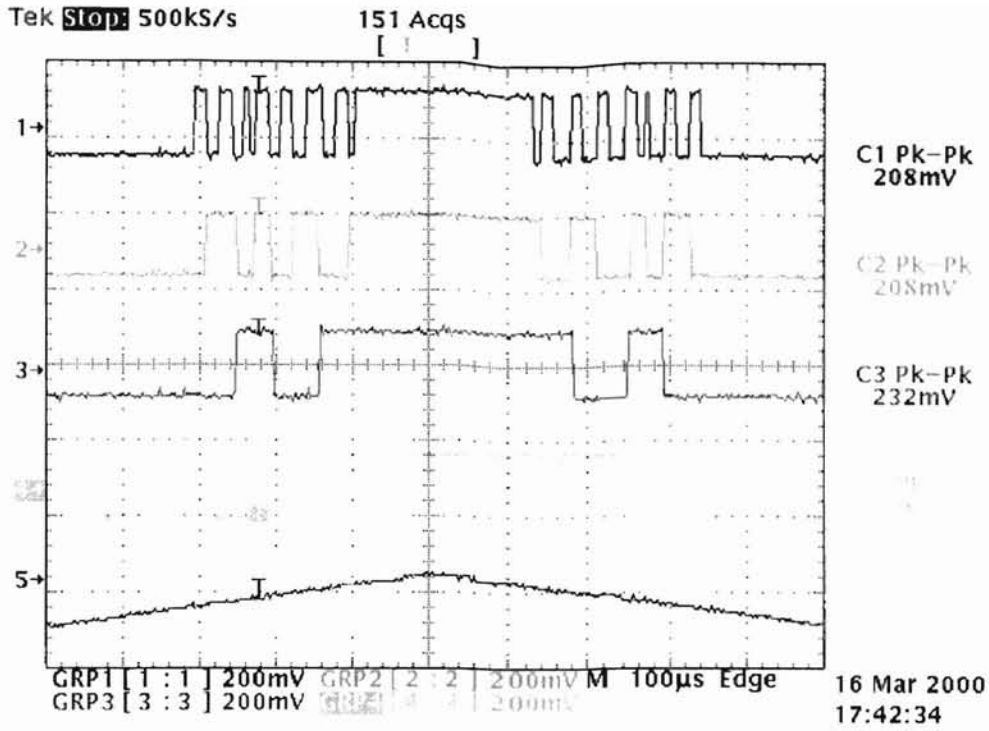


Figure 3.29 ADC output for a 1KHz triangualar input

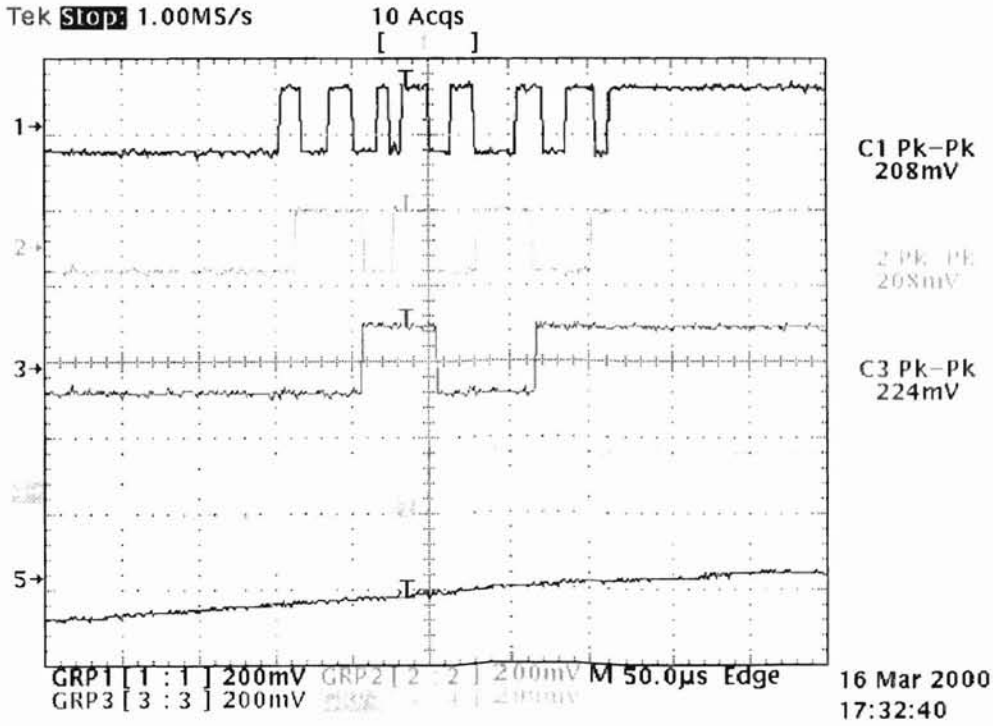


Figure 3.30 ADC output zoomed

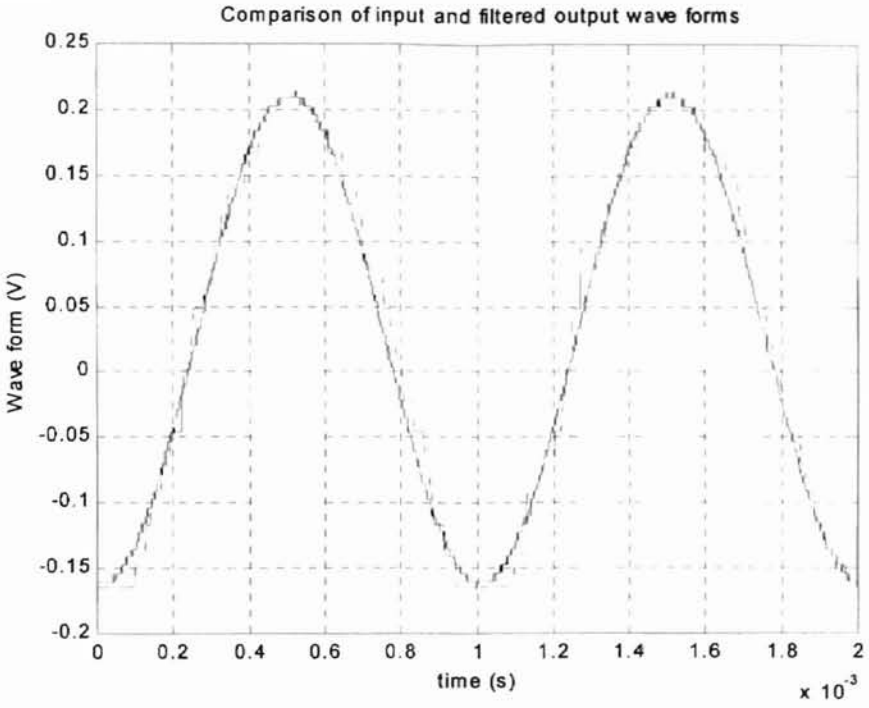


Figure 3.31 Input and reconstructed output of ADC

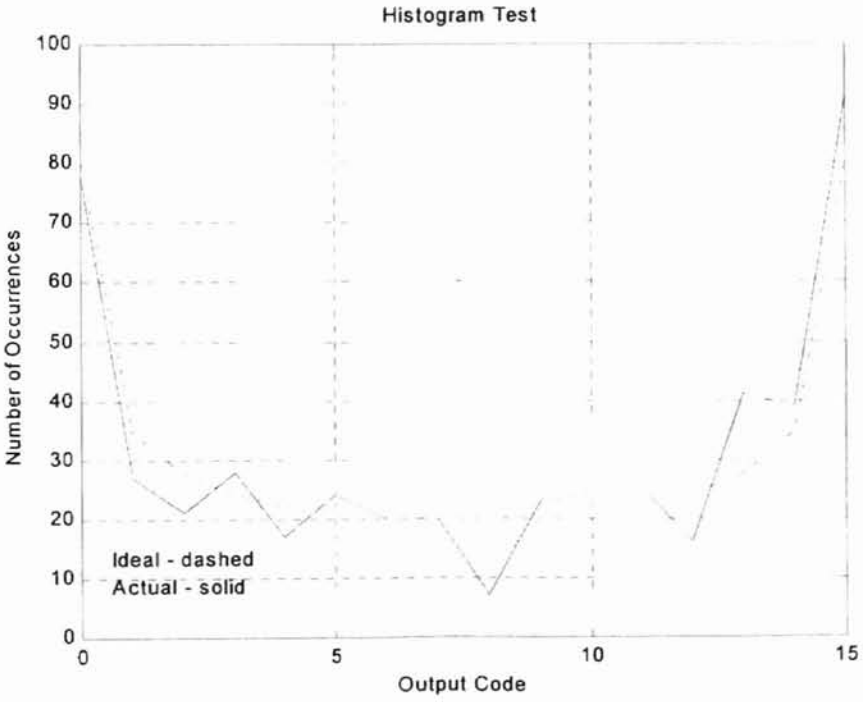


Figure 3.32 Histogram test results

the histogram test. Note the vertical scale is in units of LSB. The maximum non-linearity is 0.65LSB. Note that DNLE must be less that ½ LSB for accurate conversion.

The spectral analysis of the output is shown in Figure 3.34. The 1024 point DFT of the output is taken after passing through a Hanning window. The SFDR was found to be 24.5dB and this resulted in an ENOB of at least 4 bits. This confirms a good SNR at 1KHz.

Test results and observations have given insight into the 4-bit ADC performance and existing problems. They are summerized below.

- Although functionality was proven beyond doudt, the speed perfromace was very poor. The circuit did not perform better than 4KHz. Reasons for this may be due to power supply inductance and insufficient decoupling capacitance. The analog ground had to be connected to the power supply ground externally which introduced a large inductance. The solution to this is to connected the analog ground (see Figure 3.28) to an unused pad of the 10-pin DC wedge on the layout itself which would then connect to the power supply ground and thus reducing any inductance. Dice and bond up would be the next step to obtain high-speed operation.
- It was noticed in Figure 3.27 that the comparator bank inverters do not pull up entirely to V_{DD}. The reason for this is that the zero threshold NMOS devices used in the comparator bank were weak in turning off. This resulted in leakage but would give good input voltage swing.
- Figure 3.30 revealed the outputs not being synchronized. This resulted in error codes being present in the output digital word. The solution to synchronize the outputs is to add latches to the bubble detector or encoder outputs. A decision to place the latches

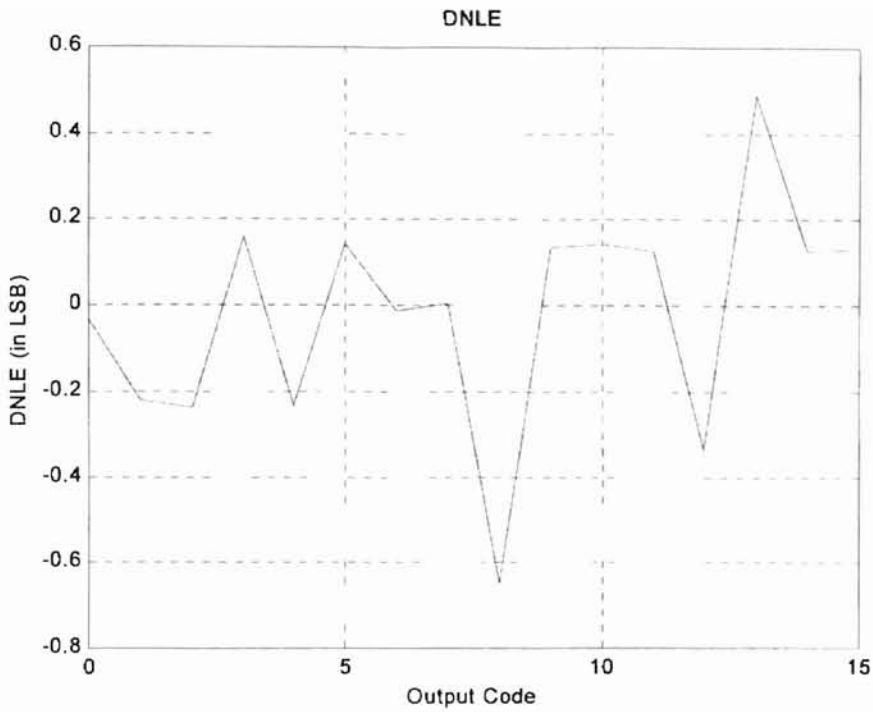


Figure 3.33 Measurement of DNLE

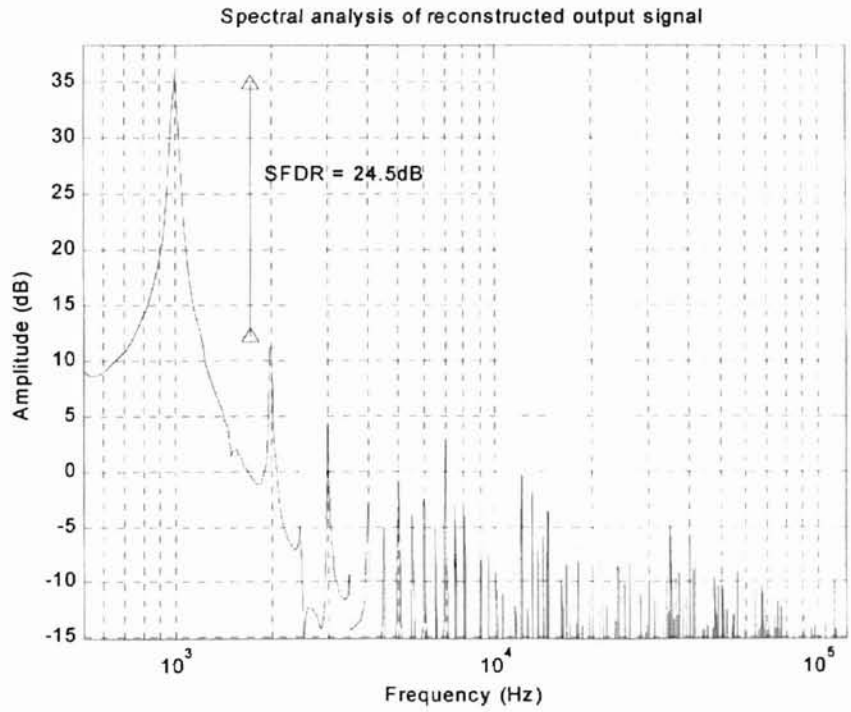


Figure 3.34 Spectral analysis of ADC output

at the output of the encoders were reached since only four are required and this can be easily added into the existing layout. This would however affect expected ADC speed performance.

- Power consumption of the comparator bank was measured at 18mW. The Bubble detector and encoder stages were at 0.2W. The pad drivers consumed 2mW of power. All values were measured at 4KHz. Back calculation using ring oscillator data revealed the latter two values to be too high. Therefore it is suspected that the circuits have high leakage.

The functionality of the 4-bit ADC has been proved and problems identified. The solutions to these problems have also been discused. This concludes the presentation of the test results and analysis of the 4-bit ADC performance. The next chapter presents two applications using the 4-bit flash ADC discussed in this study.

CHAPTER 4

APPLICATION OF 4-BIT FLASH ADC

This chapter outlines two applications of flash ADC. The first example is a time interleaved ADC. The second is an AGC (automatic gain control) for a receiver.

4.1 A 4-bit Time-Interleaved ADC

In a time interleaved ADC [4][40][41][42], M number of ADCs are connected in parallel. A sample and hold circuit provides the sampled input signal to each ADC. The clocks of the sample and hold circuits apply the input to each ADC successively. This enables the ADCs to operate at ¼ their maximum sample frequency while providing the same or better accuracy and speed performance. The basic block diagram of a time-interleaved ADC is shown in Figure 4.1 for the case when M=4. The sample and hold (S/H) circuits are clocked by four clock (ϕ) signals also shown at the bottom of Figure 4.1.

The advantage of the time-interleaved method is that to obtain the same bandwidth of a single ADC, the time-interleaved ADCs may operate at a speed of 1/M. This in turn increases ADC dynamic range and accuracy. Another advantage is to use

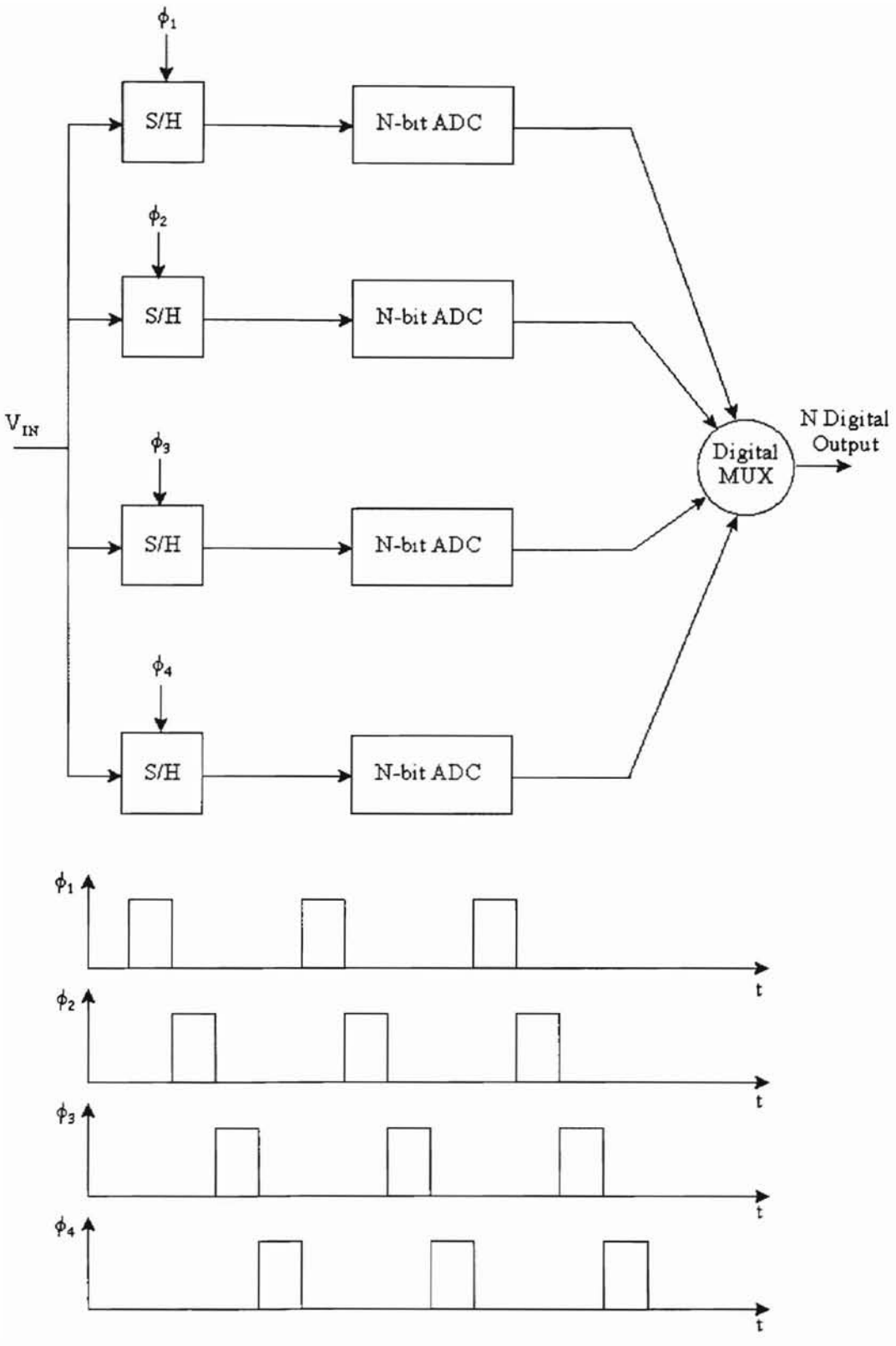


Figure 4.1 Time-interleaved ADC

slower speed but low area consuming ADCs such as SAR [39] or algorithmic converter [40] in a time-interleaved system. This approach will result in a time-interleaved ADC having far less area than an equivalent flash ADC having similar operating speed and accuracy.

However, a few problems exist with this scheme. The major disadvantage is the need to match the ADCs well, both in time and in voltage (ADC input offset voltage problem [42]). Because of this, each ADC will output a slightly different output for the same DC input. The effects of gain and offset error on a time-interleaved ADC are analyzed in [40]. Reference [42] proposes to use a non-linear digital smoothening filter to replace the output by a running average of four adjacent values. Another method discussed in reference [41] reduces gain error and offset effects by channel randomization. Randomly choosing ADC channels will reduce the correlation between different converter digital outputs, the effects of the mismatches will tend to average out. Therefore, using channel randomization, a reduction in the noise power is expected and is proved in [41].

Another problem present in time–interleaved ADCs are the S/H circuits introducing additional noise and harmonic distortion [41], which again can be reduced by careful design and layout techniques.

4.2 Automatic Gain Control (AGC) Using ADC

AGC is an integral part of any communication device (TV, radio, and cellular phones) [43]. It essentially conditions the signal received from the antenna to be applied

to the DSP circuitry. The strength of a signal received varies depending on the location from the transmitter and obstacles in the path of the signal. Signals of varying amplitude are amplified by the AGC system to meet the amplitude requirements of the ADC. If the received signal is low, it must be amplified to prevent gross under drive. Especially at the input of an ADC, if the input signal is full scale, all the possible ADC output values are exercised and this improves ADC output signal resolution. The AGC must also attenuate the received signal if it's too large. This is due to the fact that overdriving circuits can result in distortion and clipping. High-speed AGC circuits are required especially in cellular systems were the input signal may drastically and suddenly vary as trees or buildings come in between signal path and the mobile receiver. The AGC circuit will pick up this change in signal strength and automatically adjust it so that user reception is maintained at good quality (user does not notice signal degradation).

The example of an AGC system in which an ADC is used is shown in Figure 4.2. Adding the ADC will eventually merge part of the DSP system with the front preconditioning system. Figure 4.2 illustrates the system blocks. The antenna received (V_{IN}) signal is passed through an ADC. V_n represents the quantization noise of the ADC. From this point forward the signal is processed using digital circuits. The amplitude of V_{IN} is determined by taking the absolute value and then by lowpass filtering to obtain its DC component. For example a full wave rectified sinusoidal waveform of peak voltage V has a DC component of $2V/\pi$ from Fourier series analysis.

The feedback signal is passed through a digital-to-analog converter (DAC). The difference between the DC component and $3V_{FS}/\pi$ is then found. The effect of negative feed back is to increase the gain when the input amplitude is low and decrease the gain

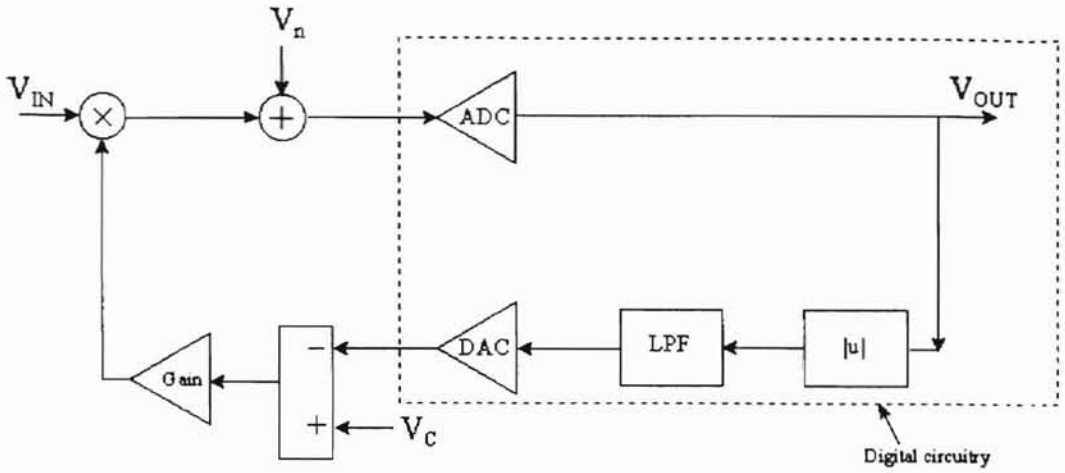
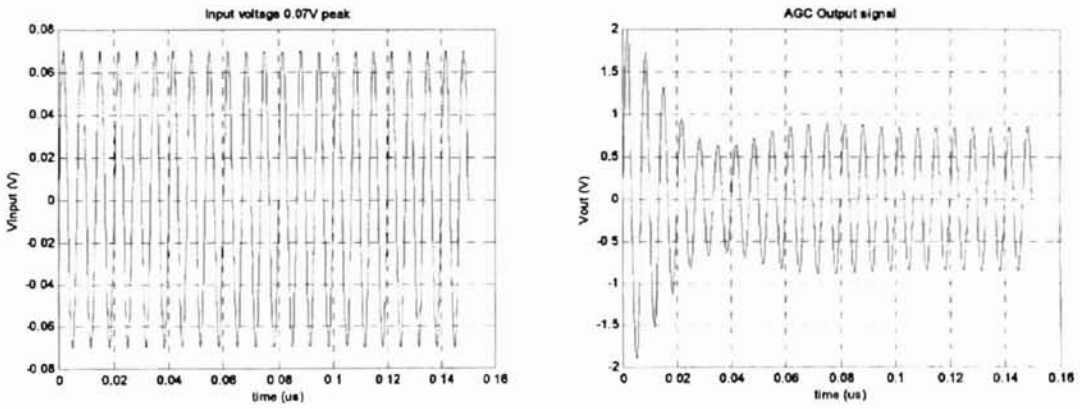
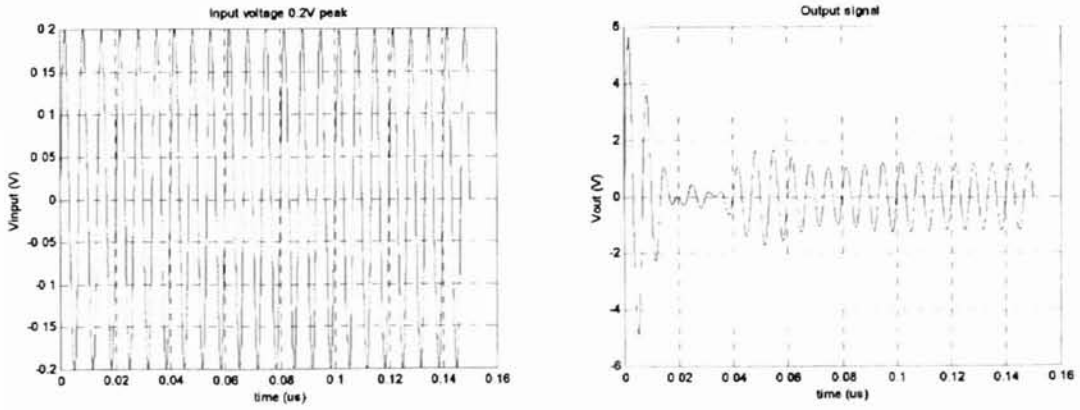


Figure 4.2 AGC system block diagram



(a)



(b)

Figure 4.3 AGC simulation results (a) Vinput=0.07V (b) Vinput=0.2V

when the input amplitude is high. The DAC output is amplified and then multiplied with the input signal to obtain the full-scale signal. Note that the V_{OUT} represent the data being sent for DSP.

The system works for input values in the range from 0 to $0.3V_{FS}$. The system is unstable for other input values for the parameter settings used in the MATLAB simulation. Stability of the system can be adjusted by varying the gain.

Simulation results are shown in Figure 4.3 for two sinusoidal inputs (Vinput) having amplitudes of $0.07V_{FS}$ and $0.2V_{FS}$. The function of the system is demonstrated. The low pass filter used was a 2^{nd} order butterworth filter having a cut off frequency of 10KHz.

The advantage of this configuration is the signal being digitized as close as possible to the antenna. Currently AGC systems are implemented purely in the analog circuit domain. The addition of the ADC enables the latter part of the system, i.e. rectification and filter circuits to be implemented in the digital domain. This reduces circuit complexity by conveying the signal preconditioning into the digital domain as shown above in Figure 4.2.

CHAPTER 5

CONCLUSION AND SUGGESTIONS

The growth in the use of digital systems has increased the use of monolithic high-speed and high resolution ADCs as the interface for the acquisition and measurement of many signals that exist in the real world as analog signals. Especially in personal mobile communication systems, low power consuming, fast, and low cost ADCs are in great demand. Furthermore large die size and process bandwidth requirements have prevented integration of ADCs with VLSI digital signal processing. To this end a 4-bit 1Gsps high-speed low-power flash ADC has been developed in this study.

This study investigates design requirements of ADCs. It starts out by introducing different types of ADCs and discusses in detail the system building blocks of the flash or parallel type ADC. Then design considerations of flash ADCs and factors that limit accuracy are discussed. ADC converter specifications that are used to measure ADC performance are described in detail. Lastly in this section, ADC static and dynamic test procedures are discussed.

The unique design of the 4-bit flash ADC in this study uses inverters as comparators. Each inverter in the comparator bank has a unique trip voltage set by inverter transistor geometry. This design eliminates the resistor string along with its

power consumption, resistor string bow effect error, and element mismatches. A feedforward stage amplifies the quantized signal. The thermometer code output of the feed forward stage is then applied to the bubble detector stage were error correction techniques are used to obtain an addressable code that is used by a 4-bit encoder. The encoders are regenerative providing fast circuit performance to produce a digital word equivalent of the thermometer code that represents the input voltage level. Pad drivers are then used to drive the output pads and external circuitry.

Simulation and test results obtained from this ADC design that were fabricated on IBM 0.1μm, MIT/LL 0.25μm, and Peregrine UTSi 0.25μm process have revealed its full potential for low power and high-speed performance. Testing the full 4-bit ADC has proved functionality so far. The speed performance though was not up to expectations. Reasons for this is because of inadequate decoupling capacitance and parasitic inductance in the power supply lines.

Test results also revealed that the outputs were not synchronized. This added error values to the output. To eliminate this problem, latches need to be added to the existing design either at the sixteen bubble detector outputs or at the four encoder outputs. Simulation results obtained from this improvement will be used to decide the final location of latches. To further improve this flash ADC design, pipelining techniques can be applied to improve the throughput.

This new ADC system can be used for a time-interleaved ADC that uses M number of flash ADCs operating at a much lower speed but combined together operate at the same maximum speed as a signal ADC with the additional advantage of accuracy but at the expense of area. The flash ADC is applied in an automatic gain control systems.

The simulation proves that the system is feasible. Its advantage is that part of the preconditioning circuitry is handed over to be implemented in the digital domain which makes it is far less complex to design.

Future work will include, as mentioned above, adding latches to synchronize the outputs, layout modifications to reduce inductance in the power supply lines so that the ADC will performance at its full speed, implementing the design in an interleaved ADC and automatic gain control system.

Conclusively, a 4-bit flash ADC has been designed, simulated, and tested. The results obtained have demonstrated functionality. This system can be a solution to the problem of low power and high-speed circuit requirements in may applications especially in the telecommunications area. Flash ADCs are however limited in resolution by mismatches and area being exponentially proportional to the number of bits.

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APPENDIX A

RESISTOR STRING BOW EFFECT ANAYSIS

Figure A.1 shows a flash ADC having a resistor string that generates the reference voltages for each comparator. Looking into resistor string from the reference voltage input of each comparator, the impedance seen is different for each comparator. For a 4-bit ADC, there are 15 comparators and the middle comparator would then be the 7^{th} from the top or bottom. Impedance seen at the 7^{th} comparator is,

$$R_7 = \frac{n}{2} \cdot R // \frac{n}{2} \cdot R .$$

Where n is the number of resistors ($n=2^4=16$). The impedance seen by the comparator next to the middle comparator i.e. 6^{th} or 8^{th} is,

$$R_6 = R_8 = \left(\frac{n}{2} - 1\right) \cdot R // \left(\frac{n}{2} + 1\right) \cdot R .$$

Generalizing this equation for any ith comparator we get

$$R_i = \left(\frac{n}{2} - \left|\frac{n}{2} - i\right|\right) \cdot R // \left(\frac{n}{2} + \left|\frac{n}{2} - i\right|\right) \cdot R . \qquad \text{(A.1)}$$

Where i is the position of the comparator counting from top or bottom and satisfies the condition $0 < i < n$.

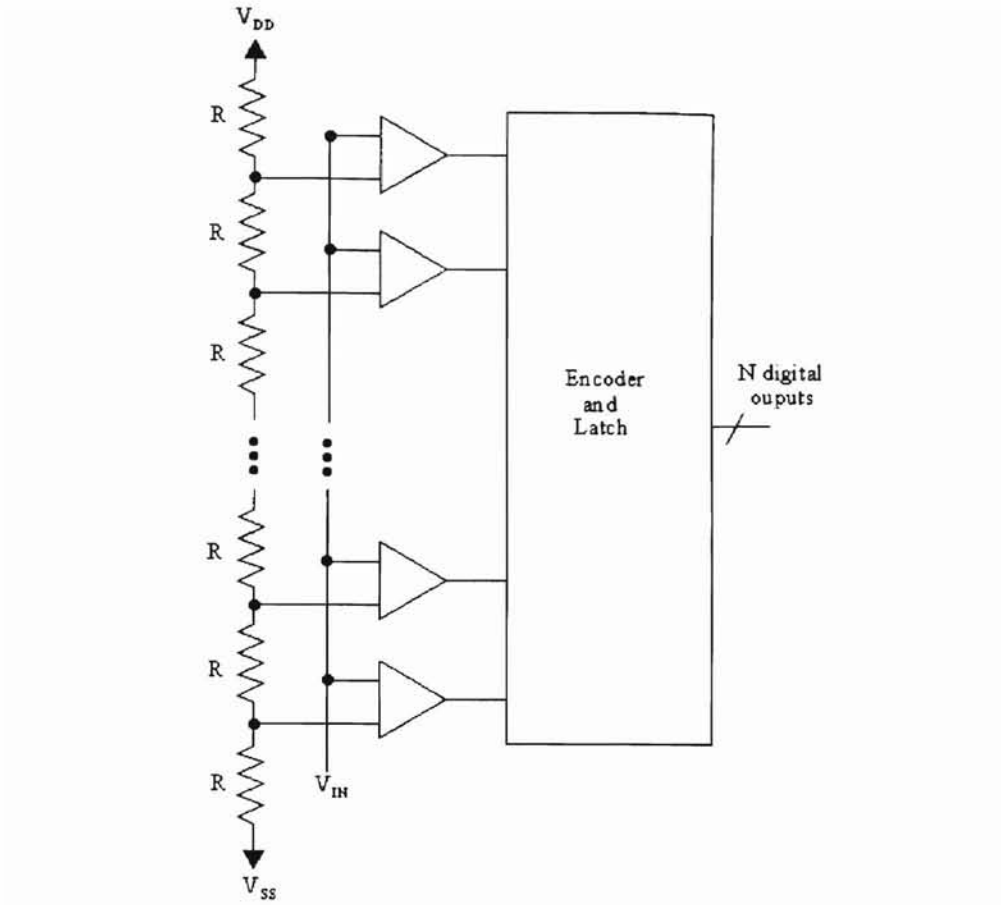

Figure A.1 Flash ADC with resistor string

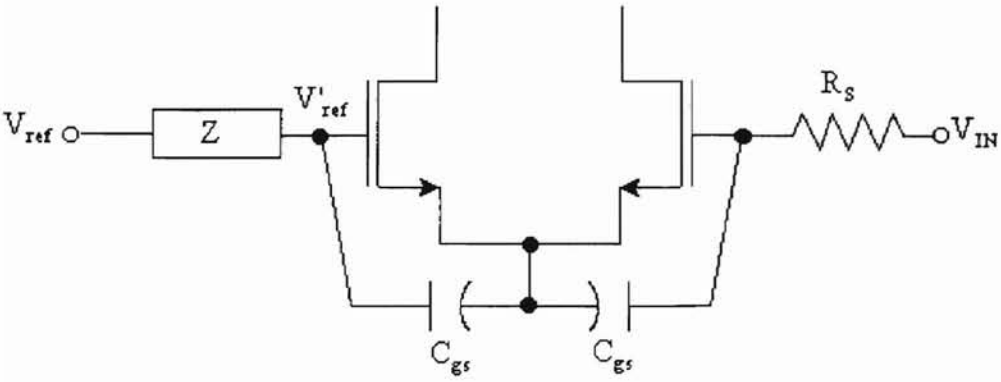

Figure A.2 Equivalent circuit at a comparator input

Figure A.2 shows the equivalent circuit at the input of a differential pair comparator. V_{IN} is the input voltage and R_S is the source resistance (50Ω). Z is the impedance looking back into the resistor string which depends on the position of the comparator discussed above. The actual reference voltage seen by the comparator is V'ref and not Vref. Therefore it is extremely important to keep Z as low as possible. According to equation A.1, the error in Vref will be greatest at the center comparator and decrease as you move away from the center. The minimum error is at the two outer most comparators. Since the error resembles a bow, this effect is known as the bow effect.

APPENDIX B

SOI PROCESS PARAMETERS

B.1 Peregrine UTSi 0.5μm model parameters

t_{ox}	10nm
u_n	$5.1x10^{-6}m^2s/V$
u_p	$2.4x10^{-6}m^2s/V$
Lmin	0.5μm
Wmin	1.2μm
Cox	$3.4515x10^{-3}F/m^2$

Table B.1 Peregrine 0.5μm UTSi process parameters

B.2 IBM SOI 0.15μm model parameters

t_{ox}	3.4nm
u_n	$400x10^{-4}$ m^2s/V
u_p	$150x10^{-4}$ m^2s/V
Lmin	0.15μm
Wmin	1.7μm
Cox	$1.0151x10^{-2}F/m^2$

Table B.2 IBM 0.15μm process parameters

B.3 MIT/LL 0.25μm model parameters

t_{ox}	7.5nm
u_n	$3.4x10^{-6}m^2s/V$
u_p	$8.16x10^{-6}m^2s/V$
Lmin	0.25μm
Wmin	1.0μm
Cox	$4.6020x10^{-3}F/m^2$

Table B.3 MIT/LL 0.25μm process parameters

APPENDIX C

IDEAL HISTROGRAM CURVE FOR A SINUSOIDAL INPUT

The histogram test for determining ADC performance is described in section 2.5.2.1. Derived below is the histogram curve for an ideal n-bit ADC. This curve can be compared with the test data generated histogram curve to determine ADC accuracy.

Let m be the m^{th} bin number of the ADC, i.e, $0<m<=2^n-1$. An equation that relates the ADC output analog voltage to the sampled input sine wave is,

$$\left(\frac{m-2^{n-1}+1}{2^n}\right)V_{FS} = \frac{V_{FS}}{2}\cdot\sin\left(\frac{2\pi f}{f_S}N_m\right). \qquad (C.1)$$

where, f is the sinusoidal input frequency, f_S is the sampling frequency, and N_m is the number of samples taken up to and including the m^{th} bin. Solving for N_m in equation C.1 gives,

$$N_m = \frac{f}{2\pi f_S}\sin^{-1}\left(\frac{m-2^{n-1}+1}{2^{n-1}}\right). \qquad (C.2)$$

A similar equation to that of C.1 can be written for m-1^{th} bin,

$$\left(\frac{m-1-2^{n-1}+1}{2^n}\right)V_{FS} = \frac{V_{FS}}{2}\cdot\sin\left(\frac{2\pi f}{f_s}N_{m-1}\right). \qquad (C.3)$$

Solving equation C.3 to find N_{m-1} gives,

$$N_{m-1} = \frac{f}{2\pi f_S} \sin^{-1}\left(\frac{m-2^{n-1}}{2^{n-1}}\right). \tag{C.4}$$

The difference between N_m and N_{m-1} equals the number of samples taken in the m^{th} bin. This is also represent the number occurrences of a particular code for the sine wave in the m^{th} bin. Therefore,

$$\Delta N_M = N_m - N_{m-1} = \frac{f}{2\pi f_S}\left[\sin^{-1}\left(\frac{m-2^{n-1}+1}{2^{n-1}}\right) - \sin^{-1}\left(\frac{m-2^{n-1}}{2^{m-1}}\right)\right] \tag{C.5}$$

where, ΔN_m is the number of code occurrences in each bin. If the test data is collected over N_{per} number of periods,

$$\Delta N_M = N_{per}\frac{f}{\pi f_S}\left[\sin^{-1}\left(\frac{m-2^{n-1}+1}{2^{n-1}}\right) - \sin^{-1}\left(\frac{m-2^{n-1}}{2^{n-1}}\right)\right]. \tag{C.6}$$

Note that equation C.6 is multiplied by $2N_{per}$ since ΔN_m is only for a half cycle. As an example let n=4, then equation C.6 reduces to,

$$\Delta N_M = N_{per}\frac{f}{\pi f_S}\left[\sin^{-1}\left(\frac{m-7}{8}\right) - \sin^{-1}\left(\frac{m-8}{8}\right)\right] \tag{C.7}$$

APPENDIX D

INVERTER TRIP VOLTAGE ANALYSIS

D.1 Derivation of equation that relates transistor width to inverter trip voltage

The drain current through a transistor in velocity saturation is,

$$I_D = k \cdot W \cdot \Delta V \tag{D.1}$$

where $k = v_{SAT} \cdot \mu \cdot C_{ox}$, W is the device width, and ΔV is the effective voltage $(V_{GS} - V_t)$.

At the voltage trip point of an inverter, both devices are in saturation. The n device current is equal to the p device current.

$$I_n = -I_p . \tag{D.2}$$

Substitute velocity saturation equation in to D.2 gives,

$$k_n \cdot W_n \cdot (V_{TRIP} - V_{SS} - V_{Tn}) = -k_p \cdot W_p \cdot (V_{TRIP} - V_{DD} - V_{Tp}) . \tag{D.3}$$

Expanding the above gives,

$$k_n \cdot W_n \cdot V_{TRIP} - k_n \cdot W_n \cdot V_{SS} - k_n \cdot W_n \cdot V_{tn} = -k_p \cdot W_p \cdot V_{TRIP} + k_p \cdot W_p \cdot V_{DD} + k_p \cdot W_p \cdot V_{tp}$$

rearranging above equation gives,

$$(k_n \cdot W_n + k_p \cdot W_p) \cdot V_{TRIP} = k_p \cdot W_p \cdot V_{DD} + k_n \cdot W_n \cdot V_{SS} + k_n \cdot W_n \cdot V_{Tn} + k_p \cdot W_p \cdot V_{Tp} \tag{D.4}$$

Substituting $V_{DD} = -V_{SS}$ and $V_{Tn} + V_{Tp} = V_{OS}$ in equation D.4 gives,

$$(k_n \cdot W_n + k_p \cdot W_p) \cdot V_{TRIP} = (k_n \cdot W_n - k_p \cdot W_p) \cdot V_{DD} + k_n \cdot W_n \cdot V_{Tn} + k_p \cdot W_p \cdot (V_{OS} - V_{Tn})$$

Further simplification gives,

$$V_{TRIP} = \frac{(V_{DD} - V_{Tn}) \cdot (k_p \cdot W_p - k_n \cdot W_n) + k_p \cdot W_p \cdot V_{OS}}{(k_p \cdot W_p + k_n \cdot W_n)} \tag{D.5}$$

Substitution $K_R = \frac{k_n}{k_p}$ gives,

$$V_{TRIP} = \frac{(V_{DD} - V_{Tn}) \cdot (W_p - K_R \cdot W_n)}{(W_p + K_R \cdot W_n)} + \frac{W_p \cdot V_{OS}}{(W_p + K_R \cdot W_n)}$$

D.2 Derivation of the trip voltage difference between two adjacent inverters

$$V_{TRIP_m} = \frac{(V_{DD} - V_{TN})(K_R W_{p_m} - W_{n_m})}{(K_R W_{p_m} + W_{n_m})} + \frac{K_R W_{p_m} V_{OS}}{(K_R W_{p_m} + W_{n_m})} \tag{D.6}$$

$$V_{TRIP_{m+1}} = \frac{(V_{DD} - V_{TN})(K_R W_{p_{m+1}} - W_{n_{m+1}})}{(K_R W_{p_{m+1}} + W_{n_{m+1}})} + \frac{K_R W_{p_{m+1}} V_{OS}}{(K_R W_{p_{m+1}} + W_{n_{m+1}})} \tag{D.7}$$

Subtract equation D.6 from equation D.7 gives,

$$V_{TRIP_{m+1}} - V_{TRIP_m} = (V_{DD} - V_{Tn}) \left(\frac{K_R W_{p_{m+1}} - W_{n_{m+1}}}{K_R W_{p_{m+1}} + W_{n_{m+1}}} - \frac{K_R W_{p_m} - W_{n_m}}{K_R W_{p_m} + W_{n_m}} \right) + \left(\frac{K_R W_{p_{m+1}} V_{OS}}{K_R W_{p_{m+1}} + W_{n_{m+1}}} - \frac{K_R W_{p_m} V_{OS}}{K_R W_{p_m} + W_{n_m}} \right)$$

Simplification gives,

$$\Delta V_{TRIP} = \frac{2K_R (V_{DD} - V_{Tn})(W_{p_{m+1}} W_{n_m} - W_{p_m} W_{n_{m+1}})}{(K_R W_{p_{m+1}} + W_{n_{m+1}})(K_R W_{p_m} + W_{n_m})} + \frac{K_R V_{OS} (W_{p_{m+1}} W_{n_m} - W_{p_m} W_{n_{m+1}})}{(K_R W_{p_{m+1}} + W_{n_{m+1}})(K_R W_{p_m} + W_{n_m})}$$

$$\Delta V_{TRIP} = \frac{2K_R \left(V_{DD} - V_{Tn} + \frac{V_{OS}}{2} \right) (W_{p_{m+1}} W_{n_m} - W_{p_m} W_{n_{m+1}})}{(K_R W_{p_{m+1}} + W_{n_{m+1}})(K_R W_{p_m} + W_{n_m})} \tag{D.8}$$

APPENDIX E

RING OSCILLATOR DELAY VERSUS PAD DRIVER DELAY

The following calculations were made using the MIT/LL 0.25μm process measured parameters. Table E.1 shows Ron values calculated from the transistor characteristic test data.

	Wn=20u	Wn=19u	Wn=12u	Wp=20u	Wp=21u	Wp=28u
Chip 1	1333	1217*	1972	421	500*	421*
Chip 2	892	1129	1842	696*	488	488
Chip 3	1400	1600	2478	1699	1522	1257

*suspect transistor

Table E.1 Ron Values for MIT/LL transistors

E.1 Ring Oscillator Calculations

Ring oscillator inverter transistor size: Wn=Wp=4μm and L=0.25μm

Using the Ron values obtained from Table E.1,

$$Ron_n = \frac{1}{3}\cdot\frac{1}{4\mu m}\cdot(1400\cdot 20\mu m + 1600\cdot 19\mu m + 2478\cdot 12\mu m) = 7345\Omega$$

$$Ron_p = \frac{1}{3}\cdot\frac{1}{4\mu m}\cdot(1699\cdot 20\mu m + 1522\cdot 19\mu m + 1257\cdot 12\mu m) = 8428\Omega$$

$$C_L \approx Cgs_n + Cgs_p$$

Note: C_L is the ring oscillator inverter load.

$$C_L = 2 \cdot \frac{2}{3} \cdot W \cdot L \cdot C_{ox} = 6.136 fF$$ Note: t_{ox} = 7.5nm and Cgs_n=Cgs_p.

$$t_{dr} = 2.2 \cdot Ron_p \cdot C_L = 113.7 ps$$

$$t_{df} = 2.2 \cdot Ron_n \cdot C_L = 99.2 ps$$

$$\tau_P = \frac{t_{dr} + t_{df}}{2} = 106.5 ps \quad \text{(E.1)}$$

$$f_{ringoscillator} = \frac{1}{2 \cdot n \cdot \tau_P} = 72.2 MHz$$ Note: n=65

E.2 Calculation of Pad Driver Rise Time (t_r)

$$C_L \approx C_{CABLE} + C_{OSCILLOSCOPE} + C_{PAD}$$

$$C_L \approx 167 pF + 30 pF = 197 pF$$ (assuming C_{pad} is negligible)

Pad driver rise time is approximated as,

$$t_r \approx 2.2 \cdot Ron_{p6} \cdot C_L$$

where $R_{on_{p6}}$ is the on resistance of the final stage inverter PMOS.

$$t_r = 2.2 \cdot 156\Omega \cdot 197 pF = 67 ns \quad \text{(E.2)}$$

The results shown in E.1 and E.2 conclude that,

Pad Driver t_r < Ring Oscillator τ_p.

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