SYSTEM LEVEL SPECIFICATIONS FOR AN INTEGRATED RF POWER SENSOR

By

VENUGOPALAN PRANESAN

Bachelor of Science

Annamalai University

Tamil Nadu, India

1996

Submitted to the Faculty of the
Graduate College of the
Oklahoma State University
in partial fulfillment of
the requirements for
the Degree of
MASTER OF SCIENCE
May, 2000

SYSTEM LEVEL SPECIFICATIONS FOR AN

INTEGRATED RF POWER SENSOR

Thesis Approved:

Thesis Advisor

Dean of the Graduate College

ACKNOWLEDGEMENTS

I should express my gratitude and appreciation to Dr. Chris Hutchens for providing me with the technical guidance and encouragement throughout my studies. I should also thank for all the personal guidance and support he had given to me. My sincere appreciation extends to my other committee members Dr. Louis G. Johnson and Dr. Rama Ramakumar.

I must thank my fiancé, Anu for her continous online support, love and understanding throughout my life here at OSU. I must express my gratitude to my parent's back home for giving me the opportunity to rise to this level in life.

Moreover, I wish to express my sincere gratitude to my colleagues Liu, Reghu, Jeff, Prasanna, Derek and Steve for all their help in the lab and also for this study. A big merci to all.

TABLE OF CONTENTS

Chapter Page

LIST OF FIGURES

NOMENCLATURE

AAF	Anti-aliasing filter
ADC	Analog-to-digital converter
AMI	American Microsystem Incorporation
A_v	OTA open-loop gain
C_{gs}	Gate to Source Capacitance of Transistor
C_{db}	Drain to Body Capacitance of Transistor
C_L	Load Capacitance
DAC	Digital-to-analog converter
DR	Dynamic range
e	Quantization error introduced in the ΣΔ loop
FFT	Fast Fourier Transform
f_N	Nyquist frequency in hertz
f_s	Sample frequency in hertz
KSPS	Kilo sample per second
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
NTF	Noise transfer function
OSR	Oversampling ratio
OTA	Operational Transconductance Amplifier
SNR	Signal to Noise Ratio
P	Average noise power
g_m	Transconductance Parameter
g_{ds}	Drain to Source Transconductance Parameter
t_{ox}	Thickness of Oxide Layer

V_{DS}	MOSFET drain to Source Voltage
V_{GS}	MOSFET gate to Source Voltage
V_{IH}	Minimum Input High Voltage
V_{IL}	Maximum Input Low Voltage
V_T	Threshold Voltage
W	Channel Width of Transistor
W_{eff}	Effective Channel width of Transistor
x	Input to $\Sigma\Delta$ loop
y	Output signal of modulator

CHAPTER 1

INTRODUCTION

The trend and growth of designing precision analog circuits that operate at low voltages is increasing exponentially. Low power dissipation eases the drive for battery operated applications. With this increasing demand for low power electronics, it is desirable to operate circuits at low power voltages while retaining good noise performance. Moreover as the speed and complexity of the circuit increases, the minimization of power dissipation and circuit simplification becomes an important design issue. The recent explosion in applications for radio frequencies (RF) and wireless systems has resulted in an extensive research and design effort to develop low power, low cost RF integrated circuits. The development of low power integrated RF power sensors open up a wide range of applications in defense and biomedical fields.

The overall goal of the project funded by SPAWAR (Space and Naval Warfare) Systems is to develop a potential single chip RF power sensor. As a part of the overall goal to develop the RF power sensor, the specific objective of this work is to determine the feasibility of stable operation on system of operational blocks, which have been

provided by the sponsor. As a result of the stability analysis, each block was re-specified in order to ensure stable and accurate operation.

1.1 System Review

Integrated RF power sensor systems can be made more efficient by sharing common modules and thereby increasing hardware utilization. This helps in decreasing the cost and area. One of the main challenges in the system is to assess the complexity, and design the system for functionality and cost effectiveness. The other challenge is to test and verify the complete system, as there are a number of potential hardware combinations. The RF power sensor is designed and fabricated on a standard CMOS process [29]. Since the performance of all the components that make up the system is important, it brings in the necessity to specify the characteristics of the system components. One aim of the thesis is to summarize the specifications for the power sensor system and also SPICE simulations, and layout for the temperature ADC. These specifications include dynamic range, signal-to-noise ratio, settling time, and bandwidth and metal migration limitations. The stability of the system is studied and frequency plots are generated using Matlab®.

The overall system consists of an RF antenna, thermopile, Correlated double sampled (CDS) amplifier, ADC, calibrated resistors, decimation filter, DSP core and temperature sensors proposed to be placed at various locations on the chip as shown in

figure 1.1. Brief discussions on the thermopile sensor, OTA and decimation filter with specifications is provided in chapter 3. The system also requires temperature sensors to be placed at different parts on chip. The placing of these temperature sensors at different locations assist in maintaining calibration and to provide the ambient temperature for correction of temperature dependent effects. The RF antenna receives the incident RF signals and instantly converts RF power to heat, effecting resistor temperature. The 50Ω resistor is implemented using poly-silicon and referred to as the characteristic impedance. The characteristic impedance and the hot junction of the thermopile are thermally isolated. The thermopile picks up the heat and converts it to voltage using the Seebeck effect [29] with a sensitivity of 3V/W. This voltage is then amplified with a correlated double sampled OTA, which is over-sampled and converted to digital using a Delta Sigma ADC. The decimation filter operates at a oversampling rate of 64 times providing a base band output at 1Kilo samples per second (KSPS). The eventual processing of all the data as well as control is to be done using a DSP chip.

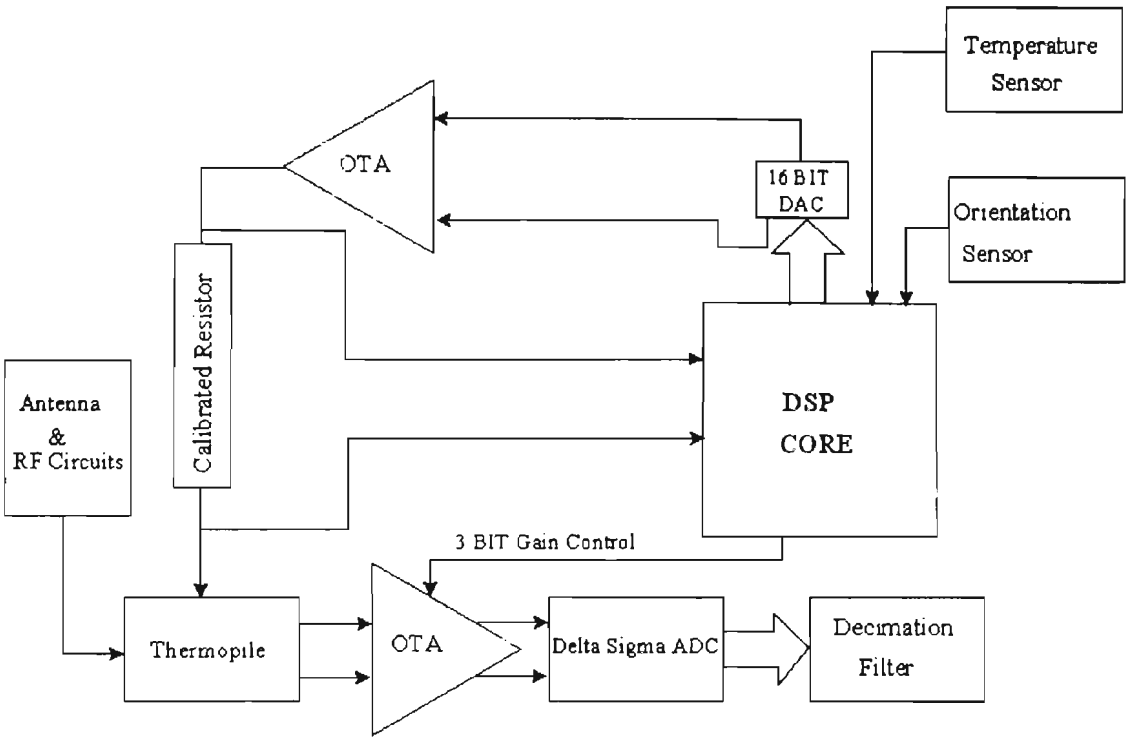


Fig 1.1 Overall System Review

The following discussion on the RF power sensor system is based on the block level diagram shown in figure 1.2, which is composed of a thermopile sensor, CDS OTA, ADC, decimation filter and a power feedback. The feedback is to compensate for the non-linear error in the sensor loop by ensuring that the sensor maintains a fixed quiscient operating point. P_{in} is defined as the input RF power and P_{fb} is the feedback power.

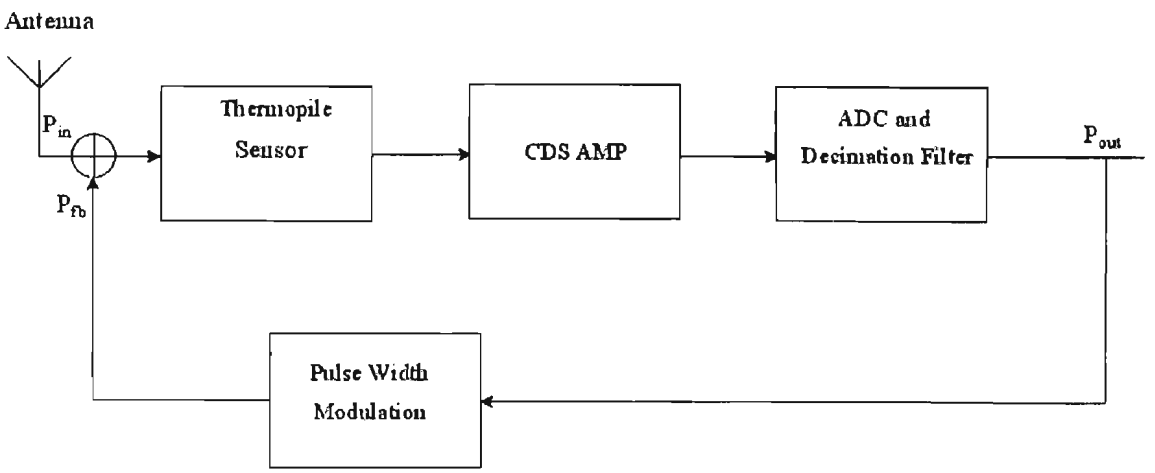


Fig 1.2 RF Power Sensor System Block Diagram

The feedback is provided by the pulse width modulation (PWM) which acts like a DAC in this case. Modulation in which the duration of pulses is varied in accordance with some characteristic of the modulating signal is defined as pulse width modulation. To achieve power integration, the bandwidth of the bipolar PWM stream needs to be greater than the bandwidth of the sensor. A bipolar PWM is used to so as to aviod dc power without creating a system disturbance.

1.2 Organization

In chapter 1, a brief review of integrated RF sensing is presented. The overall system is shown and the importance of system specification is stressed.

Noise reduction, which is essential for better system performance, is reviewed in Chapter 2. Various noise compensation techniques are covered and trade-offs are analyzed. There is also a brief review of curvature compensation for bandgap references.

Chapter 3 presents a detailed analysis of the power sensor system. The sources of noise in the thermopile sensor, dynamic range, signal-to-noise ratio, settling time and power consumption of the RF power sensor are analyzed. The analysis is based on the assumption of an ideal CDS amplifier and an ADC. This chapter gives the specification and stability analysis for the complete system.

The basic concept and the architecture for voltage and current reference are studied. Simulation results for the OTA, current and voltage reference generator, and temperature ADC is discussed in chapter 4.

In Chapter 5, conclusions based on this work and with suggestions for future work and possible improvements in the design are discussed.

CHAPTER 2

NOISE REDUCTION METHODS AND COMPENSATION TECHNIQUES

Noise in electronic circuits can be described as a disturbance, which originate from thermal, electrostatic or electromagnetic coupling sources, which are external to the circuits or can be self generated, by the circuit elements themselves. Crosstalk, which occurs between parallel wires of high-density circuits, is an example of electrostatic coupled noise.

For any system, the noise floor along with the signal amplitude determines the dynamic range. The reduction in the dynamic range due to dc offset and low frequency noise is significant. So this brings in the necessity to review the effects of noise and noise reduction in circuits.

The fundamental noise cannot be totally eliminated but it can be minimized. The various types of noise are listed below and the following sections give a brief explanation of each type of noise.

- Thermal noise
- Flicker or 1/f noise
- Shot noise
- Electronic Noise

2.1 Thermal Noise

This noise is caused by random vibration of charge carriers (electrons or holes) by the thermal excitation in a conductor. The electrons tend to vibrate in a random motion above the absolute zero having a white spectral density, which is proportional to absolute temperature. The noise power in a conductor is given by,

$$V_N^2 = 4kT\, R\Delta f \qquad (2.1)$$

where, k is the Boltzmann's constant, Δf is the noise bandwidth in hertz, and R is the resistance and T being the temperature of the conductor in Kelvin.

2.2 Flicker Noise

The 1/f noise can be observed in vacuum tubes, transistors, diodes, resistors, thermistors, thin films and even light sources. Studies have attributed the cause for 1/f noise in semiconductor, to properties of the surface of the materials [3]. The surface junctions between silicon and oxide in MOSFETS are prone to generate 1/f noise. The generation and recombination of carriers in the surface energy states and the density of

surface states are considered as important factors. The origin of 1/f noise is constantly undergoing studies. An effort to completely understand its origin is believed to help in better control of 1/f noise [7]. Carrier trapping-detrapping [5] between the transistor channel and oxide traps [5-7], and mobility fluctuations, is identified as the cause for 1/f noise in CMOS transistors [5]. The origin of low frequency noise in MOS devices is debated as to whether it is due to mobility or due to carrier number fluctuations caused by tunneling of free charge carriers into oxide traps [7].

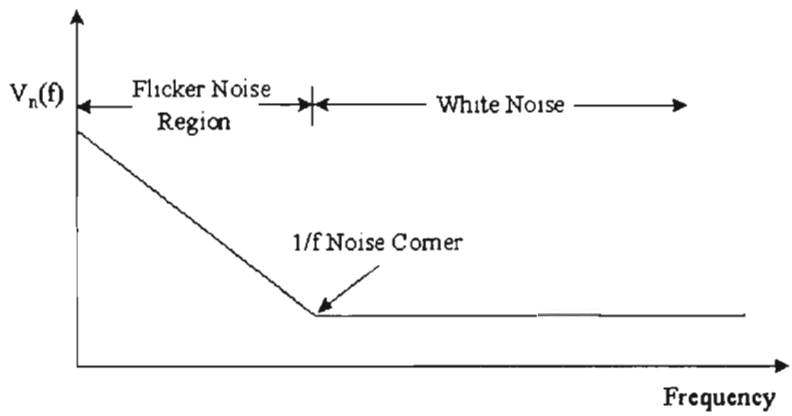


fig 2.1 Flicker noise and white noise signal

The Spectral density of noise voltage which is proportional to the mean square value of the output noise is given by

$$S_f(f) = \left(\frac{V_n^2}{f}\right) V^2 / \sqrt{Hz} \tag{2.2}$$

The 1/f noise rolls-off at the rate of approximately -10 dB/Dec and as a result inversely proportional to $\sqrt{f}$.

2.3 Shot Noise

Shot Noise is caused by the sum of energy or pulse of current caused by the movement of carriers. This impulse or surge in current results when the charge carriers crosses the potential barrier in semiconductor devices. This pulsing flow of current results in shot noise.

The root mean square of shot noise is given by

$$I_{sh} = \sqrt{2qI_{dc}\Delta f} \tag{2.3}$$

where, q is the electron charge, I_{dc} is the dc current in amperes, and Δf is the noise bandwidth.

2.4 Electronic noise

This type of circuit noise is also known as substrate and power supply noise. In circuits where the clock frequency is very high, power supply noise easily couples to the substrate and would result in errors. To minimize this noise, the analog and digital power supplies must be isolated and the clocks must be shielded from analog circuits. Making use of differential signal lines running close to each other will also minimize the coupling to the substrate.

2.5 Noise Models for Circuit Devices

The noise power equations for some of the devices are tabulated and shown in figure 2.2. In MOSFETs, the sources of noise is thermal noise, 1/f or flicker noise and shot noise and with the dominant ones being the thermal and 1/f noise. In bipolar transistors, shot noise, thermal noise and 1/f noise sources are combined into two equivalent noise sources. The main source of noise in resistors is the thermal noise. It is modeled as a voltage source in series with a noiseless resistor. All notations are the usual notations and K_f is the flicker noise coefficient.

	MOSFETS	Bipolar Transistors	Resistors
Noise Power	$V_i^2(f)=\frac{8kT}{3g_m}+\frac{K_f}{2K_p f C_{ox} W L_{eff}}$	$V_i^2(f) = 4kT[r_b + \frac{1}{2g_m}]$	$V_i^2(f) = 4kTR$

Fig 2.2 Noise power equations for MOSFETS, BJTs and Resistor.

2.6 Noise Reduction Techniques

Noise in any system is considered undesirable and needs to be removed. Complete elimination of the noise is practically impossible. However many useful circuit techniques are employed to reduce the noise and thereby increase the dynamic range.

Various approaches have been discussed to reduce the 1/f noise [8]. The first approach is to use large geometries for the input devices. This approach offers some level of noise reduction, but takes up large area for processes with high surface densities. The second approach is to use buried channel devices to isolate the channel from surface [8]. But these methods presently face manufacturing problems, as the process steps involved are not yet used for large-scale integration. The third approach, which is viewed as a more practical and effective one for noise reduction, is to use circuit techniques. The popular methods that are employed for reducing the low frequency noise are discussed in the following sections.

2.6.1 Chopper Stabilization (CHS)

The CHS technique for the suppression of low frequency noise will be reviewed and this is compared with Auto Zero (AZ) and CDS methods. CHS employs the process of modulation to transpose the signal to a higher frequency where 1/f noise is not present and demodulate it back to the base band.

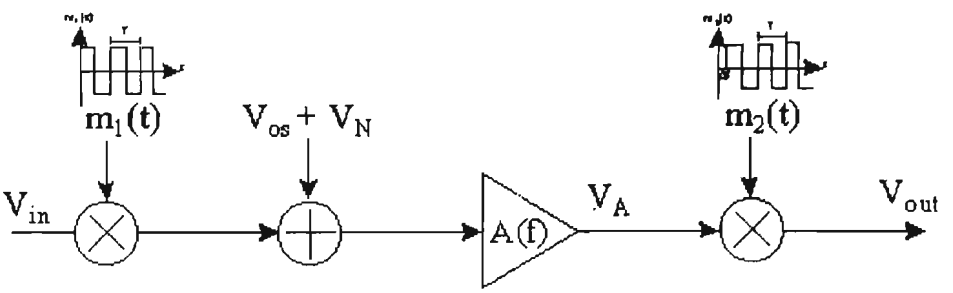
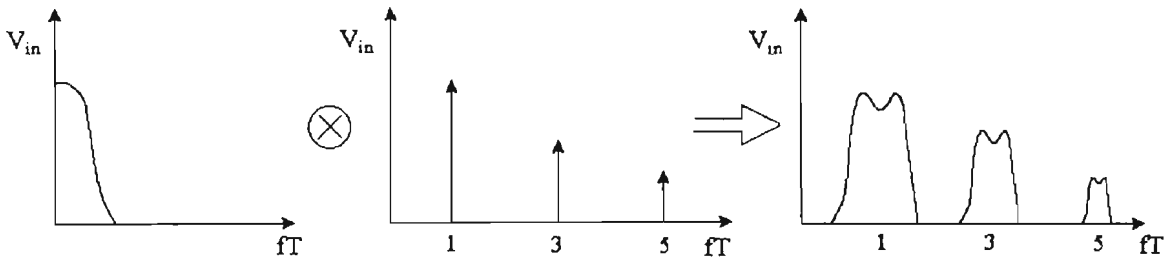
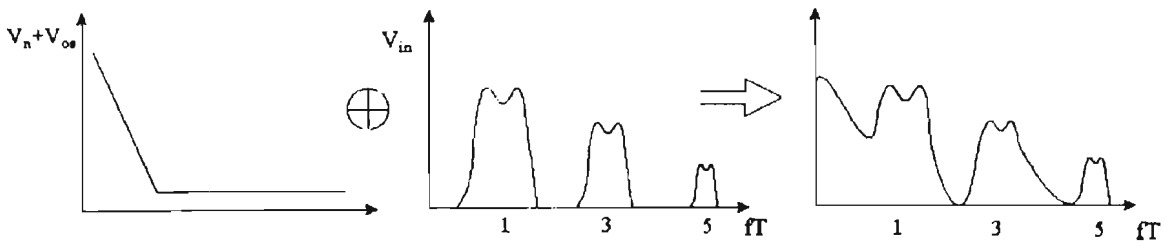


Fig 2.3 Chopper Amplification Principle

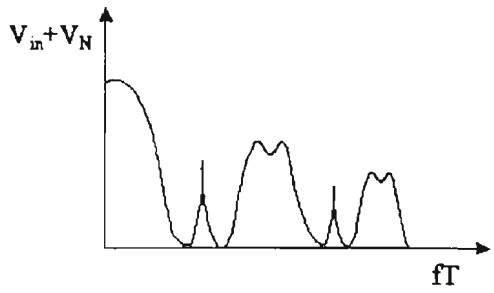
The first modulation is when the input signal is multiplied by the square wave carrier signal represented by $m_1(t)$ as shown in figure 2.3. The signal is then transposed to the odd harmonics frequencies. This is then amplified and demodulated back to the original band by multiplying by square wave carrier signal $m_2(t)$ with time period $T = \frac{1}{f_{chop}}$. The figure 2.3 graphically shows the modulation process and the waveform of the carrier signals.



(a)



(b)



(c)

Fig 2.4 Waveforms for Chopper Amplification

The waveform in figure 2.4a graphically describes the first modulation of the input signal to the odd harmonics. Figure 2.4b shows the summation of noise and offset with the modulated input signal.

The signal is then demodulated back after it is amplified, shown in figure 2.4c. The noise in this signal can be filtered out using a simple low pass filter. By this method the 1/f noise is removed from the signal.

The mathematical analysis for chopping is summarized below. The multiplication of the carrier and the input signal results in the sum and difference signals. The second multiplication by $\cos\alpha_2$, which is the carrier signal, gives back the input signal and the rest of the terms are harmonics.

$$Cos\alpha_1 Cos\alpha_2 = \frac{1}{2}[Cos(\alpha_1 - \alpha_2) + Cos(\alpha_1 + \alpha_2)] \tag{2.8}$$

$$\frac{1}{2}[Cos(\alpha_1 - \alpha_2) + Cos(\alpha_1 + \alpha_2)]Cos\alpha_2 \tag{2.9}$$

$$= \frac{1}{4}[Cos(\alpha_1 - \alpha_2 - \alpha_2) + Cos(\alpha_1 - \alpha_2 + \alpha_2) + Cos(\alpha_1 + \alpha_2 - \alpha_2) + Cos(\alpha_1 + \alpha_2 + \alpha_2)]$$

$$= \frac{1}{2}Cos\alpha_1 + \frac{1}{4}Cos(\alpha_1 - 2\alpha_2) + \frac{1}{4}Cos(\alpha_1 + 2\alpha_2) \tag{2.10}$$

From the equation 2.10, we see that the signal contains both the information and the harmonics. The $\cos\alpha_1$ term is the information and the other two sum and difference terms in (2.10) are harmonics and needs to be removed. A low-pass filter is used to remove higher order harmonics and modulated 1/f noise. A CDS amplifier should be designed such that the clock frequency is greater than the sum of the bandwidth of the information and 1/f corner frequency to effectively gain back the signal without noise.

2.6.2 The Correlated Double Sampling (CDS)

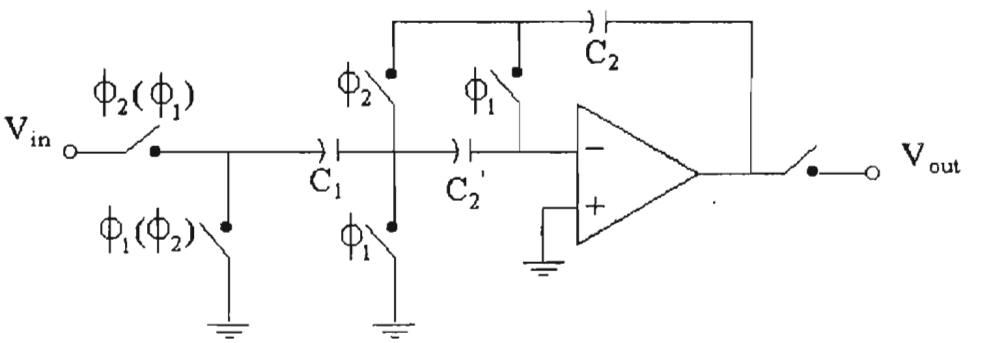


Fig 2.5 Correlated Double Sampling

This technique is useful especially in oversampling ADC designs to reduce offsets and 1/f noise because of the need for accurate integrators [10]. The technique makes use of switch capacitor circuits and using two-phase operation. The first phase also called as calibration phase wherein the finite input voltage of the OTA is stored across the capacitors. During the second phase of operation wherein the output voltage is sampled and the offset is cancelled by the switch capacitor network. A detailed description and analysis on this technique is carried out in [9]. For simplicity, figure 2.5 shows the switched capacitor circuit for implementing CDS for a singled-ended OTA. During phase ϕ_1 the offset voltage is stored across the capacitor $C_2^{'}$. This offset is cancelled as a common mode during phase ϕ_2, when the output is sampled. The merits and demerits of this method in comparison with CHS are tabulated in section 2.6.

2.6.3 Auto Zero Method (AZ)

The auto zero method removes the 1/f noise and the offset. This particular method achieves noise reduction by sampling the noise and the offset and then subtracting it from the input signal, which has the undesired components either at the output or input of the OTA. This method also involves two phase of operation. During the first phase the inputs are shorted and the offset voltage and noise voltage are stored. Here the inputs are set to appropriate common mode voltage. During the second phase of operation, the OTA is connected to the signal path and the offset is nulled by means of a

sample and hold circuit configuration or by using an algorithm [9]. The figure 2.6 shows the stages of a basic auto zeroing technique that is described here.

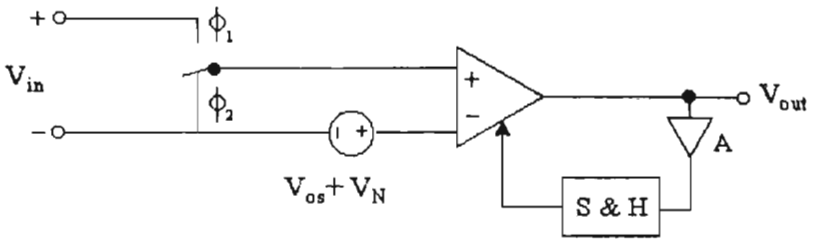


Fig 2.6 Auto Zero Technique

The dc offset noise, which is constant over time is cancelled and 1/f noise is also reduced by high pass filtering, but this increases the noise floor due to aliasing of wideband noise.

2.7 Comparison Table

CHS	CDS	AZ
Reduces the offset and 1/f noise in the circuit using sampling methods.	Uses the method of transposing and demodulation for removing 1/f and reducing the offset.	Uses the method of sampling noise and offset and subtracting from the signal.
Delay introduced by the amplifier needs to be considered for chopping.	Delays are not a problem in this method.	Delays are not a problem.
Common mode clock feed-through problems.	Common mode feed-through is less of a problem in this method.	Common mode clock feed-through problems are not seen.
Charge injection errors may be critical as switches are used. Also depends on circuit configuration.	A greater number of switches as compared to CHS and therefore the charge injection is more critical.	Charge injection is less critical in this method as number of switches is fewer.

Fig 2.7 CHS, CDS and AZ Comparison Chart

2.8 Curvature Compensation

A stable voltage reference is an integral part of any modern mixed signal VLSI circuits and its applications. Temperature stability is achieved by using curvature-compensated switched-capacitor bandgap reference [11]. The temperature stability factor plays a major role in bandgap references and this can be improved curvature-compensation. The non-linearity of the base-emitter voltage of the bipolar devices with temperature is the major reason for the temperature dependencies in voltage references.

Bang-Sup Song and Paul Gray [11], have described ways to overcome these drawbacks and circuit implementations for curvature-compensation and differential offset cancellation. The authors have implemented a ΔV_{be} ladder topology to adjust the overall temperature coefficient of the circuit. The authors chose to reduce the offset voltage of the OTA using Correlated Double Sampling (CDS) technique. A different approach to the thermal non-linearity compensation is described by Filanovsky and Yui Fai Chan. This is a BICMOS cascaded implementation to obtain the PTAT and temperature independent currents which is transmitted to the translinear circuit [12]. Third order curvature corrected bandgap reference, proposed by Jonathan M. Audy, has two additional passive resistors added to the Brokaw bandgap cell. But the circuit faces limitations due to thermal hysterisis of the transistor [14].

As there is an increased desire for battery operated systems, designers are encouraged to reduce the supply voltage lower values and also to use simpler process due

to economic reasons. A low power voltage reference is described by Kong-Meng Tham and Krishnaswamy Nagaraj whose implementation consumes less power and also achieves very high power supply rejection ratio (PSSR) [13]. The authors have presented an opamp-less voltage reference, which results in reduced silicon area and power consumption. The temperature coefficient is 85ppm/C and Power supply rejection ratio (PSRR) is 95dB at low frequencies and 40dB at 1 MHz. The authors have enhanced the circuit [15] to bring the supply down to 2.7 V without using low threshold devices.

Various techniques for noise reduction allows the designer to choose and apply the method that best suit the application. The CHS method faces clock feed-through problems and serious considerations have to be given regarding the delay due to the amplifier. The CDS method is free from these factors and so can be used for better performance in this application but does suffer from lower SNR. Curvature compensation is required to have a stable voltage reference. The ΔV_{be} ladder topology [11] is considered as one of the methods that can be applied for curvature compensation. Reducing the supply voltage reduces the power consumption, but for this application, the supply voltage has to be sufficient to account for the drop due to the resistors and diodes used for generating the reference (refer equation 4.3).

2.9 Chapter Summary

In this chapter, the basic definitions of various types of noise were reviewed. The noise models for some basic circuit elements were discussed in the earlier sections of this chapter. The initial discussion on noise is followed by a discussion on noise reduction, whose detailed analysis and discussion of which are given in latter sections. The merits and demerits of the three main compensation techniques (correlated double sampling, chopper stabilization, and auto zero) are tabulated. The chapter concluded with a brief discussion of curvature compensation for temperature stability in bandgap reference.

CHAPTER 3

ANALYSIS AND SPECIFICATIONS FOR THERMAL SENSOR SYSTEM

The thermopile, which is a set of thermocouples, uses the Seebeck effect and converts RF power to electrical voltage. This signal is amplified with a CDS amplifier and converted to digital equivalent using an ADC. Down sampling occurs in the decimation filter. The figure 3.1 shows the system blocks for the RF power sensor. A brief description of the system was provided in chapter 1.

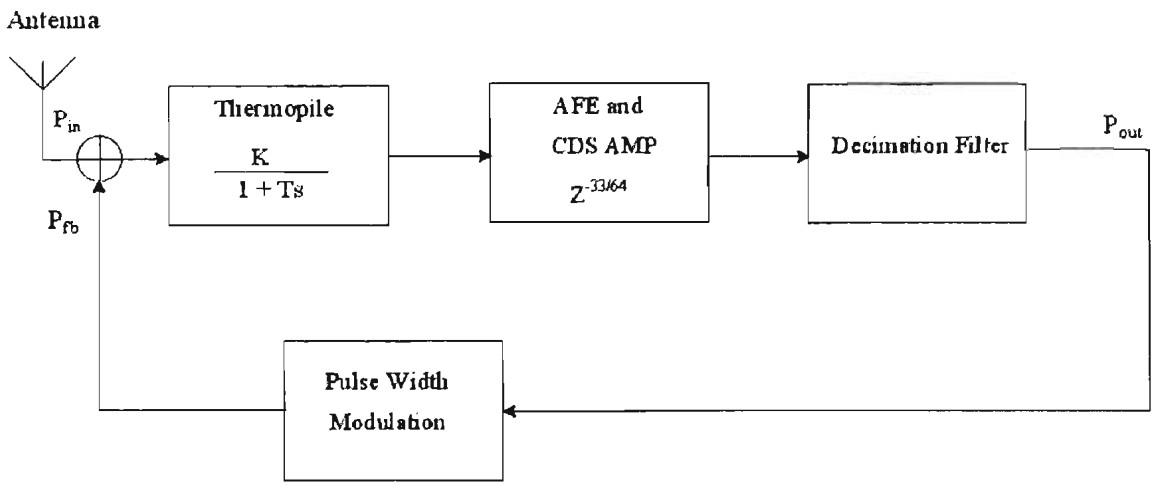


Fig 3.1 Stability issues for RF power sensor system

In this chapter, the system specifications for measures of performance including dynamic range, signal-to-noise ratio, aging and power consumption are analyzed. Stability of the system is analyzed using bode analysis for the complete RF power system which includes the thermopile sensor, CDS amplifier, ADC and decimation filter. The system is broken apart and each module is considered and analyzed separately. The overall frequency response is studied and conclusions are gathered.

3.1 Thermopile sensor

A thermopile is a serially interconnected array of thermocouples, each of which consists of two dissimilar materials with a large voltage. The thermopile is placed across the hot and cold regions of a structure and the hot junctions are thermally isolated from the cold junctions. The thermopile modeled and fabricated by Veljko of the Berkeley sensor group [29], consists of polysilicon and aluminum with the substrate acting as the cold junction. These layers are easy to implement, as they are readily available in most modern VLSI CMOS process. A number of thermopile structures have been implemented using Al/poly, Al/ p^--active, poly/p^+-active and poly/ p^- active layers [18]. The type of material chosen for designing the thermopile primarily depends on processes used and the Seebeck coefficient.

The thermopile has an output resistance of 15Kohms and an approximate capacitance of 10pf. The measured bandwidth is 160Hz with a sensitivity of 3V/W [29].

Figure 3.2 shows the measured thermopile output voltage with respect to time. The thermal time constants of the sensors were found by measuring their response with respect to an applied 1.5V input step function in ambient air and in vacuum [29]. The approximate thermal time constants of $\tau_{th} = 1.37\ ms$ and $\tau_{th} = 1.49\ ms$ were extracted, in air and vacuum respectively. The 99% settling time for the two cases is 7.42 ms and 7.85 ms [29].

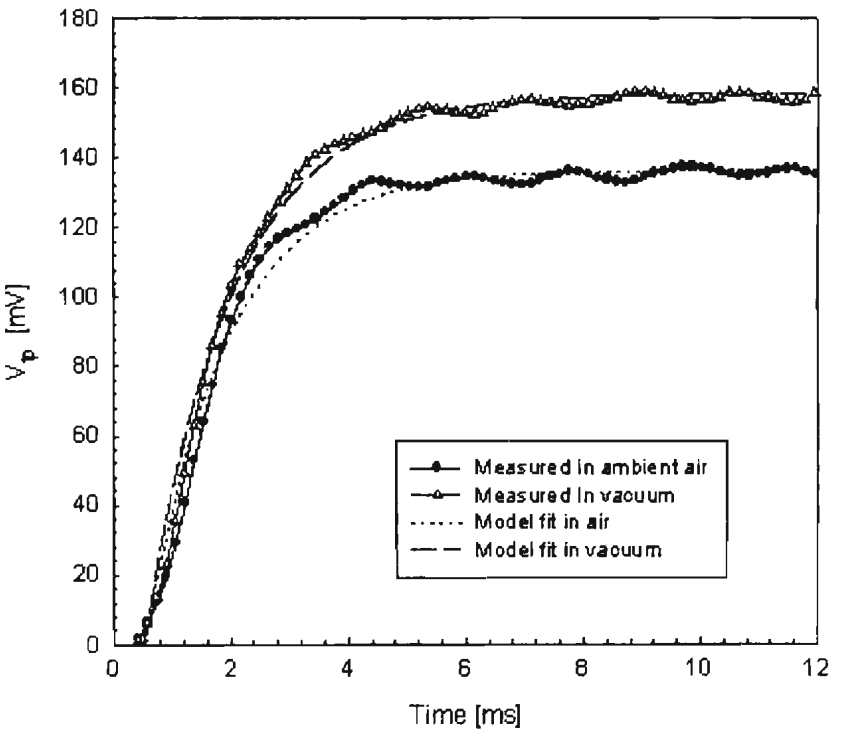


Fig 3.2 Measured thermopile output voltage in ambient air and in vacuum, as a function of time for an applied step input power [29].

3.1.1 Noise sources and Signal to Noise Ratio (SNR)

The main sources of noise are attributable to the 50Ω matching resistor and the thermopile resistance. Power loss occurs due to thermal conduction through the contacts to the substrate, radiation of heat from the resistor and by convection. Figure 3.3 shows the resistive losses to the substrate. R_{sen} is the internal resistance of the thermopile whose noise contribution is neglected for reasons discussed later in this section. Power is modeled as a current source, which is the thermal equivalent of heat. R_{sub} models the thermal resistance of the substrate to account for the heat loss while the capacitor models the thermal equivalence of heat capacity of the island of the thermopile. In this analysis η (Seebeck efficiency is assumed to be in the range of 0.1 to 0.3).

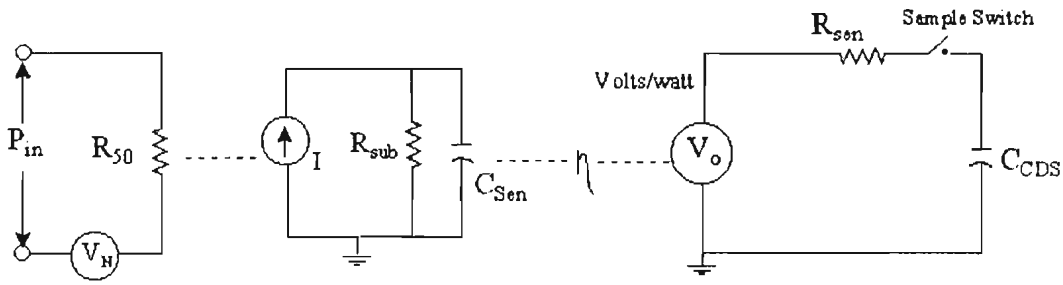


Fig 3.3 Thermopile sensor model

The noise voltage of R_{50} and R_{sen} is compared at the output of the thermopile sensor. The input RF power is given by (3.1) and using the conversion factor of K=3V/W, we can analyze the noise voltage of 50Ω resistor at the output of the thermopile.

$$P_{in} = \frac{V_{N50}^{\ 2}}{R_{50}} \tag{3.1}$$

The noise voltage of the 50Ω resistor is then given by

$$V_{N50} = 4kTKf_{44} \text{ Volts} \tag{3.2}$$

where, K is the sensitivity of thermopile and equals to 3V/W and f_{44} is the RF bandwidth which is equal to 44Ghz.

The dc noise power due to 15kΩ of the thermopile is given by

$$V_{Nsen}^{\ 2} = 4kTR_{sen}f_{sen}OSR \tag{3.3}$$

where, k is the boltzman's constant, R_{TC} is the internal resistance of the thermocouple, n is the number of thermocouples and OSR is the oversampling ratio (64).

Taking the ratio of (3.2) and (3.3), we get

$$\frac{V_{N50}}{V_{Nsen}} = \frac{4kTKf_{44}}{\sqrt{4kTnR_{TC}f_{sen}OSR}} = 137.5 \tag{3.4}$$

From the above analysis, it is seen that the noise power of the 50Ω resistor is more dominant as V_{N50}= 137.5 V_{Nsen}.

Signal to noise ratio (SNR) in a system is expressed in decibels and is defined by

$$SNR = 20\log\left(\frac{V_{inrms}}{V_{nrms}}\right) \tag{3.5}$$

Ignoring the noise power due to 15kΩ of the thermopile, as noise power due to 50Ω resistor is more dominant, the SNR relative to $1V_{rms}$ at the output is given by

$$SNR = 20\log\left(\frac{1V_{rms}}{\sqrt{4kTKf_{44}}}\right) = 86.61dB \tag{3.6}$$

Substituting the values calculated for the equation (3.6), the SNR is calculated to be 86.61 dB relative to 1 V_{rms} at the output of the thermopile sensor. In order to increase the output signal amplitude, a large number of thermocouples can be added in series. This was seen to increase the series resistance in the thermopile and thereby lowers the signal to noise ratio as reported in [29]. There is a trade off between the output signal amplitude and SNR [29]. But, it is also seen from equation (3.7) that SNR increases as square root of n with the increase in the number of thermocouples.

$$SNR = 20\log\left(\frac{nV_{in}}{\sqrt{4kTnR}}\right) \tag{3.7}$$

where, n is the number of thermocouples.

Since the noise is dominated by the 50Ω matching resistor, theoretically we can increase the number of thermocouples to 2^{17}. However practical limits on the area

restrict the number of thermocouples to 14. Figure 3.4 shows the layout of the thermopile.

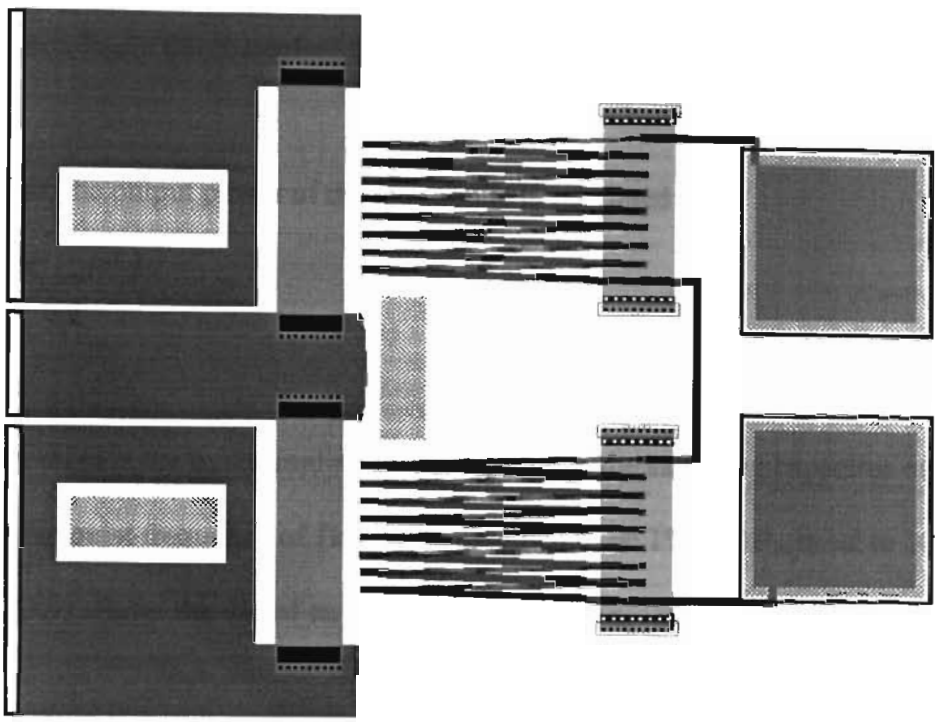


Fig 3.4 Layout of the thermopile and 50Ω matching resistor [29]

3.1.2 Power measurement

The output power level is an important factor in the RF power sensor. The reason for continuously measuring the output power of the sensor is to monitor the overall performance of the system. This output power is measured in terms of voltage or directly as power. The input power is set to 10mW for analysis purposes since the objective is to have minimum power dissipation.

During normal operations, the input power is given by

$$P = I^2 R_{50} = 10mW \tag{3.8}$$

where, R_{50} is the characteristic impedance.

Also, the output power of the thermopile is restricted by,

$$\frac{mC_{CDS}V^2 f}{2} << \eta P_{in} \tag{3.9}$$

where, m is the oversampling rate (64), C_{CDS} is the sampling capacitor of 10pF and f is the nyquist frequency of 1kHz. η is assumed to be 1% and P_{in} is set to 10mW. Equation (3.9) allows the use of an open circuit voltage measurement.

Therefore, $V << \sqrt{\frac{2\eta P_{in}}{mC_{CDS} f}}$

Substituting the values we get V<< 17.67V.

Evaluating at 10mW, the minimum measurable power is given by (3.11).

$$P_{in} << \frac{m}{2} C_{CDS} (P_{in} K)^2 f_N = 2.88E-12W \tag{3.11}$$

where, K is the sensitivity of 3V/W and f_n is the nyquist frequency, m is the oversampling rate and η is the Seebeck efficiency and P_{in} is the input power. Since measured voltage is equal to 30mV at 10mW, open circuit assumption is valid.

Oversampling at 64 increases the SNR for the thermopile sensor. The SNR for the thermopile sensor was calculated in 3.1.1 to be 86.61dB. Oversampling at 64 gives an additional 18dB (input power is proportional to $\sqrt{64} = 8$). So the SNR is increased to approximately 104dB.

3.1.3 Dynamic range of CDS amplifier

The dynamic range of the power sensor is defined as the ratio of the maximum and minimum input power, and expressed in decibels (dB). The dynamic range can be calculated from the data available.

The noise power in rms for the CDS amplifier is given by the sampling capacitor or the CDS amplifier, whichever is greater.

$$V_n = \sqrt{\frac{kT}{mC_{CDS}}} = 2.54\mu V \tag{3.13}$$

where, C_{CDS} is the sampling capacitor of the thermopile and it is assumed to be 10pF for this analysis and m is the OSR of 64. Therefore the noise voltage, V_{nrms} is 2.54μ V. The noise voltage given by SPAWAR (Space and Naval Warfare) Systems for the CDS amplifier is 0.715μV.

The dynamic range relative to 1V rms is given by,

$$DR = 20\log\left(\frac{1V}{V_{nrms}}\right) \tag{3.14}$$

By substituting the calculated values in (3.13), the theoretical value of dynamic range (DR) is calculated to be 112dB. A choice of mC equals to 640pFd is sufficient to preserve the dynamic range of the power sensor.

The figure 3.5 shows the dynamic range of the power sensor system with respect to $1V_{rms}$ at the input of the CDS amplifier. The dynamic range of the CDS amplifier is shown at 112dB and the SNR of the thermopile sensor is shown at –86dB (-104dB at OSR of 64). 10mW is set as the maximum measurable power, which corresponds to 30mV (-11dB). Giving a safety margin of 9dB, the useful dynamic range of the power sensor is seen to be 66dB. This can be restated, as for a minimum to maximum power range of 5μW to 10mW, the measured sensor voltage is 15μV to 30mV. Given that the CDS amplifier has a gain range of 50 to 1000, the CDS amplifier output voltage will be 15mV to 2.5V full-scale.

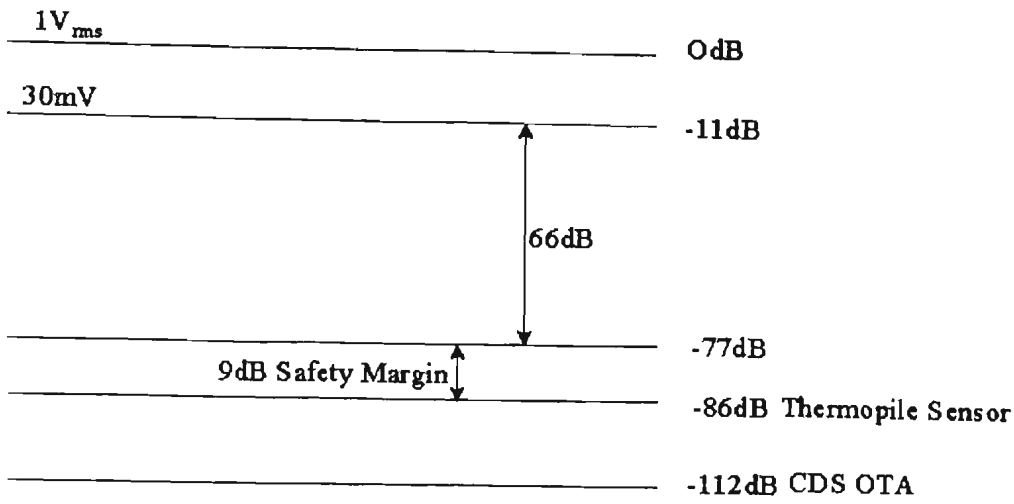


Fig 3.5 Effective Dynamic range of the RF power sensor

3.1.4 Settling time of the CDS amplifier

The settling time can be calculated by assuming the settling accuracy to n bits.

$$t_{set} \approx 2\tau \ln 2^{n+1} \tag{3.15}$$

where, t_{set} is the settling time of the node between the power sensor and τ is the time constant of the thermopile sensor output resistance and the sample capacitor of the CDS amplifier.

$$\text{Also, } mf = \frac{1}{t_{set}} \tag{3.16}$$

where, m is the oversampling ratio.

$$\text{Therefore, } mf < \frac{1}{2\tau \ln(2^{n+1})} \tag{3.17}$$

So from (3.17) we see that by keeping the settling time small, we can oversample at a higher rate. For output resistance equal to 15k and C_{eff} equal to 10pF, choice of mf equal to 64kHz is very sufficient.

3.1.5 Bode plot analysis for thermopile model

In feedback circuits it is necessary to determine the gain or the phase margin for the complete path around the loop. The phase margin is used as a measure for the stability of the system. Matlab® was used to complete the bode analysis for the transfer function of each block in figure 3.1.

The transfer fuction for the thermopile model from the experimental data is given by (3.18). Since the transfer function is in a laplace form, it is converted to z domain for furthur analysis, using the bilinear transformation.

Bilinear transformation of the laplace function to z domain is done using Tustins' approximation [20]. The following calculations are done to get the transformation.

$$H(s) = \frac{k}{1 + \tau s} \tag{3.18}$$

$$\text{where, } s = \frac{2}{h}\left(\frac{z-1}{z+1}\right) \tag{3.19}$$

Using the above approximation the tranformation for H(s) is carried out. From the thermopile data [29], the time constant τ was found to be 0.9msec.

$$h = \frac{1}{f_s} = \frac{1}{64000} = 0.015ms \tag{3.20}$$

Here f_s is the sampling frequency and after substituting for s, we get

$$H(z) = \frac{k(1+z^{-1})}{z^{-1}(1-\alpha)+(1+\alpha)} \tag{3.21}$$

Substituting value of α in (3.21), we get,

$$H(z) = \frac{3(1+z^{-1})}{116.2 - z^{-1}(114.2)} \tag{3.22}$$

The magnitude and phase plot for the thermopile sensor transfer function is plotted using Matlab® and shown in figure 3.6 and 3.7. The phase at 3dB bandwidth of the thermopile is 45 degrees at 170Hz. The x axis scale in figure 3.6 is normalized and 1 on the x axis corresponds to 500Hz.

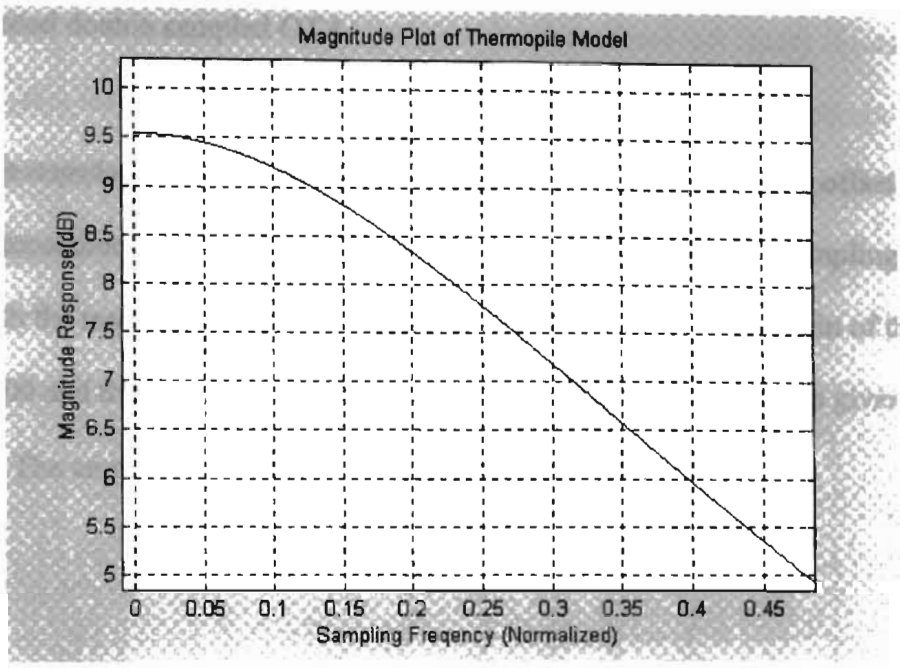


Fig 3.6 Magnitude plot for thermopile model

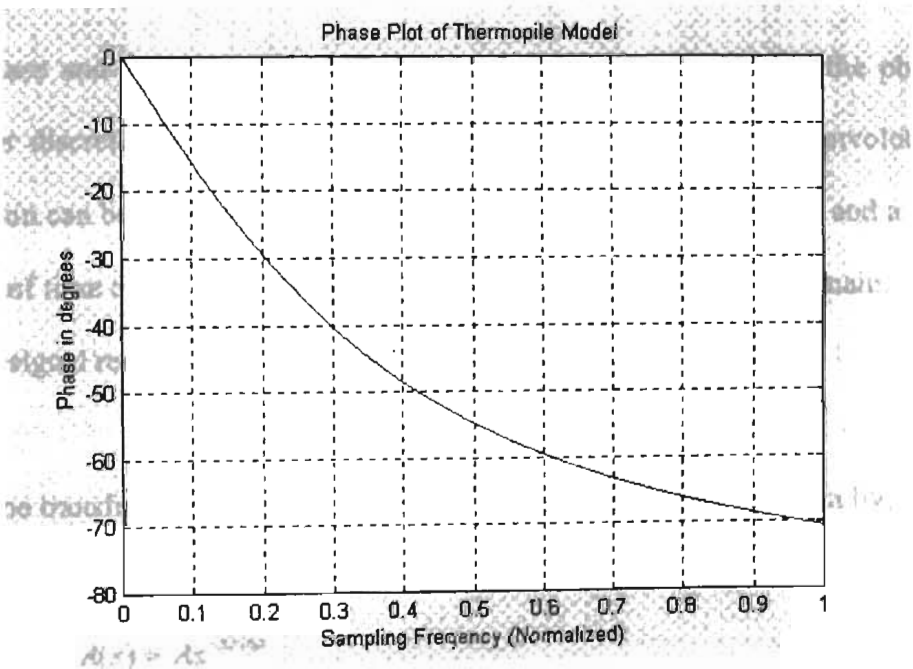


Fig 3.7 Phase plot for thermopile model

3.2 Correlated double sampled OTA

The correlated double sampling was selected to reduce noise and offset whose detailed discussion was shown in section 2.5.2. The CDS OTA has a sampling rate of 64kHz with the maximum output swing is from –2.5V to +2.5V. The gain of the OTA is around 1000 and the bandwidth product is 500KHz. The noise voltage is given to be 0.715μV. The amplifier is designed to have a gain of 1000.

3.2.1 Bode plot analysis for CDS OTA

Phase and delay are directly related. Delaying a signal shifts the phase of the signal. For discrete time signals, z-transform properties are used. Convolution in the time domain can be represented as simple multiplication in the z domain and a time delay of k units of time can be represented by multiplication by z^{-k} in the z domain. A uniform delay in a signal results in a linear phase shift.

The transfer function of the CDS OTA including the AFE is given by,

$$A(s) = Az^{-33/64} \tag{3.23}$$

where, A is the gain of the CDS OTA. Figure 3.8 and 3.9 shows the magnitude and phase plots for the CDS OTA. The phase is linear and and the magnitude is the dB value of the OTA gain. This contributes 2.85 degrees of phase to the system at 170Hz. In figure 3.8 and 3.9, 1 on x axis corresponds to 500Hz.

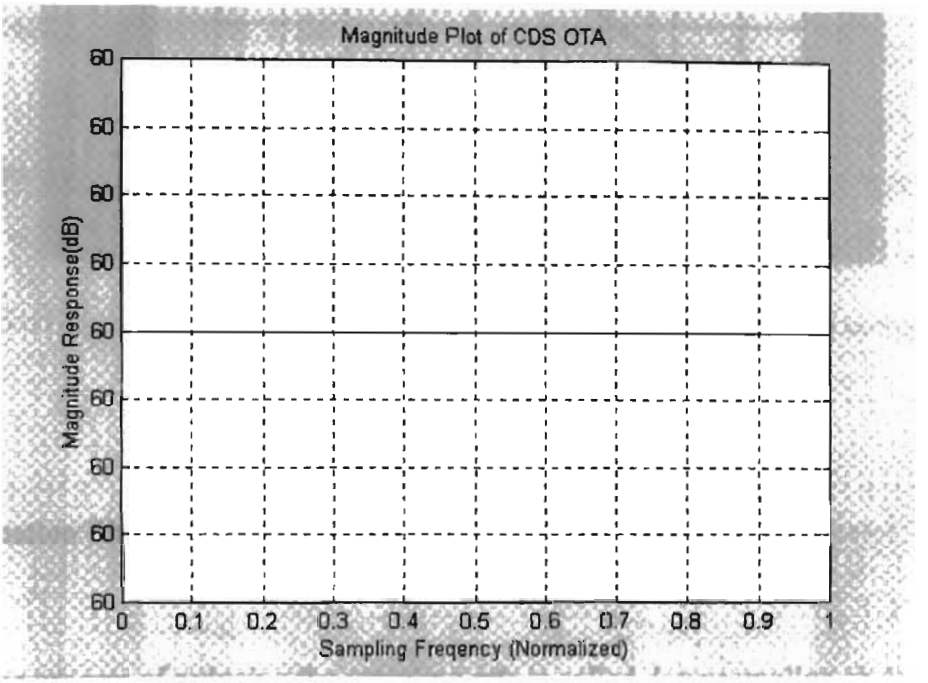


Fig 3.8 Magnitude plot for CDS Amplifier

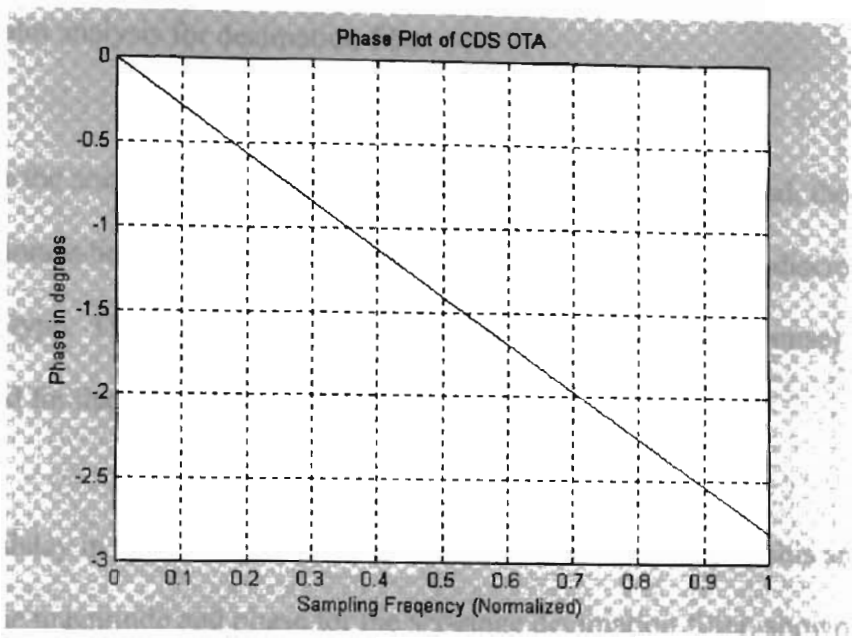


Fig 3.9 Phase plot for CDS Amplifier

3.3 Decimation filter

The process of reducing the sampling rate is called downsampling or decimation. The sampling rate can be reduced by a factor m without aliasing if the orginal sampling rate was m times the nyquist rate. If this condition is not satisfied aliasing error would result. More illustrations on downsampling are given in [19]. A system which does downsampling with a low pass filtering techniques is known as a decimator.

3.3.1 Bode plot analysis for decimation filter

Once the analog signal has been sampled and converted to digital, the signal is no longer continuous but is discrete. So the filter used for decimation is a discrete time digital filter type. This analysis was done on a FIR (finite impulse response) filter model that was used for decimation in the ADC.

The delay in the six stages of the decimation filter discussed in this analysis is uniform. The magnitude and phase for the six-stage decimation filter, shown in figure 3.10 and 3.11 (1 on x axis corresponds to 500Hz), is seen to be linear due to the uniform delay.

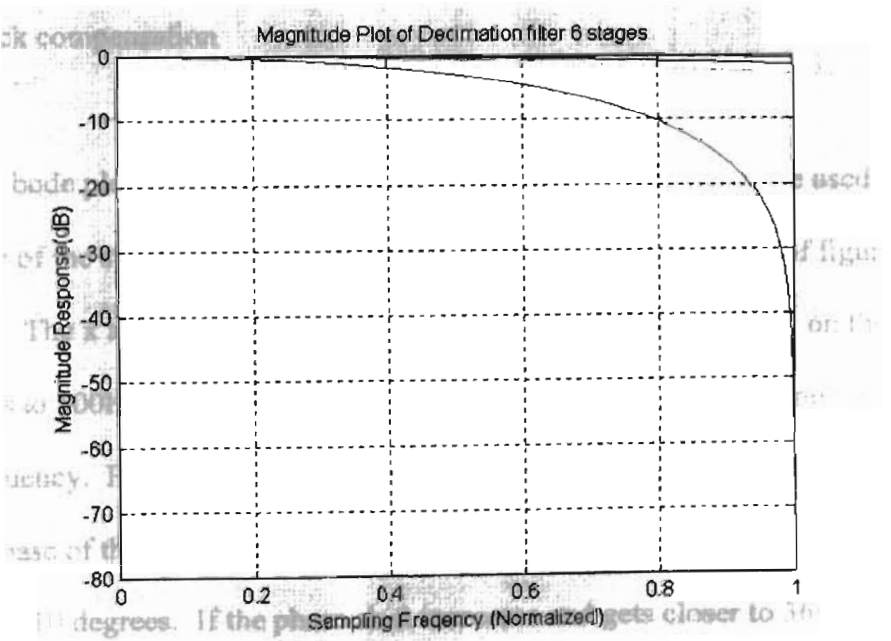


Fig 3.10 Magnitude plot for 6 stages of the decimation filter

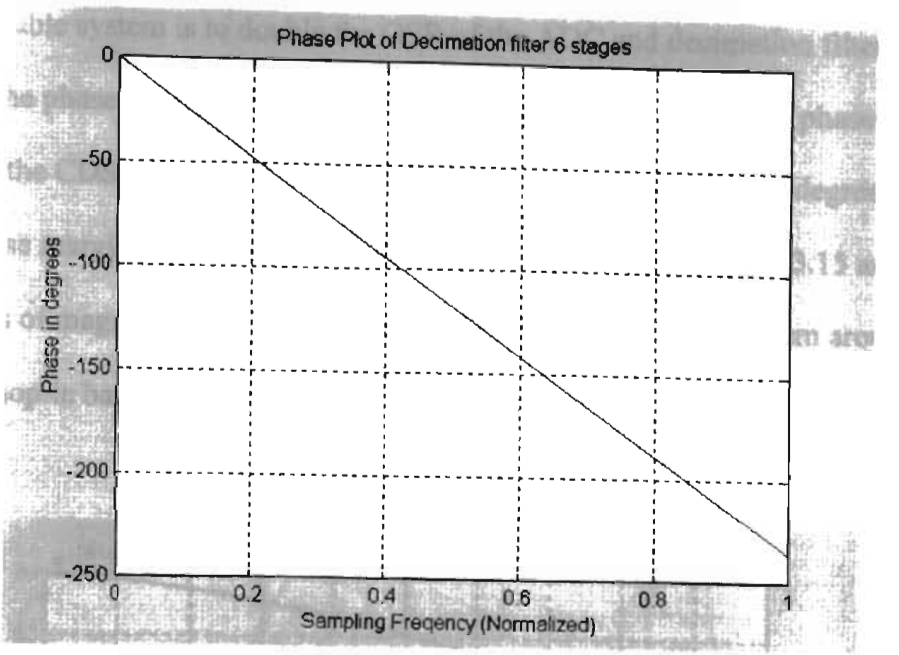


Fig 3.11 Phase plots for 6 stages of the decimation filter

3.4 Feedback compensation

The bode plot analysis that was done in the previous sections, are used to study the stability of the system and to generate the open loop bode response of figure 3.12 and figure 3.13. The x axis scale in figure 3.12 and 3.13 is normalized and 1 on the x axis corresponds to 500Hz. The phase margin for the system is 360 degrees minus the phase at 0dB frequency. For a stable system we need a phase margin of at least 75 degrees. The total phase of the complete system was calculated from figure 3.12 and 3.13 and was found to be 310 degrees. If the phase shift increases and gets closer to 360 degrees, than the system will approach instability. To achieve better phase margin of at least 75 degrees, the phase curve shown in figure 3.11 should be of 285 degrees at 455Hz. One

solution for a stable system is to double the OSR of the ADC and decimation filter, as it would reduce the phase delay by half. So by increasing the OSR to 128 the phase shift contributed by the CDS OTA, ADC and decimation filter is reduced to 110 degrees. This results in a phase margin of 160 degrees (360-200). Figure 3.14 and figure 3.15 are the magnified plots of magnitude and phase respectively, for the complete system around the region of thermopile bandwidth of 170Hz.

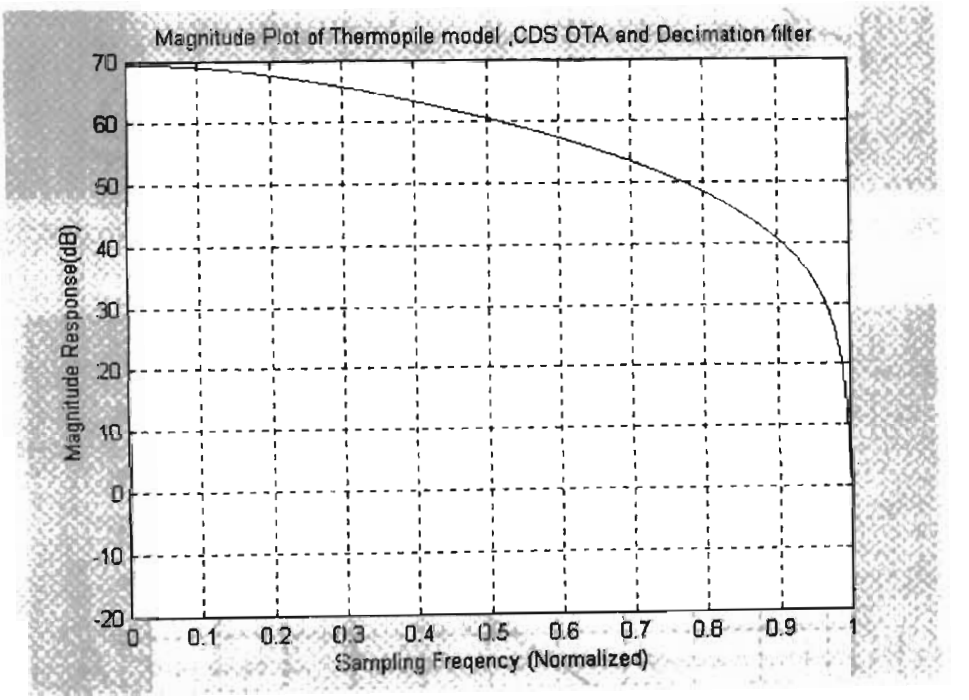


Fig 3.12 Magnitude plot for RF power sensor system

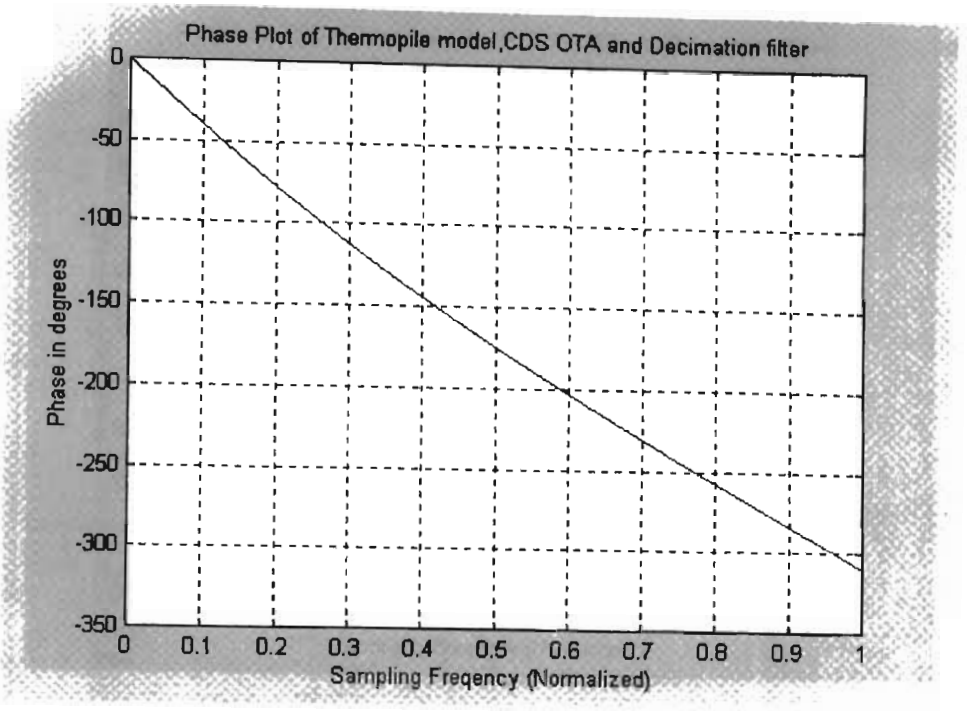


Fig 3.13 Phase plot for RF power sensor system

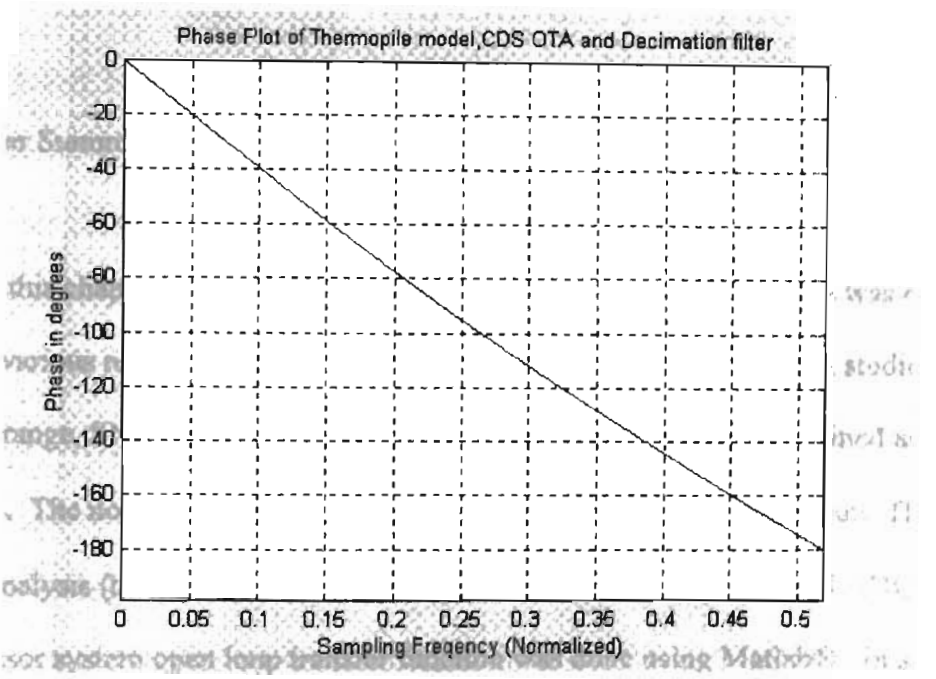


Fig 3.14 Phase plot (magnified around thermopile 3dB bandwidth) of the system

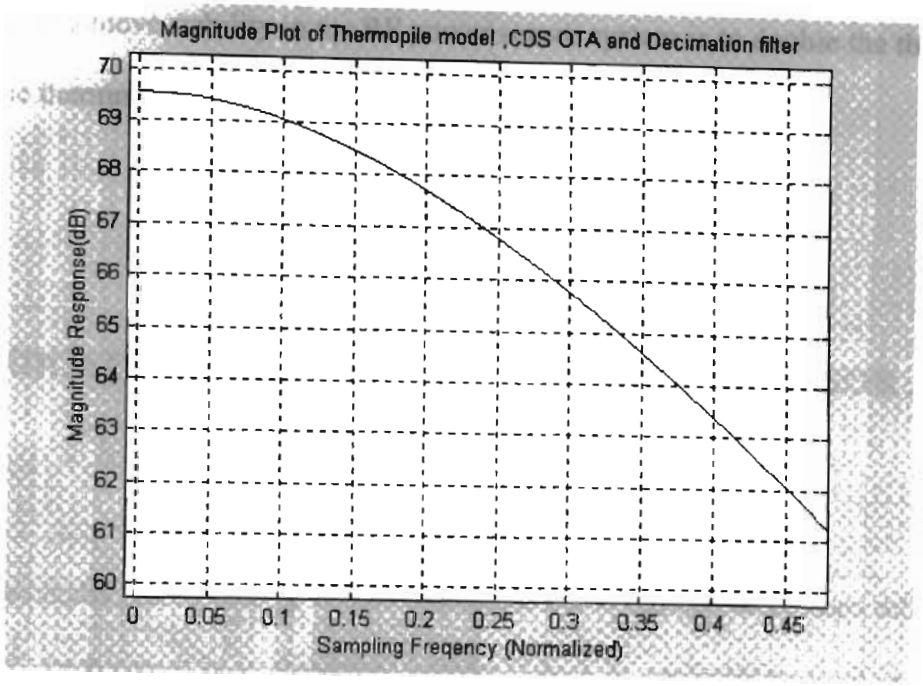


Fig 3.15 Magnitude plot (magnified around thermopile 3dB bandwidth) of the system

3.5 Chapter Summary

In this chapter a system level analysis for the power sensor system was carried out. The various noise sources in the thermopile sensor system have been studied. Dynamic range, SNR and settling time of the power sensor have been defined and calculated. The noise power due to 50Ω matching resistor is more dominant. The stability analysis (bode plot) for the thermopile sensor, CDS amplifier and ADC and the power sensor system open loop transfer function was done using Matlab®. In section 3.4, its been concluded that the system has a total phase of 310 degrees. One solution to achieve adequate phase margin is to double the OSR of the ADC and decimation filter which will reduce the phase by half and give a phase margin of 160 degrees. An

alternative to achieve stability in the RF power sensor system is to double the thermal mass of the thermopile.

CHAPTER 4

BANDGAP REFERNCE AND TEMPERATURE SENSOR ADC

Practically, every analog circuit requires a stable current or voltage reference. A voltage reference circuit is an important building block in applications such as analog-to-digital and digital-to-analog converters. Bandgap voltage references are used in data-acquisition systems, voltage regulators, and measurement and instrumentation equipment. The temperature sensor is also widely used for various practical applications. The factors that determine the type of temperature sensor required depends on temperature range, response time, sensitivity etc. In this chapter, analysis and, simulation of the bandgap reference and temperature ADC are discussed.

4.1 Bandgap voltage reference

The basic principle for the bandgap reference is to sum the base-emitter junction voltage and the voltage proportional to absolute temperature (PTAT). The base-emitter voltage has a negative temperature coefficient and while, PTAT that is the difference of two base-emitter voltages, has a positive temperature coefficient. Amplifying PTAT and

summing with V_{be}, gives a voltage independent of temperature (V_{ref}) [4]. Figure 4.1 shows the basic circuit ideas behind a bandgap reference.

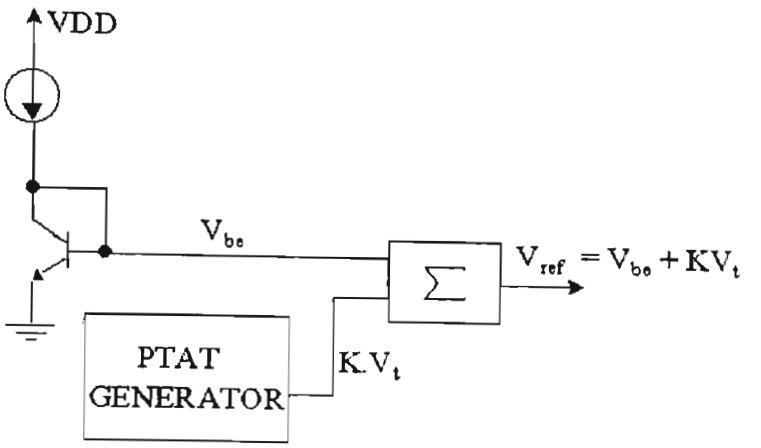


Fig 4.1 Simple Bandgap Reference

The reference voltage designed is 1.07 V and circuit operates between $\pm 3.3V$. The circuit is chopped to eliminate 1/f noise and reduce power consumption to $100\mu W$. The objective is to limit the inaccuracy to $\pm 0.025\%$ over the full range of temperature.

4.2 Temperature Sensor

The basic circuit blocks are a sensor circuit (chopped), delta-sigma ADC and a decimation counter. The current generator produces currents dependent on temperature and independent of temperature. The circuit incorporates chopper stabilization for reducing the dc offset and 1/f noise in the system. The I_{ref} and I_{temp} currents are fed to a

delta-sigma ADC, where it is oversampled and converted to digital logic data stream. The delta-sigma output is then fed to a counter, which acts as a digital decimation filter. This results in digital value of the temperature sampled. Figure 4.2 shows a block diagram of all the stages.

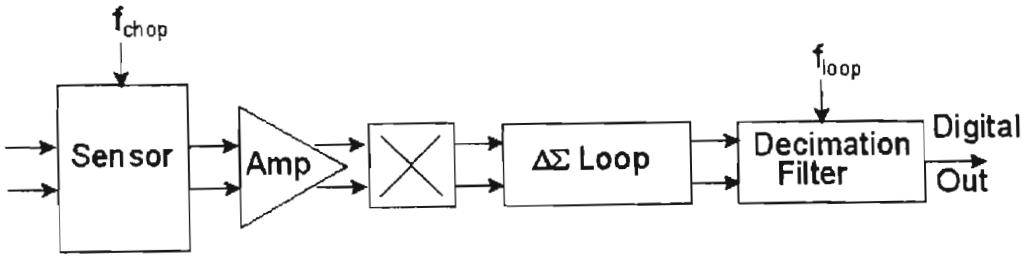


Fig 4.2 Temperature Sensor System Blocks

The power supply range is $\pm 3.3V$ and the OTA is expected to have a Power Supply Rejection Ratio (PSSR) of 60-80dB at 128KHz. The objective is to limit the power consumption of the temperature ADC to 1.6mW and the error to $\pm 1C$ over the temperature range of –40C to +120C. The input bandwidth to the delta sigma ADC is less than 1KHz.

4.3 Circuit Implementation

The circuit was implemented from the architecture that was described by Anton Baker and Johan H. Huijsing [17]. This circuit was targeted at low power, high performance, and low cost market. This circuit is claimed to consume only 7μW

operating as low as 2.2V, which ensures longer battery life. The OTA characteristics are discussed first and later the complete sensor results with respect to temperature are discussed.

4.4 OTA Characteristics

An integral piece of many analog systems is an operational transconductance amplifier (OTA). The bandgap reference, current generator and an integrator, all have the OTA as a critical block. Figure 4.3 shows the schematic for the single ended cascode OTA exclusive of the bias string.

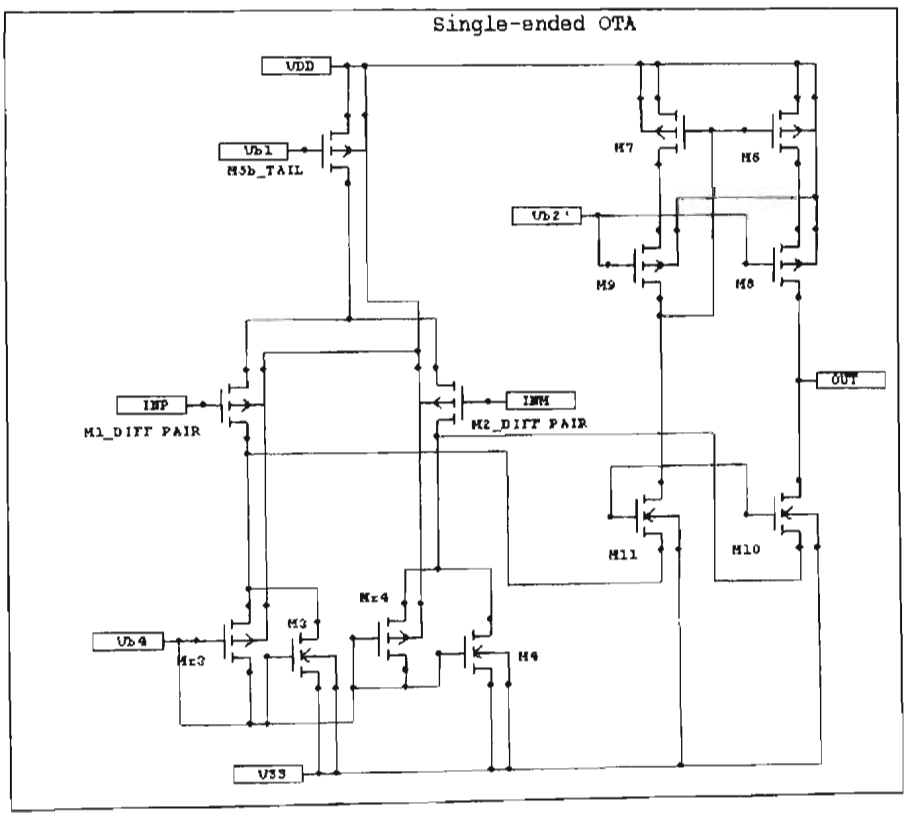


Fig 4.3 Schematic of an OTA.

The OTA circuit has the diode connected transistors, M_{r3} and M_{r4} which, improves the performance when the OTA is slew-rate limiting. During normal operation, these transistors are turned off, but during times of slewing they clamp the drain voltages of the differential pair [4].

The PSPICE simulation results for the OTA under maximum and minimum temperature ranges are discussed in the following sections. The AC analysis for the OTA is setup for simulation. The frequency response plots shows the gain and bandwidth of the OTA decreases with increase in temperature.

4.5 Gain and phase margin dependence on temperature

The gain of the OTA decreases with increase in temperature due to mobility degradation due to temperature rise. Figure 4.4 and figure 4.5 illustrates the gain reduction as temperature rises. The gain decreases by 7.8 percent while, the phase margin increases by 4.5 percent over the complete range of –40C to +120C from its nominal temperature value.

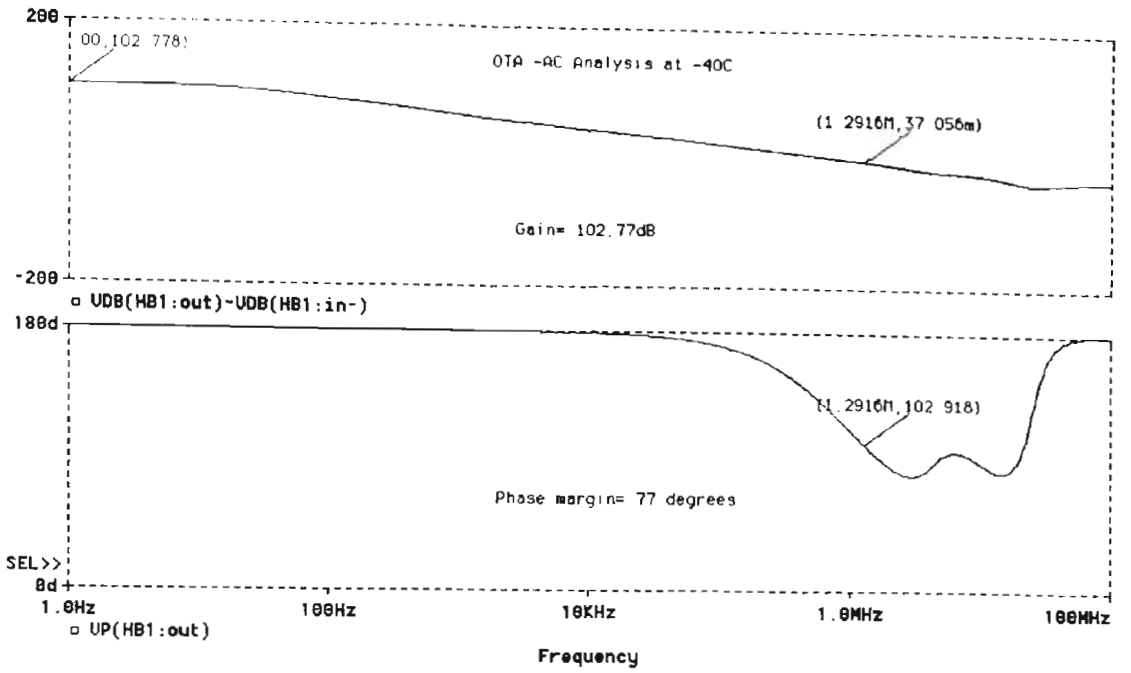


Fig 4.4 OTA Gain and phase margin plots at –40 C

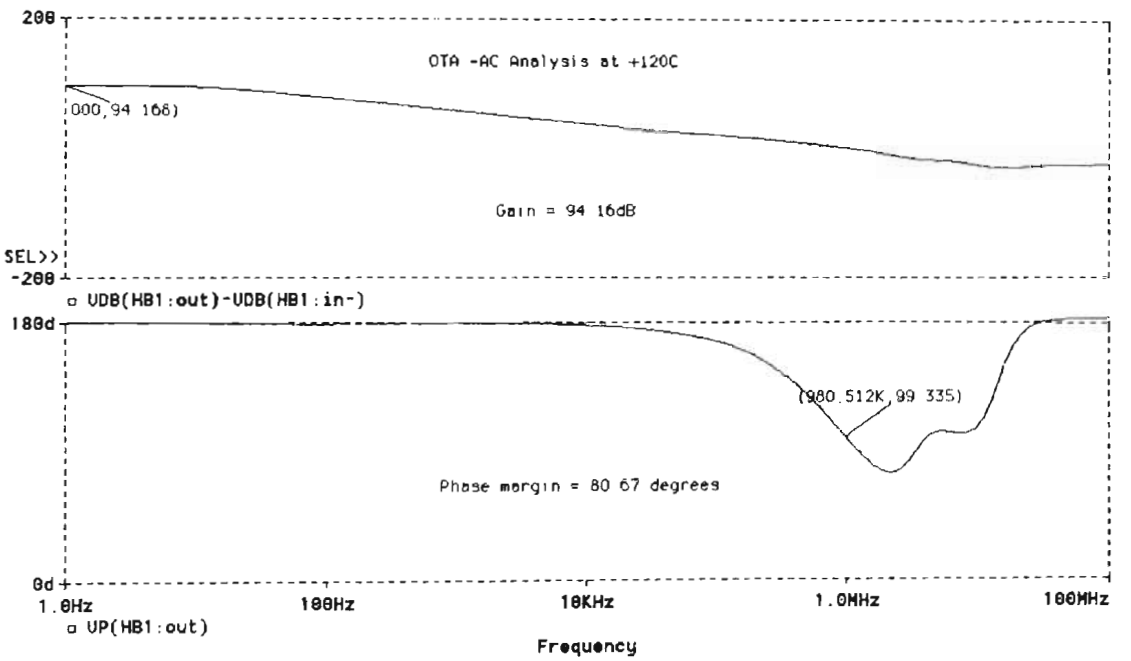


Fig 4.5 OTA Gain and Phase Margin plots at +120 C

4.6 Current Generator

The current generator circuit generates the reference current and the temperature dependent current. The reference voltage is also obtained from the same circuit. The temperature dependency is cancelled by accurate geometry scaling of the MOSFETS which is shown in equation (4.4). The OTA providing the feedback is chopped to reduce the flicker noise and minimize offset, while the voltage to current converter OTA is unchopped as the offset drift is minimal. The transistor level circuit diagram is shown in figure 4.6. The transistor geometries are calculated such that the negative temperature dependency term of I_{D4} is compensated by the additional current I_{D3} thus resulting in a current independent of temperature. The ratio of the resistors are critical in the bandgap reference.

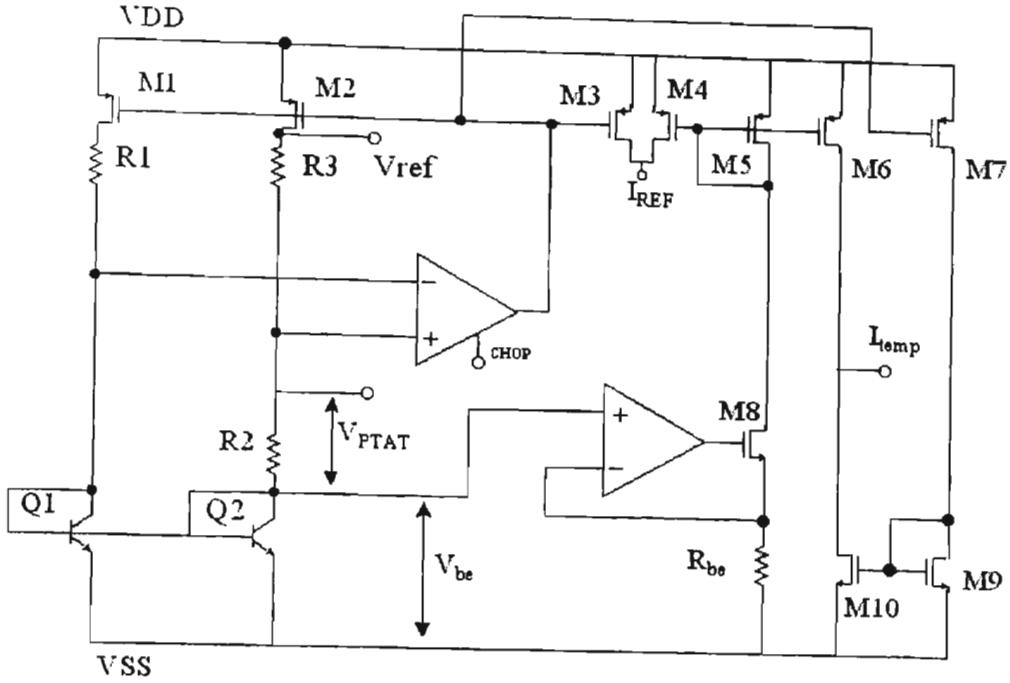


Fig 4.6 Current generator circuit

The reference voltage is given by

$$V_{ref} = V_{be2} + V_{ptat} + I(R_2 + R_3) \tag{4.1}$$

$$I = \frac{V_{ptat}}{R_2} = \frac{KT}{q} \ln\left(\frac{J_1}{J_2}\right) \tag{4.2}$$

where, J_1 and J_2 are the current densities of the collector current of the bipolar transistors. Different current densities are realized by having different values for R_3 and R_2 [4].

So, by substituting (4.2) and expanding, we get V_{ref} equation (4.3).

$$V_{ref} = V_{be2} + [\frac{KT}{q}\ln(\frac{W_1}{W_2}\frac{A_2}{A_1})]\left(1+\frac{R_3}{R_2}\right) \tag{4.3}$$

where, W_1, W_2 are widths of M1 and M2 respectively. K is the boltzman constant and q is the electron charge. A_1 and A_2 are the area of the BJT's junctions. The fingers of the bipolar pn junctions are set to 1:8 ratio to ease common centriod layout of the devices for matching accuracy.

The reference current equation (4.4) is constructed in such a way that the temperature dependent terms are cancelled. Equation (4.4) consists of three terms. The first term is the I_{ptat} (proportional to absolute temperature) and second term is the base-emitter current through R_{be} and the third term is due to the linear temperature dependence of the bipolar device. ΔT is the temperature difference. V_{be} decreases approximately at a rate of 2mV/C.

The constraining equation for I_{ref} is given by,

$$I_{ref} = \frac{W_3}{W_2}\frac{V_{ptat}}{R_2} + \frac{W_4}{W_5}\frac{V_{be}}{R_{be}} - 2mV\left(\frac{W_4}{W_5}\frac{\Delta T}{R_{be}}\right) \tag{4.4}$$

where, W_2, W_3, W_4, W_5 are the widths of the MOSFETs M2, M3, M4, M5 respectively and R_{be} and R_2 are the interdigitated resistors with a ratio of 5:1 respectively. MOSFETs M1-M2-M3 and M4-M5-M6 form mirror sets.

So from (4.2), for I_{ref} to be independent of temperature, the equation (4.3) must be satisfied. This means that the widths have to be sized such that the temperature dependence is cancelled.

$$\frac{W_3}{W_2}\frac{V_{ptat}}{R_2} = 2mV\left(\frac{W_4}{W_5}\frac{\Delta T}{R_{be}}\right) \tag{4.5}$$

Figure 4.7 shows the simulation plot for the reference current and voltages. The reference voltage is 1.07V and the reference current which is fed to the delta sigma loop is 20μA. The temperature dependent current decreases from 0 to -20μA for a full range sweep of temperature from –40C to 120C.

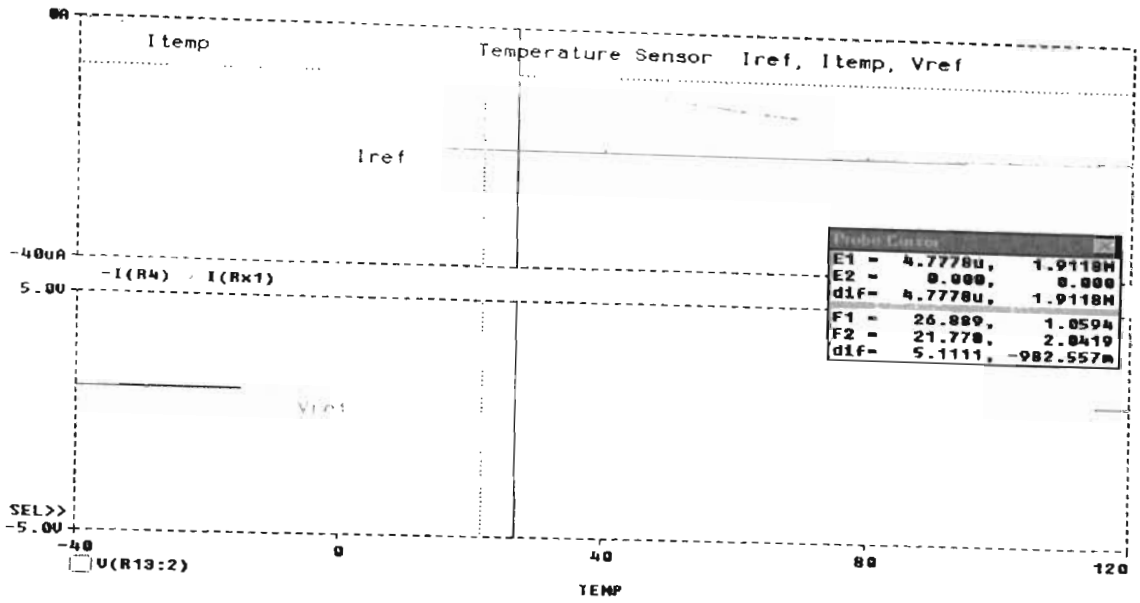


Fig 4.7 Current generator plots

4.7 Error Analysis

This error analysis is to verify the level of resolution achievable for the voltage reference and the current reference for the AMI process. The matching of the resistors is critical for the reference to achieve the specified accuracy of 14 bits. The AMI process has a matching offset of +/-0.4% error for the resistors, which restricts the references ability to achieve high resolution. The error due to the mismatch of the MOSFETs is approximated to 2% for this analysis. The verification was done using Matlab® for equations (4.6) and (4.7) and the figure 4.8 and figure 4.9 shows the variation of the voltage and current reference due to the resistor mismatch. The notations in the equations (4.6) and (4.7) are with reference to figure 4.6. In both the plots the top curve is due to the positive gradient of mismatch, which indicates that, the reference current and voltage increases with increase in temperature. Similar observation is seen for the bottom

curves in figure 4.8 and 4.9, where the reference current and voltage decreases with decrease in temperature. The middle curve is the ideal plot for voltage and current reference. The voltage reference can achieve 7 bits over the error range of +/-0.24% to +/-0.42% and the current reference can achieve 5 bits over the error range +/-0.498% to +/-2.62%. The voltage reference can achieve 10 bit of relative accuracy and the current reference can achieve 5 bits of relative accuracy.

$$V_{Eref} = V_{be2} + \frac{kT}{q}\left(\ln(1 \pm 2\varepsilon_w)\frac{A_2}{A_1}\right)\left(1 + \frac{R_3}{R_2}\left(1 \pm \sqrt{\varepsilon_{R3}{}^2 + \varepsilon_{R2}{}^2}\right)\right) \tag{4.6}$$

$$I_{Eref} = \frac{V_{PTAT}}{R_2}\left(1 \pm \frac{\Delta W_3}{W_3}\right)\left(1 \mp \frac{\Delta W_2}{W_2}\right) + \frac{W_4}{W_5}\frac{1}{R_{be}}\left(1 \pm \sqrt{\varepsilon_4{}^2 + \varepsilon_5{}^2 + \varepsilon_{rbe}{}^2}\right)\left(V_{be} - 2mV\Delta T\right) \tag{4.7}$$

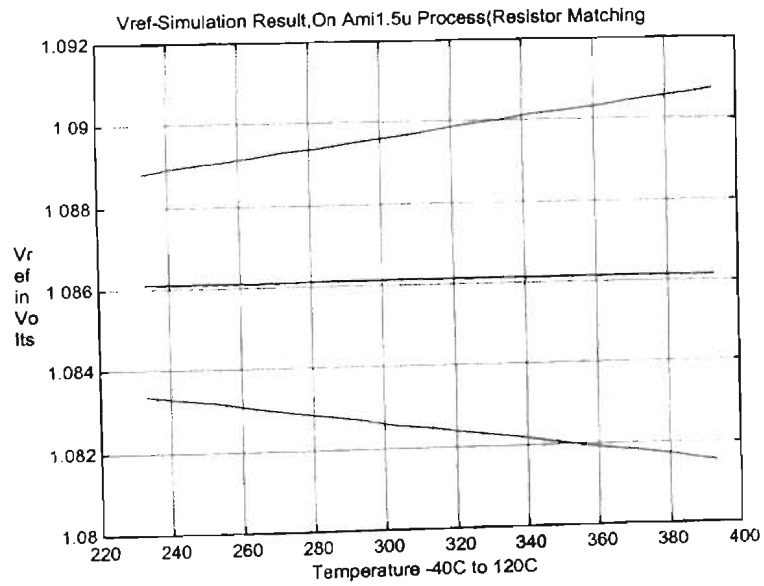


Fig 4.8 Error analysis for reference voltage

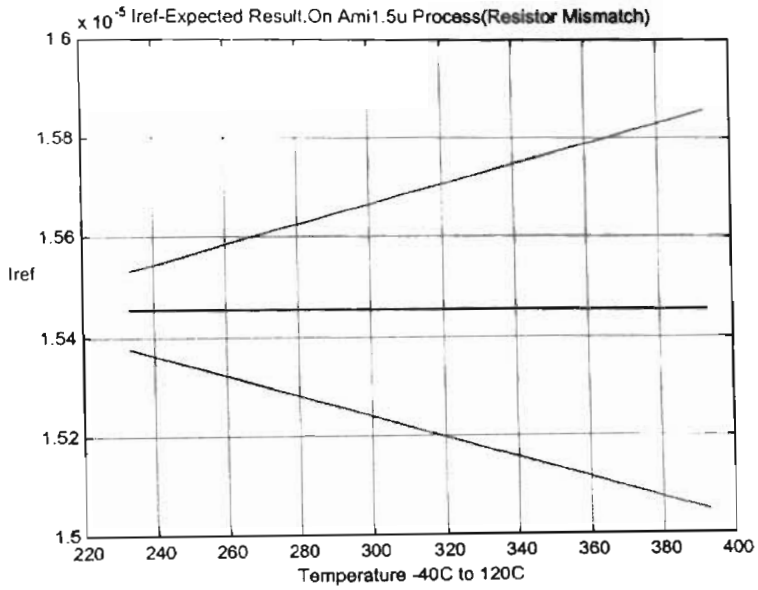


Fig 4.9 Error analysis for reference current

4.8 Temperature Sensor ADC

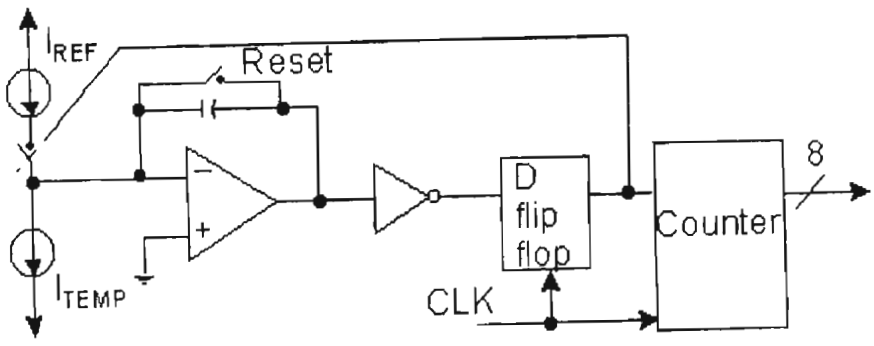


Figure 4.10 Temperature ADC blocks

The temperature ADC block level diagram is shown in figure 4.10 which consists of a first order delta sigma modulator and a decimation counter. The reference current and temperature varying current are the outputs of the current generator which are steered into the integrator of the ΔΣ modulator. Here an inverter acts as an 1 bit ADC and the output is held in the D register. The delta sigma clocks are decimated using toggle filp-flops. Brief discussions on the analysis of the ADC is shown in the following sections.

4.8.1 Delta Sigma Modulator

When many samples of a signal are taken and averaged, the averaged signal has much reduced noise level. This is the reason for using oversampling techniques. Oversampling ratio (OSR) is given by,

$$OSR = \frac{f_s}{2f_o} \tag{4.8}$$

where, f_s is the sampling rate and $2f_o$ is the nyquist frequency or the minimum sampling rate for a signal of bandwidth f_o. The advantage of oversampling with a 1^{st} order ΔΣ modulator is that for every doubling of OSR, the quantization noise power decreases approximately by 9dB or 3/2 bit.

The ΔΣ modulation combines sampling at rates well above the nyquist rate using the classical negative feedback technique to shape the quantization noise. The ΔΣ

converter used for this design is a first order loop for simplicity. The basic components of a ΔΣ loop are an analog filter and a quantizer enclosed in a feedback loop. The function of the feedback loop is to attenuate quantization noise at low frequencies. The high frequency noise is reduced by using digital low pass filtering techniques at the output of the ΔΣ modulator, which is discussed in section 3.3.

In the first order implementation, a single integrator acts as an analog filter and an inverter is a simple quantizer. The advantage of using the first order implementation is that the 1 bit DAC and 1 bit ADC are inherently linear and does not require laser trimming or calibration to obtain linearity.

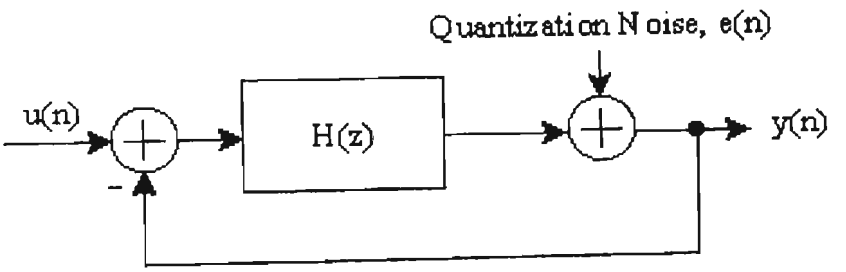


Fig 4.11 Linear model of a modulator

The signal transfer function S_{TF} and the noise transfer function N_{TF} are derived from the block level model. The model of the modulator with injected quantization noise is shown in figure 4.11.

$$S_{TF}(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)} \tag{4.9}$$

$$N_{TF}(z) = \frac{Y(z)}{E(s)} = \frac{1}{1 + H(z)} \tag{4.10}$$

where, H(z) is given by (4.11).

$$H(z) = S_{TF}(z)U(z) + N_{TF}(z)E(z) \tag{4.11}$$

H(z) can be designed with a large magnitude ranging from DC to the input signal bandwidth. The signal transfer function $S_{TF}(z)$ is unity over the band of interest and the noise transfer function $N_{TF}(z)$ is approaches zero over the same band.

The ΔΣ modulator was simulated on PSPICE®. The output waveform is shown in figure 4.12. The ΔΣ modulator implemented is a 1st order implementation and has an accuracy of approximately 10 bits with a clock frequency of 333kHz and a nyquist frequency of 2kHz with a OSR of 7 to 8.

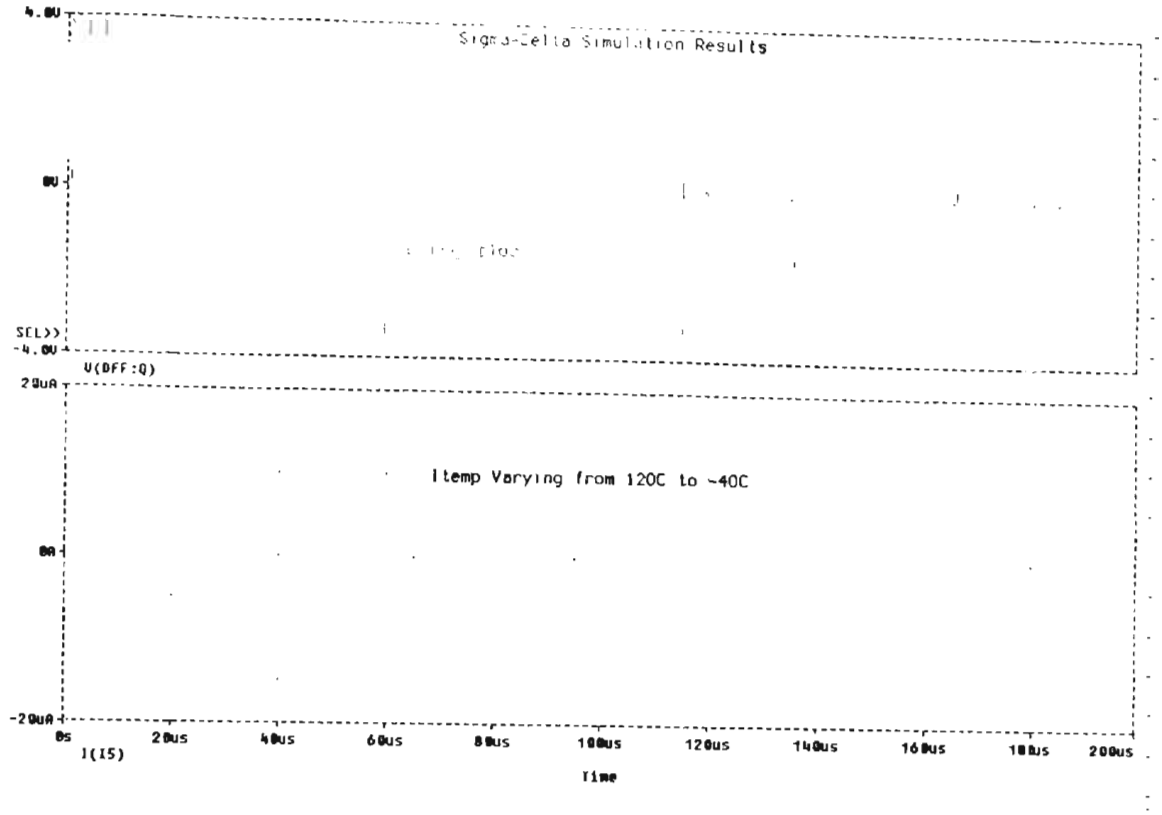


Figure 4.12 ΔΣ modulator output

4.9 Decimation filter

A digital decimation filter is used to remove the out of band quantization noise. The decimation filter implemented is a simple counter, which consists of 10 cascaded toggle flip-flops. The output of the delta sigma is averaged which also averages the quantization noise in the signal. So this acts as a digital low pass filter which removes the higher frequency signal content from the input signal. This 10 bit decimation counter averages 2^{10} bit streams giving a 10 bit digital output.

4.10 Chapter Summary

The basic concepts for the bandgap reference and temperature sensor are presented in the initial sections. The circuit level analysis for the reference and the current generators were presented and its functionality is presented. OTA, which is the main building block, is simulated under maximum and minimum temperature conditions. The complete temperature ADC is studied. The simulations have proved the functionality of the circuit and also its behavior under various conditions of operating temperature ranges. The error analysis on section 4.7 shows that the AMI process cannot be used to achieve the desired specifications, but the voltage reference can achieve a relative accuracy of 10 bits. The simulated results of delta sigma ADC is presented, with description on functionality and performance. The necessity for a decimation filter is discussed and time and frequency waveforms for oversampling ADC are also discussed.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

Power and temperature measurements are essential in a wide range of applications such as biomedical equipment, environmental control, defense applications etc. Designing an efficient circuit in terms of low power, high speed, low noise, less area and low cost is not a trivial task. There is a mutual tradeoff between these performance factors. Detailed discussions on the interaction of many of these performance factors have been presented.

The RF power sensor needs to be broad band, cost effective and portable. The essential requirement for any integrated system is to have a well-defined set of specifications. This study includes re-specifying the specifications for the RF power system with the aim of improving the performance of the complete system. Power measurement is critical for monitoring the system performance and a study was conducted to analyze its properties in the power sensor. Various sources of noise were identified and the power loss and minimum measurable converted power was

theoretically calculated. The theoretical dynamic range, response time and Signal-to-Noise Ratio (SNR) for the sensor were calculated. The useful dynamic range of the RF power sensor was calculated and found to be 66dB. The open loop stability of the system has been studied and simulated using Matlab®. Conclusively, from the discussion in section 3.4, the stability of the system may require compensation to have a phase margin of at least 75 degrees. This can be achieved by doubling the OSR from 64 to 128. So by increasing the OSR to 128 the phase shift contributed by the CDS OTA, ADC and decimation filter is reduced to 110 degrees. This results in a phase margin of 160 degrees (360-200). This will be the solution if there is an instability issue for the system. Also, it has been concluded in chapter 4 that it is not possible to achieve 14 bits of accuracy for the voltage reference and 8 bits for the current reference using AMI process. It is only possible to achieve 10 bits of relative accuracy for voltage reference and 5 bits of relative accuracy for the current reference due to the resistor and MOSFET mismatch.

The design of reference circuit and the temperature ADC was implemented on supertex2.0μm process and also fabricated on the same process through MOSIS service. The designed has also been submitted for fabrication in AMI1.2μm process. The analog design makes use of poly2 transistors as they have an advantage of having higher gate oxide and channel breakdown voltages. The design, which is the complete version of the integrated RF power sensor, has been sent for fabrication.

The specifications of the RF power sensor are tabulated and shown in figure 5.1.

SNR (Thermopile Sensor)	$SNR = 20\log\left(\frac{1V}{\sqrt{4kTKf_{44}}}\right) = 86dB$
DR (CDS OTA)	$DR = 20\log\left(\frac{1V}{V_{nrms}}\right) = 112dB$
Settling Time of CDS OTA	$t_{set} \approx 2\tau \ln 2^{n+1}$=2.70μs for 12 bits
Noise Sources	Due to R_{50} (50Ω) and R_{sen} (15KΩ). R_{50} is Dominant.

Figure 5.1 Summary of specifications for RF Power Sensor

5.2 Future work

The thermopile model exhibited non-linear phase at low frequency and this has been confirmed from the Matlab® simulation in section 3.1.5. An alternate solution is to use the pn junction diode, which can be etched for thermal isolation. Discussions regarding diode junction etching are illustrated in [31]. The idea is to have a linear sensor for the transducer. This can be achieved in the following manner by replacing the thermopile with pn junction diodes [31]. Figure 5.2 illustrates one method of this implementation.

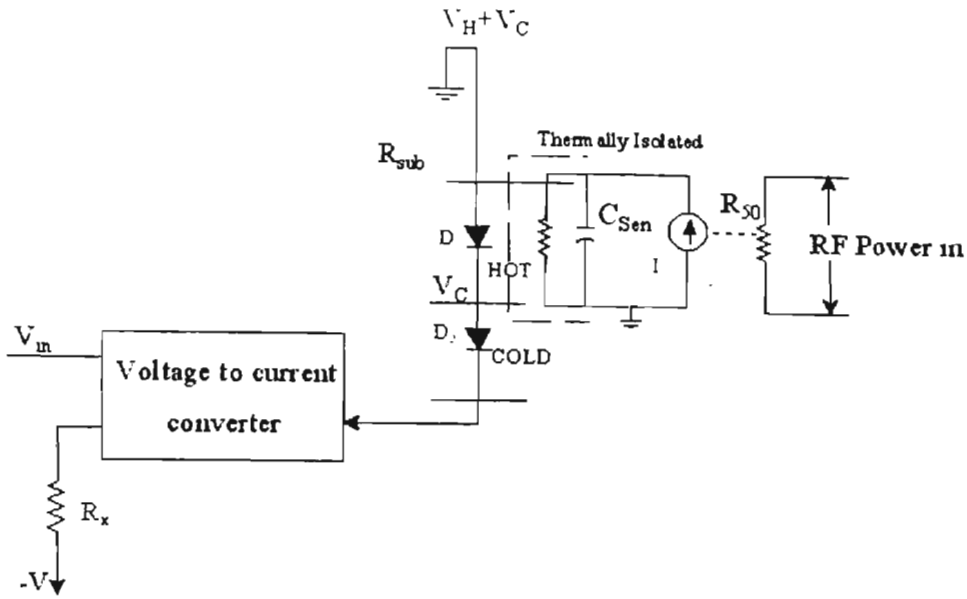


Fig 5.2 Diode transducer implementation for power sensor

The following assumptions need to be made. The currents are identical through both hot and cold diodes for two different voltages and to compensate for the thermal loss to substrate etc., thermal loss must be correctable for all hot and cold junction temperatures by direct measurement of V_H and V_c or $V_H + V_c$.

Temperature dependency can be found as follows from the diode equations (5.1) and (5.2).

$$I_{d0} \approx I_s e^{V_1/nV_t} \tag{5.1}$$

$$I_{d1} \approx I_s e^{V_2/nV_t} \tag{5.2}$$

I_s is the reverse saturation current. k and q are Boltzman constant and electronic charge, respectively and T is the absolute temperature of the junction and n is a constant, which depends on the junction material.

Dividing equation (5.1) and (5.2) and taking natural logarithm, we get

$$\ln\left(\frac{1}{\alpha}\right) = \frac{1}{nV_t}(V_0 - V_1) \tag{5.3}$$

where, α is the current ratio. By substituting for $V_t = kT/q$, we get

$$T = \frac{q}{nk}(V_0 - V_1)\ln(\alpha) \tag{5.4}$$

Using equation (5.4), the temperature can be calculated by measuring the voltage across the hot and cold junctions of the diodes. The volume of silicon for the diodes (including the etch pit) [33] was calculated and found to be approximately 45 times smaller compared to the thermopile [29]. This should result in increased response time of better than an order of magnitude.

From [29], the sensitivity of the thermopile is 3V/W [29] and from (5.4), the sensitivity of the diode transducer can be written as

$$\frac{V}{T} = \frac{mk}{q\ln(\alpha)} V/\deg \tag{5.5}$$

The diode sensor has sensitivity of (V/deg) and this is converted to V/Watts for comparing with the thermopile.

$$\frac{\Delta T}{I^2 R_T} \deg/watts \tag{5.6}$$

where, R_T is the equivalent resistance of the isolation resistance. If number of diodes (m) equals to 3 and α equal 10 then $\Delta V/\Delta T$ equals 589 uV/K or 196.3 uV/K per diode compared to 110 μV/K for a ploy-metal1 thermocouple. By using the data observations from [29], R_T is approximately equal to 4deg/mW resulting in 7.85V/W. The sensitivity can be increased by a factor of n, by stacking n diodes in the present implementation.

Based on the above discussion it can be seen that varying the diode current ratios can control the sensitivity. The thermal loss is less due to low R_{on} for diodes as compared to the thermopile sensor.

A different method of implementing a temperature sensor with a single p-n junction diode has been presented [27]. The currents through the p-n junction diode are alternatively switched between two values and their corresponding voltages are measured

and stored using a sample and hold circuit [4]. This can be implemented using auto zero technique.

BIBLIOGRAPHY

[1] N.H.E. Weate and K. Eshraghian, Principles of CMOS VLSI Design, A System Perpective, Santa Clara, CA, Addison-Wesley Publisher Ltd. 1993

[2] Johnson, Howard W., High-speed Digital Design: a Handbook of black magic. Upper Saddle River, NJ: A simon & Schuster Company, 1993.

[3] C.D. Motchenbacher and J.A. Connelly., Low Noise Electronic System Design, A Wiley-Interscience Publication.

[4] David A. Johns and Ken Martin., Analog Integrated Circuit Design, John Wiley and Sons, Inc. 1997.

[5] C.G. Jakobson, I.Bloom and Y.Nemirovsky., 1/f Noise in CMOS Transistors For Analog Applications, Technion-Israel Institute of Technology, Haifa

[6] Daniel M Fleetwod, Senior member IEEE and Timothy L.Meisenheimer, and John H. Scofield, 1/f Noise and Radiation effects in MOS devices., IEEE transactions on electron devices, 1994.

[7] L.K.J. Vandamme, Xiaosong Li, and Dominique Rigaud, 1/f Noise in MOS devices, Mobility or Number of fluctuations?, Invited Paper, IEEE transactions on electron devices, 1994.

[8] Kuo-Chiang Hsieh, Paul R. Gray, Daniel Senderowicz and David G. Messerschmitt, A Low Noise Chopper Stabilized Differential Switched Capacitor Filtering Technique, IEEE Journal Of Solid State Circuits, December 1981.

[9] Christian C. Enz, IEEE and Gabor C. Temes, Fellow, IEEE, Circuit Techniques for Reducing the effects of Opamp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization, IEEE 1996.

[10] P.J.Hurst and R.A.Levinson Delta-Sigma ADC with Reduced Sensitivity to Opamp Noise and Gain, Proc. Of IEEE trans. And Circuits and Systems, 1989.

[11] Bang-Sup Song and Paul Gray, A Precision Curvature-Compensated CMOS Bandgap Reference And Circuits and Systems, IEEE Journal Of Solid State Circuits, December 1989.

[12] I.M.Filanovsky and Yiu Fai Chan, " BICMOS Cascaded Bandgap Voltage Reference" , University of Alberata, Canada. IEEE, 1997.

[13] Kong-Meng Tham and Krishnaswamy Nagaraj, " A Low Supply Voltage High PSSR Voltage Reference in CMOS Process, IEEE Journal Of Solid State Circuits, May 1995.

[14] Jonathan M. Audy, " Third order curvature corrected Bandgap Cell", Analog Devices, IEEE 1996.

[15] J.L. Sonntag and T.R. Viswanathan, " A High PSSR CMOS Bandgap Reference," AT&T Tech. Memo. 52254-870915-12TM, Sep 1987.

[16] Tanner Tools, Tutorial, 1997.

[17] Anton Bakker and Johan H. Huijsing, Micropower CMOS Temperature Sensor with Digital Output, IEEE Journal Of Solid State Circuits, July 1996.

[18] R. Lenggenhger, H.Baltes, Digest, International Conf. On Solid State Sensors and Actuators (TRANSDUCERS '95), Yokohoma, Japan, June, 1993.

[19] Alan V.Oppenheim and Ronald W.Schafer, Discrete-time Signal Processing, Prentice-Hall, Inc. New Jersey, 1989.

[20] Karl J. Astrom and Bjorn Wittenmark, "Computer Controlled Systems", Prentice-Hall, Inc. New Jersey, 1984.

[21] Chia-Ming Liu and Dr. Chris Hutchens, "Low power decimation filter design for delta sigma converters", Advanced Analog VLSI Design Center, Oklahoma State University, 1999.

[22] Bernhard E. Boser and Bruce A. Wooley, "The Design of Sigma-Delta Modulation Analog-to-Digital Converters", IEEE Journal Of Solid State Circuits, Dec 1988

[23] J.C.Candy, " Decimation for sigma delta modulation," IEEE Trans. Commun.,vol. COM-34, Jan. 1996.

[24] Godi Fischer and Alan J.Davis, "Alternate topologies for Sigma Delta Modulators- A Comparative Study", IEEE, Trans. On Circuit and Systems, Vol 44, Oct. 1997.

[25] Chi-Tsong Chen, " Analog and digital control system design", Sauders College Publishing, 1993.

[26] T.Hayashi, Y.Inabe, K.Uchimura, and A.Iwata, " A multi stage delta sigma modulator without double integrator loop, " IEEE ISSCC Dig.Tech papers, pp. 182-183, Feb. 1986

[27] Raimundo Carlos, Serigo Daher, and Gurdip singh deep, senior member, IEEE, " A Highly Linear Single p-n junction Temperature Sensor, IEEE Trans. On Intrumentation and measurements, Apr. 1994

[28] Soon G. Lim, " A 2KSPS 1mW Low power multibit delta sigma modulator with 16bit dynamic range, Oklahoma State University, May 1999.

[29] Veljko Milanovi, "Micromachined Broadband Thermocouple Microwave Power Sensors in CMOS technology", The George Washington University, Jan 1999.

[30] T. Takken and D. Tuckerman, "Intergral Decoupling Capacitance Reduces Multichip Module Ground Bounce," IEEE Trans. On Electron Device. Vol. ED-32 No.12 pp79-84, 1993

[31] George T.A. Kovacs, Micromachined Transducers Source Book, WCB McGraw-Hill, Inc., Ney York, 1998.

[32] Laker Sanaer, Design of Analog Integrated Circuits and Systems. Princeton Road, Hightstown, NJ: McGraw-Hill, Inc., 1994.

[33] Tanner Tools. Pasadena, CA: Tanner Research, Inc. 1996

[43] Yuan Taur et, al "CMOS Scaling into the Nanometer Regime", Proceeding of The IEEE, Vol.85, NO. 4, pp486-504, April 1997

VITA

Venugopalan Pranesan

Candidate for the Degree of

Master of Science

Thesis: SYSTEM LEVEL SPECIFICATIONS FOR AN INTEGRATED RF POWER SENSOR

Major Field: Electrical Engineering

Biographical:

Personal Data: Born in Chengalpattu, Tamil Nadu, India on 10th February 1973, and the proud son of Pranesan and Bagyavathi.

Education: Completed High School at St.John's School, Beasant Nagar, Madras, in March 1992. Completed Bachelor of Engineering in Electrical Engineering from Annamalai University, India, in March 1996. Satisfied requirements for Graduate studies with a major in Electrical Engineering at Oklahoma State University in May 2000.

Experience: Raised in Besant Nagar, Madras, India; employed by Oklahoma State University, School of Electrical and Computer Engineering as a research assistant from February 1998 to February 2000; Currently working for LSI Logic Corporation, Fort Collins, Colorado.

Professional Memberships: The Institute of Electrical and Electronics Engineers.