FABRICATION OF POLY-SI NANOWIRE DEVICES

FOR THERMOELECTRIC CHARACTERIZATION

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FABRICATION OF POLY-SI NANOWIRE DEVICES

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ABSTRACT:

Thermal conductivity measurement is always a challenge and difficult task for thermoelectric characterization of semiconductor nanowire. A process flow for poly-Si nanowire device fabrication is been reported in this thesis. The device includes the nanowires as a part of its fabrication which avoids complicated placement of nanowire on the device for experiment and also avoids the contact resistance on the both sides of nanowire. The process flow is repeatable, reliable, and able to produce functional devices. Specifically, processes were found in this research to optimize the stress of Si nitride thin films and isotropic etching of Si substrate by using particular gas mixtures. By this device, thermal conductivity of nanowires of any materials compatible to micro/nano- fabrication, can be measured rather than poly-Si nanowires only.

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CHAPTER I

INTRODUCTION

Modern infrared (IR) detector technology basically originated during the Second World War. IR detectors have been essential for today's digital battlefield. IR detectors are used not only for military applications, but also in many other emerging fields, for example: medical diagnosis, vehicle safety etc. [1, 2]. Thermal detection is a widely used mechanism for IR detection because of its low cost, capability of operating at room temperature, and response to a wide range of IR spectrum.

Human eyes can sense only a small portion of the electromagnetic spectrum. The electromagnetic radiation spectrum includes many types of radiations: gamma ray, X-ray, radio wave, visible light, microwave, infrared, etc. The spectrum is divided into different classes based on the frequencies or wavelengths. We know that the relationship between the frequency and wavelength of electromagnetic wave is given by:

$$c = f\lambda \qquad\qquad (1.1)$$

Where, f and λ represent the frequency and the wavelength respectively of the electromagnetic wave and c is the speed of light. Therefore in the electromagnetic spectrum, a higher frequency wave has a smaller wavelength and vice versa. Table 1 shows the frequency distribution of the electromagnetic spectrum.

The relationship of the energy of a photon to the frequency (*f*) or wavelength (*λ*) of an electromagnetic wave is defined by:

$$E = hf = \frac{hc}{\lambda} \qquad (1.2)$$

where, h is the Plank's constant.

Light Comparison			
Name	**Wavelength**	**Frequency (Hz)**	**Photon Energy (eV)**
Gamma ray	less than 0.01 nm	more than 10 EHZ	100keV - 300GeV+
X-Ray	0.01 nm to 10 nm	30 EHz - 30 PHZ	120eV to 120keV
Ultraviolet	10 nm - 390 nm	30 PHZ - 790 THz	3eV to 124eV
Visible	390 nm - 750 nm	790 THz - 405 THz	1.7eV - 3.3eV
Infrared	**750 nm - 1 mm**	**405 THz - 300 GHz**	**1.24meV - 1.7eV**
Microwave	1 mm - 1 meter	300 GHz - 300 MHz	1.24μeV - 1.24meV
Radio	1 mm - 100,000 km	300 GHz - 3 Hz	12.4feV - 1.24meV

Table 1: Frequency and wavelength distribution of the electromagnetic spectrum

From Table 1 we see that infrared (or IR) radiation covers the wavelengths in the range from 750 nm to 1 mm. Objects generally emit infrared radiation across the spectrum of wavelengths, but usually only a limited region of the spectrum is of interest. Sensors usually collect radiation only within a specific bandwidth. Therefore IR spectrum is divided into three subdivisions:

    a.   Short wavelength IR (SWIR, 750nm-2μm)

    b.   Mid-wavelength IR (MWIR, 3-5μm)

    c.   Long wavelength IR (LWIR, 8-13μm) [3]

Human body and different types of warm objects radiate heat waves usually in the LWIR range which contains a low range of energy. So for detecting the radiation either an ultra-cool environment is required or the IR energy has to be directly converted into thermal energy [1].

This work focuses on the fabrication of thermoelectric poly-silicon nanowires which convert IR energy to thermal energy for IR radiation detection i.e. thermoelectric IR detectors in LWIR region. Chapter II contains the basics of IR detectors, thermoelectric IR detectors, thermoelectric materials, and the previous work. Chapter III focuses on the design and fabrication process flow of silicon nanowire devices. All the steps of the fabrication process are discussed in detail. The results and discussion are compiled in chapter IV. Chapter V summarizes the work.

CHAPTER II

TERMOELECTRIC INFRARED DETECTORS

2.1 IR detectors

An infrared detector is a system which absorbs the IR radiation radiated from an object and converts it into an electrical signal. IR systems can be divided into three generations. The first generation includes the IR scanning systems. The second generation incorporates the full framing systems i.e. the detector pixel configuration is a 2D array. The third generation is not specified clearly, yet. Usually third generation of IR systems refers to systems with higher number of pixels, better performance, and enhanced capability [4].

IR detectors can be categorized to two classes:

- Photonic IR detectors
- Thermal IR detectors

Photon detectors convert photons directly into free current carriers by photo exciting electrons across the energy bandgap of the semiconductor to the conduction band. The excited electrons produce a current, voltage or resistance change of the detectors. On the other hand, in thermal IR detectors some properties of the sensing material change due to the absorption of IR radiation [5].

2.1.1 Detector Figure of merit

Performance measurement of an IR detector has always been a challenge due to the involvement of a number of parameters. Performance measurement is more difficult for big 2D arrays instead of a single detector. The performance of an IR detector can be determined by measuring the following quantities: responsivity (R), noise equivalent power (NEP), and detectivity (D).

2.1.1.a. Responsivity (R)

The ratio of the root mean square value of the fundamental component of the electrical output signal of the detector to the root mean square (rms) value of the fundamental component of the input radiation power is defined as the responsivity of the detector. The units of responsivity are volts per watt (V/W) or amperes per watt (A/W).

The voltage responsivity of a detector can be expressed by the following equation:

$$R_v(\lambda, f) = \frac{V_s}{\Phi_e(\lambda)\Delta\lambda}$$
(2.1)

where, V_s is rms value of the signal voltage due to Φ_e, and $\Phi_e(\lambda)$ is the spectral radiant incident power in W/m at wavelength λ and $\Delta\lambda$ is the bandwidth of the detector.

2.1.1.b. Noise equivalent power (NEP)

Noise equivalent power is the incident power level that produces a signal to noise ratio (SNR) of 1 or that outputs a signal equivalent to the rms noise output. If the responsivity of the detector is R_v for voltage output and R_i for current output, NEP can be written as-

$$NEP = \frac{V_n}{R_v} \ or, NEP = \frac{I_n}{R_i} \qquad (2.2)$$

where, V_n and I_n are the rms noise voltage and current respectively at output. The unit of NEP is watt. Alternatively, the NEP can be used for a specific reference bandwidth, usually 1Hz. In that case the unit is $W/Hz^{1/2}$.

2.1.1.c. Detectivity (D)

If the noise equivalent of detector is NEP, the detectivity D can be written as:

$$D = \frac{1}{NEP} \qquad (2.3)$$

For many detectors, the NEP is proportional to the square root of the detector signal which is proportional to the detector area, A_d. This implies that both NEP and D are related to the bandwidth and the detector area. A normalized detectivity D* has been defined and can be expressed as-

$$D^* = D(A_d \Delta f)^{1/2} = \frac{(A_d \Delta f)^{1/2}}{V_n} R_v = \frac{(A_d \Delta f)^{1/2}}{I_n} R_i = \frac{(A_d \Delta f)^{\frac{1}{2}}}{\Phi_e}(SNR) \qquad (2.4)$$

where, the unit of D* is $cmHz^{1/2}W^{-1}$ [6,7].

2.2 Thermal detector:

Considering the requirement of large array integration, the three most convenient thermal detecting mechanisms are: resistive bolometers, pyroelectric detectors, and thermoelectric detectors.

In a resistive bolometer the resistivity of the material changes due to change in temperature due to IR radiation absorption. Usually, a material with a high temperature coefficient of resistance should be chosen as the sensing material so that the change in the resistance is high for a small temperature change.

A pyroelectric detector measures a voltage resultant from a spontaneous electric polarization in the sensing material of the detector for absorbing IR radiation. Unlike the resistive bolometers and thermoelectric detectors, pyroelectric detectors do not show any DC response [5]. In a thermoelectric detector, the temperature change is converted to an electrical voltage by using a thermopile [7].

Thermal detectors are not as efficient as photon detectors. Photon detectors show better detectivity and responsivity than thermal detectors. But, thermal detectors have some advantages over the photon ones, such as: they do not need cryogenic cooling system, they are cheap, and they have a longer life time. Another advantage of thermal detectors is that they can be operated over a wider range of bandwidth than the photon detectors. Therefore, thermal IR detectors operating at room temperature have been an attractive topic for the researchers.

2.2.1. Fundamental performance limits for thermal detectors

Temperature fluctuation noise fundamentally limits the performance of a thermal IR detector [ref 9]. The temperature fluctuation noise limited D* or D*$_{TF}$ is given by,

$$D^*{}_{TF} = (\frac{\eta^2 A_d}{4kT_d^2 G})^{1/2}$$ (2.5)

where η is the absorptance of the material, A_d is the detector area, k is the Boltzmann's constant, T_d is the detector temperature, and G is the thermal conductance between the sensitive element and its support structure. If the heat exchange occurs mainly through radiation, the temperature fluctuation noise limit turns into the background fluctuation noise limit. The temperature fluctuation noise limit is written as,

$$D^*{}_{TF} = [\frac{\eta}{8k\sigma(T_d^5+T_b^5)}]^{1/2}$$ (2.6)

where, σ is the Stefan-Boltzmann constant and T_b is the background temperature [5].

In an imaging array, the equation for the noise equivalent temperature difference or NETD is,

$$NETD = \frac{(4F^2+1)V_N}{A_d\tau_0 R(\Delta P/\Delta T_s)_{\lambda_1-\lambda_2}}$$ (2.7)

Where F is f/# of the optics, V_N is the bandwidth electrical noise, τ_0 is the transmittance of the optics. $(\Delta P/\Delta T_s)_{\lambda1-\lambda2}$ is the rate of change with temperature of the radiated power per unit area of a blackbody temperature T_s, measured within λ_1-λ_2. $(\Delta P/\Delta T_s)_{\lambda1-\lambda2}$ is equal to 2.62x10^{-4} Wcm^{-2}K for T_s of 300K and λ_1-λ_2 between 8μm and 14μm. [5].

2.3 Thermoelectric IR detectors

A thermoelectric (TE) detector uses two junctions between two different electrical conductors. One junction is exposed to the incident IR radiation and gets heated while the other junction remains cold. For the Seebeck effect the temperature difference induces a voltage which is measure as the output from the two ends of the cold junction [5]. Figure 1 shows the basic working principle of a thermoelectric IR detector. The junction of two TE materials is heated up by the IR absorption. The increase in temperature results in an electrical voltage for the seebeck effect. One can select a metal-semiconductor or a semiconductor-semiconductor TE junction for detection. TE materials with a high Seebeck coefficient should be selected for good performance.
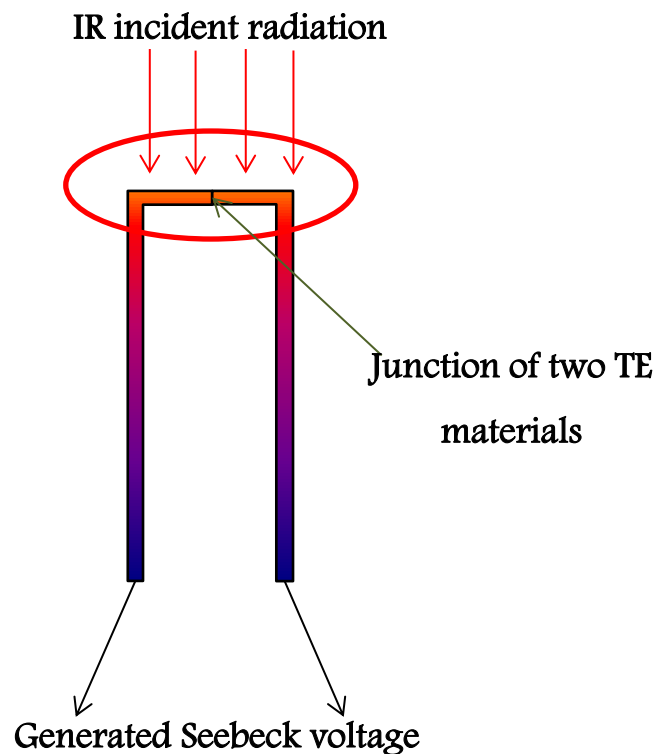
Figure 1: Basic work mechanism in a thermoelectric IR detector

The responsivity of a thermoelectric detector is,

$$R = \frac{NS\eta}{G(1+\omega^2\tau^2)^{1/2}}$$ (2.8)

Where, S is the Seebeck coefficient of the junction between the materials, N is the number of thermocouples in electrical series, G is the thermal conductance between the sensing element and its supportive structure, η is the absorptance of the material, ω is the angular modulation frequency of the IR radiation, and τ is the response time [5].

2.3.1   Previous work on thermoelectric IR detectors

As stated earlier, thermoelectric IR detector technology has grabbed attention as a potential substitute for photon and thermal detectors because of its much lower cost and reduced size. The performance of thermoelectric IR detectors is not as good as photon detectors, but efforts continue to improve the performance. Improvement of performance of a detector means increase in responsivity and detectivity. Size reduction is an important goal, also. Choi and Wise reported a responsivity of 12 V/W and a detectivity of 5×10^7 cmHz$^{1/2}$W^{-1} in 1986 with a detector area 400μm x 700μm [8]. A responsivity of 500 V/W was found for a single detector with thermocouples of BiSbTe and BiSb pairs in 1991[10]. Another report with a responsivity of 150 V/W was published by ETH for a detector with p and n type thermocouple pair which was fabricated on a chip with Op-Amps in 1992 [10]. In 1994, a responsivity of 1550 V/W was reported by Japan Defense Agency and NEC Corporation together for a 100μm x 100μm unit size array with p-n thermocouples [10]. In 1998, Foote, Jones, and Caillat got a responsivity of 1100V/W and a response time of 99ms for a 1500μm x 75μm linear array detector of BiTe and BiSbTe thermopiles [11]. Nissan Research Laboratory (NRL) reported a responsivity of 2100V/W for a 48 x 32 pixel array with a pixel size of 116 μm x 116 μm in the same year. Each pixel consisted of six pair of thermocouples. After three years NRL reported an improved responsivity of 2770 V/W in 2001 with a reduced pixel size of 100 μm x 100 μm. In 2005, NRL

achieved their highest responsivity and, so far, the best one of 4300 V/W for 48 μm x 48 μm pixels [11]. In 2009, David Kryskowski and Justin Renkenc reported 300V/W responsivity for a large array of 80μm x 60μm pixels [12]. In 2011, Mohammad J. Modarres-Zadeh reported a responsivity of 100 V/W and a response time of not greater than 26ms for an umbrella-like absorber detector with an area of 20μm x 20μm at room temperature. The value of D* was found to be 2.9 x 10^6 cmHz$^{1/2}$W^{-1} [13].

2.3.2   Why thermoelectric detectors?

The thermoelectric sensing method has some advantages, which make it a superior choice for IR imaging devices. Firstly, thermoelectric detectors do not need any temperature stabilization. Since the temperature coefficient of resistance of the material in a resistive device and the dielectric constant of the material in a pyroelectric device are strongly related to the absolute temperature, the temperature of the sensing array has to be properly controlled to operate in a wide range of temperature. Usually the material in use is set at transition temperature to increase responsivity [14]. In the case of thermoelectric detectors, the reference temperature is always fixed by the bulk substrate, which is acting as a heat sink, so there is no need to control it. Thermoelectric IR detectors don't need any bias signal, which is not the case of resistive and some pyroelectric detectors [14]. The lack of a bias signal offers a low noise operation for thermoelectric detectors. Also, thermoelectric detectors don't need any mechanical chopper as they are capable of measuring constant radiation.

2.3.3   Materials for efficient thermoelectric detectors

The performance of a thermoelectric detector can be improved by using more efficient thermoelectric materials. The efficiency of a thermoelectric material is defined by a dimensionless entity "Figure of merit" or ZT and defined by [15]-

$$ZT = \frac{S^2\sigma}{k}T \qquad\qquad (2.9)$$

Where S is the Seebeck coefficient, k is the thermal conductivity, σ is the electrical conductivity, and T is the absolute temperature in Kelvin. $S^2\sigma$ is defined as the power factor for the semiconductors.

BiTe compounds show high ZT and the detectivity of the detectors with BiTe compound material has been reported in the range of $10^9\,cmHz^{1/2}W^{-1}$. The value is comparable to the detectivity of pyroelectric and resistive devices [16]. Figure 2 shows a graphical representation of the progress in research to improve the ZT of thermoelectric materials over the past seven decades.
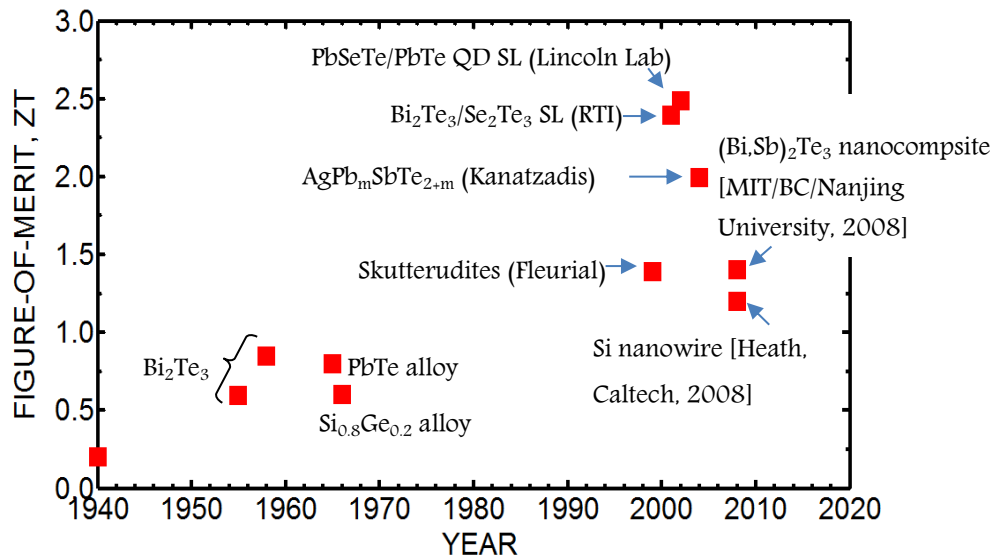
Figure 2: ZT enhancement over the last seven decades

From equation 2.9 it is clear that ZT is directly related to S, k and σ. So for a higher ZT, S and σ should be as large as possible and k should be as small as possible. At first people tried to increase σ by increasing the doping concentration of the semiconductors. But the problem is, it has a reverse effect on S. So there is a trade-off between the two parameters. Figure 3 shows the relationship among S, σ, and k [17].
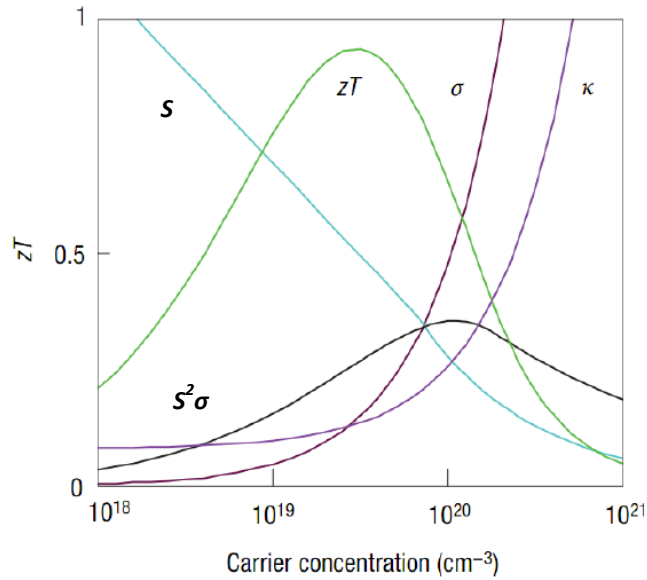
Figure 3: Change in ZT with the carrier concentration in Bi_2Te_3

Here we can see that excess carrier concentration exceeding certain concentrations has an adverse effect on $S^2\sigma$ as well as ZT. So increasing the carrier concentration beyond a limit didn't help at all and the ZT remained less than 1. In the 1990's some research was carried out on the lower dimension thermoelectric structures [18]. Especially the association of nanotechnology showed an improvement in the power factor and ZT and many groups reported higher ZT. Nanostructures usually improve ZT by maintaining the power factor by quantum size effect [18, 19, 20], or by reducing the thermal conductivity through phonon scattering at the lattice interfaces [19, 21], or by interface energy filtering [22, 23]. Figure 2 shows a ZT of 2.6 reported by Lincoln lab, which has been a motivation for further investigation in thermoelectric (TE) research area [24].

2.3.4 Silicon nanowire as a prospective TE material

In Figure 2, several TE materials have been shown as well as their corresponding ZT. A big problem with these materials is that their preparation process is not straightforward and the materials are rare. Also, the semiconductor alloys have compatibility difficulties for microelectronics fabrication. Doped silicon can be a strong candidate as the TE material for micro-machined thermoelectric IR detectors.

Bulk Si shows a very large thermal conductivity ($k>100Wm^{-1}K^{-1}$) which makes it a very poor TE material with a very low ZT (<0.01 at 300K) [37]. But for $Si_{0.8}Ge_{0.2}$ alloy the thermal conductivity reduces to a value of $5Wm^{-1}K^{-1}$ at high temperature which results a ZT of about 1 at 1300K. Still the TE alloy doesn't show a good ZT at room temperature (0.2 at 300K) [25].

On the other hand, nano scaled Si wires show a dramatically improved ZT. Various simulations and theoretical work indicate that there is a large reduction in thermal conductivity with the decrease of cross sections of nanowires [26-29]. Experimental work has been reported on the thermal conductivity measurement of silicon nanowires and the reported results indicate a consistent decrease in k with decrease in the cross section of nanowires [30-34]. From theoretical and experimental data, ZT values in the range of 0.11~1 have been reported for silicon nanowires [30, 31, 35, 36]. This range of ZT is considered promising for thermoelectric applications. The highest reported ZT for a 20nm wide silicon nanowire is about 1with a doping concentration of $7x10^{19}cm^{-3}$ and this value is 100 times larger than that of bulk silicon [30]. This is due to the decrease in k value drastically for the increase of phonon scattering at the nanowire surface with a diameter less than the phonon mean free path yet higher than that of electrons and holes [30], while the other two parameters S and σ remain the same as bulk Si. The principle motivation for selecting Si nanowire as the sensing TE material for our IR detectors was its high ZT as well as the compatibility of Si for microelectronic fabrication.

CHAPTER III

FABRICATION OF POLY-SILICON NANOWIRE DEVICES

Silicon nanowire fabrication always has been a complicated job. In addition to fabrication, characterization is also important. There are numbers of methods for silicon nanowire fabrication [38, 39, 40, 41, 42, 43, 44, 45], for example:

- Vapor liquid solid (VLS) method

- Metal assisted etching (MAE) method

- Superlattice nanowire pattern transfer (SNAP) method

- Oxidation

- Electron beam lithography (EBL)

VLS is the most popular way to fabricate single crystalline silicon nanowire. The VLS mechanism is associated with the adsorption of a vapor by introducing a catalytic liquid metal. A liquid droplet of usually gold is prepared on the substrate. Then the material to be grown (Si for silicon nanowire) is introduced as vapor. The desired material atoms are adsorbed by the liquid surface of the droplet and get diffused to it. Supersaturation and nucleation at liquid/solid interface cause a vertical growth of the nanostructure. In this method the dimension of the nanowires can be directly controlled by the size of the metal droplet. A dimension of some tens of nm is possible by this method and VLS is good for a mass production [38, 39].

Metal Assisted Chemical Etching (MAE) is a wet-etching technique used to prepare crystalline micro or nanostructures, such as: nanowires, micro/nano channels, in bulk semiconductors. The method is based on an electrochemical reaction between a semiconductor surface and a solution of hydrofluoric acid and hydrogen peroxide, where a metal, usually Au or Ag, is used as a catalyst. Nanowire prepared by MAE is vertical like VLS. MAE has its applications in electronics, optics, plasmonics, energy storage, and energy conversion. It is an economical, scalable and self-assembled alternative fabrication process for the semiconductor industry. Nanowires with a diameter of less than 10nm are possible by this method [41, 46].

Superlattice nanowire pattern transfer or SNAP is a method to fabricate planer nanowires. This method has some distinctive advantages. A large nanowire array including metals, insulators, and semiconductors, with a dimension range from sub 20nm to few nanometers can be produced by this method. The process is fully compatible to the traditional electronics manufacturing procedure. Another big advantage is fabrication of a millimeter long or longer nanowire is possible by this method [43]. This method is also good for bulk production of nanowire like VLS.

Another method for preparation of silicon nanowires is oxidation method. In this method at first single crystalline silicon nanowire is produced by any conventional method, like VLS, and then the nanowire is oxidized at high temperature. A successive HF etching is carried out to remove the surface oxide to obtain the core nanostructure with a smaller diameter [44]. In this way one can control the diameter of the nanowire by controlling the oxidation time.

Electron beam lithography or EBL is another popular method to fabricate silicon nanowire. For our device we selected EBL to fabricate silicon nanowire for its some inherent advantages. In next section this will be discussed in details.

3.1 Electron Beam Lithography (EBL)

EBL consists of shooting a narrow, concentrated beam of electrons onto a resist coated substrate. The concept is similar to the conventional photolithography method, but EBL is used to obtain nanoscale features which are not possible by normal light wave based tools. Though the process of E-beam lithography is simple, the schematics and the parts required are quite complex. Two main components required for E-beam lithography are described below:

Electron Gun: The main component of an EBL system is an electron gun. The electron gun is an apparatus that is able to produce a beam of electrons in a specific direction. Two common E-beam emitters are lanthanum hexa-boride crystal and a zirconium oxide coated tungsten needle. At first the emitter is heated up to initiate and excite electrons. Then a high voltage is applied to accelerate the excited electrons towards a structure called the anode. By changing this voltage, the trajectory and the focus of the beam can be controlled.

Electron Optical Column: The electron optical column is a system of lenses. The system is a combination of electromagnetism and optics, and has the ability to focus the electrons into a concentrated beam in a desired direction. Parallel plates placed inside the column can be electrostatically charged to a precise degree. The resulting electric field is able to bend the beam to a desired direction.

After the beam is directed and concentrated by the optical column, it is ready to be focused on the surface. The surface is coated with an electron beam photoresist. PMMA is most commonly used photoresist for EBL method. The pattern is written as a series of interconnected dots with user adjustable spacing. The electron beam movements are controlled by computer software where the pattern is already loaded in the specific format. The system uses either raster method or vector method for scanning. A normal SEM tool can be converted to an electron beam lithography machine with an appropriate modification.

Using EBL to pattern silicon nanowires provides two genuine advantages. Firstly, the main advantage of EBL is its independence from the diffraction limit, which the normal light severely suffers from. The ability of beating the diffraction limit makes EBL have a resolution of almost 20nm. In our device we have 25 nm minimum features and hence EBL was an appropriate option. Secondly, EBL is very similar to the conventional photolithography process. Therefore it was the most compatible method available to our device process flow to produce planer silicon nanowires.

3.2 The device structure

As stated in chapter II, our purpose of silicon nanowire fabrication is to measure its Figure of merit or ZT. Figure 4a shows the basic structure for ZT measurement of silicon nanowire.
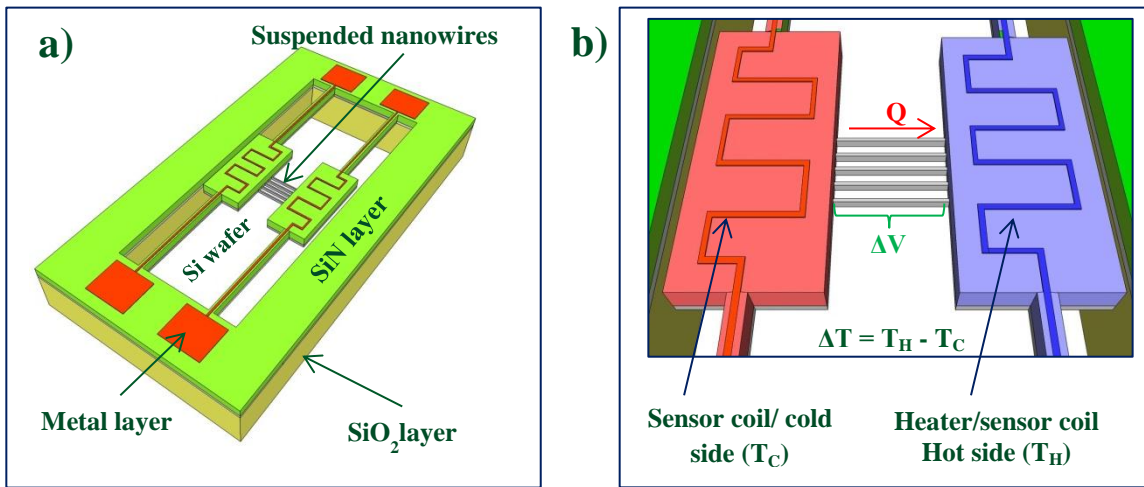
Figure 4: a) 3D schematic of Si nanowire device; b) A schematic of the experiment

The device contains two metal coils, which can be used as both heater and temperature sensor. One coil is heated up by a DC current flow through it and temperatures at both sides of the nanowire are measured by the coils. The induced voltage for Seebeck effect as well as the voltage for σ calculation is measured by the electrodes fabricated on both sides. The whole structure including nanowires is suspended to avoid any unwanted heat losses. We used a silicon nitride

layer between the doped poly-silicon and metal thin films as an insulator. This will be discussed in details in the process flow section. Heat flow measurement is the most cumbersome and complex among all the parameters. Since the whole structure is suspended, it can be assumed that the heat loss trough conduction is negligible if we take into account the heat losses through the holding arms. Also, convection and radiation losses can be made negligible by conducting the experiment under vacuum and at room temperature respectively. A number of reports have been published based on this structure [30, 32, 33, 34, 47-50].

Equation 2.9 shows the need to measure Seebeck coefficient S, electrical conductivity σ, and thermal conductivity k. The expressions for S, σ, and k are:

$$S = \frac{\Delta V}{\Delta T} \tag{3.1}$$

$$\sigma = \frac{l}{RA} \tag{3.2}$$

$$k = \frac{Ql}{\Delta TA} \tag{3.3} [37]$$

Where, A is the cross section and l is the length, R is the electrical resistance, and Q is the heat flow from hot to cold side through each nanowire (Figure 4b).

3.3   Process flow

For our silicon nanowire device fabrication we followed a six step process flow. Figure 5 and 6 show the steps and schematics of the cross sections of the device after different steps respectively of the process. The poly-Si layer deposition and the successive EBL for nanowire patterning were done outside of our laboratory. Hence our process starts from an inductively coupled plasma (ICP) etching of silicon nanowire.

Figure 5 shows the main steps as well as the mask used at the corresponding steps.

Step 01

> **Poly-Si NW etching (EBL)**

Step 02

> **Poly-Si rest etching (mask 1)**

Step 03

> **Nanowire protector deposition and patterning (mask 2)**

Step 04

> **SiN deposition and patterning (mask 3)**

Step 05

> **Metal deposition and patterning (mask 4)**

Step 06

> **Releasing of the device (mask 5)**
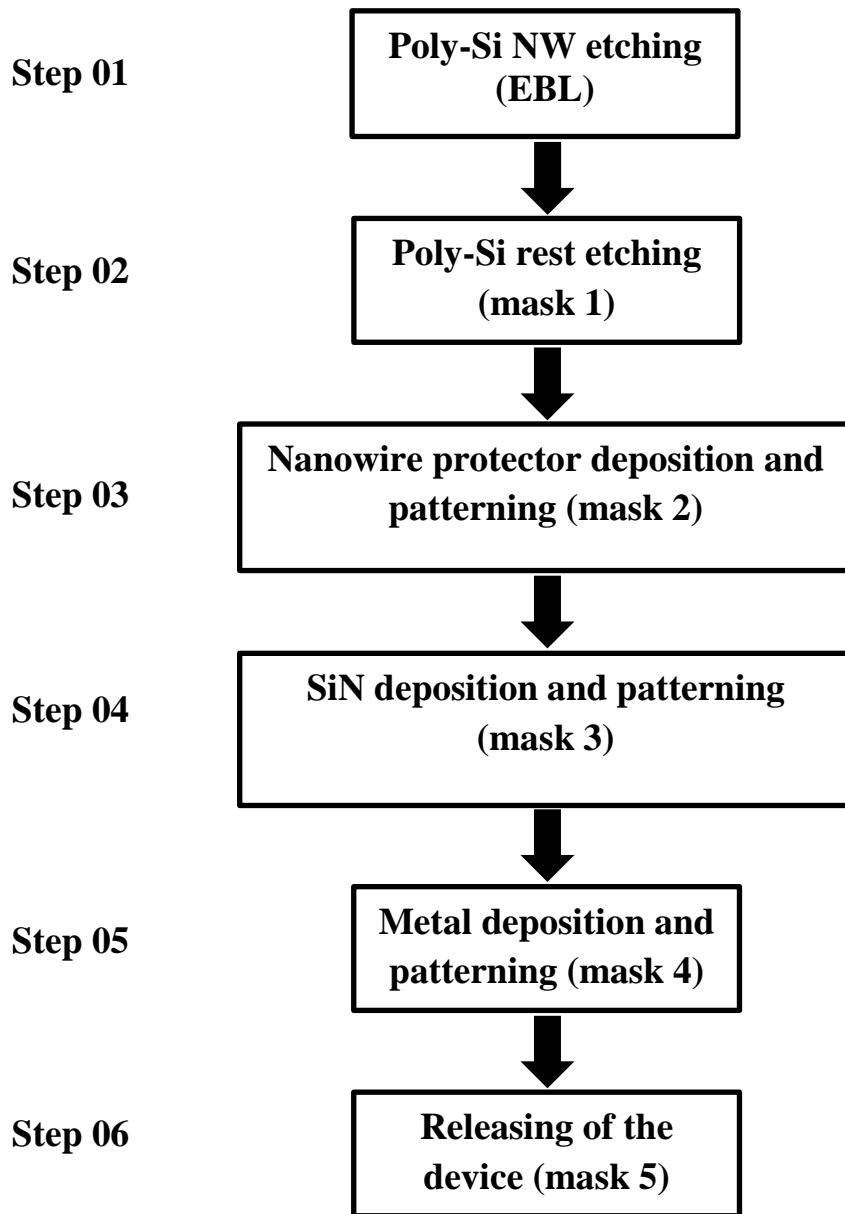
Figure 5: Steps of the silicon nanowire device process flow

Suspended Poly-Si nanowire

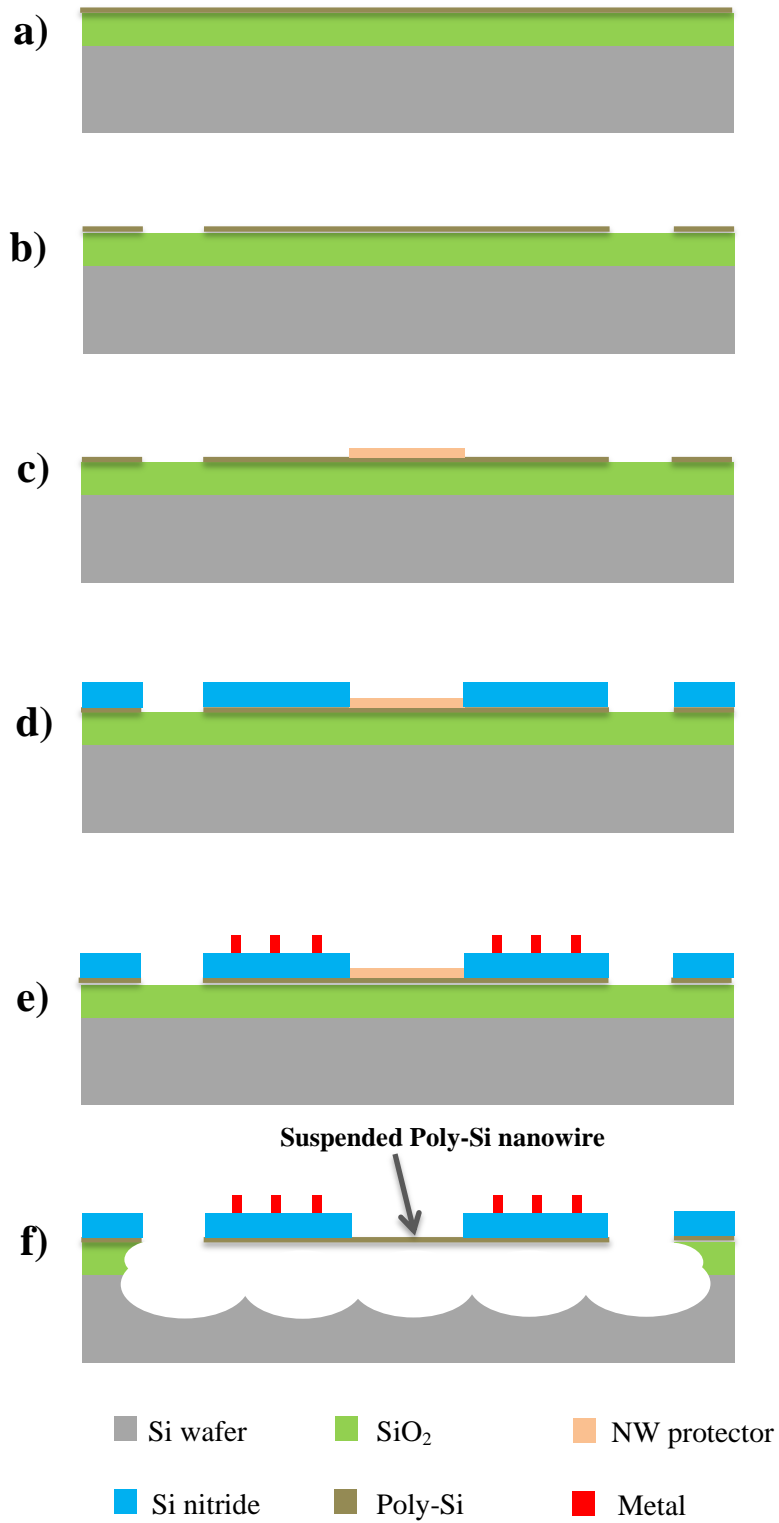|	Si wafer		SiO₂		NW protector
	Si nitride		Poly-Si		Metal

Figure 6: The fabrication process flow

As shown in Figure 6, the process starts with a sacrificial oxide layer deposition on a one side polished silicon wafer and a successive poly-Si thin film deposition by LPCVD. After poly-Si deposition, the nanowire patterning was carried out by EBL and ICP etching, which was done in our cleanroom. The rest of the poly-Si thin film was patterned by using the first mask (Figure 6b). An electrical insulator layer is supposed to be deposited (Si nitride) between the doped poly-Si and metal layer after poly-Si rest patterning. But since there are some very small nanowire features a protector layer is decided to be used to cover the nanowire portions of the wafer, so that the next steps don't destroy the features of tens of nanometer range (Figure 6c). Then the nitride layer was deposited and patterned (Figure 6d). In the next step, the metal layer was deposited and patterned by lift off process (Figure 6e). In the final step the whole device was released by a unique recipe combined both wet and dry etching (Figure 6f). The nanowire protector was etched away during the releasing process. In the next section each step has been discussed in details with scanning electron micrographs. Also problems faced in each step and the solutions have been included.

3.4 Fabrication Steps

As stated earlier, the poly-Si deposition and the EBL patterning of the nanowires were done outside of our cleanroom. Therefore the fabrication starts with the ICP etching of Si nanowire shown in Figure 5 (step 01). The process started with a one side polished silicon wafer with a 2μm SiO_2 and about 120-150nm thick poly-Si layers deposited on it. The poly-Si layer was patterned by EBL.

3.4.1 ICP etching of poly-silicon nanowire

An anisotropic etching process was needed for this step for the survival of nanowires. Otherwise any sort of undercut could destroy the nanometer range features. A gas mixture ($O_2 = 10$ sccm; $CHF_3 = 12$ sccm; and $SF_6 = 30$ sccm) was used in ICP to etch the poly-Si nanowire patterns. The

process was carried out for 10s and the nanowires were found nicely etched away. Figure 7 shows some SEM images after this step:
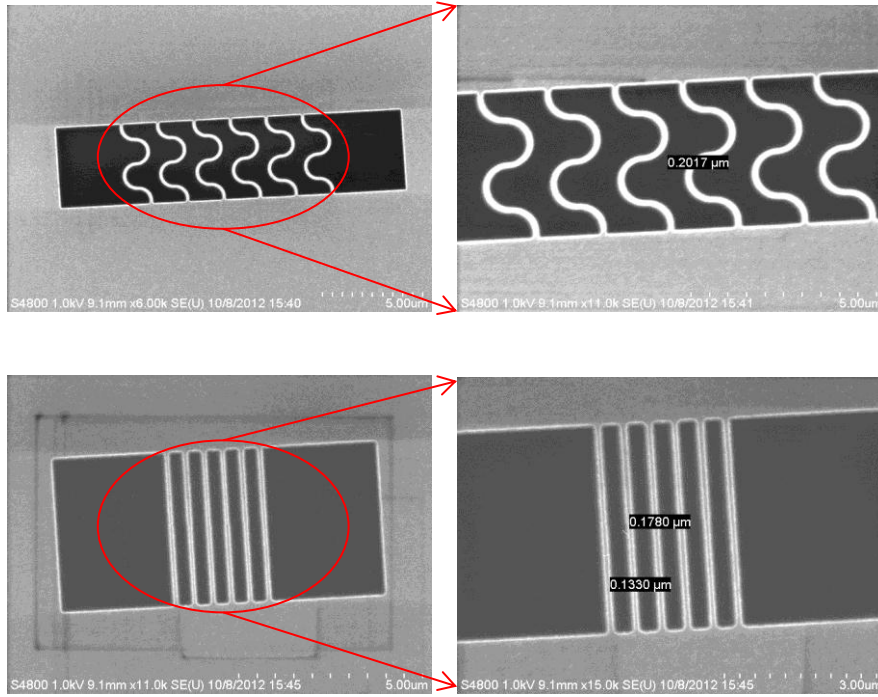

Figure 7: After 10s anisotropic ICP etching of EBL patterned silicon nanowires

There are both curved and straight nanowire patterns and the numbers in the pictures indicate the approximate widths of the nanowires (~200 nm for the first picture and 130-170 nm for second picture).

3.4.2 Poly-silicon patterning

In this step (Step 02 in Figure 5 and Figure 6b) the rest of poly silicon area rather than the nanowire portions, is patterned by the same ICP etching process as in the previous step run for 10s. The first mask of the process was used in this step. Figure 8 shows the patterns after this step.
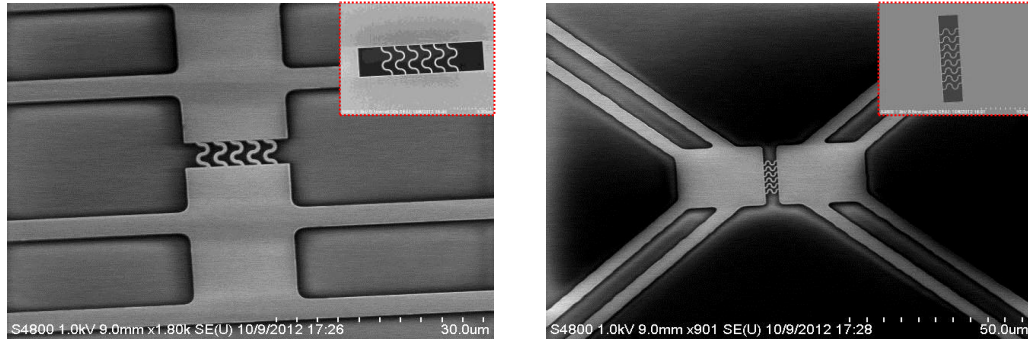
Figure 8: After 10s ICP etching of the rest of the poly-Si;
Inset shows the nanowire patterns only for comparison

There are two types of devices with vertical and horizontal nanowires (Figure 8). The purpose
was to have variations in the structure so that the possibility of survival of the nanowire devices
after the final releasing increases.

3.4.3 Nanowire protector layer deposition and patterning

Since the nanowire patterns are very sensitive and there is a large possibility that the patterns
might get harmed during the complex fabrication steps, a thin silicon dioxide layer was used as
the nanowire protector. Since the layer will be removed later, a low quality oxide layer was
adequate, which can be etched away easily. The oxide layer was deposited by PECVD and the
thickness was about 260nm measured by a nanospec (NA109) tool. Then the layer was patterned
by using the second mask (Step 03 in Figure 5 and Figure 6c) followed by a combined (dry +
wet) etching process. Since our requirement was a stiff etching profile of silicon dioxide, at first
an ICP dry etching process was run for 90s. As ICP etching doesn't have good selectivity to the
other materials (photoresist or poly-Si), the rest of the oxide thickness was etched by a 5:1
buffered oxide etch (BOE) solution. The thickness was continuously checked and the etching was
carried out until it was found 2μm which is the thickness of the lower oxide layer. To avoid
undercut during wet etching, the photoresist layer was hard baked at 150°C for 10min after
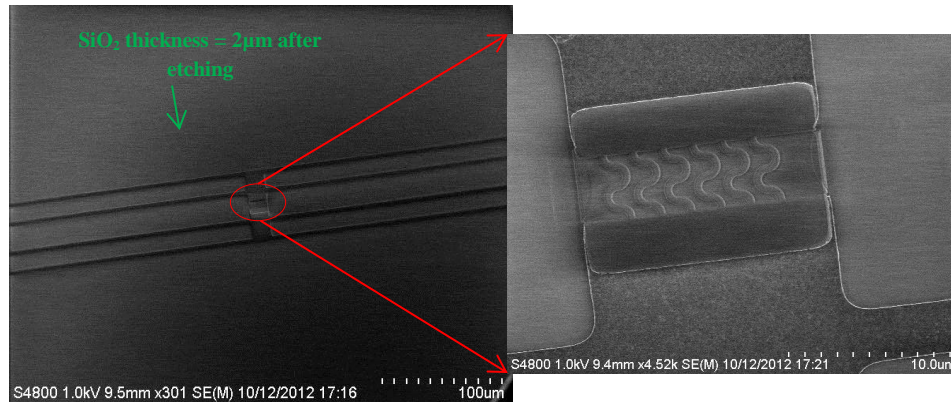photolithography.

Figure 9: nanowire protector after etching process

Figure 9 shows the SEM picture of the pattern after nanowire.

3.4.4 Electrical insulator layer deposition and patterning

For the characterization of nanowire, two metal coils are needed to be placed on the both sides of
the nanowire array. But the problem is that the poly-Si layer is doped and hence conductive.
Therefore electrical insulation is required between poly-Si and metal layers. This insulator layer
has to have:

- A very high selectivity to the oxide etchant solutions (BOE or HF).
- A high thermal conductivity so that it can transfer heat quickly to the poly-Si layer
  underneath while characterization as well as can conduct the local heat to the cold
  places.

Taking the above two points into account, silicon nitride was selected as the insulator layer. It
shows high thermal conductivity [51] and can easily be deposited by PECVD. The etch rate of
silicon nitride layer can be precisely controlled by selecting an appropriate deposition recipe [52].
For our process, the following recipe was tried at first.

Temperature (^{0}C)	SiH$_4$ + He (sccm)	He (sccm)	N$_2$ (sccm)	RF power (W)	Pressure (mTorr)
300	**1600**	**1200**	**450**	**80**	**750**

Table 2: Nitride deposition recipe

This recipe produces a low stress nitride layer which has a low etch rate in BOE or HF solutions. For patterning the layer (Step 04 in Figure 5 and Figure 6d), an ICP etching process was run with CHF$_3$ gas for 4min15s. The thickness of the nitride layer measured by nanospec was around 400nm. Figure 10 shows the SEM pictures after silicon nitride patterning.
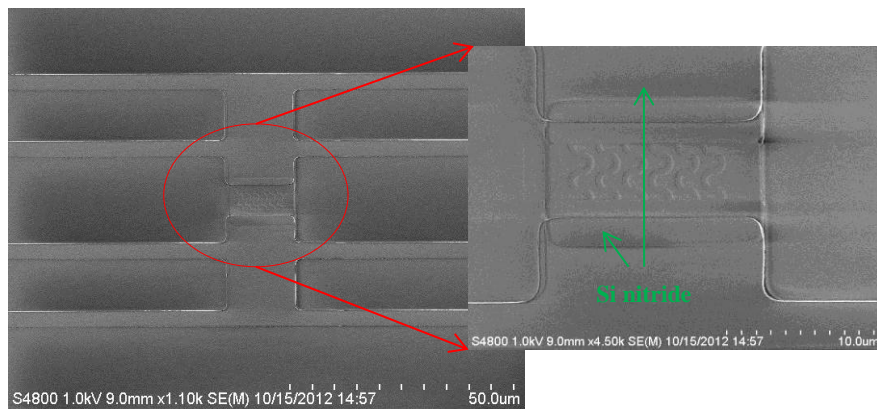

Figure 10: Si nitride layer after patterning

The nitride layer deposited by the mentioned recipe caused a big problem after releasing the device. The structure was getting distorted due to the large compressive stress of the nitride layer. Therefore a detailed characterization of PECVD silicon nitride layers was conducted. This will be discussed in section 3.5.

3.4.5 Metal deposition and patterning

As shown in Figure 4b, metal coils act as heater as well as temperature sensor during the thermoelectric characterization of silicon nanowire. It is done by using the temperature dependent resistance property of the metals. We know that the resistance of metals increases with the increase of temperature. Usually the relationship follows the following equation:

$$R = R_o(1 + \alpha \Delta T) \qquad\qquad (3.4)$$

where, α is the temperature coefficient of resistance (TCR) of the metal, R_o is the resistance of metal at temperature T_o, R is the resistance of metal at temperature T, and $\Delta T = T\text{-}T_o$. For selecting an appropriate metal one should consider the following issues:

- The metal should have a linear and repeatable resistance vs. temperature (R vs. T) curve over a wide range of temperature.
- The metal should have a high α for a high detection.
- The metal should be inert and immune to chemical reaction over time to avoid inaccuracy in data.

Platinum is a noble metal and shows the most stable R vs. T relationship over a wide range of temperature (-272.5^0C to 961.78^0C). Though the TCR of Platinum is not the best one ($0.003729/^0$C, which is enough for our use) among some other metals, considering the other criterion it is the best option as a temperature sensing material. Therefore Pt has been selected for the nanowire devices.

Metal liftoff process was applied to pattern the Pt thin film (Step 05 in Figure 5 and Figure 6e). At first about a micron thick positive photoresist layer was patterned by conventional lithography process. Then a thin Pt film was deposited.

For Pt deposition, sputtering deposition process was chosen. Table 3 shows the recipe for Pt deposition.

Temperature (^{0}C)	Power (W)	Pressure (mTorr)	Work distance (cm)	Time (min)	Thickness (nm)
Room	150	3	15	10	~ 62

Table 3: Sputtering deposition recipe for Pt deposition

After Pt deposition the wafer was sonicated in acetone for 4min to get rid of the unwanted portions of the metal layer. Figure 11 shows the Pt coils after liftoff process.
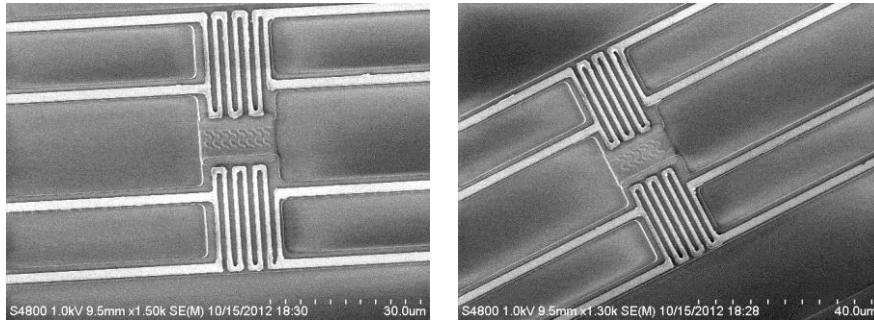

Figure 11: Platinum coils on the both sides of nanowire
after liftoff process

In the coil, the platinum bars were of 1μm width and the spacing was also 1μm.

3.4.6 Releasing of the device

Releasing of the whole device has been the most complicated and tricky steps of the fabrication process flow (Step 06 in Figure 5 and Figure 6f). Suspension became more challenging as the nanowire structures are very sophisticated and fragile. Figure 12 shows the schematics of the cross sections of the releasing process.
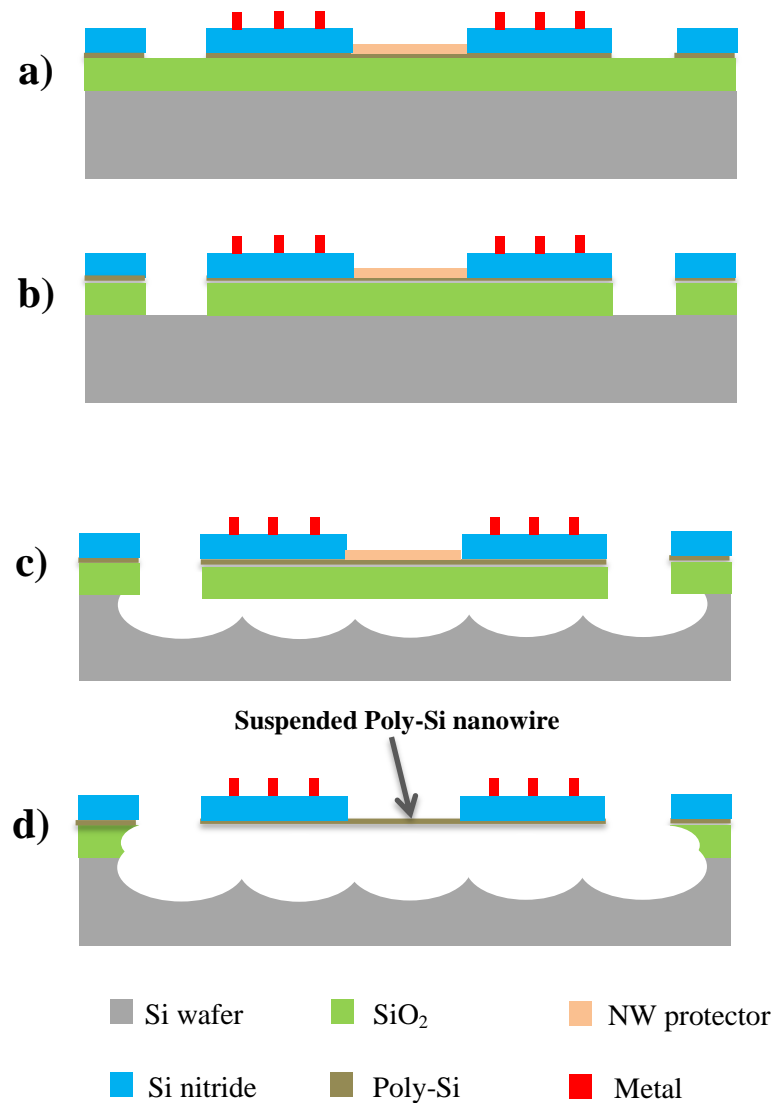

Figure 12: Process flow of the releasing step

For releasing the devices it takes a long time to etch silicon dioxide and silicon substrate by ICP. ICP etching has a disadvantage of poor selectivity to the other materials including photoresist. Therefore for this step a thicker photoresist layer than the previous steps was needed. SE^{TM}1827 was coated at a speed of 2000rpm for 30s, which gave a thickness of about 4.2μm. The layer was patterned by using the last mask. Figure 13 shows the photoresist pattern after photolithography.
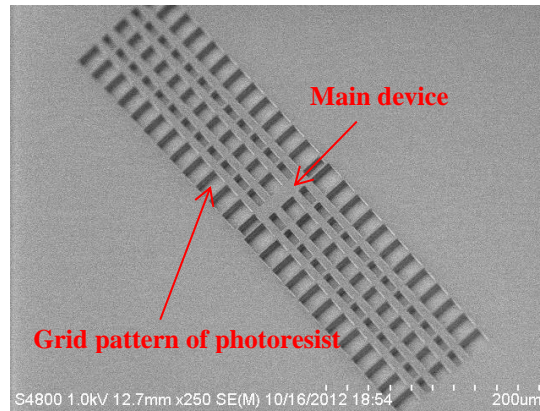

Figure 13: Photoresist layer after patterning
for final release of the device (Figure 12a)

A grid pattern was used to make holes to have a balanced etching of silicon/SiO$_2$. The 2μm thick silicon dioxide layer had to be etched away to reach to the silicon substrate for etching. For that an anisotropic etching by ICP was chosen so that the oxide layer still remained underneath the device structure to hold it during long time silicon etching (Figure 12c). Figure 14 shows the devices after directional etching of 2μm SiO$_2$ by ICP.
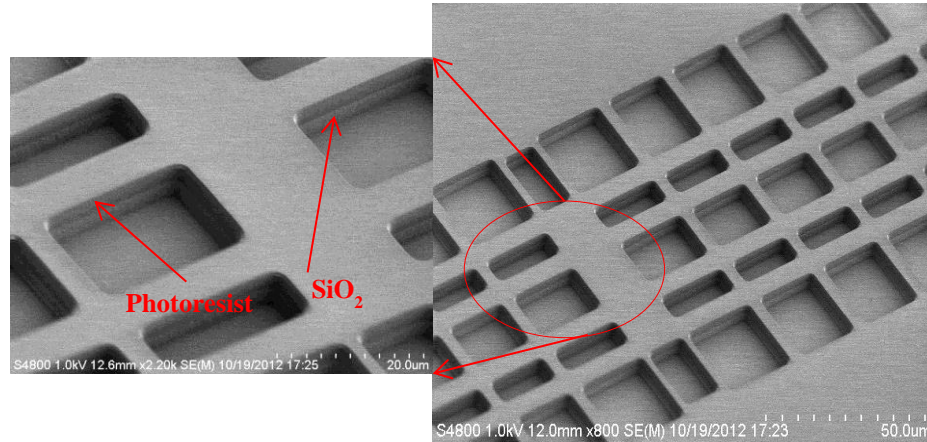
Figure 14: After anisotropic etching of 2µm SiO_2 layer (Figure 12b)

After oxide etching, the next step was to etch silicon substrate to release the device from it. At first it was tried to accomplish by an anisotropic etching. The same gas mixture used for nanowire and poly-Si rest etching was tried for silicon etching. But the problem was that there was a very small undercut. The etching was too directional for the etchant that it was not able to reach to the portions covered by photoresist. As a result it was taking long time for releasing, which introduced a new problem. As mentioned earlier, for the poor selectivity of dry etching process the photoresist layer got affected by the etchant. Before the full releasing of the device, the photoresist layer was etched away while the SiO_2 removal was yet to be done. Figure 15 shows the results after 5min and 25min of silicon etching.
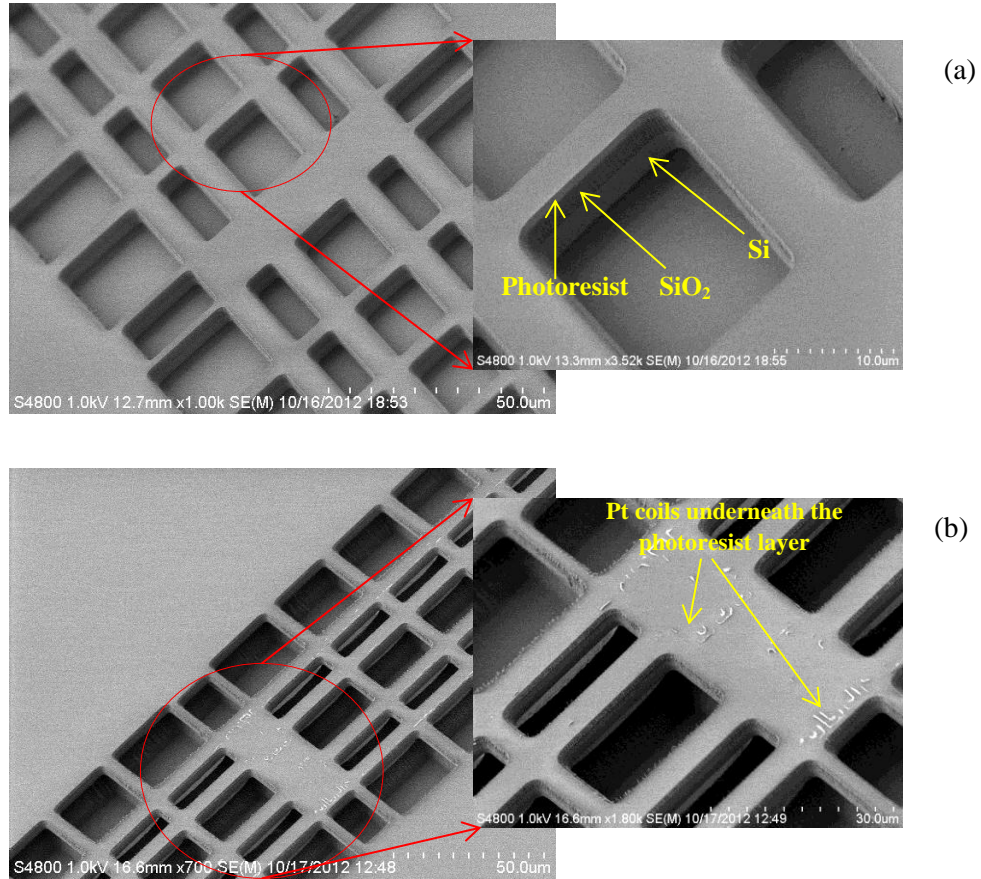
Figure 15: Directional etching of silicon; (a) after 5min & (b) after 25min

As anisotropic etching didn't work, a very aggressive etching process of SF_6 gas was tried. SF_6 etching is a highly isotropic silicon etching process. By varying the amount of SF_6, the undercut can be controlled. For releasing of the device, a large undercut was needed within a comparatively short time so the main device (red circled in Figure 15b) got released before attacking the photoresist severely. A combination of the directional and isotropic etching process was tried. But then the main device was not released completely while the other part of the device was released and the photoresist was affected. Figure 16 shows the SEM pictures of the device after running the combined etching process. The photoresist layer was cleaned up for better visualization.
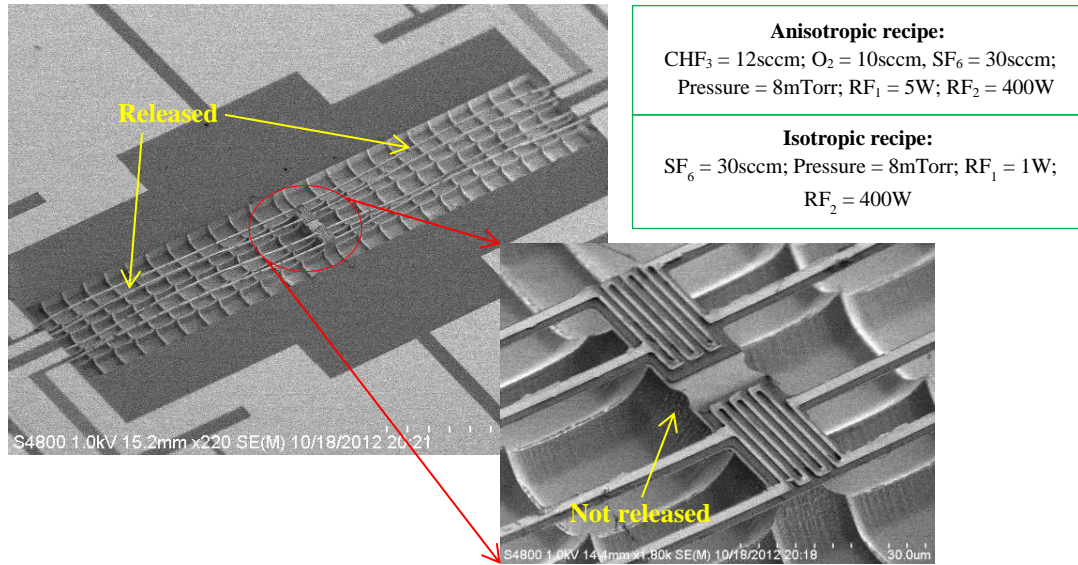
Figure 16: Device after 20min of anisotropic and 5min of isotropic etching

Finally an etching process of SF_6 only was tried and it achieved the desired result. After several

trials, 30min of SF_6 etching was found enough for a complete release of the structure. Figure 17

and 18 show the devices after 20min and 30min SF_6 etching of silicon.

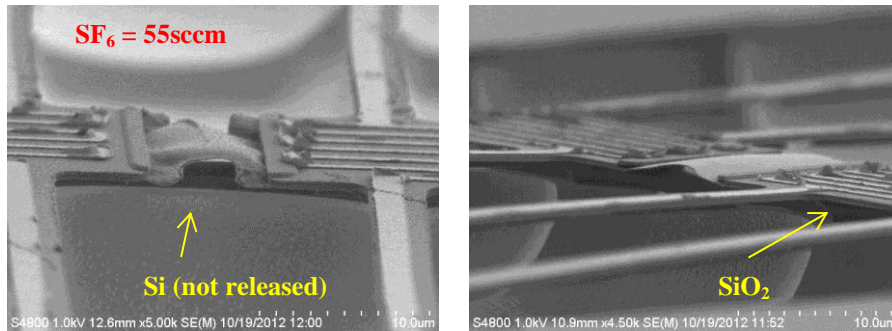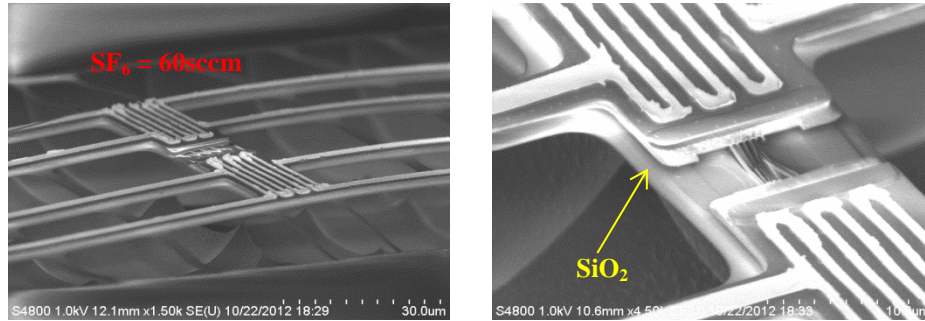Figure 17: After 20min of SF_6 etching

Figure 18: Completely released device after 30min SF$_6$ etching (Figure 12c)

After releasing the device completely from the substrate, the next step was to remove the oxide layer underneath the device as well as the nanowire protector beyond the nanowire area. Since the process needed an etchant which should not attack the poly-Si, nitride layer, and the photoresist layer at all, wet etching was the appropriate option. There were two options for this:

1. 49% HF solution
2. 5:1 buffered oxides etch (BOE) solution

The etch rate of oxide is slow in BOE solution. For the 2μm oxide layer etching it takes about 15-18min. This long time wet etching is not good for other materials as well as for the suspended structure. Therefore the HF solution was selected for oxide removal. Several trials were performed to optimize the etching time and 55s-1min was found enough for 2μm oxide removal. During this time the nanowire protector layer was etched away (Figure 12d). After oxide removal the photoresist residual was removed by successive oxygen plasma etching by ICP for 15min. Figure 19, 20, and 21 show the suspended nanowire devices after 30s, 45s and 1min HF (49%) etching respectively.
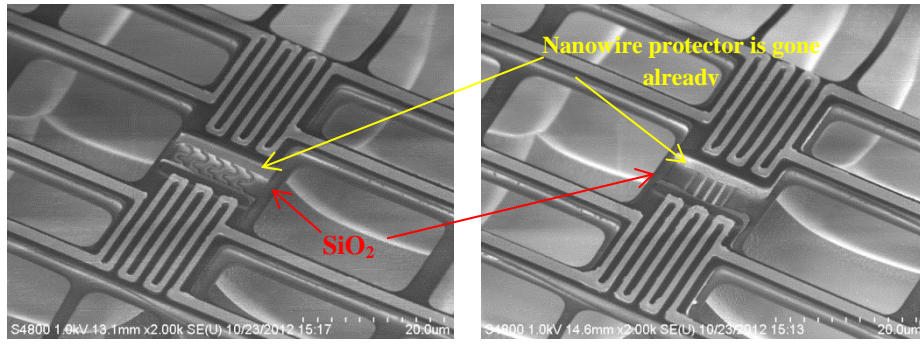
Figure 19: Oxide layer was not removed after 30s HF etching
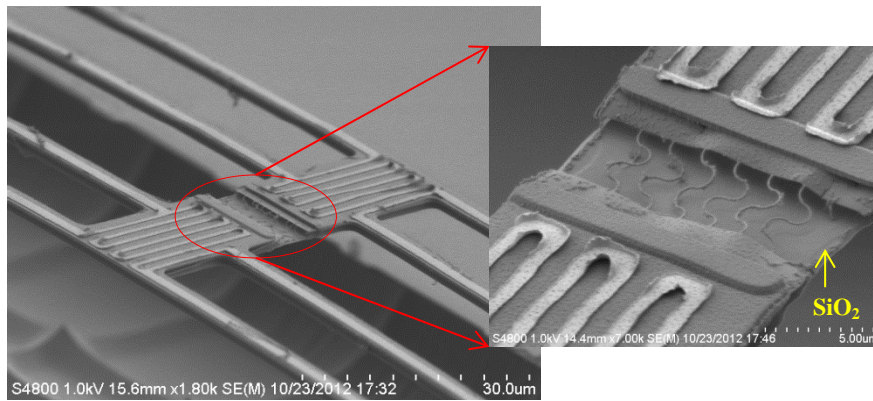
Figure 20: Nanowire devices after 45s of HF etching for oxide removal
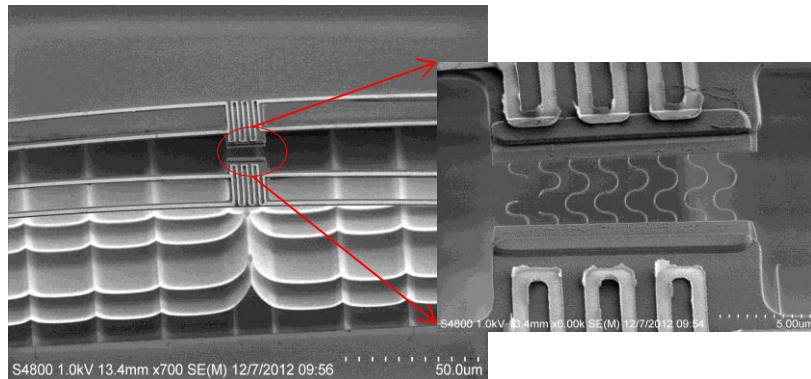
Figure 21: A completely suspended nanowire device after 1min of HF etching

Curved silicon nanowire structures showed better sustention than the straight ones. The curved structure showed less stiffness for spring effect, which is not the case for the straight nanowire. Figure 22 shows the SEM picture of two devices after the same fabrication process, where the curved one survived and the curved one broke.
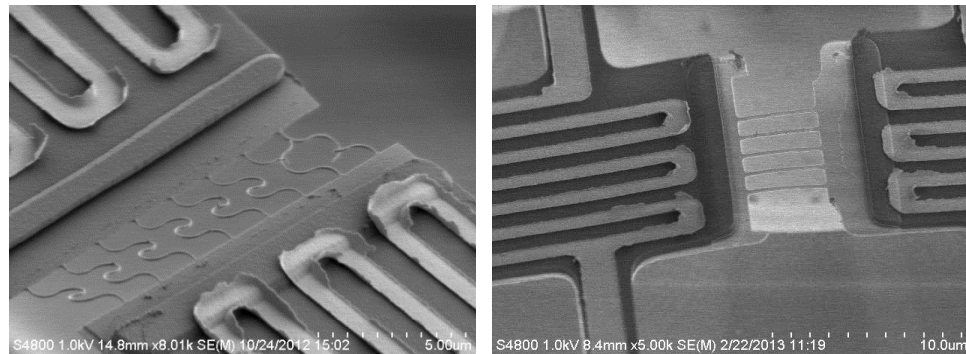
Figure 22: Curved and straight nanowires after same fabrication process

3.5 Characterization of silicon nitride thin film deposited by PECVD

In the silicon nanowire devices, the main problem was the distorted shape of silicon nitride layer due to its low or compressive stress. This was causing breaking of the devices. Figure 23 shows the wavy shape of the device structure and the broken devices.
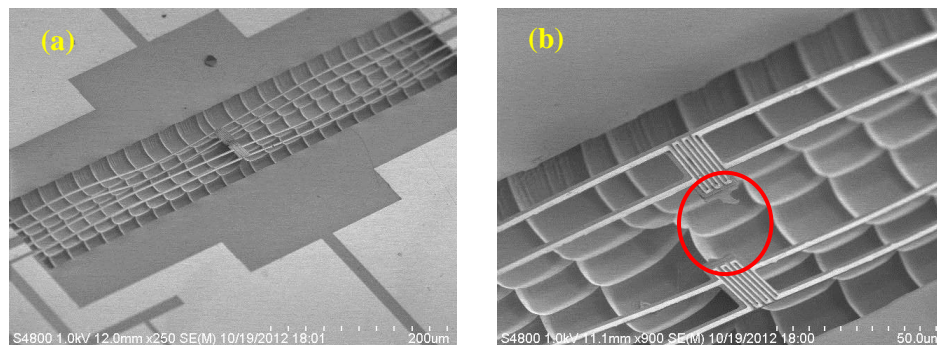
Figure 23: a) Distorted wavy shape of the device structure and b) the broken device due to this reason

To overcome this problem, the characterization of the silicon nitride layer was necessary. Since the low or compressive stress was responsible for this, nitride films with higher stress were deposited. The stress of silicon nitride films deposited by PECVD can be increased by increasing the amount of N_2 in the deposition recipe as well as adding some NH_3 to it [52]. Therefore the recipe mentioned in Table 2 has been changed. Table 4 shows the amount of gases used for the depositions. Also the etch rates in HF and BOE solutions have been recorded.

| Sample	N2 (sccm)	NH3 (sccm)	Deposition rate (nm/min)	ICP etch rate (nm/min)	49% HF etch rate (nm/min)	5:1 BOE etch rate (nm/min)
1	1000	5	13.67	≈126	≈75	≈8
2	1000	7.5	13.33	≈127	≈100	≈16
3	1000	10	13.5	≈137	≈200	≈18

Table 4: Data for Silicon nitride deposition with NH_3

For the deposition no extra He was used to increase the percentage of N_2 in the gas mixture and the amount of (SiH_4 + He) was same as in Table 2.

Addition of NH_3 helped to obtain a nice and flat suspended nitride structure. Figure 24, 25, and 26 show the suspended structures of nitride with different amount of NH_3.
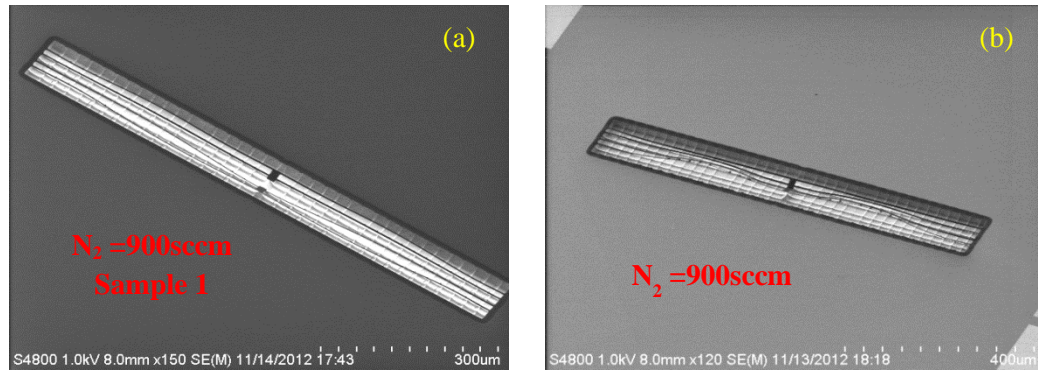
Figure 24: a) Improved shape of the device structure with no He and 5sccm NH_3 and b) wavy structure with no He and no NH_3
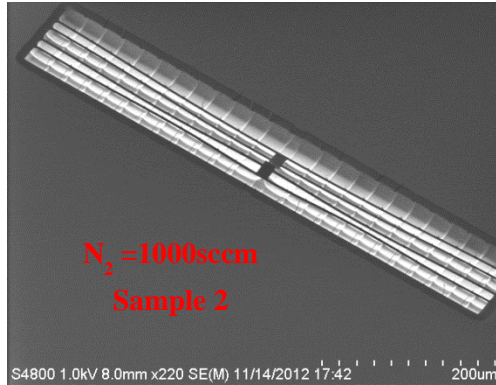
Figure 25: Almost straight shape with 7.5sccm NH$_3$
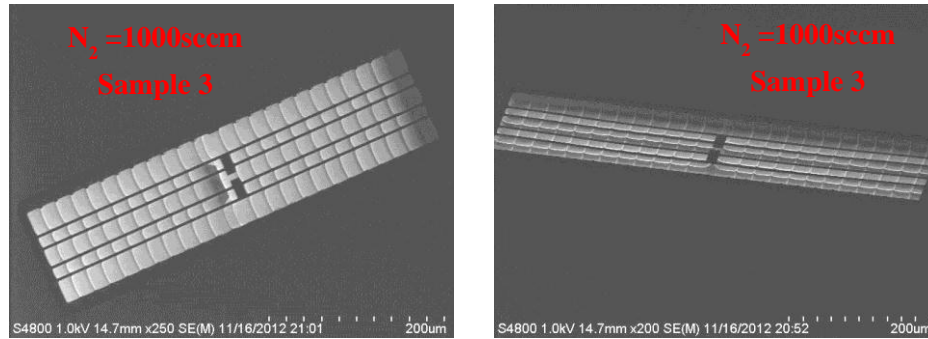
Figure 26: Perfect straight shape with 10sccm NH$_3$

For all the samples, the thickness of the nitride layers was about 400nm. Sample 3 (Table 4) was found perfect for the device, but the problem was its high etch rates in BOE or HF solution. This lowered the selectivity severely for oxide etching which was not desirable for the main device. To solve this problem a three layer nitride film was used for the device. Figure 27 shows the schematic of the layer. The two outer layers have low stress and low etch rate in the solutions, and hence protect the core high stress nitride layer during oxide wet etching. The middle layer keeps the structure straight.

Nitride with recipe in Table 2	50nm
Nitride with recipe in Table 4 (sample 3)	300nm
Nitride with recipe in Table 2	50nm
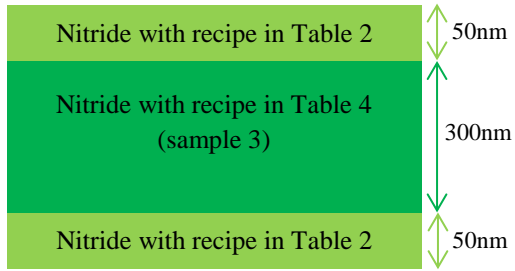
Figure 27: Three layered silicon nitride used
for the device

Figure 28 shows the SEM pictures of a nanowire device by using the three layered nitride film.

The improvement is clearly visible compared to Figure 23.
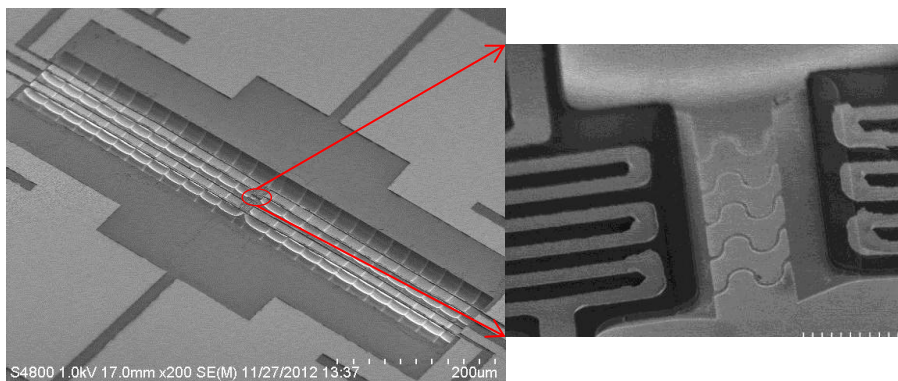
Figure 28: Straight structure of a suspended nanowire device by
using 3-layered nitride film

CHAPTER IV

MEASUREMENT AND DISCUSSION

The fabrication process flow of a suspended silicon nanowire device structure has been discussed in this dissertation. The purpose of fabricating such device was to measure the thermoelectric efficiency of the nanowires. From equation 2.9, thermal conductivity (k) measurement is the most complicated and susceptible to error because of unpredictable heat losses. A suspended structure was necessary to minimize the conductive heat loss, which is the dominant way of heat propagation. Heat losses through convection and radiation can be minimized by conducting the experiment in a vacuum chamber at room temperature. The experimental method was described in the previous chapter.

To check the functionality of the fabricated devices, a simple but effective experiment was conducted. Figure 29 shows a simple schematic of the setup.
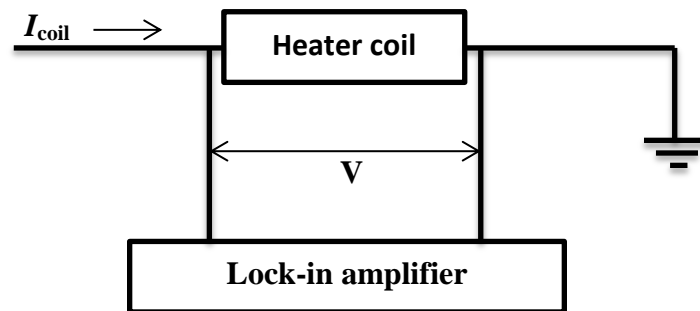
Figure 29: Schematic of the experimental setup

A very small ac current (~100nA) is passed through the coil and the voltage across the coil is input to a lock-in amplifier. Here ac current is used because the lock-in amplifier deals with only ac signals and lock-in amplifier is used for an accurate measurement.

From the Figure if, for $I_{coil} = i$ (ac only) the measured voltage is v, then the resistance of the coil r = v/i is the resistance of the coil before heating. Here it should be mentioned that the frequency effect on the resistance was very negligible. The change in impedance of the coil for a 10 kHz change in frequency (1 kHz to 11 kHz) was found only a few ohms. Therefore it can be assumed that the impedance of the coil was basically its resistance r during ac measurement. The cold side coil measurement is done in the same way. After the ac current measurement, a dc current I is passed through only the heater coil for heating up the membrane underneath it. The resistance of the coil increases with the increase in temperature. Therefore the voltage drop across the coil would be (V + v), where V represents the dc portion. Since the lock-in amplifier only measures the ac voltage drop across the heater coil, the resistance R measured this time will be r + Δr. Here Δr is the difference between r and R, before and after current flow I. The structure is suspended and the experiment is conducted under vacuum at room temperature. Therefore the induced heat for the dc current will mainly propagate by conduction through the nanowire which bridges the hot and cold membranes of the device. If the device is functional, the cold coil resistance will increase from its initial value measured by ac current flow like the hot coil.

The whole experiment was conducted on the device shown in Figure 21. Figure 30 shows the sample preparation process for testing. Wire bonds were done on the contact pads for making the electrical connections. In the main picture, arrangement of contact pads has been shown. Pad (1,2) and (5,6) are current pads for heater and sensor side respectively. On the other hand, pad (3,4) and (7,8) are for voltage measurement. Inset picture shows the current flow path for both coils.
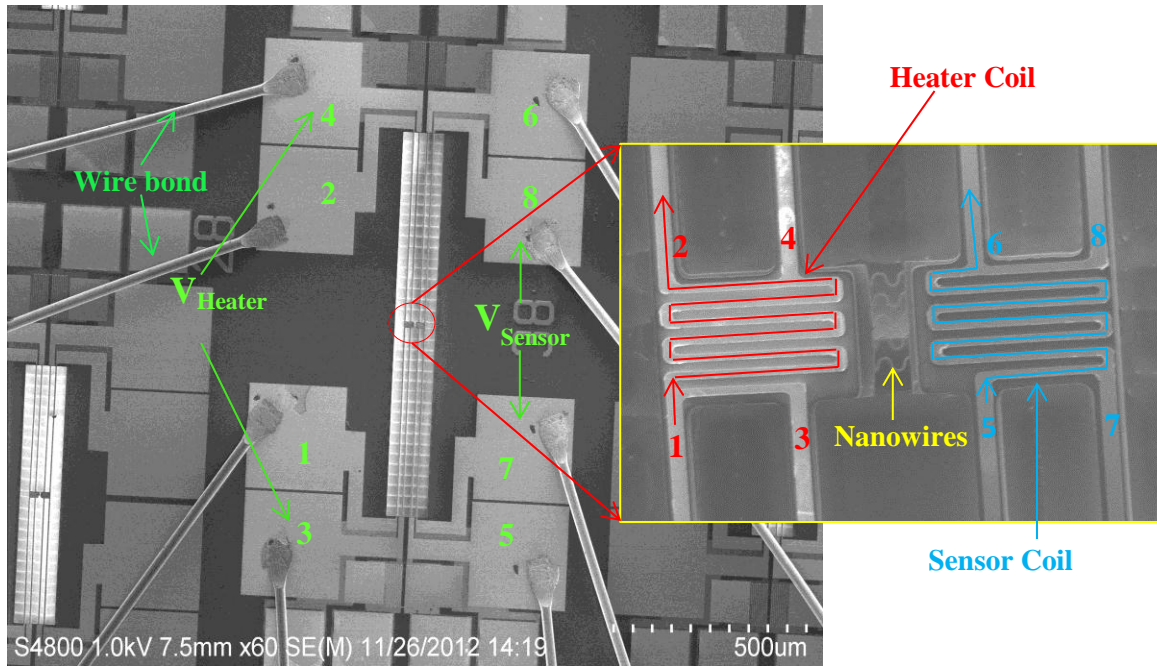
Figure 30: Devices after wire bonding for testing. Current and voltage pads are marked in the main picture. Inset shows the current flow paths

Figure 31 shows the experimental setup for the characterization. In the picture the sample is placed in the vacuum probe station. Inset shows the vacuum pump used to get the vacuum and a pressure in the range of 10^{-4} Torr is possible by this pump. N_2 gas was used to break the vacuum after experiment. The flow of N_2 can be controlled by a pressure gauge. An AMETEK 7270 DSP lock-in amplifier was used as the ac power supply as well as to measure the voltage across the coils. A FLUKE-287 multi-meter was connected in series to the DC power supply (Agilent E3631A) to measure the DC current flow for heating up the coil.
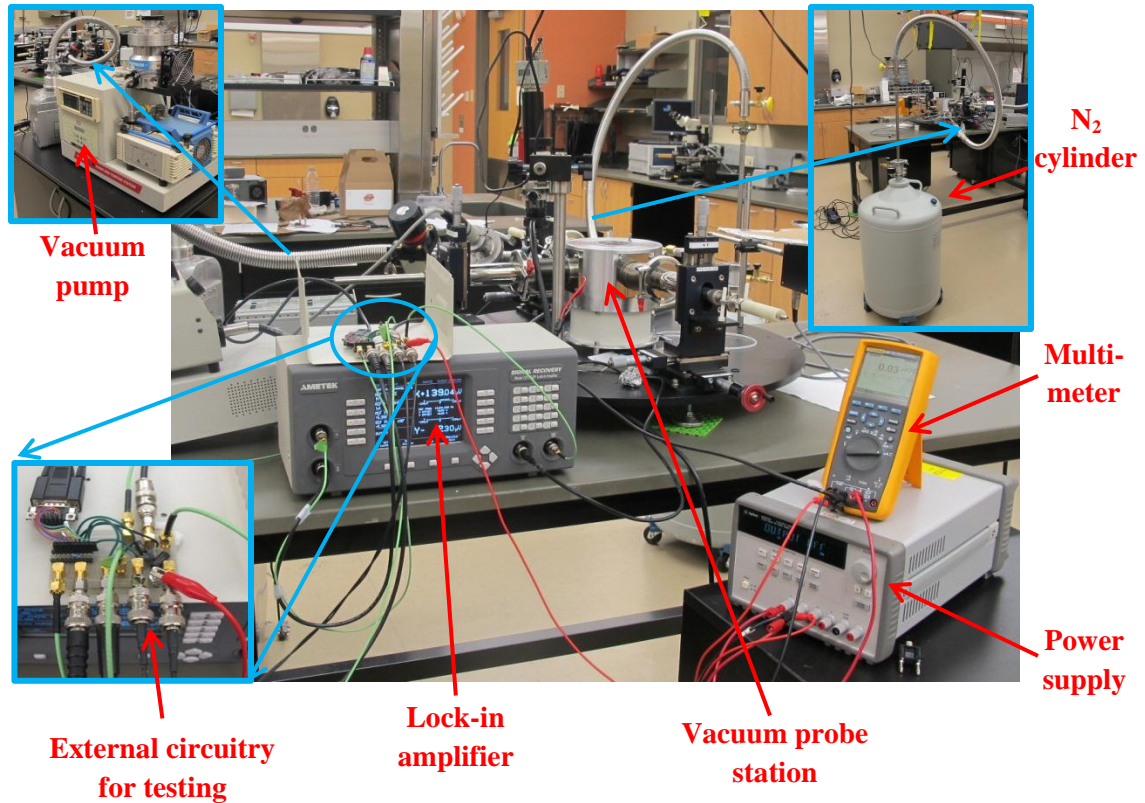
Figure 31: Experimental setup for characterization

Here it should be mentioned that before using a resistance as a temperature sensor, the temperature coefficient of the resistance (TCR) measurement is essential. For TCR measurement, the device sample was placed in the vacuum chamber (JANIS ST-500 probe station) on a metal plate which was connected to a temperature controller.

After placing the sample in the vacuum chamber, the temperature controller was set at room temperature (T_o) at first and the resistance was measured by a FLUKE-287 multi-meter. Then the temperature was increased by 10^oC and the resistance was measured again. The system should be given enough time for stabilization before measurement. Then the temperature coefficient of resistance α was calculated by using equation 3.4. The whole process was repeated for checking the validity and repeatability of α. Table 5 shows the collected data for TCR calculation.

Temperature (^{o}C)	Current flow (i) (μA)	Voltage drop across the coil (v) (mV)	$R_{coil} = v/i$ (Ω)
35	100.15	69.19	690.86
20	101.86	68.79	675.33

Table 5: Data for TCR measurement

By using equation 3.4 the resultant TCR was $1.5 \times 10^{-3} \Omega/^{o}$C. This value has been used for temperature measurement before and after dc current flow through the coil. Table 6 shows the data before and after dc current flow through the coil.

	r (Ω)	R (Ω)	Δr (Ω)	α ($\Omega/^{o}$C)	Temperature increase due to dc current flow (^{o}C)
Heater coil	847.5	853.8	6.3	0.0015	~4.9
Cold/sensor coil	890.5	892	1.5	0.0015	~1.1

Table 6: Resistance and temperature change data due to a dc current of 100nA

The changes in the resistances of cold/sensor coil indicate that heat was flowing through the nanowires, which proves the proper functionality of the device. Therefore the device is appropriate to conduct the experiment for thermoelectric measurement.

CHAPTER V

CONCLUSION

In this thesis, the fabrication process of poly-silicon nanowire devices has been described in details. The purpose of making the devices is to conduct experiment to measure the parameters for thermoelectric characterization. The device structure has some genuine advantages-

- The fabrication process flow is able to produce completely suspended and clean devices including the nanowires. With proper care it is possible to obtain high rate of survival of suspended devices with nanowires.

- The nanowires are patterned by EBL with is very compatible to the successive steps of the process flow. No extra care is needed for the nano-patterns.

- The nanowires are a part of the device and one doesn't need to do the complicated placement of the nanowire on the device to prepare the device for experiment. In this way the contact resistances at the both contacts of the nanowire can be avoided. Also the sample preparation becomes easier

- This device is useful for not only silicon, but also for all other thin films (<500nm) compatible to deposit on SiO2 surface and micro-fabrication process.

The motivation of this work was to introduce a functional and efficient device for complicated thermal conductivity measurement of silicon nanowires. Though the utilization of the device was

limited to silicon nanowire only for this work, one can extend the usage of the device for

nanowires of other materials.

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