FEASIBILITY STUDY OF A HIGH TEMPERATURE DC-DC CONVERTER EMPLOYING V^2 CONTROL ARCHITECTURE

By

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Hyderabad, Andhra Pradesh

India, 2003

Submitted to the Faculty of the
Graduate College of the
Oklahoma State University
in partial fulfillment of
the requirements for
the Degree of
MASTER OF SCIENCE
May, 2006

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Dedication

To my family…

ACKNOWLEDGEMENTS

Although it has just been just two years studying in Oklahoma State University, it is an experience that will stay with me forever. My stay in Stillwater has given me a lot to cherish, good friendships, an excellent studying environment to name a few.

First of all I would like to thank my parents, Vijayalakshmi Rayakota and Appa Rao Rayakota. They have inspired me throughout my life and have taught me never to give up. I would also like to thank my brother, Balaji Rayakota, for his constant support and encouragement.

I am thankful to all my colleagues in Mixed Signal VLSI (MSVLSI) lab for assisting and helping me on numerous occasions. I consider myself fortunate enough to have made a lot of good friends. I would like to thank all of them for the help and support they extended towards me.

I wish to extend my sincere appreciation to my adviser Dr. Chris Hutchens for his able guidance, intelligent supervision and inspiration that helped me finish this thesis. My sincere appreciation also extends to my committee members Dr. Yumin Zhang and Dr. Louis Johnson whose assistance and encouragement are also invaluable.

Finally, I would like to thank the Department of Electrical and Computer Engineering for supporting me during these two years of study.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Chapter 1

Introduction and Thesis organization

1.0 Thesis Introduction

This thesis is a feasibility study of a high-temperature step-down DC-DC converter employing V^2 control architecture. The objective of this study is to prove the feasibility of a high-temperature DC-DC converter and determine the design metrics on the individual components in the model to insure stability over a range of temperature from room temperature to 200°C. The study details the working of the V^2 control architecture (Chapter 3) with reference to a step-down DC-DC converter and aims at providing performance specifications for individual blocks in the feedback design.

The working of the V^2 control has been studied and relevant design equations have been developed (Chapter 3). A SPICE model for the V^2 control architecture has been developed as applicable to a buck converter. The model incorporates the individual blocks in the feedback system (Chapter 4). The model includes the implementation of a soft-start mechanism, Under-Voltage Lockout (UVLO) mechanism, Over Current (OC) protection and a 100% Duty Cycle (DC) comparator. The

design challenges involved with high temperature design of a V^2 control architecture have been detailed in Chapter 4. An iterative design algorithm has been developed that aids in the selection of design parameters in the design of the DC-DC converter (Chapter 4).

The developed model has been tested against a given set of input specifications to observe the response of the model for variations in line and load conditions. The effect of temperature variation on the response of the model has also been observed (Chapter 4). The design example takes a 25V input voltage and steps it down to 5V with an accuracy of better than 5% output voltage regulation over variations in line, load and temperature. The model is shown to work for the given input specifications at both room temperature and 200°C.

1.1 Motivation

The oil field reservoir development and recovery industry has requirements for DC-DC converters with an ambient temperature greater than 200°C [1]. The DC-DC converters are used to power up electronic equipments used in down-hole oil exploration and recovery. This has led to research in the issues involved in the design of a DC-DC converter system that can operate over a range of temperatures ranging from room temperature to greater than 200°C. The research undertaken in this thesis focuses on the design of a V^2 control architecture for elevated temperature applications.

The choice of V^2 control architecture as the feedback mechanism for output voltage regulation is prompted by the need for a feedback architecture that has a fast transient response time to variations in load and line conditions. As more and more complex integrated circuits are being designed for higher and higher speeds, power consumption has become an important issue in integrated circuit design. The most general solution for this problem is the reduction in the power supply voltage levels. But this decrease in the power supply levels has resulted in an increase in the current slew rate as the integrated circuits switch from one mode to another [3]. Thus the increase in the current slew rates has prompted for DC-DC converters with faster transient response times while still maintaining the output voltage efficiencies. Literature [2] shows the V^2 control architecture to have a faster transient response compared to voltage mode and current mode control mechanisms [2]. Power demands of computing and telecom applications are driving rapid developments in semiconductor components for power conversion [4]. Thus the obvious choice of control mechanism for the next generation extreme temperature DC-DC systems is V^2 control architecture.

A system-level model of voltage mode control, current mode control and V^2 mode control has been developed [5] and a comparison of the response times to changes in the load conditions to all the three models has been undertaken. The simulation results show that for the same input specifications V^2 control architecture provides the fastest transient response time. In this thesis, the system-level model developed in [5] has been extended to SPICE level circuit model V^2 architecture as applicable to a buck converter to perform the step-down operation. The developed model is used to provide design specifications for the individual blocks in the feedback system which would insure system stability.

1.2 Thesis Organization

This thesis is divided into five chapters. Chapter 2 explains the working of the buck converter. The input-output transfer function for a buck converter has been derived and the problems with the stability of a buck converter without the implementation of an appropriate compensation network have been discussed. The need for a feedback structure has been explained and a brief discussion on the advantages of the V^2 control architecture over the other feedback architecture has been presented. The complexity in the design of the compensation network for other control mechanisms has been explained by way of reviewing a Type II compensation network for a voltage mode control. A brief discussion of the switch mode regulators as against linear regulators has been given with stress on the advantages of a switch mode regulator over a linear regulator. Chapter 3 outlines the working of a V^2 control mechanism. A detailed explanation of the proposed model is presented and the working of all the individual blocks is explained. Next the SPICE model of the buck converter employing the V^2 control mechanism has been shown. Simulation results have been presented for the design for a given set of input specifications to demonstrate that the model functionality. The performance metrics of the individual blocks and the discrete components in the design are tabulated symbolically. The developed model is shown to work for a 25V-5V step-down conversion with better than 5% output dc regulation at 150KHz. Chapter 4 details the issues involved in high temperature design in an SOS (Silicon On Sapphire) process. The individual design blocks in the design of the feedback system are analyzed from a circuit level implementation perspective. Various circuit implementations of the individual

blocks have been discussed and an optimal design topology has been suggested to meet the performance metrics that had been identified in Chapter3. Chapter 5 presents the conclusion of this thesis proving the feasibility of a step-down DC-DC converter system for elevated temperature applications. Future works that can be carried out beyond this study are aimed at a printed circuit board implementation of this design. This is recommended along with further suggestions on improving the design to better the performance metrics from a power consumption/effiency perspective have been detailed in Chapter 5.

Chapter 2

Buck Converter

2.0 Introduction

In this section the working of a buck converter is explained. A Buck converter is used to perform the step-down voltage conversion. A buck converter is shown in figure 2.1.

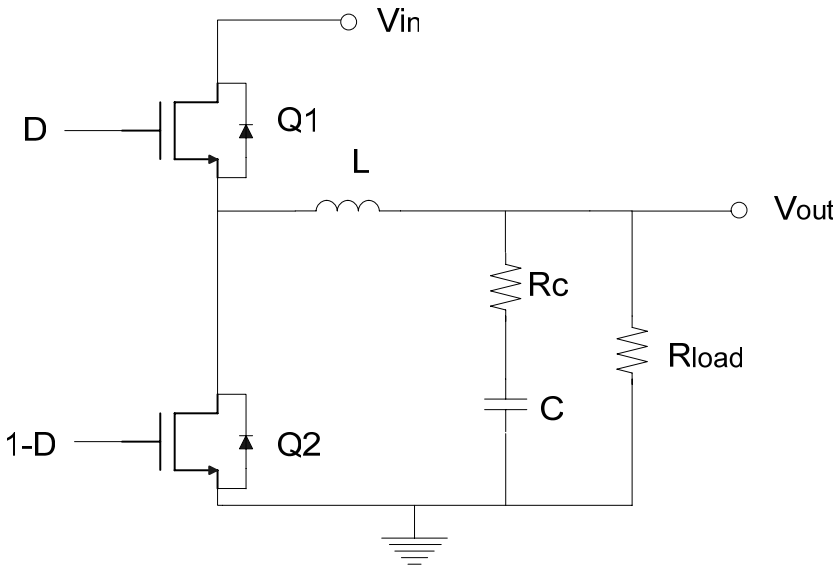

Figure 2.1: Buck Converter

As can be seen from figure 2.1 a buck converter consists of an LC low pass filter at its output with power MOSFETs M1 and M2 that connect the inductor to the input voltage Vin (via M1) and ground (via M2) in a periodic fashion. MOSFET M1 is ON for

D times the switching period, Tsw, of the buck converter while M2 is ON for the rest of the switching period. The Buck Converter in conjunction with the feedback control loop performs the step-down voltage conversion in the DC-DC converter.

D and 1-D are complementary digital signals that simultaneously turn on and turn off the power MOSFETs M1 and M2 respectively [5]. The source of these complementary signals is the PWM (Pulse Width Modulated) feedback control loop (not shown in figure 2.1). The PWM controller modulates the on/off action of the high side switch M1 (shown as D in figure 2.1) to regulate the output voltage. A complementary switching action governs the low side M2 (shown as 1-D in figure 2.1). When the transistor M1 is on and M2 is off, the input voltage appears across the inductor and current in the inductor increases linearly. In this same cycle the capacitor is charged thus increasing the voltage at the output node in a linear ramp. When transistor M2 is ON and M1 is OFF, the inductor node that was connected to the input voltage Vin is now connected to ground. The voltage across the inductor is reversed to maintain the current flow via the inductor. However, current in the inductor cannot change instantaneously and the current starts decreasing in a linear fashion. In this cycle the capacitor is charged with the energy stored in the inductor while being discharged by the load. A non-overlapping time is always inserted between the turn-on signals of M1 and M2 to prevent cross conduction. To ensure the continuation of the inductor current, the body diode of the M2 will temporarily conduct when both switches are turned off.

In the next few paragraphs the equations that govern the working of the buck converter in its two states of operation are detailed. The analysis is done using a method known as Inductor Volt-Second Balance wherein the equations for current flow via the inductor in both the states are analyzed and the input-output relationship is determined in terms of the duty cycle, D.

In the first state wherein the input voltage Vin is connected to the inductor-capacitor filter via MOSFET M1, a voltage of Vin-Vout is applied across the inductor to make its current linearly increase and as a result the output voltage ramps up linearly owing to the charging of the output capacitor through the inductor. Here Vout is the voltage at the output of the buck converter (figure 2.1). The equations that govern the operation of the circuit when M1 is ON and M2 is OFF are [6]

$$\frac{di_L}{dt} = \frac{V_{in} - V_{out}}{L} \tag{2.1}$$

$$\frac{dV_{out}}{dt} = \frac{i_L - V_{out}/R}{C} \tag{2.2}$$

The equations that govern the operation of the circuit when M1 is OFF and M2 is ON are

$$\frac{di_L}{dt} = -\frac{V_{out}}{L} \tag{2.3}$$

$$\frac{dV_{out}}{dt} = \frac{i_L - V_{out}/R}{C} \tag{2.4}$$

Analyzing the inductor current waveform determines the relationship between output and input voltage in terms of duty cycle. Inductor current is found by integrating

the inductor voltage waveform. Inductor voltage and current waveforms for a buck converter are as shown in figure 2.2.

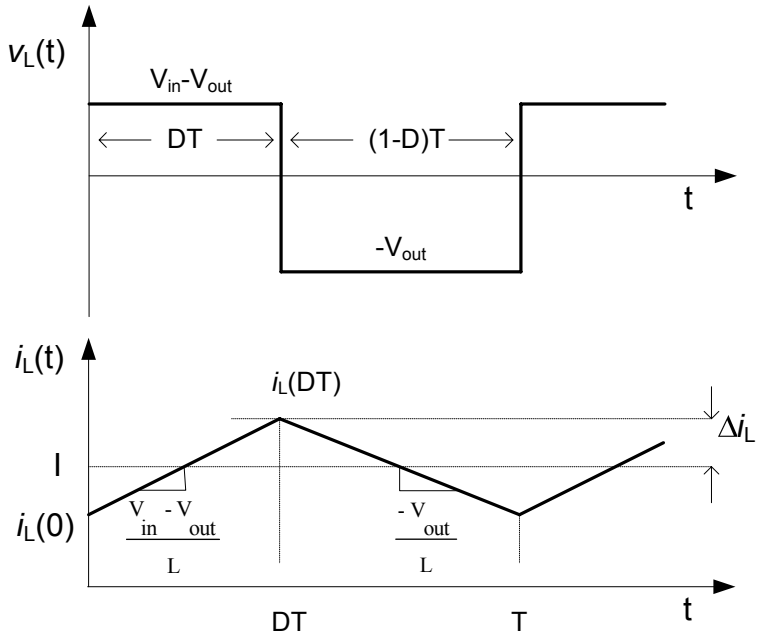

Figure 2.2: Inductor voltage and current waveforms

In steady state, the observation that over one switching period the net change in inductor current is zero is the principle of inductor volt second balance. The inductor voltage definition is given by [7]

$$v_L(t) = L\frac{di_L}{dt} \tag{2.5}$$

Integration over one complete switching period yields,

$$i_L(T_{SW}) - i_L(0) = \frac{1}{L}\int_0^{T_{sw}} v_L(t)dt \tag{2.6}$$

The left hand side of equation (2.9) is zero. As a result (2.2) can be written as

$$\int_0^{T_{sw}} v_L(t)dt = 0 \tag{2.7}$$

Equation (2.7) has the unit of volt-seconds or flux-linkages. Also, total area under the $V_L(t)$ waveform over one switching period must be zero. The area under the $V_L(t)$ curve is given by

$$A = \int_0^{T_{sw}} v_L(t)dt = (V_{in}\text{-}V_{out})\times(D\times T) + (-V_{out})\times(1\text{-}D)\times T) \tag{2.8}$$

Average value of inductor voltage is given by,

$$\langle v_L \rangle = \frac{A}{T_{sw}} = D\times(V_{in}\text{-}V_{out}) + (1\text{-}D)\times(-V_{out}) \tag{2.9}$$

By equating $\langle v_L \rangle$ to zero and solving for Vout yields the average output voltage as

$$V_{out} = D\times V_{in} \tag{2.10}$$

2.1 Transfer Function

The open loop buck converter system is shown in figure Fig. 2.3.

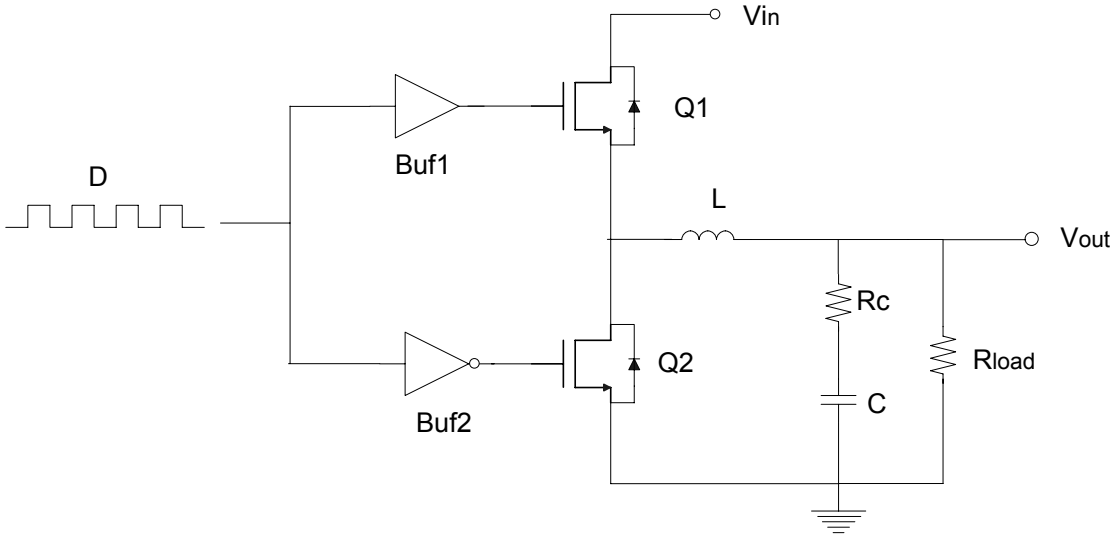

Figure 2.3: Open loop Buck converter system

In figure 2.3, D is fed to M1 and M2 via buffers Buf1 and Buf2 to control the ON-OFF action of M1 and M2. Note that Buf1 is a non-inverting buffer whereas Buf2 is an inverting buffer. This is done so that M1 and M2 are switched ON and OFF in a complementary fashion.

The transfer function of the open loop system gives the location of the poles and zeros of the system. It is important to look at the poles and zeros of the open loop system because the location of poles and zeros determine whether the system has sufficient phase margin to guarantee stability over the entire frequency range of operation. The transfer function of the open loop system is derived using the state-space averaging approach wherein the buck converter is analyzed in its two states of operation [8]. The two states of operation are (i) when M1 is ON and M2 is OFF wherein the current via the inductor ramps up linearly and the output voltage across the capacitor also rises linearly in a ramp fashion and (ii) when M1 is OFF and M2 is ON wherein the input voltage is isolated from the LC filter section leading to the capacitor discharging via the inductor to ground. The derivation of the transfer function is not presented here. It can be found in [8]. The open loop transfer function is given as

$$G_d(s) = \frac{V_O}{D}\left[\frac{1 + sCR_C}{1 + s\left[\frac{L}{R + R_{ON} + R_L} + \frac{CR(R_{ON} + R_L)}{R + R_{ON} + R_L} + CR_C\right] + s^2 LC\left[\frac{R + R_C}{R + R_{ON} + R_L}\right]}\right] \tag{2.11}$$

where,

C = Output Capacitance,

L = Output Inductance,

R = Load Resistance,

R_{ON} = On Resistance of the Power MOSFET,

R_C = ESR of the Capacitor,

R_L = Series Resistance of the Inductor.

Equation (2.11) for the transfer function of the buck converter takes into account the equivalent series resistance of the output inductor, R_L and the ON resistance of the power MOSFET, R_{ON}. As can be seen from equation (2.11), the transfer function exhibits a zero and two pole frequencies (since the order of the numerator is one and the order of the denominator is two). The zero frequency is due to the output capacitor and the ESR (Equivalent Series Resistance) associated with the output capacitor. If the numerical value of R_{ON} and R_L are much less than the numerical value of R, the load resistance then the system exhibits a double pole frequency instead of two poles at two different frequency locations. The double pole frequency is due to the output inductor and output capacitor combination. At frequencies around the double pole frequency the system transfer function has a phase of around -180° which can lead to potential oscillations when negative feedback is applied [14]. This is because a negative feedback around the buck converter by definition gives a -180° phase shift and if the buck converter itself provides a phase shift of -180° then the total phase of the closed loop system will be 0° i.e. positive feedback.

The expressions for the double pole frequency, f_{LC} and the zero frequency, f_{ESR} can be derived from the transfer function of equation 2.14 as

$$f_{LC} \approx \frac{1}{2\pi\sqrt{LC}}$$
$$f_{ESR} = \frac{1}{2\pi R_C C} \tag{2.12}$$

The open loop Bode response of the buck converter is shown in Fig. 2.4. In figure 2.4, the double pole frequency location is shown as f_{LC} and the zero frequency is shown as f_{ESR}.

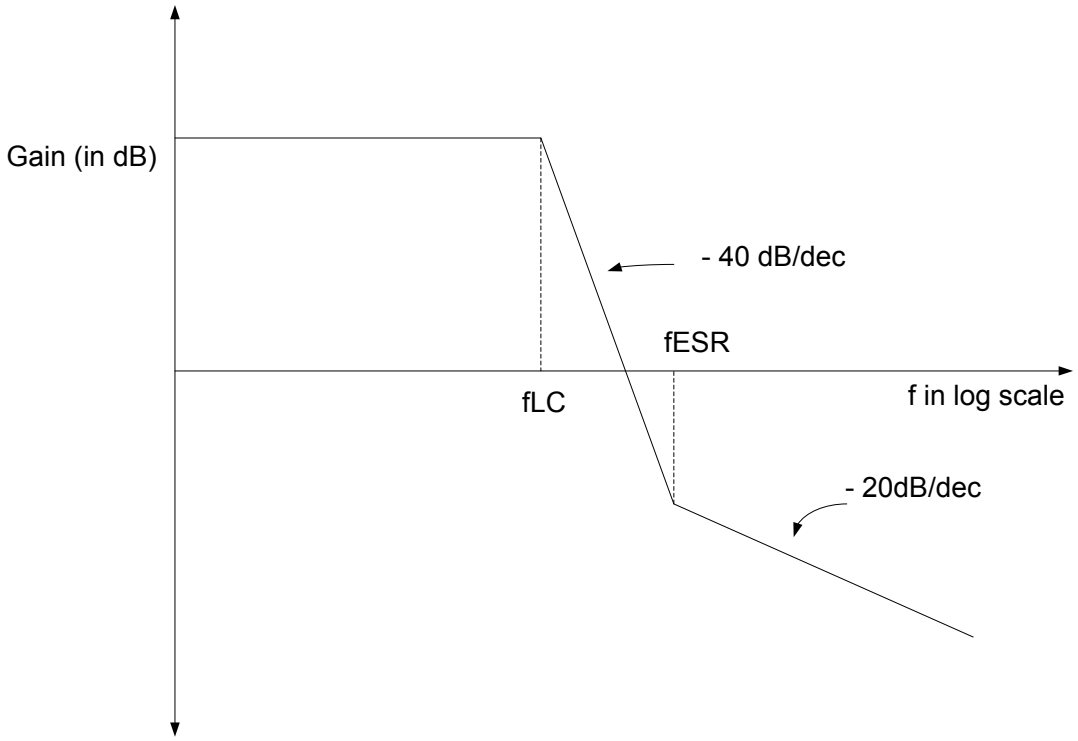

Figure 2.4: Open loop frequency response of the Buck converter

The double pole can cause the phase margin of the open loop system to approach 0° which is not good for system stability. The system may not oscillate but can be very underdamped at the operating frequency resulting in system instability. The Bode phase response of the open loop system is shown in figure 2.5. As seen in the figure the phase starts at 0° at starts to fall at the rate of -90°/dec at about $0.1f_{LC}$. The phase response

finally degrades to around -180° at $10f_{LC}$. To maintain the output voltage regulation negative feedback is employed which by definition adds at phase shift of -180° of its own. This phase shift combined with the -180° at $10f_{LC}$ corresponds to a total phase shift of 360° which leads to system instability manifested at the output in the form of oscillations leading to improper system functionality. The effect of the zero frequency beginning at $0.1f_{ESR}$ is also shown. The net effect of the zero frequency is that it lifts the phase of the open loop system to around -90° at around 10 f_{ESR}.

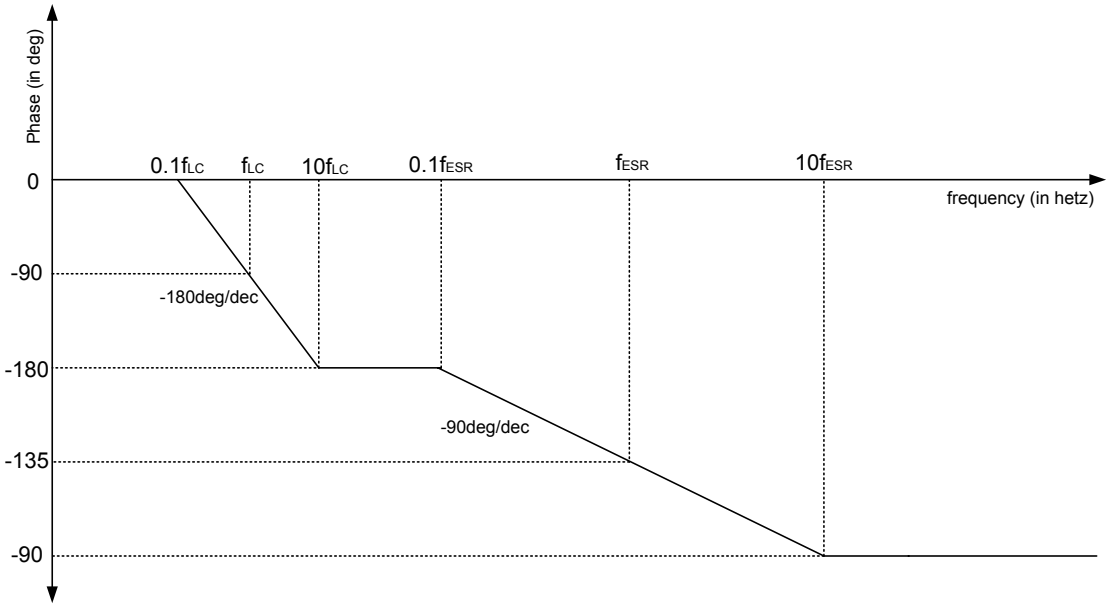

Figure 2.5: Open loop phase response of the Buck converter

For systems with a very low ESR, the phase will experience a very sharp slope downward at the double pole while the gain will have a high peak at the double pole frequency. Systems that have such resonant output filters will be more difficult to compensate.

Looking at the magnitude and phase plots of the open loop system it is very obvious that the source of the problem is the location of the double pole frequency, f_{LC}.

The double pole frequency must be compensated with a zero placed at or less than $0.1f_{LC}$ in the frequency domain. This insures the phase margin of the system will be around -90° at f_{LC} thus preventing oscillations. With adequate gain it is now feasible to design the control system to have an acceptable PM.

2.3 Feedback Control

The output voltage needs to be held in regulation for changes in line and load conditions. This is accomplished by using some form of feedback mechanism which senses the changes in the output voltage and adjusts the open loop response so that the output voltage remains constant. The buck converter system can be controlled in two ways, namely,

1. Constant-frequency operation or pulse-width modulation control.
2. Variable-frequency operation or control by frequency modulation.

With pulse-width modulation control, the regulation of output voltage is achieved by varying the duty cycle while keeping the frequency of operation constant. Usually control by pulse width modulation is preferred over constant frequency operation as it allows easier optimization of the LC filter selection and control of the ripple content in the output voltage. On the other hand, if the load on the converter is below a certain level, voltage regulation of output becomes a problem and in such a case, control by frequency modulation is to be preferred [9]. In frequency modulation control, the ON period of the power MOSFET (duty cycle) is kept constant while modulating the frequency of

operation in accordance with the changes in the output voltage. The drawback of this method of control is that the design of the LC filter is more complex.

From the derivations of the duty cycle of a buck converter in section 2.1, it can be seen that changing the duty cycle controls the steady-state output with respect to the input voltage. This is a key concept governing all inductor-based switching circuits. Negative feedback is employed to maintain the output voltage constant regardless of disturbances in input voltage or load current. The duty cycle is varied in the feedback loop to compensate for these variations. A typical block diagram of a Switching regulator is as shown in figure 2.6 [10].

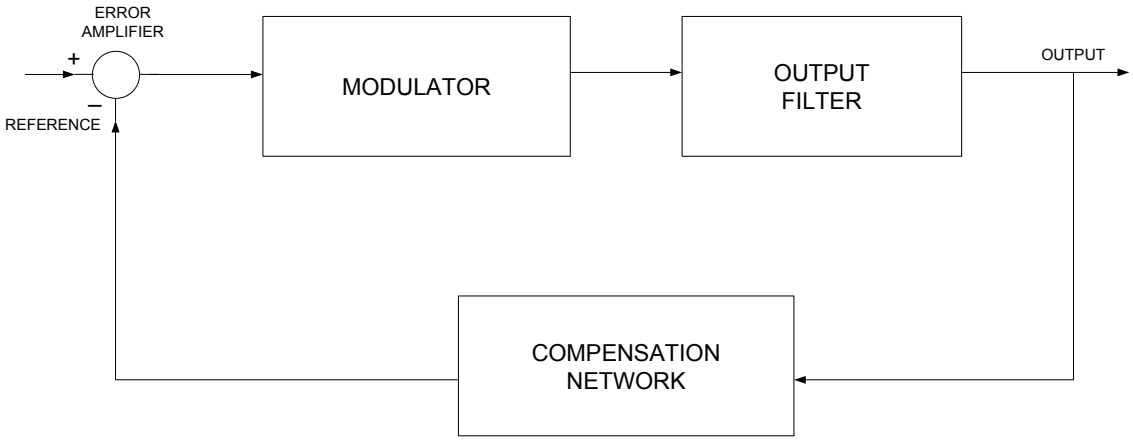

Figure 2.6: Block diagram of Switching Regulator

The output filter shown in the figure above is the buck converter with its LC filter section. The output of the buck converter is fed to a compensation network that compensates for the double pole frequency inherent in the transfer function of an open loop buck converter. The output of the compensation network is then compared with a reference voltage and their difference is given to a modulator. The difference signal is generated from an Error Amplifier. The modulator modulates either the duty cycle, in the

case of a pulse width modulated system, or the frequency of operation, in the case of frequency modulated system thus regulating the output voltage of the buck converter.

In this thesis a pulse-width modulated feedback system is chosen. Figure 2.7 shows a pulse-width modulated (PWM) system.

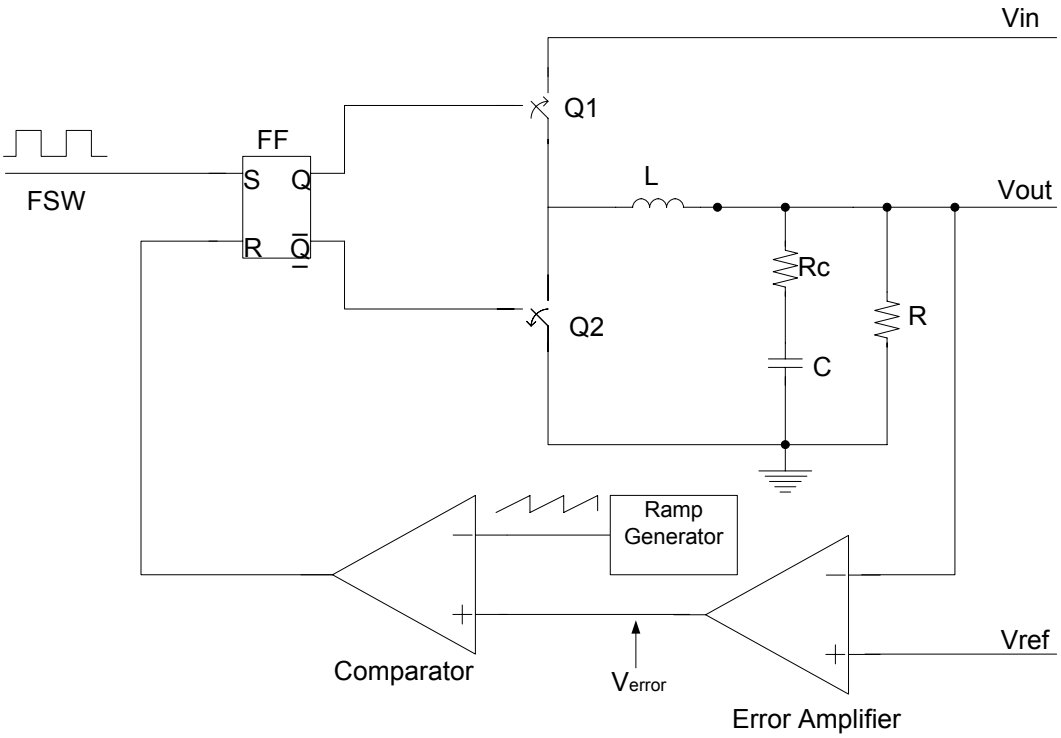

Figure 2.7: Feedback control of a buck converter

This method takes the output voltage and subtracts it from a reference voltage to generate an error signal (V_{error}). This error signal compared with an oscillator ramp signal. The comparator outputs a digital output (PWM) that modulates the ON/OFF action of the power MOSFETs M1 and M2 thus modulating the duty cycle of the buck converter as the output voltage changes. When the output voltage changes, V_{error} also changes causing the comparator output to change which in turn changes the pulse width of the duty cycle. This change in duty cycle causes the output voltage to change reducing

the error signal to zero, thus completing the control loop. The source of the ramp voltage differentiates between the different feedback topologies.

The three most common control schemes are voltage mode control, current mode control and V^2 control. Other hybrid schemes are derived from combinations of these control schemes. A discussion of the working of voltage and current mode controls along with their SIMULINK models is given in [8]. A comparison of their advantages and disadvantages has also been provided.

The feedback structure needs to incorporate a compensation network to compensate for the double pole frequency f_{LC} to improve system stability and avoid oscillations. As suggested in section 2.2 this is done by introducing a zero with the compensation network at approximately $0.1f_{LC}$. In the next few paragraphs the complexity in designing a compensation network for a voltage mode control scheme is shown. The ease with which a V^2 control architecture is implemented can be appreciated only when the difficulty in the designing the compensation network for other control schemes is realized. For simplicity of discussion a Type II compensation scheme, which is relatively easy to design, compared to Type III compensation scheme, is shown here. The relevant design equations are also detailed.

2.3.0 Type II Compensation

Figure 2.8 shows a generic Type II compensation network [9]. The Type II network helps to shape the profile of the gain with respect to frequency and gives a 90° boost to the phase. The phase boost is necessary to compensate for the double frequency due to the output LC filter in the buck converter.

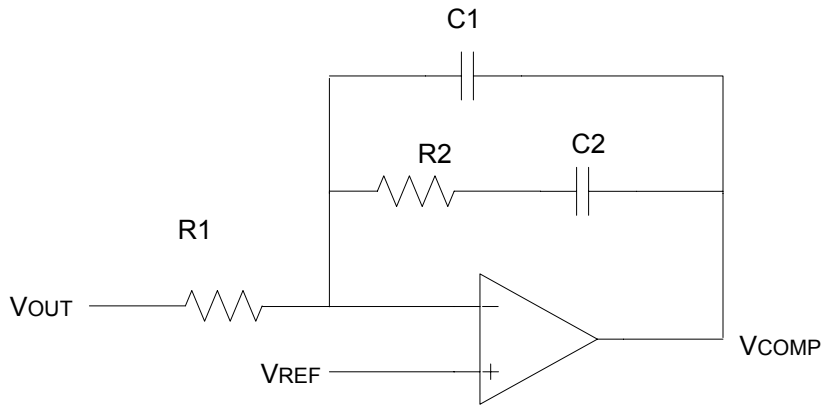

Figure: 2.8: Type II Compensation

The transfer function of Type II compensation exhibits a zero and a pole frequency. The zero frequency, f_{ZERO} is given as

$$f_{ZERO} = \frac{1}{2\pi \cdot \mathrm{R}_2 \cdot \mathrm{C}_2} \tag{2.13}$$

This zero frequency has to be designed to be at a frequency of one-tenth the double pole frequency of the buck converter, f_{LC} so that it partially compensates for the -180° phase shift resulting from the double pole. The compensation network also introduces a pole, f_{POLE}, given as

$$f_{POLE} = \frac{1}{2\pi \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2} \right)} \tag{2.14}$$

This pole frequency must be designed to be greater than ten times the bandwidth of the closed loop system so that the pole from the compensation network does not add any appreciable phase shift of its own to the closed loop system. This condition places a great demand on the design of the error amplifier since the error amplifier must now be designed with a bandwidth of at least ten times the bandwidth of the closed loop buck converter system. Figure 2.9 shows Bode plot of a Type II compensation network. The location of the zero and pole frequency are shown and the corresponding effect on the phase plot of the compensation network is also shown.

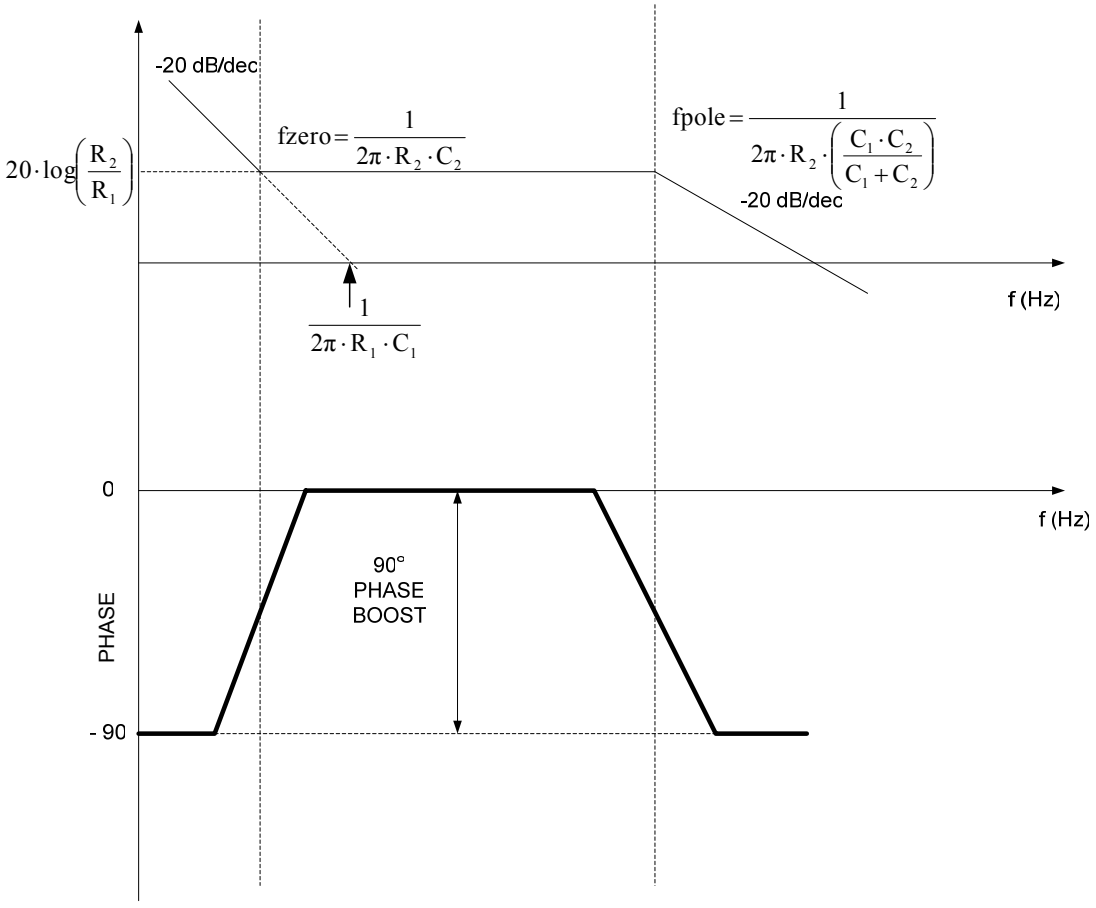

Figure 2.9: Frequency response of a Type II Compensation Network

The design of the compensation network is discussed next. The following guidelines in conjunction with equations 2.13 and 2.14 will help calculate the component values for a Type II network [9].

1. Choose a value for R1, usually between 2k and 5k.
2. The compensation network gain is (R2/R1). The Bode plot of the buck converter will be increased by this value when the compensation network is connected in the feedback. This also increases the bandwidth of the closed loop system as shown in figure 2.10 below.

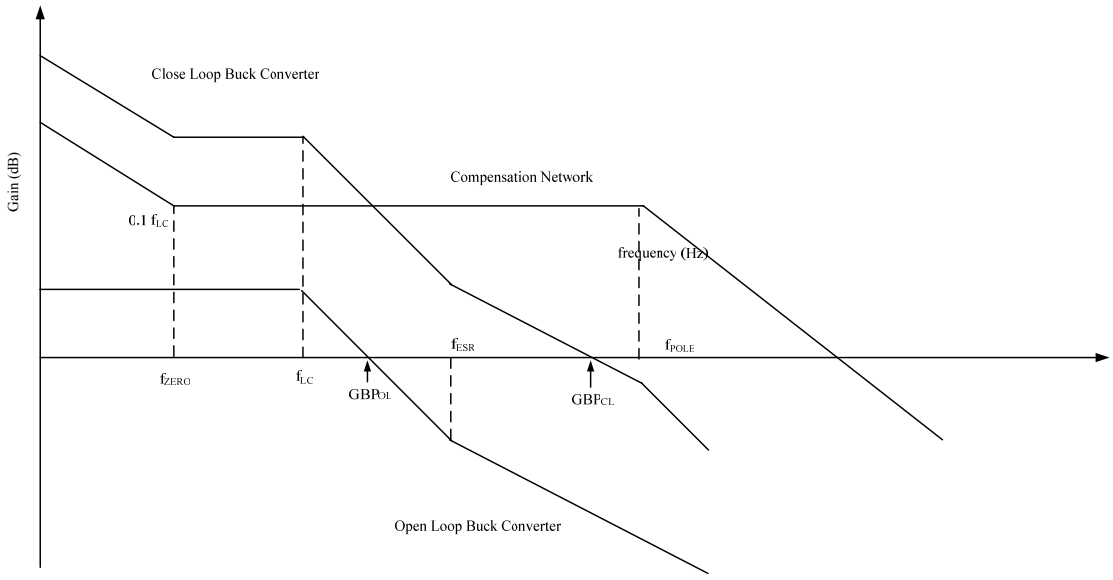

Figure 2.10: Frequency response of a Type II Compensation Network

The following equation will calculate an R2 that will accomplish this given the system parameters and a chosen R1.

$$R_2 = \left(\frac{f_{ESR}}{f_{LC}}\right)^2 \times \frac{GBP_{CL}}{f_{ESR}} \times \frac{\Delta V}{V_{in}} \times R_1 \qquad (2.15)$$

3. Calculate C2 by placing the zero at one-tenth the double pole frequency f_{LC}.

$$C_2 = \frac{10}{2\pi \times R_2 \times f_{LC}} \tag{2.16}$$

4. Calculate C1 by placing the second pole at half the switching frequency, f_{sw}.

$$C_1 = \frac{C_2}{\pi \times R_2 \times C_2 \times f_{sw} - 1} \tag{2.17}$$

From the discussion in the previous few paragraphs we observe that the compensation network design for a voltage mode control is complicated and involves a number of steps. On the other hand V^2 control mechanism offers a very simple compensation network in the form of a compensation capacitor at the output of the error amplifier [3]. The compensation network scheme of a V^2 control scheme will be explained in chapter 3.

2.4 Design Issues

In this section the some of the primary design issues involved in the design of a buck converter are outlined. The topics covered are the selection of the output capacitor and inductor in the buck converter stage and the choice of synchronous buck regulators against conventional buck regulators.

2.4.0 Inductor

An inductor is used in a filter to reduce the ac current ripple at the output of the buck converter. This reduction occurs because current through the inductor cannot change suddenly and so when the current through an inductor tends to fall (during the

negative clock cycle when the low side MOSFET is ON and the high side MOSFET is OFF), the inductor tends to maintain the current by acting as a source. The inductance and current-carrying capability of the inductor is very straightforward to calculate. The size of the inductor is selected such that a certain ripple current requirement is met which is given as part of the input design specifications. The amount of allowable ripple current and the equivalent series resistance (ESR) of the output capacitor combined to determine the output ripple voltage present at the output. Solving the standard inductor equation for inductor ripple current (ΔIL) yields,

$$\Delta I_L = (V_{in} - V_{out}) \times \frac{D}{L} \times T_{sw} \tag{2.18}$$

The peak inductor current is calculated by

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{1}{2} \times \Delta I_L \tag{2.19}$$

The inductor selection must be completed using the maximum input voltage for which the buck converter is being designed as this will determine the worst case losses from the inductor, the maximum peak current via the inductor and the maximum energy the inductor must handle [11].

2.4.1 Capacitor

A capacitor is used in the filter to reduce output voltage ripple. Since switched power regulators are usually used in high current, high-performance power supplies, the capacitor should be chosen for minimum loss. Loss in a capacitor occurs because of its internal series resistance. Capacitors for switched regulators are chosen on the basis of effective series resistance (ESR). The output capacitor is chosen to meet the output ripple

specification and to provide storage for load transients. To reduce the output voltage ripple ESR of the output capacitor can be reduced by choosing a parallel combination of capacitors instead of a single output capacitor. Solving the standard capacitor equation for the output ripple voltage (ΔV_C) yields

$$\Delta V = I_L \cdot R_c \tag{2.20}$$

As previously stated the ripple voltage in the above equation is due to the ESR of the output capacitor.

2.4.2 Conventional vs. synchronous buck regulators

In figure 2.1 MOSFETs M1 and M2 act as switches that switch in and out the input voltage to the LC filter. The switches can be implemented as in figure 2.1 with two power MOSFETs or M1 can be implemented with a power MOSFET and M2 with a reverse biased Schottky diode (figure 2.10). The buck converter configuration shown in figure 2.1 is known as a synchronous buck regulator whereas the buck converter configuration shown in figure 2.10 is known as a conventional buck regulator. In this section the advantages and disadvantages of conventional regulators as against synchronous regulators are discussed and the choice of a synchronous buck regulator in this thesis is justified.

A conventional buck regulator using a power MOSFET and a Schottky diode as its two main switching devices is shown in figure 2.10 [12]. The operation of this buck regulator is explained next. When the MOSFET is turned ON, the input voltage Vin is applied to the LC filter. When the MOSFET turns off, the output capacitor discharges to

ground via the Schottky diode. In this way, the MOSFET along with the diode regulates the output voltage of the buck converter. One of the largest power-loss factors in a conventional buck regulator is the Schottky diode. The power dissipated is simply the forward voltage drop multiplied by the current going through it. The reverse recovery for silicon diodes creates an even greater loss. These power losses reduce overall efficiency of the buck regulator.

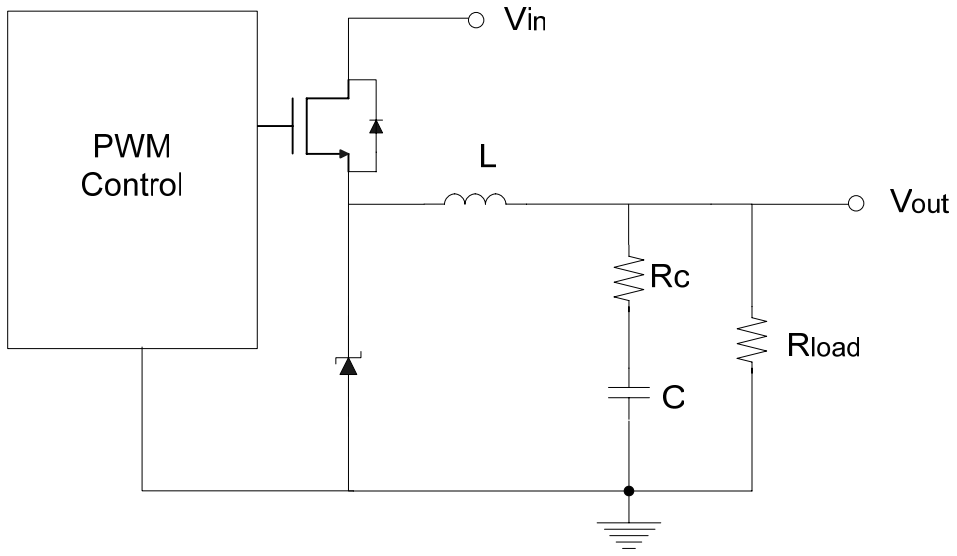

Figure 2.10: Conventional Buck Regulator

A synchronous buck regulator is shown in figure 2.11 for comparison with the one in figure 2.10. Here the output regulation is done by using two power MOSFETs that are switched ON and OFF simultaneously in a periodic fashion thus producing a stepped-down DC voltage at the output. The operation of a synchronous Buck converter was previously reviewed in section 2.0 and will not be repeated here.

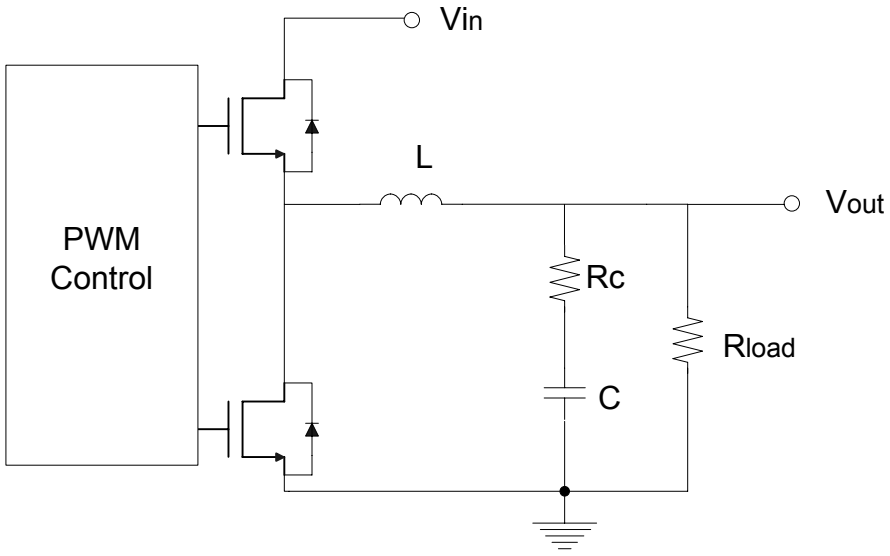

Figure 2.11: Synchronous Buck Regulator

A synchronous buck regulator minimizes the power loss due to the Schottky diode by replacing it with a power MOSFET (figure 2.11), increasing the efficiency of the converter. This is because the voltage drop across the MOSFET is smaller than the forward voltage drop of the Schottky diode. When the MOSFET is ON current flows through the MOSFET and due to its very low channel resistance the forward voltage drop of the MOSFET is very low. Synchronous rectification using MOSFETs causes variable switching delays due to the variation in the gate charge and threshold voltages from one MOSFET to another [12]. This problem can be solved by delaying the turn-on drive of the low side MOSFET until the gate of the high side MOSFET has fallen below its threshold voltage. Such a mechanism introduces a dead time between the turn-on and turn-off of the high side and low side MOSFET so that both of them are not simultaneously conducting. During the dead times, the inductor current flows through the lower MOSFET's body diode and develops stored charge in the depletion region of the

MOSFET. This stored charge must be removed so that the body diode is reverse-biased again. The time it takes to remove this stored charge increase reverse recovery time of the converter reducing the converter's efficiency. This problem is mitigated by placing a Schottky diode in parallel with the lower MOSFET as shown in figure 2.12.

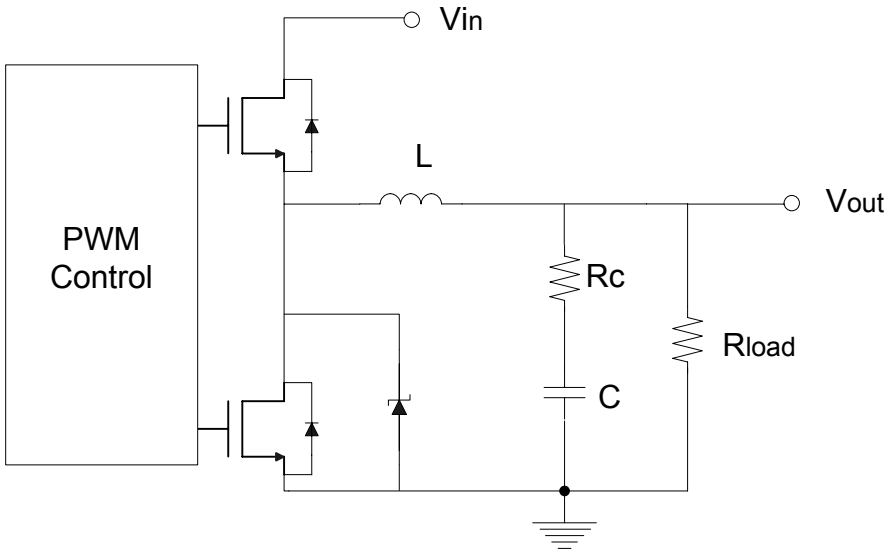

Figure 2.12: Synchronous Buck Regulator with Schottky diode

Chapter 3

V^2 Architecture

3.0 Introduction

V^2 control scheme is a novel control architecture that has been widely accepted in the industry as the control scheme with the fastest transient response to variations in load and line conditions. The V^2 control scheme offers inherent over-voltage protection and ease in the design of the compensation network in addition to the improvement in the transient response time over other control schemes [2].

In this chapter the working of V^2 control architecture and the design strategy in designing a DC-DC converter employing V^2 control is explained. Section 3.1 explains the working of V^2 control architecture. As was explained in section 2.3 the design of any buck converter requires the implementation of a feedback mechanism to hold the output voltage in regulation during load and line variations. A compensation network in the feedback loop is needed to boost the phase margin of the closed loop system to avoid oscillations. The implementation of the compensation network for V^2 control is explained in section 3.2. Section 3.3 explains the design philosophy of a DC-DC converter

employing V^2 control mechanism. Finally section 3.4 discusses the issues involved with high-temperature design of Integrated Circuits (ICs).

3.1 Working of V^2 architecture

The working of the V^2 control architecture is explained in this section. A simplified block diagram of the V^2 control scheme is as shown in figure 3.1.

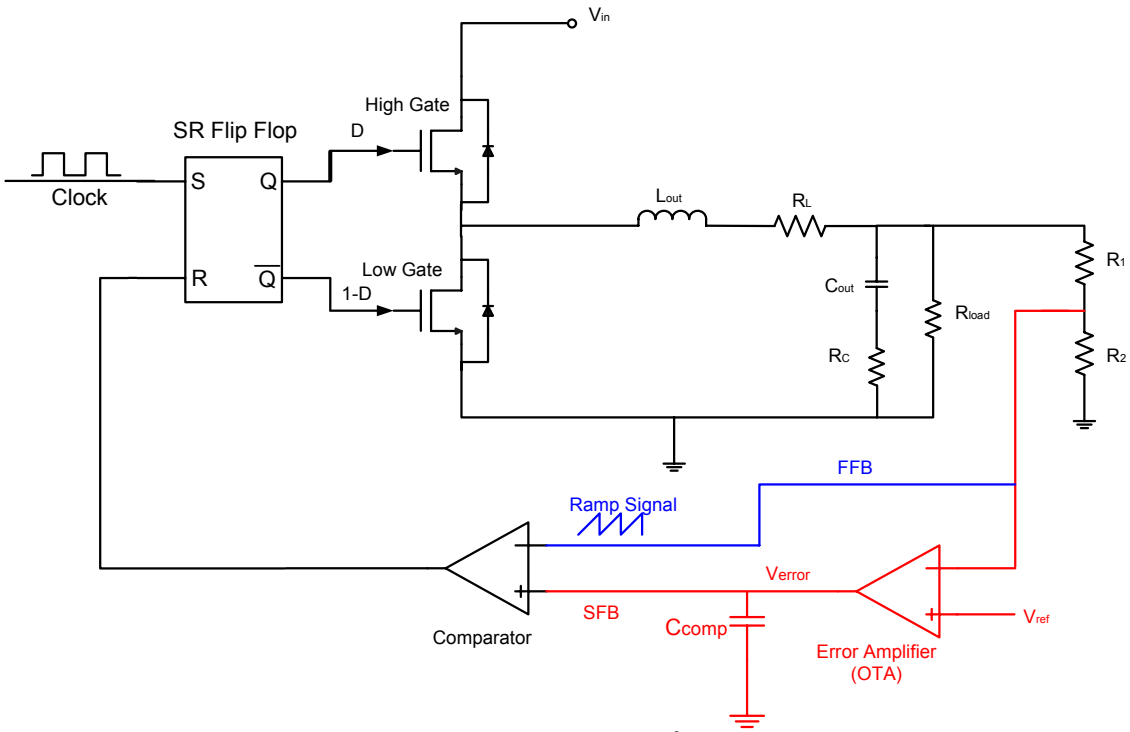

Figure 3.1: Block diagram of V^2 control scheme

In figure 3.1, high gate and low gate are power MOSFETs which act as switches. L_{out} and C_{out} are the output inductor and output capacitor forming the output LC filter or the buck converter. R_C is the ESR (equivalent series resistance) of the output capacitor, R_L is the equivalent series resistance of the inductor and R_{load} is the load resistance of the buck converter.

The feedback control modulates the D signal which in turn controls the ON-OFF action of the high side gate. A complementary action governs the ON-OFF timing of the low side gate, i.e. when the high side gate is ON the low side gate is OFF and vice versa. The negative feedback to the buck converter comprising of the error amplifier, comparator and the circuitry for the generation of signals D and 1-D (figure 3.1) modulates the duty cycle of the buck converter upon changes in the load and line conditions thus holding the output voltage in regulation.

As seen in figure 3.1 of the feedback stage the output voltage is fed to the error amplifier to be compared with a reference voltage, V_{ref}. The reference voltage is selected such that V_{ref} determines the desired value at the output voltage V_{out} during buck converter regulation. For an on-chip implementation of the error amplifier there is a limit to the maximum voltage at the input of the amplifier subject to its input common mode range (ICMR) limitations [13]. If the output of the buck converter falls outside of the ICMR of the error amplifier then a voltage divider network similar to the one shown in figure 3.1(implemented with resistors R1 and R2) must be used to step down the output voltage. The same argument applies to the choice of the reference voltage also. One must select a reference voltage that fall in the ICMR of the error amplifier. The equation governing the choice of the resistors R1 and R2 is

$$V_{ref} = V_{out} \frac{R2}{R1 + R2} \tag{3.1}$$

The error signal generated at the output of the error amplifier is fed to the comparator which then compares it with a ramp signal to modulate the duty cycle. The ramp signal in a V^2 control topology is derived from the output of the buck converter itself. The derived

ramp signal is due to the ESR of the output capacitor (figure 3.1). The ramp signal is equal to the product of the AC load current via the inductor and the ESR of the output capacitor R_C. The output of the buck converter is used to generate both the error signal and the ramp signal. The ramp voltage is the output voltage of the buck converter itself, any changes in the load causes an output change which shows up immediately at the input of the comparator as the ramp. Similarly any changes in the line conditions change the current through the inductor which in turn affects the ramp voltage and again shows up immediately at the input of the comparator. Hence, the V^2 control scheme inherently compensates for variations in load and line conditions. Time response delays to changes at the input and output are limited by V^2 feedback control.

There are two voltage feedback paths in V^2 control, namely FFB (Fast Feedback – Blue line in figure 3.1) path and SFB (Slow Feedback – Red line in figure 3.1) path. In the FFB path, the output of the buck converter connects directly to the input of the comparator carrying the ac ramp at the output of the buck converter as well as the dc voltage information. The SFB path connects the output of the buck converter to the input of an error amplifier whose output, the error voltage V_{error}, feeds the other input of the comparator. A change in load and line condition is fed back to the comparator directly through the FFB path which in turn modulates the duty cycle to proportionately vary the output voltage. As can be seen from figure 3.1, the transient response time is determined by the feedback elements in the FFB path and hence is determined by the speed of the comparator and the delay through the SR flip flop, pad driver, and switching FETs. The error amplifier is used to set the DC accuracy of the feedback loop.

3.2 Compensation

The output of the error amplifier presents a pole in the feedback system that needs to be compensated by placing a zero at one-tenth the pole frequency. Section 2.3.0 explained the implementation of a Type II compensation network scheme for voltage mode control. The compensation network for a V^2 control topology is achieved by simply placing a compensation capacitor C_{comp} at the output of the transconductance error amplifier [3]. The arrangement can be seen in figure 3.1. The combination of the SFB path and the FFB path along with a compensation capacitor C_{comp} produces a zero frequency in the feedback path whose position must be designed to compensate for the output pole of the error amplifier. The analysis leading to the expressions for the pole and zero frequency in the feedback path is given in [3]. In the derivation for the expressions of pole and the zero frequency, the error amplifier is an Operational Transconductance Amplifier (OTA) with transconductance g_m and output impendence r_{out}. The analysis shows that the pole and zero frequency are

$$f_{pole-ota} = \frac{1}{2\pi \times r_{out} \times C_{comp}} \tag{3.2}$$

$$f_{zero} = \frac{g_m}{2\pi C_{comp}} \tag{3.3}$$

The zero frequency generated due to the feedback loop is position at one-tenth the pole frequency i.e.

$$f_{zero} = 0.1 f_{pole-ota} \tag{3.4}$$

The frequency response of the feedback loop after the addition of the compensation capacitor is discussed next. In the analysis of the feedback loop [3], the

error amplifier is a single-pole OTA (Operational Transconductance Amplifier) whose transfer function is given as

$$A_v(s) = \frac{A_{vol}}{1 + \frac{s}{\omega_{pole-ota}}} \tag{3.5}$$

where A_{vol} = open loop gain of the error amplifier = $g_m \times r_{out}$ (3.6)

and $\omega_{pole-ota} = 2\pi \times f_{pole-ota}$ (3.7)

Hence, the frequency response of the feedback loop is given as

$$H(s) = A_v(s) = \frac{A_{vol}}{1 + \frac{s}{\omega_{pole-ota}}} \tag{3.8}$$

So in the absence of the compensation capacitor the feedback frequency response is that of a single pole OTA as shown in figure 3.2.

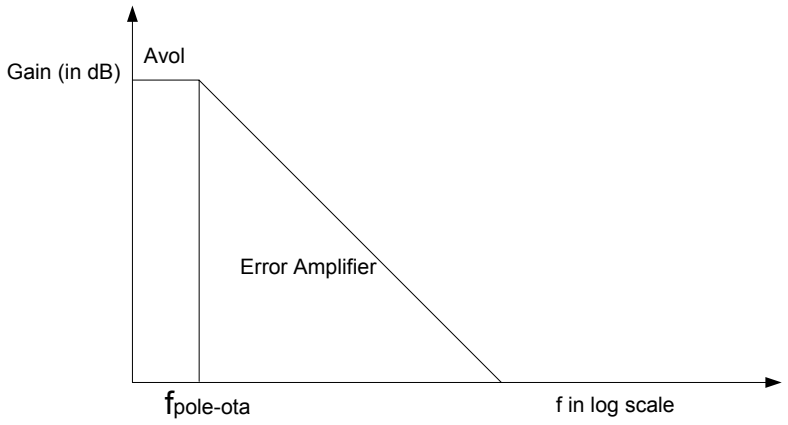

Figure 3.2: Frequency response of feedback loop H(s).

After the introduction of the compensation capacitor C_{comp}, the frequency response of the feedback loop is given by ([3], [8]),

$$H(s) = FM(1 + A(s))$$
$$= FM\left(\frac{1 + \frac{s}{\omega_{zero}}}{1 + \frac{s}{\omega_{pole-ota}}}\right) \tag{3.9}$$

where, FM = gain in the feedback loop

$$= \frac{2 \times L_{out}}{(V_{in} - V_{out}) \times R_C \times T_{sw}}$$

$$\omega_{zero} = 2\pi \times f_{zero} \tag{3.10}$$

and $$\omega_{pole-ota} = 2\pi \times f_{pole-ota} \tag{3.11}$$

The frequency response of the feedback loop in the presence of the compensation capacitor is shown in figure 3.3.

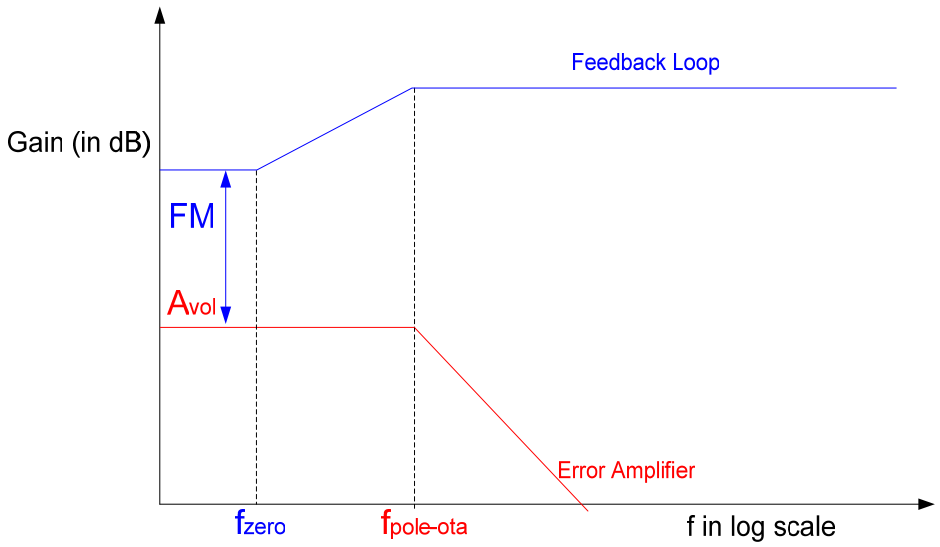

Figure 3.3: Frequency response of feedback loop (blue) H(s) after the introduction of C_{comp}.

The blue curve shows the frequency response after the introduction of C_{comp} while the red curve shows the frequency response before C_{comp} was present. The double pole frequency

due to the LC combination at the output of the buck converter is compensated by placing the zero frequency due to the output capacitor and its associated ESR at 2-5 times the double pole frequency. This was discussed in section 2.1. The frequency response of the DC-DC system before and after compensation is shown in figures 3.4 and 3.5 respectively.

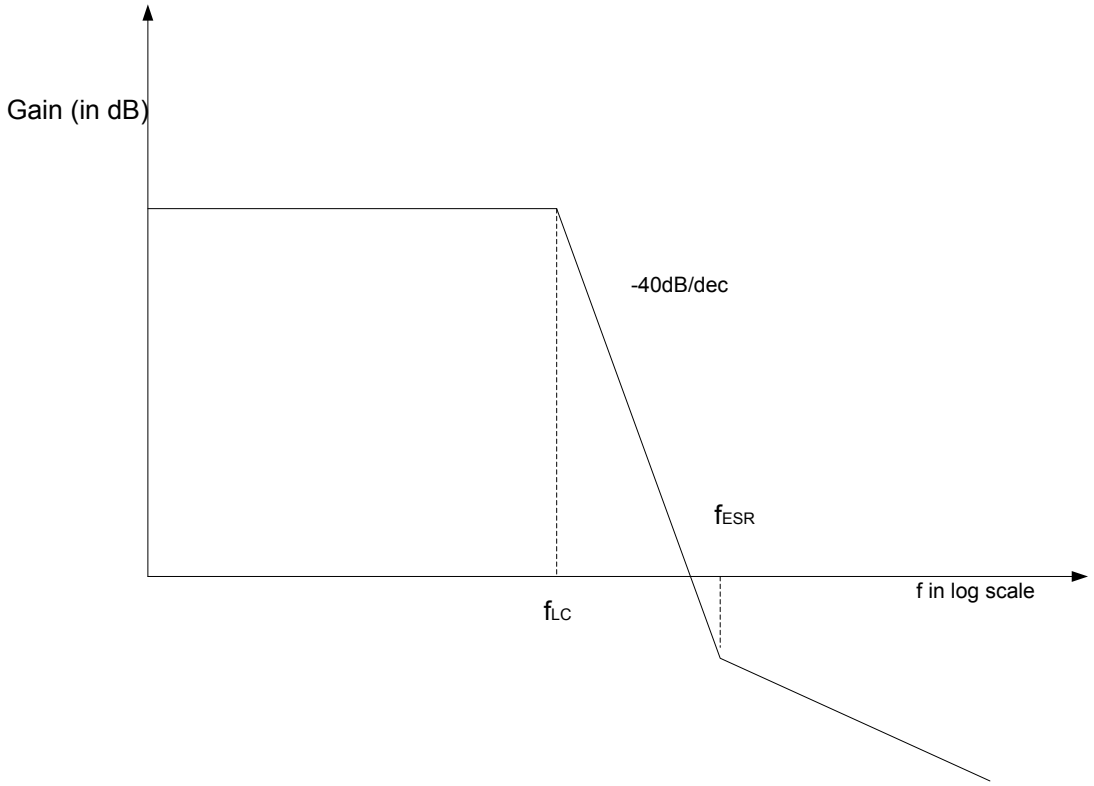

Figure 3.4: Frequency response of uncompensated DC-DC system Gd(s).

As can be seen from figure 3.4, the uncompensated DC-DC system starts rolling at -40dB/dec from the double pole frequency f_{LC} and hence at the unity gain frequency there might not be enough phase margin to guarantee oscillation free operation. In contrast, in figure 3.5, the error amplifier pole frequency is compensated by the zero from the feedback compensation network and hence the error amplifier output pole does not degrade the frequency response and the double pole frequency is compensated by placing

the zero frequency from the buck converter at approximately 2-5 times the double pole frequency so that the frequency response of the closed loop system rolls off at approximately -20dB/dec. This ensures that at unity gain frequency of the closed loop system there is sufficient phase margin to allow oscillation free operation.

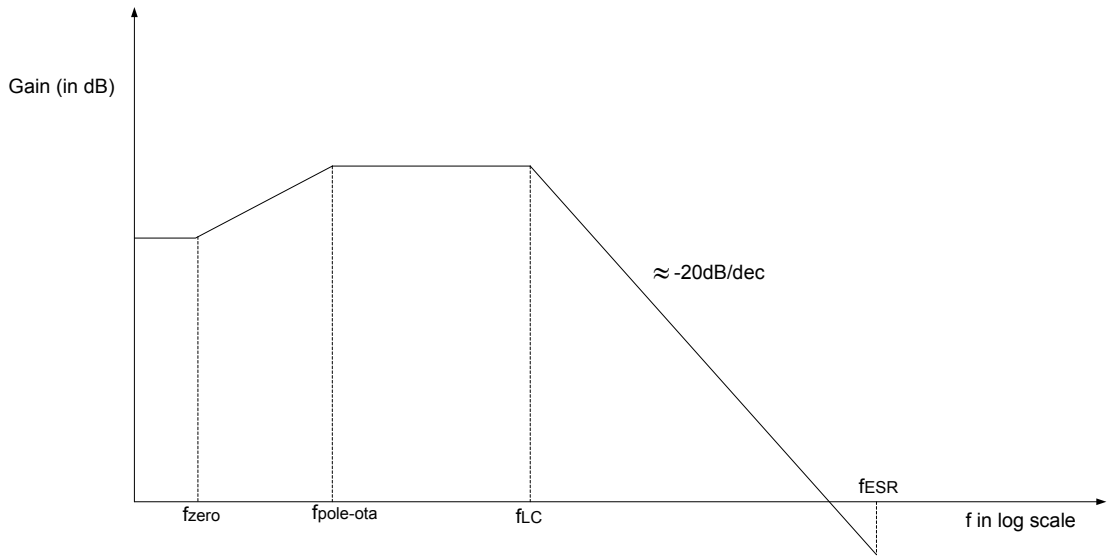

Figure 3.5: Frequency response of DC-DC system with compensation.

The considerations for closed loop system stability are summarized as below:

1. The double pole frequency f_{LC} must be compensated by designing the output zero from the buck converter to be at 2-5 times the double pole frequency, i.e.

$$\frac{f_{ESR}}{f_{LC}} \approx 2-5 \tag{3.12}$$

2. The error amplifier output pole is compensated by designing the zero frequency from the FFB path and SFB path at or less than one-tenths the error amplifier pole frequency. This condition is given by equation 3.4.

3.3 Design Strategy

Figure 3.6 shows the design flow algorithm for DC-DC converter design.

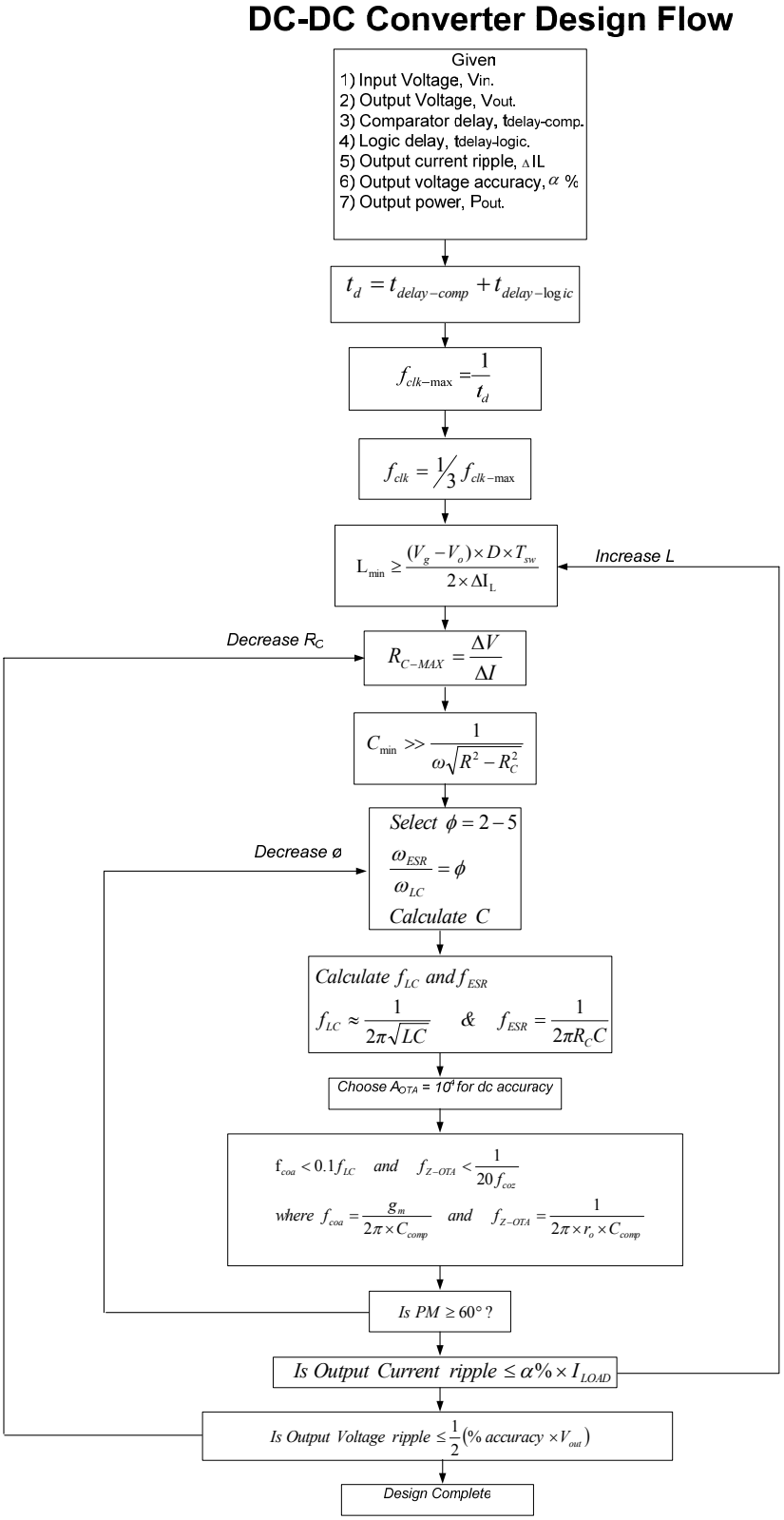

Figure 3.6 DC-DC converter design flow algorithm.

The design of any DC-DC converter system starts with a set of input specifications while the design elements are chosen to meet these requirements. A design flow diagram helps in this process. One can feed in the input specifications and follow the algorithm to generate the practical design variables resulting in a useful design.

During the study of a step-down DC-DC system employing V^2 control architecture a design flow diagram (figure 3.6) was formulated that gives an estimate of the design variables in the form of the values for the; inductor, capacitor, its associated ESR and the like. These values can be fed into the DC-DC system model that was developed in SPICE (chapter 4) and tweaked in simulation to arrive at the exact values that satisfy all the design requirements given in the input specification. The design flow algorithm will be explained next.

The first step in the design process is to acquire all the input specifications for the design in the form of (i) Input voltage, Vin, (ii) Output voltage, Vout, (iii) Output current ripple requirement ΔI_L, (iv) Output voltage accuracy, α, (v) Output power, Pout, (vi) delay through the comparator, $t_{delay\text{-}comp}$, (vii) SR flip flop delay (logic delay in figure 3.6), $t_{delay\text{-}logic}$. The input voltage and the output voltage it has to stepped down to give us the duty cycle of the buck converter in regulation. Duty cycle, D can be calculated using equation 2.10 (rewritten here in a different form so that it directly gives D).

$$D = \frac{V_{out}}{V_{in}}$$

The current that flows in the load of the buck converter when the output is in regulation i.e. Vout is given by,

$$I_{out} = \frac{P_{out}}{V_{out}} \tag{3.13}$$

The next step is to calculate the maximum delay through the feedback system. Since in V^2 control the feedback signal flows through the comparator and the logic circuitry (SR flip flop) the delay is limited by the delay through the comparator and the speed of the digital logic. Hence, the delay is given by

$$t_d = t_{delay-comp} + t_{delay-\log ic} \tag{3.14}$$

Note that since this is a high-temperature design and the delay of both the comparator and SR flip flop increase with temperature, the delay calculation in equation 3.14 has to be computed for the worst case i.e. for the highest temperature of operation (at 200°C in this thesis). This is done since the choice of the maximum clock frequency at which the closed loop DC-DC system can operate is limited by the delay via the feedback system. The next step is to calculate the maximum clock frequency at which the system can work. This is given by

$$f_{clk-\max} = \frac{1}{2t_d} \tag{3.15}$$

If the clock frequency is more than that given by equation 3.15 then the feedback system will not be able to respond to variations in the output voltage in one clock cycle.

Select a clock frequency of approximately one-third the maximum clock frequency given in equation 3.15. Hence

$$f_{clk} = 1/3\, f_{clk-\max} \tag{3.16}$$

The ac current ripple through the inductor is given by ([7])

$$\Delta \mathrm{I_L} = \frac{(V_{in} - V_{out}) \times D \times T_{sw}}{2 \times \mathrm{L_{out}}} \tag{3.17}$$

where, $\mathrm{T_{sw}}$ = switching period = $\dfrac{1}{f_{clk}}$

The input specifications specify a minimum value on the current ripple at the output. This places a lower bound the value of the output inductor. Rearranging equation 3.17 gives the minimum value of the output inductor, $\mathrm{L_{min}}$ as

$$\mathrm{L_{min}} = \frac{(V_{in} - V_{out}) \times D \times T_{sw}}{2 \times \Delta \mathrm{I_L}} \tag{3.18}$$

Select this minimum value of $\mathrm{L_{min}}$ as the starting value for the output inductance, $\mathrm{L_{out}}$.

The next step is to calculate the maximum ESR that the output capacitors can have. The output voltage ripple is due to the ac current ripple via the inductor being dropped across the ESR of the output capacitor. The maximum ESR is then determined by the input specifications on the output voltage and current ripple requirements, i.e.

$$R_{C-MAX} = \frac{\Delta V}{\Delta I_L} \tag{3.19}$$

It is recommended that the ESR value be selected as one-fifth the value given by equation 3.19 so that variations in the ESR due to tolerance and temperature variations to avoid violating the maximum current and voltage requirements of the design.

The output of the buck converter is the parallel combination of the output capacitor with its ESR and the load impedance (figure 3.1). With regard to the output voltage and currents during regulation the output network must be resistive [8]. This condition determines the minimum value of the output capacitor given as

$$C_{\min} >> \frac{1}{\omega\sqrt{R^2 - R_C^2}} \tag{3.20}$$

where ω is the operating frequency in radians/sec.

As presented in section 3.2, to compensate the double pole frequency of the buck converter the ESR zero frequency is placed at 2-5 times the double pole frequency, i.e.

$$\begin{aligned} &\frac{\omega_{ESR}}{\omega_{LC}} = \phi \approx 2-5 \\ \Rightarrow\ &\frac{1}{R_C}\sqrt{\frac{L_{out}}{C_{out}}} = \phi \\ \Rightarrow\ &C_{out} = \frac{L_{out}}{(\phi \times R_C)^2} \end{aligned} \tag{3.21}$$

Equation 3.21 gives the value of the output capacitance for which the closed loop system is stable. As a first estimate select Φ as 5. The selected values of C_{out} and L_{out} are used as inputs to the model for the DC-DC converter system (chapter 4). During simulations care should be taken check for oscillations at the output of the buck converter as the input voltage V_{in} is ramped up to its final value.

The next step is to select the open loop gain of the error amplifier. The gain of the error amplifier provides DC accuracy in the feedback loop [3] and as a result the higher the gain greater the DC accuracy in the feedback. From equation 3.6 the open loop gain of the error amplifier contains the transconductance term and the output impedance term of the error amplifier. Since, g_m and r_{out} figure in equation 3.4 which governs the compensation condition in the feedback network, the gain of the error amplifier must be chosen such that the choice of g_m and r_{out} does not violate equation 3.4. Select an open loop gain of approximately 1000 times the reciprocal of the percent error, e.g.10^4 and calculate C_{comp}, g_m and r_{out} such that equations 3.4 and 3.6 are satisfied. At this point all the design variables have been computed and need to be tested in the SPICE model for DC-DC converter system to confirm or fine tune the results until all design requirements have been met.

There are three critical design requirements that must be satisfied for the successful completion of the design. They are (i) phase margin of at least 60°, (ii) output voltage accuracy (as given in the input specifications) and (iii) output current ripple requirement (as given in the input specifications). If the criterion (i) is not met i.e. the closed loop does not have a phase margin of at least 60° then there will be oscillations at the output of the buck converter. To increase the phase margin decrease the value of Φ (figure 3.6) and then one must go through the remainder of the steps as explained above. This is shown in the design flow graph of figure 3.6. Similarly, if either (ii) and/or (iii) are not met then one again follows the design flow graph to decrease the output voltage accuracy or output current ripple by decreasing the value of R_C or by increasing the value

of the output inductance respectively. This is accomplished by making the adjustments by going through the design flow graph repeatedly as required until all the design requirements are met. In this fashion all the circuit design paramaters can be generated from the algorithm in figure 3.6.

3.4 Temperature Issues

The issues related to the design of mixed signal integrated circuits (ICs) with variation in temperature are discussed in this section. At elevated temperatures the performance of integrated circuits in bulk CMOS (Complementary Metal Oxide Semiconductor) process is limited by latch-up and leakage currents [14]. In a SOS (Silicon On Sapphire) process, the substrate is dielectrically isolated from the NMOS (n-channel MOS) and PMOS (p-channel MOS) devices which allows full DC isolation of the PMOS and NMOS devices thus eliminating latch-up. The error amplifier and comparator in the feedback loop of the V^2 control discussed in section 3.1 are to be implemented on-chip using an SOS process. Hence before a discussion of the error amplifier and comparator is undertaken an introduction to the issues involved in high temperature CMOS IC design is in order.

The various effects on the characteristics of a MOSFET (Metal Oxide Semiconductor Field Effect Transistor) have been discussed in detail in [14]. A summary of these effects is presented here. They are

1) The absolute value of the threshold for both PMOS and NMOS devices decreases with increase in temperature. This leads to an increase in the overdrive voltage ΔV. This increase in the overdrive voltage leads to a decrease in the self gain of the devices.
2) Leakage current increases with increase in temperature which results in degradation of the transconductance of the devices.
3) Mobility of both PMOS and NMOS devices decreases with increase in temperature leading to a decrease in their drain currents.

The two important elements in the V^2 feedback topology are the error amplifier and the Pulse Width Modulated (PWM) comparator. The error amplifier and the comparator have a minimum open loop gain and GBP (Gain Bandwidth Product) requirement that they must satisfy at both maximum temperature and maximum load in order for the feedback loop to function properly. The performance metrics from the error amplifier and the comparator will be discussed in the next section. The gain and bandwidth requirements have to be met for the entire range of temperature operation. For this it is important to understand and analyze the effects of temperature variation on the gain and bandwidth of the comparator and the error amplifier. A detailed study of the variations in overdrive voltage, transconductance g_m and the mobility for a constant current design in an SOS process has been conducted in [15]. The plot in figure 3.7 shows the variation in the overdrive voltage ΔV, the transconductance g_m and the mobility for a constant current design. It can be observed from the figure that the overdrive voltage increases with rise in

temperature – increasing by almost 25% from room temperature to 200°C. The mobility reduces by almost 30% from room temperature to 200°C.

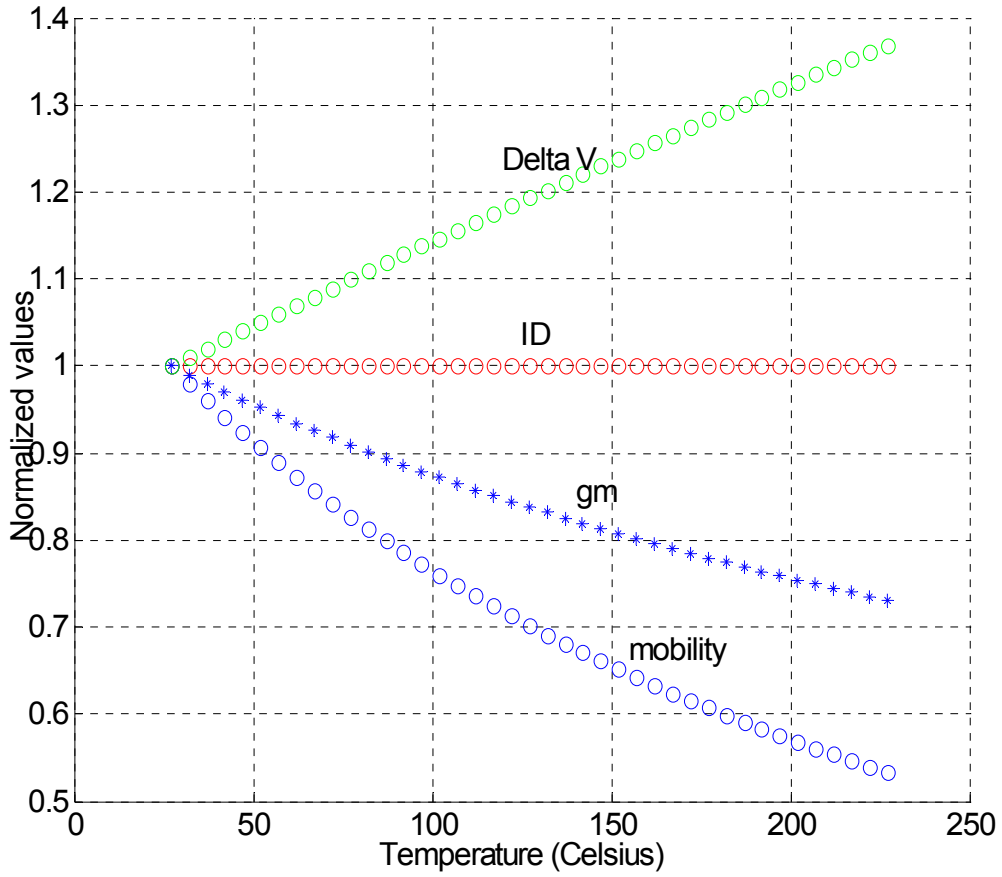

Figure 3.7: Variation of ΔV (overdrive voltage), g_m (transconductance), and mobility with temperature for constant current design.

In this thesis, the approach is to design the comparator and the error amplifier OTA (Operational Transconductance Amplifier) as a constant g_m design circuits. The reason in choosing a constant g_m design is that the bandwidth of both the OTA and the comparator is given by [14],

$$BW = \frac{g_m}{2\pi \times C_{LOAD}} \tag{3.22}$$

where C_{LOAD} equals load capacitance at the output of the error amplifier or the comparator.

In the case of the error amplifier, the load capacitance is the compensation capacitor C_{comp} (figure 3.1) and in the case of the PWM comparator the load capacitance is the input capacitance of the SR flip-flop.

Since, the load capacitance in this particular design does not change significantly with variation in temperature a constant g_m design insures a constant bandwidth with variations in temperature. Now we are left with only one remaining issue i.e. the open loop gain of the comparator and the OTA. The design of the error amplifier and the comparator as an integrated circuit will be discussed in chapter 4. The variation in their performance with temperature will be highlighted along with possible circuit implementations are shown in chapter 4.

Chapter 4

V^2 Model in SPICE

4.0 Introduction

In order to prove the feasibility of the V^2 control topology, a SPICE model of the controller architecture as applicable to a step-down buck converter has been developed. The developed model is shown to follow all the design equations presented in Chapter 3 with regard to the operation of the buck converter and the V^2 control topology. The developed SPICE model of the buck converter employing V^2 control architecture is explained in this chapter. This is followed by the simulation results of a design example using the developed model proving the feasibility of the V^2 control architecture as applied to a buck converter to perform step-down voltage conversion. The simulation results are also used to determine the performance requirements for the individual building blocks in the feedback design, namely the error amplifier, switch drivers and the comparator with hysterisis. The simulation results include the variation in component values (capacitors, inductors and transconductance of the error amplifier) anticipated with temperature and time proving that the developed model of the step-down converter works for the expected range of temperatures.

The block diagram of the model is shown in figure 4.1 [15]. The developed model incorporates soft-start implementation, UVLO (Under Voltage Lock Out) implementation, Over-Current protection and 100% Duty Cycle (DC) comparator. Each of these features is explained in detail in the next few sections in this chapter. In figure 4.1 the buck converter is not shown because the buck converter with its feedback loop does not fit well in one figure (Figure 4.1). The buffers labeled Gate(H) and Gate (L) drive the inputs of the high side MOSFET M1 and the low side MOSFET M2(from figure 3.1) respectively. The buck converter lies on the right hand side of the diagram in figure 4.1. The block diagram shown in figure 4.1 is solely the feedback network that senses variations at the output of the buck converter and responds to these changes by modulating the duty cycle.

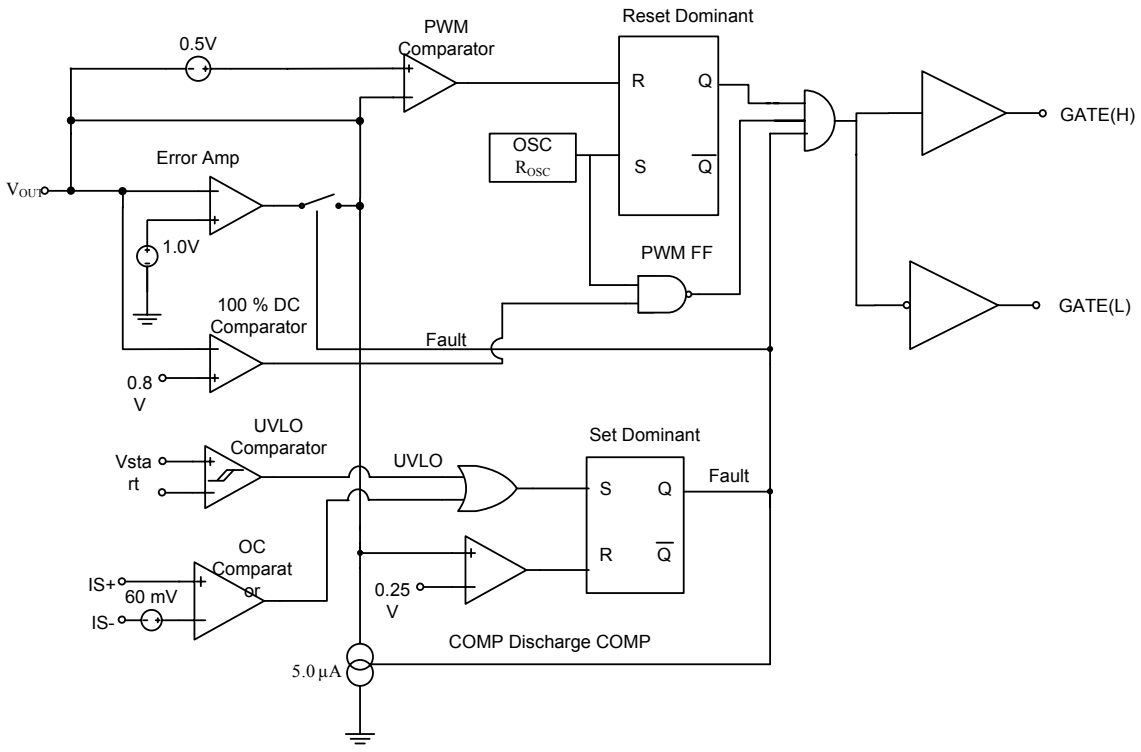

Figure 4.1: The developed V^2 control topology

The working of the V^2 control architecture was explained in section 3.1. The working of the V^2 topology is explained here again in brief, as pertaining to figure 4.1. This is done so that the working of the Soft Start, UVLO, OC protection and 100% duty cycle comparator can be built upon the basic V^2 controller loop.

Normally, GATE(H) transitions to a high voltage at the beginning of each oscillator cycle [16] thus turning ON the upper power MOSFET. Inductor current ramps up until the combination of the current sense signal, the internal ramp and the output voltage ripple trip the PWM comparator and bring GATE(H) low. Once GATE(H) goes low it will remain low until the beginning of the next clock cycle. While GATE(H) is high, the V^2 feedback loop will respond to line and load variations increasing the output voltage until it exceeds the set point. On the other hand, once GATE(H) is low, in earlier classical control techniques the feedback loop could not respond to any variations in the output voltage until the beginning of the next clock cycle. GATE(H) and GATE(L) must have enough current drive strength to be able to drive the input capacitance of the power MOSFETs (high side switch and low side switch). The MOSFET drivers must have enough current drive capability so that the rise time at the MOSFETs does not occupy a substantial amount of the input clock pulse width. Usually a rise time of around 1% of the clock pulse width is chosen so that the ON and OFF times of the buck converter and hence the output accuracy is not drastically effected. Hence the current drive capability from GATE(H) and GATE(L) must be

$$I_{drive} = C_{ISS} \frac{V_{in}}{1/100 \times t_{clk}} = C_{ISS} \frac{V_{in} \times f_{clk}}{1/100} \tag{4.1}$$

where $C_{ISS} = C_{GD} + C_{GS}$ of the power MOSFET.

However, in V^2 control architecture the feedback loop will respond to disturbances within the off-time of the converter via the fast feedback path thus providing more accurate regulation in the output voltage. The output voltage of the buck converter is subtracted from a reference voltage in an error amplifier. The error signal thus generated is then given to the negative input terminal of a PWM (Pulse Width Modulator). The PWM comparator compares the error signal from the error amplifier with a ramp signal derived from the output of the buck converter and generates a reset pulse to modulate the duty cycle of the buck converter and hence keep the output voltage in regulation. The reset pulse generated turns OFF the high side gate GATE(H) turning OFF MOSFET M1 and simultaneously turns ON the low side gate GATE(L) resulting the MOSFET M2 being turned ON. The functionality of the feedback loop described above is only valid when the system does not generate any fault conditions. There are two conditions that can lead to the generation of a fault signal,

i). If the input to the buck converter V_{in} is below the minimum input value of V_{start} which leads to an under-voltage lockout of the feedback system. In such a state, the feedback loop is disabled until V_{in} reaches the preassigned valued of V_{start}. (The value of V_{start} is to assigned from careful simulations of the converter block with its feedback circuitry as the value of the input voltage below which the system is not able to regulate the output voltage within the given output voltage accuracy requirements. This value of V_{start} is generally around 75-90% of V_{in}.)

ii). When there is a sudden inrush of current into the buck converter. This condition is encountered when the buck converter is powered up and any time the output voltage ramps up to its desired value. During this period there maybe a sudden inrush of current through the inductor that has the potential to damage the output inductor by saturating it and also holds the potential to damage the output capacitor. This condition is prevented by incorporating an over-current protection mechanism. The working and implementation of an over-current mechanism is explained in section 4.3 in detail.

As soon as a fault signal is generated, the feedback loop is broken by disconnecting the connection between the output of the error amplifier and the PWM comparator input. This is done by means of a switch between the output of the error amplifier and the input of the PWM comparator. The opening and closing of the switch is controlled by the fault signal. When the fault signal is high the switch is open and closed otherwise. When the fault signal is high the feedback loop is broken by opening the switch. Hence, the feedback loop no longer modulates the duty cycle of the buck converter as long as the fault signal is high. The feedback loop stays in this state until the fault latch is cleared and then the output of the error amplifier is again reconnected to one of the inputs of the PWM comparator thus resuming normal operation of the V^2 feedback loop.

The fault signal is generated by a set-dominant SR flip flop. The S input of the SR flip-flop is the OR function of two signals – the "Under-Voltage Lockout" (UVLO)

condition and the "Over-Current" (OC) condition (figure 4.1). The fault latch is cleared when the output of the error amplifier (capacitor, C_{comp}) is discharged by a small current, e.g. 5 μA current sink to a predetermined voltage, typically 0.25*V_{ref}. When the output of the error amplifier falls below this predetermined voltage (shown as 0.25V in figure 4.1), the reset signal goes high and the fault latch is cleared which leads to the feedback loop again resuming its normal operation. In the next few sections the working and implementation in SPICE of the individual components in the model of figure 4.1 are explained. The individual components implementing; the set dominant and reset dominant SR flip-flops, Soft Start, Under-Voltage Lockout (UVLO), Over-Current (OC) protection, and 100% Duty Cycle (DC) comparison circuits are presented in detail.

4.1 Reset Dominant SR Flip-Flop

In general, a set-reset latch (SR) is used for the pulse width generator in Fig. 4.1. However, when both S and R are high, both Q and $\overline{Q}$ are forced to zero. This does not correspond to the constraint that Q and $\overline{Q}$ must be complementary, and so this input mode is must be forbidden. When both S and R inputs are high, the reset signal must take precedence and thus force the Q output low. In the steady-state operation of the V^2 mode feedback loop, both inputs may be high simultaneously leading to incorrect functionality of the feedback loop. However, during the startup, the output of the buck converter will be lower than the reference voltage and hence the output of the comparator will be a high. R is therefore always high during the startup. In a normal SR flip flop this leads to both Q and $\overline{Q}$ being forced to a low. To avoid such a condition a set dominant SR flip flop has

to be designed which forces the output Q to a high and the output $\overline{Q}$ to a low, one implementations of a set dominant SR flip flop is shown in Fig. 4.2. The addition of AND and NAND logic ensures that both inputs of SR latch are not high simultaneously. When both inputs (and clock signal) are high, the latch is set. Thus, the outputs are complementary for all cases even when both inputs are high.

A reset dominant SR flip flop behaves similarly to a normal SR flip flop for 00, 01 and 10 input combinations. The implementation is different than a normal SR flip flop in that it evaluates the forbidden 11 input combination to a logic low at the Q output. The name reset dominant SR flip flop comes from the observation that when both the S and the R inputs are a high the reset pulse takes precedence and the output Q is evaluated to a logic low.

The schematic for the set dominant and reset dominant SR flip flops are shown in the figures below (figures 4.2 and 4.3 respectively).

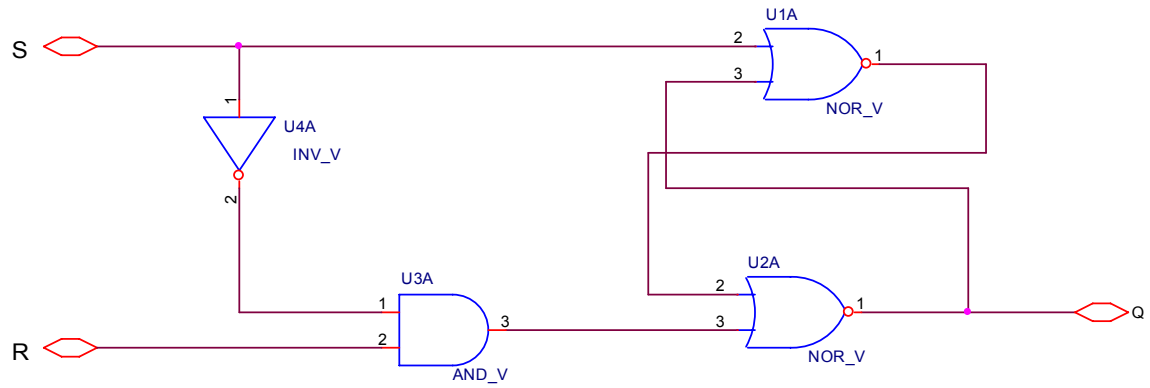

Figure 4.2: Set dominant SR flip flop.

The truth table for a set dominant SR flip flop is given in Table 4.1 below.

S	R	Q_n
0	0	Q_{n-1}
0	1	0
1	0	1
1	1	1

Table 4.1: Truth table of a set dominant SR flip flop.

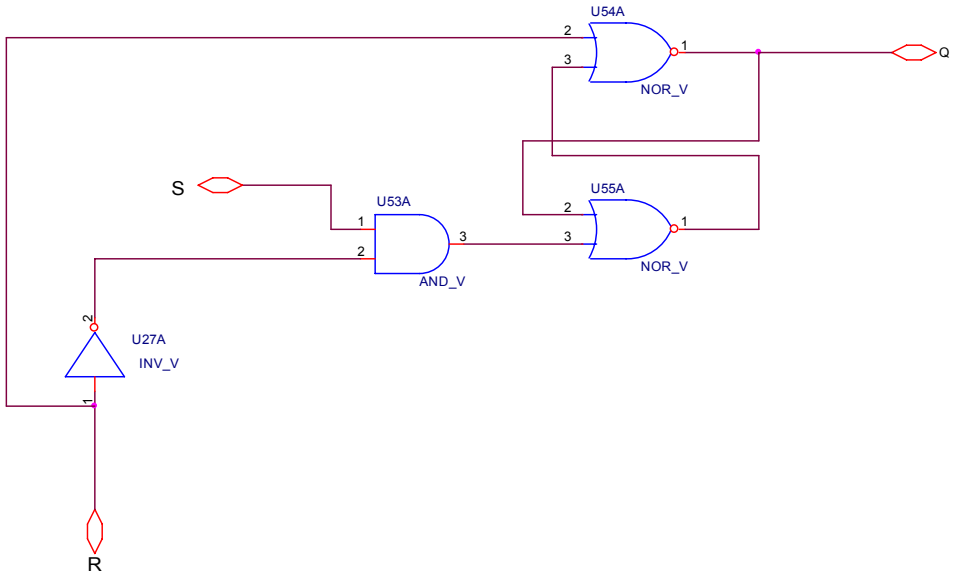

Figure 4.3: Reset dominant SR flip flop.

The truth table for a reset dominant SR flip flop is given in Table 4.2 below.

S	R	Q_n
0	0	Q_{n-1}
0	1	0
1	0	1
1	1	0

Table 4.2: Truth table of a reset dominant SR flip flop.

The schematic of a reset dominant SR flip flop using the cell library developed at MSVLSI lab is as shown in figure 4.4.

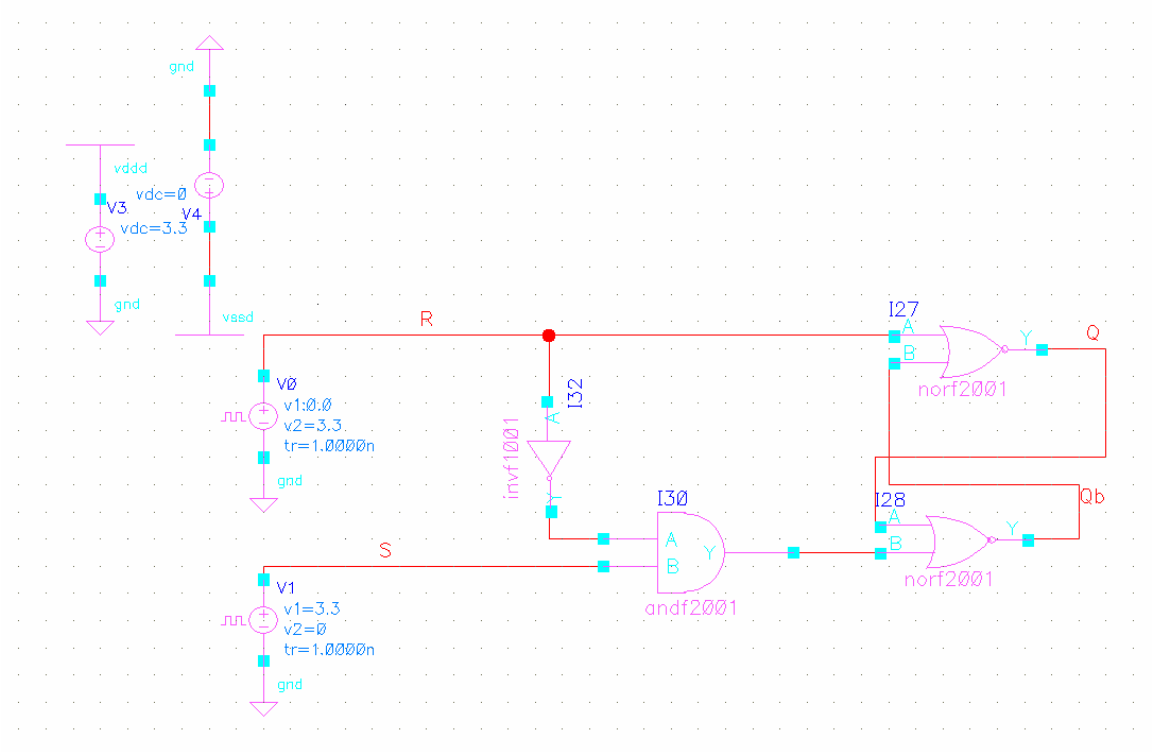

Figure 4.4: Reset Dominant SR Flip Flop

The delay through the individual elements of the flip flop is shown in Table 4.3.

Intrinsic Delay		
Gate	Rise Intrinsic (nsec)	Fall Intrinsic (nsec)
Inverter	0.448 ± 0.028	0.448 ± 0.029
2-Input NAND	0.660 ± 0.170	0.512 ± 0.060
2-Input NOR	0.655 ± 0.030	1.145 ± 0.118
Transition Delay		
Gate	Rise Intrinsic (nsec)	Fall Intrinsic (nsec)
Inverter	0.330 ± 0.017	0.350 ± 0.025
2-Input NAND	0.320 ± 0.120	0.255 ± 0.024
2-Input NOR	0.281 ± 0.010	0.352 ± 0.039

Table 4.3: Intrinsic and Transition delays of an inverter and 2-input NAND and NOR gates.

4.2 Soft Start

Soft-start is a feature commonly used in pulse width modulated (PWM) control circuitry to avoid converter output voltage overshoot and large transistor current spikes [17]. By controlling the voltage applied to the output of the error amplifier, V_{error}, the output duty-cycle increases from zero to its steady- state operating value very "softly". Due to its importance to the starting transient, soft-start has become a basic or required function of modern power supply circuits.

During power up, the buck converter tends to quickly charge the output capacitors to reach the desired output voltage. This gives rise to the potential for an excessive in-rush current which can be harmful to the inductor at the output of the buck converter. When the input voltage is initially applied, the full input voltage is applied across the inductor since one end of the inductor is the output of the buck converter which is initially at zero potential. If the higher side gate is allowed to be ON for the duration of D times the pulse width of the clock this causes large transient currents to flow into the inductor each clock cycle and the value of these transients might be greater than the saturation current rating for the output inductor. This is harmful because as the inductor saturation current is exceeded and the value of the inductance drops which in turn causes the peak to peak value of the inductor current ripple to increase. The inductor ripple current when dropped across the ESR of the output capacitor causes the output voltage ripple or ac current ripple during start-up to exceed the maximum allowable ac current rating resulting in excessive heating and damage to the load capacitor. Hence, the duty

cycle of the buck converter is regulated to very small values during start-up so that the value of this inductor current is reduced avoiding potential damage to the C_L and MOS switches M1 and M2. With every clock cycle the duty cycle is increased till it reaches the designed duty cycle of the buck converter at which point the feedback loop is enabled and then the feedback system modulates the duty cycle depending upon the transients at the buck converter output. The soft-start operation timing (not to scale) is illustrated in Fig 4.5. In the figure, V_{error} is the output voltage of the error- amplifier, and V_{in}, is the input voltage. Duty-cycle, D is the output signal of the buck converter and determines the turn-on ratio of the main switch. As can be seen from figure 4.5, the duty cycle during the start-up period is very low which reduces the stress on the discrete component in the buck converter from a sudden inrush of current during start-up. Maximum peak inrush current can be written as

$$I_{peak} = (V_{in-\max} - V_{error})\frac{D}{f_{clk} \times L_{out}} = (V_{in-\max} - V_{error})\frac{t_{ss}}{L_{out}} \approx (V_{in-\max})\frac{t_{ss}}{L_{out}} \qquad (4.2a)$$

where I_{peak} is the lesser of the peak currents associated with the switches (M1 and M2), the inductor saturation current and the load current C_L.

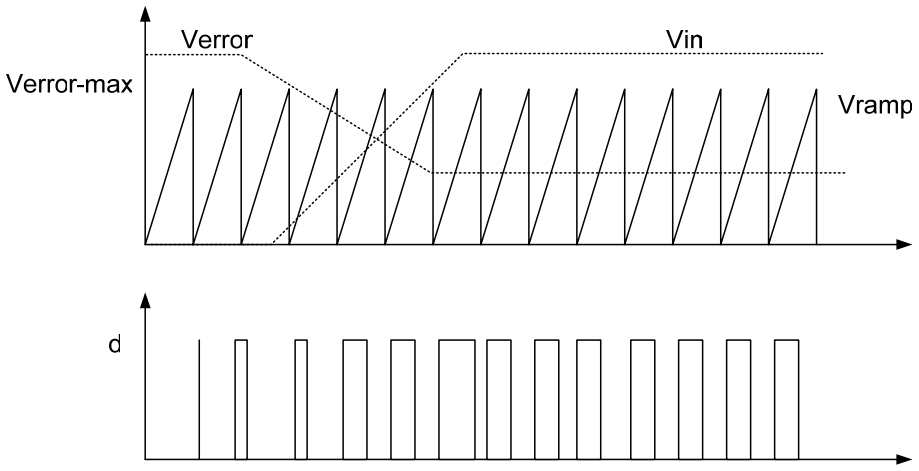

Figure 4.5: Timing diagram during start-up

Since, the buck converter is basically a LC low pass filter when the input is applied to the buck converter, the output voltage over-shoots and the amount by which the output overshoots must be regulated because the DC-DC system has an output voltage accuracy requirement. By allotting more time for start-up the output capacitor ramps up to its final value in a smoother fashion without any over-shoot. The amount of over-shoot is determined by the Q factor of an LC filter [7]. To determine the required soft-start duration, the DC-DC system must be given a ramp input voltage V_{in} and the output voltage must be observed for various start-up times. The calculation of the soft-start time is explained in the next paragraph.

In V^2 control, the compensation capacitor provides Soft-Start with no need for additional circuitry. During power up, the tail current of the error OTA amplifier charges the compensation capacitor which forces the output voltage to ramp up gradually. The output capacitor of the error amplifier combined with the tail OTA current controls soft start slope. When a fault is detected due to an over-current condition the converter will enter a low duty cycle mode. During this mode the converter will not switch from the time a fault is detected until the "Soft Start" capacitor has discharged below the Soft Start discharge threshold. The Soft Start will disable the converter when pulled below the maximum Soft Start discharge threshold.

The Soft-Start duration can be calculated as

$$t_{ss} = \frac{V_{in} \times C_{comp}}{I_{error}} \tag{4.2b}$$

where, V_{in} is the steady-state voltage, which is approximately equal to error amplifier's reference voltage.

C_{comp} is the compensation capacitor connected to the output of the error amplifier,

I_{error}, is the tail current of the OTA error amplifier.

Since V_{in} is given as an input specification and C_{comp} is determined by the compensation requirements of the feedback loop as was described in the design algorithm in chapter 3 the only variable to available to change the t_{ss} is I_{error}. I_{error} is determined from equation 4.2b depending upon the required soft-start current constraint. Since I_{error} is derived from the tail current source of the OTA which functions as an error amplifier, I_{error} must be designed so that the criterion in equation 4.2b is met even for the lowest value of the tail current source for the entire range of operation and inductor saturation current. For a chosen design topology of the error amplifier the variation of the tail current source with temperature must be taken into account and equation 4.1b must be satisfied for the worst case i.e. when the tail current source is the lowest.

In the absence of a soft-start mechanism, there is a sudden inrush of current via the inductor which has the detrimental effect of possibly saturating the inductor or exceeding the current rating of the power MOSFET thus destroying the device or causing the output of the buck converter to overshoot. The output capacitors chosen must have a current rating higher than the current spikes that occur at start-up. If more current flows into the output capacitance than its maximum rated current this causes the values of the output capacitance to change and hence causes the position of the double pole frequency

and the zero frequency to change causing a change in the frequency profile (the position of the double pole frequency and the zero frequency and hence the phase shift in the open loop system) to change which is undesirable. Hence, the output capacitor must be selected to be able to sustain these current spikes during start-up. Hence, in conclusion a soft-start mechanism is essential for any power supply system.

4.3 Under-Voltage Lockout Implementation (UVLO)

The input to the buck converter V_{in} is compared with a pre-assigned voltage level "V_{start}" using a comparator as shown in figure 4.6. If the applied input voltage is less than Vstart then the comparator generates a fault thus shutting off the converter. Hence the name given to the circuit implementation is, Under Voltage Lock-Out. Unless the applied input voltage is greater than V_{start}, the converter system is not allowed to start-up. V_{start} is the minimum value of the input voltage V_{in} for which the feedback loop is able to regulate the output voltage and hold it within the required output voltage accuracy requirements. The exact value of V_{start} for a given design is arrived at by sweeping the input voltage and then observing the buck converter output voltage. The value of V_{in} for which the feedback loop is no longer able to regulate the output of the buck converter must be selected as V_{start}.

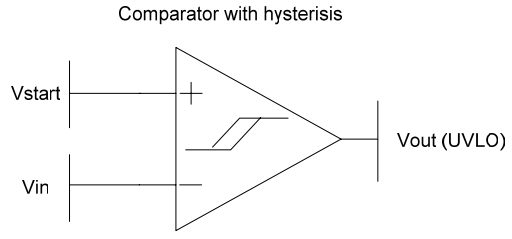

Figure 4.6 UVLO implementation using a comparator with hysterisis.

The output of the comparator is given as one of the inputs to an OR gate, the other input coming from the output of the OC (Over Current) comparator. The output of the OR gate is then fed to a set dominant SR flip flop which generates a fault signal when Vin is less than Vstart thus turning of the upper transistor which powers the buck converter.

A comparator with hysterisis is implemented using the general design methodology shown in figure 4.7. The operation is described as follows. When the input voltage V_{in} exceeds $V_{ref\text{-}high}$ the upper comparator goes high which sets the output of the SR flip flop high and when V_{in} falls below $V_{ref\text{-}low}$ the lower comparator goes high resetting the output of the SR flip flop to a low. In the V^2 implementation, $V_{ref\text{-}low}$ is V_{start} and $V_{ref\text{-}high}$ is a voltage greater than V_{in}. In figure 4.7, $V_{ref\text{-}high}$ is V_{start} and $V_{ref\text{-}low}$ is the given specification of V_{in}.

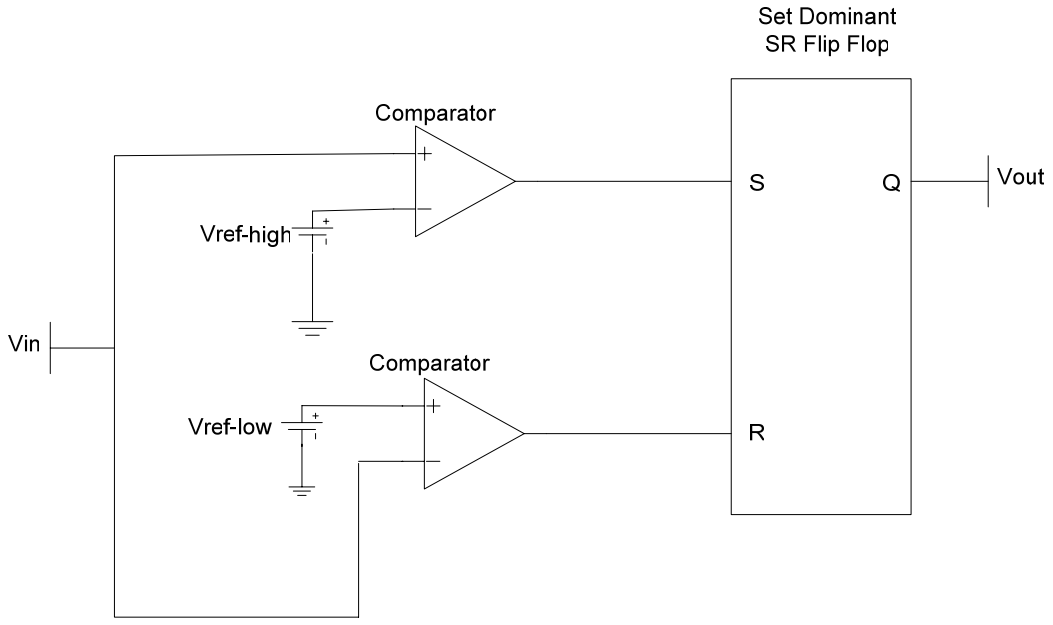

Figure 4.7: Comparator with hysterisis.

The hysterisis curve of the above implementation is shown in the figure below (Figure 4.8)

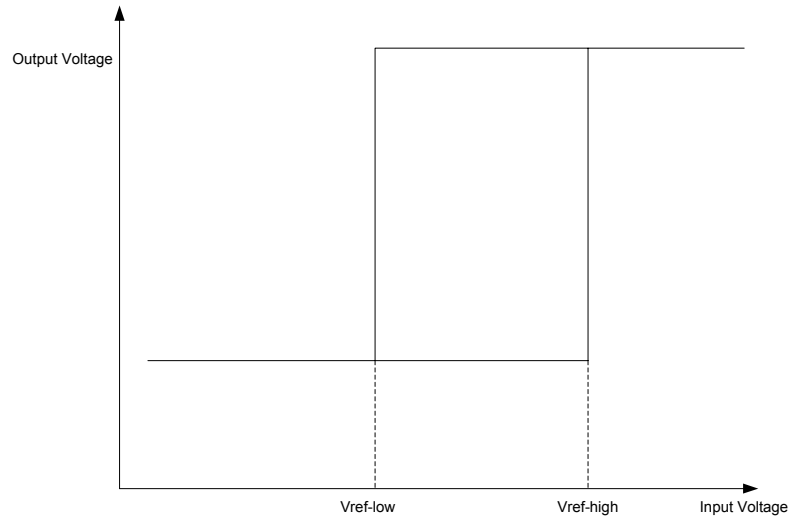

Figure 4.8: Hysterisis curve of the comparator.

The schematic of the comparator with hysterisis in PSPICE is shown in figure 4.9. The implementation shown in figure 4.9 is for modeling the behavior of a comparator with hysterisis in PSPICE only. An on-chip implementation for a given process will require an implementation as described in [22]. The diodes shown in figure 4.9 can be implemented using the parasitic BJT or a diode connected MOSFET in a MOS process.

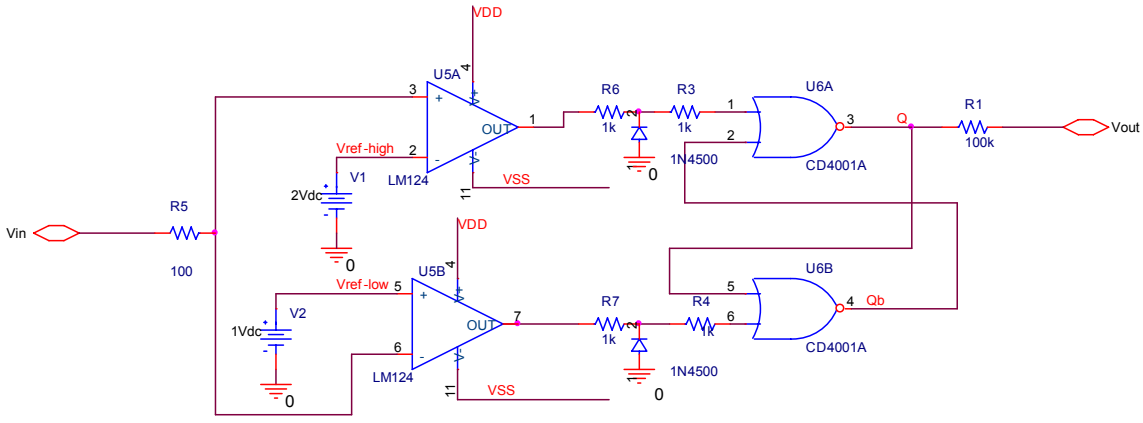

Figure 4.9: Comparator with hysterisis in PSPICE

4.4 100% Duty Cycle Comparator

The 100% duty cycle comparator, with hysteresis is implemented as shown in figure 4.10. The development of hysteresis is covered in section 4.5.

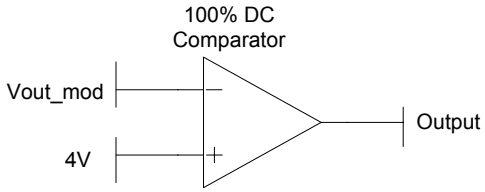

Figure 4.10: 100% Duty Cycle Comparator

The output of the modulator (buck converter), V_{out_mod}, is compared with a 4V dc voltage. The operation of the 100% duty cycle comparator is described as follows. The output of the buck converter is given to the inverting input terminal of the 100% DC comparator. When the output of the buck converter falls below 4V from the nominal value of 5V and the clock generator is generating a high pulse, the comparator goes high and disables the high transistor thus preventing any more input being applied to the buck converter and thus ensuring that the duty cycle does not increase any more. Note here that the 4V and 5V (output of the buck converter) values are used here to explain the functionality of a 100% duty cycle comparator When the output of the buck converter reaches 4V and is still continuing to fall, the feedback loop tries to increase the duty cycle D so that the buck converter output is pulled up to around 5V. But at this point the duty cycle will have reached 80% of the pulse width and any further increase should be avoided because when D reaches 100% of the clock pulse width it cannot increase anymore. . Note that for an on-chip implementation the 4V can be implemented by a 1V

voltage reference and V_{out_mod} must be scaled down to 1.25V using a resistor divider network at the output of the buck converter.

4.5 Over-Current Protection

Over Current protection is included in the design to protect the discrete components in the buck converter such as inductors, switches and capacitors from the stress of an excess influx of current from V_{in}. Excess influx of current through the converter is detected by sensing the current flowing through the inductor and then taking appropriate action (i.e. cutting off the input voltage source from the buck converter) when a sudden inrush of current is detected [16]. Initially when the input voltage is applied to the buck converter the output node (output of the buck converter) has not yet reached its final DC value of V_{in} times the duty cycle, D and the output node is at ground potential. Hence, the entire input voltage is applied across the output inductor causing a sudden increase in inductor current. This initial current spike is defined as the excess influx of current.

The implementation of over-current protection is shown in figures 4.11 and 4.12.

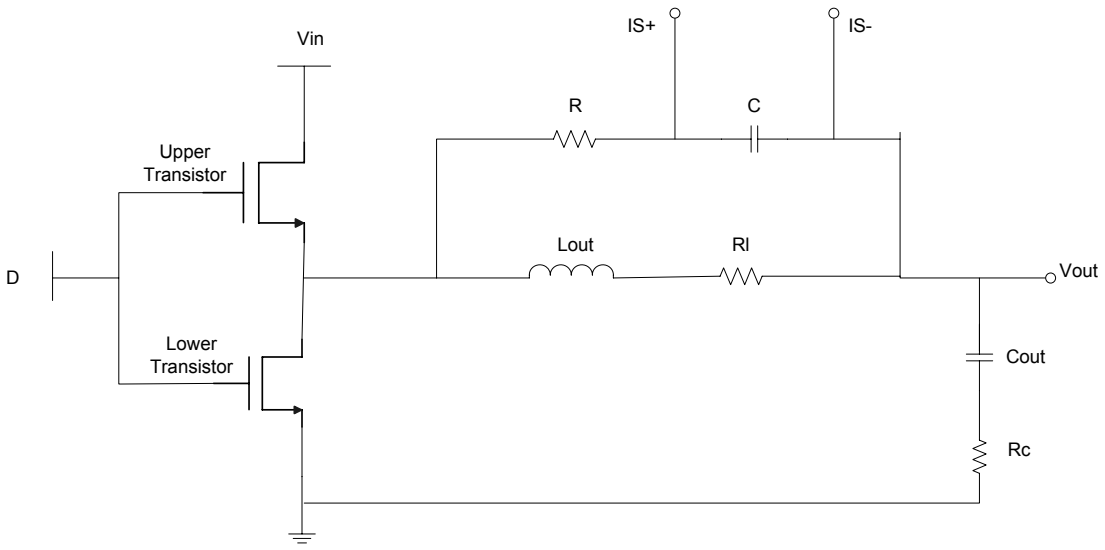

Figure 4.11: Current sensing mechanism.

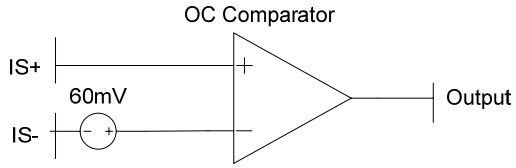

Figure 4.12: OC protection scheme.

The current flowing through the inductor is sensed using the equivalent series resistance of the inductor R_L. The output current is sensed using an RC network in parallel with the inductor as shown in figure 4.11. The voltage across the capacitor C is then fed to the OC comparator. If the values of R and C are chosen such that,

$$\frac{L}{R_L} = RC \tag{4.3}$$

If the above criterion is met, the voltage across the capacitor then represents the instantaneous value of the inductor current. The voltage across the capacitor is given by,

$$V_C = I_L \times R_L \tag{4.4}$$

where I_L is the current through the inductor. Hence, according to equation 4.4 the voltage across the capacitor is proportional to the inductor current. For a designed value of the output inductor, the inductor datasheets give the saturation current and the equivalent series resistance of the inductor. Substituting this value in equation 4.4 the value of V_C provides the designer with the threshold voltage across the capacitor. As a design example for a 1.75mH output capacitor the values of saturation current and the equivalent series resistance are 3A and 30mΩ respectively (Source: www.alldatasheet.com, www.ctparts.com). Selecting 2A as the maximum allowable current via the inductor (to be safe even though the datasheet gives a maximum saturation current of the inductor to be 3A) V_C from equation 4.3 turns out to be 60mV (shown in figure 4.1). This value of threshold voltage has been used in the simulation of the DC-DC system in this thesis. A 60mV offset at the input of the comparator in figure 4.12 can be generated by using a comparator with hysterisis.

Under normal load conditions, the voltage across the IS+ and IS– pins of Figure 4.11 is less than the 60 mV overcurrent threshold. If the threshold is exceeded, the overcurrent fault signal is generated, the high side gate driver is forced to shut down and the compensation capacitor C_{comp} at the output of the error amplifier is discharged with 5.0 μA. The threshold voltage of 60mV and the discharging current sink of 5 μA depends upon the maximum current rating of the output inductor. This concept is explained in more detail after the over-current protection is explained.

External hysteresis has to be included in the Over-Current (OC) comparator to incorporate the 60mV hysteresis at the comparator input to implement over-current protection in the DC-DC system. Such an implementation is shown in figure 4.13. The block which shows the comparator with hysteresis contains the circuit in figure 4.7. The positive feedback using resistors R1 and R2 incorporate an external 60mV hysteresis.

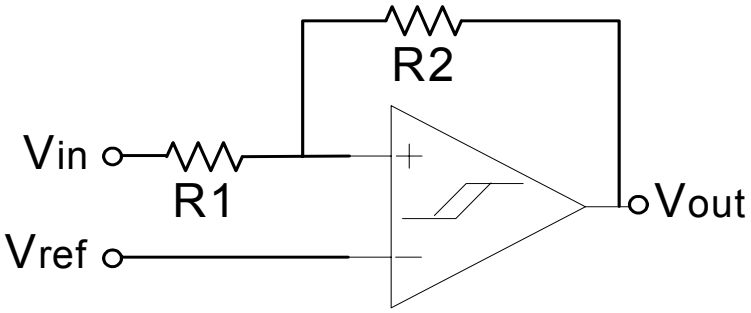

Figure 4.13: OC comparator with external hysteresis.

Hence, this external hysteresis is superimposed upon the hysteresis provided by the circuit in figure 4.7. If a single polarity power supply V_{DD} is utilized, then the hysteresis threshold is given by,

$$V_{th} = V_{DD}\left(\frac{R1}{R1+R2}\right) \tag{4.5}$$

For a supply voltage of 3.3V and a required threshold of 60mV, a possible value of resistors R1 and R2 are 2KΩ and 0.1MΩ respectively.

4.6 Voltage Reference

This section details the circuit design implementation of the voltage reference at the input of the error amplifier. This voltage must be a constant with variation in

temperature. This requirement is satisfied by a bandgap reference circuit which uses the positive temperature co-efficient of a resistor and the negative temperature co-efficient of the body to source voltage of a diode junction to generate an output voltage that remains constant with temperature variations. One such implementation of a bandgap reference circuit is shown in figure 4.14. Transistors M1-M4form a current mirror that mirrors the current produced by the combination of the resistors R1 and R2 and transistors M1 and M2. The diodes D1 and D2 can be implemented in a CMOS process by either the parasitic BJT or by a diode connected MOS device [23]. The reference voltage hence is given as [23],

$$V_{ref} = \frac{R3}{R2}\left(V_D + \frac{R2}{R1} \times \ln(N) \times V_t\right) \tag{4.6}$$

Where V_D is the forward diode voltage and V_t is the thermal voltage KT/q.

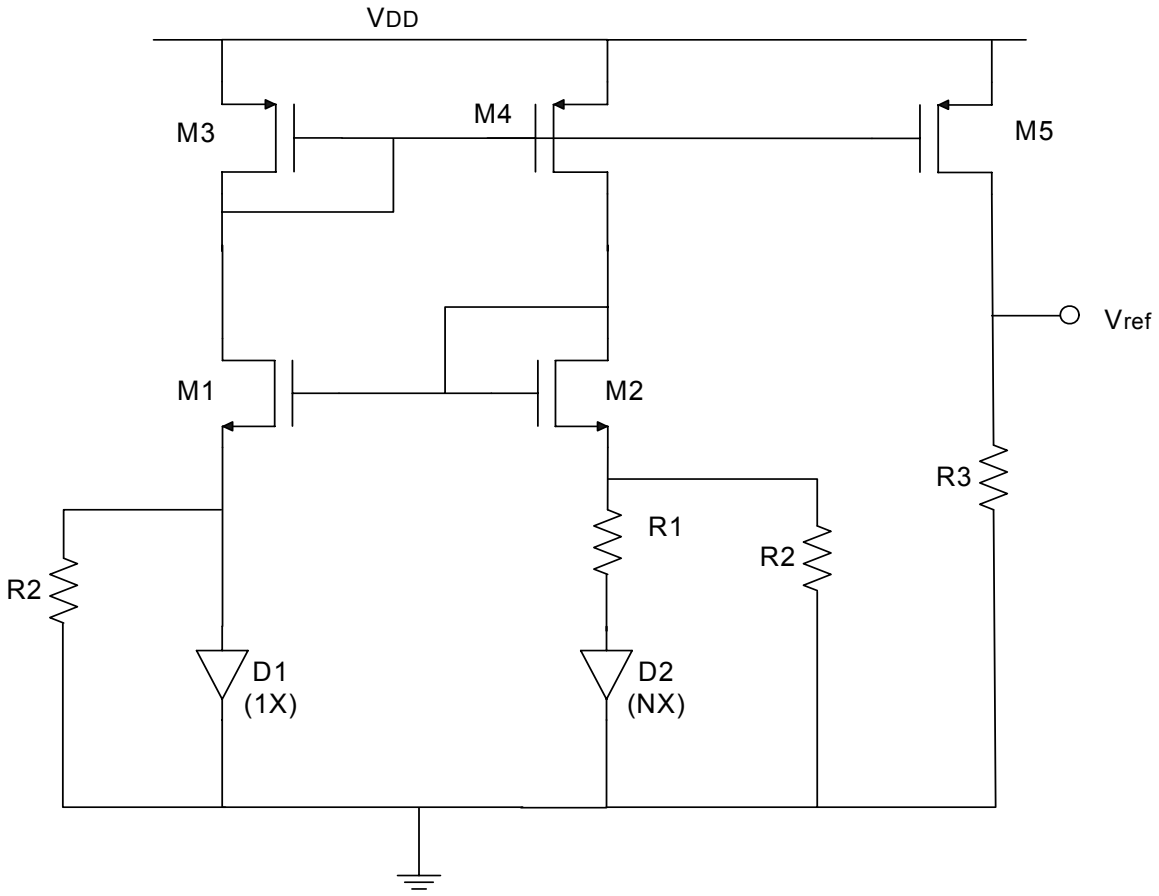

Fig. 4.14: Bandgap Reference

R1, R2, R3 and N can be chosen to obtain a voltage reference of 1V from the circuit in figure 4.14 [23].

4.7 Error Amplifier

This section details the transistor level implementation of the error amplifier and also the specifications of the error amplifier. The error amplifier is implemented as a single dominant pole Operational Transconductance Amplifier (OTA). There are three major requirements from the error amplifier, namely,

(i) Open loop gain, Av and

(ii) Offset voltage, V_{OS}.

(iii) GBP

The inputs to the error amplifier are the reference voltage, V_{ref}, at the positive input terminal and the output of the buck converter, V_{out}, at the negative input terminal. The output of the error amplifier is given to the PWM (Pulse Width Modulated) comparator. Note that the V_{out} at the error amplifier input is the scaled down version of the actual output of the buck converter. The output of the error amplifier must be equal to V_{ref} because the PWM comparator compares this DC value with the ramp signal derived from the output of the buck converter which has a DC value of V_{ref}. Hence, the error amplifier must have enough open loop gain to be able to amplify the smallest differential input to V_{ref}. The differential signal at the input of the error amplifier depends upon the maximum accuracy at the output of the buck converter. Hence, the maximum open loop gain from the error amplifier is given by,

$$A_v \geq \frac{100}{Hsensor \times \%accuracy} \tag{4.7}$$

The gain from equation 4.7 must be attained for the entire range of temperature operation. A possible circuit implementation of the error amplifier is shown in figure 4.15.

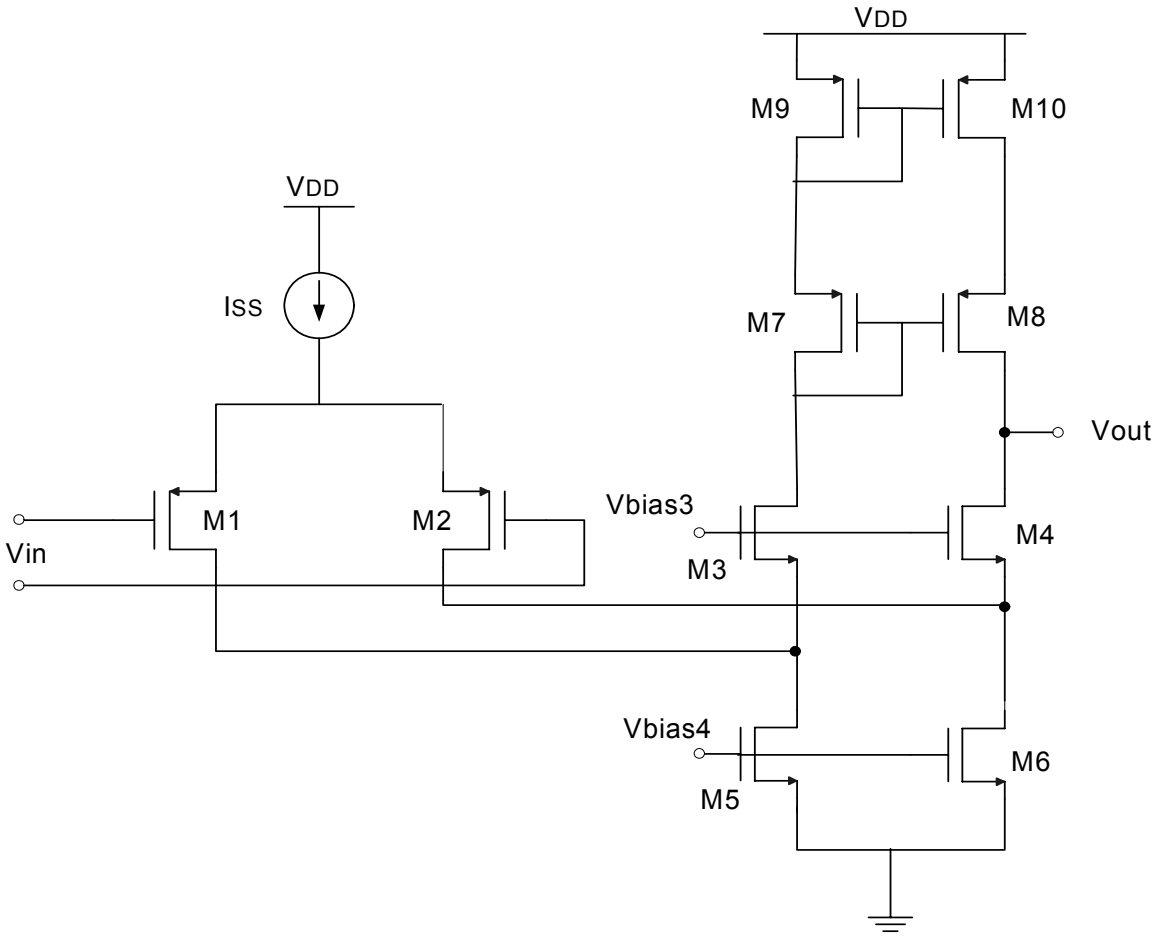

Figure 4.15: Error Amplifier implemented as a folded cascade OTA.

The open loop gain from the above (figure 4.15) is given by [21],

$$A_{vol} \approx g_{m1,2} \times \left(g_{m4} ro_4 ro_6 \parallel g_{m8} ro_8 ro_{10} \right) \tag{4.8}$$

Also the transconductance of the input differential pair is given by,

$$gm = I_{Tail} / V_{ov1,2} \tag{4.9}$$

Since for a 1msec start-up time I_{tail} was chosen to be 100uA (equation 4.2b), hence from equation 4.9 for an overdrive voltage of 200mV for the design in figure 4.15 gives a g_m of 0.5mS.

A telescopic cascade with a PMOS input pair implementation has been chosen to accommodate V_{ref}, which is 1V, is closer to ground potential and a PMOS input pair implementation ensures that V_{ref} falls within its input common mode range. If more gain is required from the OTA then either a two stage implementation or a gain boosted telescopic cascode OTA must be chosen. These implementations will not be discussed in this thesis.

Since, the speed of the error amplifier is not critical in determining the overall transient response of the error amplifier hence bandwidth is not a major issue in the OTA design. However, it is critical that all the OTA non-dominant poles be approximately 2.5 times the system closed loop GBP. For folded cascade OTA implementation shown in figure 4.15, there is a non-dominant pole at the input of the differential pair due to its tranconductance, $g_{m1,2}$ and its input capacitance C_{gs}. Due to the negative feedback formed due to the combination of the fast feedback path and the slow feedback path as explained in chapter 3 a zero is generated but the non-dominant pole from the error amplifier generates a doublet at its non-dominant pole frequency which leads to degradation in the settling response of the feedback network. The analysis is as follows.

Let ω_{p1} = dominant pole = $\dfrac{1}{r_{out} \times C_C}$ (r_{out} is the error amplifier output impedance and C_C is the compensation capacitor at its output) and

$$\omega_{p2} = \text{non-dominant pole} = \frac{g_{m1,2}}{C_{gs1,2}} \tag{4.10}$$

where, $C_{gs1,2} = \dfrac{2}{3}(WL)_{1,2} C_{ox}$.

The open loop transfer function of the error amplifier is now,

$$Av(s) = \frac{A_0}{\left(1 + \frac{\omega}{\omega_{p1}}\right)\left(1 + \frac{\omega}{\omega_{p2}}\right)} \tag{4.11}$$

Hence, the transfer function from the output of the buck converter to the output of the comparator is given as

$$\begin{aligned}
\frac{\hat{vo}}{\hat{d}} &= -FM(1 + Av(s)) \\
&= -FM\left(1 + \frac{A_0}{\left(1 + \frac{\omega}{\omega_{p1}}\right)\left(1 + \frac{\omega}{\omega_{p2}}\right)}\right) \\
&= -FM\left(\frac{A_0 + \left(1 + \frac{\omega}{\omega_{p1}}\right)\left(1 + \frac{\omega}{\omega_{p2}}\right)}{\left(1 + \frac{\omega}{\omega_{p1}}\right)\left(1 + \frac{\omega}{\omega_{p2}}\right)}\right) \\
&\approx -FM \times A_0\left(\frac{\left(1 + \frac{\omega}{\omega_z}\right)\left(1 + \frac{\omega}{\omega_{p2}}\right)}{\left(1 + \frac{\omega}{\omega_{p1}}\right)\left(1 + \frac{\omega}{\omega_{p2}}\right)}\right)
\end{aligned} \tag{4.12}$$

where, $\omega_z = A_0 \times \omega_{p1}$

As can be seen from equation 4.12 there is a doublet at ω_{p2} which affects the settling time response of the feedback. This scenario can be avoided by designing ω_{p2} to be at least 2.5 times greater than the system GBP so that the settling response time is not drastically effected. This condition dictates the selection of the input differential pair geometry from equation 4.10.

The input referred offset from the error amplifier must be at least ten times lesser than the minimum differential signal at the error amplifier inputs so that the feedback loop does not respond to an offset voltage inherent in an OTA design instead of an actual fluctuation at the buck converter output. Hence,

$$V_{os-OTA} \leq \frac{\Delta I_L \times R_C}{10} \tag{4.13}$$

4.8 Comparators

This section details the comparators used in the DC-DC system and the performance requirements from these comparators. In the DC-DC system there are four comparators, namely,

(i) PWM (Pulse Width Modulated) Comparator used to modulate the duty cycle,

(ii) 100% DC (Duty Cycle) Comparator used to ensure that the duty cycle does not reach 1,

(iii) UVLO (Under-Voltage Lock Out) Comparator used to ensure the feedback loop is not enabled until the input voltage V_{in} exceeds V_{start} and

(iv) OC (Over-Current) Comparator used to ensure that the current via the output inductor does not exceed its rated saturation limit.

Of all the four comparators only PWM (Pulse Width Modulated) Comparator has a stringent requirement on its open loop gain and the 3-dB bandwidth since only the PWM comparator appears in the actual feedback path which is responsible for modulating the duty cycle of the buck converter. Also all four comparators should use

some form of hysteresis to avoid logic bounce or chatter. The implementation of the Under-Voltage Lock Out (UVLO) comparator has been detailed in section 4.3. The over-current comparator is implemented in the same way as the UVLO comparator except that it is designed for a hysterisis of V_{th} (shown as 60mV in figure 4.1). The OC comparator must have enough gain to be able to amplify this threshold voltage V_{th} to a logic high level at the comparator output, V_{OH}. V_{OH} is approximately 90% of the supply voltage V_{DD}. Hence open loop gain from OC comparator is

$$A_{vol-OC} \geq \frac{0.9 \times V_{DD}}{V_{th}} \tag{4.14}$$

Also with OC comparator the input offset voltage is an important specification since the comparator should always give an output for a valid differential signal and not its own offset voltage. Hence, the offset from the OC comparator must be at least an order of magnitude less than the threshold voltage, V_{th}, i.e.

$$V_{os-OC} \leq \frac{V_{th}}{10} \tag{4.15}$$

The inputs to the PWM comparator are the output of the buck converter at its negative input terminal and the error signal generated by the error amplifier at its positive input terminal. The buck converter output is the ramp voltage due to the inductor current ramp and the ESR of the output capacitor which is DC offset by the magnitude of the error signal. The PWM comparator must have enough open loop gain to be able to amplify the lowest amount of differential signal to a valid output voltage level. Hence, the minimum open loop gain requirements from the PWM comparator is

$$A_{vol-PWM} \geq \frac{\left(V_{OH} - V_{OL}\right)}{\left(\frac{1}{2} \times \Delta I_L \times R_C\right) H_{Sensor}} = \frac{\left(0.9 \times V_{DD} - 0.1 \times V_{DD}\right)}{\frac{1}{2} \times \Delta I_L \times R_C \times H_{Sensor}} \tag{4.16}$$

where, V_{OH} = Output high of the comparator = $0.9V_{DD}$,

V_{OL} = Output low of the comparator = $0.1V_{DD}$

Hsensor = Sensor gain between buck converter and the comparator input

ΔI_L = inductor ripple current and

R_C = ESR of the output capacitor.

For most applications minimum gains of 500 are adequate assuming a sensor gain of 0.2, 3.3V logic levels, 100mV of ripple voltage and a modest safety factor. Offset voltage specification is an important specification with the PWM comparator as well since it must only generate a reset signal for a valid change in the voltage at the output of the buck converter and not due to its inherent offset voltage. Hence, the offset voltage from the comparator must be an order of magnitude less than the least amount of differential signal at the PWM comparator input. Hence,

$$V_{os-PWM} \leq \frac{\Delta I_L \times R_C}{2 \times 10} = \frac{\Delta I_L \times R_C}{20} \tag{4.17}$$

The same comparator used for the PWM comparator can be used for the 100% DC (Duty Cycle) comparator. The offset voltage requirement from the 100% DC comparator is not as stringent as in equation 4.17.

4.9 Simulation Results

The V^2 architecture shown in figure 4.1 was implemented in PSPICE for the following specifications.

Input Voltage, V_{in} = 25V

Output Voltage, V_{out} = 5V

Output Power, P_{out} = 3W

Inductor Current ripple = 20% of the output current

Output Voltage accuracy = 5% of output voltage

Clock Frequency, f_{sw} = 150 KHz

Using the design algorithm described in chapter 3 the design variables calculated are:

L_{out} = 1mH

C_{out} = 1.75mF

C_{comp} = 17.5uF

g_m = 0.5mS

R_L = 30mΩ and

R_C = 100mΩ

$I_{error} = I_{tail} = g_m \Delta V$ = 50-200uA resulting in a t_{ss} from equation 4.2b of 87 to 350ms for V_{ref} of 1V.

The simulation results of the model are presented in this section. The simulation results prove the feasibility of a step-down DC-DC converter employing V^2 control mechanism for high temperature applications. With variation in temperature the component values of the capacitor and the inductor as well as the transconductance of the error amplifier change. The design of a DC-DC system has to take into account these variations and still hold the output voltage in regulation within the required output

voltage accuracy requirements. The simulation results of the developed model show that the output voltage is observed to hold in regulation over a range of temperatures from room temperature to 200°C within 5% of the output voltage.

The first simulation presented shows the response of the V^2 model with variation in the load of the buck converter (figure 4.16). The presented simulation result verifies that the V^2 topology works with variation in load from a nominal load to 50% and back again to nominal load. Throughout this exercise the output voltage of the buck converter is within $\pm$ 5% of the expected output voltage i.e.5V. This simulation hence verifies that the V^2 topology works with variation in load and that the response time is limited by the speed of the comparator at the output of the Error Amplifier, the logic delay through the set-dominant SR flip flop and the choice of the size of the output inductor in the buck converter.

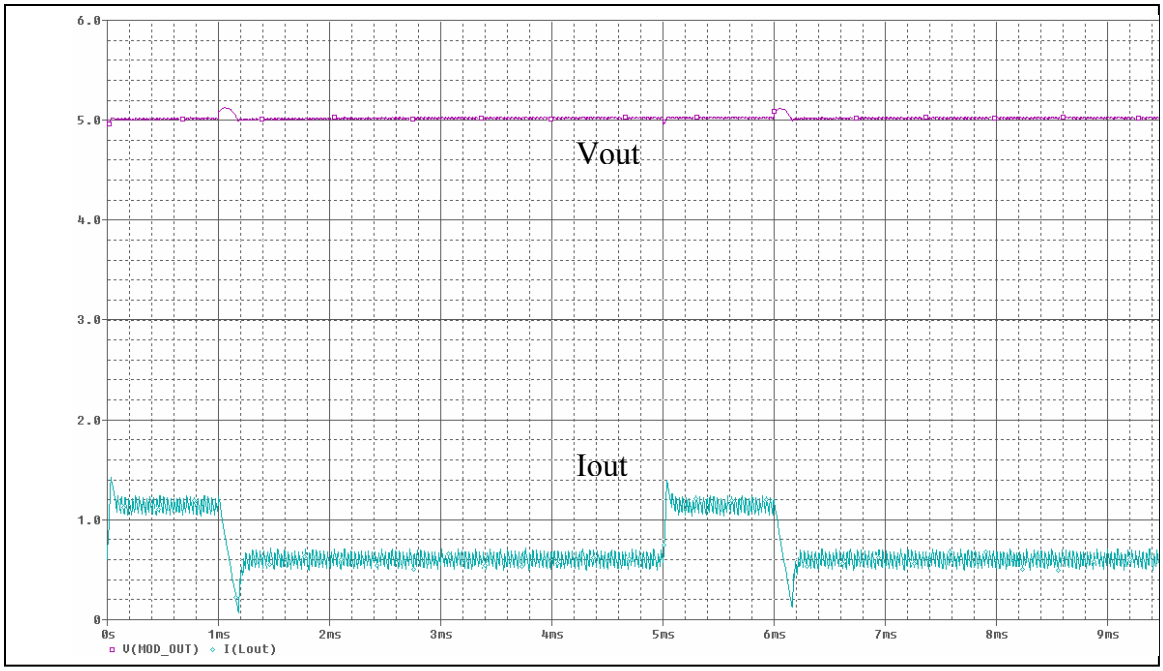

Figure 4.16: Variation in the load from full load to half load and then back to full load.

In the above simulation (Figure 4.16) the load resistance has been varied from the nominal value of $8.33\,\Omega$ to half of $8.33\,\Omega$ i.e. $4.165\,\Omega$ and the output voltage and current at the output of the buck converter have been plotted over a duration of 10msecs. Note that the output voltage is being held constantly within 250mV of 5V, which is 5% of 5V throughout this entire process.

The next simulation (Figure 4.17) shows that the V^2 topology works even when the values of the output capacitor and inductor vary by 20% from their nominal values.

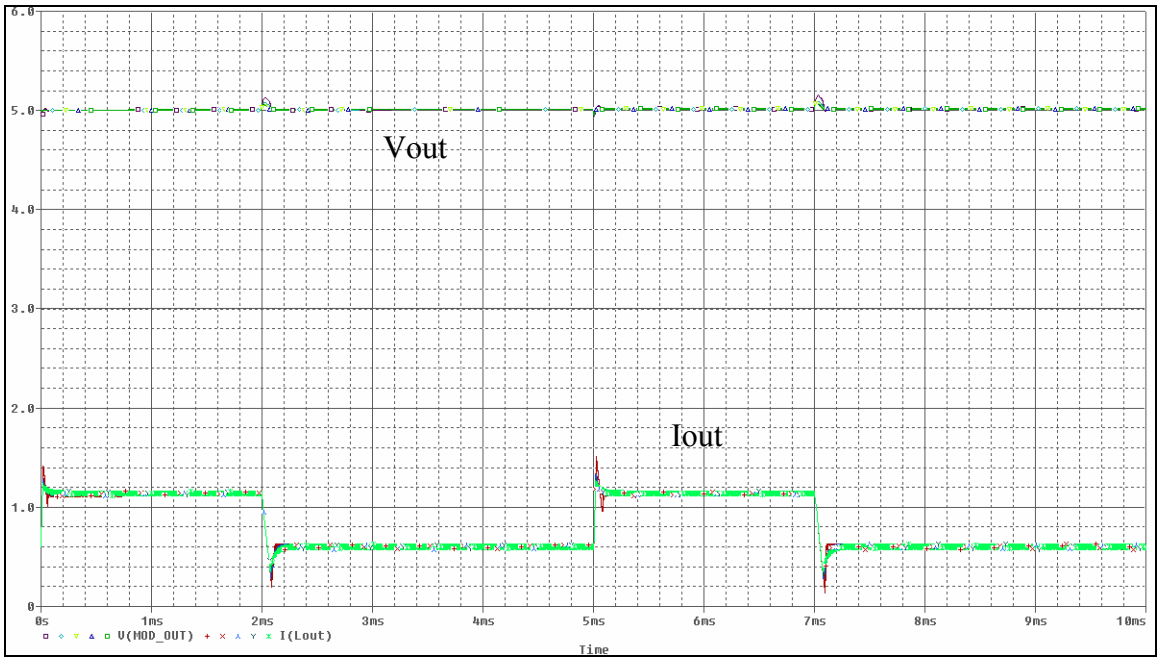

Figure 4.17: Plots of Vout and Iout with change in Cout (output capacitance of the buck converter).

The above figure (Figure 4.17) shows the plots of Vout and Iout when the output capacitor is swept from 240 μF to 360 μF for five values of Cout namely, 240 μF, 270 μF, 300 μF, 330 μF and 360 μF. The designed value of Cout is 300 μF. So the value of Cout has been swept by 20% around the designed value of 300 μF to account for the change in the capacitance of the output capacitor with variation in temperature. The temperature co-efficient of capacitor values in the range of 100-400 μF range are in the range of $\pm$1-15% (Source: www.alldatasheet.com). The capacitors that were found to operate in the temperature range of -40°C-125°C. The temperature range for the design of the DC-DC system in this thesis extends up to 200°C. Since, capacitors that can work at 200°C were not found a worst case temperature co-efficient of $\pm$20% is assumed in this work.

The response of V^2 topology with variation in the output capacitor confirms that the designed value of the output capacitor is sufficient to hold the output voltage within 5% of the nominal output voltage of 5V even with temperature variations. Note that the above simulation also includes the change in load from full load to half load and then back again to full load. The simulation results show that the output voltage variation is within 5.1V.

A similar exercise is repeated for a $\pm 20\%$ variation in the value of the output inductance in the buck converter. The simulation result is shown in the figure below (figure 4.18).

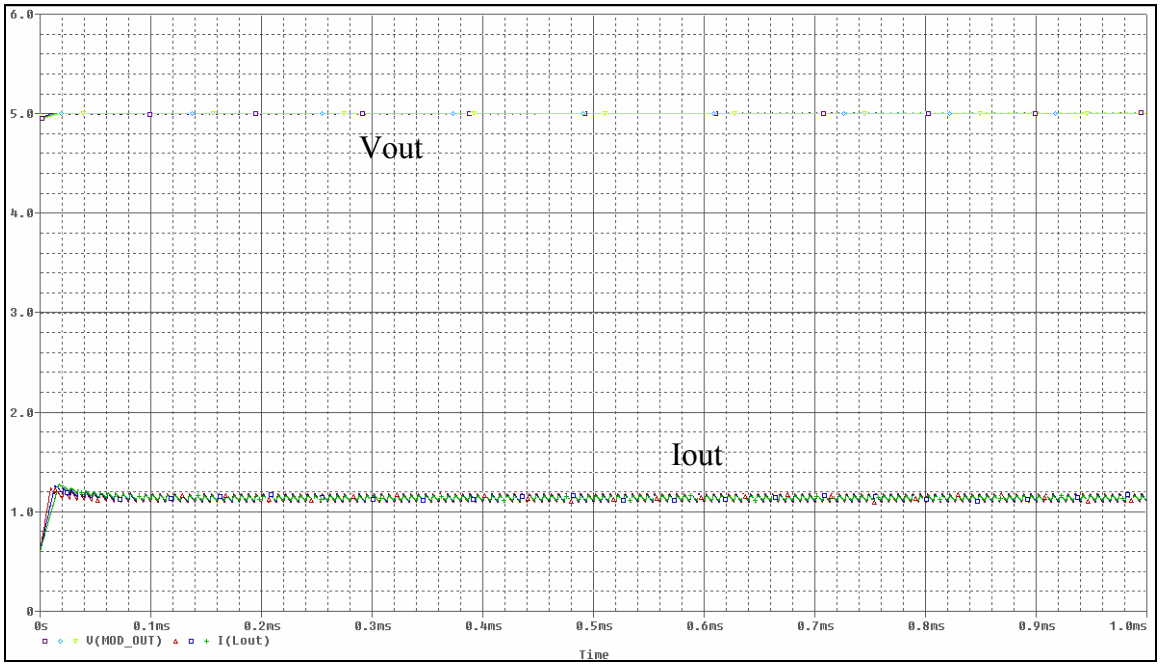

Figure 4.18 Plots of Vout and Iout with change in Lout (output inductance of the buck converter)

The above figure (Figure 4.18) shows the plots of Vout and Iout when the output inductor is swept from $180\,\mu$H to $270\,\mu$H for five values of Lout namely, $180\,\mu$H,

200 μH, 225 μH, 240 μH and 270 μH. The designed value of Lout is 225 μH. So the value of Lout has been swept by 20% around the designed value of 225 μH to account for the change in the inductance of the output inductor with variations in temperature. Again the above simulation result shows that the V^2 topology does not fail with variation in output inductance value with variation in temperature.

The next simulation result (Figure 4.19) shows that the V^2 topology holds the output voltage within 5% of its nominal value even when the transconductance, gm, of the Error Amplifier is derated to 1.5 times the designed value [18].

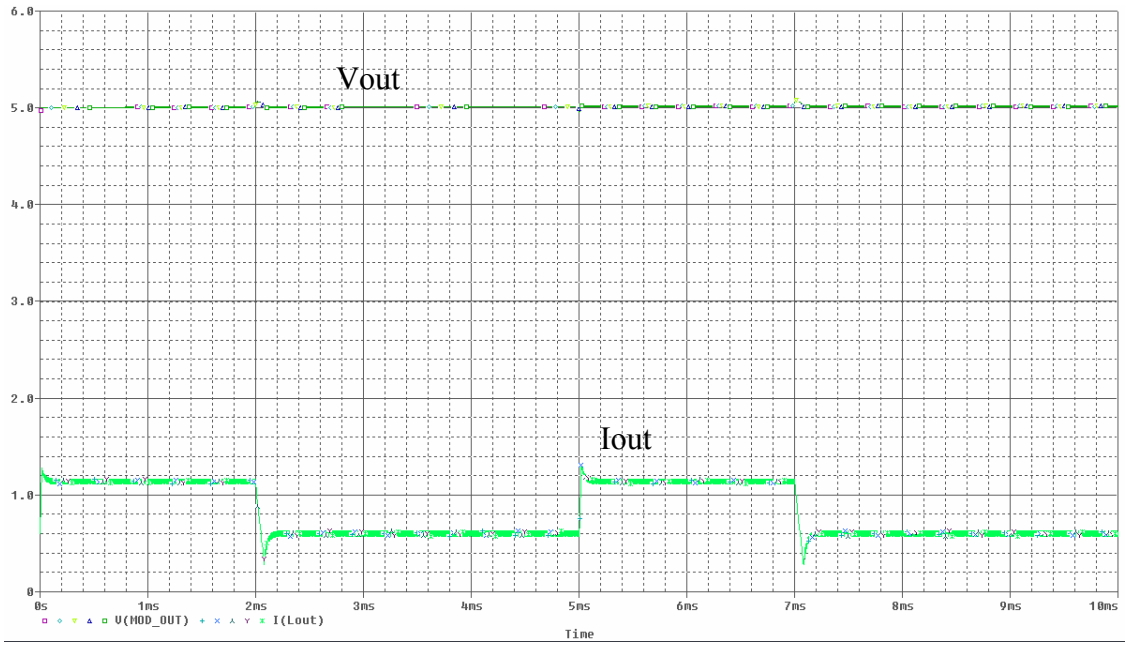

Figure 4.19: Plots of Vout and Iout with change in gm (transconductance of the error amplifier)

The above figure (Figure 4.19) shows the plots of Vout and Iout when the transconductance of the error amplifier is swept from 0.1mS to 0.9mS for five values of gm namely, 0.1mS, 0.3mS, 0.5mS, 0.7mS and 0.9mS. The transconductance of the error

amplifier has been swept to account for the mobility degradation with increase in temperature and hence the variation in the transconductance of the error amplifier. The designed value of the transconductance of the error amplifier is 0.5mS. So the value of the transconductance has been reduced by 2.5 times and the response in as shown in figure 4.16.

From the above simulation result shows that the V^2 topology does not fail with variation in the transconductance of the error amplifier with variation in temperature. Here only the transconductance of the error amplifier has been varied and not the gm's of the comparators and OTA's used to implement UVLO (Under Voltage Lock-Out), OC (Over Current) comparator and the 100% DC comparator.

The simulation results shown in this section show the feasibility of a DC-DC step-down converter system employing V^2 control topology is operational from room temperature to about 200°C and that the design equations and analysis detailed in chapter 3 give a very good basis to start any DC-DC converter design once the input specifications in the form of the input voltage to be stepped down, the output voltage to be stepped down to, the output current ripple requirements, the output voltage accuracy requirements and the process information is given to the designer.

Chapter 5

Conclusion and future work

5.0 Conclusion

In this thesis a detailed study of a step-down converter employing V^2 control architecture has been undertaken. Design equations for the design of a DC-DC system using V^2 control scheme have been developed and an iterative design algorithm has been developed to aid in the system design. The compensation scheme of the DC-DC system, which includes the buck converter and the feedback network, has been addressed and a simple compensation scheme as applicable to the V^2 control scheme has been shown. A SPICE model of the buck converter employing V^2 control scheme has been developed. This model incorporates the implementation of an over-current protection, under-voltage lockout mechanism, 100% duty cycle comparator and a soft-start implementation. The model is observed from room temperature to 200°C by incorporating the change in the discrete component values (such as resistors, capacitors and inductors) and the transconductance of the error amplifier and comparator into the model. A design example to perform 25V to 5V step-down operation with an output voltage accuracy of less than 5% is shown has been undertaken and simulation results pertaining to this design

example have been shown. The voltage at the output of the buck converter is observed for variation in load conditions from half load to full load and then back to half load again. The discrete component values as well as transconductance values have been varied and the buck converter output voltage has been observed while the load is changed from full load to half load and then again to full load. The output of the buck converter is shown to be within the output accuracy requirements. The design equations and the design algorithm used in the design example can be used to design the step-down operation for a different set of input specifications.

The individual blocks in the feedback network have been identified and their performance metrics have been characterized. Transistor level implementation of the blocks in the feedback network has been suggested. Suggestions on the implementation of the individual design elements in the feedback design have been made. The studied modeled has been applied to an example design and simulation results show that the design works as described in theory. The final conclusion is that the V^2 control topology can be applied for the design of a high temperature DC-DC converter and that the design analysis and design equations detailed in chapter 3 will guide the design steps in such a design.

The study conducted in this thesis also shows that not only is the V^2 feedback topology presents the designer with a fast transient response, a reduced number of design components in the feedback design and reduced complexity in the design of a stable DC-

DC converter. In conclusion a first of its kind study of a DC-DC system using V^2 control scheme for high temperature applications is reported.

5.1 Future work

As far as practical implementation of the model presented in this thesis is concerned it is important to find high temperature capacitors in the range of 0.5-1.5mF range and high temperature inductors in the range of 1-2mH. The temperature co-efficients and tolerances of these components have to included in the developed model and the buck converter output voltage must be observed to satisfy the output voltage accuracy requirements. If the output accuracy requirement is not achieved then the design algorithm described in chapter 3 must be used to redesign the DC-DC system.

The design shown in this thesis allows only a single input voltage level to be stepped down to an output voltage. This can be extended to multiple input-output step-down voltage combinations by the use of switched resistor divider network at the buck converter output as shown in figure 5.1 below.

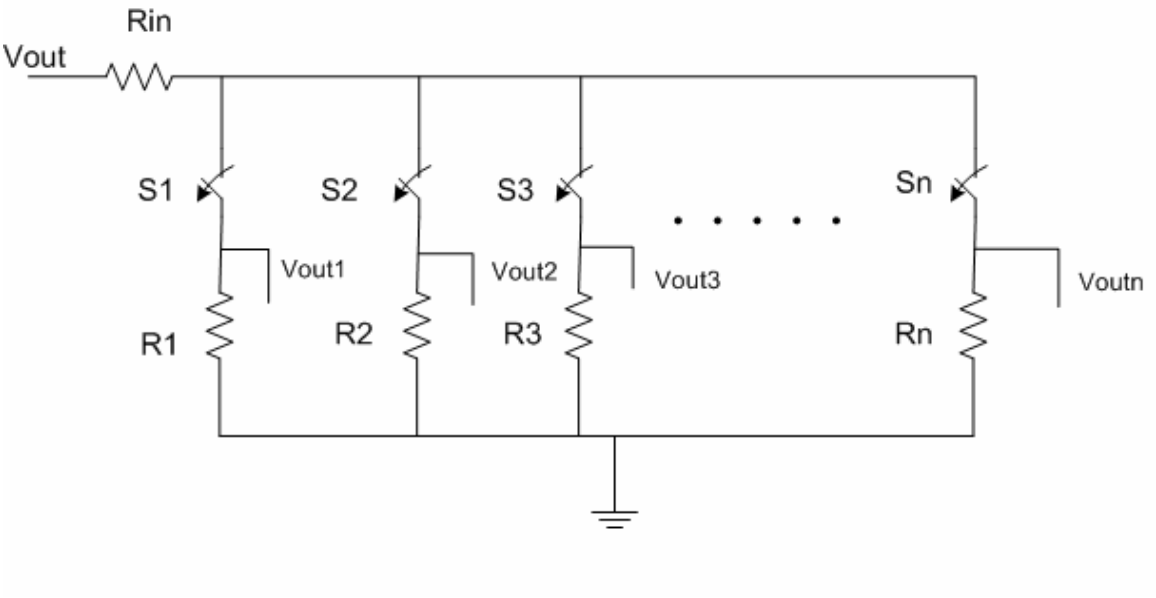

Fig. 5.1 Switched resistor divider network to generate a range of output voltages.

Finally the buck converter design can be extended to include a two phase design wherein two buck converters working 180° out of phase are employed. The advantage of this type of design is that the inductor current is shared equally between two inductors thereby reducing the requirement of using inductors with high saturation currents [24]. Hence stress on individual components is reduced which leads to more freedom in the choice of individual components (output capacitor and inductor) in the design of a buck converter.

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