DESIGN AND FABRICATION OF UNCOOLED THERMOELECTRIC INFRARED DETECTORS

By

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DESIGN AND FABRICATION OF UNCOOLED

THERMOELECTRIC INFRARED DETECTORS

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CHAPTER I

1. Introduction

There are numerous applications which involve detection of infrared radiation. FTIR or Fourier transform infrared spectroscopy which is used to identify unknown materials or to determine absorption, reflection and transmission of a surface at each wavelength is a good example. Night vision cameras and heat sensors are other useful devices that detect infarred radiation.
Infrared (IR) is an electromagnetic wave which is radiated from any object above zero degree Kelvin. Based on Stefan's law, the total radiated power from an object is

$$(1) \qquad P_{rad} = \epsilon(T) * \sigma * T^4$$

Where σ is Stefan Boltzmann constant and equal to $5.6 * 10^{-8}$ $(\frac{W}{m * K})$, and Emissivity (or ϵ) is defined as the power radiated by an object to the radiation from a black body. The radiated power varies in different frequencies. The amount of power radiated at each wavelength at a known temperature follows Planck's radiation law which is

$$(2)\ M_e, \lambda = \frac{2\pi hC^2}{\lambda^5} \frac{1}{\exp\left(\frac{hc}{\lambda KT}\right) - 1}$$

Where h is $6.6 * 10^{-34}$ (Joule $*$ Sec), C is the speed of light, λ is the wavelength in centimeters and K is Boltzmann's constant $1.3 * 10^{-23}$ $(\frac{Joul}{K})$. Based on the above equation, the maximum radiation at room temperature happens at 10 um wavelength. Some of the radiated power is absorbed by the atmosphere. For example, water molecules would absorb all of the radiation

between 5 um to 7.4 um [1]. At room temperature, radiations between 8 um to 14 um can propagate through the atmosphere without being absorbed.

As it was described, materials with different temperature radiate in different wavelengths. This infrared radiation spreads over a wide frequency range and can be divided into different regions (see Table 1).

	Near IR (um)	Intermediate IR (um)	Far IR (um)	Extreme or very far IR (um)
Wavelength	0.75-1.5	1.5-15	15-100	100-1000

Table 1- Infrared frequency range [2]

In general, IR radiations are not visible but they can be detected with different means such as thermal detectors and photo-detectors.

Infrared detectors can be split into two main categories: thermal detectors and photon detectors; and for any kind of detector, the aim is to convert the incoming radiation to an electrical signal.

In the thermal detectors, the incident radiation causes a change in a physical property of a material. A read out circuit measures the amount of the variation in that specific property. Bolometers, thermoelectric detectors, Golay cells, and pyroelectric detectors are examples of thermal detectors. In a bolometer the change in the resistance of a material is measured. In thermoelectric detectors the Seebeck effect is used to generate a voltage. In pyroelectric detectors, the change in the pyroelectric material temperature causes internal polarization. In Golay cells, the absorbed infrared radiation raises the temperature of a gas and that gas would expand due to temperature change and deforms a membrane. The induced stress in the membrane can be measured with different techniques. The challenge in thermal detectors is to limit the heat

conduction from the sensitive element to the surrounding. By further limiting this heat conduction assuming that the incoming radiation power remains constant, the sensitive element temperature would raise more and results in a higher responsivity. Responsivity is defined as the ratio of .readout circuit output voltage to the input power. [1]

The second group of infrared detectors is photon detectors. There are two main classes of photon detectors, photoconductors and photovoltaics. The incident radiation on the device would excite an electron from the valence band to the conduction band and changes the electrical properties of a semiconductor. Mercury cadmium telluride (HgCdTe) or MCT is a famous photoconductor that can operate up to 30 um wavelength and can almost reach to the theory limitations. MCT can also be used as a photovoltaic device by stacking CdTe/HgTe on top of each other. The operating temperature for these detectors is ~77 Kelvin. At higher temperatures, thermionic noises can also excite electrons as well as the incident radiation and the signal generated from the infrared radiation can be drawn in the noise completely. There are fabrication challenges associated with MCTs which makes them unsuitable for 2D arrays. [1]

Fabrication of uncooled thermoelectric infrared detectors is the focus of this thesis. In the next section, previous works will be discussed. In chapter 2, the operation of thermoelectric devices will be described and the materials that are used in the fabrication process are explained in details.

Chapter 3 is dedicated to the fabrication process. At first, process flow is explained and then each step as well as its fabrication difficulties is clarified. The final chapter is conclusion which contains the summary of the results.

2. History

Since the discovery of Seebeck effect, there have been numerous works on thermoelectric detectors and sensors and especially in the past decades, micro-machined infrared detectors have been the focus of many researchers. In 1986, Choice and Wise reported the fabrication of a thermopile array with the responsivity of 12 V/W and the detectivity of $5 * 10^7 \ \frac{\mathrm{cm} * \sqrt{\mathrm{Hz}}}{\mathrm{W}}$ [3]. As it is already described, responsivity is defined as the electrical output voltage per input radiation power. Detectivity is defined as

$$(3) \qquad \mathrm{D}^* = \frac{(\mathrm{A_d} * \Delta \mathrm{f})^{0.5}}{\mathrm{Vn}}$$

Where A_d is the area of the detector, Δf is the electronic bandwidth, and V_n is the RMS electronic noise. The higher the responsivity and detectivity are the better the detectors. Choice [3] used 40 thermocouples of polysilicon and gold. Their detector area was 400 um * 700 um, which is relatively large compared to the today's technology. Volkein et al. reported a fabrication of single pixel detector by using BiSbTe and BiSb thermocouple pairs with the responsivity of 500 V/W in 1991 [7]. A year later, a responsivity of 150 V/W was reported by ETH for a detector with p type and n type thermocouple pair that was fabricated on a chip with Op-Amps [7]. Kanno et al. in 1994, from the Japan Defence Agency in collaboration with NEC Corporation made a 128 * 128 pixel thermoelectric array using p and n type polysilicon. The responsivity of 1550 V/W was measured with the pixel size of 100 um * 100 um [7]. In 1998, Foote et al. reported the construction of 1500 um * 75 um, linear array detector which was made of BiTe and BiSbTe thermocouple materials. Their device had a responsivity of 1100 V/W while the response time of

the device was about 99 ms [43]. In the same year, Nissan research laboratory, (Hirota et al.) reported the fabrication of a 48 * 32 pixel array with a pixel size of 116 um * 116 um. Their pixel was supported with two isolation beams that each one was 14 um wide. The thermopile itself was 0.8 um. Each pixel consisted of a six pair thermocouple and they could reach 2100 V/W responsivity. Three years later, in 2001, they improved their pixel performance and could reach 2770 V/W. To do so, they reduced the isolation beam width from 14 um to 4.4 um. This time the pixel size was also reduced to 100 um * 100 um with a absorber size of 65 um * 65 um. Four years later, 2005, they made an array of 48 * 48 pixels with their best devices with the responsivity of 4300 V/W. This improvement was due to reduction of the beam and the thermopile width to 2.4 um and 0.34 um respectively. [4]

David Kryskowski and Justin Renkenc, in 2009, made a large array of 80 * 60 pixels. n and p type silicon was used as the thermoelectric materials to produce the responsivity of 300 V/W for a detector size of 130 um * 130 um. [5]

The research continues on the thermoelectric detectors and other thermal detectors. It has been tried to further limit the thermal conduction from the sensitive element to the surrounding area. New materials have been put in use to achieve better efficiency. This research also focuses in implementation of new materials in the fabrication of thermoelectric infrared detectors to further improve the thermal isolation.

CHAPTER II

Thermoelectric detectors

Thermal detectors are transducers that convert the incident infrared radiation on the detector to an electrical signal. There are three main types of thermal detectors: bolometers, pyroelectric, and thermoelectric detectors. In all three categories, the incident infrared radiation converts to heat and raises the temperature of a sensitive element. In the bolometers, this element is a temperature sensitive resistor. The output signal can be produced by applying a DC voltage across this resistor and measuring the change in the resistance. In the second type of the detectors, pyroelectric detectors, the change in the temperature of the element produces spontaneous surface charge due to its internal polarization [6]. For example, this surface charge can be applied to a gate of a metal oxide semiconductor filed effect transistor (MOSFET) with an active load to produce an electric signal [7]. In the last type of the thermal detectors, thermoelectric detectors, the difference in the temperature of the hot element and the rest of the detector which is called substrate or cold junction is directly converted to an electric voltage.

In the following chapter, it is discussed why thermoelectric detectors are the choice of this research and then the concept of operation will be explained followed by describing the detector structure in detail.

2.1 Why thermoelectric detectors?

Thermoelectric detectors do not need temperature stabilization as opposed to bolometers. In the bolometers, small ΔR variation should be detected with an amplifier. If both the substrate and the hot element temperature are changing within the operation temperature, it would be difficult for the amplifier to detect any resistance variation of the detector [7].

As it was discussed earlier, pyroelectric detectors respond to a change in temperature. Thus, mechanical chopper is required to chop the incoming radiation and therefore the induced temperature in the hot element. Additionally, since all the pyroelectric materials are piezoelectric, vibrations may induce microphonic noise in the output signal [7].

On the other hand, thermoelectric detectors do not need choppers and are not sensitive to environment temperature (no temperature stabilization is required). Additionally, if good thermoelectric materials such as polysilicon, compatible to the integrated chip processes, are used, low cost detectors can be mass produced [7].

2.2 Thermoelectric detector operation

Any thermal detector has a structure like the one shown in Figure 1. The incoming infrared radiation incidents on the sensor and is absorbed by the absorber layer on the surface. This causes the temperature of the sensor to rise and creates a temperature difference between the sensor area and the substrate.

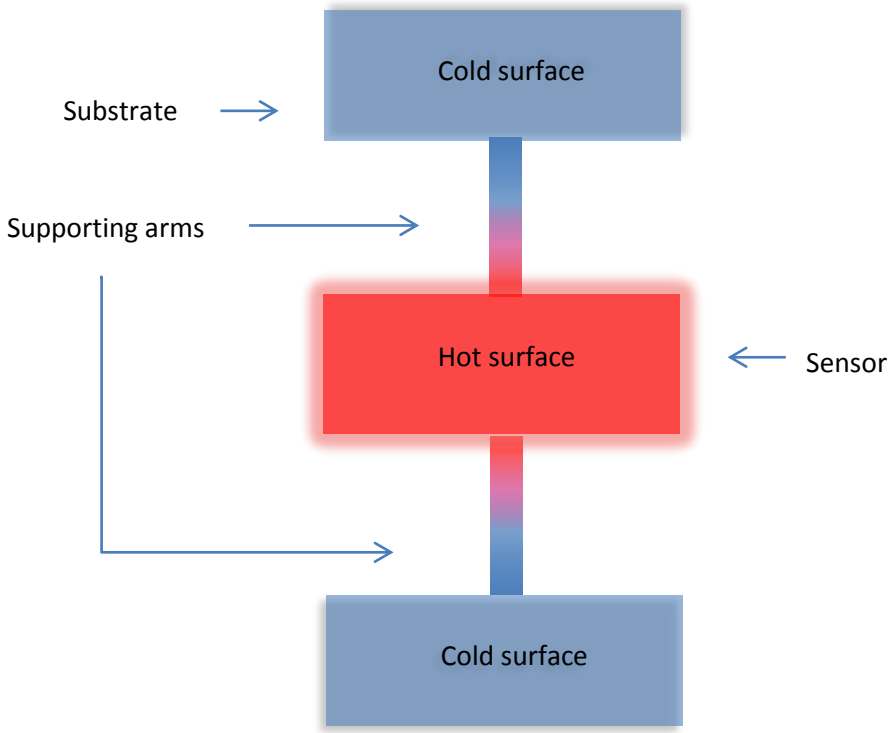


Figure 1 - Principle of thermoelectric detector

2.2.1 Thermoelectric material

The temperature difference between the hot element and the substrate can be converted to an electric signal and measured by a precision voltmeter. The output voltage can be expressed in the following mathematical format:

$$\delta V = S * \delta T \quad (4)$$

Where S is called Seebeck coefficient and δT is the temperature difference between the cold and hot junctions. As it can be seen in the above equation, materials with large Seebeck coefficient can produce large output voltages with a same temperature difference. This is the first important point in the thermoelectric detectors that a material with high Seebeck coefficient should be used. Metals usually have Seebeck coefficients less than $50 * 10^{-6}$ V/K and semiconductors have larger Seebeck coefficient (e.g. Silicon = $400 * 10^{-6}$ V/K and Se = $900 * 10^{-6}$ V/K [8]). Unfortunately, intrinsic semiconductors have very low electrical conductivity, and hence very high electrical resistivity which is not desired for sensor applications. One reason is that the noise voltage generated by the thermal noise (shown in the equation below) will be very large if the electrical resistance is high.

$$V_n = \sqrt{4k_B T R \Delta f} \quad [9] \quad (5)$$

Therefore, materials with low resistivity are required. From another point of view, if the output impedance of the detector is high, most of the output voltage drops across the internal resistor and there would be no detectable voltage at the output of the device.

To increase the electrical conductivity, semiconductors have to be doped to some level. When semiconductors are highly doped (if possible), their properties becomes similar to that of metals meaning that the Seebeck coefficient decreases and the electronic part of the thermal conductivity increases. Both of these effects are not desired. The importance of low thermal conductivity of

the thermoelectric materials will be discussed later in the next section.

ZT is the thermoelectric figure of merit which is used to express the performance of a thermoelectric device. [10] ZT is defined as

$$(6) \qquad ZT = \frac{S^2\sigma}{K} T$$

Where T, S, σ and k are temperature in Kelvin, Seebeck coefficient, electrical conductivity and thermal conductivity respectively. It has been shown that high ZT is achievable on highly doped semiconductor where the doping concentration is somewhere between 10^{19} to 10^{21} $\frac{\text{carrier}}{\text{cm}^3}$ [11]. Figure 2 shows the variation of ZT versus doping concentration [11].

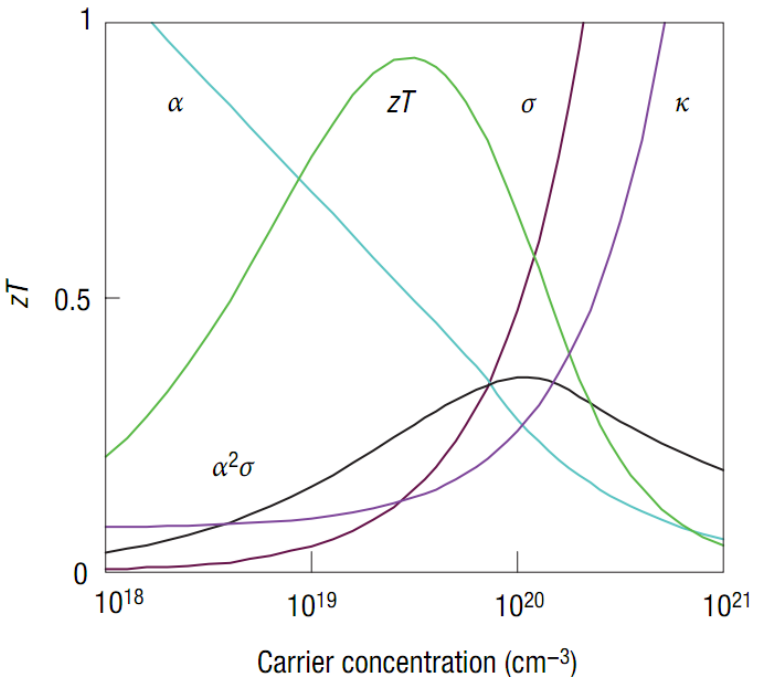


Figure 2 - ZT and power factor vs. doping concentration for Bi_2Te_3

Power factor which is defined as $S^2\sigma$ is also shown in Figure 2. Power factor is also important in the nanostructured materials where lattice thermal conductivity is dominant portion of the thermal conductivity. In this situation, power factor is tried to become maximum and once that is

achieved, reduction in the thermal conductivity by the means of nanostructuring is also attainable at the same time [12,13].

The conclusion is that to produce a large electric signal at the output, a material with high ZT at room temperature should be chosen. This material should also be compatible with the fabrication processes like deposition and etching. Polysilicon is a good option since it is compatible with conventional CMOS processes. It is not the best thermoelectric material at room temperature because of its high thermal conductivity but it has relatively high ZT comparing with other materials especially if nanowires are used instead of a bulk material [14,15].

2.2.2 Supporting arms

Earlier in the previous section, it was noted that the thermal conduction from the hot surface to the surroundings should be minimized. The reason is that to make a larger δT and hence larger δV ((4) $\delta \mathrm{V} = \mathrm{S} * \delta \mathrm{T}$) with the same amount of input radiation. There are three major mechanisms for heat transfer from the hot element to the surroundings: conduction, convection and radiation (Figure 1) [7]. Uncooled infrared detectors should operate under vacuum (<10 mTorr) to eliminate convection and conduction through the gas in the package [16]. Heat loss from the hot element due to radiation is usually negligible compared to heat loss through the supporting arms which is the principal heat loss mechanism. Thus, the heat conduction through the supports should be minimized. Supports are composed of the thermoelectric materials and few protective layers which enclose the thermoelectric materials to protect them in different steps of fabrication from solvents and other corrosive gases and also to provide the required mechanical strength.

In our work, polysilicon used as the thermoelectric material but since it has high thermal conduction, the cross section of the wires is made very small to lessen its undesired effect. As it is seen in the below equation (7),

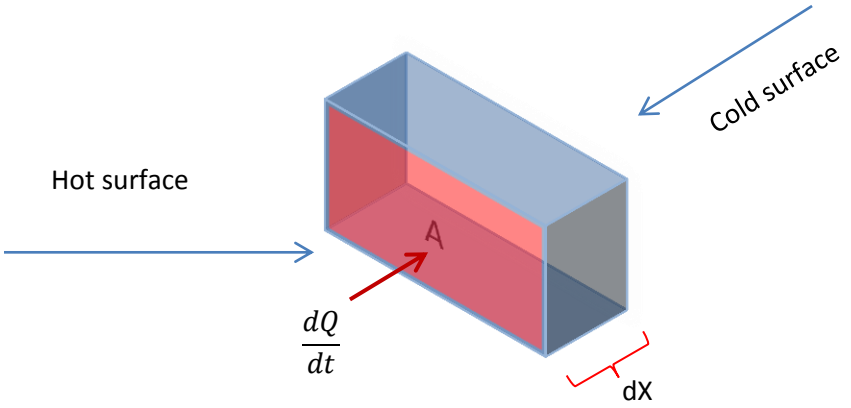


Figure 3 - Fourier law in 1D

$$\frac{\mathbf{dQ}}{\mathbf{dt}} = -\mathbf{K} * \mathbf{A} * \frac{\mathbf{dT}}{\mathbf{dx}} \quad (7)$$

where the parameters are shown on the Figure 3, the rate of the heat flow (dQ/dt) can be decreased by reducing the thermoelectric material cross section, A, between hot and cold surfaces. In addition, the longer the length of the support is, the lower would be the rate of the heat flow. In conclusion, a long silicon nanowire would be proper for the TE wire. There is also another important phenomenon that should be stated here. Silicon nanowires have electrical conductivity and Seebeck coefficient that do not vary from the bulk values, but their thermal conductivity is almost 100 times less than the bulk value [17].

Unfortunately, Silicon nanowires do not have enough mechanical strength to survive the fabrication process and they might break. Therefore, another material with low thermal conduction should support and protect the nanowires during the fabrication steps. Silicon dioxide and silicon nitride films have been used for the purpose of protecting different thermoelectric materials [18,19].

In our work Parylene has been used to support the silicon nanowires. Parylene is a polymer that has been used in printed circuit board industry and has a very low thermal conductivity ($\sim 0.1\ \frac{W}{m * K}$) [20]. Comparing the thermal conductivity of Parylene to silicon dioxide ($\sim 1 \frac{W}{m * K}$ for thickness larger than 250 nm) [21] and silicon nitride ($\sim 32\ \frac{W}{m * K}$) [22] shows that using Parylene as the supporting arms can substantially improve the detector performance (Actual values of thermal conductivity for the stated material may change with different thicknesses and the deposition techniques).

2.2.3 Absorber

Another important part of any thermal detector is its radiation absorber. High radiation absorption is necessary to produce large output signals. Different materials and structures have been proposed and used for the absorber. Metal-black coatings such as gold-black, silver-black, platinum-black, etc. have been used by researchers and companies for years [19, 23, 24]. Most of the metal-black coatings are deposited using evaporation technique at high nitrogen pressure. Among the coatings, gold-black has relatively low density, low reflection, and high thermal conduction. If the Au-black is deposited thick enough, the transmittance would be also zero and hence the incident radiation would be fully absorbed. In addition, it can be used for a wide range from 1 um to 50 um wavelengths range [23]. The reflectance spectrum of an Au-black coating is shown in Figure 4.

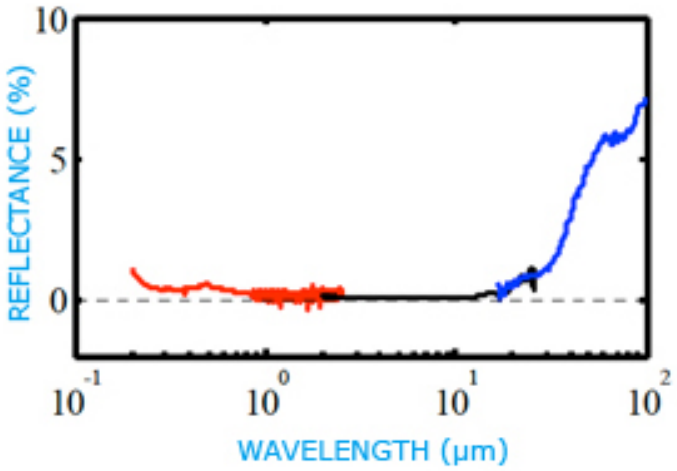


Figure 4 - Reflectance measurements of an Au-black coating for 25um thick film [25]

Unfortuantely, the gold-black coatings can be easily scratched, damaged and destroyed with a physical contact, air flow and/or if they become wet [23]. Therefore, it is very hard to pattern the deposited film and it has to be the last step in the fabrication process. Usually proximity masks [26] or laser trimming is used to pattern the film. Overall, consistency is a problem in using gold-black coatings.

Silver-black is also can be deposited in high argon pressure [27] and it also has low reflectance. One advantage of silver-black over gold-black is that it is more mechanically stable and scratch resistant [23].

Other black coatings like graphite-black, catalac-black, etc. can also be used as an absorber material but when the absorber size is so small like 80 um * 80 um, it would be difficult to pattern them and if there is an array of detectors that are closely fabricated, thick coatings can connect the adjacent absorbers to each other and reduce the final image resolution.

Optical cavities are also being used to maximize the absorption of the incident radiations. Two different optical cavity designs are shown in Figure 5 [28].

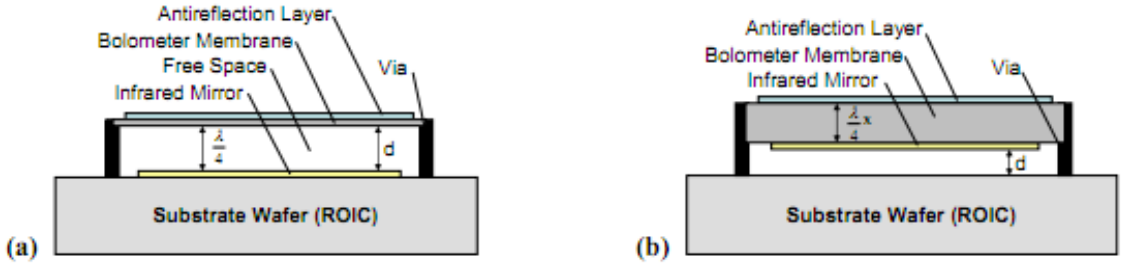


Figure 5 - Two different optical cavity designs to improve infrared absorption

It has been shown that in a metal – dielectric – metal configuration with two different metals of different thicknesses, high absorption can be achieved [29].

In our work, configuration Figure 5 (b) is chosen due to ease of fabrication. The top and bottom metals are made out of nichrome (Nickel 80% - Chromium 20%) and the dielectric material is silicon nitride.

Metals usually have high reflection because of their high refractive index. To increase the absorption or lower the refractive index, the metal layer should become thin [29,30]. At normal incidence to the surface, reflectance, R, can be calculated using Fresnel equations.

$$\mathbf{R} = \left(\frac{\mathbf{n_1 - n_2}}{\mathbf{n_1 + n_2}}\right) * \left(\frac{\mathbf{n_1 - n_2}}{\mathbf{n_1 + n_2}}\right)^{*} \quad [31] \tag{8}$$

As an example, at the interface of air ($n_1 = 1$) and copper ($n_2 = 10.8 + j\ 47$ at9.5 um [32]), 98% of the incident radiation will be reflected.

In the infrared region, refractive index can be approximated by

$$\mathbf{n} = \mathbf{k} = \left(\frac{\boldsymbol{\sigma}}{\mathbf{2 * \omega * \epsilon_0}}\right)^{.5} \tag{9}$$

Where k is the extinction coefficient, σ is electrical conductivity, ω is the incoming light frequency in radian, and finally $\epsilon_0 = 8.85 * 10^{-12}$ is the vacuum permittivity [29]. Therefore,

based on the above equation, if the metal film thickness is reduced, its sheet resistance ($\frac{1}{\sigma}$) increases and hence the final refractive index will be lowered. As a result, the reflection is lowered.

If a ray can make into inside of a metal film, it will be absorbed since metals are generally good absorber because of their large extinction coefficient but if they are made very thin, the ray may go through the film without being absorbed, therefore, the optical cavity is required to make multiple passes for any ray to assure its absorption.

2.3 Sensor structure and simulation

2.3.1 Detector structure

There are two main structures for thermal detectors. The one which is shown in Figure 6 is called a single level detector design which is mostly used for resistive bolometers. A membrane is raised and supported with two legs.

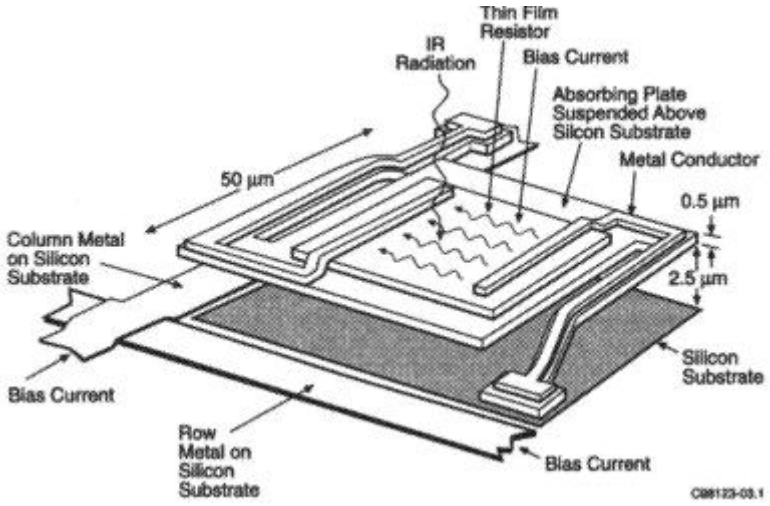


Figure 6 - The membrane structure [33,28]

There is also another design which is called umbrella design and provides a better fill factor. Fill factor is defined as the absorber area to the total area occupied by the detector. This design is shown in Figure 7 [34].

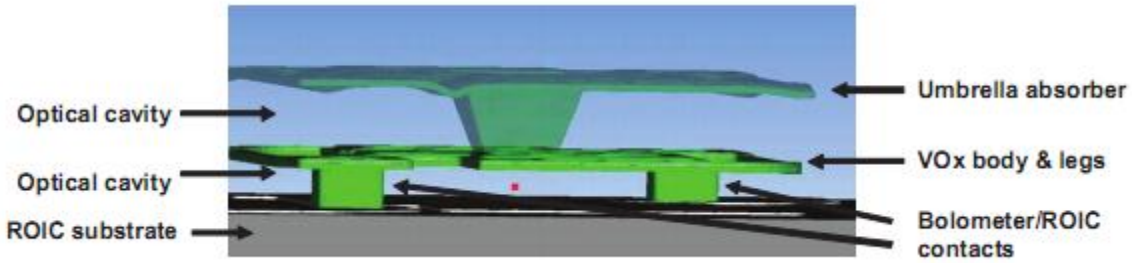


Figure 7 - DRS umbrella design [34]

In our research, umbrella design structure is used which helps to achieve high fill factor and to squeeze more detectors in a specified area. The detector schematic is shown in Figure 8.

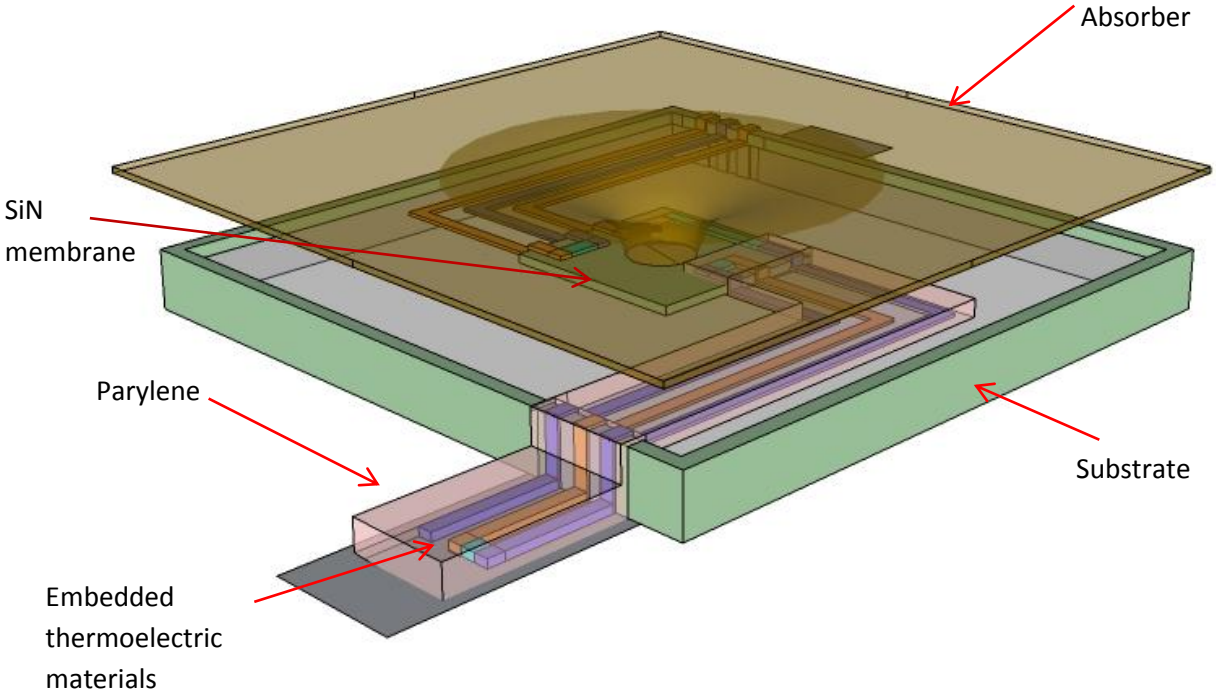


Figure 8 - The schematic view of the detector

The absorber is spread out over the detector area and is connected to a silicon nitride membrane through a post. The silicon nitride membrane is the hot element and because of its high thermal conductivity, its temperature would be the same as absorber temperature. Supporting legs are made out of Parylene because of its low thermal conductivity. Thermoelectric wires that are

enclosed in the Parylene arms are running from the substrate (or cold junction) to the suspended silicon nitride membrane (or hot junction) and then coming back to the substrate again. The substrate is a thin layer of silicon nitride on a silicon wafer. Doped silicon wafers may short the thermoelectric wires together and to avoid this, a thin layer of silicon nitride can be deposited to provide electrical isolation. Undoped silicon wafers can also be used as the substrate but they are very expensive.

2.3.2 Simulation results

Heat distribution in the detector which is simulated using COMSOL software can be seen in Figure 9.

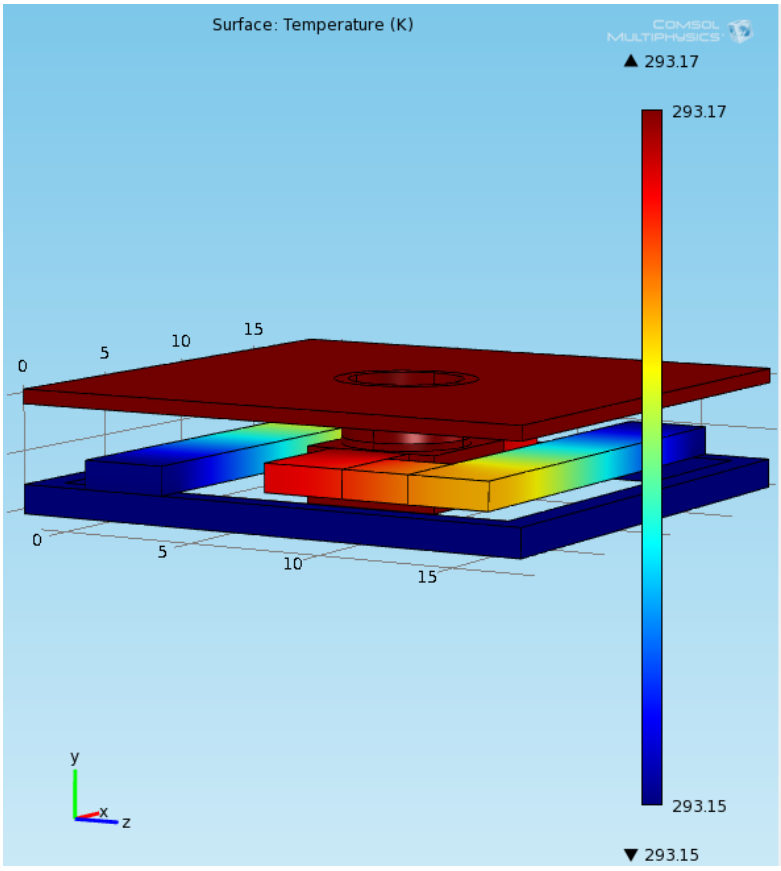


Figure 9 - Heat distribution in a pixel

The incident radiation is absorbed by the absorber and causes the temperature of the absorber to increase. Substrate which is shown in blue is still cold and because of its relatively infinite thermal mass with respect to the detector, it will always stay cold. The thermoelectric materials will convert this temperature difference between the absorber and the substrate to an electrical signal.

Assume that there is a short radiation pulse which causes the absorber temperature to increase 0.5 ℃ to become 293.65 ℃. Hot absorber loses its temperature in some time and becomes equal to substrate temperature again. This duration is called the response time of the detector.

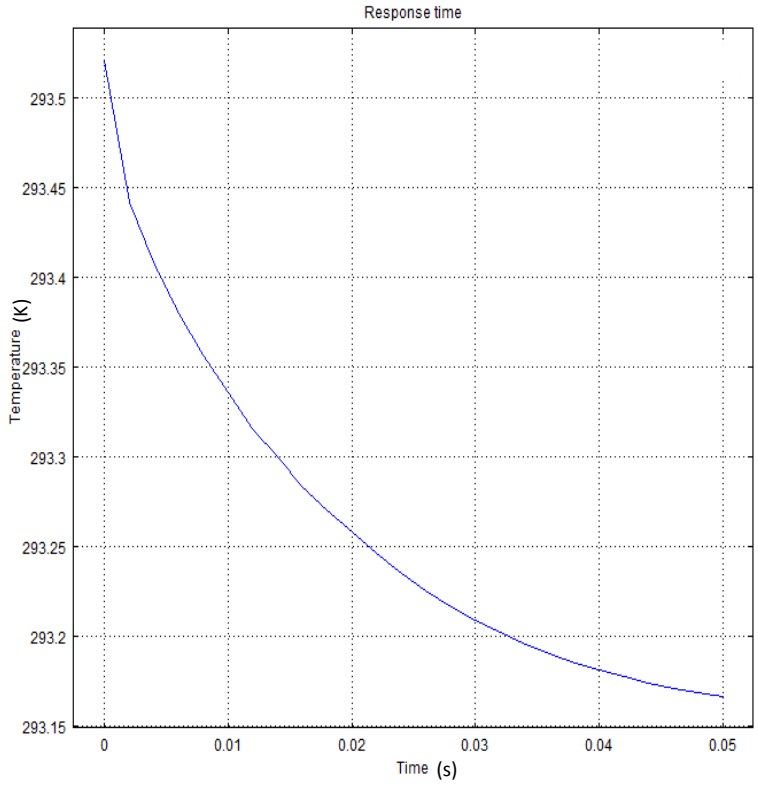


Figure 10 - Response time of the detector

The response time of the detector is also simulated in COMSOL and plotted in Figure 10. With changing the cross section of the Parylene supporting arms, faster or slower response time can be achieved.

CHAPTER III

Fabrication of the thermoelectric detector

Different detector structures have been discussed in the previous section. In this chapter, process flow and the fabrication steps are discussed. Practical problems are described in detail and possible solutions are specified.

3. 1 Process flow

Prototype devices with various absorber sizes and different number of thermocouple junctions have been fabricated using a 7-step surface-micromachining process which utilizes two sacrificial layers and is schematically represented in Figure 11. This process begins with the deposition of a sacrificial PECVD SiO_2 layer, which is patterned to serve as the platform for the suspended heat-collector. Silicon nitride is then deposited and patterned by dry etching to serve as an insulation layer for the electrical connections on top of both the substrate and the heat-collection post in the middle (Figure 11 (a)).

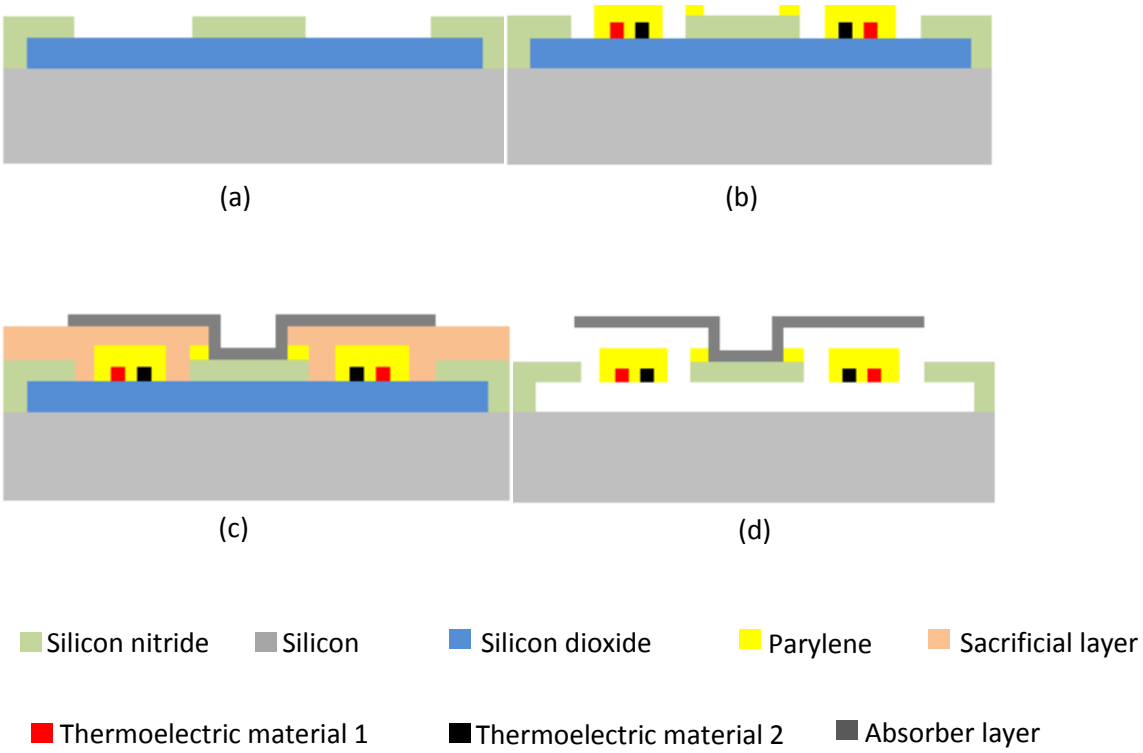


Figure 11 - The fabrication process flow

Next, the TE junctions are formed by sputtering/patterning two different metallic traces and then the Parylene film is deposited in a Parylene-coating chamber at room temperature and is consequently patterned in O_2 plasma (Figure 11 (b)). The absorber is then formed and patterned to create access to the bottom silicon nitride post (Figure 11(c)). The heat-collector (Cu) is then deposited/ patterned and is anchored to the post through the patterned hole in resist. At last, both sacrificial layers are removed to completely release the structure (Figure 11 (d)). The described steps will be described in details in the rest of this chapter.

3.2 Fabrication step

3.2.1 Sacrificial layer deposition\patterning

The fabrication process begins with a single side polished silicon. The wafer is cleaned prior to any deposition to make sure that it is free of any contamination. Any contamination may cause some unknown effects and undesired film formation in the later steps.

There are different choices of sacrificial layers. Polymers such as photoresist can be used as a sacrificial layer but they are not suitable for high temperature processes since they might burn. Some polymers can tolerate high temperature but ash technique which is used for removal is harmful to Parylene films which itself is a polymer. Other sacrificial layer like silicon dioxide, silicon nitride, polysilicon, etc. can also be used but except silicon dioxide, other materials either hard to remove or their etchant attacks other material on the wafer. Silicon dioxide can be etched in Hydrofluoric solutions (HF). The HF solution slightly attacks Parylene and silicon but this is not the concern here, the important is that it strongly attacks oxide and gives a good selectivity.

After cleaning, sacrificial oxide is deposited. This can be done either in oxidation furnace or PECVD. PECVD oxide is preferable because this film will be removed later on and has higher etch rate in the etchant comparing to the thermal oxide. Also the oxide deposition rate in PECVD (2 um per hour) is much higher than the frowth rate in furnace (more than 8 hours for 2 um).

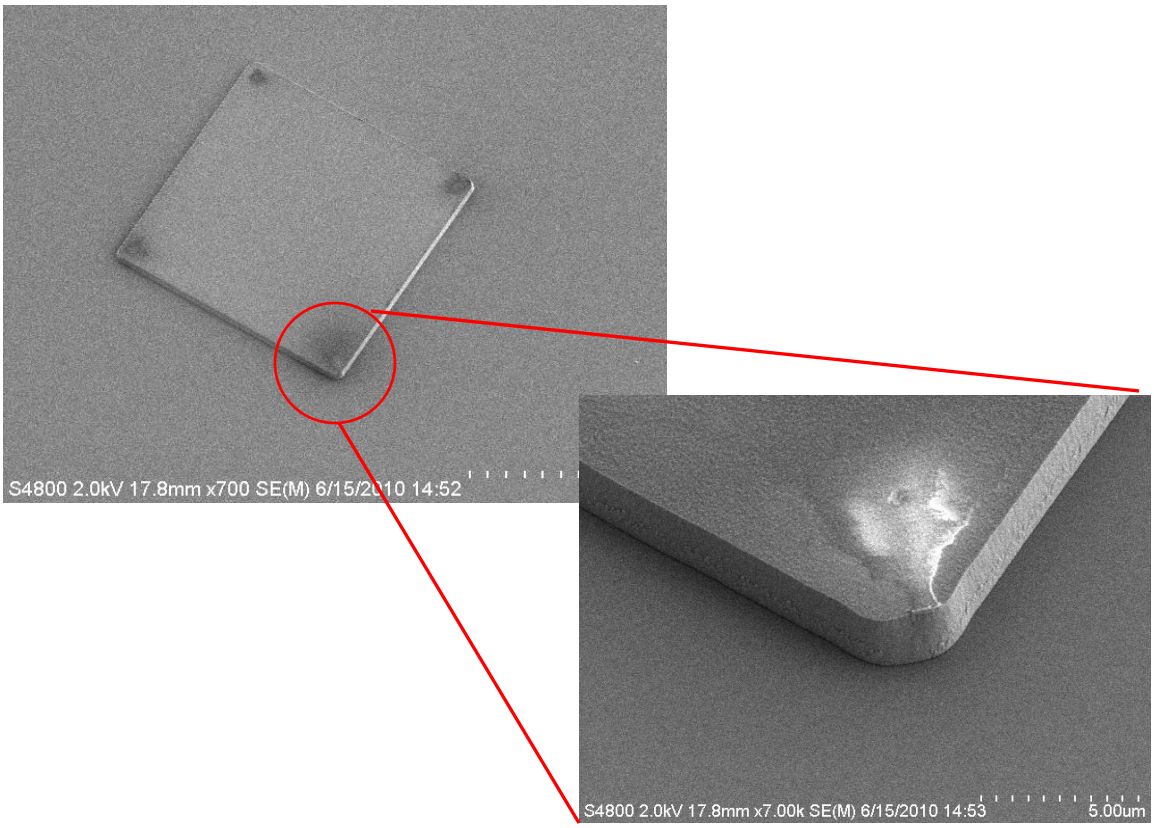


Figure 12 - SEM showing the etched oxide step

Figure 12 shows the SEM of the oxide sacrificial layer after dry etching in ICP. It should be also noted that in ICP or any dry etching, the sidewalls are very steep. This may cause discontinuity in thermoelectric traces in future steps. To change the sidewall slopes, the mask should have sloped sidewalls. If the photoresist is used as the mask, it can be reflowed by baking it at 150°C.

3.2.2 Electrical insulator layer deposition\patterning

Undoped silicon wafers can be very expensive and doped ones may short the thermoelectric traces to each other and cause malfunction. To avoid this, a thin layer of an insulator material should be deposited. This layer will not be removed and should not be etched in HF solution. Silicon nitride is the choice of option since it can tolerate high temperature, it is slightly attacked in HF, and it can be deposited with the common IC fabrication tools. Another requirement is that

the insulator film should have high thermal conductivity to dissipate the transferred heat from the hot element quickly. Silicon nitride has high thermal conductivity [22] and can rapidly conduct any local heat to the other cold areas.

Silicon nitride was chosen because it could be deposited using PECVD and has high deposition rate. Upon different parameters in the process, the deposited film may have different etch rates [35]. A recipe was developed to produce films with low stress and low etch rate in BOE and is shown in Table 2

Temperature (C)	$\mathbf{SiH_4 + He}$ (sccm)	$\mathbf{NH_3}$ (sccm)	He (sccm)	$\mathbf{N_2}$ (sccm)	RF power (watts)	Process pressure (mTorr)
300	1600	5	1200	450	80	750

Table 2 - Nitride deposition recipe

After nitride deposition, the film should be patterned to form a SiN membrane on the center of the sacrificial oxide which will act as the hot junction as shown in Figure 8.

For patterning the nitride, phosphoric acid should be used for the wet etching process. However, phosphoric acid attacks the photoresist and hence, photoresist cannot be used as a mask. Dry etching is another option which can be done by using the same recipe as oxide etching and since the selectivity of photoresist over nitride is 1 to 2, the photoresist can be used as the mask. The result after etching is shown in Figure 13.

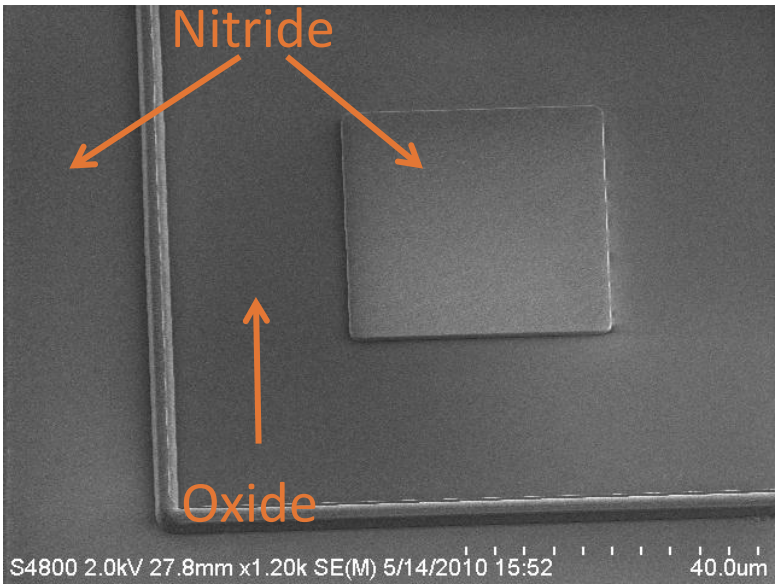


Figure 13 - SEM of a device after patterning the nitride layer

The next step after electrical insulator deposition (or SiN) is polysilicon deposition for the thermoelectric material. Polysilicon deposition is carried out in a furnace which requires 600°C. PECVD nitride cannot withstand that high of a temperature and cracks. Therefore, a substitution is required with thermal and chemical properties close to silicon nitride.

Aluminum nitride (AlN) has high thermal conductivity (320 $\frac{W}{m*K}$ [36]), high melting point, inert to the solvents and etchants and can be deposited by the sputtering method. Aluminum nitride etch-rate in its etchant which is TMAH (Tetramethylammonium hydroxide) and hydrofluoric acid (HF), strongly depends on its quality. TMAH is important because it is the solution which is used to develop (or pattern) the photoresist after the exposure. The etch rate in TMAH should be minimized to prevent undesired undercuts. Various films with different recipes were deposited and their quality was measured with X-ray diffraction (XRD) technique. FWHM or full width half maximum of the rocking curve is the figure of merit that shows how well the crystallites inside a film are aligned in one direction. The FWHM can be calculated by integrating a 2D detector data over chi axis.

Most of the sputtered film exhibit etch rate as low as 0.5 $\frac{\text{nm}}{\text{min}}$ in BOE 5:1 (BOE or buffered oxide etchant is a solution that contains HF as well as buffered agents and surfactants for more controllable etching) but they have high etch rate in TMAH which is extremely undesired. One way to get over this problem is that to use other photoresist developers that are not based on TMAH. This also has been tried and the films were also attacked by those developers but milder than TMAH. However, their undesired effect could be minimized by timing the developing process.

The XRD of the best produced sample is shown in Figure 14. There is a peak around 35 degrees which is corresponding to the AlN 002 plane. This peak is on the right side of the reference which shows that the film has tensile stress.

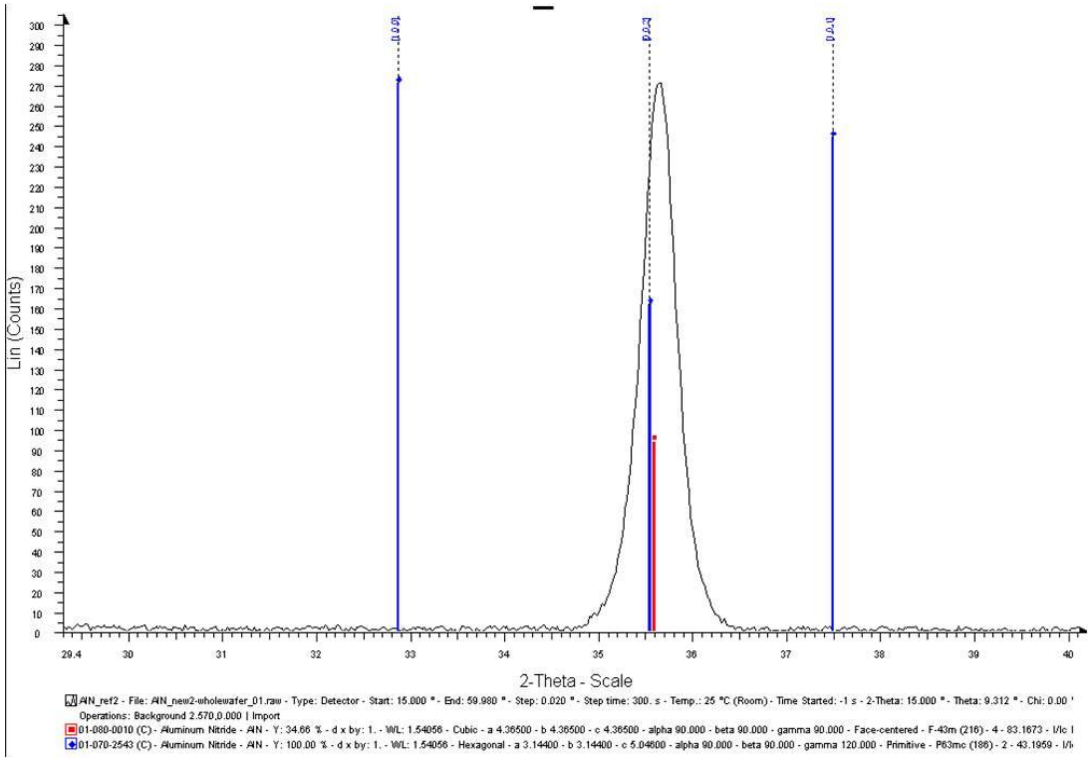


Figure 14 - X-ray diffraction of AlN shows tensile stress in the film since the AlN peak is on the right side of the reference

To make sure that this film can withstand high temperature processes, the film was annealed at 800 °C for 3 hours. The XRD of the film after annealing is shown in Figure 15. The film still shows tensile stress.

Inconsistency in the properties of the sputtered AlN films is another issue that should be addressed here. Chamber condition, previous coatings, base pressure, etc. cause the quality of the films to vary from one to another. Also the deposition rate is low comparing to PECVD and batch fabrication is not possible since the tool can process one wafer at a time. Further on, Parylene does not adhere well to AlN which is a challenging problem.

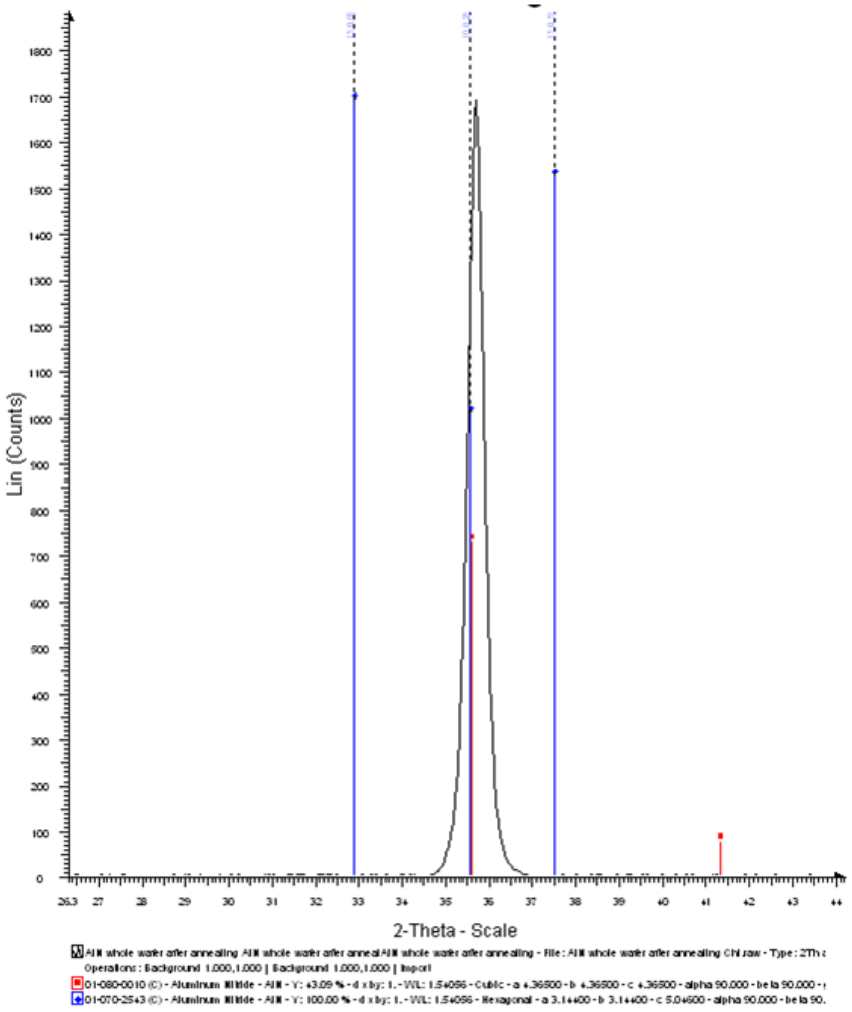


Figure 15 - X-ray diffraction of the film after annealing showing that the film is still tensional

These problems cannot be resolved easily. Thus, it was decided to use low stress silicon nitride instead. Low stress low pressure chemical vapor deposition (LPCVD) silicon nitride is deposited at $850°C$, shows low etch rate in BOE and can easily withstand high temperature processes such as polysilicon deposition.

3.2.3 Thermoelectric wires deposition and patterning

Thermoelectric wires are required to generate voltage due to the temperature difference on their ends. Among metals, Bismuth's Seebeck coefficient is relatively large. Therefore, it was tried to deposit Bismuth by thermal evaporation technique. Lift-off process was used to pattern the evaporated film. As it can be seen in Figure 16, the bismuth traces have adhesion problem and they do not stick well to the underneath layer.

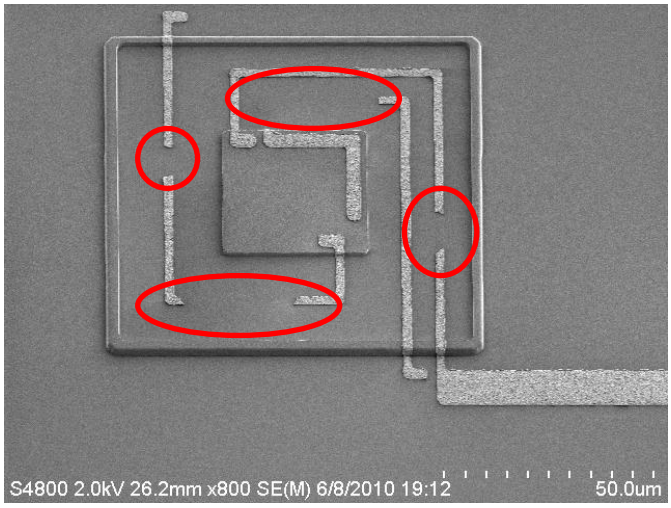


Figure 16 - Bismuth evaporated film after lift-off

The adhesion problem can be solved easily by depositing a thin layer of Chromium or Titanium prior to bismuth deposition. Chromium is preferred because it is not etched in BOE as opposed to titanium. There is still another problem and that is the step coverage of the evaporated bismuth

film on the sidewalls. Evaporation technique is directional and it usually does not provide any film on the steep sidewalls. Therefore, in the nitride etching step, the slope of the sidewalls are decreased by post baking the photoresist at high temperature and causing it to reflow before etching the film in ICP(dry etching). However, the problem is not completely resolved and the evaporated film does not cover the sidewalls with uniform thickness. It was decided to use sputtering technique instead of thermal evaporation. In general, sputtering provides better sidewall coverage. The difference in the sidewall coverage between sputtering and thermal evaporation can be seen in Figure 17.

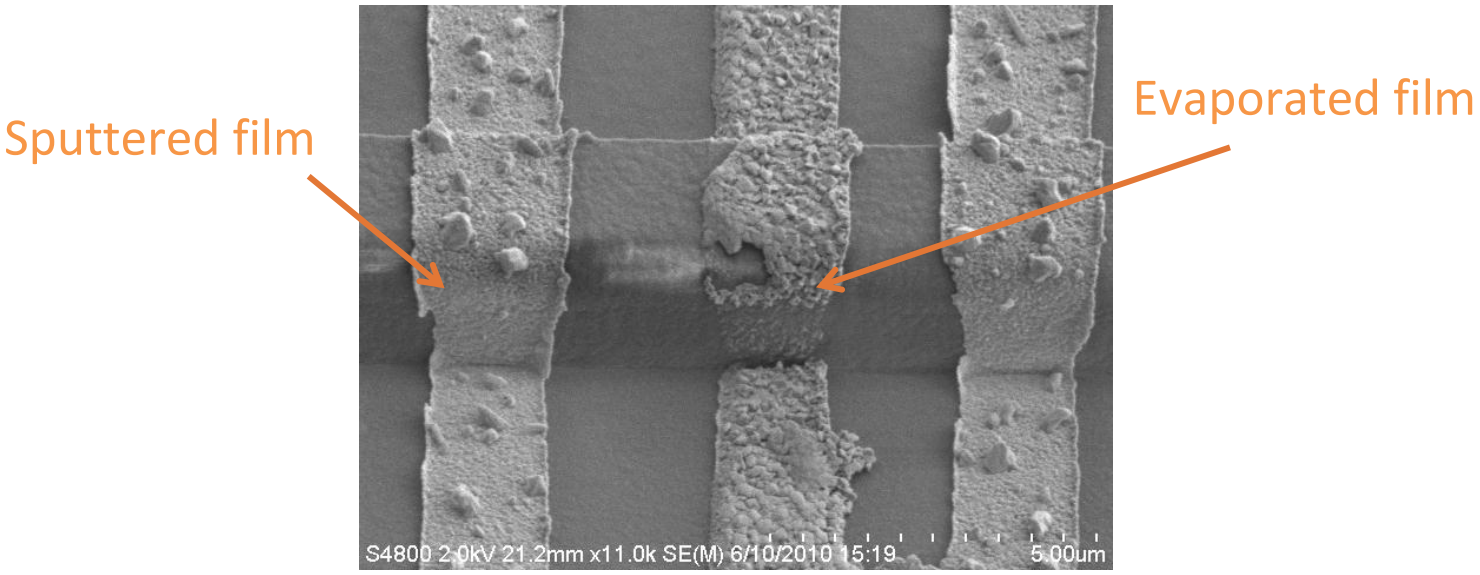


Figure 17 - sidewall coverage in sputtering vs. evaporation

To try the fabrication process and see if the proposed process flow works, Molybdenum was chosen as the second thermoelectric material to make a complete device. The result is shown in Figure 18.

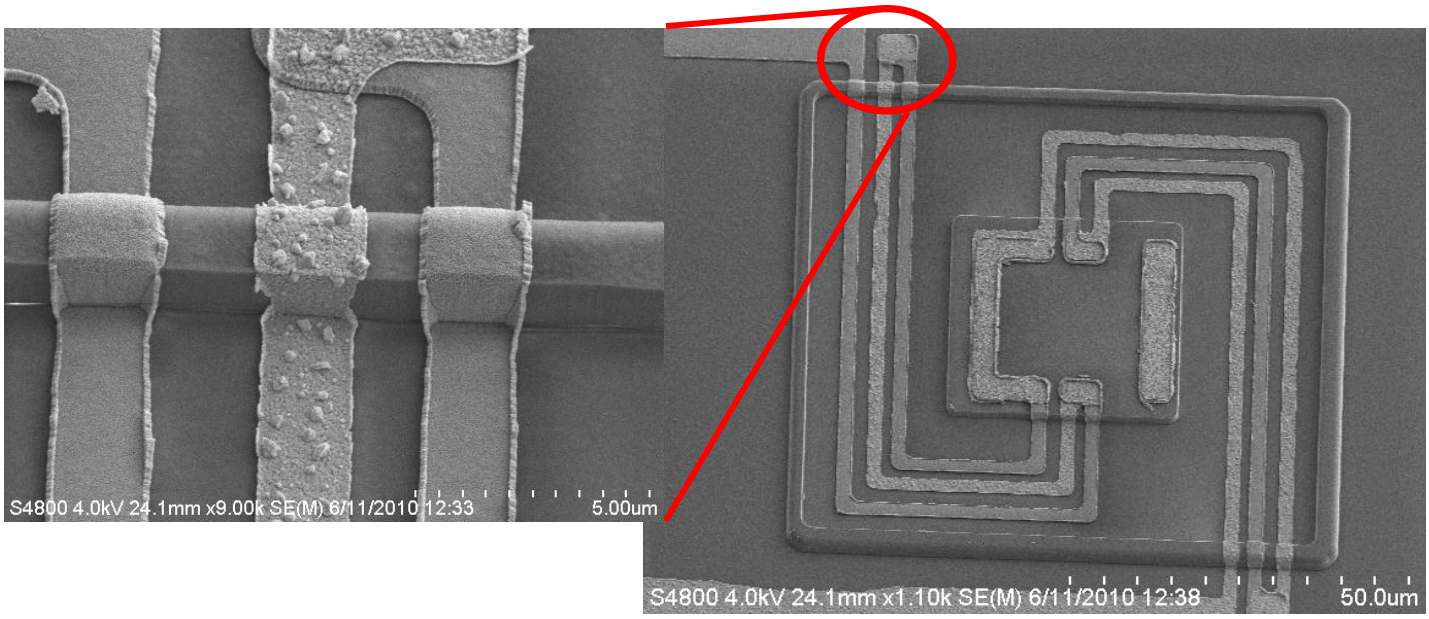


Figure 18 - Top view of the sputtered thermoelectric wires after lift-off

After making the devices with two metal thermoelectric wires, it is time to change one of them to polysilicon since it has higher ZT. Polysilicon is deposited in a LPCVD furnace at 600 $°C$ which should be followed by annealing for dopants activation at 900 $°C$. Since this film is deposited at high temperature, lift-off is not an option because photoresists are polymers and they cannot withstand temperatures higher than 150C unless they are cured. If they are cured, they can no longer be removed in Acetone and another method which is called ash technique should be used for removal. So, the film has to be dry etched in ICP. Another consideration is that a recipe should be used for etching polysilicon that does not etch the underneath layer especially since polysilicon is thin and timing the process is difficult. This polysilicon layer is deposited over silicon nitride and silicon dioxide. Thus, a great selectivity is required. In addition, the etching

should be isotropic and a great undercut can be attained and hence, the width of the wire can be controlled. Thus, a recipe was developed based on SF6 plasma for etching the polysilicon layer.

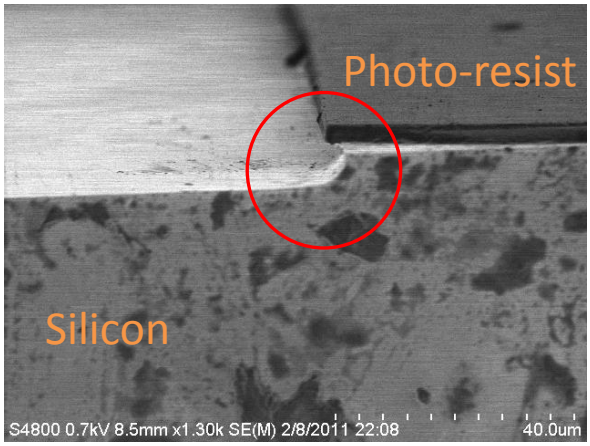
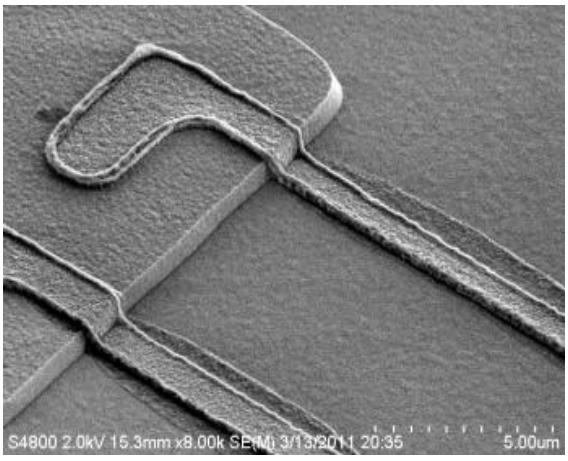
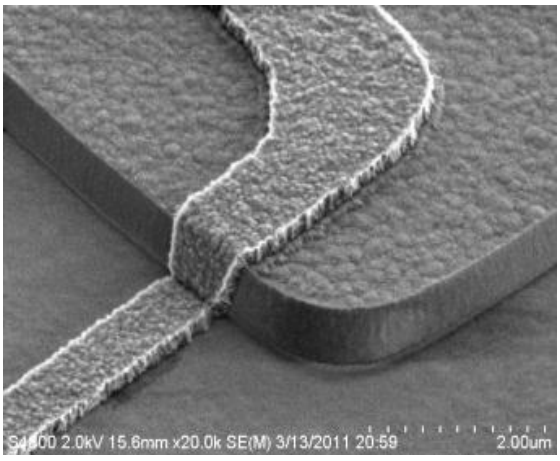


Figure 19 - SEM showing etched silicon and the formed undercut underneath the photoresist mask

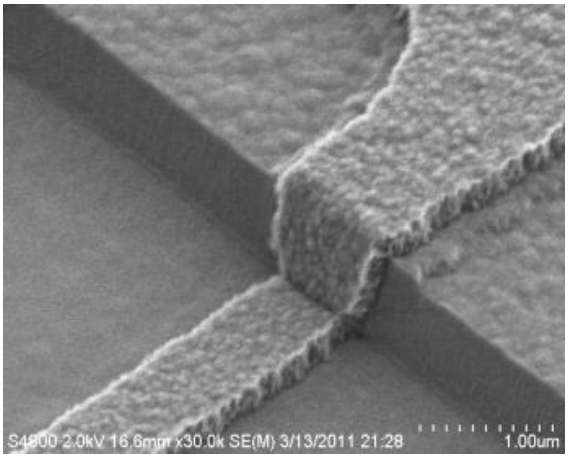
In the developed recipe the etch-rates of photoresist, silicon dioxide and polysilicon are 85, 43, and >1000 nm/min respectively. The undercut can be clearly seen in Figure 19. This method was used to create wires with different widths and the fabricated wires are shown in Figure 20.



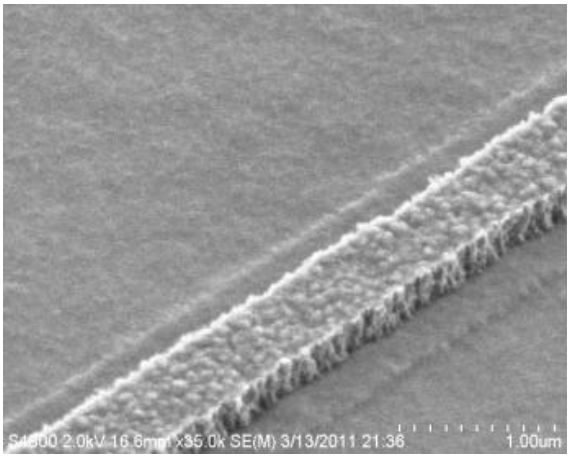
A) Polysilicon wires after etching for 15 seconds



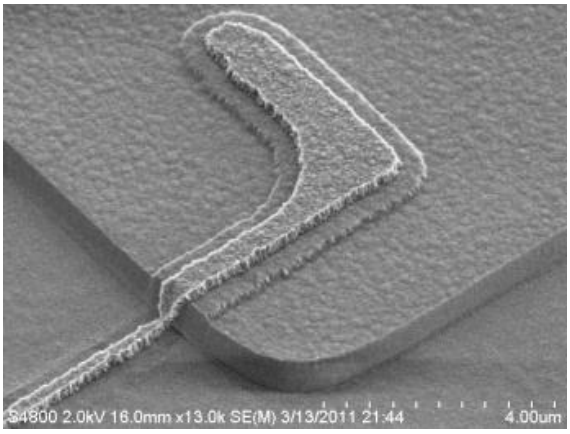
B) Polysilicon wires after etching for 35 seconds



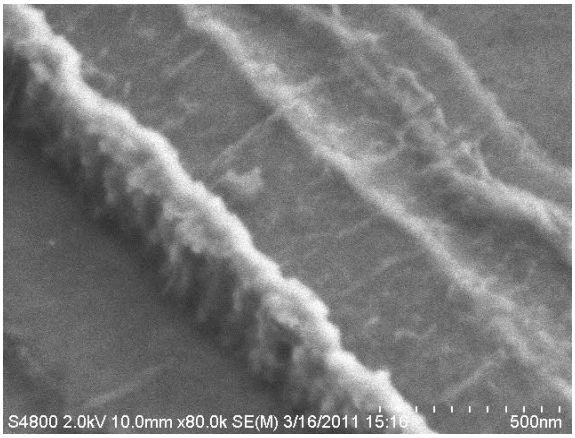
C) Polysilicon wires after etching for 60 seconds



D) Polysilicon wires after etching for 80 seconds



E) Polysilicon wires after etching for 100 seconds



F) Polysilicon wires after etching for 120 seconds

Figure 20 - SEMs of the fabricated wires showing the wire width reduction versus time etching time

The described technique was used to fabricate a complete device and it is shown in Figure 21.

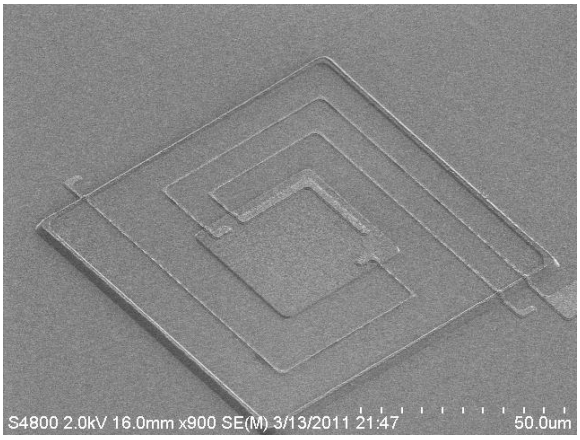


Figure 21 - SEM of a complete etched device after etching for 100 seconds in ICP

The only problem that was observed with this technique was that the widths of the wires on the sidewalls were much smaller than other places. In other words, the polysilicon etch-rate on the sidewalls is more than the flat surfaces. This non-uniform etching can be taken care of by changing the wire patterns. Thus, in the design step, wires with larger widths on the side walls are drawn.

3.2.4 Parylene deposition and patterning

Parylene is deposited at room temperatures with Specialty Coating Systems (SCS) tool. The thickness of the result film depends on the amount of the loaded dimer. Parylene-C with different thicknesses were deposited and patterned. Oxygen based plasma is used to etch the Parylene film in ICP. Since photoresist is a polymer as well as Parylene, it cannot be used as a mask. Even if the thickness of the photoresist mask is chosen much thicker than the thickness of the Parylene film, the etched film result will not have sharp and good sidewalls. A hard mask such as silicon dioxide should be used. The fabrication result after patterning the Parylene film is shown in Figure 22.

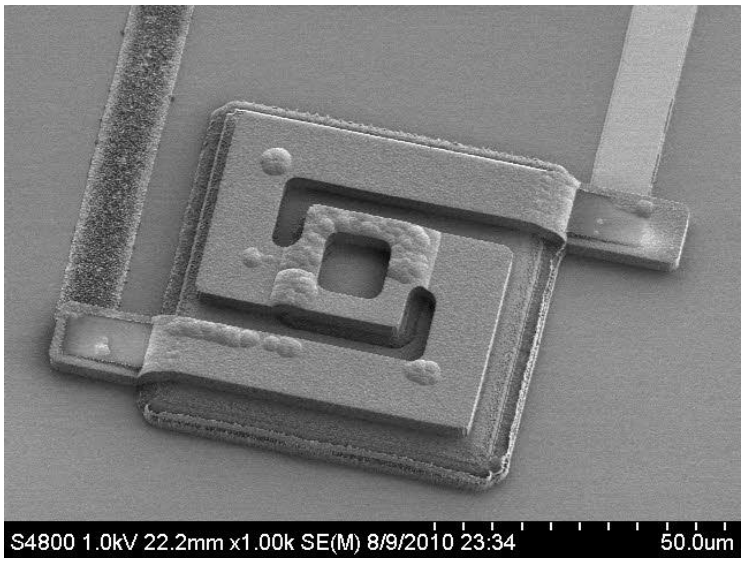


Figure 22 - Top-view of a device after etching Parylene

The next step in the fabrication process is absorber deposition. Since the absorber may be deposited at high temperature, higher than 300°C, parylene C is not proper because its melting point is 290°C. Parylene N has almost the same characteristic but it has higher melting point, 480°C. Thus, Parylene N films were deposited by acquiring the necessary dimer and applying some modifications inside the tool.

3.2.5 Prototype absorber fabrication

After etching Parylene, sacrificial layer for absorber should be deposited. Again, for the sake of simplicity, photoresist was used as the sacrificial layer and copper was used as the absorber material. As it was shown in Figure 11 (c), the sacrificial layer should be etched in order to gain access to the silicon nitride membrane. As a result, the absorber can be anchored to silicon nitride membrane through a post. Photoresist, the sacrificial layer, can be easily patterned for the post and then the absorber can be deposited at room temperature. If the temperature of the substrate rises during the absorber deposition, the post might crack and after releasing, the absorber would be detached. A SEM of the post after Cu deposition is shown in Figure 23.

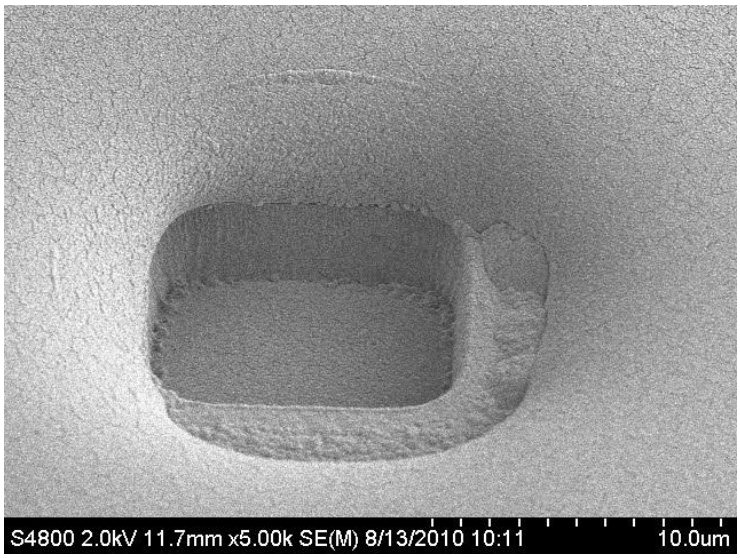


Figure 23 - SEM showing how the absorber is anchored to the post after sputtering

Different recipes for Cu sputtering were tried to avoid heat damage to the sacrificial photoresist. Among different parameters in the process, the applied power to the target had the greatest effect. By reducing this power, a uniform film with no heat damage to the sacrificial layer was deposited. This deposited film should be etched to form the absorber. This can be done by using a photoresist as a mask and wet etching the Cu film.

3.2.6 Releasing step

After patterning the absorber, the absorber and the device can be released by submerging the device in acetone to remove the sacrificial photoresist followed by BOE dip for removing the sacrificial oxide.

The final device after releasing is shown in Figure 24 and a side view is shown in Figure 25. The Parylene thickness is 1.4 um.

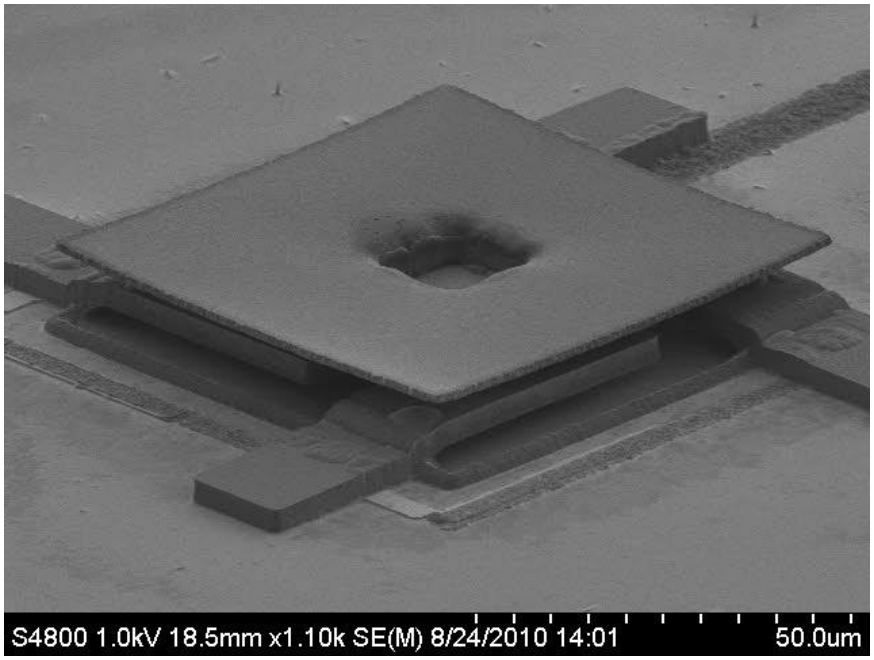


Figure 24 - The SEM of a fully fabricated device (Parylene thickness 1.4um)

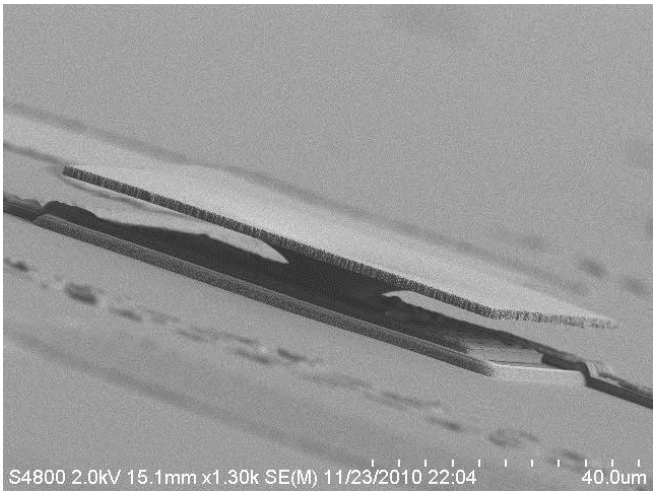


Figure 25 - A side view of a completed device

Devices with four arms could survive the releasing process. Devices with two arms, thinner Parylene, or long arms had stiction problem. In the final step, the whole wafer should be submerged in BOE to dissolve the sacrificial oxide to have free standing structure and then the

wafer should be washed and cleaned with DI water. This process can cause mechanical failure since it interacts directly with liquids. Next, assuming that no mechanical failure happens in this step, when the water dries out (since water has an asymmetric molecule which results in high surface tension) it causes the supporting arms of the devices to bend down and stick to the underneath surface as it is shown in Figure 26.

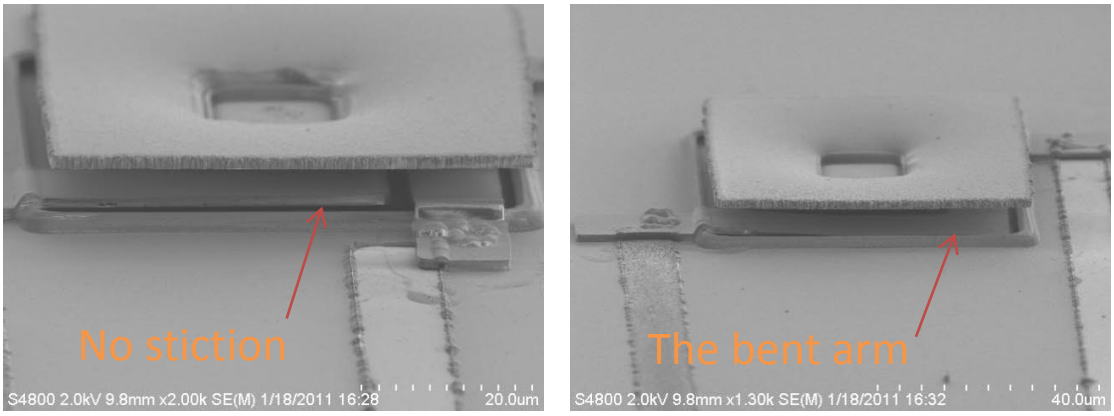


Figure 26 - SEMs comparing a device survived the release step and a device failed due to stiction

When a polar molecule like water is evaporating or removed from an area between two surfaces, the liquid surface tension forces the two surfaces to move towards each other and stick together. Hexan has a low polarity and can be used to replace the water and then wafer should be left to dry. This technique helps a little bit but the number of failures is still high. This can be avoided by using other releasing techniques like super critical drying, vapor phase etching, etc.

Vapor etching was chosen since it was the easiest one to try. The block diagram of the built setup is shown in Figure 27.

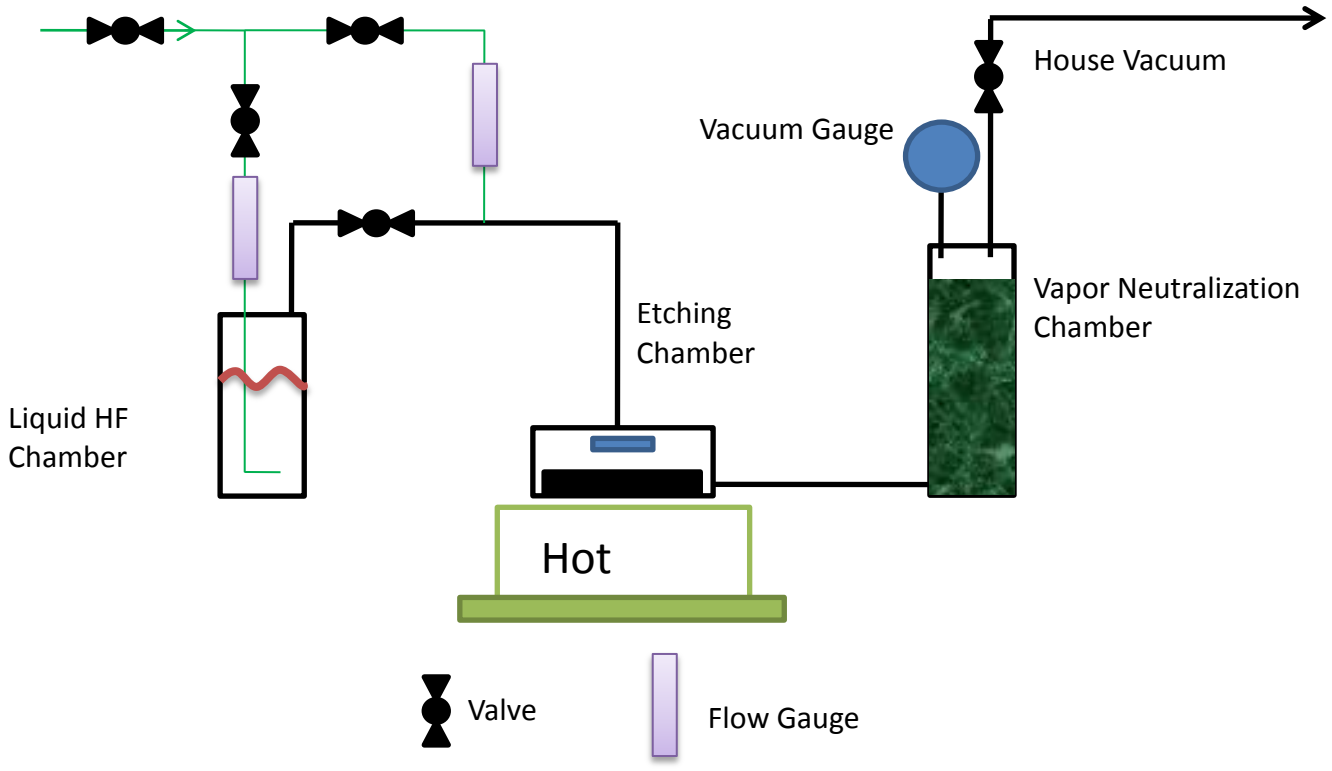


Figure 27 - Block diagram of the HF vapor phase etching setup

In the HF vapor phase etching, HF vapor is used to etch the silicon dioxide to avoid stiction. To produce HF vapor, N_2 is bubbled through liquid HF. The HF vapor with N_2 is passed through a chamber where the wafer is placed. The HF vapor etches the silicon dioxide, and the byproducts and the remaining gases are pushed to another chamber, neutralization chamber, in order to consume the remaining HF vapor before releasing to the pump.

Silicon dioxide etching needs water vapor to initiate the process. Thus, the etch rate depends on water vapor concentration on the wafer surface. However, a large amount of water vapor may cause condensation on the wafer surface and this would cause stiction again. To reduce the amount of condensation, the wafer should be heated but heating causes less water molecules on the surface and reduces the etch rate, and therefore the temperature should be carefully chosen

[37, 38]. The nitrogen flow should be also controlled because it can change both water and HF concentration.

The built setup is made out of plastic and PVC which both are inert to HF vapor. The setup is shown in Figure 28.

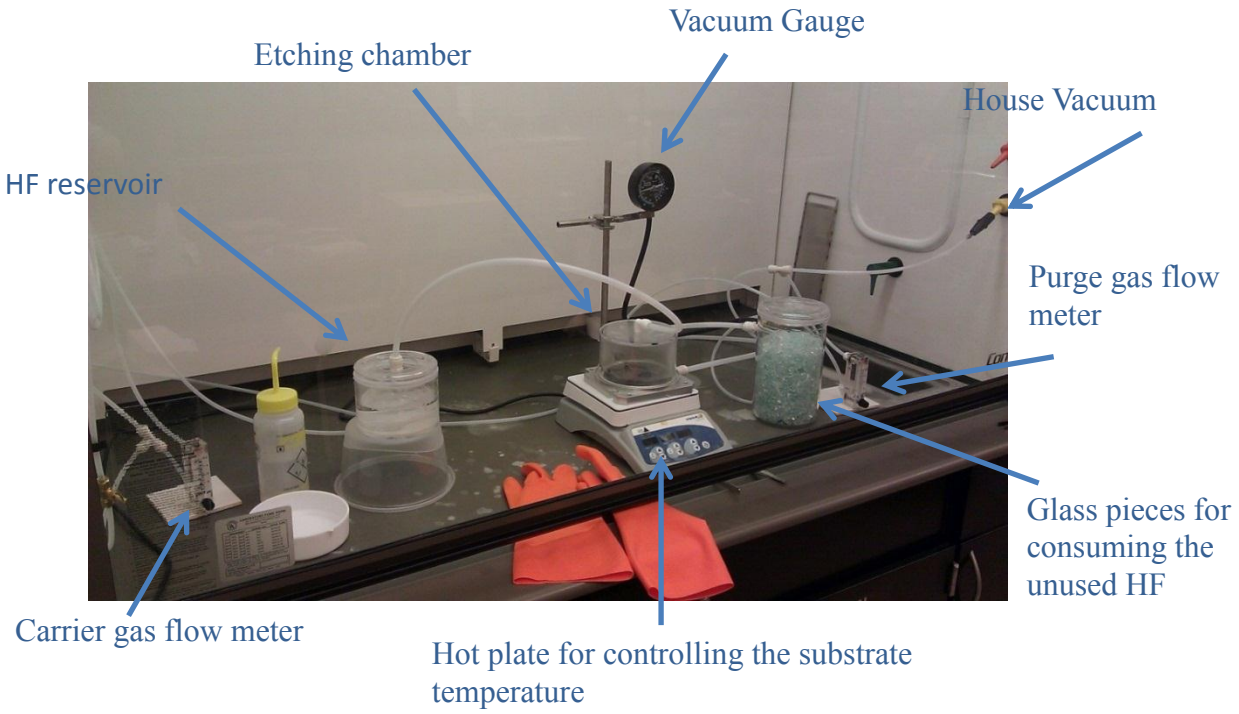


Figure 28 - HF vapor-phase etching setup

The setup was used to release some devices. It was observed that oxide leaves a residue which is not in a gas phase. The residue is shown in Figure 29.

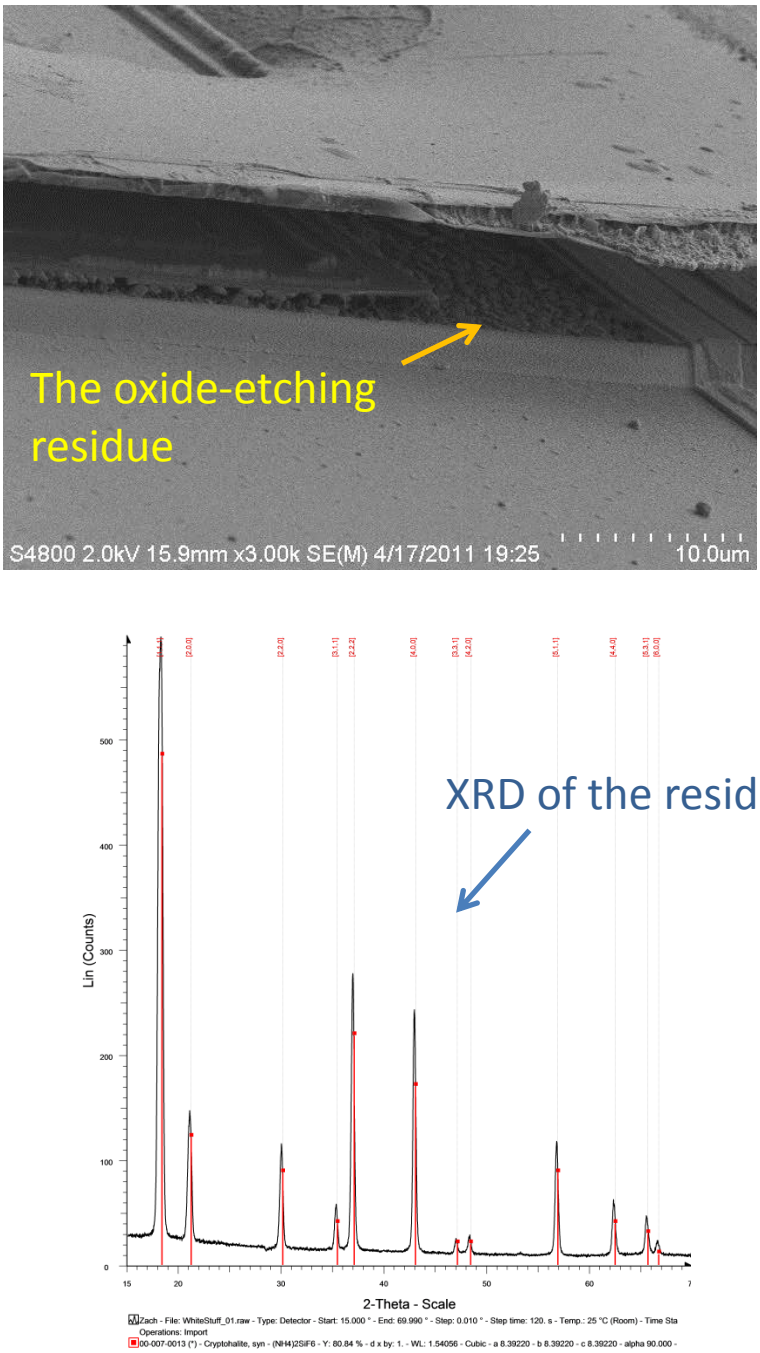


Figure 29 - SEM and XRD from the silicon dioxide HF vapor etched residue

The residue is seen only when PECVD oxide is being etched. If thermal oxide is etched, all oxide will be etched and there will not be any residue. The residue was collected and identified as Cryptohalite (ammonium fluorosilicate $(NH_4)_2SiF_6$) by using XRD. This nitrogen in Cryptohalite comes from N_2O gas which was used for silicon dioxide deposition in PECVD and cannot be avoided.

To prevent the formation of this residue, thermal oxide can be used as the sacrificial layer. The only problem is that the etch rate of thermal oxide is much lower than the etch rate of PECVD oxide in any etchant. This causes a long exposure of components on the wafer to for example HF vapor and therefore some of them may be strongly attacked.

Cryptohalite is soluble in water. Therefore, the wafer can be rinsed with water after etching but this causes stiction again. Another option is to heat up the wafer after etching because Cryptohalite decomposes at temperatures higher than $100°C$. Therefore, it was decided to release the devices in HF vapor and then bake them to remove the residue.

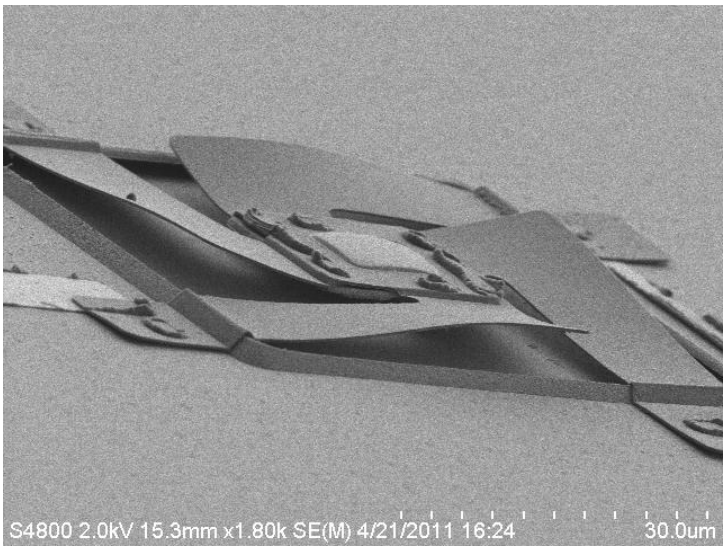


Figure 30 – A SEM showing a device released in HF vapor and baked after

This SEM (Figure 30) is showing how the device is completely released without stiction. As it is apparent from the SEM, due to internal stress of the Parylene film, supporting arms are bent upwards. To avoid this problem, the film was annealed at 130°C for an hour before releasing and then the device was released in HF vapor but it wasn't helpful.

To avoid the last step baking, it was decided to release the devices from the backside of the wafer. There are two known ways to etch a wafer from the backside. One way is Bosch process or DRIE (deep reactive ion etching) which results to steep side walls. The other way is anisotropically wet etching with KOH or TMAH. For this process, larger holes on the backside are required. Both of the techniques were pursued to release the devices.

After completing a process on the wafer, the front side was protected with 2 um of PECVD oxide for wet etching the backside. After an hour of etching in TMAH, it was observed that the front side has been attacked and the polysilicon wires were wiped off the front surface. Apparently, PECVD oxide is not a good protecting mask. Another protective layer, Protek, was added to the front side and etching lasted for 6 hours. Figure 31 shows a SEM from a device etched from the back in TAMH. The front side is released after in HF for 5minutes.

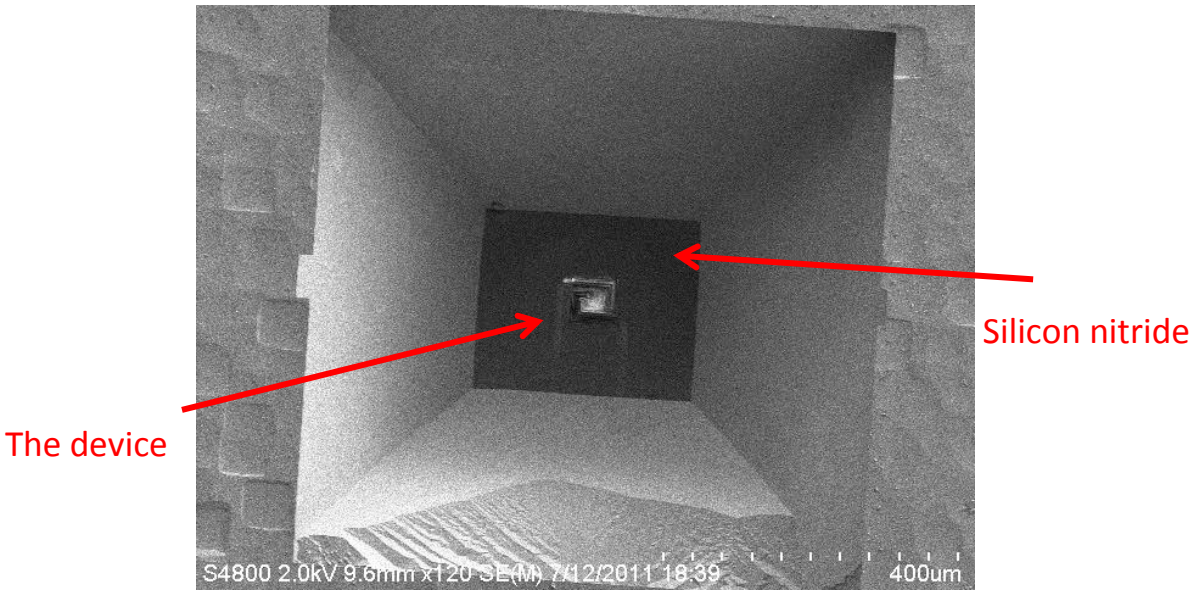


Figure 31 - A SEM from a device (backside view)

As it is evident in the above SEM, since the TMAH etching of silicon is anisotropic meaning that the etch rate is not equal in different planes, the right size of the backside hole should be used. TMAH etch rate on the silicon (111) plane is very low [39]. Since the wafer thicknesses might vary from one to another, the whole size should be changed or wafers with constant thickness should be used. Unfortunately, on the processed wafer, the hole sizes were miscalculated and the result was that the etched holes on the other side of wafer were much bigger than the devices and therefore none of the devices could be probed without breaking.

As it was described earlier, another way of backside etching is Bosch process (Deep reactive ion etching or DRIE). One wafer with polysilicon and molybdenum wires was processed to try back side DRIE. The wafer then was released in HF liquid. The result is shown in Figure 32.

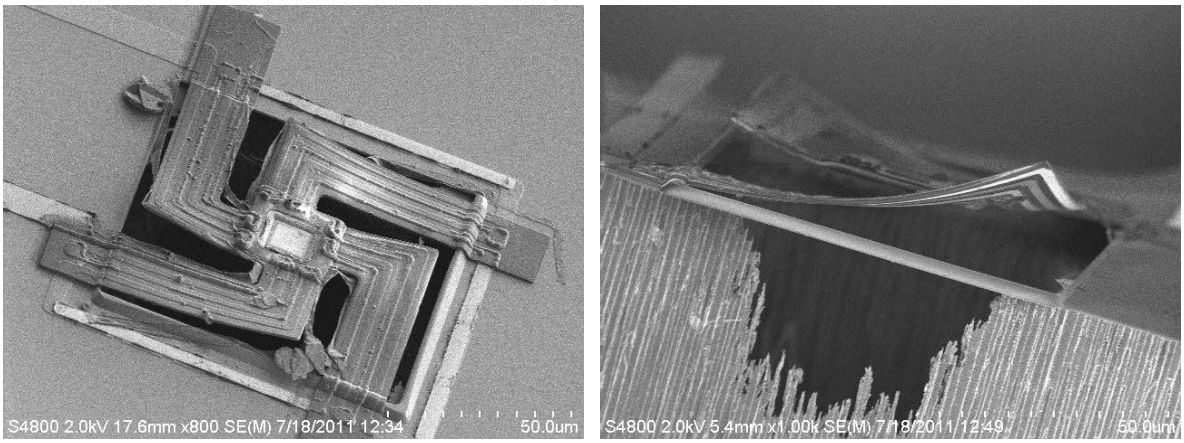


Figure 32 - SEM showing the released devices from the back, top view (left) and side view (right)

As it is noticeable in the above SEMs, the absorbers are broken. The author believes that this is because HF attacks the nitride layer and causes the absorber to peel off. The other point is that the Parylene arms are again bent upwards.

When the Parylene film goes under heat cycles, an internal stress will be induced. The author believes that the film eases the internal stress at the annealing temperature and the induced stress is the result of thermal coefficient mismatch between the Parylene film and the underneath layer [40]. It has been shown that at first, the deposited Parylene has tensile stress, but after a heat cycle, the stress will become compressive. Specifically, Parylene N goes under phase change at 250°C and 270°C which these phase changes will reduce the internal stress. To further lessen this stress, in any heat cycle, the sample should be slowly cooled down [41]. This induced stress is the result of thermal mismatch between the Parylene film and the underneath layer.

To overcome this arm bending problem, the size of the detectors were reduced to 20 um * 20 um instead of 80 um * 80 um. In addition, to understand the effect of the film stress, two devices were prepared with two different conditions. One of the devices was baked and then released in HF vapor and then the other one was first released and baked. The result is shown in Figure 33.

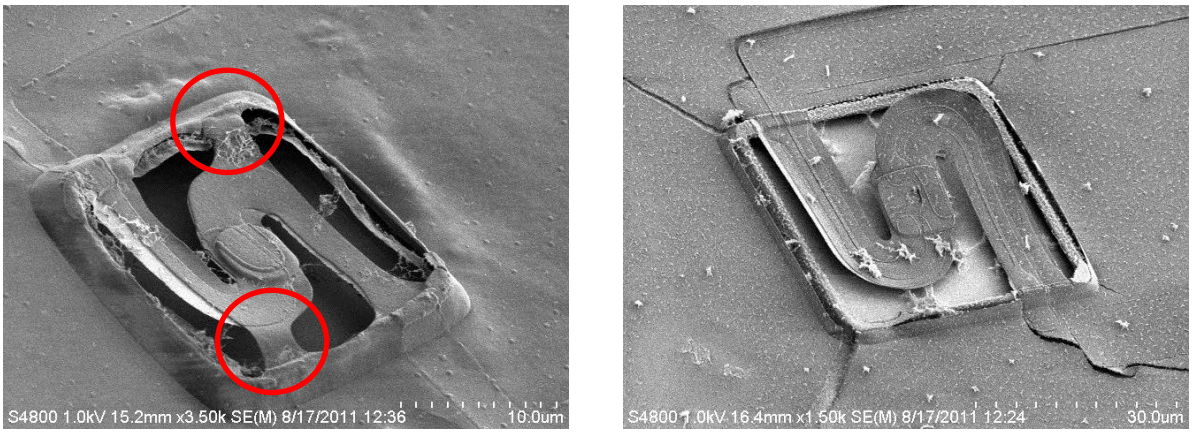


Figure 33 - The SEM on the right shows a device baked at 300°C for 5 hours and then released and the SEM on the left shows another device released in HF vapor and then baked under same condition as the previous one

The above result completely supports the described reason regarding the stress generation inside the film. The one that is baked and then released cracked due to high internal stress. This stress was generated due to thermal coefficient mismatch between Parylene and silicon dioxide and silicon nitride. Silicon nitride is the bottom layer on the substrate and the silicon dioxide is the layer on top of the Parylene film which was used for patterning the film.

Since the generation of stress inside the Parylene film is inevitable, two small supports were added to the Parylene film to hold the arms down. Those supports are shown in Figure 33 and circled in red.

3.2.6 Absorber deposition and releasing

As it was discussed in the previous chapter, the proposed absorber is an optical cavity and composed of three layers of nichrome/ nitride/ nichrome. To ensure the good adhesion of the absorber to the post, a thin layer of silicon nitride was first deposited and the rest of absorber was then deposited. The nitride is deposited at 300°C. The photoresist can no longer be used as the absorber sacrificial layer. Silicon dioxide was used again as the sacrificial layer since it can be deposited relatively fast in PECVD ($2\ \frac{\text{um}}{\text{hour}}$) and can be removed in the same way that the other

sacrificial layer can be dissolved. After depositing the sacrificial oxide, the film should be patterned in ICP. To have sloped sidewalls, photoresist mask which is used for patterning should be hard baked to reflow and becomes tapered. After etching the post and before depositing the adhesive nitride layer for the absorber, a quick O_2 clean is required to remove the polymers created during the oxide etching. The absorber deposition is consisted of 5 steps. First a nitride layer is deposited in PECVD. Then, a thin layer of nichrome should be deposited followed by PECVD nitride again. The last step which is deposited at the top of nitride layer is nichrome deposition using sputtering technique. After this, another Parylene film may be deposited to protect the top films from exposure to HF vapor but if the nichrome is thick enough it would protect the underneath layers form HF. Then it is the time to pattern the absorber. The thickness of the photoresist should be carefully chosen since the absorber is composed of different layers and it takes time to etch all of them.

Nichrome can be wet or dry etched. Special photoresist with excellent adhesion to nichrome is required to mask the nichrome layer from its etchant (TFN). Otherwise, the photoresist will peel off or a large undercut occurs. Dry etching is also possible and can be done in chlorine based plasma. The selectivity of nichrome to photoresist in the developed recipe is 24 over 400 which is not good at all. In this work, 5 um thick resist is spun on the wafer and used as the mask.

There would be four steps in the formation of the absorber, etching the top nichrome, nitride, nichrome, and finally nitride. After this last step, photoresist can be removed and the devices can be released with either of wet or vapor phase etching techniques. Figure 34 shows the result of using only dry etching technique for releasing a device.

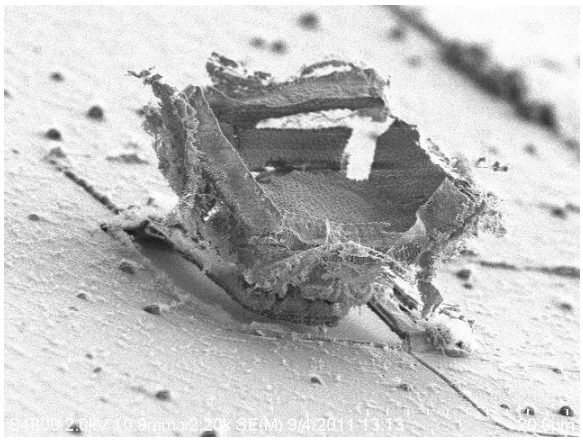


Figure 34 - SEM showing a device released in HF vapor

As it can be seen in the above SEM, the absorber was attacked and completely deformed. To protect the absorber from HF vapor, the photoresist mask on top can be used as a protection layer for the absorber during the etching. As it can be seen in Figure 35, the absorber is not deformed but it cracked.

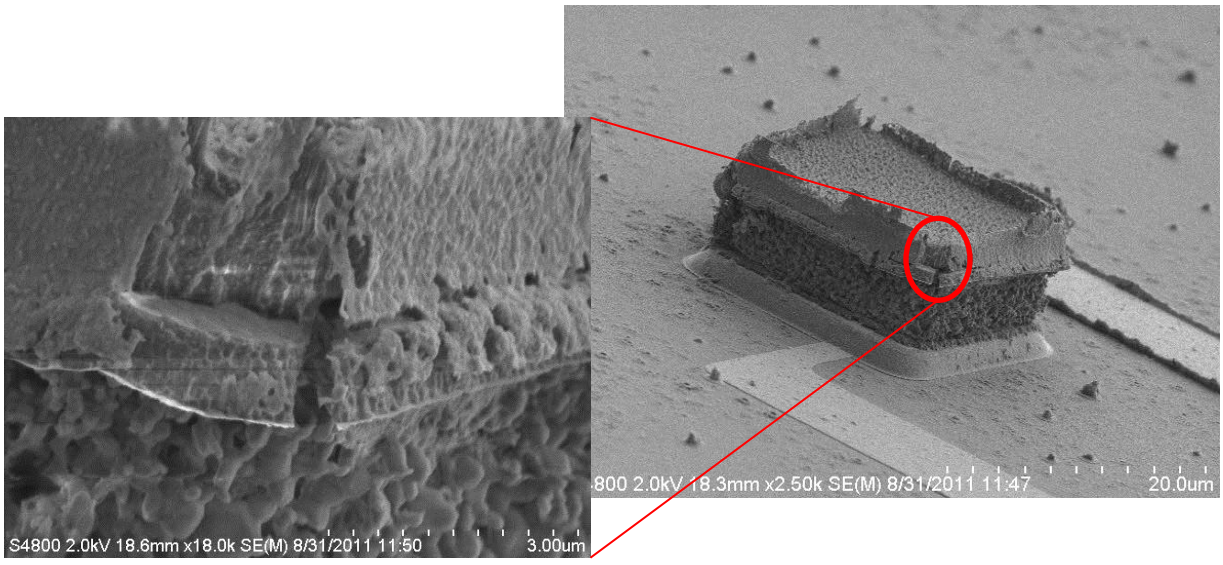


Figure 35 - SEM showing a device released in HF vapor while the top photoresist mask is not removed

Cryptohalite occupies more volume than silicon dioxide. Therefore, its thickness increases and causes the absorber to break. This problem has been reported by other groups as well [42]. Another problem is that even after baking, the residue is not completely gone (Figure 36).

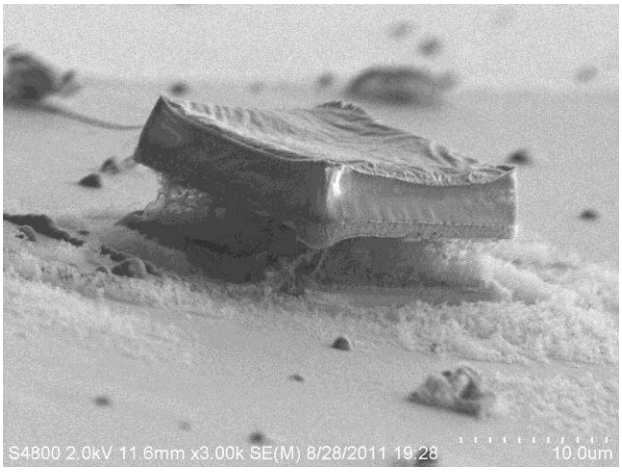


Figure 36 - SEM showing some residue that are not removed even after baking

It has been also reported that during HF etching a new residue, something other than Cryptohalite, is being formed right at the boundary of silicon dioxide and silicon nitride which cannot be removed later on by baking.

This residue is yet unknown but at this situation that there is boundary between oxide and nitride, a combination of dry and wet etching is required for releasing [42].

Below, SEMs of the completely fabricated devices after releasing using wet and dry etching techniques are shown.

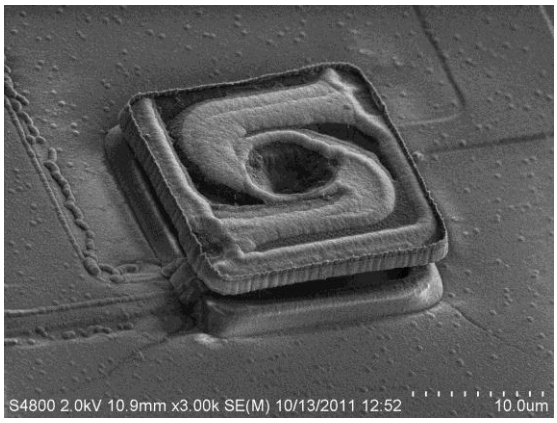


Figure 37 - SEM of a fabricated single detector

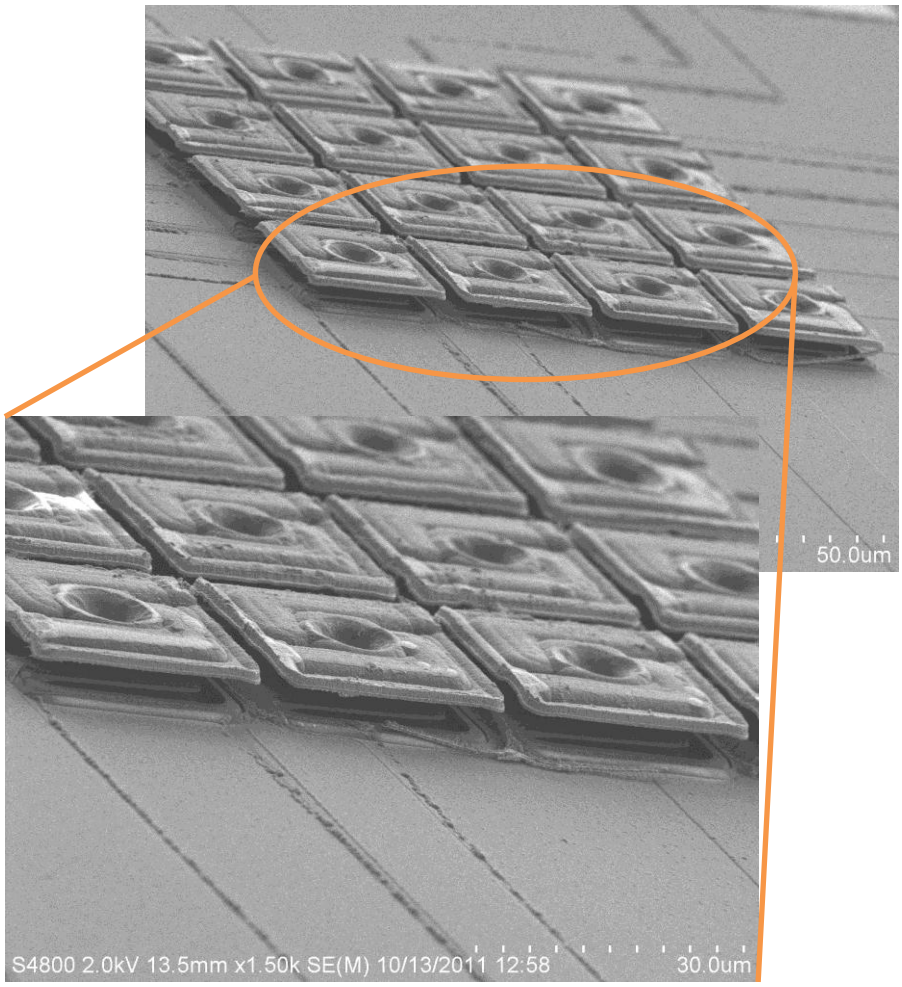


Figure 38 - A side view of a fabricated array

CHAPTER IV

Conclusion

In this thesis, design and fabrication of an uncooled surface-micromachined thermoelectric (TE) infrared detector is presented that features p -doped polysilicon/Nichrome (Cr 20-Ni 80) as the thermocouple material pair embedded in Parylene N. Thin silicon wires are desired since they have very low thermal conductivity. However, thin traces may not survive the fabrication process and they have to be supported by other means. Parylene N which is chosen for this task is a polymer with a very low thermal conductivity of $\sim 0.1 \frac{W}{m * K}$ that can be deposited at room temperature. In addition, it is resistant to common etchants and can be easily patterned in O_2 based plasma. In previous works, silicon nitride and silicon dioxide have been used instead but their thermal conductivity is many times higher than that of Parylene N. Thus, by use of Parylene N and small polysilicon wires, it is expected to reach the performance predicted by theory limit for these detectors.

COMSOL simulation was used to investigate the effect of thermal conduction of Parylene and thermoelectric wires. This simulation shows that the thermal conduction from the hot junction to the substrate happens through both Parylene arms and thermoelectric wires. Additionally, it was conceived that the thermal conduction through the TE wires is the dominant way of heat loss ($G_{TE} \gg G_{Parylene}$). Therefore, by further reducing the size of the TE wires, G_{TE} could be decreased and hence, the detector responsivity could be improved while Parylene can provide the mechanical strength for the thin TE wires.

The presented detector features an umbrella-like absorber that permits high fill factors. High fill factor is defined as the device active area or absorber area to the total area. For the smallest fabricated device, the device area is 20 um * 20 um and the absorber area is about 19 um * 19 um leading to a fill factor of as high as 90%. Although, if this detector is fabricated on a CMOS chip and in an array format, it might require more spacing between the pixels but absorber size can also be extended to cover those spacing. The absorber is an optical cavity composed of a three-layer stack NiCr/SiN/NiCr. It has been shown that metals are good absorbers but since they have many free electrons, their refractive index is large which causes high reflection coefficient. By the use of Maxwell theory, it has been shown that the refractive index is in correlation with electrical conductivity. In other words, if the sheet resistance of a metallic thin film increases, its refractive index decreases. The reflection, transmission, and the absorption of a three layer film are calculated by Silberg [29]. In our design, the sheet resistances of 377 and 45 ohm/square for the top and bottom metallic thin films are chosen respectively to achieve absorption.

Preliminary results show the responsivity of 100 V/W at 5 Hz and the response time of not greater than 26 ms in vacuum when viewing a 500 K blackbody with no concentrating optics.

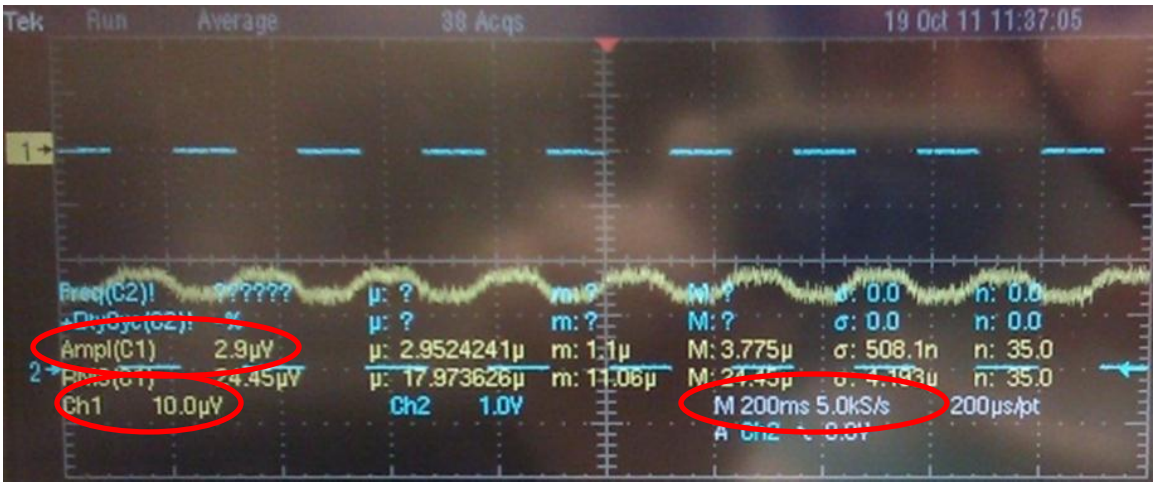


Figure 39 - The output waveform of the device

The device output signal is shown in Figure 39. The blue line is the inverse of the chopper signal and the yellow signal is the device output passing it through a low pass filter and averaging it. The response time of the device is measured using the above waveform.

To measure responsivity, the device is placed in front of a black body at a certain temperature. The output voltage of the device is measured. Then the detector is replaced with a NIST calibrated IR sensor. With this sensor, the amount of incoming infrared radiation is measured and then responsivity was calculated by dividing the output voltage by the power of the incoming radiation. Carrying out any measurement at zero frequency is associated with lots of different noises. To eliminate the effect of those noises, a chopper was placed in front of the black body. In this way, the incoming radiation is chopped at a certain frequency. Then a lock in amplifier is used to extract the signal from the detector output. The advantage of using a lock in amplifier is that only a small bandwidth of sum of the noise (0.1 Hz) is integrated into the output. Therefore, a very weak signal even few nanovolts can also be measured. The dominant source of noise in thermoelectric IR detectors is typically Johnson noise because these detectors are operating under open circuit condition and therefore, the current is almost zero. Shot noise which is defined as

$$\mathbf{i_{n,shot}} = \sqrt{\mathbf{2qi_{avg}\Delta f}} \quad (10)$$

Where Δf and q are the electronic bandwidth and charge of electron, is zero when there is no current flowing in the circuit. The generation recombination noise is negligible for the same reason. The other source of noise which limits the performance of the circuit in low frequencies is Flicker noise. The Flicker noise which is also called 1/f noise is defined by the following equation:

$$\mathbf{i_{n,f}} = \sqrt{\mathbf{K}\frac{\mathbf{i_{avg}^{\alpha}\Delta f}}{\mathbf{f^{\beta}}}} \quad (11)$$

Where k is a proportionality factor. α, and β are constants. Even this noise would be zero when the detector current is zero.

As a result, the total noise, for the detectors with resistances from 50 to 60 KOhm is equal to Johnson noise which is about $32\ \mathrm{nV/Hz^{0.5}}$. However, due to ambient noise (e.g. pump vibrations, measurement setup, etc.) the measured noise at 5 Hz is about $68\ \mathrm{nV/Hz^{0.5}}$. The D* is calculated to be $2.9 * 10^6\ \frac{\mathrm{cm} * \mathrm{Hz^{0.5}}}{\mathrm{W}}$.

Future work:

1- For further improving the device performance, the width of the thermoelectric polysilicon wires should be improved. As of now, the widths of the wires are 1.6 um. By reducing the widths of the wires, the thermal conduction from the hot junction to cold junction will be reduced. To increase the output voltage, the nichrome TE wire can be replaced with a polysilicon wire with a different doping than the other polysilicon TE wire. On the presented infrared detectors, p doped polysilicon wires has been used. Adding an n doped polysilicon TE wire which has negative Seebeck coefficient could increase the total Seebeck coefficient of the system and this results in larger output voltage.

2- The absorber has the pattern of the underneath layers. This pattern may cause some weak areas on the absorber. Thus, before absorber deposition, it will be tried to remove the pattern from the sacrificial oxide.

3- The response time of the detector should be improved by reducing the thermal capacitance of the absorber. In the described detector, the thickest layer in the absorber is silicon nitride which is 1 um. By making small holes in the absorber the thermal capacitance can be reduced. These holes should be small enough (each dimension smaller than $\frac{\lambda}{4}$) in a way that not to change the absorption efficiency.

4- The absorption of the absorber should be improved. Different materials and even different structures should be tested to achieve better results.

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Scope and Method of Study:

Described is an uncooled surface-micromachined thermoelectric (TE) infrared detector that features P-doped polysilicon/Nichrome (Cr20-Ni80) as the thermocouple material pair embedded in Parylene-N, which isolates the hot junction from the substrate. Simulation shows that the thermal conduction from the hot junction to the substrate through the TE wires is dominant ($G_{TE} \gg G_{parylene}$). By further reducing the size of the TE wires, G_{TE} could be decreased and hence, responsivity could be improved while parylene can provide the mechanical strength for the thin TE wires.

Findings and Conclusions:

The fabricated detector features an umbrella-like absorber that permits high fill factors. The device area is 20 um * 20 um and the absorber area is about 19 um*19 um leading to a fill factor of as high as 90%. The absorber is an optical cavity composed of a three-layer stackNiCr/SiN/NiCr.
At room temperature, the responsivity of 100 V/W @5 Hz and the response time of not greater than 26 ms were measured in vacuum when viewing a 500K blackbody with no concentrating optics. The D* is calculated to be $2.9 * 10^6$ cmHz^0.5/W.

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