VLSI DESIGN AND COMPARISON OF BANK MEMORY WITH MULTIPORT MEMORY CELL VERSUS CONVENTIONAL MULTIPORT AND MULTIBANK SRAM MEMORY

By

SUNIL KUMAR LAKKAKULA

Master of Science in Electrical Engineering

Oklahoma State University

Stillwater, Oklahoma

2009

Submitted to the Faculty of the
Graduate College of the
Oklahoma State University
in partial fulfillment of
the requirements for
the Degree of
MASTER OF SCIENCE
December, 2009

VLSI DESIGN AND COMPARISON OF BANK MEMORY WITH MULTIPORT MEMORY CELL VERSUS CONVENTIONAL MULTIPORT AND MULTIBANK SRAM MEMORY

Thesis Approved:

Dr. Louis G. Johnson

Thesis Adviser

Dr. Sohum Sohoni

Dr. James E. Stine

Dr. A. Gordon Emslie

Dean of the Graduate College

ACKNOWLEDGMENTS

As I am interested in digital memory design I met Dr. Louis G. Johnson to work on a thesis topic that involves memory design. He suggested to me a wonderful idea of designing a hybrid memory from conventional multibank and multiport memories for my thesis. In addition to the design we wanted to compare our design with the other two common designs. Also Mr. Ben White, former OSU graduate student has already done the comparison between conventional multibank and multiport memories in AMI 0.6um technology for the memory sizes 16Kb, 64Kb, 256Kb & 1Mb and found that the multiport memory is better for smaller memories in terms of area and performance where as the multibank memory is better for larger memories in terms of area and performance. As my work is related to Ben's work I have used some of his layouts that fit my design and some text from his documentation. I am designing the memory sizes of 4Kb, 16Kb & 64Kb with a different design criteria from Ben's hence there are considerable differences in the number of banks used in the case of multibank design.

TABLE OF CONTENTS

Chapter Page

LIST OF TABLES

Table Page

LIST OF FIGURES

Figure Page

CHAPTER I

INTRODUCTION

Modern digital systems require the capability of storing and retrieving large amounts of information at high speeds. In the semiconductor industry, memory is used for electronic data storage and is often referred to as computer memory. Memories are circuits that store digital information in large quantity. Much research and advancement is taking place in this particular field and thus memory is a critical part that can be improved upon in a computer or any digital device that uses it. The focus of my thesis is specifically on Static Random Access Memory (SRAM). My thesis is about designing and comparing a multibank memory with multiport memory cell versus the conventionally used multiport and multibank memory design techniques. By analyzing different sizes and arrangements of these memories an answer can be determined as to whether or not the use of multibank memory with multiport memory cell is better than the multiport and multibank memories for some memory sizes. The memory sizes used in this thesis are 4Kb, 16Kb and 64Kb.

1.0 Research Interest & Literature review

As the semiconductor technology advances the design of SRAM is becoming more dynamic and creative. After taking various courses that discuss memory and its common design techniques, I got interested in doing a thesis related to memory design. There are two commonly used design techniques: multiport and multibank. From

the previous studies, it was understood that multiport memories are better for smaller memories and multibank memories are better for larger memories. Conventional bank memories use six transistor standard memory cells, which are single port cells.

In my thesis, 4Kb, 16Kb and 64Kb memories are designed. The multibank memory approach uses a 1-port memory cell, the hybrid memory (bank memory with multiport memory cell) approach uses a 2 port memory cell instead of a single port memory cell and the multiport memory approach uses a 4-port memory cell. Thus there are three designs for each memory size and hence a total of nine designs were presented in my thesis. After designing, the area of each design was calculated and then compared for 4Kb, 16Kb and 64Kb. Because of time constraints and other technical problems, the delay simulations were limited to the 4kb memory size only.

The knowledge used to create this thesis comes from Dr. Johnson's suggestion to design a hybrid memory from multiport and multibank in order to avoid the sudden transistion between multiport and multibank techniques.

1.1 Major Design Considerations

In our design, the external memory ports are fixed to four (U=4) and we determined the minimum number of banks required for each design based on the average number of data returns and that the average number should be greater than or equal to 90% of the total available number of data returns, which is equal to the value of U [1]. If 'r' is the number of data returns, then the average 'r_bar' should be greater than or equal to 3.6. With four external memory ports the conventional multibank design requires 16 banks to have the average number of data returns to be greater than or equal to 90% of U i.e 3.6, whereas the hybrid bank memory with a 2-port memory cell requires 4 banks and

with 3-port memory cell requires 2 banks to meet the above criteria. The multiport memory is a single bank memory, and hence it requires only one bank.

1.2 Organization

This thesis is organized in such a way that it will explain how each element in the design works before moving on to explain the larger pieces. This thesis is divided into chapters followed by sub notations for each element of the different memory techniques that corresponds to the chapter. Chapter 1 gives some introduction to the topic. Chapter 2 explains the background behind the components with the memory arrays for 1-port, 2-port and 4-port memory cells. Chapter 3 explains the techniques used to optimize the layouts and the testing process. Chapter 4 displays the findings from the SRAM memory designs and detailed analysis of the data collected. Finally, chapter 5 concludes with what the data reveals, and future enhancements.

CHAPTER II

BACKGROUND

Static Random Access Memory consists of a few main parts that are necessary for all SRAM designs. SRAM design starts with an array of interconnected memory cells. These memory cells receive and distribute data through bi-directional lines that are connected to a pre-charge, write drivers, and sense amplifiers. An important part is the decoder which determines the section of memory cells that need to have a read or write performed on them. The inputs into the decoder, called the address, combined with the corresponding data coming from the bus into the SRAM are the elements that make up an external port. This is not to be confused with the internal ports within the multi-port memory cell. The ports in the multi-port memory cell correspond to the number of bit lines that are connected to the same memory cell.

2.0 Memory cell

A memory cell is used to store 1-bit of data. The memory cell in SRAM consists of two static inverters that feed into each other creating a latch [3] [5]. The pass transistors connected between the read/write logic and the memory cell itself controls the access into the memory cells and the switching for these pass transistors is controlled by word lines. To protect the validity and correctness of the data stored in the memory cell, read/write actions should not be done simultaneously. There are several ways of

designing a SRAM memory cell. In my thesis I discuss only two forms of SRAM memory cell designs that are necessary for understanding my work. They are the standard six transistor memory cell (Figure 1) used in the multi-bank memory and the six transistor memory cell with additional logic for read and write bit lines (Figure 2) used to create separate port elements [2].

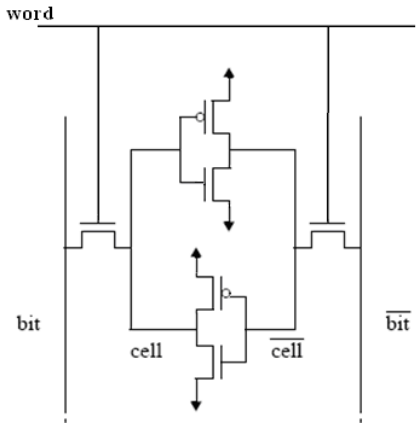


Figure 1: 6T Memory Cell

The 6T memory cell used in multi-bank memory consists of six transistors. There are two static inverters that feed into each other as shown in the figure 1. Each line in the inverter that feeds its output into the other's input is also connected to one end of an nFET pass transistor. The gates of these pass transistors are connected to the word line and turn on only when the word line is high. The other end of the pass transistors are connected to two bit lines referred to as bit and bit_bar. During successful read and write operations the values of bit and bit_bar will be opposite in value where as during pre-charge both bit and bit_bar has the same value since both lines are brought to a high value. By using two lines into the latch within the memory cell less power than from a single line becomes needed [6]. Bit and bit_bar can be designated on either the left or

right side of the cell. As long as you maintain the same consistency throughout the design it does not matter which side you are designating them.

Write Operation:

Before writing any value into the memory cell the bit and bit_bar lines should be loaded with the desired value. Now, allow a high value onto the word line that turns on the pass transistors connected on either side of the cell allowing the value from bit and bit_bar to pass through and drive the previous value out of the memory cell. Once the value is passed in, the word line can be driven low, this locks the written value into the inverter loop and the memory cell will store the written value until it is overwritten.

Read Operation:

The read operation is similar to writing to the memory cell. During the read operation you don't load any value on the bit and bit_bar line before making the word line high. A precautionary note is that since bit and bit_bar are used to write and read into the memory cell it is important to include some switching logic in the read/write design elements to make sure the circuitry that is accessing read values is turned off during the write process and vice versa [6].

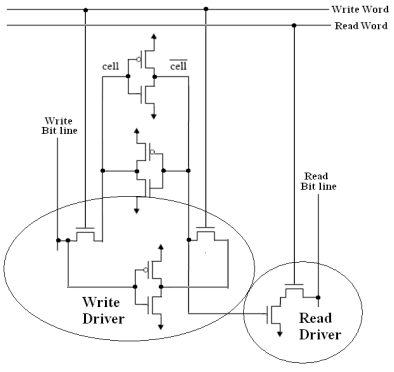


Figure 2: Multi-Port Memory cell (with two ports)

In multiport memory cells, with separate read and write lines the setup is similar to the 6T standard cell but with some key differences. For the circuitry that will be used

for the multi-port a separate read and write is necessary. Now there is a read and write bit line on the sides of the memory cell as shown in the figure 2. For each read and write bit line there is a separate word line.

Write Operation:

To initiate a write, it is necessary to load the desired value onto the write bit line before turning on the word line connected to the write line. Since the circuitry doesn't have the benefit of a bit_bar line an inverter is connected from the bit side to the bit_bar side. This inverter compensates for bit_bar by helping bring the value being written in to overcome the value previously there.

Read Operation:

To read a value from the memory cell, the lines need to be pre-charged high because the read driver circuitry for reading can only open the channels of the memory cell to ground. The read driver circuitry from the read line to the memory cell consists of an nFET transistor that has its gate tied to the read word line. The other end of this nFET is tied to another nFET in which the gate is tied to the bit_bar and the other end is tied to ground. Only when bit_bar and the word line are high, the read line is drawn to ground; otherwise the read bit line will stay high from the pre-charge.

2.1 Pre-charge Circuit

Pre-charging is also referred as bitline conditioning. The precharge circuit is used to charge the bitlines to high before operation. The precharge circuit consists of a pair of pMOS transistors connected as shown in figure 3. Another technique is to precharge through nMOS transistors to Vdd – Vt. This results in faster single ended bitline sensing because the bitlines do not swing as much, but reduces noise margins and may require

more precharge time [2]. Hence in my thesis I have used the precharge circuit consisting of pMOS transistors. This pre-charging enables the bitlines to have a high value at all times except during write and read cycles in case of multibank memory where as the lines must be pre-charged during the read cycle in case of multiport memory.

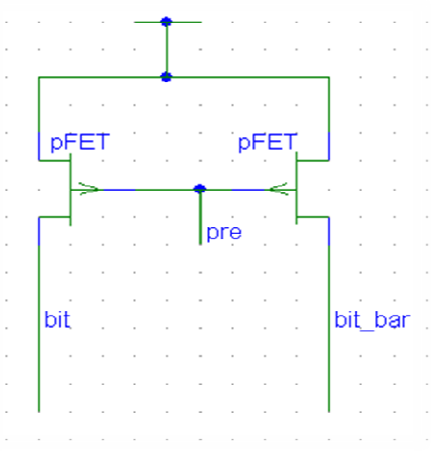


Figure 3: Precharge Circuit

From the above circuit when the precharge signal is low, both the transistors will be turned on and sends a high on both bit and bit_bar. When the precharge is high, both the transistors will turned off and the bitlines will float high till bit and bit_bar are loaded with the desired values during write operation. The bit lines are pre-charged to high before the read operation.

2.2 Sense Amplifier & Write driver

A sense amplifier is used when reading data from the memory cell. The sense amplifier is on the outputs from both bit lines in multi-bank and only on the read ports in the multi-port memory. A 2-bit AND gate is used as a sense amplifier in all the designs and have some key differences in the circuit used in case of multibank and multiport designs [1].

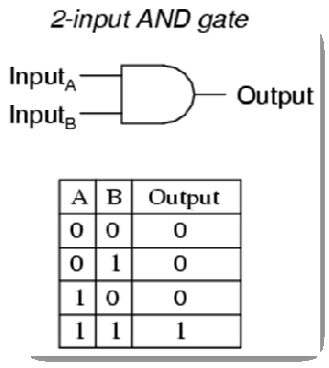


Figure 4: Sense amplifier

Turning off the sense amplifier during write operations and pre-charging the input read prevents the outputs from being able to turn on.

Write drivers pull the bitlines high or low during the write operation inorder to write into the cell.The write driver is also used to overcome the capacitive load on the bit lines as well as turn off the writing element when it is not needed.

Sense amplifier and write driver are explained more in detail in the methodology (Chapter III).

2.3 Decoder [6]

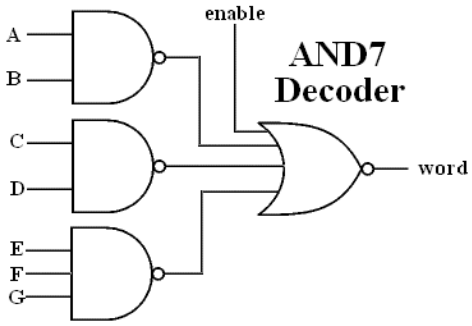


Figure 5: 7-bit Input Decoder

A decoder is a collection of AND gate's. Since SRAM calls for static cells, a static AND gate is used for creating faster speeds without sacrificing area significantly. The design of an AND gate consists of multiple stages of NAND and NOR gates. To

minimize delays the NAND and NOR should nominally have two inputs, but no more than four inputs. The number of inputs to be used on the NAND and NOR is dependent on tradeoffs between speed and area, where more stages and fewer inputs causes more area to be used. To determine the number of inputs the decoder needs is logarithmically dependent on the number of rows that are in the memory array. A memory array with 32 rows will need 5 address bits to reach all memory locations. A single decoder consisting of two stages and 7 inputs will need 3 NAND gates followed by 1 NOR gate. For decoders with even number of stages, it will be looking for high inputs in order to give a positive output. For decoders with odd number of stages, it will be looking for low inputs in order to give a positive output. The output from the NOR gate called the word line will only go high once all the inputs into the NAND are high. An additional enable input is needed into the NOR gate to turn off the decoder during pre-charge cycles. After the layout for a single decoder is created an array of decoders is made that will match up to the number of rows in the memory array. Each decoder row is connected in a way to give each row a separate address code that will trigger its word line high once that address code matches the pattern for that row. The inputs into the column of decoders are connected to a buffer and inverter of each address value. The need for these driver elements is to reduce capacitive load from the address inputs as well providing an inverted signal to allow a unique address code without adding inverters at every row.

2.4 Decoder Driver [6]

The decoder driver is the buffer circuitry for the word line between the decoder and the memory array that allows for the decoder outputs to not be overloaded by the

large capacitance load of the memory array. The inverter from the driver that is connected to the memory array is scaled to minimize the load and delay into the memory array. The other inverter in the buffer is scaled to approximately one half the size of the larger inverter to minimize the load that will be acting on the word lines from the decoder. The actual size of the decoder is dependent upon the size of the memory array. The delay it takes for the decoder to power up the word lines in the array is critical and should be minimized as small as possible with a properly sized driver.

2.7 Switching Network [6]

The switching network, used in multi-bank memory, is a series of wires that connect the input port through a switch to the bank and address within the bank that need an operation performed [7] [8]. The layout consists of a series of inputs from the ports to a series of switches that will forward the next address to a specific bank [8]. The specific bank that is selected is determined by the bank decoder which powers the gates of the corresponding bank that needs to be reached.

The bank decoder consists of enough significant bits from the address to determine which bank the port should be connected to and a series of AND gates like before with the row decoder for the memory array. The bank decoder is arranged in the same way as the row decoder with each row consisting of a unique address. An inverter and buffer are also used for powering the bank decoder's inputs. The enable is also a necessary part of the bank decoder, where the enable value is provided from another element called the bank conflict checker.

A problem that occurs with multi-bank memory is bank conflict. Bank conflict occurs when two ports are trying to write to the same bank. Since bank conflicts are

possible then additional circuitry is needed for practical applications in the form of a bank conflict checker.

A bank conflict checker takes the same bits used by the bank decoder to determine the bank location for each port and compares them to all the bank decoder addresses of all the ports. If a conflict occurs the bank conflict checker sends a signal to the bank decoders to stop decoding for all but one of the ports that a conflict occurs in. By creating a bank conflict checker, the multi-bank system is forced to put off for at least one cycle all except one of the conflicting ports trying to write to the same bank location.

2.6 Two Common memory design techniques

The two commonly used design techniques for SRAM memory are multiport and multibank approaches.

Multiport Memory

As the name indicates, the memory cell has multiple ports, so that all ports can access any memory cells without conflict. This approach can achieve good performance, but the chip size increases in proportion to the square of the number of ports, because all memory cells have multiple ports [4]. The arrangement of the basic multiport memory cell is as shown in the figure 6. For the read and write operations it needs additional circuitry called read/write circuitry connected between the bitline and the memory cell as shown in figure 2.

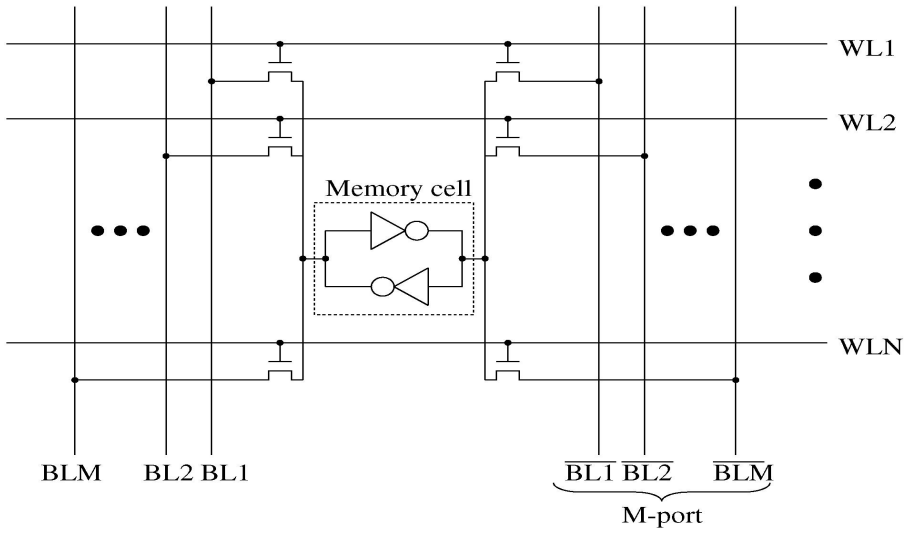


Figure 6: Multiport memory cell [4]

Each port has its own word line. For each additional read/write line it is called adding a port. The ratio of read to write ports is normally two read ports for every write port because data is twice as likely to be read as it is to be written. Simultaneous writes into the same cell is not possible while simultaneous reads is possible for as many read ports that are available [6]

Multibank Memory

In the multibank memory approach, each port is connected to multiple single port memory blocks called bank memory. In contrast to the multiport memory approach, this approach can be implemented in a smaller chip size because of the use of single port memory cells. However, because this approach uses single port memory as bank memory, if two or more ports access one bank simultaneously, a bank conflict occurs. To reduce bank conflicts, it is necessary to have more number of banks [4].

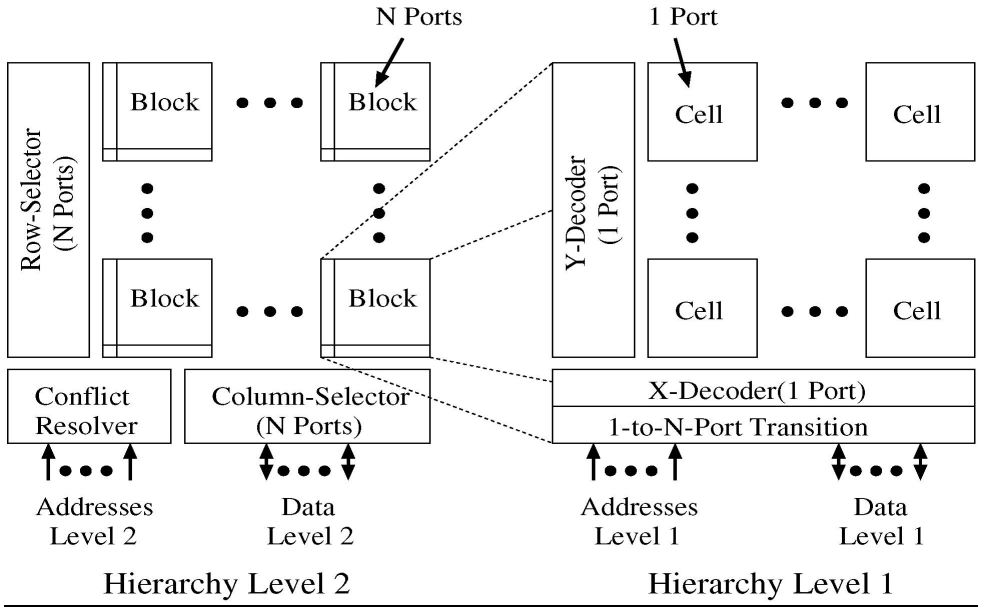
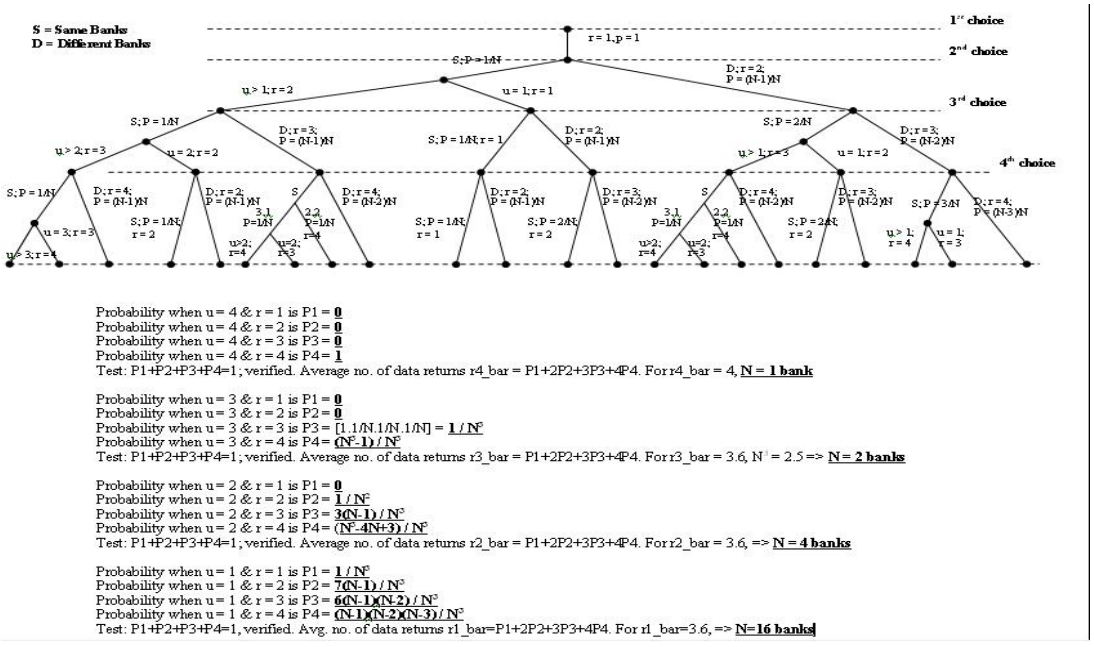


Figure 7: Multibank memory [4]

CHAPTER III

METHODOLOGY

In order to determine whether the hybrid design (multibank memory with multiport memory cell) is beneficial over conventional multibank and multiport memories for intermediate memory sizes (not too small and not too big) it is necessary to create several layouts for each approach and for different memory sizes. The total memory sizes used for all the three approaches are 4096, 16384 and 65536 possible bit locations each with 4 external ports (two ports dedicated to read and two ports dedicated to write). A tree structure was made to determine the number of banks required and is as shown in figure 8.



Probability when u = 4 & r = 1 is P1 = **0**
Probability when u = 4 & r = 2 is P2 = **0**
Probability when u = 4 & r = 3 is P3 = **0**
Probability when u = 4 & r = 4 is P4 = **1**
Test: P1+P2+P3+P4=1; verified. Average no. of data returns r4_bar = P1+2P2+3P3+4P4. For r4_bar = 4, **N = 1 bank**

Probability when u = 3 & r = 1 is P1 = **0**
Probability when u = 3 & r = 2 is P2 = **0**
Probability when u = 3 & r = 3 is P3 = [1.1/N.1/N.1/N] = **1 / N^2**
Probability when u = 3 & r = 4 is P4 = **(N^2-1) / N^2**
Test: P1+P2+P3+P4=1; verified. Average no. of data returns r3_bar = P1+2P2+3P3+4P4. For r3_bar = 3.6, N^1 = 2.5 => **N = 2 banks**

Probability when u = 2 & r = 1 is P1 = **0**
Probability when u = 2 & r = 2 is P2 = **1 / N^2**
Probability when u = 2 & r = 3 is P3 = **3(N-1) / N^2**
Probability when u = 2 & r = 4 is P4 = **(N^2-4N+3) / N^2**
Test: P1+P2+P3+P4=1; verified. Average no. of data returns r2_bar = P1+2P2+3P3+4P4. For r2_bar = 3.6, => **N = 4 banks**

Probability when u = 1 & r = 1 is P1 = **1 / N^2**
Probability when u = 1 & r = 2 is P2 = **7(N-1) / N^2**
Probability when u = 1 & r = 3 is P3 = **6(N-1)(N-2) / N^2**
Probability when u = 1 & r = 4 is P4 = **(N-1)(N-2)(N-3) / N^2**
Test: P1+P2+P3+P4=1, verified. Avg. no. of data returns r1_bar=P1+2P2+3P3+4P4. For r1_bar=3.6, => **N=16 banks**

Figure 8: Tree structure [1]

Where u=number of internal ports in the memory cell, r=number of data returns, r_bar=average number of data returns, P=probability and N=number of banks required.

With four external memory ports the number of banks required for the multibank layouts and hybrid layouts were determined to be 16 banks and 4 banks respectively based on the required design criteria described in section 1.1.

The layouts of all the elements are carefully designed in order to have as minimal area as possible for the whole memory. The creation process of all the elements undergoes a series of design and testing procedures. Cadence Virtuoso is used to design the layouts and IRSIM is used to test the layouts.

After creating a layout for each element, first it should be checked for zero DRC errors (verify → drc). Then the layout is extracted (verify → extract). Then open the extracted layout and launch spectre (Launch → Simulation → Spectre) and then a spectre netlist for the layout is retrieved. As the designs in my thesis are tested using IRSIM the spectre netlists are converted to .sim files which is in the format required by IRSIM to simulate. This can be done using the **"spectre2sim**" program in the command prompt. The syntax for that would be "**spectre2sim 30 <netlist path> filename.sim**". Here 30 represents lambda=0.30u. Then an IRSIM command file is created for each design that has the input and output commands. Now the .sim file is run together with the corresponding IRSIM command file that tests a series of stimulus on the inputs and verifies the output accuracy. This was done using the following command in the command prompt "**irsim scmos30.prm filename.sim –filename.cmd**" [9]

Example:

Current directory name = Thesis

Cell name: Memory

Netlist path: spectre.run1

Spectre2sim 30 spectre.run1/netlist memory.sim

irsim scmos30.prm memory.sim –memory.cmd

3.0 Memory cell

Since the memory cell is the biggest element in all the three approaches it is necessary to keep its design as small as possible. Keeping the same width as the memory cell, the height of the pre-charge, sense amp, write driver and decoders are minimized as much as possible. The design of the memory cell for the multibank and multiport memory approaches are different as described in section 2.1. In this thesis I used a 6T standard memory cell for Multibank memory design, 2-port memory cell with one read line and one write line for Hybrid memory design and a 4-port memory cell with two read lines and two write lines for Multiport memory design. The layouts of these memory cells are shown in figures 9, 10 and 11. To make the routing between metal2 and metal 3 wires easier it was followed that all the metal2 bitlines are drawn vertical and all the metal3 wordlines are drawn horizontal.

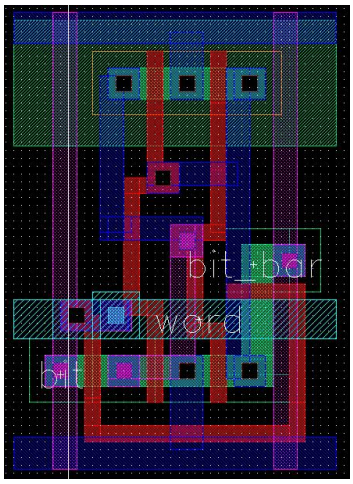


Figure 9: 6T Standard memory cell layout

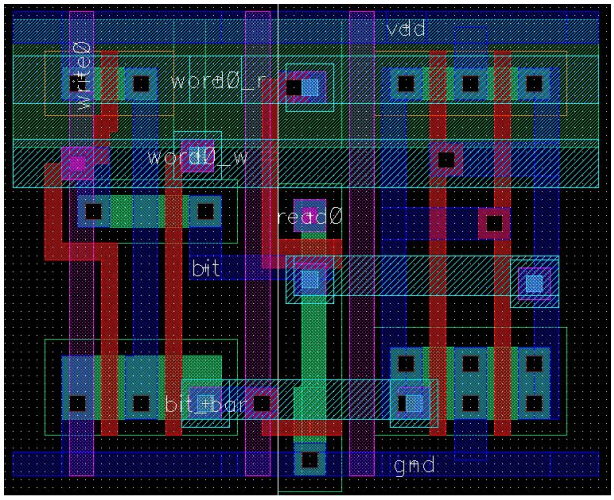


Figure 10: 2-port memory cell layout

Two read bitlines are used instead of one for each read bitline in case of 2-port and 4-port memory cells inorder to eliminate noise from the read bitlines. Each end of the read bitline is then connected to both ends of the sense amp (different from the one described in section 2.3, refer to sense amplifier in this chapter for more information) and given its own pre-charge. One read bitline is connected to even number memory cells while other is connected to odd number memory cells in the memory array. [6]

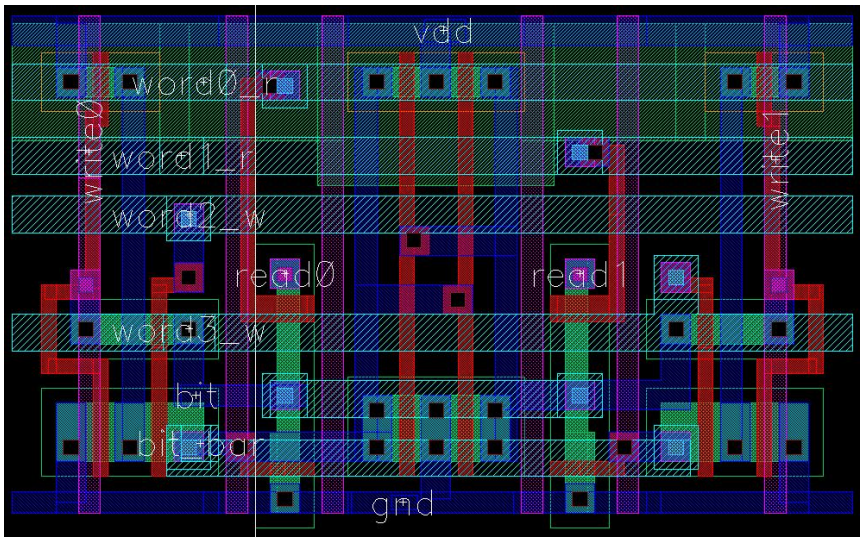


Figure 11: 4-port memory cell layout

In the case of 2-port and 4-port memory cells the height of the cell is mainly based upon the metal3 word lines as well as the metal3 lines that connect the bit and bit_bar of the memory cell to the read/write drivers.

3.1 Pre-charge

The pre-charge circuit is designed in such a way that it spends as minimal time on precharging as possible. The layout for the basic precharge circuit used for the memory array is shown in figure 12.

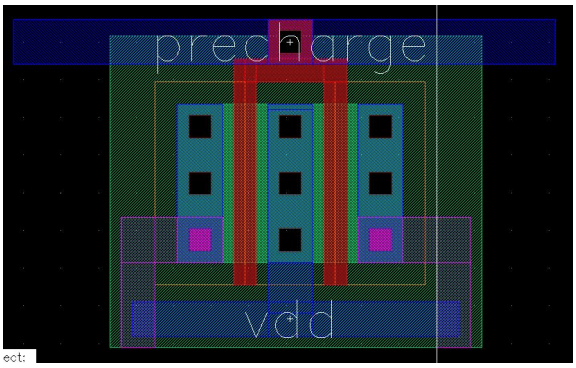


Figure 12: Precharge circuit layout

The precharge signal is connected to the gates of the two pMOS transistors. One end of both the transistors are connected to Vdd. In multibank design the other end goes to bit and bit_bar. In case of hybrid and multiport design the other end goes to the two read lines that are provided for the read port.

3.2 Sense Amplifier

As the sense amplifier connects to the bitlines from the memory cell the width of the sense amplifier is limited to the width of the corresponding memory cell where as its height is independent but should be maintained as low as possible. With a greater number of read ports additional sense amplifiers are needed to reach all the ports in the memory cell. In the case of multibank design a single sense amplifier is needed to sense the

bitlines from each memory cell; in the case of hybrid design a single sense amplifier is needed to sense the two read lines used for a single read port in the memory cell; and in the case of multiport design two sense amplifiers are needed to sense the four read lines used for two read ports in the memory cell.

In multibank design both the bit lines are connected to the two inputs of an AND gate. In order to get the valid data output from the sense amplifier while reading a ‘0’ or ‘1’ the bit_bar value is inverted and given as the input to the sense amplifier.

In the case of hybrid and multiport designs during read operation one read line will go low or high based on the data written previously into the memory cell and the other will stay high from the precharge. If the data written is low the senseamp should return a low and if the data written is high the sense amp should return a high.

As the sense amp output is connected to the read/write databus it can affect the content of the databus during a write operation, hence an additional nFET switch is used to prevent this.

3.3 Write driver

The width of the write driver is critical and is matched to the minimum width used by the memory cell. The write driver is designed to be powerful enough to write to all elements in the column and should be able to turn off when not writing.

The components that make up a write driver consist of two very large nFET latches and an inverter [2]. In the case of multibank design both the latches are connected to ground whereas in hybrid and multiport designs one latch is connected to ground and the other is connected to vdd. There are two gates needed to power each latch, with one gate connected to an enable and the other gate connected to the data line [2]. One latch is

connected directly to the data line while the other is connected to an inverter before being connected to the latch 2]. The data lines are also wired across the write driver to also be connected to the output of the sense amplifier.

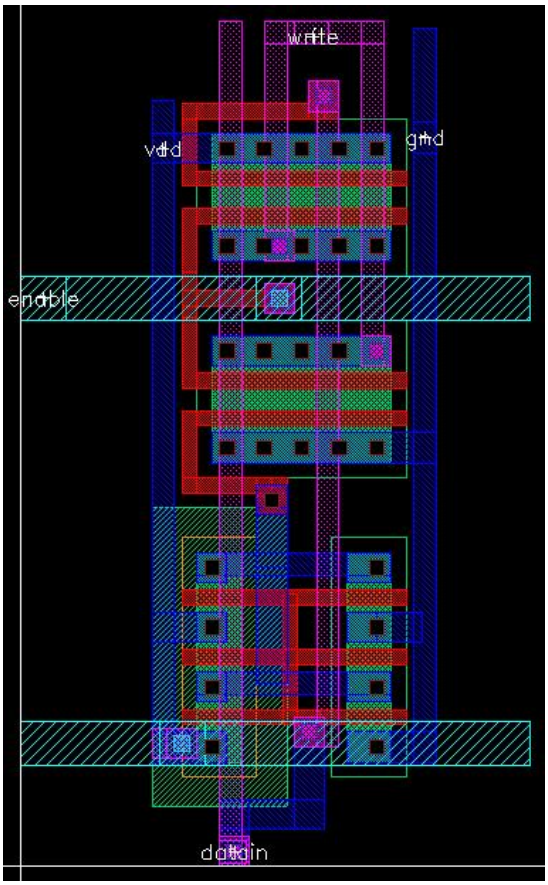


Figure 13: Writedriver hybrid layout

The writedriver circuit used in the hybrid and multiport design is almost similar to the one used in multibank. The key differences are one latch is connected to vdd instead of ground and the lines from the both the nFET latches are shorted and then connected to the write bitline of the memory cell.

3.4 Decoder

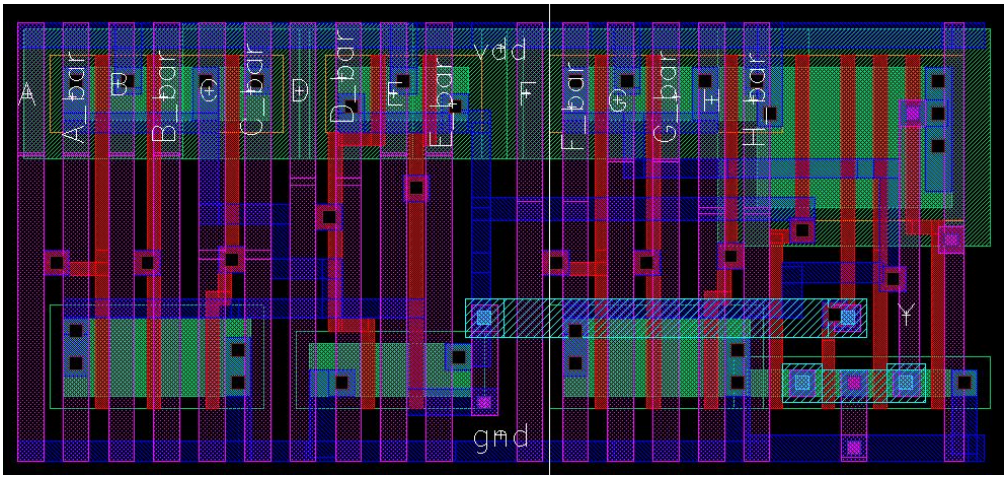


Figure 14: Decoder (AND 8) layout

The decoder is chosen based on the row size in the memory array. AND8 is for 256x256 memory array similarly AND7 is for 128x128 memory size and so on. In the case of 2-port hybrid and 4-port multiport designs two and four AND gates are used in a row respectively, one for each port. The decoder output is connected to the corresponding word line in the array row.

3.5 Decoder Driver

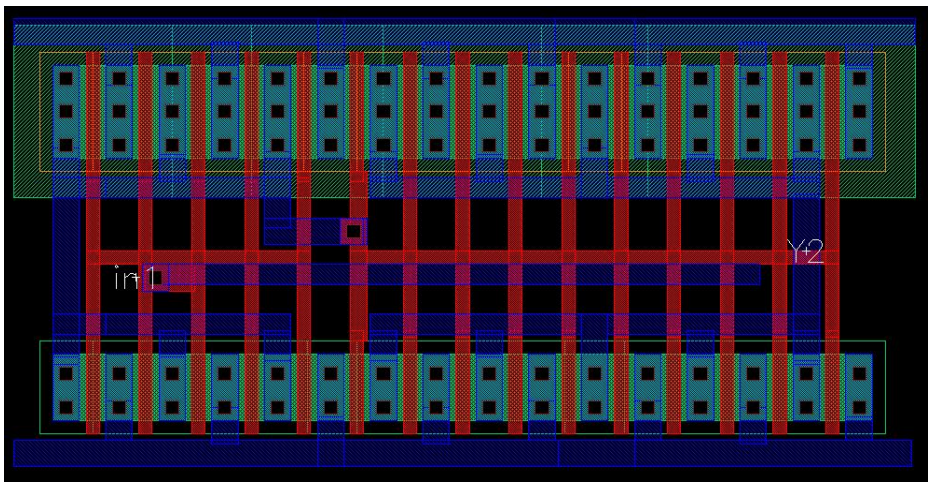


Figure 15: Decoder (AND8) Driver layout

The driver is also located in the same row as the decoder and splices the word line between the decoder and the memory row. The driver is used to create the buffer and inverter used to power the capacitive load of all the rows of the decoder.

3.6 Bank Decoder

The bank decoder is used in the case of multibank and hybrid designs. It is similar to the design of the regular decoder. The only difference is the number of address bits it decodes. For banks of 4 and 16, bank decoders need only 2 and 4 additional address bits to determine the correct bank location. The outputs of the bank decoder need to be connected to the switching network.

3.7 Switching Network

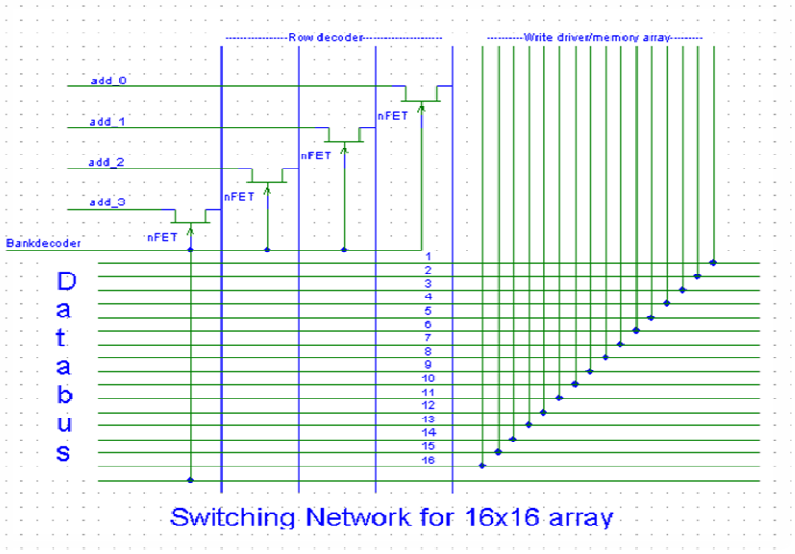


Fig 16: Switching Network

The figure shown above is the switching network using a 4-bit switch. The top four lines are the address bits for the row decoder and last line which connect all the gates of the nFET's is the input line for the switching network. The switching network gets the input from the bank decoder to select the bank to perform a read or write. If the input is

high it turns on all the nFETs and sends the address to the row decoder and also loads/receives the data bits into the corresponding bank. Each data line in the data bus has a nFET switch similar to the 4-bit switch whose gate is connected to the last line in the figure and sends the data in or out from the memory array once the bank gets selected.

3.8 Multiport memory

As the name indicates the memory cell in this design has multiple ports. The elements of multiport memory consist of a memory array, precharge, sense amp, writedriver and decoder arranged as shown in the figure 17.

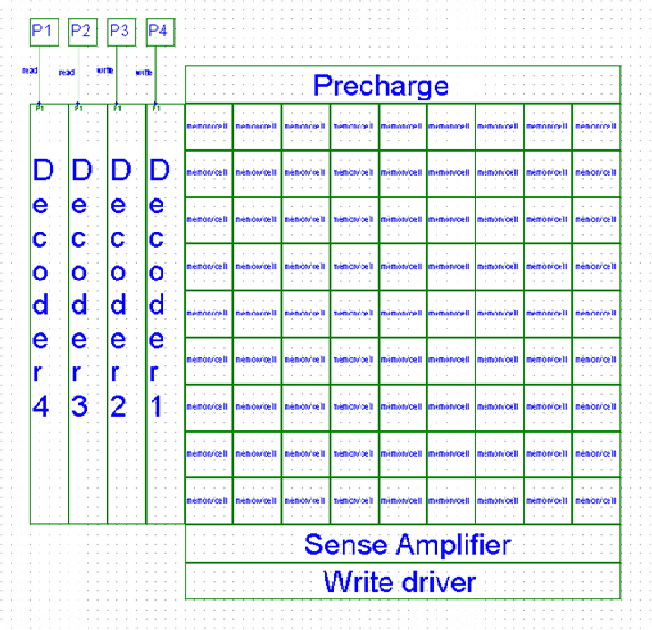


Fig 17: Multiport memory

The design starts with the memory array. The array size is determined based on the memory size you are designing. A 4Kb memory requires 64x64 size memory array, 16Kb memory requires 128x128 size memory array and a 64Kb memory requires 256x256 size memory array. The precharge circuit is used to precharge the read bit lines and the sense amp is used to sense the read bit lines. The decoder is used to decode the

word lines to select the array row to be written or read. Since there are four internal ports in a memory cell, four decoders are needed to decode them one for each internal word line.

As there are four external ports, two ports share the read ports separately and the other two share the write ports separately from the memory cell. Hence reading can be done only through two external ports and similarly writing can be done by the other two external ports. Data cannot be written simultaneously into the same memory location from the different ports and cannot be read simultaneously from the same memory location from different ports. Conflict occurs when the address to the external ports used either to write or to read the data matches with another port. However, a read and write operation to the same bank is allowed simultaneously.

3.9 Multibank Memory

The conventional multibank memory uses the 6T standard cell. The elements of a single bank consist of a memory array, precharge, sense amp, write driver, switching network, decoder and decoder driver

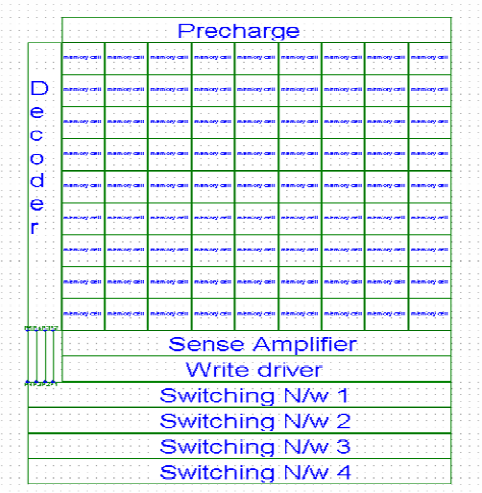


Figure 18: Single bank in Multibank design

The design starts with the memory array. The array size is determined based on the memory size to be designed and the number of banks required. In my thesis, multibank memory uses 16 banks to meet the design criteria. A 4kb memory requires 16x16 memory array, 16kb memory requires 32x32 memory array and the 64kb memory requires 64x64 memory array for one single bank. Precharge circuit is used to precharge the bit lines and sense amp is used to sense the bit lines. Write driver writes data into the array during write operation and turns off during read operation. The decoder is used to decode the wordlines to select the array row to be written or read. Switching network is used to connect to the bank decoder.

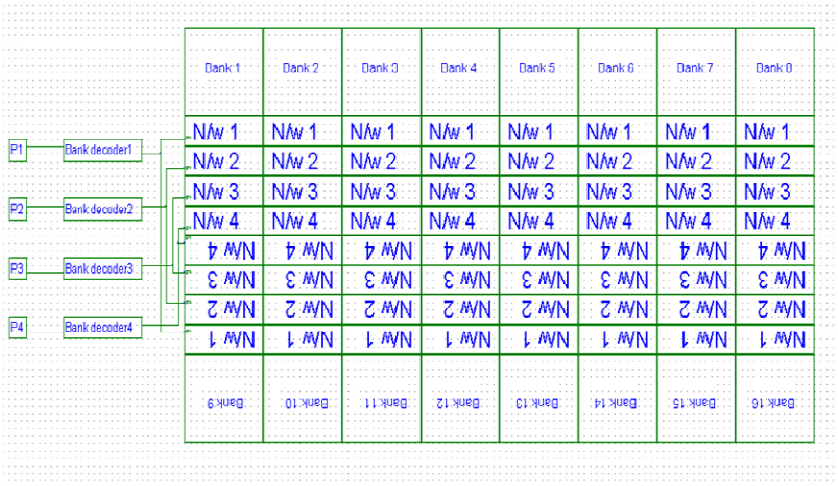


Figure 19: Multibank Memory

Normally the banks are arranged as shown in the above figure. Once again simultaneous writes or reads to the same memory location or same bank are not allowed. Conflict occurs when one or more external port addresses matches with each other.

3.10 Hybrid memory [1]

The design and arrangement of the banks in the hybrid design is almost the same. The only difference is that the bank memory uses a two port memory cell instead of a 6T standard memory cell.

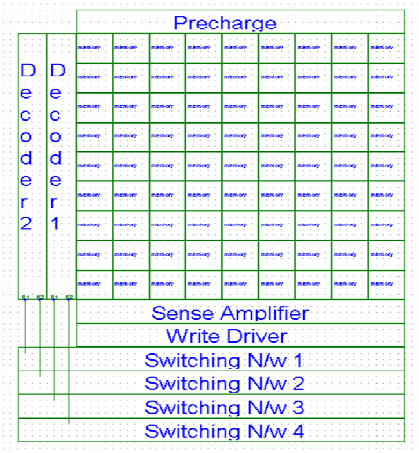


Figure 20: Single bank in Hybrid design

Two decoders are needed to connect to the read and write port available from the memory cell. One decoder is connected to the read port and the other is connected to the write port.

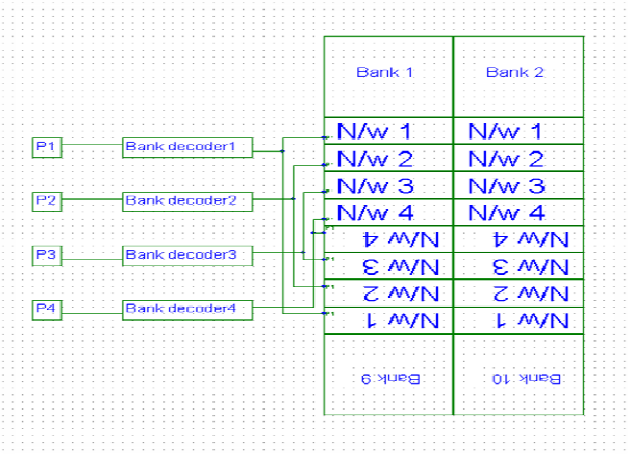


Figure 21: Hybrid memory

CHAPTER IV

FINDINGS

After making sure that all the designs are checked for no DRC errors and simulated using IRSIM, the area and delays of all the designs were calculated.

4.0 Area comparison

4kb memory	**Multibank**	**Hybrid**	**Multiport**
Area(um^2)	1,927,071.0	2,716,215.84	2,953,262.16
16kb memory	**Multibank**	**Hybrid**	**Multiport**
Area (um^2)	5,880,199.5	9,345,070.8	11,136,735.09
64kb memory	**Multibank**	**Hybrid**	**Multiport**
Area (um^2)	20,120,609.52	36,261,055.44	43,104,407.4

Table 1: Area comparison

For the memory sizes chosen, multibank design consumed less area compared to the other two designs whereas the multiport consumed more area. The area of the hybrid design lied in between these two. For smaller memories the difference in the areas of multibank, hybrid and multiport is less but as the memory size increases the difference increased.

4.1 Delay comparison

The following table shows the delays of the memory cell in each design to perform a read or write. The write delays correspond to the time took to write the data into the memory cell after making the word line high whereas the read delay correspond to the time took to change the bit and bit_bar values after making the word line high.

1 port cell	Write a ‘0’	Write a ‘1’	Read
Delay (ns)	0.05ns/0.25ns	0.22ns/0.05ns	0.04ns
2 port cell	Write a ‘0’	Write a ‘1’	Read
Delay (ns)	0.09ns/0.30ns	0.28ns/0.10ns	0.08ns
4 port cell	Write a ‘0’	Write a ‘1’	Read
Delay (ns)	0.12ns/0.40ns	0.38ns/0.14ns	0.09ns

Table 2: Memory cell delay

Because of the time constraints the total memory delay simulations are limited to 4kb memory size only.

	Multibank	Hybrid	Multiport
Delay (ns) to write a ‘0’	7.26ns	10.16ns	3.46ns
	Multibank	Hybrid	Multiport
Delay (ns) to write a ‘1’	8.33ns	11.25ns	3.51ns

	Multibank	Hybrid	Multiport
Delay (ns) to read	16.69ns	14.12ns	8.27ns

Table 3: Total memory delay Comparison

From the table, the multiport memory is superior in its performance with respect to write and read access times. The write-driver I used in all the three designs has the same driving strength hence it took less time to drive the data onto the bit lines in multibank design compared to the hybrid design because the array size is big in the hybrid design. In contrast to the write access times, hybrid design took less time during read compared to the multibank memory.

CHAPTER V

CONCLUSION

The results found by this study show where the hybrid design is advantageous over the other two designs. For the memory sizes chosen multibank memory finds itself always beneficial in taking up less area. Hybrid design is beneficial in case of bigger memories over the multiport memory with respect to the area.

Multiport finds itself superior in its read and write ability in comparison to the other two designs. Hybrid memory is beneficial in its read ability over multibank memory.

5.0 Future Enhancements: Because the delay simulations were limited to 4kb memory size in this thesis, a final conclusion cannot be made with respect to the design performance. Hence more simulations are needed for various memory sizes in order to make a perfect comparison. Also this project as a whole is not complete and needs some additional circuitry like column selector, column decoder, bank conflict checker etc. By using column selector the area of the hybrid design can be further reduced.

REFERENCES

[1] Johnson, L.G. Personal Interview Jan – Nov 2009.

[2] Harris, D. and Weste, N. CMOS VLSI Design: A Circuits and Systems Perspective. 3rd ed. Boston: Pearson Education Inc, 2005. pp. 713-759

[3] Hodges, D., Jackson, H., and Saleh, R. Analysis and Design of Digital Integrated Circuits: In Deep Submircon Technology. 3rd ed. New York: McGraw Hill, 2004. pp. 368-377.

[4] Hironaka, T., Inoue, T., Koide, T., Mattausch, H., and Sasaki, T. "Chip Size and Performance Evaluations of Shared Cache for On-Chip Multiprocessor." Wiley InterScience. Hiroshima, Japan. March 2004: pp. 350-363.

[5] Yeo, K., and Roy, K. Low-Voltage, Low-Power VLSI Subsystems. New York: McGraw Hill, 2005. pp. 177-213

[6] Benjamin D. White. VLSI DESIGN COMPARISON OF MULTI-PORT SRAM VERSUS MULTI-BANK SRAM. Master's thesis, Oklahoma State University, 2008.

[7] Mai, K. "Low-Power SRAM Design Using Half-Swing Pulse-Made Techniques." IEE Journal of Solid-State Circuits. November 1998.

[8] Cho, S. I-Cache Multi-Banking and Vertical Interleaving. Pittsburg: University of Pittsburg. March 2007.

[9] Dr. L.G. Johnson. Cadence Inverter Cell Design Tutorial. ECEN 4303. http://lgjohn.okstate.edu/cadence/virtuoso.pdf

APPENDIX A: Layout designs

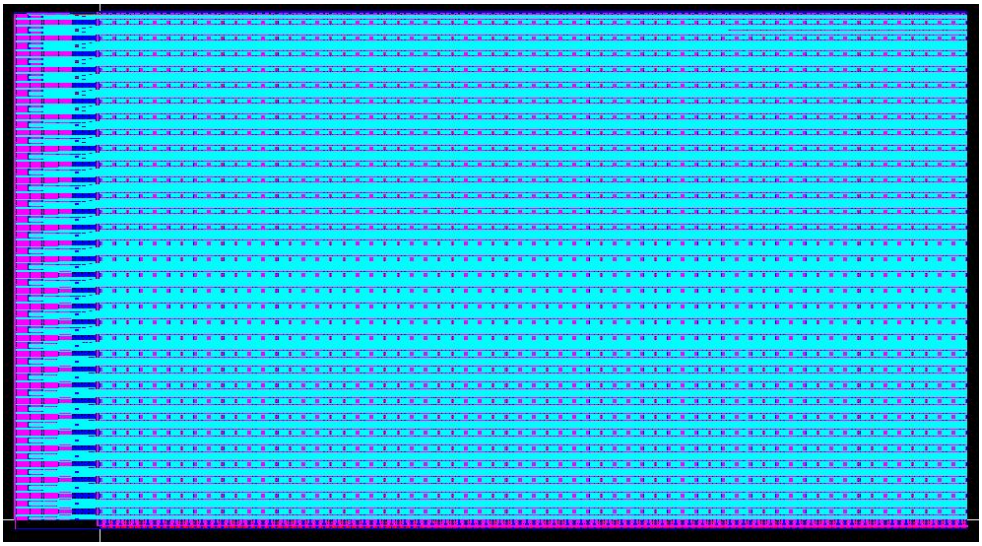


Figure 22: 4kb Multiport memory

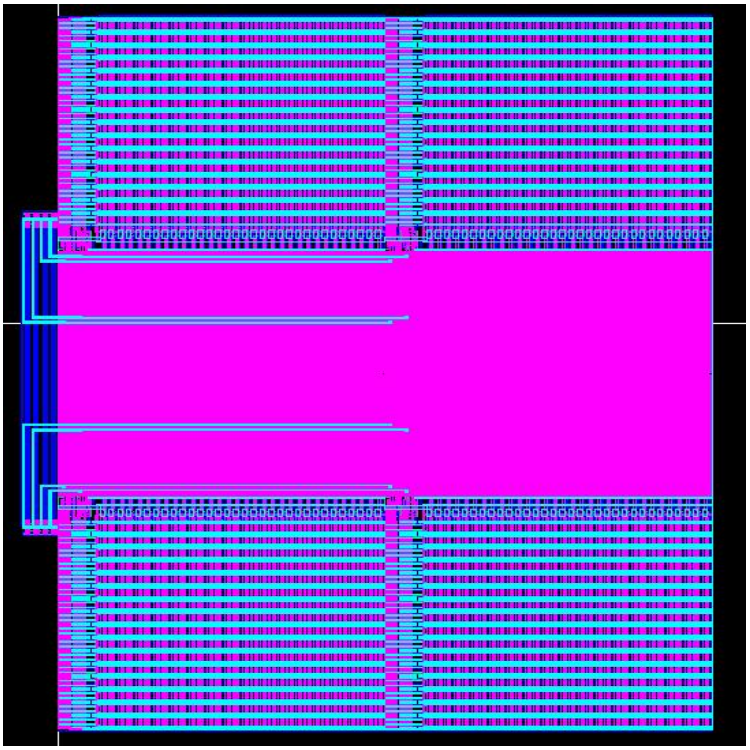


Figure 23: 4kb Hybrid memory

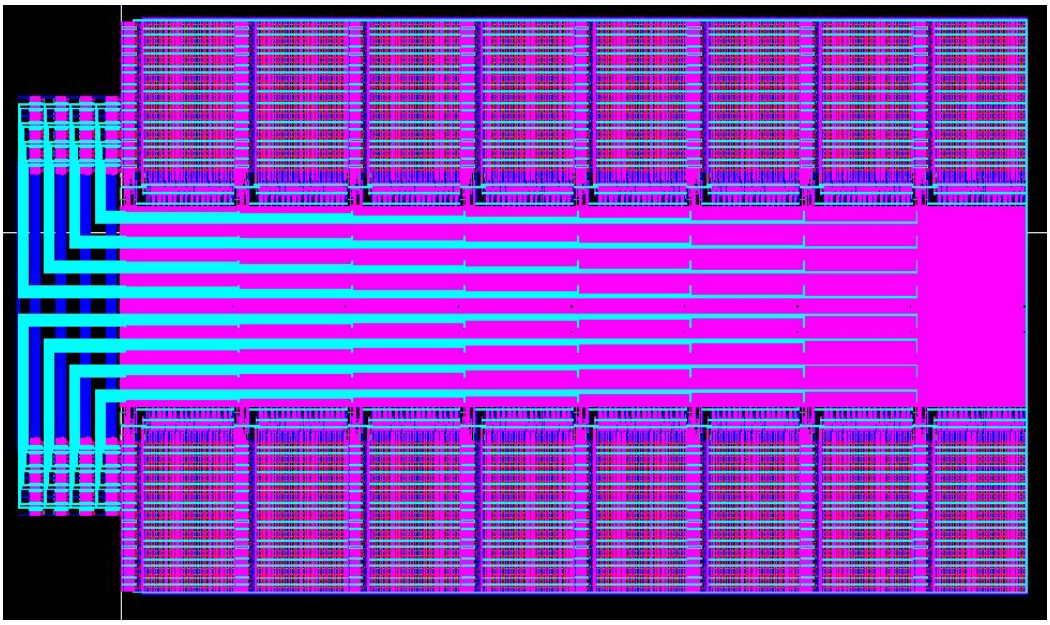


Figure 24: 4kb Multibank memory

APPENDIX B: Testing Code

1 port memory cell:

```
t word bit bitbar cell cellbar

|****write a 1

l bitbar
h word
s 10
l word
assert cell
assert cellbar

|****read a 1

h bit bitbar
s 10
x bit bitbar
h word
s 10
assert bit
assert bitbar

|****write a 0

l bit
h word
s 10
l word
assert cell
assert cellbar

exit
```

2 port memory cell:

t read0 write0 word0_w word0_r bit bit_bar

|****write a 0
l write0
l word0_r
h word0_w
s 10
assert bit
assert bit_bar

|****read a 0
h bit bit_bar
s 10
x bit bit_bar
l word0_w
h word0_r
s 10
assert bit
assert bit_bar

|**** write a 1
h write0
l word0_r
h word0_w
s 10
assert bit
assert bit_bar

|****read a 1
h bit bit_bar
s 10
x bit bit_bar
l word0_w
h word0_r
assert bit
assert bit_bar

exit

4 port memory cell:

t read0 read1 write0 write1 word0_r word1_r word2_w word3_w bit bit_bar

|****write a 0 from write0

l write0
l write1
h word2_w
l word3_w
l word0_r
l word1_r
s 10
assert bit
assert bit_bar

|*****read from both ports

h read0 read1
s 10
x read0 read1
h word0_r
h word1_r
l word2_w
l word3_w
s 10
assert read0
assert read1

|****write a 1 from write1

l write0
h write1
l word2_w
h word3_w
l word0_r
l word1_r
s 10
assert bit
assert bit_bar

exit

VITA

Sunil Kumar Lakkakula

Candidate for the Degree of

Master of Science

Thesis: VLSI DESIGN AND COMPARISON OF BANK MEMORY WITH MULTIPORT MEMORY CELL VERSUS CONVENTIONAL MULTIPORT AND MULTIBANK SRAM MEMORY

Major Field: Electrical Engineering

Biographical:

Personal Data: Born in Chirala, AP, India on April 9, 1986

Education:

Bachelors: Earned Bachelors Degree of Technology in Electrical Engineering on April 2007.

Masters: Completed the requirements for the Master of Science in Electrical Engineering at Oklahoma State University, Stillwater, Oklahoma in Dec, 2009.

Name: Sunil Kumar Lakkakula Date of Degree: December, 2009

Institution: Oklahoma State University Location: Stillwater, Oklahoma

Title of Study: VLSI DESIGN AND COMPARISON OF BANK MEMORY WITH MULTIPORT MEMORY CELL VERSUS CONVENTIONAL MULTIPORT AND MULTIBANK SRAM MEMORY

Pages in Study: 37 Candidate for the Degree of Master of Science

Major Field: Electrical Engineering

Scope and Method of Study: The main focus of this thesis is to determine whether designing a bank memory with multiport memory cell (hybrid design) is advantageous over conventionally used multibank and multiport memory designs. The layout designs are created using Cadence Virtuoso with the ami06u C5N technology process and simulated using IRSIM.

Findings and Conclusions: The area of multibank, multiport and hybrid designs are compared to each other for 4kb, 16kb and 64kb memory sizes. I found that hybrid is advantageous over multiport design in case of bigger memories. Also a delay comparison was done for 4kb memory size and found that hybrid is faster in its read ability in comparison to multibank memory.

ADVISER'S APPROVAL: Dr. Louis G. Johnson