ANALYSIS AND DESIGN METHODOLOGY FOR PCB AND INTEGRATED CIRCUIT PULSE TRANSFORMER

By

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ANALYSIS AND DESIGN METHODOLOGY FOR PCB AND INTEGRATED CIRCUIT PULSE TRANSFORMER

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In loving memory of my mother.

This thesis is the result of research I have realized at the MSVLSI group of Oklahoma State University. Given this opportunity, I would like to thank all the people who have helped me directly or indirectly in completion of this work.

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Nomenclature

AC	Alternating Current
C_d	Distributed Capacitance
CISS	Input Capacitance
CMOS	Complementary metal Oxide semiconductor
CLT	Coreless Transformer
DC	Direct Current
DUT	Device under Test
FET	Field Effect Transistor
IC	Integrated Circuit
I_s	Secondary current
I_p	Primary Current
JFET	Junction Field Effect Transistor
K	Coefficient of Coupling
L_p	Inductance of primary winding
L_s	Inductance of secondary winding
L_{lk}	Leakage Inductance
M, L_m	Mutual Inductance
N	Number of Turns
PCB	Printed Circuit Board
Q	Quality Factor
R_g	Source Resistance
SiC	Silicon Carbide
SMPS	Switch Mode Power Supply
VNA	Vector Network Analyzer
V_p	Primary Voltage
V_s	Secondary Voltage
Z_l	Load Impedance

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Chapter 1

Introduction

1.1 Background:

As electrical circuits become more complex, the demand for expert electrical engineering becomes more critical. Precise engineering is essential at every stage of designing a circuit, and it is equally important in the design of the components. One component of many that must be carefully designed is the gate-drive transformer in a switch-mode power supply (SMPS).

The demand for power supplies in modern electronic equipment is ever increasing as it is essential for all electronic systems. The need for compactness of the power converter has led to the increase in operating frequency and the use of planar magnetics. Additionally, the efficiency of the switch mode power supplies can be increased by using higher operating frequencies.

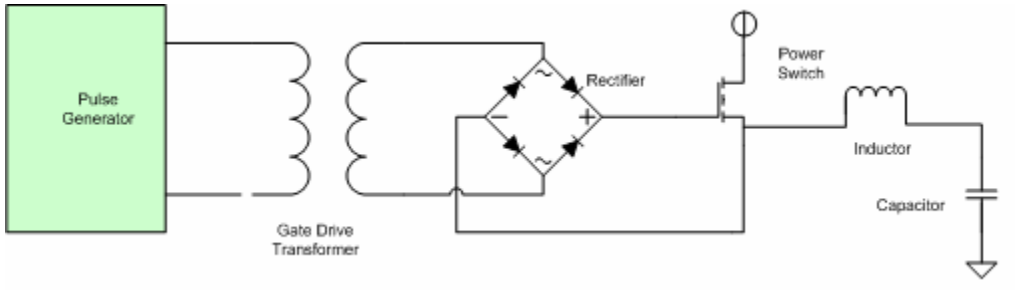


Figure1.1: Conceptual Gate Drive Circuit.

Gate drive circuits for power inverters and converters often require electrical isolation. Among the various isolation techniques, the isolation transformer along with optical coupling is probably the most widely used method. As the frequency of the switching operation increases the size of the passive components, such as output capacitors, transformers and inductors are further reduced in proportion to the switching frequency.[18]

Nowadays the common solution to realize either functional or safety isolation for low and medium power applications is the usage of optocouplers, discrete transformers, or monolithic level-shifters. All of them have their typical advantages and disadvantages which are well known. The primary goal of the coreless transformer technology is to combine these advantages by avoiding at the same time the disadvantages. This means in detail a high insulation capability, no ageing and therefore constant reliability over the projected lifetime, small package size, easy integration of additional logic functions, and cost effective production. The basic principle of the coreless transformer (CLT) is the implementation of a micro planar transformer embedded within the semiconductor process. The transformer provides the desired galvanic isolation and signal transmission between input and output stages.

Problems in High Frequency Magnetics:

The problem with miniaturization of power conversion circuits such as AC to DC switch mode power supplies and DC to DC converters is the construction of the inductors and transformers. In general, the increased switching frequency leads to a reduction in size of the magnetic components but at frequencies in MHz region several other issues arise. The core materials commonly used in 20-500 KHz region have increased hysteresis and eddy current loss at the higher frequencies. Also the problems due to the skin effect and proximity effect get added up at high frequency.

Commonly used magnetic core-based transformers for isolated gate drive circuits or low-power converters require a manual winding process, which not only increases the labor

cost, but also prohibits full automation of the circuits in their manufacture. This is the motivation to use coreless transformers (CLT).

1.2 Motivation

The goal this thesis is to design a compact and cost efficient gate drive circuitry to operate at high temperatures for switch mode power supplies (SMPS). A gate drive transformer is needed in SMPS to control the timing of the circuit. These gate-drive transformers are basically pulse transformers that are used to drive the gate of an electronic switching device. This work essentially concentrates on designing 1:1 coreless pulse transformers that would drive the gate of both silicon carbide JFET and CMOS power FETs and validating via simulation the feasibility of fabrication an integrated high side switch controller. For power FETs the typical worst case switching task can be bounded by the following device parameters; CISS less than 5 nF, Qg < 100nC, V_{GS} < 10V. For modern CMOS processes off chip drive is accomplished with legacy I/O devices of 2.5 and/or 3.3V. Typical coreless switching supplies operate in the frequency range of 0.1 to 500MHz.

Traditionally, magnetic cores are used in transformers for providing good magnetic paths for the energy to transfer from the primary to the secondary, or vice versa. Because of the relatively high manufacturing cost of manually wound transformers and inductors, recent research has focused on making transformer and/or inductor windings on printed circuit boards (PCB's). Besides the cost factor, such a PCB-based transformer and inductor winding concept is highly attractive to the automation of the manufacturing process.

Planar transformers provide a good solution for high-frequency switching-mode power supplies (SMPS). Since this class of transformers has advantages that improve the SMPS performance, their use has grown in recent years. Some of the high frequency parasitics can be drastically reduced due to their planar geometry and the proximity of the windings [4]. Leakage inductance can be drastically reduced in these transformers due to the

proximity of the windings. The AC resistance is also reduced due to the high perimeter or area ratio of the conductors [1].

Critical coreless transformer parameters with upper bounds on the requirements can be summarized as follows:

Table1.1: Critical parameters for the coreless transformer for high side switching.

Parameter	Estimation Factors	Typical worst case
Turns ratio	V_{GS}/I/O drive	1 to 4
I_{peak} Secondary	$Qg/(t_{rise} + t_{ondelay})$	1 Amp
V_p Secondary	Power MOS V_{GS}	10V
Secondary load (CMOS)	CISS	5 nF
Secondary loading (SiC JFET)	CISS & R_{GS}	200pf & 100ohm

Two of the more critical electrical parameters to control when designing a pulse transformer are the leakage inductance and winding capacitance. A high leakage inductance and winding capacitance may result in an unusable transformer and cause an undesirable output signal as a result of phase shift and overshoot. Leakage inductance occurs when windings have poor coupling. High winding capacitance results when a winding has many turns and the turns are not laid uniformly during the winding process or windings are too closely spaced horizontally or vertically. Therefore, proper layout of the windings is an important consideration for the transformer design and it is reviewed in chapter 4. Figure1.2 is an example of proper layout of a 1:1 transformer structure on a PCB board.

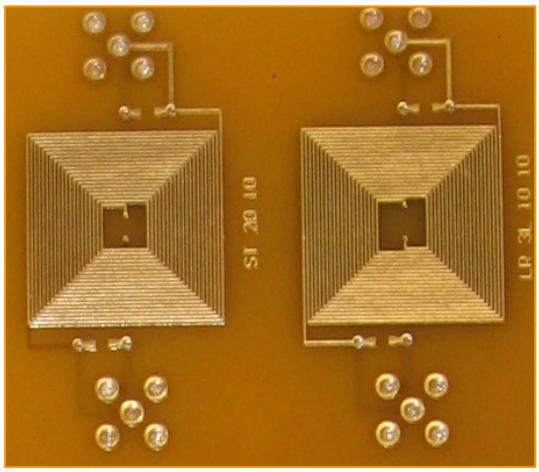


Figure 1.2: PCB Transformer.

1.3 Organization of the Thesis

An overall review of the characteristics of a CLT is presented in Chapter 2. This includes a brief description of the ideal and non ideal characteristics of transformer and a physical overview of transformer with the effect of various fields on the performance. The effect of high frequency on windings including the skin effect and proximity effect are also described. The basic transformer structures such as planar and stacked structures and a description of their performance measures are presented in the concluding section of Chapter 2.

Chapter 3 gives a detailed description of the equivalent circuits for a coreless pulse transformer. It includes frequency modeling of the transformer with respect to different frequency bands; low, mid and high. After making suitable assumptions regarding the circuit parameters, the transformer equivalent model for low frequency, midband frequency and high frequency are described along with the transfer functions and the input impedance. Chapter 3 includes the modeling of the pulse transformer using the described models to design the transformer with the desired required rise time, droop and damping factor. The design equations developed to design the coreless pulse transformer are also presented.

The Implementation of the coreless pulse transformer on a PCB/IC substrate has been presented in Chapter 4. It includes a brief overview of the characteristics of the PCB/IC transformers and their advantages and disadvantages. A discussion of the influence of the various geometrical parameters on the layout of the transformers structures is presented. This chapter is concluded with a brief summary of the software used and the layout structure.

Chapter 5 presents a discussion of the results obtained and the validation of the design methodology. The performance measures, namely coefficient of coupling and quality factor of the designed structure are presented. Also transformer parameters such as the inductance and the leakage inductance are determined and validated with the estimated values. The rise time of circuit for the given load is simulated and verified with the specified requirements. Also, the various assumptions made in the development of the design equations are verified.

A brief summary of this research work, its application, advantages and the future scope is presented in the chapter 6.

Chapter 2

Transformer Model

This chapter discusses the basic characteristics and desired properties of coreless transformer (CLT). It introduces the fundamentals of the ideal transformer and its variation in the practical transformer followed by the physical overview of the transformer and the effect of various time varying fields on the transformer windings. The high frequency effect on the windings which are the skin effect and the proximity effect are discussed. The classification of the basic transformer structures and the performance measures of CLT are described. This chapter is summarized by the comparison of the performance measures of the different structures which is used to determine the required structure for the current application.

2.1 Transformer Fundamentals:

A transformer is an alternating current device that transforms voltage, current and impedance. Faraday's law of electromagnetic induction is the principle of operation of the transformer: The induced *emf* equals the negative rate of time variation of the magnetic flux through the contour.[19]

2.1.1 Ideal transformers:

A circuit model for an ideal transformer is shown in Figure 2.1. The magnetic flux produced by time-varying current I_p owing into the primary winding, induces a time-varying current of I_s in the secondary winding.

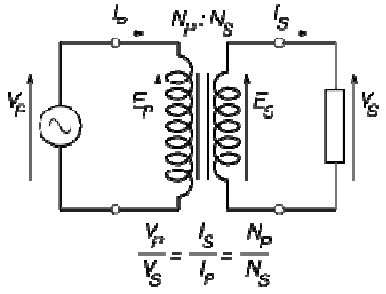


Figure2.1: Transformer Model.

The terminal voltages and currents of this ideal transformer are related as follows:

$$\begin{bmatrix} V_s \\ V_p \end{bmatrix} \equiv \begin{bmatrix} j\omega L_p & j\omega L_m \\ j\omega L_m & j\omega L_s \end{bmatrix} \begin{bmatrix} I_p \\ I_s \end{bmatrix} \tag{2.1}$$

Where L_p and L_s are the self-inductance of the primary and secondary. L_m is the mutual inductance between the primary and secondary. The magnetic coupling coefficient *k* is given by

$$K = \frac{L_m}{\sqrt{L_p \times L_s}}, \tag{2.2}$$

where L_p and L_s are the primary and secondary inductance respectively. For an ideal transformer coefficient of coupling is 1 i.e. magnetic coupling and energy transfer between the primary and secondary windings is maximum. In order to have maximum voltage or current transfer the coefficient of coupling needs to be close to 1.

2.1.2 Non Ideal transformers:

The non idealities of a practical transformer include the parasitic capacitance, leakage inductance and primary and secondary resistance due to ohmic losses in the windings. The leakage inductance accounts for the reduced magnetic coupling between the primary and secondary windings.

$$L_{lk} = (1 - K^2)\sqrt{L_p L_s} \tag{2.3}$$

In the case of the 1:1 transformer the above equation reduces to

$$L_{lk} = (1 - K^2)L_p$$

These parasitic values can be taken care of by proper design of the transformer.

2.2 Physical Overview:

The time varying voltage applied between the ends of the winding induces a two electrical fields and a magnetic field. The reasons and their effects on the behavior of the two windings are discussed below:

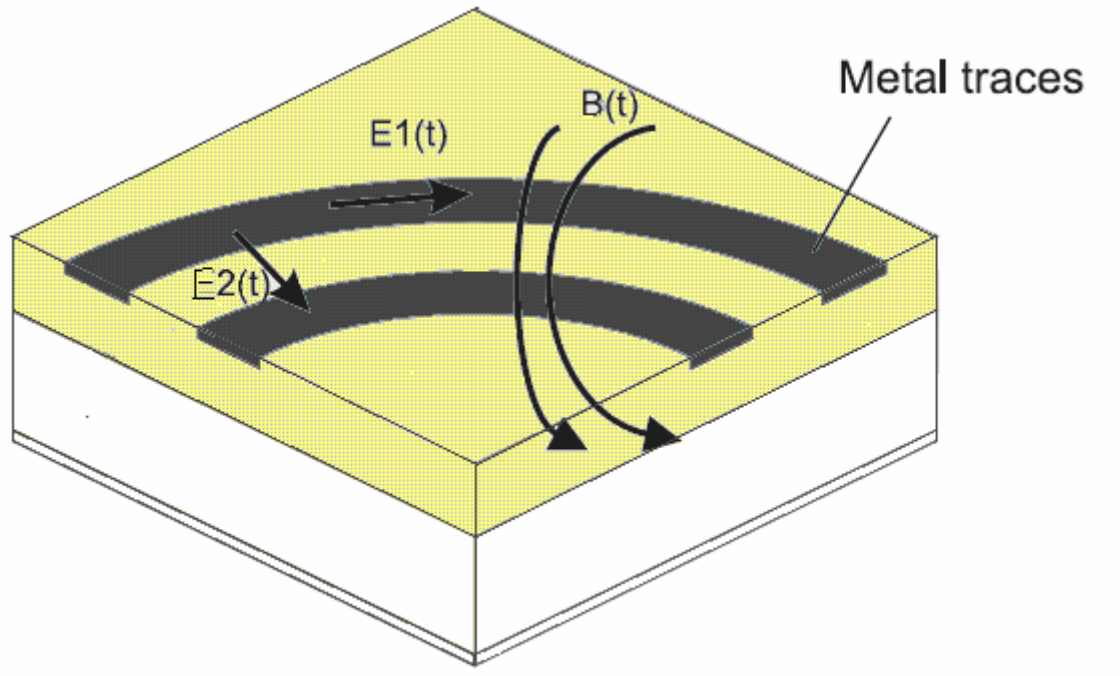


Figure2.2: Time varying fields in the windings.

- **Magnetic Field B (t):** The magnetic field is induced by the time varying current flowing along the conductor and it produces self and mutual coupling between the metal tracks.
- **Electrical Field E1(t):** The electrical field is generated along the winding due to the existing voltage difference between the two ends and it *causes ohmic losses due to the resistivity* of the metal track.
- **Electrical Field E2 (t):** The electrical field between the strips caused due to voltage difference between the adjacent strips *induces capacitive coupling* between the coils.

2.2.1 Inductance:

The inductance of an inductor has two components; self and mutual inductance.

2.2.1.1 Self Inductance:

According to Ampere's law, an alternating current flowing along a conductor induces a magnetic field .The self inductance of a rectangular conductor derived by Grover [16] and written as:

$$L_{self} = 2 \times l \left\{ \ln\left(\frac{2 \times l}{w+t} \right) + 0.5 + \frac{w+t}{3 \times l} \right\} \qquad (2.4)$$

Where L_{self} denotes the conductor self inductance in nH and l, w and t represents the length, width and the thickness of the conductor in cm respectively.

This equation is used to determine the inductance of the rectangular spiral structure which is used for the layout of the PCB/IC transformer. Using the equation 2.4, the inductance of the windings of the coreless transformer is determined or modeled.

2.2.1.2 Mutual Inductance:

Mutual inductance M_{12} between two circuits 1 and 2 is defined as the ratio between the flux generated by circuit 1 crossing to circuit 2(Φ_{12}) and the current that flows in circuit1(I1).It is determined by the equation:

$$M_{12} = \frac{d\phi_{12}}{dI_1} \tag{2.5}$$

In case of two parallel conductors the mutual inductance is defined as

$$M=2xLxQ \tag{2.6}$$

Where M is the inductance in nH, L is the length of the conductor in cm and Q is a coefficient that depends on geometry.

Mutual inductance between two segments depends on their angle of intersection, length and separation. Two orthogonal metal tracks have no mutual inductance as their magnetic flux is not linked together. Hence for the mutual inductance to be more the tracks should be parallel and the separation should be minimal depending on the process technology.

2.2.2 Resistance:

When a DC current flows through a conductor, the current distribution is uniform over its entire surface. The resistance of the conductor is given as:

$$R = \rho \times \frac{l}{wt} \tag{2.7}$$

Where ρ is the resistivity, l is the length and A equal wxt the conductor area where w and t are the width and thickness respectively. As the frequency increases, the resistance is no longer constant due to the fact that the distribution of the current is not uniform across the conductor cross section. The dependence of the resistance with frequency not only depends on the conductor itself (skin effect) but also on the influence of neighboring strips (proximity effect).

For coreless transformers, the influence of the skin effect and the proximity effect are negligible (This is dealt with in detail in the high frequency section (2.3)) so the a.c

winding resistance is drastically reduced 1]. The methods to reduce the D.C winding resistance is discussed in chapter 4.

2.2.3 Parasitic Capacitance:

When a voltage is applied to the ends of a coil, it creates a voltage distribution along its metal tracks. The structure metal/dielectric/metal used in both PCB and IC appears as a parasitic capacitance between the metal tracks. Due to the voltage difference between the plates, energy will be accumulated in the capacitor. This capacitance includes both the adjacent capacitance between the tracks on the same metallic layer and potentially the vertical capacitance between tracks located on different layers. This is applicable for both PCB and the IC CLT layout and only becomes significant at higher frequencies.[1]

2.3 High Frequency Effects on the Winding:

2.3.1 Skin Effect:

The skin effect of a conductor accounts for the alteration of the current density distribution from the magnetic field generated by the current itself. When a magnetic field generated by a current in a conductor crosses its cross-section, it induces a force over itself. This force is perpendicular to the magnetic field and the direction of the current flow. Thus the current is pushed toward the outer surface of the conductor. The higher the frequency is, the higher the resistance of the conductor will be, since the current is restricted to a small part of its total cross-sectional area.

The influence of the skin effect over the resistance of a conductor is evaluated by the means of the skin depth. This parameter is defined as the equivalent thickness of a hollow conductor having the same resistance at the frequency of interest. The average current depth (skin depth) is a function ω (in rad/sec), the magnetic permeability of the conductor μ and the volume resistivity p.

$$SkinDepth = (\frac{2p}{\omega\mu})^{0.5} \quad (2.8)$$

At low frequencies when the skin depth is comparable or greater than the wire radius only the DC resistance of the wire is taken into account. When the skin depth is less than the wire radius, the resistance per inch goes up proportional to the square root of the frequency.

In case of both the PCB and IC Planar transformers, the skin depth is much higher than the conductor thickness and hence the influence of the skin effect on the resistance is negligible for wire thickness less than 3um at approximately 3GHz. For the flat rectangular conductor that are used in the case of the planar PCB/ IC transformers the critical depth is half the conductor thickness. The AC resistance is also very low in planar transformers. The reason is that the area/perimeter ratio of the planar transformer conductors is very low. This makes possible a better usage of the copper because the current flows across the whole conductor section, reducing skin effect. The optimum conductor height to be used is given by the skin depth which will also be dealt in chapter 4 while discussing the geometrical parameters.[4]

2.3.2 Proximity Effect:

Proximity effects in a conductor are a consequence of the influence of an external time-varying magnetic field over the conductor and so disturb the flow of the high frequency currents. In this case, an induced current is generated regardless whether or no there is a current flow through the conductor. In case there is an alternating current, the skin effect and the proximity effect will add together, changing the current distribution and increasing the resistance of the conductor.

The magnitude of the proximity effect at equilibrium is determined by the ratio of wire separation between the centers to the wire diameter. The proximity effect is most

noticeable when two wires are almost touching. This may lead to reduced total loop inductance.

The induced currents in the tracks of a spiral inductor have a negative side effect, especially in the inner coils turns since it is in the centre of the spiral where the magnetic field reaches its maximum intensity. In a fully winding coil (the coil turns reach the centre) a large portion of the magnetic field passes through the inner coil turns, inducing in these turns a strong current density and therefore increasing their resistivity.

In order to reduce this effect the inner coils of the primary and secondary winding of the planar coreless transformer should not be closely packed. Hence by maintaining some internal radius the influence of the proximity effect on the transformer windings can be effectively eliminated [21] which is again dealt in chapter 4.

2.4 Performance measures of the transformer:

Based on the application and the operating frequency requirements the transformer design varies. For the DC-DC converter the transformer needs to be optimized for the voltage transfer and the coupling.

2.4.1 Coefficient of coupling (K) and Turn ratio (N)

For voltage or current coupling, high coupling coefficient and specific turns ratio is desired. To increase *k*, the spacing between the primary and secondary should be as small as possible, constrained by the coupling capacitance and self-resonant frequency. The turn ratio will be constrained by the area limitations.

2.4.2 Quality Factor (Q):

For a simplified transformer model where all the capacitances are ignored and only the loss of the inductors are included .The quality factor of the primary and the secondary windings are given as:

$$Q_p = \frac{\omega \times L_p}{R_p} \quad ; \quad Qs = \frac{\omega \times Ls}{Rs} \tag{2.9}$$

Where, Rp and Rs are the series resistance of the primary and the secondary winding. So for the quality factor to be high the inductor impedance must be much greater than (approximately 6 to 8) the winding resistance.

2.5 Basic transformer structures:

Based on whether the coupling between the primary and secondary is lateral or vertical the transformers can be classified as:

- Planar transformer
- Stacked transformer.

2.5.1 Planar Transformer:

In planar transformers the coupling between the windings is lateral. That is the primary and secondary windings are placed in same layer. Hence the planar transformers occupy larger area and have a small coefficient of coupling and greater resistance and lower Q.

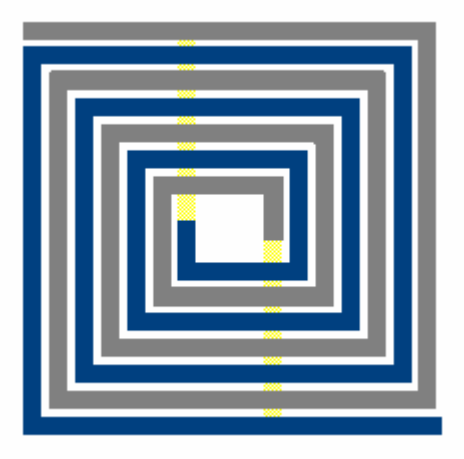


Figure 2.3: Planar Transformer (single plane).

2.5.2 Stacked Transformer:

As the name suggests in stacked transformers the primary and the secondary are stacked in different layers and hence the coupling is both vertical and lateral increasing inductance. Due to the stacked structure these transformer occupy lesser area and also have better coefficient of coupling. For an identical area with wider traces and equal turns; resistance reduces, L remains approximately constant or and as a result Q increases. However, the coupling capacitance between the primary and secondary windings increases.

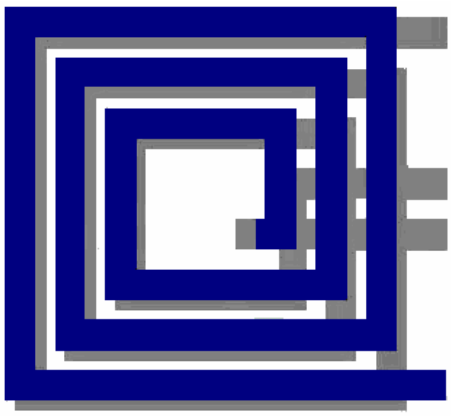


Figure 2.4: Stacked Transformer (two planes).

2.5.3 Segmented and Interleaved structure:

One of the techniques to improve the performance the transformer is to split the wide traces into multiple parallel segments and interleave to improve *k*. This also helps in mediating the proximity effect. Because the effective width of the primary or secondary winding can be enlarged, the self-inductances *Lp* and *Ls* are reduced while the resistance remains about the same for an equal area. So the Q_P and *Qs* will be reduced at low frequencies. However, the coupling capacitance between the primary and secondary windings increases.

Hence, thought the segmentation improves the coefficient of coupling but the decrease of Q offsets the benefits.

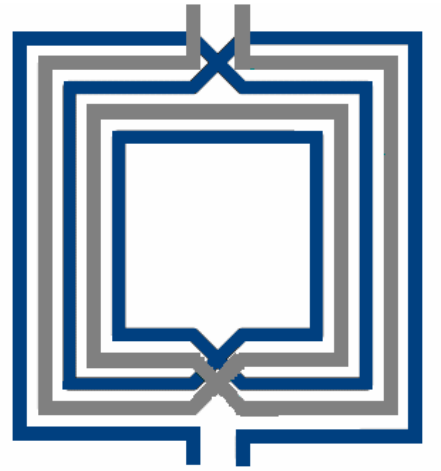


Figure2.5 : Segmented and Interleaved stacked transformer (two plane).

These are the various transformer topologies that are available for the layout of the windings for both PCB and IC structures.

2.6 Summary:

The different topologies described above offer varying trade-offs among the self inductance and series resistance of each port, the mutual coupling coefficient, the port-to-

port and port-to-substrate capacitances, resonance frequencies, symmetry and area. These desired characteristics of the transformer are application dependent.

Table 2.1: Performance measures of different structures for equal areas and turns.

Transformer Type	Area (Assuming equal Inductance)	Coefficient of Coupling (K)	Self Inductance	Quality Factor	Self resonance
Planar	High	Low	Low	Low	High
Stacked	Low	High	High	High	Low
Segmented Stacked	Low	High	Low	Low	High

The stacked transformer (Fig.2.4) uses multiple metal layers and exploits both vertical and lateral magnetic coupling to provide the best area efficiency, the highest self-inductance and highest coupling *(k* ≈ 0.8).[17] The main drawback is the high port-to-port capacitance, or equivalently a low self-resonance frequency. In some cases, such as narrowband impedance transformers, this capacitance may be incorporated as part of the resonant circuit. Also, in modern multi-level processes, the capacitance can be reduced by increasing the oxide thickness between spirals. For example in case of IC, in a five metal process, 50 - 70% reductions in port-to-port capacitance can be achieved by implementing the spirals on layers five and three instead of five and four. The increased vertical separation will reduce ***k*** by less than ***5%.*** One can also trade off reduced coupling for reduced capacitance by displacing the centers of the stacked inductors. [1]

Chapter 3

Frequency Modeling of the Transformer

This chapter discusses the frequency models used to represent a transformer and based on these models the 1:1 coreless pulse transformers are developed by making suitable assumptions. Using these models some design equations have been developed for designing the coreless pulse transformer for a given rise time requirement. Based on these equations the circuit parameters of leakage inductance, allowable load capacitance and resistance and the source resistance can be estimated for required rise time with proper damping.

3.1 Transformer equivalent circuit:

Equivalent circuits are used to model the performance of the transformers with acceptable accuracy. Although equivalent circuits are not exact replicas of real transformers, they are sufficiently close to realize accurate results for engineering design. A detailed pulse transformer equivalent circuit is modeled as shown in Figure 3.1

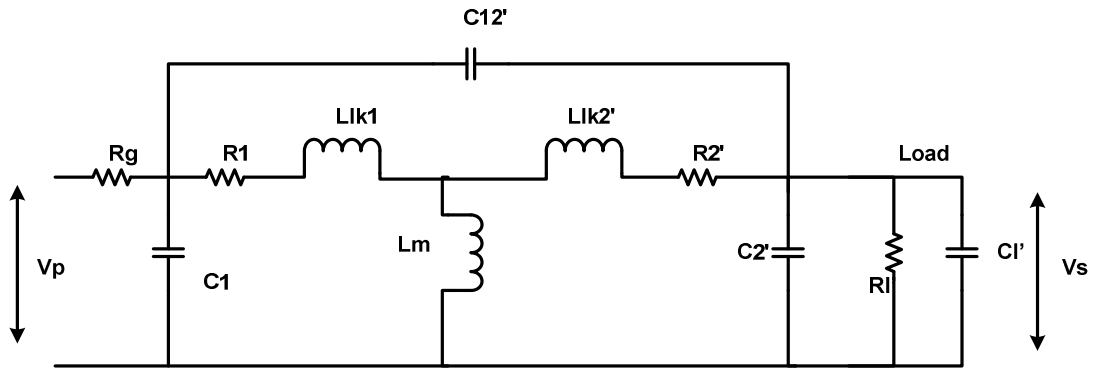


Figure3.1: Transformer Equivalent Circuit.

The leakage inductance of both coils has been modeled by an inductor in series with resistance. The stray capacitance between the turns of the coils is represented by a capacitor placed across the terminals of the coils. The capacitance is larger for coils with more turns. Although the capacitance is distributed in practice, it is lumped in the equivalent circuit in order to simplify the analysis. The mutual inductance is represented by shunt inductor Lm. As no magnetic core is used, the core loss resistance in the traditional low-frequency model is ignored. The transfer function of the complete equivalent circuit is given as equation 3.1.

$$\frac{V_s}{V_p} = \frac{Z_l(Z_pZ_s + Z_mZ_p + Z_mZ_s)}{Z_pZ_l + Z_pZ_m + Z_pZ_s + Z_pZ_sZ_l + Z_mZ_l + Z_mZ_s + Z_pZ_mZ_l + Z_mZ_sZ_l} \qquad (3.1)$$

The transfer function of the complete equivalent circuit is quite complex. So, the equivalent circuit is broken up into several equivalent circuits, each of which is valid for a limited set of operating conditions. Each simplified circuits is analyzed for its pertinent operating conditions to arrive at a set of design equations assisting the design of a transformer.

3.1.1 Equivalent circuit for Low Frequency:

In the low frequency, the transformer acts like a high pass filter. Above the corner frequency, the output voltage is nearly equal to the input voltage. Below the corner frequency the output voltage is attenuated due to the presence of the shunt inductor Lm. The distributed capacitance and the leakage inductances can be neglected. The equivalent circuit for a coreless transformer at low frequencies with a RC load is as shown in Figure 3.2.

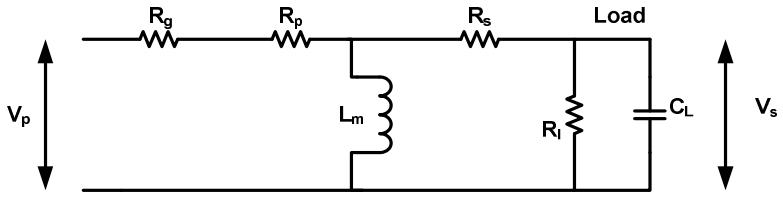


Figure 3.2: Low Frequency Equivalent Circuit.

For the above equivalent circuit it is assumed that $R_p << R_g$ and $R_s << R_l$, hence the primary and the secondary resistances are reduced to R_g and R_l.

The transfer function for the voltage and current and the input impedance for the transformer are given as in equations 3.2, 3.3 and 3.4 respectively.

$$\frac{V_s}{V_p} = \frac{sL_m * Z_l}{sL_m(Z_l + R_g) + R_g * Z_l}, \tag{3.2}$$

$$\frac{I_s}{I_p} = \frac{R_g(Z_l + sL_m)}{sL_m(Z_l + R_g) + R_g * Z_l} \tag{3.3}$$

$$Z_{total} = \frac{sL_m * Z_l + R_g(Z_l + sL_m)}{Z_l + sL_m} \tag{3.4}$$

This low frequency model and the transfer function determined are used in developing the low frequency model of the pulse transformer. This model is required while determining the droop of the pulse signal generated and in order for the droop to be less the impedance caused by the mutual inductance must be much greater than that of the load.($X_m >> X_l$)

3.1.2 Equivalent circuit for Midband Frequency:

This is the intended operating range for the coreless transformer. The frequency is high enough that the mutual inductance can be neglected and low enough that the leakage inductance and distributed capacitance are still not a concern. The resulting equivalent circuit and the transfer function for both voltage and current and the input impedance are as in equations 3.5, 3.6, 3.7:

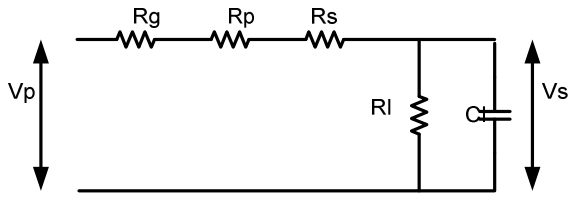


Figure 3.3: Equivalent circuit for Midband Frequency.

$$\frac{V_s}{V_p} = \frac{Z_l}{Z_l + R_g} \tag{3.5}$$

$$\frac{I_s}{I_p} = \frac{R_g}{Z_l + R_g} \tag{3.6}$$

$$Z_{total} = Z_l + R_g \tag{3.7}$$

3.1.3 Equivalent circuit for High Frequency:

The factors that influence the high frequency response of a transformer are the leakage inductance, winding capacitance, source impedance and the load impedance. At higher frequencies, the leakage inductance begins to dominate the transformer's response. The following is the equivalent circuit for the high frequency model where again $R_p << R_g$ and $R_s << R_l$. For simplification of the model and the calculations, it is assumed that the winding capacitances or the parasitic capacitance are lumped together with load capacitance and denoted as distributed capacitance (C_d).

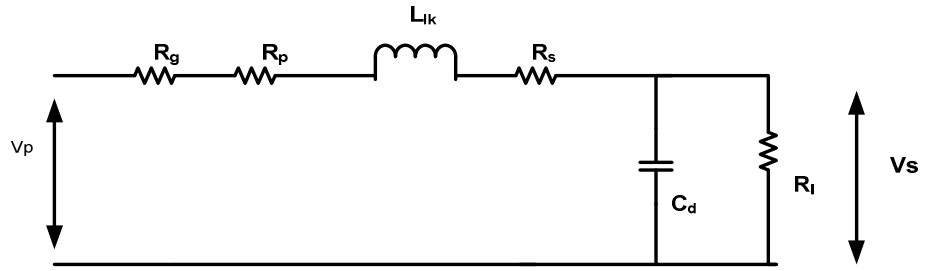


Figure 3.4: Equivalent Circuit for High Frequency.

The high frequency equivalent circuit transfer functions for voltage and current are given:

$$\frac{V_s}{V_p} = \frac{Z_l}{Z_l + sL_{lk} + R_g} \tag{3.8}$$

$$\frac{Is}{Ip} = \frac{sL_{lk} + R_g}{Z_l + sL_{lk} + R_g} \tag{3.9}$$

$$Ztotal = Z_l + R_g + sL_{lk} \tag{3.10}$$

This model and the equations are useful in determining the rising and falling response of the pulse transformer due to the high frequencies present in it. Using these, a set of

equations can be formulated to design the pulse transformer for a given set of constraints and requirements.

3.2 Pulse Transformers:

Gate-drive transformers are essentially pulse transformers that are used to drive the gate of an electronic switching device. Assuming optimal values for rise time, droop and overshoot for the application is what discriminates the gate-drive transformer from other transformers. There are several factors external to the transformer that affects its operation. These are:

1. Impedance of the source
2. Impedance of the load
3. Pulse frequency or Pulse width
4. Relationship of the input and output impedances to the frequency and the amplitude of the signal.

Shape of a typical pulse is shown below:

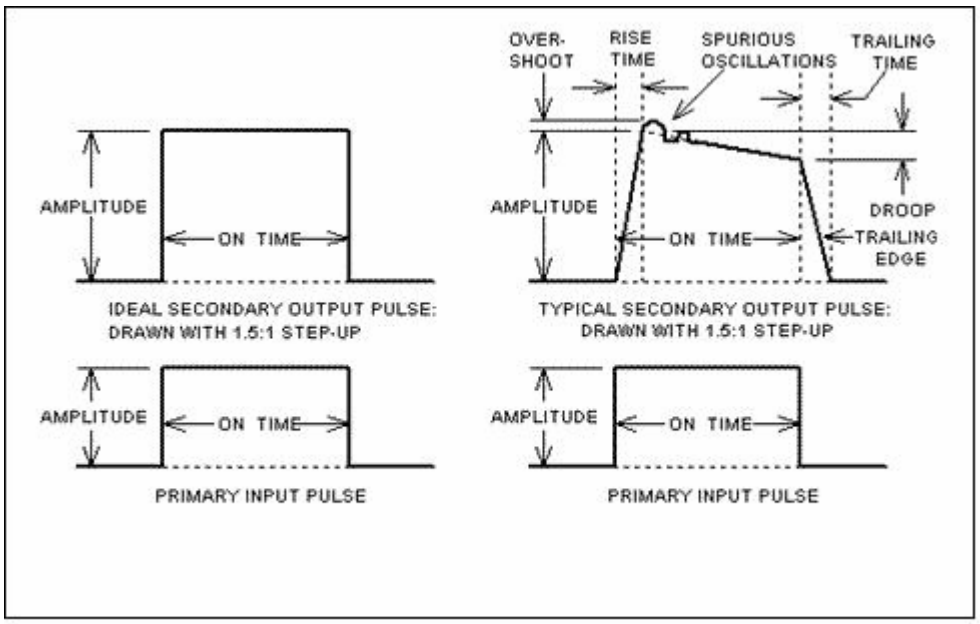


Figure 3.5: Typical Pulse Waveform.

A pulse applied to the primary winding of an ideal transformer would provide an exact replica of the pulse's waveform at its unloaded secondary, scaled in amplitude by the transformer's turns ratio. In practice, a transformer exerts a number of distortions on the pulse which in extreme cases may cause the resultant pulse to be unusable.

Due of the complex nature of the pulse, it is often divided into three stages or phases which are analyzed separately. The rising edge of the pulse is analyzed using the high frequency equivalent circuit for step up or step down transformers due to the high frequencies present in the edge that must be supported by the transformer. The top of the pulse is analyzed using the low frequency equivalent circuit since it is a low frequency. The trailing edge is again analyzed using the high frequency model.

3.2.1 Edge Response:

The edge periods consist of rise time, fall time and ringing, which encroaches the top period if it is extreme. We may refer to the high-frequency equivalent circuit for our analysis of the edge periods as shown in the Figure 3.4.

The equations 3.8 through 3.10 are applicable for the edge response of the pulse. For the both the step up transformer and the 1:1 transformer with a RC load the transfer function is obtained from the following analysis.

Writing the nodal equation for the high frequency model shown in Figure 3.4, the following transfer function is obtained:

$$V_p = \frac{\dfrac{R_l}{1+sR_lC_d}}{R_g + sL_{lk} + \dfrac{Rl}{1+sR_lC_d}} V_s \qquad (3.11)$$

Simplifying the above equation:

$$\frac{V_S}{V_p} = \frac{R_L}{s^2(R_L C_d L_{lk}) + s(L_{lk} + R_L R_g C_d) + R_L + R_g}$$

$$\frac{V_S}{V_p} = \frac{Rl}{R_L C_d L_{lk}} \frac{1}{s^2 + s(\frac{L_{lk} + R_L R_g C_d)}{(R_L C_d L_{lk})} + \frac{R_L + R_g}{(R_L C_d L_{lk})}} \tag{3.12}$$

Where, $b = \frac{R_g}{L_{lk}} + \frac{1}{R_l C_d}$ $\qquad$ $c = \frac{R_l + R_g}{L_{lk} C_d R_l}$

The time domain response of the above equation is:

$$\frac{V_l}{V_g} = \frac{R_l}{R_l + R_g}\left[1 - \exp\left(\frac{-b}{2}t\right)\left(\frac{b}{\sqrt{b^2 - 4c}}\sinh\frac{\sqrt{b^2 - 4c}}{2}t + \cosh\frac{\sqrt{b^2 - 4c}}{2}t\right)\right] \tag{3.13}$$

$$\text{Damping factor } (\varsigma) = \frac{b}{2\sqrt{c}} = \frac{R_g R_l C_d + L_{lk}}{2\sqrt{R_l L_{lk} C_d (R_l + R_g)}} \tag{3.14}$$

$$\text{Natural Frequency} = \omega_n = \sqrt{\frac{R_l + R_g}{L_{lk} C_d R_l}} \tag{3.15}$$

Where, $C_d = C_l + C_p$.

If $4c < b^2$ then the circuit is over damped .If $4c > b^2$, then the circuit is under damped, and the overshoot is larger. The damping factor is defined in above equation. The rise time is less for lower damping factors but the overshoot also increases for lower damping factors. A damping factor of 0.707 is optimum in the sense that it produces the shortest rise time with no overshoot.

For step down transformers the following substitutions can be used:

$$b = \frac{R_l}{L_{lk}} + \frac{1}{R_g C_d} \qquad\qquad c = \frac{R_g + R_l}{L_{lk} C_d R_g}$$

The transformer's rise time may be calculated from the distributed capacitances and leakage inductance. It is assumed that the rise time is the period defined when the output pulse is between 10% and 90% of its full output level. The rise time of a second-order [8] is:

$$\text{Rise Time} = T_r = \frac{\Pi - \beta}{\omega_d} \tag{3.16}$$

Where $\beta = Cos^{-1}(\varsigma)$ and $\omega_d = \omega_n \sqrt{1 - \varsigma^2}$

In the case of CMOS IC design where the pulse generator has the same R_g in both rise and fall modes of operation, the fall time of the pulse is the same duration as the rise time, assuming there are no nonlinear elements involved in the circuit. Ringing of the output waveform occurs when the load and source are mismatch with the load impedance being much higher than the appropriate value to meet the matched condition (under damped condition) is potential problem.

But in the general case, the falling edge of the pulse transformer is analyzed using the high frequency model, with an assumption that the source is an open circuit. The distributed capacitance and the mutual inductance now produce a voltage on the load with stored energy. The equivalent circuit for the trailing edge consists of mutual inductance ($L_m = K\sqrt{L_p L_s}$), distributed capacitance and a shunt resistance parallel.

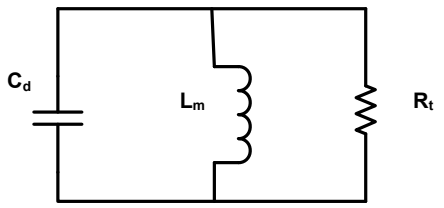


Figure 3.6: Equivalent Circuit for Trailing edge.

The response of the trailing edge circuit is given by:

$$\frac{E(t)}{E_0} = \exp(-2\Pi DT)(\cosh 2\Pi T\sqrt{D^2-1} - \frac{D+F}{\sqrt{D^2-1}}\sinh 2\Pi T\sqrt{1-D^2}) \quad (3.17)$$

$$\text{Damping Factor} = D = \frac{1}{2R_l\sqrt{L_m C_d}} \quad (3.18)$$

$$\text{Initial current Factor} = \text{F} = \frac{\tau}{\sqrt{L_m C_d}} \quad (3.19)$$

$$\text{Normalized Time} = \text{T} = \frac{t}{2\Pi\sqrt{L_m C_d}} \quad (3.20)$$

τ =Pulse width

3.2.2 Top of the Pulse:

The top period refers to the duration just after the pulse is applied to the transformer until just before the pulse is removed. The *droop* and backswing of a transformer are functions of its finite magnetizing inductance. By inspecting the low-frequency equivalent circuit shown in Fig3.2, we can see how a finite magnetizing inductance is the cause of droop and backswing. As the pulse continues in the high state, the mutual inductance begins to conduct more current away from the load resistance. Since the rate of change of the voltage during this period is relatively small, the parasitic capacitance or winding capacitance can be neglected. The ratio of the load voltage to the input voltage is given by:

$$\frac{V_l}{V_g} = \frac{R_l}{R_l + R_g}\exp\left[-\frac{R_l R_g}{L_m(R_l + R_g)}t\right] \quad (3.21)$$

The negative exponential form in the above equation indicates that the output voltage decays or droops with time. The larger mutual inductance is, the slower the rate of decay. It is necessary to know the source resistance during the top of the pulse in order to accurately estimate the droop.

Droop is caused by the increase in magnetizing current that occurs as the magnetic flux build around Lm. It may be approximated as follows by taking the derivative of the above function:

$$D = 100\frac{R_g R_l}{L_m(R_g + R_l)}t \tag{3.22}$$

Rearranging the above equation the minimum L_m can be determined to be

$$L_m = 100\frac{R_g R_l}{D(R_g + R_l)}t \tag{3.23}$$

In the case of $R_g << R_l$ the above equations are further simplified to

$$L_m = 100\frac{R_g}{D}t$$

3.3 Frequency Response:

From the circuit shown in Figure 3.1 we have seen that the transformer equivalent circuit consists of the leakage inductance, mutual inductance and parasitic capacitances. Among these the mutual inductance is responsible for the lower cutoff frequency, f_L. Similarly, the high-frequency cutoff point f_h, is dependent on a different set of elements: leakage inductance and parasitic capacitance.

Transformers having two or more decades of bandwidth ($f_h > 100\ f_L$) can be thought of as having simpler and distinctly different equivalent circuits below and above the mid-point frequency of their pass bands, typically the geometric mean of their low- and high- cutoff frequencies, $\sqrt{f_L f_H}$. As a result broadband transformer must be low Q.

3.4 Design Equations:

Gate-drive transformers are essentially pulse transformers that are used to drive the gate of an electronic switching device. Assuming optimal values for rise time, droop and overshoot, the application is what discriminates the gate-drive transformer from other transformers.

Hence using the high frequency models and their transfer function the pulse transformer can be designed for required rise time and damping ratio using the following set of design equations which have been taken from the section 3.2.1:

Rise Time = $T_r = \dfrac{\Pi - \beta}{\omega_d}$

$\beta = Cos^{-1}(\varsigma)$ and $\omega_d = \omega_n \sqrt{1-\varsigma^2}$

Where

Damping Factor = $\varsigma = \dfrac{b}{2\sqrt{c}} = \dfrac{R_g R_l C_d + L_{lk}}{2\sqrt{R_l L_{lk} C_d (R_l + R_g)}}$

Natural Frequency = $\omega_n = \sqrt{\dfrac{R_l + R_g}{L_{lk} C_d R_l}}$

From the discussion above we know that $R_l >> R_g$. Hence making the required substitutions in above equations we obtain the following equations:

$$\varsigma = \frac{R_g C_d}{2\sqrt{L_{lk} C_d}} + \frac{L_{lk}}{2R_l \sqrt{L_{lk} C_d}} \approx \frac{R_g C_d}{2\sqrt{L_{lk} C_d}} \tag{3.24}$$

$$\omega_n \approx \frac{1}{\sqrt{L_{lk} C_d}} \tag{3.25}$$

Substituting these equations into rise time equation and for the damping ratio of 0.707 as described in section 3.2.1 we get the new rise time equation as:

$$T_r = 3.11\sqrt{L_{lk} C_d} \approx 3.11\sqrt{L_{lk} C_L} \tag{3.26}$$

For any given application the load capacitance is a known value and as discussed previously the distributed capacitance C_d is dominated by the load capacitance. Hence using equation 3.20 for the given requirement of the rise time and load capacitance we can determine the limits on the leakage inductance.

Since the damping ratio for equation 3.26 has been set to 0.707 hence the according to the equation 3.24, the values of L_{lk} and R_g must satisfy the requirement of ς=0.707. Therefore, the value of R_g is determined from the equation 3.24 using the leakage inductance value obtained from equation 3.26.

The above equations and values determined only satisfy the criteria for the rise time and damping ratio constraints, so these values need to be verified to satisfy the droop constraint using equation 3.27. If the droop constraint is not met then the value of the source resistance need to be iterated so as to meet all the three criteria in best possible way such that it does not have bad impact on the application.

$$D = 100\frac{R_g}{L_m}t \tag{3.27}$$

The greater the transformer leakage inductance and distributed capacitance the slower the rate of voltage rise. This rate of rise is affected by R_g and R_l since these values are important in determining the damping factor.

For a given application the load resistance and the load capacitance are constant hence using the set of design equations (3.24-3.27) the source resistance and the leakage inductance values can be estimated. Hence for a given application the transformer can be designed for a required rise time. A detailed flowchart for designing the transformer using the developed equations is presented in the appendix.

Limitations for the design equations:

These set of equations are applicable only, when the load time constant is far greater than the transformer time constant.

i. $(T_L >> T_{t)}$ where $T_L = R_g C_d$ and $T_t = L_{lk}/R_l$

ii. $R_g << R_{l.}$

Chapter 4

DESIGN OF THE PCB/IC TRANSFORMERS

This chapter discusses about the relationship between the performance measures and the geometries for both the printed circuit board and the integrated circuit transformer structures. It introduces the effect of the geometry on the coefficient of coupling (K) and quality factor (Q) of the transformer and discusses in detail the influence of the all geometrical parameters on the circuit inductance. Based on this discussion, the transformer with the required inductance obtained from Chapter3 for the rise time constraints is designed. The suitable geometry for the structure is estimated from the discussion and the simulation results obtained from Sonnet which is high frequency electromagnetic software.

4.1 Introduction:

Although transformers are more complicated than the inductors, many techniques that are applicable to the optimization of the inductor are also applicable to the transformers especially the methods used to improve the quality factor (Q) of the metal windings. There are several ways to improve *Q*. Some improvements can be made through the fabrication process, such as using thick copper or aluminum top layers or strapping multiple levels of metal layers to reduce the ohmic losses; or using a thick oxide or dielectric layer.

Transformers make use of the magnetic coupling between the primary and secondary windings. The magnetic coupling of the transformer greatly depends on the geometry and layout of the structure. Hence, in order to have sufficient Q and K the structure should be designed with some optimal geometrical parameters which are discussed in detail in the section 4.2.

4.2 Optimal Design of the Transformers:

The inductance and thus the quality factor of the coreless PCB transformer depend on the geometry of the transformer as discussed previously. Therefore, the geometry of the transformer needs to be optimized to give better quality factor and coefficient of coupling. The various geometric parameters that influence the performance of the transformer as listed below and shown is figure 4.1:

1) Winding separation or spacing
2) Number of turns
3) Lamination/Oxide thickness or interlayer spacing
4) Conductor width
5) External radius or Outer Dimension
6) Conductor thickness

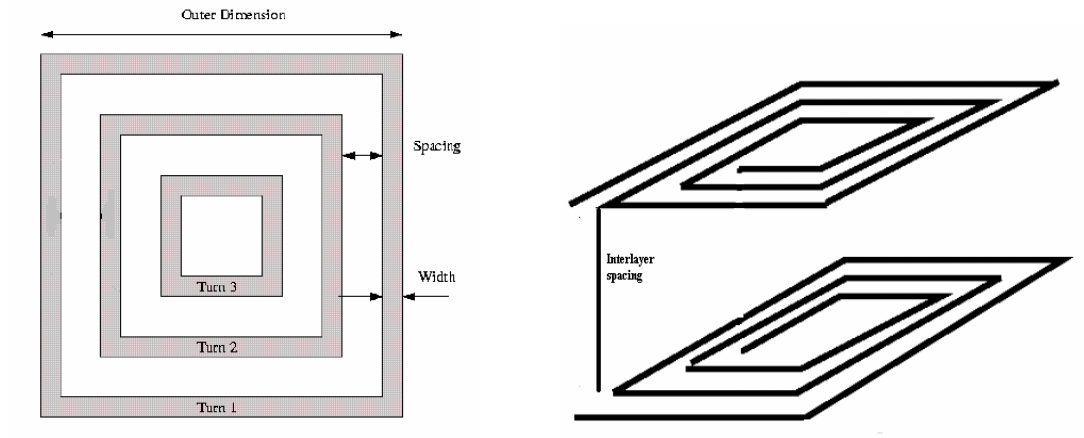


Figure 4.1: Various geometrical parameter of the transformer.

4.2.1 Spacing between tracks:

Increasing the spacing between the tracks by a small percent:
-The mutual inductance between the tracks decreases so does the total inductance. This causes the quality to diminish because the resistance is maintained and the inductance is reduced.
In case the spacing is reduced:
-The mutual inductance grows and the total inductance which also improves the quality as the resistance is maintained and inductance is increased faster than linear.

From the above argument it is clear that for optimal Q the spacing between the windings should be the smallest allowable by the technology. But this assumption is valid conditioned by the working frequency because if the spacing is reduced the coupling capacitance between the tracks increases. So depending on the working frequency this capacitance could affect the performance of the transformer. As the spacing between tracks is reduced the quality curve shifts to lower frequencies.

4.2.2 Different number of Turns:

Increasing the number of turns assuming the remaining geometric parameters to be fixed:
-The inductance and the resistance will grow but it is important to evaluate which grows faster as it could introduce an important effect proximity effect. It influences all the turns but its effect is stronger in the inner turns according to the previous study made.
Also as the number of turns increases so does the shared metal area and the magnetic field value. The parasitic capacitance increases shifting the quality curve (resonant frequency) to a lower frequency.

The transformer radius is kept constant so that the track separation decreases as the number of turns increases**.** Increasing the number of turns without increasing the area or decreasing the laminate thickness does not improve the transformer coupling factor significantly.

When the winding separation is fixed, the transformer radius increases as number of turns increases. As the number of turns increases (the transformer area also increases), the rates of increase of self-inductance and mutual inductance are much greater than that of leakage inductance. Thus, the coupling factor can be increased by increasing the transformer area with or without an increase in the number of turns. However, increasing the number of turns has another advantage, the self-inductance increases substantially.

4.2.3 Laminate/Oxide Thickness:

The separation between the primary and secondary windings plays an important role in coreless planar transformer design. The smaller the separation between the primary and the secondary windings is, the greater the magnetic flux coupling becomes. As separation increases, the magnetic coupling between the primary and secondary windings decreases.

As discussed in section 4.1.1 this is also conditioned by the working frequency as a reduction in separation will cause an increase in the capacitance which again moves the quality curve to lower frequencies. But the laminate or oxide thickness does not have a significant effect on the self inductance.

4.2.4 Conductor Width:

Once the geometrical parameters are fixed to meet a desired inductance value the width can be increased to reduce the resistance but as the width grows so does the metal shared by the spiral. This increases the capacitive coupling and causes the resonant frequency to drop so again the quality curve shifts to lower frequency. Hence, the width increase is limited by several issues like the skin effect, reduction of the inductance and added electric parasitic coupling.

From the previous research work [1] it is recommended that the transformer track width should be set between 10um and 20um for the integrated circuit transformer. The tracks

with width less than 10 um are strongly affected by the corner effect whereas widths greater than 20um exhibit low inductance per unit length. This always must be tempered by the number of turns required as resistance increases with length and decreases with width.

Corner effect:

This effect takes in account the variation of the current density in the corners due to the corner geometry, altering the overall current density and therefore increasing the track resistance as frequency increases.

4.2.5 Different Outer Dimension:

As in the case of number of turns and width, this is another parameter that cannot be analyzed correctly without an empirical analysis. This is due to large number of effects that are linked to the external radius e.g magnetically and electrically induced losses.

Based on the previous research the external radius has to be selected in accordance with the condition of not having a small internal radius (i.e 4 to 5 times w) which may add up to proximity effect as discussed in chapter 2.

4.2.6 Conductor Thickness:

The metal resistivity, width and the track length determine the winding resistance value. Since the metal resistivity is fixed by the technology and the width and the length are fixed by the desired inductance, the only way to reduce the DC resistance is by changing the metal thickness.

The thickness of the single metal layer is also fixed by the technology. In case of the PCB (IC) transformer conductor thickness can be 35um to 70 um (0.5um to 3 um). In case of IC or PCBs there is more scope of variation in thickness when multiple metal layers are available. Another option is to connect different metal layers in parallel which increases the winding thickness and reduces the DC resistance. So the reduced effective resistance helps in improving the quality factor.

Varying the transformer metal thickness does not have a significant influence on the self, leakage and mutual inductance of the transformer but affects the quality factor.

In this section it has been analyzed analytically the impact of transformer geometrical parameters on its performance. In some cases like the winding spacing and the interlayer spacing the influence can be understood from the analytical study but for the parameters like width, number of turns and the external radius it is not as easy. The influence of these parameters on the transformer performance is very complex due to the various parasitic effects like the electrical and magnetic losses. Hence it needs an empirical analysis to evaluate the impact of these parameters.

4.3 Transformer layout Specifications:

Based on the inductance value obtained from the design equations, the dimension coordinates for the structure are estimated in accordance with the geometrical parameters described for the optimal design of transformers in previous section.
For the current application, the transformer is designed for the rise time of 10ns with the load constraints of 100pf and 1KΩ with the damping and drooping constraints of 0.707 and 10%.

For these requirements, the leakage inductance was determined to be 103nh using the equation 3.26 in chapter 3.
The inductance value required for the1:1 transformer was found to be 287nh using the equation 2.3 in chapter 2:

$$L_{lk} = (1 - K^2)L_p$$

Since the stacked transformer uses multiple metal layers and exploits both vertical and lateral magnetic coupling to provide the best area efficiency, the highest self-inductance and highest coupling *(k* ≈ 0.8)[3]. Hence the stacked structure is implemented and the coupling coefficient is taken to be k=0.8 which can be verified from the simulation results.

Based on the area and cost efficiency requirement and the operating frequency range being from 100 KHz to 100 MHz the PCB transformer was used and simulated for this application.

Since the External diameter for the transformer to meet the area requirement is fixed to 400 Mil X 400 Mil i.e. 10mm X 10mm the remaining geometrical parameters are designed accordingly. The spacing and the dielectric thickness are taken to be the minimum allowable values for the PCB fabrication which are 6 Mil and 6 Mil respectively.

In this application the turns ratio is taken to be 1:1 and so the design factors reduce to the number of turns and the width of the winding. These parameters need to be selected to meet the inductance requirement which is 287nh in this case.

For the purpose of estimating these values set of structures with varying turns and width were designed and simulated in sonnet.

4.4 Sonnet Simulation:

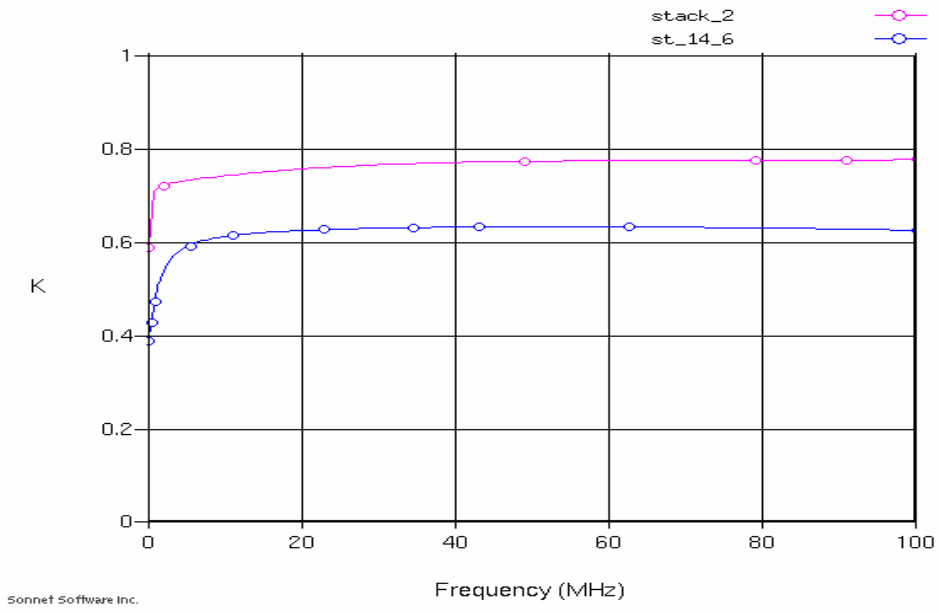
SONNET is a suite of products which provides high-frequency planar electromagnetic analysis for different products. It uses a modified method of moments analysis based on Maxwell's equations to perform a true three dimensional current analysis of predominantly planar structures. Em, the electromagnetic engine, computes S, Y, or Z-parameters, transmission line parameters (Z0 and Eeff), and SPICE equivalent lumped element networks.

The suite includes a number of tools like emvu and patvu which are visualization tools to help the user better interpret the results.

SONET software is also used for design and analysis of high-frequency circuits, distributed filters, transitions, RF packages, waveguides and antennas. Some of the features include modeling of micro strip lines, modeling of via analysis along with some packaging effects and spiral inductors.

As discussed previously the number of turns and the width need to be determined such that the quality factor and the coefficient of coupling are adequate for proper performance of the transformer.

In the following results all other dimension; area, inner diameter and vertical and horizontal spacing, are kept constant and the turns is changed from 10 to 14.



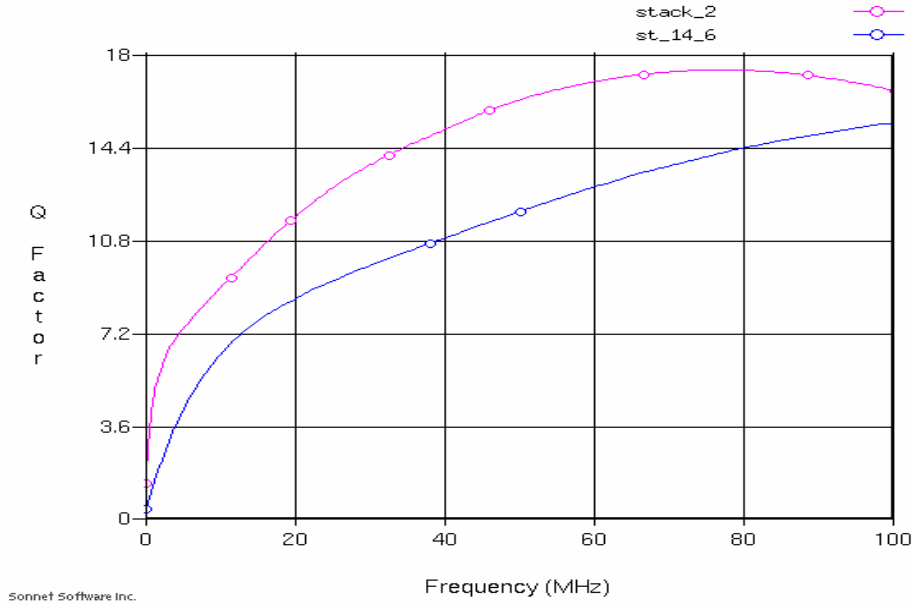
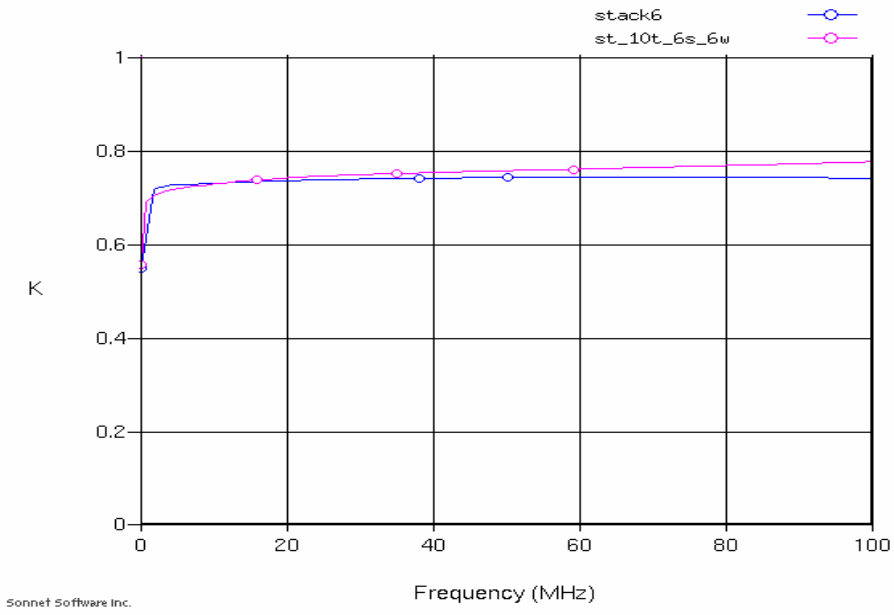


Figure 4.2: K and Q with varying number of turns n = 10 (pink) and n =14 (blue).

From the discussion in section 4.2, we know that once the required inductance value is obtained the variation of width does not have much influence inductance. Now in order to obtain optimal width the different structures with 10 turns and constant parameters with width varying from 6mil to 10mil were simulated and following are the results obtained.



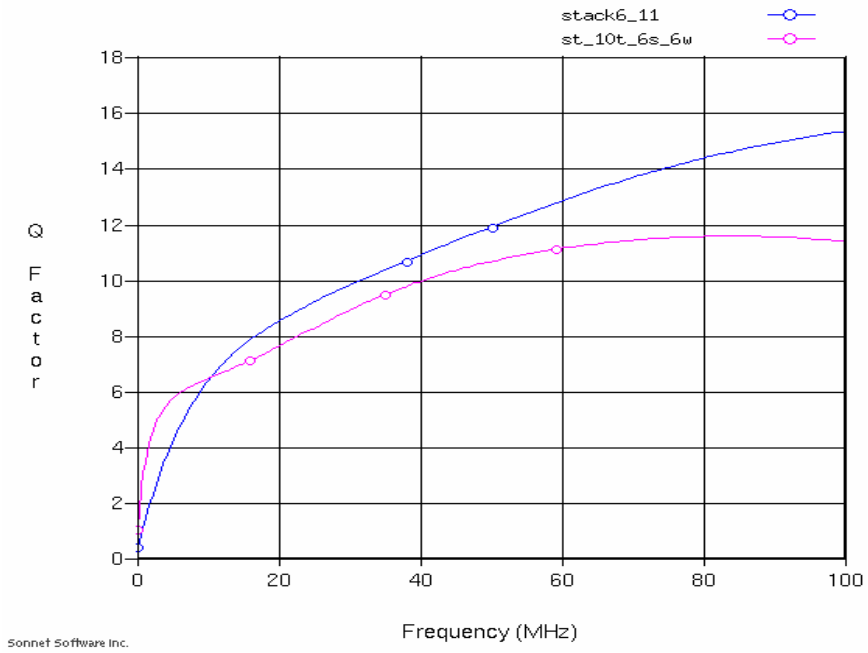


Figure 4.3: K and Q with varying width n= 10, w=6 mil (pink) and n= 10, w=10 mil (blue) .

From the above simulation we see that once the required inductance is obtained the increase in turns ratio with same external radius, and vertical and horizontal spacing, Figure 4.2 degrades transformer performance further, However, when the width is increased same external radius and vertical and horizontal spacing Figure 4.3 the coupling factor does not improve but the quality factor of the transformer improves as the winding resistance is reduced.

So based on the design factors discussed above and the observed simulation results the following values were found to be near optimal for the transformer layout for the current application.

Table 4.1 : Transformer Layout Specifications.

Shape	Rectangular Planar Stacked Structure
Dimension of coil area	400 Mil X 400 Mil
Turns	Primary :10 Secondary :10
Track Width	10 Mil
Track Spacing	6 Mil
Track Thickness	35µm
Dielectric thickness	6 Mil

Based on the data from the Table 4.1 the transformer shown in figure4.4 and figure 4.5 are designed and simulated in the Sonnet software.

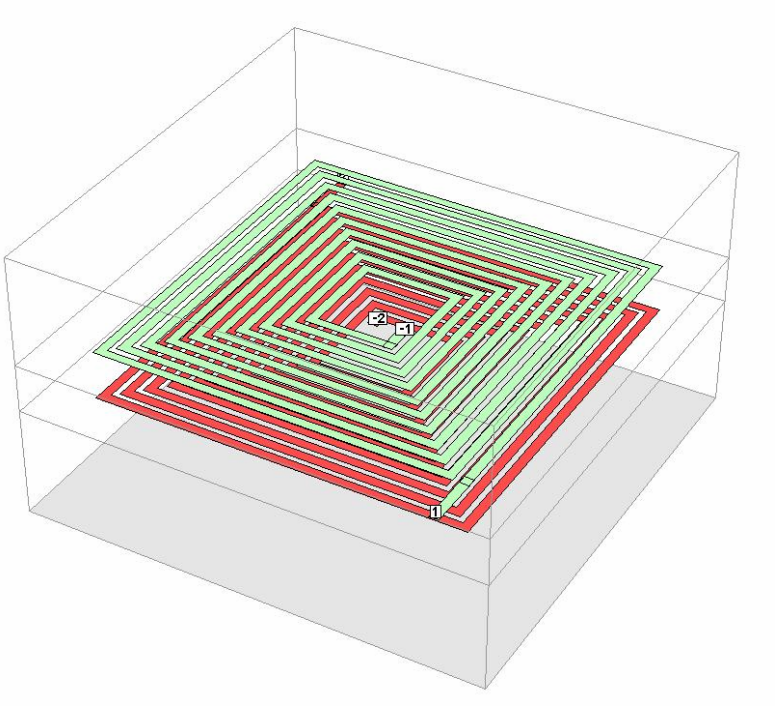


Figure 4.4: 3-DView of the stacked structure.

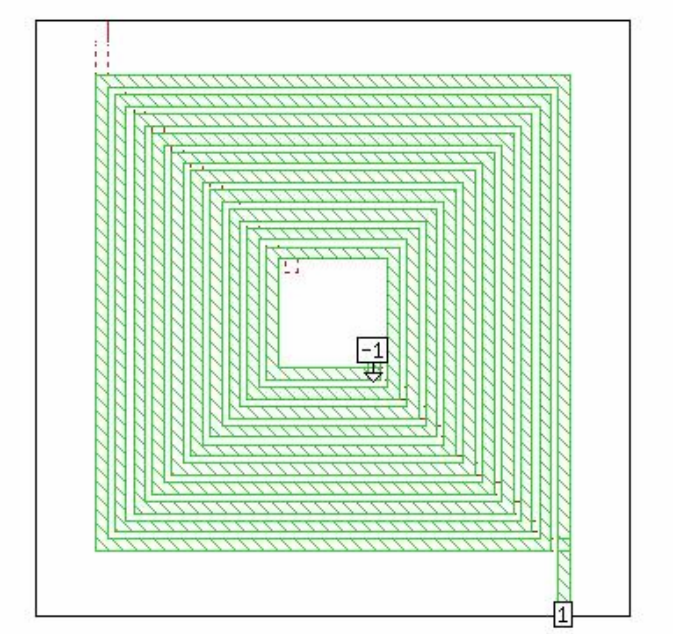


Figure 4.5: Transformer Layout.

The inductance value for these structures can be verified from the equation 2.4 in chapter 2. The simulation results and data validation for these structures are discussed in the Chapter 5.

Chapter 5

Results

Using the basic transformer structures discussed in chapter 2 and the design equations derived in chapter 3 various transformer structures are designed in chapter 4 to verify the performance measures and the geometrical parameters. Based on the review of the first 4 chapters a stacked planar transformer with geometry listed in Table 4.1 was designed and found suitable for the high side switch applications.

The Transformer Structure designed in chapter 4 was simulated in sonnet and fabricated on the PCB. The s-parameters for the simulated and the fabricated transformer were measured using the two port model. The s-parameter files extracted from the simulation and the measurement from the fabricated structure were imported into cadence and used to determine the transformer parameters: primary and secondary inductance, leakage inductance, coupling coefficient and the quality factor of the transformer. This chapter discusses the results obtained and validates the design values with the measured values. The rise time of the transformer with the desired load is obtained and verified against the given design specifications. Finally the high side switch simulation results are presented and discussed.

5.1 Two-Port Network:

This section reviews the relationship of the scattering parameters with the impedance of the network under characterization when the equivalent circuit of the impedance to be measured is known. The scattering parameters of a generic two port network are given by:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} \frac{Z_{11} - Z_{01}}{Z_{11} + Z_{01}} & -2\sqrt{Z_{01}}\sqrt{Z_{02}}\,\frac{I_1}{E_2} \\ -2\sqrt{Z_{01}}\sqrt{Z_{02}}\,\frac{I_1}{E_2} & \frac{Z_{22} - Z_{02}}{Z_{22} + Z_{02}} \end{bmatrix} \tag{5.1}$$

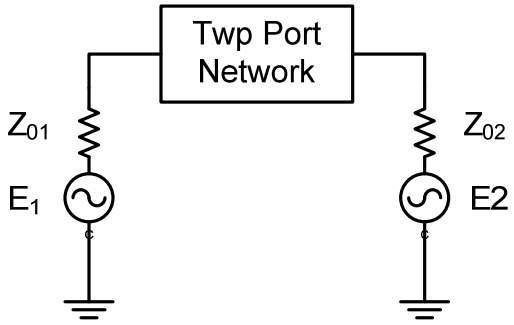


Figure 5.1: Two-Port Network.

S_{11} and S_{21} are derived with the generator E2 shorted to ground and vice versa for the derivation of S_{22} and S_{12}. Z_{11} and Z_{22} are the impedances observed looking into port 1 and port 2 respectively. Also Z_{01} and Z_{02} represent the reference impedance of each port [1].

The scattering parameters of the designed transformer i.e the S_{11} and the S_{21} are obtained from the sonnet simulations and an experimental setup similar to Figure 5.1 using the HP 8735 network analyzer. The simulated and measured results are plotted in Figure 5.2. Only S_{11} and S_{21} are plotted since for a 1:1 transformer $S_{11} \approx S_{22}$ and $S_{12} \approx S_{21}$.

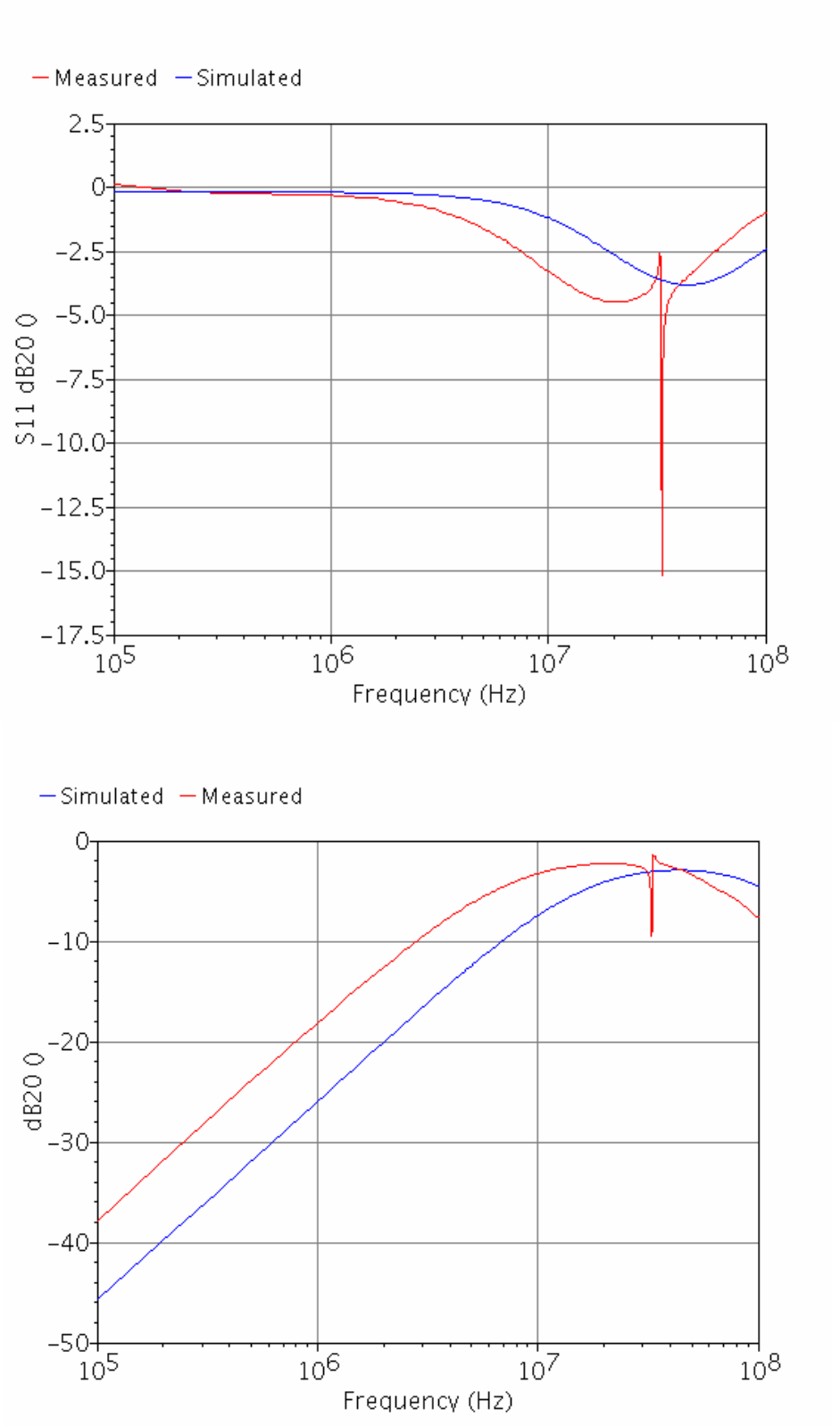


Figure 5.2: Scattering Parameters (i) S11 and (ii) S21.

5.2 Coefficient of Coupling:

From [3] the coefficient coupling for the planar stacked structure was assumed to be *(k* ≈ 0.8). The coefficient of coupling for the designed structure is plotted in figure 5.3 from the simulated and measured s-parameter data using the equation:

$$K(L_p, L_s) = \frac{\mathrm{Im}(Z_{12})}{\mathrm{Im}(Z_{11})} \tag{5.2}$$

The result obtained using the equation 5.2 plotted in figure 5.3 shows the K≈ 0.74 and 0.76 for the sonnet and measured data respectively which is a close to the estimated value K=0.8.

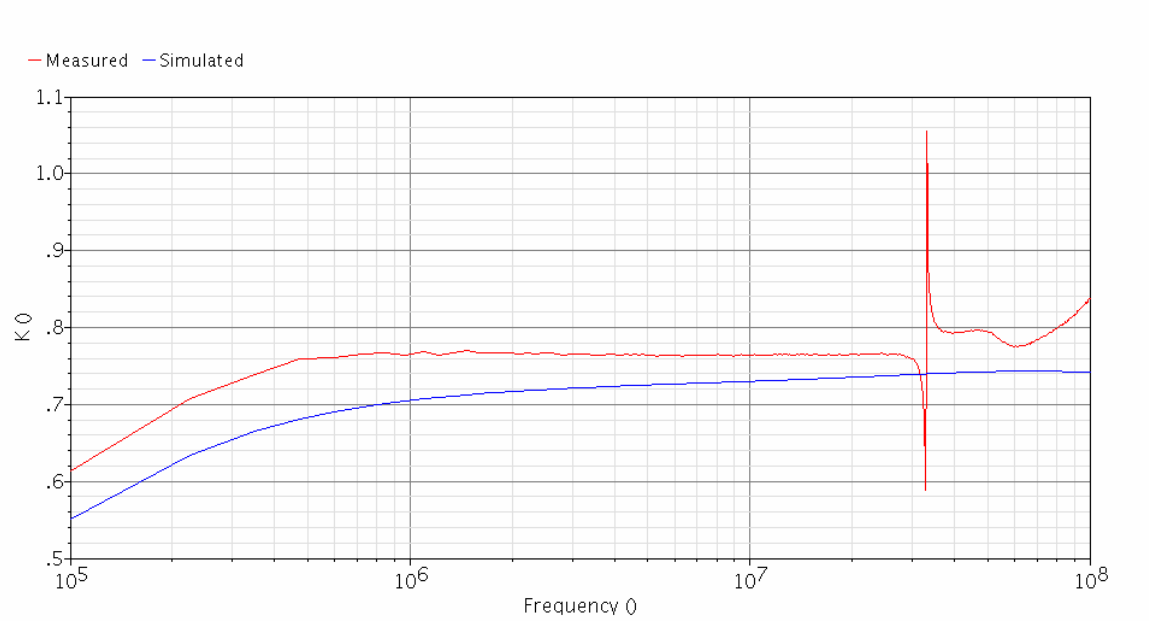


Figure 5.3: Coefficient of Coupling.

5.3 Leakage Inductance:

The leakage inductance of the transformer was obtained from the design equation 3.26 in Chapter 3 for the rise time constraint of 10ns for the load capacitance of 100pf and was estimated to be 103nh.

For the extracted s-parameter model the leakage inductance can be measured by shorting the secondary of the transformer and using equation 5.3.

$$L_{lk} = \frac{\mathrm{Im}(Z_{11})}{2\Pi f} \tag{5.3}$$

Where $Z_{11} \approx Z_{22}$ in this example as it is a 1:1 transformer.

Figure 5.4 is the plot for the simulated and measured model which is close to the required value of the leakage inductance.

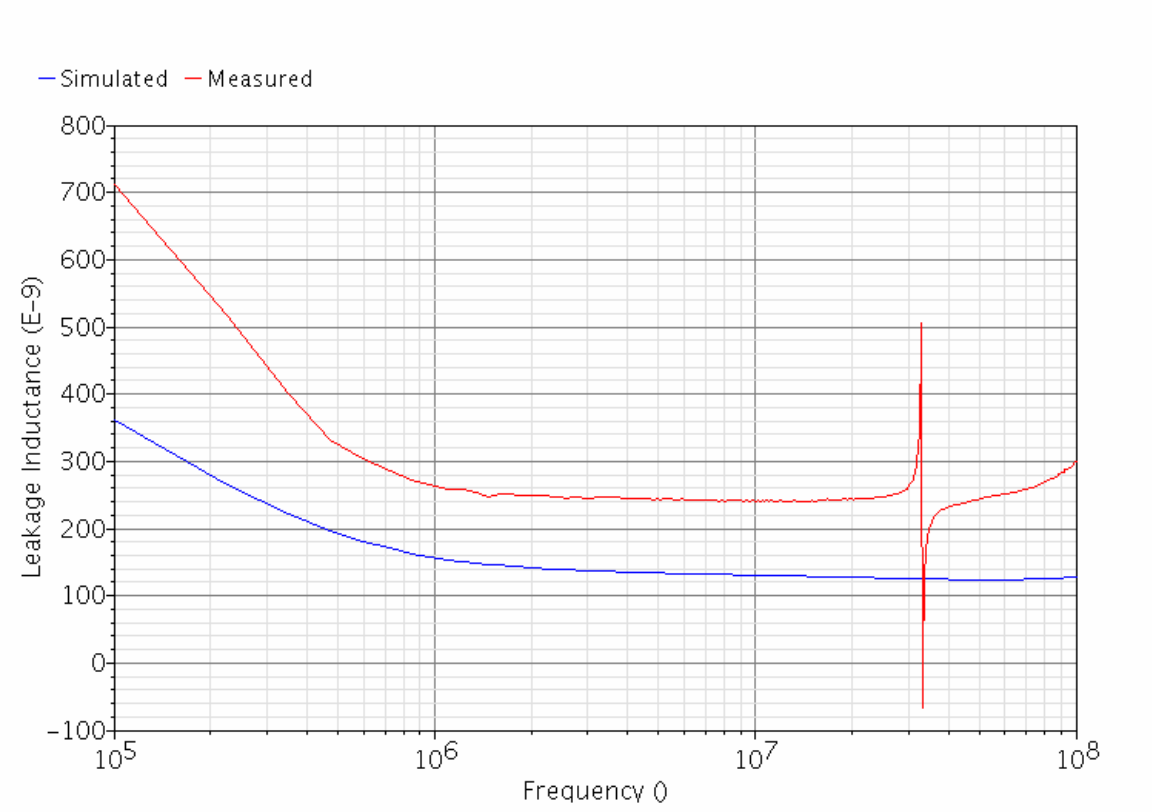


Figure5.4: Leakage Inductance of the winding obtained for the designed structure.

5.4 Inductance:

Since the transformer is 1:1 so the inductance of the primary and secondary winding are approximately equal. The inductance of the winding for the two port transformer can be measured using the following relationship:

$$L_s = L_p = \frac{im(Z_{11})}{2\Pi f} = \frac{im(Z_{22})}{2\Pi f} \tag{5.4}$$

The inductance value with $k \approx 0.8$ coupling for leakage of 103nh was estimated to be 287nh. So for the simulated data of K≈ 0.74 and leakage of 124nh the inductance should be about 278nh. Figure 5.5 is the plot obtained from the simulation and measurement data for the inductance.

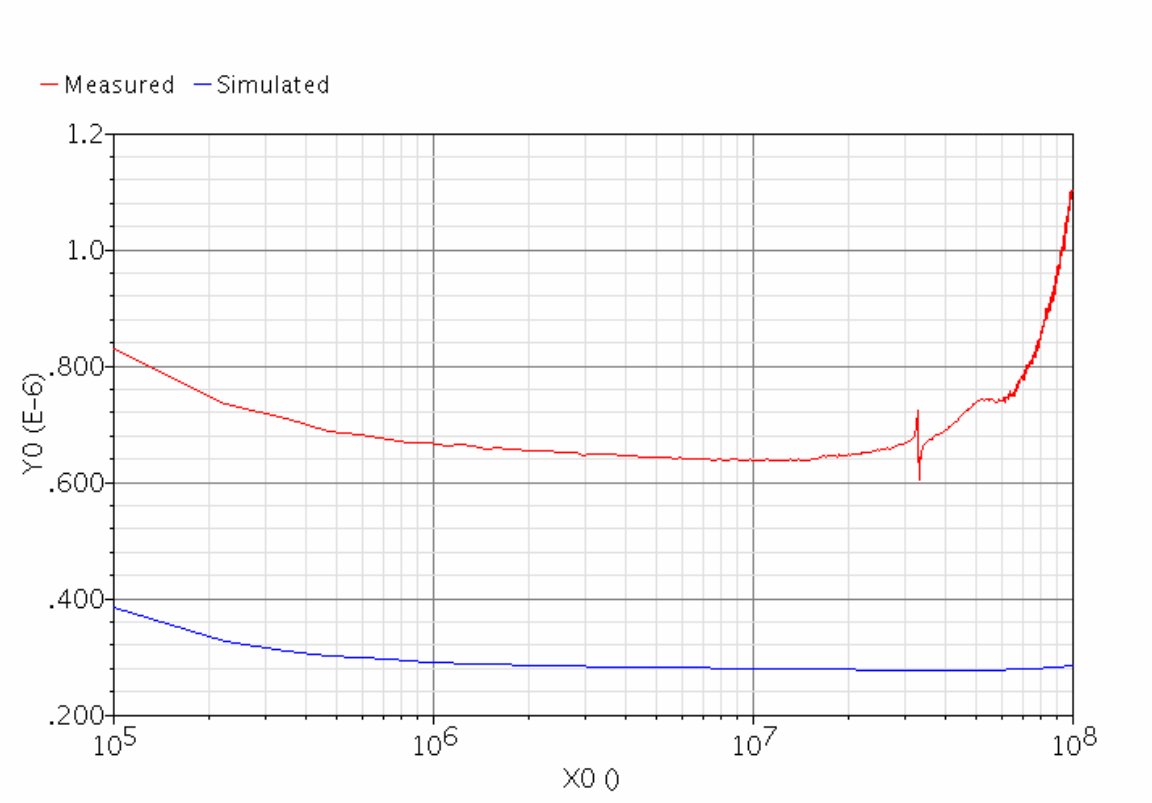


Figure 5.5: Inductance of the windings obtained for the designed structure.

5.4 Quality Factor:

The quality factor of the primary and secondary transformer winding is plotted in Figure 5.6 using the relationship in equation 5.5:

$$Q = \frac{im(Z_{11})}{real(Z_{11})} \tag{5.5}$$

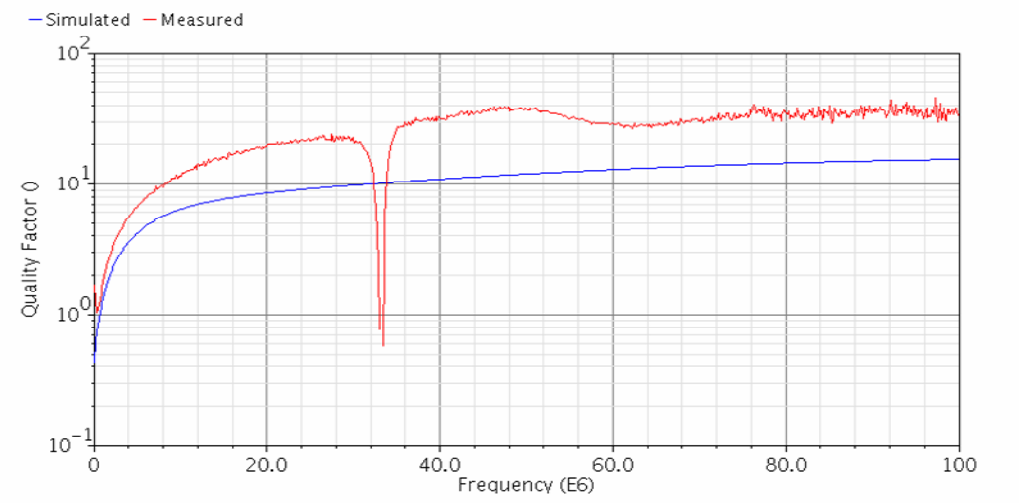


Figure 5.6: Quality factor of the transformer winding.

Based on the quality factor obtained we can conclude that the winding resistance is very small and the assumption made in Chapter 3 regarding the winding resistance R_1 and R_2 is valid.

5.6 Voltage Gain

The voltage gain for the simulated and measured transformer is close to 0.74 and 0.76 respectively which implies that the transformer can support the required secondary voltage to drive the power switch.

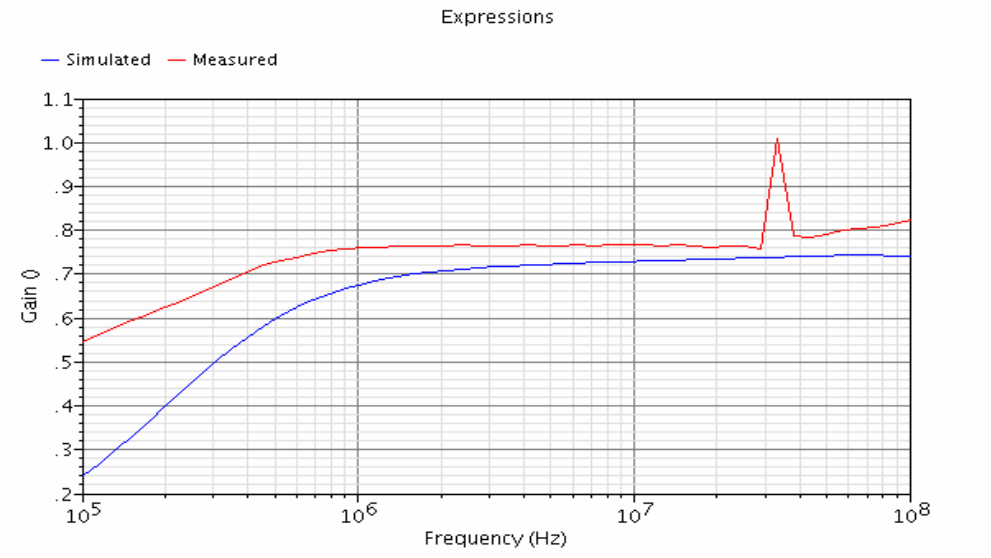


Figure5.7: Voltage gain.

All the above transformer parameters estimated to achieve the desired rise time and droop requirement of the transformer are in close agreement with the simulated and measured values for the structure with the exception of the winding inductance.

5.7 Rise Time:

The rise time is nominally defined as the time when the output pulse slews between 10% and 90% of its final value. The transformer was designed for the rise time and droop requirement of 10ns and 15% respectively. This rise time requirement is for the load of 100pf and 1KΩ.The following is the simulated result for the rise time measured in Cadence using the measured s-parameter model of the transformer for this load. The loaded transformer was designed to have a damping ration of 0.707

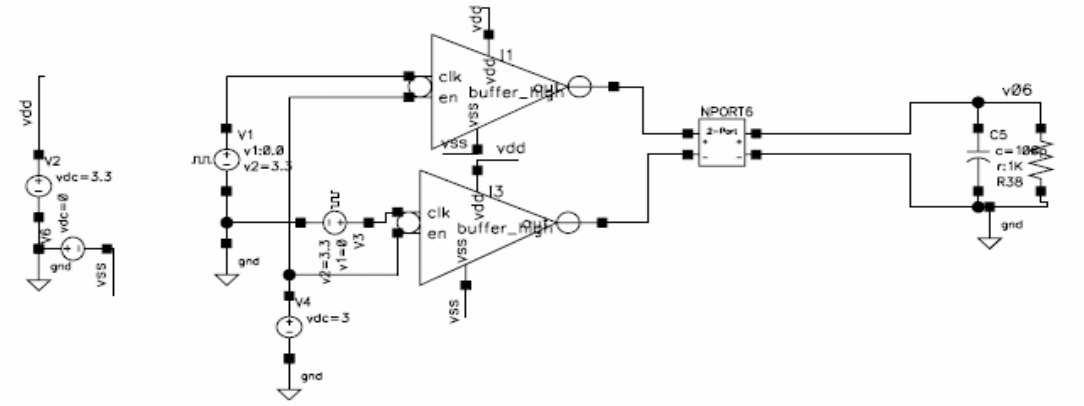


Figure5. 8: Schematic to determine the rise time with load.

From the plot in Figure 5.9 the rise time is obtained to be 7.4ns and 8.2 ns for the simulated and measured data, respectively. Also though the droop requirement is also met but the overshoot and oscillations occur due to insufficient damping in the system.

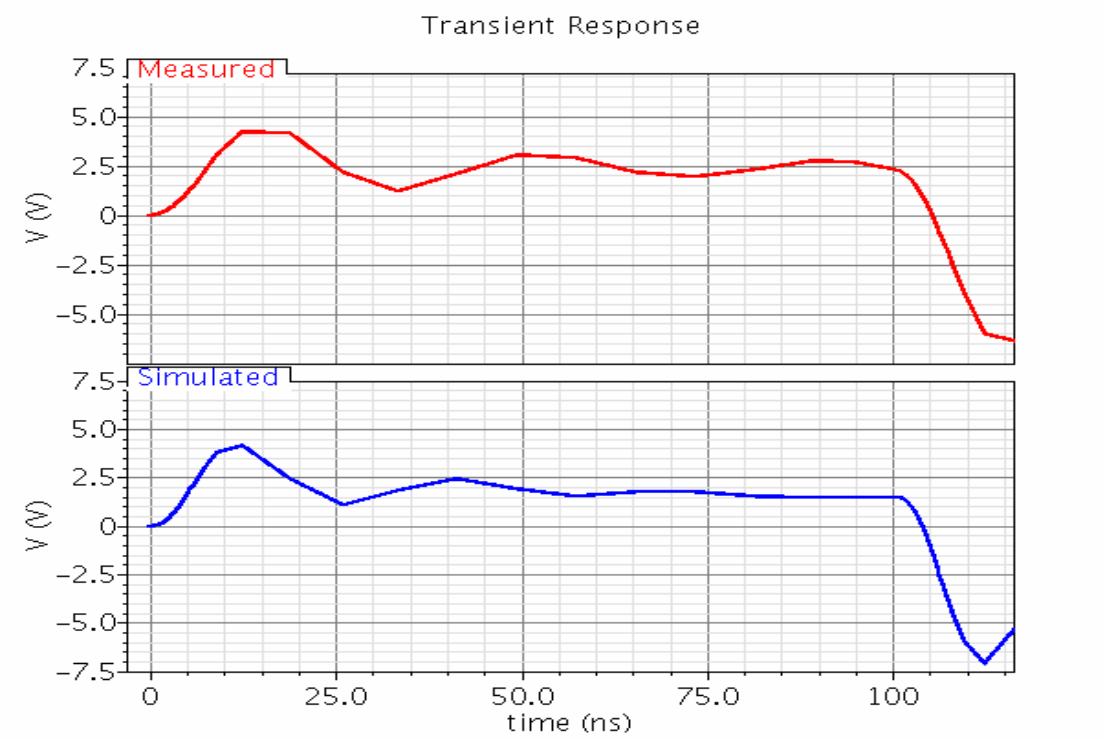


Figure5. 9: Rise Time for the transformer with load.

5.8 High Side Switching Circuit Implementation:

The Transformer designed in section 4.4 is used in the implementation of the high side switching circuit for the switch mode power supply for switching the SiC JFET. Figure 5.10 is the schematic of the high side switching circuit. The CMOS buffers have been designed for the required source resistance of 1.4 Ω to satisfy the required droop constraint. The measured s-parameter model for the fabricated transformer structure was imported into the cadence to provide the required signal transfer and isolation in the circuit. The CMOS bridge rectifier is implemented using the PMOS and NMOS transistors for full wave rectification at the secondary. The secondary circuit consists of the series resistance and capacitance, MOS-diode and a discharge transistor which facilitates the discharge of the SiC JFET during the off cycle. The SiC JFET was modeled to be the parallel combination of the load capacitance and load resistance of value 200pf and 2KΩ respectively. The detailed discussion for this is presented in [23].

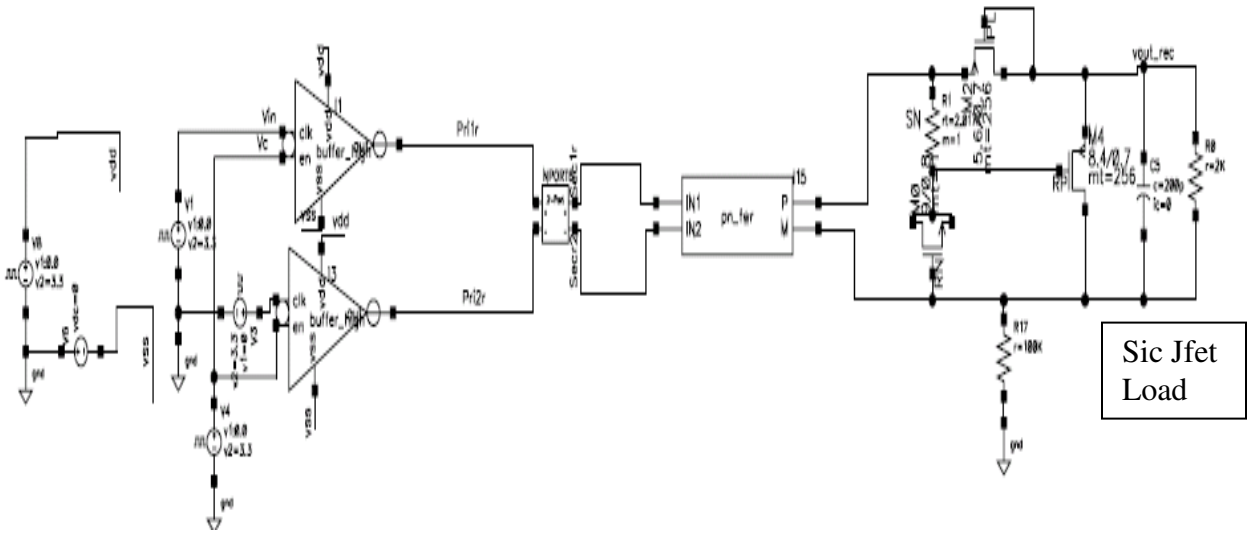


Figure 5.10: High Side Switching Circuit for the SMPS.

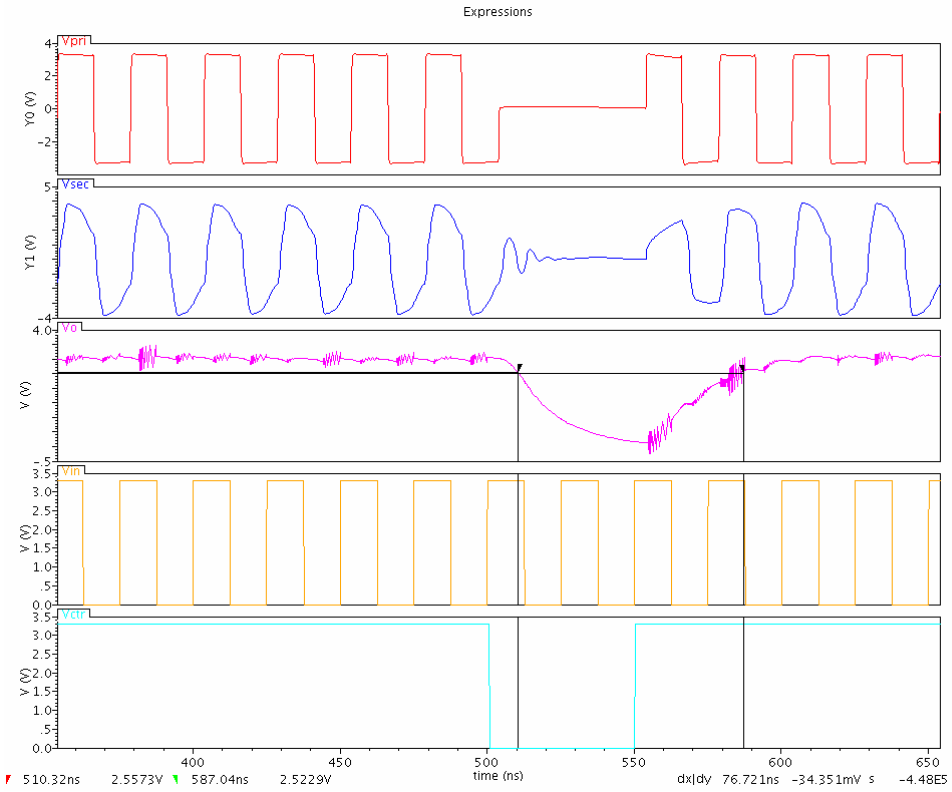


Figure 5.11: Waveforms at various stages in the high side switching Circuit. (i) o/p at buffer (Y0)(ii) o/p at secondary of the transformer(Y1) (iii) o/p at the diode with the required rise and fall time(V1) (iv) input to the circuit (V2)(v) the control signal at the buffer(V3).

Based on the circuit requirements the input to the SiC JFET should have the equal rise and fall time less than 50ns with minimum V_{gs} of 2.5 V to turn on the transistor. It may be observed from the simulation plots with the extracted data from PCB transformer the

rise and fall times were determined to be 35ns for a V_{gs}=3.1V at room temperature usinfg typical models. Hence the coreless planar transformer demonstrates the potential for successfully implementation in high side switching circuits.

5.9 Summary:

From the simulation and measured data obtained the design equations presented in this work are validated as the results are in close agreement with the estimated data based on the design equations except for the self inductance.

Table 5.1:Data Validation for estimated and obtained results.

Parameters	Design Values	Sonnet Extraction	Extracted Measurement
Coupling Coefficient	0.8	0.74	0.76
Leakage Inductance(nH)	103	126	240
Self Inductance (nH)	287	278	620
Rise Time(ns) (from cadence simulation)	10	7.46	8.2

The variation in the self inductance value that is observed in the measured data, greater than predicted by geometric equation, is due to the inaccuracy in the expressions used to calculate the inductance from the geometrical parameters. Most of the expressions underestimate the actual inductance. This is also observed from the measured result. The self inductance value from the expression by Grover [16] was used to determine the design value; 287.83nH whereas the expression in [17] gives the self inductance for the same geometry to be 147nH and the expression by Ronkanien predicts the inductance to be 324nH.

The results from the high switching circuit implementation demonstrate the feasibility of the coreless transformers use as CMOS high side switch where the potential exist to place the transformer on substrate or on the PCB.

Chapter 6

Summary and Concluding Remarks

6.1 Summary:

In this work a design procedure for designing coreless planar PCB/IC pulse transformers for a specified rise time and droop requirements with adequate damping is developed and presented. This design flow is based on the low and high frequency equivalent circuit models for the transformer. These models are used to develop the pulse waveform structure and hence determine the effect of various circuit parameters on the performance of the transformer.

Leakage inductance and parasitic capacitance are the major factors affecting the performance of the transformer. The effects of parasitic transformer capacitance should be accounted for when selecting and designing the transformers. For a well designed transformer the load capacitance typically dominates the transformers parasitic capacitance. Based on the equations developed appropriate values for the leakage inductance for a given of rise time are determined .With these values as guidelines the PCB /IC transformer has been designed. It has been simulated in the high frequency electromagnetic software and fabricated on a two sided PCB. The performance measures of the transformer, namely coefficient of coupling and quality factor have been verified by importing the measured s-parameter data of the transformer into cadence. In addition the utility of the coreless transformer has been validated by simulation of a high side

switch for use in a switched mode power supply with a 200pF load were the rise and fall times are less than 50nS across temperature and process.

6.2 Advantages of Coreless Planar Transformers:

Fabrication of the transformer on the printed circuit board or the IC eliminates the manufacturing cost of manual windings. The coreless transformers do not need space to accommodate the magnetic core and have no core limitations such as core losses and saturation. But the absence of the core in the CLT transformers limits the lower cutoff frequency which reduces the bandwidth of the transformer. Hence these transformers are more suitable for applications greater than 100 Khz and for lower frequency ranges core based transformers should be used. Their sizes can be smaller than those of core-based transformers.

This inherent low-profile property makes the coreless transformers suitable for applications in which stringent space and height requirements have to be met. Moreover, the dielectric breakdown voltage of PCB typically ranges from 15 kV to 40 kV while IC interlayer dielectrics may range from 10s to 100s of volts providing an acceptable degree of isolation for use in a number of applications, i.e. high side switches.

6.3 Future work:

The gate drive transformers are essential part of the electronic circuits. Including the parasitic capacitance effect in the modeling and analysis can help in better understanding of the transformer operation and improve the performance of the transformer. Also having more accurate expressions for determining the geometrical parameters for required inductance both in the case of PCB and IC would help in designing a better transformer.

This work needs to be implemented on the IC version. Also multiple versions need to be implemented in different electromagnetic soft wares to strive for better match between in the simulated data and the physically measured data. A more detailed study needs to be done for the implementation of the step-up transformer.

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APPENDIX

A. The following is the Pi-Model file for the stacked structure implemented in Sonnet:

```
  Sonnet Data File
  From: emgraph Version : 11.52
  From Emgraph Data: stack
  Data File Written: 05/29/2008 16:27:37
 < HDATE 04/24/2008 12:40:56
 < MDATE 05/28/2008 22:14:56
  Spice Data
 Limits: C>0.01pF L<10000.0nH R<1000.0Ohms K>0.01

simulator lang=spectre
; Analysis frequencies: 0.1, 2.0 MHz
inline subckt stack_0 1 2 GND
R_R1 1 GND resistor r = 243.352733486
R_R2 1 2 resistor r = 9.3880793987094
R_R3 2 GND resistor r = 144.1238778743
L_L1 1 3 inductor l = 360.64961241112n
R_RL1 3 GND resistor r = 0.0585112573757
L_L2 1 4 inductor l = 216.45178488729n
R_RL2 4 2 resistor r = 0.0373262781879
L_L3 2 5 inductor l = 356.78932329498n
R_RL3 5 GND resistor r = 0.0597303953222
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3942620562841
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.6983094702359
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 0.9013844901528

ends stack_0


simulator lang=spectre
;  Analysis frequencies: 2.0, 15.0 MHz
inline subckt stack_1 1 2 GND
R_R1 1 2 resistor r = 131.41045661299
L_L1 1 3 inductor l = 334.6110727441n
R_RL1 3 GND resistor r = 0.2907596525019
L_L2 1 4 inductor l = 161.03016323766n
R_RL2 4 2 resistor r = 0.4364987182225
L_L3 2 5 inductor l = 330.39654069403n
R_RL3 5 GND resistor r = 0.2983525415132
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3559375118355
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7578673708314
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_1
```

```
simulator lang=spectre
;  Analysis frequencies: 15.0, 16.0 MHz
inline subckt stack_2 1 2 GND
R_R1 1 2 resistor r = 319.97172399335
L_L1 1 3 inductor l = 333.87369001738n
R_RL1 3 GND resistor r = 0.846262210617
L_L2 1 4 inductor l = 158.95508900671n
R_RL2 4 2 resistor r = 1.4656375578864
L_L3 2 5 inductor l = 329.63045380685n
R_RL3 5 GND resistor r = 0.855850754189
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3542072001993
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7604464530845
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_2


simulator lang=spectre
;  Analysis frequencies: 16.0, 18.0 MHz
inline subckt stack_3 1 2 GND
R_R1 1 2 resistor r = 364.14821870053
L_L1 1 3 inductor l = 333.31755232009n
R_RL1 3 GND resistor r = 0.8922055381974
L_L2 1 4 inductor l = 157.63178992835n
R_RL2 4 2 resistor r = 1.5379639306324
L_L3 2 5 inductor l = 329.0443050652n
R_RL3 5 GND resistor r = 0.902273797927
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3531663927934
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7620314578114
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_3


simulator lang=spectre
;  Analysis frequencies: 18.0, 20.0 MHz
inline subckt stack_4 1 2 GND
R_R1 1 2 resistor r = 425.80378240482
L_L1 1 3 inductor l = 332.89846610122n
R_RL1 3 GND resistor r = 0.9559554847199
L_L2 1 4 inductor l = 156.4933502434n
R_RL2 4 2 resistor r = 1.6433115979466
L_L3 2 5 inductor l = 328.59338083077n
R_RL3 5 GND resistor r = 0.966921268738
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3522475508841
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7634397826948
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_4


simulator lang=spectre
;  Analysis frequencies: 20.0, 22.0 MHz
inline subckt stack_5 1 2 GND
C_C1 1 GND capacitor c = 0.070727229647p
```

```
R_R1 1 2 resistor r = 490.25588682103
L_L1 1 3 inductor l = 332.45841979186n
R_RL1 3 GND resistor r = 1.0164475303244
L_L2 1 4 inductor l = 155.5426617351n
R_RL2 4 2 resistor r = 1.7440989900448
L_L3 2 5 inductor l = 328.18342255506n
R_RL3 5 GND resistor r = 1.0291281926545
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3513996605836
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7645742726363
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_5


simulator lang=spectre
;  Analysis frequencies: 22.0, 24.0 MHz
inline subckt stack_6 1 2 GND
C_C1 1 GND capacitor c = 0.1641375088765p
R_R1 1 2 resistor r = 557.44393111328
L_L1 1 3 inductor l = 332.01353136716n
R_RL1 3 GND resistor r = 1.0742017862482
L_L2 1 4 inductor l = 154.74265168869n
R_RL2 4 2 resistor r = 1.8412765211094
L_L3 2 5 inductor l = 327.81486050154n
R_RL3 5 GND resistor r = 1.0892910912445
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3506096921911
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7654959569835
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_6


simulator lang=spectre
;  Analysis frequencies: 24.0, 26.0 MHz
inline subckt stack_7 1 2 GND
C_C1 1 GND capacitor c = 0.234064205811p
R_R1 1 2 resistor r = 626.96547102631
L_L1 1 3 inductor l = 331.64801531835n
R_RL1 3 GND resistor r = 1.1299235717381
L_L2 1 4 inductor l = 154.07021665209n
R_RL2 4 2 resistor r = 1.9351300391218
L_L3 2 5 inductor l = 327.52962682753n
R_RL3 5 GND resistor r = 1.1475402318576
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3499025866024
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.766284005735
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_7


simulator lang=spectre
;  Analysis frequencies: 26.0, 29.0 MHz
inline subckt stack_8 1 2 GND
C_C1 1 GND capacitor c = 0.2980243782398p
C_C2 2 GND capacitor c = 0.0333324129316p
R_R1 1 2 resistor r = 717.10239984546
L_L1 1 3 inductor l = 331.20213906633n
```

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R_RL1 3 GND resistor r = 1.195038082281
L_L2 1 4 inductor l = 153.27531977836n
R_RL2 4 2 resistor r = 2.0433074850864
L_L3 2 5 inductor l = 327.14758009813n
R_RL3 5 GND resistor r = 1.2152828538168
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3491391339925
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7671970739793
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_8


simulator lang=spectre
;  Analysis frequencies: 29.0, 32.0 MHz
inline subckt stack_9 1 2 GND
C_C1 1 GND capacitor c = 0.353105720217p
C_C2 2 GND capacitor c = 0.1257658961674p
R_R1 1 2 resistor r = 829.61515330203
L_L1 1 3 inductor l = 330.64477414874n
R_RL1 3 GND resistor r = 1.2726616304074
L_L2 1 4 inductor l = 152.6250363111n
R_RL2 4 2 resistor r = 2.1755823416014
L_L3 2 5 inductor l = 326.55992549518n
R_RL3 5 GND resistor r = 1.294345690245
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3487969466461
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7677811957618
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_9


simulator lang=spectre
;  Analysis frequencies: 32.0, 35.0 MHz
inline subckt stack_10 1 2 GND
C_C1 1 GND capacitor c = 0.3924962124761p
C_C2 2 GND capacitor c = 0.1922300445983p
R_R1 1 2 resistor r = 946.30491951215
L_L1 1 3 inductor l = 330.17770483981n
R_RL1 3 GND resistor r = 1.3472169068022
L_L2 1 4 inductor l = 152.12881123755n
R_RL2 4 2 resistor r = 2.3036308173223
L_L3 2 5 inductor l = 326.06448813092n
R_RL3 5 GND resistor r = 1.3701705255846
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3485686012096
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7681970005238
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_10


simulator lang=spectre
;  Analysis frequencies: 35.0, 38.0 MHz
inline subckt stack_11 1 2 GND
C_C1 1 GND capacitor c = 0.4217584756063p
C_C2 2 GND capacitor c = 0.2414900381749p
L_L1 1 3 inductor l = 329.78286157611n
R_RL1 3 GND resistor r = 1.4191139167146
```

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L_L2 1 4 inductor l = 151.76111824397n
R_RL2 4 2 resistor r = 2.4283778474089
L_L3 2 5 inductor l = 325.6430224486n
R_RL3 5 GND resistor r = 1.4432237068278
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3484371769738
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7684695176686
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_11


simulator lang=spectre
;  Analysis frequencies: 38.0, 40.0 MHz
inline subckt stack_12 1 2 GND
C_C1 1 GND capacitor c = 0.4408279882639p
C_C2 2 GND capacitor c = 0.2730483744854p
L_L1 1 3 inductor l = 329.50326854399n
R_RL1 3 GND resistor r = 1.4782112323045
L_L2 1 4 inductor l = 151.56242098792n
R_RL2 4 2 resistor r = 2.5326342627708
L_L3 2 5 inductor l = 325.34142494374n
R_RL3 5 GND resistor r = 1.5031876218154
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3484180633923
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7685676345712
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_12


simulator lang=spectre
;  Analysis frequencies: 40.0, 49.0 MHz
inline subckt stack_13 1 2 GND
C_C1 1 GND capacitor c = 0.4704710203059p
C_C2 2 GND capacitor c = 0.3223595642291p
L_L1 1 3 inductor l = 329.05456416084n
R_RL1 3 GND resistor r = 1.5900179522248
L_L2 1 4 inductor l = 151.32689423938n
R_RL2 4 2 resistor r = 2.7316873953702
L_L3 2 5 inductor l = 324.85716032079n
R_RL3 5 GND resistor r = 1.6167493983048
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3484786978643
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7685979094946
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_13


simulator lang=spectre
;  Analysis frequencies: 49.0, 79.0 MHz
inline subckt stack_14 1 2 GND
C_C1 1 GND capacitor c = 0.5184261383186p
C_C2 1 2 capacitor c = 0.8873196021071p
C_C3 2 GND capacitor c = 0.3998566962609p
L_L1 1 3 inductor l = 327.66665883302n
R_RL1 3 GND resistor r = 1.8880451837623
L_L2 1 4 inductor l = 149.57998205066n
R_RL2 4 2 resistor r = 3.2486323883045
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L_L3 2 5 inductor l = 323.42078383801n
R_RL3 5 GND resistor r = 1.9216116234254
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3474133340311
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7702776795793
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_14


simulator lang=spectre
;  Analysis frequencies: 79.0, 91.0 MHz
inline subckt stack_15 1 2 GND
C_C1 1 GND capacitor c = 0.5381892203444p
C_C2 1 2 capacitor c = 1.4393354703863p
C_C3 2 GND capacitor c = 0.4300561293304p
L_L1 1 3 inductor l = 325.88359210906n
R_RL1 3 GND resistor r = 2.2094226176306
L_L2 1 4 inductor l = 146.50480149877n
R_RL2 4 2 resistor r = 3.8044429279635
L_L3 2 5 inductor l = 321.62952929902n
R_RL3 5 GND resistor r = 2.2571834967566
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.344981403703
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7737590423753
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_15


simulator lang=spectre
;  Analysis frequencies: 91.0, 100.0 MHz
inline subckt stack_16 1 2 GND
C_C1 1 GND capacitor c = 0.5436350473976p
C_C2 1 2 capacitor c = 1.5868214746546p
C_C3 2 GND capacitor c = 0.4375336150739p
L_L1 1 3 inductor l = 325.2762496124n
R_RL1 3 GND resistor r = 2.3067561662394
L_L2 1 4 inductor l = 145.475129107n
R_RL2 4 2 resistor r = 3.9938981058258
L_L3 2 5 inductor l = 321.02998230282n
R_RL3 5 GND resistor r = 2.3637245485816
m1 mutual_inductor ind1 = L_L1 ind2 = L_L2 coupling = 0.3441385470035
m2 mutual_inductor ind1 = L_L1 ind2 = L_L3 coupling = 0.7749297279967
m3 mutual_inductor ind1 = L_L2 ind2 = L_L3 coupling = 1.0

ends stack_16
```
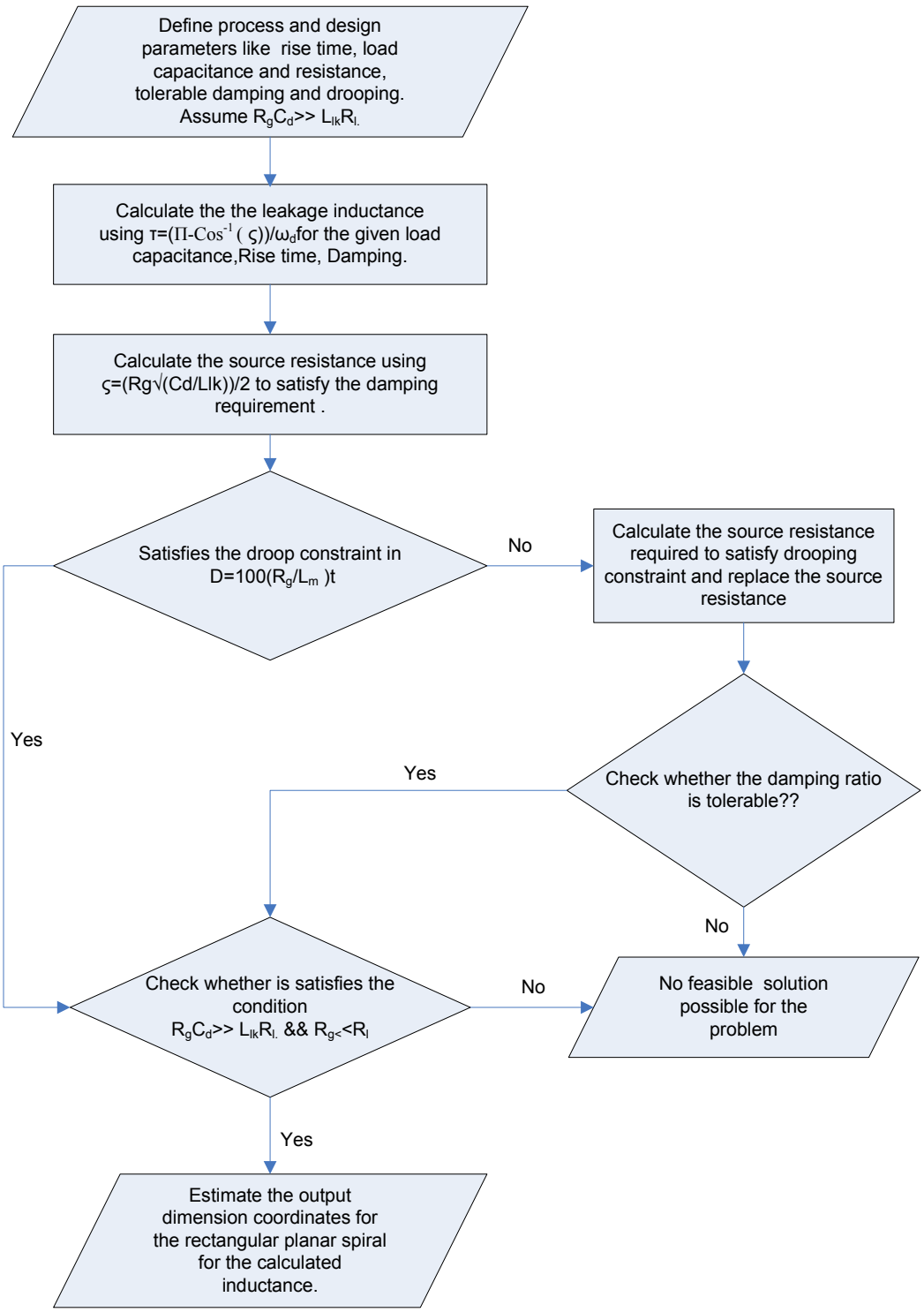

B. The Design Flowchart for the Pulse Transformer :



VITA

PRATIBHA KOTA

Candidate for the Degree of

Master of Science

Thesis: ANALYSIS AND DESIGN METHODOLOGY FOR PCB AND INTEGRATED CIRCUIT PULSE TRANSFORMER

Major Field: Electrical and Computer Engineering

Biographical:

Personal Data: Born in Hyderabad, India

Education:

- Completed the requirements for the Master of Science in Electrical and Computer Engineering at Oklahoma State University, Stillwater, Oklahoma in July, 2008.
- Bachelor of Technology in Electrical and Electronics Engineering from Jawaharlal University of Technology, India in May, 2005.

Experience:

- Research Assistant for Mixed Signal VLSI Lab., Oklahoma State University, Since Jan'07.

Name: PRATIBHA KOTA Date of Degree: July, 2008

Institution: Oklahoma State University Location: Stillwater, Oklahoma

Title of Study: ANALYSIS AND DESIGN METHODOLOGY FOR PCB AND INTEGRATED CIRCUIT PULSE TRANSFORMER

Pages in Study: 64 Candidate for the Degree of Master of Science

Major Field: Electrical and Computer Engineering

Scope and Method of Study:

This work involves the study and implementation of pulse transformers for gate drive circuits in switch mode power supplies. A gate drive transformer is needed in SMPS to control the timing of the circuit. These gate-drive transformers are basically pulse transformers that are used to drive the gate of an electronic switching device. This work essentially concentrates on designing a 1:1 coreless pulse transformer that would drive the gates of power switches.

Findings and Conclusions:

Based on this study, using low and high frequency band models for the transformer a set of design equations have been developed to model a pulse transformer for a given rise time and droop requirements with proper damping. Based on the developed equations an appropriate value for the inductance for the given of rise time is determined .With these values as guidelines the PCB /IC transformer has been designed and simulated in the high frequency electromagnetic software. Based on the simplified models and the simulation data a PCB transformer has been fabricated and measured to validate the design methodology. Additionally, the feasibility of the CMOS Integrated high side switching with the measured PCB transformer S-parameter data has been demonstrated based on the Cadence Spectre simulations.

ADVISER'S APPROVAL: Dr. Chriswell Hutchens