ANALYSIS, DESIGN AND MODELING OF DC-DC CONVERTER USING SIMULINK

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Dedication

To mummy and papa…

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Although it has just been just two and a half years studying in Oklahoma State University, it is an experience that will stay with me forever. My stay in Stillwater has given me a lot to cherish, good friendships, an excellent studying environment to name a few.

First of all I would like to thank my parents, Lalita Kasat and Bhagwandas Kasat. They have inspired me throughout my life and have taught me never to give up. I would also like to thank my sister and brother-in-law, Shradha Gattani and Ashish Gattani, for helping me realize my long standing dream of studying in an esteemed university. I would also like to thank my Cousin, Amit Kasat for his help and support.

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Glossary

Upper case variables refer to steady state DC conditions. Lower case symbol with a caret on top is the small signal perturbation around steady state.

d	Duty cycle
d’	Complement of duty cycle 1-d
f_{sw}	Switching frequency
FM	Modulation gain of duty cycle
$G_c(s)$	Compensation network
$G_d(s)$	Output voltage to duty cycle transfer function
$G_i(s)$	Inductor current to duty cycle transfer function
$G_{vg}(s)$	Output voltage to input voltage transfer function
i_L	Inductor current
i_C	Capacitor current
Q	Q of double pole due to LC filter section in buck converter
R	Output load
R_c	Capacitor equivalent series resistance
R_L	Inductor series resistance
R_{on}	Transistor ON resistance
v_L	Voltage across inductor
v_g	Input line voltage

v_o Output load voltage

v_c Compensator output voltage

$T_c(s)$ Current control loop transfer function

$T_i(s)$ Current control current loop transfer function

T_{on} Switch on time

T_{off} Switch off time

T_{sw} Switching period

$T_v(s)$ Voltage control loop transfer function

$T_{v2}(s)$ V^2 control loop transfer function

Chapter 1

Introduction and Thesis organization

1.0 Thesis Introduction

Every Electronic circuit is assumed to operate off some supply voltage which is usually assumed to be constant. A voltage regulator is a power electronic circuit that maintains a constant output voltage irrespective of change in load current or line voltage. Many different types of voltage regulators with a variety of control schemes are used. With the increase in circuit complexity and improved technology a more severe requirement for accurate and fast regulation is desired. This has led to need for newer and more reliable design of dc-dc converters.

The dc-dc converter inputs an unregulated dc voltage input and outputs a constant or regulated voltage. The regulators can be mainly classified into linear and switching regulators. All regulators have a power transfer stage and a control circuitry to sense the output voltage and adjust the power transfer stage to maintain the constant output voltage. Since a feedback loop is necessary to maintain regulation, some type of compensation is required to maintain loop stability. Compensation techniques vary for different control

schemes and a small signal analysis of system is necessary to design a stable compensation circuit.

State space analysis is typically used to develop a small signal model of a converter and then depending on the type of control scheme used, the small signal model of converter is modified to facilitate the design of the compensation network. In contrast to a state space approach, PWM switch modeling develops a small signal of switching components of converter [4].

Behavioral modeling of the IC system represents the functionality of an IC with macro models rather than actual implementation of the circuit using more efficient modeling techniques. Matlab Simulink and Verilog-A are powerful tools to develop behavioral models of electronic system. Simulink offers the advantage of its graphical user interface and block diagram implementation of any system. It also supports writing your own function and integration of C program code.

The study undertaken in this thesis develops a system level design approach for switching voltage regulators of the three major control schemes. The basic converter topologies and their waveforms are reviewed. In Particular, a small signal model along with the various transfer functions of a buck converter are derived using state space method. A very simple and easy technique to arrive at the PWM model and compensation for three types of control schemes: namely voltage control, current control and V^2 control scheme is discussed. The performance of the two control schemes namely voltage mode

and V^2 mode is compared to load and line variation. The current mode response to load and line variation is inferred from simulation results of other two schemes. The buck converter is implemented with all control schemes and the merits and demerits of each of them are highlighted. The simple techniques developed can be applied to the design of any converter system. A set of macro models for all sub-blocks of the three control schemes are connected to come up with complete dc-dc converter models suitable for simulation. The control circuitry is discussed and implemented. The V^2 control scheme is tested to study the feasibility of its implementation on silicon on sapphire technology. The complete macro model is used to get performance metrics of each sub-block and to establish a road map for silicon on sapphire implementation.

System level models are implemented using the simulink in Matlab. The following study provides details of methodologies for designing each component or block used in the switching regulator. Finally, simulation results are presented for voltage and V^2 control schemes and their performance results are compared and inferences are drawn on the performance of current mode control.

1.1 Background Study

1.1.0 Preliminary Studies

Behavioral modeling is a fast, efficient and easy manner to establish a given theory and more importantly the most efficient manner to develop a direct comparison between competing methods. The voltage control scheme is the basis for more advanced

control schemes [4]. In [7], a simulink implementation of voltage controlled buck converter is presented. Voltage control has a slow transient response due to the bandwidth limitation of the error amplifier in the feedback path. The DC-DC converter is inherently a high ripple system and to exploit this feature current mode control [4] was widely used for better transient response to line variation. However this approach depends on error amplifier speed to control load variation. The continuous time model of current mode control is developed in [11]. The UC1842 [19] and LTC1625 [18] are IC implementations of current mode control while they differ in inductor current sensing techniques. The V^2 [1] control scheme satisfies the need for fast transient response to both load and line variation. However, to my knowledge there is no literature quantifying the V^2 scheme providing or allowing for a direct comparison to current or voltage schemes. This thesis accomplishes the task of deriving small signal models and Matlab models allowing for direct performance comparisons of V^2 scheme to current and voltage mode. The CS51313 [3] and NCP1570 [17] are recent IC implementation of this scheme. A new hybrid control scheme combining both current and V^2 control is discussed in [9]. In this thesis all analysis are for constant frequency control or pulse width modulation.

1.1.1 Control bandwidth and transient response

The feedback loop design is critical to stable and accurate operation of switching regulators. [20] discuss the control loop gain and bandwidth relation to transient response. A critical bandwidth exists above which a spike in transient response cannot be reduced. Also high bandwidth systems are more susceptible to noise. Since the state space averaged models are accurate only up to half of the switching frequency, the loop

bandwidth is chosen around one fourth of switching frequency. High DC gain in the loop is required to maintain the DC accuracy and sufficient phase margin for stability, avoiding ringing or under damping.

The analysis of all three control schemes in this thesis develops the loop gain equation with compensator. Bode plots for the loop assuming a compensator equal to unity is observed and the compensator is designed for desired phase margin and gain. In [5] the different compensator techniques and their effect on steady state error, percent overshoot are illustrated.

1.2 Thesis Organization

This documentation is divided into seven chapters. Chapter 2 covers the basic topologies of different types of converters and their operation. Chapter 3 reviews the state space analysis of buck converter. The Inductor and transistor parasitics are added to traditional methods. Chapter 4 describes the PWM modeling and compensation of the voltage control, current control and V^2 control schemes. Chapter 5 presents the MATLAB simulink implementation of the buck converter with all three control scheme and V^2 control scheme transient response to load and line variations are shown. Chapter 6 details the implementation of gate drive circuitry. Chapter 7 concludes the discussion by proposing future work beyond this study. Appendix A presents the simulation results from PCB board of gate drive circuitry. Appendix B details about implementation of DC-DC converter in simulink.

Chapter 2

Switched Converter Topologies Overview

2.0 Introduction

Switching regulators are preferred over linear regulators for their high efficiency and providing step up, step down or inverter output unlike linear regulator which does only step down operation. In practice, the conversion efficiency of linear regulators is limited to only 30% and they find application in analog circuits to ensure nearly constant supply voltage providing high power supply rejection ratio (PSRR).

In switching regulator circuits, semiconductor switches control the dynamic transfer of power from input to output with very short transition times. Because of this switching action there is ripple added to output voltage. The output requirement is a dc voltage with a minimum superimposition of ac ripple. Pulse width modulation (PWM) is the most widely used method for controlling the output voltage. It maintains a constant switching frequency and varies the duty cycle. Duty cycle is defined as the ratio of switch on time to reciprocal of the switching frequency (f_{sw}). Since the switching frequency is fixed, this modulation scheme has a relatively narrow noise spectrum allowing a simple low pass filter to sharply reduce peak-to-peak ripple at output voltage. This requirement

is achieved by arranging an inductor and capacitor in the converter in such a manner as to form a low pass filter network. This requires the frequency of low pass filter to be much less than switching frequency (f_{sw}).

The following section discusses various converter topologies and their operation. Idealized circuits are considered for ease of understanding and explanation. The key difference between each is the arrangement of the switch and output filter inductor and capacitor. A more rigorous analysis of the buck converter is completed in chapter 3.

2.1 Buck Converter

The buck converter is used for step down operation. A buck converter with its output filter arrangement is as shown in figure 2.1

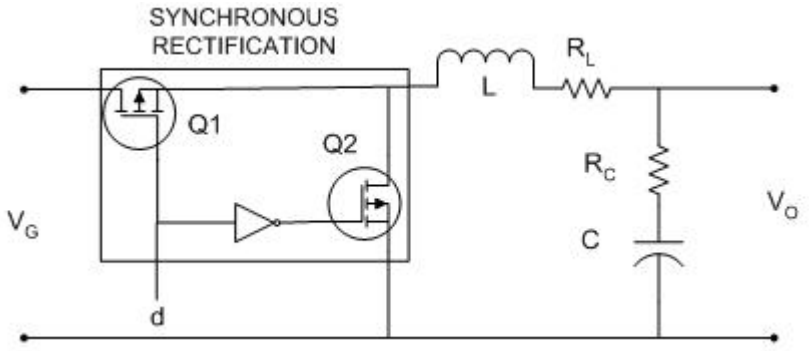

Figure 2.1: Buck Converter.

When the transistor Q1 is on and Q2 is off, the input voltage appears across the inductor and current in inductor increases linearly. In the same cycle the capacitor is charged. When the transistor Q2 is on and Q1 is off, the voltage across the inductor is

reversed. However, current in the inductor cannot change instantaneously and the current starts decreasing linearly. In this cycle also the capacitor is also charged with the energy stored in the inductor.

There is the possibility of two modes of operation namely continuous and discontinuous mode. In continuous mode, the inductor current never reaches zero and in discontinuous mode the inductor current reaches zero in one switching cycle. At lighter load currents the converter operates in discontinuous mode. The regulated output voltage in discontinuous mode no longer has a linear relationship with the input voltage as in continuous conduction mode operation.

2.1.1 Synchronous rectification

The transistor Q2 is used instead of a diode for higher efficiency. This is synchronous rectification. The forward voltage drop across a diode during the second cycle is appreciable and reduces the converter efficiency. To the contrary in a well designed circuit transistor voltage is much less than the forward diode voltages drop. However, synchronous rectification requires non-overlap logic to avoid supply shunt currents which results when both transistors are on.

2.1.2 Inductor Volt-Second Balance

Analyzing the inductor current waveform determines the relationship between output and input voltage in terms of duty cycle. In a well designed converter, the main objective is to have small percentage of ripple at the output. As a result, the output voltage can be approximated by its DC component [5]. Inductor current is found by

integrating the inductor voltage waveform. Inductor voltage and current waveforms for a buck converter are as shown in figure 2.2.

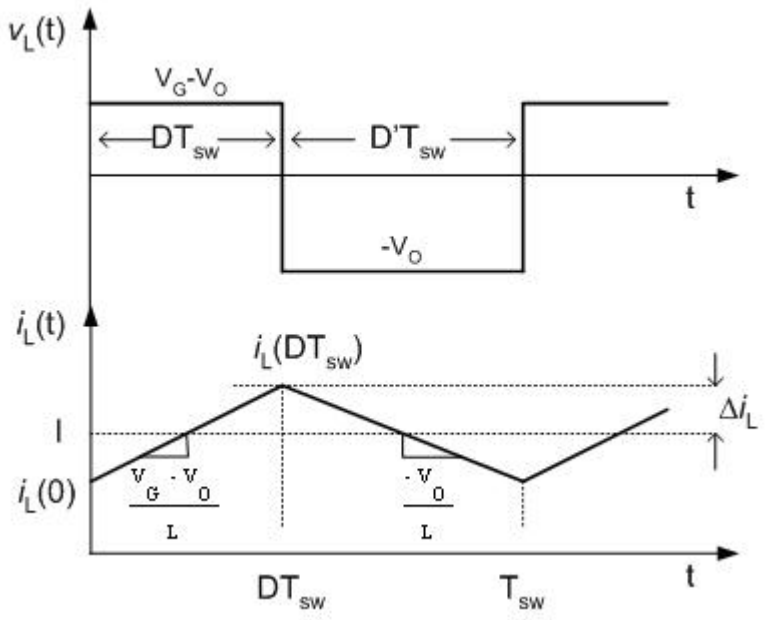

Figure 2.2: Steady-state inductor voltage and current waveform, buck converter

In steady state, the observation that over one switching period the net change in inductor current is zero is the principle of inductor volt second balance. The inductor voltage definition is given by

$$v_L(t) = L\frac{di_L}{dt} \tag{2.1}$$

Integration over one complete switching period yields,

$$i_L(T_{SW}) - i_L(0) = \frac{1}{L}\int_0^{T_{sw}} v_L(t)dt \tag{2.2}$$

The left hand side of above equation is zero. As a result (2.2) can be written as;

$$\int_0^{T_{sw}} v_L(t)dt = 0 \tag{2.3}$$

The equation 2.3 has the unit of volt-seconds or flux-linkages. Alternatively, total area under the $v_L(t)$ waveform over one switching period must be zero. Area under the $v_L(t)$ curve is given by

$$A = \int_0^{T_{sw}} v_L(t)dt = (V_G - V_O)(DT_{sw}) + (-V_O)(D'T_{sw}) \tag{2.4}$$

Average value of inductor voltage is given by,

$$\langle v_L \rangle = \frac{A}{Tsw} = D(V_G - V_O) + D'(-V_O) \tag{2.5}$$

By equating $\langle v_L \rangle$ to zero and using relation d+d' = 1, and solving for VOUT yields

$$V_O = D.V_G \tag{2.6}$$

2.1.3 Capacitor charge balance

Similar to the inductor volt-second balance, the defining equation for capacitors is

$$i_C(t) = C\frac{dv_C(t)}{dt} \tag{2.7}$$

Integration over one complete switching period yields,

$$v_c(T_{sw}) - v_c(0) = \frac{1}{C}\int_0^{T_{sw}} i_c(t)dt \tag{2.8}$$

In steady state, the net change over one switching period of the capacitor voltage must be zero, so that the left hand side of the above equation is zero. Equivalently stated the average value or the DC component of the capacitor must be zero at equilibrium.

$$\langle i_C \rangle = \frac{1}{T_{SW}} \int_0^{T_{sw}} i_C(t)dt = 0 \qquad (2.9)$$

Thus the principle of capacitor charge balance can be used to find the steady state currents in a switching converter.

2.2 Boost Converter

The boost converter is capable of producing a dc output voltage greater in magnitude than the dc input voltage. The circuit topology for a boost converter is as shown in figure 2.3.

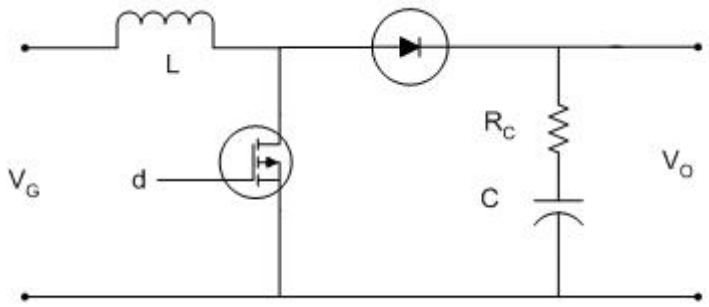

Figure 2.3: Boost Converter

When the transistor Q1 is on the current in inductor L, rises linearly and at this time capacitor C, supplies the load current, and it is partially discharged. During the second interval when transistor Q1 is off, the diode D1, is on and the inductor L, supplies the load and, additionally, recharges the capacitor C. The steady state inductor current and voltage waveform is shown in figure 2.4.

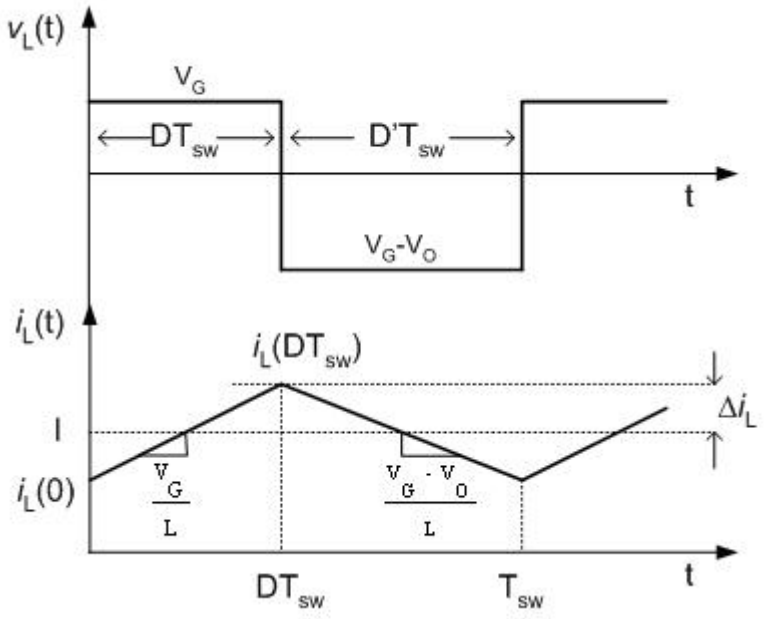

Figure 2.4: Steady-state inductor voltage and current waveform, boost converter

Using the inductor volt balance principle to get the steady state output voltage equation yields

$$V_G . T_{ON} + (V_G - V_O).T_{OFF} = 0 \tag{2.10}$$

$$\frac{V_O}{V_G} = \frac{T_{SW}}{T_{OFF}} = \frac{1}{1-D} \tag{2.11}$$

Since the converter output voltage is greater than the input voltage, the input current which is also the inductor current is greater than output current. In practice the inductor current flowing through, semiconductors Q1 and D1, the inductor winding resistance becomes very large and with the result being that component non-idealities may lead to large power loss. As the duty cycle approaches one, the inductor current becomes very large and these component nonidealities lead to large power losses. Consequently, the efficiency of the boost converter decreases rapidly at high duty cycles.

The detailed analysis of boost converter is beyond the scope of this thesis. The guidelines to select the inductor and capacitor for boost converter are discussed in reference [5]. The small signal model of boost converter and its control to output transfer function are explained in detail in reference [15].

2.3 Buck-Boost Converter

The buck-boost converter is capable of producing a dc output voltage which is either greater or smaller in magnitude than the dc input voltage. The arrangement for the buck-boost converter is as shown in figure 2.5.

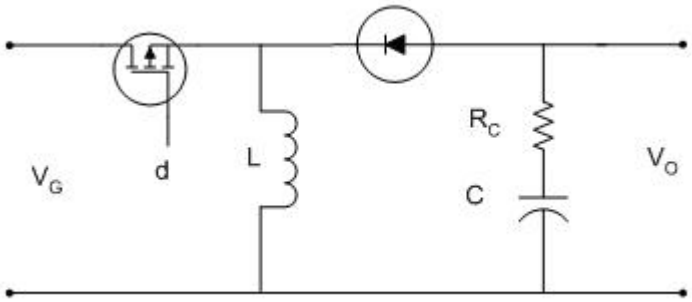

Figure 2.5: Buck-boost converter

When the transistor Q1 is on, input voltage is applied across the inductor and the current in inductor L rises linearly. At this time the capacitor C, supplies the load current, and it is partially discharged. During the second interval when the transistor is off, the voltage across the inductor reverses in polarity and the diode conducts. During this interval the energy stored in the inductor supplies the load and, additionally, recharges the capacitor. The steady state inductor current and voltage waveform is shown in figure 2.6

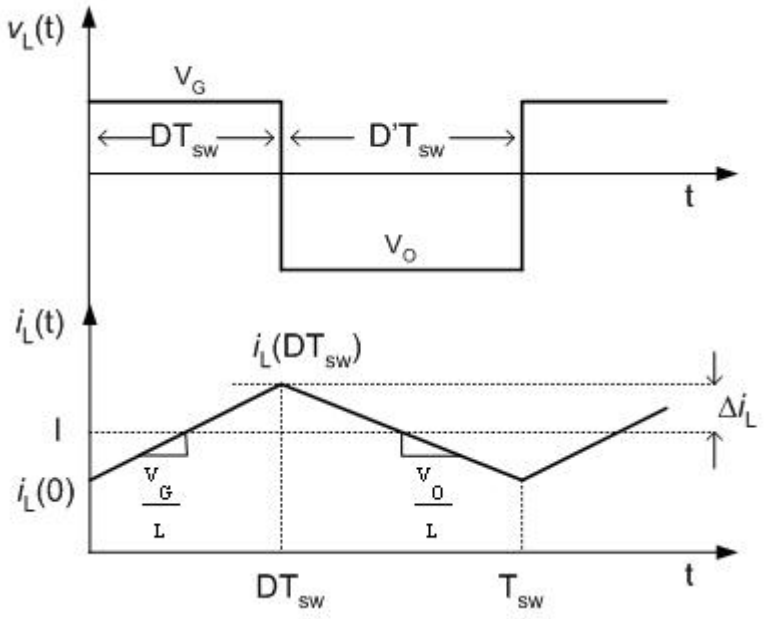

Figure 2.6: Steady-state inductor voltage and current waveform, buck-boost converter

Using the inductor volt balance principle to find the steady state output voltage equation yields

$$V_G . T_{ON} + V_O . T_{OFF} = 0 \tag{2.12}$$

$$\frac{V_O}{V_G} = \frac{T_{SW}}{T_{OFF}} = -\frac{D}{1-D} \tag{2.13}$$

The d varies between 0 and 1 and thus output voltage can be lower or higher than the input voltage in magnitude but opposite in polarity.

2.4 Cuk Converter

Cuk converters are derived from the cascading of buck and boost converters. The buck, boost and buck-boost converter all transfer energy between input and output using the inductor and analysis is based on voltage balance across the inductor. The Cuk

converter utilizes capacitive energy transfer and analysis is based on current balance of the capacitor.

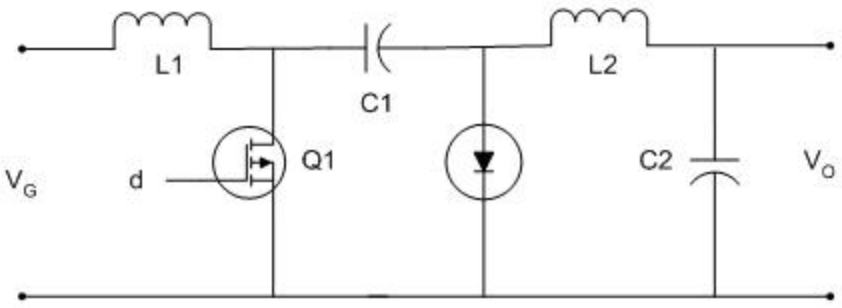

Figure 2.7: Cuk Converter

When the diode is on, the capacitor is connected to input through L1 and source energy is stored in capacitor. During this cycle the current in C1 is I_{IN}. When transistor Q1 is on, the energy stored in the capacitor is transferred to the load through inductor L2. During this cycle the current in C1 is $I_{OUT.}$ The capacitive charge balance principle is used to obtain steady state solution.

$$I_G . T_{OFF} + (-I_O) . T_{ON} = 0 \tag{2.14}$$

$$\frac{I_O}{I_G} = \frac{(1-D)}{D} \tag{2.15}$$

Using the power conservation rule

$$\frac{V_O}{V_G} = -\frac{D}{(1-D)} \tag{2.16}$$

This voltage ratio is the same as the buck-boost converter.

2.5 Isolated DC-DC converter

2.5.1 Transformer Isolation

The use of a transformer allows dc isolation and multiple outputs in a dc-dc converter. Since the transformer size and weight vary inversely with frequency, significant improvements can be made by incorporating the transformer into the converter. Through a proper choice of transformer turns ratio and switching frequency stresses imposed on the transistors and diodes can be minimized. This leads to improved efficiency at lower cost.

Multiple dc outputs are obtained by adding multiple secondary windings and converter secondary side circuits. The secondary turns ratios are appropriately chosen to get the desired output voltages. Many different topologies are discussed in [5]

2.5.2 Flyback Converter

When the transistor Q1 is turned on, the energy is stored in the power transformer while the load current is supplied from output capacitor C. When the transistor is turned off, the energy stored in transformer is transferred to output as load current and to recharge the capacitor.

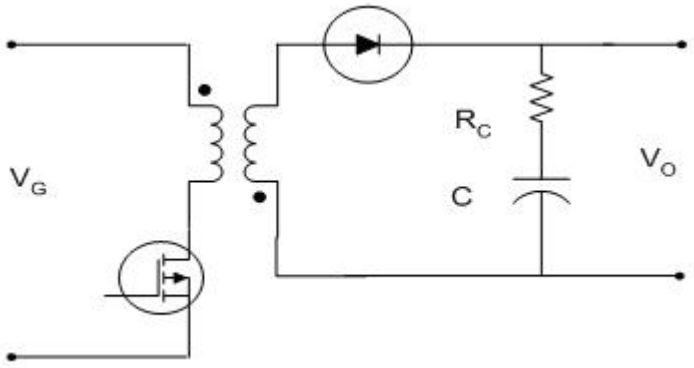

Figure 2.8: Flyback converter

One of the major advantages of Flyback converter is that they don't require an output filter inductor, thus saving cost and volume. This also makes Flyback converters valuable for high output voltages unlike forward converters which have an output inductor potentially causing problems as the inductor must sustain large voltages. Flyback also doesn't require a high voltage freewheeling diode.

The filter capacitor at the output is typically larger in Flyback converters as it alone supplies the load current when the transistor is ON. Equivalently the full DC current flows from ground through the capacitor to the load during the transistor ON time. Thus the ripple current rating of the capacitor and output ripple voltage requirement collectively determines the final choice of output filter capacitor.

This chapter discusses about the basic topologies of switching regulator and shows their output to input voltage relationship with duty cycle. The analysis done in further chapters is specifically for buck converter. But the analysis can be modified for any converter topology.

Chapter 3

Buck Converter

3.0 Introduction

Switch mode power converters are nonlinear and discontinuous in nature and are cumbersome to analyze directly using standard linear circuit theory due to their inherent large signal nature. Linearizing the converter circuit is essential to understanding converter circuit as it allows the designer to apply the control theory. Any model of converter circuits should readily accommodate both monitor and control circuitry. A typical dc-dc system incorporating a buck converter and feedback loop block diagram is shown in figure 3.1.

A dynamic switching converter model is helpful in analyzing how the variations in the input voltage, the load current, or the duty cycle affect the output voltage. Traditionally, State space representation of dynamical systems is used to derive the small-signal averaged equations of PWM switching converters. However, in [4], a simplified model is developed by modeling only the non-linear switching action of a converter as a three terminal circuit element. This model is easily applied to any

converter topology. The following section summarizes the use of state space approach for buck converter modeling, which can be generalized to any converter topology.

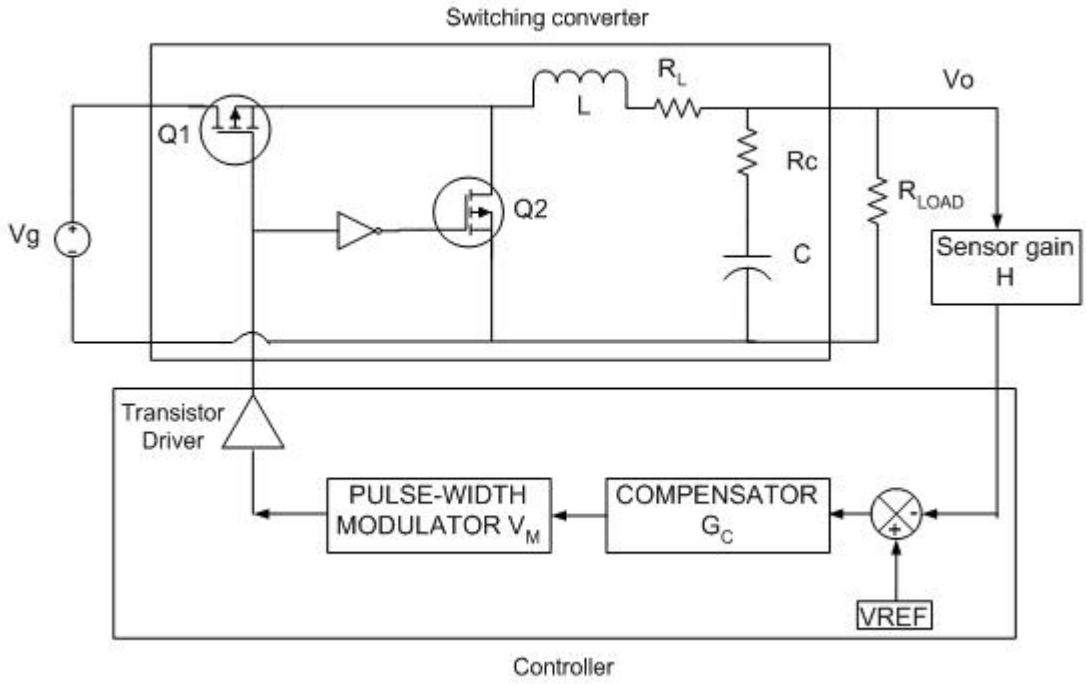

Figure 3.1: Buck converter regulator system

3.2 Basic state space averaged model

A state space description is a canonical form for writing the differential equations that describe a system. Although the state space averaged model has been derived using ideal components [5]. The following analysis takes into consideration the inductor and capacitor parasitic and also models the transistor ON voltage. For a converter system, the physical state variables are the independent inductor currents and capacitor voltages to form a state vector x(t), and the converter is driven by independent sources that form input vector u(t). K is a matrix containing the values of capacitance and inductance. y(t)

is a vector consisting the output variable and any other variable dependent on state vector x(t).

During the first subinterval, the converter reduces to a linear circuit that can be described by the following state equations

$$\begin{aligned} \mathrm{K}\frac{d\mathrm{x}(\mathrm{t})}{d\mathrm{t}} &= \mathrm{A}_1\mathrm{x}(\mathrm{t}) + \mathrm{B}_1\mathrm{u}(\mathrm{t}) \\ \mathrm{y}(\mathrm{t}) &= \mathrm{C}_1\mathrm{x}(\mathrm{t}) + \mathrm{E}_1\mathrm{u}(\mathrm{t}) \end{aligned} \tag{3.1}$$

During the second subinterval, the converter reduces to another linear circuit that can be described by the following state equations

$$\begin{aligned} \mathrm{K}\frac{d\mathrm{x}(\mathrm{t})}{d\mathrm{t}} &= \mathrm{A}_2\mathrm{x}(\mathrm{t}) + \mathrm{B}_2\mathrm{u}(\mathrm{t}) \\ \mathrm{y}(\mathrm{t}) &= \mathrm{C}_2\mathrm{x}(\mathrm{t}) + \mathrm{E}_2\mathrm{u}(\mathrm{t}) \end{aligned} \tag{3.2}$$

A state space averaged model that describes the converter in equilibrium is

$$\begin{aligned} 0 &= \mathrm{AX} + \mathrm{BU} \\ \mathrm{Y} &= \mathrm{CX} + \mathrm{EU} \end{aligned} \tag{3.3}$$

where the averaged matrices are

$$\begin{aligned} \mathrm{A} &= D\mathrm{A}_1 + D'\mathrm{A}_2 \\ \mathrm{B} &= D\mathrm{B}_1 + D'\mathrm{B}_2 \\ \mathrm{C} &= D\mathrm{C}_1 + D'\mathrm{C}_2 \\ \mathrm{E} &= D\mathrm{E}_1 + D'\mathrm{E}_2 \end{aligned} \tag{3.4}$$

The above equation can be solved to find the equilibrium state and output vectors

$$\begin{aligned} \mathrm{X} &= -\mathrm{A}^{-1}\mathrm{BU} \\ \mathrm{Y} &= (-\mathrm{CA}^{-1}\mathrm{B} + \mathrm{E})\mathrm{U} \end{aligned} \tag{3.5}$$

The state equations of the small signal ac model are

$$K\frac{d\hat{x}(t)}{dt} = A\hat{x}(t) + B\hat{u}(t) + \{(A_1 - A_2)X + (B_1 - B_2)U\}\hat{d}(t)$$
$$\hat{y}(t) = C\hat{x}(t) + E\hat{u}(t) + \{(C_1 - C_2)X + (E_1 - E_2)U\}\hat{d}(t) \quad (3.6)$$

The quantities $\hat{x}(t)$, $\hat{u}(t)$, $\hat{y}(t)$ and $\hat{d}(t)$ are small ac variations about the equilibrium solution.

3.3 State space averaged model of buck converter

The first task is to write the state equation for the two switch positions. To get a more accurate small signal model, transistor on resistance, inductor resistance and capacitance ESR are taken into account. The equivalent circuit when switch Q1 is on and Q2 is off is as shown in figure 3.2.

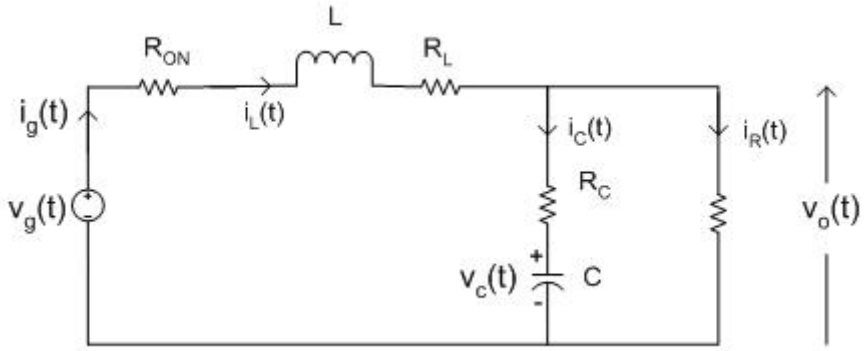

Figure 3.2: Buck converter ON state

The differential equations related to state variables are

$$
\begin{aligned}
&v_g(t) = R_{on} i_L(t) + L\frac{di_L(t)}{dt} + R_L i_L(t) + v_o(t) \\
&\therefore L\frac{di_L(t)}{dt} = v_g(t) - R_{on} i_L(t) - R_L i_L(t) - v_o(t) \\
&\text{Also, } C\frac{dv_C(t)}{dt} = \frac{R}{R+R_C} i_L(t) - \frac{1}{R+R_C} v_C(t) \\
&\text{And, } v_o(t) = i_R R
\end{aligned}
\tag{3.7}
$$

Using kirchoff voltage and current laws to obtain state equation as

$$
\begin{aligned}
&L\frac{di_L(t)}{dt} = v_g(t) - [R_{on} + R_L + (R//R_C)] i_L(t) - \frac{R}{R+R_C} v_C(t) \\
&C\frac{dv_C(t)}{dt} = \frac{R}{R+R_C} i_L(t) - \frac{1}{R+R_C} v_C(t) \\
&i_g(t) = i_L(t) \\
&v_o(t) = (R//R_C) i_L(t) + \frac{R}{R+R_C} v_C(t)
\end{aligned}
\tag{3.8}
$$

State equation matrices are given as

$$
\begin{aligned}
&\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -(R_{on} + R_L + (R//R_C)) & \frac{-R}{R+R_C} \\ \frac{R}{R+R_C} & \frac{-1}{R+R_C} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} v_g(t) \\
&\begin{bmatrix} v_o(t) \\ i_g(t) \end{bmatrix} = \begin{bmatrix} (R//R_C) & \frac{R}{R+R_C} \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_g(t)
\end{aligned}
\tag{3.9}
$$

Therefore,

$$A1 = \begin{bmatrix} -(R_{on} + R_L + (R//R_C)) & \frac{-R}{R+R_C} \\ \frac{R}{R+R_C} & \frac{-1}{R+R_C} \end{bmatrix},$$

$$B1 = \begin{bmatrix} 1 \\ 0 \end{bmatrix}, \qquad (3.10)$$

$$C1 = \begin{bmatrix} (R//R_C) & \frac{R}{R+R_C} \\ 1 & 0 \end{bmatrix}$$

$$E1 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

Similarly the equivalent circuit when switch Q1 is off and Q2 is ON

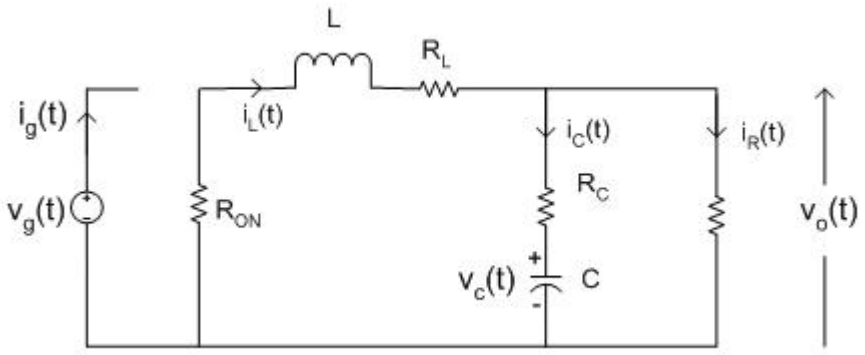

Figure 3.3: Buck converter OFF state

State equation for above circuit is given by

$$L\frac{di_L(t)}{dt} = -[R_{on} + R_L + (R//R_C)]i_L(t) - \frac{R}{R+R_C}v_C(t)$$

$$C\frac{dv_C(t)}{dt} = \frac{R}{R+R_C}i_L(t) - \frac{1}{R+R_C}v_C(t) \qquad (3.11)$$

$$i_g(t) = 0$$

$$v_o(t) = (R//R_C)i_L(t) + \frac{R}{R+R_C}v_C(t)$$

State equation matrices are given as

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -(R_{on}+R_L+(R//R_C)) & \frac{-R}{R+R_C} \\ \frac{R}{R+R_C} & \frac{-1}{R+R_C} \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_g(t)$$

$$\begin{bmatrix} v_o(t) \\ i_g(t) \end{bmatrix} = \begin{bmatrix} (R//R_C) & \frac{R}{R+R_C} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_g(t) \qquad (3.12)$$

Therefore,

$$A2 = \begin{bmatrix} -(R_{on}+R_L+(R//R_C)) & \frac{-R}{R+R_C} \\ \frac{R}{R+R_C} & \frac{-1}{R+R_C} \end{bmatrix},$$

$$B2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, \qquad (3.13)$$

$$C2 = \begin{bmatrix} (R//R_C) & \frac{R}{R+R_C} \\ 0 & 0 \end{bmatrix}$$

$$E2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

3.4 Steady state equilibrium

As described in section 3.2, the steady state equilibrium equations of buck converter can be defined as

$$0 = \begin{bmatrix} -(R_{on}+R_L+(R//R_C)) & \frac{-R}{R+R_C} \\ \frac{R}{R+R_C} & \frac{-1}{R+R_C} \end{bmatrix}\begin{bmatrix} I_L \\ V_C \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} V_G$$

$$\begin{bmatrix} V_O \\ I_G \end{bmatrix} = \begin{bmatrix} (R//R_C) & \frac{R}{R+R_C} \\ 1 & 0 \end{bmatrix}\begin{bmatrix} I_L \\ V_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_G \qquad (3.14)$$

Solving the above matrices to obtain the steady state solution as

$$\frac{V_O}{V_G} = D\frac{R}{R + R_L + R_{ON}}$$
$$I_G = D^2 \frac{V_G}{R + R_L + R_{ON}} \tag{3.15}$$

When the parasitic resistance of an inductor and on resistance of the transistor is included, the ideal voltage transfer function is multiplied by a correction factor. The efficiency of the converter can be calculated as

$$\eta = \frac{Pout}{Pin} = \frac{V_O I_O}{V_G I_G} = \frac{V_O}{DV_G} = \frac{R}{R + R_L + R_{ON}} \tag{3.16}$$

3.5 Small signal ac model

As detailed in section 3.2, the small signal ac equation can be represented in matrices form as

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \begin{bmatrix} \frac{d\hat{i}_L(t)}{dt} \\ \frac{d\hat{v}_c(t)}{dt} \end{bmatrix} = \begin{bmatrix} -(R_{on} + R_L + (R//R_C)) & \frac{-R}{R+R_C} \\ \frac{R}{R+R_C} & \frac{-1}{R+R_C} \end{bmatrix} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_c(t) \end{bmatrix} + \begin{bmatrix} D \\ 0 \end{bmatrix} \hat{v}_g(t) + \begin{bmatrix} Vg \\ 0 \end{bmatrix} \hat{d}$$

$$\begin{bmatrix} \hat{v}_o(t) \\ \hat{i}_g(t) \end{bmatrix} = \begin{bmatrix} (R//R_C) & \frac{R}{R+R_C} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_c(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \hat{v}_g(t) + \begin{bmatrix} 0 \\ I_L \end{bmatrix} \hat{d}$$

The small signal ac equations and the equivalent ac circuit is as shown

$$
\begin{aligned}
L\frac{d\hat{i}_L(t)}{dt} &= -[R_{on} + R_L + (R//R_C)]\hat{i}_L(t) - \frac{R}{R+R_C}\hat{v}_c(t) + D\hat{v}_g(t) + V_g\hat{d} \\
C\frac{d\hat{v}_c(t)}{dt} &= \frac{R}{R+R_C}\hat{i}_L(t) - \frac{1}{R+R_C}\hat{v}_c(t) \\
\hat{i}_g(t) &= D\hat{i}_L(t) + I_L\hat{d} \\
\hat{v}_o(t) &= (R//R_C)\hat{i}_L(t) + \frac{R}{R+R_C}\hat{v}_c(t)
\end{aligned}
\tag{3.17}
$$

Also, to model the variation of load current, a load current source is added in parallel to the load resistance R. Taking the laplace transform of the above equation and arranging to result in the small signal equivalent ac model as shown in figure 3.4.

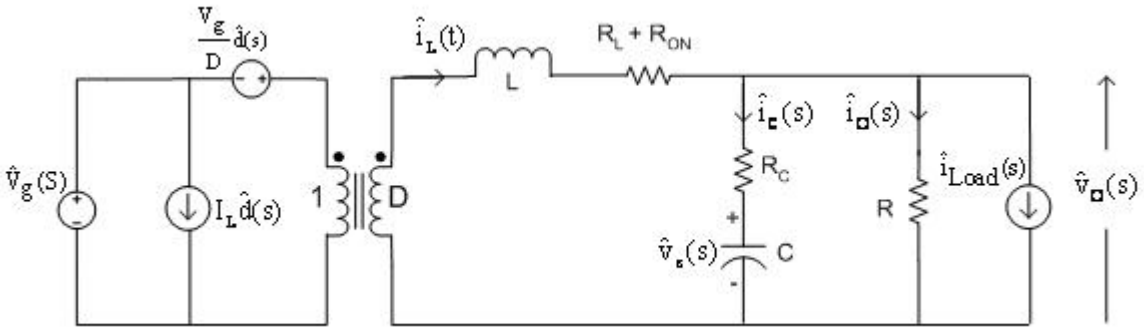

Figure 3.4: ac model of buck converter

The small signal transfer functions are readily derived from this ac small signal model. The most important transfer functions are variation in output voltage with variation in duty cycle and input voltage.

$$
\begin{aligned}
G_d(s) &= \frac{\hat{v}_o(s)}{\hat{d}(s)}\bigg|_{\hat{v}_g(s)=0,\,\hat{i}_{Load}(s)=0} \\
G_i(s) &= \frac{\hat{i}_L(s)}{\hat{d}(s)}\bigg|_{\hat{v}_g(s)=0,\,\hat{i}_{Load}(s)=0} \\
G_{vg}(s) &= \frac{\hat{v}_o(s)}{\hat{v}_g(s)}\bigg|_{\hat{d}(s)=0,\,\hat{i}_{Load}(s)=0} \\
Z_{out} &= \frac{\hat{v}_o(s)}{\hat{i}_{Load}(s)}\bigg|_{\hat{d}(s)=0,\,\hat{v}_g(s)=0}
\end{aligned}
\tag{3.18}
$$

Evaluating the above expression from the small signal ac model yields,

$$
G_d(s) = \frac{V_O}{D}\left[\frac{1+sCR_C}{1+s\left[\frac{L}{R+R_{ON}+R_L}+\frac{CR(R_{ON}+R_L)}{R+R_{ON}+R_L}+CR_C\right]+s^2LC\left[\frac{R+R_C}{R+R_{ON}+R_L}\right]}\right]
$$

$$
G_i(s) = \frac{V_G}{R+R_{ON}+R_L}\left[\frac{1+sC(R_C+R)}{1+s\left[\frac{L}{R+R_{ON}+R_L}+\frac{CR(R_{ON}+R_L)}{R+R_{ON}+R_L}+CR_C\right]+s^2LC\left[\frac{R+R_C}{R+R_{ON}+R_L}\right]}\right]
$$

$$
G_{vg}(s) = \left[\frac{DR}{R+R_{ON}+R_L}\right]\left[\frac{1+sCR_C}{1+s\left[\frac{L}{R+R_{ON}+R_L}+\frac{CR(R_{ON}+R_L)}{R+R_{ON}+R_L}+CR_C\right]+s^2LC\left[\frac{R+R_C}{R+R_{ON}+R_L}\right]}\right]
$$

$$
Z_{out} = R\|R_c\left[\frac{\left(s+\frac{R_L+R_{ON}}{L}\right)\left(s+\frac{1}{R_CC}\right)}{s^2+s\left[\frac{1}{(R+R_C)C}+\frac{R_L+R_{ON}+(R\|R_C)}{L}\right]+\left[\frac{R+R_L+R_{ON}}{LC(R+R_C)}\right]}\right]
$$

3.6 Component Selection

3.6.1 Inductor

The magnitude of switching ripple in the output voltage in a properly designed DC supply is much less than the dc component. As a result the output voltage is approximated by its dc component and the value of inductor can be calculated by using the defining equation of the inductor

$$V = L\frac{di_L}{dt} \tag{3.19}$$

Referring back to figure 2.1 for the steady state inductor current waveform, it can be easily deduced the change in inductor current is its slope times the length of subinterval.

$$\Delta I_L = (V_G - V_O) \cdot \frac{D}{L} \cdot T_{sw} \tag{3.20}$$

The ripple requirement in inductor current sets the inductor value. Typically ΔI_L lies in the range of 10-20% of the full load or maximum value of the dc component of I_O. The peak inductor current which is equal to the DC component plus the peak to average ripple $\Delta I_L/2$, flows through the semiconductor switches and is necessary when specifying device ratings. To reduce the peak current a larger value of inductor is required. A secondary benefit in lowering the ripple current is that it reduces core/inductor, ESR and load losses

3.6.2 Capacitor

The output section of the buck converter is as shown in figure 3.5. The only steady state component of output capacitor current is that arising from the inductor

current ripple. Hence inductor current cannot be neglected when calculating the output voltage ripple. The inductor current contains both a DC and ripple current component. The DC component must flow entirely through the load resistance R. While the ac switching ripple divides between the load resistance R and the filter capacitor C.

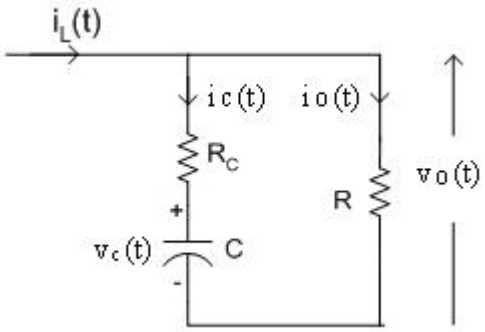

Figure 3.5: Output filter section-buck converter

The series impedance of R and C at switching frequency is given by

$$Z_{Rc,C} = R_C + \frac{1}{j\omega C}$$
$$\left|Z_{Rc,C}\right| = \sqrt{Rc^2 + \frac{1}{\omega^2 C^2}} \qquad (3.21)$$

To ensure minimum ripple at rated output load, the equivalent condition states that the series R C branch impedance appear resistive over the frequency band of switching component. This is the condition of minimum ripple and is a reason for requiring low ESR

$$\sqrt{Rc^2 + \frac{1}{\omega^2 C^2}} << R$$
$$C >> \frac{1}{\omega\sqrt{(R^2 - R_C{}^2)}} \qquad (3.22)$$

The output voltage ripple requirement puts an upper bound on capacitor ESR. Thus the voltage ripple peak magnitude is estimated by

$$\Delta V = \Delta I_L \cdot R_c + \frac{\Delta I_L}{8 \cdot C \cdot f_{sw}}$$
$$\Delta V \cong \Delta I_L \cdot R_c \tag{3.23}$$

With the ESR requirement met, the capacitance value can be selected to achieve adequate filtering. Capacitors are typically paralleled to meet the ESR requirement. An alternate approach to reduce ΔV is to reduce ΔI but this requires a larger value of inductor.

3.6.3 Power mosfet selection

Mosfets are used as power switches for their near zero DC gate current and fast switching times. Its turn-on delay time is proportional to Cgs which is illustrated as Ciss minus Crss in datasheets. The delay time is equal to product of Cgs and impedance of source driving it ignoring any miller effect. It is a requirement to have delay time much less than switching period. Mosfets power dissipation impacts converter efficiency. This includes Rdson conduction losses, leakage losses, turn on-off switching and gate transition losses. Rdson of the power mosfet determines the current it can handle without excessive power dissipation. Rdson directly affects the converter efficiency. To minimize Rdson, the applied gate signal should be large enough to maintain operation in the linear, triode or ohmic region. Mosfets positive temperature coefficients means conduction loss increases with temperature.

A second important consideration when designing gate drive circuitry is due to Cgd, illustrated as Crss in data sheets. During turn-on and turn-off, the large swing in Vgd requires extra current sourcing and sinking capabilities for the gate drive as a direct result of miller effect.

Chapter 4

Control Schemes and Compensation Techniques

4.0 Introduction

Negative feedback is employed to maintain voltage regulation regardless of disturbances in input voltage, $v_g(t)$, or load current, $i_{load}(t)$, or variations in component values. The duty cycle is varied in the feedback loop to compensate for these variations. A typical block diagram of a Switching regulator is as shown in figure 4.1.

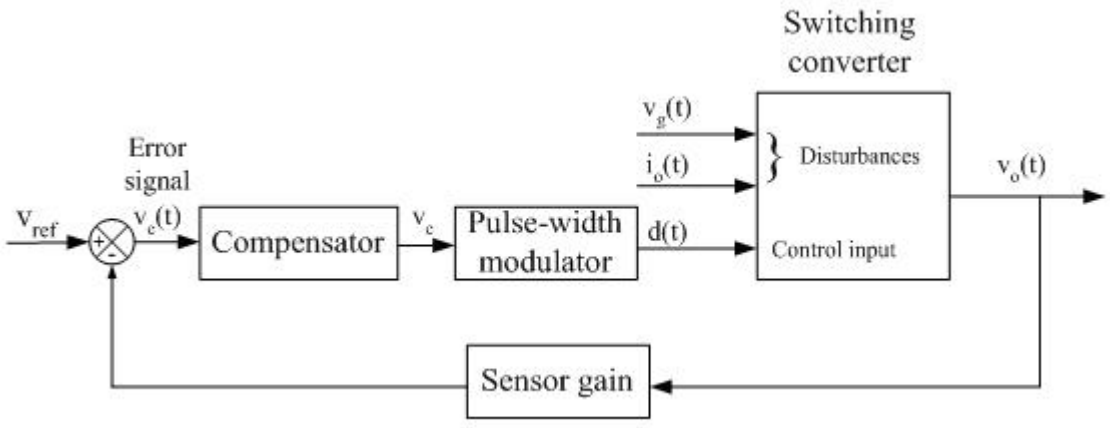

Figure 4.1: Block diagram of feedback system

A voltage reference is used to compare with the output voltage. Sensor gain is used to scale down the output to be equal to voltage reference. The error signal thus

generated is fed to the compensator which is the key part to be designed to ensure stability of total feedback loop. Compensator design affects the overshoot, steady state error and transient response of the loop. The PWM block compares the compensator output with another ramp signal to give the variation in duty cycle. The source from where the ramp signal is generated leads to different control schemes. The three most common control schemes are voltage mode control, current mode control and V^2 control. Other hybrid schemes are derived from combinations of these control schemes [9]

The small signal transfer function for the buck regulator was discussed in chapter 3. The following topics discuss the effect of feedback loop on the small signal transfer function for all the three control schemes. Also, the compensation techniques for each control scheme are discussed.

4.1 Basic control operation

The switching converter along with feedback controller in its simplest form is as shown in the figure 4.2. An internal oscillator operating at switching frequency (f_{sw}) and generates narrow pulses at the start of each switching cycle. The output of the switching converter is subtracted from the reference signal to generate an error signal. This error signal is compared with a ramp signal to generate a pulse to reset the flip-flop and maintain a steady state duty cycle.

For any variations in the input voltage or output load current, the error signal either increases or decreases. If the output voltage increases, the error signal increases and the reset pulse is generated earlier to reduce the duty cycle and eventually lower the output voltage. Similarly, if the output voltage decreases, the error signal decreases and the reset pulse is generated at later duration to increase the duty cycle and bring the output voltage back into equilibrium.

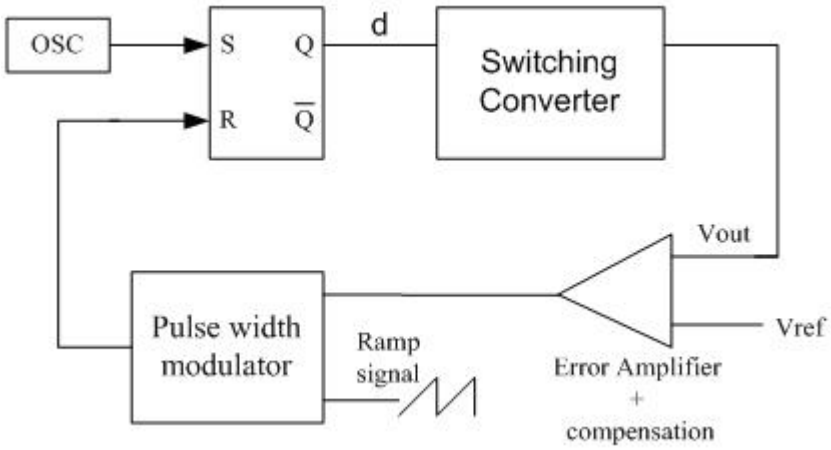

Figure 4.2: Basic control principle

4.2 Frequency response of buck converter

The first step in designing the feedback loop after selecting the components of the converter is to plot the open loop response of buck converter. The transfer function of output voltage to duty cycle was derived in the small signal analysis of buck converter section in chapter 3. The transfer function reveals a left half plane zero associated with ESR of capacitor and a double pole at approximately resonant frequency of LC. Typically, the transfer characteristic peaks at resonant frequency. The magnitude of this

peak is given by the quality factor. Ignoring the inductor series resistance and transistor on resistance, a simple expression for Q can be derived in terms of L, C, R and ESR of capacitor. It can be easily deduced that Q gets lowered as a result of ESR of the capacitor.

$$Q \cong \frac{1}{\left[\sqrt{\frac{L}{C(R+R_C)R}} + R_C\sqrt{\frac{R_C}{(R+R_C)}}\right]} \approx \frac{R}{\left[\sqrt{\frac{L}{C}}\right]} = R\sqrt{\frac{nC'}{L}} \tag{4.1}$$

The asymptotic plot for open loop response with corner frequencies is as shown. The corner frequencies are approximately given by

$$\begin{aligned} f_{LC} &\cong \frac{1}{2\pi\sqrt{LC}} = \frac{Q}{2\pi\, RC} = \frac{Q}{2\pi\, nRC'} \\ f_{ESR} &\cong \frac{1}{2\pi.R_C.C} = \frac{1}{2\pi.R_C'.C'} \end{aligned} \tag{4.2}$$

Where C equals nC' and Rc equal Rc'/n and n equals number of capacitors in parallel

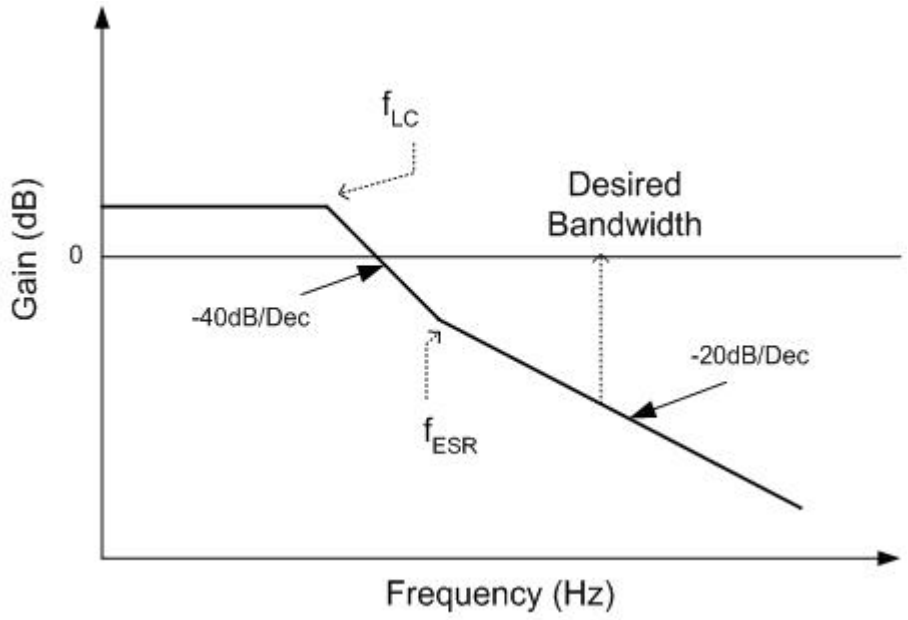

Figure 4.3: Open loop response

The Inductor is fixed by current ripple requirement and the Capacitor chosen large enough such that Q is small. Thus in a well constructed system

$$\begin{aligned} BW &\le 1/4\, f_{SW} \\ BW &\ge 8\text{-}10\, f_{LC} \\ f_{ESR} &\ge 2 f_{LC} \end{aligned} \tag{4.3}$$

Network Compensation is designed in such a way that the total loop gain transfer function crosses 0 dB point with -20dB/dec slope. This ensures sufficient phase margin and in turn closed loop stability. In the use of this model one assumes that Rdson of transistor and series resistance of inductor R_L are much less than R and R_C.

4.3 Voltage mode control

4.3.1 PWM modeling

Traditionally the voltage mode was used in designing the feedback loop. The ramp signal is derived from the oscillator using a simple RC time constant network. The sawtooth linearly varies with time and using the slope of the sawtooth waveform as shown in figure 4.4, it can be easily deduced that

$$d(t) = \frac{v_C(t)}{V_M} \quad \text{for } 0 \le v_C(t) \le V_M \tag{4.4}$$

Small signal variation of the duty cycle with the control voltage is obtained by substituting $V_c(t)$ by ac and dc quantities and taking the partial derivative of duty cycle with respect to control voltage.

$$\frac{\hat{d}(t)}{\hat{v}_C(t)} = \frac{1}{V_M} \tag{4.5}$$

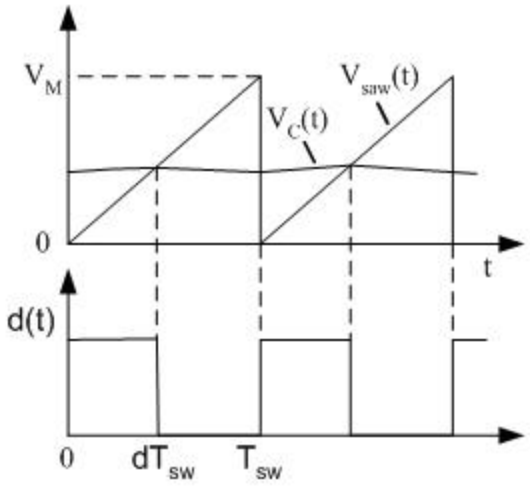

Figure 4.4: PWM voltage mode control

With the PWM block small signal transfer function defined, the small signal model for the voltage mode buck converter is as shown in figure 4.5

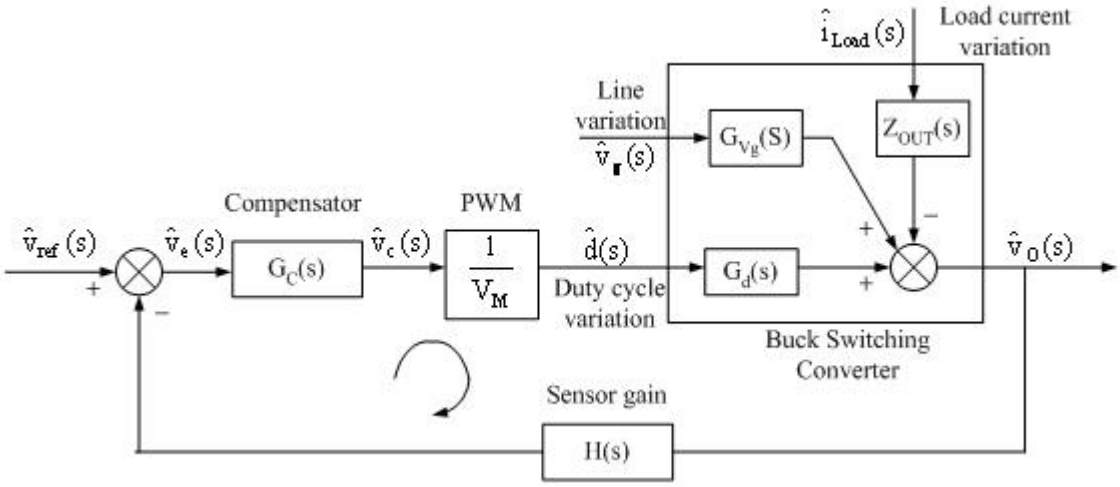

Figure 4.5: Block diagram voltage mode regulator

The small signal model accommodates the variation due to line voltage and load. The effect of the feedback is loop is to reduce the influence of load and line variations. This can be easily verified by writing the equation for each type of variation around the loop

from which it is deduced that the variation due to load and line are reduced by the factor $1+T_v(s)$, where $T_v(s)$ is given as

$$T_v(s) = H(s)G_C(s)\frac{G_d(s)}{V_M} \tag{4.6}$$

4.3.2 Compensation of voltage mode loop

To design the compensation network $T_v(s)$ is plotted assuming Gc(s) equal to one. The phase margin and the required gain are determined to assist in design of the compensator in a manner that total loop gain crosses the 0 dB point with -20dB/decade slope. Additional phase boost is required to meet design stability criteria. Type II compensation can theoretically provide 90 degrees phase boost but it is commonly used for phase boost less than 70 degrees. Typical type II compensation with its gain and phase plot is as shown in figure 4.6.

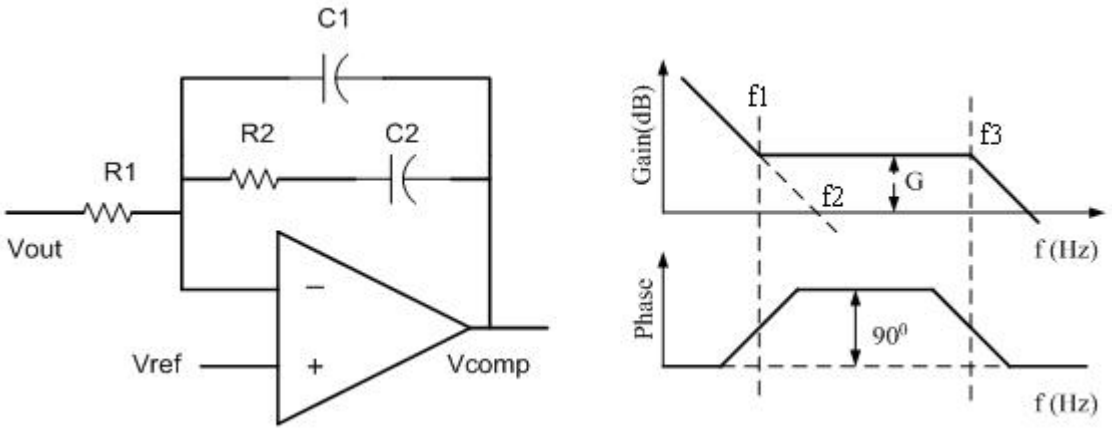

Figure 4.6: Type II compensation

The transfer function of the type II compensator and corner frequencies are given by

$$Gc(s) = \frac{1 + s \cdot R2 \cdot C2}{R1 \cdot R2 \cdot C1 \cdot C2 \cdot s^2 + R1 \cdot (C1 + C2) \cdot s}$$

$$f1 = \frac{1}{2\pi R_2 C_2}, f2 = \frac{1}{2\pi R_1 C_1}, f3 = \frac{1}{2\pi R_2 \frac{C_1 C_2}{C_1 + C_2}}, G = 20\log\left(\frac{R_2}{R_1}\right) \quad (4.7)$$

In type II compensation, a zero is introduced at $0.1f_{LC}$ to give phase boost or advance. Additional gain is required to ensure a -20dB/dec slope at the gain crossover frequency. The additional required gain is determined directly from modulator attenuation at the desired unity gain bandwidth. As can be seen from the figure, the bandwidth requirement of OTA is 4-5 times f_{SW}, the switching frequency. Achieving this high bandwidth for voltage controlled DC-DC converter is more demanding and less desirable as it will require an OTA with high bandwidth, resulting in greater power consumption. This wider bandwidth potentially introduces greater noise.

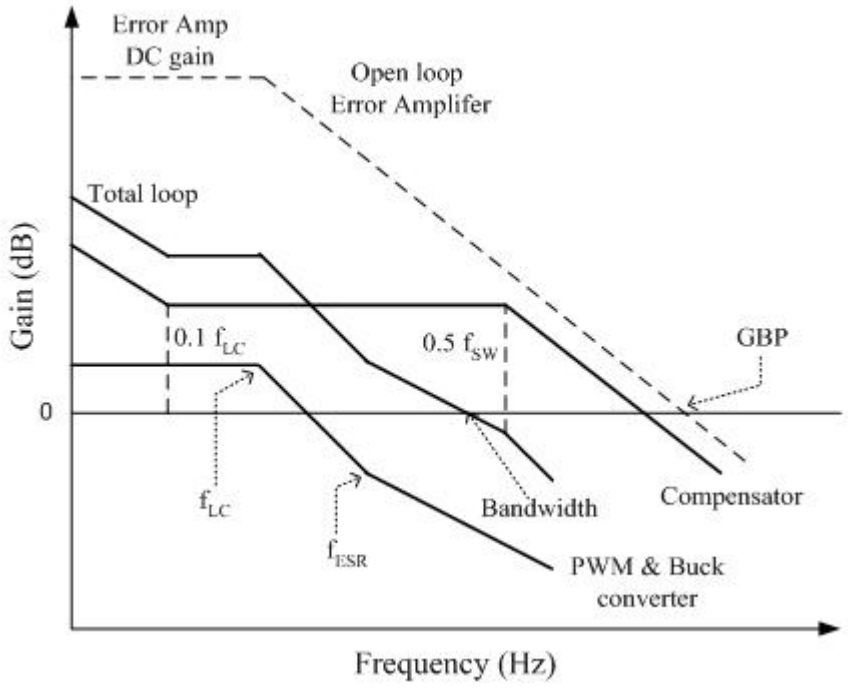

Figure 4.7: feedback loop response type II compensation

4.4 Current mode control

There is strong motivation to use a naturally occurring ramp in power circuit which leads to current mode control [11]. Many different topologies of current mode control are proposed. This scheme requires sensing of inductor current to generate a ramp signal.

4.4.1 Current sensing techniques

Different methods of sensing current and their accuracies, efficiencies and costs are compared in this section. The different locations where current can be sensed are shown in figure 4.8.

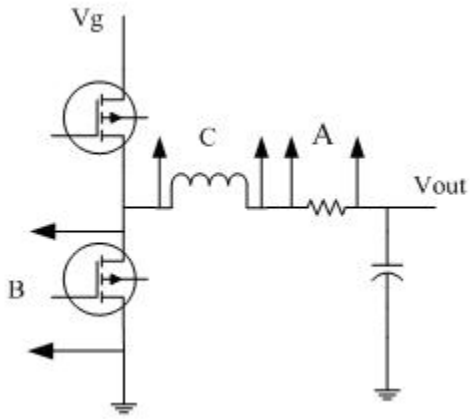

Figure 4.8: Commonly used current sense locations.

Location A is a low value output current sense resistor across which voltage is measured. The accuracy depends on type of resistor and resistor variation with temperature and is taken into account when selecting the resistor value. The power loss is determined by output current and sensing level required of the IC.

Location B is MOSFET sensing as they behave just like a resistor when on. However, sensing must be accomplished during on time otherwise there is a high Vds across MOSFET, which can cause saturation of sensing amplifier. The accuracy depends on the initial value of R_{DSON} and its temperature coefficient of R_{DSON}. This method doesn't introduce any additional power loss unlike sensing at location A.

Location C uses the winding resistance of inductor as the sense resistor. Inductor voltage has a large AC signal component in addition to current information as the inductor left side is switched between Vg and ground. Single pole RC filtering is used to control the introduction of errors. The signal level for IC amplifier estimates the pole frequency. The bandwidth shouldn't be too low as the signal will not be useful for loop control or current limiting. Similar to MOSFET sensing there is no additional power loss.

4.4.2 PWM Modeling

The subharmonic oscillations in current mode control are observed for duty cycle greater than 50% [19]. To circumvent this problem, an artificial sawtooth ramp is added to the control signals. The small signal variation of duty control is derived keeping this sawtooth ramp. Many different variations of duty cycle control have been studied [10], however in this thesis an easy and fast way of analyzing constant frequency current mode control is discussed.

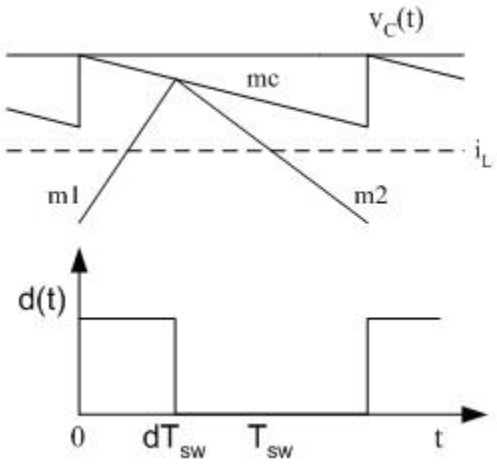

Figure 4.9: PWM modeling of current mode control with slope compensation

$$\begin{aligned} i_L + m1\frac{dT_{SW}}{2} &= v_c - m_c dT_{SW} \\ m1 &= \frac{v_g - v_o}{L} \end{aligned} \tag{4.8}$$

Small signal variation in duty cycle can be derived by substituting ac and dc quantities for m1, d, mc, vc and i_L.

$$\hat{d} = \frac{2(\hat{v}_C - \hat{i}_L)}{nM1T_{sw}} - \frac{D\hat{m}1}{nM1}, n = 1 + \frac{2M_c}{M1} \tag{4.9}$$

This result can be applied to any converter given the slope m1. For a buck converter, the slope m1 during on interval 1 and DC conversion ratio from chapter 3 are given as

$$\begin{aligned} m1 &= \frac{v_g - v_o}{L} \\ V_O &\cong DV_G \end{aligned} \tag{4.10}$$

The small signal duty cycle variation is given as

$$\hat{d} = \frac{2.D(\hat{v}_C - \hat{i}_L)L}{n(1-D)V_O T_{SW}} - \frac{D^2}{n(1-D)V_O}\hat{v}_g + \frac{D^2}{n(1-D)V_O}\hat{v}_O$$

$$\hat{d} = FM\left[(\hat{v}_C - \hat{i}_L) - \frac{DT_{SW}}{2L}\hat{v}_g + \frac{DT_{SW}}{2L}\hat{v}_O\right] \tag{4.11}$$

Substituting the value of $\hat{d}$ in state space equations from chapter 3 and solving for the characteristic polynomial, it can be verified that current control breaks the complex conjugate pole pair of original system into two real poles. The small signal model of current mode control is now as shown in figure 4.10.

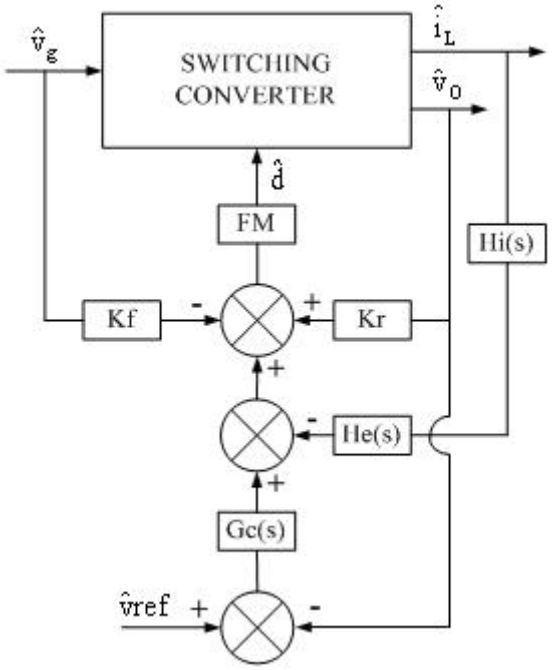

Figure 4.10: Small signal model current mode control

The Hi(s) varies for different current sensing schemes [6]. Also the gain of current sense amplifier is not shown but should be included. He(s) models the sampling action for current mode control [10] and is given by

$$He(s) \cong 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega n^2}, Q_z = \frac{-2}{\pi}, \omega_n = \pi f_{SW} \quad (4.12)$$

The current loop gain ignoring the effect of Kr is approximately given by

$$T_i(s) = H_i(s)He(s)FMG_i(s) \quad (4.13)$$

The block diagram reduction gives the total loop gain as

$$T_c(s) = \frac{G_c(s).FM.G_d(s)}{1 + He(s)H_i(s)G_i(s)FM - K_r FMG_d(s)} \quad (4.14)$$

4.4.2 Compensation current loop

Bode plot of loop gain is observed for optimum slope compensation and the compensation of current loop can be easily designed for sufficient phase margin. It is shown in chapter 5 that compensation for current control is a simple first order network around the error amplifier.

4.5 V^2 mode control

The recent generation processors require extremely high current slew rate and thus power supplies should have a fast transient time. With processor speed in the GHz power demand can more than double in less than a few nanoseconds. The conventional voltage mode and current mode control depends on speed of error amplifier to load variations. The unique feature of V^2 control is its fast transient speed and simple compensation design. The transient speed is maximized by using the output voltage as a ramp signal. In the following section a small signal model of V^2 control is developed.

4.5.1 PWM modeling

Similar to earlier compensation scheme the relation for on time can be easily deduced from figure 4.11 as

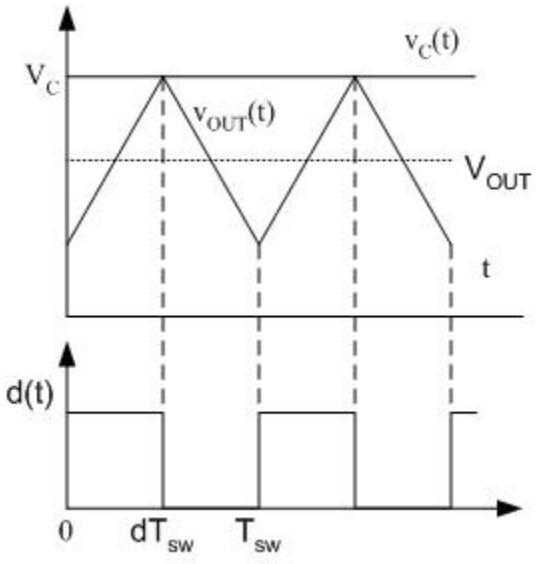

Figure 4.11: PWM modeling V^2 control

$$V_o(t) + m1.\frac{T_{ON}}{2} = V_c(t)$$
$$\therefore T_{ON} = 2.\frac{[V_c(t) - V_o(t)]}{m1} \quad (4.14)$$

Slope m1 at output voltage Vo is due to ESR of output capacitor C, and is given by

$$m1 = \frac{(V_g - V_o).R_c}{L} \quad (4.15)$$

Small signal variation of duty cycle D can be derived as

$$\hat{d} = \frac{2.L(\hat{V}_C - \hat{V}_O)}{(V_g - V_o).R_c.T_{sw}} \quad (4.16)$$

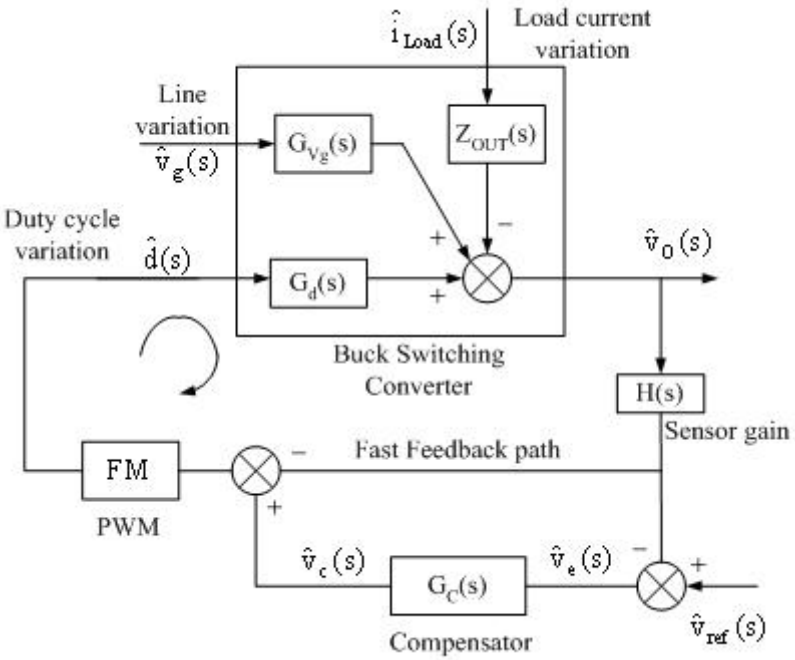

Figure 4.12: Small signal model V^2 control

The expression for FM is estimated from small signal duty cycle relation as

$$FM = \frac{2.L}{(Vg - Vo).R_C.Tsw} \tag{4.17}$$

Total loop gain $T_{v2}(s)$ is derived as

$$T_{v2}(s) = H(s).[1 + G_c(s)].FM.G_d(s) \tag{4.18}$$

4.5.2 Compensation of V^2 loop

As evident from voltage control scheme, compensator requires introduction of a zero at a frequency below the LC double pole frequency. This zero is inherent in V^2 control scheme as a result of fast feedback path and will be explained in detail. This simplifies the compensation network to as shown in figure 4.13. The zero location is set by compensation capacitor Ccomp and the OTA gm to achieve sufficient phase margin.

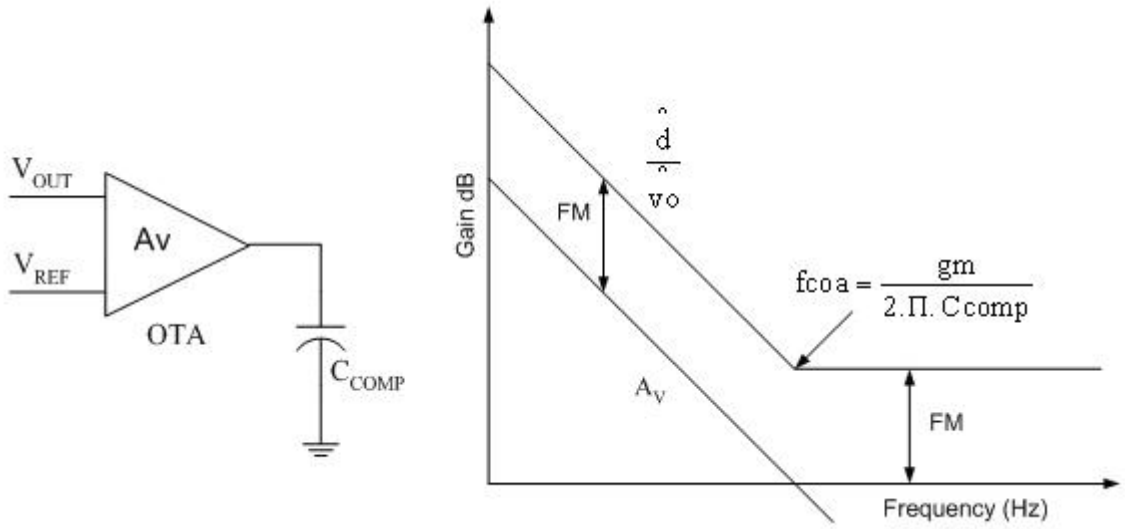

Figure 4.13: V^2 Compensation

$$G_c(s) = A_v = \frac{gm.R_O}{1 + s.R_O C_{COMP}}$$

$$\text{on solving, } [1 + G_c(s)] \cong \frac{gm.R_O\left[1 + s.\frac{C_{COMP}}{gm}\right]}{1 + s.R_O C_{COMP}} \qquad (4.19)$$

There are two feedback paths, slow and fast. The error amplifier cascaded with FM in the slow feedback path provides tremendous gain for DC accuracy. FM is maintained at high frequency to ensure strong feedback for fast transient response.

4.6 Comparison of three control schemes

The following table compares the important features of three types of control schemes.

Features	Voltage mode	Current mode	V^2 mode
Ramp Signal	External ramp	Inductor current	Output voltage
Transient response to line variation	Limited by error amplifier response	Limited by current sense amplifier response	Not limited
Transient response to load variation	Limited by error amplifier response	Limited by error amplifier response	Fast
Compensation	Second or third order required	First order	Single capacitor to ground
Over current protection	Current sensing and circuitry required	Inherent	Current sensing and circuitry required
Over voltage protection	Extra circuitry required	Extra circuitry required	Inherent due to fast transient response
Slope compensation	Not required	Required	Required

Table 4.1: Comparison of control schemes

The use of ramp signal derived from the system itself is attractive for fast transient response. V^2 scheme uses output voltage as ramp signal and has fastest transient response to both line and load variation. Also the compensation for V^2 is simple as compared to voltage and current mode. Overcurrent protection is to be implemented separately in V^2 mode but overvoltage protection is inherent. The hybrid of current control and V^2 control has both type of protection inherent in the system [9]. Slope compensation is required for current mode and V^2 mode to avoid sub-harmonic oscillation. With fast transient response and ease of compensation, V^2 scheme is widely embraced for use in power supplies.

This chapter outlined the three basic control schemes for DC-DC control. The small signal for the loop was derived for all the control schemes and the compensation

design for each of the scheme was illustrated. The performance using each of control schemes is discussed. The next chapter details about the simulink implementation of all control schemes and their performance is compared for variations in line and load.

Chapter 5

Simulink Implementation and Design Example

5.0 Introduction

The complexity of device models and switching nature of switching converters make simulation difficult due to converge in Pspice. Simulink is a windows oriented dynamic modeling package that is an extension to Matlab. The advantage is that models are entered as block diagrams after corresponding mathematical equations are developed for the target system. Matlab uses ordinary differential equation solver (ode45) to solve sets of linear and non-linear differential equations which in this case are emulated by block diagrams. Thus to simulate an electrical system such as DC-DC converter, one has to write equations for various blocks in the system and construct an equivalent block diagram using icons in simulink. The parameters for individual icons can be set for the process. Finally, a choice of equation solver and simulation time is made. The output of system could be observed or recorded into file.

Simulink also provides the feature of writing S-functions which implements the equations of a block. The disadvantage in using s-functions is that no bode plots can be observed if an s-function is in the block diagram.

5.1 Simulink models

5.1.1 Buck converter

Referring back to the equations for buck converter in its two switch positions in chapter 3, a simulink model can readily be constructed as shown in figure 5.1.

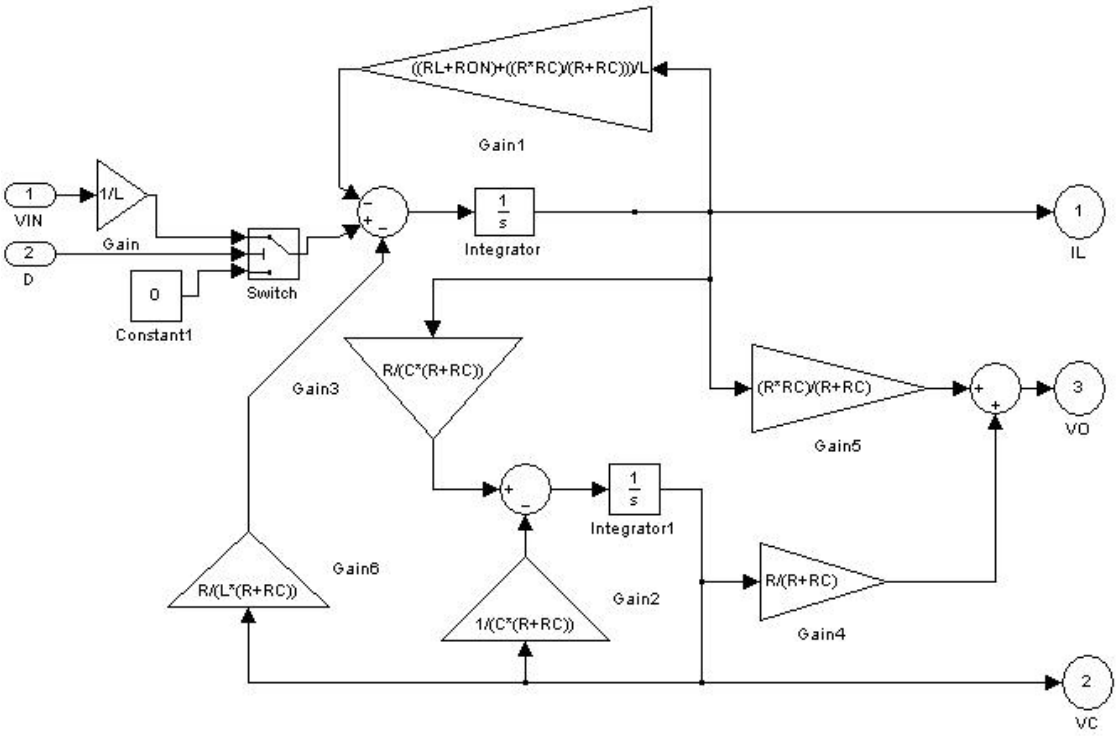

Figure 5.1: Simulink model of buck converter

To facilitate subsequent simulation, and feedback controller design and verification, the inputs to buck converter sub-block are, input voltage Vg and duty ratio d. The outputs are inductor current, capacitor voltage and output voltage. The non-idealities of transistor ON resistance and inductor series resistance are appropriately included. To

validate the correctness of the simulink model, the results from simulink simulations of buck converter were compared to pspice simulations.

5.1.2 OTA

A single pole dominant model of an OTA is shown in figure 5.2. The model has the input parameters as transconductance gm, output conductance go and load capacitance CL. The simplified model estimates gain, bandwidth, and slew rate requirement of OTA.

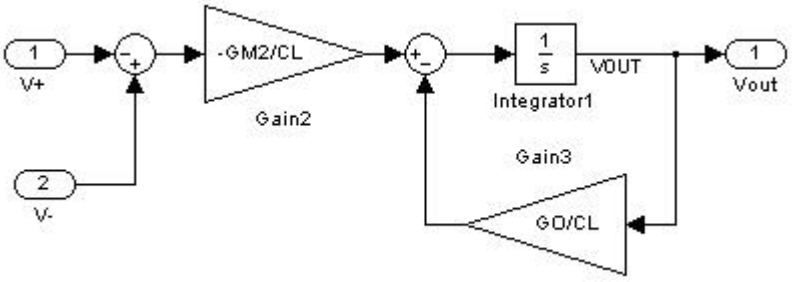

Figure 5.2: Simulink model of OTA

5.1.3 Comparator

A comparator model implemented in simulink is as shown in figure 5.3. The model has the input parameters of open loop gain Avol, offset voltage Vos, Propagation delay Td. The S-function implements the equations that govern the comparator operation.

$$\begin{aligned} a &= VIN - VREF - VOS \\ V_{OH} &= 0.8.Vdd \\ V_{OL} &= 0.2.Vdd \\ b &= \frac{Voh - Vol}{2.Avol} \end{aligned} \tag{5.1}$$

if a>b, output is high and low otherwise.

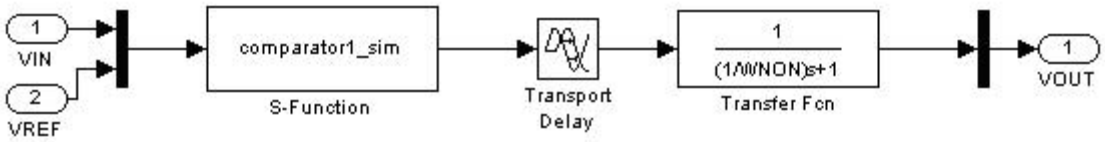

Figure 5.3: Simulink model of comparator

5.2 Design Example

An example using specification from Halliburton Energy Services Inc. is simulated to illustrate the design of a complete dc-dc converter is presented. The specifications are as follows: input voltage range 15-25V, output requirement 1.5V to input voltage, output voltage ripple requirement is <2%, output power equal to 3W and efficiency of 80% over all voltage range. The following design example implements 25 to 5V step down converter.

At 5V, 3W output, the current requirement is 600mA with 20% ripple. Using the design equations from chapter 3, the inductor value L equals 225uH, the ESR requirement is less than 833mΩ and the capacitor requirement is greater than 0.1uF. For this design example ESR is chosen as 100mΩ and C as 300uF. The series resistance of inductor is 100mΩ and Rdson of transistor as 1mΩ. Using the small signal transfer function from duty cycle to output voltage, the open loop bode plot of the buck converter is shown in figure 5.4. The complex pole, the pole due to ESR of capacitor and the peaking due to LC output filter are shown. The Q is approximately 13dB. The cross-over frequency of the targeted system is 1/5 of the switching frequency. The following sections details about the behavior of all three control schemes.

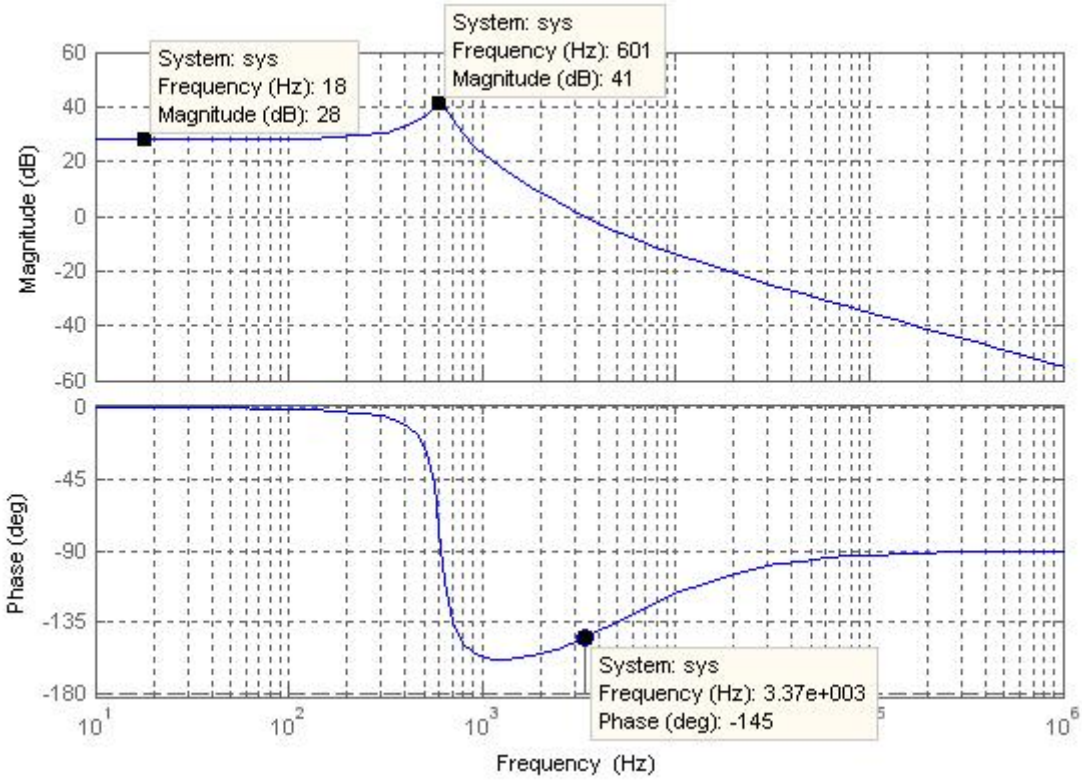

Figure 5.4: Open loop buck converter response

5.2.1 Voltage mode control

Using (4.6), The loop gain, $T_v(s)$ without compensator is observed and the compensator is designed [8]. The magnitude V_M of reference triangular wave is 3V. The sensor gain H(s) is 1 assuming a Vref of 5V is available.

The values for compensation network are calculated as R1 = 5kΩ, R2 = 254kΩ, C1 = 6pF, C2 = 10.23nF. The open loop frequency response with compensation is shown in figure 5.5.

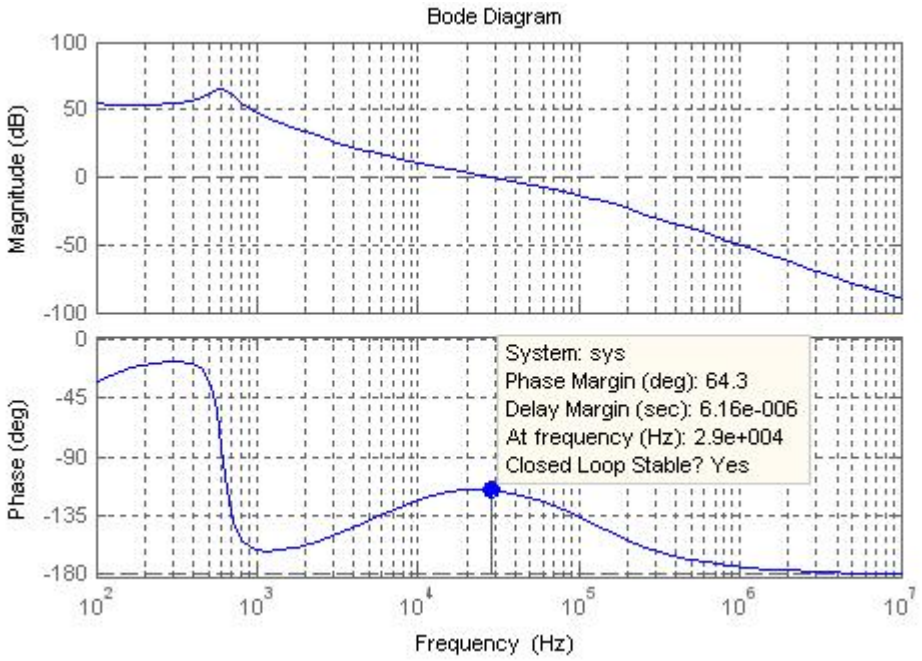

Figure 5.5: Open loop voltage mode compensated transfer function

5.2.2 Current mode control

The approximate current loop gain Ti(s) for different value of slopes of compensating ramp and Hi = 1 is shown in figure 5.6. It can be observed that without any compensating ramp i.e. n=1, the gain and phase margin are not good for a stable closed loop. These results closely match with results in [10]. Also the phase is -180 degrees at half the switching frequency which is in accordance with nyquist sampling theory and verifies the accuracy of model only up to half the switching frequency. The n = 3 - 5 gives sufficient phase margin for stable loop. The control to output transfer function, $T_C(s)$ from (4.14) is shown in figure 5.7. The peaking at half the switching frequency shows the existence of complex poles and also the cause of instability. As more external ramp is added, the complex poles break into real poles. The one pole merges with low frequency pole to give LC double pole and other moves beyond switching frequency.

This means that as more external ramp is added, the current mode control behaves just like voltage mode control.

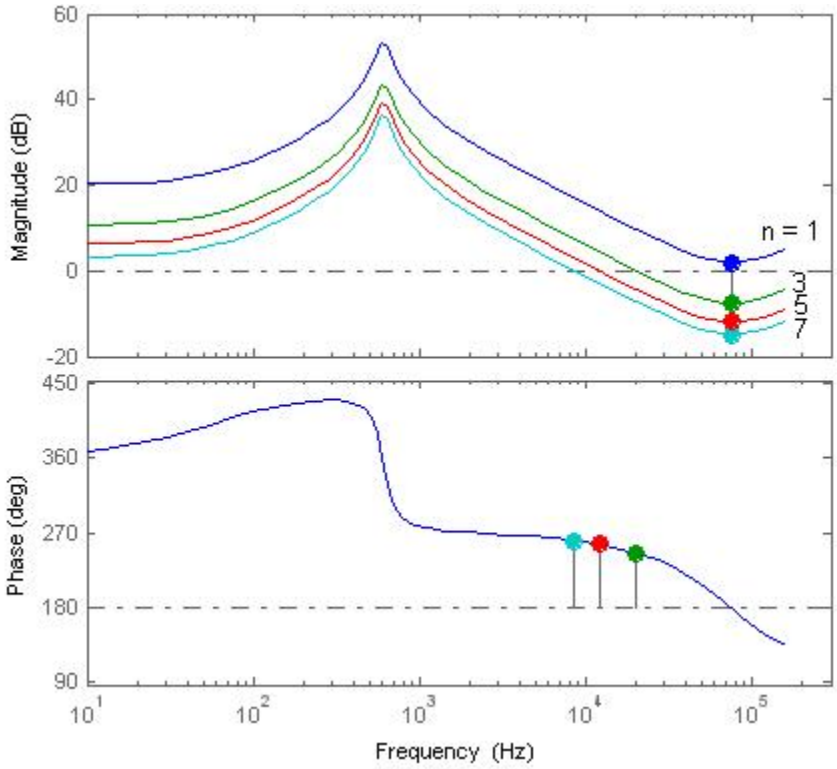

Figure 5.6: Current loop bode plot – current mode control

As can be seen from the control to output loop gain from figure 5.7, the crossover frequency of the required system is not what is desired. To achieve the required crossover frequency of 30 kHz for n = 3, the compensation network is designed around an error amplifier. Required error amplifier gain at the cross-over frequency is approximately 22dB. ESR zero, f_{ESR}, is cancelled by pole, f_P, of error amplifier at $f_{ESR}/10$ where f_{ESR} is 5.3 kHz. This increases low frequency gain and adds 45 degrees phase lag, still leaving 45 degrees of phase margin. Therefore, error amplifier gain required below f_P is

$$22 + 20\log\left(\frac{30000}{530}\right) = 57\text{dB}$$

The value of R_f is chosen 1 MΩ, high enough such that gm.R_f > 57dB. Therefore Ri = 1.4kΩ and solving $fp = \frac{1}{2\pi R_f C_f}$ gives C_f = 300pF.

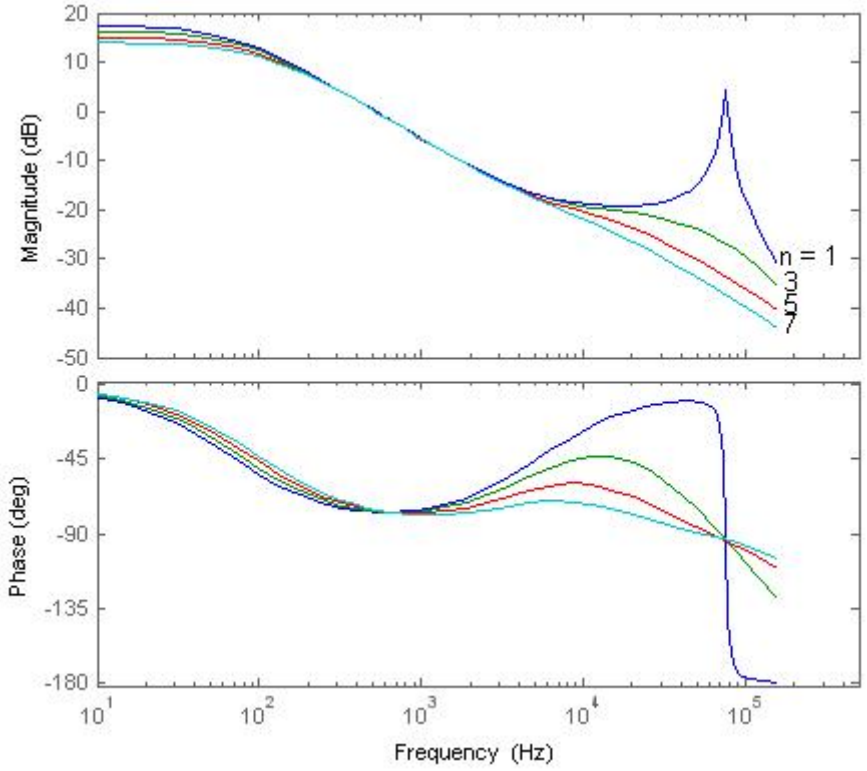

Figure 5.7: Control to output bode plot - current mode control

The control to output transfer function with compensation and compensator is shown in figure 5.8. The required crossover frequency is achieved but system has little phase margin. The location of compensator pole should be changed to achieve appropriate phase margin. There is a trade off in achieving DC gain and sufficient phase margin.

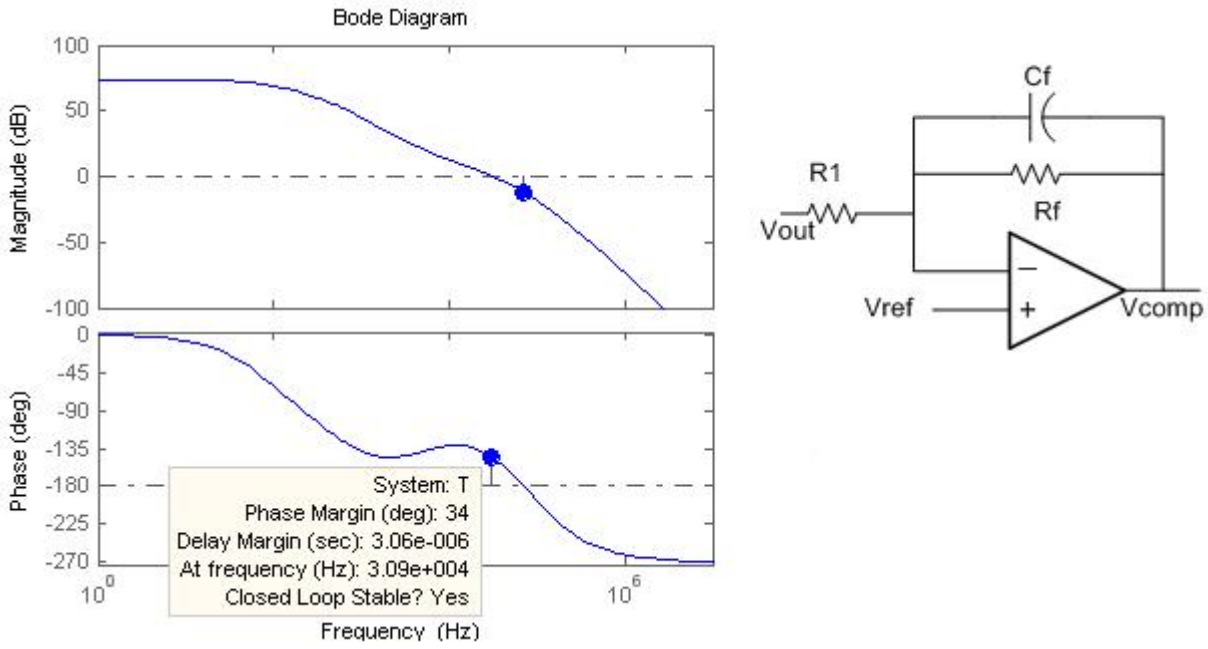

Figure 5.8: Compensated control to output loop and compensator

5.2.3 V^2 control

Using (4.19), the loop gain equation for V2 control, $T_{v2}(s)$ is examined and the compensator is an error amplifier with a capacitor of 5.2uF at its output to ground. The transconductance gm is 5mS, and output impedance of 5 MΩ. The compensated open loop frequency response is shown in figure 5.9.

5.3 Transient response

Voltage and V^2 control mode paradigms were designed and compensated for identical load, load regulations, and output voltage conditions and simulated. The line voltage was varied from minus 40% to plus 50% (25V to 15V and 15V to 30V) and the load was then varied from plus 200% to minus 300% (8.33Ω to 4Ω and 4Ω to 12Ω). The settling behavior is observed to determine the best control paradigm for transient

response or recovery. This considers response duration, and current and voltage spiking. Current mode control transient response to input line and load variation is limited by the current sense and the error amplifier respectively. See Table 4.1. It may be feasible for current mode control to respond as fast as V^2. However, this comes at a price. Two modestly complex wide band amplifiers are required while V^2 requires a single simple low bandwidth OTA. In general, however V^2 response to line and load variations is only limited by the comparator bandwidth.

5.3.1 V^2 controlled

The compensation so designed is incorporated in simulink block diagram to test the validity of stable operation, transient response to load and line variation and other design specifications.

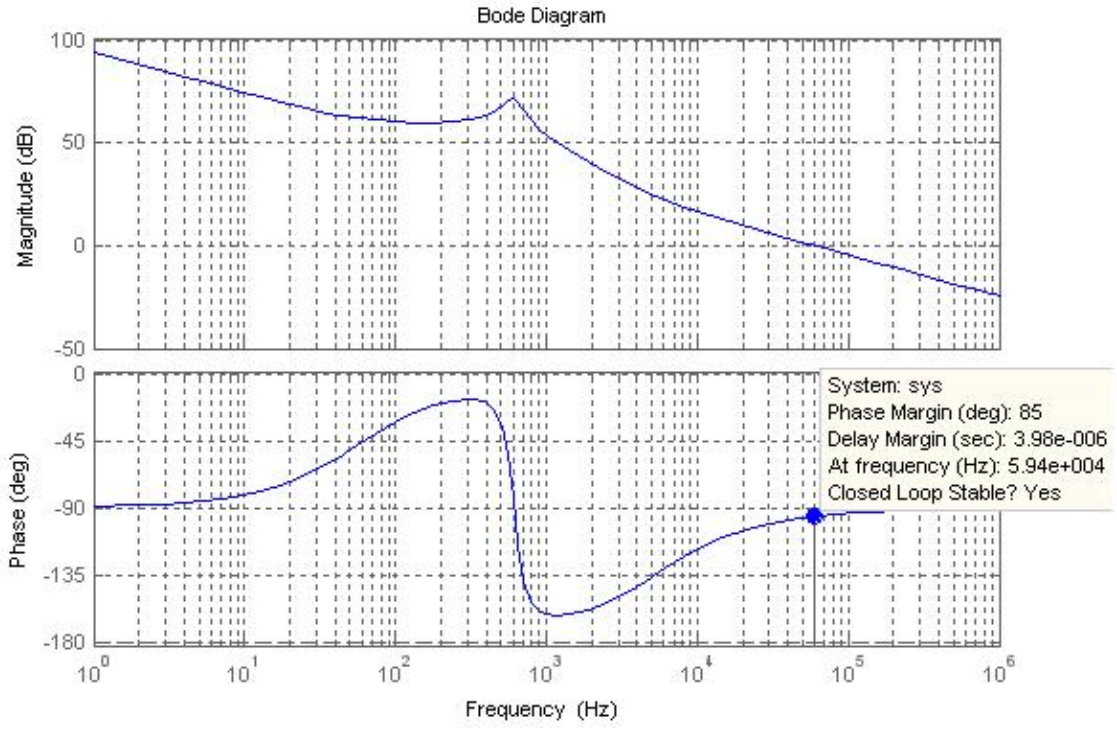

Figure 5.9: Open loop V^2 mode compensated transfer function

The simulink block diagram with compensator implementation is shown in appendix B.

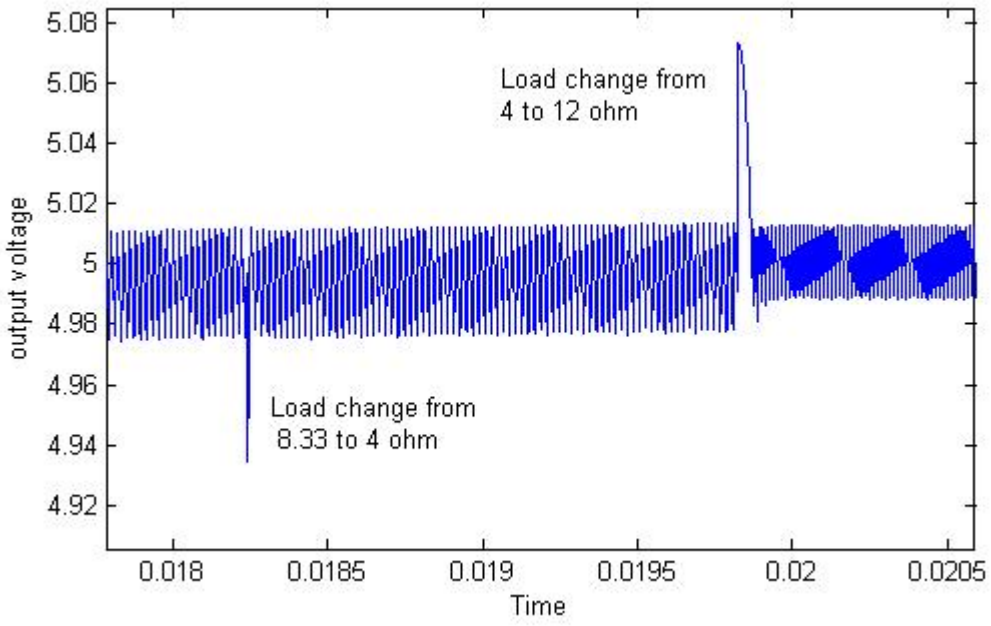

Figure 5.10: V^2 response to load variations

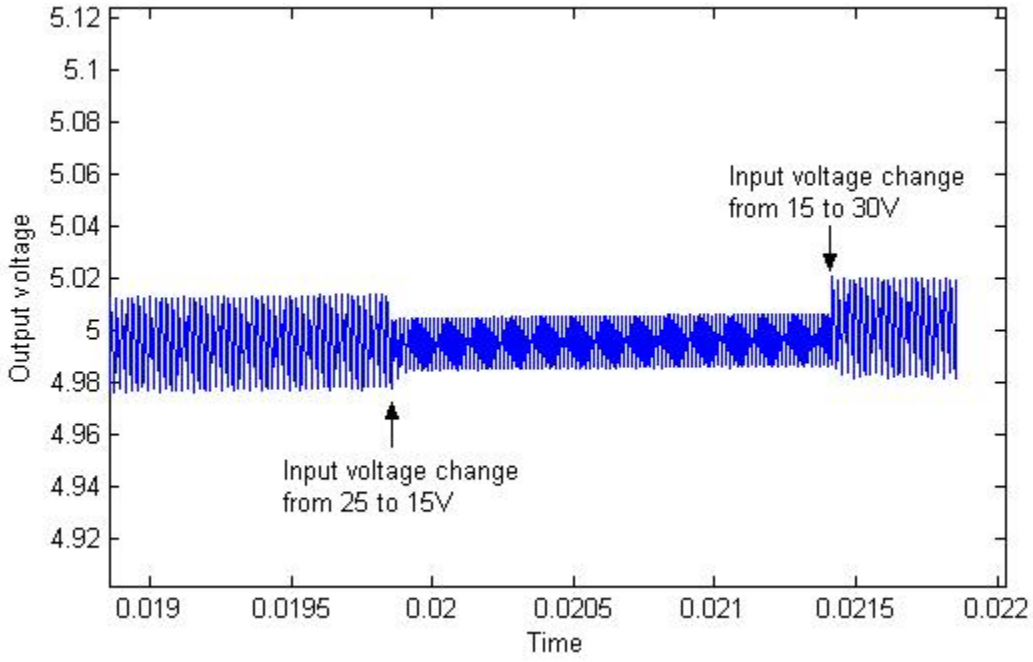

Figure 5.11: V^2 response to line variations

Figure 5.10 shows the V^2 response to load variations. The graph shows the transient response to harsh load variations is less than 1ns. The overshoot is less than 5% and output voltage ripple is maintained less than 2%. From figure 5.11, it is confirmed that V^2 has fast response to line variations. The error amplifier bandwidth requirement is only 250 kHz to achieve fast transient response.

5.3.2 Voltage controlled

Figure 5.12 shows the Voltage mode response to load variations. The graph shows the transient response to harsh load variations is less than 0.1us. The overshoot is less than 5% and output voltage ripple is maintained less than 2%. Figure 5.13 shows Voltage mode response to line variations. The error amplifier gain bandwidth requirement to achieve this transient response is greater than 2.9 MHz.

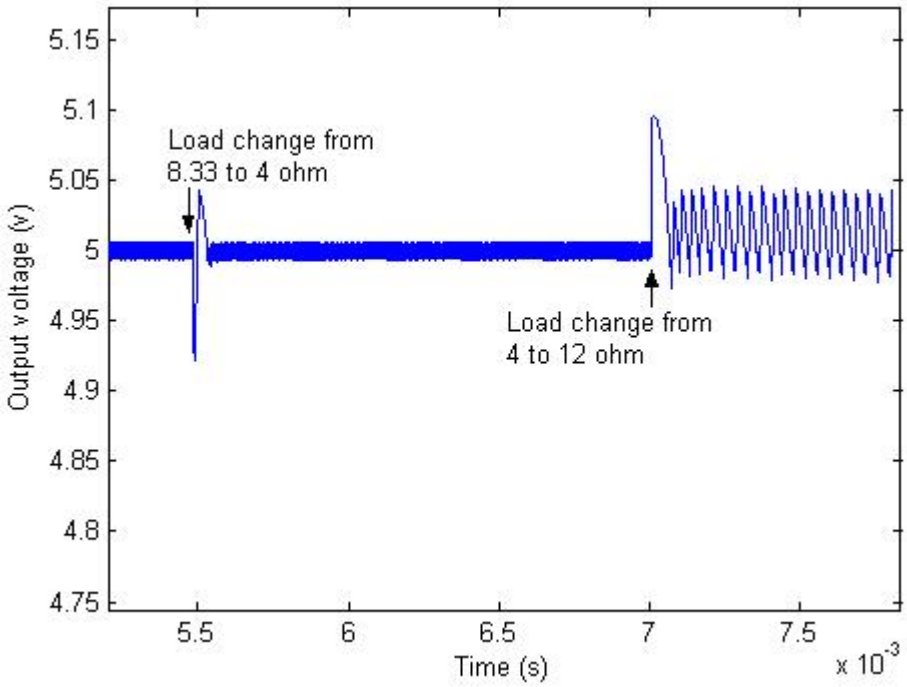

Figure 5.12: Voltage mode response to load variations

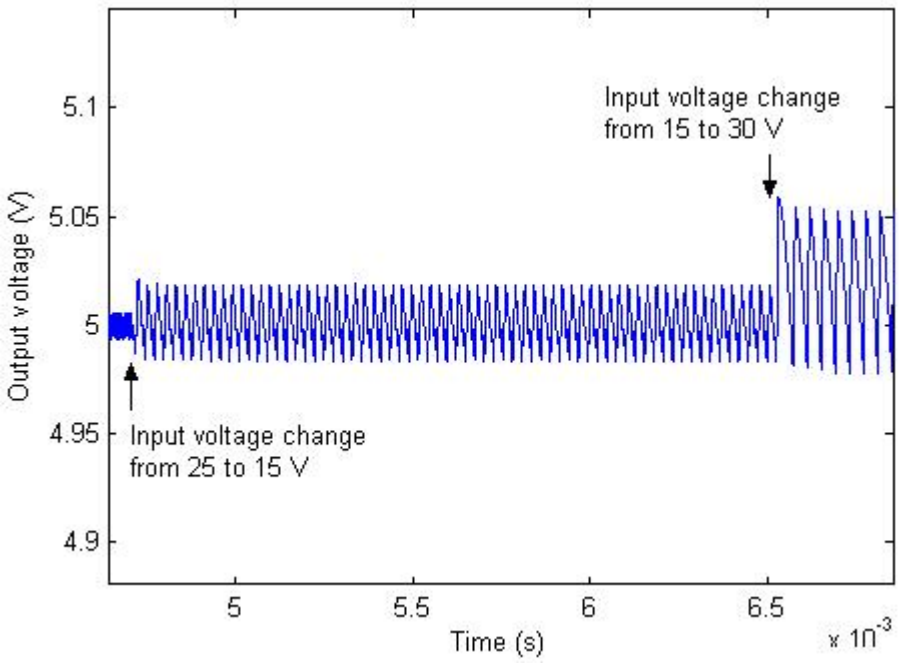

Figure 5.13: Voltage mode response to line variations

5.3.3 Current controlled

From the simulation of voltage mode and V^2 control, it is inferred that line variation for the current mode control is limited by the response of current sense amplifier which is not the case with V^2 scheme. See table 4.1. Load variation is limited by error amplifier response as load variations are first sensed by error amplifier and than applied to PWM comparator. It may be feasible for current mode control to respond as fast as V^2. However, this comes at the expense of two modestly complex and power consuming wide band amplifier while V^2 requires a single low bandwidth OTA.

5.4 Conclusions

This chapter discusses the design example and simulink implementation of dc-dc converters using models for sub-blocks in the converter system. The model successfully simulates the V^2 and voltage mode control scheme and verifies the validity of the model. The graphical method to determine the loop transfer function discussed in chapter 4 and the compensation design performed exceptionally as demonstrated by excellent results. It is observed for voltage mode control that the bandwidth requirement of error amplifier can be severe when demanding fast transient response. This applied equally well to current mode control and its error amplifier. The V^2 control scheme shows a faster transient response with a significantly lower bandwidth requirement for the error amplifier and thus validates its figure of merits as in table 4.1. From the simulation results of voltage and V^2 control, it is inferred that line and load variations in current mode are limited by current sense and error amplifier respectively. As previously noted current mode control can be designed to respond fast and potentially as fast as V^2. However, this requires two modestly complex wide band power consuming amplifiers while V^2 requires a simple low bandwidth OTA. Additionally voltage over sensing is inherent in V^2 (as current sensing in current mode control) but, the addition of over current protection in V^2 control requires a simple low fidelity low bandwidth OTA. In conclusion V^2 is the preferred SMPS control paradigm, providing equal or better performance than both current and voltage control modes with reduced complexity and lower overall power consumption. V^2 is therefore; faster, lower power, more robust and in the end more efficient.

Chapter 6

Gate drive circuitry

6.0 Introduction

The drive circuit is required to control the switching of the power MOSFET. During turn on both drain and source are maintained at a high input voltage and to keep the transistor on, the gate voltage should be greater than input or source voltage. This essentially means that drive circuitry is also at high potential, which can cause damage to a low voltage PWM IC. To circumvent the problem, a pulse transformer is used to isolate the logic circuitry from power MOSFET operating at high voltages. Another advantage of pulse transformers is that it maintains constant Vgs during turn on and has the capability to either step up or step down.

Pulse transformer based gate drive circuits can deliver only AC signals as the flux core must reset every half cycle. The Inductor Volt second principle reviewed in chapter 2 results in large voltage swings if a narrow reset pulse, i.e., a large duty cycle is required.

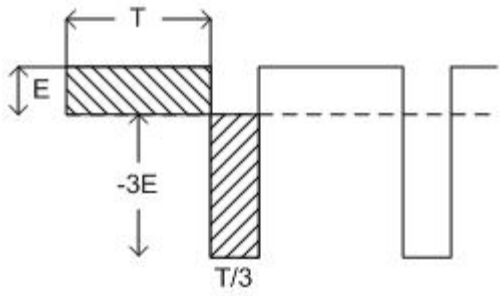

Figure 6.1: Volt-Seconds characteristics of Transformers

Or restated this means that area under the curve during positive and negative segments of a full cycle must be equal as shown in figure 6.1. This limits the use of pulse transformers to 50% duty cycle as the large voltage swings may be higher than voltage rating of the semiconductor switches and logic devices.

6.1 Gate drive basic operation

The selected pulse transformer based gate drive circuit is as shown in figure 6.2 where Diode D1 represents the internal source to drain diode of transistor M2. The purpose of this circuit is to provide enough Vgs to turn on M1 irrespective of voltage levels at source of M1.

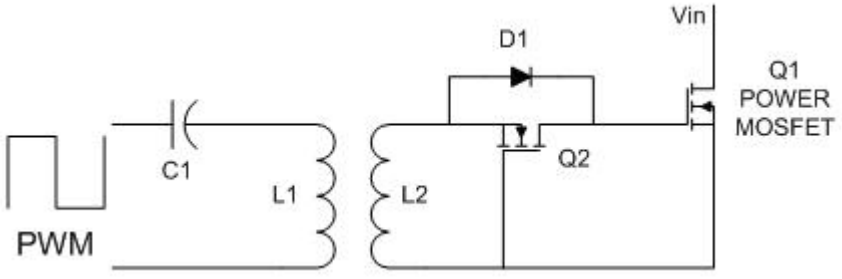

Figure 6.2: Gate drive using pulse transformer

The duty cycle output from the PWM circuit is to be switched by power mosfet M1. During the positive cycle, transformer supports the pulse by changing flux until it saturates. During this period, diode D1 conducts and the Cgs of M1 is charged with a positive gate to source voltage. When the transformer saturates, the diode D1 isolates the collapse of voltage at winding L2 from gate of M1 and input capacitance Ciss of M1 holds the gate bias for the time limited by the drain to source leakage current of M1.

When the PWM output goes negative, the transistor M2 is fully turned on as its source goes negative discharging input capacitance Ciss of M1 through M2. When the transformer saturates during this cycle, the gate to source of M1 has discharged and remains at zero bias.

6.2 Design considerations

The self inductances of primary and secondary coil are related to number of turns N, area of coil A, and length of coil L by

$$L = \mu N^2 A/L \tag{6.1}$$

The transformer primary and secondary current are related to number of turns as

$$\frac{V1}{V2} = \frac{I2}{I1} = \frac{N1}{N2} = \sqrt{\frac{L1}{L2}} \tag{6.2}$$

Power mosfet Si9945AEY is used as an example for designing the gate drive circuitry of figure 6.2. From chapter 5, the drain current through M1 when on is 600mA. From datasheet the required Vgs for this current is approximately 3V. Also the source to drain

forward voltage drop of the lower MOSFET is 1.2V. Thus to get Vgs of 3V on MOSFET M1, the voltage on secondary of transformer needs to be around 4.5V. Primary side of the transformer L1 is driven by the PWM IC with a peak voltage of 3.3V and hence a step-up transformer is used to achieve required Vgs. Therefore,

$$\frac{N1}{N2} = \frac{4.5}{3.3} = 1.36 \tag{6.3}$$

A second requirement that also needs to be met is the sufficient current required to charge the input capacitor Ciss of power MOSFET. The time to charge the gate capacitance is 20-100 times smaller the on time of input PWM. The capacitor equation gives the secondary current as

$$Ipeak = 1.5C\frac{\Delta V}{\Delta t} \tag{6.4}$$

The Ciss = 600pF, $\Delta V = 3V$ and $\Delta t = 1.332us/10 = 100ns$ gives Ipeak = 27mA. Thus the primary current is $\frac{N1}{N2}$ times 27mA which is equal to 36mA. Thus the PWM should have the current sourcing capability greater than 36mA.

The value of inductance on the primary side is determined on the basis of time constant of primary side circuit and this needs to be less than 1/10 time the on time of PWM output. The series winding resistance plus output impedance of PWM IC and transformer primary winding make a series LR circuit. Therefore, the steady state current assuming a 50ohm driver, flowing in the circuit is given by

$$I = \frac{V}{R} = \frac{3.3}{50} = 66mA \tag{6.5}$$

The time dependent current equation on the primary side of transformer is given by

$$i(t) = I\left(1 - e^{-t/\tau}\right) \tag{6.6}$$

Solving for i(t) = 36mA at t = 1.332us/10 yields $\tau = 0.168e-6$. From which the value of inductance is calculated as less than 8.5uH.

A Prototype of the gate drive circuitry was implemented on a printed circuit board. The waveforms and voltage levels at different location in the circuit are shown in Appendix A. The number of turns calculated in the above discussion ignored any core and winding losses. Thus to get appropriate Vgs on power MOSFET, the Ratio of number of turns was increased to 1.8. The input capacitance Ciss of power mosfet is derated by 50%. The results after simulation of the gate drive circuitry are discussed in Appendix A.

Chapter 7

Conclusion and future work

7.0 Conclusion

DC-DC converters and their design remain an interesting topic and new control schemes to achieve better regulation and fast transient response are continually developed. Step down switching regulators are the backbone of electronic equipments that employ IC's running at supply voltages lower than 5V. A key challenge to design switching regulators is to maintain almost constant output voltage within acceptable regulation.

Pspice is the industry standard for design and simulation of electronic circuits. But the problem of convergence and time for simulation makes it inconvenient for complex systems such as a DC-DC converter to be simulated. In this thesis, Matlab simulink is preferred over Pspice for its enhanced equation solver. The block diagram of the converter system in Matlab simulates the functionality of the system while providing specification for each individual block to facilitate IC implementation.

Traditional method of arriving at small signal model is complex. In this thesis, a simple graphical method to develop the small signal system model for three most predominant control schemes is discussed. The small signal model so developed is then used to develop the loop equation without compensator. The stability is then examined via the bode plot of loop gain and the compensator is designed to make the SMPS stable in closed loop. The results from graphical method closely match with the traditional method. The converter system so designed is simulated under different load condition

In particular, the state of the art V^2 control scheme is analyzed in detail. IC versions of the scheme are implemented but not much analysis has been documented on its small signal model and compensation on its relative figure of merit versus other control schemes. The graphical method is applied to this scheme and the compensation is designed. The full system model is implemented with compensation and transient response is observed under different load conditions. It is concluded that V^2 has fast transient response and easy compensation that doesn't require demanding performance from the OTA.

7.1 Future work

Protection circuits are integral part of the converter system to protect the load from application of high voltage in case of failure in converter. Over-voltage and over-current protection could be added to existing block diagram. Soft-start is necessary to

avoid inrush of current at start up and could be appropriately modeled. An easy way to implement soft-start is by using a RC network following the reference voltage.

The discussed modeling technique can be extended to enhanced V^2 control scheme and to verify the improvement in transient response and avoid the use of external over voltage and over current protection scheme.

Appendix A - Gate Drive Circuitry

A.1 Introduction

The chapter 6 of this thesis details about the analysis of gate drive circuitry to switch the power mosfet of buck converter. To verify the analysis, a bench prototype of the gate drive circuit and buck converter as shown in figure A.1 was built.

Figure A.1: Bench prototype of gate drive circuitry

Step up transformer was hand built on ferrite cores and the values were measured using HP impedance analyzer. The circuit is 15-3V step-down converter and a output voltage ripple of less than 2% is desired. Agilent function generator inputs a 20% duty cycle rectangular wave to transformer and 15V is applied from power supply to drain of power mosfet. The waveforms tapped at various points are shown in next section.

A.2 Simulation results

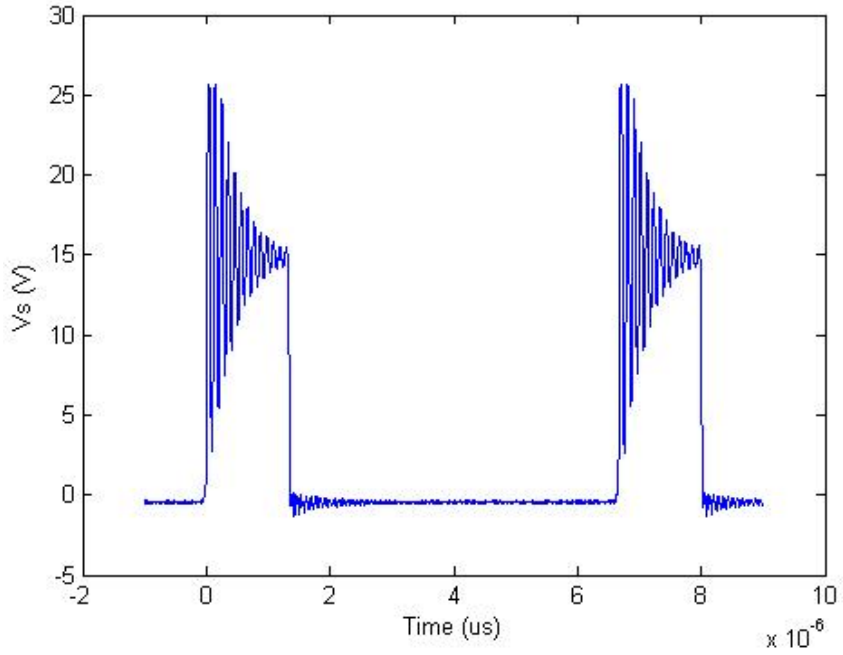

Figure A.2: Switched input voltage waveform at source of power mosfet

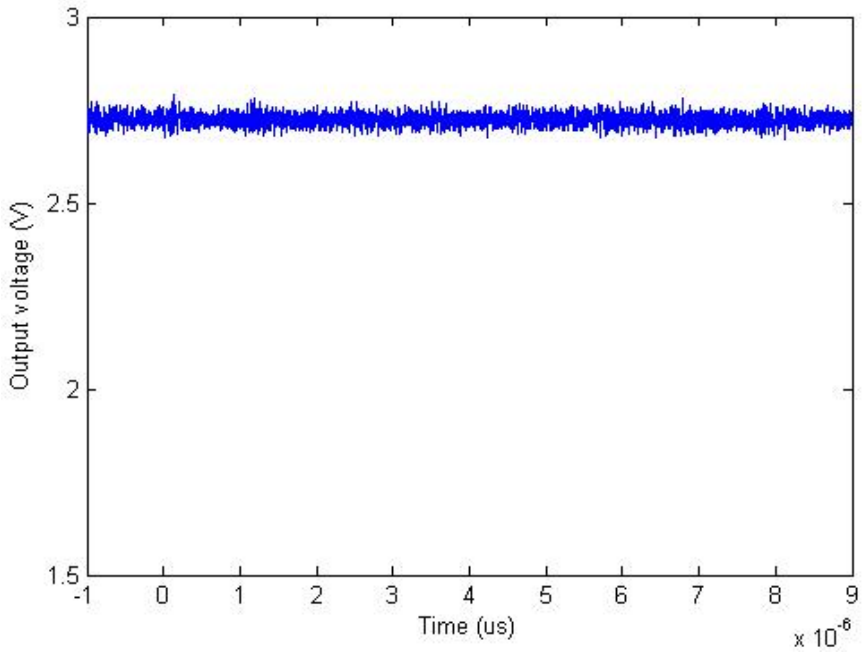

Figure A.3: Output voltage waveform

Lots of Ringing is observed in switched input voltage waveform. The reasons of ringing are stray inductances and coupling from other noisy sources. The output voltage is held at 2.75 volts instead of 3. The reasons are the losses due to inductor series resistance, transistor on voltage and other parasitics in the circuit.

Appendix B – Simulink models

B.1 Small signal model

The discussion in chapter 3, 4 and 5 shows the importance of small signal models for different control schemes. The following section shows the simulink block diagram or Matlab code for generating loop transfer functions as discussed in chapter 4. The bode plots for a block diagram that uses only simulink inbuilt blocks can be observed with following commands.

```
[W X Y Z] = linmod('buck_fullsmallsignal');
sys = ss(W,X,Y,Z);
bode(sys,{10,10e9});
```

The model file name is entered in single quotes. The linmod function linearizes the block diagram and returns the four state space matrices. These matrices can then be used to generate a state-space system for which bode plot can be plotted. The parametric values for blocks are entered at Matlab command prompt.

B.1.1 Voltage mode control

The loop gain transfer function derived in chapter 4 is implemented using simulink block diagrams as shown in figure B.1. The bode plots are obtained after Linearizing the block diagram.

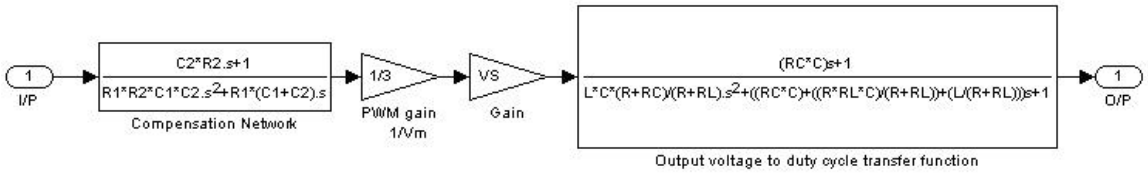

Figure B.1: Voltage mode small signal block diagram

B.1.2 V^2 mode control

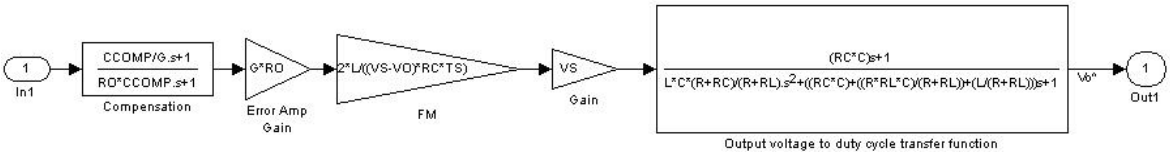

Figure B.2: V^2 control small signal block diagram

B.1.3 Current mode control

The bode plot of loop transfer functions for current mode control are observed using Matlab code as follows.

```
clear;
C=300e-6;
L=225e-6;
RL=7e-3;
RC=100e-3;
R=8.33;
TS=6.66e-6;
FS=150e3;
VS=25;
VO=5;
D=0.2;
RON=1e-3;

% setting s as Laplace variable
s=tf('s');
n=5; % n = 1 + (2*m)

% Setting various parameter related to current mode control
FM = 2*L*D/(n*(1-D)*VO*TS);
```

```
kf=D*TS/(2*L);
kr=D*TS/(2*L);
wn=pi*FS;
Qz=-2/pi;
Hi=1;
He=1+(s/(wn*Qz))+((s*s)/(wn*wn));
Gd= (VO/D)*(1+s*C*RC)/(1+(s*((L/R)+(C*RC)))+(s*s*(L*C*((R+RC)/R))));
Gi= (VS/R)*(1+s*C*(R+RC))/(1+(s*((L/R)+(C*RC)))+(s*s*(L*C*(R+RC)/R)));

% Inner current loop transfer function
Ti = Hi*He*FM*Gi;
bode(Ti,{1e1,1e6});

% Total loop gain transfer function
T = FM*Gd/(1+ (Hi*He*FM*Gi) -(Gd*FM*kr));
bode(T,{1e1,1e6});

% Compensation design for n =5
R1 = 1.4e3;
Cf = 300e-12;
Rf = 1e6;

% compensated loop gain transfer function
T = FM*Gd*(Rf/R1)/((1+s*Rf*Cf)*(1+ (Hi*He*FM*Gi) -(Gd*FM*kr)));
bode(T,{1,1e9});
hold
```

B.2 Simulink OTA block

The block diagram for OTA from chapter 5 is derived from the circuit as shown in figure B.3.

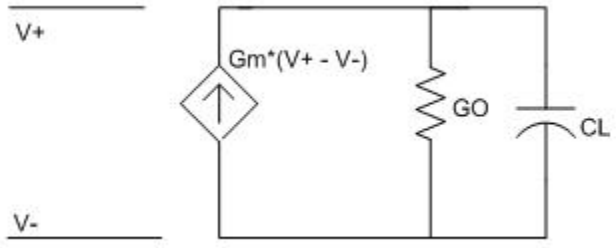

Figure B.3: Simplified OTA circuit

The simulink model of OTA with feedback and example feedback network is as shown in figure B.4. The feedback network is implemented using Simulink power systems blockset.

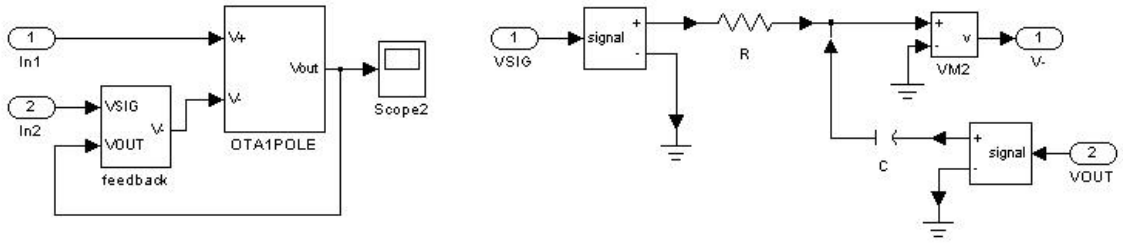

Figure B.4: OTA with feedback and feedback sub-block

B.3 Voltage mode model

The full simulink model of voltage mode control is as shown in figure B.5.

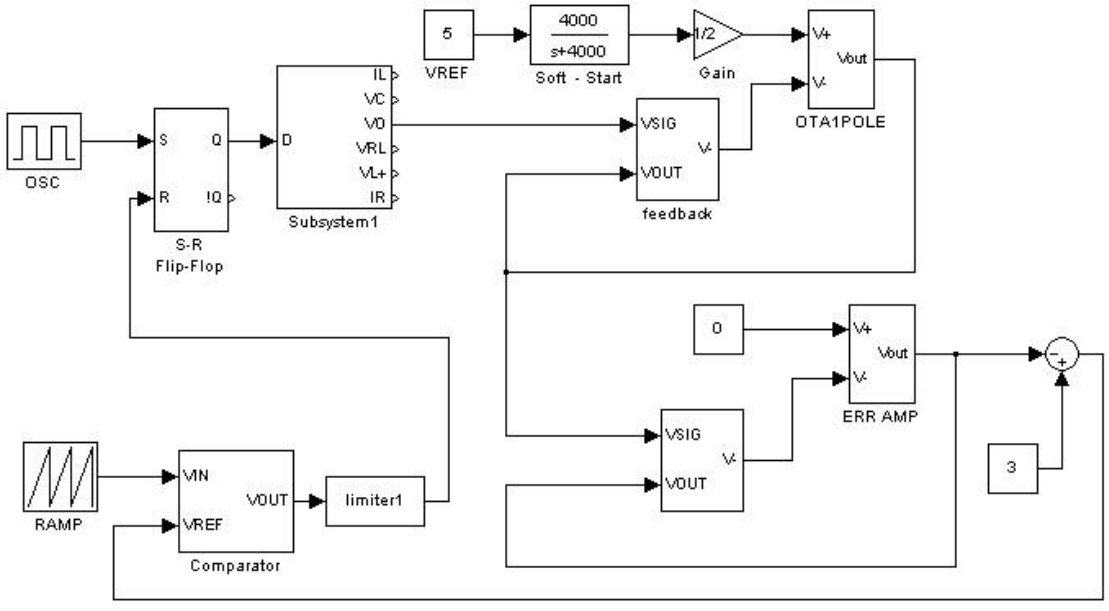

Figure B.5: Full simulink model of voltage mode control

B.4 V^2 mode model

The full simulink model of V^2 mode control is as shown in figure B.6.

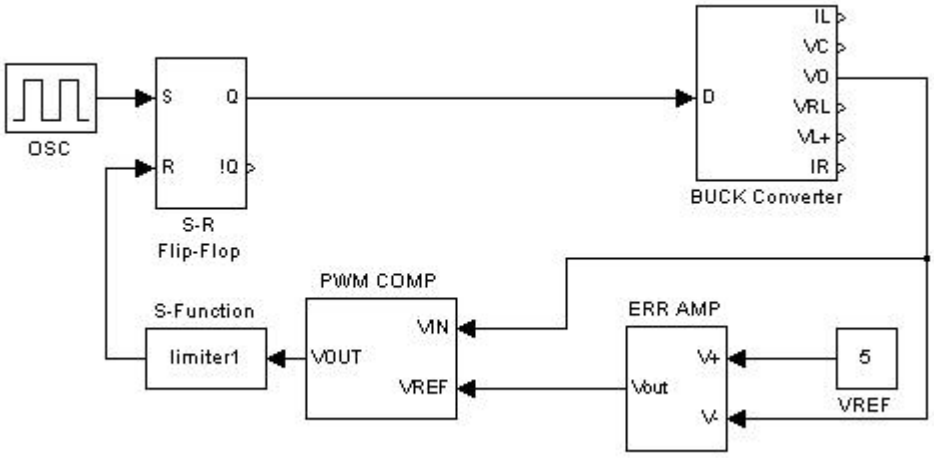

Figure B.6: Full simulink model of V^2 mode control

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