MAJOR CONCERNS IN CLOCK RECOVERY OF MANCHESTER ENCODED DATA USING A PHASE LOCK LOOP

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Dedication

To my family…

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In the course of this thesis I have a learnt a lot about myself and have had the opportunity to expand my technical knowledge beyond books. This experience will always be etched in my memory.

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GLOSSARY

ΔV	Overdrive voltage of a transistor
C_{GS}	Gate to Source capacitance
C_{GD}	Gate to Drain capacitance
C_{LF}	Loop Filter Capacitor
CP	Charge Pump
Din	Input Data
Dout	Retimed Data Out
DW	Refers to the charge pump switch which causes a decrease in the VCO frequency or refers to the current when the switch is on.
g_m	Transconductance
I_P	Charge Pump current
I_D	Drain Current
I_S	Source Current
K_{VCO}	Sensitivity of the VCO in Hz/V
LPF	Low Pass Filter
PFD	Phase Frequency Detector
R_{LF}	Loop Filter Resistor
RCLK	Reference Clock

UP Refers to the charge pump switch which causes an increase in the VCO frequency or refers to the current when the switch is on.

V_B Bias voltage

V_{DS} Drain to source voltage across a transistor

V_T Threshold voltage of a transistor

VCLK Clock of the Voltage Controlled Oscillator

VCO Voltage Controlled Oscillator

Chapter 1

Clock Recovery Circuits

1.1 Introduction

Signals in communication systems pick up noise and delays while traversing their respective mediums. Also, the data is asynchronous when we take into consideration that the receiver and the transmitter are signal wise independent with the exception of the communication link path(s). In other words, since the clocks used in the receiver and transmitter have different phase relationships, the data transmitted by the transmitter becomes asynchronous with respect to the receiver. Therefore, for effective communication between two Rx-Tx units there must be a mechanism for recovering the original signal from the asynchronous, noisy distorted signal. Clock recovery circuits perform such an operation – which is retiming and "cleaning" or reconstruct the signal.

In brief, as depicted in Figure 1.1, we can summarize the primary functions of a clock recovery system as:

1. Recovery of clock.
2. Retiming of data.

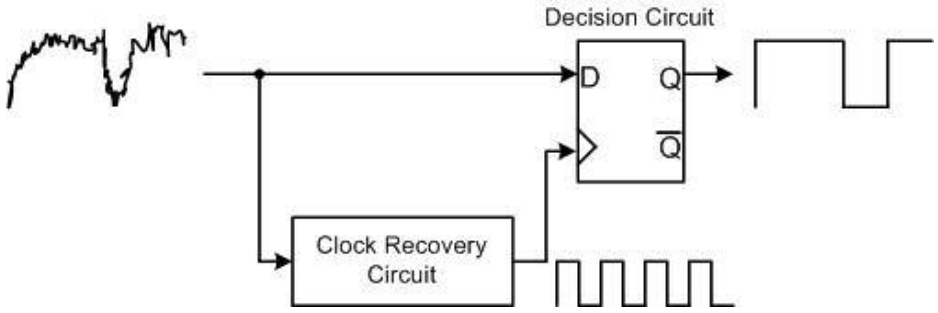


Figure 1.1 Primary function of a clock recovery system

1.2 Clock Recovery Mechanisms

1.2.1 Oversampling Technique

The Oversampling Technique decouples the clock generator from the sampling or tracking of data. Data is over-sampled and the phase alignment is performed digitally. Figure 1.2 shows the block diagram for this technique.

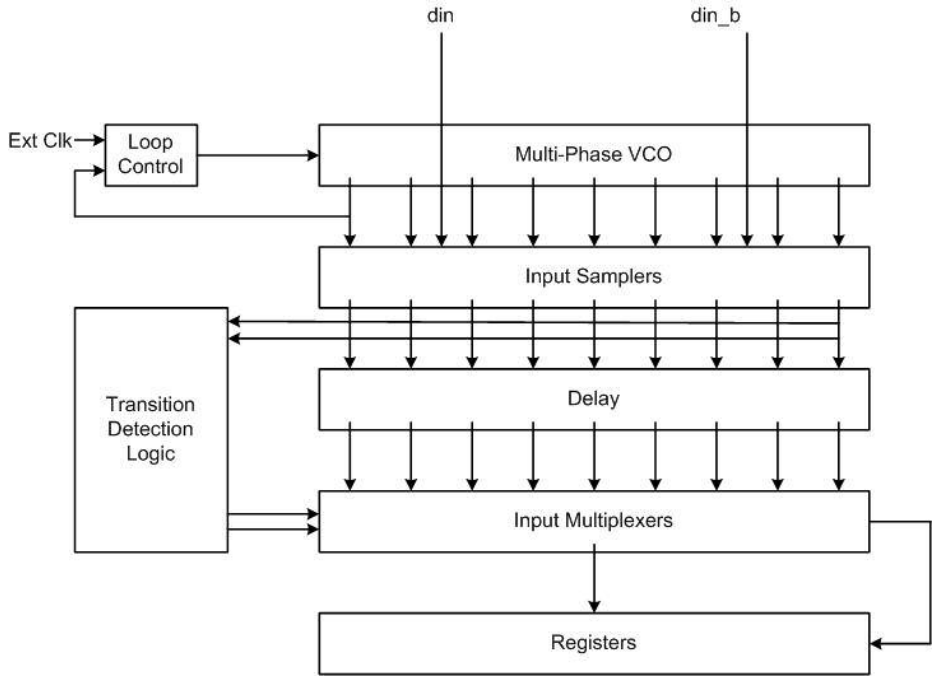


Figure 1.2 Oversampling Technique for Clock Recovery

The loop control consists of a PLL which tries to lock on to the “ext_clk” signal. The Voltage Controlled Oscillator generates the clocks which are used to oversample. Multiple phase clocks can be generated by tapping the different stages of the VCO as shown in Figure 1.3.

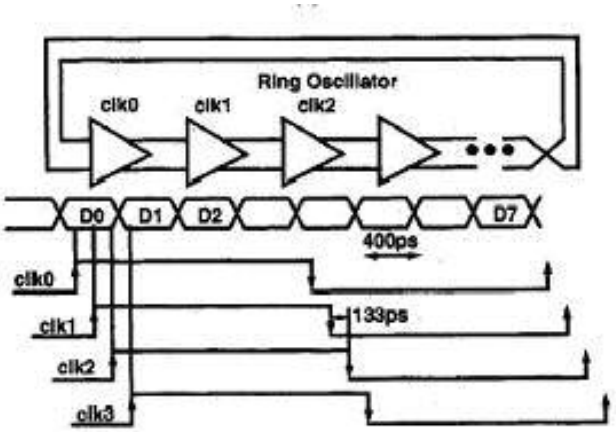


Figure 1.3 Multi-phase clocks used to oversample the data

Input samplers shown in Figure 1.2 use these multi-phase clocks to sample the input data. Transition Detection/Phase Selection Logic finds the position of data transitions in the sampled data and then generates a control signal for the multiplexers which select the data farthest from the transition. The sampled data is delayed by an amount which is equivalent to the time the Transition Detection/Phase Selection Logic takes to generate the control signal.

Generation of clocks with precise phase relationship is required otherwise considerable quantization jitter can result. Also, extra decision logic is required for post-processing, leading to a large active area and in turn high power consumption. Latch meta-stability is also an issue. The external clock used is an estimate of the time period or clock of the input data.

1.2.2 Clock Recovery using Hogge's Phase Detector

The Hogge's phase detector does the phase detection and retiming the data in the same circuit [1]. Figure 1.4 shows a Hogge's Phase Detector that can be used for clock recovery.

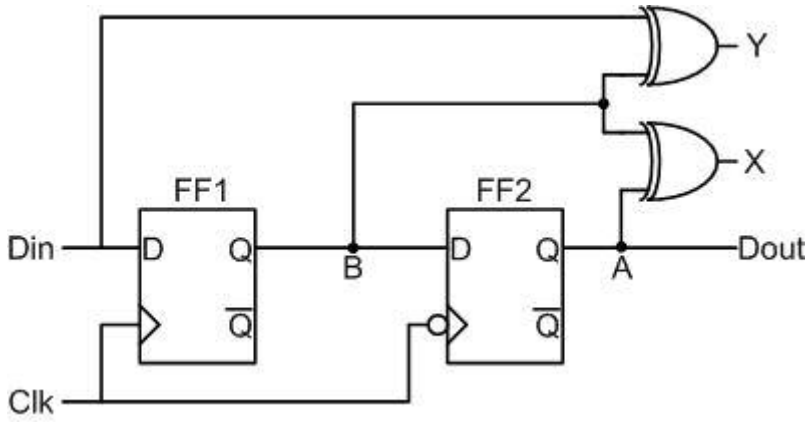


Figure 1.4 Hogge's Phase Detector

The above phase detector has two outputs X and Y. Referring to Figure 1.5 Y output gives us the phase difference between D_{in} and *CK* inputs. To understand this let us consider the output *B* of FF_1. It is effectively a delayed replica of D_{in}. It changes only when *CK* goes high. Therefore, if we pass them (D_{in} and *B*) through an XOR gate we would get the phase difference between the two. X is an output with constant width with pulses appearing only on data edges. If we refer back to Figure 1.4 we can see that FF_2 receives an inverted clock. Since the points *A* and *B* are connected to the XOR gate the output *Y* will have pulses only when there is a transition otherwise there will be no pulse. These pulses will be of fixed width $T_{CK}/2$. These pulses are also referred as the *reference clock*. Now, *Y* will be dependent on the transition density and *X* is dependent on the phase difference. The difference in the on time between these two pulses will give the required

phase difference. As shown in Figure 1.6 this difference can be obtained using a charge pump.

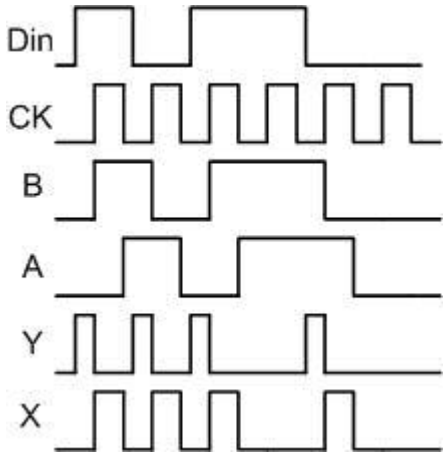


Figure 1.5 Output Waveforms of the Hogge's Phase Detector

Hogge's Phase Detector can be used as a Clock and Data Recovery circuit as shown in Figure 1.6. The retimed data is available at *Dout* and the recovered clock is

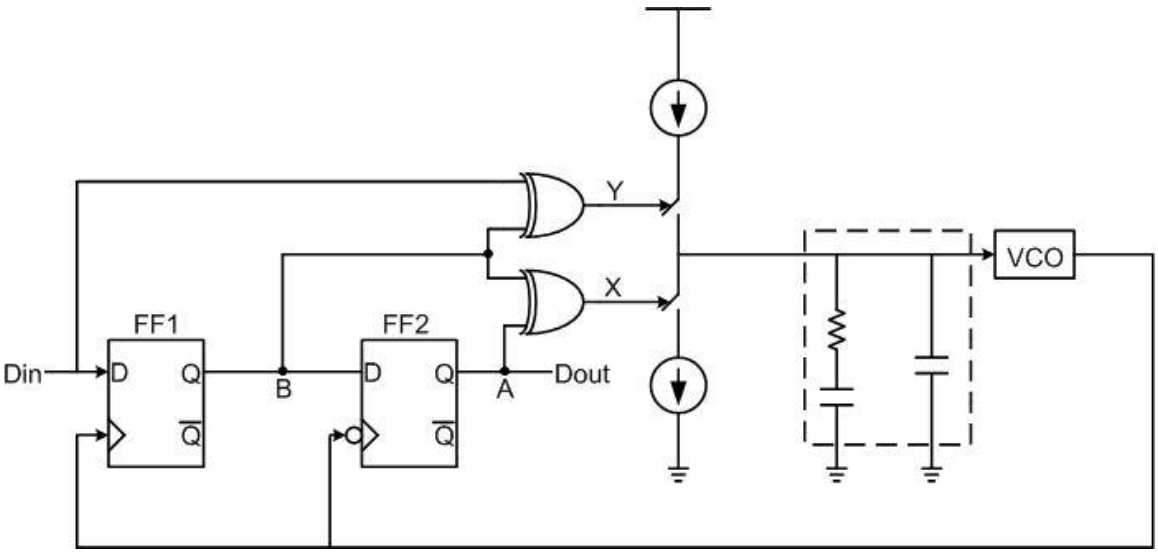


Figure 1.6 Hogge's Phase Detector in a Clock Recovery Circuit

obtained from the VCO. A draw back of the circuit in Figure 1.6 is that it produces a triangular wave as shown in Figure 1.7 when in lock.

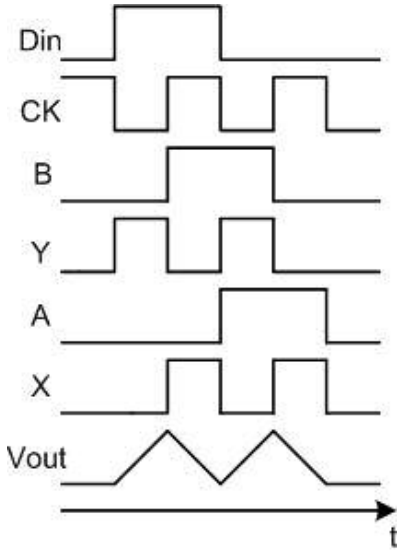


Figure 1.7 Waveforms of Hogge's PD when in lock

This Triangular wave exhibits a non-zero net area. As a result, the VCO frequency and phase is constantly disturbed due to this perturbance on its control voltage. Also, as will be seen in section 3.2 activity on the charge pump inputs causes other problems. In order to improve this situation in Hogge's Phase Detector it can be modified to include extra Flip Flops which provide extra reference pulses [2]. These pulses attempt to reduce the disturbances on the VCO control line by producing a *negative* triangular pulse. Consequently, a net zero area under locked condition is produced, lowering the disturbance level on the VCO phase. However, there is still some disturbance on the control line and this may lead to undesired charge deposit due to the non ideal operation of the charge pump. Also, there is a range of phase differences close to zero which this

phase detector is not able to detect. This range is decided by the meta-stability of the flip-flops.

Most importantly, the clock is extracted from the data stream unlike the Oversampiling Technique where is the clock used is an estimate of the input data.

1.2.3 Clock Recovery using Half-Rate Phase Detector

Clock recovery circuits employing a Half-Rate phase detector are used with data streams with *full-rate* but the VCO employed runs at *half* the input rate [3]. This type of phase detector is used in high speed clock recovery systems.

Figure 1.8 shows the configuration of a Half-Rate PD. Its principle of operation is depicted in Figure 1.9.

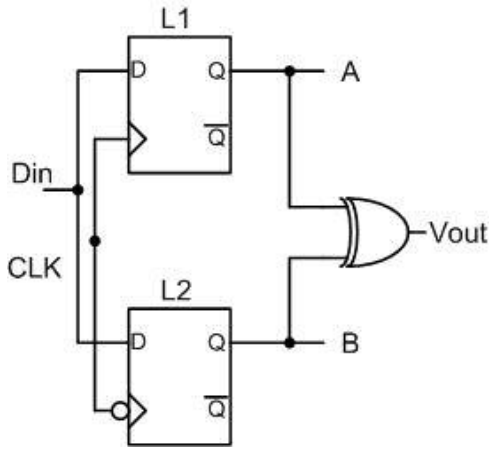


Figure 1.8 Simple Half-Rate PD

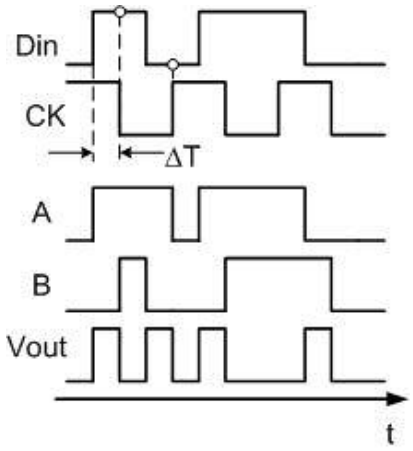


Figure 1.9 Principle of Operation of Half-Rate PD

As shown in Figure 1.9, to detect transitions in the data both edges of the half-rate clock are utilized. Referring to Figure 1.8, the latch L_1 is level high sensitive latch and L_2 is a level low sensitive latch. In the Figure 1.9 D_{in} is assumed to lead *CK* by ΔT. The output of L_1 thus will have a pulse width of $T_{CK}/2+\Delta T$. Similarly, the output of L_2 will be $T_{CK}/2-\Delta T$ because it is transparent when *CK* is low and latches when *CK* goes high. When we pass these outputs through a XOR gate the resulting output will have a pulse width of ΔT.

However, just like the Hogge's phase detector shown in Figure 1.4 this topology also exhibits the same dc output for two different phase differences resulting in a false lock. This can also be remedied by adding a reference pulse, as shown in Figure 1.10, with the help of L_3 and L_4.

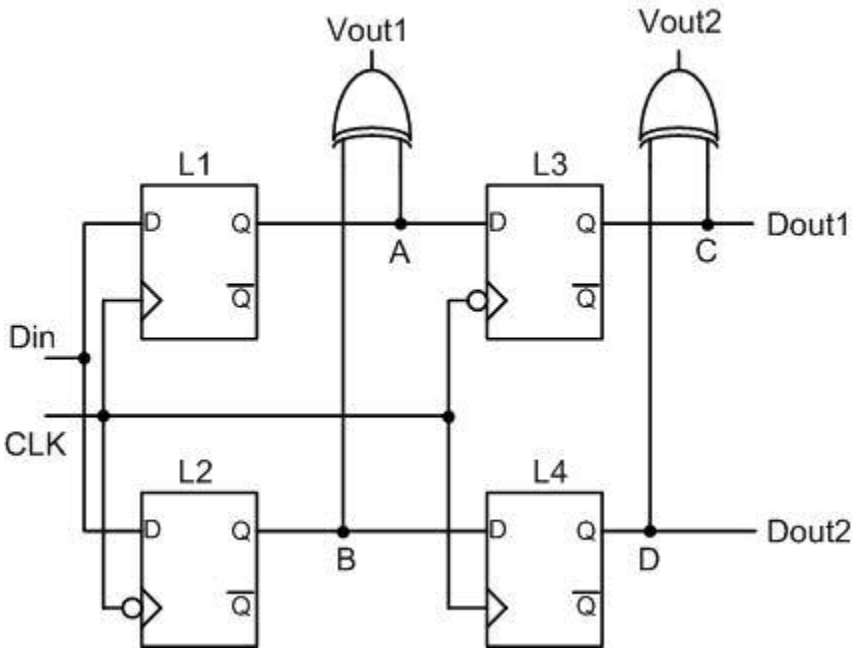


Figure 1.10 Complete Half-Rate PD

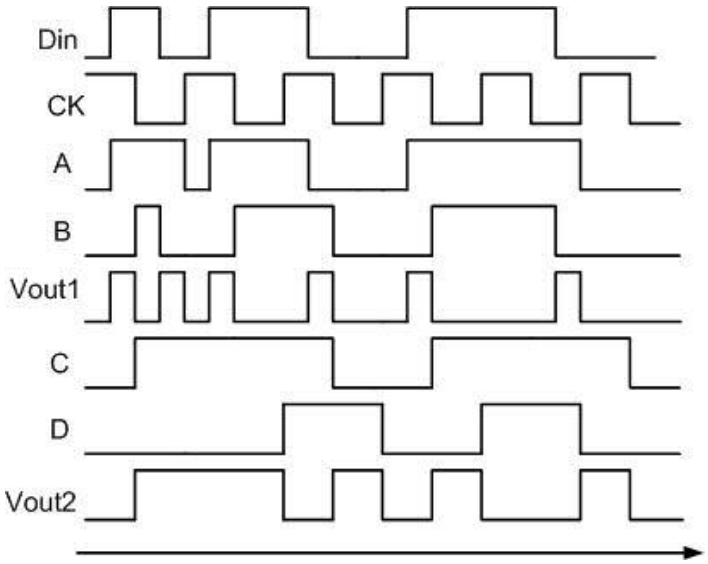


Figure 1.11 Waveforms of the Half-Rate PD

From Figure 1.11 we can observe that while *Vout1* gives information about the phase difference between the input data, *Din*, and the clock, *CK*, *Vout2* gives information about the transition density. In this way the drawback of the topology of Figure 1.9 can

be overcome. However, meta-stability of the flip-flops still affects the phase detection range of the phase detector.

1.2.4 Clock recovery using Gated VCO [4]

Figure 1.12 shows the block diagram for the gated recovery scheme.

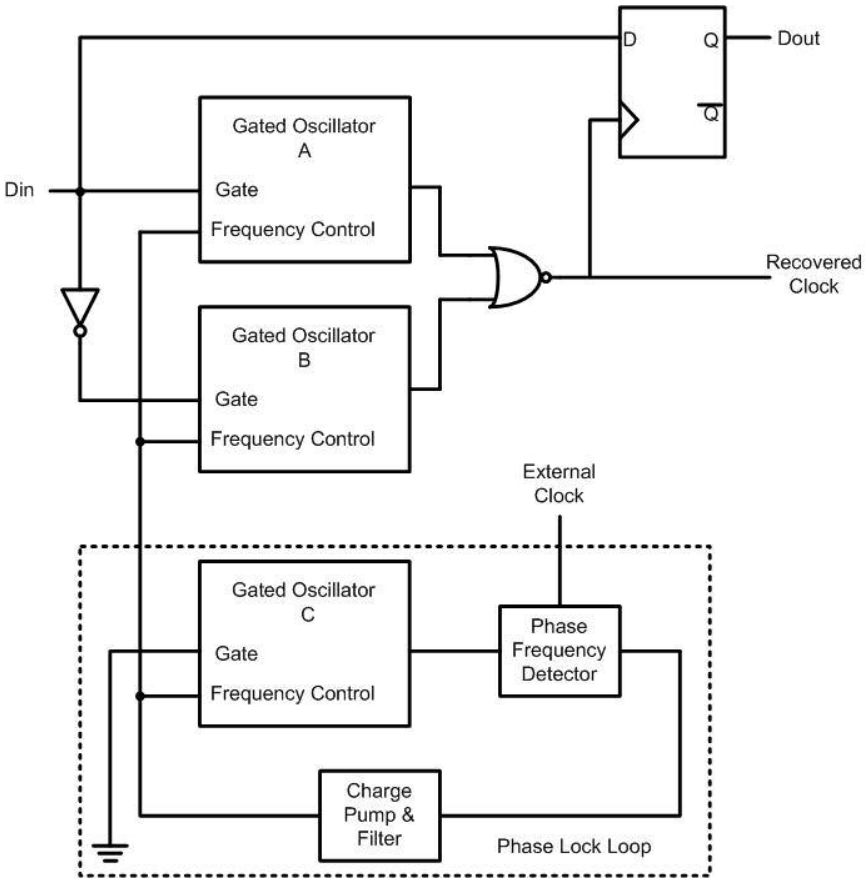


Figure 1.12 Clock Recovery using Gated Oscillators

In this recovery method a gated VCO is used – the VCO is started and stopped according to the incoming data. Figure 1.13 shows a Gated VCO. Their outputs are then

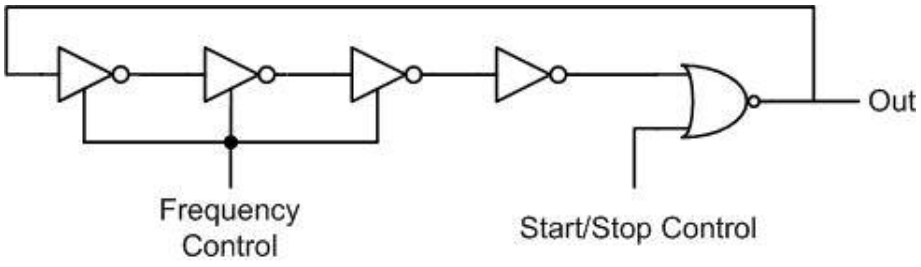


Figure 1.13 Gated VCO Oscillator

passed through a NOR gate which gives the recovered clock. The recovered clock is then used to retime the data using a D-latch. Figure 1.14 shows the recovered clock and data waveforms of the

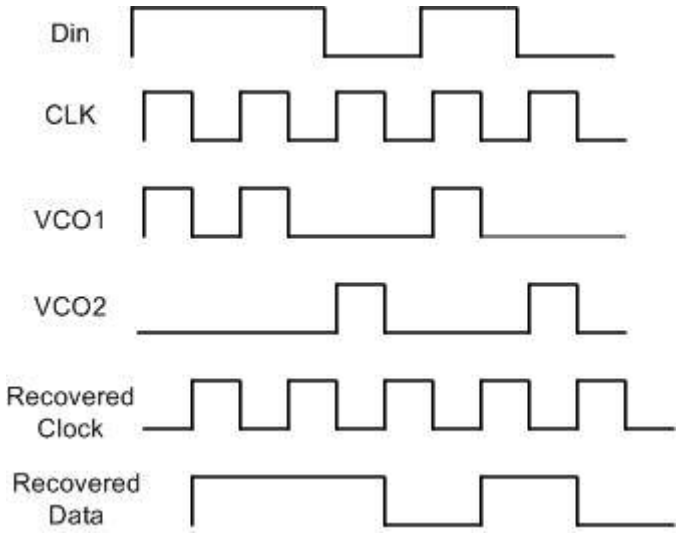


Figure 1.14 Clock and Data recovery using Gated VCO.

A key requirement for this clock recovery circuit is that the three oscillators should match each other in phase. All the oscillators are controlled by the same control voltage generated by the phase lock loop. The phase lock loop locks on to the external

reference frequency. Glitches may appear in the recovered clock if there are mismatches between the oscillator phases.

1.3 Brief Overview of Design and Estimation of PLL parameters

As is observed in the section 1.2, the crux of a clock and data recovery circuit is the PLL. To develop a feel for the PLL let us first recognize the important parameters in a PLL and then estimate their values. This will give us a rough idea of what must be considered while designing the different blocks.

The block diagram of a PLL is shown in Figure 1.15. The transfer function of each of the blocks is shown in Figure 1.16.

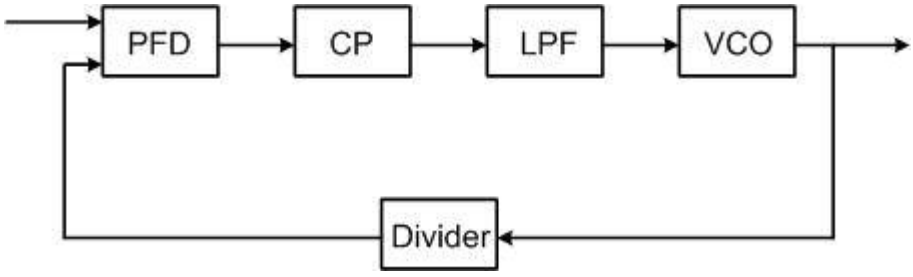


Figure 1.15 Block Diagram of a charge pump PLL

Both the charge pump and VCO contribute a pole at the origin. PLL with two poles at the origin are referred to as Type II PLLs. The presence of two poles at origin makes the system unstable without added compensation. Therefore, a zero in the form of loop filter is added to the loop to compensate or stabilize it. Figure 1.16 shows the linear

model of the charge pump PLL in the Laplace domain. All delays of the phase detector can be ignored.

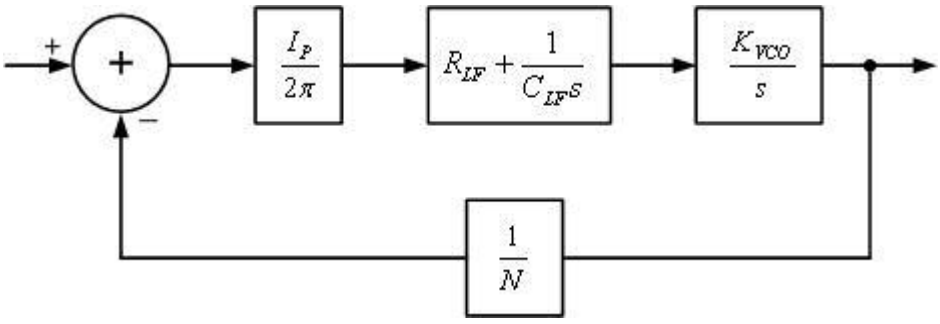


Figure 1.16 A Linear model of simple charge-pump PLL

From Figure 1.16 the open-loop transfer function is derived as given in equation(1.1).

$$\left.\frac{\phi_{out}}{\phi_{in}}(s)\right|_{open} = \frac{I_P}{2\pi}\left(R_{LF}+\frac{1}{C_{LF}s}\right)\frac{K_{VCO}}{s}, \tag{1.1}$$

Where, R_P and C_P form the loop filter resistor capacitor network. K_{VCO} is the sensitivity of the VCO in *Hz/V*. I_P is the charge pump current.

The closed loop transfer function then becomes

$$H(s) = \frac{N\left(1+sC_{LF}R_{LF}\right)}{1+sC_{LF}R_{LF}+\dfrac{s^2}{\dfrac{I_P}{C_{LF}}\dfrac{K_{VCO}}{N}}}, \tag{1.2}$$

In control systems or system theory form the general equation for the closed loop transfer function may be rewritten as;

$$\frac{\phi_{out}(s)}{\phi_{in}(s)} = N\frac{1+2\zeta\left(s/\omega_N\right)}{1+2\zeta\left(s/\omega_N\right)+\left(s/\omega_N\right)^2} \tag{1.3}$$

where, ζ is the damping factor and it is equal to

$$\zeta = \frac{1}{2}\sqrt{\frac{1}{N} I_P K_{VCO} R_{LF}^2 C_{LF}} \tag{1.4}$$

and ω_N is defined as the loop bandwidth and it is equal to

$$\omega_N = \sqrt{\frac{1}{N}\frac{I_P K_{VCO}}{C_{LF}}}\,. \tag{1.5}$$

The denominator of equation (1.3) can also be written as

$$1 + \frac{s}{\omega_N Q} + \frac{s^2}{\omega_N^2} \tag{1.6}$$

Q is the Q-Factor of the transfer function and is given by

$$Q = \frac{1}{2\zeta} \tag{1.7}$$

Q = ½ or ζ = 1 is recommended for most PLL applications [5].This value of Q results in a critically damped system. Further, to ensure stability ω_N should be much less than the ω_{Osc}, preferably 10 times less [5]. This is a practical limitation or implementation of sampling theory.

From equations (1.4) and (1.5) we have,

$$R_{LF} C_{LF} = \frac{2\zeta n}{\omega_{Osc}} \tag{1.8}$$

Assuming a value of *5pF* for the loop filter capacitor. Then from equation(1.8) we obtain a value of 16KΩ for the loop resistor R. If we further assume a value of 30μA for the charge pump current, I_{CH} and N as 2, we get a value of about K_{VCO} = *200MHz/V* from equation(1.4).

1.4 Thesis Organization

There are a total of 6 chapters in this thesis. Chapter 2 presents a Manchester Encoder-Decoder developed using the Harsh Environment Cell Library developed in the lab using Peregrine 0.5u process. It presents the test results attained at both room and high temperature.

Chapter 3 discuss the Charge Pump. A review of different topologies reported in the literature is presented where their advantages and disadvantages are enumerated. A discussion in section 3.2 attempts to convey the fact that the charge pump is the most critical aspect of any PLL. Factors affecting Charge Pump performance are discussed and means to mitigate their effects are formulated. A selected topology is then proposed that tries to minimize all non-ideal operations of the charge pump.

Chapter 4 discusses the Voltage Controlled Oscillator. Topologies from literature are discussed and again an optimum topology is selected. Section 4.4 briefly discusses the "kink effect" found in Peregrine transistors on the performance of the VCO and it effects on circuit design. Ways to reduce the "kink effect" on VCO performance are proposed in section 4.5. Chapter 5 introduces and reviews significant topologies of Phase Frequency Detectors available in literature. A future effort for a high temperature PLL design for use with the Manchester Decoder of Chapter 2 is outlined in Chapter 6.

Chapter 2

Manchester Encoder and Decoder

2.1 Introduction

Manchester encoding is a mechanism 1) to convert parallel data to serial data and 2) to redefine data (ones and zeros) representation from level to an edge (rising or falling) at mid clock, i.e. to represent “ones”, as shown in Figure 2.1**,** Manchester encoded data starts high at the start of clock period and goes low (a falling edge) at mid clock period. It is opposite for a “zero”. Decoder’s function is to recover the encoded data back to level representation.

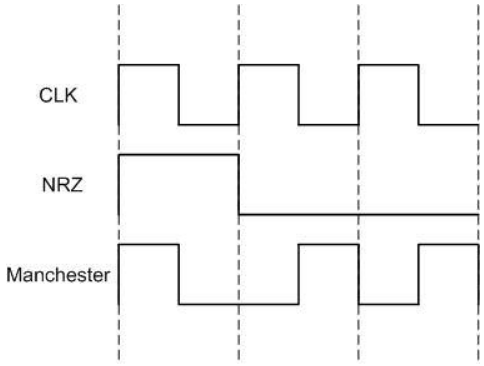


Figure 2.1. Data Representation

The general format of the transmitted data is shown in Figure 2.3. The additional Sync signal and Parity are inserted to the front and back before transmission. Sync signal has two variations; command and data. Command Sync signal is used by master devices and the Data Sync signal is used by slave devices (Figure 3). Figure 4 shows an example waveform of 16 bit data stream (3814H) with Command Sync and odd parity. An even parity can also be used. However, in the encoder discussed in this report an odd parity was used.

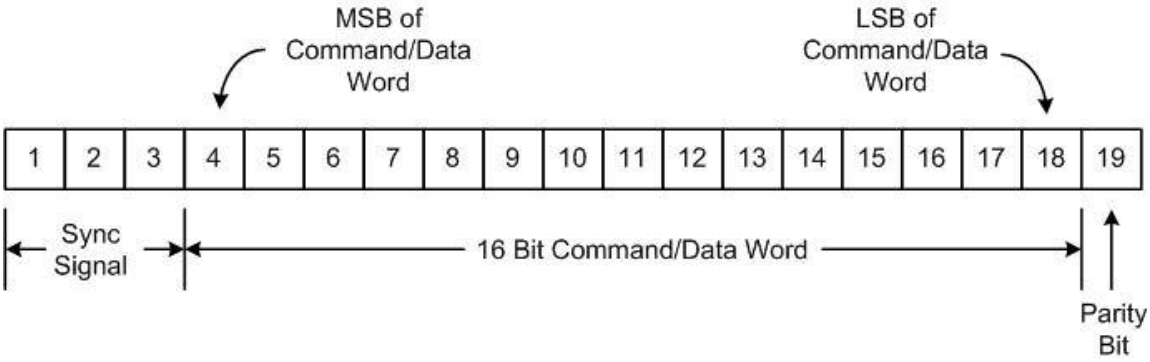


Figure 2.2. General format of a Manchester Encoded Data

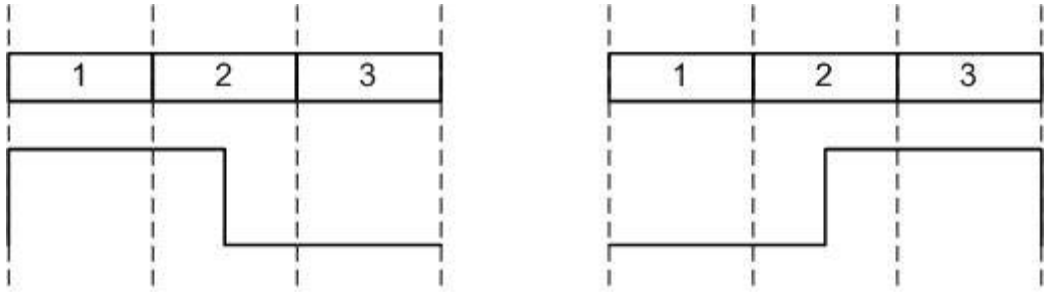


Figure 2.3. (a) Command Sync (b) Data Sync.

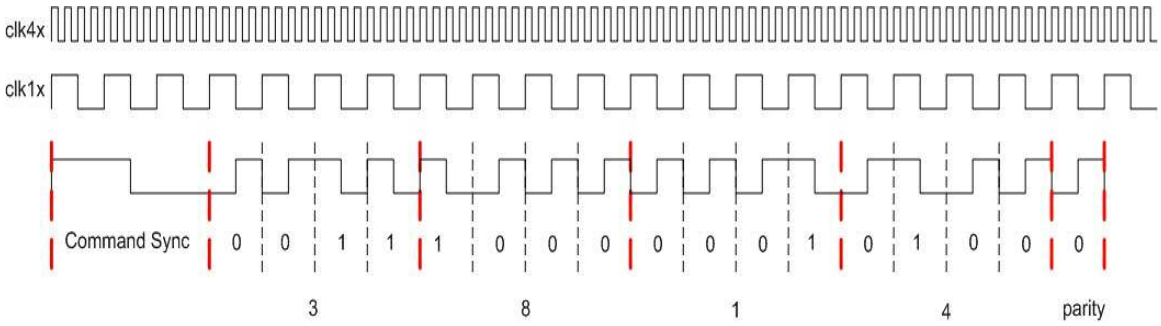


Figure 2.4. Waveform of 16 bit data "3814H" with odd parity (4X oversampling is used to encode and decode the data).

If we observe the waveform in Figure 2.4 clock rate of the embedded clock (clk1x) is half the data rate of the Manchester stream.

2.2 Encoder

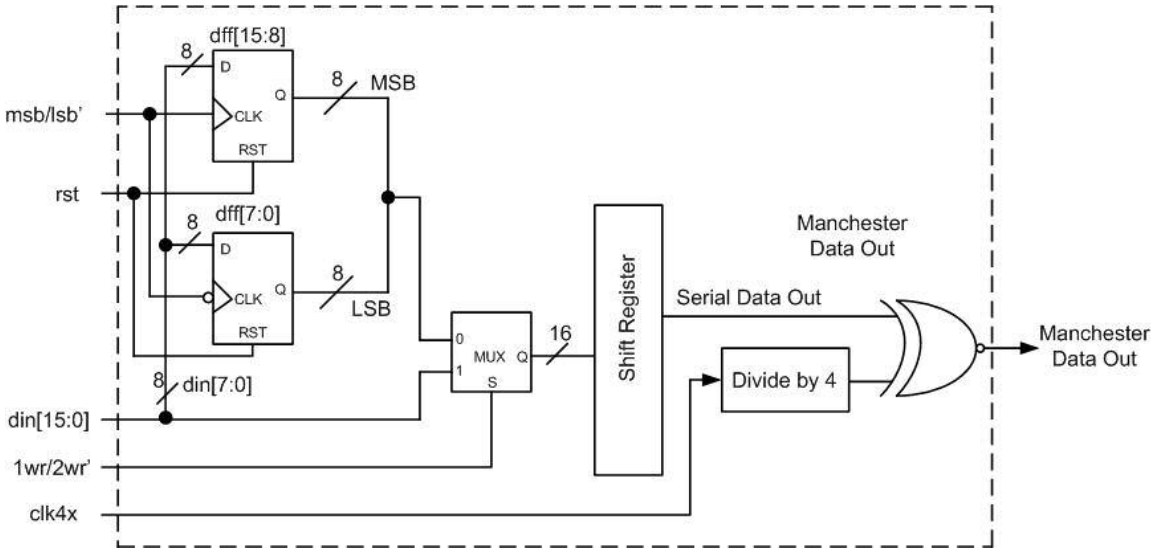


Figure 2.5 Encoder System Diagram

The encoder operates in two modes: single write mode and two byte write mode. A high on *1wr/2wr'* pin indicates a single write mode, whereas a low indicates double

byte write mode. During the single write mode the *din[15:0]* is directly routed to the shift register by the multiplexer. During the double byte write mode a positive edge on the *msb/lsb'* pin latches the data on *din[7:0]* to the upper byte of the internal register. A negative edge on the *msb/lsb'* pin latches the data on *din[7:0]* to the lower byte of the internal register. The multiplexer then selects this 16 bit internal register and passes it on to the shift register. The serial data out from the shift register is passed through a XNOR gate whose second input is a divide by 4 clock, derived from the input clock (*clk4x*). The output of XNOR gate is the Manchester Data Out.

2.3 Decoder

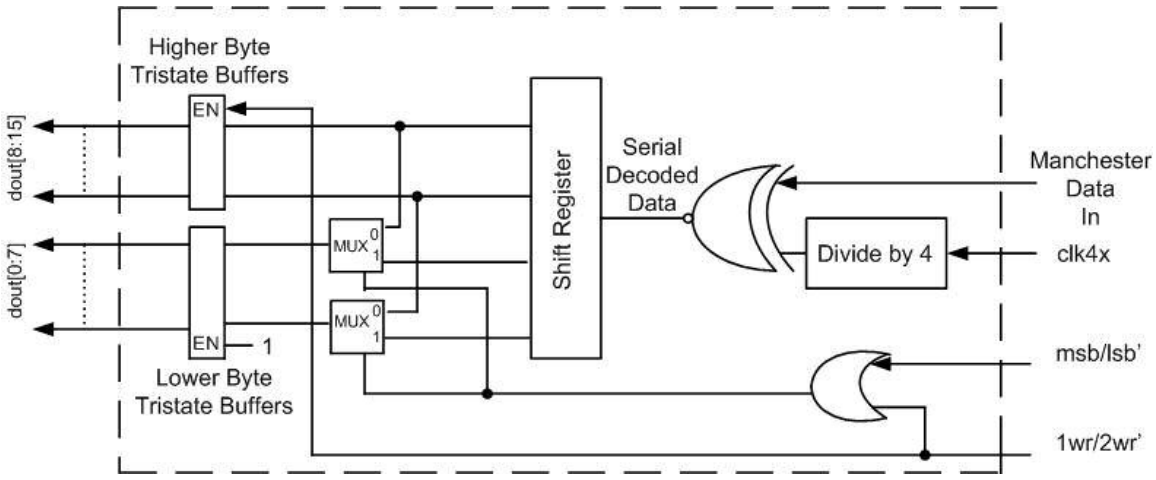


Figure 2.6. Decoder System Diagram

As shown in Figure 6 the decoded parallel outputs of the Decoder (*dout[15:0]*) are connected to tri-state buffers with a high enable. Also as shown, EN is the enable pin of the tri-state buffers. The serial Manchester Data In is decoded using a XNOR gate

whose second input is a divide by 4 clock derived from the clock input (*clk4x*). The result is then stored in a shift register. If the decoder operates in a single write mode, *1wr/2wr'* signal is high and all the tri-state buffers are enabled. Since the output of the OR gate is always high in this mode the 16 bit output is at *dout[15:0]* pins. If the decoder operates in a double byte write mode then the tri-state buffers of *dout[8:15]* are disabled since *1wr/2wr'* is low. When *msb/lsb'* pin is pulled high the output of the OR gate is high, the upper byte of the shift register is valid at *dout[7:0]*. When it is low the output of the OR gate is low, the lower byte is valid at *dout[7:0]*.Decoder converts the incoming serial Manchester data to parallel data.

2.4 Simulation and Test Results

2.4.1 Encoder

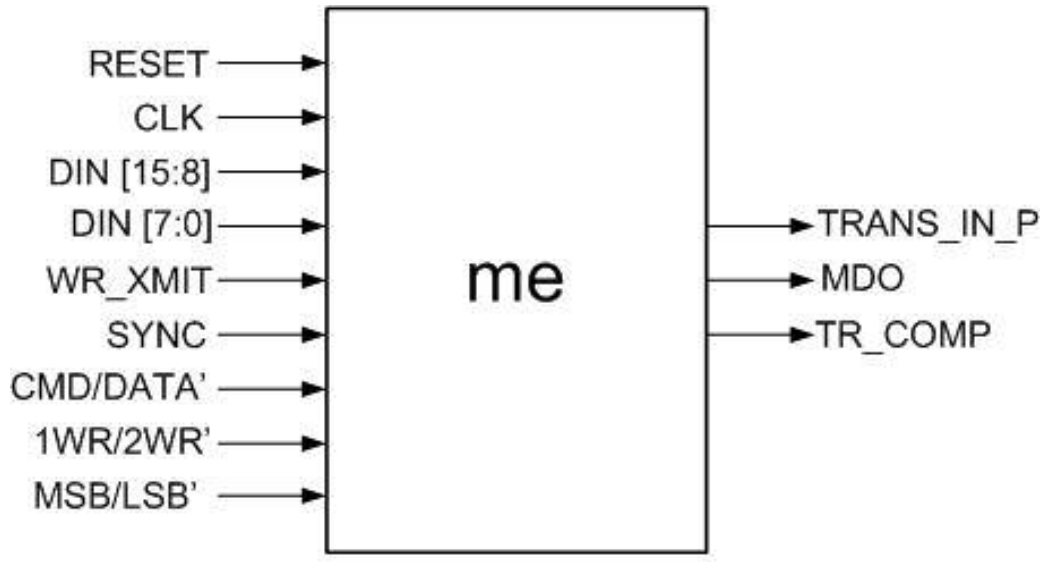


Figure 2.7 Pin diagram of Encoder

As shown in Figure 2.7 the input pins are:

1. 1WR/2WR' – when this pin is low, the encoder operates in double write mode and accepts two 8 bytes. It operates in single write mode when this is high.
2. MSB/LSB' – when this pin is high DIN[7:0] pins should have MSB loaded onto them. When low it indicates LSB should be loaded. This pin can go low to high or high to low. A low to high transition is needed to load MSB into the internal registers and similarly a high to low transition is needed to load LSB into the internal registers.
3. DIN[7:0] – LSB of the input data during both double and single write operation.
4. DI/DIN[15:8] – Disabled internally during double write mode, MSB input data during single write mode.
5. RESET – resets all internal flip-flops.
6. CLK – clock input
7. WR_XMIT – input pulse which tells the encoder to latch data on its input bus and start encoding of data. A low to high transition is all that is needed. Width of the pulse is not important.
8. DATA'/CMD – attaches Data Sync when this pin is low and a Command Sync when high.

The output pins are :

1. MDO – Manchester Data Out.
2. TRANS_IN_P – indicates that transmission is in progress.
3. TR_COMP – when high it indicates that transmission is complete. Encoder waits for the next data.

2.4.1.1 Single write mode with a Command Sync inputs - 1WR/2WR' = 1, cmd/data' = 1, din = A863H

Figure 2.8 shows the simulation results in this mode. The "1wr/2wr' " or "bit16" signal is high, so the encoder operates in the single write mode. It accepts a 16 bit input and encodes it. Encoding starts when there is a rising edge on the "wrn" input. Since the "sync" or "cmd/data' " signal is high the encoder attaches a Command Sync to the encoded Manchester output signal. During encoding the "trans_in_p" is high. When encoding is complete "trans_in_p" goes low. At the end of encoding, "tbre" or "tran_comp" signal goes high indicating that the encoder is ready for the next data. Any change on the "msb" or "msb/lsb' " pin does not affect the operation of the encoder during the single write mode.

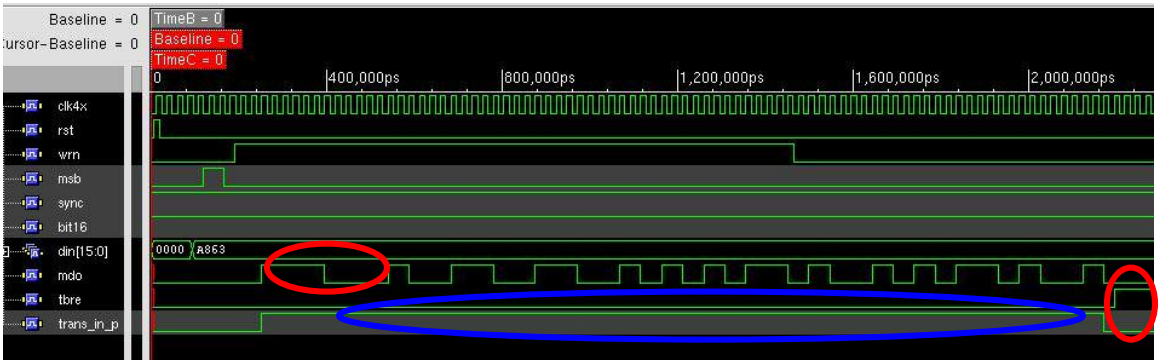


Figure 2.8. Simulation of single write mode with a Command Sync inputs 1WR/2WR' = 1, cmd/data' = 1, din = A863H

Figure 2.9 shows the measurement results of the Encoder obtained from Logic Analyzer at room temperature. Figure 2.10 shows the measurement results at 195°C.

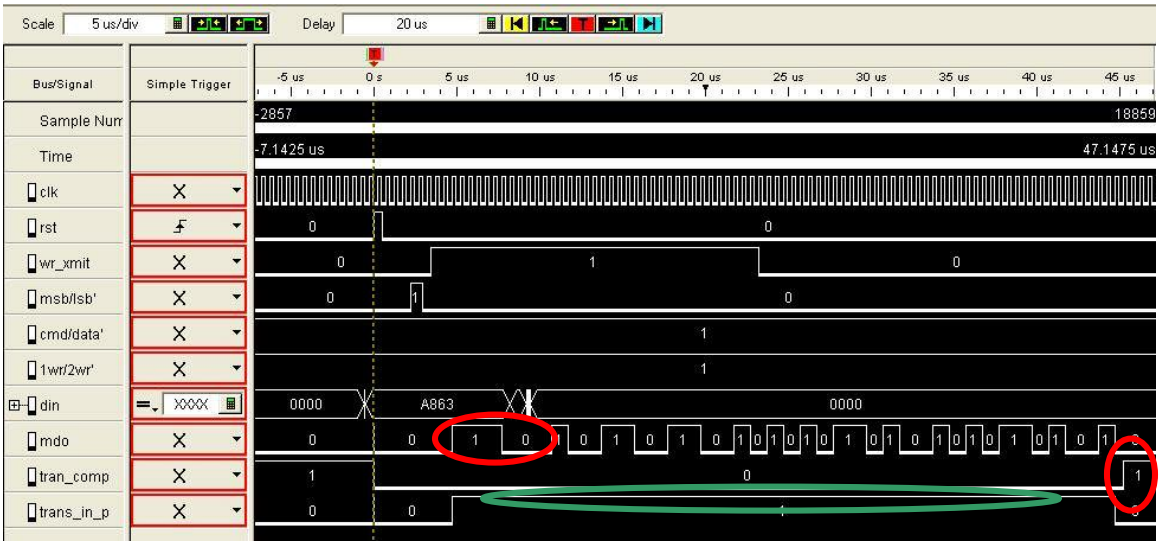


Figure 2.9. Measurement of Single write mode with a Command Sync, 1WR/2WR' = 1, cmd/data' = 1, din = A863H at Room Temperature

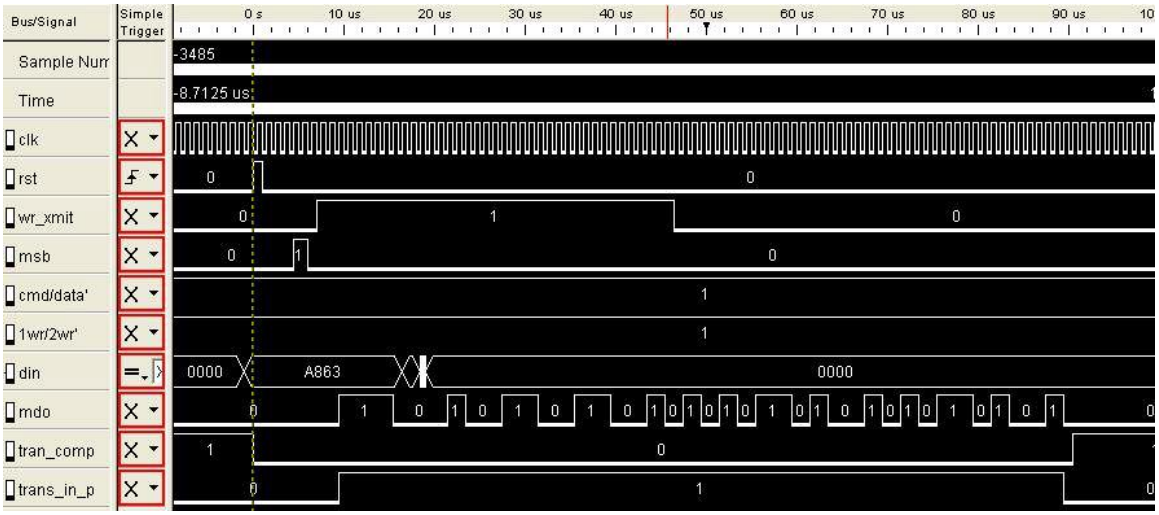


Figure 2.10. Measurement of Single write mode with a Command Sync, 1WR/2WR' = 1, cmd/data' = 1, din = A863H at 195°C

2.4.1.2 Single write mode with a Data Sync inputs - 1WR/2WR' = 1, cmd/data' = 0, din = A863H

Figure 2.11 shows the simulation results in this mode. In this mode the "sync" or "cmd/data' " signal is low, so a Data Sync is attached.

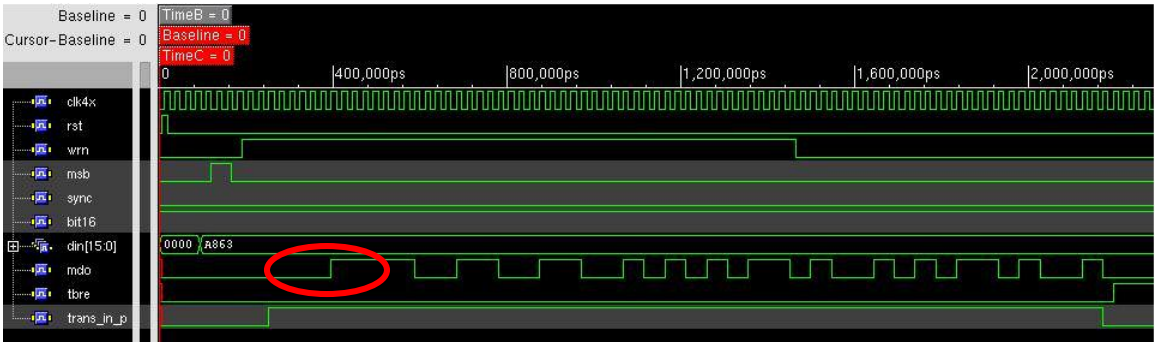


Figure 2.11. Simulation of Single write mode with a Data Sync inputs - 1WR/2WR' = 1, cmd/data' = 0, din = A863H

Figure 2.12 shows the measurement results of the Encoder obtained from Logic Analyzer at room temperature. Figure 2.13 shows the measurement results at 195°C.

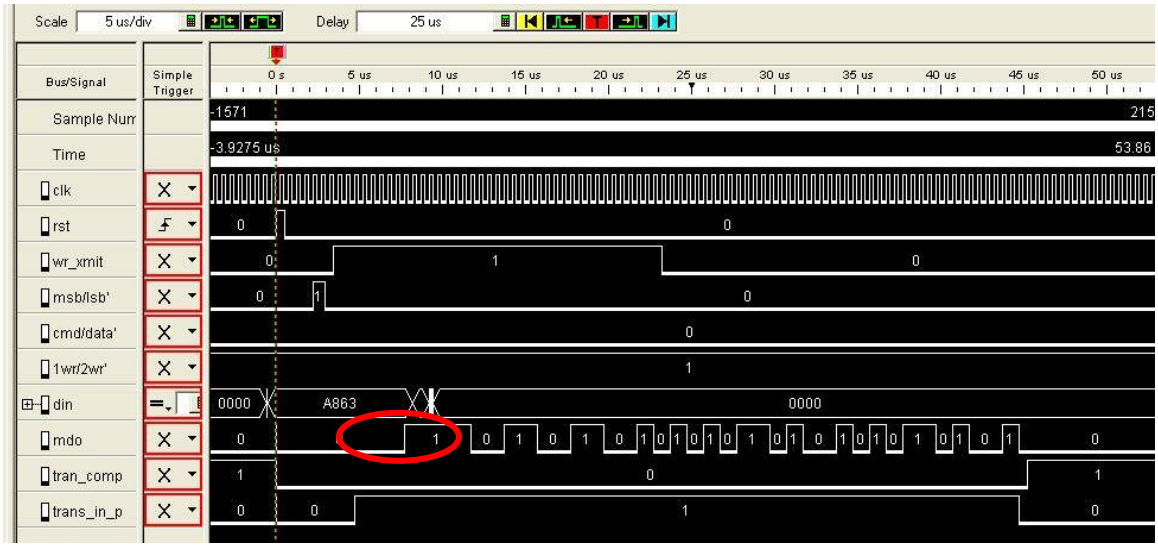


Figure 2.12. Measurement of Single write mode with a Data Sync inputs - 1WR/2WR' = 1, cmd/data' = 0, din = A863H, at Room Temperature

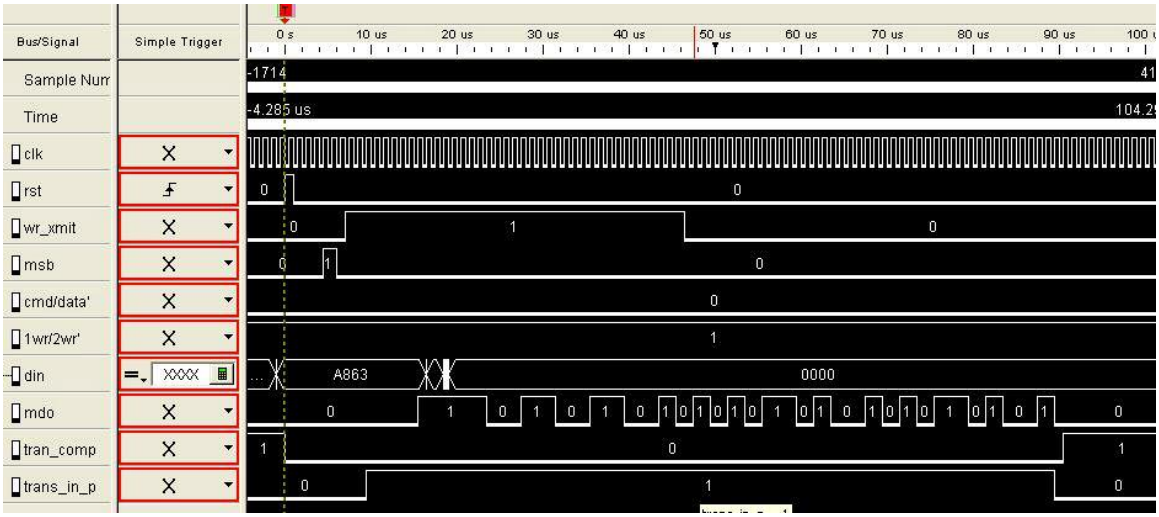


Figure 2.13. Measurement of Single write mode with a Data Sync, inputs - 1WR/2WR' = 1, cmd/data' = 0, din = A863H, at 195°C

2.4.2 Decoder

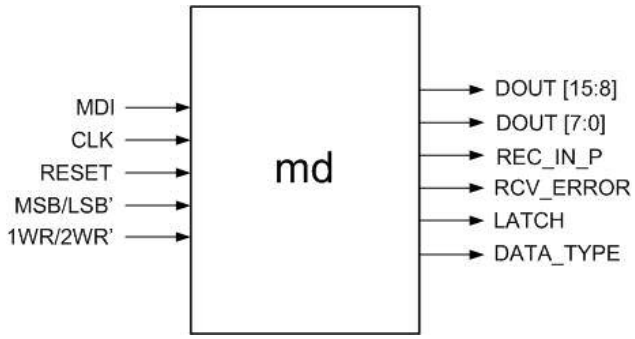


Figure 2.14 Pin diagram for Decoder

As shown in Figure 2.14 the input pins are:

1. MDI – Manchester Data In.
2. RESET – resets all internal flop-flops.
3. CLK – clock input
4. 1WR/2WR' – when this pin is low, the encoder operates in double write mode and accepts two 8 bytes. It operates in single write mode when this is high.

5. MSB/LSB' – when this pin is high it indicates that the data on DOUT[7:0] pins have MSB loaded onto them. When low it indicates that LSB is loaded. This pin can go low to high or high to low.

The output pins are

1. DOUT[7:0] – LSB of the output data during both double and single write operation.
2. DOUT[15: 8] – Tri-stated during double write mode and MSB of output data during single write mode.
3. LATCH – when high it indicates that the data is ready and is ready to be latched.
4. DATA_TYPE – when low it indicates that the input Manchester data has Data Sync and when high it has a Command Sync attached to it.

2.4.2.1 Single write mode with a Command Sync input, 1WR/2WR' = 1, 'mdi' corresponds to AAD5

Figure 2.15 shows the simulation results in this mode. Since the "bit16" or "1wr/2wr' " input is high, the decoder operates in a single write mode. As soon as the decoder detects the sync command at the beginning of serial Manchester data input it begins decoding. If a Command Sync is attached to the data input the "data_type" output goes high. If a Data Sync is attached to the data input the "data_type" output goes low. At the completion of decoding the output signal "data_ready" or "latch" goes high.

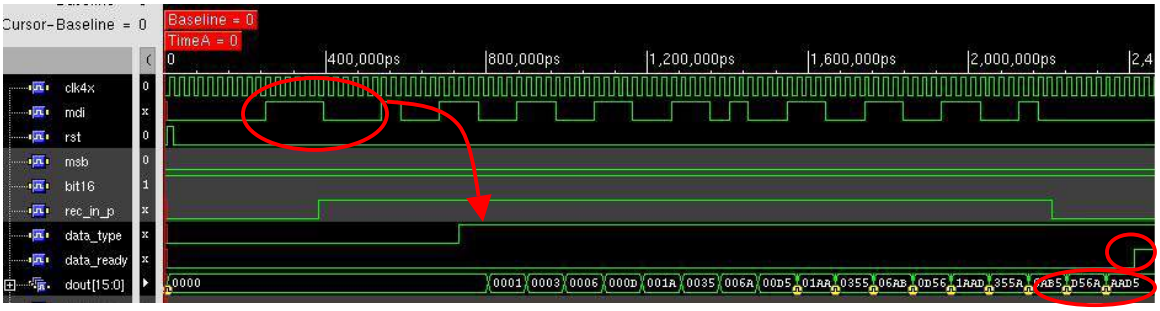


Figure 2.15. Simulation of Single write mode with a Command Sync input, 1WR/2WR' = 1, 'mdi' corresponds to AAD5H

Figure 2.16 shows the measurement results of the Encoder obtained from Logic Analyzer at room temperature. Figure 2.17 shows the measurement results at 195°C.

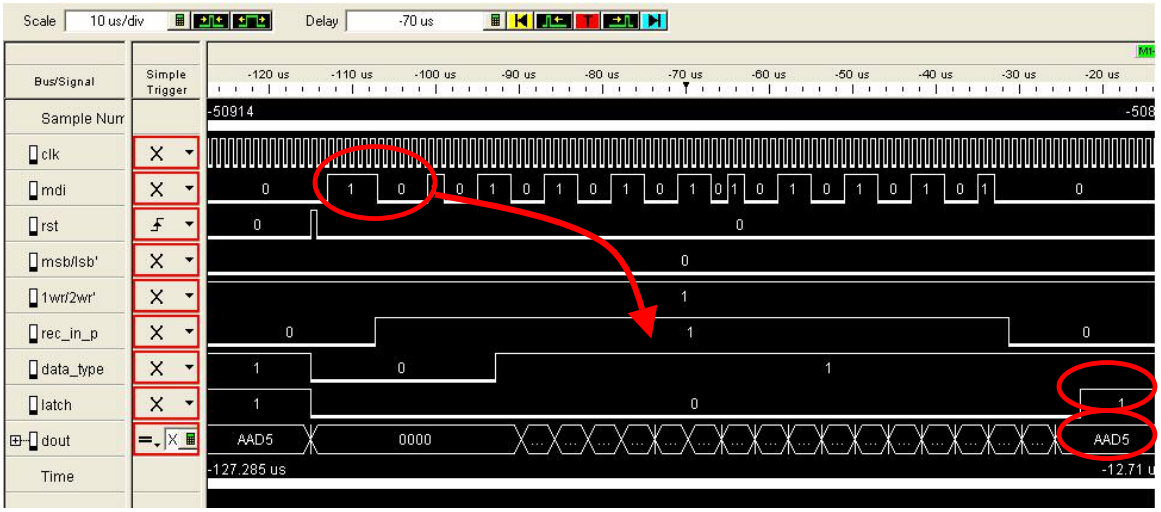


Figure 2.16. Measurement of Single write mode with a Command Sync input, 1WR/2WR' = 1, 'mdi' corresponds to AAD5H, at room temperature

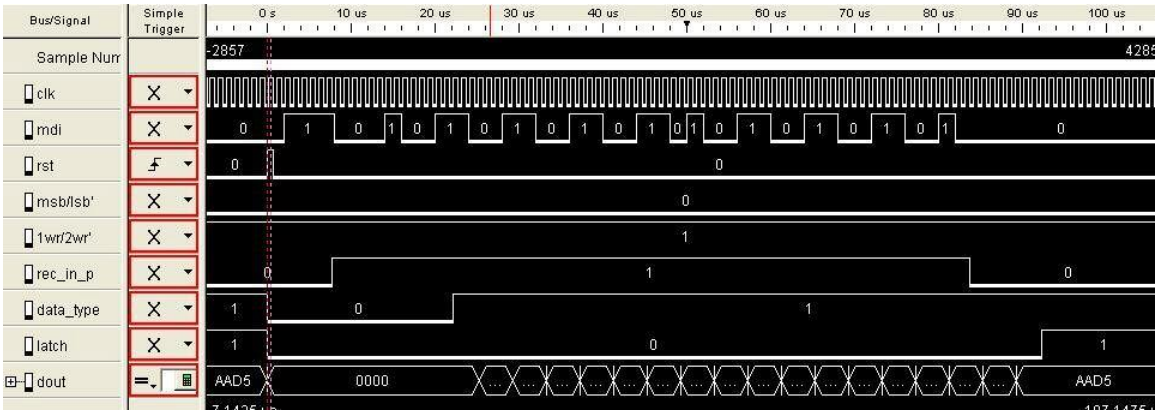


Figure 2.17. Measurement of Single write mode with a Command Sync input, 1WR/2WR' = 1, 'mdi' corresponds to AAD5H, at 195°C

2.4.2.2 Single write mode with a Command Sync input, 1WR/2WR' = 1, 'mdi' corresponds to AAAA

Figure 2.18 shows the simulation results in this mode. In this case a 16 bit data of AAAA is decoded.

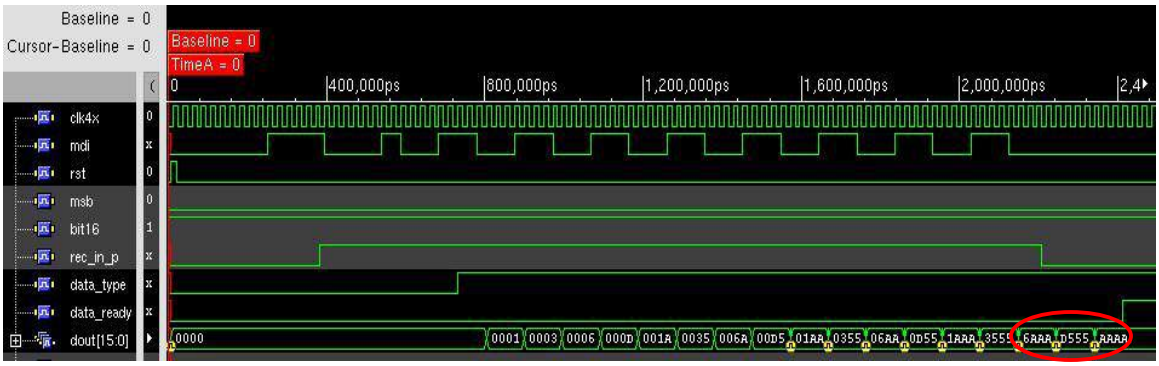


Figure 2.18. Simulation of Single write mode with a Command Sync input, 1WR/2WR' = 1, 'mdi' corresponds to AAAAH

Figure 2.19 shows the measurement results of the Encoder obtained from Logic Analyzer at room temperature. Figure 2.20 shows the measurement results at 195°C.

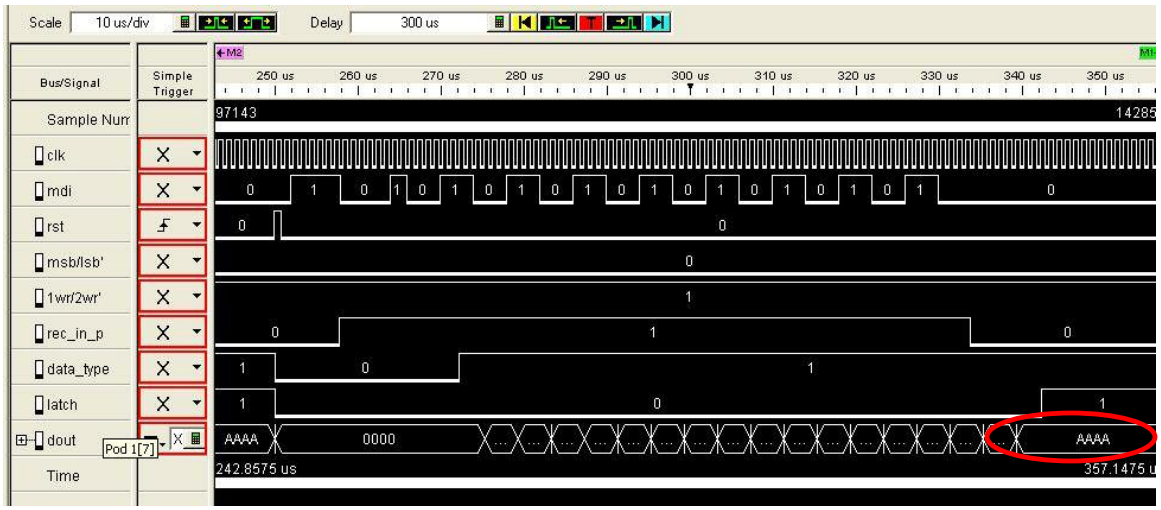


Figure 2.19. Measurement of Single write mode with a Command Sync input, 1WR/2WR' = 1, 'mdi' corresponds to AAAAH, at Room Temperature

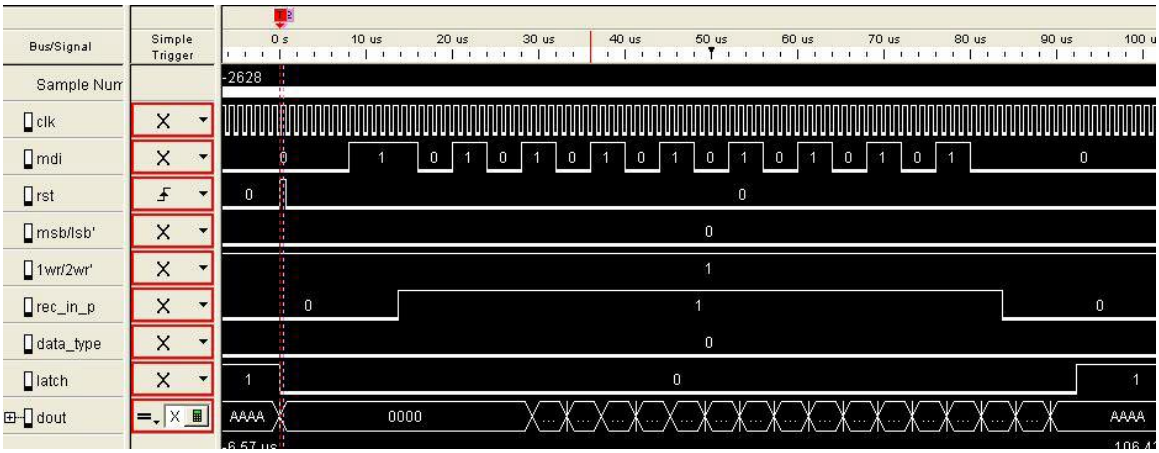


Figure 2.20. Measurement of Single write mode with a Command Sync input, 1WR/2WR' = 1, 'mdi' corresponds to AAAAH, at 195°C

2.4.2.3 Single write mode with a Data Sync input, 1WR/2WR' = 1, 'mdi' corresponds to AAAA

Figure 2.21 shows the simulation results in this mode. In this case a Data Sync is attached to the input serial Manchester data.

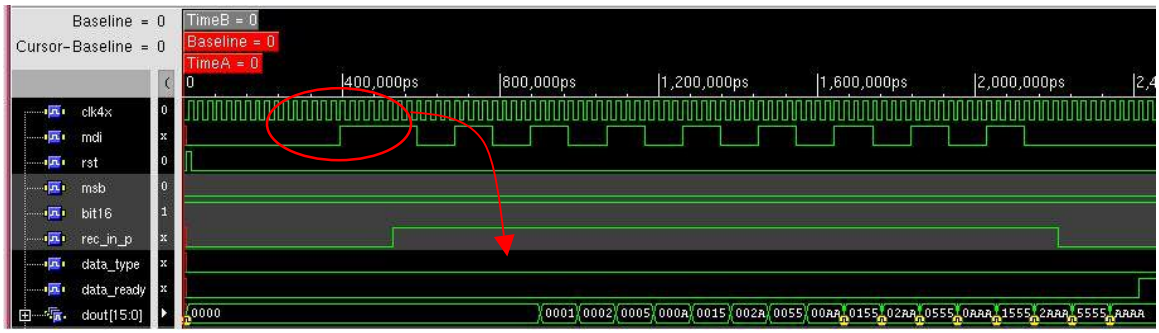


Figure 2.21. Simulation of Single write mode with a Data Sync input, 1WR/2WR' = 1, 'mdi' corresponds to AAAAH

Figure 2.22 shows the measurement results of the Encoder obtained from Logic Analyzer at room temperature. Figure 2.23 shows the measurement results at 195°C.

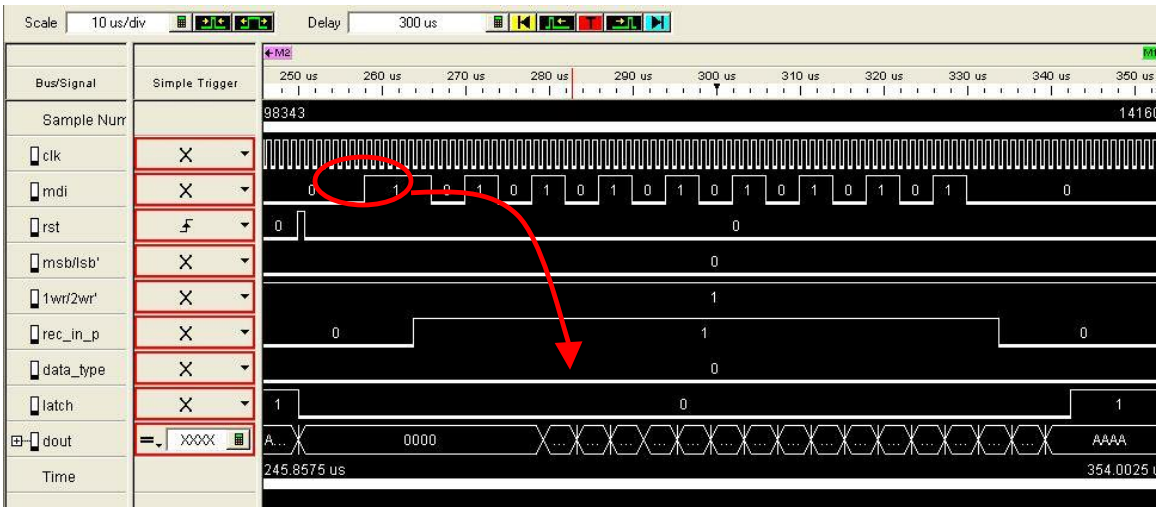


Figure 2.22. Measurement of Single write mode with a Data Sync input, 1WR/2WR' = 1, 'mdi' corresponds to AAAAH, at Room Temperature

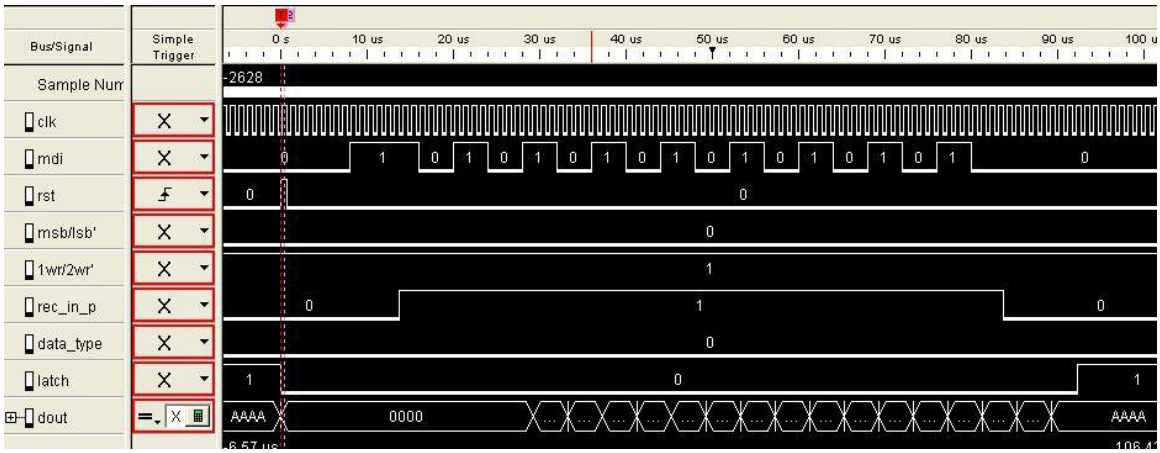


Figure 2.23. Measurement of Single write mode with a Data Sync input, 1WR/2WR' = 1, 'mdi' corresponds to AAAAH, at 195°C

2.4.3 Summary of Test Results

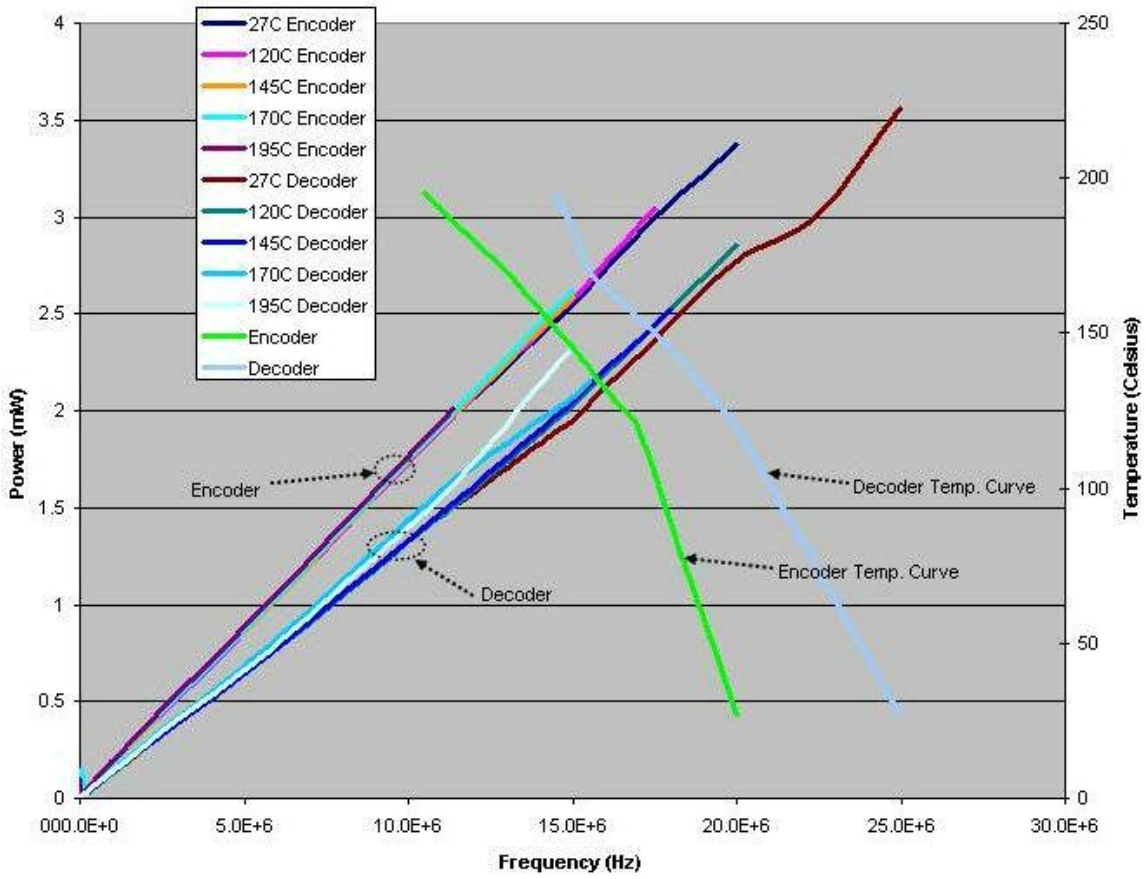


Figure 2.24. Frequency vs Power and Frequency vs Temperature for Manchester Encoder and Decoder

Figure 2.24 shows the power consumption of the Manchester Decoder and Encoder with varying frequency at different temperatures (27°C, 120°C, 145°C, 170°C and 195°C). The curves show that the power consumption follows the classic CV^2f curve and is independent of temperature. The maximum operational frequency of the Decoder at Room Temperature was found to be 25MHz, whereas, the Encoder was found to operate at a maximum frequency of 20MHz at room temperature. Temperature de-rating of both circuits was found to follow the mobility degradation with temperature, measured in the MSVLSI Lab [6].

Chapter 3

Charge Pump

3.1 Introduction

The Charge pump is the critical block of any PLL the PFD-charge pump combination PLL. It is responsible for the accurate conversion of digital levels of the PFD to stable analog levels. Charge pump has two inputs – up (UP) and down (DW). One of these inputs causes either a deposition or removal of the charge from the capacitor following it. The capacitor is a part of the loop filter in Phase Locked Loop. The PFD, which precedes it, determines which of these events occur. By doing so, it changes the voltage across the capacitor. This voltage is fed to the VCO modifying its frequency of operation. The input which increases the frequency is designated as UP. Depending on the architecture of the VCO this input may either deplete or deposit charge in the output capacitor.

Since the voltage generated by the charge pump in conjunction with the loop filter acts as a control voltage of the VCO, any spike in this voltage produces undesirable spurious tones in the VCO output signal[7]. Ripples or spikes in the control voltage are

produced mainly due to the following reasons – charge injection, charge sharing, mismatch in the UP and DW currents due to channel length modulation, mismatch in the switching time of the UP and DW switches and off-state leakage. When we examine the aforementioned causes of non-ideal behavior we can conclude that the charge pump in a PLL is the most critical block. A thorough understanding of these irregularities is essential in order to build a close to ideal PLL.

3.2 Factors causing Non Ideal Operation

The factors can be separated into two categories. Factors like mismatch in UP – DW currents due to channel length modulation, mismatch in turn on times of the UP – DW switches and leakage of the switches can be categorized together. The reason for flocking them together is that they cause the loop filter voltage to either rise up or go down slowly or quickly during the UP or DW phases. The loop finally reaches the desired frequency and phase. Thus it is desirable to reduce these error but not extremely critical.

Other causes – charge injection and charge sharing can be grouped together as well. Minimizing the error due to these is *very* critical for the operation of PLL because they result in a frequency error that exists between the VCO and reference clocks. The following sub-sections discuss these errors in depth.

3.2.1 Charge Injection

Charge injection occurs when switches turn off. When an NMOS (PMOS) switch is opened, the electron (hole) charge accumulated in the channel of the MOS switch to

escape either through the drain or the source. If this escaping charge gets deposited on the loop filter then it causes ripples or spikes in the control voltage as mentioned before. In order to minimize this we must first recognize the factors causing it and then attempt to find ways of mitigating its impact on the loop filter error voltage.

The charge in the channel is mainly composed of (1) Body Charge and (2) Channel Charge. Body charge appears in the channel when the switch reaches weak inversion. When the switches go to inversion, channel charge shows up in the channel. In most commonly used charge pump topologies - [8], [9], [10], [11], [12], a differential pair is used. When one of the transistors in the source coupled pair is turning on, the other is turning off. To investigate where or how the charges of the switches move when the switching or current steering operation occurs a differential pair shown in Figure 3.1 was used. The swing on the inputs was chosen such that the switches go from strong inversion to weak inversion.

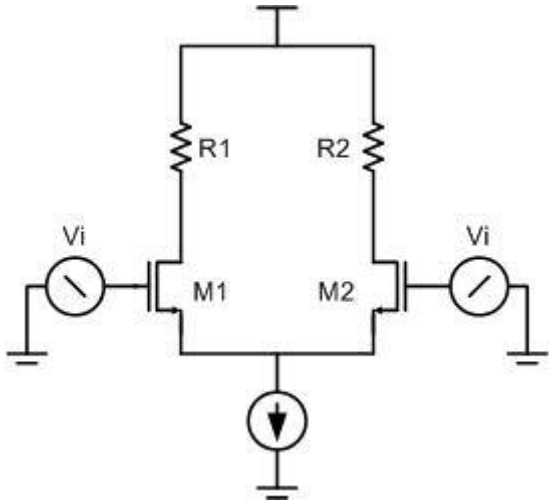


Figure 3.1 Differential Pair Used for Charge Flow Investigation

As is depicted in Figure 3.1 transistor M1 is being turned off and M2 is being turned on. When the switch M2 goes from weak inversion to strong inversion additional electrons (NMOS) are required to charge up or invert its channel. In an NMOS, electrons flow from source to drain. Therefore, for this to be true, the source current should be higher than drain current for transistor M2 i.e. more electrons enter the source than are leaving the drain. The "missing" electrons are used to charge up the channel.

On the other hand, M1 in Figure 3.1 is turning off. The inversion charge in its channel must be removed as transistor M1 moves towards accumulation. It can only accomplish this by ejecting it through its drain. This conclusion can be supported by realizing that in a differential pair the potentials at each node necessitate that the common terminals in M1 and M2 act as sources. We know that the source in an NMOS device always acts as a supplier of electrons and as current flows from source to drain. Due to the imposed potentials across the terminals of the differential pair electrons always end up ejecting out of the drain. As a result, the drain current of M1 should be higher than its source current.

To verify the conclusions presented in the above paragraphs a simulation of the differential pair was carried out using Spectre of Cadence. Figure 3.2 shows the difference in drain and source currents (I_D-I_S) of the switches M1 and M2, observed when simulating the pair.

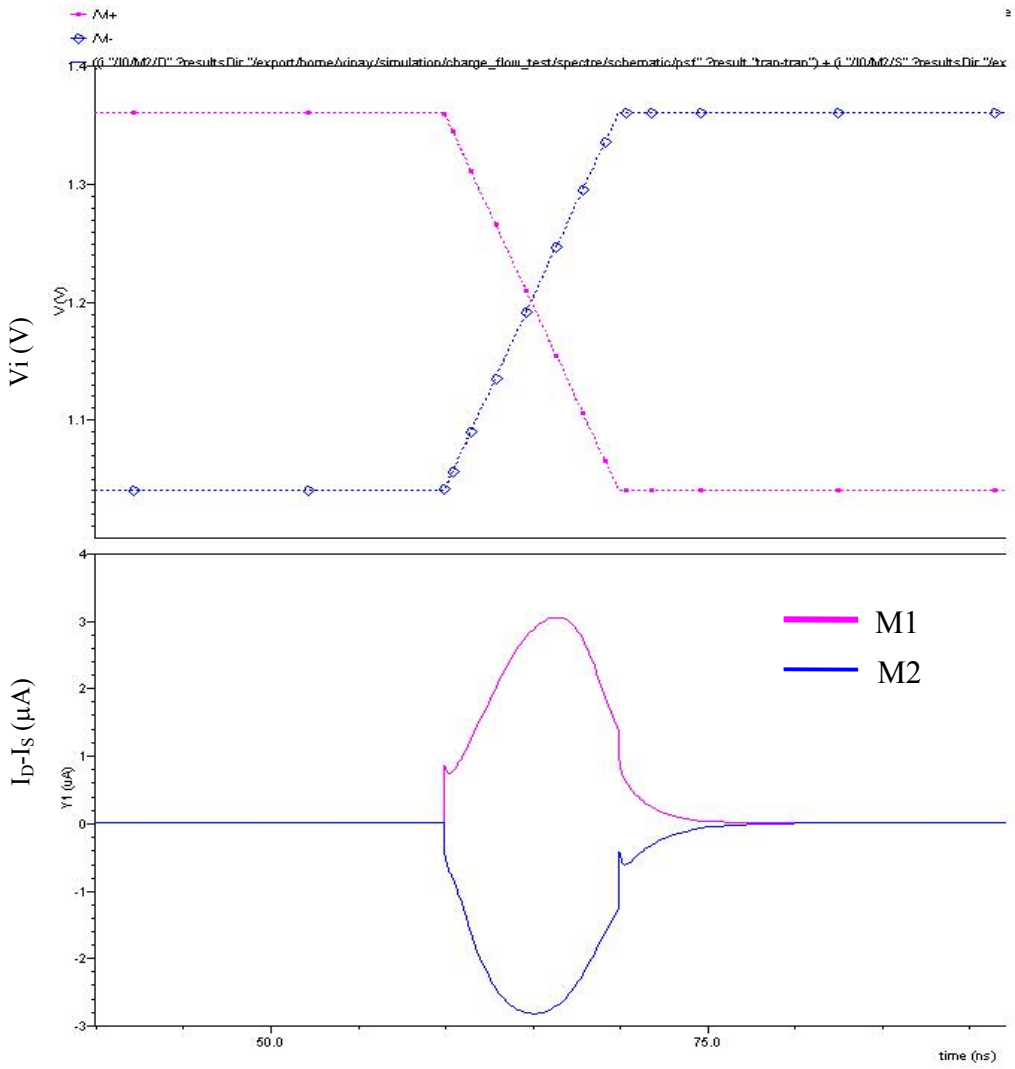


Figure 3.2 Simulation of differential pair

As observed in Figure 3.2, source current is higher than drain current in M2 as M2 is turning on. Doubling the widths and hence the currents while maintaining the same voltage bias conditions doubles the difference in drain and source currents, implying that double the charge is required to charge up the channel. This is consistent with the fact that charge in the channel doubles with a doubling of the width. After this initial transient phase, as observed in Figure 3.2, the difference in currents settles to zero during the steady state.

Conversely, the drain current is higher than the source current in the transistor which is turning off – M1 in this case. Thus, it is verified that channel charge escapes through the drain when the switch goes towards accumulation. This is bad news with respect to a charge pump because the loop filter is classically connected to the drain of the differential switch.

We know that the depletion region and inversion under the channel go away when the switch reaches the edge of accumulation. The depletion region is replenished by holes from drain. The net result being that negative charge is ejected from drain on to the filter capacitor.

It would be better if the switch is turned off to the extent that it remains in weak inversion but with *only* a negligible current compared with its allow able error.

The objective here is to develop a few guidelines with respect to the choice of widths and lengths of the devices so that charge in the channel is minimized. To accomplish this let us identify the parameters that constitute the total charge in the channel. It consists of two components:

- Body Charge, Q_b.

$$Q_b = \sqrt{4qN_A\varepsilon_{Si}\,|\,\phi_F\,|} \tag{3.1}$$

- Channel Charge, Q_{ch}

$$Q_{ch} = WLC_{ox}\Delta V \tag{3.2}$$

Let Q_{inj} the injected charge be a fraction of the total channel charge, Q_{ch} and body charge, Q_b that is injected due to the switching operation. Then, the error voltage due to this charge is given by equation(3.3).

$$\Delta V_{out,inj} = \frac{Q_{inj}}{C_{Loop}} \tag{3.3}$$

Worst case Q_{inj} is the sum of Q_b and Q_{ch}. For a given process Q_b is fixed. We have different processes – bulk, SOI, thin film SOI. The amount body charge as well as depletion region varies in these processes.

We control Q_{ch} by optimally selecting the dimensions of the switch. Assuming that the switch is turned on in saturation to minimize the channel charge as well as for other reasons to be explained in section 3.2.2 Assuming square law operation equation (3.2) can be written in the following form.

$$Q_{ch} = \frac{2}{3} WLC_{ox}\Delta V = \frac{2}{3} WLC_{ox}\sqrt{\frac{2I_D}{\beta}} = \frac{2}{3} WLC_{ox}\sqrt{\frac{2I_D L}{Wk_p}} \tag{3.4}$$

Since the current of the charge pump is decided by the loop factors of the PLL we can consider it as constant and conclude that

$$Q_{ch} \propto \sqrt{WL^3} \tag{3.5}$$

Based on equation (3.5) we can develop the following guidelines,

- Choose the minimum length possible. Decreasing length improves the switching speed but the lower limit is set by the minimum analog length allowable, set by channel length modulation, leakage and matching.
- Decreasing width improves the situation only by its square root, because, though we are decreasing the area we are increasing the ΔV for the same current. The lower limit is set by matching requirements to minimize offsets.

To have a better estimate of the amount of charge being injected while switches turn off, it is desirable to match the UP and DW switches. Equation for matching the currents in the two legs of a current mirror is given in equation(3.6) [6].

$$\sigma^2\left(\frac{\Delta I_d}{I_d}\right)=\sigma^2\left(\frac{\Delta\beta}{\beta}\right)+\frac{4}{(V_{GS}-V_{th})^2}\sigma^2(\Delta V_{th}) \tag{3.6}$$

Therefore, to improve matching one has to increase the overdrive voltage. Matching of currents is also essential for bringing UP and DW currents close to each other, given that there is still the effect of channel length modulation to account for.

3.2.2 Charge Sharing

Another cause of frequency spike or ripple is charge sharing. Charge sharing takes place across switches when ever V_{GS} changes potential. Parasitic capacitances C_{gd} and C_{gs} form a capacitor divider network which relays changes in the inputs to the output. This is conceptually depicted in Figure 3.3.

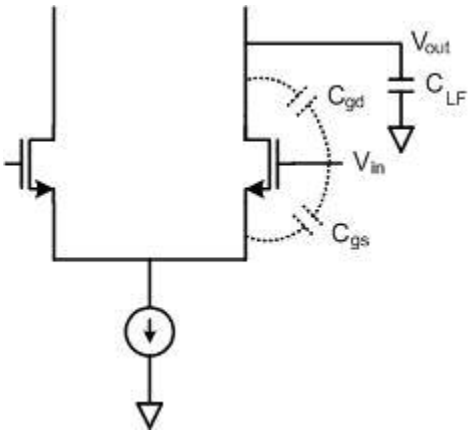


Figure 3.3 Parasitic Capacitances causing Charge Sharing

Changes in input voltage V_{in} are conveyed to the output through the parasitic capacitances shown in Figure 3.3. A relationship between the two is given in equation (3.7).

$$\Delta V_{out} = \Delta V_{in} \frac{C_{gd}}{C_{Loop} + C_{gd}} \approx \Delta V_{in} \frac{C_{gd}}{C_{LF}} \tag{3.7}$$

As seen from equation (3.7) to reduce fluctuations on the output voltage one should reduce the swing on the output and keep C_{gd} to a minimum. Again this speaks towards minimizing device width W. Both these objectives can be realized if we prevent the input to the charge pump from swinging rail to rail – which throws the switch into triode and increases C_{gd}, along with pushing ΔV_{in} to its maximum value. Again it is desirable to reduce W. Limiting the swing of the ensures that the switches turn on while keeping all devices in saturation and throughout both their switching period. C_{gd} is at its minimum during saturation keeping charge coupling to its minimum.

It is worthwhile to note here that using the topology shown in Figure 3.3 can lead to mismatch in the UP and DN currents due to channel length modulation effects. To improve the situation one has to increase the length of the transistors. This, however, leads to reduction in switching speed and also increase in C_{gd}.

One could use a cascoded structure as shown in Figure 3.4. This would allow us to use short channel devices. Adding a cascode device does not improve or improve the charge sharing situation if short channel devices were used in Figure 3.4 but does reduce the effects of channel length modulation on the UP and DW currents.

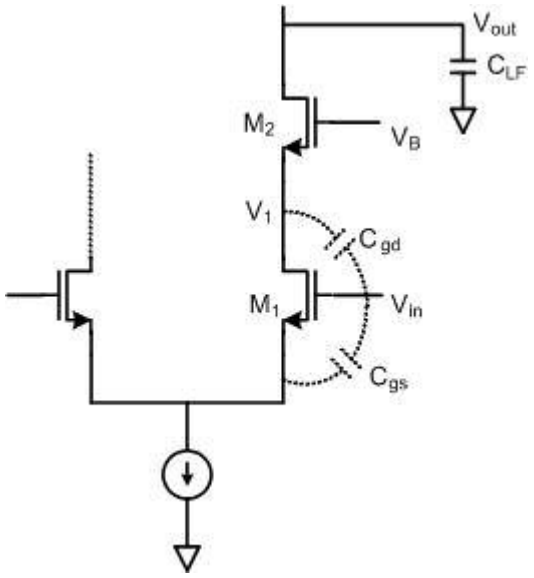


Figure 3.4. Using a Cascoded Architecture

3.3 "Frequency Jump"

The factors described in sections 3.2.1 and 3.2.2 contribute to an error charge which translates to a "frequency jump" of VCO clock. In other words this represents the closest we can get to a reference clock given a particular topology of a charge pump. To understand how this "frequency jump" comes to existence lets consider generic switch prevalent in charge pump topologies (refer to Section 3.4) shown in Figure 3.5.

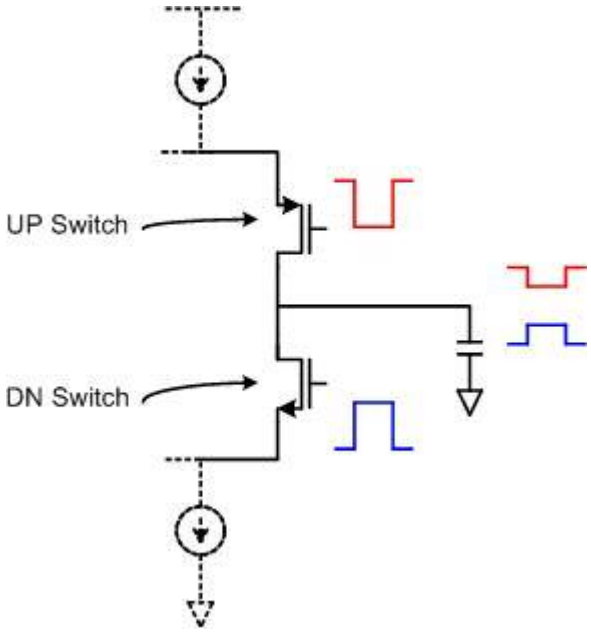


Figure 3.5 Generic Switch occurring in charge pumps

These switches are controlled by a Phase Frequency Detector (Chapter 5) which produces pulses as shown in Figure 3.5. Due to the charge sharing effect discussed in Section 3.2.2 a small disturbance occurs at the output of the charge pump. This deposits and then takes away charges at the positive and negative edges respectively. Therefore, the net effect on the output due to charge sharing is almost zero when both devices have matched C_{GD}. However at the negative edge the switch is turned off and charge injection occurs from the channel, depositing charges on the capacitor and thereby changing the frequency. This can be depicted pictorially as shown in Figure 3.6.

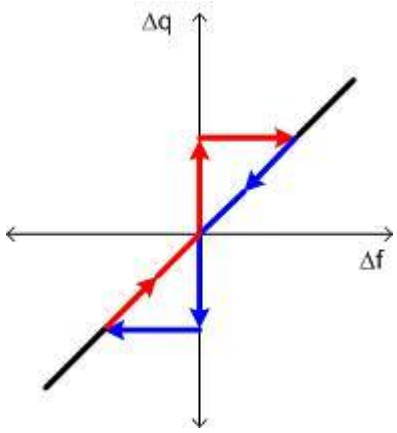


Figure 3.6 “Frequency Jump”

In Figure 3.6 Δf is the difference in VCO frequency and the Reference Frequency. Δq is the difference in positive charge (or holes) corresponding to the VCO frequency and the positive charge (or holes) corresponding to the Reference Frequency. Let us now assume that the VCO frequency is higher than the Reference Frequency (i.e. Δf is positive). Also let’s assume that the VCO frequency is directly proportional to the positive charge in the capacitor. The NMOS switch shown in Figure 3.5, which acts as DN switch of the charge pump, takes out holes or increases electrons when it is turned on using the pulse shown. At the negative edge, however, there is a jump in the total number of electrons due to charge injection by the NMOS switch. This reduces the total number of holes beyond the desired level resulting in a frequency jump – depicted by the arrows in blue in Figure 3.6. The PLL tries to increase the frequency by producing an UP pulse. If we assume the UP switch is a PMOS as shown in the Figure 3.5 then holes or positive charges get deposited on the loop filter when the switch is turned on. When, the PMOS switch is turned off there is an injection of extra holes and the frequency change follows the red curve shown in Figure 3.6.

The "frequency jump" can be quantified by using the equation**Error! Reference source not found.**. The error charge due to charge injection, Δq_{Err}, can be written as in equation(3.8).

$$\Delta q_{Err} = C_{LF} \Delta V_{out,inj} \tag{3.8}$$

$$\Delta V_{Err} = \frac{\Delta q_{Err}}{C_{LF}} \tag{3.9}$$

C_{LF} is the loop filter capacitor. The corresponding frequency error Δf_{Err} is can then be given by equation(3.10).

$$\Delta f_{Err} = \Delta V_{err} K_{VCO} \tag{3.10}$$

K_{VCO} is the sensitivity of the VCO in *Hz/V*.

3.4 Overview of Topologies of Charge Pump

3.4.1 Switch at Drain

A Charge Pump with switch connected to the drain of the current source is shown in Figure 3.7.

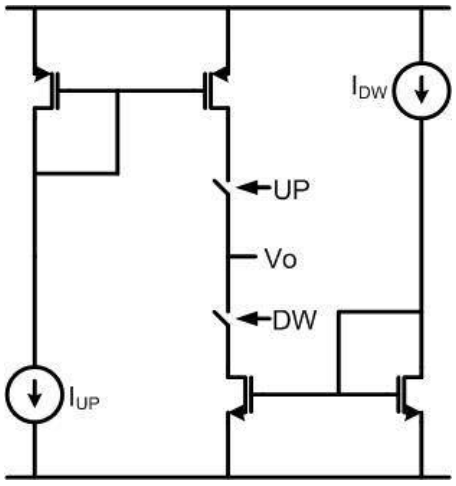


Figure 3.7 Charge Pump with Switch at Drain

When the UP switch is turned on the current I_{UP} is mirrored through M4 and M2 and pumped into the output capacitor increasing its voltage. Turning on the DW switch mirrors the current I_{DW} through M3 and M1 to the output and capacitor is discharged, decreasing the voltage.

This charge pump circuit shown above has many limitations. Problems of charge injection and charge sharing are obvious. UP and DW currents can differ due to channel length modulation effect. Also, when both the switches are turned off, the voltage at capacitor C is left floating, while the voltages at the drains of M2 and M1 are rapidly pulled to VDD and ground respectively. When one of the switches is turned on charge sharing takes place between the capacitor of the filter and the capacitor at the drain nodes. This results in a jump or spiking of the voltage of the loop filter capacitor.

3.4.2 Switch at Source

Figure 3.8 shows a charge pump with the switch connected to the source of the current source.

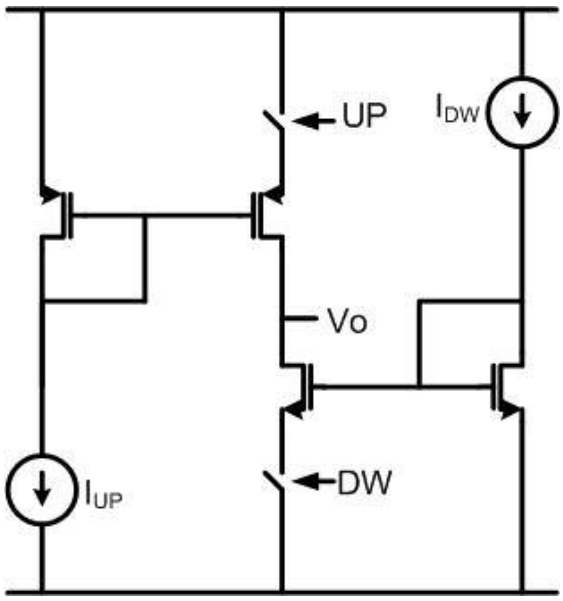


Figure 3.8 Charge Pump with switch at Source

With the switch connected at the source, charge injection problems are avoided to some extent. Switches DW and UP see a resistance of $1/g_m$ towards their drain due to the cascoding transistors M1 and M2, Figure 3.9. Therefore the charges tend to flow into the power rails where they face less resistance. Also, as discussed in section 3.2.2, cascoding also reduces charge sharing. Figure 3.10 shows the complete schematic with switches at the source [13]. M_4 and M_3 act as switches instead of M_2 and M_1. Hence, when compared with switch at drain in Figure 3.7 this topology does a better job of avoiding the problem of charge sharing and charge injection. Still, the problem of charge injection exists when M1 or M2 turn off.

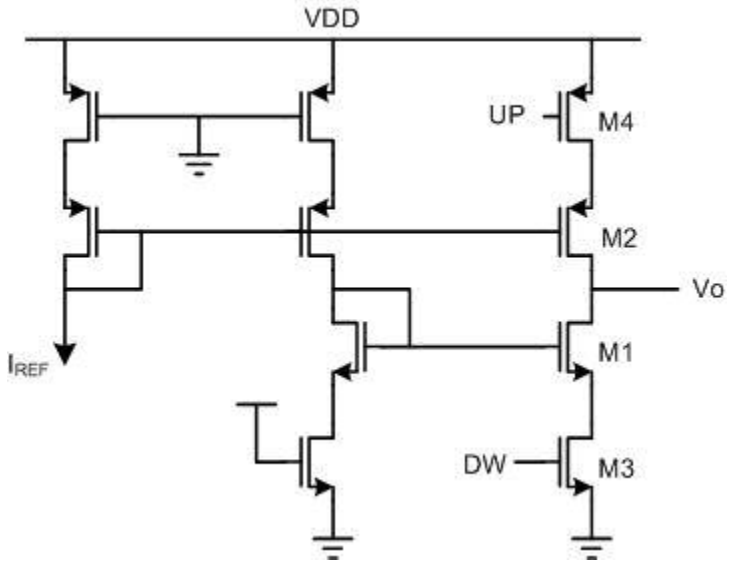


Figure 3.10 Complete Schematic of a Switch at Source

Figure 3.10 however suffers from long fall time of current pulses because of large impedances seen at the sources of M_2 and M_1 when they are off. During this period their overdrive voltages become very small. The topology shown in Figure 3.11, proposed by Chih-Ming et al, [14] seeks to remove this shortcoming.

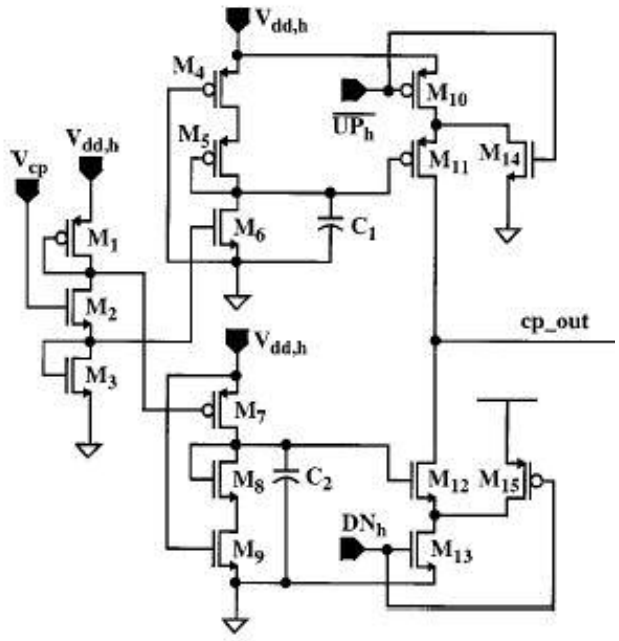


Figure 3.11 Charge Pump Proposed by Chih-Ming et al

Transistors M_1, M_2 and M_3 form a current reference. V_{cp} is mostly connected to V_{DD}. The current is copied by M_6, M_5 and M_9, M_8. Transistors M_4 and M_9 are added for accurate copying of current to the transistors forming the actual charge pump (M_{10}, M_{11}, M_{12} and M_{13}). Glitches due to the switching of M_{10} and M_{13} are absorbed at the sources of M_{11} and M_{12} and are not conveyed to the output as the latter are still off [14]. M_{11} and M_{12} are softly turned on due to the time constants seen at their sources. This minimizes charge injection. Transistors M_{14} and M_{15} improve the switching time constant of the switches M_{10} and M_{13} by provided extra charging/discharging paths. The 10pF bypass capacitors C_1 and C_2 help attenuate glitches as they provide additional paths to ground [14].

This architecture, however, still has the problem of mismatches between UP and DW switches. The UP switch is implemented as a PMOS and the DW switch is implemented as NMOS. Also, channel length modulation effects can lead to a difference in UP and DW current.

3.4.3 Current Steering Charge Pump

The problems of Switch at Drain topology shown in Figure 3.7 can also be mitigated to an extent by introducing an op amp as shown in Figure 3.12 [8]. It is a current steering charge pump which implements the UP switch with PMOS and DW switch. The op amp serves to avoid channel length modulation effects by keeping the drain voltages at equal values thereby reducing disparity in UP and DW currents. The op amp also stabilizes the voltages at the two points thereby preventing the jump phenomenon as discussed in section 3.4.1.

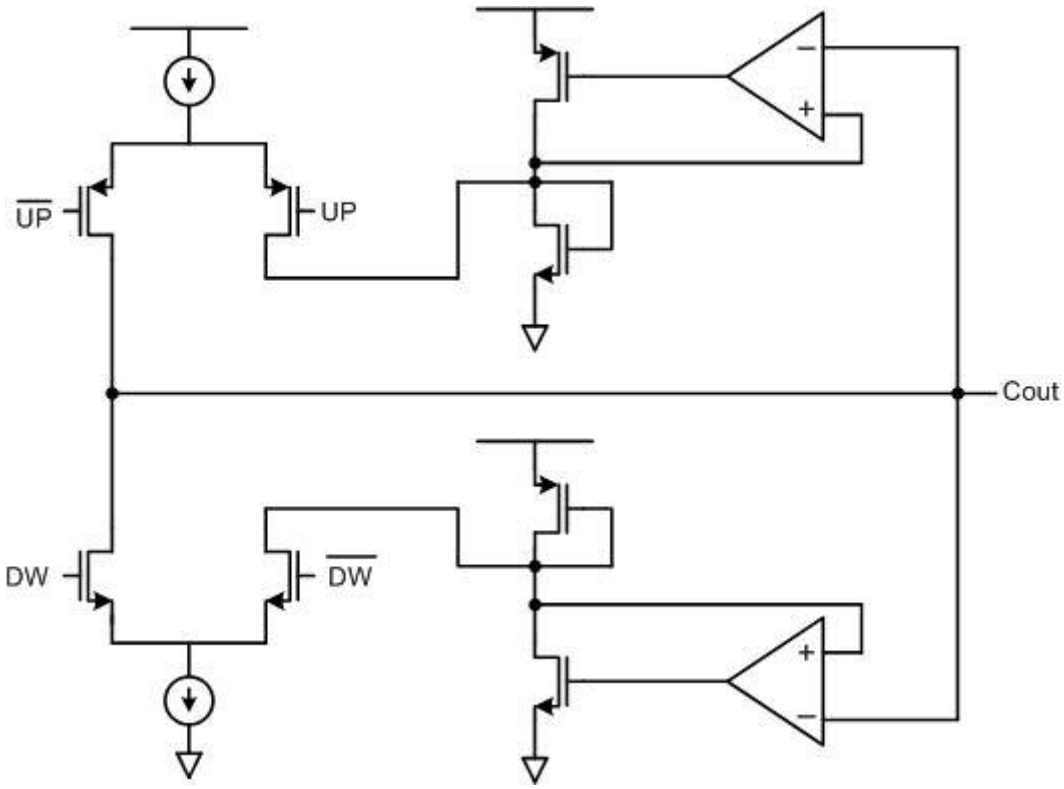


Figure 3.12 Current Steering Charge Pump suggested by Chen et al

However in this case matching the UP and DW switches is a problem. Also, just like the switch at drain topology discussed in section 3.4.1 the problems of charge injection and charge sharing are present.

Figure 3.13 shows a topology [9] which achieves almost the same performance as that in Figure 3.12 but uses less area and power. It employs only one op amp in unity gain configuration.

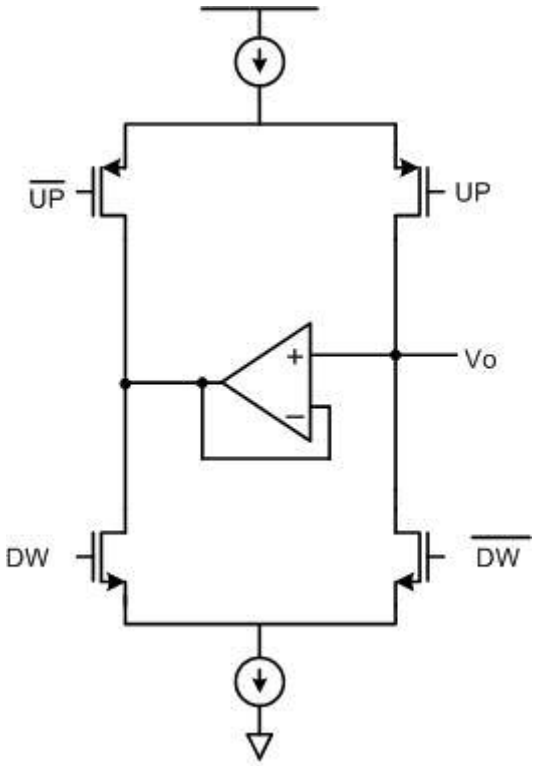


Figure 3.13 Current Steering Charge Pump suggested by Young et al

The topology of Figure 3.13 still suffers from the problems of charge injection and charge sharing. Arshak et al [10] proposes the placement of dummy switches M3, M4, M5 and M6 shown in Figure 3.14 to ameliorate these problems.

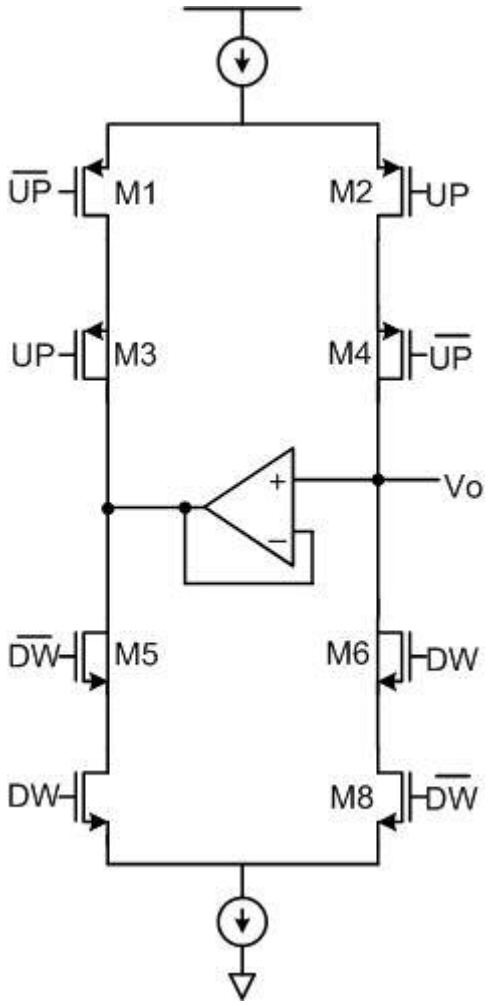


Figure 3.14 Switches at Drain with Dummy Switches

However, in the above discussed topology, switching time of the UP and DW switches varies due to the use both N and PMOS types of MOS devices.

Topology shown in Figure 3.15 achieves better matching between the turn on time of UP and DW switches since it uses NMOS devices for implementing them. A schematic for understanding this type of charge pump is shown in Figure 3.15 [11].

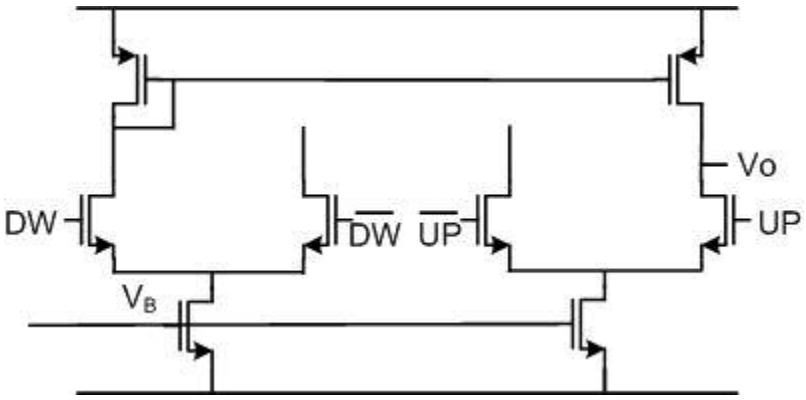


Figure 3.15 Current Steering Charge Pump suggested by Maneatis et al

This topology has two source coupled pairs. The left pair comes into play when DW signal is high and the right pair comes into play when UP signal is high. Owing to the current mirror, charge will be transferred to the loop filter when DW signal is high. Capacitor charge will be depleted when UP signal is high. The current mirror will not be active during this period. However, it does provide a leakage path that is near constant and puling up. A complete schematic is shown in Figure 3.16 [11].

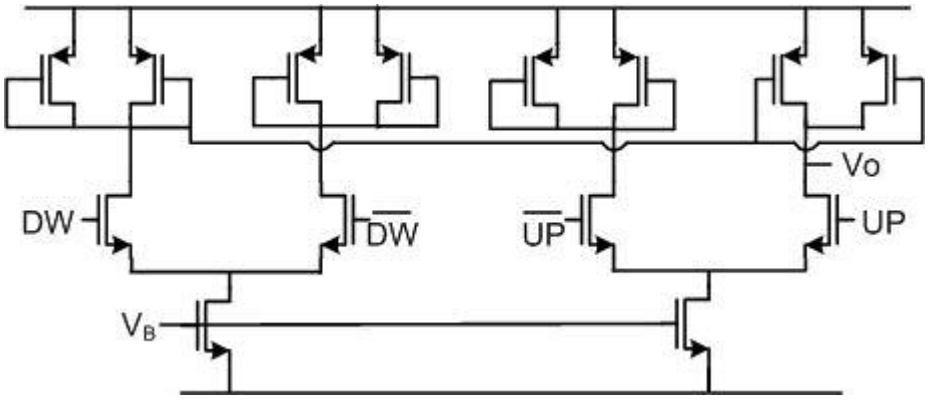


Figure 3.16 Complete Schematic of Current Steering Charge Pump suggested by Maneatis et al

As can be observed from the Figure 3.15 that matching is readily obtained between UP and DW switches. Matching is reduced to having sufficient area. When

compared with Figure 3.11 where one is required to take in consideration the differences in mobility in addition to area.

Figure 3.17 shows a charge pump suggested by Chang et al [12]. This topology also helps achieve matching between the UP and DW switches just like the topology in Figure 3.15. However, Figure 3.17 still has the problem of charge sharing. Also, when compared with the topology in Figure 3.15 it has a longer delay time constant in its DW path.

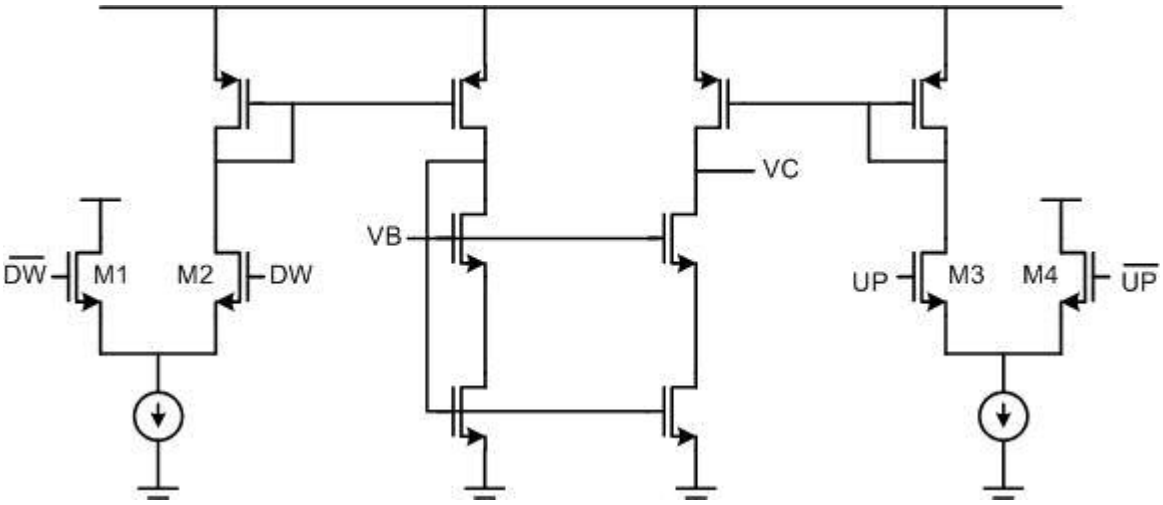


Figure 3.17 Current Steering Charge Pump suggested by Chang et al

3.5 Proposed Topology

Figure 3.18 shows the topology selected. It is essentially an improved version of the topology of Figure 3.16. As discussed in 3.2.2, cascoding the switches reduces the channel length modulation effects. Also, a swing limiting circuit is added to it to limit the changes in the inputs which again, as discussed in section 3.2.2, reduces charge sharing and injection.

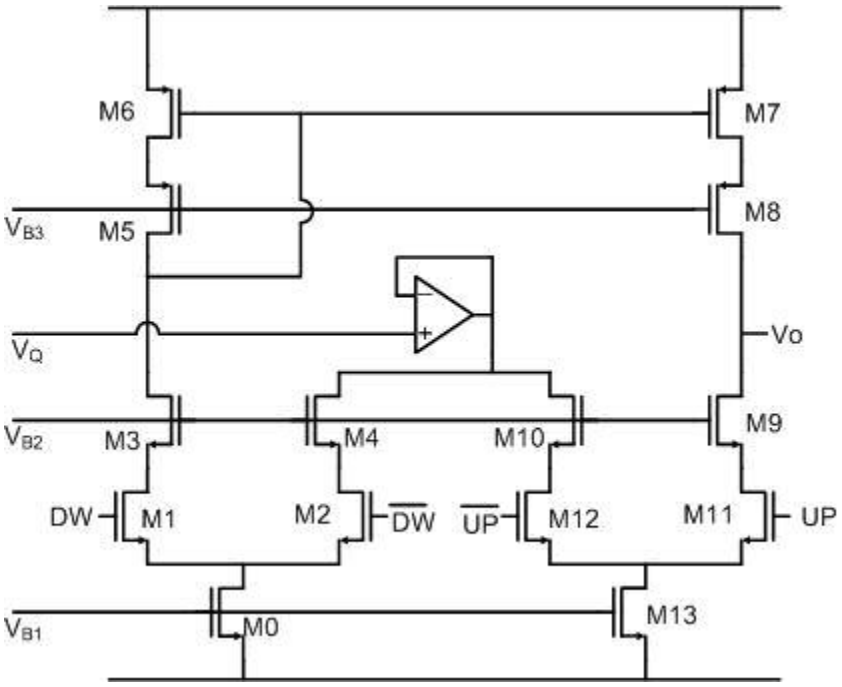


Figure 3.18 Proposed Topology

Under quiescent conditions, the output settles at an operating point (V_Q) and moves around this point. The op amp connected in a unity gain mode helps maintain the drains of transistors M4 and M10 at this point. This op amp is a simple single ended differential pair shown in Figure 3.19. The down side is the high VDD or high headroom requirement.

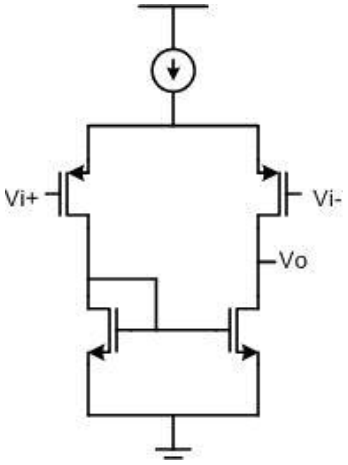


Figure 3.19 Op Amp used in the Proposed Topology

Following the discussion in section 3.3, since the VCO frequency is inversely proportional to the positive charge in the loop filter capacitor and also due to the fact that when DW switch is turned off electrons are mirrored and injected to the loop filter capacitor Figure 3.6 can be redrawn as shown in Figure 3.20.

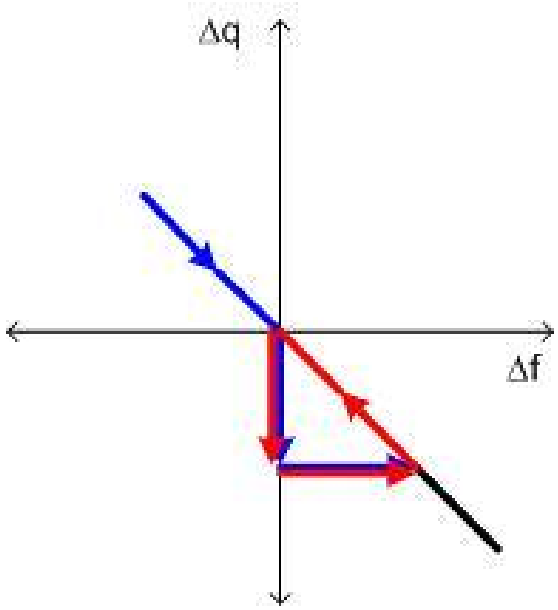


Figure 3.20 "Frequency Jump" in the proposed topology

Where the blue line represents the change when UP switch, of Figure 3.18, is turned on and off. Red line represents the time when DW switch is turned on and off. As is evident from the Figure 3.20 the "Frequency Jump" is reduced to half of the value in Figure 3.6.

The problem of headroom can be lessened by introducing an Op Amp as shown in Figure 3.21. It is a NMOS differential pair.

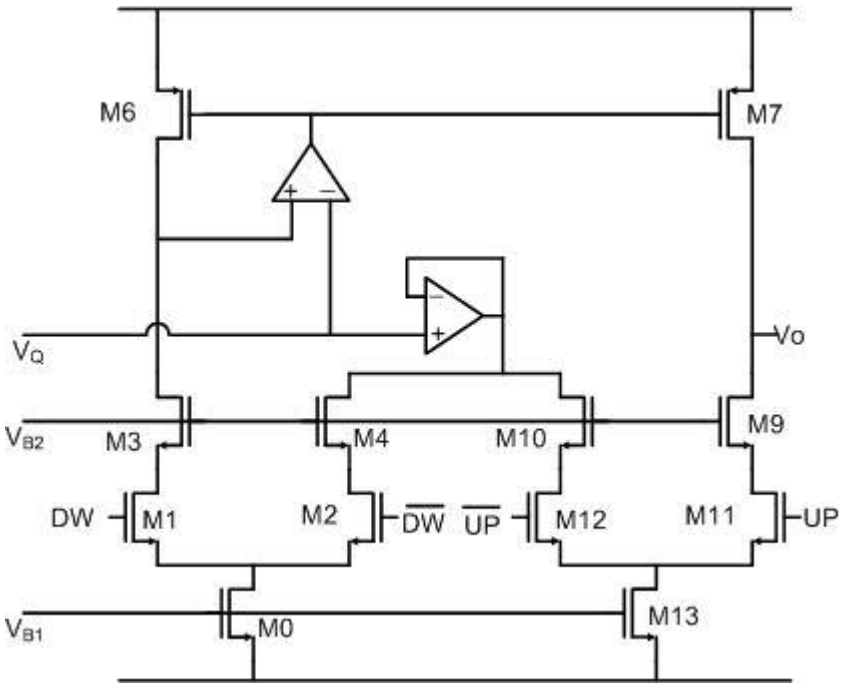


Figure 3.21 Improving headroom available constraint

3.5.1 Swing Limiting Circuit

A swing limiting circuit has the job of limiting the swing on the inputs of the charge pump so that the problems of charge sharing are a bit alleviated. The upper level of the swing is limited such that the switches (M1, M2, M11 or M12 of Figure 3.18) turn on in saturation for reasons discussed in 3.2.1 and 3.2.2. For reasons discussed in 3.2.1, the lower level is decided so that the switches turn off to the extent that the switches remains in weak inversion but with *only* a negligible current compared with an allowable error.

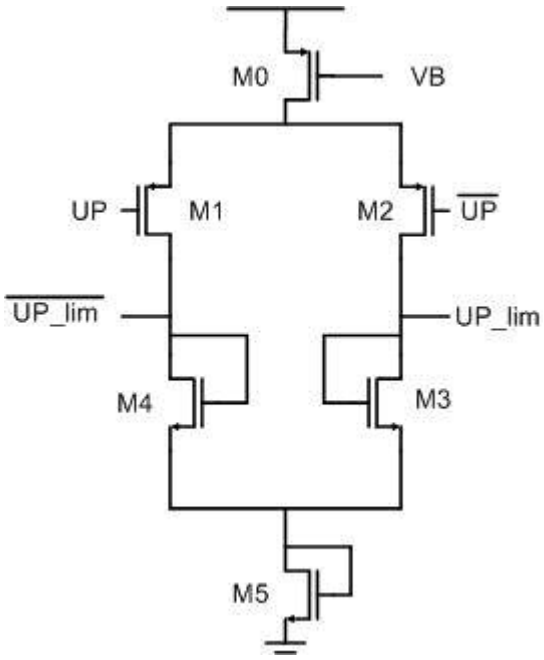


Figure 3.22 Swing limiting circuit

Figure 3.22 shows the swing limiting circuit that can be employed. Note the V_{GS5} voltage can be controlled by an OTA similar to that of Figure 3.19 to further improve accuracy.

Output swings of Figure 3.22 are shown in Figure 3.23. The swings are represented in terms of the ΔV of the charge pump in Figure 3.18.

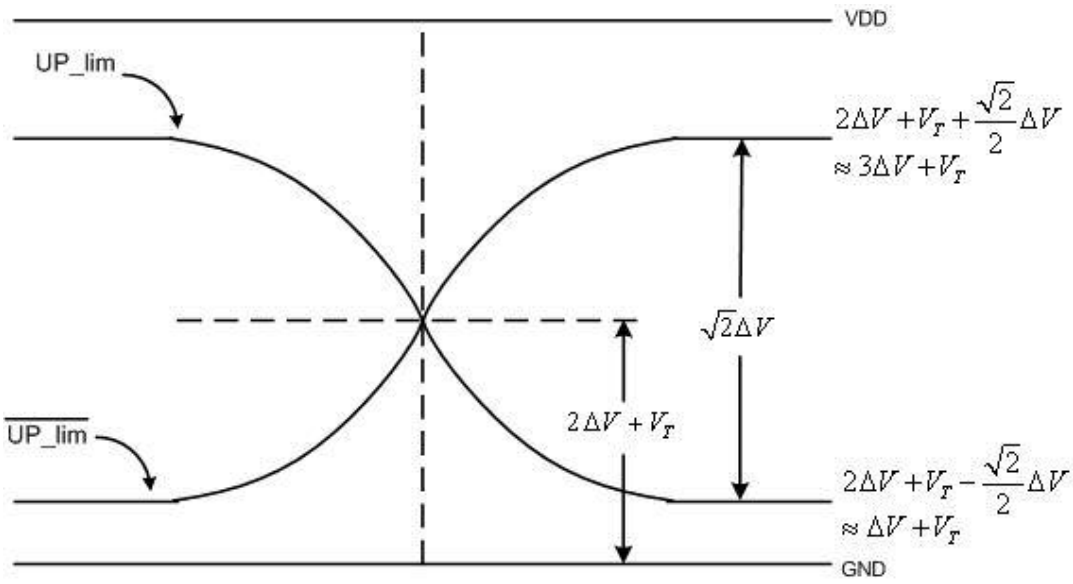


Figure 3.23 Outputs Swings of the swing limiting circuit

To turn on the switch in saturation the final output level of the circuit should be at least $2\Delta V+V_T$. To completely switch the current from one branch to the other the difference in the levels of the two outputs should be greater than $\sqrt{2}\Delta V$.

Figure 3.24 shows the output of the charge pump of Figure 3.18 when only the DW signal is active. DW comes in the form of pulses. In the presence of a pulse there is an increase in the loop filter voltage indicated by the ramp. In the absence of the pulse the voltage remains approximately constant. An increase in the loop filter voltage decreases the frequency since frequency is inversely proportional to the control voltage in the selected topology of the VCO. Figure 3.25 shows the output when only the UP signal is active. UP signal effects a decrease in the loop filter voltage increasing the frequency because.

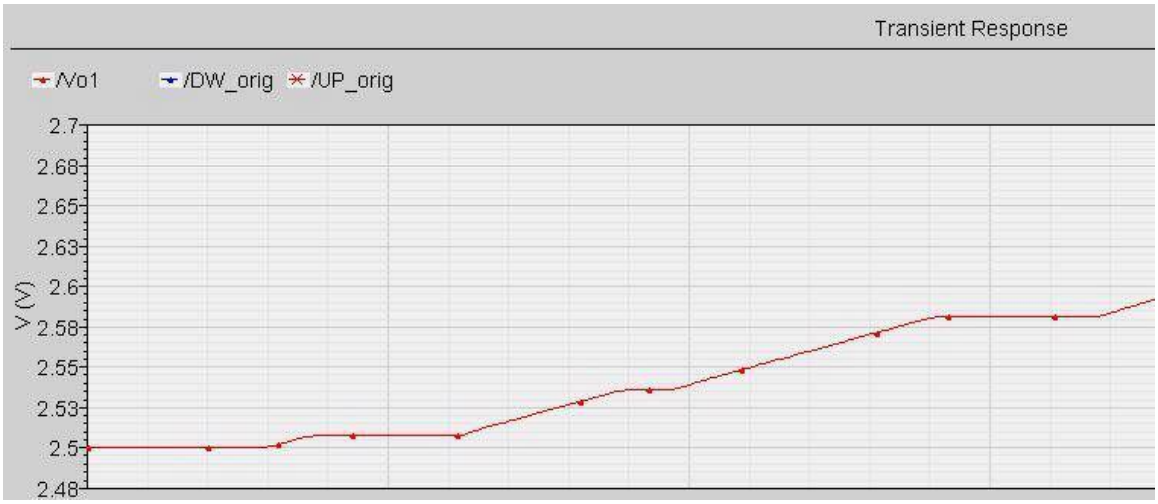


Figure 3.24 Output Voltage of the Charge Pump when DW signal is active

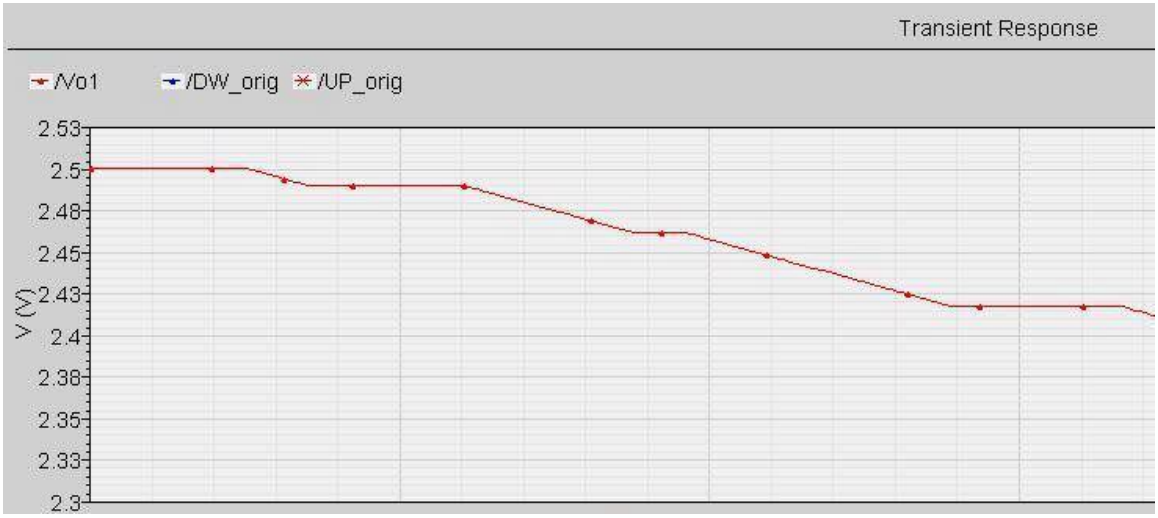


Figure 3.25 Output Voltage of the Charge Pump when UP signal is active

Chapter 4

Voltage Controlled Oscillator

4.1 Introduction

A Voltage Controlled Oscillator changes its frequency of Oscillation based on a voltage control applied to it. It is basically a CMOS ring oscillator which has several stages connected in a loop. The applied control changes the bandwidth or delay through each stage of the oscillator which in turn changes the frequency of oscillation.

The Barkhausen requirement for an oscillator to sustain oscillations is that it should have a gain of greater than one and a phase shift of 360° around the loop. In the case of an oscillator with single ended topology an odd number of stages give a DC phase shift of 180°. The remainder of the 180° phase shift is voltage dependent, i.e., at a frequency decided by the bias conditions of the stages in the oscillator the total phase shift around the loop becomes 360°. This frequency becomes the oscillation frequency of the oscillator. By changing the bias conditions on the oscillator stages the delay can be varied and thereby the oscillation frequency.

$$f_{osc} = \frac{1}{2N\tau_d} \tag{4.1}$$

In a differential ring oscillator the 180° DC phase shift can be attained with the help of even number of stages by swapping the feedback lines. An even number of stages is particularly useful for obtaining quadrature signals. The choice of the number of stages affects the amount of power consumed and also the frequency of operation. Using a fewer number of stages increases the frequency of operation and the power consumption along with it. The effect of an increase in frequency on power consumption may get mitigated to some extent by the decrease in the number of stages. As the number of stages go down it also becomes increasingly difficult to get the required gain and phase shift from each stage.

Consider a four-stage differential ring oscillator as shown in Figure 4.1.

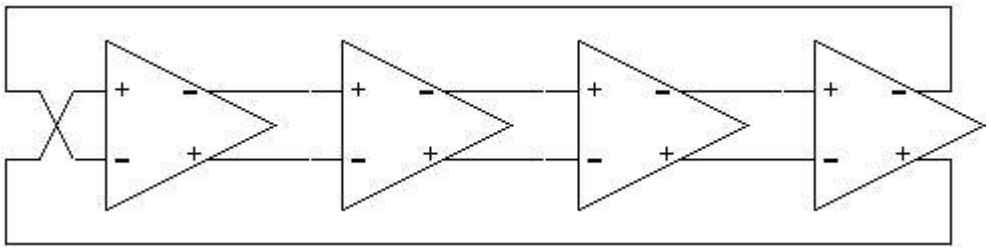


Figure 4.1 Four Stage Differential Ring Oscillator

The transfer function of each stage may be approximated, by neglecting the gate to drain overlap capacitance, as shown in equation(4.2).

$$-\frac{A_0}{1+\frac{s}{\omega_0}} \tag{4.2}$$

The total loop gain can now be written as

$$H(s) = \frac{A_0^4}{\left(1 + \frac{s}{\omega_0}\right)^4} \tag{4.3}$$

Oscillations occur if the total phase shift around the loop is 360°. The total frequency dependent phase shift should be 180°. The balance of the phase shift is provided by the negative feedback of the four stages. Hence, with four stages, then the phase shift introduced by each stage is 45° i.e.

$$\tan^{-1}\left(\frac{\omega_{osc}}{\omega_{3dB}}\right) = 45^\circ \left(= 180^\circ / 4\right) \tag{4.4}$$
$$\text{i.e. } \omega_{osc} = \omega_{3dB}$$

Therefore, in a four stage oscillator the oscillation frequency is equal to the bandwidth of a single dominant pole stage. This simplifies the design greatly because the desired frequency of operation can be achieved by adjusting the bandwidth of a single stage.

Not only does the Barkhausen require the total phase shift around the loop to be 360° but also the minimum gain at the frequency of oscillation should be greater than or equal unity. i.e.

$$\frac{A_0}{\sqrt{1 + \frac{\omega_{osc}}{\omega_{3dB}}}} = 1 \Rightarrow A_0 = \sqrt{2} \tag{4.5}$$

Therefore, the minimum gain per stage should be around 1.414 to ensure oscillators. Generally, the minimum gain is designed to be much greater than this to account for process and temperature variations.

As can be seen, selecting the number of stages as four, simplifies the design of a ring oscillator. Frequency of operation is simply equal to the bandwidth of a single stage.

4.2 Overview of Topologies

4.2.1 Single-Ended Topologies

Single ended topologies are implemented as either a shunt capacitor or as current starved inverters. These topologies have full swing outputs. Hence, they have high SNR. They also have fewer intrinsic noise contributing devices.

4.2.1.1 Shunt Capacitor Inverter

A shunt capacitor inverter topology is shown in Figure 4.2 [15]. In this topology the output time constant is varied by varying the resistance of the shunt transistor. The capacitor is usually implemented using a MOS device.

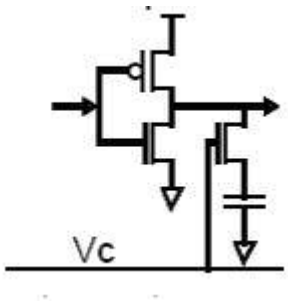


Figure 4.2. Shunt Capacitor Inverter

Matching of the resistor and the capacitor is an issue. Also, the capacitor, which is most frequently implemented using a MOS device, may take up large area for low frequency designs.

4.2.1.2 Current Starved Topology

Figure 4.3 shows a current starved topology [16]. Change in frequency is achieved by varying the delay by limiting the current through the inverter.

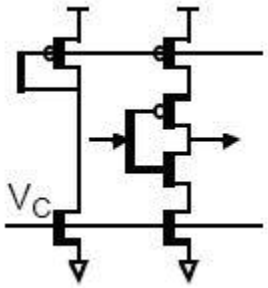


Figure 4.3 Current Starved Inverter

Single ended topologies, however, have the problem of being susceptibility to supply- voltage variation and even order harmonic distortion. In other words, these topologies have low PSSR.

4.2.2 Differential Topology

A differential topology reduces the effect of common mode noise and the magnitude of current spikes injected into the VCO from the power supply and the substrate. Their ability to reject common mode noise results in high PSSR.

While deciding on the topology, however, we have to make sure that the loads of the differential cell remain linear during the operation of VCO. Nonlinearities in a VCO cell cause the up-conversion of low frequency noise [17]. This can be averted by choosing a load which has a linear relationship between voltage and current. In other words the load should act like a linear variable resistor.

4.2.2.1 Loads in Triode

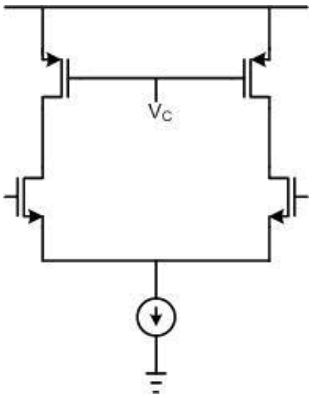


Figure 4.4 Differential Pair with Triode Loads

A MOS device biased in triode behaves like a linear resistor. For small drain to source voltages compared to its gate to source bias its drain current is approximately directly proportional to its drain-source voltage. Figure 4.4 shows a differential pair with MOS loads. Its control voltage V_C can be adjusted to bring it into triode. Resistance of the MOS can also be varied by changing V_C. The disadvantage of using a triode load, however, is low gain.

4.2.2.2 Loads in Saturation

The differential pair of Figure 4.4 can be biased in saturation by adjusting the voltage V_C. When the load is in saturation we achieve the maximum gain as a result of the high output resistance. However, there is reduced swing of the output at higher overdrive voltages.

4.2.2.3 Maneatis Load [18]

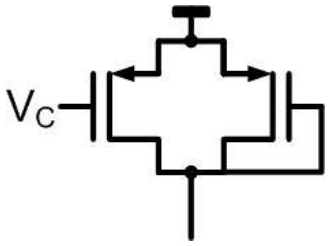


Figure 4.5 Load for the Differential Pair suggested by Maneatis [18]

The load suggested by Maneatis [18] is shown in Figure 4.5. It consists of a diode connected MOS device and a current source connected in parallel. This combination has an I-V characteristic as shown in Figure 4.6.

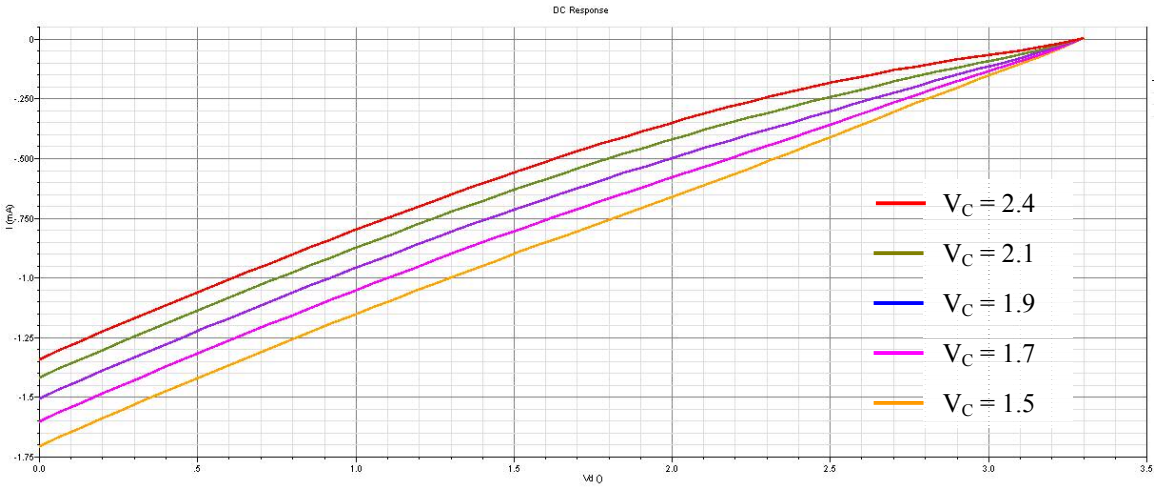


Figure 4.6 Simulated Characteristics of Maneatis Load

As is implied by Figure 4.6 the characteristics are approximately linear. This load also maintains sufficient gain and swing.

4.3 Selected Topology

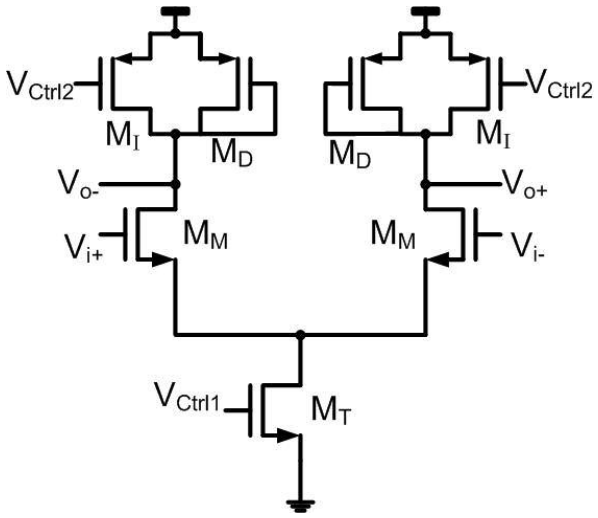


Figure 4.7 Differential Pair with Maneatis Loads

The selected topology uses a differential amplifier with MOS diode loads [19]. A PMOS current source is also connected in parallel with the diode load. This combination of diode and current source provides a near linear load [19]. It acts as a variable resistor whose resistance can be changed with the help of a control voltage connected to the current source. Variation in resistance translates to variation in the frequency of oscillation.

4.3.1 Expression for Gain and Oscillation Frequency

The small signal model of Figure 4.7 is shown in Figure 4.8.

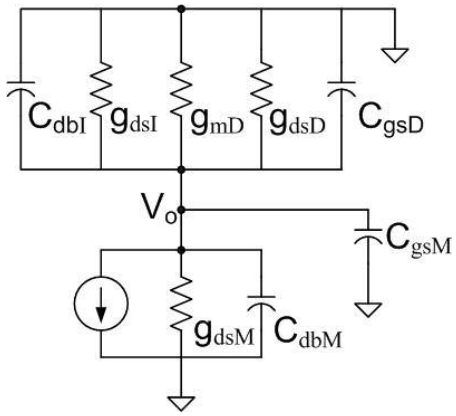


Figure 4.8 Small Signal Model of the differential pair

Using Figure 4.8 one can derive the transfer function as

$$\frac{V_o}{V_i} = -\frac{\dfrac{g_{mM}}{g_{mD} + g_{dsM} + g_{dsI} + g_{dsD}}}{1 + s\left(\dfrac{C_{gsM} + C_{gsD} + C_{dbM} + C_{dbI}}{g_{mD} + g_{dsM} + g_{dsI} + g_{dsD}}\right)} \tag{4.6}$$

Equation(4.6) can be written in the following form

$$H(s) = -\frac{A_0}{1 + \dfrac{s}{\omega_0}} \tag{4.7}$$

Where A_0 is the gain of the differential pair and is given in equation(4.8) and ω_0 is the 3dB frequency of the differential pair and is given in equation(4.9).

$$A_0 = -\frac{g_{mM}}{g_{mD} + g_{dsM} + g_{dsI} + g_{dsD}} \tag{4.8}$$

$$\omega_0 = \omega_{3dB} = \frac{g_{mD} + g_{dsM} + g_{dsI} + g_{dsD}}{C_{gsM} + C_{gsD} + C_{dbM} + C_{dbI}} \approx \frac{g_{mD}}{C_{gsM} + C_{gsD}} \tag{4.9}$$

From equation(4.9), where g_{mD} equal $\beta\Delta V_D$, we can conclude that the oscillation frequency is *approximately* proportional to ΔV_D, the overdrive voltage of the diode. Hence, the frequency can be varied by varying ΔV_D.

4.3.2 Bias Circuit for the Differential Pair

Control voltages V_{ctrl1} and V_{ctrl2} in Figure 4.7 are generated from a bias circuit shown in Figure 4.9.

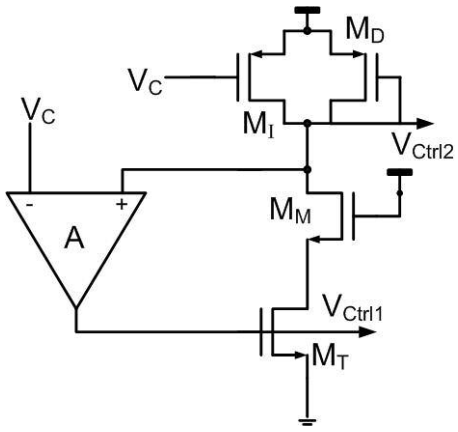


Figure 4.9 Bias Circuit for the Differential Pair of Figure 4.7

The Bias Circuit generates the control voltages from the voltage V_C, which comes from the loop filter. Amplifier A continually adjusts V_{Ctrl1} which is the gate voltage of M_T. This adjusts the current through M_T so that V_{Ctrl2} closely follows V_C. The complete circuit of the bias circuit is shown in Figure 4.10.

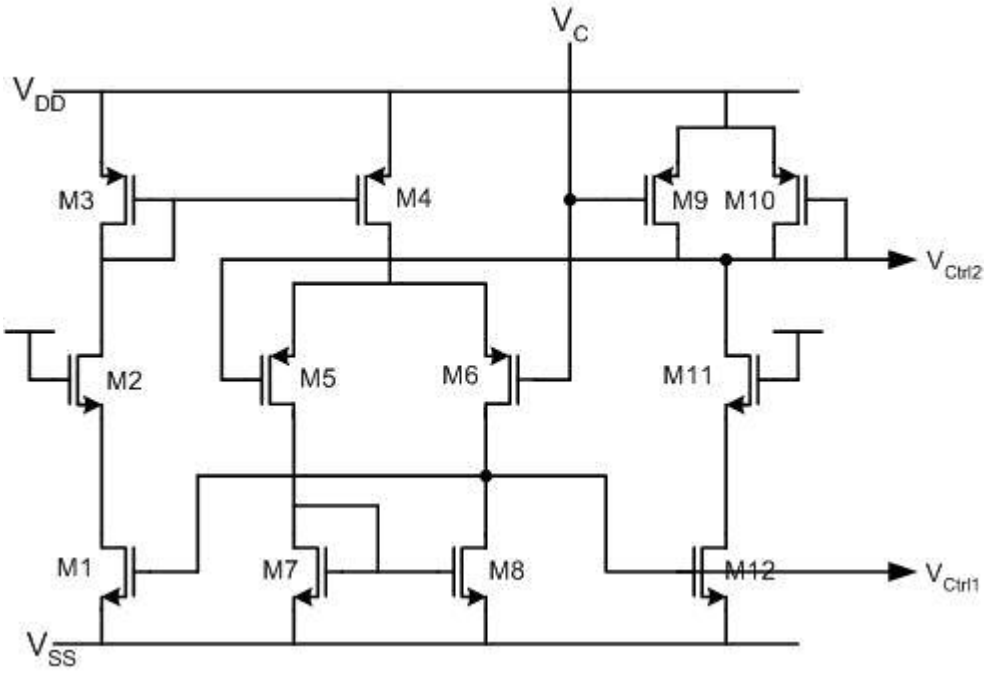


Figure 4.10 Complete Schematic of the Bias Circuit

Figure 4.11 shows the transistor level details of the amplifier *A* in Figure 4.9 including its bias circuit. Transistors M_1, M_2 and M_3 form its bias circuit. They continually adjust the bias of the current source M_4 so that the circuit chooses its ΔV based on the control voltage V_C. The voltages V_{Ctrl1} and V_{Ctrl2} are also generated accordingly.

M1	W_{nl} / L_l	M7	W_p / L
M2	W_{nl} / L	M8	W_p / L
M3	W_{pl} / L_l	M9	$(1/8)(W_p / L)$
M4	$2W_{pl} / L_l$	M10	$(1/8)(W_{pl} / L_L)$
M5	W_p / L	M11	W_n / L
		M7	W_p / L

Table 4.1. Geometries of the transistor in Figure 4.10

4.4 Test Results

4.4.1 Test Setup

Figure 4.11 shows the test setup bed for testing the Differential Pair of Figure 4.7 along with its Bias Circuit.

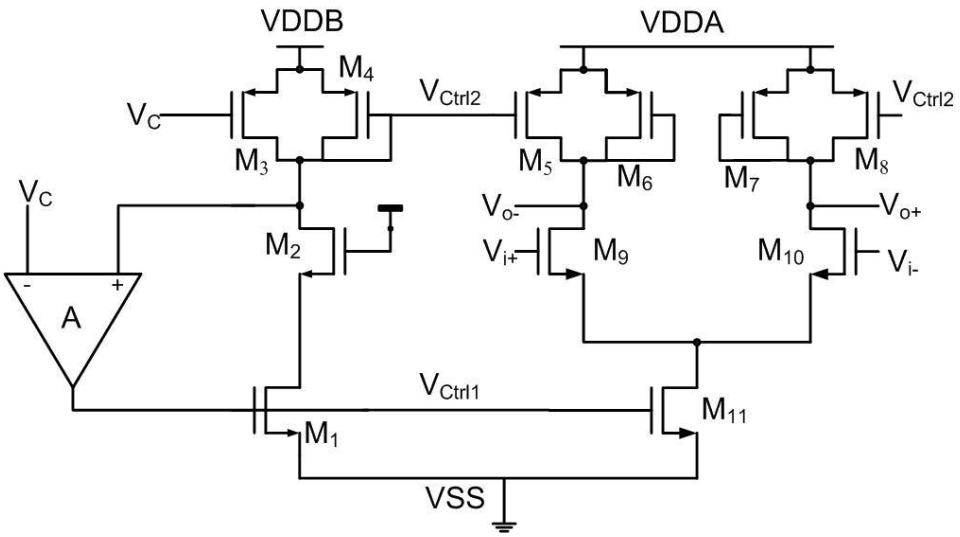


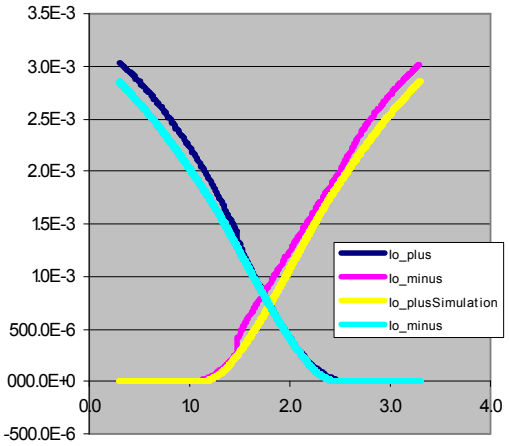
Figure 4.11 Test Setup

Bias Circuit and Differential run on different V_{DD} supplies but they have a common V_{SS}. The outputs V_{o+} and V_{o-} were padded out. Inputs V_C, V_{i+} and V_{i-} were also padded out.

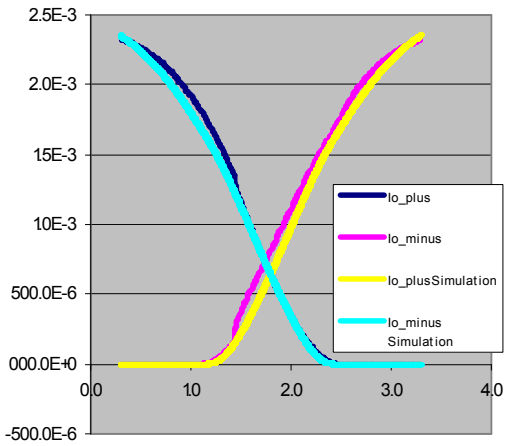
4.4.2 Tail Current Test

To test the tail current of the differential pair of Figure 4.11, VDDA was disconnected from the supply. VDDB and VSS were however connected to the supply. Differential inputs were applied to V_{i+} and V_{i-} and currents at V_{o-} and V_{o+} were measured using a Keithley 4200 Semiconductor Parameter Analyzer.

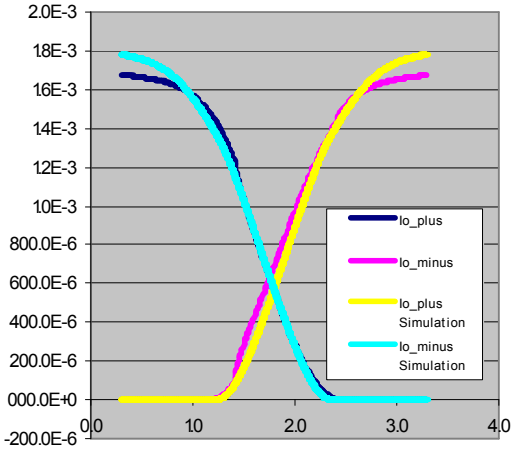
Results of the measurements done are shown in figure 3. Test results show a decrease in current in the differential pair as the control voltage V_C is increased. This decrease in current is attributed to the kink effect present in Peregrine transistors [6].



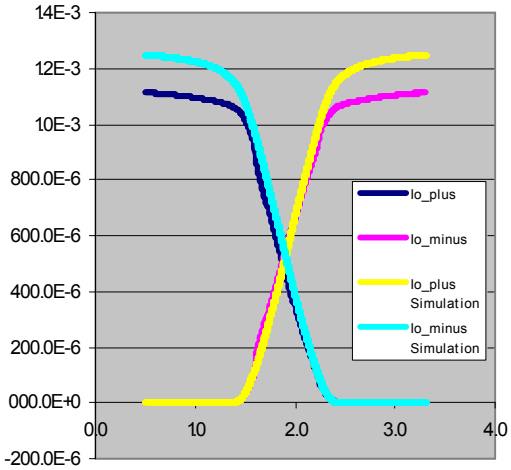
(a) $V_C = 0.9$



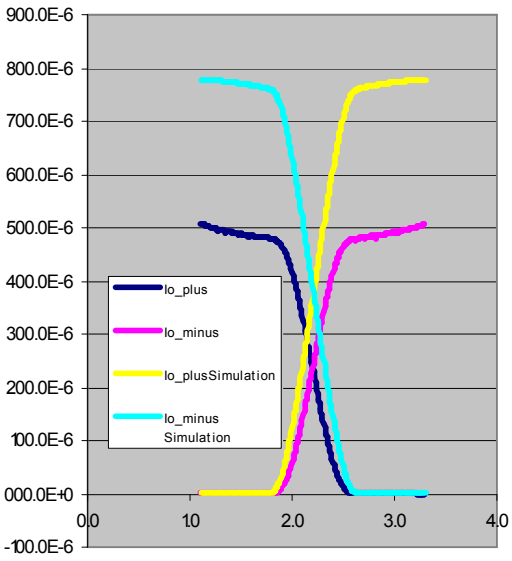
(b) $V_C = 1.2$



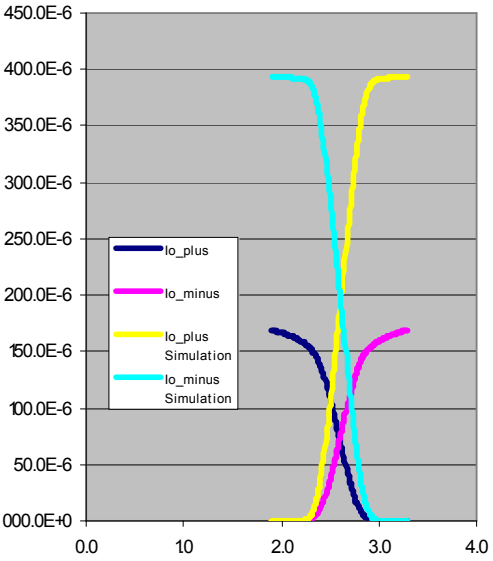
(c) $V_C = 1.5$



(d) $V_C = 1.8$



(e) $V_C = 2.1$



(f) $V_C = 2.4$

Figure 4.12 Results of the tests done to measure tail current

In the Peregrine transistors the kink effect sets in when the V_{DS} is greater than 1.5V. Referring to Figure 4.11, for values of V_C above 1.5V M_1 enters the kink region. This is happens because, V_{Ctrl2} closely follows V_C and M_2 is in triode. As a result, the V_{DS} drop across it ($3.3 - V_{Ctrl2} - V_{DS2}$) can get greater than 1.5V. This is illustrated in Figure 4.13, which shows the simulated V_{DS} across the transistor M_1.

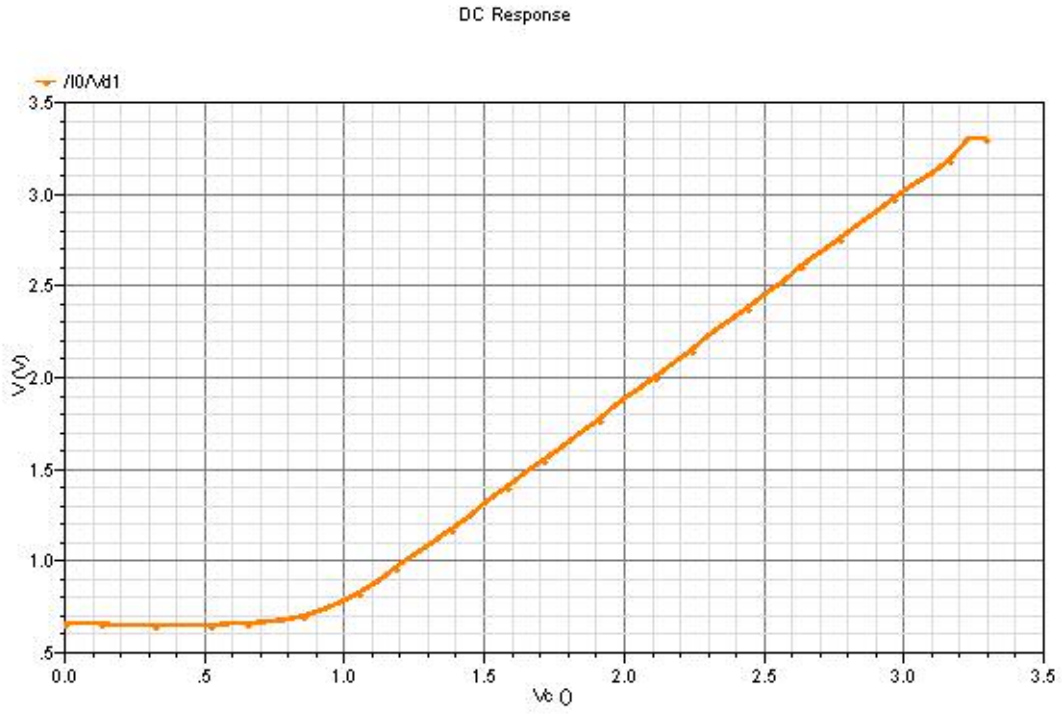


Figure 4.13 Simulation showing the magnitude of V_{DS} of M_1 while sweeping V_C from 0 to 3.3V.

On the other hand M_4 is not in the kink region. In fact it enters kink region only when V_C is less than 1.8V. V_{Ctrl2} has to closely follow V_C no matter which transistor is in the kink region. Since M_4 is not in the kink region, to develop the required voltage across itself, the current required by it does not change. However, to supply this current the V_{gs} across M_1 has to drop since current through a transistor increases when it enters kink. This lowers the V_{gs} across M_{11} too and the current in the gain stage is lesser than desired.

Tying the gate of the transistor M_2 to V_{DD} allows the V_{DS} across M_1 to increase beyond 1.5V. This is because M_2 enters triode and V_{DS} across it is very small – allowing higher V_{DS} drops across M_1. Similar problems occur in the branch consisting of M_1, M_2 and M_3 in Figure 4.10.

4.5 Proposed Improvements

To ensure operation of the circuit in the desired way it is necessary to make sure that V_{DS} across M_1 does not get larger than 1.5V. To achieve this, the gate voltage of M_2 must not be connected to V_{DD} but should be dynamically adjusted based on the existing operating conditions or in other words, the existing ΔV.

Figure 4.14 shows the improved circuit which has the modifications done to the circuit Figure 4.9 indicated in blue.

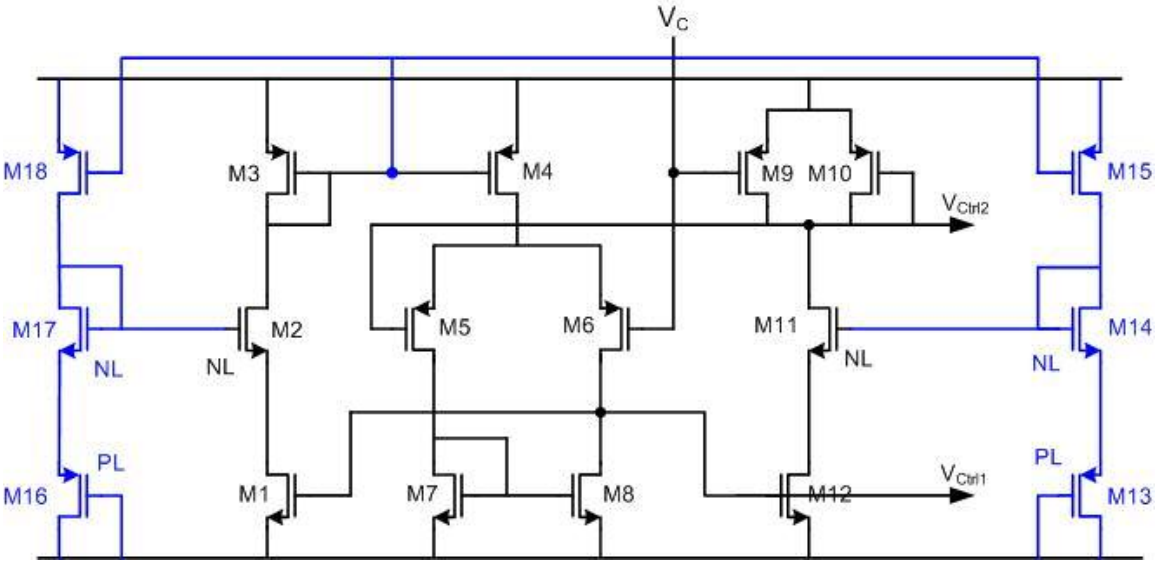


Figure 4.14 Bias Circuit with proposed improvements

Transistors M_{13}, M_{14} and M_{15} (M_{13}, M_{14} and M_{15}) serve to control the gate bias of M_{11} (M_2) according to the ΔV conditions of the circuit set by the control voltage V_C. To maintain transistors M_{12} (M_1) and M_{11} (M_2) in saturation equation(4.10) must be satisfied.

$$V_{G11} = \Delta V_1 + \Delta V_2 + V_{T,NL} + V_{SafetyM\,arg\,in} \tag{4.10}$$

V_{G11} can also be calculated from the equation(4.11),

$$V_{G11} = \Delta V_{17} + V_{T,NL} + \Delta V_{16} + |V_{T,PL}| \tag{4.11}$$

Comparing equation (4.10) and equation (4.11) we have a $V_{Safety\ Margin} = |V_{T,\,PL}|$.

Figure 4.15 shows the V_{DS} across the transistors M_{12} and M_{15} of Figure 4.14.

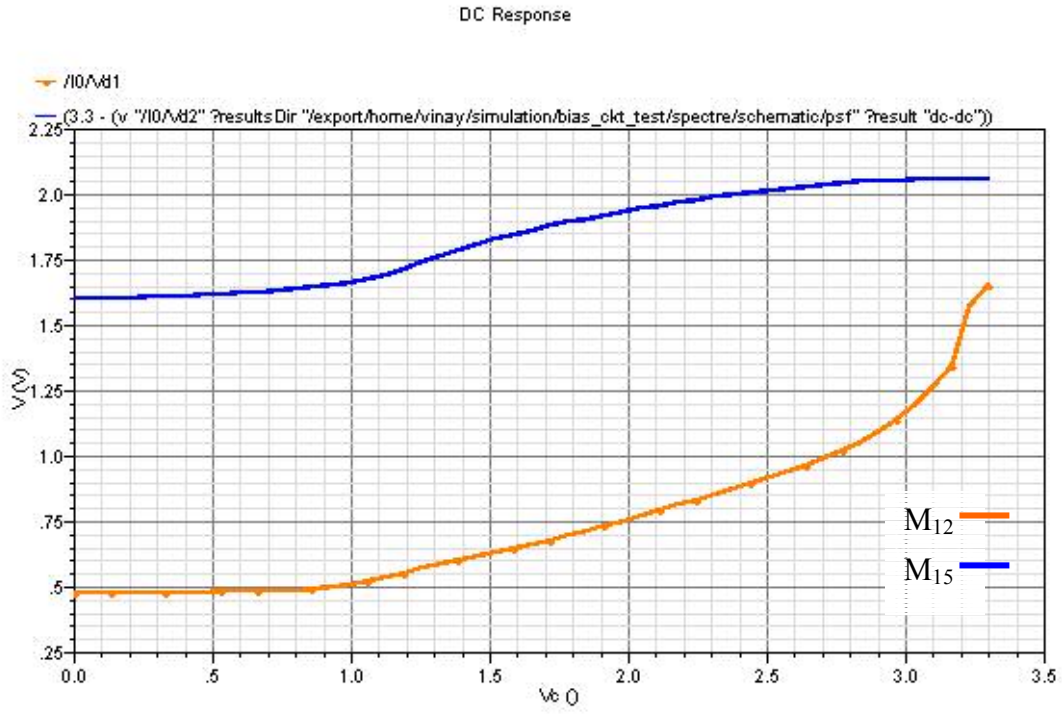


Figure 4.15 Simulation showing the V_{DS} across M_{12}, in orange and M_{15}, in blue of Figure 4.14

As is evident the V_{DS} across the transistor M_{12} stays below 1.5V keeping out of the "kink region". However, M_{15} is in the "kink region". In the peregrine PMOS transistors "kink effect" is not as severe as NMOS transistors [6]. Therefore, we can more easily afford to keep the V_{DS} across M_{15} higher than 1.5V.

Chapter 5

Phase Detector

5.1 Introduction

In a PLL there is a need for comparison of the frequency generated within the loop and a reference frequency. The purpose of comparison is solely the correction of generated frequency. Corrections are possible only when one knows the magnitude of disparity between the generated and reference frequency. This difference has to be then fed, in a compatible form, to a voltage controlled oscillator present in the loop which is responsible for copying the reference frequency for use by the application.

Phase Detector is the name given to the block in PLL which performs this function of comparing two frequencies and generating an error signal or phase difference voltage which is proportional to the difference of the two frequencies. The selection of its topology depends on the type of input, i.e. a sine wave or a square wave. With a sine input the phase detector is usually a multiplier, often implemented with a Gilbert-type topology. Square inputs entail the use of XOR or sequential detectors. These are mostly

digital and hence present a relatively less arduous design effort. Being digital also makes them attractive for use in digital applications.

Another important criterion is type of lock desired in the application. Some applications require only a phase lock between the two frequencies whereas others require both the frequency and phase to match. For some applications it's only sufficient to achieve a quadrature lock whereas others require a zero phase difference between the two frequencies of concern. Analog multipliers necessitate locking at quadrature for PLLs employing them because their gain is maximum at that point. Sequential detectors on the other hand can assist in lock at zero phase difference and also provide frequency detection.

A phase detectors average output, $\overline{V_{out}}$, is linearly proportional to the phase difference, $\Delta\phi$, of its inputs. Ideally their relationship is linear as shown in figure 3.1, crossing the origin for $\Delta\phi = 0$. K_D is defined as the gain of the phase detector and it is the slope of the line in figure 3.1. It is expressed in V/rad.

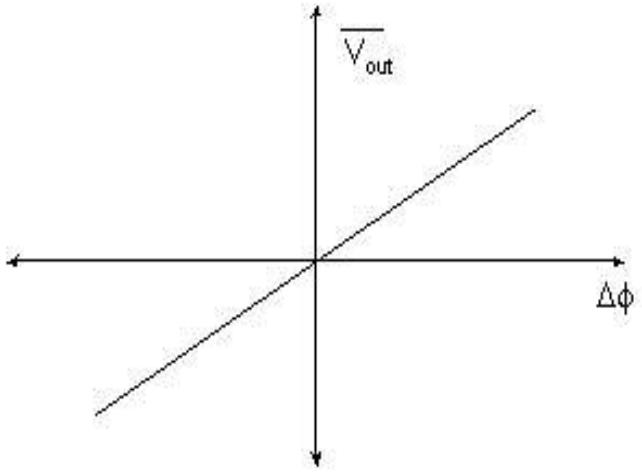


Figure 5.1 Ideal Characteristic of a Phase Detector

5.2 Overview of Phase Detectors

5.2.1 Analog Multiplier

An analog multiplier as indicated before is used in PLLs with sine wave inputs. Its output my be expressed as in equation (5.1),

$$AB\cos\omega t\cos\left(\omega t+\phi\right)=\frac{AB}{2}\left[\cos\phi-\cos\left(2\omega t+\phi\right)\right] \tag{5.1}$$

As is evident the output consists of a DC term and a double-frequency term. The DC term is used for phase detection. Phase detector gain for a multiplier is given in equation (5.2).

$$K_D=\frac{d}{d\phi}\left(V_{out}\right)=-\frac{AB}{2}\sin\phi \tag{5.2}$$

Where V_{out} is the output of the phase detector, A and B are the amplitudes of the two inputs and ϕ is the phase difference between the two inputs. From equation (5.2) we note that phase detector gain constant is zero when the phase difference is zero. It is maximum when the phase difference is 90°. Therefore a PLL utilizing the multiplier as a phase detector lock at a phase difference of 90° to maximize the useful phase detection range.

An advantage of this phase detector is that it can operate at high speeds. However it exhibits high static power consumption and moreover cannot detect frequency differences. Also its phase detection range is limited to 0 to 90°. Another problem of the analog multiplier is that it has the tendency to lock on to harmonics of the input frequency.

5.2.2 XOR Phase Detector

If an analog multiplier is driven with square inputs it becomes a XOR phase detector. In other words, it starts behaving like a digital two input XOR gate with the

reference and generated frequencies applied at its inputs. Figure 5.2(b) shows the operation of an XOR phase detector.

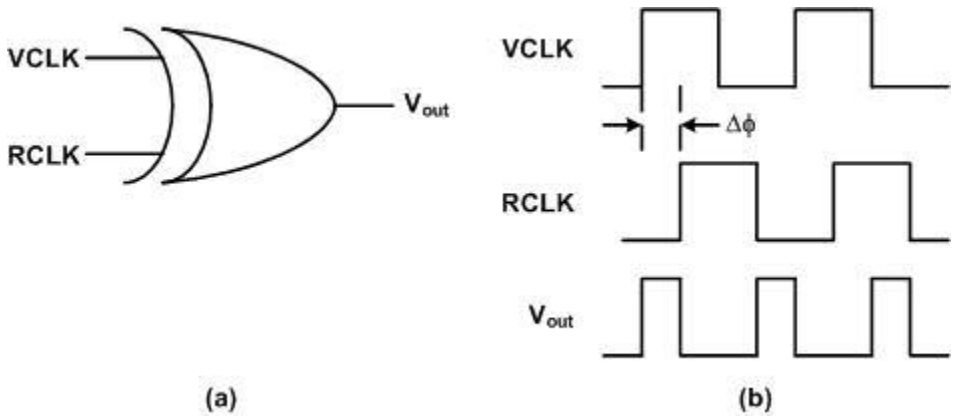


Figure 5.2 (a) XOR gate as a PD (b) Input and Output Waveforms

As indicated, with increase in phase difference between the inputs, the width of the output pulses increases thereby producing a DC level in proportion with the phase difference, $\Delta\phi$, of the inputs.

This phase detector has the undesirable property of dependence on the duty cycle of its inputs. Even if both of them have the same frequency and phase it will produce a DC value. The acquisition range of this phase detector is 0 to 180°.

5.2.3 Sequential Detectors

Sequential detectors, also known as Phase Frequency Detectors (PFD), are used for many digital applications, like clock recovery, where the phase difference required is zero. Sequential phase detectors become necessary in such cases. They can compare both phase and frequency of the input with reference clock and thus assist the PLL achieve a lock of zero phase difference. Further, in some applications it is important to have some information about the magnitude of any frequency difference between the inputs. Multiplier based phase detectors cannot provide such information but sequential phase

detectors can. They are also independent of the duty cycle of the inputs. Their operation depends only on the edges present in the inputs.

Phase Frequency Detectors are made up of flip flops. The simplest form of this phase detector is shown in Figure 5.3.

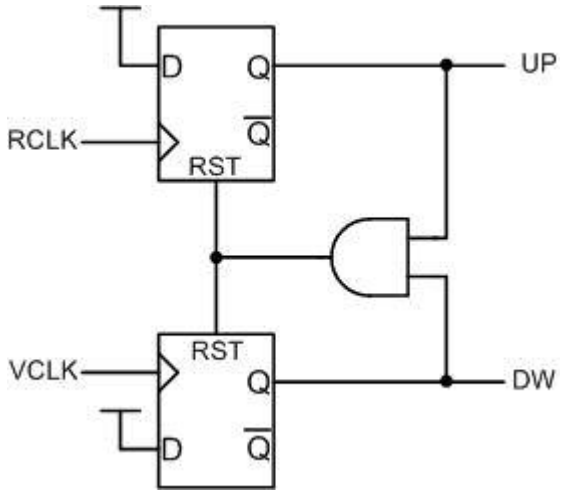


Figure 5.3 Phase Frequency Detector

The operation of the circuit shown in Figure 5.3 can be explained as follows. If we initially assume that UP = DW = 0, then a rising edge on RCLK leads to UP = 1, DW = 0. This state is preserved until there is a rising edge on the VCLK input. A rising edge on VCLK causes DW to go high. The AND gate now gives a true value and resets both the flip-flops. Both the outputs now return to zero. A similar sequence of events follow when there is a rising edge on VCLK before RCLK. In this case, however, DW goes high.

Figure 5.4 depicts the situation when the two inputs have equal frequencies but RCLK has phase difference with VCLK.

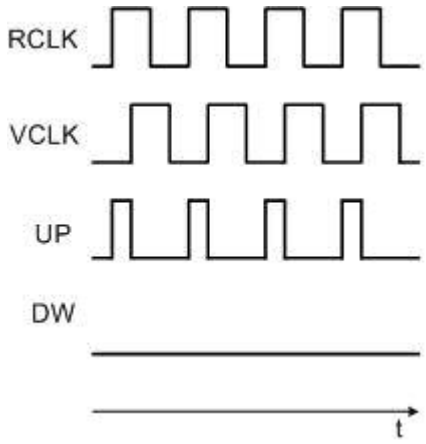


Figure 5.4 Operation of PFD when $\phi_{RCLK} \neq \phi_{VCLK}$

As is seen, DW stays at zero while UP produce pulses whose width is proportional to $\phi_{RCLK} - \phi_{VCLK}$. Figure 5.5 shows the case when RCLK has a higher frequency than VCLK.

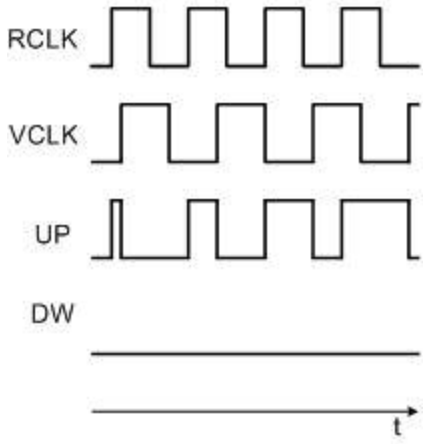


Figure 5.5 Operation of PFD when $\omega_{RCLK} \neq \omega_{VCLK}$

Now UP generates pulses while DW does not. It follows that if RCLK lags VCLK or has a lower frequency than VCLK, then DW produces pulses and UP remain quiet. It

can be inferred from the above that the DC contents of UP and UP indicate the relationship between $\phi_{RCLK} - \phi_{VCLK}$ or $\omega_{RCLK} - \omega_{VCLK}$.

From the Figure 5.6, which shows the characteristic of a PFD, we can observe that this phase detector has a range of 4π. It has a constant gain given by equation(5.3), in this region.

$$K_D = \frac{V_{DD}}{2\pi} \tag{5.3}$$

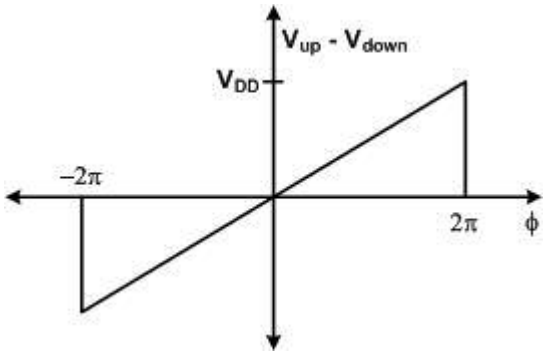


Figure 5.6 Characteristic of a PFD

However, in the real world the characteristic does not look this perfect. There is a dead zone in the region around zero phase difference - depicted in Figure 5.7(b) and explained in section 5.3.

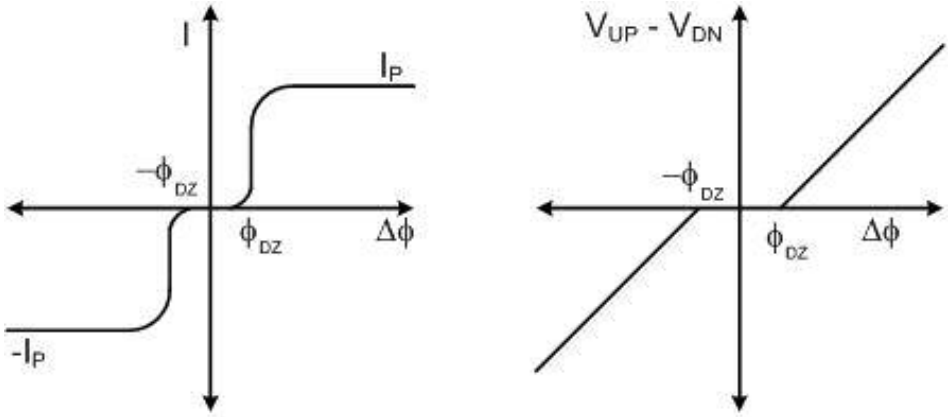
Sequential phase detectors have the advantage of and extended phase detection range as shown in Figure 5.6. Since they perform phase detection based on the edges of the input, they can be quite sensitive to missing edges. This makes them unsuitable for detecting phase differences between the incoming data (like Manchester or NRZ encoded data) with clock.

5.2.4 Phase Detectors for Data and Clock recovery

These phase detectors are insensitive to missing edges. Detectors like Hogge's phase detector among others as discussed in section 1.2 are used to recover clock from the data stream and also retime the data.

5.3 Dead Zone

Dead zone is the name given to the range of phase differences for which the PLL does not take any corrective action. This problem arises when the charge pump fails to deposit or take out sufficient charge from the loop filter. Figure 5.7(a), shows the behavior of the charge pump current, I_P, for different phase differences, $\Delta\phi$, between the reference clock and the VCO clock. For phase differences below ϕ_{DZ} the charge pump fails to turn on. This results in the dead zone as shown in Figure 5.7(b).



(a) (b)

Figure 5.7 (a) Charge Pump Current for different Phase Differences (b) Dead Zone of PFD

This problem can be traced back to the PFD. For small phase differences the PFD produces small UP (or DW) pulses (Figure 5.8). The dotted lines represent the actual

pulses and the solid lines indicate the pulses due to the finite time constant the PFD sees at its output. These small pulses fail to turn on the charge pump. As a result, no current is sourced or sinked and the VCO maintains its phase. This allows the VCO to accumulate phase error as no corrective feedback is provided.

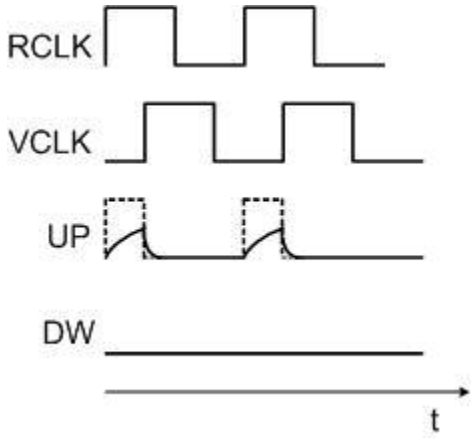
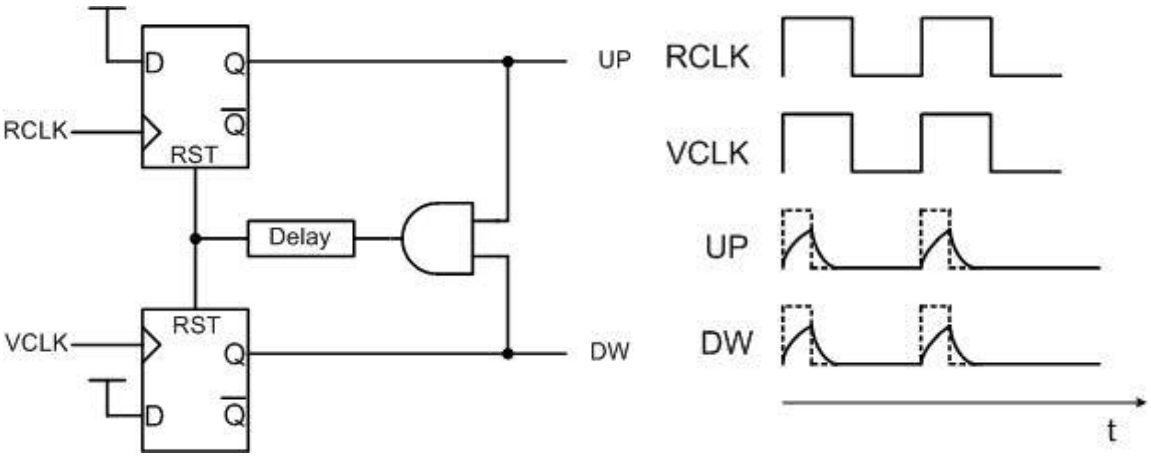


Figure 5.8 Cause of Dead Zone in PFD

The dead zone can be reduced if the PFD provides simultaneous UP and DW pulses of sufficient width when the PLL is in lock, or in other words, when there is no phase difference between input and VCO frequencies the PFD should produce UP and DW pulses instead of remaining calm, as illustrated in Figure 5.9(b). This can be achieved by introducing a delay in the reset path as shown in Figure 5.9(a). This delay prevents the pulling down of UP and DW outputs. These pulses of sufficient widths, created by the delay, ensure that the UP and DW pulses reach considerable voltage levels, so that a small phase difference is enough to bring them to adequate levels, ensuring that they turn on the charge pump.



(a) (b)

Figure 5.9 (a) Reducing Dead Zone introducing Delay (b) Resulting Waveforms

5.4 Overview of Topologies of Phase Frequency Detectors

A Phase Frequency Detector is a suitable topology because of its wide phase detection range and an all digital topology. However, a charge pump has to follow to ensure proper frequency setting of the control voltage of VCO.

5.4.1 Conventional Phase Frequency Detector [20], [21], [22]

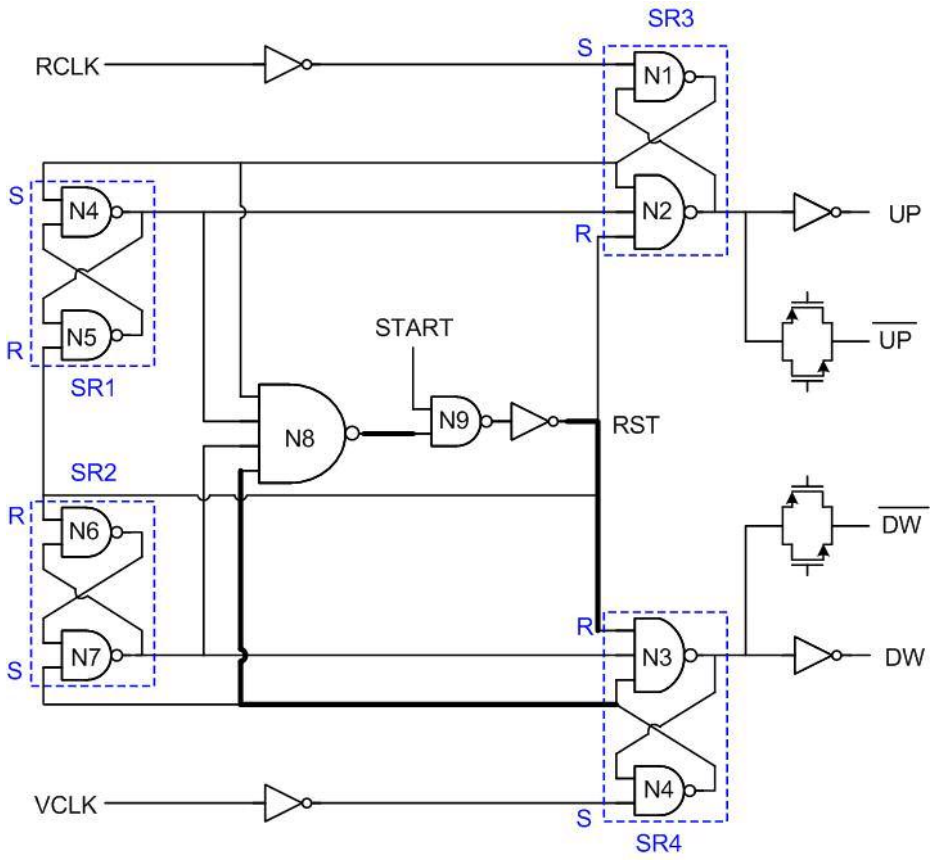


Figure 5.10 Conventional PFD

START is used to set the initial conditions of the circuit. When START is initially low, RST is low. Now assuming that both VCO and REF signals are low then both UP and DW signals are low. When START is held high RST becomes high, DW and UP outputs remain the same but the Q outputs of SR1 and SR2 become high. Let's now suppose that the REF signal comes before VCO signal. As soon as REF signal becomes high Q output of SR3 and so does UP. Since RST is high SR1 maintains its state. Now, three of the four inputs to N8 are high. As soon as the VCO signal goes high the fourth input also goes high and RST becomes zero. Both the inputs of SR3 and SR4 are held at zero and both of their outputs become high. This resets DW and UP signals. As soon as

any of the REF or VCO inputs go low RST is pulled high and the circuit is ready to perform its next comparison.

The reset path shown in Figure 5.10 in bold acts and resets both DW and UP outputs. The reset path consists of the gate N8 and not SR2 because the latter's output is already set. When VCO signal gets high, Q output of SR4 begins to go high and as a result all the inputs to N8 are high. Now the output of N8 goes low and so does RST – resetting both the DW and UP outputs.

If we add delay in this path the UP and DW outputs remain high for some time. This can help reduce or eliminate the dead zone [23].

5.4.2 PFD suggested by Won-Hyo et al [24]

The PFD suggested by Won-Hyo et al [24] uses the circuit shown in Figure 5.11 as the flip flop.

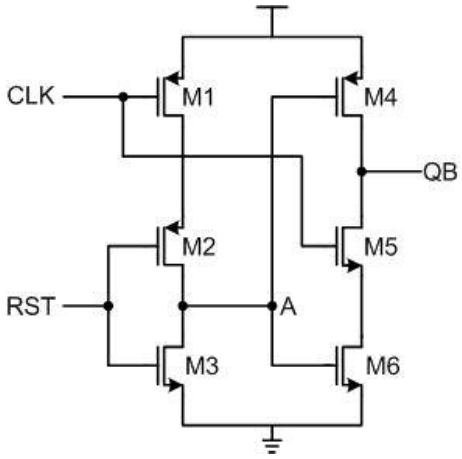


Figure 5.11 Schematic of D Flip Flop for use in PFD

Referring to Figure 5.11, initially when the CLK and RST inputs are low, node A is connected to VDD through M1 and M2. This charges the node to VDD during this time. This turns off M4 and since M5 is off when the CLK is low, QB is pulled high. If

the CLK now goes high then M5 turns on. Since M6 is already on, as A was previously charged to VDD, QB is pulled low. To reset the flip-flop, RST is pulled high, the node A now gets connected to GND through M3. This turns off M6 and turns on M4. The flip-flop is now reset and QB goes high.

The flip-flop of Figure 5.11 can be used in PFD as shown in Figure 5.12.

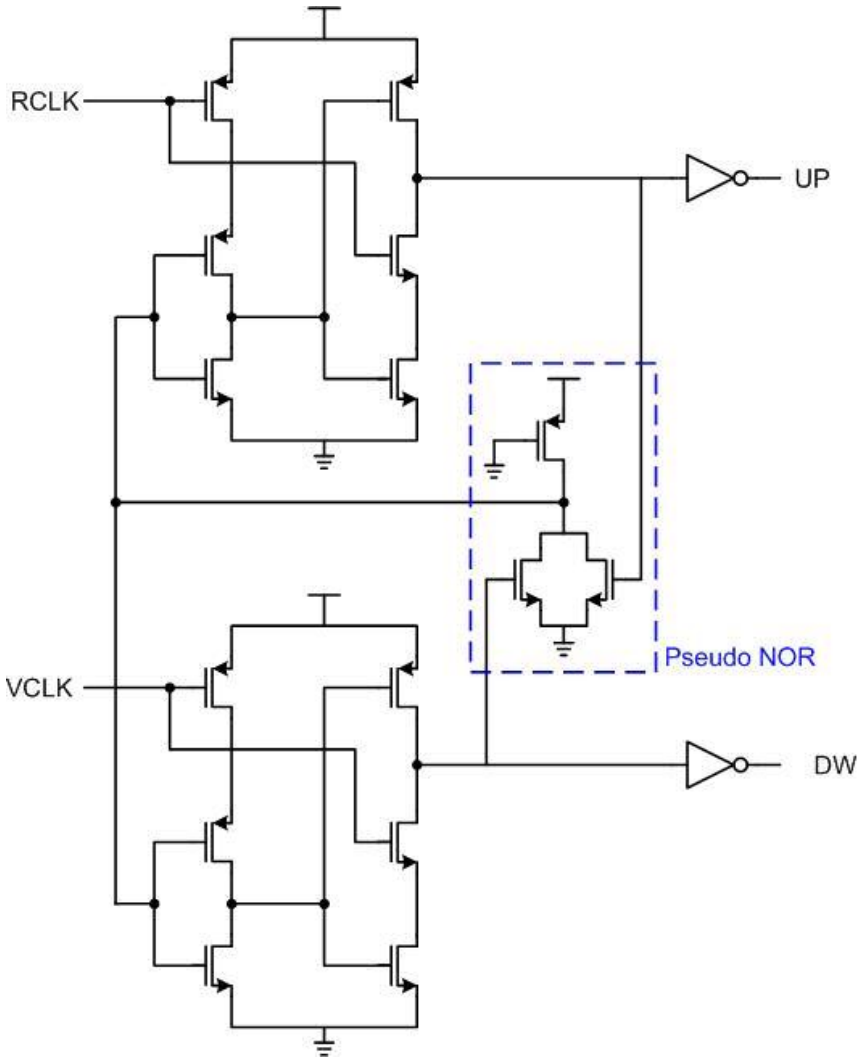


Figure 5.12 PFD suggested by Won-Hyo et al

The flip-flops of the PFD showed in Figure 5.12, have a functionality similar to that of those in the topology in Figure 5.3, however with less delay. A Pseudo-NOR gate is used to generate the reset signal.

5.4.3 PFD suggested by Sungjoon et al [25]

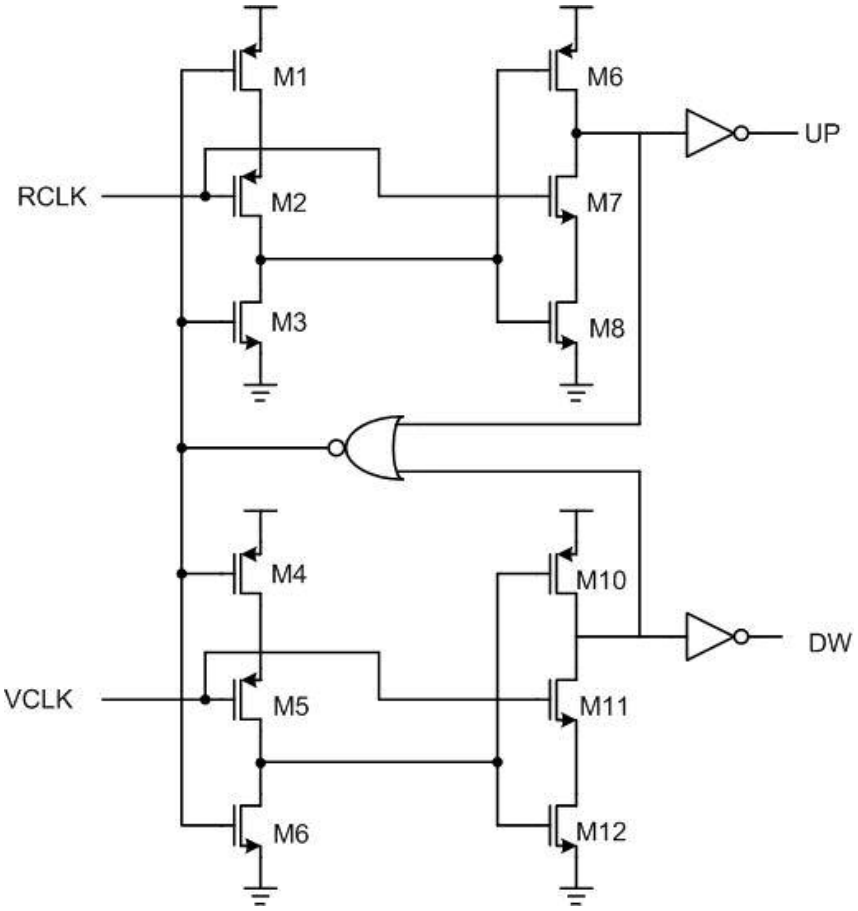


Figure 5.13 PFD suggested by Sungjoon et al

Referring to Figure 5.13, initially the both inputs to the NOR gate are high pulling the gate of M1 low. Let us assume that the RCLK edge has not arrived yet (a logic 1) and hence the gates of the transistors M1 and M2 are pulled low. This brings the gates of M6 and M8 to V_{DD} turning off M6 and turning on M8. When the RCLK edge arrives M7 is

turned on and M2 is turned off. Since the gates of M6 and M8 were held high before the UP signal now becomes high.

Through a similar sequence of events on the respective gates, DW is pulled high when the VCLK arrives. Now both the inputs to the NOR gate are low forcing the gates of M3 and M6 high. Since M2 and M5 are off as both RCLK and VCLK are high the gates of M6 and M10 are pulled low and as a result UP and DW are reset to zero.

5.4.4 PFD suggested by Kondoh et al [26]

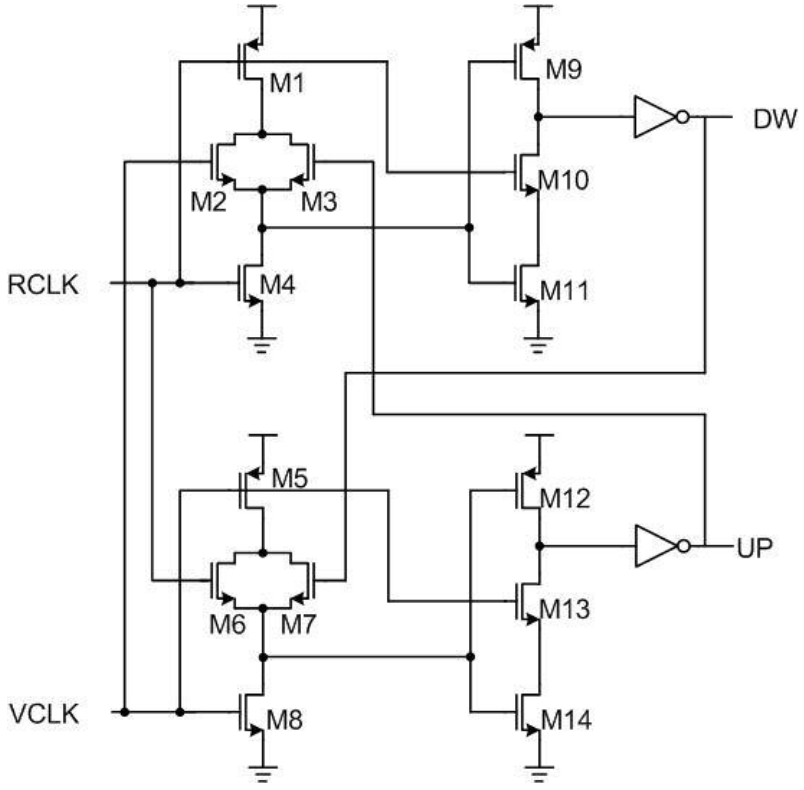


Figure 5.14 PFD suggested by Kondoh et al

Referring to Figure 5.14 let us supposed that RCLK signal arrives before VCLK. Then M4 turns on forcing the gates of M9 and M11 to be held low. Since M10 is also turned on, M9-M11 act as an inverter and DW is pulled low. In the UP half, M5 is on and

M8 is off, forcing the gates of M12 and M14 high. M13 is also off and so is M12. Since M14 is on, UP is pulled high – indicating that the VCLK frequency should be increased.

When the VCLK arrives, M8 turns on and M5 is turned off. This pulls the gates of M12 and M14 low. As a result UP is pulled low, because M12 is on, resetting the PFD.

Chapter 6

Future Efforts

First, a decision on the clock recovery architecture needs to be made. Clock recovery using a Hogge's phase detector type topology ensures that the clock is directly recovered from the data. This is the most desirable way of determining the clock of the input data. However, there are problems with the dead zone of the phase detector and ripples on the control line of the VCO as discussed in sections 1.2.2 and 1.2.3. Therefore, Clock recovery scheme suggested in section 1.2.3 could be adapted for use in the recovery of Manchester Encoded Data, if clocks of the transmitter and receiver drift too much with respect to each other.

However, if the clocks of the transmitter and receiver don't drift too much with respect to each other then Clock recovery scheme discussed in section 1.2.4 could be used because of its simple architecture. In this case a conventional phase frequency detector of section 5.4.1 should be used which has the advantage of being able to eliminate dead zone. It will work for frequencies close to 30MHz using the Harsh Environment Peregrine Cell-Library developed in the MSVLSI lab. For higher frequencies one has to adopt a faster PFD discussed in sections 5.4.2 - 5.4.4.

Charge pump discussed in section 3.5 could be used in the PLL because it reduces the "frequency jump" phenomenon to half the value as discussed in the same.

If "kink effect" is found to affect the performance of the VCO then the technique discussed in section 4.5 could be employed. However, it may not be the complete or universal solution.

Variation of temperature during operation of the PLL changes the loop parameters like charge pump current, K_{VCO} etc. resulting in degradation of the bandwidth of the PLL. As a result temperature considerations must be carefully considered in the design of bias generators for the charge pump. PLL design techniques discussed in [11, 27], called *Adaptive Bandwidth PLLs* could be employed to make the bandwidth independent of temperature dependent variables. This would prevent the bandwidth from being effected by temperature variations.

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VITA

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ABSTRACT

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Signals traveling in communication systems pick up noise and delays while traversing in their respective mediums. Also, the data is asynchronous when we take into consideration the receiver and the transmitter clocks. For effective communication between the two units there should be a mechanism of recovering the original clock and signal from the asynchronous and distorted or noisy signal – thus the need for a Clock Recovery Circuit.

The target application is the recovery of clock and data from Manchester encoded data stream generated by a Manchester Encoder-Decoder designed using the Harsh Environment Cell Library developed in the MSVLSI lab. This thesis also presents the successful test results for the 16 bit (single write) Manchester encoder/decoder pair for temperatures up to 195°C.

In any Clock Recovery System the PLL is the crucial block. The PLL charge pump generates the control signal for the Voltage Controlled Oscillator; any disturbance on its output adversely affects the performance of the VCO. This in turn has a significant impact on the locking behavior of the PLL. Factors contributing to the non-ideal operation are recognized and ways to minimize their effect are discussed. A new term called “frequency jump”, referring to the frequency shifts due to non-ideal charge pump operation, is coined.

Owing to the presence of “kink effect” in the 0.5u Peregrine SOS process the transistors in the VCO don’t bias up to the designed levels. To ensure proper operation of the circuit the drain to source voltage across the affected transistors has to be controlled to avoid the “kink effect” from degrading performance. A technique is proposed in this thesis which attempts to prevent the drain to source voltages from becoming too high.

ADVISOR’S APPROVAL: Dr. Chris Hutchens_____