EXTREME TEMPERATURE SWITCH MODE POWER SUPPLY BASED ON VEE-SQUARE CONTROL USING SILICON CARBIDE, SILICON ON SAPPHIRE, HYBRID TECHNOLOGY

By

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NOMENCLATURE

A,B,C,E		State matrices
AC	-	Alternating current
Ac	-	Comparator gain
Ae	-	Error amplifier gain
C	-	Capacitance
Cc	-	Compensation capacitor
Cgd	-	Gate drain capacitance
Cgs	-	Gate source capacitance
Ciss	-	Input capacitance
Cl	-	Load capacitance
Coss	-	Output capacitance
Crss	-	Reverse capacitance
D	-	Duty cycle
DC	-	direct current
D-mode	-	Depletion mode
DUT	-	Device under test
dB	-	Decibel
Ec	-	Energy in capacitor
El	-	Energy in inductor
EMI	-	Electro Magnetic Interference
E-mode	-	Enhancement mode
FEM	-	Finite element
fr	-	Resonant frequency
Gm	-	Transconducatance
I	-	Current
Id	-	Drain current

Ids	-	Drain source current
Ig	-	Gate current
Igs	-	Gate source current
Ip	-	Peak current
Is	-	Source current
JFET	-	Junction Field Effect Transistor
K	-	Coupling coefficient
L	-	Inductance
LDO	-	Low drop out
Ll	-	Leakage inductance
Lm	-	Mutual inductance
Lp	-	Primary inductance
Ls	-	Secondary inductance
MOS	-	Metal Oxide Semiconductor
P	-	Power
PFM	-	pulse frequency modulation
PWM	-	pulse width modulation
R	-	Resistance (Load)
Rc	-	Equivalent series resistance of capacitor (ESR)
RD	-	drain resistance
Rdc, Rl	-	DC resistance of inductor
Rg	-	Generator (source) resistance
rms	-	root mean square
ro	-	output resistance
Ron	-	On resistance of transistor
RS	-	source resistance
s	-	Laplace operator
SiC	-	Silicon carbide
SiO2	-	Silicon di oxide
SOI	-	Silicon on Insulator

SOS	-	Silicon on Sapphire
Toff	-	Off time of controller
Ton	-	On time of controller
Tr	-	Rise time
u	-	Input vector
V	-	Voltage
V2	-	Vee – square
Vds	-	Drain source voltage
vg, vi	-	Generator (input) voltage
Vgs	-	Gate source voltage
Vt	-	Thereshold voltage
x	-	State vector
Xc	-	Capacitive reactance
Xl	-	Inductive reactance
y	-	Output vector
Y	-	Admittance
Z	-	Impedance
ζ	-	Damping factor
ω	-	angular frequency
ωr	-	Resonant frequency
τ	-	Time constant
H	-	Henry (Inductance)
F	-	Farad (Capacitance)
K	-	kilo = 10^3
M	-	mega = 10^6
G	-	giga = 10^9
m	-	milli = 10^{-3}
μ	-	micro = 10^{-6}
n	-	nano = 10^{-9}
p	-	pico = 10^{-12}

Chapter 1

1.1 Introduction

Power electronics is a basic and ever demanding field in the electrical engineering domain. Electric power conditioning at various stages: generation, transmission or utilization is inevitable. The input parameters and the requirements from the system vary based on the stage where the electronics is involved. A wide variety of power conditioning has emerged based on various applications. Figure 1-1 shows a pictorial view of the power electronics at a basic level and its branches in the dc-dc conversion domain. DC-DC conversion is a dc transformation mechanism similar to that of ac transformers [1-5]. The depth of development of dc-dc converter is clearly evident from the complex tree structure.

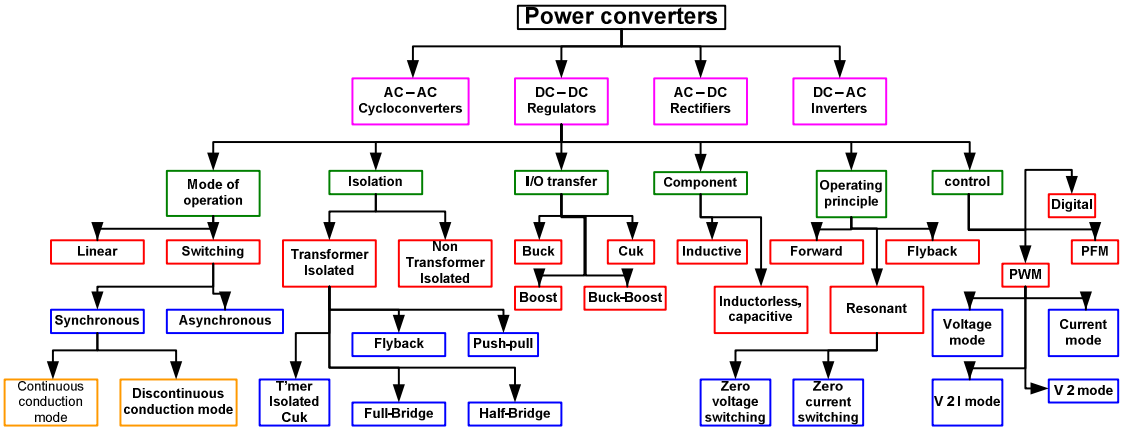


Figure 1-1. Hierarchy of power converters with emphasis on dc-dc conversion.

1.2 High temperature electronics

High temperature electronics is strongly a market driven technology [6-13]. Based on operating temperature the electronics are classified as commercial (<80°C), industrial or automotive (<125°C), military/aerospace (<200°C) and deep space and downhole (>250°C) [14]. The automotive and military electronic parts often used for downhole applications are protected by the use of appropriate Environmental Control Systems (ECS). ECS maintains the ambient temperature of the electronics by providing proper housing and cooling to maintain the enclosed electronics within their specified limit. However the development of ECS itself is very expensive in terms of both area and power.

The circuits designed for extended temperature operation includes some level of design complexity to adjust the operating characteristics at elevated temperatures to sustain acceptable performance. However as temperature increases above 200°C most commercial designs suffer from their physical limits and a minimal performance can no longer be satisfied. Hence a need for alternate materials for circuit design is critical for high temperature operation. Silicon on Insulator (SOI) based designs and silicon carbide (SiC) power technology have been a viable alternatives for harsh environment circuit design. In addition to elevated temperature, the vibration, shocks, wear and tear, pressure and radiation hazard makes the working environment hostile and hence increase the vulnerability of any electronic system. Both SOI and SIC devices satisfy these extreme requirements posed for the harsh environment systems.

A wide range of discrete products are now commercially available for high temperature operation through vendors like Honeywell [15] and Sissoid [16]. With increasing interests in deep space missions and interest in deeper oil and geothermal well planning, the role of high/extreme temperature electronics is more critical than ever before. The market growth for high temperature electronics have also been in a better phase for several decades.

1.3 Research objective

The objective of this research work is to demonstrate a solution for power supply used in extreme temperature applications. Operating temperature of electronics involved in deep space explorations easily extend from -150°C to +250°C and in case of deep natural resource wells like geothermal and oil well, the ambient temperature exceeds 300°C. As present generation electronic systems are highly dependent on extensive thermos packing and cooling for reliable operation in these hostile environments, a high temperature sustainable electronics would greatly reduce the cooling required for extended temperature operation and hence reduce the operating costs of these systems.

In this research the focus is to develop a DC to DC Switched Mode Power Supply (SMPS) capable of 275°C operation. This SMPS is proposed to be a power source for all the electronics incorporated in the drill string for Measuring While Drilling (MWD). More importantly it is desired to make the system a commercial off the shelf (COTS) product. A step down converter known as a buck converter is chosen based on the requirement [17]. The design parameters and the expected performance characteristics of the converter are shown in Table 1-1.

Table 1-1. Specifications of the dc-dc buck converter design.

Specification	Value
Operating temperature	≤ 275°C
Input voltage range	15 to 25V
Output voltage range	1.5 to 18V
Output Watts	> 2 Watts
Regulation	2%
Efficiency	80-90%
Stability (phase margin)	>75°

1.4 Dissertation organization

This dissertation contains 9 chapters including the current one. The literature review and the basics on the dc-dc synchronous buck conversion are discussed in chapter 2. The basic classes of buck converter are briefly described and the characteristic equations of the buck converter are derived.

Chapter 3 discusses the role of silicon carbide electronics in this work. The advantages of using silicon carbide devices are pointed out and the concept of enhancement mode Junction Field Effect Transistors (JFETs) is introduced. The 'in-house' measured characteristics of the silicon carbide JFETs are disclosed.

Various control schemes used for controlling the ON/OFF state of the power switches are discussed in chapter 4. This is followed by explaining the advantages of vee-square (V2) control scheme over the conventional control mechanisms. The issues with control loop stability and modeling of vee-square controller are discussed.

Chapter 5 discusses the role of gate drive involved in the control circuitry. The transformer coupled gate drive mechanism adapted in this research is given an extensive review with a detailed description provided in this chapter.

The design of the dc-dc buck converters starting from their basic building blocks is discussed in chapter 6. The house keeping electronic circuits are also presented. The simulated and measured performance characteristics of the blocks are provided.

The discrete components like capacitor, resistor and inductors are key parts in electronics design. The challenges in obtaining these passive components for this work and the procedures followed are discussed in chapter 7. Also as mentioned previously, for making the product a COTS component, the issues with packaging technology have to be dealt with. Chapter 7 also present the solutions proposed for packaging the design.

The results obtained from various prototypes of dc-dc buck converters are presented in chapter 8. The startup and transient characteristics of the converter is discussed here.

Chapter 9 provides the conclusion of the work. The data sheets for the first and second generation control IC are provided. The commercialization plans are given consideration by providing a rough estimate for SMPS using V2 control IC.

And finally the future work and bibliographic references are provided. Several important design factors are provided as a supplementary in the appendix section.

Chapter 2

2.1 Literature Review

As any other field of electrical engineering, digging through the work done by various people in the dc-dc conversion circuits is impossible in a short period of time. After an exhaustive search a brief summary of the work is brought out here with appropriate acknowledgements.

Linear conversion that does not involve any switching was the earliest mode of dc-dc conversion. These are based on pre-referenced Zener diodes at the output node to clamp the output voltage to a required level [18]. But Zener diodes for high temperature operation are not commercial. Also the Zener regulators are not readily capable of producing custom required output voltages and were eventually replaced by linear regulators [14].

In linear regulators, the Zener diode is replaced by a transistor whose conductivity is controlled by an error amplifier. Linear regulators are simple in construction and operation, and provide excellent transient response for load variations. However due to the inherent nature of their operation, efficiency is very low at lighter loads. Low dropout regulators (LDO) which are evolved adjustable linear regulators are gaining popularity since they tackle the drawback of light load efficiency of conventional linear regulators. Also they are able to provide a custom required output voltage based on a feedback element.

Recently, the linear regulators are being replaced by switching regulators which provide higher efficiency [19]. Several circuit configurations of switching regulators evolved based on custom applications [20]. Reports of dc-dc converter designs for operation at elevated temperature can be found in literatures. These include various other dc-dc conversion types like boost and buck-boost converters in additions to buck converters [21, 22].

A control loop acts like a brain of the switch mode dc-dc converter. Conventionally voltage mode and current mode control were used for controlling the switching transistor in a dc-dc converter. Research on improvement of control mechanism for switching converters is of high interest. The method of control used in this work is the vee-square control, which presents the advantages of both voltage mode and current mode control. Modeling and advantages of vee-square control over conventional control methods have been previously reported in various literatures [23-34].

The use of silicon carbide and silicon on insulator technologies for high temperature design were proved in various instances [15, 35-43]. The power handling capacity of silicon carbide devices are of high merit for high temperature design. Also the high reliability of silicon on insulator control circuits suitable for harsh environments has been taken advantage of in high temperature designs.

Exhaustive information on gate drive requirements of a switch mode power supply is widely available for commercial applications. However none of the available information is directly applicable in current work due to temperature limitation. Commercially available photo couplers are limited to 150°C operation. An optocoupler circuit based on SiC UV photodiodes and the planar transformers with integrated rectifiers are the novelty of this work applied to gate drive application.

Applications of planar transformers in pulse circuits have also been previously analyzed [44-61]. Practical design basics on pulse transformers can be obtained from the video amplifier designs. A high fidelity pulse transformers such as the ones used in video

amplifier designs are extremely difficult to design and hence very challenging given a planar structural constraint. However by use of an intelligent on chip rectifier combination, the challenge is easily tackled in this work.

All the above fundamental concepts are discussed in detail in the appropriate chapter sections of this work. This work differs from the previous work in the sense that the control circuitry is implemented in a silicon-on-insulator technology for 275° C operations. Also silicon carbide power switches are used. A hybrid design using silicon-on-insulator and silicon carbide with relatively inexpensive packaging techniques is the key attraction for this research work. ***This is the first and only demonstration of a SMPS as a completely integrated solution for 275°C.***

2.2 Silicon-on-insulator

Conventionally, transistors have been fabricated on a bulk silicon substrate where the thickness of the substrate is in order of several hundred micrometers. Silicon-on-insulator (SOI) technology is based on development of a thin film of silicon on an insulator layer. The devices are fabricated on the thin silicon films and do not have any "well process" as in bulk substrates. Figure 2-1 illustrates the transistors fabrication in bulk and SOI process. By eliminating a bulky leaky body, the leakage current in SOI transistor circuits are significantly smaller than the bulk counterparts. This phenomenon is explained by schematics presented in Figure 2-2. Also by reducing the silicon thickness to few hundred microns the radiation induced damage is minimum. The radiation hardened property of SOI is one of its biggest advantages for space applications. Therefore SOI is the preferred technology for high temperature harsh environment circuit design. Silicon-on-sapphire technology is used in this work.

Peregrine 0.5µm SOI CMOS process is used for fabrication the control circuit. The characteristics of this process have been well established. The circuits fabricated on this process are functional up to 275°C with very low leakage current[62]. In comparison, the

circuits designed on bulk silicon substrate are limited to 200°C operation at the expense of high leakage currents and power dissipation.

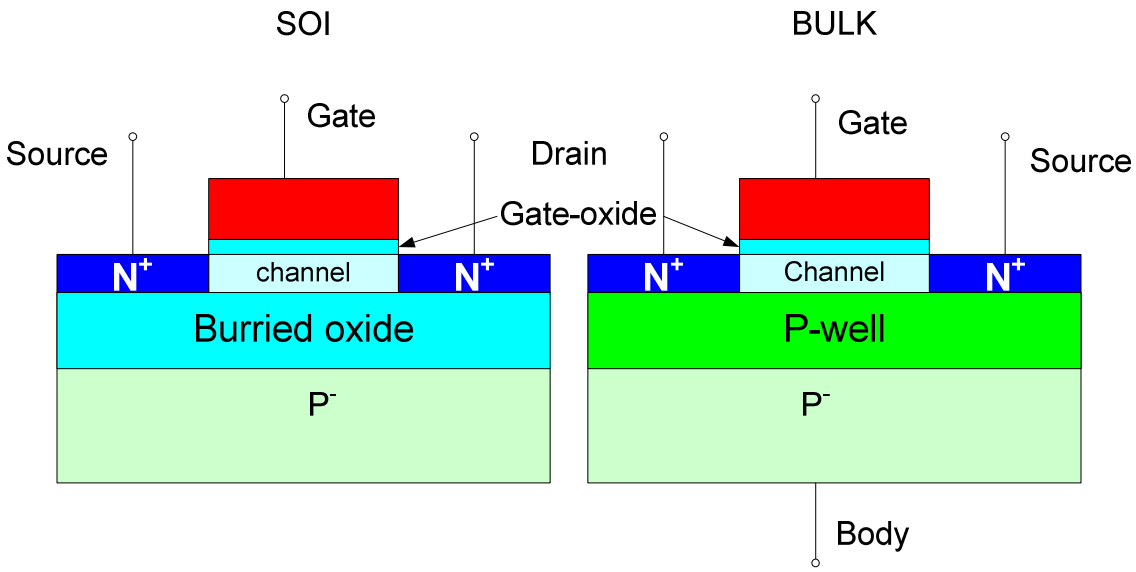


Figure 2-1. Cross sectional view of NMOS transistors in SOI and bulk fabrication process.

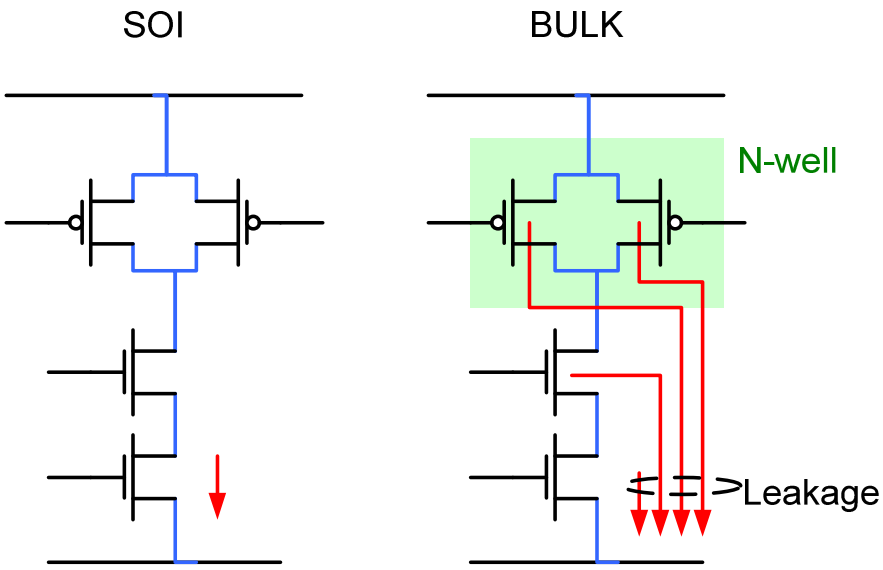


Figure 2-2. Comparison of leakage components in silicon-on-insulator and bulk process technology.

2.3 Modulation techniques

2.3.1 Pulse width modulation

Modulation of switches in a switching regulator is a key for obtained the required output characteristics. Several modulation techniques have evolved based on various applications. The modes of operation of dc-dc converters based on its control loop modulation are

- Pulse width modulation mode (PWM)
- Pulse frequency modulation mode (PFM)
- All Digital mode
- Delta Sigma

Of these control modes, pulse width modulation is widely used because of its simplicity. Pulse width modulation is duty cycle modulation of a constant period waveform based on an error signal and a reference signal. The duty cycle is the ratio between a switch on time to a predefined switching cycle period. Based on its operation PWM controllers are also known as ‘constant frequency variable time’ controllers.

In this work the pulse width modulation (PWM) technique is adopted. A system clock in a suitable wave shape (saw tooth, triangular or square pulse) and a comparator form a basis for pulse width modulation. A conventional PWM scenario commonly used in switching converters is shown in Figure 2-3. The figure shows an error signal and ramp signal superimposed. A comparator compares the two signals to generate a pulse width modulated output as shown in Figure 2-3. As a general rule, the greater the error signal, wider the pulse width. The resulting PWM output can be inverted based on the logic required to turn ON/OFF the corresponding switch by interchanging the inputs to the comparator.

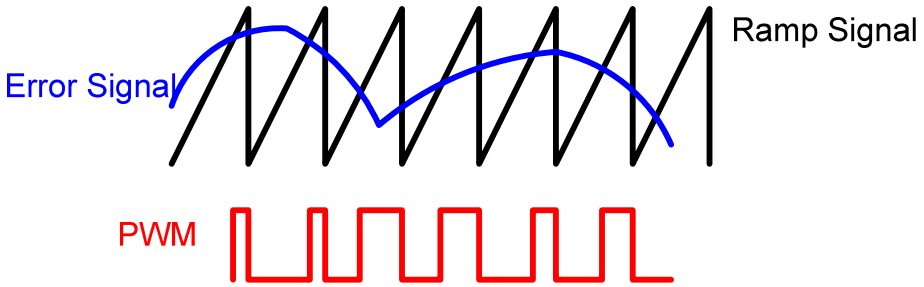


Figure 2-3. Principle of pulse width modulation.

2.3.2 Pulse frequency modulation mode (PFM)

While PWM control is efficient for high power, longer duty cycle cases, the efficiency of the system is significantly reduced at lighter loads. Pulse frequency modulation is adopted for low power designs especially in cases where the duty cycle in case of PWM is small. PFM is a 'constant time variable frequency' control also known as gated control. Figure 2-4 illustrates the pulse frequency modulation for 3 different levels of load current.

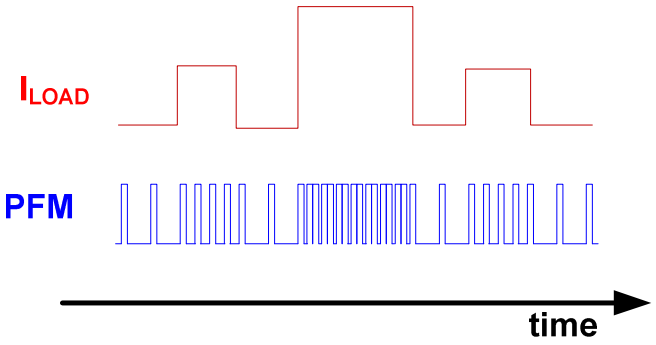


Figure 2-4. Pulse frequency modulation with respect to load current variation.

In case of random load fluctuations, a continuous change in the control frequency results in higher harmonic distortions in PFM controllers. PFM is usually avoided due to its complexity and higher electromagnetic interference (EMI).

2.3.3 All Digital mode

Recently, digital controls of converters are gaining popularity due to widespread use of digital designs and their inherent advantages. The transistor cost per functionality has been drastically reduced as a result of dynamic shrinking of the transistor size. Also from a general perspective digital designs are less sensitive to noise when compared to analog circuitries and also consume fairly lesser area and power when similar functionality is feasible. The simplicity of digital designs based on their behavioral descriptions and simulations eases implementation of multiple algorithms in a single controller. Hence digital control offers a hybrid approach where the choice of control strategy is dependent on the load and hence provides the potential for optimal controller operation. However, the transition from long established and well understood analog control mechanisms to digital domain is yet to happen. In case of high temperature designs it is preferred to keep the transistors channel length notably larger than the minimum permissible limit of the process to avoid excessive leakage at higher temperatures. For instance in this research work even though the controller was implemented in 0.5 µm technology, based on our previous understanding about the leakage current of the transistors at high temperature, the minimum gate length of the transistors for digital circuitries are limited to 0.8 µm for PMOS and 1.4µm for NMOS. This choice limits the full utilization of semiconductor process bandwidth and additionally results in area penalties.

2.3.4 Delta Sigma modulation

Delta-sigma modulation is an advanced mixed signal implementation of PWM control. Figure 2-5 shows the operation of delta-sigma controllers. The PWM signal shown in the middle plot (pink) is subtracted from the reference signal (green) shown in the top to generate an error signal (top-blue). The error signal is then integrated and compared with preset threshold limits. Delta-sigma modulators oversample the system at much higher frequency. In ADCs the digital output is later decimated in the follow on stages.

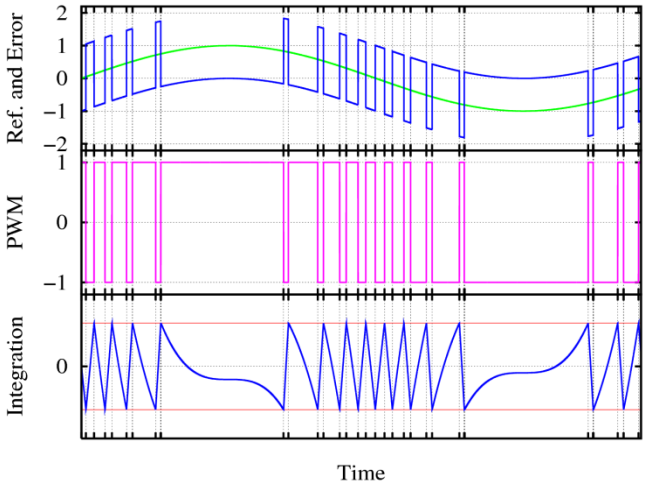


Figure 2-5. Illustrating the delta sigma PWM (Source: Wikipedia.com).

In this way delta sigma modulators provide noise shaping characteristics which reduce the noise power in the output spectrum of interest. Applications of these complex modulation techniques are where there is a need to remove the noise in certain spectral range of the converter.

As mentioned earlier PWM based control is of interest in this work and shall be used throughout the fore coming chapters. However it must be pointed out that with shrinking channel lengths, the transistor models impose statistical design of circuits and hence a transition to digital control design over analog circuitries shall soon will likely be inevitable.

2.4 Buck converters

Buck converters are the simplest and most widely used converters in dc-dc conversion. Buck converters are dc-dc transformers that produce an output lower than the input. By their nature of operation they are also referred to as step-down converters. Figure 2-6 shows a basic dc-dc buck converter. The 'V_{in}' represents a dc input voltage and 'V_{out}' represents a stepped down output voltage. The 'PS' is the power switch that connects the input to output and 'D' is the catch diode. The inductor 'L' and capacitor 'C' form the

output filter network. The passive LC network also serves as energy storage elements with inductor and capacitor energy given by equations 2-1 and 2-2, respectively.

$$E_l = \frac{1}{2} LI^2 \qquad [2\text{-}1]$$

$$E_c = \frac{1}{2} CV^2 \qquad [2\text{-}2]$$

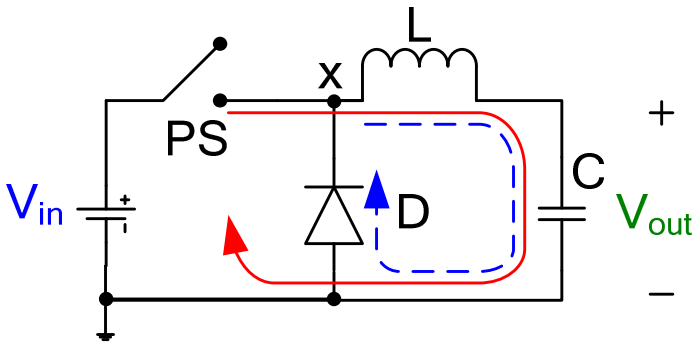


Figure 2-6. Basic switch mode power supply with catch diode.

2.4.1 Operation of PWM buck converter

The basis of operation of any PWM switching converter can be explained by analyzing their behavior at different periods in a switching cycle. An asynchronous buck converter as shown in Figure 2-6 is chosen to keep the explanation simple. When the power switch (PS) is switched ON the output voltage increases linearly as current flows through the inductor, into the capacitor. During this time the diode (D) is reverse biased and does not affect the circuit. When a preset threshold is reached at the output (V_{out}), a control circuitry (not shown in the figure) switches off the power device. A basic characteristic of an inductor is that "the current flowing through an inductor cannot change instantaneously". This phenomenon reverses the polarity of voltage at the node 'x'; driving it to a voltage lower than the ground (zero volts), thereby forward biasing the diode (D). Therefore the diode "catches" the circuit and provides a path for current flow.

Hence the diode is called a catch diode and since the turn on time of the diode is not well defined with respect to system clock, the process is referred to as asynchronous switching. As the voltage at the output falls below a preset threshold the control circuitry repeats turning ON the power switch and hence the process continues.

2.5 Synchronous rectification

In case of asynchronous rectification described in previous section, based on the forward voltage of the diode and steady state operating current, a considerable voltage drop across the diode is required to keep and the current circulating through the inductor. This results in significant power loss across the diode during the OFF time of the every switching cycle. The worst case condition is the ‘no load’ (no power delivered to load) case when the duty cycle is at its minimum and the diode is ON for longer time in a switching cycle. To reduce the power loss due to this forward voltage drop, a semiconductor switch is used as a synchronous switch. Since the operation of this switch is synchronized with the system clock and is complimentary to the power switch the converter is called ‘synchronous switching’ converter.

An ideal synchronous switch possesses zero ‘on-resistance’ and infinite ‘off-resistance’ thereby resulting in zero power loss. This largely minimizes the conduction loss and thereby improves the overall efficiency of the system. The control circuitry is however made more complicated to ensure “timely turn ON” of the synchronous switch complimentary to the power switch. Proper firing of the two switches with appropriate dead times is a challenge and discussed in later chapters. Moreover the practical switches implemented using transistors presents finite ON resistance and OFF resistance that results in power dissipation during the ON and OFF state, respectively. These parasitic resistances are taken in to account in system analysis in later sections. Figure 2-7 shows a synchronous rectifier.

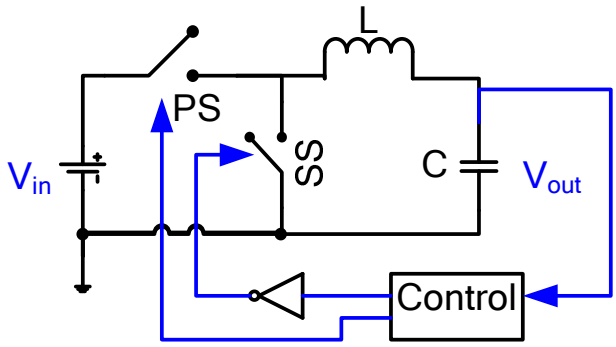


Figure 2-7. Synchronous buck converter.

2.6 Transfer function of PWM buck converter

A mathematical model of a PWM buck converter is of interest for analyzing its behavior and a better understanding of the system dynamics. The effect of duty cycle on the output voltage for a given input voltage is described by the transfer function of the system. The transfer function obtained here is on the basis of energy balance in inductor. The energy balance in the inductor during steady state operation states that the average current through the inductor in a single switching cycle (T_s) is zero. Figure 2-8 gives a pictorial representation of steady state operation of PWM buck converter. During the ON time (T_{on}) the inductor current (I_L) and the output voltage (V_{out}) increases linearly and during OFF time (T_{off}) I_L and V_{out} fall linearly. Mathematically this can be described by equation 2-3 where relatively large charge and discharge time constants are assumed. Rearranging the equation the expression for transfer function (V_{out}/V_{in}) is obtained to be the duty cycle (D).

$$(V_{in} - V_{out}) \times T_{on} = V_{out} \times T_{off} \qquad [2\text{-}3]$$

$$\frac{V_{out}}{V_{in}} = \frac{T_{on}}{(T_{off} + T_{on})} = D \qquad [2\text{-}4]$$

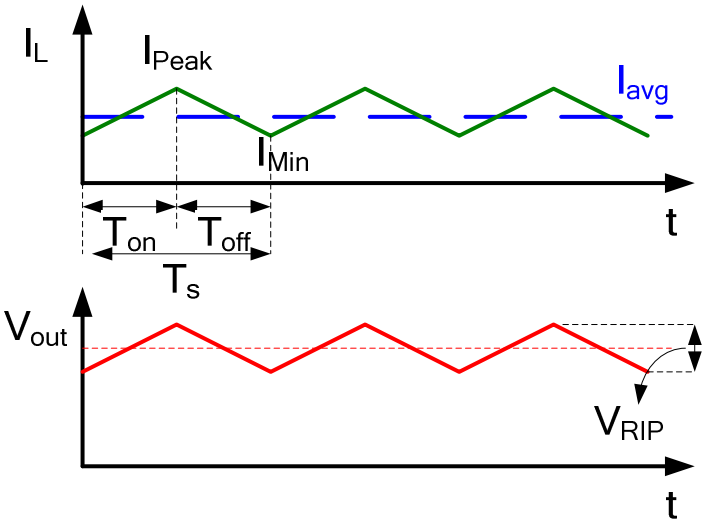


Figure 2-8. Inductor current and output voltage during steady state operation of buck converter.

2.7 Transfer function of output filter

The LC filter network at the output of the converter acts like a second order system as shown in Figure 2-9. Even though the transistor acts like a switch, the on resistance of the transistor is a non-zero value. Particularly at elevated temperature the on resistance maybe significantly higher and cannot be neglected. The dc resistance of the wire used in the inductor also affects the system performance. To account for these factors, the on resistance of the transistor is represented by R_{on} and the dc resistance of the coil is represented by R_{dc} in the circuit model. The load resistance R_l also plays a significant role in the transfer function. The mathematical analysis of the system in frequency (Laplace) domain is as follows.

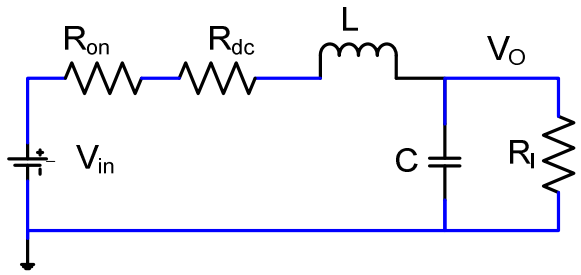


Figure 2-9. Second order RLC representation of buck converter.

Using KCL,

$$\frac{Vin(s)-Vo(s)}{R_x + j\cdot\omega\cdot L} = \frac{Vo(s)}{Zc(s)} + \frac{Vo(s)}{R_l} \qquad [2\text{-}5]$$

where $$R_x = R_{on} + R_{dc} \qquad [2\text{-}6]$$

Further simplification of equation 2-6 to obtain the transfer function yields,

$$\frac{Vo(s)}{Vin(s)} = \frac{1}{s^2 + s\cdot\left(\frac{R_x}{L} + \frac{1}{C\cdot R_l}\right) + \left(\frac{1+R_x/R_l}{L\cdot C}\right)} \qquad [2\text{-}7]$$

The transfer function analysis is later used in designing compensation network for the control loop. The equivalent series resistance (ESR) of the capacitor is not considered in this analysis. However the stability of the control loop is dependent upon the ESR and is discussed in detail in section 4.2.1.

Chapter 3

3.1 Silicon carbide electronics

Power switches in the dc-dc converters are the primary cause of failure or limitation of the systems at high temperatures. Many power semiconductor manufacturers integrate control circuitry on the power die resulting in smart power converters. However, high power dissipation across these switches demands tolerating capabilities (high voltage and current stress) of the semiconductor and hence integration of power switches to the SOI control chip is not efficient for high temperature operation. Silicon carbide as a wide band gap semiconductor will play a major role in high temperature electronics design [19, 63-73]. It possesses some exceptional properties making it well suited for high temperature applications. Silicon carbide exists in various polytypes of which the 4H type is most popular.

It can be observed that the silicon carbide outperforms silicon except for the carrier mobility and production cost. However when we consider that for power devices that breakdown voltage, thermal conductivity are more significant as a result of greater power dissipation at the drain terminal, SiC has an advantage by a factor of 30. The mobility is less of an issue for a power device compared to the cost penalty. With increasing interest in SiC the commercial cost is expected to reduce significantly.

Table 3-1. Comparison of properties of silicon and silicon carbide.

Property	Silicon	4H-SiC
Material Bandgap (eV)	1.12	3.2
Thermal conductivity (W cm^{-1} K^{-1})	1.3	4.9
Breakdown field (V cm^{-1})	3×10^5	2×10^6
Relative permittivity	11.7	9.7
Hole mobility (cm^2 V^{-1} s^{-1})	450	120
Electron mobility (cm^2 V^{-1} s^{-1})	1400	950
Saturation electron velocity (cm s^{-1})	1.0×10^7	2.0×10^7
Commercial wafer size (cm)	15	10
Maximum operating temperature (°C)	300+	600+

3.2 Characterization of silicon carbide JFET

To understand the operational behavior of the junction field effect transistors it is necessary to obtain their electrical characteristics. Several parameters are required to completely model a device for all operating conditions. Threshold voltage, leakage current, ON resistance and transconductance are the few basic parameters to predict the switching characteristics of the device. In addition the device terminal capacitances are required to model the transient behavior of the device. A junction field effect transistor can be modeled using diodes, resistors, capacitors and transconductor as shown in Figure 3-1. The diodes are used to model the leakage currents in the device. Within normal operating conditions the voltage across the gate-source diode is below its knee voltage to keep it in OFF state. Similarly the gate drain diode is reverse biased and does not conduct. The C_{gs} and C_{gd} are the terminal capacitances that determine the switching performance of the device.

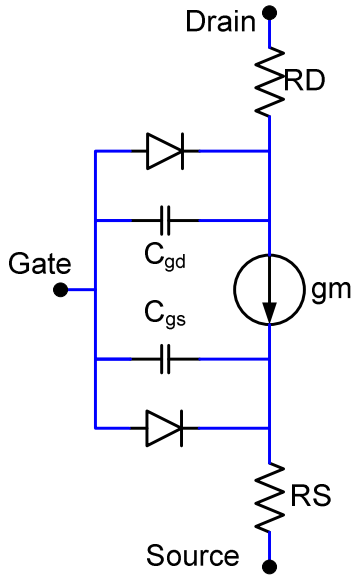


Figure 3-1. Equivalent circuit model of a junction field effect transistor.

3.2.1 Enhancement mode JFET

JFETs are commonly used as depletion mode device. The absence of an oxide interface as in MOSFET results in better noise performance of JFETs and because of its depletion mode characteristics and the defects associated with the oxide interface; it's a preferred choice of input transistors of low noise amplifiers. However the disadvantage of depletion mode operation of a device over enhancement mode is the requirement of negative gate source voltage to turn off the transistor. This greatly complicates the requirements of the system operating under unipolar supply voltage. Enhancement mode operation of JFETs in conventional silicon is limited to less than 0.7 volts however, with excessive gate leakage. This limit is due to the presence of a p-n junction diode between gate and source terminal which forward biases as the gate-source voltage increases above the diode turn on voltage. Due to the wide bandgap nature of silicon carbide, the turn on voltage of the gate source diode in SiC JFETs is above 2.7V. This lends itself to facilitating operation and use of SiC JFETs in the enhancement mode of operation. Further, buried gate technology is used to create enhancement mode operation in vertical JFETs which enables lower positive threshold voltage while attaining high overdrive capabilities. The JFETs used in this research work are procured from Semisouth

laboratories inc., USA [14]. The cross-sectional view of the enhancement mode JFETs based on buried gate technology is shown in Figure 3-2. The die snapshot of a packaged device is shown in Figure 3-3.

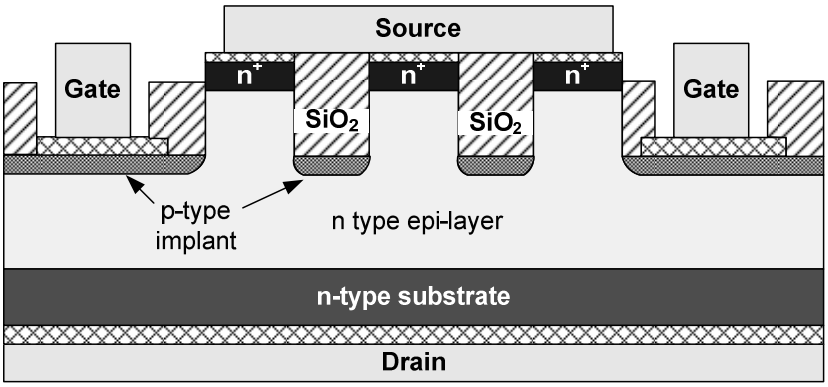
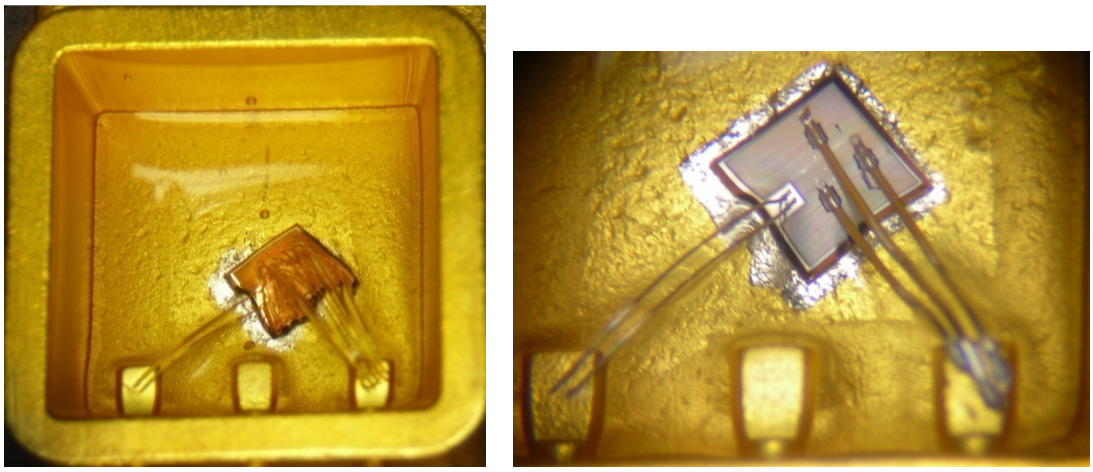


Figure 3-2. Cross section of a silicon carbide JFET on a 4H substrate.



3-3.Snapshot of the enhancement mode JFET in a TO package (Gold pads –left; Aluminum pads – right.)

3.2.2 Gate source characteristics

The gate source characteristics also known as input characteristics gives information about the threshold voltage, off state leakage current and transconductance of the device. Figure 3-4 shows the turn on characteristic of a SiC JFET measured using a Keithley 4200 semiconductor characterization system. The different curves show the varying behavior of device at corresponding temperatures. The threshold voltage is extracted from the gate source characteristics. In order to measure the leakage current of the device

which is similar to the reverse biased current of a gate source diode the measured data are plotted in semi-logarithmic scale. Figure 3-5 shows the leakage characteristics of four different SiC JFETs. It can be seen that device 'J25' behaves like an ideal device whereas others show increased or excessive gate-source leakage current. This type of increased leakage can be explained as a fault in the fabrication of these devices with this behavior expected to be absent in commercially available devices. Higher leakage current indicates the need for an increased drive current requirement from gate drive circuitry at around the 2V "turn on" point.

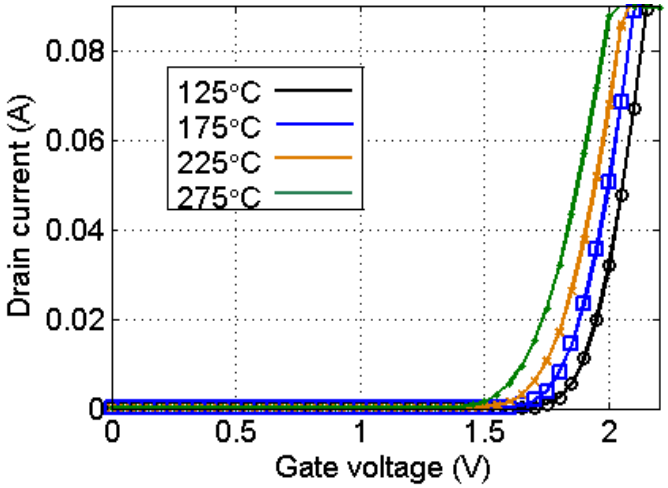


Figure 3-4. Gate characteristics of E-mode SiC JFET.

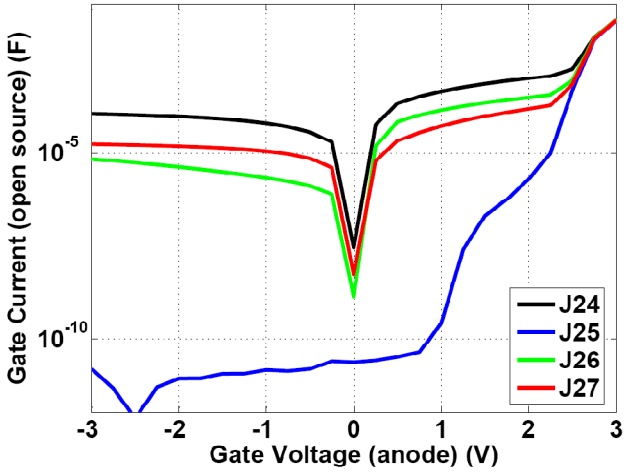


Figure 3-5. Gate source diode characteristics of E-mode SiC JFET.

3.2.3 Output characteristics

The effect of drain voltage on drain current for various gate voltages is the output characteristics of a transistor. The on-resistance of a switch affects the efficiency of a SMPS since considerable power can be wasted across the switch as I^2R loss. On-resistance is measured from the Id-Vd characteristics of the transistor. The Id-Vd characteristics measured in the laboratory is shown in Figure 3-6. Behavior of the device at elevated temperatures (125°C and 275°C) is shown in the figure.

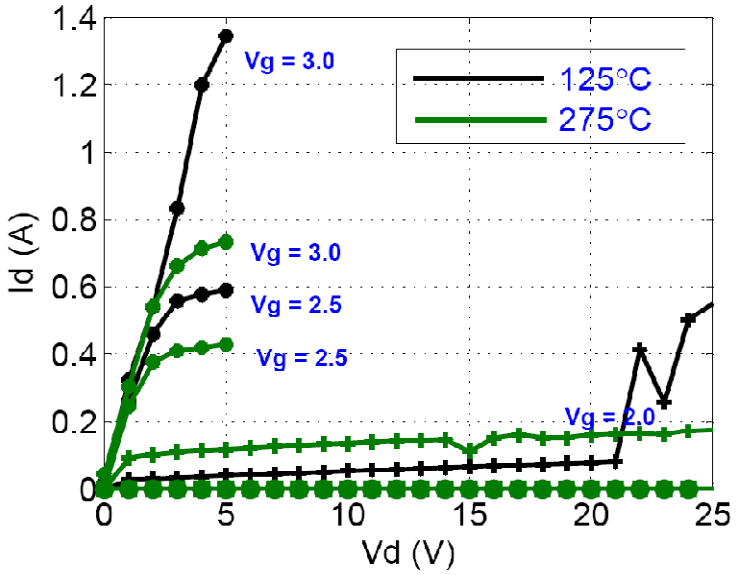
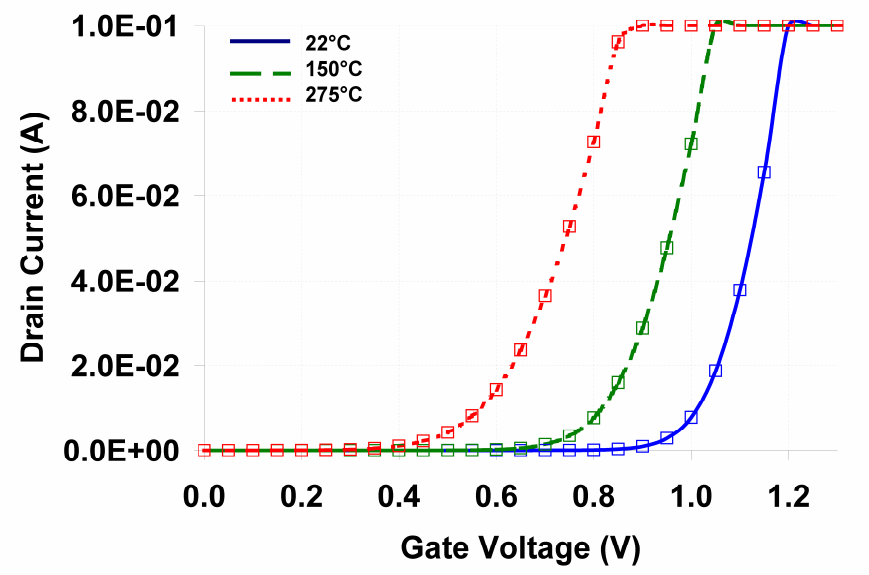
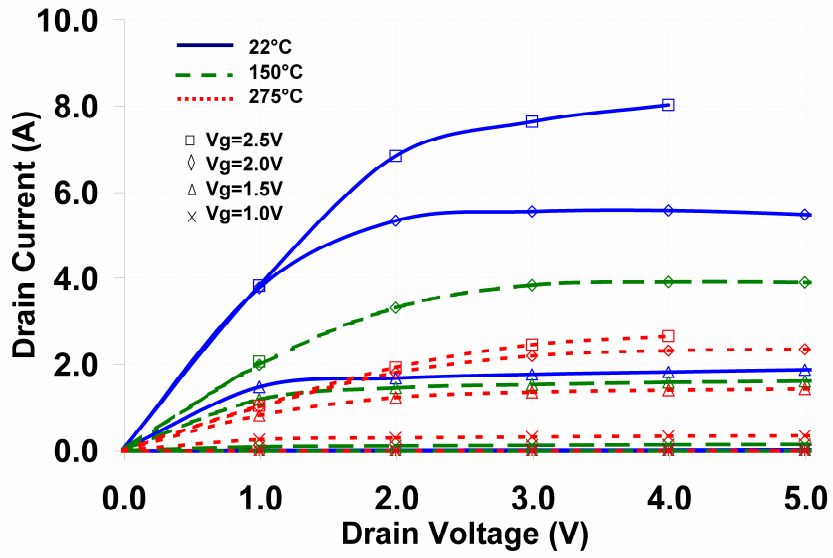


Figure 3-6. Drain characteristics of E-mode SiC JFET.

An improved device is made available to succeed the older generation SiC devices, with the goal of lower threshold voltage and higher breakdown voltage. The characteristics of an improved version of these devices are shown in Figure 3-7 and 3-8. Significant lowering of threshold voltage and improvement in the device current can be seen from the figure. Both these improve the device performance and hence are beneficial.



3-7. Gate source characteristics of the second generation SiC JFETs.



3-8. Drain source characteristics of second generation SiC JFETs.

3.2.4 Pulsed measurements

Continuous operation of JFETs at higher currents leads to self heating at the device junctions. This reduces the conductivity of a transistor and hence degrades its performance. Figure 3-9 shows such an effect on a silicon carbide device for gate drive voltages of 2.0V and 2.5V.

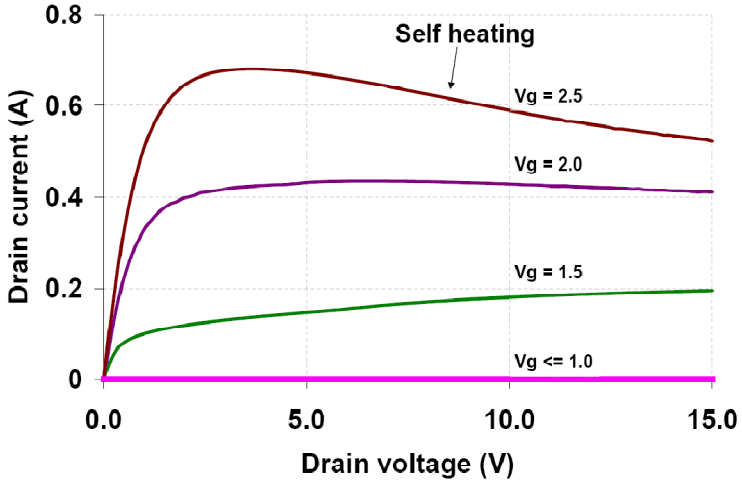


Figure 3-9. Drain characteristics of an E-mode SiC JFET illustrating the self heating effect.

To avoid self heating and to get the normal characteristics of the device, pulsed measurements are used. In pulsed measurements the device under test (DUT) is electrically stressed for a limited time over a pre-determined switching cycle. Therefore by keeping the duty cycle lower the internal temperature of the DUT can be maintained at nominal ambient value and actual characteristics can be obtained. In this work the drain characteristics as shown in Figure 3-6 is obtained by pulsing the gate at 4 Hz with 20% duty cycle. The measured RMS current is converted to the peak current using the formula given by equation 3-1.

$$I_p = \frac{I_{rms}}{2 \times (D - D^2)} \qquad [3\text{-}1]$$

where I_p – peak current

I_{rms} – rms current

D – duty cycle

The calculated peak current is cross checked for its consistency with DC spot measurement. Agilent E3236A power supply and 33250a signal generator is used as drain voltage source and gate pulse generator. Agilent 34401 multimeter is used to measure drain current. The instruments are virtually controlled using the labview virtual instrumentation (VI) interface as shown in Figure 3-10.

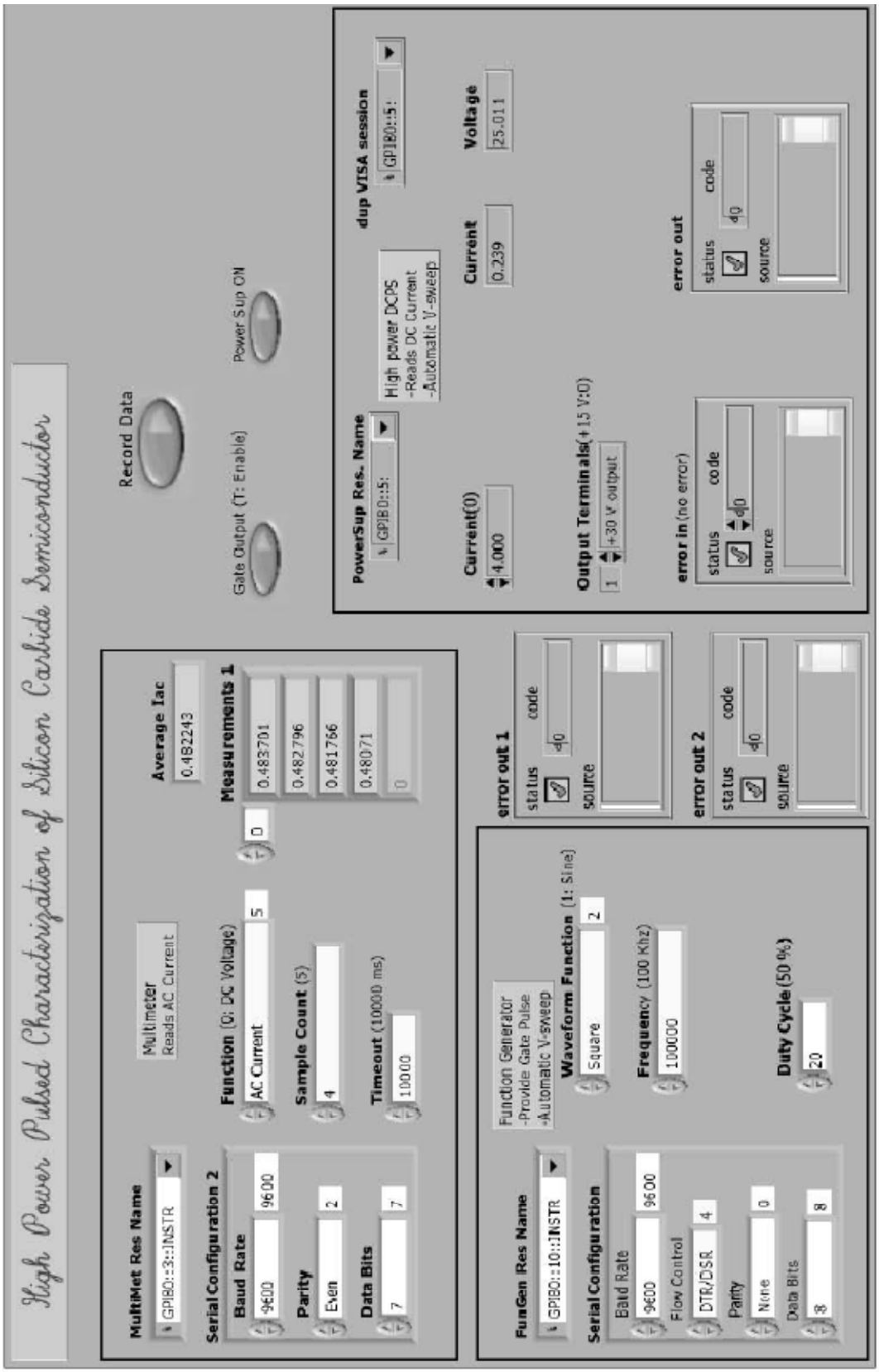


Figure 3-10. Labview VI interface for pulsed power characterization of SiC devices.

3.2.5 Capacitance measurements

The transient behavior and the frequency response of the devices are dominated by the junction capacitance of a device. “Keithley 510 CV analyzer” is used to measure the two terminal capacitance of JFET. The third terminal is left open during the measurements. The Figure 3-11 shows the gate-source (Cgs), gate-drain (Cgd) and drain to source (Cds) capacitances as a function of voltage across those terminals. The voltage sweep across the terminal is shown in x-axis and the measured value of capacitance is plotted on the y-axis. The third terminal is kept open while measuring the capacitance. As seen from the figure the Cgs and Cgd raises exponentially after a certain positive voltage, indicating the turn on of the forward biased diodes. Commercial power devices datasheets specify the input, output and reverse capacitance of the device, which are related to the two terminal capacitances as given by the following equations.

Input capacitance	$Ciss = Cgs + Ggd$	[3-2]
Output capacitance	$Coss = Cds + Ggd$	[3-3]
Reverse capacitance	$Crss = Cgd$	[3-4]

The input capacitance (Ciss) dominates over the output and reverse capacitances and hence a consideration in the gate drive design.

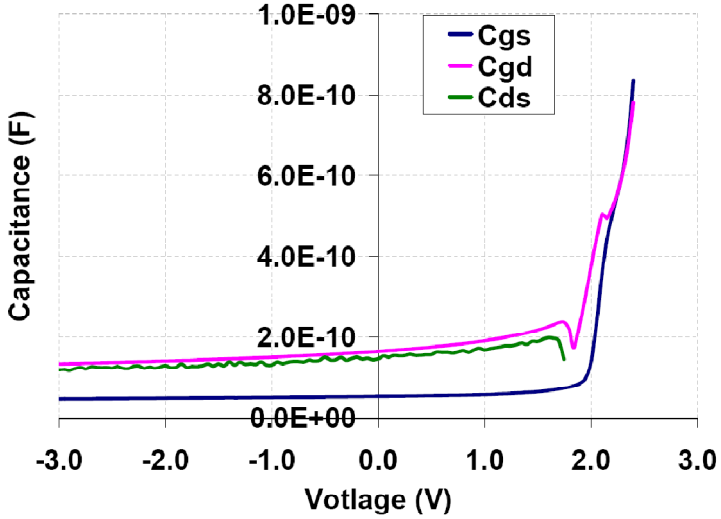


Figure 3-11. Two terminal capacitances of the JFET.

3.2.6 Verilog model of SiC JFET

Based on gate and drain characteristics and capacitance measurements, the extracted parameters are used to describe the behavior of the device in simulations. Verilog hardware description language is then used to model the behavior of the device and use in simulation of the SMPS design. A summary of parameters extracted from the measured characteristics with their temperature coefficients are given in Table 3-2. The Verilog mode file used in simulations is given in the appendix section.

Table 3-2. Basic model parameters of SiC E-mode JFET.

Parameter	Value	Units	Comment
Threshold voltage	1.1	V	At 25°C
Vt – temp coeff	-1.6	mV/ºC	
On resistance	<250	mΩ	Vgs = 2.5 V; 25ºC
Rds – temp coeff	+3	mΩ/°C	
Ciss	450	pF	Vgs = -1.0V; 27ºC
Crss	50	pF	Vgs = -1.0V; 27ºC
Conductance	5ms 4ms		Vgs = 2.0V; 27ºC Vgs = 2.5V; 275ºC

It must be noted that the model file given here is based on measurements from four devices. The JFET technology in silicon carbide is ever improving and the characteristics of the devices are expected to change and improve with every generation for the near term. It must also be stated that the modeling strategy for enhancement mode devices are carried out in similar to the (n-channel) MOSFETs. This is in contrast with the textbook equations for the JFETs which are usually applicable only for depletion mode devices. The simulated characteristics of the JFET based on the Verilog model are shown in Figure 3-12 and Figure 3-13. The Verilog model file used for simulation is provided in appendix section.11.1.

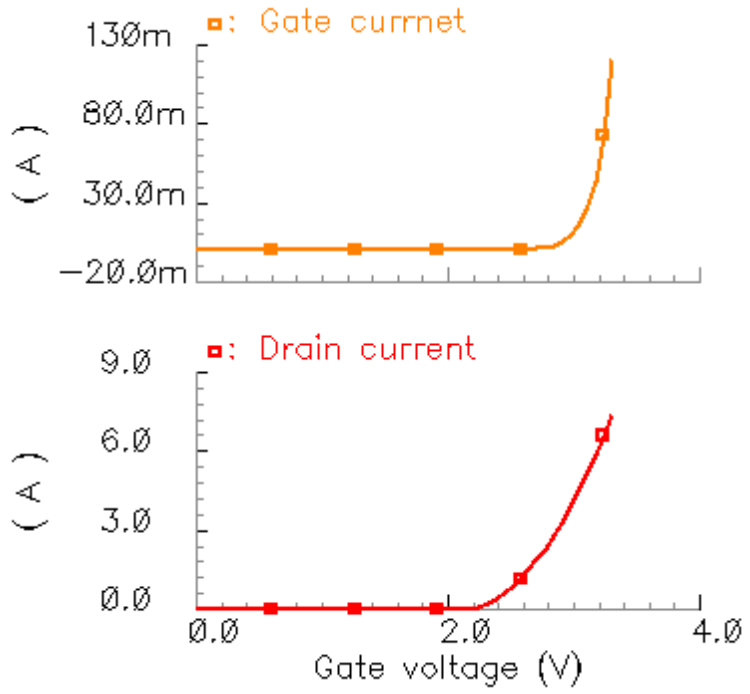


Figure 3-12. Simulated gate and drain current characteristics of the JFET based on Verilog model.

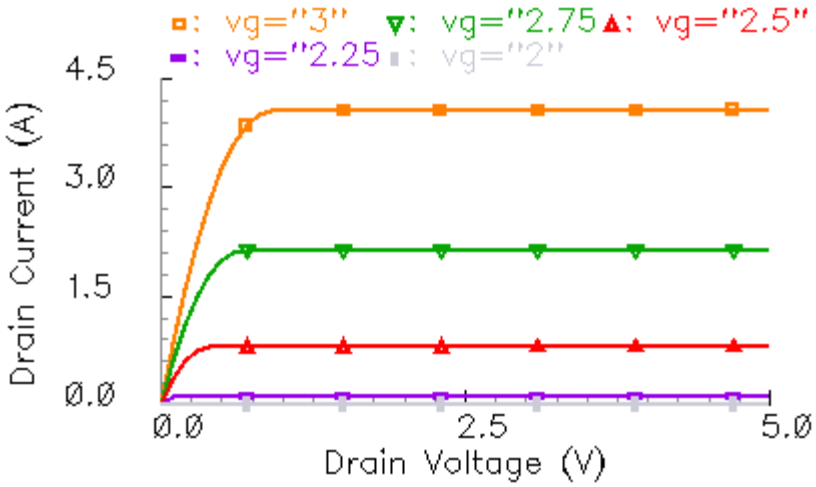


Figure 3-13. Simulated Id-Vd characteristics of the JFET based on Verilog model.

Chapter 4

4.1 Control circuitry

The on/off control of the power and synchronous switches is provided by control circuitry. The control unit forms the feedback part of the dc-dc conversion system. There are several different types of control mechanism adopted for various applications. The more common control modes are as follows.

- Voltage mode
- Current mode
- Vee-square (V2) mode
- V2I mode
- Hysteretic

A brief discussion about the individual mechanism is presented in following sections.

4.1.1 Voltage mode control

Voltage mode control of dc-dc converters is the earliest and easiest form and is still widely used. A simple block diagram for voltage mode control is given in Figure 4-1. In this mechanism an error amplifier produces an error voltage by comparing the output voltage with a preset reference voltage. The error voltage sets the threshold limit for the comparator which compares it to an artificial ramp (or sawtooth) and produces a pulse

width modulated output. An inverter is used to generate the complementary control signals for controlling the power and synchronous switch. The advantage of voltage mode control is its simplicity and fast transient response to load variations, limited by the control loop bandwidth. However the compensation scheme needed for stable operation of control loop is more complex.

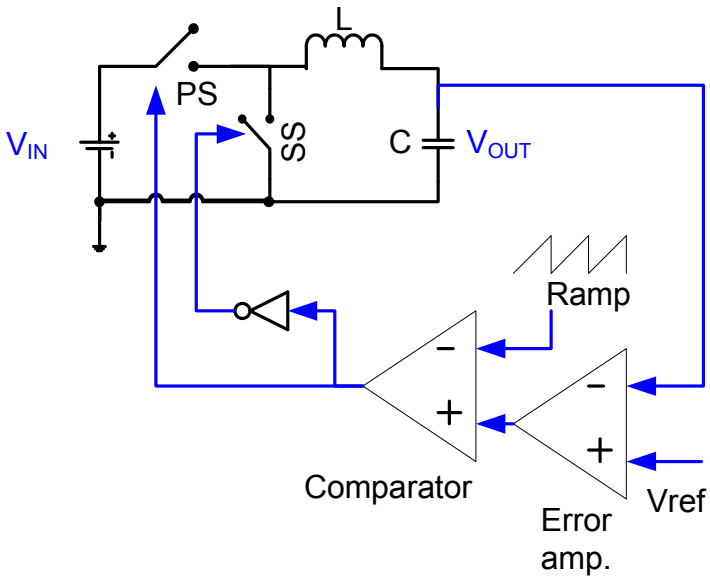


Figure 4-1. Voltage mode control of PWM converters.

The double pole response of the buck converter results in sharp phase drop near the natural resonant frequency. To obtain a required phase margin for the system, compensations schemes are required. The three commonly used compensation schemes for error amplifier are as follows:

- Type I compensation
- Type II compensation
- Type III compensation

4.1.2 Current mode control

Similar to voltage mode control a current mode control produces an error voltage based on the output voltage and a preset reference voltage. However instead of artificially generating a ramp waveform, the inherent ramp nature of inductor or transistor current is sensed and used. Figure 4-2 shows the block diagram of current mode control. The placement of sense resistor to monitor current is complicated as well as have a modest effect on the overall efficiency of the control scheme. An isolation transformer is used to sense the current in high power applications where a sense resistor is not efficient. Current mode control provides fast transient response to line variations and inherently protects from over currents. However the associated control circuitry is complicated and EMI problems were reported in the past.

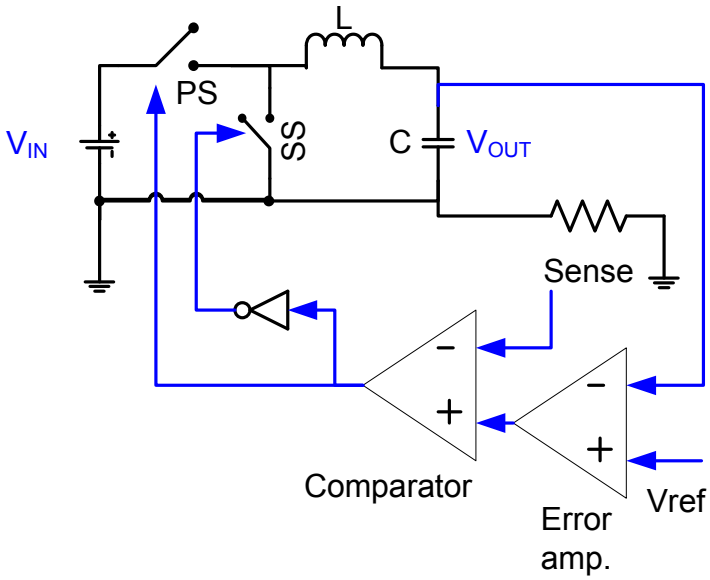


Figure 4-2. Current mode control of PWM converters.

The behavior of the error amplifier in current mode control is similar to voltage mode control and hence the compensation mechanisms are also same. A brief discussion of compensation schemes is later discussed in section 4.2.1.3.

4.1.3 Vee-square mode control

Vee-square (V2) control is used in this research work. This is a two loop control method that derives the ramp from equivalent series resistance (ESR) of load capacitor. Since the ramp is generated via the output voltage the dc output level is available in the ramp. This makes the transient response of V2 control loop much faster to load variations compared to voltage and current mode control, in particular to rising load demands. The operation of V2 control loop is explained using Figure 4-3.

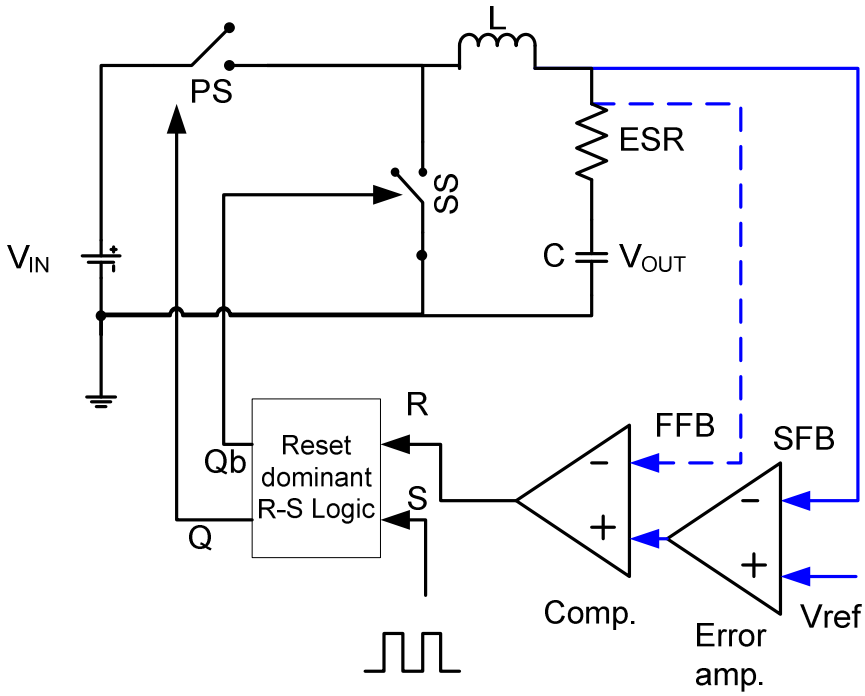


Figure 4-3. Vee-square mode control of PWM converters.

The outer loop that involves the error amplifier is in a slow feedback (SFB) mode that sets the dc accuracy of the output. The inner loop acts as a fast feedback (FFB) loop to address the transients in load. The reset dominant flip-flop logic is used to override the system clock based on the comparator output. In this way any sudden change in the load is more immediately addressed thereby provided a much smoother output voltage to transient changes in the load. Transient response is bound by the sum of the delay of comparator, logic and power switches, where the logic delay may typically be neglected.

In case of voltage and current mode control the error amplifier is required to have a larger bandwidth to track the transient changes in output. As a result controller power consumption is higher. In case of V2 control, the transients in load are directly monitored by the comparator and hence ease the bandwidth requirement of error amplifier. The resulting PWM is also significantly different from the conventional scheme described in section 2.3. Nevertheless the operation of the control is similar to the one previously discussed. A detailed operation of the system is later described in chapter 7.

4.1.4 Other control methods

In addition to the above mentioned control methods hysteretic control is another mode of control. Hysteretic control is also known as bang-bang control where a hysteretic comparator is used as a controller. The minimum hysteretic window that could be set using the comparator and the speed at which loop responds determines the output voltage ripple. Hysteretic converters do not have a fixed system clock and as a result generate greater Electro Magnetic Interference (EMI) related issues.

The EMI issues related to hysteretic control and PFM (described earlier) can be illustrated by considering load transients and corresponding output spectrum. Figure 4-4 illustrates the EMI issues of non PWM mode controllers. Different current levels shown in trace (a), represents 3 different loading conditions, I_1, I_2 and I_3. The pulse modulation characteristics of PFM and hysteretic controller are shown in trace (b) and trace (d) respectively. As mentioned before the pulse frequency increases proportional to the load current in PFM. In hysteresis mode, both pulse width and frequency changes with respect to load. The pulse width (both high and low) is limited by the loop (component) delay and largely depends on the load condition. This change in pulse frequency in these controller results in introducing spikes (noise) in the frequency domain based on its operating condition. Traces (c) and (e) shown the spurs introduced due to different operating conditions for PFM and hysteresis mode controllers. On comparison with

PWM control, where the spike occurs only at the (fixed) switching frequency, this distribution of spikes over frequency spectrum results in EMI issues.

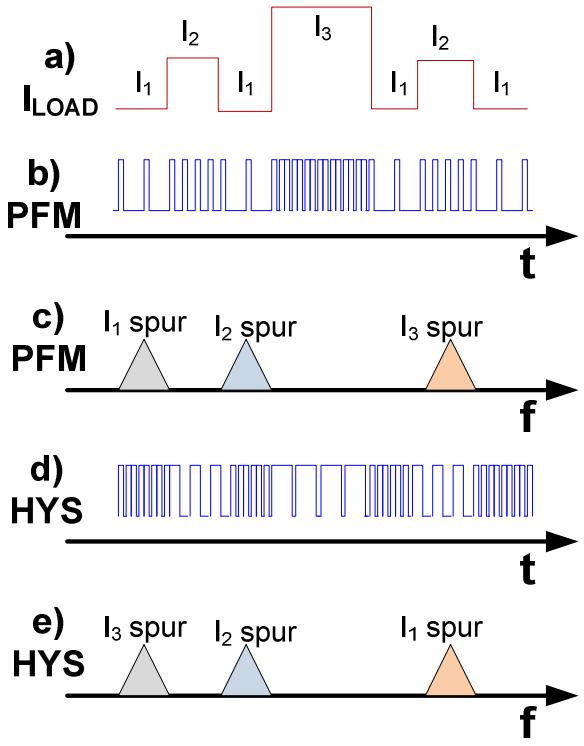


Figure 4-4. EMI issues with non PWM mode controls.

Recently V2I (Vee square I) mode control is proposed which combines a current mode converter to a V2 mode control. The performance of V2I control is comparable to V2 control with minor advantages in transient response.

4.2 Compensation in control loop

The goal for any control loop is to automatically adjust the system parameters to obtain the required output without any issue of instability. In circuit design, the control loop stability is characterized by observing the loop transfer function roll off in the frequency domain. It is desirable to have one dominant pole to provide -20dB/decade roll off at

unity gain cross over point and have the non dominant poles and zeros out of the spectrum of interest (at least 10 times away from switching frequency). This ensures the phase margin of a system is adequate enough for system stability. Often the natural response of the system has to be explicitly compensated to achieve this required response. General control systems theory discusses the various compensations schemes as

- Lag compensation
- Lead compensation
- Lag-Lead compensation

The same approaches in circuit design are commonly referred to

- Dominant pole compensation
- Feed forward compensation
- Pole-zero compensation

The feed-forward loop of the inductor-capacitor (LC) buck converter resembles a second order system that inherently provides a double pole at the output at a resonant frequency (ω_r) given by equation 4-1. This double pole provides a 180 degree phase shift of the input signal. In the feedback loop an additional 180 degree phase shift is introduced by the error amplifier or the comparator. This results in the total phase shift being potentially in excess of 360 degrees when error amplifier or comparator are considered and hence creates a potential oscillatory circuit rather than a stable control system. A properly compensation scheme is required to ensure the stability of the system. A general rule of thumb is to provide at least 75 degrees of phase margin for both good stability and a reasonable settling time (critically damped system).

$$\omega_r = \frac{1}{\sqrt{L \cdot C}} \qquad [4\text{-}1]$$

The frequency domain analysis of the control loop is analyzed in the following section to illustrate the need and effect of compensation.

4.2.1 Frequency domain analysis

Frequency domain analysis of control loops using the magnitude and phase plots (BODE plots) is the most popular technique and is discussed in the following section. The analysis is based on the frequency response of the individual blocks as given below. It must be noted the ideal expected behavior of the block / components are discussed here. A numerical illustration is provided in later sections to correlate the theory and design.

4.2.1.1 Output filter

The LC low pass filter in the forward path of the converter including the parasitic elements is shown in Figure 4-5. The schematic represents a second order system. The transfer function of this output filter is earlier derived in section 2.7. The equivalent series resistance of the output capacitor is included here since it plays a significant role in the control loop.

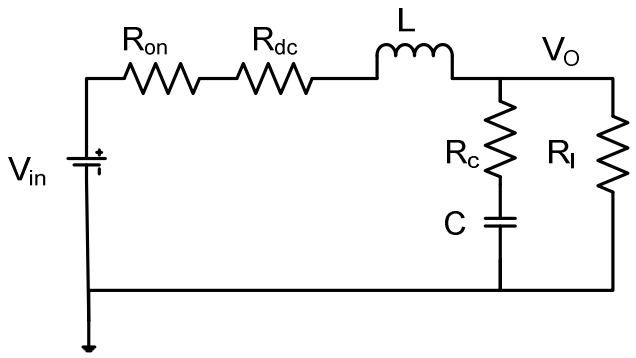


Figure 4-5. Schematic of feed forward path of buck converter including parasitic elements.

The modified second order system can be described by equation 4-2. It can be noted that the numerator of the transfer function introduces a zero. The zero frequency is introduced via the output capacitance and its equivalent series resistance (ESR), R_c. Most dc-dc converters depend upon the equivalent series resistance of the capacitor for stable operation of converters. The ESR zero cancels the effect of double pole thereby resulting in a -20 dB/decade roll off beyond the ESR frequency. This can be easily observed from the magnitude bode plot as shown in Figure 4-6. The gain rolls off at -40 dB/decade past

the natural resonance frequency (ω_{LC}) of the LC network. The zero introduced by the ESR at ω_{ESR}, gives a gain and phase boost reducing the gain roll off to -20 dB/decade. The phase plot is not explicitly shown here.

$$\frac{Vo(s)}{Vin(s)} = \frac{\left(1+\frac{s}{\omega_{ESR}}\right)}{s^2 + s\cdot\left(\frac{R_x}{L}+\frac{1}{C\cdot R_l}\right)+\left(\frac{1+R_x/R_l}{L\cdot C}\right)} \qquad [4\text{-}2]$$

where $\omega_{ESR} = \frac{1}{2\cdot\pi\cdot R_c\cdot C}$

and $R_x = R_{on} + R_{dc}$

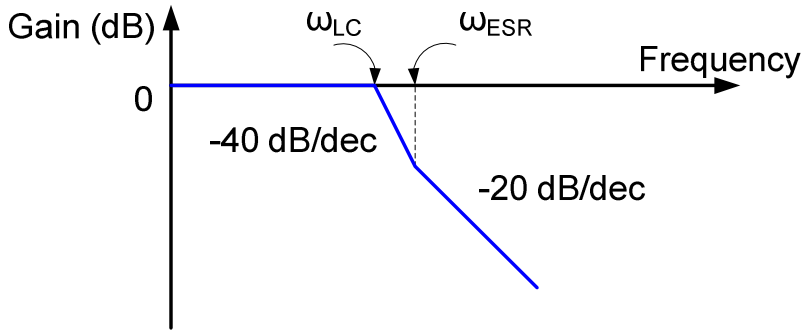


Figure 4-6. Magnitude response of second order LC system with ESR effiect.

4.2.1.2 Feedback loop

In the V2 feedback loop the cascade connection of error amplifier and comparator are the dominant blocks and their transfer functions are analyzed. The ideal magnitude response of the error amplifier based on its transfer function described by equation 4-3 is given in Figure 4-7. The expected response of the comparator is also shown in the same figure. The dominant pole of the error amplifier and its unity gain cross over frequency based on the transfer function is given by equation 4-4 and 4-5, where 'r_O' is the output resistance

of error amplifier, ‘gm’ is the transconductance of error amplifier and ‘C’ is the effective load capacitance.

$$TF = \frac{v_o}{v_i} \approx (gm \times r_o)\left[\frac{\left(\frac{C}{gm}\right)s + 1}{1 + (r_o \times C)s}\right] \qquad [4\text{-}3]$$

$$\omega_{rc} = \frac{1}{r_O \times C} \qquad [4\text{-}4]$$

$$\omega_{0A} = \frac{gm}{C} \qquad [4\text{-}5]$$

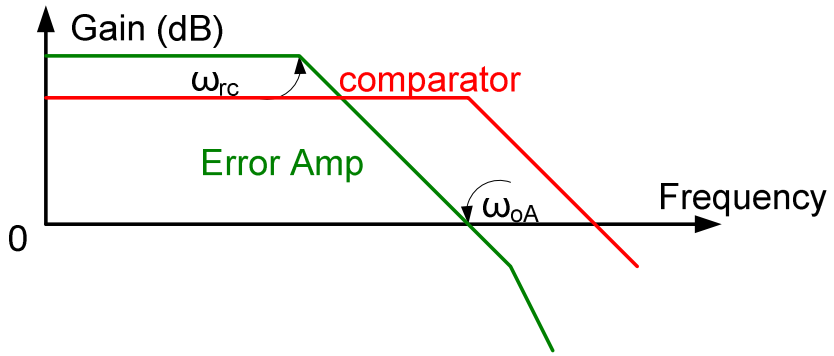


Figure 4-7. Frequency response of comparator and error amplifier blocks.

With the frequency response characteristics of the individual blocks the overall ‘control to output voltage’ response can be obtained by adding their gains in the log scale (dB). The Bode magnitude plot of the overall system is demonstrated or estimated in Figure 4-8. As it can be seen the roll off at unity gain is -40dB/decade. Except for the case with extremely high dc gain the double pole roll off would yield poor phase margin (almost close to zero) and hence causes potential instability.

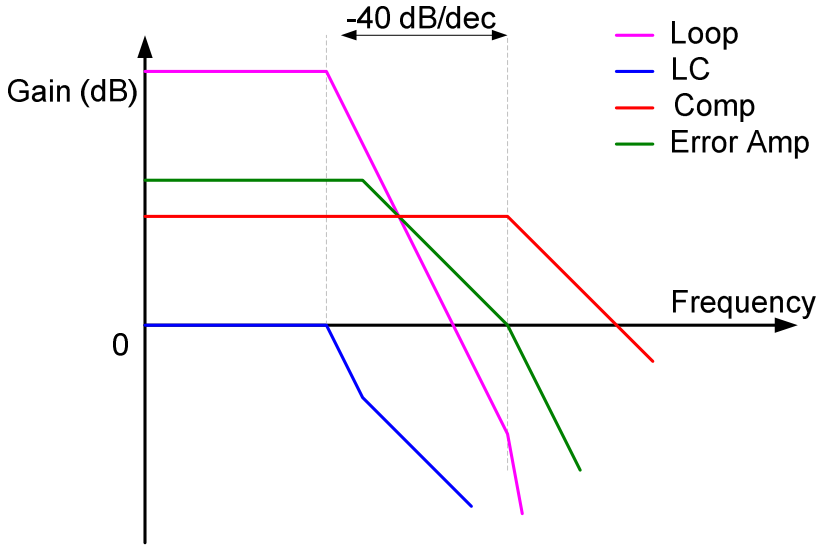


Figure 4-8. Magnitude response of loop transfer function versus frequency.

4.2.1.3 Compensation

In order to compensate the system and obtain a -20dB /decade roll off a capacitor is used at the output of the error amplifier as a compensation element. The selection of a capacitor is such that it reduces or moves the dominant pole of the error amplifier to a very low frequency. In other words addition of compensation capacitor limits the speed of the error amplifier such that the transient response is only controlled by the feedback through comparator. Considering the error amplifier individually, adding a compensation capacitor reduces the bandwidth of the error amplifier and moves its dominant poles to a lower frequency in the spectrum. This reduced bandwidth results in slower response time for the error amplifier. Hence the error amplifier path is referred to 'slow feedback path' and is not responsive to the transients at the load. Also the cascade configuration of comparator and error amplifier provides a very high DC gain for better accuracy of output voltage. The effect of capacitor on the magnitude response is shown in Figure 4-9. The modified dominant pole and gain crossover frequency of the error amplifier after compensation is given by equation 4-6 and 4-7, respectively (details in section 4.2.4).

$$\omega_{rc} = \frac{1}{r_O \times C_C} \qquad [4\text{-}6]$$

$$\omega_{0A} = \frac{gm}{C_C} \qquad [4\text{-}7]$$

where Cc is the compensation capacitor

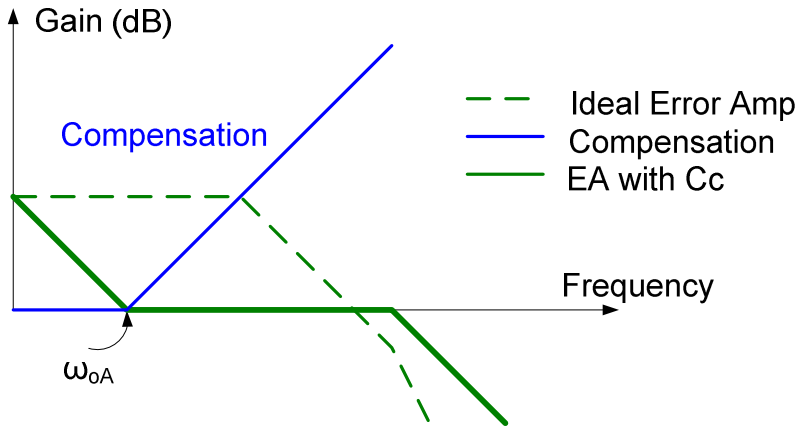


Figure 4-9. Effect of compensation capacitor on error amplifier.

The selection of compensation capacitor is such that the frequency where zero is introduced is 1/10th of the LC double pole frequency. This concept is further expanded in the error amplifier design discussed in chapter 6.

The overall response of the loop with the compensation capacitor can be obtained by adding the response of individual blocks. Figure 4-10 shows the overall open loop magnitude response. It can be observed that the roll off at unity gain is -20 dB/decade.

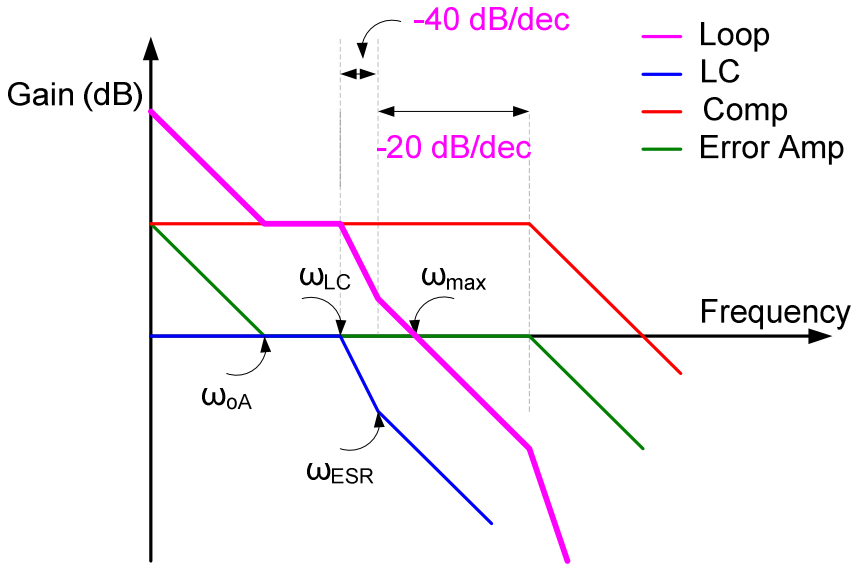


Figure 4-10. Compensated magnitude response of the control to output loop.

A higher loop bandwidth reduces the settling time for the output and hence improves transient response. However the total control system is based on the sampled data system controlled via the loop clock. Hence the maximum operation frequency of the control loop has to be a considerable factor (usually greater than two) of the loop bandwidth (ω_{max}) to satisfy the Nyquist sampling rate.

In order to illustrate the simplicity of the compensation mechanism in vee-square control, a brief analysis of type I, type II and type III compensations used in conventional control methods are described below.

1. Type 1 compensation

Type 1 compensation is the simplest dominant pole compensation of the error amplifer as shown in Figure 4-11. It resembles the transfer function of a simple integrator represented by equation 4-8.

$$\frac{Vo}{Vin} = -\frac{1}{s \cdot R_1 \cdot C_1} \qquad [4\text{-}8]$$

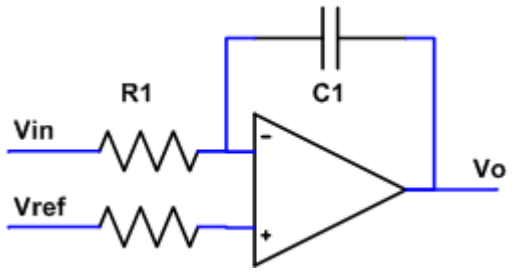


Figure 4-11. Type 1 compensation of error amplifier.

2. Type 2 compensation

Type 1 compensation is seldom used in practical applications since the bandwidth of error amplifier is strictly limited in this case. For wider bandwidth, type 2 compensation as shown in Figure 4-12 is used. Here using additional components in feedback a pole zero pair is introduced to extend the dominant pole of error amplifier. Hence by adding a second degree of freedom, type 2 compensation provides wider bandwidth for error amplifier compared to type 1. The transfer function of type 2 compensation is given by 4-9.

$$\frac{Vo}{Vin} = \frac{R_2 \cdot C_2 \cdot s + 1}{s \cdot R_1 \cdot (C_1 + C_2) \cdot \left(\left(R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2} \cdot s \right) + 1 \right)} \qquad [4\text{-}9]$$

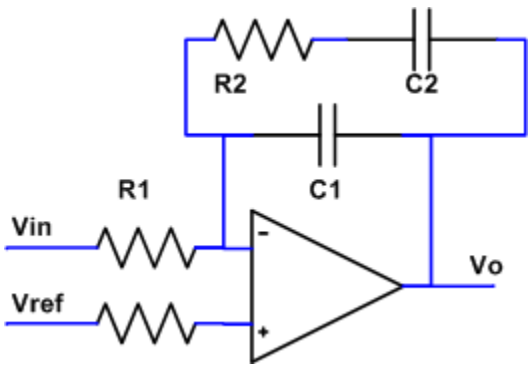


Figure 4-12. Type 2 compensation of error amplifier.

3. Type 3 compensation

Similar to type 2compensation, type 3 compensation introduces more components in the system as shown in Figure 4-13 to allow higher degree of freedom. In reality it introduces two pole-zero pairs to extend the bandwidth of the error amplifier to very high value. The transfer function of the type 3 compensation network is given by 4-10.

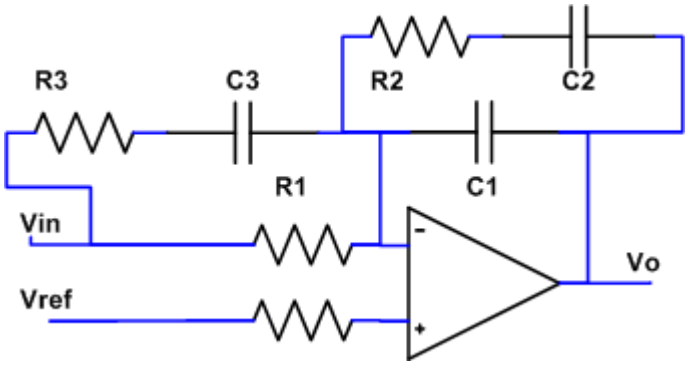


Figure 4-13. Type 3 compensation of error amplifier.

$$\frac{Vo}{Vin} = \frac{(R_2 \cdot C_1 \cdot s + 1) \cdot [(R_1 + R_3) \cdot (C_3 \cdot s) + 1]}{s \cdot R_1 \cdot (C_1 + C_2) \cdot \left(\left(R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2} \cdot s \right) + 1 \right) \cdot (R_3 \cdot C_3 \cdot s + 1)} \qquad [4\text{-}10]$$

It must be evident that the complexity in compensation required for error amplifier to run as fast as system clock as system clock frequency increases is tremendous. On the other hand the compensation for error amplifier in vee-square control requires one simple capacitor since the error amplifier is in slow feedback path. The reduced component count increases reliability of vee-square control particularly at elevated temperature operations.

Understanding and design of system based on classical control theory has been a wide spread practice among engineers. However the modern control theory design based on state space yield more mathematical insights towards the system and is described in the following section.

4.2.2 State space analysis

The state space analysis provides the transfer function of the system to model its behavior. A state space model is required to determine the transient behavior of the system. While the frequency domain analysis discussed in the previous section ensures stability in frequency domain under steady state condition, the transient response can be obtained using the complete transfer function representation. The stability of a system can also be determined from the state matrices of the system. Above all, the state space analysis is useful in describing the effect of individual elements of the control loop and hence the most appropriate procedure to follow for the controller design.

The general state equations and output equations of any system is described by equations 4-11 and 4-12, respectively.

$$\dot{x} = Ax + Bu \qquad [4\text{-}11]$$

$$y = Cx + Eu \qquad [4\text{-}12]$$

Where X is the state variable, Y is the output variable, U is the input variable and A, B, C and E are co-efficient matrices. (The variable E is used since D is used to represent the duty cycle of the converter, later in the analysis). The inductor current and capacitor voltages are commonly used as the state variables of the system. For PWM based converters the system can be analyzed independently using the ON time and OFF time equivalent circuits. The ON-time equivalent circuit is shown in Figure 4-14. The parasitic components are included to obtain a more accurate model; R_{on} represents the on resistance of the transistor and the R_L represents the inductor series resistance.

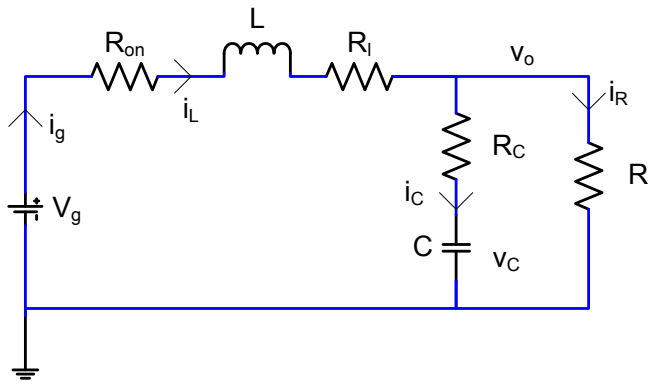


Figure 4-14. ON time equivalent circuit of the buck converter.

4.2.2.1 ON time analysis

For the ON time equivalent circuit, the basic equations using the KVL and KCL are given by equation 4-13 and 4-14, respectively. The state equation in terms of inductor current and capacitor voltage is given by 4-15 through 4-18.

$$v_g(t) = i_L(t)\left[R_{on} + R_l\right] + L\frac{di_L(t)}{dt} + v_O(t) \qquad [4\text{-}13]$$

$$i_g(t) = i_L(t) = i_R(t) + i_C(t) \qquad [4\text{-}14]$$

where,

$$i_C(t) = C \cdot \frac{dv_C(t)}{dt} = i_L(t) - i_R(t) \qquad [4\text{-}15]$$

and

$$v_O(t) = i_R(t) \times R = v_C(t) + i_C(t) \times R_C \qquad [4\text{-}16]$$

From 4-13,

$$L\frac{di_L(t)}{dt} = v_g(t) - v_O(t) - i_L(t)\left[R_{on} + R_l\right] \qquad [4\text{-}17]$$

From 4-16 and 4-17,

$$L\frac{di_L(t)}{dt} = v_g(t) - \left[v_C(t) + i_C(t) \times R_C\right] - i_L(t)\left[R_{on} + R_l\right] \qquad [4\text{-}18]$$

From 4-15 and 4-16, $C \times \frac{dv_C(t)}{dt} = i_C(t) = i_L(t) - i_R(t) = i_L(t) - \frac{v_C(t) + i_C(t) \times R_C}{R}$ [4-19]

After few steps of algebra,

$$C \times \frac{dv_C(t)}{dt} = i_L(t) \times \left(\frac{R}{R + R_C} \right) - v_C(t) \times \left(\frac{1}{R + R_C} \right) \quad [4\text{-}20]$$

Substituting for $i_L(t)$ from 4-20 in 4-18 and after some algebraic manipulations,

$$\frac{di_L(t)}{dt} = v_g(t) - v_C(t) \times \left(\frac{R \times R_C}{R + R_C} \right) - i_L(t) \times \left[R_{on} + R_L + \frac{R \times R_C}{R + R_C} \right] \quad [4\text{-}21]$$

From equations 4-20 and 4-21 the state equations for the on-time equivalent circuit is given as follows

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{dv_C(t)}{dt} \end{bmatrix} = \begin{bmatrix} -\left(R_{on} + R_l + \frac{R \times R_C}{R + R_C} \right) & -\frac{R}{R + R_C} \\ \frac{R}{R + R_C} & \frac{-1}{R + R_C} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} \begin{bmatrix} v_g(t) \end{bmatrix} \quad [4\text{-}22]$$

The output equation derivation is as follows:

From 4-16, $$v_O(t) = v_C(t) + i_C(t) \times R_C = v_C(t) + C \times \frac{dv_C(t)}{dt} \times R_C \quad [4\text{-}23]$$

Substituting for $\frac{dv_C(t)}{dt}$ from 4-20 and solving for $v_O(t)$,

$$v_O(t) = v_C(t) \times \left(\frac{R}{R + R_C} \right) + i_L(t) \left(\frac{R \times R_C}{R + R_C} \right) \quad [4\text{-}24]$$

Therefore the output equation is given by,

$$\begin{bmatrix} v_O(t) \\ i_g(t) \end{bmatrix} = \begin{bmatrix} \left(\frac{R \times R_C}{R + R_C}\right) & \frac{R}{R + R_C} \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} \begin{bmatrix} v_g(t) \end{bmatrix} \quad [4\text{-}25]$$

The state and output matrices (ABCE) for ON state equivalent circuit are given by 4-26 through 4-29.

$$A1 = \begin{bmatrix} -\frac{1}{L}\left(R_{on} + R_l + \frac{R \times R_C}{R + R_C}\right) & -\frac{1}{L}\frac{R}{R + R_C} \\ \frac{1}{C}\frac{R}{R + R_C} & \frac{1}{C}\frac{-1}{R + R_C} \end{bmatrix} \quad [4\text{-}26]$$

$$B1 = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \quad [4\text{-}27]$$

$$C1 = \begin{bmatrix} \left(\frac{R \times R_C}{R + R_C}\right) & \frac{R}{R + R_C} \\ 1 & 0 \end{bmatrix} \quad [4\text{-}28]$$

$$E1 = 0 \quad [4\text{-}29]$$

4.2.2.2 OFF time analysis

The off state equivalent circuit of the buck converter is shown in Figure 4-15. During off state the equivalent circuit is similar to ON state, except that the generator voltage is zero. Therefore the only change in the state equation is that the matrix B is zero. The output equation remains the same.

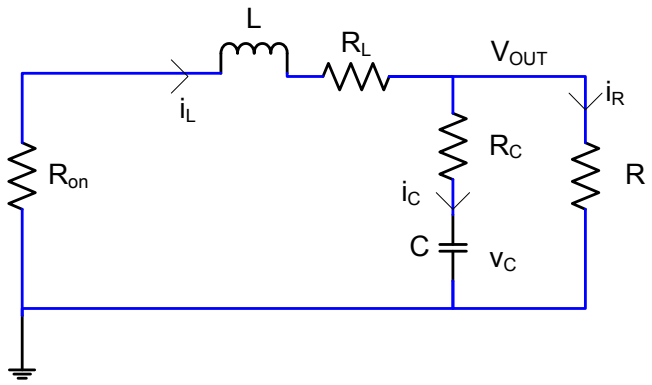


Figure 4-15.OFF time equivalent circuit of buck converter.

As the ON state and OFF state representation of the buck converter are individually obtained, based on an state space averaging technique reported by Middlebrook and Cuk [74], the coefficient matrices of the averaged system can be computed as given below. The variable 'd' represents the duty cycle. The state and output matrices are weighted (time averaged) based on the duty cycle where the multiplication by represents ON time weighting and (1-d) represented OFF time weighting.

$$A = A1 * d + A2 * (1 - d) \quad [4\text{-}30]$$

$$B = B1 * d + B2 * (1 - d) \quad [4\text{-}31]$$

$$C = C1 * d + C2 * (1 - d) \quad [4\text{-}32]$$

$$E = E1 * d + E2 * (1 - d) \quad [4\text{-}33]$$

Equation 4-30 through 4-33 represents the state and output matrices of the time averaged buck converter. For a buck converter the steady state output voltage (Vo) and input voltage (Vg) are related to duty cycle (d) as given by equation 4-34.

$$d = \frac{Vo}{Vg} \quad [4\text{-}34]$$

Therefore a change in output load of the power supply translates into a change in output voltage and a corresponding change in duty cycle to maintain the steady state output. This requires analysis of output voltage to duty cycle transfer function also known as control to output transfer function in order to determine the stability of the system.

4.2.3 Small signal analysis

Small signal analysis is used to obtain control to output transfer function of the buck converter. The small signal analysis is performed by perturbing the system variables around the dc operating point. The state matrix, output matrix and duty cycle can be represented by the steady state parameter plus a small signal values is given by equations 4-35 to 4-37.

$$x = X + \hat{x} \qquad [4\text{-}35]$$

$$y = Y + \hat{y} \qquad [4\text{-}36]$$

$$d = D + \hat{d} \qquad [4\text{-}37]$$

Where the upper case letters represent steady state DC parameters and lower case letters with 'hat' represent small signal values. Recognizing that the derivatives of steady state parameters are zero, the state equation can be described in terms of coefficient matrices and small signal parameters as given below (4-38).

From 4-11, 4-30 and 4-31,

$$\dot{\hat{x}} = \left\{[A1(D+\hat{d}) + A2(1-(D+\hat{d}))] \bullet [X+\hat{x}]\right\} + \left\{[B1(D+\hat{d}) + B2(1-(D+\hat{d}))] \bullet [U+\hat{u}]\right\} \qquad [4\text{-}38]$$

We know that the matrix A1 = A2 and B2 = 0. Further assuming that the input voltage is constant yields,

$$\dot{\hat{x}} = [A1 \cdot [X + \hat{x}] + B1(D + \hat{d})][Vg] \qquad [4\text{-}39]$$

Since the duty cycle is modulated and presents itself as an input to the system, the above equation is non linear. The equation can be linearized by small signal restriction and omitting the product of ac terms [75, 76]. This result in small signal state equation as given below,

$$\dot{\hat{x}} = [A1 \cdot \hat{x}] + B1(\hat{d})][Vg] \qquad [4\text{-}40]$$

Taking the Laplace transform of the functions and rearranging,

$$\hat{x}(s) = [sI - A1]^{-1} \cdot B1 \cdot \hat{d}(s) \cdot [Vg] \qquad [4\text{-}41]$$

where I is the identity matrix and s is Laplace operator.

The relation between the output voltage and the duty cycle is obtained as

$$\hat{v}_O(s) = C \cdot \hat{x}(s)C \cdot [sI - A1]^{-1} \cdot B1 \cdot V_g \cdot \hat{d}(s) \qquad [4\text{-}42]$$

Therefore,
$$\frac{\hat{v}_O(s)}{\hat{d}(s)} = C \cdot [sI - A1]^{-1} \cdot B1 \cdot V_g$$

The above equation gives the effect of small signal duty cycle on the output voltage. After substituting the coefficient matrices and algebraic manipulations the standard form of transfer function is given as in 4-43.

$$\frac{\hat{v}_O(s)}{\hat{d}(s)} =$$

$$V_g\left[\frac{R(1+sCR_C)}{s^2LC(R+R_C)+s(C(R(R_l+R_C+R_{on})+R_C(R_l+R_{on}))+L)+(R_l+R_C+R_{on})}\right]$$

[4-43]

In similar fashion the load current to duty cycle, output voltage to input voltage and the output voltage to output current transfer functions can also be derived. Since these are not of major interest at this juncture, they are not explicitly discussed [77].

4.2.4 Loop transfer function

The control to output transfer functions is obtained from the small signal analysis of the buck converter as detailed in previous section. In his section the compensator transfer function is obtained. The compensator transfer function represents the feedback characteristics that show the effect of change in output voltage on the duty cycle. The overall block diagram is shown in Figure 4-16. The closed loop system is analyzed by breaking the loop at the output node and applying a small signal perturbation.

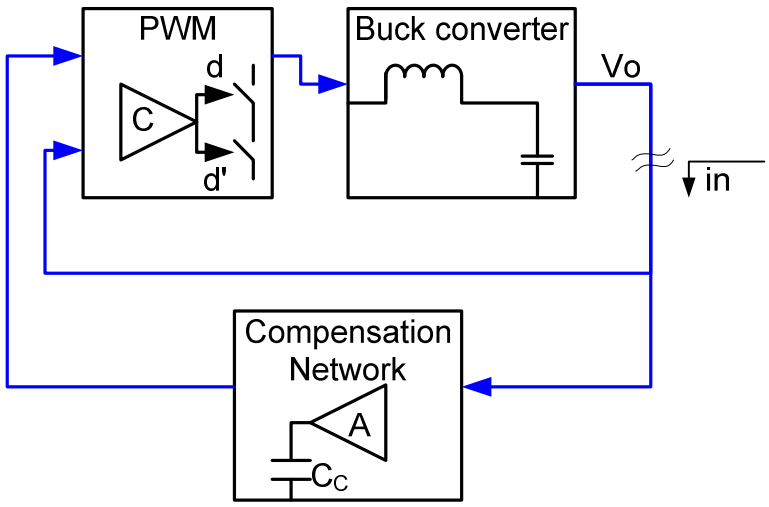


Figure 4-16. Block diagram of V2 control buck converter.

The analysis of the cascaded compensation network and the PWM circuit is observed initially. This is later added to the control to output buck converter part to obtain the overall loop transfer function of the system.

Considering the circuit model of the compensation network (error amplifier and capacitor) and the PWM (comparator) individually as shown in Figure 4-17 the equation for the output voltage V_o can be expressed as given by equation 4-44.

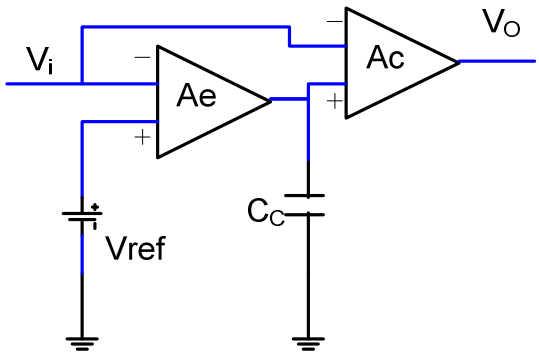


Figure 4-17. Equivalent circuit for analysis of compensation network,

$$Ac\left(-v_i - \frac{v_i \times Ae}{1+\tau s}\right) = v_o \qquad [4\text{-}44]$$

where Ac and Ae are the open loop gain of comparator and error amplifier, respectively. Through the following discussion we have justifiably assumed that bandwidth if the OTA is much less than that of the comparator. Rearranging the equation,

$$\frac{v_o}{v_i} = -Ac\left[1 + \frac{Ae}{1+(r_o \times C_c)s}\right] \qquad [4\text{-}45]$$

$$\frac{v_o}{v_i} = -Ac\left[\frac{1+(r_o \times C_c)s + gm \times r_o}{1+(r_o \times C_c)s}\right] \qquad [4\text{-}46]$$

where gm and r_o are the transconductance and output resistance of the error amplifier. Cc is the value of compensation capacitor.

$$\frac{v_o}{v_i} \approx -Ac\left[\frac{(r_o \times C_c)s + gm \times r_o}{1 + (r_o \times C_c)s}\right] \quad [4\text{-}47]$$

$$\frac{v_o}{v_i} \approx -Ac \times (gm \times r_o)\left[\frac{\left(\frac{C_c}{gm}\right)s + 1}{1 + (r_o \times C_c)s}\right] \quad [4\text{-}48]$$

$$\frac{v_o}{v_i} \approx -Ac \times Ae\left[\frac{\tau_z s + 1}{1 + \tau_p s}\right] = -Ac \times Ae\left[\frac{\frac{s}{\omega_z} + 1}{1 + \frac{s}{\omega_p}}\right] \quad [4\text{-}49]$$

where the ωp and ωz is the pole and zero frequency of feedback path.

$$\omega_p = \frac{1}{r_o \times C_c} \quad [4\text{-}50]$$

$$\omega_z = \frac{gm}{C_c} \quad [4\text{-}51]$$

Therefore the overall (open) 'loop transfer function' that includes the control to output and output to duty cycle transfer blocks can be obtained from 4-49 and 4-43 as given below 4-52.

$$TF = -Ac \times Ae \times V_g \times \left[\frac{\frac{s}{\omega_z} + 1}{1 + \frac{s}{\omega_p}} \right] \times$$

$$\left[\frac{R(1 + sCR_C)}{s^2 LC(R + R_C) + s(C(R(R_l + R_C + R_{on}) + R_C(R_l + R_{on})) + L) + (R_l + R_C + R_{on})} \right]$$

[4-52]

The transfer function yields information about the low frequency or DC gain and the pole and zero locations of the buck converter including the parasitics. This transfer function remains valid as long as the phase delay of the comparator, logic and power switches remains small relative to the OTA. This is readily observed via the previous Bode analysis.

4.3 Effect of components

The transfer function derived in the previous section provides a more accurate representation of the system since the parasitic are included in the model. It should be noted that not every parameter affects the system performance equally in all domains. Assumptions need to be made to simplify the system for better understating. To facilitate this task, the estimated operating values of the individual parameters for a 5V converter are summarized in Table 4-1. The comments has been made to indicate the effect of the parameter in the feedback loop using the bode analysis.

Table 4-1. Estimated values of components of SMPS.

Symbol	Parameter	Expected value	Temperature coefficient	Remarks
Ac	Comparator DC gain	≥ 50	Positive	Higher gains reduces systematic offset but introduce stability issues
Ae	Error amplifier DC gain	≥ 100	Positive	
Rc	ESR of capacitor	≥ 20 mΩ	Positive	Plays significant role in compensation
Ron	Transistor ON resistance	≤ 2 Ω	Positive	Higher resistance implies higher loss
Rl	DC resistance of inductor wire	≤ 2 Ω	Positive	
L	Output inductance	> 65µH	Negative	Changes affects the required value of compensation capacitor
C	Output capacitance	> 220µF	Positive	
Vin	Input voltage	≥ 10 V	-	
R	Load resistance	1Ω	-	
Cc	Compensation capacitor	>1nF	Negative	-

To summarize, a high dc gain in error amplifier reduces the systemic offset, and loop gain is the product of comparator gain by error amplifier gain in the feedback loop. Comparator gain must be adequate to convert ripple error to a valid logic level i.e. $VDD/V_{ripple} > 50^{+}$ for 2% regulation. However high gain systems are difficult to compensate for a fixed switching frequency since it requires larger filter components to roll off the gain. As discussed before the ESR of the output capacitor plays a major role in compensation and hence must be carefully chosen. The value of output capacitor and inductor depends on the system requirement. The methods to select these components are

discussed in later chapters; however the value of compensation capacitor is based on the output filter and hence has to be considered in parallel. Any dc parasitic resistance contributes to loss and hence must be minimized.

4.3.1 Effect of parasitics

The parasitic elements in the design components has significant role on the system stability. A bode analysis of the transfer function with different (Equivalent Series Resistance) ESR values is shown in Figure 4-18. The figure shows the effect of ESR on the control loop stability. The blue curves show represents a zero ESR condition where the phase margin is lesser than 20 degrees. The green curve represents a 20 mΩ ESR which introduces a zero in the transfer function. The zero provides phase and gain boost, resulting in 65 degrees of phase margin. Similarly the effect of the parasitic resistances is shown in Figure 4-19.

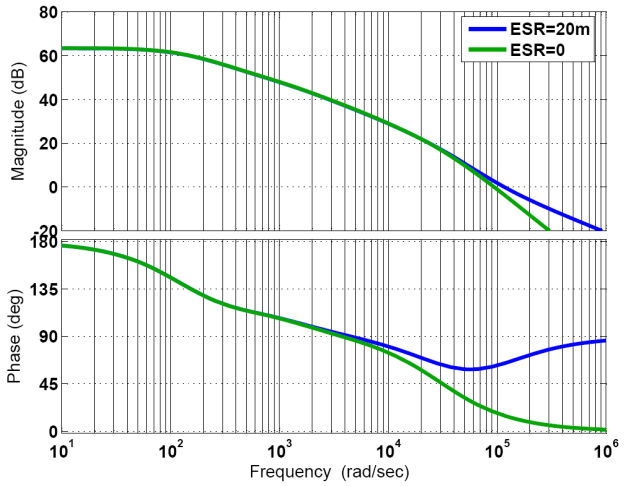


Figure 4-18. Effect of ESR on the phase margin of the control loop.

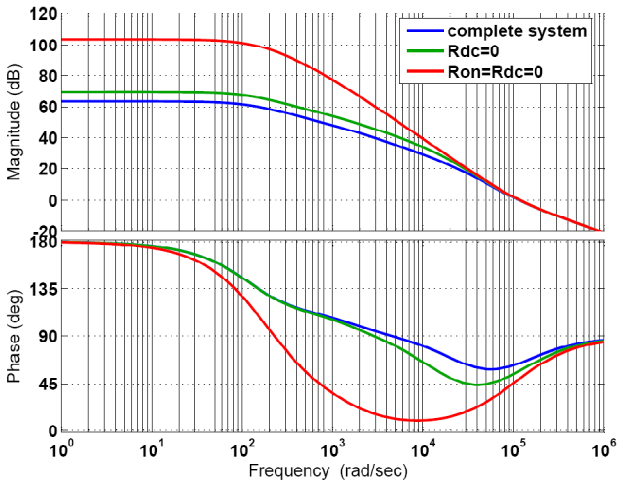


Figure 4-19. Effect of parasitic resistances on the control loop.

As it can be seen from the Figure 4-19 the DC gain is severely attenuated by the parasitic resistances however the bandwidth and gain cross over frequencies remains unaffected. The difficulties in compensating high gain systems can also be observed from the figure as the top (red) curve marginally passes the phase margin requirement (45 degrees). A larger ESR is required in such cases to compensate the system. The plot indicates the importance role that parasitic can in the system design since a zero parasitic provides lower phase margin than the actual system for given ESR. This actually eases the compensation design and enhances system performance.

4.3.2 Robust control design

Detailed analysis of the control theory presented above is based on the assumption of linear model of the equivalent circuit. Exact values of components used in system must be known to guarantee the system stability. However in practice, the components values vary a wide range over the operating temperature, and it is necessary to analyze the robust stability of the system.

An exhaustive analysis of stability of any control system can be analyzed using Kharitonov polynomials [78, 79]. The Kharitonov theorem states that for an interval polynomial as shown in equation 4-53 whose coefficients a_i has a real boundary limit

$[x_{imin}, x_{imax}]$, the interval polynomial is stable if and only if the four Kharitonov polynomials are stable. The Kharitonov polynomials are given by 4-54 through 4-57. Since the stability of the interval polynomial is dependent upon the stability of the four Kharitonov polynomials, this method is widely used to establish the robustness of a control system.

$$P(s) = a_0 + a_1 s^1 + a_2 s^2 + \ldots + a_n s^n \qquad [4\text{-}53]$$

where, $a_i \in \Re$; $x_{imin} \leq a_i \leq x_{imax}$

$$F_1(s) = x_{0min} + x_{1min} s^1 + x_{2max} s^2 + x_{3max} s^3 + x_{4min} s^4 + x_{5min} s^5 + x_{6max} s^6 + \ldots \qquad [4\text{-}54]$$

$$F_2(s) = x_{0min} + x_{1max} s^1 + x_{2max} s^2 + x_{3min} s^3 + x_{4min} s^4 + x_{5max} s^5 + x_{6max} s^6 + \ldots \qquad [4\text{-}55]$$

$$F_3(s) = x_{0max} + x_{1min} s^1 + x_{2min} s^2 + x_{3max} s^3 + x_{4max} s^4 + x_{5min} s^5 + x_{6min} s^6 + \ldots \qquad [4\text{-}56]$$

$$F_1(s) = x_{0max} + x_{1max} s^1 + x_{2min} s^2 + x_{3min} s^3 + x_{4max} s^4 + x_{5max} s^5 + x_{6min} s^6 + \ldots \qquad [4\text{-}57]$$

A worksheet to analyze the robust stability using Kharitonov theorem is shown in Table 4-2. The analysis is based on the maximum and minimum values of the components (capacitors and inductors) described later in Chapter 7. The process is to analyze the stability of Kharitonov polynomials which are formed by the coefficients obtained from the maximum and minimum value of the system components.

Table 4-2. Worksheet to analyze Kharitonov robust stability analysis of buck converter.

	max	min	
c	1.00E-03	1.00E-04	output capacitance
l	1.00E-04	1.00E-05	output inductance
r	1.00E+03	1.00E+00	load resistance
rc	1.00E-01	5.00E-03	ESR of output capacitance
rl	2.00E+00	1.00E-01	ESR of output inductance
ron	2.00E+00	3.00E-01	On resistance of switch
vg	2.50E+01	5.00E+00	Input raw voltage
ae	1.00E+03	1.00E+03	Error amplifier gain
ac	1.00E+03	1.00E+01	Comparator gain
ro	5.00E+05	5.00E+05	Output resistance of error amp.
gm	3.00E-05	1.00E-05	Transconductance of error amp.
cc	1.00E-06	1.00E-11	Compernsation capacitor
wz	3.00E+01	1.00E+06	zero frequency
wp	2.00E+00	2.00E+05	pole frequency

Range of coeffecients

	MAX (yi)	MIN (xi)
a1	3.00E-03	1.01E-03
a2	5.00E+06	3.10E+05
a3	5.02E+10	1.54E+10
a4	1.50E+12	1.00E+16

Kharitonov polynomials Coefficients

F1	3.00E-03	5.00E+06	1.54E+10	1.50E+12
F2	1.01E-03	5.00E+06	5.02E+10	1.50E+12
F3	3.00E-03	3.10E+05	1.54E+10	1.00E+16
F4	1.01E-03	3.10E+05	5.02E+10	1.00E+16

stable

Routh Hurwitz Stability

F1		**F3**	
3.00E-03	1.54E+10	1.01E-03	5.00E+06
5.00E+06	1.50E+12	5.02E+10	1.50E+12
1.54E+10	0	5.00E+06	0
1.50E+12		1.50E+12	
F2		**F4**	
3.00E-03	1.54E+10	1.01E-03	5.02E+10
3.10E+05	1.00E+16	3.10E+05	1.00E+16
1.53E+10	0	5.01E+10	0
1.00E+16		1.00E+16	

The range of maximum and minimum values of the components are provided as input and the excel sheet is programmed to obtain the coefficients of the control to output transfer function. The maximum and minimum coefficients are used to create the Kharitonov polynomials. The stability of these four polynomials is analyzed using the Routh Hurwitz stability criterion. A sign change in the Routh stability analysis would indicate instability in the system.

In order to handle multiple variables a matlab program is developed and provided in the appendix section 11.2. Here the output capacitance and the ESR of the capacitance are considered the critical parameters that changes widely over temperature and hence are used in the stability analysis.

Chapter 5

5.1 Gate drive electronics

An isolated or floating voltage supply is required to turn on the high side switch of switching converters. Various mechanism exits to achieve this operation. They are as follows

- Bootstrap
- Switched capacitor
- Optocoupler
- Transformer coupled gate drive

Of these techniques bootstrapping and switched capacitor gate drives are more competitive for low power, commercial applications. For higher drive power, optocoupler gate drives are commonly used in the commercial market. Only transformer coupled gate drives are applicable for high temperature switch mode power supply.

5.2 Transformer coupled gate drive

A typical block diagram of a transformer coupled gate drive is shown in Figure 5-1. A differential driving circuit in the primary side helps to minimize the saturation of transformer core. NP and NS are the number of turns of coil in primary and secondary. The mutual coupling between the primary and secondary is represented by the coupling

coefficient ‘K’. The switching frequency of the control loop is usually set at a few hundred KHz. Direct switching of the power switches (turn ON and OFF) with respect to control loop switching cycle is less efficient as this would require larger transformer size. For this reason higher switching frequency is used for the gate drive circuit and an auxiliary dc supply is generated at the secondary using a full wave rectifier. This type of gate drive mechanism is described as a transformer coupled gate drive with control and signal transfer. The gate drive buffers are turned ON (enabled) based on a control signal proportional to the switching frequency. During this period, the power is transferred from primary to secondary. In the secondary side the received signal is rectified to produce a DC voltage for turning ON the high side load switch, which in this case is a MOS or SiC transistor. When the control signal disables the buffer, the voltage at the secondary side is allowed to bleed down or discharge to zero based on the natural decay response of RLC circuit or by adding an active discharge circuit.

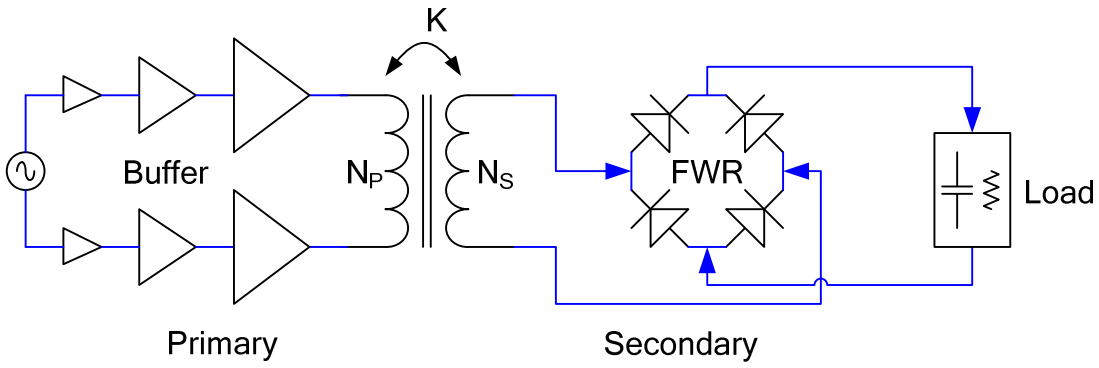


Figure 5-1. Transformer coupled gate drive - differential mode; followed by a full wave rectifier and load circuit

5.3 Pulse transformer

Unlike a sinusoidal voltage source as shown in Figure 5-1 the electronic circuits often require pulse voltages for digital (binary) operation for simplicity. A square wave is hence dominant in electronic circuits rather than sine wave. Conventional transformer theories are mainly based on single input frequency characteristic of a sine wave; whereas a pulse waveform is mathematically an infinite or at least a broadband sum of

sine waves with multiples of fundamental frequency. The fundamental frequency corresponds to the pulse period.

Pulse transformers are those specifically designed to operate in electronic circuits where pulse inputs are encountered. These are conventionally referred to wide band transformers or video transformers. The rise time of the input pulse determines the bandwidth required in the transformer for efficient pulse reproduction in secondary. As a transformer itself is a band pass network with attenuation at lower and higher frequency, the resonant frequency of a transformer is then given by equation 5-1.

$$fr = \sqrt{fl \times fu} \qquad [5\text{-}1]$$

where the fl and fh are the lower and upper cut-off frequency, respectively. The lower cut-off frequency is dominated by the source resistance and the mutual inductance of the circuit. The higher cut-off frequency is dominated by the leakage inductance and load capacitance of the transformer.

It must be noted that the presence of a rectifier at the secondary eases the strict requirement of square pulses at the secondary. The final output available after rectification is based on the sum of the power transferred in individual pulse cycles. Hence unlike a normal pulse transformer where the fidelity of the output is important, the objective here is to transfer maximum energy in each cycle. This concept is applied later in selecting the operating frequency for the gate drive transformers.

5.4 Coreless Planar transformers (CPT)

Conventional core type transformers are bulky and are not volume efficient. Planar transformers based on printed circuit board (PCB) technology and on-chip processes are much more efficient for certain applications. In niche applications the planar transformers are made on a magnetic substrate for higher quality factor and coupling. However this requires exotic processing steps and is not cost effective in our application. Therefore in most cases planar windings are fabricated on a highly resistivity substrate and hence

known as coreless transformers. In this work coreless planar transformer based on PCB technology is adopted.

5.4.1 Characteristics of planar transformer

The factors affecting the characteristic of a planar transformer are as follows:

- Physical Area
- Metal lines
- Metal spacing
- Substrate
- Operating frequency
- Orientation of primary and secondary windings

5.4.1.1 Physical area of transformer

As the goal is reduce the volume occupied by the transformer, usually a comfortable minimum area is picked to work with. In this study a 10 square centimeter area is considered for the transformer. A larger area could incorporate increased number of windings and hence improves the coupling. However it also decreases the bandwidth of the transformer since capacitance increases proportional to area. It is desirable to have the bandwidth of the transformer to be at least 10 times higher than the maximum switching frequency. For instance, a minimum of 60 MHz bandwidth is desirable for better reproduction of pulse at the secondary for a switching frequency of 6 MHz.

5.4.1.2 Metal lines

The width and thickness of the metal lines affect the resistance of the conductors. Wider width and thicker conductors are preferred for reducing the resistance and thereby

improving the quality factor. The inductance of a metal strip is logarithmically proportional to metal thickness and width and linearly proportional to its length. For a given area, increasing the metal width reduces the number of turns in the transformer and in turn the coupling as well as increasing capacitance and reducing bandwidth. Since the inductance is proportional to the square of number of turns, it is important to optimize the width of the conductors to obtain maximum inductance.

5.4.1.3 Metal spacing

The spacing between the adjacent conductors of primary and second windings directly affect the coupling between the lines. Also for a fixed area, increasing the spacing reduces the number of turns in the winding. The metal spacing affects the bandwidth of the system as it controls the inter-winding and intra-winding capacitances.

5.4.1.4 Substrate

The substrate on which the metal tracks are fabricated determines the losses and bandwidth of the transformer. High resistivity substrates are preferred for lower electrical losses and lower dielectric constant enables wider bandwidth for the system. In MEMS post-process flow the substrate underneath the metal layers is removed to improve the quality factor of on-chip inductors and transformers. In VLSI circuits, upper layers of metal are used along with thicker metals.

5.4.1.5 Frequency of operation

The frequency of operation of the transformer largely determines the physical size of the transformer along with the secondary loading. The reactance of inductor and capacitor is given by equation 5-2 and 5-3 respectively. Higher frequency operation helps in reducing the component size to meet required impedance.

Inductive reactance, $X_L = \omega L = 2 \times \pi \times f \times L$ [5-2]

Capacitive reactance, $X_C = \frac{1}{\omega \times C}$ [5-3]

5.4.1.6 Orientation of windings

There are several different types of orientations of primary and secondary windings of a transformer. Figure 5-2 shows the most popular types of conductor winding. The planar type windings are also known as “Frlan” transformers result in negligible interwinding capacitances and hence are highly preferred for wide band operation. On the other hand the stacked type transformers provide good coupling and more turns for a given area. However due to large coupling area the capacitance is significantly increased. Often a modified stacked transformer known as diagonally stacked transformers are used as a trade-off between coupling and capacitance.

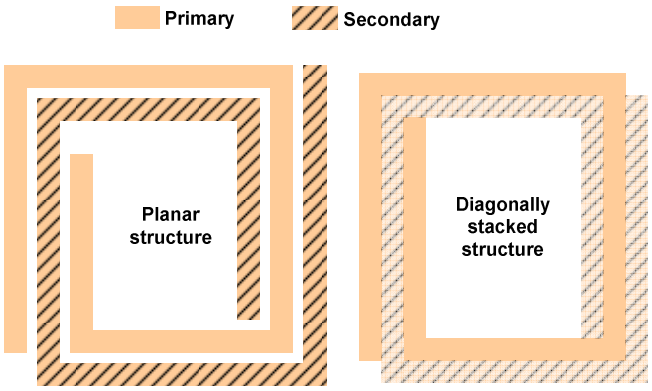


Figure 5-2. Common layouts of planar transformer structure: Frlan (left) in a single plane, “diagonally” stacked (right) in two planes.

5.5 Pulse transformer design

As seen in the previous section various factors affect the design and performance of the transformer and there exists no unique solution to satisfy all design constraints. An effort to modify a parameter during design results in automatic change in another, typically resulting in undesired response. The best example would be the increase in inductance by increasing the number of turns also increases the capacitance and hence decreases bandwidth. The suggested starting point is to start with a maximum permissible area for the transformer based on operating frequency and use a software based approach to verify the performance. A systematic design flowchart is presented in section 5.9. A design approach based on fundamental understanding of CPT and simulations is presented in following section.

5.5.1 Mathematical Analysis of CPT

Mathematical analysis of the transformer provides insights that help to design the CPT. The turns ratio in the transformer is assumed to be unity in following analysis. This simplifies the analysis to some extent while being extendable to transformers with non unity transformation ratio. The transformers can be represented using a T or π equivalent circuit. For simplicity the 'T' equivalent circuit of the transformer used for the mathematical analysis is shown in Figure 5-3. The model includes the parasitic capacitances and resistance of the transformer winding. The behavior of the transformer is also dependent upon the source and load characteristics and thus are included in the model. Applying nodal analysis in the s domain, the transfer function of the equivalent circuit in Figure 5-3 is obtained. Since the overall transfer function is very complicated with fourth order terms in numerator and denominator, suitable simplifying assumptions are made to reduce the complexity.

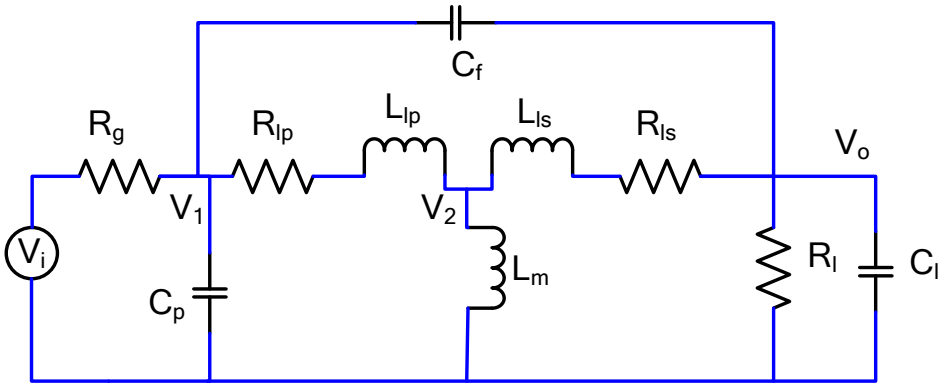


Figure 5-3. Equivalent circuit model of the transformer including parasitic, source and load components.

$$\frac{\begin{aligned}&R_l \cdot s \cdot (C_f \cdot L_l \cdot R_g \cdot s^3 . (C_f + C_p) \cdot (L_l + 2 \cdot L_m) + C_f \cdot s^2 \cdot (2 \cdot C_f \cdot R_{dc} \cdot R_g \cdot (L_l + L_m) \\ &+ 2 \cdot C_p \cdot R_{dc} \cdot R_g \cdot (L_l + L_m) + L_l \cdot (L_l + 2 \cdot L_m)) + C_f \cdot s \cdot (C_f \cdot {R_{dc}}^2 \cdot R_g) + C_p \cdot {R_{dc}}^2 \cdot R_g \\ &+ (L_l + L_m) \cdot (2 \cdot R_{dc} + R_g)) + C_f \cdot R_{dc} \cdot (R_{dc} + R_g) + L_m\end{aligned}}{\begin{aligned}&L_l \cdot R_g \cdot R_l \cdot s^4 \cdot (C_f + C_l) \cdot (C_f + C_p) \cdot (L_l + 2 \cdot L_m) + s^3 \cdot (2 \cdot {C_f}^2 \cdot R_{dc} \cdot R_g \cdot R_l \cdot (L_l + L_m) \\ &+ C_f \cdot (2 \cdot C_l \cdot R_{dc} \cdot R_g \cdot R_l \cdot (L_l + L_m) + 2 \cdot C_p \cdot R_{dc} \cdot R_g \cdot R_l \cdot (L_l + L_m) + L_l \cdot (L_l + 2 \cdot L_m) \cdot (R_g \\ &+ R_l)) + C_l \cdot R_l \cdot (2 \cdot C_p \cdot R_{dc} \cdot R_g \cdot (L_l + L_m) + L_l \cdot (L_l + 2 \cdot L_m) + C_p \cdot L_l \cdot R_g \cdot (L_l + 2 \cdot L_m)) \\ &+ s^2 \cdot ({C_f}^2 \cdot {R_{dc}}^2 \cdot R_g \cdot R_l + C_p \cdot {R_{dc}}^2 \cdot R_g \cdot R_l + 2 \cdot L_l \cdot (R_{dc} \cdot (R_g + R_l) + R_g \cdot R_l) \\ &+ L_m \cdot (2 \cdot R_{dc} \cdot (R_g + R_l) + R_g \cdot R_l) + C_l \cdot R_l \cdot (C_p \cdot {R_{dc}}^2 \cdot R_g \cdot (L_l + L_m) \cdot (2 \cdot R_{dc} + R_g)) \\ &+ C_p \cdot R_g \cdot (L_l + L_m) \cdot (2 \cdot R_{dc} + R_l) + L_l \cdot (L_l + 2 \cdot L_m) + s \cdot (C_f \cdot R_{dc} \cdot (R_{dc} \cdot (R_g + R_l) \\ &+ 2 \cdot R_g \cdot R_l) + C_l \cdot R_{dc} \cdot R_l \cdot (R_{dc} + R_g) + C_p \cdot R_{dc} \cdot R_g \cdot (R_{dc} + R_l) \\ &+ (L_l + L_m) \cdot (2 \cdot R_{dc} + R_g + R_l)) + (R_{dc} + R_g) \cdot (R_{dc} + R_l)\end{aligned}}$$

[5-4]

It is reasonable to assume the leakage inductance of the primary and secondary windings and their dc resistances are equal for a 1:1 transformer. Though this does not reduce the order of the system, it greatly reduces the number of parameters. The simplified transfer function is given in 5-4. With use of Matlab®, the frequency response of the transfer function is observed for nominal values of the components. The values are based on previous reports on CPT and given source and load specifications for this work . Figure 5-4 shows the magnitude and phase response of 1) simplified system (blue curves Rlp=Rls=1000 ohms, Rg = 2ohms), 2) simplified system with Rlp=Rls=0 (green curves), and 3) simplified system with Rlp=Rls=Rg=0 (red curves).

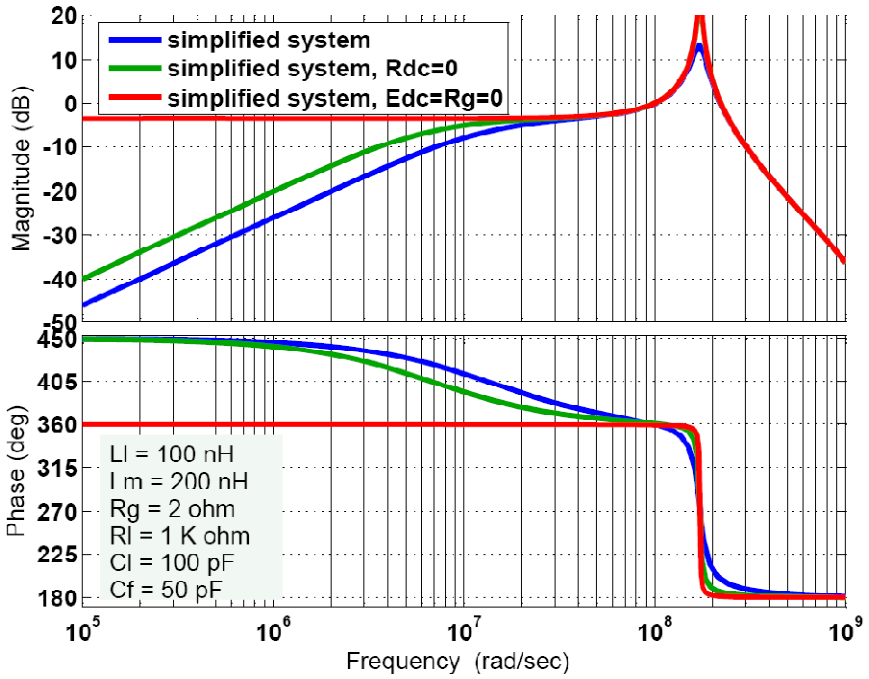


Figure 5-4. Bode plots of the complete system with several approximations.

It can be clearly seen that the dc resistance of the primary and secondary coils along with the generator resistance influence the low frequency gain of the system. The response for an ideal source with zero source resistance is largely different from a practical source. Hence the parasitic resistances of the windings along with the generator resistance are the limiting factors that set the lower operating frequency for transformer.

Conventionally the gate drive transformers referred as pulse/video/broadband transformers are analyzed with the rise time, top of the pulse and fall time of the input pulse in mind. Based on the different pulse parameter subsections, corresponding equivalent circuits are developed by elimination of non-dominant components. This typically results in low and high frequency models.

5.5.1.1 Rise time analysis

A high frequency equivalent circuit model is considered for the rise time analysis of the transformer. Figure 5-5 shows the equivalent circuit corresponding to pulse rise time.

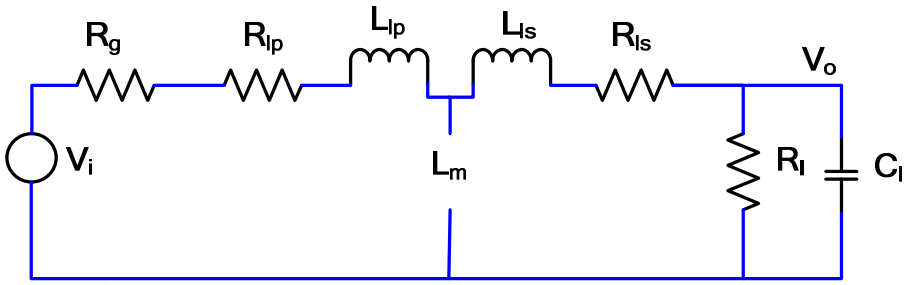


Figure 5-5. Equivalent circuit for the rise time of the input pulse.

$$\frac{V_o(s)}{V_i(s)} = \frac{R_l}{s^2 \cdot C_l \cdot R_l(L_l p + L_{ls}) + s \cdot (C_l \cdot R_l \cdot (R_g + R_{lp} + R_{ls}) + L_{lp} + L_{ls}) + R_g + R_l + R_{lp} + R_{ls}} \quad [5\text{-}5]$$

Applying nodal analysis the transfer function of the system is obtained and presented in 5-5. It is reasonable to assume that the load resistance is much greater than source resistance, as in the case of typical high side switch being a FET. Further assumptions are made such as equal leakage inductance in primary and secondary (1:1 turns ratio) and negligible resistance for the windings, to represent the transfer function as a standard second order system.

Comparing the derived transfer function with standard second order system, the natural resonance frequency of the system and the damping ratio are given by equations 5-6 and 5-7 respectively. The rise time is given by equation 5-8.

$$w_n = \frac{1}{\sqrt{2 \cdot L_l \cdot C_l}} \quad [5\text{-}6]$$

$$\zeta = \frac{Rg}{\sqrt{8}\sqrt{\left(Ll/Cl\right)}} + \frac{\sqrt{\left(Ll/Cl\right)}}{\sqrt{2} \cdot Rl} \approx \frac{Rg}{\sqrt{8}\sqrt{\left(Ll/Cl\right)}} = \frac{RgCl\omega_n}{2} \quad [5\text{-}7]$$

$$T_r = \frac{\pi - Cos^{-1}(\zeta)}{\omega_n \cdot \left(1 - \zeta^2\right)^{0.5}} \quad [5\text{-}8]$$

The load capacitance, load resistance and rise time are usually specified as design inputs. It is also desirable to obtain a damping coefficient less than 0.707 to satisfy a critical damping requirement. Therefore using the given values in the equations 9-1 and 9-2 a relation between the leakage inductance and source resistance can be obtained. For a load capacitance of 200 pF in parallel with 2KΩ and a rise time of less than 50nS, leakage inductance and source resistance requirements are as given in equation 5-9 and 5-10.

$$0 \le L_l \le 5.5 \times 10^{-7}\, H \qquad [5\text{-}9]$$

$$R_g = \sqrt{L_l} \cdot (1.414 \cdot 10^5 - 5 \cdot 10^6 \cdot \sqrt{L_l}) \qquad [5\text{-}10]$$

In the application under consideration for this work the source resistance of the drivers is fixed to the lowest possible value while avoiding under-damping. As seen from the previous section an ideal source with zero resistance provides excellent low frequency response. In the current work the generator resistance is given to be 2 ohms. Therefore to satisfy the critical damping constraint with this source resistance, the leakage inductance has to be lower than 0.2 nH. This is a very small value and cannot be obtained in practice. Hence it is not possible to obtain the desired rise time for given conditions with a critically damped system. However the damping requirement shall be relaxed. The resulting low damping coefficient results in oscillatory behavior for a unit step input. The step response of the rise time equivalent circuit (red curve) and the complete equivalent circuit (blue and green curves) are shown in Figure 5-6. The overshoot value is much higher in approximated rise time equivalent circuit response compared to the complete system. This is an indicator of the trade off in accuracy due to various assumptions made in the rise time transfer function derivation.

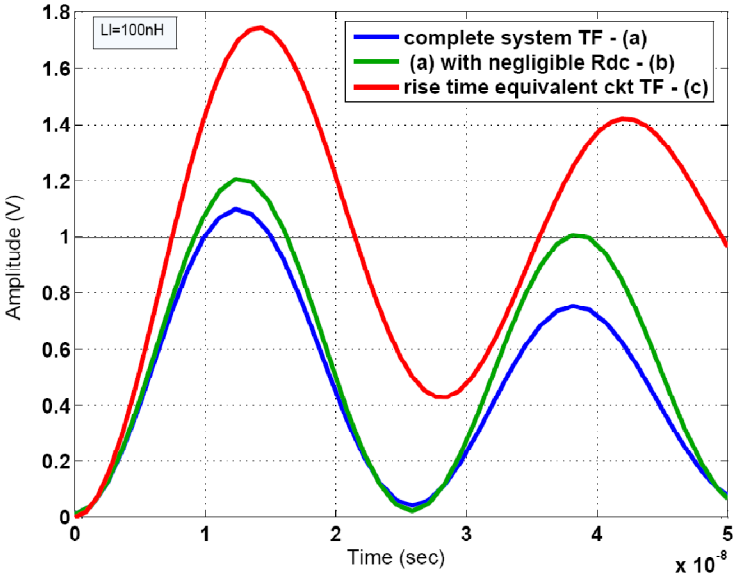


Figure 5-6. Step response of the transfer function representing the rise time equivalent circuit and complete equivalent circuit.

Therefore a suitable option is to limit the leakage inductance to meet the required rise time and trade off the low damping. In special cases an external series resistance can be added between the source and the primary windings to improve damping. It should also be noted that the second cycle representing the oscillation in the figure should not be considered since the model is only valid for the rise time duration.

5.5.1.2 Pulse top analysis

In contrast to pulse transformers the gate drive circuitry includes a rectifier at the secondary side. The use of rectifiers in the secondary side reduces the constraints in the pulse top period. The approximated equivalent circuit for the pulse top duration is shown in Figure 5-7. It must be noted load capacitance is considered, ignoring the load resistance since the MOSFETs or JFETs provide a capacitive loading to the transformer. A complete transfer function of this circuit yields a 5th order system as given by equation 5-11.

$$\frac{V_o(s)}{V_i(s)} = \frac{L_m \cdot R_l^{\,2} \cdot s}{\begin{aligned} & s^5 \cdot C_l^{\,2} \cdot L_l^{\,2} \cdot L_m \cdot R_l^{\,2} + s^4 \cdot C_l \cdot L_l \cdot L_m \cdot R_l \cdot (C_l \cdot R_g \cdot R_l + 2 \cdot Ll) \\ & + s^3 \cdot Ll \cdot (C_l \cdot R_l \cdot (Ll \cdot R_l + L_m \cdot (2 \cdot R_g + R_l)) + L_l \cdot L_m) + s^2 \cdot L_l \cdot (C_l \cdot R_g \cdot R_l^{\,2} \\ & + L_l \cdot R_l + L_m \cdot (R_g + R_l)) + s \cdot R_l \cdot (L_l \cdot (R_g + R_l) + L_m \cdot R_l) + R_g \cdot R_l^{\,2} \end{aligned}} \qquad [5\text{-}11]$$

A simplified expression obtained by assuming equal leakage inductances and negligible dc winding resistance is given in section 5-11. Further assuming that the source resistance is greater than the impedance due to leakage inductance, the following relationship is obtained.

$$\frac{V_o}{V_i} = \frac{s \cdot \left(L_m / Rg \right)}{1 + s \cdot \left(L_m / Rg \right)} \qquad [5\text{-}12]$$

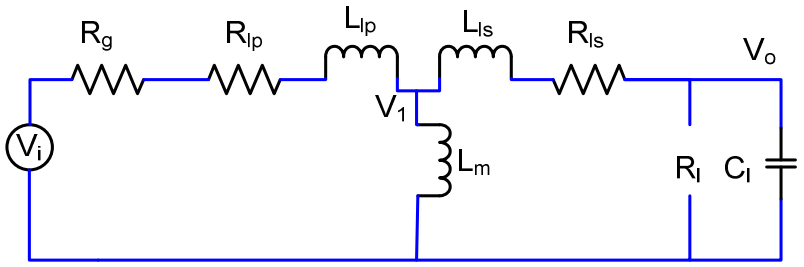


Figure 5-7. Equivalent circuit for the pulse top duration.

Equation 5-12 indicates that the response of the system during pulse top duration is dominated by the mutual inductance and dictates a low source resistance. Hence a high mutual inductance and a low source resistance are preferred.

The time constant of the primary side series RL circuit imposes a minimum required self inductance to keep the power dissipation lower. The droop in secondary voltage is proportional to the pulse duration. As a rule of thumb the on time of the circuit has to be lower than 10% of the time constant. Hence for a given operating frequency, the minimum required self inductance is given by equation 5-13, where Ton=1/f and Rp is the sum of the source and primary winding resistance.

$$T_{on} \le 10\%\left(\frac{L_p}{R_p}\right) \Rightarrow L_p \ge 10 \cdot R_p \cdot T_{on} \qquad [5\text{-}13]$$

For a given operating frequency, it is recommended to use a differential buffer to drive the transformer since it provides symmetry and twice the gain of single ended circuit. Also due to differential switching, the fall and rise time analysis are identical.

5.5.2 Finite element analysis

Finite element analysis (FEA) is useful to analyze the properties of a structure by breaking up into smaller pieces. It also helps to understand the behavior of a hardware model in less time and cost. Various FEA softwares are used to analyze the behavior of inductor and transformers in the literatures. In this study the FEA analysis were carried out using “sonnet” software. Based on the simplicity, efficiency and previous reports[44-61], stacked transformers are selected for use in this work.

For study, a two layer PCB structure with an equal number of turns in the primary and secondary winding is considered. A symmetric structure is preferred for reducing the FEA time and it also makes the primary and secondary interchangeable. A three dimensional view of the stacked transformer structure used in the study is shown in Figure 5-8. A summary of transformer specification is provided in Table 5-1.

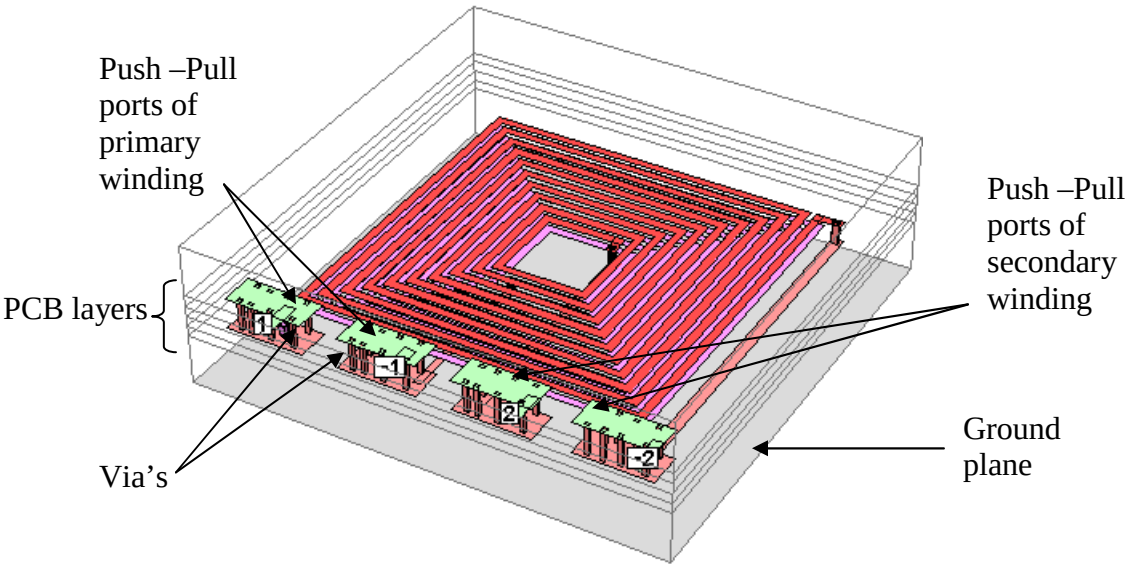


Figure 5-8. Three-dimensional view of stacked transformer structure.

Table 5-1. Specification summary of stacked transformer.

Parameter	Specification
Number of turns – primary	9
Number of turns – secondary	9
Width of metal conductor	10 mil*
Spacing between metal conductors	6 mil
Dielectric thickness	13.4 mil
First and second lengths	400 mil
Relative permittivity	3.4
Relative permeability	1
Copper weight	1 ounce

*1 mil = 25.4 micrometers

The different layers represent the layers of a printed circuit board. The top winding (shown in red) is connected to push-pull ports (2,-2) and the bottom winding (pink) is connected to ports (1,-1). The power transfer characteristic of the transformer is analyzed over the frequency range of 100 KHz to 100 MHz.

For validation the \simulated design is sent out for physical fabrication. Roger's 4350 dielectric material with one ounce copper trace is used for printing the circuit. The selection of PCB material is based on the previous evaluation of 4350 dielectric for elevated temperature operation. The high temperature characteristics of these copper clad laminates are presented in the appendix section, 11.1

5.6 S-parameter measurements

Scattering parameters, commonly known as s-parameters provide information about the transmission and reflection characteristics of an electrical port when a signal is transmitted or observed at its terminal. The s-parameter measurements of the fabricated structure are obtained using Agilent 8753ES network analyzer. The transmission and reflection characteristic as given by the FEA and the s-parameter measurements are given in Figure 5-9. In both cases (simulation and measurement) the de-embedded data is being shown. The frequency response of the test setup has been calibrated and removed by performing the SOLT (Short Open Load Thru) calibration . The figure shows a close agreement between the simulated and measured response.

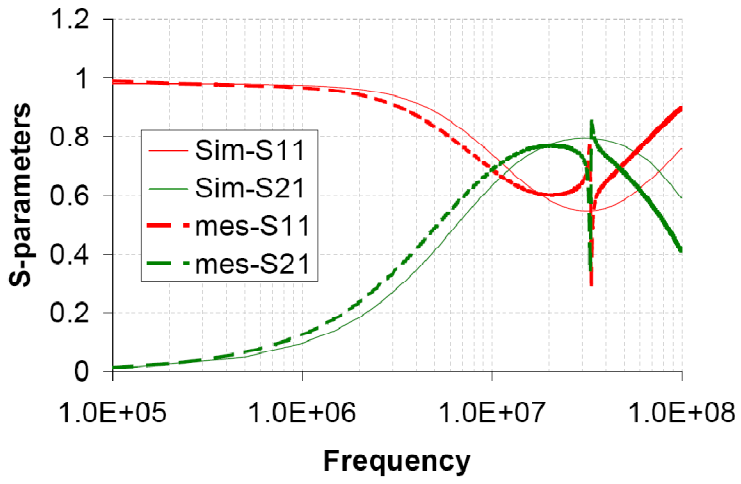


Figure 5-9. S-parameters (Transmission S21 and Reflection S11) of the stacked transformer. Measurement result versus finite element analysis.

5.6.1 Voltage gain versus power gain

The individual circuit parameters of the transformer can be extracted from the measure s-parameters based on some assumptions. Assuming the inductive impedance is significantly larger than the capacitive reactance the inductance of primary and secondary winding can be obtained using equations 5-14. Similarly assuming the coupling between the primary and secondary is dominated by mutual inductance the mutual inductance of the transformer can be obtained using equation 5-15.

$$L_P = L_S = \frac{\mathrm{Im}\, g\,(Y_{11})}{2 \times \pi \times f} = \frac{\mathrm{Im}\, g\,(Y_{22})}{2 \times \pi \times f} \qquad [5\text{-}14]$$

$$L_M = \frac{\mathrm{Im}\, g\,(Y_{21})}{2 \times \pi \times f} = \frac{\mathrm{Im}\, g\,(Y_{12})}{2 \times \pi \times f} \qquad [5\text{-}15]$$

The coupling co-efficient can be calculated from the total inductance and mutual inductance using the equations 5-16. The extracted values versus frequency is plotted and shown in Figure 5-10.

$$K = L_M \times \sqrt{L1 \times L2} \qquad [5\text{-}16]$$

$$L_{LK} = \sqrt{L_P L_S}\left[1 - K^2\right] = L_P\left[1 - K^2\right] \qquad [5\text{-}17]$$

It must be noted that the transmission co-efficient obtained by the parametric extraction and the transmission coefficient (S_{21}) measured using the network analyzer are different. The calculated coupling co-efficient is the voltage gain whereas the S_{21} is the power gain of the two port network. The power gain highly depends on the source and load impedance and is maximized when the load impedance is matched to the source impedance. In case of matched load and source impedance the power gain is same and

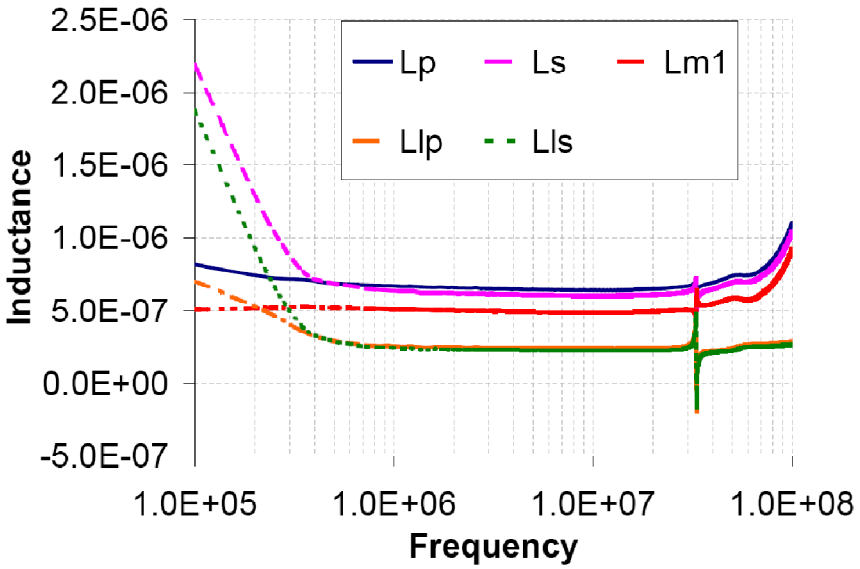


Figure 5-10. Extracted values of primary and secondary inductance (Lp, Ls), mutual inductance (Lm) and leakage inductance (Llp, Lls).

equivalent to voltage gain. The comparison between the voltage gain and power gain is shown in Figure 5-11. The figure illustrates the wide band coupling capacity of the transformer. For pulse inputs, which has only half the input in the fundamental frequency and the remaining half in the higher odd harmonics, it is recommended to select the fundamental closer to lower cut off frequency. For instance a fundamental frequency of 1MHz is preferred for transferring higher harmonics. However considering the power loss associated with lower switching frequency (power lost in primary is inversely

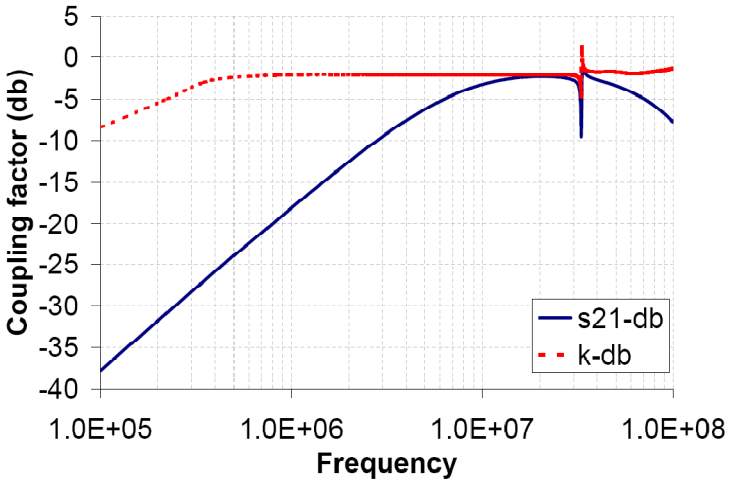


Figure 5-11. Comparison of measured transmission coefficient (S21) and the calculated coupling coefficient (k).

proportional to square of the switching frequency), it is wiser to choose a higher fundamental frequency. We have chosen 10 MHz as the fundamental frequency as this minimizes the power dissipation and at the same time allows energy from harmonics (3^{rd}, 5^{th} and 7^{th}) to couple to secondary.

It must be noted that for sinusoidal inputs, transformers with narrow band and high Q characteristics are commonly used for maximum efficiency. In such cases the bandwidth of the transformer shall be tuned such that the center frequency is the fundamental operating frequency.

Mathematical relationship between the power gain and the voltage gain are as follows.

Input power $$P_i = \frac{V_i^{\,2}}{R_i} \qquad [5\text{-}18]$$

Output power $$P_o = \frac{V_o^{\,2}}{R_o} \qquad [5\text{-}19]$$

Power gain $$G = \frac{P_o}{P_i} = \frac{V_o^{\,2}}{V_i^{\,2}} \times \frac{R_o}{R_i} \qquad [5\text{-}20]$$

For matched load and source resistance, the power gain (G_{db}) in decibels is given by

$$G_{dB} = 10\log\left(\frac{V_o^{\,2}}{V_i^{\,2}}\right) = 20\log\left(\frac{V_o}{V_i}\right) = A_{db} \qquad [5\text{-}21]$$

where A_{dB} is the voltage gain of the system.

The maximum power transfer theorem states that “maximum power is delivered to load when the load impedance is matched to the source impedance”. This can be observed

from Figure 5-11 where the S21 exhibit peak value around 20 MHz indicating the match between the load and source impedance (50 ohms).

However the maximum power transfer is not essentially same as maximum efficiency in most cases. The impedance offered by the primary inductance is directly proportional to the switching frequency. Hence a higher switching frequency reduces the peak current in the primary side in every switching cycle. Therefore, selecting a switching frequency marginally higher than the maximum power transfer frequency is advantageous. The higher limit is based on the switching looses in buffer (driver). The CV^2f losses in the differential buffers sets a point of minimum return as further increase in frequency results in reduced efficiency due to switching losses. It must be noted the above argument is only valid for gate drives involving FETs that require low input current (voltage controlled devices). For high current drive requirements the design has to be correspondingly modified.

5.7 High side buffer

Efficient design of buffers for transformer coupled gate drive, driving a non linear load is a challenging task. The source and load impedances must be considered to meet a critically damped system requirement. The design strategy proposed in Figure 5-13 illustrates the trade off in rise time, droop and damping due to low buffer resistance. In this work the design of high side buffer is based on minimum possible source resistance. The output resistance is set to be 3 ohms. This is not the optimum design, however based on transformer characteristics external manipulation of source impedance is possible in this method.

5.8 Full wave rectifier

As mentioned before a full wave rectifier is used in the secondary side of the transformer to rectify the differential output of secondary. The conventional method of using diodes for rectification results in considerable forward drop across the diodes and is not efficient. Alternative rectification techniques using MOS transistors have been demonstrated in the past [80, 81]. In this work a MOS switch based rectifier is used. Figure 5-12 shows the method of incorporating MOS switches as full wave rectifiers. The inductive link represents a RF power receptor or a secondary of a transformer. The differential signal at the transformer secondary provides current to the load through the switches that complementarily alternate between each cycle. The current flow corresponding to the polarity of input voltage is shown in the figure. The MOS transistors size must be optimized for lowest on resistance while minimizing the gate capacitance loading.

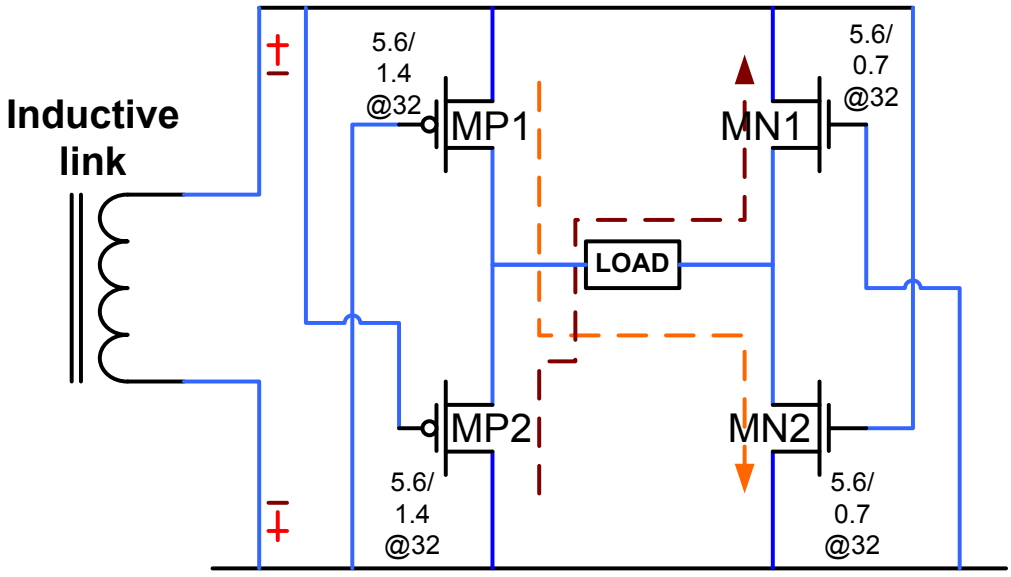


Figure 5-12. Full wave rectifier in CMOS process.

In this work the design of FWR is based on minimum voltage drop (minimum ON resistance) across the transistors and a fast rise time. However increasing the size of transistors increases the load capacitance at the secondary of the transformer and hence can reduce the bandwidth of the system. This results in the typical trade-off between load

capacitance and on resistance. Eight (8) parallel instances of the CMOS rectifier shown in Figure 5-12 is used as the rectification block.

5.9 Summary of gate drive transformer

Based on these requirements of a system, detailed mathematical analysis and design of planar transformer is discussed in the appendix section 5.5.1 There is more than one method to design CPT based on the tradeoffs made by designer. One such design flow is given in the flowchart shown in Figure 5-13.

The design flow begins with the given parameters like the load capacitance (Cl), load resistance (Rl), pulse rise time (Tr), switching frequency (f) etc. The first step is to calculate the maximum permissible leakage inductance to satisfy the rise time constraint. An alternate approach which satisfies a critical damping requirement is provided where the designer is able to custom design the buffer. Second, the minimum required self inductance is calculated using the natural time constant of 'RL' circuit. As a rule of thumb the time constant is chosen to be at least 10 times the switching period. Third, based on an assumed coupling factor, for the calculated self inductance in step 2, verify that the leakage inductance is not more than the maximum value calculated in step 1. As a final check, verify that the impedance due to mutual inductance is much higher than the source resistance. The final design involves an iterative selection process. Adjusting the switching frequency is the easy method to satisfy many design constraints.

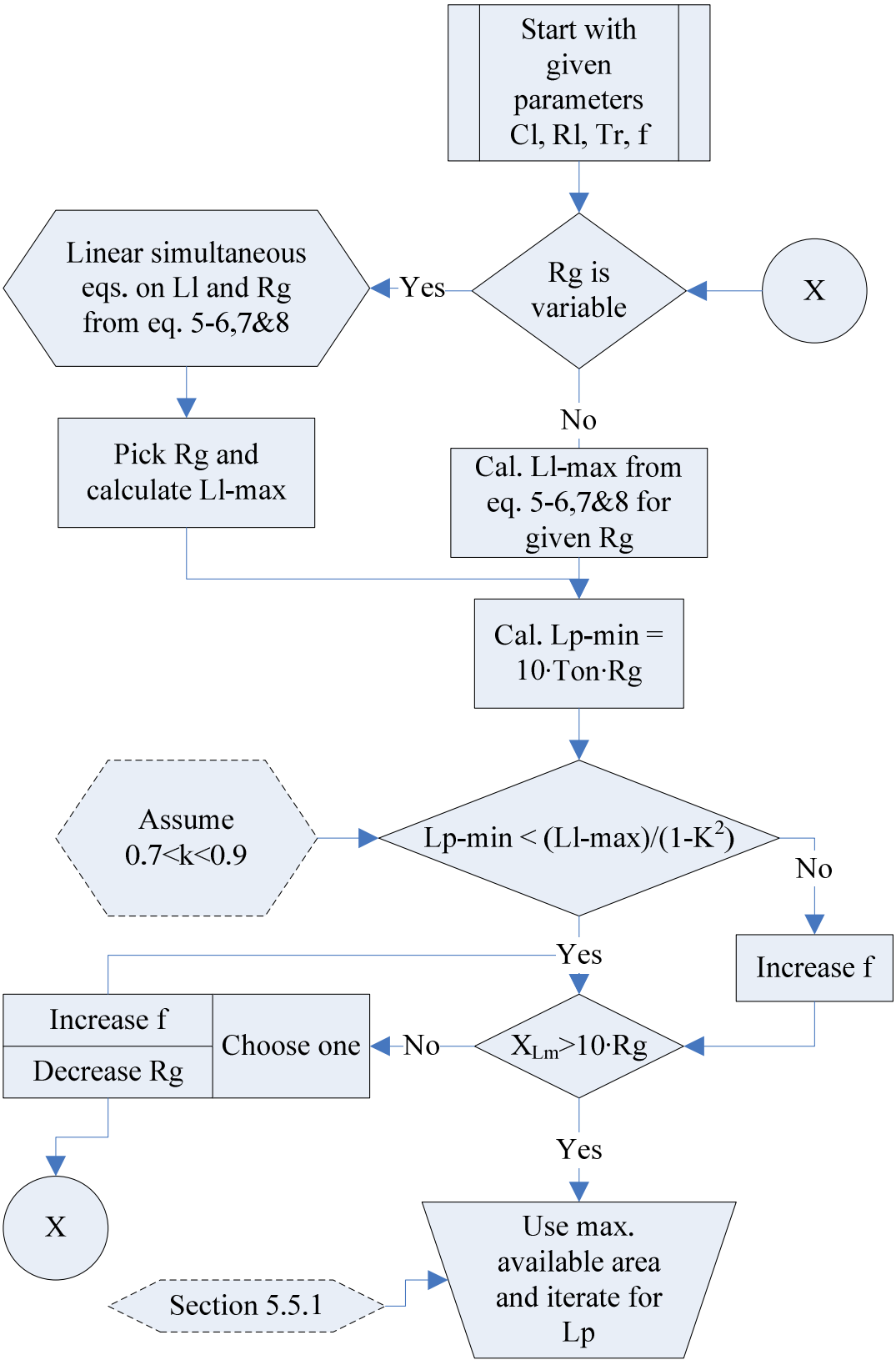


Figure 5-13. Design flowchart for gate drive transformer design.

5.9.1 Simulation results

The gate drive circuitry is simulated prior to fabrication. Figure 5-14 shows the schematic setup for gate drive verification. Experimentally obtained two port parameters of the planar transfer is used as a two port network in simulation. The oscillator, buffer, FWR and discharge circuits are also the circuits designed for this work. The simulated waveforms related to the gate drive circuitries are presented in Figure 5-15. The figure shows the (differential) voltage across the primary and secondary windings, the fall and rise characteristics of the rectified voltage with the control signal. The source resistance is about 3Ω and load capacitance and resistance are 200 pF and 2KΩ respectively. The switching frequency is 10 MHz. The average value of rectified voltage is about 2.9V which is sufficient to drive the power JFET in deep triode. The rise and fall times are lesser than 50 nS.

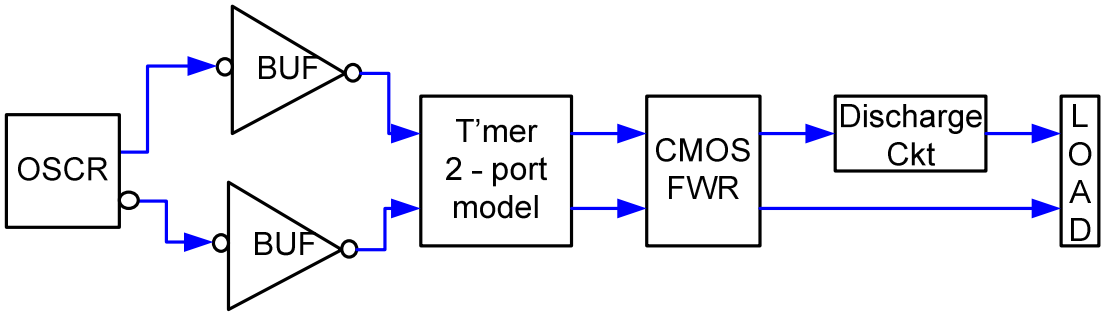


Figure 5-14. Schematic setup for the high side gate drive simulation.

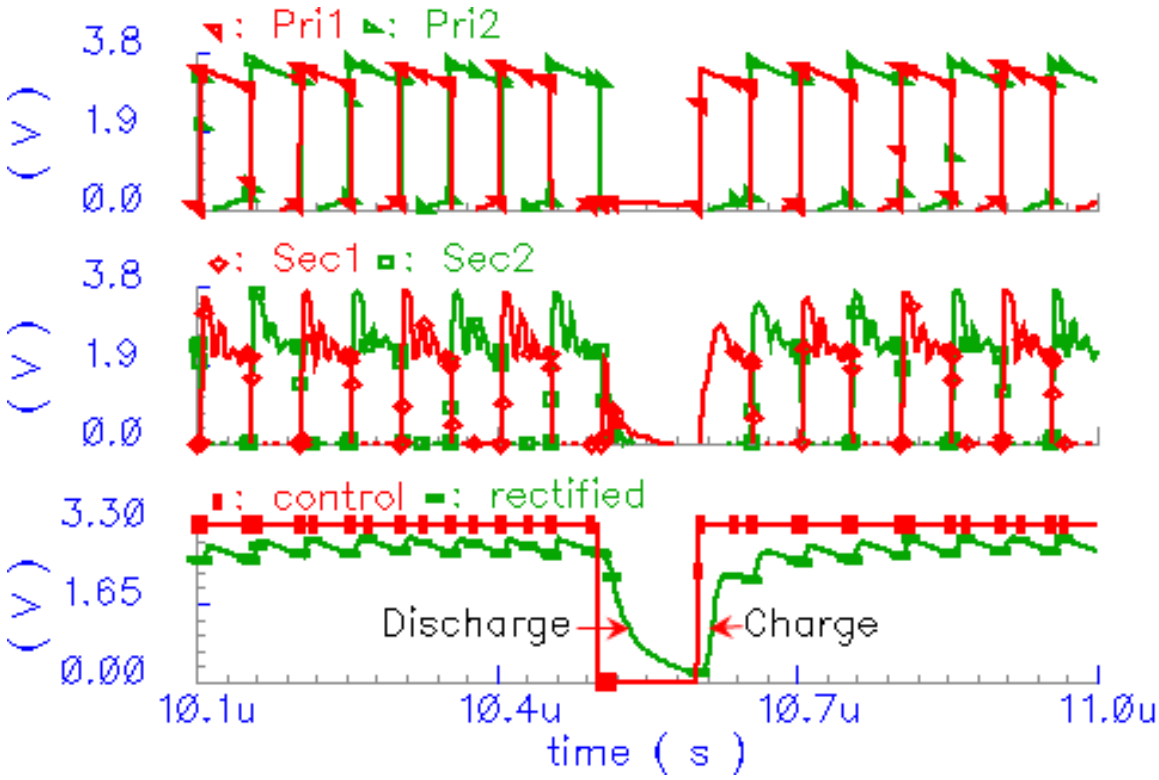


Figure 5-15. Waveforms at various stages in the high side switching Circuit. Top- Primary and secondary voltages, Middle- Differential secondary voltage, Bottom – Control and rectified voltage.

5.9.2 On chip - gate drive transformer

Transformers integrated on silicon chips were previously reported for RF applications [82-100]. With generation 2.0 control chip, a diagonally stacked transformer is fabricated on the same chip as controller to experimentally observe its characteristics. The fabricated control chip and the on chip transformers are illustrated in Figure 5-16. The transformer's primary and secondary are formed by planar spiral "metal 3" and "metal 1" windings, respectively. "Metal 2" is used to bring out the inner winding to G-S-G pad termination. The design parameters of the transformer are summarized in Table 5-2.

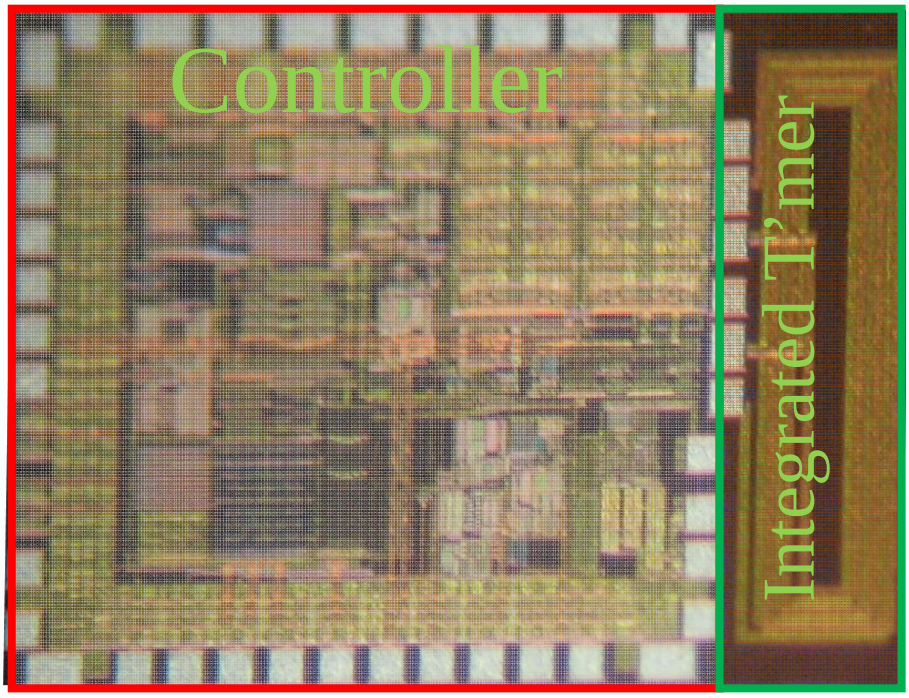


Figure 5-16. Generation 2.0 control chip with integrated gate drive transformer.

Table 5-2. Design parameters of on chip gate drive transformer.

Parameter	Remarks	
Physical size	~ 05 mm X 2.8 mm	
	Primary	Secondary
Metal layer	Thick metal MT	Metal 1
Conductor width	30 µm	30 µm
Conductor spacing	30 µm	30 µm
Sheet resistance	9 mΩ/□	48 mΩ/□
No of turns	3	3
Physical length	~ 11.2 mm	~ 11.2 mm

Raw measurement of the inductance and quality factor of these inductors are performed using network analyzer. The observed inductance and the quality factor for a range of frequencies are shown in Figure 5-17. The value of inductance is as expected and the quality factor is troublesomely lower due to high resistance conductors. Significant improvements to the quality factor can be achieved by using multilayer routing. The mutual coupling between the windings is of greater importance. However, the self

inductance limits the minimum frequency of operation. The coupling factor can also be improved by a more symmetric structure and utilizing more physical area.

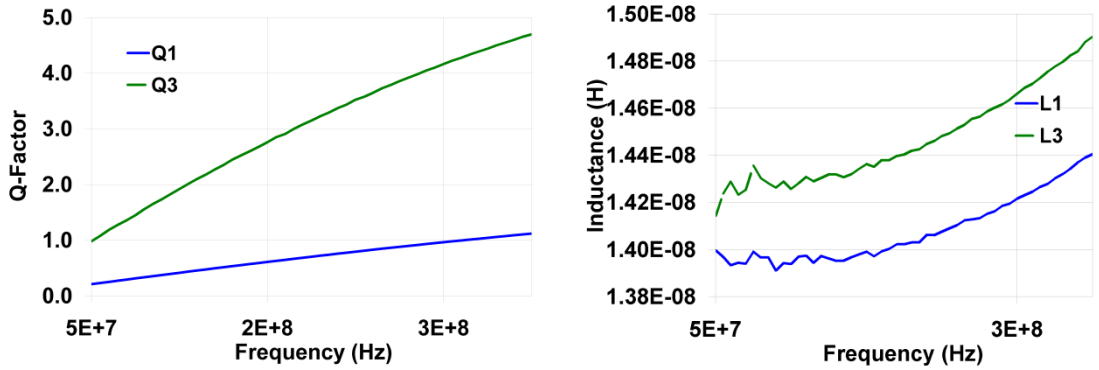


Figure 5-17. Measured inductance (right) and quality factor (left) of the on chip gate drive transformers.

To obtain the performance characteristic of the integrated transformer, the control chip is packaged on an 8 pin cerdip. The control signals are manipulated to produce the required drive functionality. The gate drive transformers are driven by the differential buffers. The input frequency is varied from 50MHz to 300MHz using VCO. The test circuit is shown in Figure 5-18. The differential output voltage can be seen from the top trace of Figure 5-19. The duty clamp functionality cannot be bypassed in the controller and hence is present in the system.

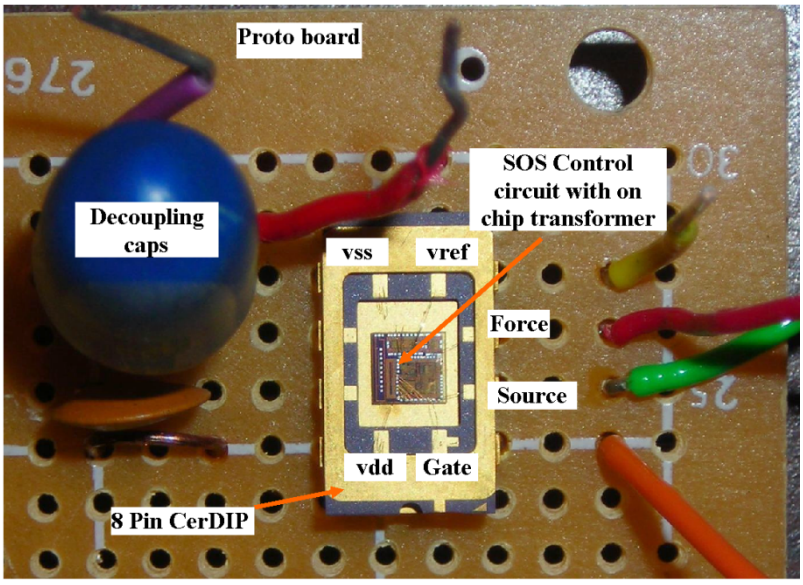


Figure 5-18. Protoboard developed to demonstrate the functionality of on chip gate drive.

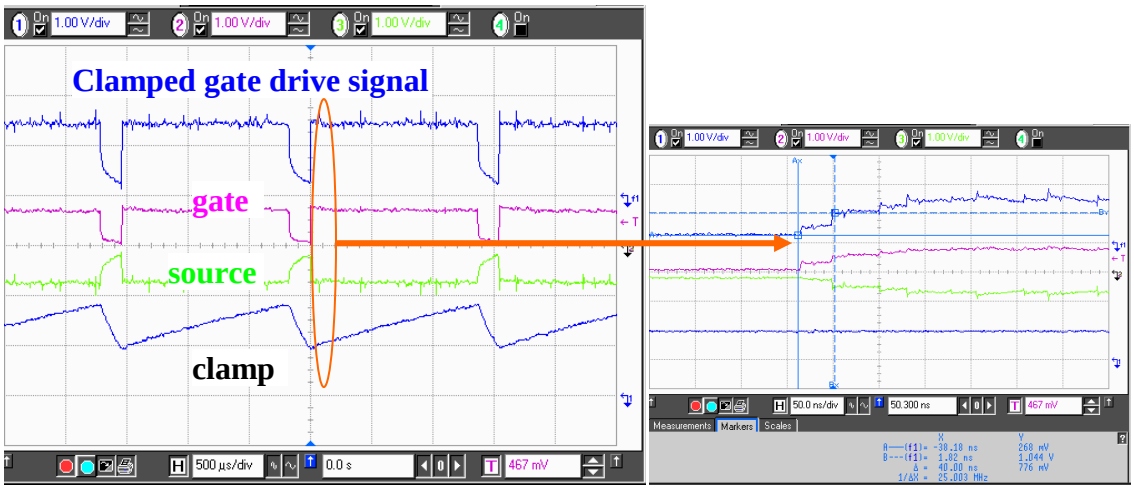


Figure 5-19. Gate drive characteristic waveforms of the on chip gate drive prototype. (Right: a zoomed-in view of the rising edge of the waveform)

In order to verify the functionality of integrated gate drive in real system a proto board is built using the integrated transformer instead of the PCB transformer. Packaged SiC JFETs are used as high side switch and the controlled is programmed for 3.3V output voltage. The demonstration board is shown in Figure 5-20.

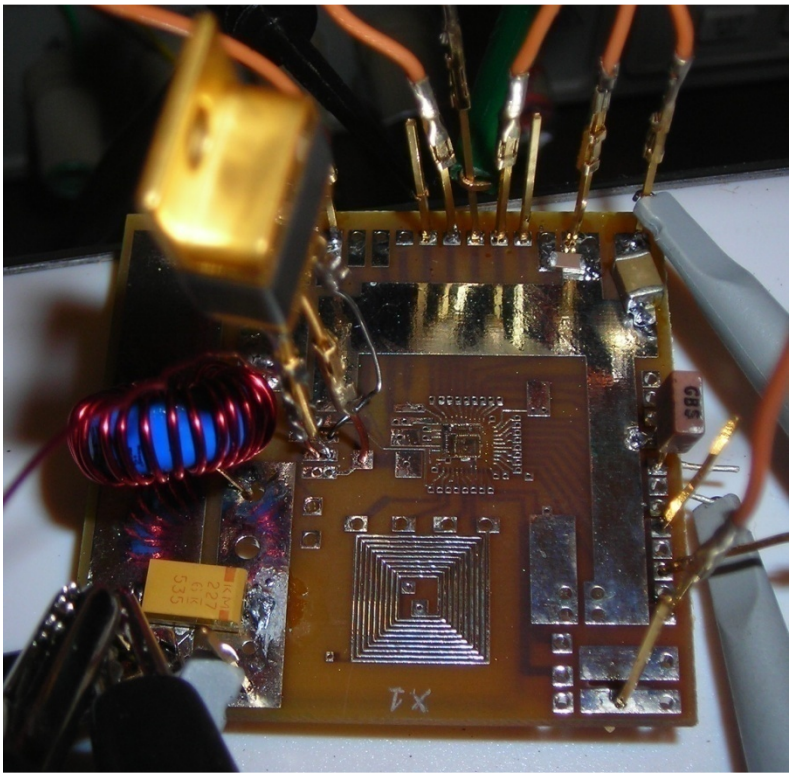


Figure 5-20. SMPS prototype using integrated gate drive transformer.

The measured results for no load operation are show in Figure 5-21. The output voltage (1) controller voltage VCC (2), the error amplifier output voltage (3) and the voltage at the gate terminal (4) are shown in the figure. It can be observed that a clean output voltage is obtained using the gate drive and hence presents as an attractive solution for the future designs.

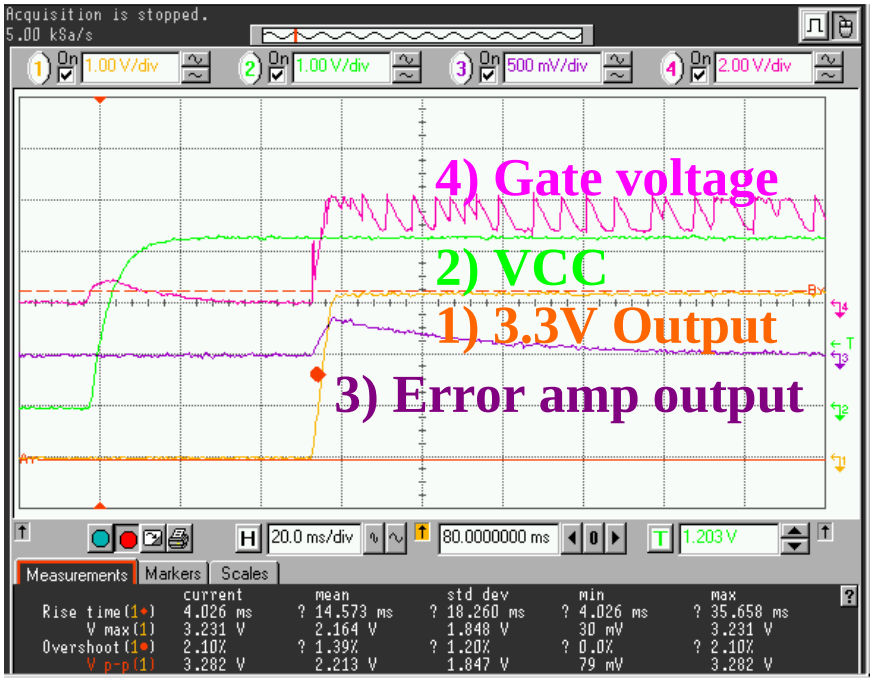


Figure 5-21. Performance of the SMPS using integrated gate drive.

5.9.3 Measured results

The fabricated gate drive circuitry is experimentally tested and its characteristics are observed. Figure 5-22. The input frequency is selected to be 10MHz. The voltage observed at the source terminal (Vsource) and the gate terminal (Vgate) is represented by the bottom traces respectively. The effective gate source voltage is represented by Vgs. The timing functionality of the duty clamp circuit is represented by Vramp. The duty clamp circuitry ensures a preset maximum duty cycle operation and is discussed in detail in section 6.3.7

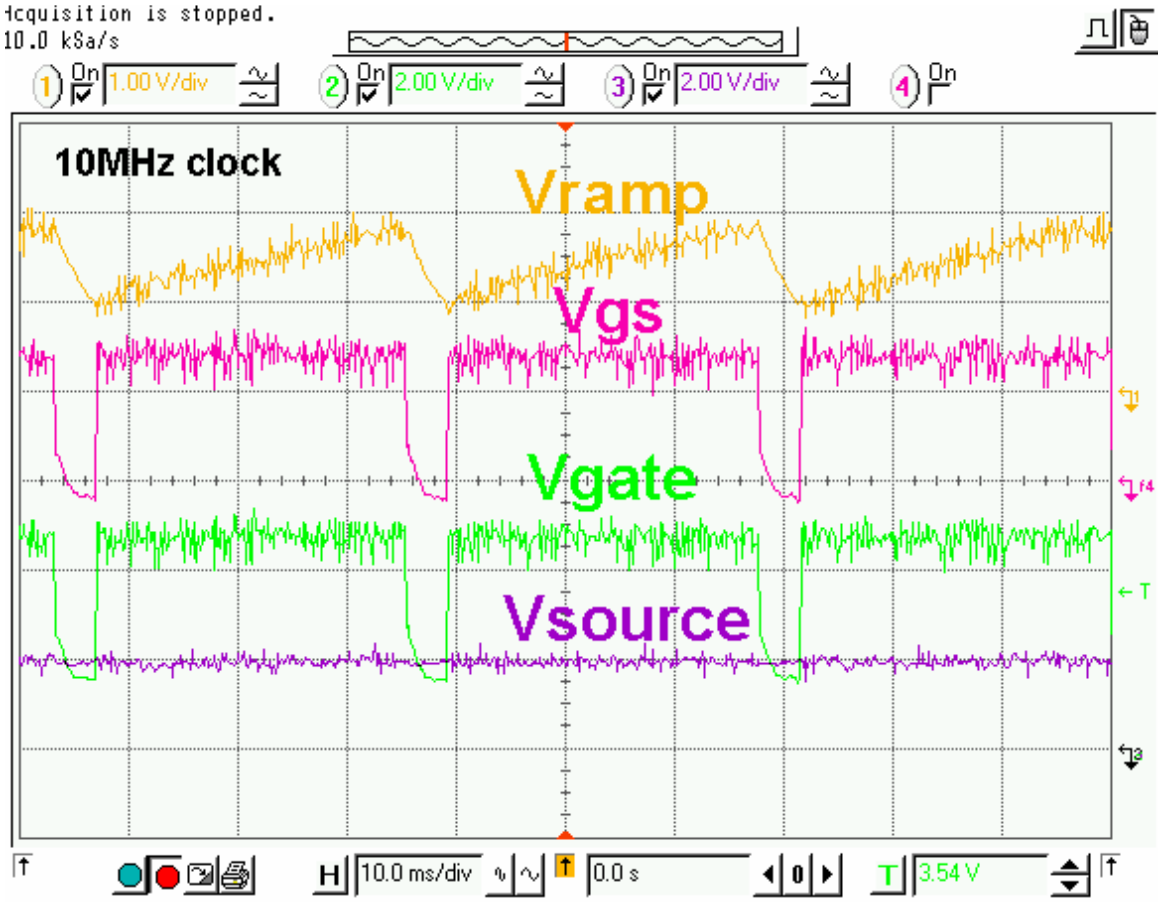


Figure 5-22. Measured characteristics of the gate drive circuitry.

Chapter 6

6.1 DC-DC Buck converter design

An overall system block diagram of a dc-dc synchronous buck converter is shown in Figure 6-1. As mentioned before the feed forward switch and filter network and the V2 control loop can be noted in the figure. In addition to these primary blocks the auxiliary house-keeping units like the over temperature monitor, under voltage lockout are also shown.

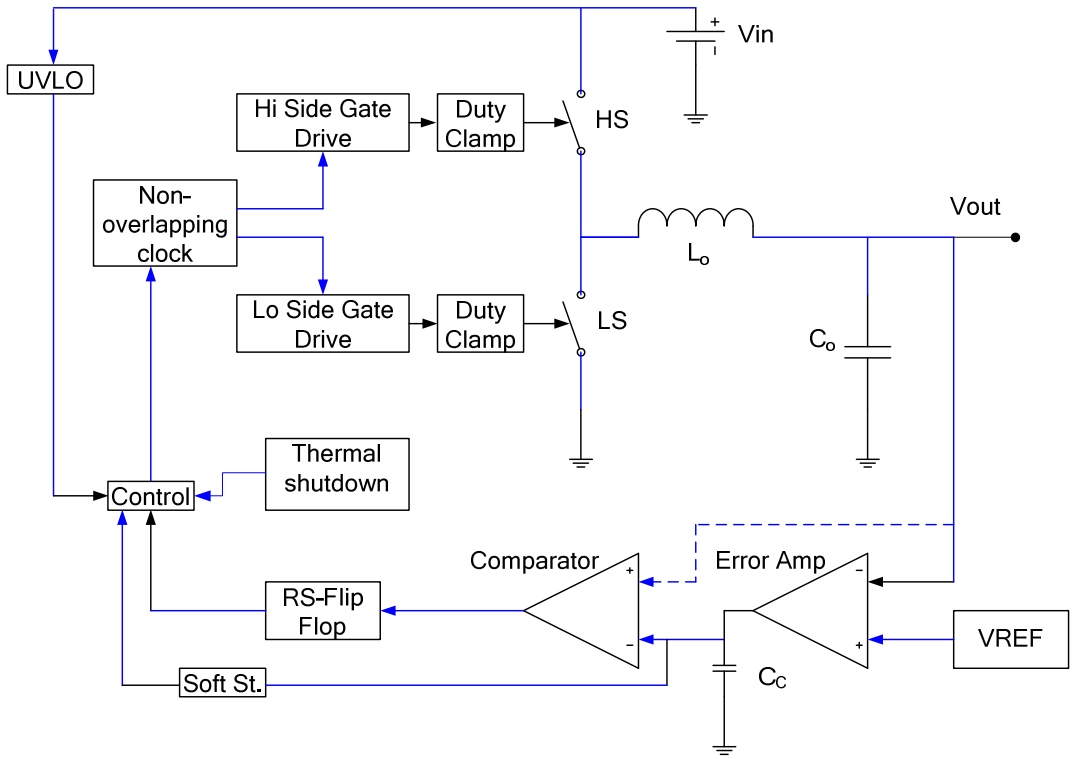


Figure 6-1. Detailed block diagram of synchronous buck converter with v2 control mechanism.

A non-overlapping clock generator provides input signal to the high side and low side switches (HS and LS), based on the control block output. The control block monitors the inputs from the V2 control and the auxiliary control circuits. A duty clamp circuit is used to limit the duty cycle to the switches to a preset amount. Other than the discrete semiconductor switches and passive L-C filter components analog building blocks are the basis of control loop and the auxiliary electronics. These building blocks and the house-keeping circuits are discusses in the following sections.

6.2 Analog building blocks

6.2.1 Voltage reference

The steady state dc output voltage of the voltage regulator is based on a reference voltage. This internally developed or externally applied reference voltage is expected to be independent of temperature, semiconductor process and supply voltage to obtain a stable required voltage at output. Designing a voltage reference for wide temperature range is a challenging task. Highly compliant model files and good knowledge on analog circuit layout techniques are important. In this work a voltage reference based on MOS-gated diodes is adopted. The schematic of the voltage reference is shown in Figure 6-2.

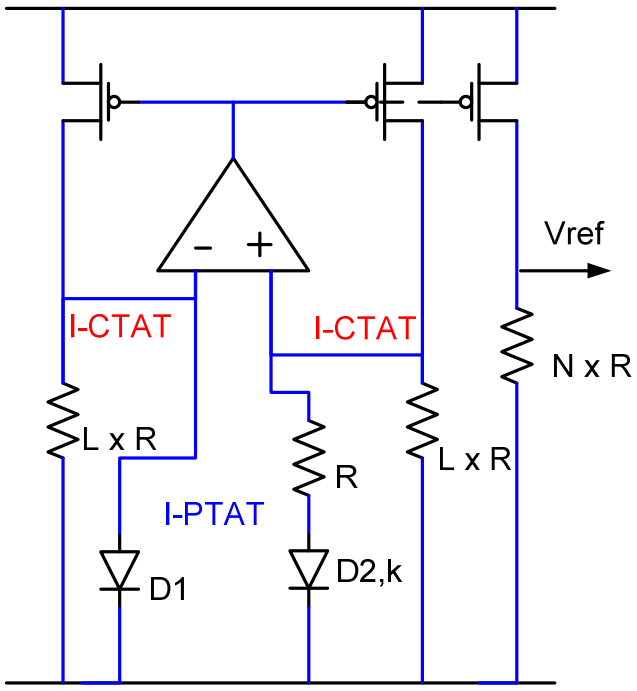


Figure 6-2. Schematic of a voltage reference circuit.

The operation of the circuit is based on the development of a PTAT (Proportional to Absolute Temperature) current and a CTAT (Complementary to Absolute Temperature) current. The resulting zero temperature co-efficient current is passed through a resistor to develop a required reference voltage(s). An important design strategy is to maintain the operating current for the diode legs (branches) in log-linear characteristic regime. In addition the areas of the resistors and diodes must be adequate to achieve the desired matching. The design equations are given by 6-1 through 6-6.

$$I_{PTAT} = \frac{n \times V_T \times \ln(k)}{R} \qquad [6\text{-}1]$$

$$I_{CTAT} = \frac{V_{D1}}{L \times R} \qquad [6\text{-}2]$$

$$V_{REF} = (n \times VT \times N) + \frac{N}{L} \times V_{D1} \qquad [6\text{-}3]$$

$$L = \frac{\frac{\partial V_{D1}}{\partial T}}{\left(n \times N \times \ln(k) \times \frac{\partial V_T}{\partial T} \right)} \qquad [6\text{-}4]$$

$$N = \frac{V_{REF,req}}{n \times V_T \times \ln(k) + \left(\frac{V_{D1}}{L} \right)} \qquad [6\text{-}5]$$

$$\frac{\partial V_{REF}}{\partial T} = \left(n \times N \times \ln(k) \times \frac{\partial V_T}{\partial T} \right) + \left(\frac{N}{L} \times \frac{\partial V_{D1}}{\partial T} \right) \qquad [6\text{-}6]$$

In this study, a 400 mV reference voltage is chosen based on previous measurement of diodes. The measure reference voltage across the temperature range of 27 to 275°C is shown in Figure 6-3.

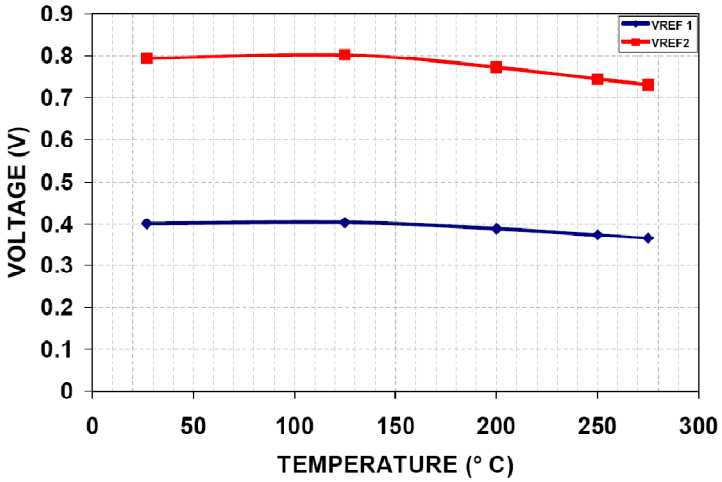


Figure 6-3. Measured value of reference voltage at various temperatures.

6.2.2 Comparator

A comparator circuit compares the two signals at its input and provides a digital output. The reference voltage of 400 mV demands PMOS input design for proper operation. The schematic of the comparator is given in Figure 6-4. The RP and RN transistor represents regular high threshold voltage (Vt) devices. The PL and NL devices are low Vt devices that are used in series with high Vt devices. This novel stacking of high Vt and low a Vt transistor yield higher early voltage and also control the kink effect. As the comparator is used in the fast feedback loop, the bandwidth of the comparator must be as fast as possible at it will set the switching or clock frequency of the system. The cascaded configuration of error amplifier and comparator affects the feedback loop gain and hence the stability of the system. The extracted value of open loop gain of the comparator at elevated temperatures is given in Figure 6-5. In case of transient response the intrinsic and transition time are major factors that decide the system performance. The measured values of delays are given in Figure 6-6.

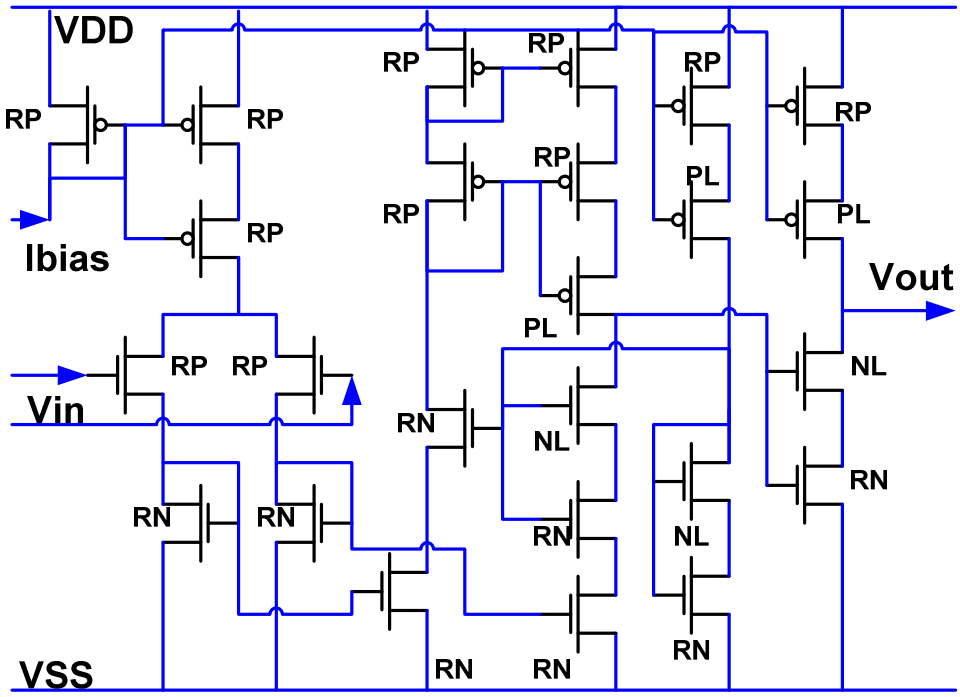


Figure 6-4. Schematic of comparator.

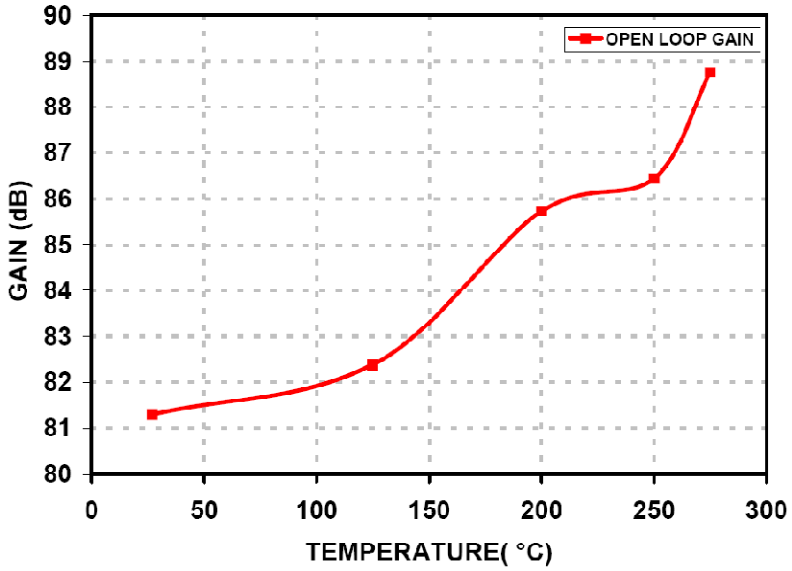


Figure 6-5. Open loop gain of comparator at elevated temperatures.

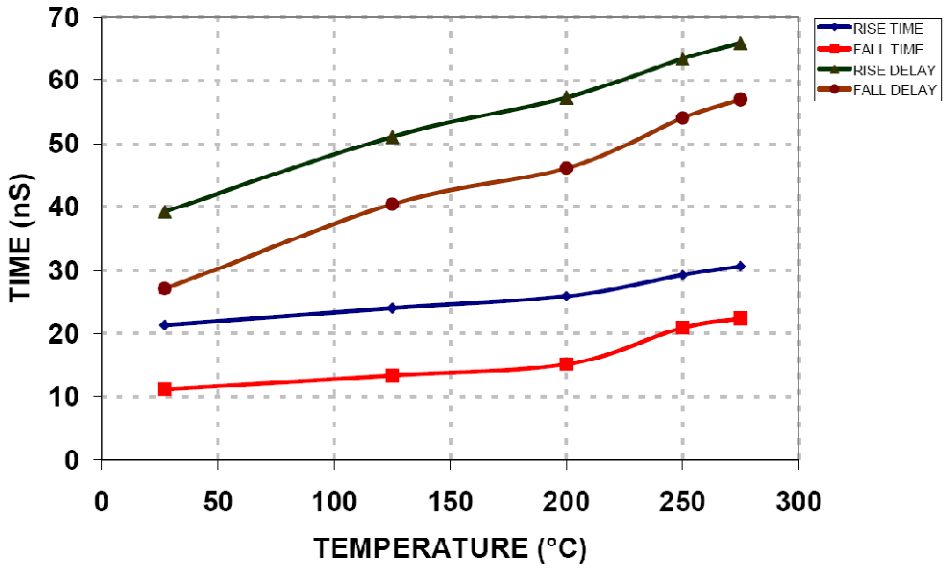


Figure 6-6. Transient characteristics of comparator at elevated temperature.

6.2.3 Hysteretic comparator

A hysteretic comparator is a special type of comparator with a memory. The memory of the comparator is called the hysteretic window. Unlike a normal comparator with two inputs, the hysteretic comparator consists of single input and two reference inputs. The reference inputs set the hysteretic window of the comparator. The upper threshold and

lower threshold determines the transition of the state at the output. In this work the hysteretic comparator is realized using dual comparators and a digital logic as shown in Figure 6-7. The performance of the hysteretic comparator at various temperatures is shown in Figure 6-8. A hysteretic comparator is a building block for the under voltage lockout circuitry discussed in section 6.3.5

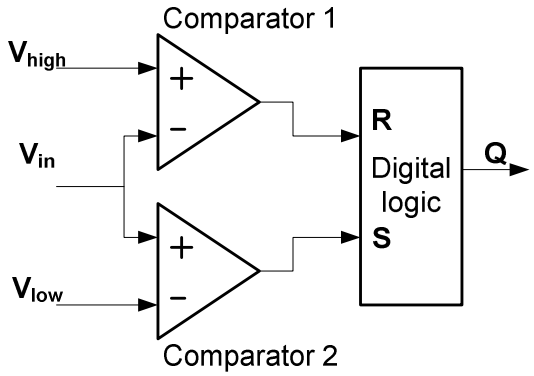


Figure 6-7. Block diagram illustrating the implementation of hysteresis using dual comparators.

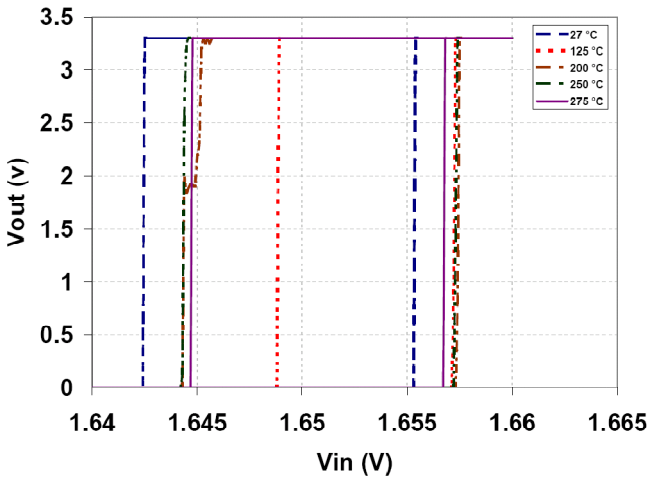


Figure 6-8. Memory window of hysteretic comparator over temperature range of 27°C to 275°C.

6.2.4 Amplifier

An error amplifier is required to amplify the error signal between the instantaneous output voltage and the reference voltage. Since the output and gain of the error amplifier sets the dc accuracy, the input offset at the error amplifier inputs must be considered. As

mentioned before, the error amplifier is used in the slow feedback loop and hence its bandwidth is not of limited concern.

In this design long channel transistors with considerable area are used for designing the input and mirroring transistors to obtain better matching and higher open loop gain. This helps in reducing the input offset voltage, 1/f noise and control the kink effect of the OTA. The transconductance of the error amplifier is chosen based on the availability of high temperature compensation capacitors . This is previously discussed in section 4-2. The schematic of the error amplifier is shown in Figure 6-9.

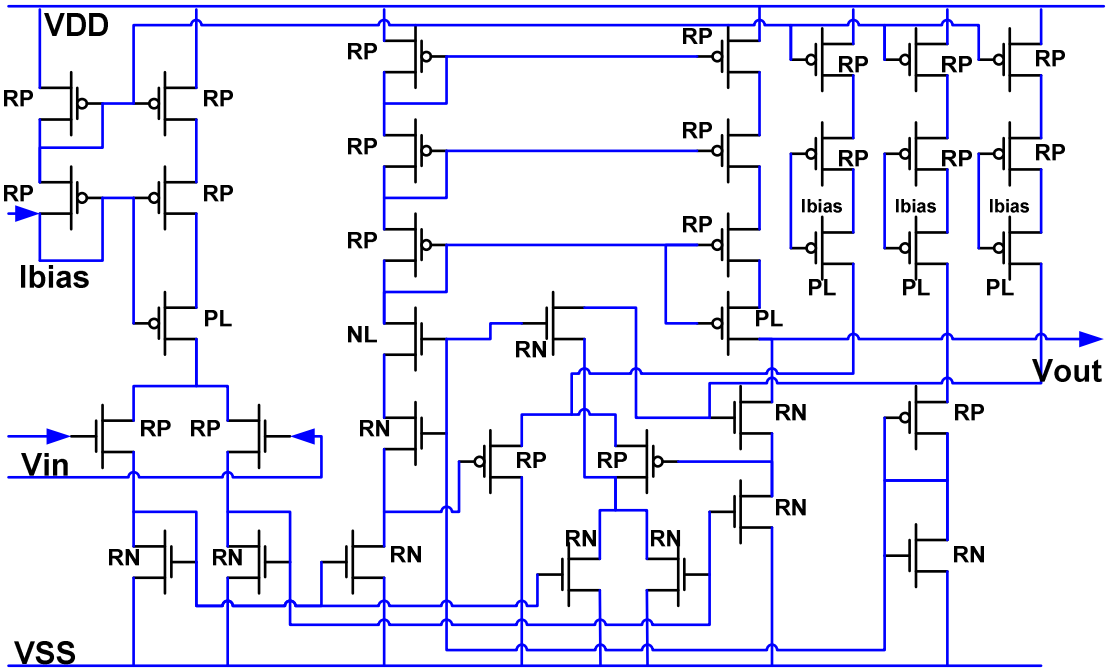


Figure 6-9. Schematic of the error amplifier circuit.

6.3 Supporting blocks

In addition to the basic building blocks several other digital gates and oscillators are required for the complete system. With use of the basic building blocks discussed in the

previous section several supporting blocks are also developed for use in the design. These are discussed in the following section.

1. System oscillator
2. Gate drive oscillator
3. Low side buffer
4. Shunt regulator
5. Zener regulator
6. Non overlap clock generator
7. Under voltage protection
8. Over current protection / Startup circuit
9. Duty clamp circuit
10. Power on reset

6.3.1 Oscillators

6.3.1.1 System oscillator

A system oscillator sets the operating frequency of the PWM converter during normal operation. Various methods exist to implement oscillator circuits. In order to improve the versatility of the control system to various converters, a voltage controlled oscillator (VCO) is implemented in this work. As suggested by the name, the oscillation frequency of a voltage controlled oscillator is a function of a control voltage. In this work a Schmitt trigger based design is adapted. The schematic of the oscillator is shown in Figure 6-10.

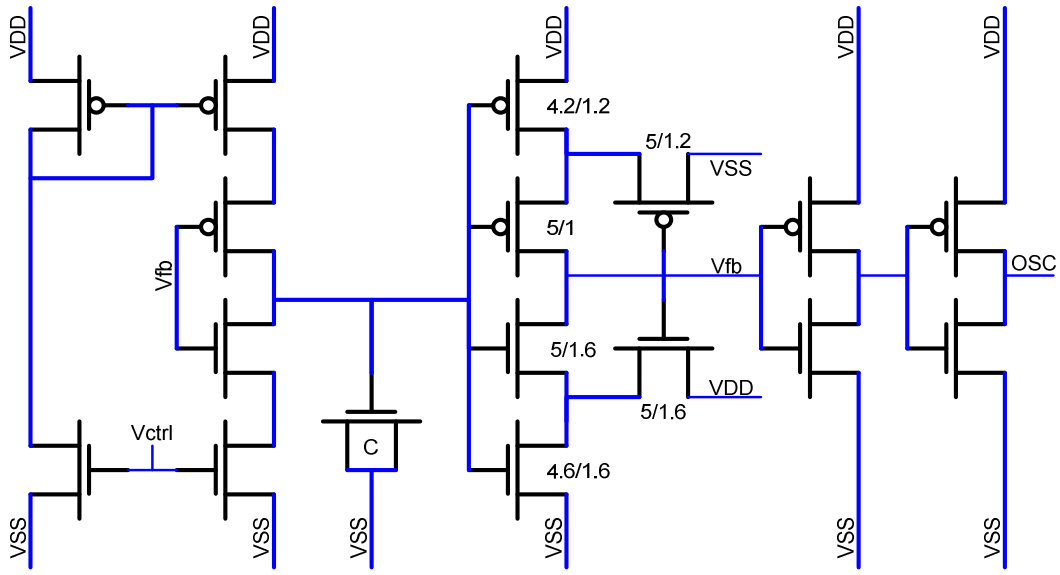


Figure 6-10. Schematic of the Schmitt trigger based oscillator circuit.

A current starved inverter circuit charges and discharges the input capacitor of the Schmitt trigger. The current is set by the externally applied control voltage. The trip points of the Schmitt trigger are based on the device dimensions. The oscillation frequency is given by equation 6-7. The design is based on 100 KHz oscillation frequency for 0.8 V control input.

$$f_{OSC} = \frac{I}{C \times 2 \times (V_H - V_L)} \qquad [6\text{-}7]$$

where, I – Controlled current; function of control voltage.

C – Capacitance at input of Schmitt trigger

V_H – Upper trip point of Schmitt trigger

V_L – Lower trip point of Schmitt trigger

It must be mentioned that the issues associated with oscillator clock jitter is considered to be negligible in this case. Also due to device mismatches, a non 50% duty cycle is expected. The measured frequency characteristic of VCO at various temperatures is shown in Figure 6-11. The oscillator has a near linear frequency response between 100 KHz and 200 KHz at all temperatures and hence satisfies the design requirement.

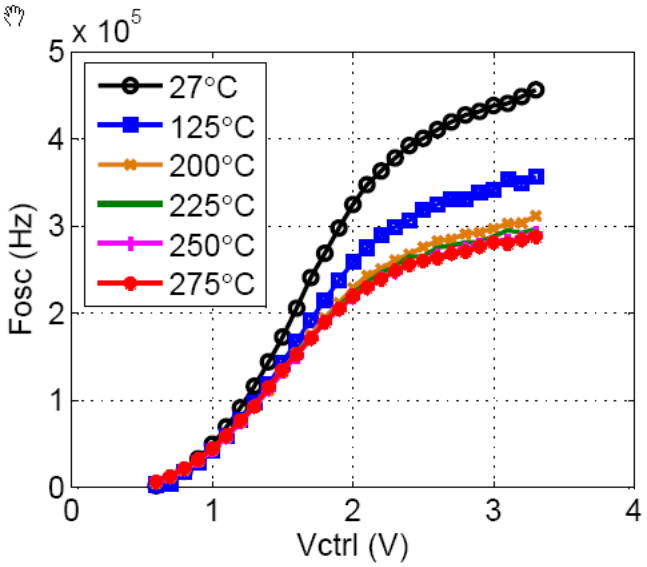


Figure 6-11. Control voltage versus oscillating frequency of VCO at different temperatures.

6.3.1.2 Gate drive oscillator

Gate drive oscillator is used to provide differential clock for the high side gate drive transformer. The gate drive transformers are driven by the clock buffers as described in previous chapter, 5.7It is desirable that the frequency of operation of gate drive circuitry is orders of magnitude higher than the control loop frequency by at least 20 times to minimize the turn on delay of high side gate drive. This requires a standalone oscillator for its operation. In this work the system oscillator is reused without the capacitor at the input of Schmitt trigger. The absence of capacitor makes the rise and fall delays shorter and in turn makes the switching frequency higher and in turn the frequency if oscillation greater . This replaces the value of ‘C’ in equation

[6-7]

with the parasitic capacitance present in the node. The voltage control mode provides a convenient means of selecting the operating frequency to match the transformer characteristics to obtain maximum efficiency if desired. The design is capable of switching from few KHZ to 50 MHz. It is not possible to explicitly measure the output

waveform since addition of probe pads to the node adds parasitic capacitance. This along with use of long probing leads result in instability and or loading of the circuit at high frequencies.

6.3.2 Low side buffer

Low side buffer is used to drive the gate capacitance of the synchronous switch at the system clock frequency. The design of buffers for low side switch is relatively straight forward. The design is based on the capacitive load (C_{ISS}) the silicon carbide JFET and the required switching rise/fall times. The input capacitance of the low side JFETs vary with their capabilities and process. A worst case capacitance of 200 pF is assumed in this design based on measured data presented in chapter 3. If the value of C_{ISS} is found to be great, multiple buffers can be paralleled to achieve the desired specification. The current required for a known capacitor load, C_{ISS} and a predetermined slew rate is given by equation 6-8.

$$i = C_{ISS} \times \frac{dV}{dt} \qquad [6\text{-}8]$$

For a 200 pF capacitance and a 3V/50nS slew rate, the current required is greater than 12 mA. A capacitive loaded buffer circuit is also equivalent to a RC delay. The time constant of the circuit is given by equation 6-9. Using a load capacitance value of 200 pF and a rise / fall time requirement of 50nS, the requirement of ON resistance of the transistor, from measurements is found to be less than 115 ohms. This criterion is easily met with the buffer designed using capacitive equation.

$$\tau = 2.2. \times R \times C \qquad [6\text{-}9]$$

From peregrine data sheet, ‘50/0.5’ device provides 16 mA of current for typical model and at 25°C. Assuming a pessimistic ‘4 X’ degradation for 275°C and 1.6 device length, the final dimension required is approximately, ‘600/1.6’. Starting with ‘1 X’ inverter of

‘2.8/0.8’ and ‘2.8/1.6’ and keeping the lengths constant, the tapering of buffers is as follows

Tapering – 3@3/, 5@6/, 5@20/, 20@15/1.6

The transistor level schematic and the simulated characteristics are shown in Figure 6-12. The performance of the buffer circuit at elevated temperatures and various process model files are given in Figure 6-13.

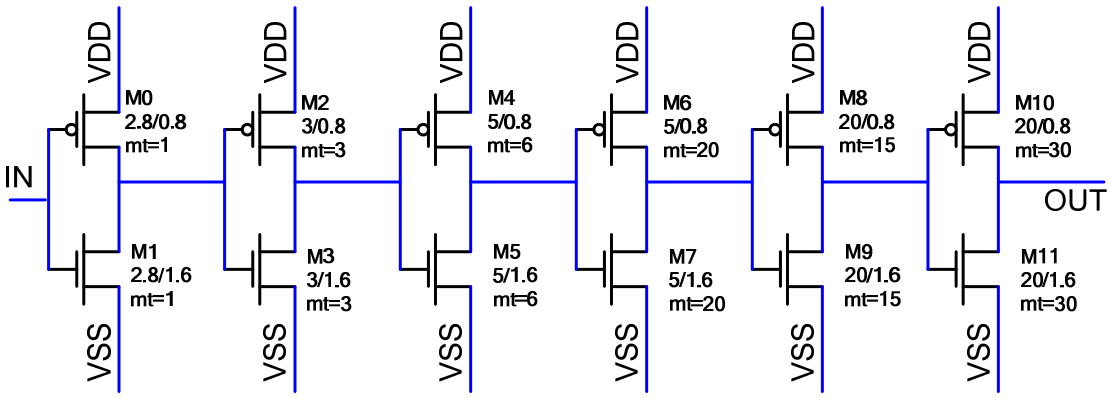


Figure 6-12. Schematic of the low side buffer

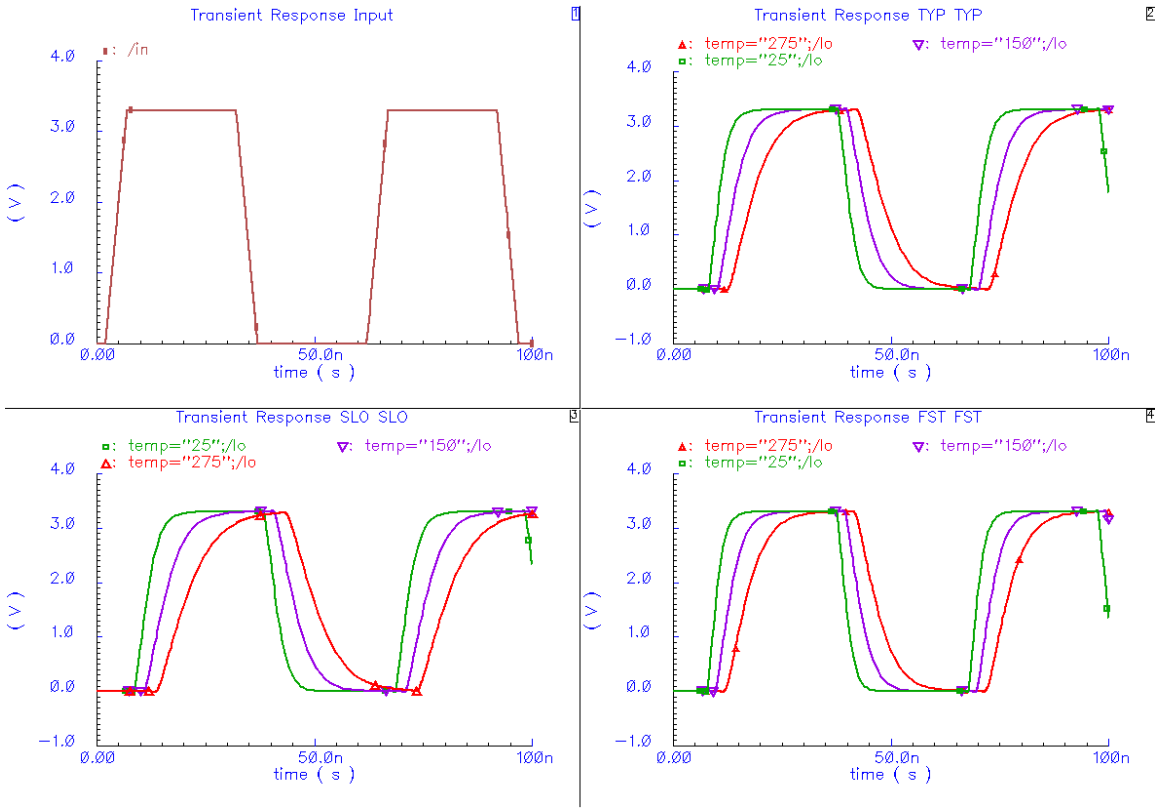


Figure 6-13. Input and Output waveforms of the low side buffer across typical, slow and fast corner at 25, 150 and 275°C

6.3.3 Internal voltage generator

6.3.3.1 Shunt regulator

The input voltage to the dc-dc converter can be arbitrary and is usually limited by the power switches via either the standoff voltage or the on resistance. The control circuitries operate under a 3.3 volts supply voltage. This power is derived by using an on-chip shunt regulator. Since the circuitry is on-chip the maximum input voltage is limited by the breakdown strength of the substrate. Proper layout care has to be taken to avoid excessive field strengths between adjacent diffusion regions in transistors. The schematic of the internally implemented voltage reference is shown in Figure 6-14. The physical size of this block is determined by the maximum load current and the input voltage. Higher load current requires wider pass gates in voltage absorber (reducing Ron) at lower operating

voltage. Lower load current requires wider shunt gates in voltage limiter at highest input voltage. The performance of the raw voltage shunt regulator is shown in Figure 6-15. A trade-off between the two is chosen here. It is important to note that the stability of the circuit is dependent upon the capacitors C1 and C2. The value of C2 has to be much larger than C1 to avoid instability and to prevent oscillations at output.

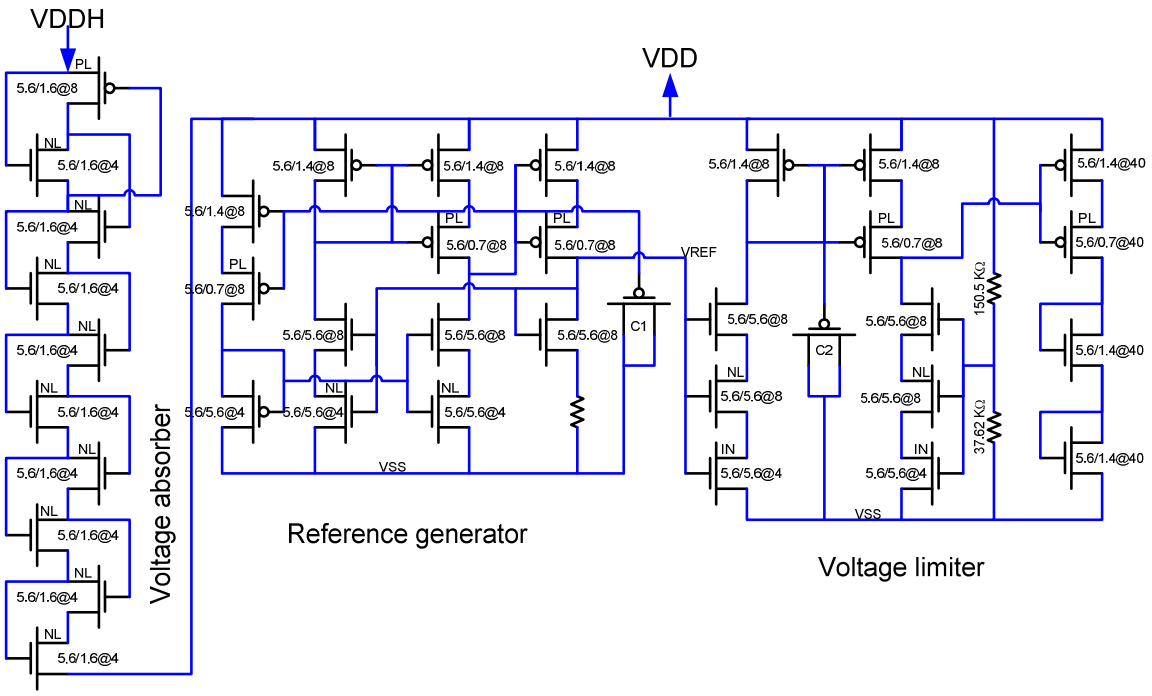


Figure 6-14. Internal power generation using shunt regulator.

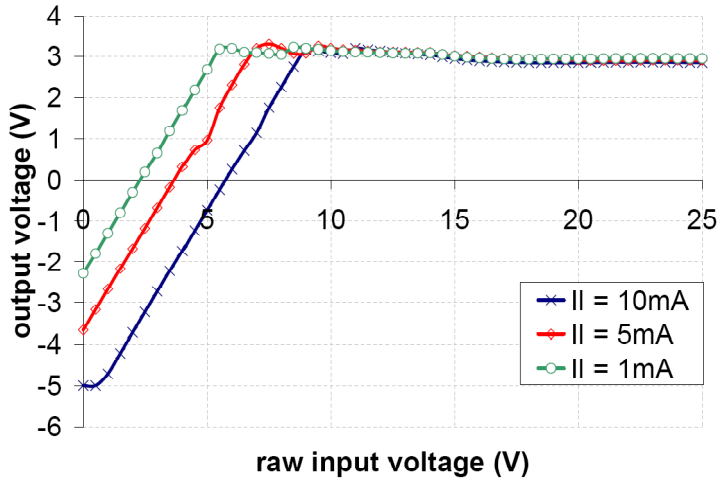


Figure 6-15. Characteristics of the shunt regulator circuit for various load currents.

As shown in the figure there are 3 main sections in the regulator. The first section is the voltage absorbing section where the high voltage is input is dropped to a lower voltage in a cascading fashion. The number of cascaded stages imposes a lower limit on the input voltage. The middle section is an internal reference generation part. The final section comprises a comparator unit and a shunt arm. The comparator compares the reference voltage with the instantaneous output voltage and controls the shunt transistors accordingly. The shunt transistors vary the output impedance in order to maintain the output voltage at required level.

6.3.3.2 Zener regulator assisted startup

The shunt regulator discussed above suffers from a basic limitation of power dissipation. The power lost in the shunt path to maintain a stable operating voltage increases proportionally to the input voltage and hence is not desirable. An alternate approach is proposed using Zener behavior of transistors is shown in Figure 6-16. Rather than a continuous power supply generator the proposed circuit kick-starts an auxiliary power supply that powers the main system. The operation of the circuit is described as follows.

The peregrine semiconductor fabrication process used in this work does not provide Zener diodes. The reverse transistors breakdown of the transistors mimics the operation of a Zener diode and hence adopted as substitute. However unlike a Zener diode where the reverse breakdown voltage is limited by process, the breakdown voltage of the transistor is dependent upon the channel length of the device.

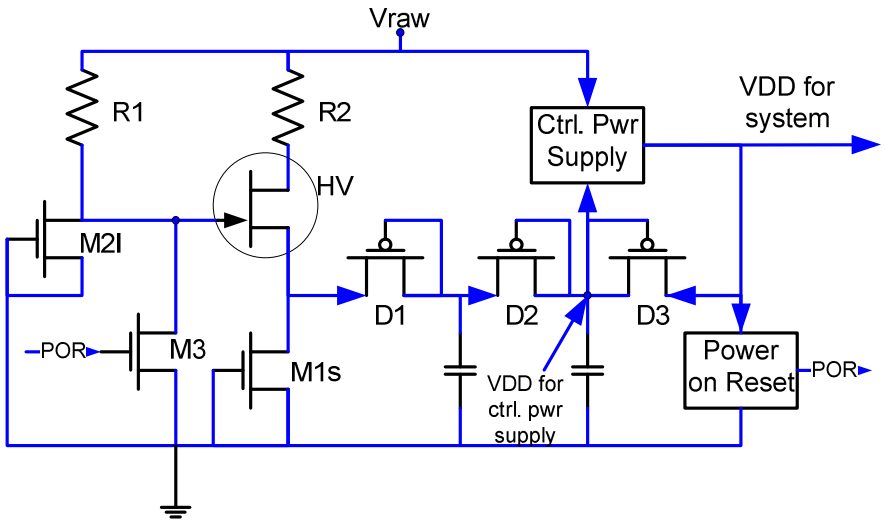


Figure 6-16. Zener based startup circuit for internal voltage generation.

The transistors M1s and M2l provide a gate source voltage for a discrete high voltage (HV) JFET/ MOSFET device. The gate-source voltage developed is due to difference in breakdown voltage of the short channel and long channel NMOS. The diode D1 and D2 feeds the internal power supply line to start the auxiliary control power supply. The control power supply develops the required voltage which is feed into the internal power line through diode d3. A power on reset circuit operating under the main power rail shuts down the startup circuit preventing continuous power dissipation.

The inherent drawback of the design is the requirement of an external discrete transistor (i.e. SiC JFET) to absorb the high voltage after start up cycle. From experimental results the breakdown voltage of the long channel and short channel devices are measured at different ambient temperatures. Figure 6-17 shows the obtained results. Since the breakdown voltage of the M1s is between 4 V to 6 V the series connected diodes D1 and D2 helps to reduce the voltage level applied to control power supply.

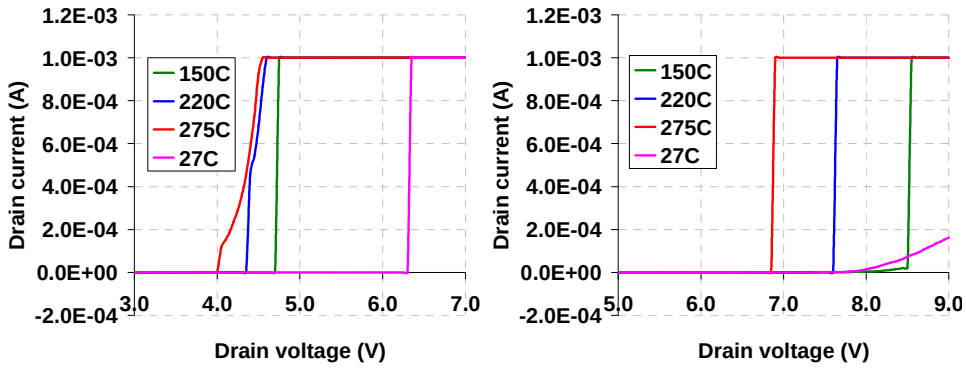


Figure 6-17. Breakdown characteristics of short channel (10 µm / 0.8 µm, left) and long channel (10 µm / 1.0 µm, right) NMOS

6.3.4 Non overlap clock generator

Non overlap drive signals are a must for high side and low side switch control. Overlapping clocks create “shoot through” and the input supply is shorted to ground. This highly degrades the performance of a converter. Designing non overlapping clocks with automatic delay control is of great interest. In this work a preset delay time is fixed based on the turn off times of the silicon carbide JFETs. The delay is based on a “RC” time constant. Additional pins are provided to increase this delay by externally addition capacitance to the RC network. The schematic of the non overlap clock generation circuit is shown in Figure 6-18. It must be noted that the turn of the switch is delayed whereas turn off is immediately applied by use of an “AND” gate.

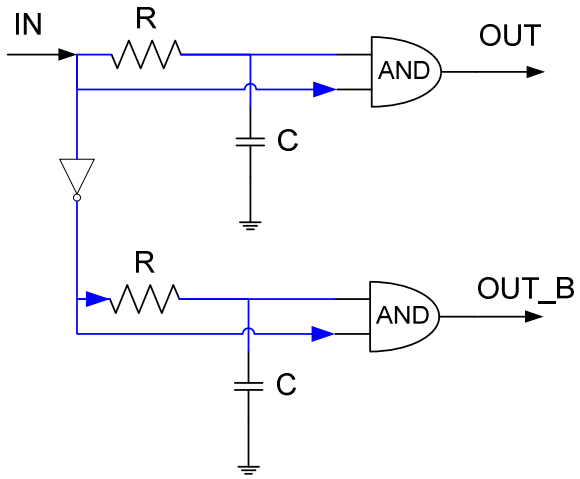


Figure 6-18. Generation of non overlapping drive signals.

6.3.5 Under voltage protection

The control loop circuitries require a stable input voltage for its operation. The under voltage lock out (UVLO) circuitry continuously monitor the supply voltage to the controller. In case of a droop in the supply voltage below a preset limit the switching operation is stopped. The schematic of the UVLO circuitry is shown in Figure 6-19. In order to avoid noises a range window has been set using a hysteretic comparator. The set voltage and trip voltage are set to be 2.7 V and 3.0 V. The selection of these voltage levels is based on the measured characteristics of individual analog blocks and their power supply rejection ratios. A more important factor is the gate drive circuitry which requires a worst case voltage of 2.7 V (at low temperature) at primary side to achieve a minimum required turn on voltage (2.1 V for SiC JFET) on the secondary side. Reference voltages corresponding to these set and trip voltages are derived from the system reference voltage using the resistive divider networks as shown in the figure. The operation of the circuit is shown in Figure 6-20.

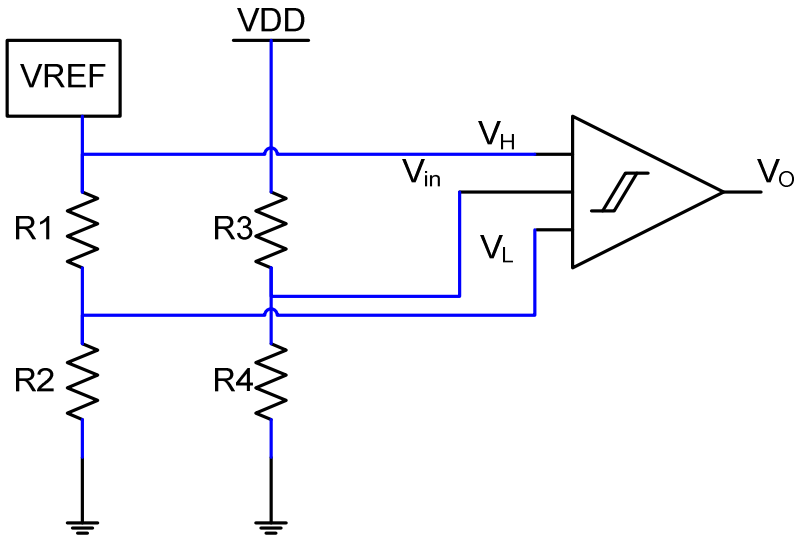


Figure 6-19. Under voltage lock out circuitry.

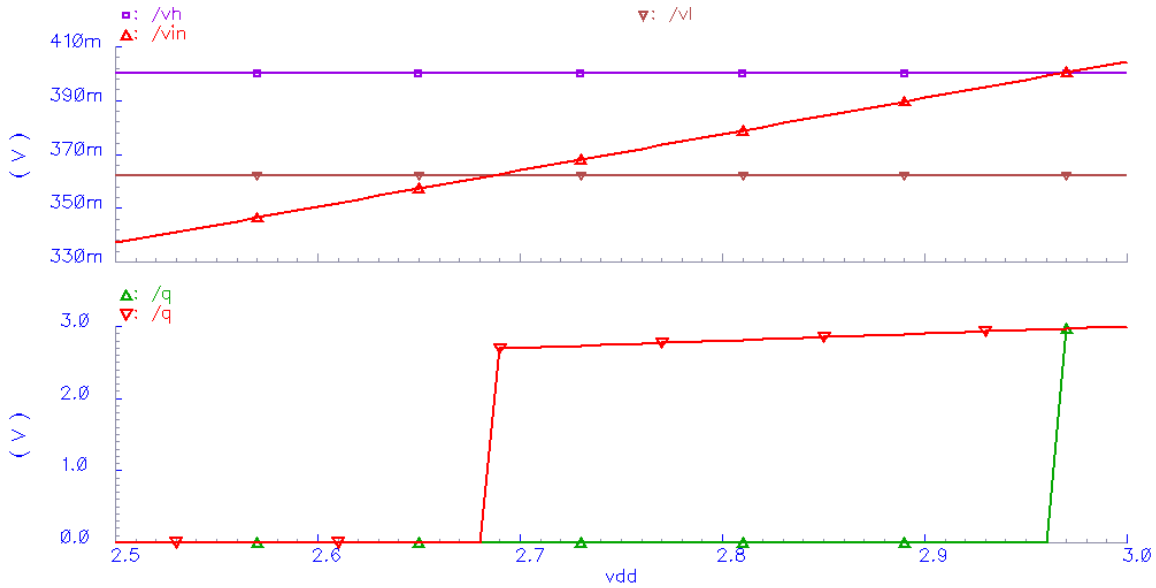


Figure 6-20 Operation of under voltage lock out circuitry.

The measured characteristic of the under voltage lockout circuitry is shown in Figure 6-21. The input supply voltage (VDD) is swept up and down and the response of the UVLO circuitry is observed. The result shows a wider hysteresis window for high temperature (275°C).

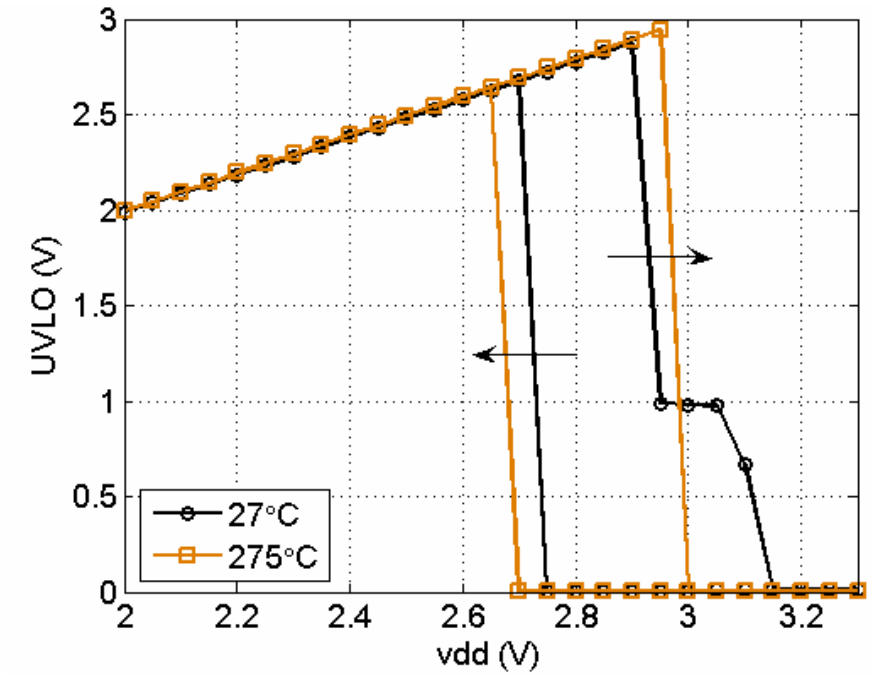


Figure 6-21. Measured characteristics of UVLO circuitry at room temperature and 275°C.

6.3.6 Over current protection

A startup circuit is implemented to prevent the sudden inrush of current through the system when it is turned on. Theoretically V2 controller does not require a startup since the switching is based on the dc reference voltage set by the error amplifier. The RC charging of the compensation capacitor determines the startup characteristics. In this study an independent startup circuit is implemented using a controlled current source. The compensation capacitor is charged using this current source until a preset level is reached after which the start up circuit is disabled and normal operation is started. The block diagram of startup circuit is shown in Figure 6-22.

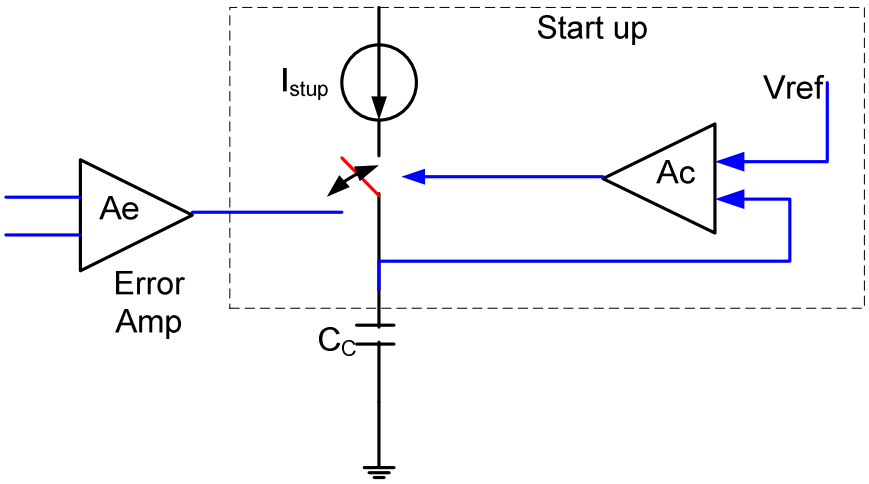


Figure 6-22. Startup implementation.

6.3.7 Duty clamp circuitry

In order to set a maximum ON time in a switching cycle, a duty clamp circuitry is implemented. As mentioned before the V2 control enables turn on of power switch to 100 percent duty cycle which is a continuous ON state. This will cause self heating of the power switches as described in chapter 3 and hence would severely affect the system performance. The schematic view of the implemented duty clamp circuitry is shown in Figure 6-23. The duty clamp operation is based on a RC time constant. The RC charging waveforms and output waveforms of the circuit is given in Figure 6-24.

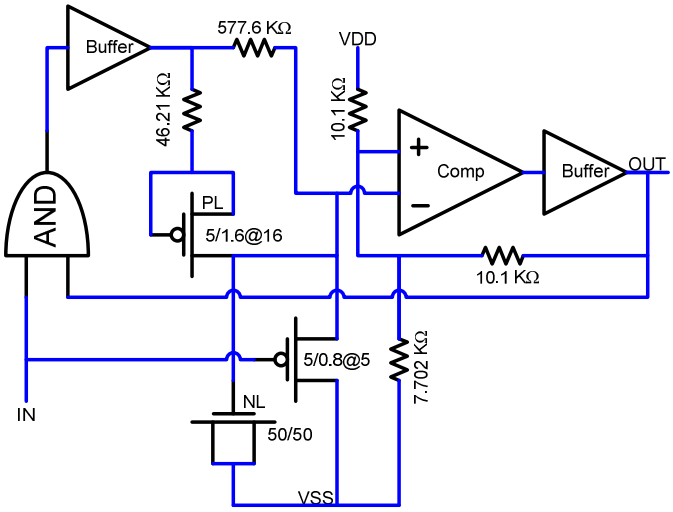


Figure 6-23. Schematic of the duty clamp circuit.

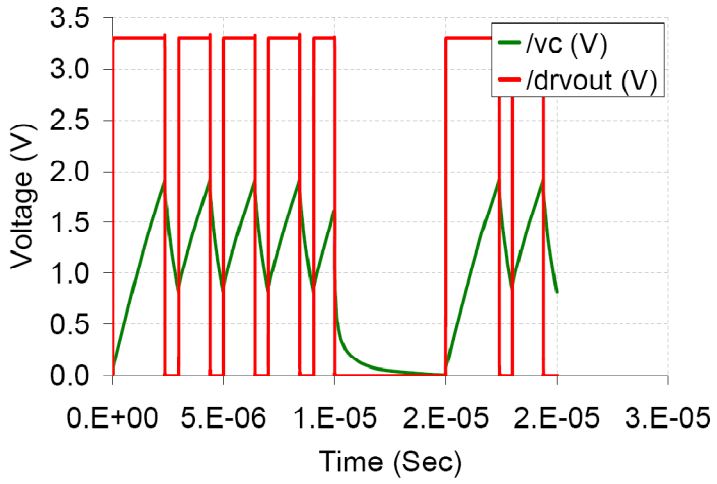


Figure 6-24. Duty clamped output waveform and the voltage across the capacitor.

6.3.8 Power on reset

A power on reset signal is a control signal to start the operation of various blocks of the control system. Normally in a digital design a power on reset circuit is used to reset (initialize) the state of flip-flops (registers) to a required binary level. The voltage reference block serves as a basic unit in the feedback loop. In order to hold the controller operation until a stable reference voltage is obtained from the voltage reference block a power on reset signal is used. A power on reset signal places the controller in reset mode

for long enough to ensure a stable reference voltage. The schematic of the power on reset circuit is shown in Figure 6-25. The characteristic operation of the power on reset circuit is based on the rise time of the raw input power (VDD). Typical rise time for modern electronics circuits are in order of sever hundred µS to few mS. The response of the POR circuit for a 10 mS rise time at room temperature and 275°C is given in Figure 6-26 and Figure 6-27, respectively.

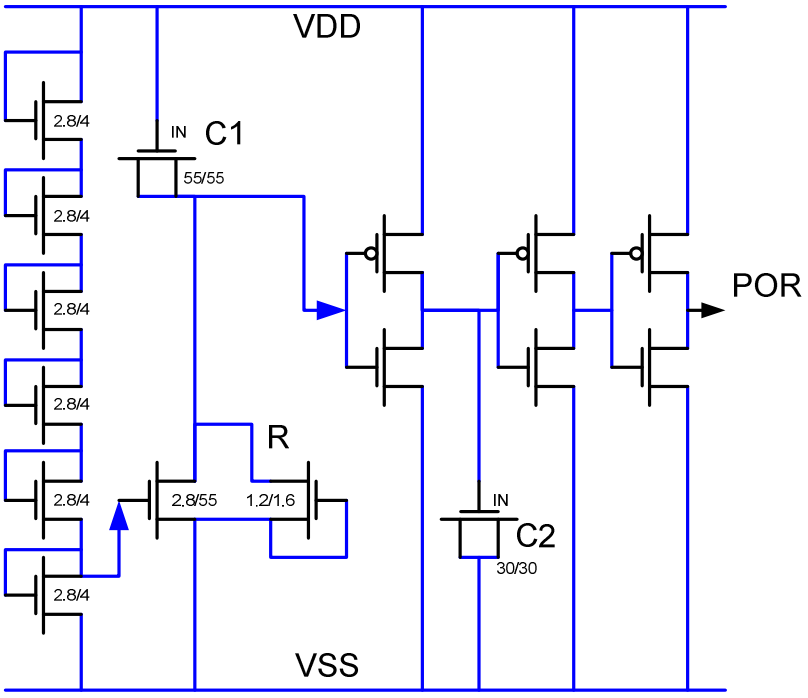


Figure 6-25. Schematic of the on chip power on reset circuitry.

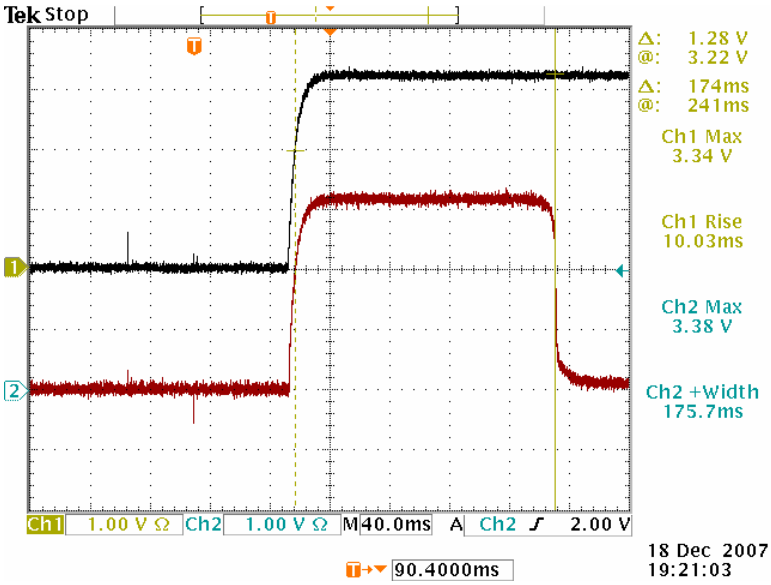


Figure 6-26. Transient response of power on reset circit for 10 mS VDD rise time at room temperature.

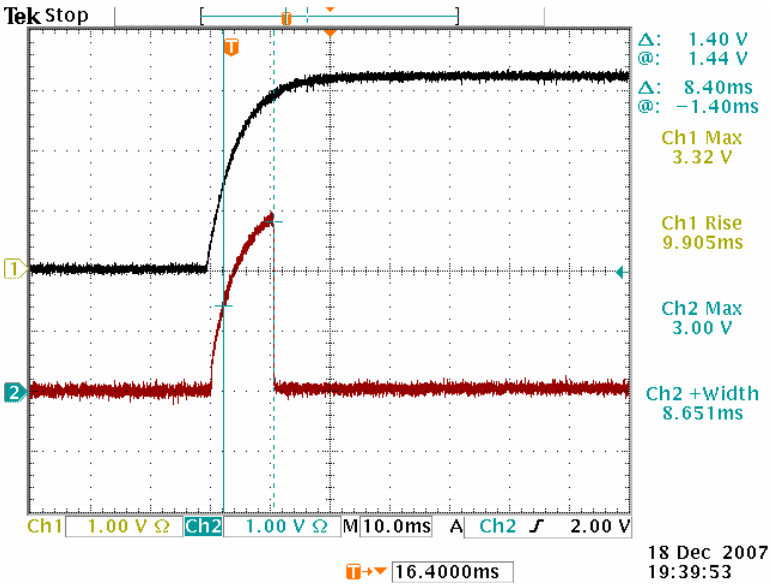


Figure 6-27. Transient response of power on reset circuit for 10 mS VDD rise time at 275°C.

6.4 Layout

The complete control circuitry that includes the auxiliary electronics is implemented in the Peregrine 0.5 micron SOI (FC) process. The pin configuration of the controller is shown in Figure 6-28. The overall layout view including the input-output pad frame is shown in Figure 6-29. The total die size is 3 mm × 2 mm. The individual circuits are pointed out in the figure. The layout of the controller is shown in. The die snapshot of the fabricated V2 controller is shown in Figure 6-30.

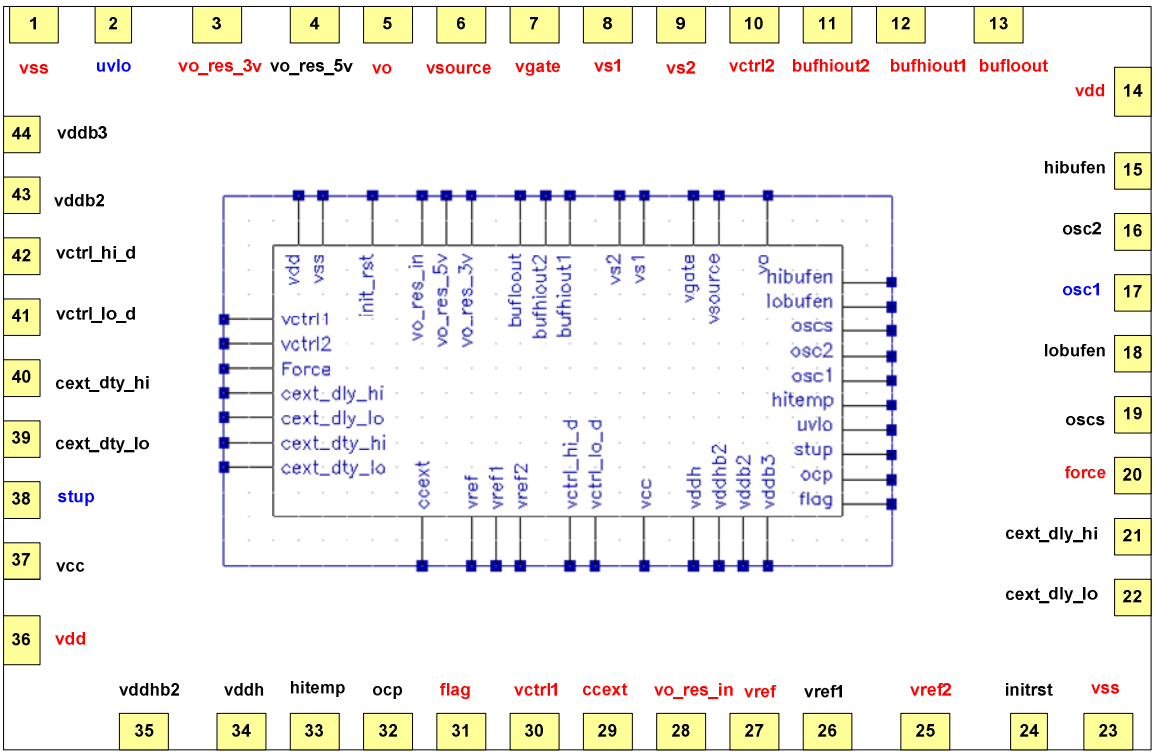


Figure 6-28. Pin configuration of V2 control chip.

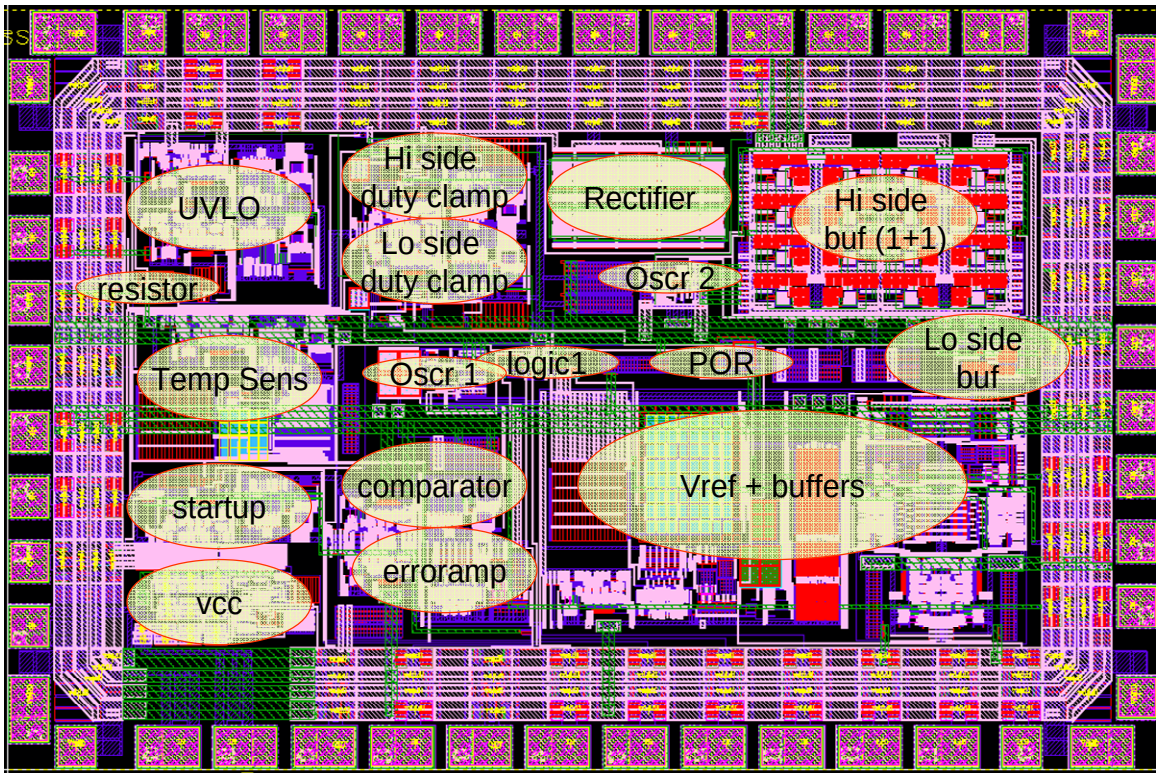


Figure 6-29. Layout snapshot of the V2 controller chip.

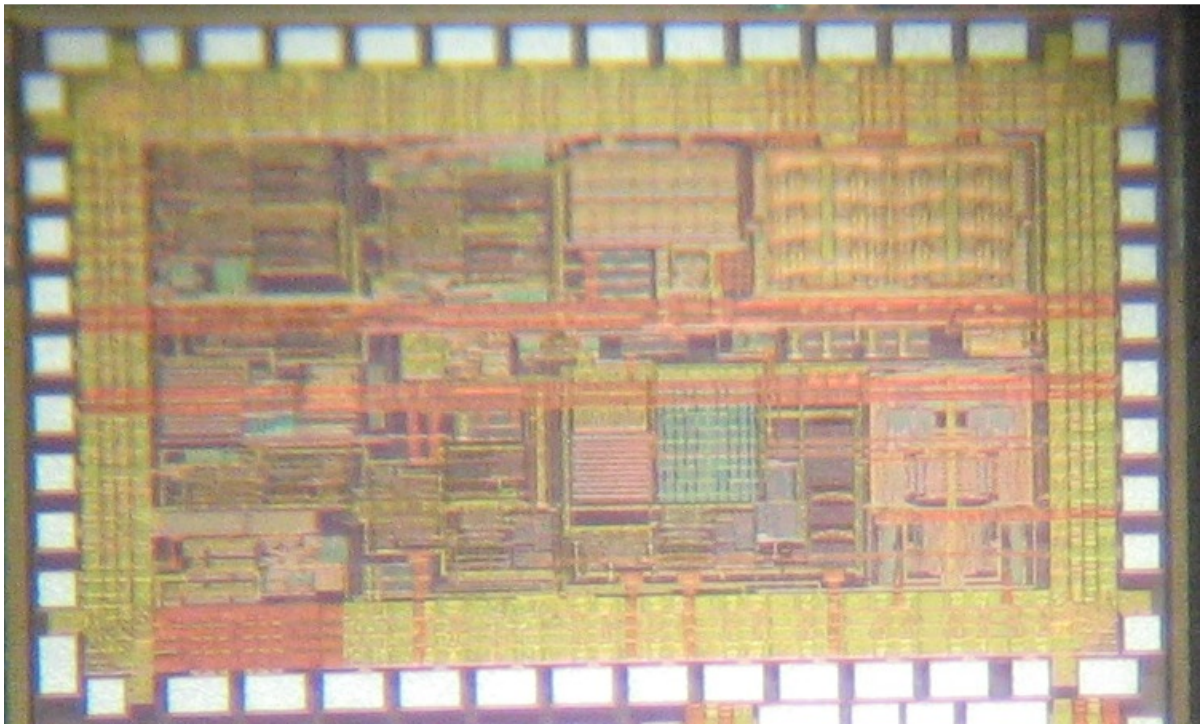


Figure 6-30. Fabricated dice of the controller chip.

Chapter 7

7.1 Passive devices

Inductors and capacitors are inevitable in power supply designs. Effort to integrate these components on chip has been limited to extremely low power applications. Medium and high power converters require off chip, discrete components for filtering the output. Identification of passive components for high temperature design is not a trivial task. Commercially available passives are tested only up to 125°C for military and automobile market and in some cased to 200°C for niche applications. The selection of inductors and capacitors used in this work is discussed in the following sections.

7.1.1 Inductors

Molybdenum Permalloy power (MPP) cores are adopted for use in the output filter. The selection is based on the previous reports of high temperature behavior of MPP cores [101-103]. Selection of inductors is much less of a hassle compared to the other components. MPP cores are commercially available at various sizes from several vendors. The size of the core depends on the inductance requirement and the permeability of the core. The formula for computing inductance of a coil is given by equation 7-1.

Inductance of coil, $$L = \frac{\mu_o \times \mu_r \times N^2 \times A}{l} \quad [7\text{-}1]$$

Where,

$\mu 0$ – permeability of free space = $4\pi \times 10\text{-}7$ H/m

μr – relative permeability of core material

N – number of turns

A – area of cross-section of the coil (m2)

l – length of coil (m)

The performance of MPP core inductors evaluated for use in the design is shown in Figure 7-1. A nearly independent characteristic with temperature is evident from the result. The quality factor of the inductor is also given in secondary axis of the figure.

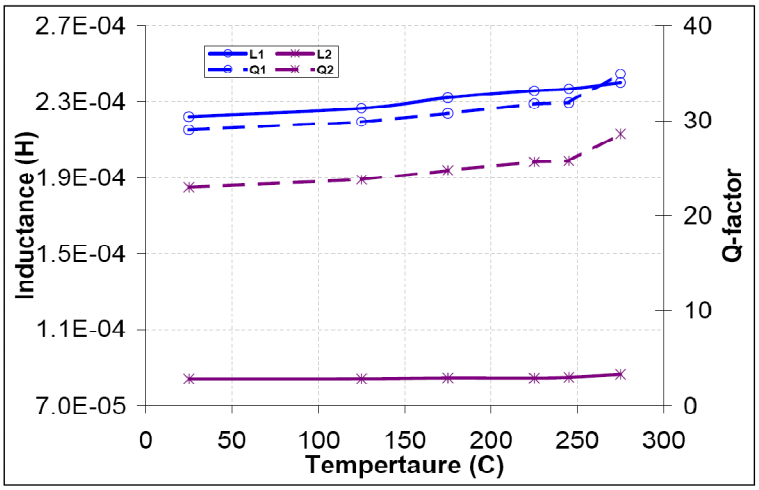


Figure 7-1. Performance of MPP core inductors over the temperature range of 25 to 275°C.

7.1.1.1 Calculation of load inductance

The value of load inductance required for the buck converter can be computed from the switching frequency, required load current ripple, input and output voltage. The transient current through an inductor and voltage across the inductor can be described by equation 7-2. By rearranging the equations, the inductance is given by equation 7-3.

$$e = L \times \frac{dI}{dt} \qquad [7\text{-}2]$$

$$L = \frac{(V_{in} - V_{out}) \times T_{ON}}{\Delta I} \qquad [7\text{-}3]$$

The equation is rewritten in terms of duty cycle (V_{out}/V_{in}) and switching frequency (f_{sw}). Hence the final equation for calculating the inductance is given by 7-4.

$$L = \frac{(V_{in} - V_{out})}{I_{\max} \times RF} \times \left(\frac{V_{out}}{V_{in}} \right) \times \left(\frac{1}{f_{sw}} \right) \qquad [7\text{-}4]$$

where RF is the ripple factor (usually around 30 percent).
The above equation yields a minimum required value of inductance to keep the controller in continuous conduction mode.

7.1.2 Capacitors

Capacitors are the primary limitations for high temperature electronics. Capacitor solutions available for high temperature operation are extremely expensive and often dominate the overall system cost. Overcoming the cost issues is only one issue. High capacitance value capacitors rated for 275°C do not exist commercially. Exhaustive efforts were made in this case to find the suitable parts. Commercially available ceramic capacitors of COG and NPO type do not satisfy the capacitance requirement of the output capacitor. As alternatives tantalum and conductive polymers are tested for their performance at elevated temperature. Figure 7-2 shows the capacitance of 47 µF conductive polymer and 220 µF tantalum capacitors at various temperatures. It must be stated that these capacitors are significantly expensive and hence contribute a major fraction of total system cost.

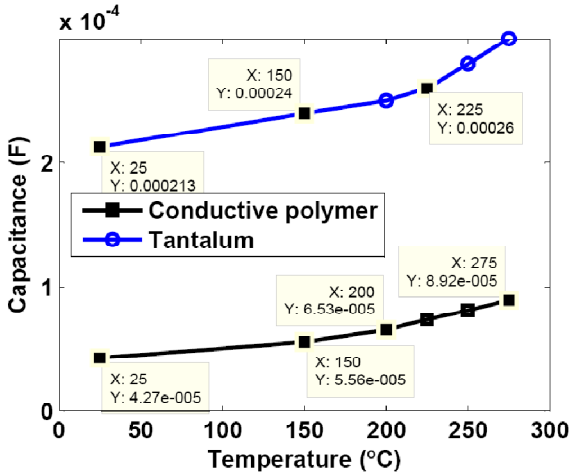


Figure 7-2. Performance characteristics of high capacitance capacitors at elevated temperatures.

The ESR of the capacitor can be obtained from the dissipation factor of the capacitor using equation 7-5. The measured dissipation factor for the high valued storage capacitors are shown in shown in Figure 7-3.

$$ESR = \frac{DF}{\omega \times C} \qquad [7\text{-}5]$$

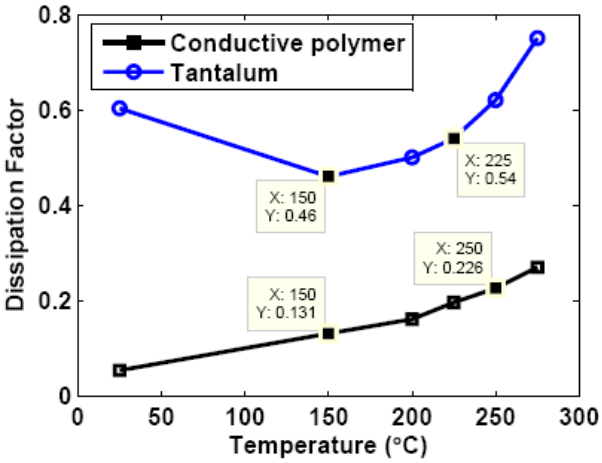


Figure 7-3. Dissipation factor of conductive polymer and tantalum capacitor.

7.1.2.1 Calculation of load capacitance

The value of load capacitance is based on energy transfer between the inductor and the transient load with the capacitor. In order to provide a “switching noise” free output the capacitor has to compensate for the transient disturbance caused by the inductor current and the load changes. For instance a microcontroller (load) going into a reset mode after a complex computation would put the power supply from a near full load to no load transient. This could result in output voltage overshoots with output voltage potentially reaching destructive levels. To avoid such effects the maximum energy capacity of the capacitor should be larger than that of the inductor. The following equations describe the transient effects and the minimum required value of capacitance for a given specification.

The r.m.s value of the overshoot voltage above the nominal output voltage is given by equation 7-6.

$$Vos = rms(Vout, Vos) - Vout = \sqrt{Vout^2 + Vos^2} - Vout \qquad [7\text{-}6]$$

Based on the energy balance, during transient change from full load to no load, the voltage across the capacitor has to increase to sustain the flow of current through the inductor. This results in a charge (energy) balance between the inductor current and capacitor voltage as given by equation 7-7.

$$\frac{L \times \left(Io + \frac{\Delta I}{2} \right)^2}{2} = \frac{C \times Vos^2}{2} \qquad [7\text{-}7]$$

Rearranging,

$$Vos = \sqrt{\frac{L}{C} \times \left(Io + \frac{\Delta I}{2} \right)^2} \qquad [7\text{-}8]$$

Substituting 7-8 in 7-6, we get

$$V_{os} = \sqrt{V_{out}{}^2 + \frac{L}{C} \times \left(Io + \frac{\Delta I}{2} \right)^2} - V_{out} \qquad [7\text{-}9]$$

The required value of capacitance is given by

$$C = \frac{L \times \left(Io + \frac{\Delta I}{2} \right)^2}{\left(V_{out} + V_{os} \right)^2 - V_{out}{}^2} \qquad [7\text{-}10]$$

Choosing the maximum tolerable overshoot and using the pre-calculated inductance, the minimum required capacitance is obtained from equation 7-10.

7.1.2.2 Equivalent series resistance

ESR of the load capacitor is an important factor for stability of the control loop. This has been previously discussed in section 4-2. In case of transient response the ESR of the load capacitor sets the lower limit on the ripple in the output voltage. For a given current, the ESR ripple is given by equation 7-11. In cases where lower ripple is required, a parallel combination of capacitors is used.

$$V_{OUT_{ESR}} = \Delta I \times ESR \qquad [7\text{-}11]$$

7.1.2.3 Compensation capacitor

In addition to the load capacitor the V2 controller requires a compensation capacitor for stable operation of the system. The capacitance values of compensation capacitor are relatively lower than the load capacitor and hence COG and NPO type dielectrics are best suited for high temperature operation. Though these capacitors are relatively expensive,

they are readily available commercially [104]. The performance of a COG type capacitor at elevated temperatures is shown in Figure 7-4.

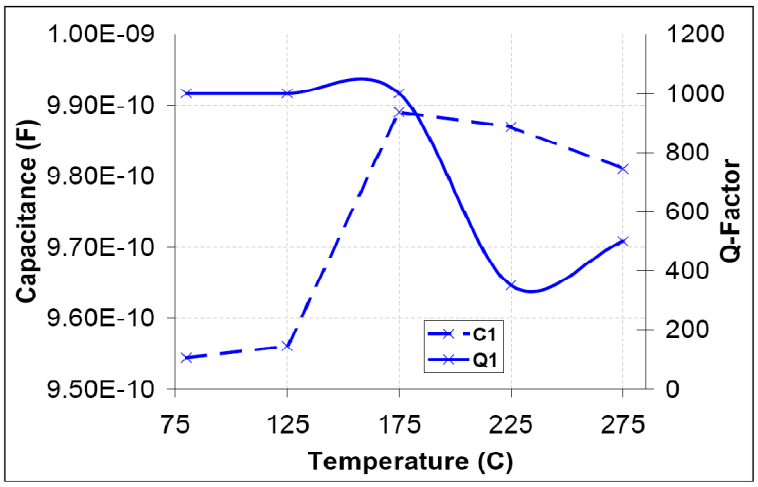


Figure 7-4. Performance of ceramic (COG) type capacitors for high temperature applications.

7.2 Hybrid packaging techniques

This study involves integration of silicon carbide JFETs, SOS control dice and handful of passive components for a complete buck converter design. Making an off the shelf components involves a major task of packaging the device for commercial use. The packaging issues are often overlooked especially for high temperature designs. In these cases packaging solutions have to be custom designed.

The starting point of the packaging issue is the substrate to be used. The commonly used ceramic packages are not good for high temperature designs as the package material. The commercially available alumina (Al_2O_3) is not an efficient thermal conductor. To reduce the thermal stress at the junctions of the power switches, aluminum nitride is commonly used. The thermal conductivity of aluminum nitride is 200 W/m-K whereas the same for 96% alumina package is only 24 W/m-K. This relatively high thermal conductivity of aluminum nitride helps in spreading the junction temperature of the power switches and hence improves the reliability and lifetime of the system.

In this work a custom made aluminum nitride planar board with metal (Gold) routing in top and bottom layer is used as substrate. In order to provide hermetic sealing of the semiconductor devices, an aluminum nitride window frame assembly is custom made. The window frame acts like a wall that encloses the semiconductors and a metallic lid is used to hermetically seal the system. This results in a three step hybrid packaging technique.

- Eutectic / epoxy bonding of SiC JFETs and SOS IC's and passive components to an AlN motherboard/substrate.
- Eutectic attachment of AlN window frame.
- Finally metallic capping of window frame.

A three dimensional perspective of packaging is given in Figure 7-5 .

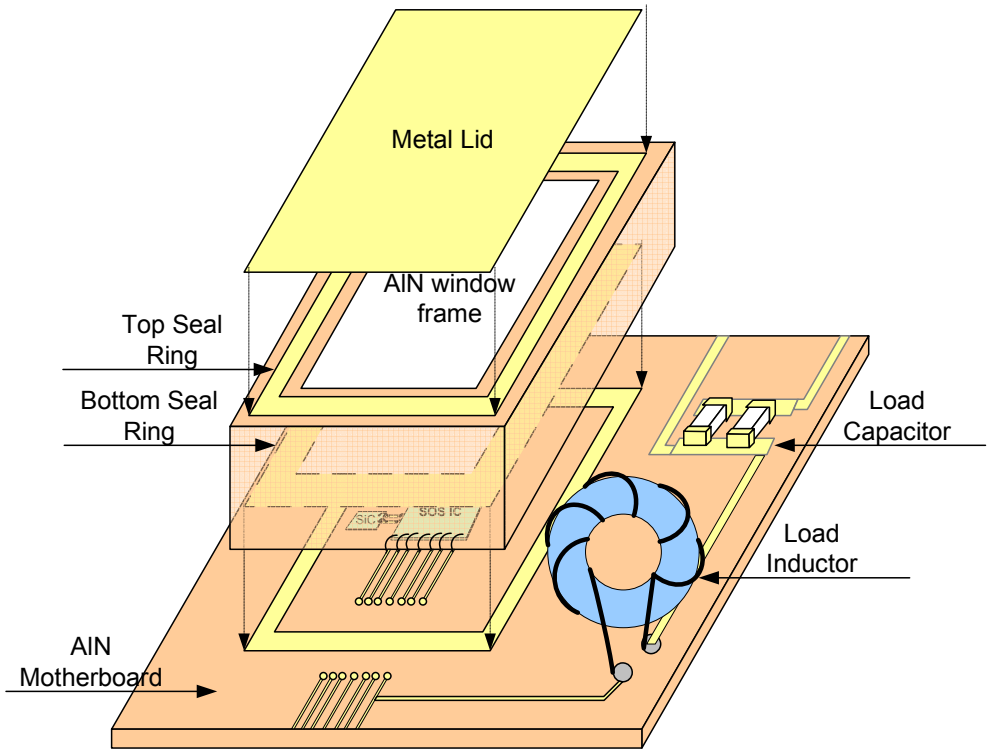


Figure 7-5. Proposed packaging method for dc-dc converter.

7.2.1 Eutectic bonding

Eutectic bonding is a process of attaching die to the substrate using a solder perform. This method of die bonding is applicable only for bonding similar metals. In this study the gold plated silicon carbide dices are bonded to the planar board using gold-germanium (Au-Ge) eutectic solder. Westbond 7200 ES eutectic/epoxy bonder is used to achieve the task.

7.2.2 Epoxy bonding

Epoxy bonding is the most commonly used type of bonding process that uses an epoxy material to glue two components. The SOS control chip is bonded to AlN substrate using thermally conductive, electrically non conductive epoxy. To attach the bulky inductors and capacitors to the substrate, electrically conductive, thermally stable silver filled epoxy is used.

7.2.3 Wire bonding

The bare dices of silicon carbide and control circuitry are bonded using gold bond wires to the planar board. K&S wire bonder is used for this task. Gold wire of two mil thickness is used for power switches to reduce the resistance.

The CAD layout out the aluminum nitride planar board is shown in Figure 7-6.

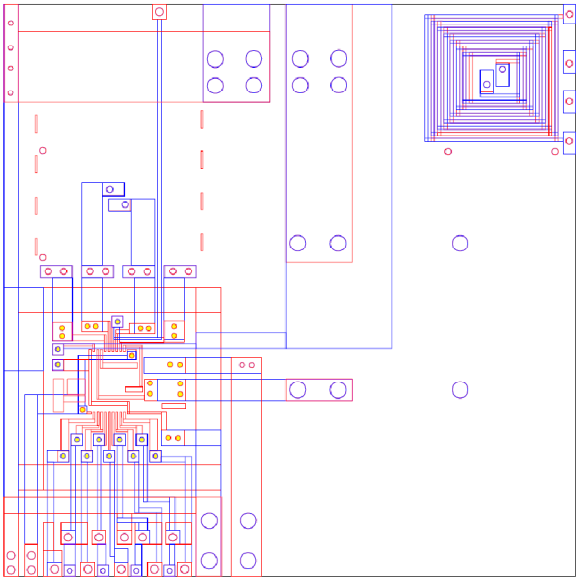


Figure 7-6. AutoCAD layout of the two layer AlN planar board.

Chapter 8

8.1 SMPS Testing Results

8.1.1 Circuit board assembly

A prototype of the SMPS was assembled on Aluminum Nitride (AlN) mother board using eutectic, epoxy and wire bonding methods. Figure 8-1 shows the assembled components on board. The output capacitor, compensation capacitor, gate drive PCB (Printed Circuit Board) transformer and inductors are attached to substrate using high temperature conductive epoxy. The Silicon-on-Sapphire (SOS) control IC is attached to the substrate and wire bonded to bring connections out from IC pads to substrate traces. The silicon carbide power devices are eutectically attached to base pads and wire bonded to top side terminals. Connecting leads are twisted through the 'via' holes in the substrate.

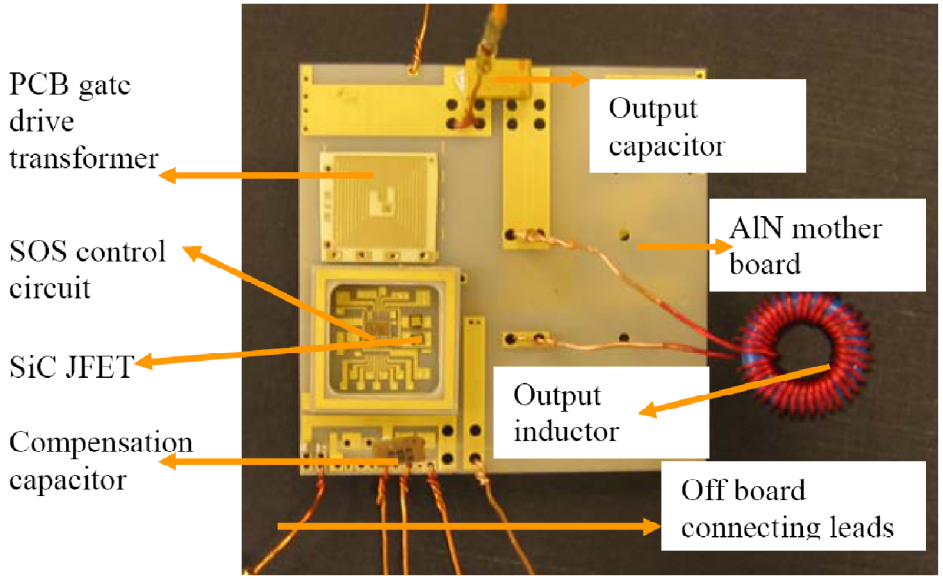


Figure 8-1. 1.8" × 1.8"Assembled 275°C SMPS circuit board with testing connections

8.1.2 Test setup

Figure 8-2 shows the test setup and the list of equipment used for the purpose. The assembled circuit board is mounted on a hot plate for elevated temperature testing. Power supply 1 (0.8 V and 0.9 V) is used for biasing the voltage control oscillators. Power supply 2 is used for powering the control IC (3.3 V) and provide high voltage raw input supply (>10 V). The oscilloscope is used to observe the output waveform during startup, standby and loading conditions. A signal generator is used for applying step inputs above and below the dc reference level to characterize loop stability.

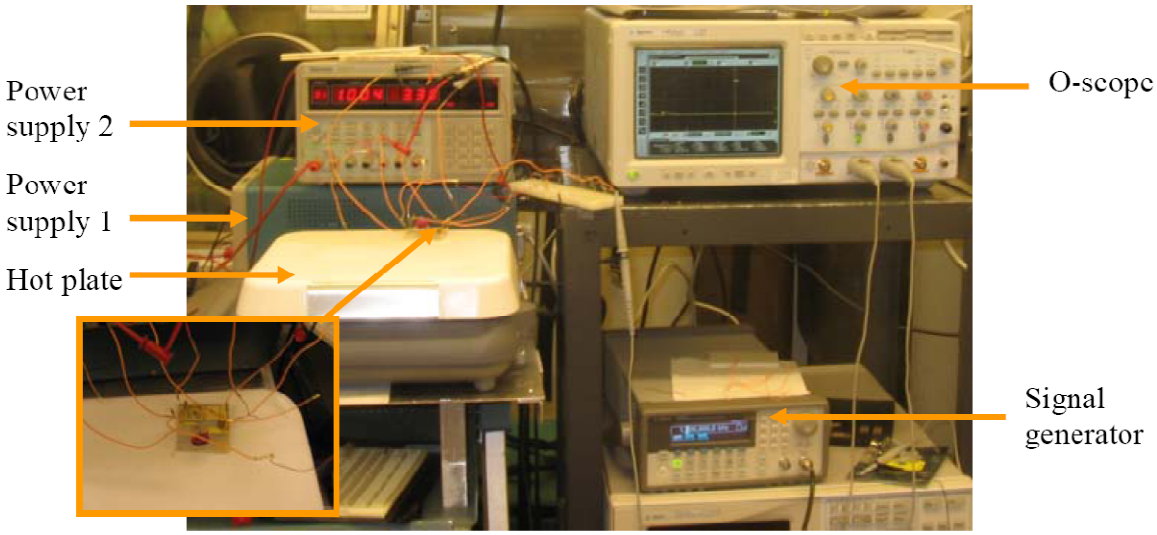


Figure 8-2. Test setup for SMPS verification. Insert shows the circuit board on hot plate.

8.1.3 Test results

8.1.3.1 3.3V converter

3.3V output operation is set by either an internal or external resistor divider. The transient startup and steady state characteristic of the prototype at room temperature under no load conditions and for a 47 ohm load are disclosed in Figure 8-3 and Figure 8-4 respectively.

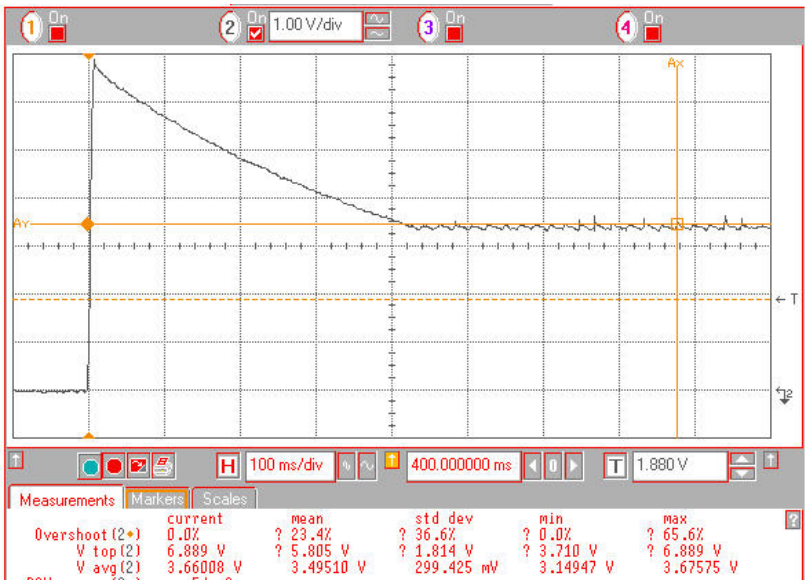


Figure 8-3. Transient output voltage plot of the 3.3V converter showing a 3 V overshoot at start up and the steady-state value under no load conditions.

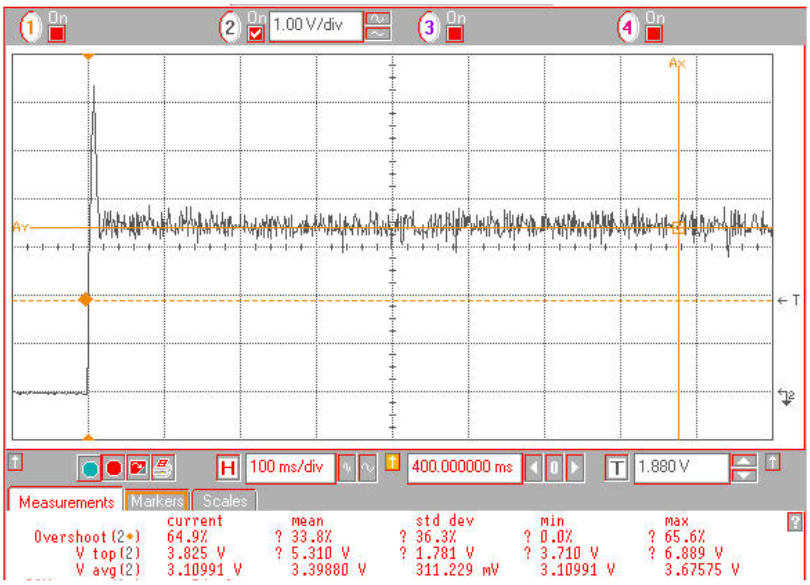


Figure 8-4. Transient output voltage plot of the 3.3V converter showing the overshoot and state-state value with 47 ohms resistive load.

The startup and steady state output observed under no load at 275°C is shown in Figure 8-5. When compared to the no load room temperature measurement result of Figure 8-3 and Figure 8-4, the plot has no overshoot and reduced output voltage ripple. Voltage ripple at normal temperature is somewhat excessive at 400mV due to inadequate on board decoupling. The AlN board was fabricated with less than adequate space for decoupling capacitors. The better response at 275°C is due to reduced intrinsic switching speed of the transistors at elevated temperature that eases the decoupling requirement. As

a result the decoupling provided is much effective at elevated temperature than at room temperature.

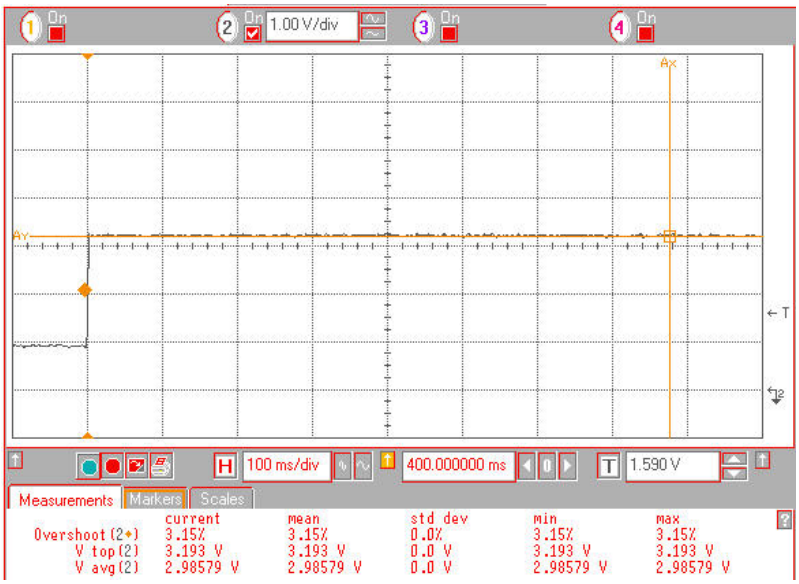


Figure 8-5. Transient output voltage plot of the 3.3 V converter.

The startup and steady state characteristic of the converter for 47 ohms and 8.2 ohms real loads are shown in Figure 8-6 and Figure 8-7, respectively. The absence of overshoot and ripple is readily observed at elevated temperatures. This is a direct result of the reduced switching speed of both the CMOS and SiC devices by roughly a factor of 3 as temperature goes from room temperature to at 275°C. A tripling of the decoupling capacitors should serve solve future ripple problems.

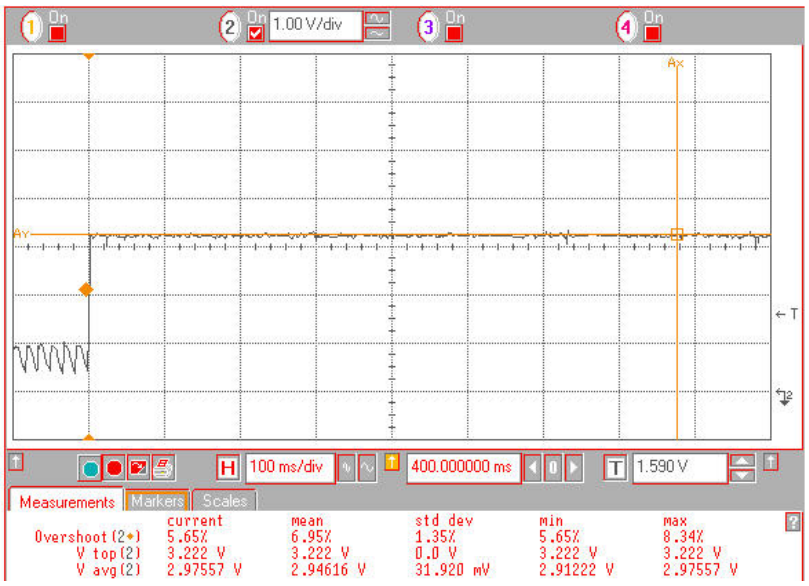


Figure 8-6. Startup characteristic of the 3V converter with 47 ohm resistive load - 275°C.

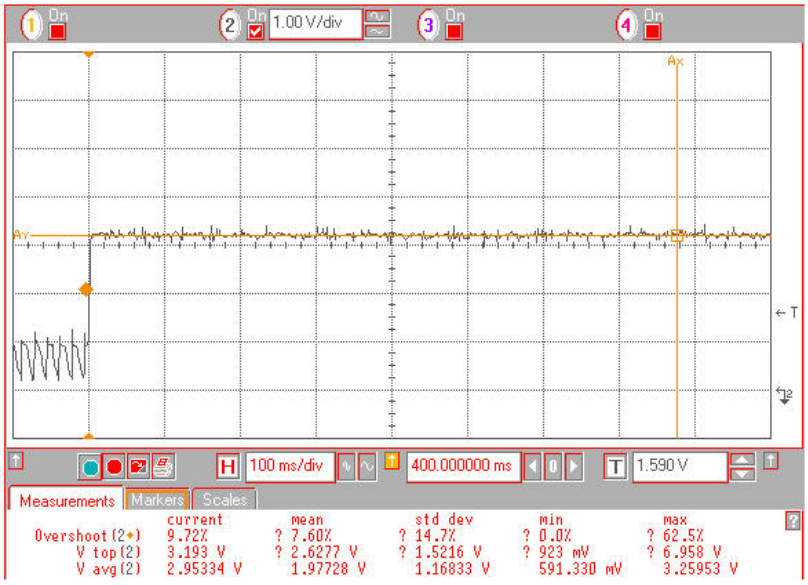
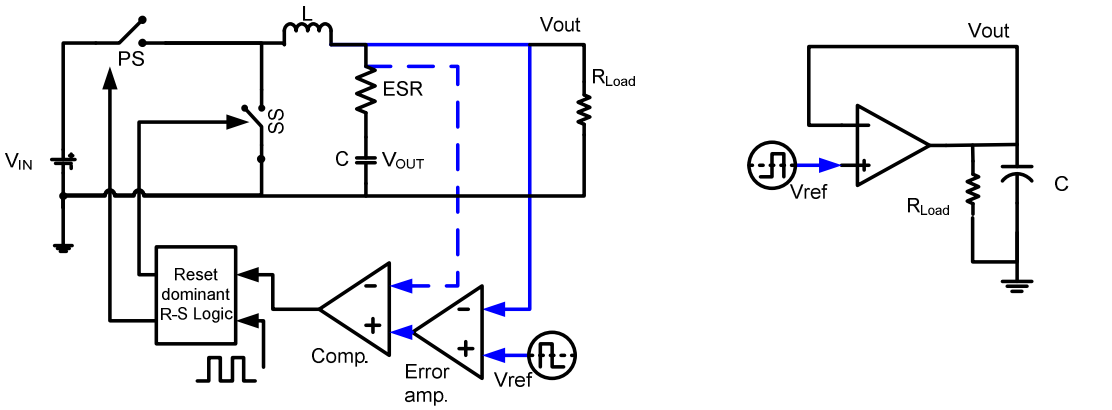


Figure 8-7. Startup characteristic of the 3V converter with 8.2 ohm resistive load - 275°C.

8.1.4 Control loop stability

The stability of the control loop can be measured indirectly by application of a step function at the reference input. From network system theory and superposition it can be shown that the application of a step change in load or a voltage step change at the reference input are equivalent. Applying a voltage at the input is both simpler and does not require power devices. By observing control loop response to a step change in input

loop stability is evaluated. A signal source is used to apply a +/-50mV step amplitude centered at 400mV to reference voltage input. This is the input to the error amplifier. This corresponds to a +/- 12.5% change in load at the output. An excellent or nearly ideal response is observed at the output as shown in Figure 8-8. This demonstrates that the control loop phase margin is greater than 75 degrees. Figure 8-8 is for no load conditions. Note that the rise time is the loop's response to an increase in load demands and responds without overshoot while the fall time is limited by the no load RC time constant.



(a)

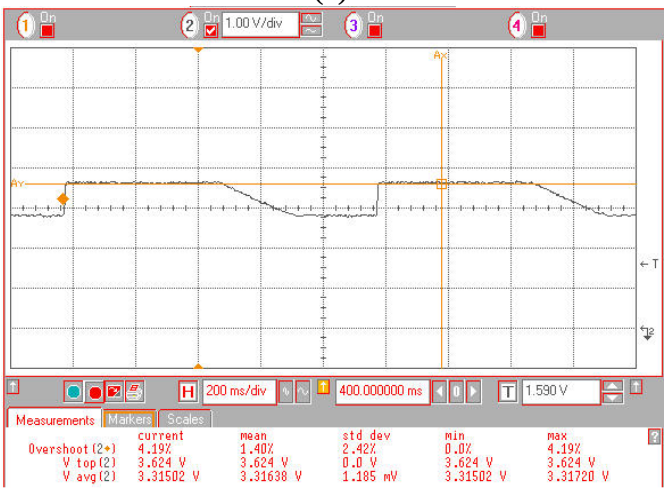


Figure 8-8. Simplified control loop with equivalent circuit (a) and output transient response to a 12.5% output referred change by pulsing the 400mV voltage reference with a 350 to 450 mV pulse train.

8.1.4.1 The 5V module

Similar to the 3.3 V module, a 5V module was also developed and tested. The output voltage in this case is set by the pre-designed internal resistor dividers. Due an undetermined error in the resistance divider value, the obtained output level is lower than the desired level. Externally added resistors demonstrated proper SMPS operation as noted above. The start up and steady state response of the converter under no load and with 47 ohm load is shown in Figure 8-9 and Figure 8-10 respectively. Again at room temperature an overshoot is observed at start up. In the 5V case slightly greater than 2 volts.

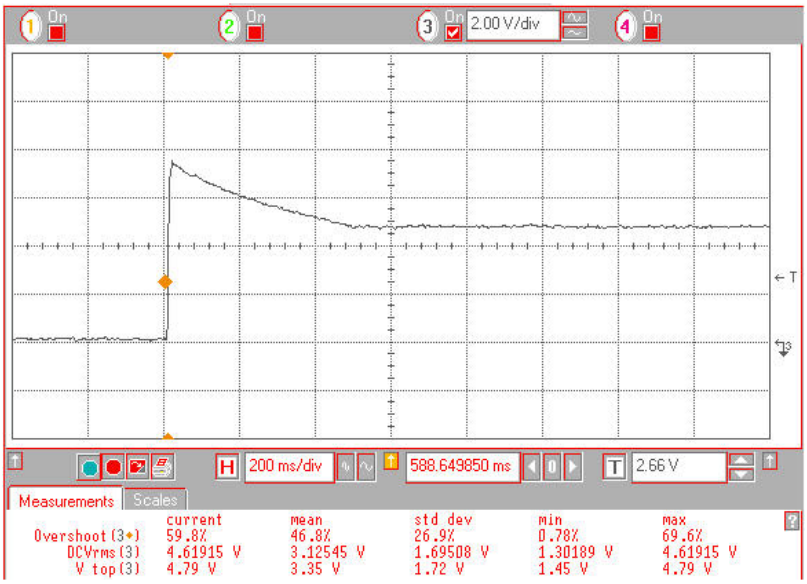


Figure 8-9. Transient output voltage plot of the 5 V converter showing a 2 V overshoot at start up and the steady-state value under no load conditions.

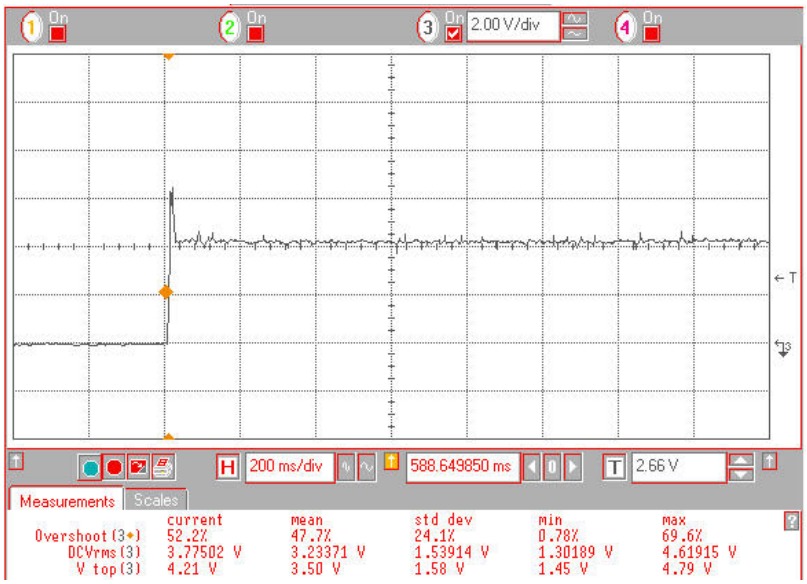


Figure 8-10. Transient output voltage plot of the 5 V converter showing a 2 V overshoot at start up and the steady-state value under a load of 47 ohms.

The control loop stability is tested for and observed using the same technique described above for the 3.3 V converter. A response somewhat less than a critically damped loop response is shown in Figure 8-11. Note that for the test of Figure 8-11 is under no load conditions and again from the rise response we observe that the loop is stable and phase margin is greater than 75 degrees. The fall response is dictated by the no load RC time constant.

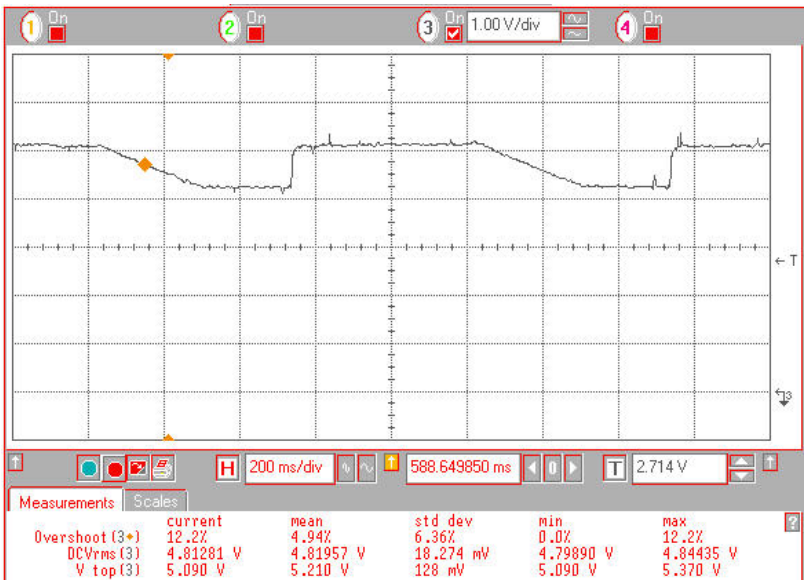


Figure 8-11. Control loop behavior for step +/- 100 mV step change applied at the reference input of the 5V SMPS module under no load conditions.

8.2 V2 controller: generation 2.0

Based on testing results and observations from the preliminary control die, few changes to the first version of the controller are applied. The performed improvements are as follows. The improvements in the performance in discussed in following sections.

8.2.1 Decoupling

Due to high frequency switching of gate buffers and overdesigned (low impedance) rectifier, the circulating currents in the chip largely affected the performance. Particularly at lower temperatures, the high ‘di/dt’ of transistors resulted in excessive noise in the power supply. Also the output of the high frequency oscillator was padded out through a pad driver for monitoring purpose. Ultimately these factors resulted in higher output noise and poor voltage regulation of the SMPS.

In the revised design, additional decoupling capacitors are provided to address to the need of high frequency currents due to gate drive buffer. The rectifier circuit design has been scaled down for optimum on resistance for 50 nS delay and reduced power. Also the gate

drive buffers are scaled down but provided with more decoupling. The on chip decoupling provided is estimated to be more than 1 nF.

8.2.2 Low side duty clamp

The duty clamp circuit which prevents 100% duty cycle operation is applied to both high side and low side switches in the initial design. However, a low side switch does not require a duty clamp circuit and hence has been removed in the second trial.

8.2.3 Global bias generator

The bias circuits used for individual comparators, amplifiers and voltage reference is grouped into a single master bias generator to make the design more robust and also save area. The schematic of the global bias generator is shown in Figure 8-12.

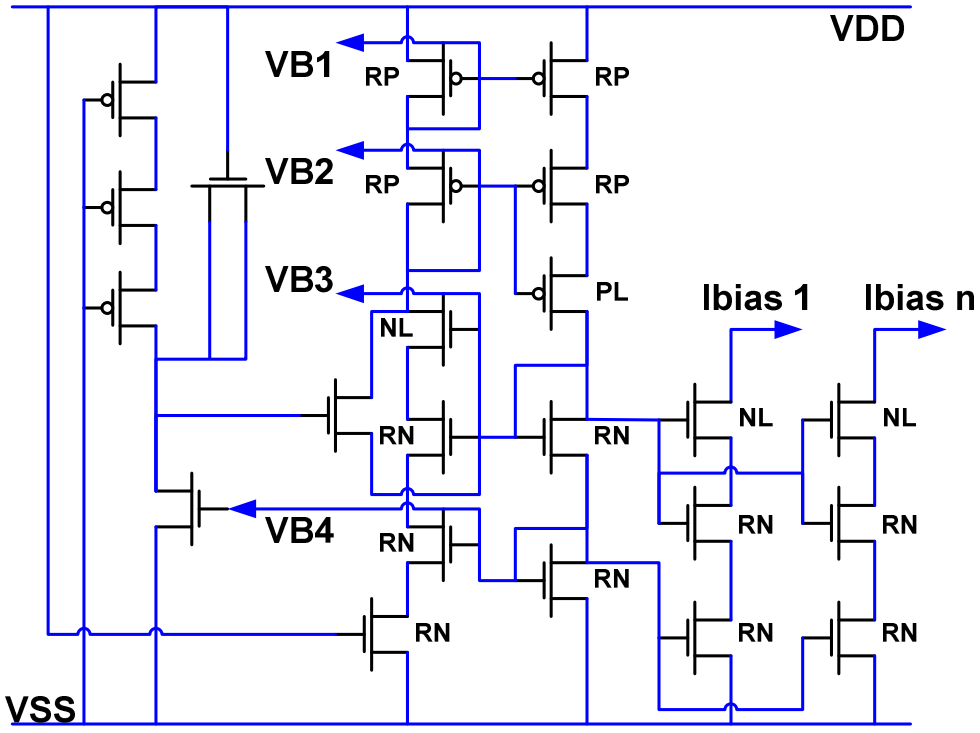


Figure 8-12. Schematic of master bias with startup circuit.

8.2.4 Modified layout

By eliminating the low side gate drive, combining bias generators and reducing buffer and rectifier sizes, the area has been reduced from 3mm X 2mm to 2 square mm. The second generator controller is laid out and fabricated. Figure 8-13 shows the layout snapshot and the corresponding pad out details. The fabricated dice is shown in Figure 8-14

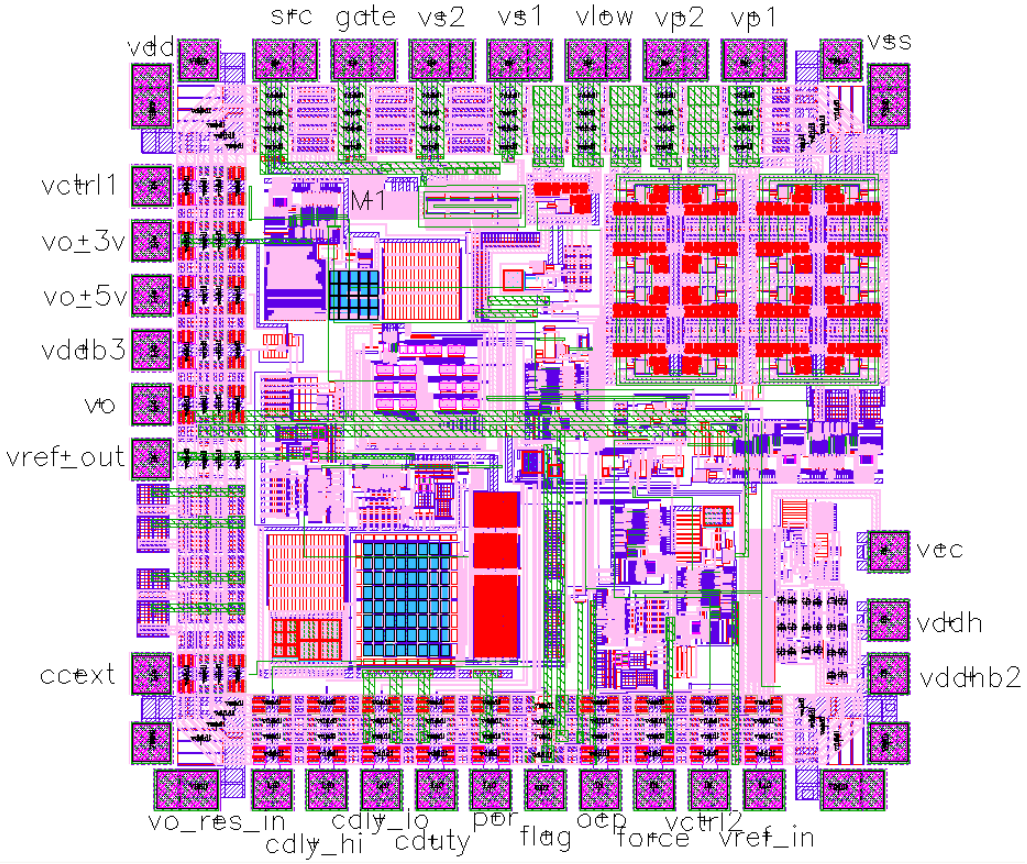


Figure 8-13. Layout snapshot of the second generation V2 control chip.

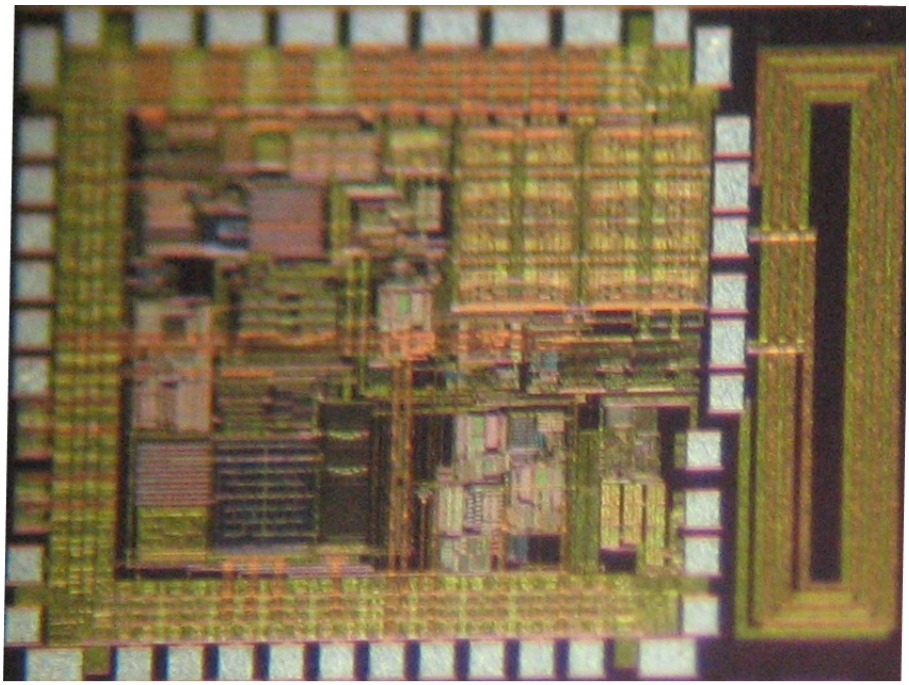


Figure 8-14. Fabrication dice of the controller chip - Generation 2.0

8.2.5 Bard layout

A modified mother board with provisions for more decoupling capacitors, power planes and ground planes is implemented. The revised board of dimension 1.8 sq. inches is fabricated on the FR4 - PCB technology. In the four layer board, the top and bottom layers are used for power and ground planes. Board level interconnects are implemented using layer 2 and 3. Figure 8-16 shows the top layer layout of the motherboard. The board is designed to be versatile, to adopt commercial MOSFETs or JFETs. Unlike the AlN motherboard the updated board integrated the gate drive transformer during fabrication and hence is much efficient in assembly.

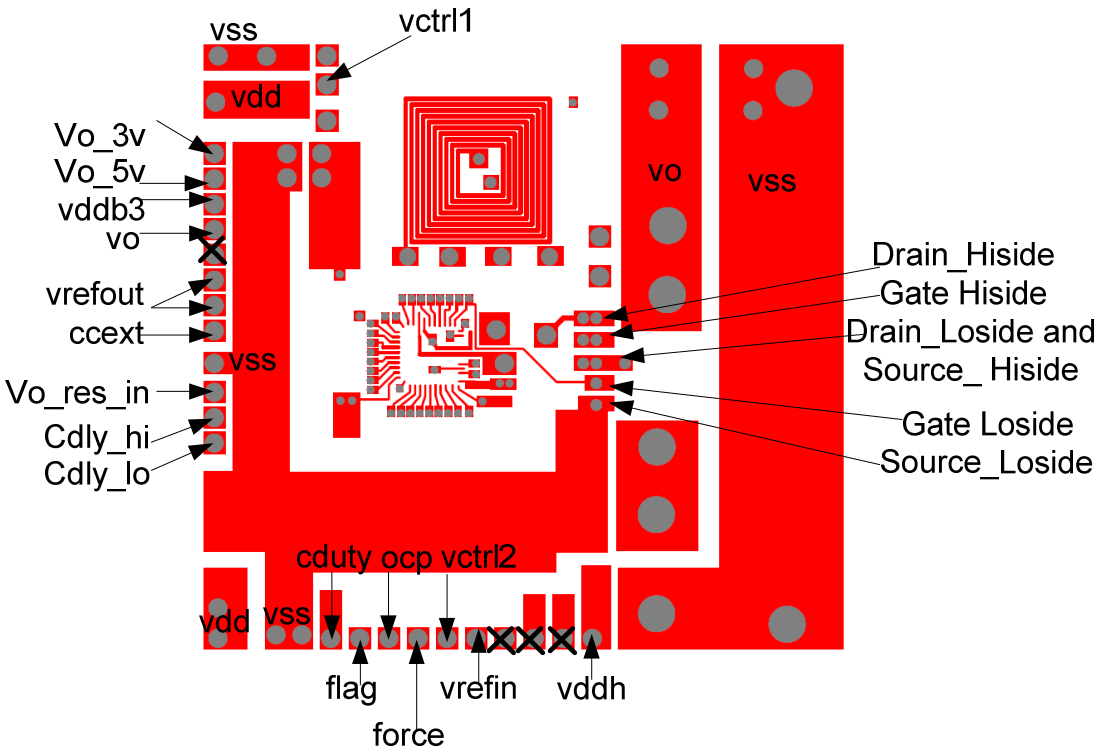

vss
vctrl1
vdd
Vo_3v
Vo_5v
vddb3
vo
vrefout
ccext
vss
Vo_res_in
Cdly_hi
Cdly_lo
vo
vss
Drain_Hiside
Gate Hiside
Drain_Loside and
Source_ Hiside
Gate Loside
Source_Loside
cduty ocp vctrl2
vdd
vss
flag
force
vrefin
vddh

Figure 8-15.

Gen 2. Test Results

The second generation V2 control IC is fabricated and mounted on the PCB motherboard for testing. Figure 8-16 shows the assembled board ready and compatible for commercial distribution. Commercial MOSFETs are used as switches in the board. Added decoupling capacitors and the easily accessible board terminal through header pins are the major advantages of the updated board.

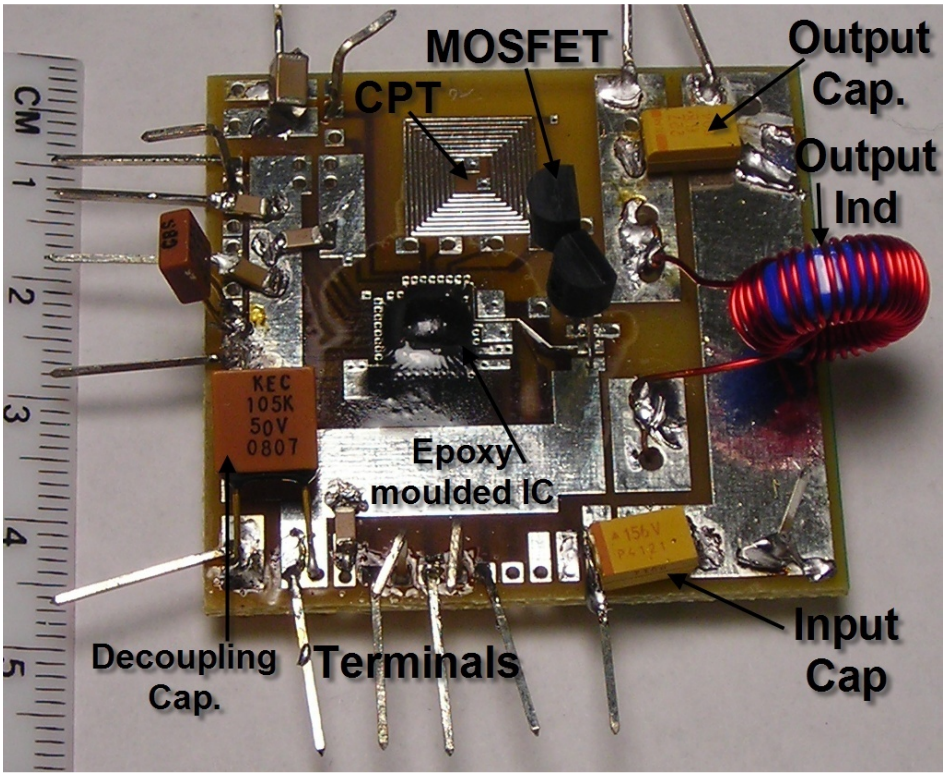


Figure 8-16. A complete SMPS prototyped on a FR4 based 4-layer board.

The start up, steady state and transient response of the SMPS based on the second generation V2 controller were experimentally verified. Figure 8-17 shows the startup characteristics of a 3.3V prototype and its steady state voltage. Unlike the earlier version a linear start up characteristic and a very low noise DC steady state output voltage can be observed from the figure. The peak-peak ripple voltage is lesser than 50mV. This illustrates the proper working of startup circuit and the slow feedback path of the controller that sets the dc output voltage.

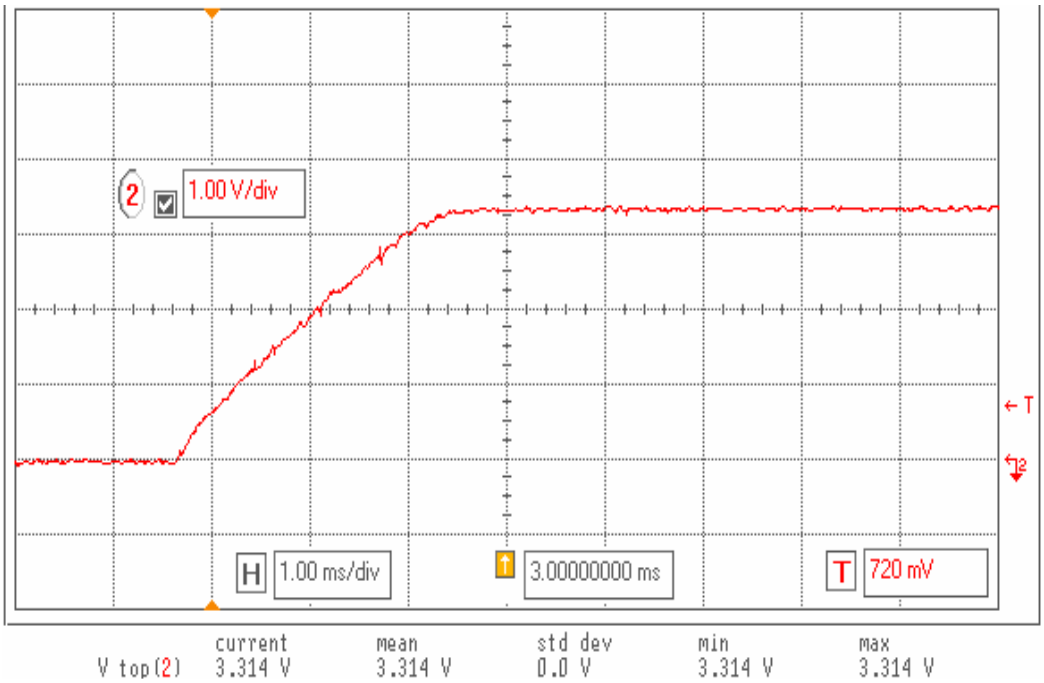


Figure 8-17. Startup and steady state characteristic of gen. 2 controller SMPS.

The transient response of the prototype is observed by switching an 8 ohm load using a MOSFET. The MOSFET gate control voltage and its transient effect on the output voltage are shown in Figure 8-18.

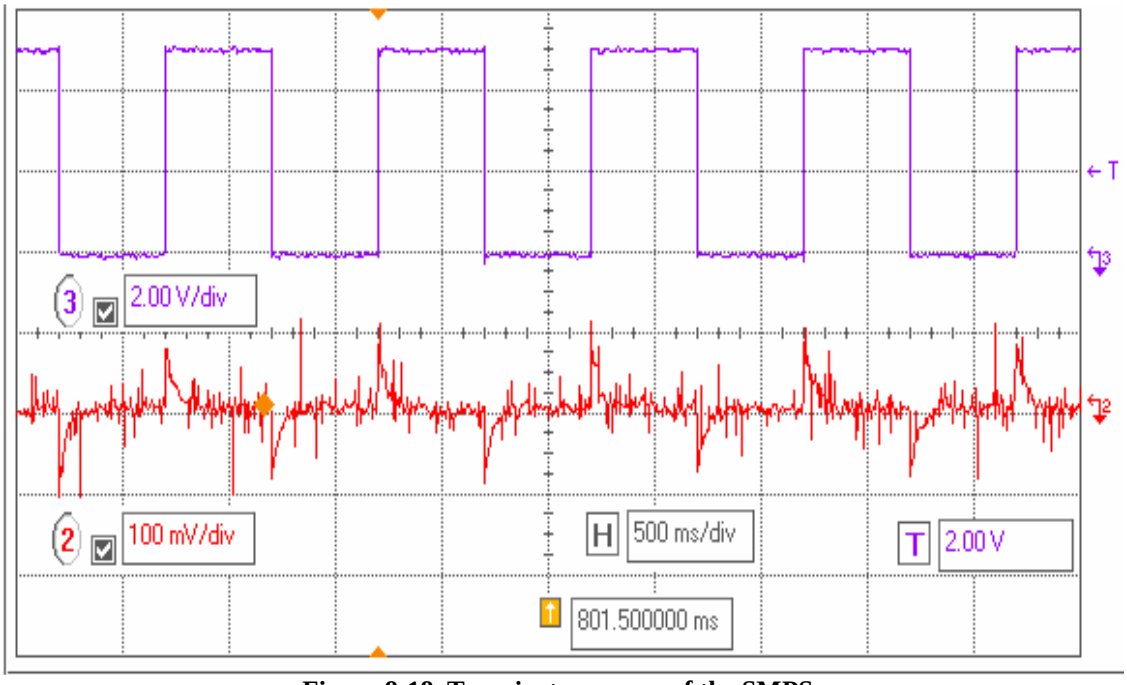


Figure 8-18. Transient response of the SMPS.
Top trace - Load current step, Bottom trace - Ac coupled output voltage.

Chapter 9

9.1 Conclusion

For the first time, a switch mode power supply capable of operating at 275 degree centigrade as a standalone component is demonstrated. The performance of the V2 controller implemented in SOS substrate is verified with the silicon carbide power switches and passive high temperature components, L and C's. Prototype converters for 3.3 V and 5 V output were developed and their performances measured under startup and loaded conditions are disclosed at room temperature and at 275°C. The prototypes are built on custom 1.8 sq. inch aluminum nitride substrates with thin film gold metallization. Excellent performance is obtained at higher temperatures. A summary of performance is provided in Table 9-1. External control of the duty cycle limit and non overlapping periods are provided to the user. Several other user programmable and debugging options such as over current protection, high temperature indicator, controller status indicator etc. are provided. With minor improvements to the preliminary design the results from the generation 2.0 controller are also presented. A demonstration of more commercially viable module is presented using the generation 2 circuitry and FR4 mother board. The complete converter can be made commercially available for an estimated cost as given in Table 9-2.

Table 9-1. Performance summary of V2 controller.

Specification	Expected	Obtained	Remarks
Operating temperature	≤ 275°C	> 275°C	High temperature limited by available capacitors
Input voltage range	15 to 25V	> 18 V	Higher limit is dependent on the JFET (In this case < 600V)
Output voltage range	1.5 to 18V	3.3, 5V, 6.6, and 10V	Limited by internal resistor divider net work and voltage reference. Extendable to any voltage from 1.5 to 18 V by the use of a external resistor divider network.
Output Watts	> 2 W	>1 W	Limited by layout and heat removal from the SiC JFETs and limited high side gated drive. Failure to adequately remove heat from JFET will result in SMPS V2 shut down at 300 °C.
Regulation	2%	<5%	- at elevated temperature. Generally limited by value of output capacitor and layout area.
Efficiency	80-90%	.>80%	Dependent on load current. ~ 81% at 3.3V, 300mA output, 275°C
Stability (phase margin)	>75°	>75°	Indirectly measured validating simulations carried out in Cadence and Matlab. Additionally stability was observed by power switching with 8Ω load (1.4 Watts)

Table 9-2. Cost estimation for commercial 275°C SMPS

Component	Estimated Cost (USD)	Vendor
SOS control IC	200	Peregrine semiconductors
AlN package	300	Stellar Industries
Capacitor	100	Kemet Inc.
Bonding accessories	100	Cotronics Corp.
Gate drive transformer	10	4PCB / Kingcircuits
Inductor	5	MWS wire Arnold Magnetics
Sub total	715	
SiC devices	300	Semisouth Laboratories
Overhead	200	OSU
Total	1215	

The estimated cost is based on the prototype fabrication cost and NOT on the commercial scale production cost. Even at this cost the system is competitive to the supplies offered by the commercial vendors. Nevertheless the versatility and 275°C operation is the unique features of the developed system.

9.2 V2 controller data sheet

The pin characteristics and performance specifications of the V2 controller is summarized in the following tables.

Table 9-3. Datasheet for V2 controller.

Available pins	Functionality	Min	Typ	Max
vdd	power supply	3	3.3	3.6
vss	ground	0	0	0
vlow	low side switch driver	3.3V, 8 ohms, 50 ns @100 pF		
vhigh1	drive signal for transformer	3.3V, 1.5 ohms, 5 ns @ 100pF		
vhigh2	complementary drive signal for transformer	3.3V, 1.5 ohms, 5 ns @ 100pF		
vs1	transformer secondary input to rectifier	-	-	-
vs2	complementary transformer secondary input to rectifier	-	-	-
vgate	rectified positive voltage for high side switch gate	2 V	2.6V	-
vsource	rectified reference voltage for high side switch source	-	-	-
vo	output voltage feedback for control	-	-	5 V
vref2	buffered voltage reference output (400 mV)	370 mV	400 mV	420 mV
vref1	buffered voltage reference output (800 mV)	770 mV	800 mV	820 mV
vrefin	reference voltage for the controller	-	400 mV	-
vo_res_in	down scaled output voltage wrt vref for comparator	400 mV @ desired vo		
ccext	external compensation capacitor terminal	10 nF	15 nF	25 nF
vctrl1	control voltage for system oscillator	0.75	0.8 V	1 V
vctrl2	control voltage for gate drive oscillator	0.8 V	1 V	1.1 V
ocp	external terminal for over current protection	tie low		
flag	indicates the status of controller	high		
force	force the controller to operation (high - force)	tie low		

Table 9-4. Pin configuration of generation 2 controller

Pin No.	Name	Functionality	Min	Typ	Max
1	vdd*	power supply	3	3.3	3.6
2	vss	ground	0	0	0
3	vo	output voltage feedback for control	-	-	5 V
4	vctrl1	control voltage for system oscillator	0.8	1.1 V	1.6 V
5	vctrl2	control voltage for gate drive oscillator	0.8 v	1.1 v	1.6 v
			10 MHz at 1.1V @ RT		
6	vref_out*	buffered voltage reference output (400 mV)	370 mV	400 mV	420 mV
7	vref_in	reference voltage for the controller	-	400mV	-
8	vo_res_in	down scaled output voltage wrt. vref for comparator	400 mV @ desired vo		
9	flag	indicates the status of controller	High- normal		
10	force	Force the controller to operation	High - force		
11	ocp	external terminal for over current protection	tie low		
12	vddb3	vdd divided by 3	1.1V control voltage		
13	cduty	duty cycle limit capacitor	> 50pF		
14	cdly_hi	sets turn on delay for high side switch	Default to 50ns non overlap		
15	cdly_lo	sets turn on delay for low side switch			
16	vo_3v	internal resistor divider output for 3.3V	0.4V		
17	vo_5v	internal resistor divider output for 5V	0.4V		

9.3 Future work

Commercialization is the next major task of this research work. The SMPS and the vee-square controller are ready as it is for the end user market. The controller chip can also be packaged in commercial IC packages or ceramic packages for use in common power supply applications. The system efficiency and performance can be improved by optimizing the circuits for lower power.

Chapter 10 References

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Chapter 11 Appendices

11.1 Verilog A model of SiC JFET

The following Verilog code is used as the model deck for silicon carbide JFET for use in simulations

```
`include "constants.vams"
`include "disciplines.vams"

module Tail (D, G, S);
inout D, G, S;
electrical D, G, S;
        parameter real area=1 from (0:inf);
        parameter real vto1= 2.1;                   // Threshold voltage
        parameter real beta=2.0 from (0:inf);       // A/V^2
        parameter real lambda=0.001;                //Channel length modulation
        parameter real is=1e-12 from [0:inf);       //reverse diode leakage current
        parameter real gmin=1p from (0:inf);
        parameter real cjs=1e-10 from [0:inf);
        parameter real cgd=1e-10 from [0:inf);      //Gate-Drain capacitance
        parameter real m=0.5 from (0:1);
        parameter real phi=1 from (0:inf);
        parameter real fc=0.5 from (0:1);
parameter real temp=25;
parameter real vttempco=-0.00174;
```

```
real vto, Vgs, Vgd, Vds;
        real Id, Igs, Igd;
real Qgs, Qgd;
        real f1, f2, f3, fcp;
        analog begin
vto=vto1-((25-temp)*(vttempco));
        @ (initial_step or initial_step("static")) begin
f1 = (phi/(1 - m))*(1 - pow((1 - fc), m));
        f2 = pow((1 - fc), (1 + m));
                f3 = 1 - fc*(1 + m);
                fcp = fc*phi;
        end
                Vgs = V(G, S);          Vgd = V(G, D);          Vds = V(D, S);

                if (Vds >= 0) begin
// forward active.
                        if (Vgs - vto <= 0) begin
                                Id = 0;
                        end else if (Vgs - vto <= Vds) begin
                                Id = beta*(1 + lambda*Vds)*pow((Vgs - vto), 2);
                        end else begin
                                Id = beta*Vds*(1 + lambda*Vds)*(2*(Vgs - vto) - Vds);
                        end
                end else begin
// reverse active.
                        if (Vgd - vto <= 0) begin
                                Id = 0;
                        end else if (Vgd - vto <= -Vds) begin
                                Id = -beta*(1 - lambda*Vds)*pow((Vgd - vto), 2);
                        end else begin
                                Id = beta*Vds*(1 - lambda*Vds)*(2*(Vgd - vto) + Vds);
                        end
```

```
                end


// parasitic diodes.
if (Vgs < 1) begin
        Igs = is*(exp(Vgs/(3*$vt)) - 1) + Vgs*gmin; end
else    begin Igs = is*(exp(Vgs/(5*$vt)) - 1) + Vgs*gmin;
end
                 Igd = is*(exp(Vgd/(5*$vt)) - 1) + Vgd*gmin;
// charge storage.
                if (Vgs < fcp) begin
                        Qgs = area*2*phi*cjs*(1 - sqrt(1 - Vgs/phi));
                end else begin
                        Qgs = area*cjs*(f1 + (1/f2)*(f3*(Vgs - fcp) + (Vgs*Vgs -
fcp*fcp)/(4*phi)));
                end
                if (Vgd < fcp) begin
                        Qgd = area*2*phi*cgd*(1 - sqrt(1 - Vgd/phi));
                end else begin
                        Qgd = area*cgd*(f1 + (1/f2)*(f3*(Vgd - fcp) + (Vgd*Vgd -
fcp*fcp)/(4*phi)));
                end
                I(D, S) <+ Id;
                I(G, S) <+ Igs + ddt( Qgs );
                I(G, D) <+ Igd + ddt( Qgd );
        end

endmodule
```

11.2 Matlab program for Kharitonov analysis

The following code is used to analyze the robust stability of the controller using Kharitonov analysis. Based on experimental results, only the interval values of output capacitance and its equivalent series resistance are considered to be dominating factor over temperature and hence are included in the analysis. However it is possible to extend the program to include other parameter variations at the expense of processing time. The programs includes Routh stability analysis of the Kharitonov polynomials and displays either 'good' or 'bad' based on the results.

```
% code begins
clear all;  format long; clc
close all;

c = logspace(-5,-3,100);      rc = [0.05:0.01:0.1];
l = 1e-4;       rl = 2;
r = 10;        ron = 2;
vg = 10;        ae = 1000;      ac = 1000;
ro = 1e5;       gm = 30e-6;     cc = 19e-9;

wz  = gm/cc;    wp = 1/(ro*cc);

len1=size(c); len2=size(rc);

for i = 1:len1(2)
   for j = 1:len2(2)
   cs3(i,j) = l*c(i)*(r+rc(j));
   cs2(i,j) = l*(c(i)*wp*(r+rc(j))+1)+c(i)*(r*(rl+rc(j)+ron)+rc(j)*(rl+ron));
   cs1(i,j) = (rl+rc(j)+ron)*(1+wp*c(i)*r)+wp*c(i)*rc(j)*(rl+ron)+l;
   cs0(i,j) = wp*(rl+rc(j)+ron);
   end
end

p1 = [min(min(cs3)) min(min(cs2)) max(max(cs1)) max(max(cs0))];
p2 = [min(min(cs3)) max(max(cs2)) max(max(cs1)) min(min(cs0))];
p3 = [max(max(cs3)) min(min(cs2)) min(min(cs1)) max(max(cs0))];
p4 = [max(max(cs3)) max(max(cs2)) min(min(cs1)) min(min(cs0))];

poly = [p1; p2; p3 ;p4];
% % % % % % Routh stability analysis begins % % % % % %
for z=1:4
   m=4; n=round(m/2); q=1; k=0;
for p = 1:length(poly(z,:))
   if rem(p,2)==0
      c_even(k)=poly(z,p);
   else
      c_odd(q)=poly(z,p);
```

```
        k=k+1;
        q=q+1;
    end
end
a=zeros(m,n);

if m/2 ~= round(m/2)
    c_even(n)=0;
end
a(1,:)=c_odd;
a(2,:)=c_even;
if a(2,1)==0
    a(2,1)=0.01;
end
for i=3:m
    for j=1:n-1
        x=a(i-1,1);
        if x==0
            x=0.01;
        end

        a(i,j)=((a(i-1,1)*a(i-2,j+1))-(a(i-2,1)*a(i-1,j+1)))/x;

    end
    if a(i,:)==0
        order=(m-i+1);
        c=0;
        d=1;
        for j=1:n-1
            a(i,j)=(order-c)*(a(i-1,d));
            d=d+1;
            c=c+2;
        end
    end
    if a(i,1)==0
        a(i,1)=0.01;
    end
end
Right_poles=0;
for i=1:m-1
    if sign(a(i,1))*sign(a(i+1,1))==-1
        Right_poles =Right_poles+1;
    end
end
Rt_poles(z)=Right_poles;
% fprintf('\n Routh-Hurwitz Table:\n')
% a
end
if (Rt_poles == 0)
    display('good')
else
    display('bad')
end
```

11.3 High temperature characteristics of copper clad laminates

The gate drive transformer is implemented on the copper laminates. The performance of commercially available 1 ounce copper laminates with RO4350B and RT6202 dielectric materials are evaluated at elevated temperatures. The test coupons used for testing is shown in Figure 11-1. The harsh effects of elevated temperature can be readily seen from the oxidation and carbon deposit on the conductor surface. The performance of the test material is evaluated by measuring the capacitance and dissipation factor of the materials. The measured results at various input frequencies are shown in Figure 11-2.

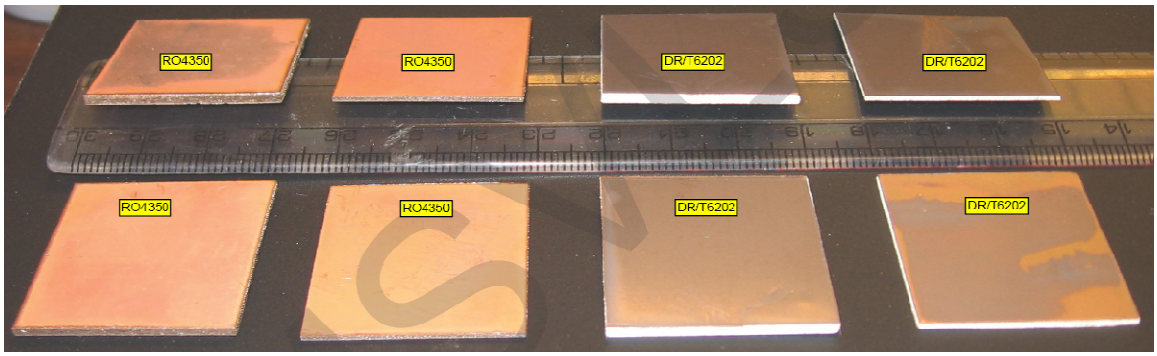

Figure 11-1. Test coupons for high temperature testing of copper laminates.

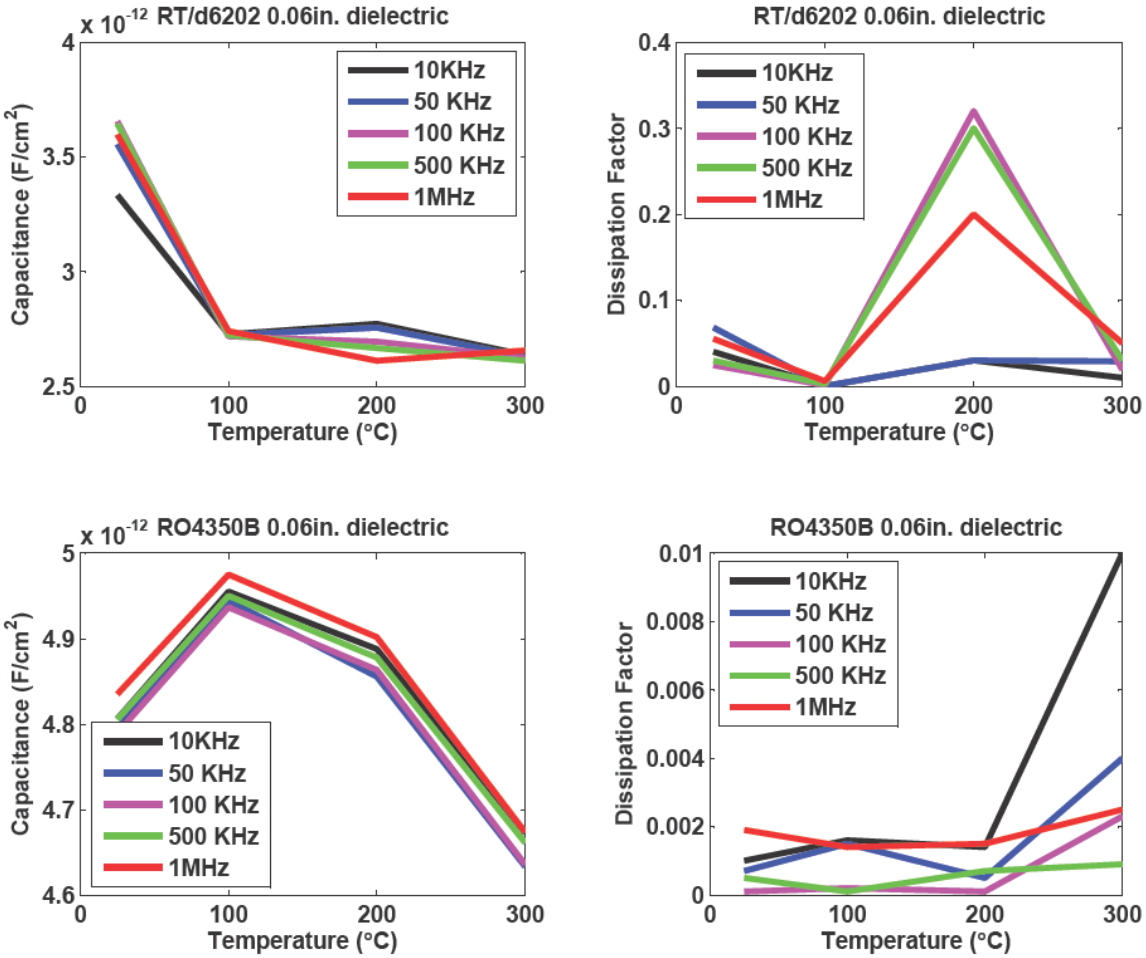

Figure 11-2. Capacitance and Dissipation factor of test coupons for various frequencies at different temperatures.

From Figure 11-2 it can be observed that the dissipation factor for the RO4350B material is significantly lower compared to RT6202 dielectric and is preferred for substrate.

11.4 Validation of high capacitance capacitors

In addition to the conductive polymer and tantalum capacitor, X5R dielectric based capacitors are also evaluated. Unlike the previously disclosed characteristics, negative temperature coefficient characteristics of the X5R capacitors can be observed from the plot. The decrease in capacitance at elevated temperature is an undesirable characteristic, however compared to polymer capacitors the dissipation factor of X5R capacitors are significantly less which yields lower ESR. The lower ESR is preferred to minimize the output ripple and the power loss.

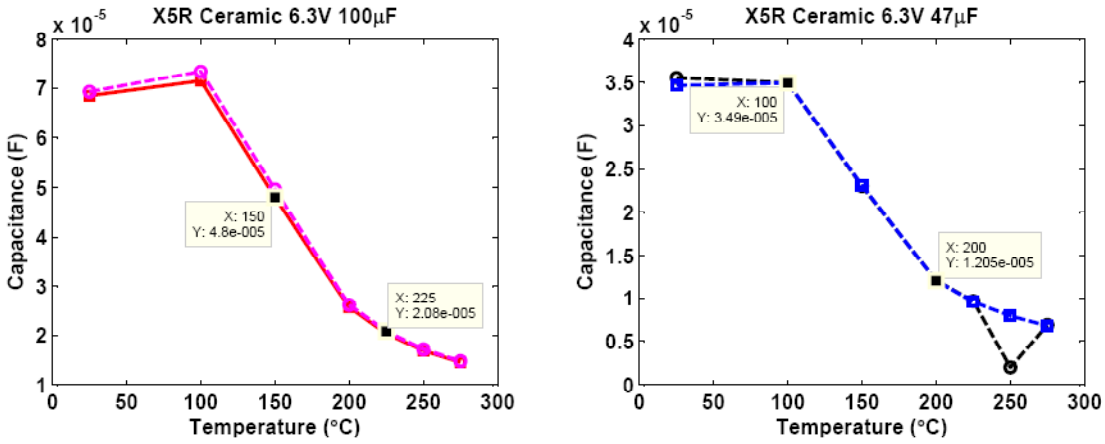

Figure 11-3. Change in capacitance of X5R capacitors with temperature

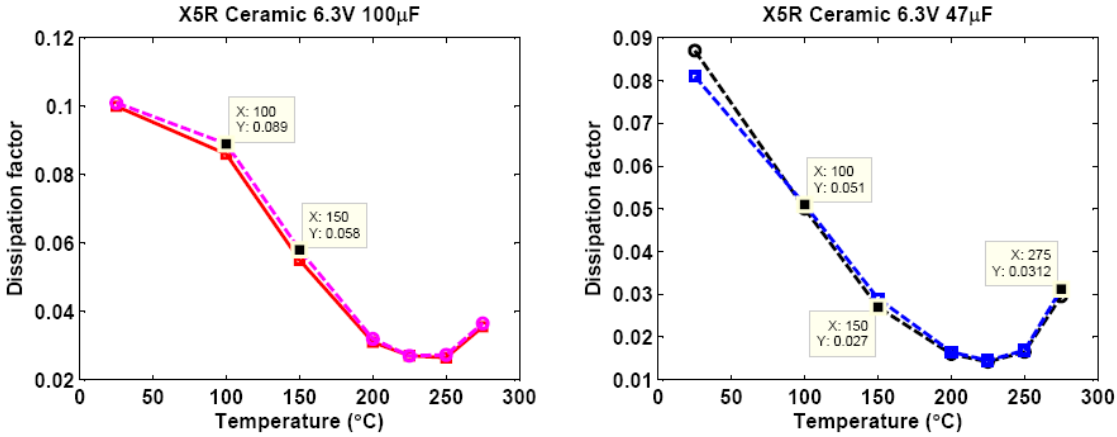

Figure 11-4. X5R capacitors: Dissipation factor versus temperature

11.5 Validation of PCB transformer gate drive

To verify the functionality and performance of various transformer structures, different layouts are fabricated on a four layer FR4 printed circuit board. The transmission and reflection characteristics are obtained by s-parameter measurements (S11, S21) using vector network analyzer (VNA).

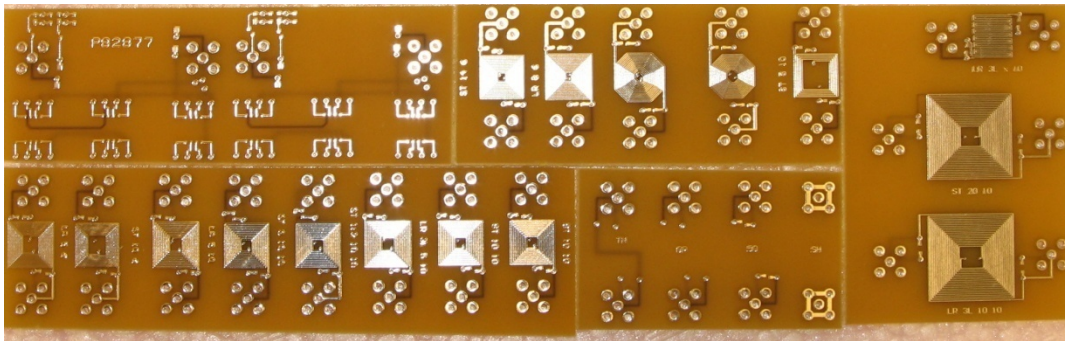

Figure 11-5. Photograph of fabricated PCB transformers

To verify the functionality of the gate drive transformer a custom test coupon is developed as shown in Figure 11-6 (left). The design is based on board implementation of a switching buffer and a full wave rectifier. This is required to minimize the effect of leakage inductance of the connecting wires. The selection of drive is either differential or single ended. A differential driver is used as a buffer to isolate the input signal source and to provide a differential drive for the transformer. The synchronous drivers are used to individually drive the transformer as a single ended input or as synchronized differential input. The fabricated transformer is diced and solder in the board as shown in Figure 11-6(right). A discrete full wave rectifier chip is used to generate the dc voltage from the switching (ac) input. The rectified output voltage is shown in Figure 11-7. The input to buffer is 3.3V amplitude at 10MHz frequency. The result obtained is consistent with the expected voltage gain for the transformer structure.

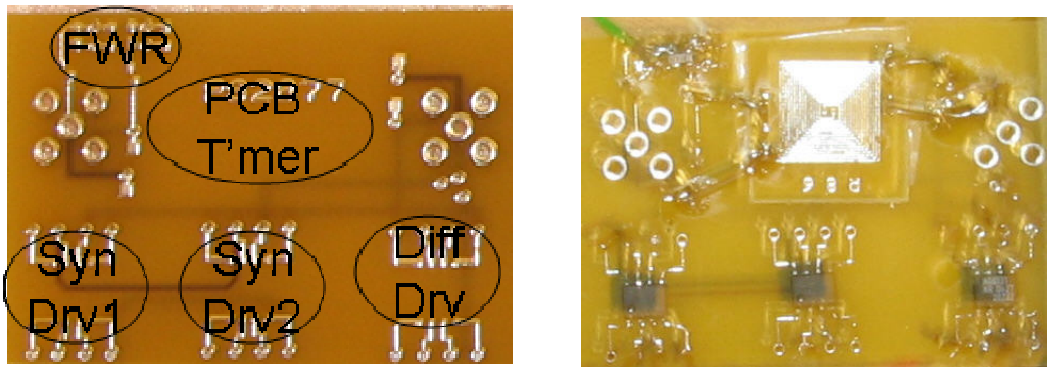

Figure 11-6. Custom test fixture for testing PCB transformers

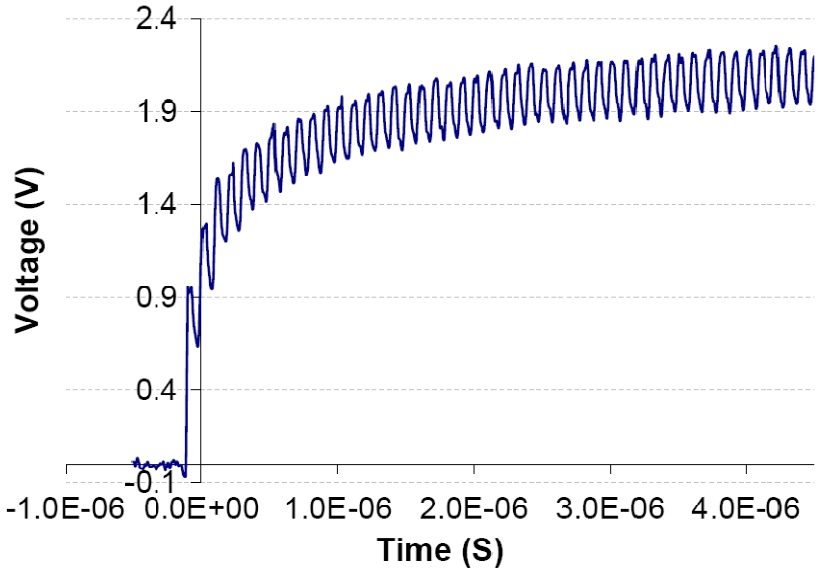

Figure 11-7. Rectified output from onboard setup for 10MHz input.

11.6 Alternative gate drive methodology

The selection of transformer coupled gate drive for high temperature operation is biased due to the availability of previous reports on this principle. A novel alternative principle is the use of silicon carbide ultraviolet (UV) photodiodes. Use of commercially available SiC UV for flame monitoring in aircraft engines was demonstrated earlier. The UV diodes on SiC technology are found to be stable for temperatures over 300°C. A reverse biased operation of the diode in detector mode, in conjunction with the forward biased emitter mode can be used to mimic the operation of a optocoupler mechanism. The proposed system is presented in Figure 11-8. Though this method seems to be promising, the added complexity of the detector – emitter assembly and the requirement of floating supply limits is practical use.

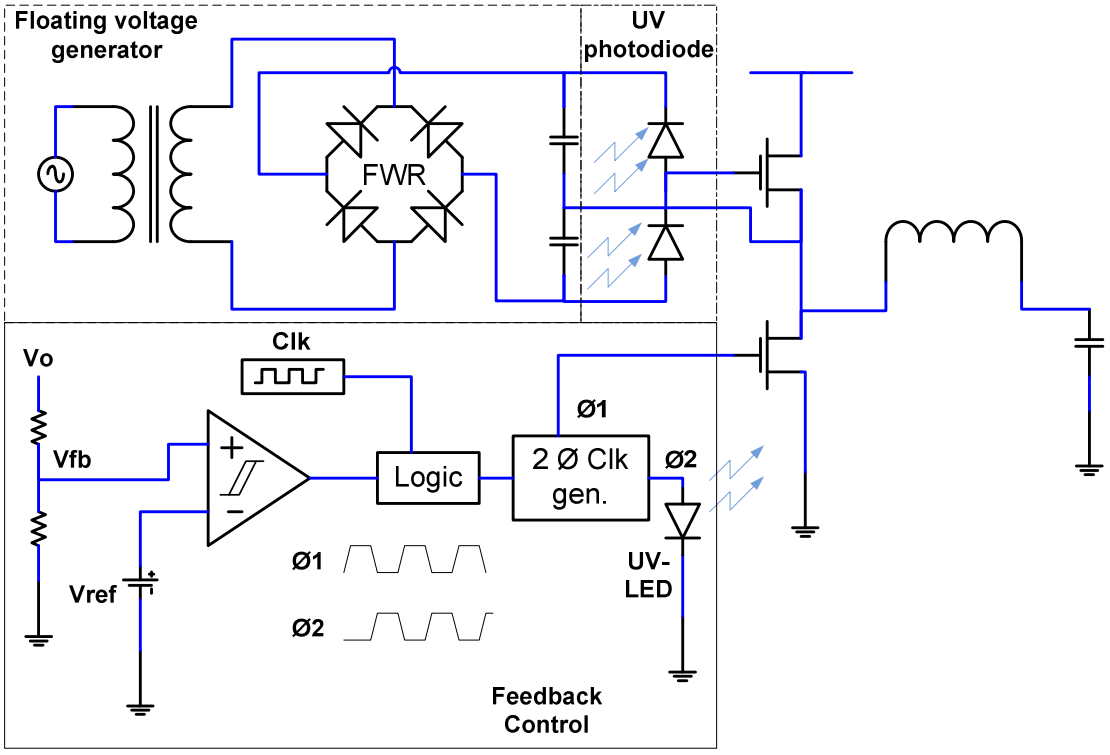

Figure 11-8. Optocoupler based gate drive mechanism suitable for high temperature operation; based on silicon carbide UV photodiodes.

11.7 Mathematical calculations – Buck converter

The following is an excel worksheet insert to calculate the inductor and capacitor based on the input parameters. Various frequencies that determine the frequency characteristics of the converter are also shown.

Table 11-1. Worksheet to calculate the inductance and capacitance for switching converter.

INPUT		
vin	25	
vo	3.3	
Switch freq	200000	
Power	5	
Max current	1.5	
Ct. ripple factor	0.3	
Regulation	0.02	
Volt. Ripple	0.066	
ESR	0.05	
ro-ea	3.00E+04	
gm-ea	3.00E-05	
cc	1.00E-08	
OUTPUT		
L	3.183E-05	(C3-C4)*(C4/C3)*(1/C5)*1/(C7*C8)
c	2.751E-04	(C19*(C7+C8*C7)^2)/((C4+C10)^2-C4^2)
f-lc-2p	1.702E+03	1/(2*3.14*SQRT(C19*C20))
f-ea-p	5.308E+02	1/(2*3.14*C13*C15)
f-cc-z	4.777E+02	C14/(2*3.14*C15)
f-esr-z	1.158E+04	1/(2*3.14*C20*C11)
Design		
esr-req	1.701E-01	1/(C22*2*6.28*C20)
cc-req	2.807E-08	C14/(6.28*C22/10)
esr-err	1.201E-01	C29-C11

11.8 Mathematical calculations – Inductance of a micro strip

The SOS IC and gate drive transformer is connected through the printed wires. These transmission lines affect the performance of the gate drive. The trace inductance adds to the leakage inductance of the transformer and hence has to be minimized. The mathematical expressions used to calculate the inductance of microstrip is applied in excel worksheet and is presented in Table 11-2. The cross-sectional view of the microstrip is shown in Figure 11-9.

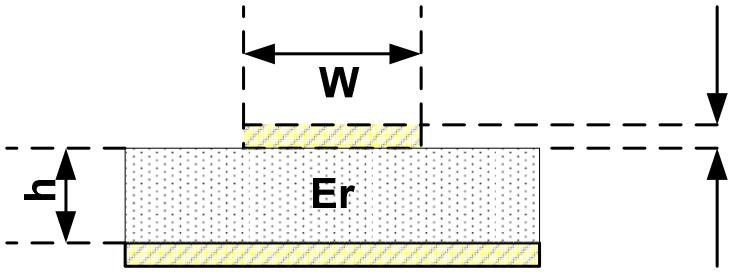

Figure 11-9. Cross-sectional view of a micro strip transmission line over a ground plane.

Table 11-2. Worksheet to calculate inductance and capacitance of a micro strip.

Inductance of microstrip (skinny w<h)

User Input			
Conductor Length	l =	0.86	
Conductor Thickness	t =	0.000176378	
Conductor Width	w =	0.06	
Dielectric Height	h =	0.02499995	
Dielectric Constant	er =	9	
Calculations			
Eff permitivity	e_skny =	6.946596673	((C8+1)/2+(C8-1)/2*(POWER(1+12*C7/C6,-0.5) +0.04*POWER(1-C6/C7,2)))
Eff perm inc thickness	eeff =	6.938676578	C11-((C8-1)*C5/C7)/(4.6*POWER(C6/C7,0.5))
Propagation delay	pd =	2.23164E-10	84.72*POWER(10, -12)*POWER(C12,0.5)
Effective width	weff =	0.060657202	C6+(1.25*C5/3.14)*(1+LN(4*3.14*C6/C5))
Characteristic Imp	z =	82.16915118	60*LN((8*C7/C6)+(C6/(4*C7)))
Result			
Inductance	L =	1.577E-08	C13*C15*C4
Capacitance	C =	2.33568E-12	C13*C4/C15

VITA

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Pages in Study: 168 Candidate for the Degree of Doctor of Philosophy

Major Field: Electrical Engineering

Scope and Method of Study:

Switch mode power supplies, commonly known as SMPS are basic building blocks of the electronic systems. SMPS performs power regulation by accepting a raw input voltage and transforming it to required voltage at output with desired characteristics. Electronic systems used in applications such as deep well oil drilling, geothermal wells and deep space explorations is expected to operate under extremely harsh conditions like elevated temperature, high pressure and radiation prone environments. To support the onboard electronics in these applications, SMPS capable of operating at extreme temperatures are of high interest.

This research work deals with the design and development of a switch mode power supply capable of operating over the temperature range of 300 degree centigrade (°C). Silicon carbide field effect transistors are used as power devices in the design to tolerate these extreme high ambient temperatures without compromising power handling capability. The simplest yet robust vee square control architecture is adopted for control mechanism. The control electronics are implemented as an integrated circuit in 0.5 µm silicon on sapphire process. The supporting components like high temperature tolerant inductors and capacitors are identified by evaluating various samples at elevated temperature.

Findings and Conclusions:

This is the first demonstration of SMPS capable of operating at 275°C as a standalone component. Also for the first time, a gate drive mechanism based on planar transformer architecture is studied and presented for high temperature operation. A low cost packaging technique suited for harsh environment operation is proposed based on gold on aluminum nitride thin film technology. The basic analog building blocks of the system, such as comparator, voltage reference and rail-to-rail amplifiers are made available in discrete packages for use at temperatures above 275°C. A SMPS prototype on a 1.8 square inches substrate is developed and tested. Test results indicate that the system is capable of operating continuously at 275°C for extended period of time, providing the desired performance characteristics.

ADVISER'S APPROVAL: Dr. Chriswell Hutchens