EXTENDED MODELS OF SILICON ON SAPPHIRE TRANSISTORS FOR ANALOG AND DIGITAL DESIGN AT ELEVATED TEMPERATURES (200°C)

By

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NOMENCLATURE/List of Symbols

A_β	area proportionality constant for current factor mismatch
$A_{V.}$	Voltage Gain
A_{VT}	area proportionality constant for Threshold voltage mismatch
BTS	Body tied Source
C_{BOX}	Capacitance of Buried Oxide layer
$C_{depletion}$	depletion capacitance
$C_{junction}$	junction capacitance
C_L	load capacitance
CMFB	common-mode feedback circuit
C_{ox}	thin oxide capacitance
DIBL	Drain Induced Barrier Lowering
DSP	Digital Signal Processing
EEPROM	electrically erasable programmable read-only memory
E_{max}	maximum electric field
F	frequency
FD	Fully Depleted
f_T	unity gain frequency
GIDL	(Gate Induced Drain Leakage
GDS	Drain to source conductance
g_m	gate transconductance
HighVt	High threshold
Id	Drain current
I_{ON}	ON current
I_{OFF}	OFF current

I_{Sense}	current flowing through sense amplifier
k	Boltzmann constant
L	Gate Length of the transistor
LDD	Lightly Doped Drain
L_{eff}	Effective Gate Length of the transistor
LowVt	Low threshold
MRAM	Magneto-resistive Random Access Memory
μ	mobility
OTA	Operational Transconductance Amplifier
PD	Partially Depleted
P_{dyn}	dynamic power consumption
PSV	Pseudo Spin Valve
q	charge of electron
R_{dummy}	resistance of dummy resistor
R_{mem}	resistance of MRAM cell
S	Sub-threshold slope
SCE	Short Channel Effects
SOC	System On Chip
SOI	Silicon On Insulator
SOS	Silicon-On-Sapphire
S/D Block	Source/Drain block
T	absolute temperature
$t_{90\%}$	timr required to reach 90%
t_d	delay time
T_{nom}	nominal Temperature
t_p	propagation time
t_{ox}	thickness of thin gate oxide
UTSi	Ultra Thin Silicon
ΔV	Overdrive Voltage
V_{dd}	supply voltage
VDS	Drain to Source Voltage

vdssat	drain to source saturation voltage
VGS	Gate to Source voltage
V_{oc}	common mode voltage
V_{os}	offset voltage
V_{th}	Threshold voltage
W	Width of the transistor
x_d	depletion region width
x_p	pinch-off region width

Chapter 1

Introduction to Silicon On Sapphire

1.1 Introduction:

The semiconductor industry has always relied on scaling for performance improvement. As we reach sub-micron dimensions short channel effects and other complexities make it difficult for the industry to follow the well-known Moore's law. From Figure 1.1 a performance droop can be observed. It can be seen that SOI aids the performance at the same dimensions.

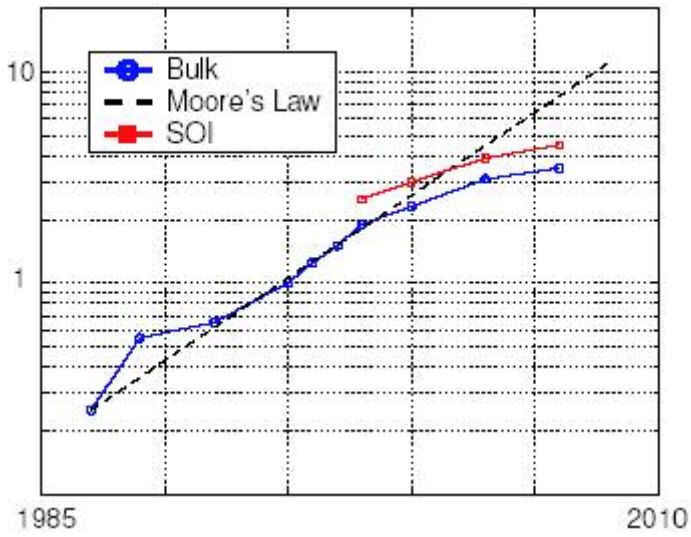


Figure 1. 1 Relative performance of Bulk and SOI and Moore's Law [1].

Silicon-On-Insulator (SOI) and Silicon-On-Sapphire (SOS) technologies have emerged as the popular contenders to bulk technologies. SOI/SOS transistors have lower drain and source parasitic junction capacitances resulting in lower power for high speed analog and digital circuits [1-3] at the same technology node. These advantages are achieved without the benefit of deeper process scaling benefiting the industry by delaying the introduction of higher precision fabrication equipment. Their unique advantages under high temperatures includes; a higher I_{ON}/I_{OFF} ratio and the absence of thermally induced latch-up, and in some instances lower threshold voltage temperature coefficients making SOI/SOS the preferred choice for elevated temperature operation. The threshold voltage temperature coefficients for Peregrine process were measured and were found to be 0.75mV/^{o}C and 1.1mV/^{o}C for NMOS and PMOS respectively. For Bulk processes these values are typically between 0.5 and 4mV/^{o}C (typically 2mV/^{o}C) [7]. The potential for integrating high voltage devices of both polarities (NMOS & PMOS) in SOI/SOS process is an added advantage. SOI/SOS has also been selected for certain RF applications because of its superior passive component capability e.g. high Q inductors and the substrate noise immunity particularly when digital circuitry is integrated onto the same IC [8-9]. SOI is comprised of a thin film of silicon, thick buried oxide on top of medium resistive silicon. SOS has a similar structure except for the silicon substrate being replaced by mono crystalline sapphire substrate. Sapphire because of its higher resistivity reduces the dielectric losses and also allows higher quality of passive elements like inductors. Sapphire has higher thermal conductance than SiO_2 thus reducing much of the 'self-heating' effects observed in SOI.

1.2 Partially Depleted (PD) Vs Fully Depleted (FD):

In partially depleted devices the active silicon film is thicker than the depletion region resulting in a body terminal (shown by the grey area) in Figure 1.2 (a). In a fully depleted device Figure 1.2 (b) the active silicon film is thinner than the depletion region hence reducing the possibility of charging the body [4]. PD SOI transistors are more easily fabricated verses FD SOI where a more highly uniformity silicon film is required. Fabricating thin film silicon poses a major challenge.

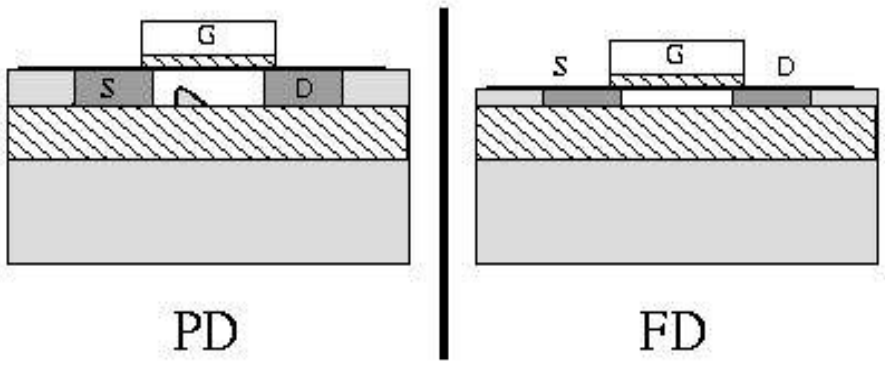


Figure 1. 2 Cross sections of partially depleted (PD) and fully depleted (FD) SOI transistors [4].

1.3 Bulk vs SOI/SOS:

The basic structural differences between bulk and SOI are as shown in Figure 1.3

- Bulk devices are built on single mono crystalline silicon.
- SOI devices have their thin mono crystalline silicon active layer separated from their substrate by a thick buried oxide.

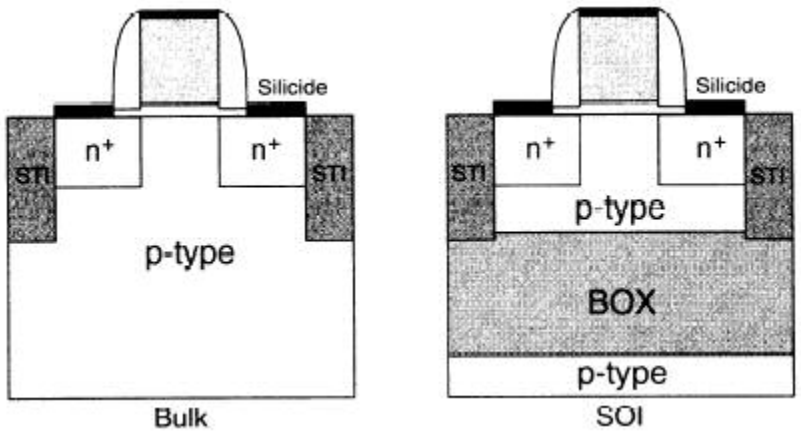


Figure 1. 3 Cross section of Bulk and SOI transistors [3].

The differences in devices and circuit performances between bulk and SOI are explained in the following subsections.

1.3.1 Reduced parasitic capacitances:

In SOI devices, the source/drain to substrate capacitance is the series combination of source/drain depletion capacitance $C_{junction}$ and buried oxide (BOX) layer capacitance C_{BOX}. Due to the lower permittivity and higher thickness of BOX layer, C_{BOX} is the smaller of the two and it dominates the overall capacitance. In the case of bulk source/drain to substrate capacitance is reduced as a result of the thinner diffusion-to-substrate junction area. As process scaling continues the threshold voltages also need to be scaled down. This is achieved by higher doping concentrations in the substrate which tends to increase the source/drain junction capacitances partially resulting from the halo implant. Absence of depletion regions near the sidewall (As a direct result of SOI being dielectrically isolated islands of silicon.) reduces the sidewall contribution to the overall

capacitance. These reduced capacitances aid in achieving higher speed performances which can be observed from Equation 1.1.

$$t_P = \int \frac{C_L}{i(v)} dv \tag{1.1}$$

The dynamic power consumption (P_{dyn}) of any CMOS topology is given in Equation 1.2

$$P_{dyn} = C_L V_{dd}^{\ 2} f \tag{1.2}$$

where C_L is the switching load capacitance, V_{dd} is the supply voltage, f is the frequency at which the circuit is switched. It can be seen that P_{dyn} is benefited by lower capacitance in a linear fashion.

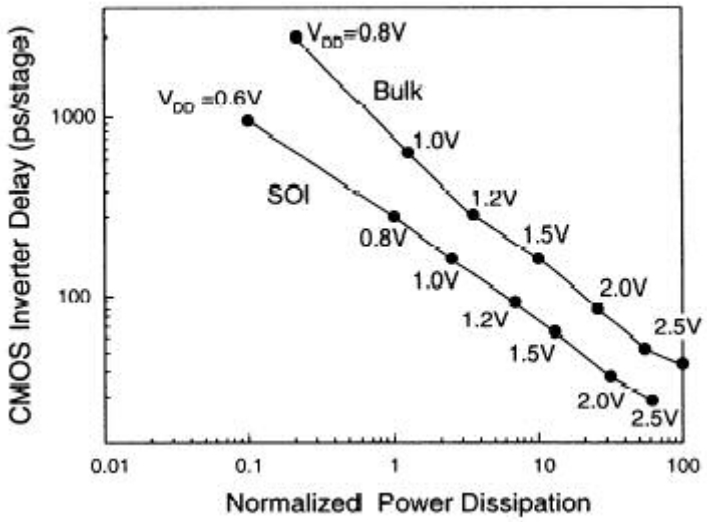


Figure 1. 4 Power dissipation and delay of 0.35um Bulk and SOI technologies for various operating voltages [5].

From Figure 1.4 it is evident that for same dimensions and supply voltage SOI has a reduced delay and lower power consumption.

1.3.2 Latch-up:

In bulk CMOS structures a parasitic thyristor is formed between supply and ground. Cross-sections of inverter in bulk and SOI are shown in Figure 1.5. Latch-up can occur as a result of transient switch triggering the PNPN thyristor. In SOI there is no direct path between devices, and as a result thyristor latch-up can never occur.

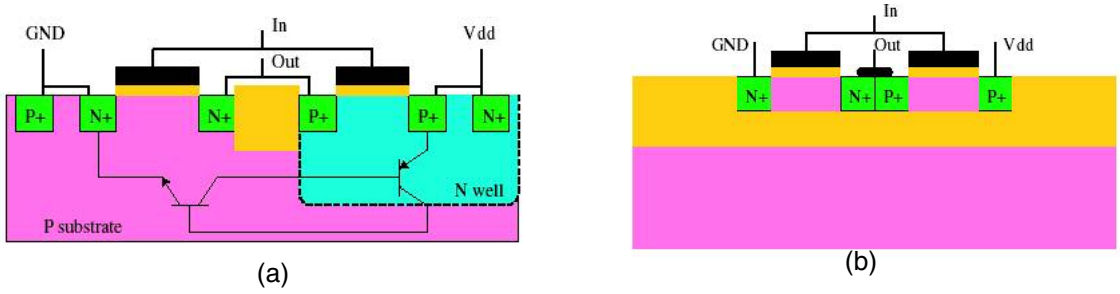


Figure 1. 5 Cross-section of Bulk (a) and SOI (b) inverter. Inverter in Bulk shows the parasitic PNP and NPN transistors.

1.3.3 Short Channel Effects (SCE):

As channel lengths are reduced short channel effects appear. As the transistors enter the short channel regime the channel is no longer under the control of just the gate, but now under the influence of both gate and drain. DIBL (Drain Induced Barrier Lowering), surface scattering, velocity saturation, hot carriers and output impedance variation with drain voltage are some of the important short channel effects [10]. The effect of DIBL is less pronounced in SOI than bulk due to the presence of buried oxide in SOI devices and this forms the main subject of discussion here. In short channel devices (devices where channel length is comparable to the depletion regions of drain/source) the potential barrier is controlled by the electric fields due to gate and drain. As the drain voltage is increased the depletion region due to drain extends more into the channel reducing the

gate voltage required to create an inversion layer [10]. The reduced absolute value of threshold voltage leads to increased off-state leakage. This occurs as a result of the reduced controllability by the gate over the depletion region due to the increased charge sharing effects of drain to gate and back gate terminals. The threshold voltage variation of DIBL effect of SOI/SOS with length is smaller than bulk due to the thin-film structure of SOI. Thin-film results in better control of the gate over the active region. Fig.6 shows the capacitive network of FD SOI and bulk transistors.

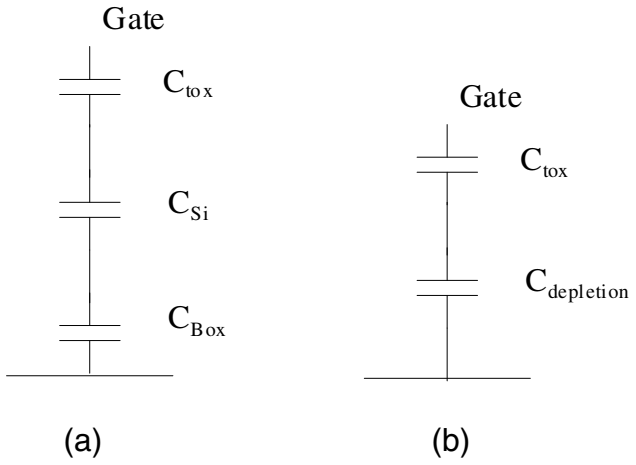


Figure 1. 6 Capacitive networks for FD SOI/SOS (a) and Bulk (b).

From Figure 1.6 it can be seen that the capacitance of (a) equivalent to the depletion capacitance $C_{depletion}$ of (b) is C_{Si} in series with C_{Box}

$$C_{eq} = \frac{C_{Si}.C_{Box}}{C_{Si} + C_{Box}} \tag{1.3}$$

The capacitance C_{eq} is dominated by C_{Box} as it is the smaller of the two. This C_{eq} is smaller than $C_{depletion}$ of bulk. This smaller equivalent capacitance of FD SOI results in better coupling of the gate voltage to the active region resulting in smaller influence of source/drain or reduced drain induced barrier lowering (DIBL).

1.3.4 OFF-State Leakage Currents:

In modern sub-micron era the leakage currents play an important role in the power consumption. In SOI channel leakage is comprised of; sub threshold currents, tunneling currents and back or side wall interface leakage. In SOI the OFF-state leakage currents are frequently dominated by the weak inversion current. In bulk leakage is dominated by the thermal generation currents of the well diode junction along with the weak inversion currents. The thermally generated current of the well junction is large as a result of the larger junction area. SOS The drain current of a MOS transistor in weak inversion is given by

$$I_{Leak} = I_0 e^{\left(\frac{V_{gs}-V_{th}}{\eta V_T}\right)} \tag{1.4}$$

where I_0 is the weak inversion current at $V_{gs}=V_{th}$, V_T is the thermal voltage and η is the body-effect coefficient.

$$\eta = 1 + \frac{C_{eq}}{C_{ox}} \tag{1.5}$$

$$V_T = \frac{kT}{q} \tag{1.6}$$

where k is the Boltzmann constant, T is the absolute temperature, q is the charge of electron. Sub-threshold slope determines the slope of the logarithm of drain current plotted as a function of gate voltage.

$$S = \frac{\partial V_{GS}}{\partial(\log_{10} I_{Leak})} = \frac{\eta V_T}{\log_{10} e} = 2.3\left(1 + \frac{C_{eq}}{C_{ox}}\right)\frac{kT}{q} \tag{1.7}$$

The lowest possible value for S is 59.5mV results for η=1 or $C_{eq} << C_{ox}$. Fig.7 shows a plot of $\log_{10} I_{Leak}$ verses V_{GS} for the Ultra thin Silicon peregrine SOS process. The sub-threshold slope for NMOS was found to be 63mV and for PMOS 65mV. As can be observed from Figure 1. 7 the smaller the value of S the better is the leakage performance and hence the I_{ON}/I_{OFF} ratio. The typical values of S for bulk and PD SOI are 80-85 mV. The significant advantage of lower value of S is that it allows lower threshold voltages with an acceptable I_{ON}/I_{OFF} ratio. The lower threshold voltages allow for the possibility of a lower power supply voltage resulting in lower switching power dissipation and deeper scaling. As the temperature is increased the threshold voltage is reduced resulting in higher I_{OFF}. It is evident from the above discussion that devices with lower sub-threshold slope have better performances at higher temperatures.

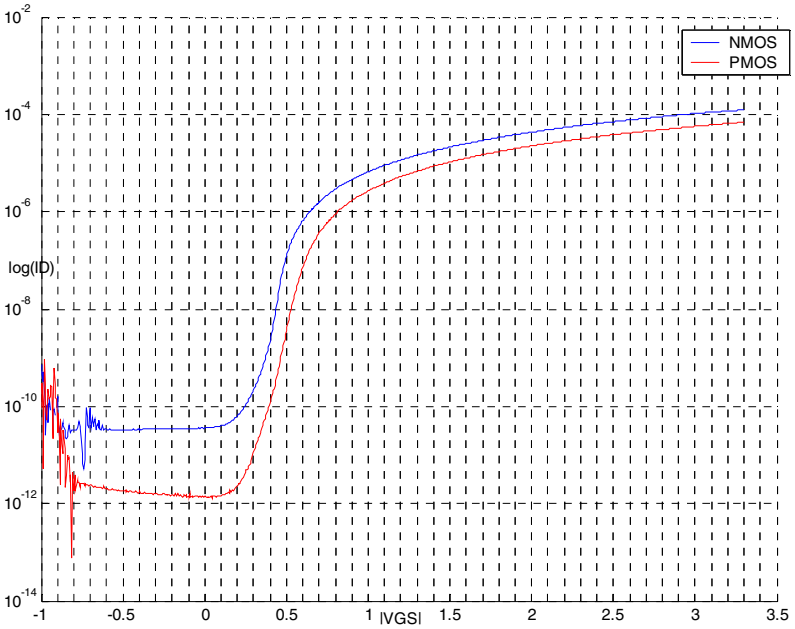


Figure 1. 7 Plot of $\log_{10}(I_{Leak})$ vs VGS for NMOS & PMOS High Vt transistors, NMOS W/L=3/1.6, PMOS W/L=3/1.6, VDS=3.3V, VGS swept from -1 to 3.3V.

1.3.5 Floating Body Effects:

In PD SOI transistors (Figure 1.2) the depletion region does not extend to the entire silicon channel region. PD SOI transistors exhibit 'kink effect' which can be eliminated by using thinner Si films as in FD SOI. This 'kink effect' is the result of floating body. The floating body problem can be reduced by using body contacts. Earlier studies [6] suggest that higher body contact resistance may in fact aggravate kink rather than reducing it. Figure 1.8 shows the parasitic BJT and the ID-VDS characteristics showing the kink effect at higher drain voltages. As the drain voltage is increased the electrons near the drain end acquire enough energy causing impact ionization leading to electron-hole pairs.

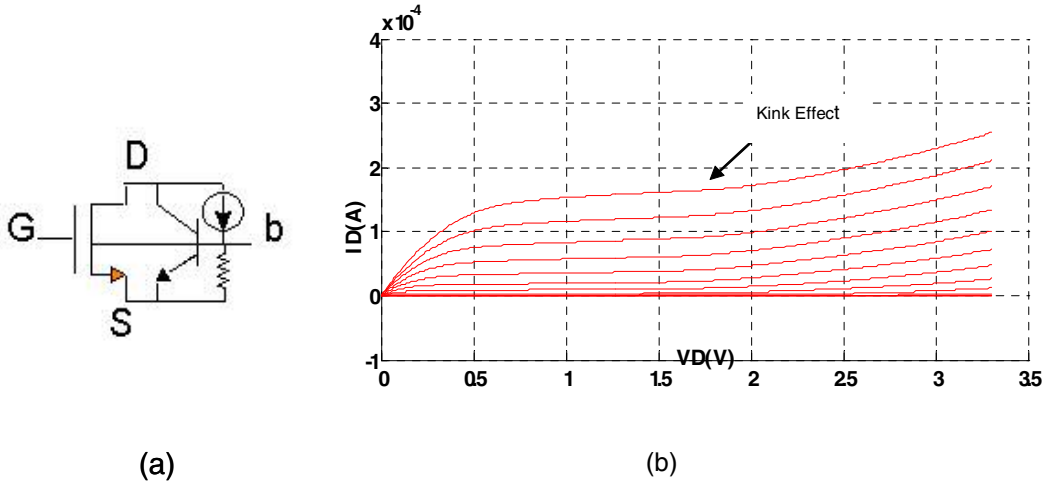


Figure 1. 8 (a) Parasitic BJT inside a PD SOI/SOS transistor. (b) ID-VDS characteristics of NMOS High Vt, W/L= 10/1, VGS = 0 to 1.2V, VDS = 0 to 3.3V at Temperature = 120^{o}C showing the kink effect.

In a NMOS device these electrons move towards the drain while the holes get accumulated in the body raising the potential of the base of the parasitic BJT. The turning

ON of this BJT introduces a sharp increase in the drain current "the kink" as shown in Figure 1.8 (b).This kink effect reduces the small signal drain resistance as shown in Figure 1.9. It can be observed that for very small gate overdrives (just above the threshold voltage) the parasitic BJT does not turn-on until 2V (Figure 1.8(b)). This late turn-on of BJT can be explained as the result of insufficient carriers in the channel which to produce hot carriers. Also it can observed that as the gate voltage is increased leading to more carriers in the channel the turn-ON voltage of the BJT gets higher for higher gate to source voltages. This 'kink effect' is smaller in PMOS devices because of the lower impact ionization of holes. While the increased drain current is beneficial for digital designs, the resulting reduced drain resistance as a function of applied drain voltage is unacceptable in most analog designs. Shown in Figure 1.9 is the small signal drain resistance, r_{ds} of a High Vt NMOS transistor.

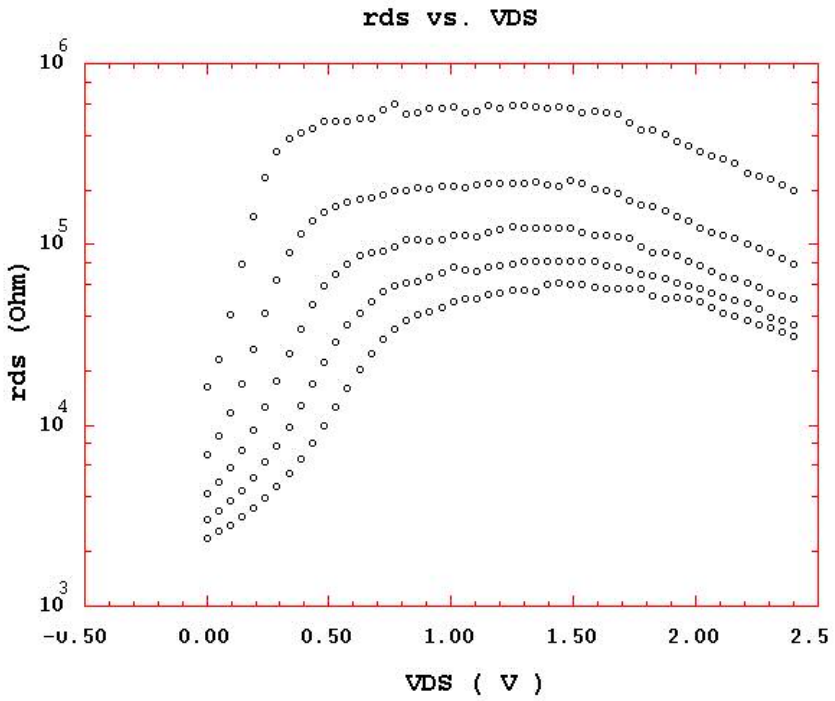


Figure 1. 9 Small signal resistance characteristics at different gate bias of an NMOS transistor, W/L=10/1, VGS = 680mV to 1.2V (5 steps), VDS= 0 to 2.4V, Temperature = 120^{o}C.

From Figure 1.9 it can be observed that the output resistance is degraded after VDS approaches 1.5V and is a moderate function of VGS due to the turn-on of parasitic BJT.

1.4 Conclusion:

From the above discussion it is clear that the Fully Depleted (FD) SOS transistors are NOT fully depleted and but are a good choice for high temperature low power high speed digital designs.

1.5 Thesis Organization:

This thesis consists of 6 chapters. Chapter 2 introduces transistor mismatch and its effects on analog design. In this chapter measurement procedures for extraction, mismatch coefficients obtained from measurements (statistical numbers) are presented for Peregrine 0.5um SOS process. In Chapter 3 design of transistors that can withstand higher voltages is presented and test results are also provided. It is also shown that these high voltage transistors are a solution to the 'kink effect'. In Chapter 4, insufficiencies of vendor (Peregrine Semiconuctor) supplied models for analog and digital simulations is presented. These model insufficiencies are addressed, the test structures used for extraction of BSIM3SOI models using Silvaco are described along with the comparative simulation results obtained from the extracted models. In Chapter 5, a brief introduction to MRAM (Magneto-resistive Random Access Memory) technology for the architectural design of 8KX8 MRAM and design of sense amplifier is presented. Chapter 6 consists of

the measurement test results of the sense amplifier and their comparison with simulated results obtained by using models extracted in Chapter 4. Finally, suggested future work is also presented.

Chapter 2

Characterization of Mismatch In SOS Process

Mismatch is defined as the finite differences between identically designed components. Mismatch is caused by variations in the processing stages, photo mask misalignment, difference in doping gradients, etc. [22]. Mismatch in this study has been treated as the mismatch in threshold voltage and current factor as a function of area, length. This chapter starts with an introduction to matching and the impact of mismatch on analog and digital design. In section 2.5 designs of test structures required for study of mismatch is discussed. For the purposes of characterizing mismatch in the Peregrine 0.5um SOS technology several identically laid out pairs of NMOS and PMOS transistors with various dimensions were tested and their results are reported in section 2.5. Statistical results were presented based on more than 2100 measurements.

2.1 Motivation:

Most of the development of CMOS technologies is biased towards digital because of lower costs involved in design and fabrication of DSP (Digital Signal Processing) chips. The effort to integrate both analog and digital on a single System On Chip (SOC) requires precision analog circuits to be built on standard CMOS technologies. As the technology is scaling down several new phenomena such as short channel effects, narrow channel effects generate mismatch. To achieve a more optimal design the analog circuit design engineer requires mismatch characterization and modeling data. For the above stated reason, characterization and modeling is very critical and is the main focus of this research. The mismatch model developed in this work focuses only on the saturation region of MOS transistors, the major region of interest to the analog circuit designer. Of all the existing commercial MOSFET models only the EKV model supports the use of mismatch parameters. The aim in this part of work is to provide mismatch model parameters that can be used during the design phase for the estimation of current mismatch and voltage offset in the circuits.

2.2 Introduction:

Mismatch in the IC world can have two origins systematic and stochastic. Systematic mismatch is defined as the mismatch whose mean is not zero. Systematic mismatch can be caused by asymmetry in devices as a result of non-identical neighboring conditions, different device orientation, asymmetric metal coverage, temperature effects due to non-uniform heating and non-uniform stress effects due to packaging. Stochastic mismatch is

caused because of random variations of physical quantities. These random errors are caused by local variations in doping concentration, oxide granularity, implantation and surface-state charges, local mobility fluctuations, random variations in oxide thickness and length and width [11]. In this exercise the differences in identically laid out transistor pairs placed very close in space and having nearly identical neighborhoods and subjected to same bias conditions were tested and parameters were extracted. Also systematic mismatch that occurs due to the absence of dummy transistors in closely laid out transistor pairs was measured. To remove the effects of packaging stress [12] all the devices were tested on the probe station with a probe card. Till date only a very few contributions have been reported on matching analysis in SOI/SOS [13][16].

2.3 Impact of matching on analog design:

The absolute accuracy of process parameters on chip is very poor but the relative matching between elements can be obtained to be as high as 100 times better [14]. The performance of many precision analog integrated circuits depends on the matching between elements. Mismatches in MOS transistors exist in V_{th}, μ , C_{ox} W and L resulting in mismatches in drain currents. DIBL also has an effect which may be included indirectly in V_{th}. Since these errors are all random, it is intuitively obvious that these become smaller if the area *WxL* is increased as a result of the averaging effects. Mismatch is the cause of mainly three phenomena dc offsets, finite even-order distortion, and lower common-mode rejection [15]. A brief analysis of mismatch in current mirrors and differential pairs is presented.

2.3.1 Current Mirror:

Mismatches are characterized in terms of standard deviations. According to [11] the variance of any parameter ΔP for short and long correlation distances is

$$\sigma^2(\Delta P) = \frac{A_P^{\,2}}{WL} + S_P^{\,2} D_x^{\,2} \tag{2.1}$$

A_P is the area proportionality constant for parameter P

S_P is the variation of parameter P with distance

The models given below are accurate only for closely laid out common-centroid transistor pairs. Mismatch in V_{th} is characterized by Equation 2.2

$$\sigma(\Delta V_{th}) = \frac{A_{VT}}{\sqrt{WL}} \tag{2.2}$$

Where A_{VT} is defined as the area proportionality constant for V_{th}, here we neglect the variation of threshold voltage with distance. Mismatch in β is given by Equation 2.3 again neglecting the distance factor.

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{WL}} \tag{2.3}$$

The mismatch in currents of the current mirror shown in Figure 2.1 is analyzed. Assuming M1 and M2 are in strong inversion region the nominal drain current through either of them follow the Equation 2.4

$$I_d = \frac{1}{2}\beta(V_{GS} - V_{th})^2 \tag{2.4}$$

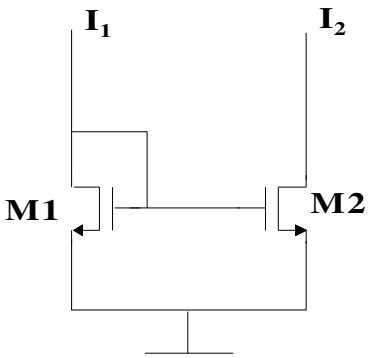


Figure 2. 1Schematic of a current mirror.

If we assume that the mismatch in threshold voltages V_{T1} and V_{T2} is ΔV_{th} and the mismatch in β to be $\Delta\beta$, then $V_{T1}=V_{th}+\frac{\Delta V_{th}}{2}$ and $\beta_1=\beta+\frac{\Delta\beta}{2}$

$$I_{d1}=\frac{1}{2}(\beta+\frac{\Delta\beta}{2})(V_{GS}-V_{th}-\frac{\Delta V_{th}}{2})^2 \tag{2.5}$$

$$=\frac{\beta}{2}(V_{GS}-V_{th})^2\left(1+\frac{\Delta\beta}{2\beta}\right)\left(1-\frac{\Delta V_{th}}{2(V_{GS}-V_{th})}\right)^2 \tag{2.6}$$

$$=I_d\left(1+\frac{\Delta\beta}{2\beta}\right)\left(1-\frac{\Delta V_{th}}{2(V_{GS}-V_{th})}\right)^2 \tag{2.7}$$

Neglecting the higher powers of the expansion and assuming that product of smaller numbers is negligible

$$I_{d1}=I_d\left(1+\frac{\Delta\beta}{2\beta}-\frac{\Delta V_{th}}{(V_{GS}-V_{th})}\right) \tag{2.8}$$

Similarly I_{d2} can be written as

$$I_{d2}=I_d\left(1-\frac{\Delta\beta}{2\beta}+\frac{\Delta V_{th}}{(V_{GS}-V_{th})}\right) \tag{2.9}$$

The difference ΔI_d in the currents I_{d1}-I_{d2} can be expressed as

$$\Delta I_d = I_d\left(\frac{\Delta\beta}{\beta} - \frac{2\Delta V_{th}}{(V_{GS} - V_{th})}\right) \tag{2.10}$$

The variance of Equation 2.10 can be expressed as below assuming that $\Delta\beta$ and ΔV_{th} are uncorrelated processes

$$\sigma^2\left(\frac{\Delta I_d}{I_d}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \frac{4}{(V_{GS} - V_{th})^2}\sigma^2(\Delta V_{th}) \tag{2.11}$$

From Equation 2.11 we can see that in order to obtain good current matching we need higher overdrive (V_{GS}-V_{th}) voltages. In fact mismatch improves as we increase overdrive and then decreases.

2.3.2 Differential Pair:

The differential pair shown below in Figure 2.2 will be analyzed for its input offset voltage assuming the currents flowing through both branches is same.

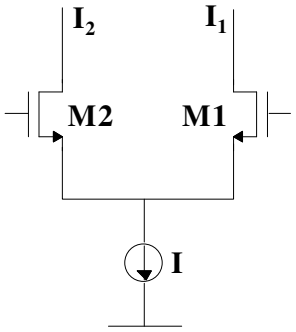


Figure 2. 2 Schematic of a differential pair.

The notation followed here would be the same as the current mirror,

$$I_{d1} = \frac{1}{2}(\beta + \frac{\Delta\beta}{2})(V_{GS} + \frac{\Delta V_{GS}}{2} - V_{th} - \frac{\Delta V_{th}}{2})^2 \tag{2.12}$$

$$= \frac{\beta}{2}(V_{GS} - V_{th})^2 \left(1 + \frac{\Delta\beta}{2\beta}\right)\left(1 - \frac{(\Delta V_{th} - \Delta V_{GS})}{2(V_{GS} - V_{th})}\right)^2 \qquad (2.13)$$

Neglecting the higher powers of the expansion and assuming that product of smaller numbers is negligible

$$I_{d1} = I_d \left(1 + \frac{\Delta\beta}{2\beta} - \frac{(\Delta V_{th} - \Delta V_{GS})}{(V_{GS} - V_{th})}\right) \qquad (2.14)$$

Similarly, $I_{d2} = I_d \left(1 - \frac{\Delta\beta}{2\beta} + \frac{(\Delta V_{th} - \Delta V_{GS})}{(V_{GS} - V_{th})}\right)$ (2.15)

In order to obtain offset voltage V_{OS} (ΔV_{GS}) we equate I_{d1} =I_{d2} and we obtain

$$V_{OS} = \Delta V_{GS} = -\frac{(V_{GS} - V_{th})\Delta\beta}{2\beta} + \Delta V_{th} \qquad (2.16)$$

Treating $\Delta\beta$ and ΔV_{th} as uncorrelated processes we can write the variance of offset voltage as

$$\sigma^2(V_{OS}) = \frac{(V_{GS} - V_{th})^2}{4}\sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \sigma^2(\Delta V_{th}) \qquad (2.17)$$

From Equation 2.17 it is evident that the offset voltage is set by the threshold voltage mismatch for smaller values of overdrive voltages.

2.3.3 Speed Accuracy and Power Consumption:

The best analog circuits are those which attain high speed high accuracy at a minimum in power consumption. The speed of a process is determined by its f_T which can be approximated by,

$$f_T = \frac{g_m}{c_{gs}} \tag{2.18}$$

The limit on the accuracy achievable is set by the relative matching of the components [17].

$$\frac{1}{Accuracy^2} = \sigma^2\left(\frac{\Delta I_d}{I_d}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \frac{4}{(V_{GS} - V_{th})^2}\sigma^2(\Delta V_{th}) \tag{2.19}$$

The power consumption for an analog circuit with a bias current of Id is,

$$P = V_{DD} \cdot I_d \tag{2.20}$$

A quality factor was defined in [17] to include all these factors,

$$\frac{Speed.Accuracy^2}{Power} = \frac{\left(\frac{g_m}{C_{gs}}\right)}{\left(\sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \frac{4}{(V_{GS} - V_{th})^2}\sigma^2(\Delta V_{th})\right)\left(V_{DD} \cdot I_d\right)} \tag{2.21}$$

$$= \frac{2}{(V_{GS} - V_{th}) \cdot C_{gs} \cdot \left(\sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \frac{4}{(V_{GS} - V_{th})^2}\sigma^2(\Delta V_{th})\right)\left(V_{DD}\right)} \tag{2.22}$$

$$\approx \frac{2}{\cdot C_{gs} \cdot \left(\sigma^2\left(\frac{\Delta\beta}{\beta}\right)(\Delta V_{Eff}) + \frac{4}{(\Delta V_{Eff})}\sigma^2(\Delta V_{th})\right)\left(V_{DD}\right)} \tag{2.23}$$

Taking derivative with respect to ΔV_{Eff} and solving for optimum ΔV_{Eff} bias point results in

$$\Delta V_{Eff\_Opt} = 2\sqrt{\frac{\sigma^2(\Delta V_{th})}{\sigma^2\left(\Delta\beta/\beta\right)}} = 2\left(\frac{A_{vth}}{A_\beta}\right) \tag{2.24}$$

What one observes 1) that with all the other parameters being set the determining factor is in the efficient use of power depends on process matching factor and 2) off set is initially large, reaches a minimum described by (2.24) and then increase again.

2.4 Mismatch effects on Digital design:

As the clock speeds in digital circuits are ever increasing and the device dimensions are decreasing, device mismatch sets the limit on operable frequency. Device mismatch introduces a time independent clock skew. To the first order, the delay through an inverter t_d can be written as in Equation 2.25. C_L is the load capacitance, μ is the channel mobility, C_{ox} is the gate oxide capacitance per unit area and α approaches unity for short-channel transistors [18]. As can be seen from Equation 2.25 delay is a function of V_{th} and β. Also t_d is a strong function of supply voltage V_{DD}. Reduced supply voltage results in increased skew for the same degree of mismatch.

$$t_d = \frac{2 \cdot C_L \cdot V_{DD}}{\mu \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_{DD} - V_{th})^{\alpha}} \tag{2.25}$$

2.5 Test Structure Design and Measurement Procedure:

Mismatch is partly geometry dependent and partly distance dependent. In order to extract the geometry dependent mismatch parameters a test matrix of transistors with various length and width combinations as shown in Table 2.1 was designed. All the dimensions shown in Table 2.1 use the notation ‘m@W/L’ where ‘m’ stands for number of fingers, W for the width of the transistor and L for the length. The other factor that affects matching between components is the distance between them. The parameter S_P in

Equation 2.1 quantifies the effect of distance on matching. To characterize this we need to make the array of transistors with same geometry placed at different distances like 50um, 100um, 200um till 500um from a reference transistor. The effect of distance is not in the scope of this study.

Table 2. 1 Transistor (NMOS & PMOS) device dimensions.

m*W	L=0.8um	L=1um	L=2um
2	2/0.8	none	None
4	2@2/0.8	none	None
8	4@2/0.8	2@4/1	2@4/2
16	8@2/0.8	4@4/1	4@4/2
32	16@2/0.8	8@4/1	8@4/2
64	none	16@4/1	None

The test geometries were chosen so that dependence of matching parameters on area for a constant length can be characterized and extracted. Each column in the Table 2.1 specifies the different widths chosen for a single transistor length. Also the variation of matching parameters with length (in an attempt to capture the length dependent effects on matching), for the same gate area.,

All of the mismatch characterization was carried out in the saturation region for the following reasons: most of analog design is carried out with transistors biased in saturation; the currents in saturation region are larger and as a result leading to smaller measurement errors. For each transistor pair four measurements were made to reduce measurement errors. Shown in Figure 2.3 are the distributions of threshold voltage mismatch and current factor mismatch for 2@2/0.8um NMOS Low Vt transistor.

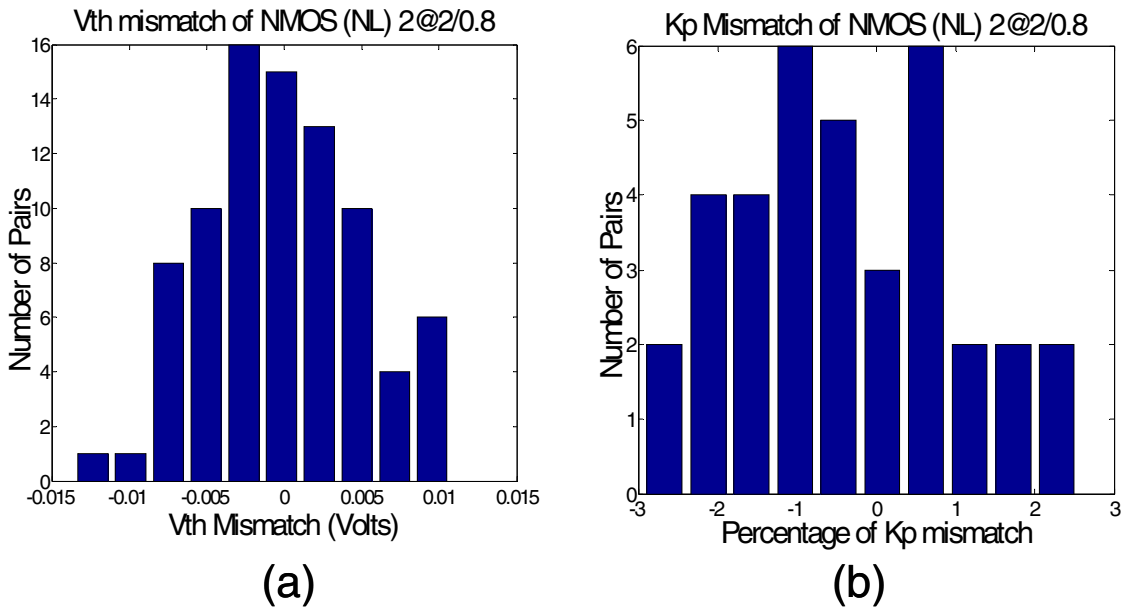
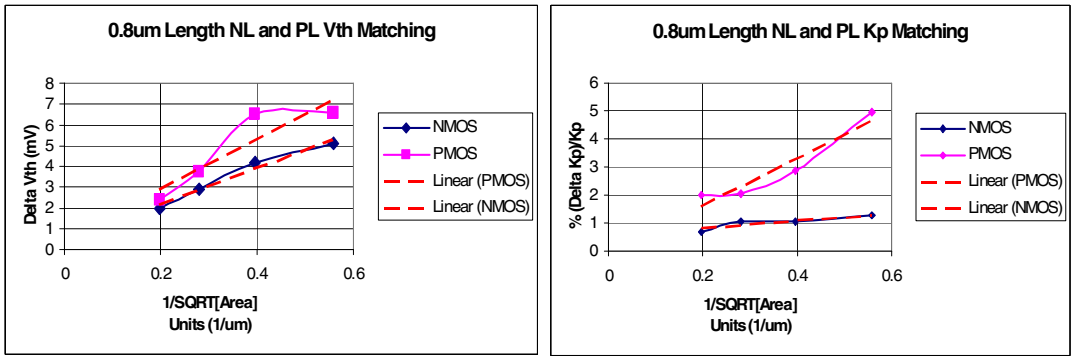


Figure 2. 3 Mismatch distributions for (a) Threshold voltage (b) current factor for 2@2/0.8 NMOS (NL) transistors.

Shown in Table 2.2 are the standard deviations and mismatch coefficients of NMOS and PMOS transistors.

Table 2. 2 Standard deviations of Vth mismatch and current mismatch factor and their respective coefficients.

		NMOS		
W/L	σ(ΔVt) [mV]	Avth	σ(Δβ/β) [%]	Aβ
2@2/0.8	5.1	9	1.2706	2.273
4@2/0.8	4.2	10.8	1.0298	2.6052
8@2/0.8	2.9	10.4	1.0493	3.753
16@2/0.8	2	10.2	0.703	3.55
2@4/1	4	11.2	0.62596	1.7705
4@4/1	2.45	9.8	0.669	2.6673
8@4/1	2.387	13.49	0.454	2.5715
16@4/1	1.762	14.1	0.326	2.61
2@4/2	2.44	9.7	0.4818	1.9273
4@4/2	2.4	13.587	0.376	2.1294
8@4/2	2.02	16.2	0.25829	2.0663
		PMOS		
2@2/0.8	6.56	11.75	3.81	6.81
4@2/0.8	6.5	16.5	2.86	7.25
8@2/0.8	3.76	12.8	2.0251	7.24
16@2/0.8	2.38	12.08	1.993	10.116
2@4/1	3.85	10.9	2.16	6.12
4@4/1	2.9325	11.73	1.74	6.97
8@4/1	2.1073	11.9	1.31	7.46
16@4/1	1.64	13.15	1.1	8.81
2@4/2	2.705	10.82	1.88	7.53
4@4/2	2.13	12.1	1.434	8.12
8@4/2	1.737	13.9	1.107	8.86



(a) (b)

Figure 2. 4 Variation of (a) threshold voltage mismatch (b) current factor mismatch with 1/sqrt(area) for NMOS (NL) and PMOS(PL) with L=0.8um. Shown in dashed lines are linear fits of data.

2.6 Systematic Mismatch:

As mentioned earlier systematic mismatch is caused due to non-identical neighboring conditions. To investigate this, transistor pairs with and without dummy transistors were fabricated. Shown in Figure 2.5 & Figure 2.6 are the distributions of current mismatch of pairs with and without dummy transistors. These values of mismatch were obtained on PMOS Low Vt transistors at a bias current value of 1mA.

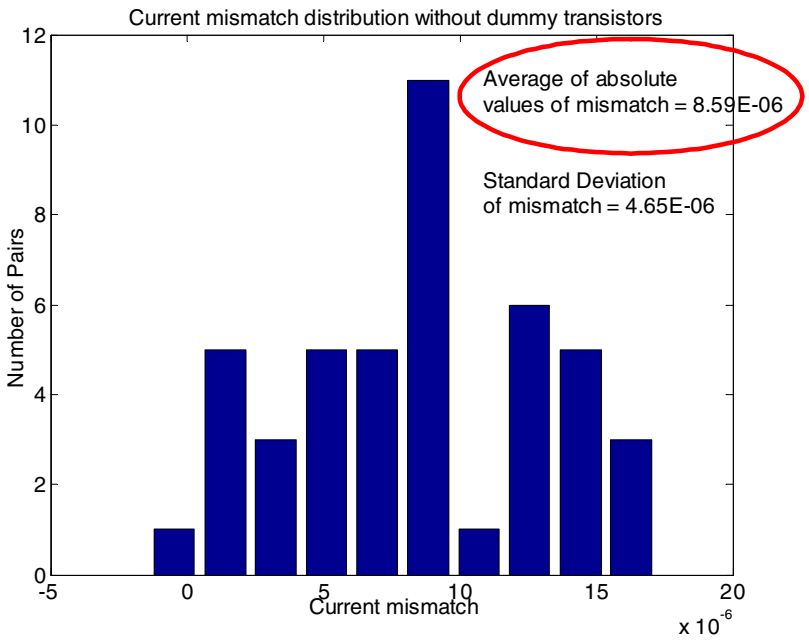


Figure 2. 5 Current mismatch distribution of the transistor pair without dummy transistors, m@W/L = 16@7.5/1.

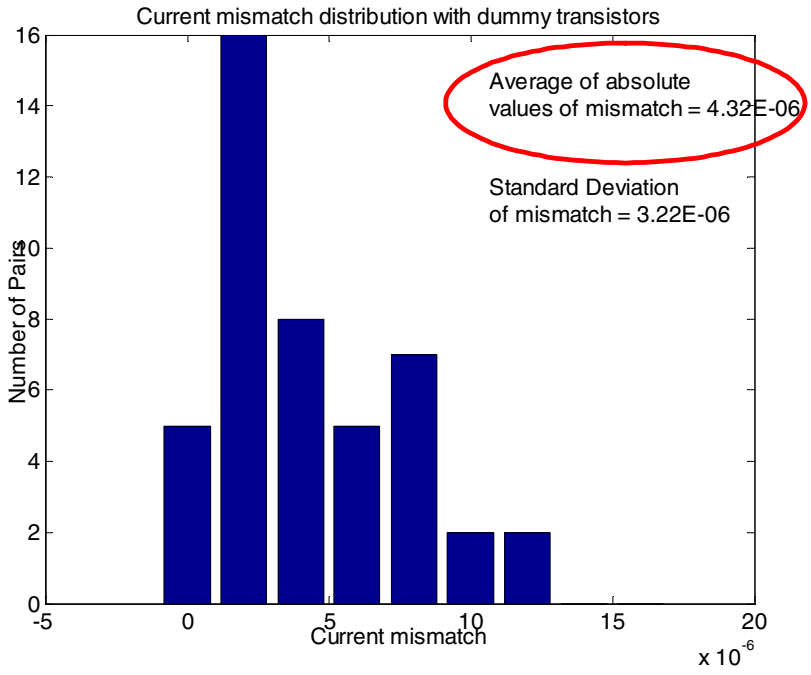


Figure 2. 6 Current mismatch distribution of the transistor pair with dummy transistors, m@W/L = 16@7.5/1.

From Figure 2.5 & Figure 2.6 it can be observed that the average of absolute mismatch in currents and their standard deviation is larger for the transistor pair without dummy transistors. This increased mismatch in currents can be attributed to the edge transistors whose neighboring conditions are different due to the lack of dummy transistors. It is clear from Table 2.2 that the percentage mismatch would be a larger if the number of fingers were less than the number of fingers used in this study (16).

2.7 Comparison with previous studies and Conclusions:

Figure 2.7 shows the threshold voltage mismatch proportionality constant A_{VT} variation with gate oxide thickness t_{ox} for several processes [20].

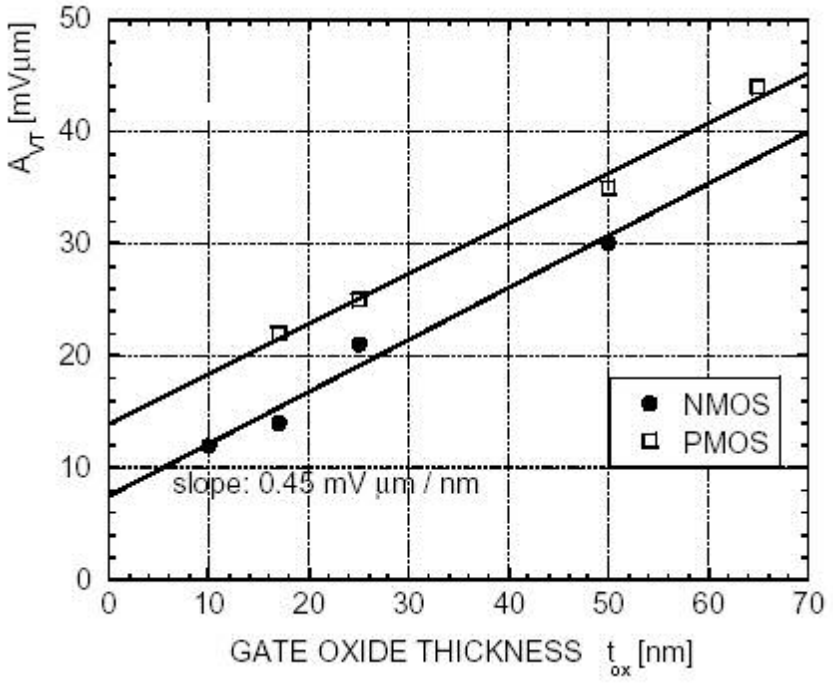


Figure 2. 7 Plot of A_{VT} variation with gate oxide thickness of several processes [20].

The minimum feature size devices used in this comparison were 0.5um[21], 0.7um & 1.2um [20], 2.5um [11], 3um [19]. A straight line fit of this data points gives a slope of 0.45 mVum/nm and intercepts of 7.5mV um and 13.8 mVum for NMOS and PMOS transistors [20]. Shown below in Table 2.3 are the values predicted from the trend discussed above and the measured values.

Fig.2.8 shows the current factor mismatch proportionality constant A_β variation with gate oxide thickness t_{ox} for several processes [20]. The minimum feature size devices used in this comparison were 0.5um [21], 0.7um & 1.2um [20], 2.5um [11], 3um [19]. The current mismatch has not scaled down with device scaling and remained at around 2-3% for NMOS and 3-4% for PMOS [20].

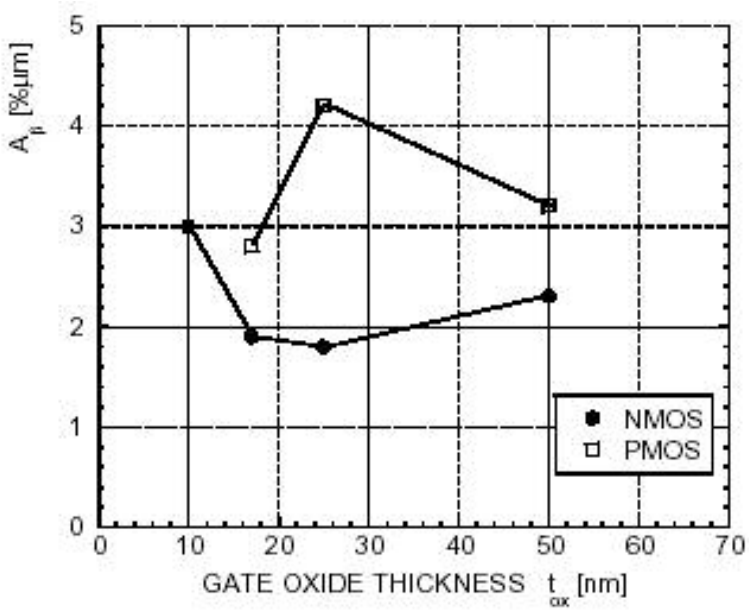


Figure 2. 8 Plot of A_β variation with gate oxide thickness of several processes [20].

Table 2. 3 Mismatch coefficients predicted from the above discussed trend and measured values on Peregrine process (tox=10nm, Lmin=0.5um).

Device	A_{VT} Predicted values	A_{VT} Measured Values	A_β measured

Type	(mV um)	(mV um)	values [% um]
NMOS	12	11.67	2.53
PMOS	18.3	12.51	7.75

From Table 2.3 it can be observed that the A_{VT} values obtained for the Peregrine (t_{ox}=10nm, L_{min}=0.5um) process are 2.75 % (NMOS) and 31% (PMOS) smaller than the predicted values. For A_β it can be observed that NMOS values lie in the range of 2 to 3% as was predicted by [20]. But in the case of PMOS A_β value is 120% in error from the predicted value.

In this chapter the Pellgrom matching rule of the variance being proportional to the inverse of root of area was verified and mismatch coefficients A_{VT} & A_β were extracted. The effect of mismatch on analog and digital design was reviewed and a comparison of mismatch coefficients with similar technologies was done and the results indicate that mismatch coefficients of Peregrine process are 2.75 % (NMOS) and 31% (PMOS) smaller than the predicted values.

Chapter 3

High Voltage Transistors

The CMOS industry has always been inclined towards scaling down the process features. Process scaling benefits traditional analog and digital circuits by improving their delay power product. Scaling down the device dimensions requires scaling down the power supply voltages to keep the electric fields constant. For applications like on-Chip DC-DC converters, EEPROM's etc., transistors that can withstand higher than nominal drain to source voltages are required. In this work transistors that can withstand higher voltages were designed in the Peregrine UTSi process. These were tested and their test results are shown in Section 3.5. These transistors also suppress the *"kink effect"* as can be observed in their drain characteristics.

3.1 Introduction:

As the applied drain to source voltage is increased the strong electric field across the pinch-off region increases causing hot carriers and favors avalanche breakdown. Increasing the transistor length can increase the operable range by a small value. To decrease the field intensity the depletion region needs to be widened. In Figure 3.1 a conventional transistor is shown. It can be seen that the depletion region cannot extend considerably into the heavily doped drain. E_{max} represents the maximum electric field intensity, x_p represents the pinch-off region, x_d represents the depletion region width in the drain.

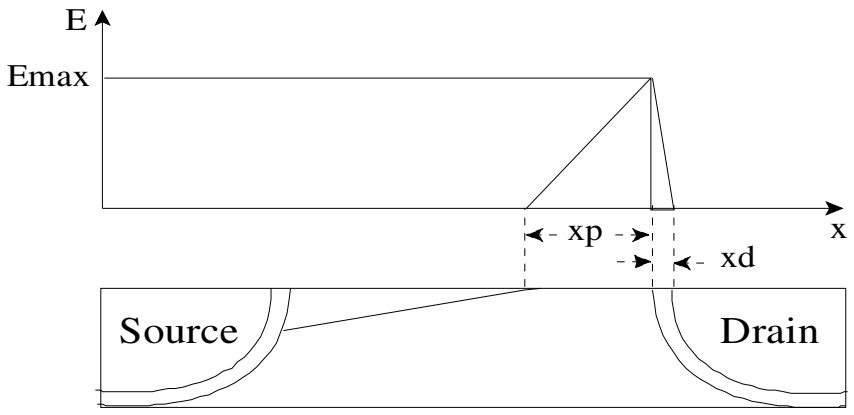


Figure 3. 1 Lateral electric field across a regular transistor.

The field intensity increases linearly across the pinch-off region x_p and drops linearly across the depletion region x_d. The total drain to source voltage *V* is the area under these triangles

$$V = \frac{E\max}{2}(xp + xd) \tag{3.1}$$

The widths of pinch-off region and the depletion region are inversely proportional to the square root of their doping concentration [23]. From Equation 3.1 it can be seen that *V* can be increased by increasing x_d. The depletion region width was increased by decreasing the drain doping concentration. However, the decrease in doping concentration of the drain however increases the drain resistance. To overcome this, a combined structure formed by a lightly doped region followed by heavily doped drain region was used as shown in Figure 3.2.

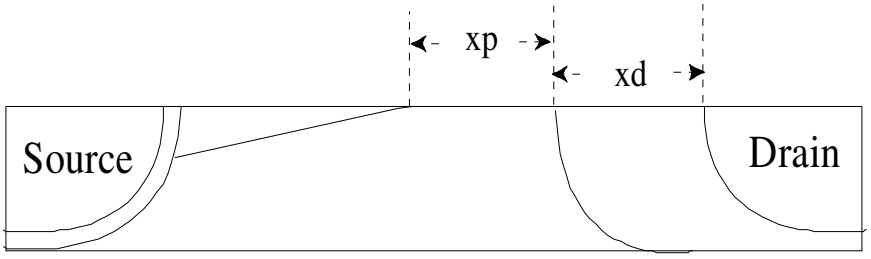


Figure 3. 2 Pinch-off and depletion regions of a Lightly doped drain transistor.

3.2 Implementation in Peregrine UTSi process:

The doping profiles for a typical NMOS transistor are as shown in the Figure 3.3 and those for a Lightly Doped Drain structure are as shown in Figure 3.4. The construction of a high voltage device involves introduction of a low doped n-type material between the channel and the drain. The typical transistors in the Peregrine UTSi process have a breakdown of about 4 to 5V and the LDD transistors presented here exhibited a breakdown voltage of about 8V to 10V, a factor of approximately 2 improvement.

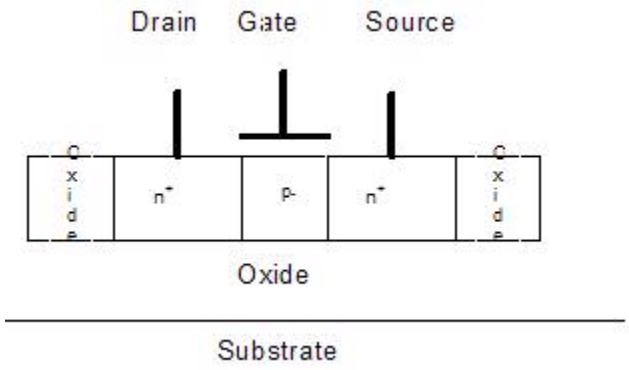


Figure 3. 3 Doping concentrations of a typical SOS NMOS transistor.

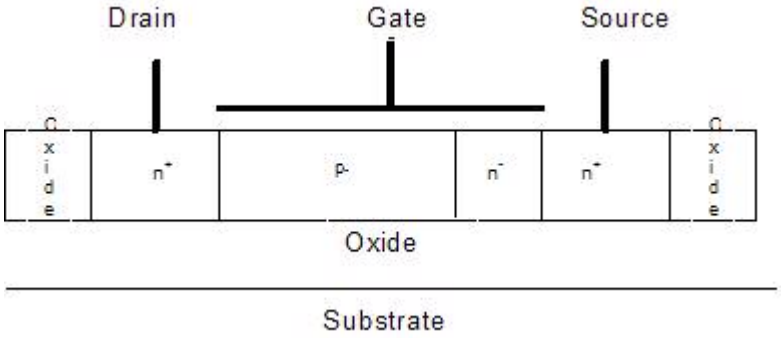


Figure 3. 4 Doping concentrations of LDD SOS NMOS transistor.

The LDD PMOS transistors were built with a low doped p-type material as an extension of the drain. The layers n^- and p^- were not directly available in Peregrine UTSi process, so an n^- layer was obtained by placing a p-type material under the gate which produced the n^- layer and the complementary was done to obtain p^- layer required for LDD PMOS device. The layouts of the high voltage NMOS and PMOS devices with and without Body-tied-source are shown below if Figure 3.5.

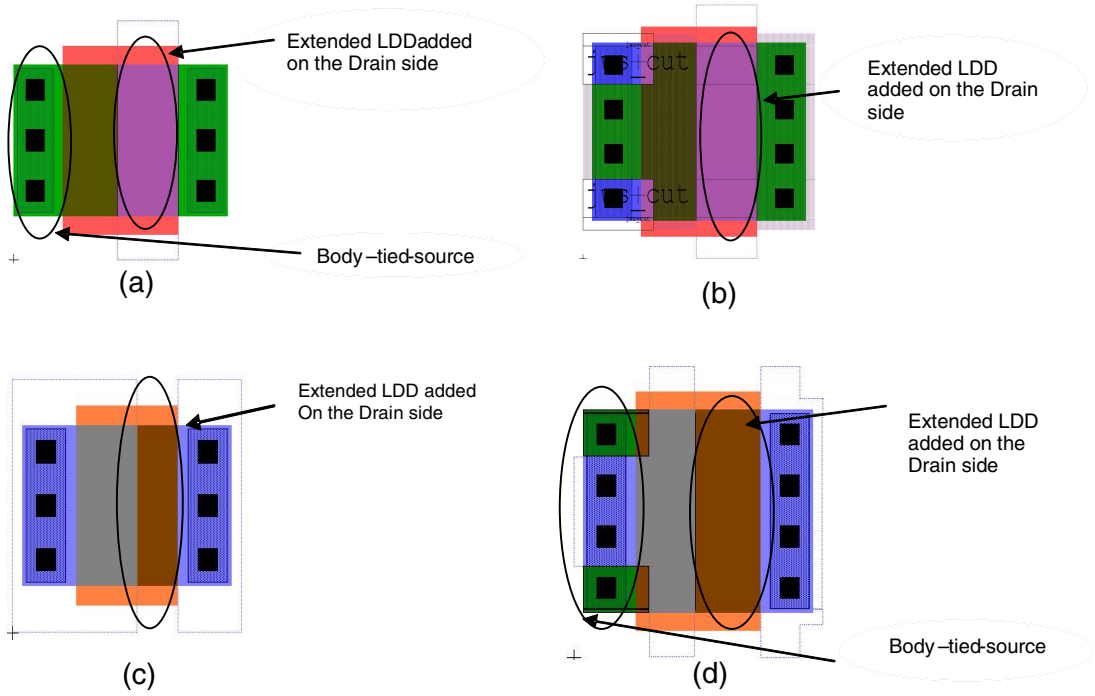


Figure 3. 5 Layouts of LDD NMOS and PMOS transistors with (a,c) and without (b,d) Body-tied-Source . W = 4.2 um for (a) & (c), W=3 um for (b) & (d), for all the transistors L=1.8um and LDD=1.2 um.

3.3 S/D Block Transistors:

As a part of this work a second type of high voltage transistors was attempted and their test results are presented. The schematic and the layout of a transistor of this device are as shown in Figure 3.6.

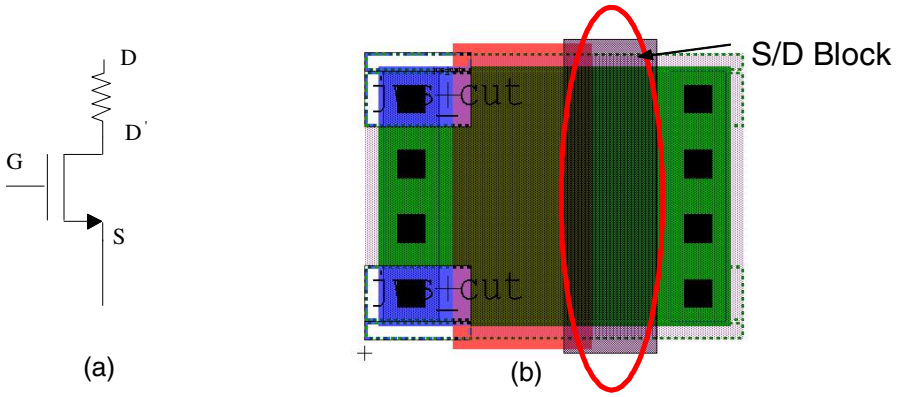


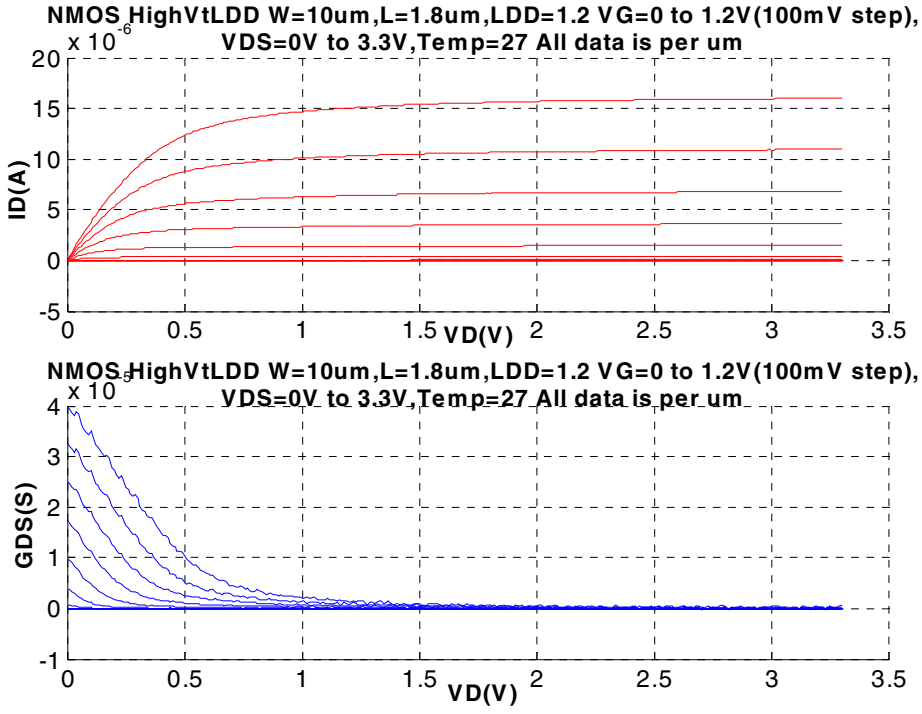
Figure 3. 6 Schematic (a) and layout (b) of a high voltage transistor with S/D Block at the drain side, W=3 um, L=3 um and L of S/D Block =2 um.

In the Peregrine process, the S/D block layer is used to block doping of diffusion areas. Since the region underneath the S/D block layer is un-doped it exhibits a very high resistance. This is particularly used in making high valued resistors that occupy smaller area compared to the resistors made from regular diffusion materials. In this implementation of high voltage transistor (Figure 3.6), a S/D Block layer was placed near the drain end of the transistor. The presence of a resistor in series with the channel imposes a lower voltage across the channel thereby allowing higher voltages across drain and source . ID-VDS characteristics of this "transistor are" as shown in Figure 3.12.

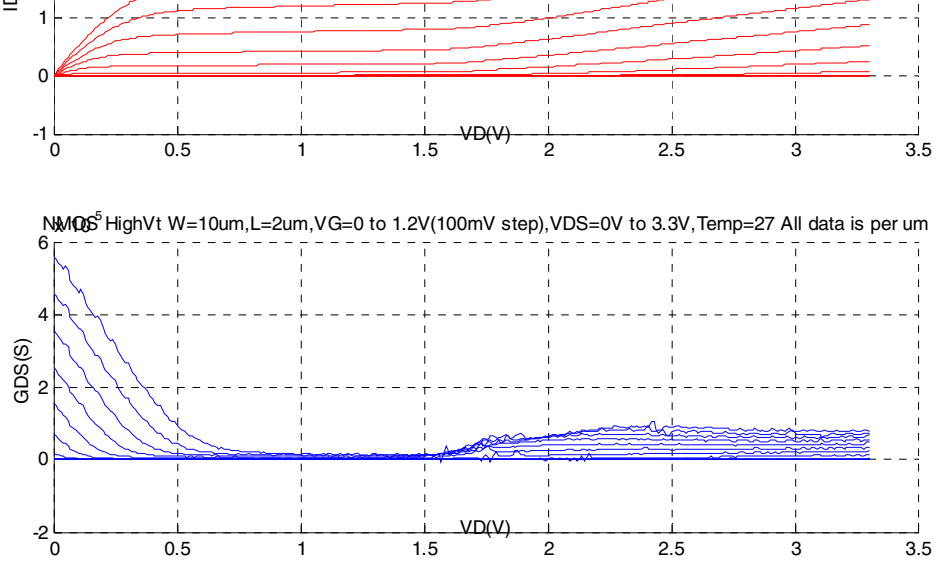
3.4 Suppression of "*Kink Effect*":

The hot carriers are generated due to high electric field in a regular SOS MOSFET are suppressed in LDD devices due to the presence of low doped region adjacent to the drain. From Figure 3.7 (b) and (c) it is easily observed that there is no "kink effect" in LDD devices. The major draw back of these devices is their higher "*vdssat*" compared to regular transistors. This can accounted for by the added resistance

offered by the lightly doped region. The device in this present discussion needs further research and refinement to obtain the best LDD dimension possessing a tolerable kink for best achievable *"vdssat"*. In Figure 3.8 a comparison of ID-VDS characteristics of High Vt NMOS with a channel length of L=2um and an LDD device with L=1.8um is shown. The currents were plotted for same effective drive strength and similar voltage conditions. It is readily observable that the LDD device has a Leff greater than 2um. The effective length, L_{Eff} of the LDD device was calculated to be 2.36 um by equating the currents of both transistors at VGS=1.2 V, VDS = 1.5V.



(a)



(b)

Figure 3. 7 (a) ID-VDS and GDS-VDS for NMOS High Vt LDD transistor, W=10um, L=1.8um, VG=0 to 1.2V (100mV step) at temperature T=27o C (b) GDS – VDS for NMOS High Vt transistor, W=10um, L=2um. (All the data in above plots was scaled to an effective W/L=1).

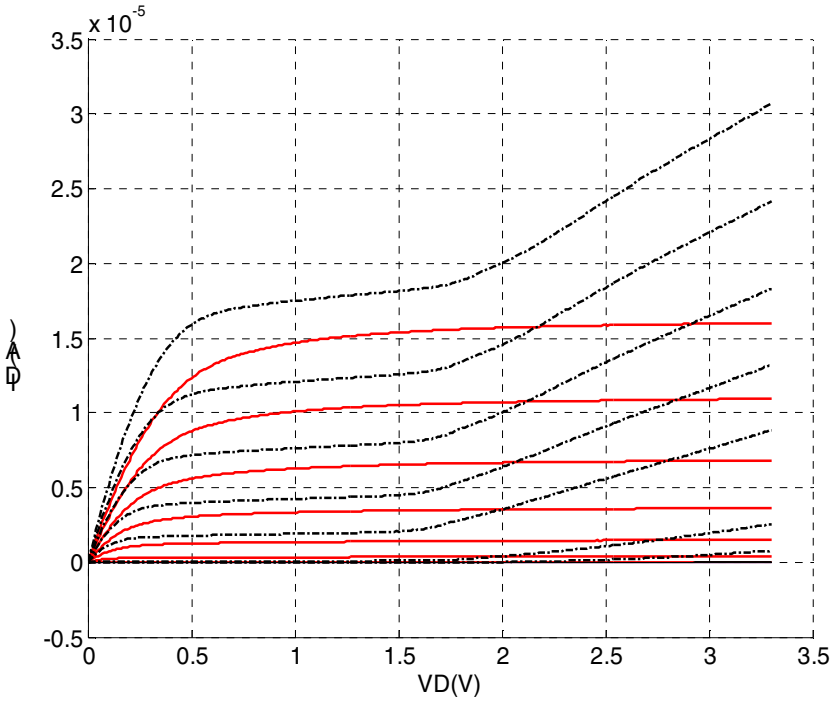


Figure 3. 8 Comparison of ID-VDS characteristics of High Vt NMOS with a channel length of L=2um (dash-dot) and an LDD device with L=1.8um (solid in red). Effective length LEff of the LDD device was calculated to be 2.36 um by equating the currents of both transistors at VGS=1.2 V, VDS = 1.5V.

The above ID-VDS characteristics were plotted with VGS varied from Vth till ΔV = 600mV for both devices which is the region of device interest for analog circuit designers, where Vth was extracted equal 610mV. The LDD transistors suffer a degraded maximum operable frequency due to the added gate capacitance of the LDD section. Given below are the calculations of maximum operable frequency for NMOS with L+LDD = (1.8+1.2) um and a regular device with L=2um.

From Figure 3.8, for a ΔV =300 mV or V_{gs} = 900 mV, $g_m = \frac{\partial I_d}{\partial V_{gs}}$ = 26.12 uS

The data in the Figure 3.8 is a normalized plot, for an effective W/L of 1, and as a result the g_m of the transistor when scaled back to original geometry (W/L equal 10/1.8) has a gm of 146.11uS and Cgs of 70.8fF (Cox equal 3.54fF/um^{2}and C_{gs} = 2/3 (W[L+LDD]C_{ox})).

The resulting unity current gain bandwidth from $f_T = g_m / 2\pi C_{gs}$, equals 326 MHz.

The f_T of a regular 2um NMOS device calculated in a similar manner results in 483 MHz or the LDD device is 50% slower as a result of the added LDD capacitance.

3.5 Test Results:

Test results confirmed the functionality of LDD transistors and they were to found to holdoff drain to source voltages up to 8V to 10V at 200^o C. ID-VDS characteristics of an NMOS LDD transistor with and without body-tied-source (BTS) at temperatures of 25^o C and 200^o C are shown in Figure 3.9.

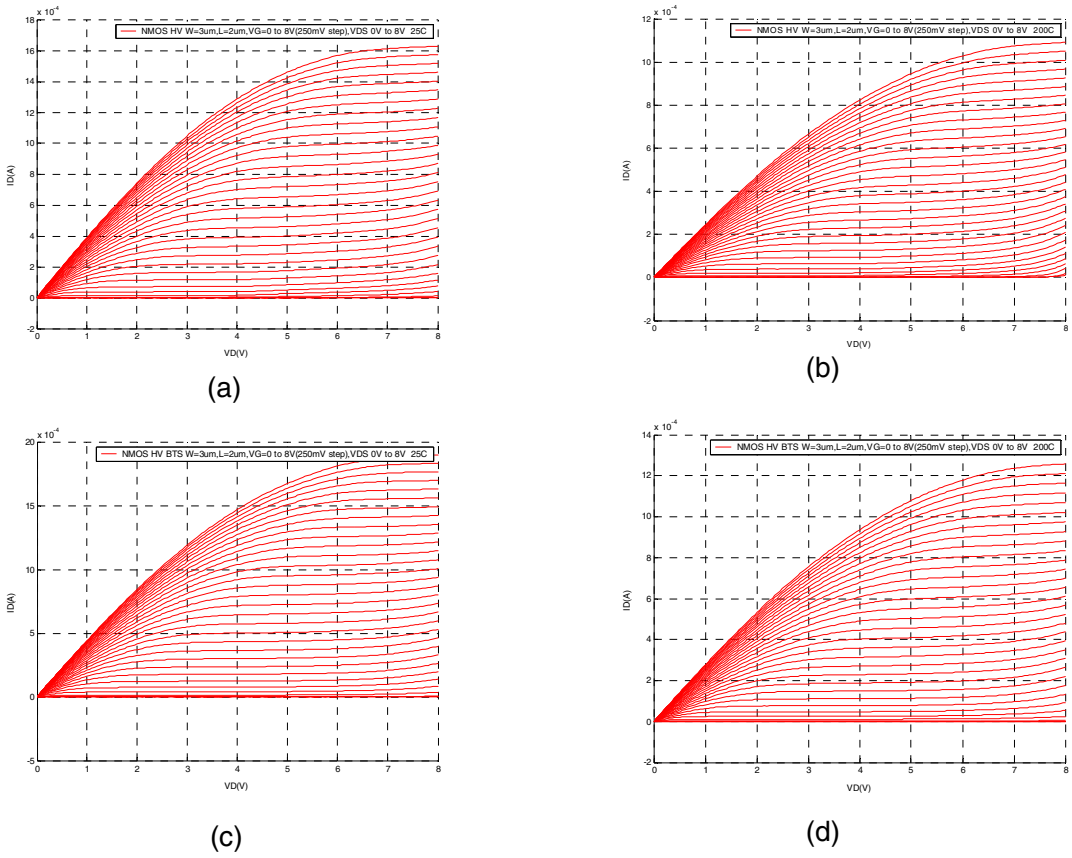


Figure 3. 9 ID-VDS characteristics of High voltage transistors (a) W/L=4.2/1.8, LDD=1.2um, LDD NMOS at 25^{o} C (b) W/L=4.2/1.8, LDD=1.2um, LDD NMOS at 200^{o} C (c) W/L=3/1.8, LDD=1.2um, LDD NMOS BTS at 25^{o} C (d) W/L=3/1.8, LDD=1.2um, LDD NMOS BTS at 200^{o} C.

Test results of LDD PMOS transistors confirmed the functionality and these were found to hold off drain to source voltages up to 10V to 12V at 200^{o} C. ID-VDS characteristics of PMOS LDD transistors with and at 25^{o} C and 200^{o} C are as shown in Figure 3.10.

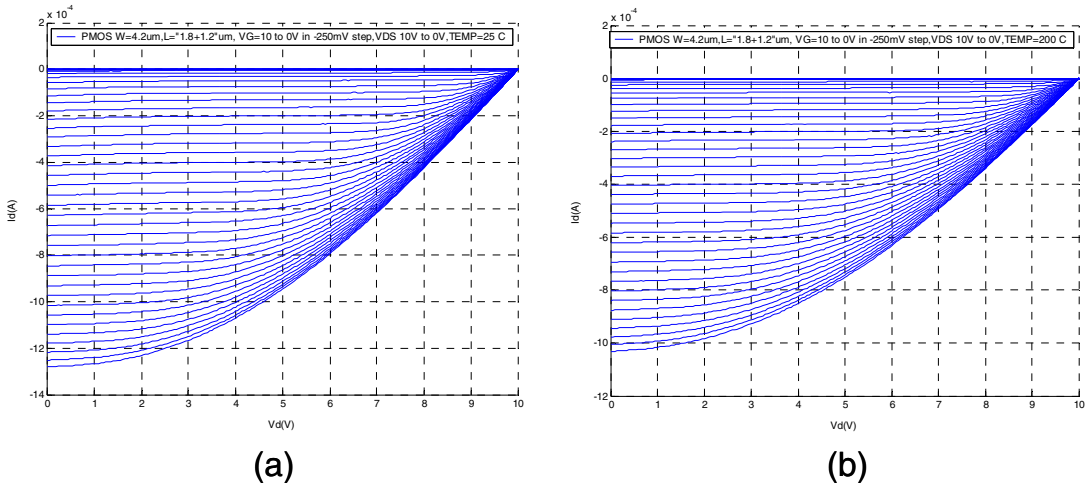


Figure 3. 10 ID-VDS characteristics of High voltage transistors (a) W/L=4.2/1.8, LDD=1.2um, LDD PMOS at 25^{o}C (b) W/L=4.2/1.8, LDD=1.2um, LDD PMOS at 200^{o} C.

The ID-VDS characteristics of PMOS LDD with BTS at 25^{o} C is as shown in Figure 3.11. It can be observed that they can be operated successfully without breakdown up to 12V.

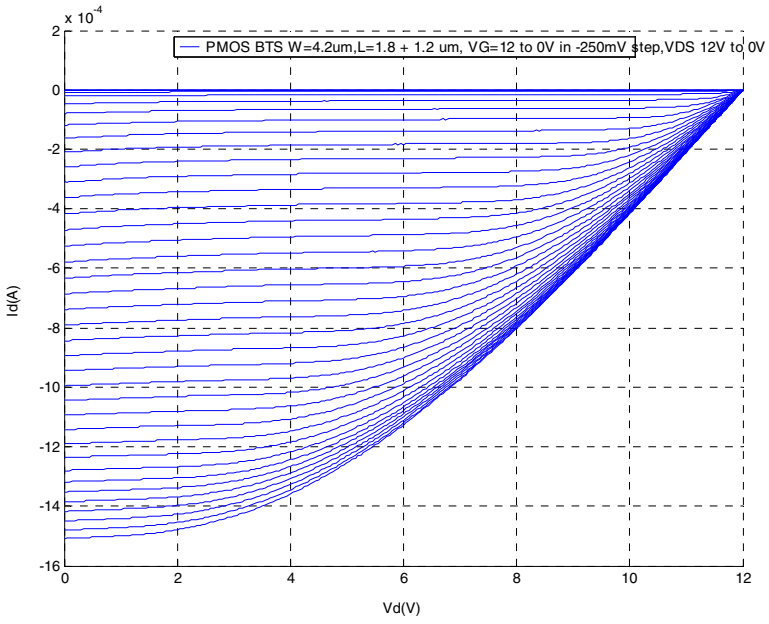


Figure 3. 11 ID-VDS characteristics of High voltage transistors W/L=3/1.8, LDD=1.2um, LDD PMOS BTS at 25^{o} C.

The ID-VDS characteristics of an S/D block Transistor is as shown in Figure 3.12. It can be seen that they can be withstand voltages up to 8V without breakdown, however with very poor conduction. For better transistor action LDD transistors are always recommended over S/D block transistors owing to the higher switching resistance and lower current drive characteristics of S/D block transistors. The use of these S/D block transistors is suggested in processes only in a case where process limitations refrain one from the fabrication and usage of LDD transistors.

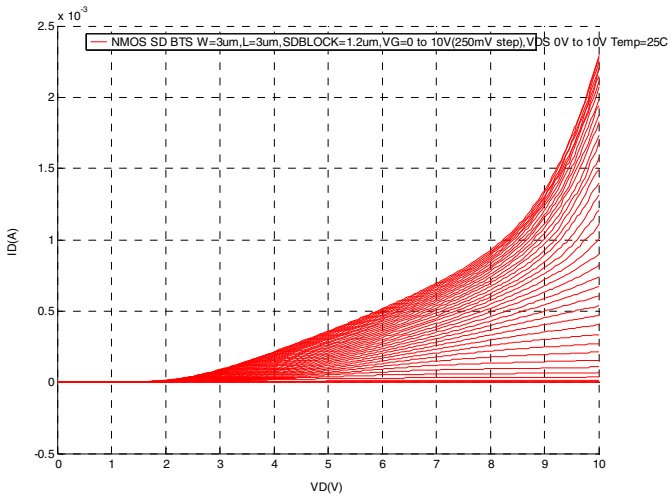


Figure 3. 12 ID-VDS characteristics of High voltage transistors S/D Block NMOS W=3 um, L=3 um and L of S/D Block =1.2 um at 25^{o} C.

3.6 Conclusions and Comments:

The transistors that can survive higher operating voltages were successfully fabricated and tested. Suppression of *"kink effect"* was also observed. However the LDD transistors have a 50% lower f_T (unity gain frequency) because of the added gate capacitance of the LDD section. The calculated f_T was to be 326 MHz for a ΔV =300 mV

verses 596 MHz for a regular RN device at L equal 1.8um. It was also observed that the S/D Block transistors have a very high switch on-resistance compared to their LDD counterparts and function poorly. However, use of these transistors is suggested only when process limitations do not allow the fabrication and usage of LDD transistors (not the case in Peregrine process). All the LDD and S/D block devices were fabricated without design rule violations in both the body tied and untied version. Body tied versions demonstrated little if any improvement over the untied. As a result the body tied versions are not recommended. The process limitations do not allow fabrication of PMOS S/D block transistors.

Chapter 4

Characterization and Analog and Digital Models for Temperatures 120^{o}C to 200^{o}C

4.1 Why separate Analog and Digital Models:

Majority of present semiconductor sales are in digital CMOS circuits, so the traditional modeling efforts are biased towards better models for digital circuits rather than analog. From this point onwards the models that are developed for accurate digital simulation will be referred to as *digital models* and those for analog will be referred to as *analog models*. Studies have proven that exact capacitance and drive current models are sufficient to predict an accurate switching of an inverter [30]. This kind of fitting does not result in good estimation of small signal parameters used in analog design.

In this work modeling efforts were performed to extract and optimize the parameters for four different kinds of transistors, NMOS Low and HighVt and PMOS Low and HighVt. Since most of the circuits developed by the MSVLSI group are for high temperature down hole applications this effort was mainly focused on extracting accurate models over the temperature range of 120°C to 195°C. Six models were extracted two of which were digital models of NMOS & PMOS HighVt devices and the remainder were analog models of NMOS High and LowVt, PMOS HighVt & LowVt.

4.2 Temperature modeling:

The major transistor parameters that change with temperature are threshold voltage, mobility, saturation velocity and series resistance. Shown below in Table 4.1 are the BSIM3SOI model equations [24] showing the temperature dependence of these parameters.

Table 4. 1 BSIM3SOI temperature dependence model equations.

BSIMSOI Parameter	Equation of Temperature dependence
Threshold Voltage	$V_{th(T)} = V_{th(Tnom)} + (K_{T1} + K_{t1l}/L_{eff} + K_{T2}V_{bseff})(T/T_{nom} - 1)$
Mobility, μ_o	$\mu_{o(T)} = \mu_{o(Tnom)}\left(\frac{T}{T_{nom}}\right)^{\mu te}$
Saturation velocity, v_{sat}	$v_{sat(T)} = v_{sat(Tnom)} - A_T(T/T_{nom} - 1)$
Parasitic resistance per unit width, R_{dsw}	$R_{dsw(T)} = R_{dsw(Tnom)} + P_{rt}\left(\frac{T}{T_{nom}} - 1\right)$
First order mobility degradation coefficient, U_a	$U_{a(T)} = U_{a(Tnom)+}U_{a1}(T/T_{nom} - 1)$
Second order mobility degradation coefficient, U_b	$U_{b(T)} = U_{b(Tnom)+}U_{b1}(T/T_{nom} - 1)$
Body-effect of mobility degradation coefficient, U_c	$U_{c(T)} = U_{c(Tnom)+}U_{c1}(T/T_{nom} - 1)$

It can be observed that all these are functions of (T/T_{nom} -1). To make modeling easier and to remove the possibilities of having to model any non-linearities that might exist on a larger range of temperature, a temperature span of 120°C to 195°C with a T_{nom} of 120°C was chosen.

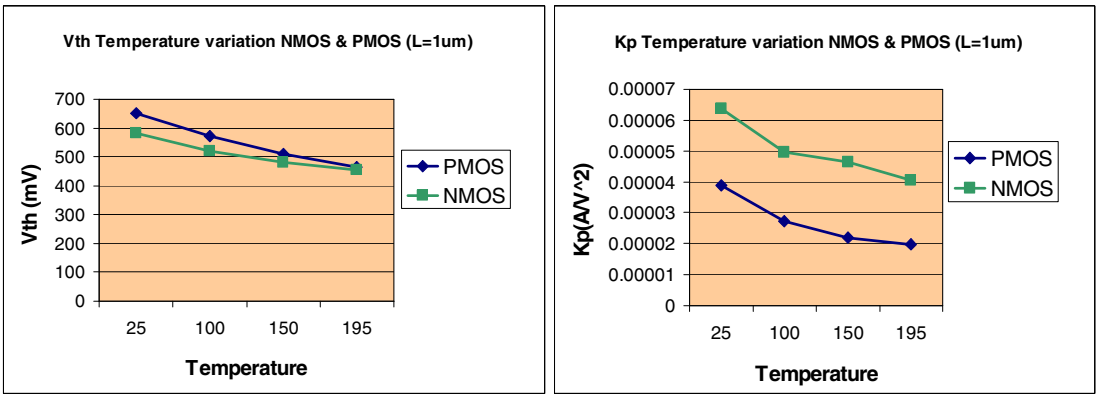


Figure 4. 1 Variation of threshold voltage and current factor with temperature (25 °C to 195 °C) for NMOS and PMOS with L=1um.

Shown in Figure 4.1 are the variations of V_{th} and K_p with temperature for L=1um NMOS and PMOS devices. The threshold voltage temperature coefficients were found to be 0.75mV/°C and 1.1mV/°C for NMOS and PMOS respectively. Current factor was found to be degrading at exponential rate of -1.11 and -1.51 for NMOS and PMOS respectively.

4.3 Requirements of a Digital model:

Digital circuits are almost always optimized for some combination of high speed and low power. The main transistor characteristics that determine speed are the drive strength, transistor ON-resistance and the load capacitance. As temperature increases the threshold voltage decreases and standby power which is dominated by the drain to source leakage currents (Sub-threshold in SOS) increases. Therefore an accurate sub-threshold

model is required to estimate leakage power consumption. A good digital model is one which accurately models the threshold voltage, off currents, on currents and delays across a wide range of input rise times and as a result must model device parasitics as well.

Shown below in Figure 4.2 are the Id-VDS characteristics plotted from measured data and using vendor supplied models for a HighVt NMOS with L=1um at 120°C and 195°C.

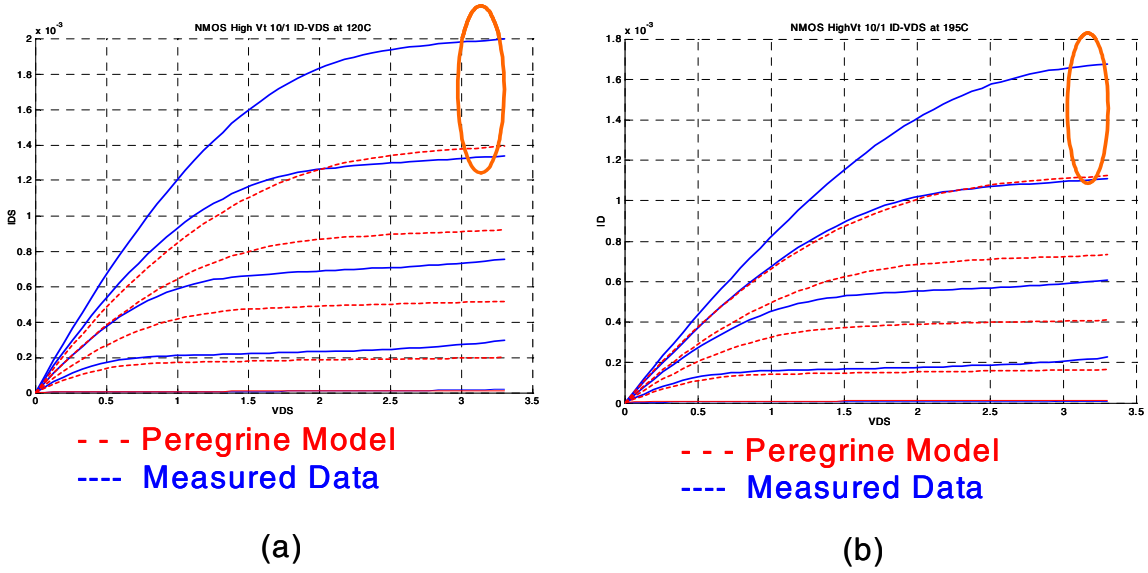


Figure 4. 2 Measured and simulated (Peregrine model) ID-VDS characteristics of HighVt NMOS with W/L=10/1, VDS=0 to 3.3V, VGS = 0.68V to 3.3V in 5 steps at (a) 120°C and (b) 195°C.

Shown below in Figure 4.3 are the Id-VGS characteristics plotted from measured data and using vendor supplied models of a HighVt NMOS with L=1um at 120°C and 195°C.

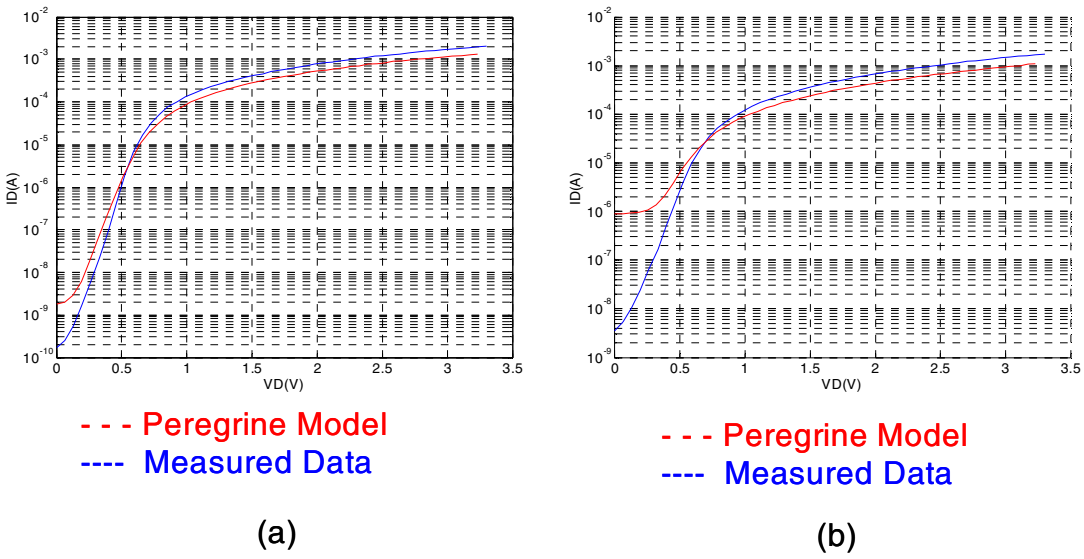


Figure 4. 3 Measured and simulated (Peregrine model) ID-VGS characteristics of HighVt NMOS with W/L=10/1, VDS=3.3 at (a)120 ^{o}C and (b)195 ^{o}C.

From Figure 4.2 and Figure 4.3 it can be observed that the model does not model I_{ON}, the drive strength and I_{OFF}, or the sub-threshold current well. The usage of these models to estimate static and dynamic power dissipation and propagation, rise, and fall time delays of digital circuit would result in gross unacceptable errors.

4.4 Requirements of an Analog Model:

The main parameters of interest in analog circuits are gain and bandwidth which are translated to; parasitic capacitances, g_m and g_{ds} in terms of transistor parameters. The small signal parameters g_m, g_{ds} are defined in Equations Equation 4.1 & Equation 4.2. Transconductance g_m is defined as the increase in drain current with increase in gate-source voltage

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=const} \tag{4.1}$$

Drain Transconductance is a measure of drain current increase with the increase in drain-source voltage

$$gds = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}=const} \tag{4.2}$$

From Figure 4.4 and Figure 4.5 it can be observed that fitting is not acceptable for I_d -V_{gs} characteristics and g_m in the saturation region. In Figure 4.6 variation of g_{ds} for different overdrive voltages is plotted in a log plot. Note, the log plot tends to mask the true variation in g_{ds}. Even though the currents match to a certain extent it can be observed that the there again is significant difference in the g_{ds} between the simulation and measurement data especially due to insufficient modeling of kink. The model used for 'simulation was supplied by the vendor. The "kink" inaccuracies in g_{ds} modeling exist as a result of the Bsim3 model being used to model a SOS process in lieu of BsimSOI.

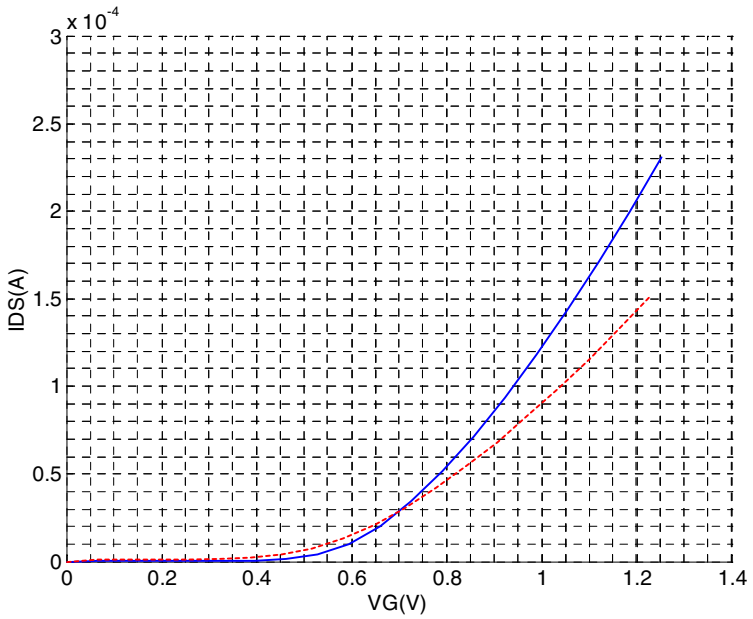


Figure 4. 4 Comparison of Id Vs Vgs of measured and simulated data of NMOS High Vt, (W/L=10/1 at 120°C, VDS=1.2V, VGS=0 to 1.2V) for the analog region of operation.

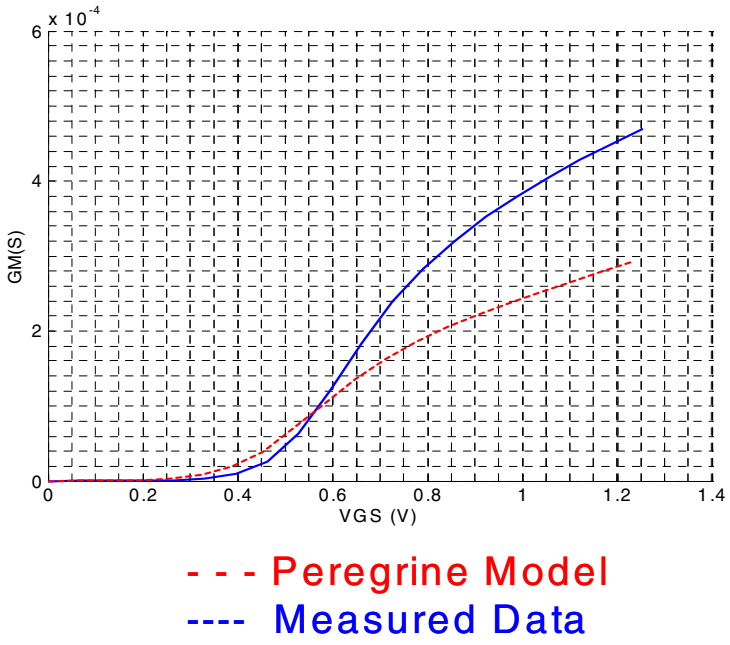


Figure 4. 5 Comparison of gm of measured and simulated data of the NMOS High Vt, (W/L=10/1 at 120°C, VDS=1.2V, VGS=0 to 1.2V) for the analog region of operation.

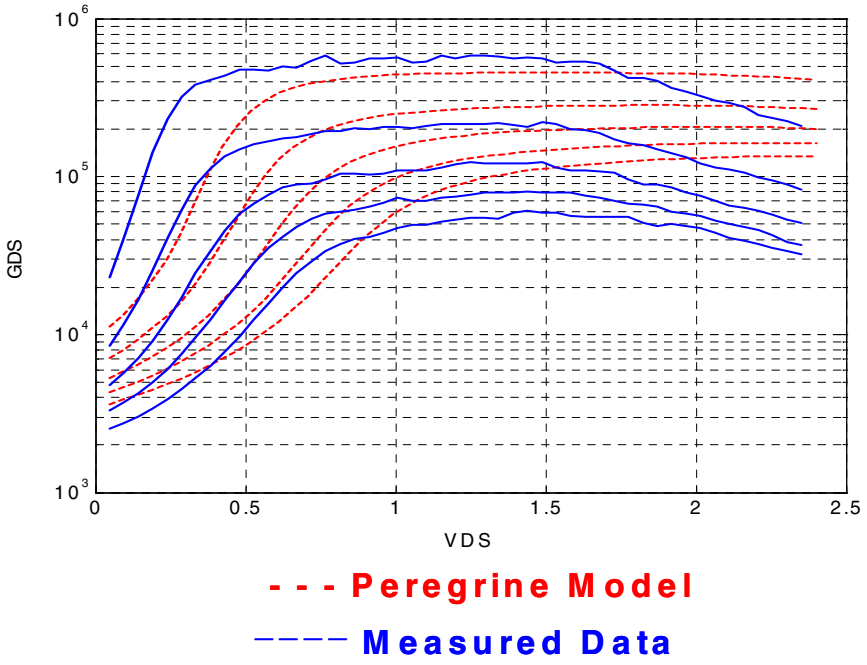


Figure 4. 6 Comparison of gds of measured and simulated data of NMOS High Vt, (W/L=10/1 at 120^{o}C, VDS=1.2V, VGS=0.7 to 1.2V) for the analog region of operation.

From Figure 4.4, Figure 4.5 and Figure 4.6 it can be observed that the vendor supplied does not satisfy the needs for accurate analog simulation.

4.5 Model Extraction:

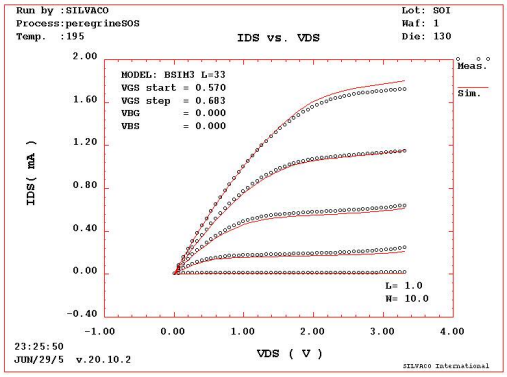
From the above discussion it is clear that the BSIM3 models provided by the vendor do not meet the requirements for either analog or digital simulations. Extracting a single model that suits both analog and digital simulations is complicated if not impossible. So, in this work separate models for both digital and analog were extracted. Extraction and optimization of model parameters for digital models was mainly done on triode region ID-VGS (for accurate on-resistance modeling), Sub-threshold region (for accurate leakage power estimation), and ID-VDS characteristics (for accurate drive strength modeling). In the case of analog model the optimizations were performed on small signal parameters like g_m and g_{ds}. Shown below in Table.1 are the geometries of transistors used in the extraction process.

Table 4. 2 Geometries of transistors used for model extraction.

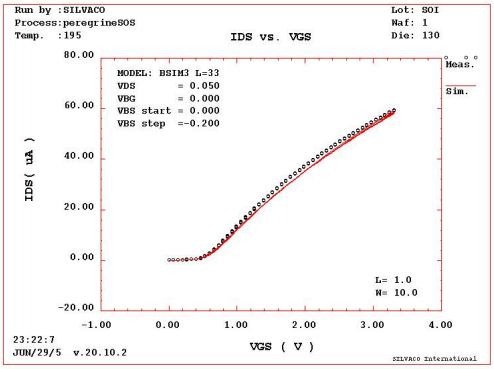
	W(um)	L(um)
1	20	20
2	20	10
3	3.2	10
4	20	0.8
5	10	1
6	10	2
7	10	20

Model extraction and optimization methods used in this study were based on BSIM3SOI user manual [24] and Silvaco manuals [25] [26]. Given below in Figure 4.7 and Figure

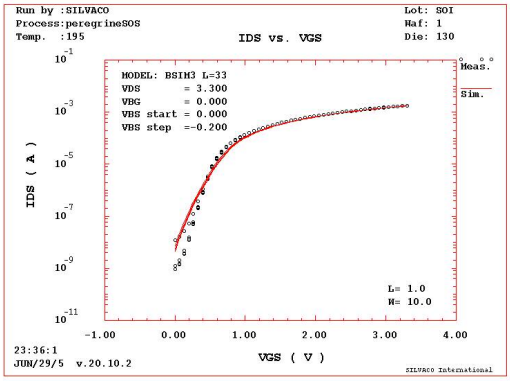
4.8 are the simulations (using extracted model) and measured data of the digital models overlaid in the same plots. As the device capacitance parasitics are relatively independent of temperature the extracted models use the capacitance parameters from the existing vendor supplied models.



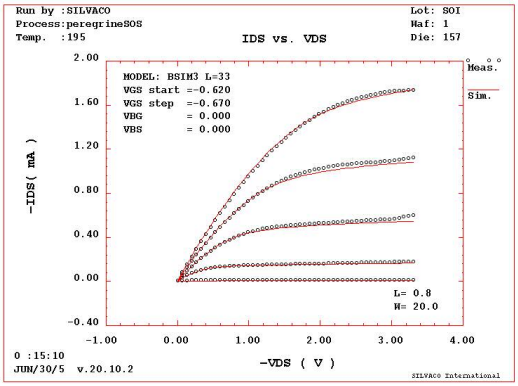
(a) NMOS High Vt, 10/1, Temp=195°C, ID-VDS



(b) NMOS High Vt, 10/1, Temp=195°C, ID-VGS (Triode)

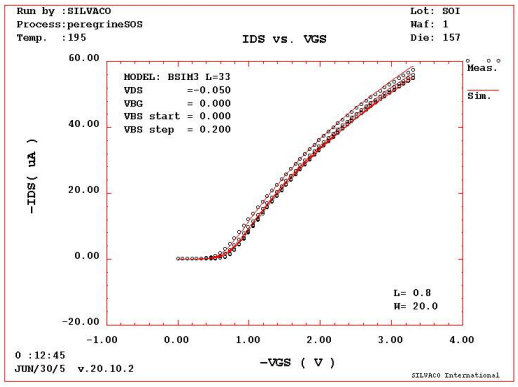


(c) NMOS High Vt, 10/1, Temp=195°C, ID-VGS (Saturation)

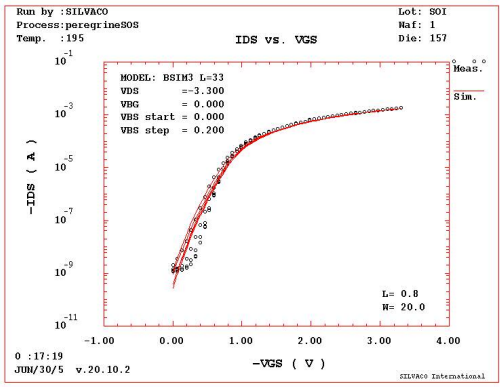


(d) PMOS High Vt, 20/0.8, Temp=195°C, ID-VDS

Figure 4. 7 Simulated (using extracted model) and measured ID-VDS, ID-VGS (Triode & Saturation) curves -- transistor geometries are noted on the figures.



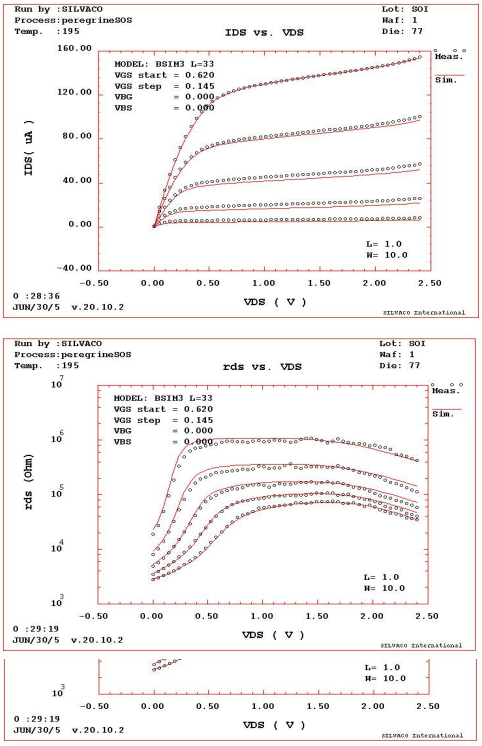
(a) PMOS High Vt, 20/0.8, Temp=195°C, ID-VGS (Triode)



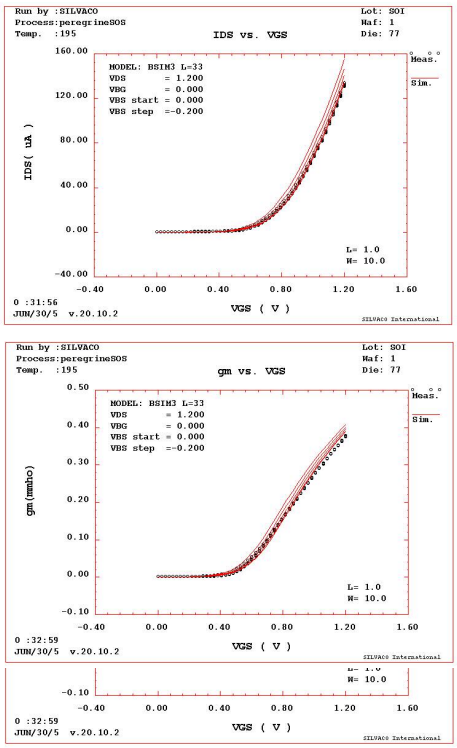
(b) PMOS High Vt, 20/0.8, Temp=195°C, ID-VGS (Saturation)

Figure 4. 8 Simulated (using extracted model) and measured ID-VGS (Triode & Saturation) curves -- transistor geometries are noted on the figures.

It can be observed from Figure 4.7 and Figure 4.8 that requirements for a digital model are accomplished in the extracted models for both NMOS and PMOS. Given below in Figure 4.9 and Figure 4.10 are the characteristics showing small signal parameters g_m and g_{ds} of NMOS and PMOS.

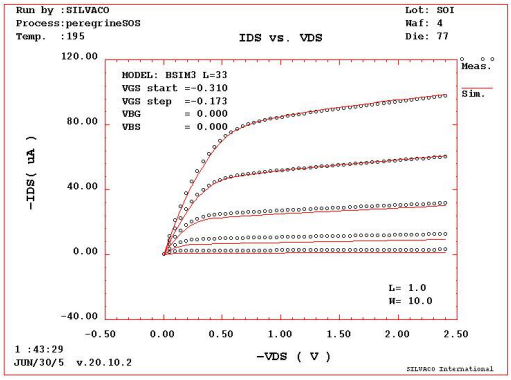


(c) NMOS High Vt, 10/1, Temp=195°C, rds-VDS

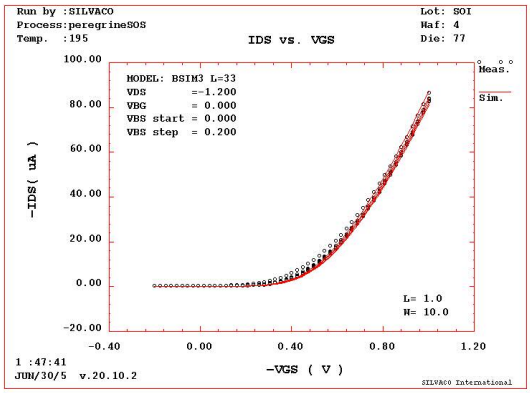


(d) NMOS High Vt, 10/1, Temp=195°C, gm-VGS (Saturation)

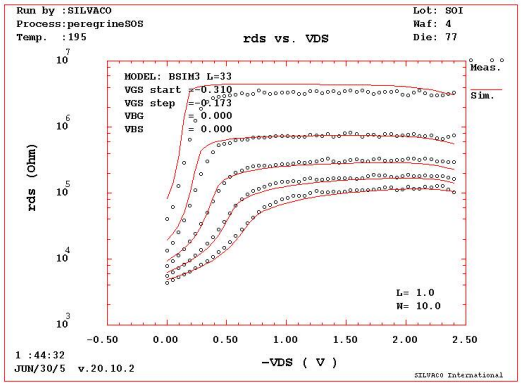
Figure 4. 9 Simulated (using extracted model) and measured ID-VDS, rds-VDS, ID-VGS (Saturation), gm-VGS (Saturation) curves for NMOS -- transistor geometries are noted on the figures.



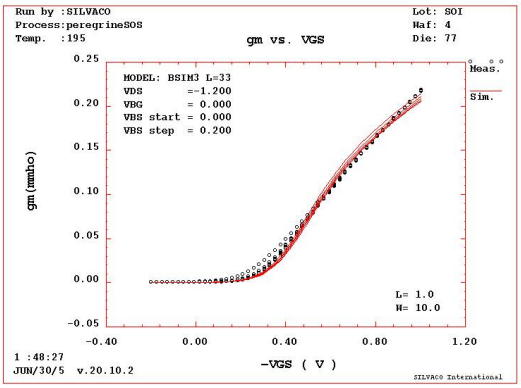
(a) PMOS High Vt, 10/1, Temp=195°C, ID-VDS



(b) PMOS High Vt, 10/1, Temp=195°C, ID-VGS (Saturation)



(c) PMOS High Vt, 10/1, Temp=195°C, rds-VDS



(d) PMOS High Vt, 10/1, Temp=195°C, gm-VGS (Saturation)

Figure 4. 10 (using extracted model) and measured ID-VDS, rds-VDS, ID-VGS (Saturation), gm-VGS (Saturation) curves for PMOS -- transistor are noted on the figures.

From Figure 4.9 and Figure 4.10 it can be observed that the requirements for a good analog model have been accomplished in this extracted model.

Comparison of Figure 4.9 and Figure 4.10 reveals that the PMOS has a reduced kink effect (the kink starts at a higher voltage, 2.2 V, for PMOS) than NMOS. This is attributed to the two reasons mentioned below

- Impact Ionization probability of holes is less than that for electrons [27]

- The existence of better (lower resistance) body contact in PMOS than in NMOS [28]

Figure 4.11 shows the ID-VGS characteristic of a PMOS long channel transistor. ID is shown on log-scale for convenience.

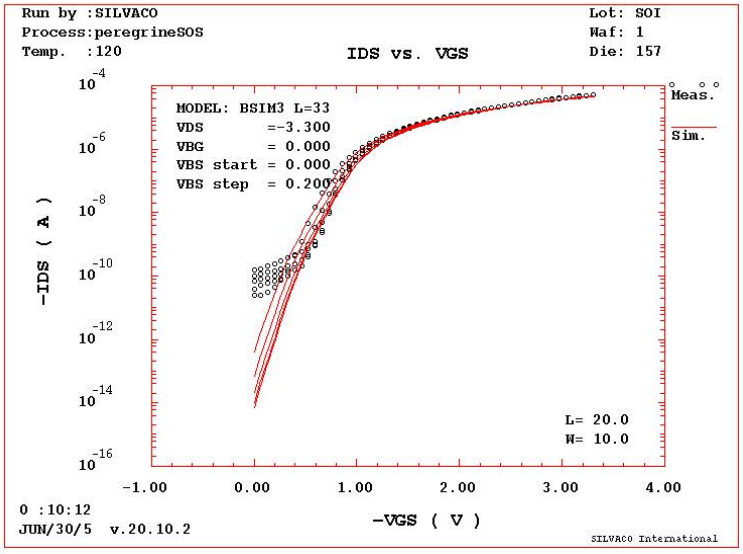


Figure 4. 11 ID-VGS of PMOS High Vt, W/L=10/20, Temp=120^{o}C, VDS=3.3V, VGS=0 to 3.3V.

From Figure 4.11 it can be observed that currents in the sub-threshold region are not modeled very well. The bending of the curves near zero gate voltages is due to GIDL [29] (Gate Induced Drain Leakage). GIDL is not modeled in BSIM3SOI model which explains the poor fit.

Chapter 5

Architecture of 8KX8 MRAM and design of Sense Amplifier:

5.1 Introduction:

MRAM (Magneto-resistive Random Access Memory) combines the best of attributes of all three memories types; the density of DRAM, the speed of SRAM and the non-volatility of Flash [32]. MRAM memory storage is based on the principle of magnetic moments rather than charge storage. In MRAM energy is required to read/write a bit but not to maintain it. The basic MRAM cell used in this work is based on a pseudo-spin valve (PSV) mechanism. The basic structure of a PSV cell is as shown in Figure 5.1. It consists of a magnetically soft layer (requires lower fields for magnetic polarization reversal) on the top and a magnetically hard layer (requires higher fields for magnetic polarization reversal) on the bottom.

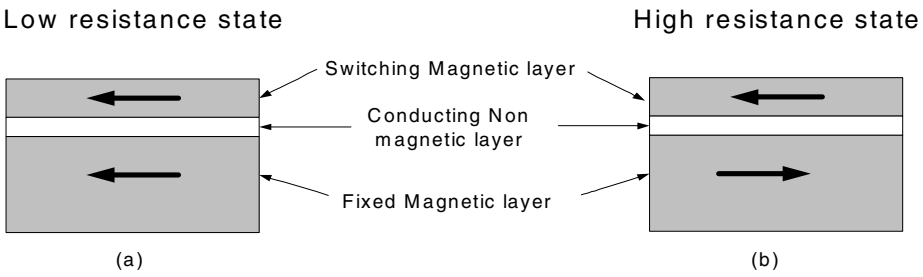


Figure 5. 1 Pseudo-Spin Valve structure (a) Low resistance state (b) High resistance state.

These two are separated by a thin conducting but non-magnetic material. The thickness of the top and bottom layers determines the field required to switch them. The resistance through the cell is low when the magnetization states are in parallel and high when they are in anti-parallel. From a circuit designer's perspective this means that there is a cell whose resistance is determined by the value of the bit stored in it.

5.2 Architecture of 8KX8 MRAM:

Each MRAM cell consists of four Magneto-resistors and one transistor. This whole structure is termed as a spot. The arrangement is as shown in Figure 5.2. Each magneto resistor has a resistance of 120Ω. The processes of writing a '1' or a '0' and reading involve currents in both column and word lines and the selection of spot transistor. The requirements for writing being word line current of +/- 30mA (Opposite polarities for programming a '1' or a '0') and a column line current of +4mA (unidirectional). For reading we need a -15mA word line current and a 2mA column line current. For successful operation of MRAM, all these currents cannot deviate above 10% over the whole temperature range. All these programming and reading currents are obtained from a single temperature independent constant current generator. The change in resistance

from a ‘1’ to a ‘0’ is almost 3% of the magneto resistance. To enhance the signal, two adjacent bits will be programmed with opposite polarities. Figure 5.3 shows the original 8-bit data (column K bits) to be written and its complementary 8-bit data (column KBar bits).

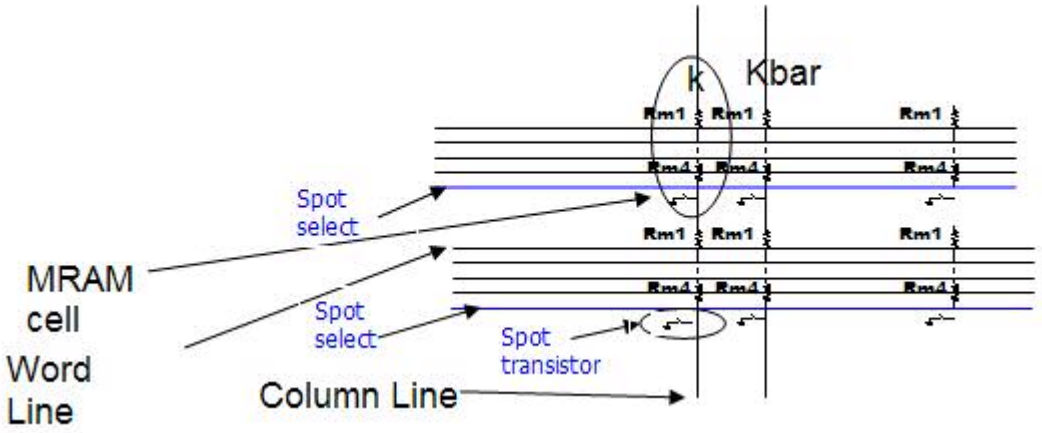


Figure 5. 2 Cell arrangement of Magneto-resistors.

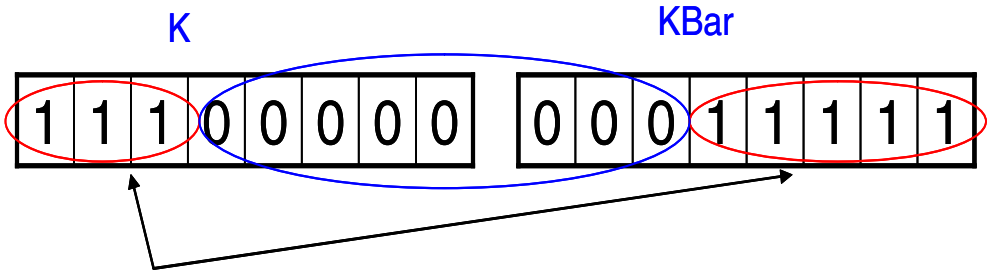


Figure 5. 3 Example showing original (column K) and complementary bits (column KBar).

The programming of ‘K’ and “KBar’ bits requires two programming clock cycles, one for writing all the ‘1’s and another for all the ‘0’s. The advantage of this architecture is a doubling of the signal and the disadvantage being a double the area.

The optimum number of rows and columns in each bank was calculated by equating the time constants for read and write currents across the chip. The capacitance

of the routing wires was assumed to be mainly dominated by the fringe capacitance between adjacent wires than by the capacitance to the substrate. The architectural block diagram is as shown in A.2 of Appendix A. During the write and read procedures in MRAM the word currents and column line currents are brought up sequentially to avoid any accidental programming if either one or both of them overshoots. A model for the MRAM cell was developed in Verilog-A and was used in cadence simulations for verification of programming and reading. The Verilog-A code is presented in Appendix A.1.

5.3 Read Operation Details:

5.3.1 Sense Amplifier Design:

The change in resistance of the magneto-resistor from its original value to '1' or a '0' is 3% with a temperature coefficient of 1000ppm /°C). A sense amplifier was designed to meet this accuracy requirement. This sense amplifier was designed to accept differential inputs and produce a single-ended logic level equivalent output and was designed to run at a clock frequency of 2 MHz. The amplifier consists of two stages. The first stage is an auto-zeroing high gain current amplifier and the second stage is a self-biased voltage amplifier. The complete process of sensing is achieved in one clock cycle. The first stage is auto-zeroed during the negative half cycle of the clock (CLK) and used to sense data during positive half cycle. The inputs to this circuit are intended to be directly connected to MRAM columns as shown in Figure 5.4. Since no actual MRAM

memory array was fabricated, resistors controlled by switches were used in testing and Verilog-A models were used in simulation.

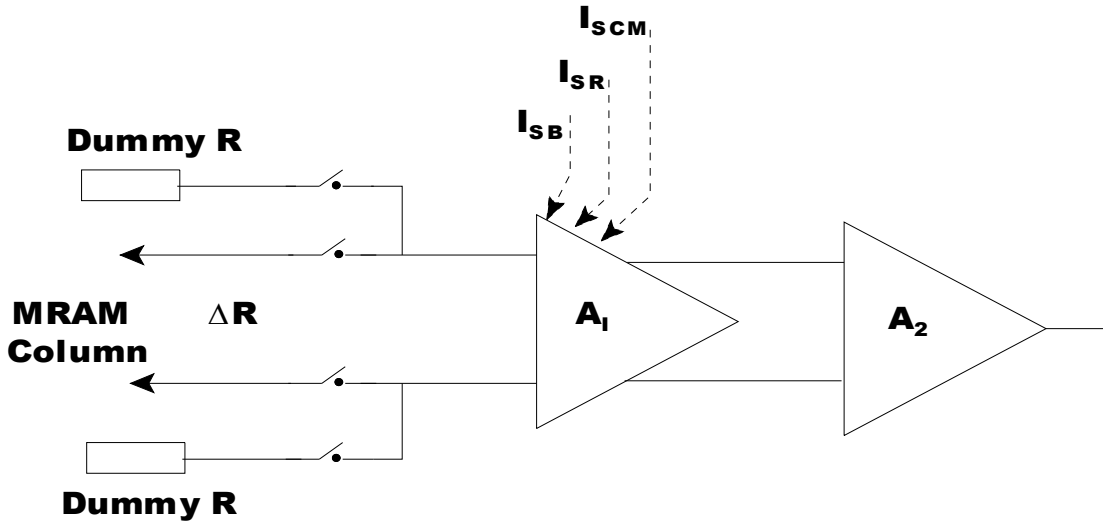


Figure 5. 4 Block diagram of sense amplifier.

The currents flowing into the resistors cannot exceed 2mA over the entire temperature range as dictated by the requirements to ensure safe reading while avoiding any accidental writes. A temperature independent constant current generator was proposed and is as shown in Figure 5.5. This circuit provides currents for the bias generator, CMFB (common-mode feedback circuit), read and write word/column currents.

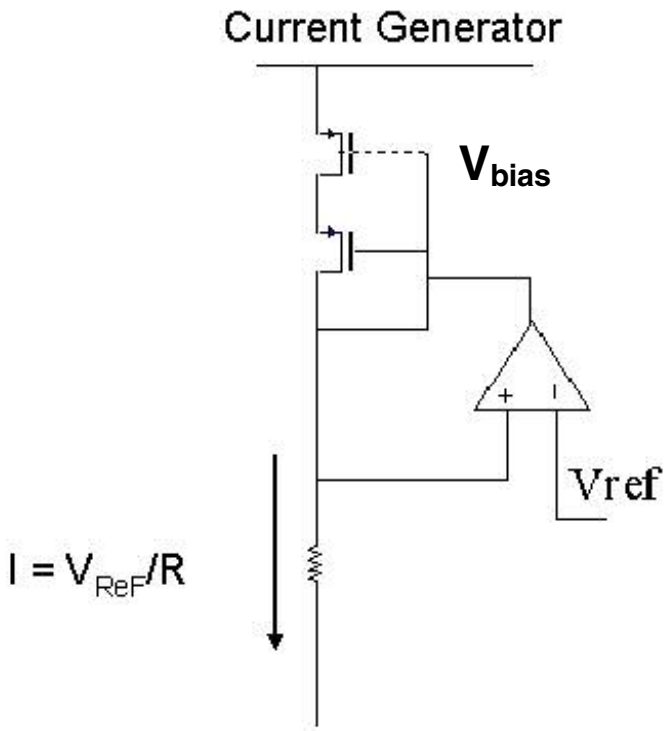


Figure 5. 5 Temperature independent constant current generator.

The resistor R in Figure 5.5 is an off-chip resistor selected for very low temperature coefficient. The input 'Vref' would be the output of a temperature independent voltage reference (earlier work done by Jerry Brewer [35]). The feedback operation of the topology in conjunction with the resistor keeps the current constant.

5.3.2 Design of Current Gain Stage:

The first stage of the sense amplifier is as shown in Figure 5.6. It consists of two OTA's used as boost amplifiers, a bias generator and a CMFB circuit. It is biased to allow 2mA of current into the MRAM columns. Common mode voltage is setup at the

inputs of the '*NBoost*' by the voltage drop impressed on the MRAM resistors. The gain is developed expression as follows;

Nominal resistance of MRAM resistors, R_{mem} = 450 Ohms

Bias Current through each leg, I_{Sense} = 2mA

Common Mode voltage at the inputs of *'NBoost'* $V_{mem} = I_{Sense}. R_{mem}$

$$\text{Voltage at node } V_{out} = \Delta I \cdot R_{out} \tag{5.1}$$

Where R_{out} is the output resistance looking into the nodes V_{out} or V_{outBar} . It is the parallel combination of output resistance looking into PMOS and NMOS. The contribution of resistance looking into PMOS is equal to $\frac{\mu 3}{2} \cdot r_{ds}$, where r_{ds} is the output resistance looking into rail side current source and μ is the self gain of the transistor. Since $r_{ds} \geq 40 \cdot R_{mem}$ the contribution of PMOS output resistance to the overall resistance (R_{out}) is negligible.

$$R_{out} = A_{NBoost} \cdot \mu \cdot R_{mem} \tag{5.2}$$

where μ is the self gain of the transistor

'NBoost' is implemented as a folded cascode, so $A_{NBoost} = \mu^2 / 2$

$$Rout = \frac{\mu^3}{2} \cdot R_{mem} \tag{5.3}$$

Due to the complementary values stored in the MRAM bits, the difference of current in the two legs of the sense amplifier is

$$\Delta I = g_m \cdot V_{in} \tag{5.4}$$

$$V_{out} = \Delta I \cdot Rout = g_m \cdot V_{in} \cdot \left(\frac{\mu^3}{2} \cdot R_{mem} \right) \tag{5.5}$$

$$V_{out}=g_m\cdot\frac{\mu^3}{2}\cdot R_{mem}\cdot\Delta R\cdot I_{Sens} \tag{5.6}$$

$$\text{Gain, } A_I=\frac{V_{out}}{\Delta R}=g_m\cdot\frac{\mu^3}{2}\cdot R_{mem}\cdot I_{Sense} \tag{5.7}$$

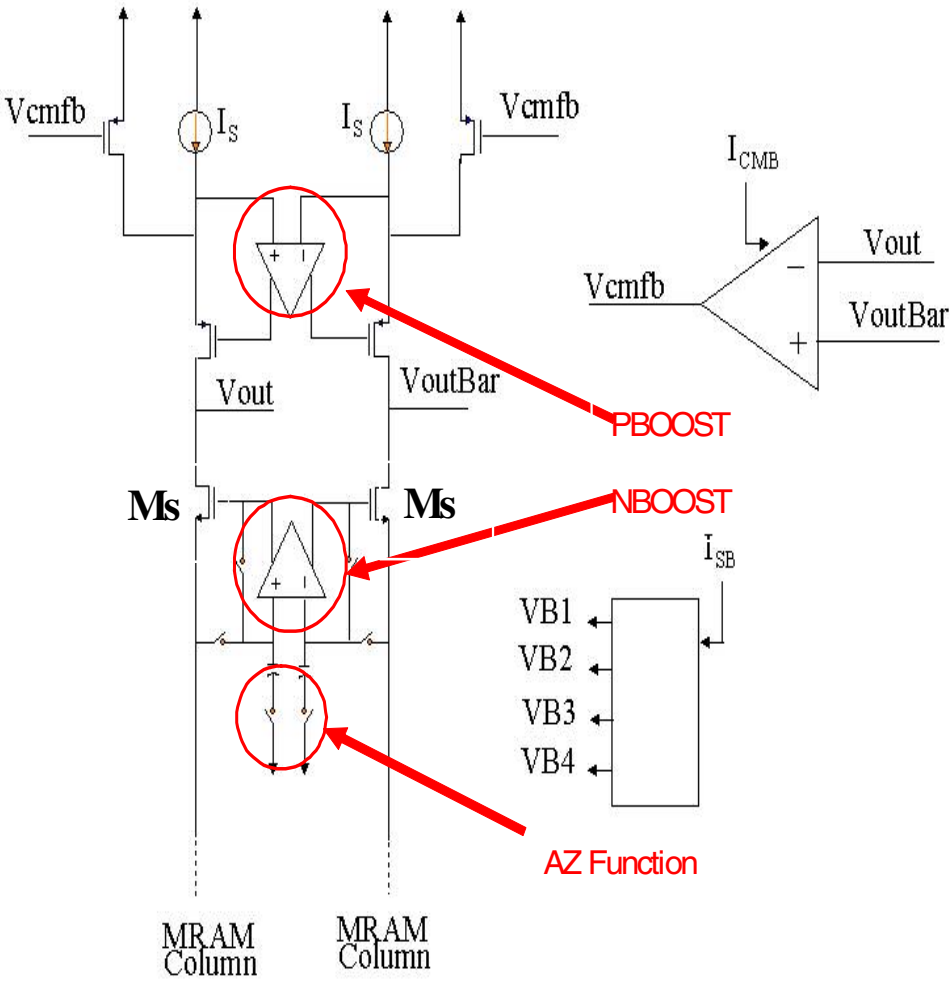


Figure 5. 6 Complete Schematic of first stage of sense amplifier.

5.3.3 Temperature gain sensitivity and overdrive selection:

Shown below in Figure 5.7 is a plot showing the variation of mobility, ΔV and g_m for constant current over the temperature range of 27 ^oC to 223 ^oC. Note that all the values are normalized. It can be observed that g_m changes by 25% from 27 ^oC to 200 ^oC.

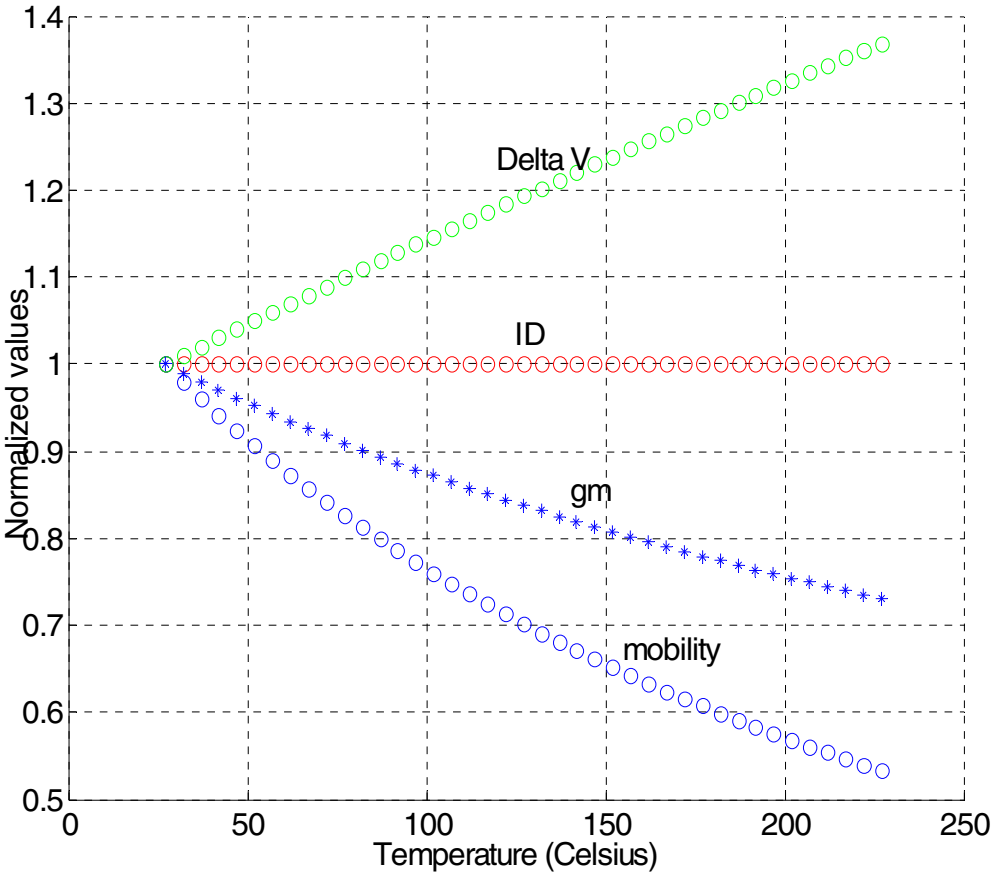


Figure 5. 7 Variation of ΔV , gm , mobility with temperature for constant current.

As can be observed from Equation 5.7 and Figurer 5.7 gain is a function of temperature. The bias current I_{sense} is independent of temperature (set by the constant current generator). g_m is dependent on temperature and changes by 25% over the temperature range. R_{mem} temperature coefficient is negligible (1000 ppm/°C). Self gain of transistor

defined by $\mu = \frac{g_m}{g_{ds}}$ changes by 25% due to the variation of g_m. The g_{ds} term in self gain is constant over the temperature range due to constant I_d.

Since the difference signal current, ΔI = 72uA, a small value the currents due to the mismatch between the two legs should be smaller than this value to guarantee accurate sensing of a "1" or "0".

Substituting the values from Table 2.3, the value of ΔV that would result in obtaining the best performance (Quality factor defined in Equation 2.24)

$$PMOS(PL), \Delta V_{Eff\_Opt} = 2\sqrt{\frac{\sigma^2(\Delta V_{th})}{\sigma^2\left(\Delta\beta/\beta\right)}} = 2\left(\frac{A_{vth}}{A_\beta}\right) = 2\left(\frac{12.5}{0.0775}\right) = 322mV$$

$$NMOS(NL), \Delta V_{Eff\_Opt} = 2\sqrt{\frac{\sigma^2(\Delta V_{th})}{\sigma^2\left(\Delta\beta/\beta\right)}} = 2\left(\frac{A_{vth}}{A_\beta}\right) = 2\left(\frac{11.56}{0.026}\right) = 889mV$$

The values used for NMOS are obtained from measurement of NL devices, but in the circuit implementation, all the rail side transistors (that are mainly responsible for mismatch) are RN devices. So, the above calculated value for NMOS somewhat in error but helpful none the less.

The decision to operate at a ΔV of 450mV has the effect of pushing the amplifier into lower offset operation but off the optimal veff. In this sense amplifier implementation, the power consumption is set at a constant value due the power supply and read current requirements. For this reason, in the quality factor defined in Equation 2.24, the power term can be neglected. Since the main requirements of the amplifier were the reliable sensing of signal at moderate speed (2MHz), low offset is a necessity and was traded off

for speed and reduced area in the case of the PMOS devices. The optimal NMOS veff is unacceptable.

The common mode output voltage for this stage is set by the CMFB circuit which generates V_{cmfb} by comparing V_{out} and V_{outBar}.

5.3.4 Common Mode Feedback Circuit:

As with any other high gain fully differential circuits the sense amplifier also needs common mode feedback to maintain the desired voltage at the output. The common mode feedback circuit using two differential pairs [33]`as shown in Figure 5.8 was used to provide CMFB for the first stage of the sense amplifier. Scaled versions of a similar topology were used in Boost amplifiers. The sources coupled transistors M2-M5 sense the common mode voltage V_{oc} i.e., the average of V_{out} and V_{outBar} and generate the output voltage V_{cmfb} which is proportional to the difference between V_{oc} and V_{ref} [33].

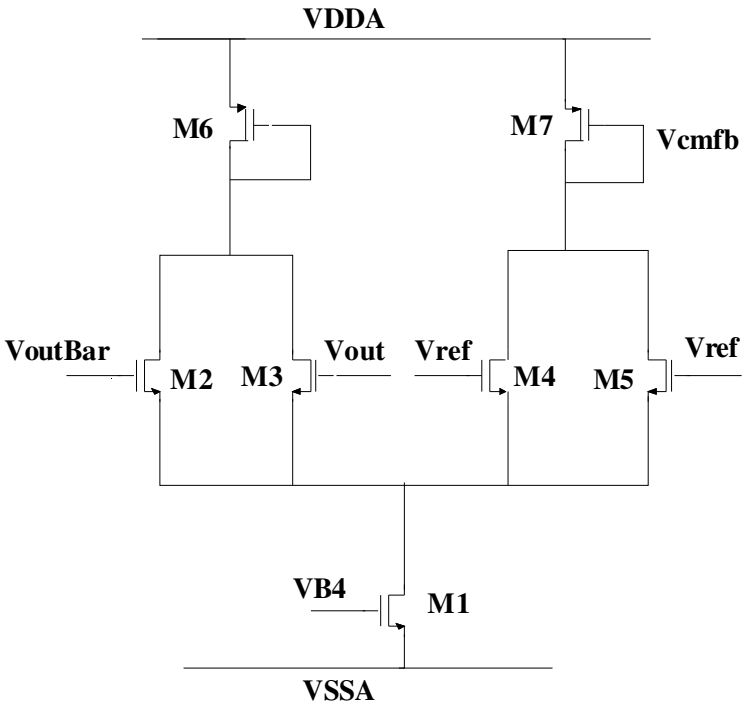


Figure 5. 8 CMFB circuit used in the sense amplifier.

The output V_{cmfb} is feed back to the rail side PMOS transistors of Figure 5.6 completing the feedback loop. This circuit topology loses control if any of the inputs swing low enough to turn off any of the input transistors. For the amplifier in this work, the swing towards the negative rail is limited to a value $I_{Sense}R+\Delta V$ which eliminates the above mentioned limitation.

5.3.5 Boost Amplifiers:

The amplifiers used as 'NBoost' and 'PBoost' were implemented as folded cascode amplifiers.as shown in Figure 5.9.

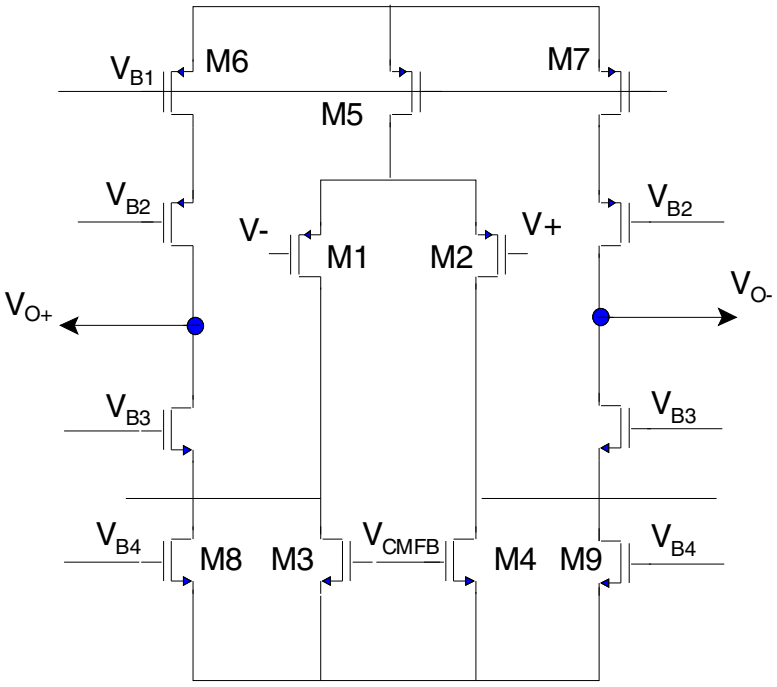


Figure 5. 9 Schematic of amplifier 'NBoost'.

Small signal gain of this circuit,

$$A_v = g_{m1}\{\mu \cdot (r_{o1} \| r_{o3}) \| (\mu \cdot r_{o6})\} \tag{5.8}$$

where μ is the gain of cascode transistor.

Transistors M8, M9, M6, M7 were all long channel transistors with L=2um and the rest of the transistors were with L=1um. The CMFB for this circuit is complementary of the circuit described previous section. The first pole w_{p1} for this amplifier is located at the output node and the second pole w_{p2} is at the cascode transistor biased with VB3.

$$w_{p1} = -\frac{1}{R_{out} \cdot C_L} \tag{5.9}$$

$$w_{p2} = -\frac{g_{m-casc}}{C_{gs-casc}} \tag{5.10}$$

5.3.6 Common Mode Reference Voltages:

Common mode reference voltages were set for the main amplifier at 200mV and at VB2 for the *'PBoost'*. For the '*NBoost*' the reference voltage has to track the MRAM cell resistance. This voltage was provided by the circuit shown in Figurer 5.10 below.

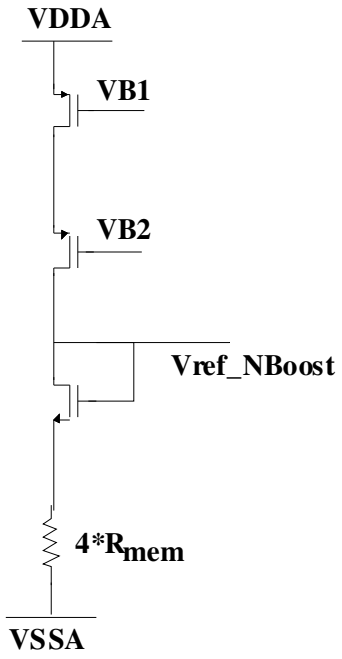


Figure 5. 10 Reference generator for amplifier 'NBoost'.

To reduce the standby power consumption, the current through this reference generator was reduced to $1/4^{th}$ of I_{Sense}. The number of fingers in each of these transistors was reduced to $1/4^{th}$ of their original value and the resistor scaled by 4 times to maintain a similar voltage drop as in the main circuit.

5.3.7 Auto Zero Offset Cancellation:

The resolution of the sense amplifier is determined by the offset inherent in the transistors. The transistors that introduce offset in the main amplifier shown in Figure 5.6 are the rail side PMOS transistors, Ms transistors and the amplifier '*NBoost*'. Since the transistors in *'NBoost'* were scaled ¼ times the transistors in the main amplifier and as a result dominate the offset transistor pairs when compared to the offset generated by rail side PMOS, and Ms transistors and the remaing transistor paris of the '*NBoost*' amplifier. The transistor pairs in *'NBoost'* that affect offset are M1-M2, M3-M4, M6-M7, M8-M9 and the offset generated by the 4 pair of devices is given by Equation.11.

$$V_{OS} = \sqrt{\left(\frac{A_{vt}^{\ 2}}{(W.L)_{M1M2}} + \frac{A_{vt}^{\ 2}}{(W.L)_{M3M4}} + \frac{A_{vt}^{\ 2}}{(W.L)_{M6M7}} + \frac{A_{vt}^{\ 2}}{(W.L)_{M8M9}} \right)} \tag{5.11}$$

To overcome this potential, input series offset cancellation was employed with the simplifed schematic shown in Figure 5.11.

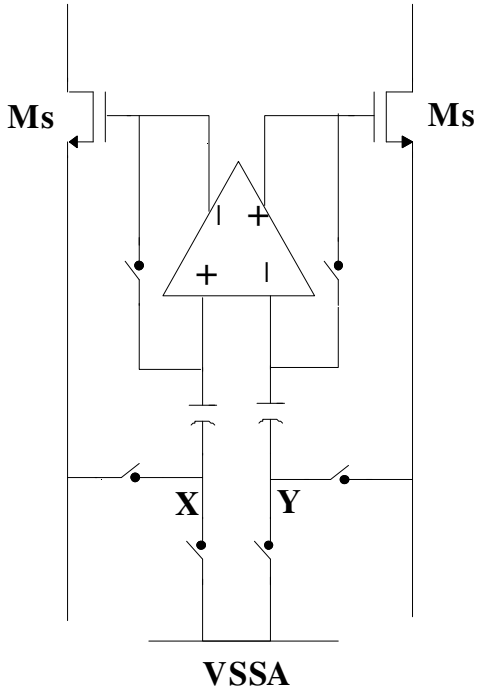


Figure 5. 11 Schematic of Auto-zero offset cancellation technique.

The voltage stored on the capacitor after offset cancellation is as shown in Equation 5.13 where A_V is the gain of the amplifier and V_C the effective charge stored on the capacitors

$$V_C = -A_V [V_C - V_{OS}] \tag{5.12}$$

$$V_C = \left(\frac{A_V}{A_V + 1} \right) \cdot V_{OS} \tag{5.13}$$

From Equation 5.13 it can be seen that the voltage on the capacitor is almost equal to the offset voltage but with opposite polarity. With a projected gain of 300 the anticipated offset Vos after offset cancellation is projected to be 0.01mV.

5.3.8 Design of Self Biased Amplifier:

The second stage of the sense amplifier is needed to introduce additional gain in the path to ensure the output is a logic level. This stage was followed by a chain of two inverters which eventually drove the output to logic levels. A complementary self biased differential amplifier [34] as shown in Figure 5.12 was used as the second stage.

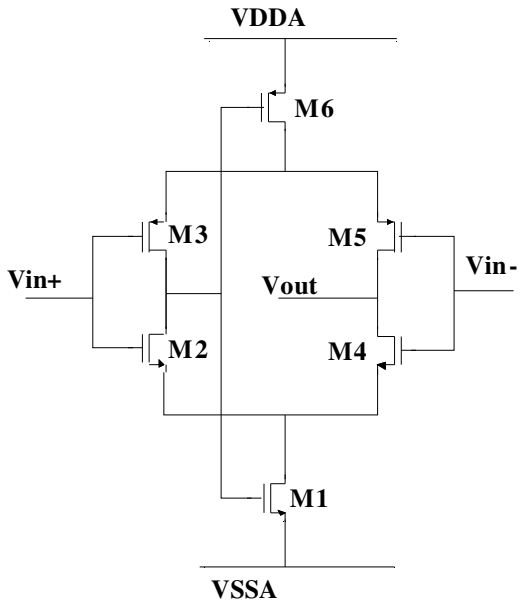


Figure 5. 12 Schematic of complementary self biased differential amplifier.

The negative feedback provides bias voltage to the M1 and M6 thus eliminating any need for external bias. The transistors M1 and M6 operate in linear region having very low standby current when there is no input differential signal and as such make the circuit less power consumptive. When Vin+ goes high it pulls the gate of M6 lower turning it on harder. At the same time Vin- goes low pulling the large current through M5. The amplifier gain is twice that of a single stage 5-transistor differential amplifier with a current source load as a result of the complementary action of NMOS and PMOS pairs. The gain of this amplifier is as shown in Equation 5.15

$$A_V = \frac{g_{mM2} + g_{mM3}}{g_{dsM2} + g_{dsM3}} \tag{5.14}$$

$$A_V = \frac{4(V_{AN} \cdot V_{AP})}{\Delta V(V_{AN} + V_{AP})} \tag{5.15}$$

This amplifier eliminates any need for extra bias voltage routing making the layout more compact.

In Chapter 6, measurement results of the sense amplifier described in this chapter are presented along with simulation results. The measured DC transfer characteristics of Boost amplifiers at 195^{o}C are also presented. Measurement results of sense and auto-zero settling times on 12 dies are presented.

Chapter 6

Test Results and Conclusions

6.1 Introduction:

The sense amplifier test results are reported in this chapter. The test structures consists of two pad frames and are as explained below in sections 6.2 & 6.3. The sense amplifier is two stages consisting of a auto zeroing current amplifier followed by a voltage amplifier. Auto zeroing (AZ) is completed during the clock bar phase of both the read and write cycles. Stage 2 is geometrically small and as a result is followed by an inverting pad driver to drive large load capacitances (co-ax cable and oscilloscope) encountered during testing. During test all circuits were operated with +/-1.65V supplies. The sense amplifier delay is 49.3nS +/-5.85nS for 12 devices with an input of +/- 3 ohms. The design target was sensing +/- 3 ohms at 195 ^{o}C in a half cycle of a 2 MHz clock (250ns). The test setup is explained in 6.3 MRAM Read Operation.

6.2 Boost Amplifiers:

6.2.1 Boost Amplifier Test Circuit pad frame:

This pad frame consists of the two OTA's used as Boost amplifier's in the sense amplifier's first gain stage and the Bias generator. These cells were primarily placed on the wafer for diagnostic purposes. Both boost amplifiers were tested at 195^0C.

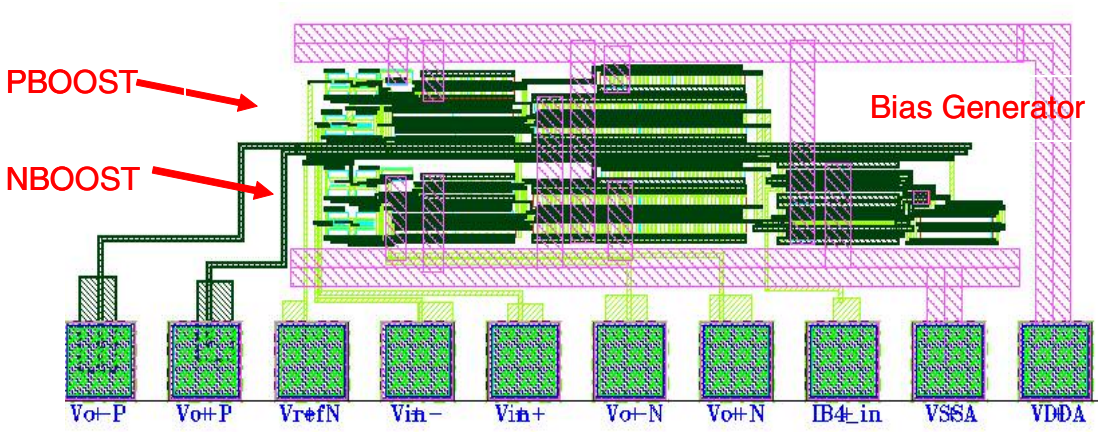


Figure 6. 1 Layout of test pad frame for Boost amplifiers.

6.2.2 Boost Amplifier DC transfer Characteristics and Gain at 195^oC:

The differential inputs for the OTA were provided from the HP 4155 and the outputs were monitored using the same. The common mode level of the inputs was biased at their nominal operating point consistent with their intended use in the sense amplifier. 1.1 to 1.3 V and -0.65 to -0.85 for the Pboost and Nboost respectively.

Test results are shown in Figure 6.3 and Figure 6.4. The measured gains were 300 and 35 for the Nboost and Pboost amps respectively. All amplifiers are measured in the

open loop configuration as shown in Figure 6.2. Both boost OTAs are functional at 195^{o} C. Sense amplifier performance is weakly dependent on Pboost gain while being directly dependent on Nboost gain (5.2.2 Design of current gain stage).

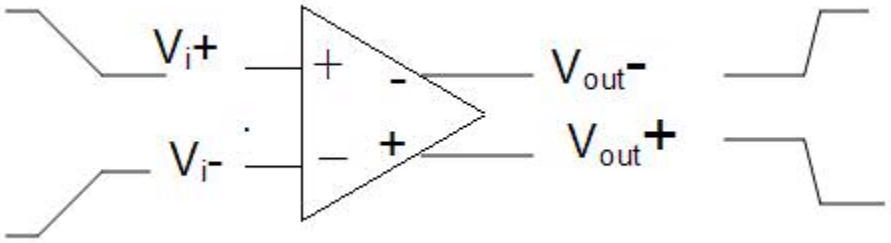


Figure 6. 2 Boost amplifier's test procedure.

6.2.3 NMOS Boost Amplifier:

The DC transfer characteristic and the corresponding gain of the NBoost amplifier measured at 195^{o}C is as shown in Figure 6.3.

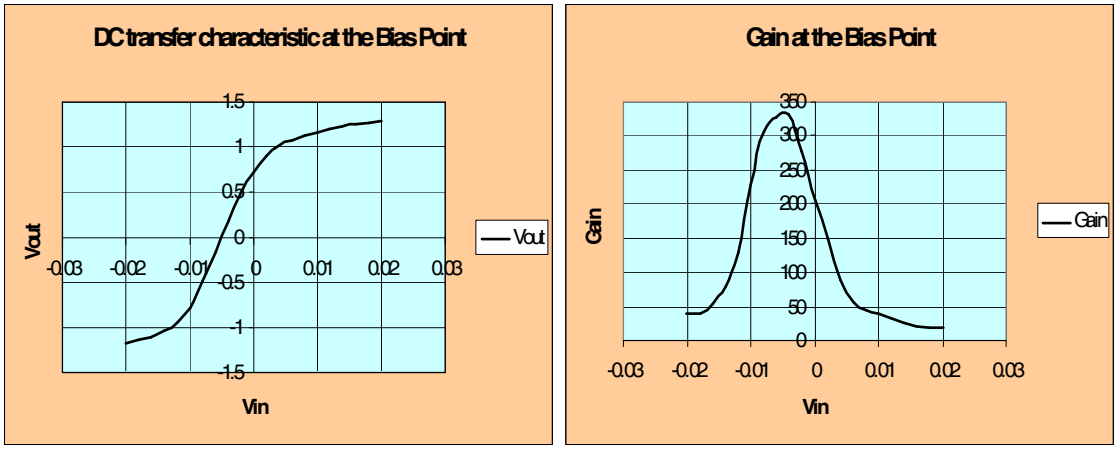
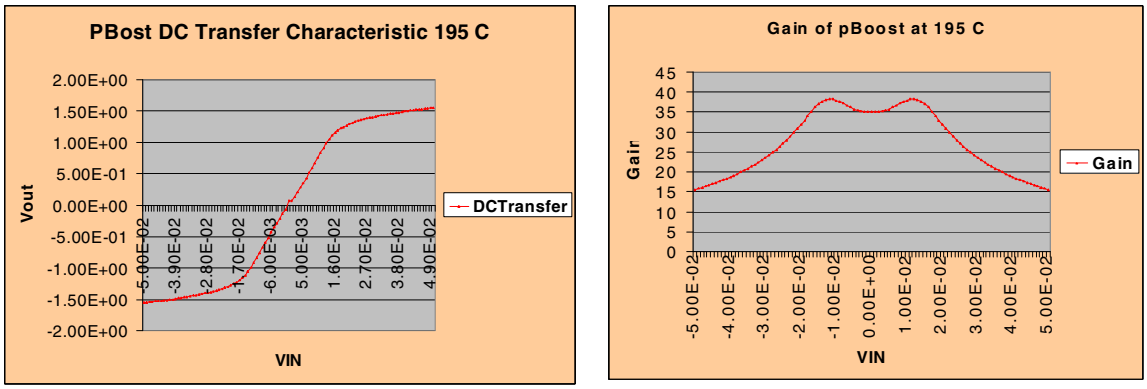


Figure 6. 3 Measured NBoost Amplifier DC transfer characteristics and gain at 195 ^{o}C.

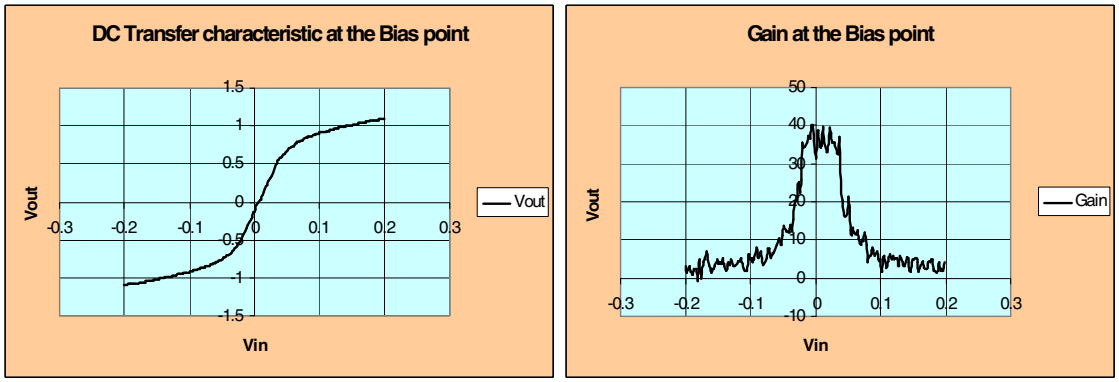
The output common mode voltage of this amplifier is approximately -0.3V (5.2.6 Common mode reference voltages). Since this amplifier is employed as a boost circuit providing gate bias voltages to transistors, the output does not have to swing more than 25mV. From discussion on kink effect in Chapter 3 &4, it is known that NMOS enters kink effect at around 1.5V across drain and source and PMOS at 2.2V. From the amplifier's bias point, lower output swing and above discussion, it can be concluded that none of the transistors enter kink region, which explains the higher gain (A_V>250) achieved as can be observed from Figure 6.3.

6.2.4 PMOS Boost Amplifier:

The DC transfer characteristic and the corresponding gain of the PBoost amplifier simulated and measured at 195^{o}C is as shown in Figure 6.4.



(a)



(b)

Figure 6. 4 (a) Simulated (using MSVLSI models) PBoost Amplifier DC transfer characteristics and gain at 195°C (b)Measured PBoost Amplifier DC transfer characteristic and gain at 195°C.

MSVLSI models (developed in Chapter 4) were used in simulation to obtain the DC transfer characteristic and gain shown in Figure 6.4 (a). It can be observed that the simulation (Figure 6.4(a)) results A_V=35 agree well with the measured (Figure 6.4(b)) results A_V=32. The output common mode voltage of this amplifier is at VB2 (~0.55 V). As explained for the case of Nboost this amplifier also has very small output swings. At the amplifier's bias point the voltage across drain and source of NMOS cascode transistors equals 1.7V forcing them into kink regime which reduces the output resistance thereby reducing the gain. This explains the factor of 10 difference in the gains of Nboost

(A_V>250) and Pboost (A_V=32). It can be observed that inaccurate modeling of kink effect would have resulted in over estimation of gain in this kind of situation.

6.3 MRAM Read Operation:

A detailed flow chart and explanation of the read operation is presented in Appendix B

The timing chart for the read operation is as shown in Figure 6.5.

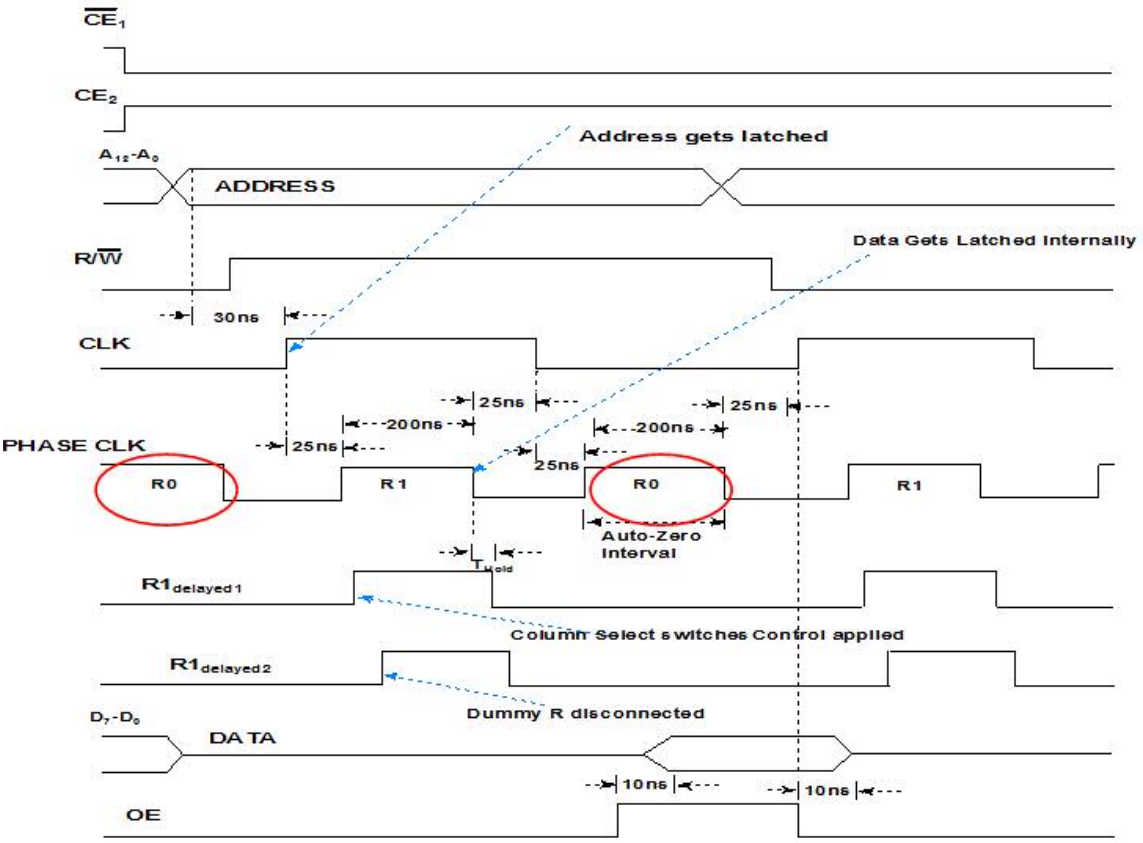


Figure 6. 5 Read operation timing chart.

Points to be noted in Figure 6.5

1. R_0 represents the Auto-Zero interval
2. Actual sensing operation starts at $R_{1delayed2}$

In the test circuit **CE_1**, **CE_2**, **Address**, **R/$\overline{W}$**, **CLK**, **R_1**, **$\overline{OE}$**, **DATA** signals are not provided since their absence would not affect the functionality of the sense amplifier. These logic signals are from MRAM control and have been tested and proved operational by Sameer Kadam. The control signals provided for the test circuit are the phase clocks; $R_{0,}$ $R_{0\ advanced}$, $R_{1\ delayed1bar}$ and $R_{1delayed2}$ and their relative timings are as captured in Figure 6.6. $R_{0advanced}$ leads R_0 to eliminate charge injection from the switch during the Auto-zero phase [36]. R_1 and R_0 clocks are non-overlapping to ensure that sense and read currents do not overlap minimizing any possibility of accidental write if either current were to overshoot. An MRAM write occurs when the combined write and sense currents become sufficiently large.

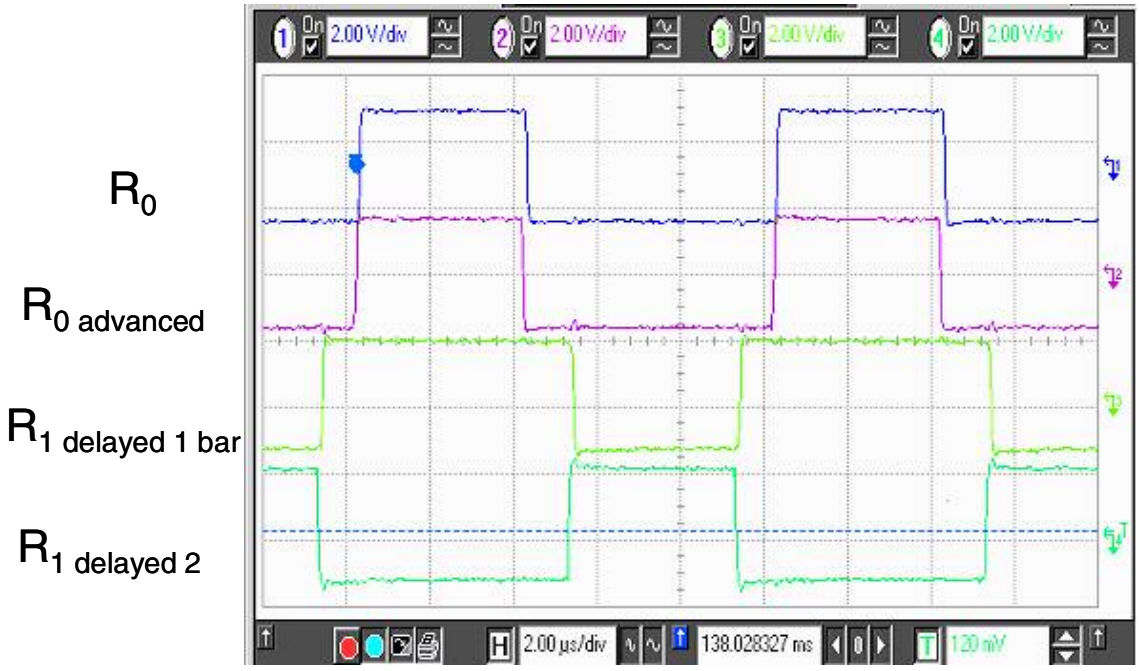
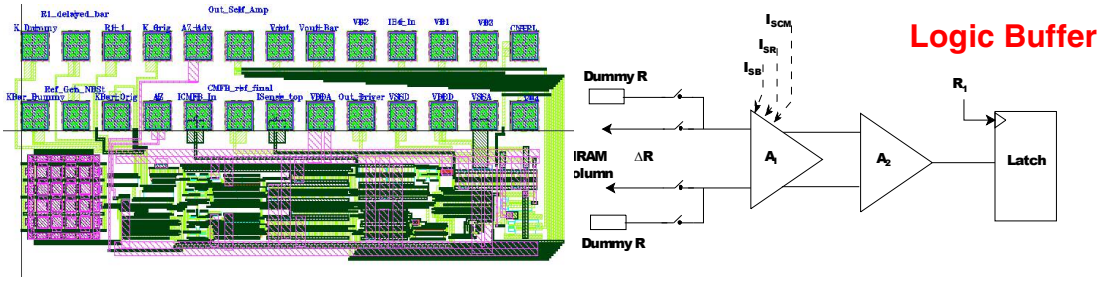


Figure 6. 6 Control Inputs for the sense amplifier during read operation.

Sense Amplifier test pad frame layout & block diagram are shown in Figure 6.7 consisting of the two stage amplifier and the inverting logic buffer. The latch shown in

Figure 6.7(b) is not a part of sense amplifier but is proposed to be used in the 8KX8 MRAM memory for latching of the sensed data.



(a) (b)

Figure 6. 7 (a) Layout of Sense Amplifier test pad frame (b) block diagram.

6.4 Test Results at 195° C:

For twelve die the sense delay for ΔR= +/-3Ω. was measured and recorded for statistical purposes. All dies were found to work successfully at 195° C. Figure 6.8 and Figure 6.9 demonstrate typical transient waveforms (simulated and measured) of V_{out}+ and V_{out}- for an applied ΔR= +/-3Ω. Data is sensed during $R_{1delayed2}$ and is to be latched at the falling edge of R_1(Figure 6.5). V_{out}+ and V_{out}- are the outputs of the stage 1 amplifier. The "logic buffer" or pad driver is not a part of the sense amp and was only added for testing purposes to drive the test setup load. The test setup is as shown in Figure 6.8.

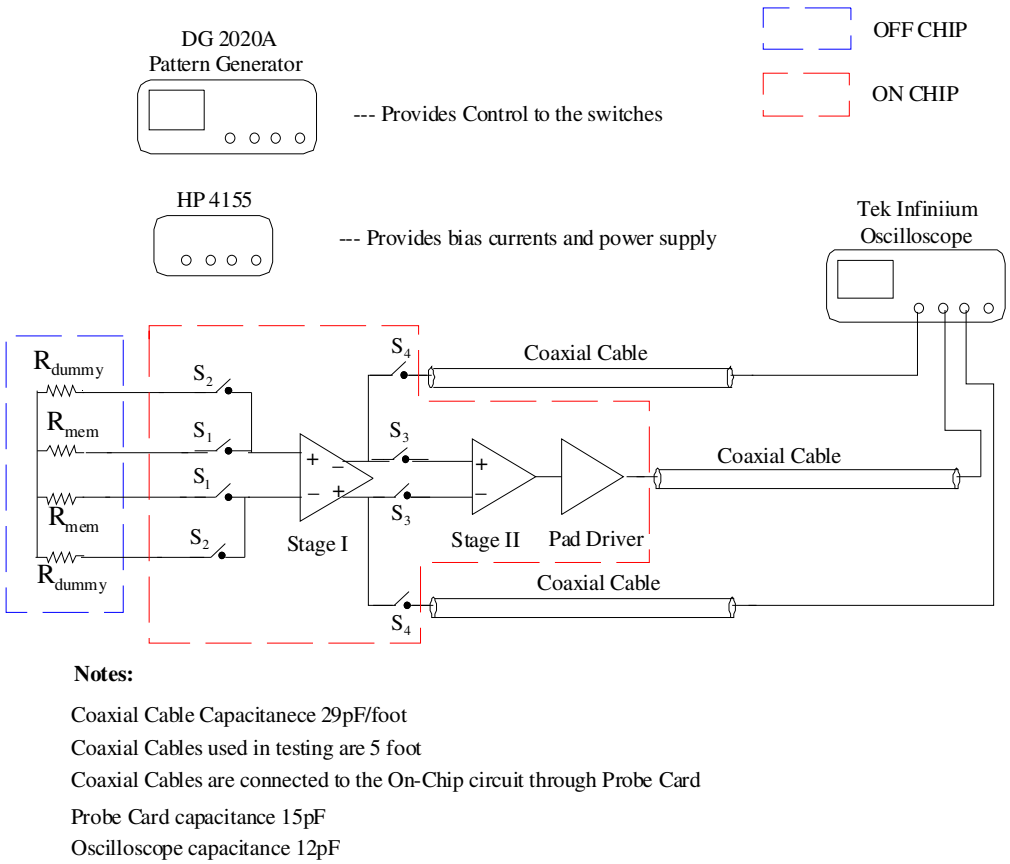


Figure 6. 8 Test setup diagram for the sense amplifier.

The testing was performed as follows. The resistors (R_{dummy} & R_{mem}) of Figure 6.8 are off chip (or wafer) while the switches (S_1, S_2, S_3, S4) amplifiers and pad driver are all on chip. The outputs of the amplifier (V_{out}+ and V_{out}-) and the logic output of the pad driver are connected to the coaxial cables via probe card. The probe card presents a load capacitance of 15pF. The coaxial cables are 5 foot long and they present a load capacitance of 145 pF (29 pF/foot). Switching ON S_4 and switching OFF of S_3 on-ship transmission gate switches allows the measurement of differential outputs of Stage I (and at this time are electrically loaded by the probe card, Coaxial cables and the Oscilloscope). These control signals were provided from DG2020A pattern generator.

Turning ON S_3 and turning OFF S_4 allows data to be observed at output of the logic buffer (Pad driver). In this condition the outputs of stage I are not loaded by the test setup capacitances mentioned previously. Testing was carried out by "programming" the off chip resistors to R_{mem}+/- 3 Ω (emulating the process of writing a '1' to one of the MRAM resistors and other to a '0'). The control signals for switching the resistors (S_1 & S_2) in and out were provided from the DG2020A pattern generator. Simulated waveforms of V_{out}+ and V_{out}- for ΔR= +/-3 Ω at 195°C along with 'Sense Cntrl'($R_{1delayed2}$) is shown in Figure 6.9 for comparison with measured results.

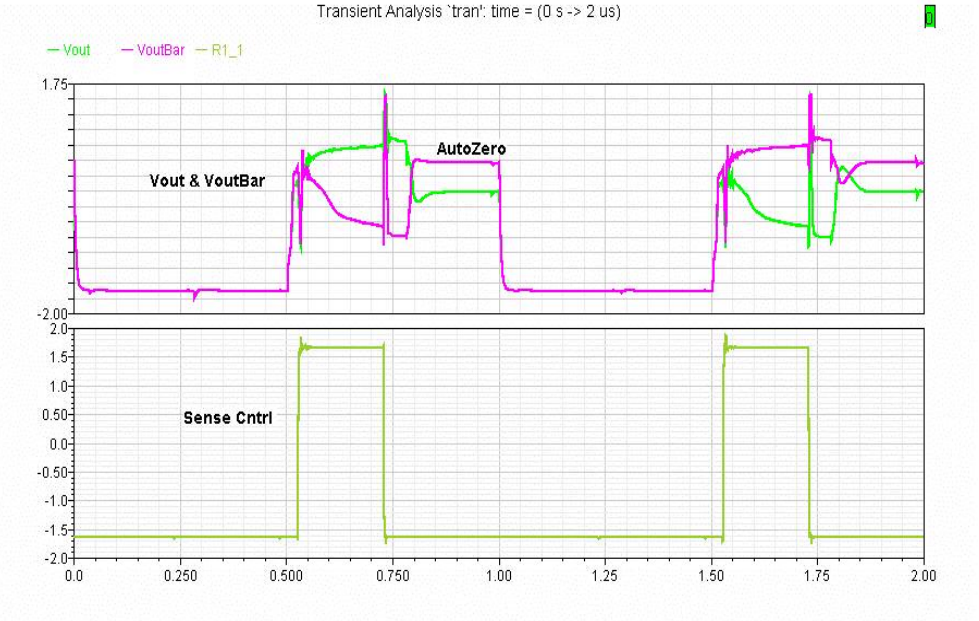


Figure 6. 9 Simulated waveforms of V_{out}+ and V_{out}- for ΔR= +/-3 at 195°C.

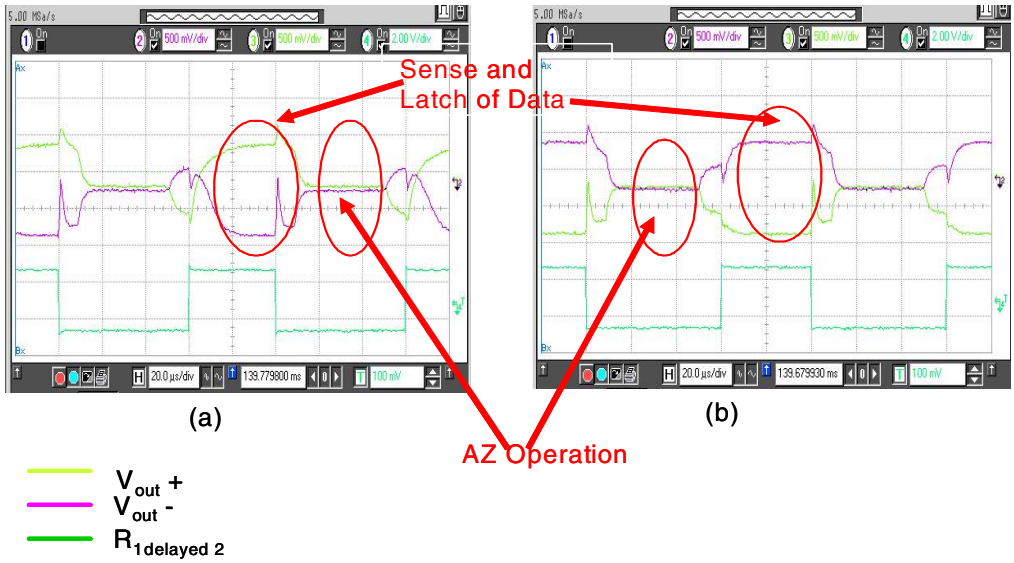


Figure 6. 10 Measured waveforms at 195°C of (a) V_{out}+ and V_{out}- for $\Delta R = 3\Omega$ (b) Vout+ and Vout- for $\Delta R = -3\Omega$.

Output signals V_{out}+ and V_{out}- are measured ahead of the logical output as shown in Figure 6.10. Shown in Figure 6.10(a) are V_{out}+ and V_{out}- signals while sensing a '1' and Figure 6.10(b) while sensing a '0'. The outputs V_{out}+ and V_{out}- during the auto-zero phase are also shown in Figure 6.10. During the auto-zero process, the input signal from the resistors is equal to zero. The voltage difference between the outputs during auto-zeroing can be explained to be a result of mismatch of the rail side PMOS and Ms transistors (Chapter 5 Auto zero offset cancellation). As mentioned in Chapter 5 the offset voltage is stored on the capacitors with the opposite polarity thus canceling out the offset.

Shown below in Figure 6.11 is the transient waveform measured at the output of pad driver with $\Delta R = +/-3\Omega$ (sensing a logic '1') applied. Note that the sense amplifier is positive or true logic and when followed by the inverting buffer resulting in inverted logic for a positive ΔR as shown in Figure 6.11.

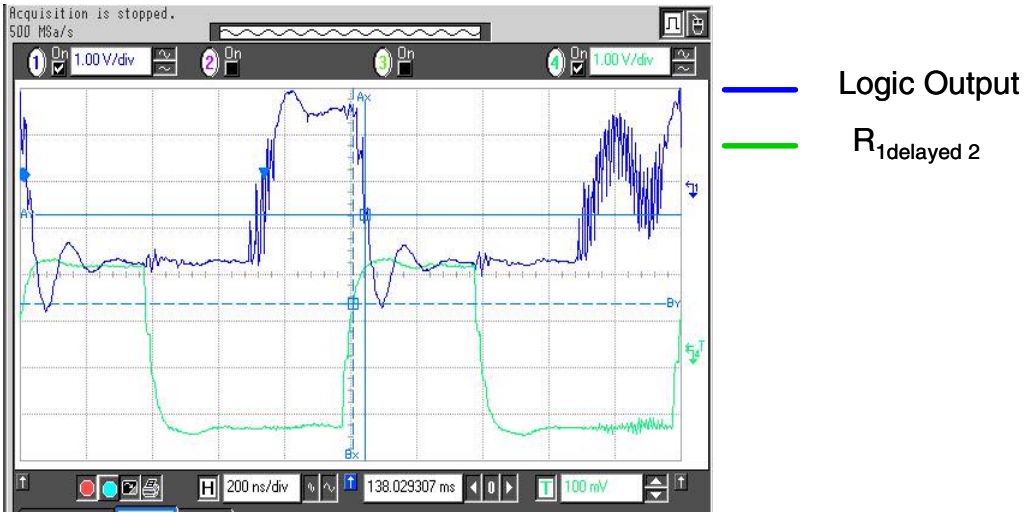


Figure 6. 11 Logic Output when applied $\Delta R = +/-3\Omega$.

The distributions of measured delays for sensing $\Delta R = \pm 3\,\Omega$ and $\Delta R = \pm 5\,\Omega$ is as shown Figure 6.12.

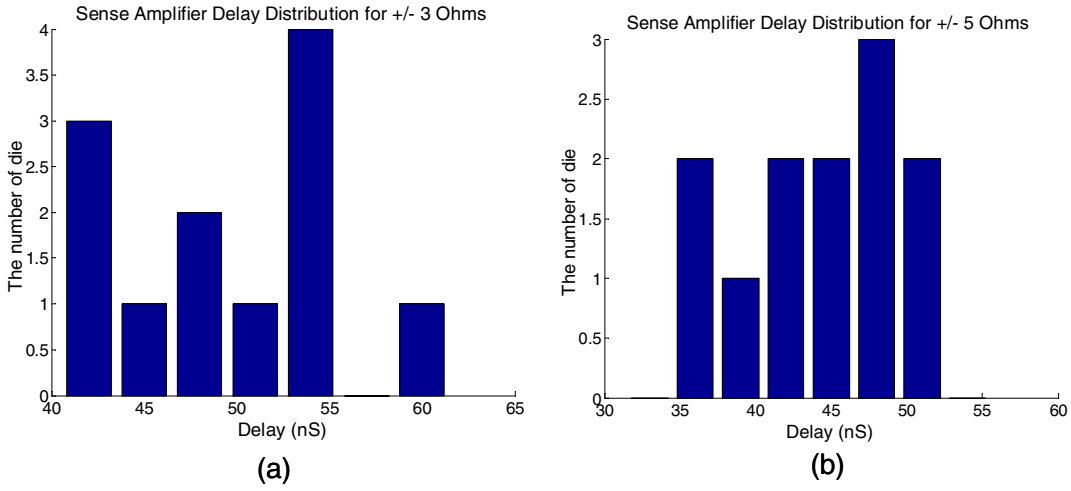


Figure 6. 12 Sense Amplifier Delay distribution for $+/-3\,\Omega$ (a) and $+/-5\,\Omega$ (b).

The average delay for $\Delta R = \pm 3\,\Omega$ is 49.33nS +/- 5.85nS (5.85 nS is the Sigma variation of delay). The results were recorded and binned in 3nS intervals. Delay predicted by

simulation was 40nS. Average delay for ΔR=+/-5Ω is 44.33nS +/- 5.05nS. It can be observed that delay obtained from test results is 25 % higher than the predicted simulation results for $\Delta R = \pm 3\Omega$. These test results prove the functionality of the sense amplifier at 195 ^{o}C.

6.4.1 Settling time details for the first gain stage of Sense amplifier:

The total test setup capacitive loading (Figure 6.8) was measured using an HP 4192A impedance analyzer is as itemized below

- Probe card → 15 pF
- Coaxial cable → 145 pF
- Agilent Infiinium Scope → 12pF

The settling time constant of the first stage was obtained by de-embedding the capacitive loading effect summarized below.

Time required to reach 90% is 2.3τ

Capacitive loading of sense amplifier with external loading (Probe card, Coaxial cable & oscilloscope);C_{ext}= 172 pF

Capacitive loading of sense amplifier without external loading (internal); C_{int}= 1.132 pF

$$\tau = RC \Rightarrow \tau_{ext} = R\ C_{ext}, \tau_{\text{int}} = R\ C_{\text{int}} \tag{6.1}$$

$$\frac{\tau_{\text{int}}}{\tau_{ext}} = \frac{C_{\text{int}}}{C_{ext}} \tag{6.2}$$

$$\text{also } \tau_{ext} = \frac{t_{90\%}}{2.3} \tag{6.3}$$

$$\text{From Eq 6.2 and Eq 6.3, Time constant } \tau_{int} = \left(\frac{t_{90\%}}{(2.3)\left(172 / 1.132\right)} \right) \tag{6.4}$$

Table 6.1 shows the measured values of $t_{90\%}$ for C_{ext} of 172 pF and de-embedded settling time constants for C_{int} of 1.132pF for all the measured dies.

Table 6. 1 Settling time constants for all the measured dies.

Die Num	Time required to reach 90% (uS)	time constant τ_{int} (de-embedded)
15	21	0.059746334
22	13	0.036985826
31	15	0.042675953
53	11	0.031295699
63	28	0.079661779
73	20	0.056901271
101	19	0.054056207
105	25	0.071126588
109	13	0.036985826
115	18	0.051211144
133	24	0.068281525
137	23	0.065436461

Average value of settling time constant is 54.5 nS. In a single settling time constant the output of the stage I (or any RC network) reaches to 63.2% of its final value. From the previous section, delay time for the output of pad driver to appear is 49.33nS +/- 5.85nS. From the above it can be concluded that one single time constant of the stage I provides enough voltage for the stage II to produce a valid logic level.

6.4.2 Auto-Zero Settling Time:

The resolution of the sense amplifier is determined by the offset inherent in the transistors. In our implementation offset-cancellation is employed to overcome this. The schematic along with the controls for the switches is as shown in Figure 6.13. $R_{0\ advanced}$ is used to reduce the effects of charge injection from the AZ switches [36].

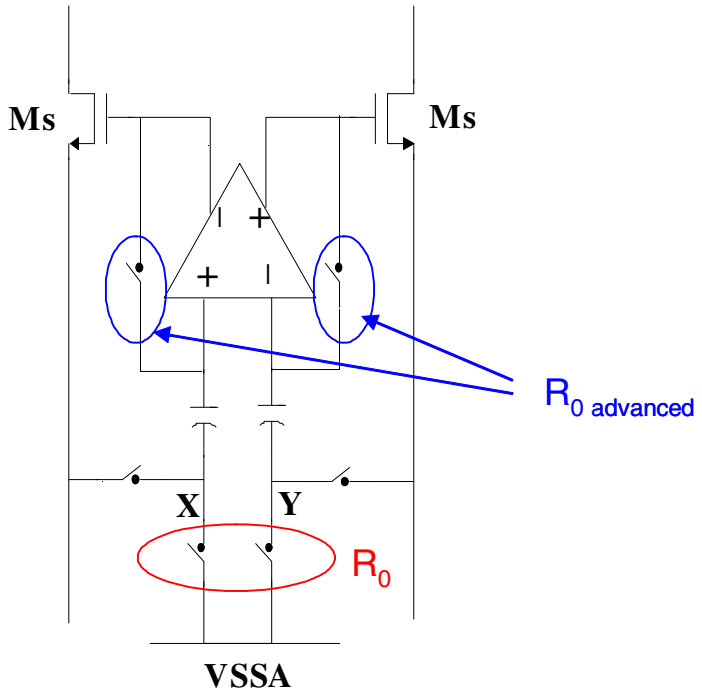


Figure 6. 13 Auto-Zeroing controls and block diagram.

The capacitive loading (See Figure 6.8) for the Auto-Zero mode is the same as in the previous case of sensing settling time or the native sense amplifier time constant.

Table 6.2 shows the Auto-Zero settling time with the external capacitive loading and the de-embedded settling time with capacitance C_{int} calculated using Eq 6.7. The settling measured was for 1% accuracy (equal to 5τ).

$$t_{99\%ext} = 5\tau_{ext} = 5RC_{ext} \tag{6.5}$$

$$t_{99\%\,\mathrm{int}} = 5\tau_{\mathrm{int}} = 5RC_{\mathrm{int}} \tag{6.6}$$

$$\text{De-embedded settling time, } t_{99\%\,\text{int}} = t_{99\%\,ext}\left(\frac{1}{C_{ext}/C_{\text{int}}}\right) \tag{6.7}$$

Table 6. 2 Auto-Zero Settling time.

Die Num	AZ Settling time, $t_{99\%\,ext}$ (uS)	De-embedded settling time $t_{99\%\,\text{int}}$ (uS)
15	10	0.065436461
22	10	0.065436461
31	10	0.065436461
53	10	0.065436461
63	12	0.078523753
73	10	0.065436461
101	10	0.065436461
105	12	0.078523753
109	12	0.078523753
115	10	0.065436461
133	12	0.078523753
137	12	0.078523753

The average Auto-Zero settling time is 70.88nS. Note that this is the settling time not the time constant. Assuming a 1% or 5 τ measurement accuracy the sense amplifier has a time constant of 14.2nS. Simulations predicted a 140nS settling time or a factor of 2X slower at 5 τ.

A close up view of the auto-zero intervals is shown for reference in Figure 6.14. The encircled area of Figure 6.14 shows the output after linear settling. During auto-zeroing, the voltage difference between V_{out}+ and V_{out}- was 50mV which translates to 2.5mV of input referred offset. The output offset voltage when referred to the input is divided by the gain of Ms transistors (Figure 6.13). The calculated value of offset using the pellgrom

numbers extracted in Chapter 2 is 0.81mV. This shows that the matching of transistors in the sense amplifier is 3 times worse than predicted for a single sample.

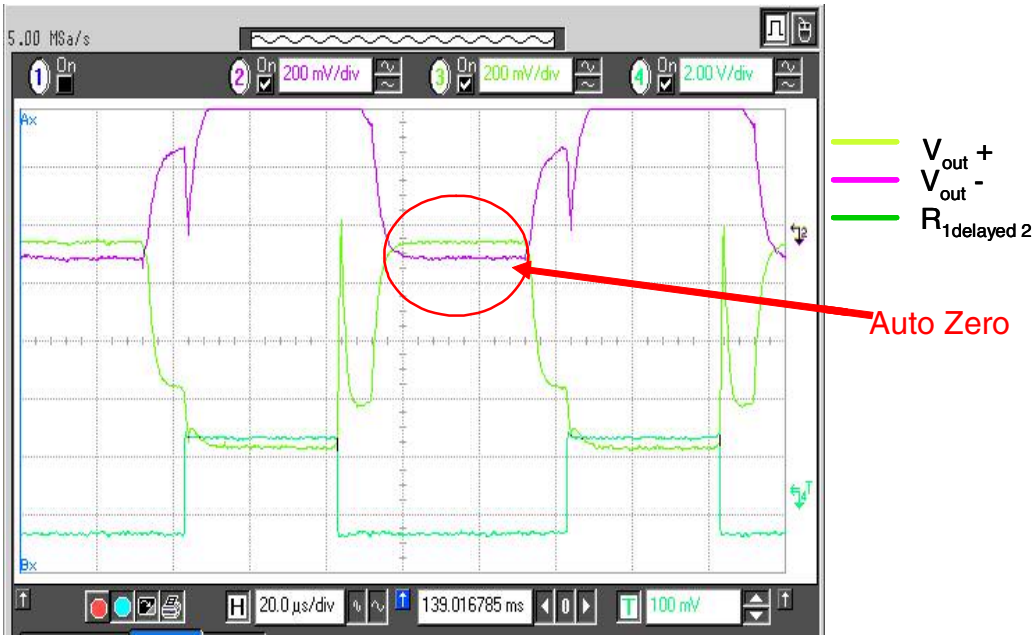


Figure 6. 14 Zoomed view of Auto Zeroing.

6.5 Summary:

Sense amplifier settling time delay for $\Delta R = \pm 3\Omega$ is 49.33nS +/- 5.85nS with an auto zero time of is 70.88nS for a 1% settling error or 5τ. The sense amplifier successfully measured a logic levels for $\Delta R = \pm 3\Omega$ for all 12 amplifiers tested with a 49.33nS +/- 5.85nS read access time. The design objective for the sense amplifier was to correctly sense a $\Delta R = \pm 3\Omega$ with settling time delay of 40nS and an auto zero period of 140nS. The allocated sense period during MRAM design was 200nS with 400% safety margin. The test results demonstrate that the sense amplifier is approximately 2X faster than required when considering a 6 sigma variation in the delay time (85nS). Comparison of measurement and simulation results on the boost amplifier was performed showing

excellent agreement with error less than 10%. The input referred offset obtained from a single measurement (2.5mV) was a factor of 3 worse than hand calculations (0.81mV).

6.6 Conclusions:

In this work characterization of Silicon On Sapphire process for high temperature was performed. The key points are summarized below

- Pellgrom matching coefficients for Peregrine SOS process were obtained from extensive measurements.
- High voltage transistors were designed, fabricated and tested with results confirming success.
- Analog and Digital models for high temperature simulation (120 ^{o}C to 195 ^{o}C) were extracted and were validated using test results.
- A sense amplifier for 8KX8 MRAM was designed and tested with results confirming the design process a success. A success not only in the design and fabrication of the sense amplifier but in validating the performance of the extracted models and Pellgrom numbers.

6.7 Future Work:

The following are the areas where future work needs to be done:

- Exchange ideas with Peregrine Semiconductor to formulate a methodology for changing doping densities in HV SOS MOSFET to obtain a *"kink-free" (until 2*VDDA - 2ΔV)* and optimized *"vdssat"*.

- Generation of mismatch models to be used in Simulation tools (Monte-Carlo statistical simulations) for yield testing.
- Design test structures for Capacitance extractions to obtain the AC parameters of the BSIM3SOI model over temperature.
- Design test structures for Noise extraction to obtain the noise parameters of the BSIM3SOI model.
- Design of high resolution analog circuits requires knowledge of matching coefficients for capacitance and resistance. So test structures need to be designed and capacitance & resistance matching coefficients need to be extracted.
- Research on frequency dependence of kink effect need to be carried for a better understanding of the kink effect.

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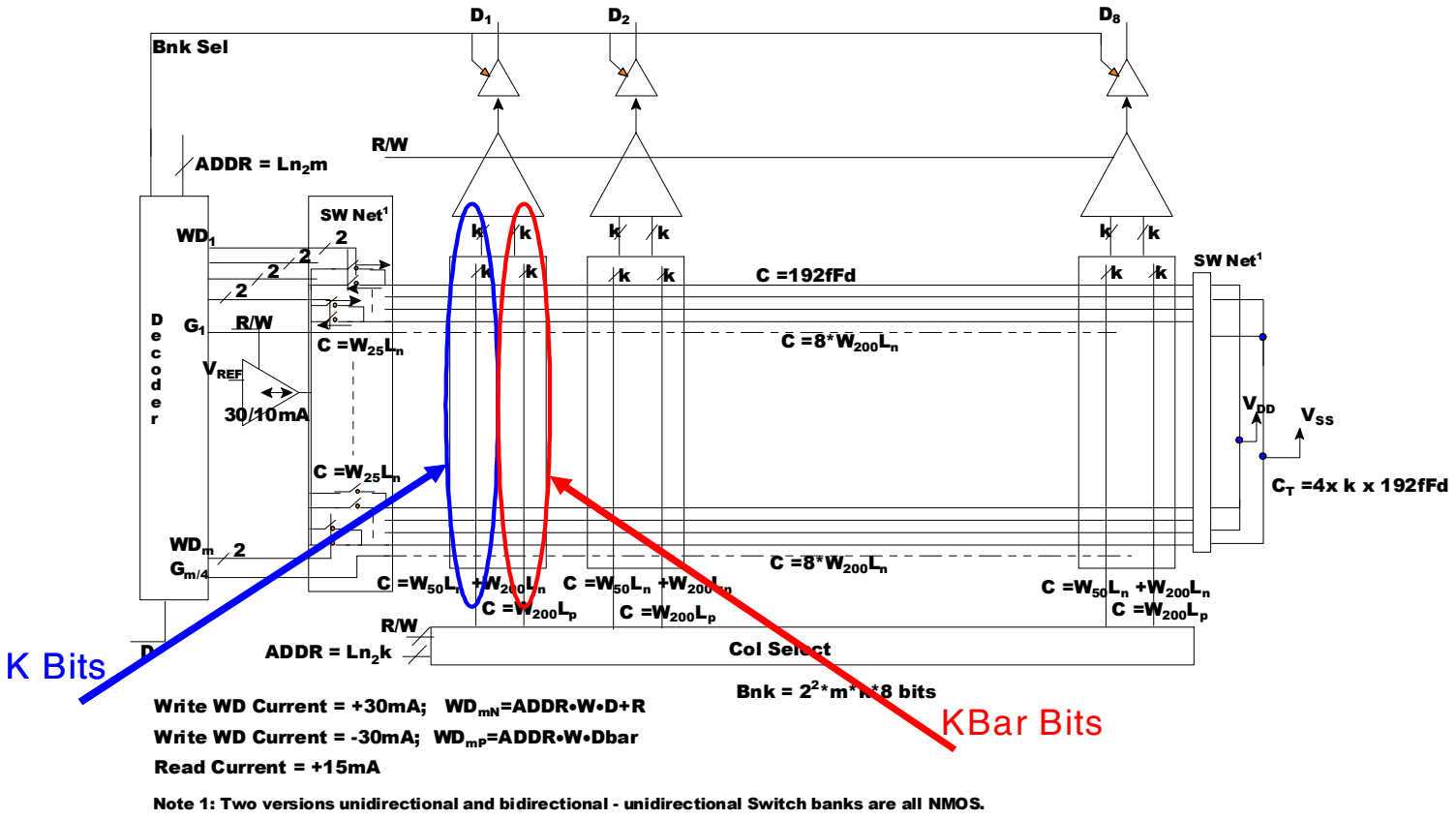
Appendix A:

A.1 Verilog-A code for MRAM Cell

Verilog-A code for MRAM cell

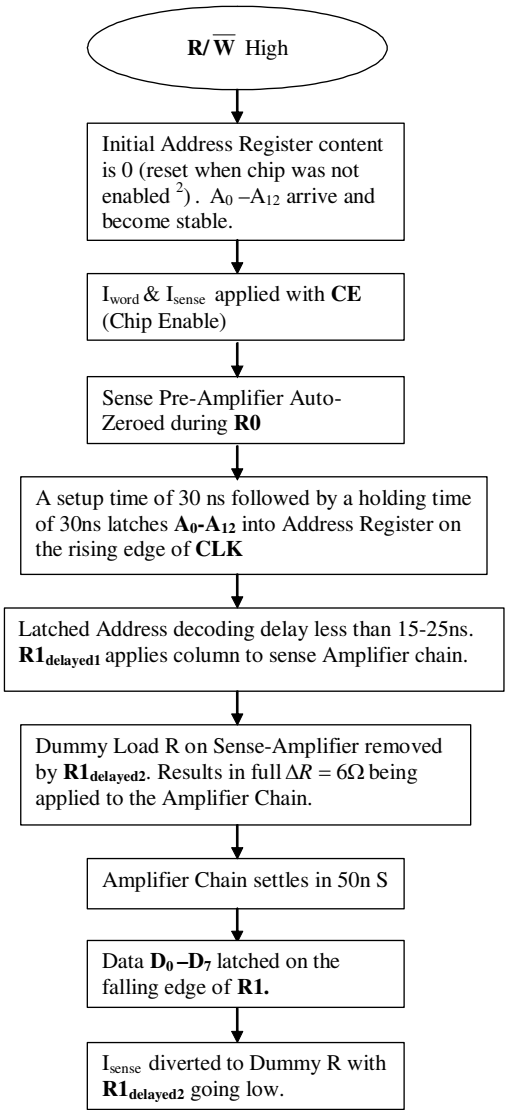
```
`include "constants.h"
`include "discipline.h"
module spinres(inp,inn,outp,outn);
inout inp,inn,outp,outn;
electrical inp,inn,outp,outn;
real res ;
real res_1 ;
real res_0 ;
parameter real cellres = 80 from (1:inf);
parameter real GMR_change = 3 from (1:inf);
analog begin

        res_1 = cellres + ((GMR_change/100) * (cellres));
        res_0 = cellres - ((GMR_change/100) * (cellres));

                @(cross (I(outp,outn)-3.6m,+1)) begin
                if ((I(inp,inn) >= 27m) && (I(inp,inn) <= 33m))
                res = res_1;
                else res = res;
                end
                @(cross (I(outp,outn)-3.6m,+1)) begin
                if ((I(inp,inn) <= -27m) && (I(inp,inn) >= -33m))
                res = res_0;
                else res = res;
                end     if ((I(inp,inn) < -13.5m) && (I(inp,inn) > -16.5m))
        V(outp,outn) <+ res*I(outp,outn);
        else V(outp,outn) <+ cellres * I(outp,outn);
        end
endmodule
```

A.2 Architectural Block Diagram of 8KX8 MRAM:



Appendix B:

B.1 Flow Chart for the read operation:



B.2 READ CYCLE:

1) A transition of **R/$\overline{\mathbf{W}}$** signal to logic high enables a read cycle and terminates a write cycle. This forces data lines $\mathbf{D_0}$-$\mathbf{D_7}$ into the high Z state.

2) I_{word} & I_{sense} are applied with Chip Enable **CE**. I_{word} is applied to the existing address or to the default address (Address register contents are reset prior to the application of **CE**) & I_{sense} is applied to the dummy load R.

3) The Pre-Amplifier in the Sense Amp is Auto-zeroed during the **R0** cycle.

4) Address ($\mathbf{A_0}$-$\mathbf{A_{12}}$) is latched on the postive edge of **CLK** into the Address Register and should be valid for 30 ns prior to the rising edge to ensure a valid latch of the address and should remain unchanged for 30 ns following the rising edge of **CLK**.

5) The latched Address is decoded.

6) I_{sense} is let to flow through both dummy R and the Spot resistance with the application of $\mathbf{R1_{delayed1}}$. Dummy R is disconnected with $\mathbf{R1_{delayed2}}$ resulting in application of full $\Delta R = 6\Omega$ at the Sense Amplifier.

7) The Sense Amplifier settles in 50n S. The Data is latched at the falling edge of **R1**.

8) The latched data appears on the external data lines $\mathbf{D_0}$- $\mathbf{D_7}$ after 30 ns (need to be checked) when $\mathbf{O_E}$ is activated externally.

9) $\mathbf{O_E}$ pulse can be applied at any desired time during a read cycle. But it gets functionally disabled internally with the beginning of a write cycle (i.e. whenever **R/$\overline{\mathbf{W}}$** goes low)or if the chip is disabled (by making any of the two chip enables inactive).

10) Data lines go to high Z state within 10 ns after $\mathbf{O_E}$ is disabled.

VITA

Narendra Babu Kayathi

Candidate for the Degree of

Master of Science

Thesis: EXTENDED MODELS OF SILICON ON SAPPHIRE TRANSISTORS FOR ANALOG AND DIGITAL DESIGN AT ELEVATED TEMPERATURES (200^{o}C)

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ABSTRACT

Name: Narendra Babu Kayathi Date of Degree: December 2005

Institution: Oklahoma State University Location: Stillwater, Oklahoma

Title of Study: Extended Models of Silicon On Sapphire transistors for Analog and Digital Design at elevated temperatures (200°C).

Pages in Study: 99 Candidate for the Degree of Master of Science

Major Field: Electrical Engineering

This work focuses on extending the vendor supplied SOS MOSFET models to suit high temperature (200°C) CMOS circuit design or more specifically accurate simulation. The SPICE parameters required have been extracted through measurement of High Vt and Low Vt NMOS and PMOS transistors on five spatially separated die (6 transistors of each type on each die) on a wafer with a wide range combinations of lengths and widths over the temperature range of interest (120°C to 200°C). Both analog and digital models were extracted and validated. The extracted models were verified by comparing measured and simulated ID-VDS characteristics of minimum geometry transistors at all temperatures. Measured results of an OTA and its bias Circuit's high temperature operation were compared with simulations using the extended model verifying the model's adequacy for analog design. Transistor mismatch (critical to analog design) was characterized as a function of device width and length for NMOS and PMOS. To support high voltage applications e.g. EEPROM read/write, a (Lightly Doped Drain) High voltage LDD SOS MOSFET was developed and its LDD length-specific model was extracted and verified. The temperature dependency of critical analog design parameters like output resistance, mobility, threshold voltage was characterized in detail.

In section-II circuit techniques suitable for high temperature operation were developed and verified with a sense amplifier (25°C to 200°C) for an 8KX8 Magneto-resistive Random Access Memory. The amplifier's first stage is a trans-resistance amplifier auto-zeroing topology followed by a self-biased differential-to-single ended amplifier second stage. In order to maintain a constant gain, a temperature independent "Veff" bias generator circuit was developed.

ADVISOR'S APPROVAL: _____Dr. Chris Hutchens_____