DEVELOPMENT OF A 5V DIGITAL CELL LIBRARY FOR USE WITH THE PEREGRINE SEMICONDUCTOR SILICON-ON-SAPPHIRE (SOS) PROCESS

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Glossary

SOC	System-On-a-Chip
ASIC	Application Specific Integrated Circuit
IC	Integrated Circuit
LVS	Layout versus Schematic
LEF	Library Exchange Format
VHDL	VHSIC (Very High Speed Integrated Circuits) Hardware Description Language
NMOS	n-channel Metal-Oxide-Semiconductor
PMOS	p-channel Metal-Oxide-Semiconductor
I_{on}	On-state Current
I_{off}	Off-state Current
Vdd	Supply Voltage
Gnd	Ground
I_{SINK}	Sink Current of a device
I_{SOURCE}	Source current of a device
V_{IL}	Voltage Input Low
V_{IH}	Voltage Input High
VTC	Voltage-transfer Characteristic
V_{OH}	Voltage Output High

V_{OL}DRC	Design Rule Check
I/O	Input/Output
GDSII	Graphic Data Systems
MOSFET	Metal –Oxide-Semiconductor Field-Effect Transistor
ALF	Advanced Library Format
LIB	Synopsys liberty file format
TLF	Timing Library Format
RTL	Register Transfer Level
T-gates	Transmission gates
3X	Three times the load represented by a minimum sized inverter
6X	Six times the load represented by a minimum sized inverter
Id	Drain current of a transistor
Vd	Drain voltage of a transistor

CHAPTER 1

INTRODUCTION

Application-specific integrated circuit, an integrated circuit intended for a particular use rather than general-purpose use, has become complex over the years with more than 100 million gates in it. Feature sizes have shrunk and design tools have improved letting processor, memory blocks including RAM, ROM, EEPROM and other large building blocks to be on a single chip (System-on-a-chip). Initial ASICs used gate array technology in which only metal interconnect mask and polysilicon layers are customizable. Designers in mid 80's had to choose an ASIC manufacturer and implement their designs using specific tools available from manufacturer and were not able to use any third party design tools due to lack of effective connecting links with layout and actual semiconductor performance characteristics of various manufactures. Standard cell based design was the solution that yielded designs with good electric performance and very high layout density. Standard cells are implemented by ASIC manufactures with their electrical performance characterized and represented in several third party tools.

1.1 Standard cell based design flow

As complexity of ASIC designs continues to increase, full-custom design does not seem to be feasible. Automating design procedure (by using CAD tools like synthesis and place & route tools) reduces time to market by huge amounts. Standard cell based design provides reusability of basic cells for various designs and gives optimal level of abstraction. The cell based ASIC design flow diagram shown in figure 1.1 categorizes the entire design procedure into tasks that fall under several design teams. The design procedure for ASICs given a fully characterized standard cell library is as follows:

1. A synthesizable behavioral description of design in high-level description language (VHDL or Verilog) is written. This is called RTL (register transfer level) design.
2. The suitable functionality of the RTL code is verified by simulation.
3. Design partitioning into few smaller blocks is performed. This provides easy handling of design, efficient synthesis results with reduced time to market and reusability.
4. Logic synthesis on the RTL description is performed. This maps design on to standard cells and connectivity between. This provides a gate-level netlist depicting standard cells and electrical connections between them.
5. Functional simulation and Static timing analysis are performed on the synthesized code.
6. Gate-level netlist is imported into a place & route tool. Floorplanning, powerplanning, placement, In Place Optimization (IPO) and trial route are performed on RTL level netlist imported. Clock tree synthesis and timing analysis

are performed. All the partitioned blocks are brought together at place & route level either with individual blocks placed & routed to give a block.

7. Post layout simulation is performed and static timing is back annotated. Testing is performed demonstrating the functional correctness of the design over all extremes of process, voltage and temperature.
8. Physical verification (DRC and LVS) is performed at the end before the design is sent to semiconductor facility for fabrication.

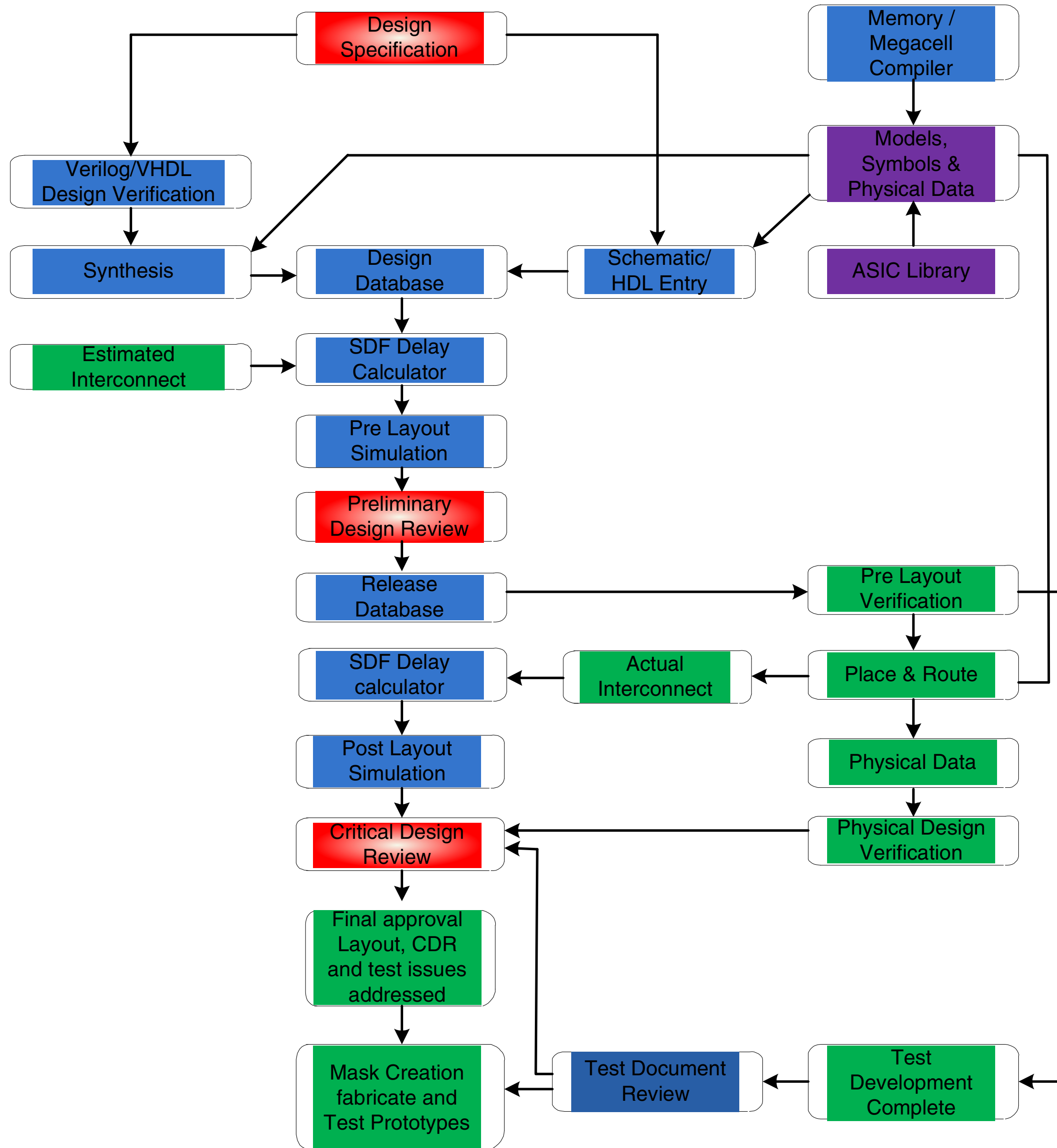


Figure 1.1 Standard cell based ASIC design flow

1.2 Thesis Organization

This thesis consists of 6 chapters. Chapter 2 describes what Silicon-on-Insulator CMOS process is as compared to bulk CMOS process, what its advantages are over bulk process

as well as design issues to be considered. Chapter 3 is about standard cell library's importance and development procedure. It also deals with design aspects/techniques of the present work. Chapter 4 is detailed regarding modeling of cell delay/timing, cell characterization methodology, characterization parameters and outputs and integration details with simulator and synthesizer. Chapter 5 describes test chip design and cell library validation process. Chapter 5 summarizes results of this work in terms of its characterization robustness and gives details regarding scope of further work.

CHAPTER 2

SILICON ON INSULATOR DEVICE TECHNOLOGY

2.1 Introduction

Bulk-silicon has been the material of choice for integrated circuits until last decade for low-voltage applications. Radiation hardness of SOI circuits was the main motivation behind developing and using SOI circuits in 80's and was used in many special applications like high-voltage or radiation hardened integrated circuits. However since last decade, SOI emerged as a realistic alternative for conventional bulk-silicon in low-power, high-performance applications also for the formidable issues that the latter was facing such as,

- Reduction in threshold voltage requirement due to rapid scaling down of device dimensions and supply voltages.
- Failing to operate satisfactorily within the power constraints or operating at lower speeds for the given power for the same node length.
- Failing to operate reliably in high temperature electronic applications like down-hole drilling and monitoring, electric vehicles, distributed engine and flight controls etc.

- SOI offers great reduction in leakage currents at high temperatures and higher packaging densities by preventing latch up due to temperature-dependent leakage currents, improves
- short channel effects and soft error immunity and offers reduction in junction capacitance allowing operation at high frequencies. By providing reduced threshold voltages, SOI process ensures that there is required drive current and tolerable off current.

2.2 Device Structure: Bulk Vs SOI

In bulk process, individual devices are fabricated in the body of silicon and large area p-n junctions are used for isolating drain and source of P/N type MOS transistors from the substrate. In an n-well process, N type MOSFETs are fabricated in p type silicon substrate and P type MOSFETs are fabricated in an n-well diffused in p type silicon substrate. Individual transistors are isolated from each other using field oxide. Drain and source of NMOSFETs are isolated from substrate by p-n junction formed by drain or source itself with si substrate. Drain and source of PMOSFETs isolated from si substrate using n-well. On the other hand, devices in SOI process are fabricated in silicon thin film active layer over a buried oxide layer. BOX being an insulator provides isolation of transistors from si substrate underneath it and local oxidation of silicon (LOCOS) or removing of unused silicon between transistors isolates individual transistors. In fully depleted SOI process, thickness of silicon film over insulator is less than approximately 50nm. Thus entire silicon film is taken by source/drain depletion region leaving no body.

Whereas in partially depleted SOI process, silicon film thickness is around 100nm to 200nm giving rise to existence of body that is floating.

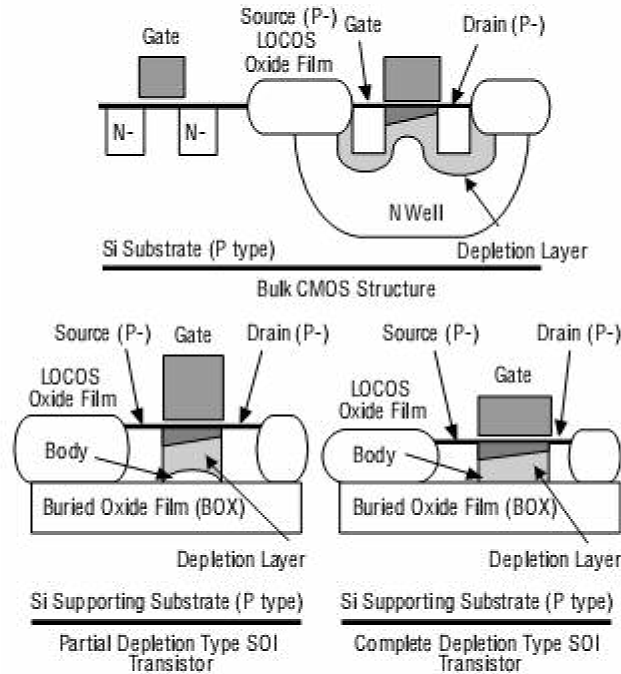


Figure 2.1 Comparison between bulk CMOS and SOI CMOS structures [8]

2.3 Advantages of SOI CMOS over bulk process

2.3.1 Parasitic effects

In bulk processes since the transistors are isolated from substrate by reverse biased p-n junctions, junction leakage currents contribute to both stand-by as well as switching leakage currents of the devices. They increase exponentially with increase in temperature and proportional to junction area. Due to isolation of devices in SOI from substrate, substrate leakage currents are absent giving rise to significant reduction in leakage currents as compared to bulk. Also surface leakage problems and field transistor action

which may occur is bulk is absent in SOI. This leads to reliable high temperature operation of SOI devices with tolerable amount of off state currents. In bulk devices parasitic bipolar transistors are formed by the substrate, well and diffusion regions that turn on (phenomenon called latch-up) when external voltages outside the normal operation range are applied or transient currents power up. In SOI CMOS devices when the silicon film containing the active devices is sufficiently thin, depletion regions reach through to the buried insulator leaving no current path to the substrate. Hence latch-up is totally eliminated.

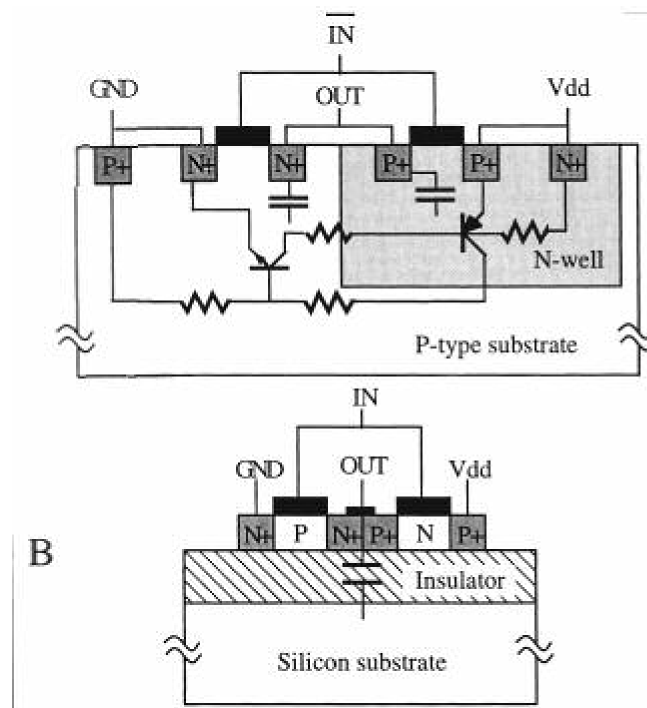


Figure 2.2 Latchup and drain parasitic capacitance in bulk and SOI CMOS inverter [2]

2.3.2 Junction capacitances

In bulk devices, a depletion capacitance is formed between source/drain and substrate due to revere biased p-n junction. Based on the voltage level on source/drain, depletion

capacitance varies with its value maximum reached for 0V on drain in n-channel transistor. This capacitance increases with doping concentration. In addition to it, a parasitic capacitance between source/drain and channel stop implant underneath field oxide also exists. In SOI, maximum value of source/drain capacitances is dictated by buried oxide layer capacitance which is much less as a result of the greater BOX thickness. This leads to faster transistor switching in SOI as compared to bulk.

2.3.3 Integration densities

SOI CMOS technology offers higher integration density than bulk CMOS for the several reasons listed below [2]:

- Devices in SOI CMOS process are isolated dielectrically requiring no wells. On the contrary bulk CMOS process uses p-n junctions formed by wells for isolating devices.
- SOI eliminates latch-up completely permitting higher packaging densities. This results in reduced silicon area and routing capacitance.
- Leaving the body floating in case of PD-SOI leads to better density and improves circuit speed.
- SOI offers possibility of having a direct contact between p and n junctions. The number of contact holes required per gate is lower in SOI as compared to bulk.

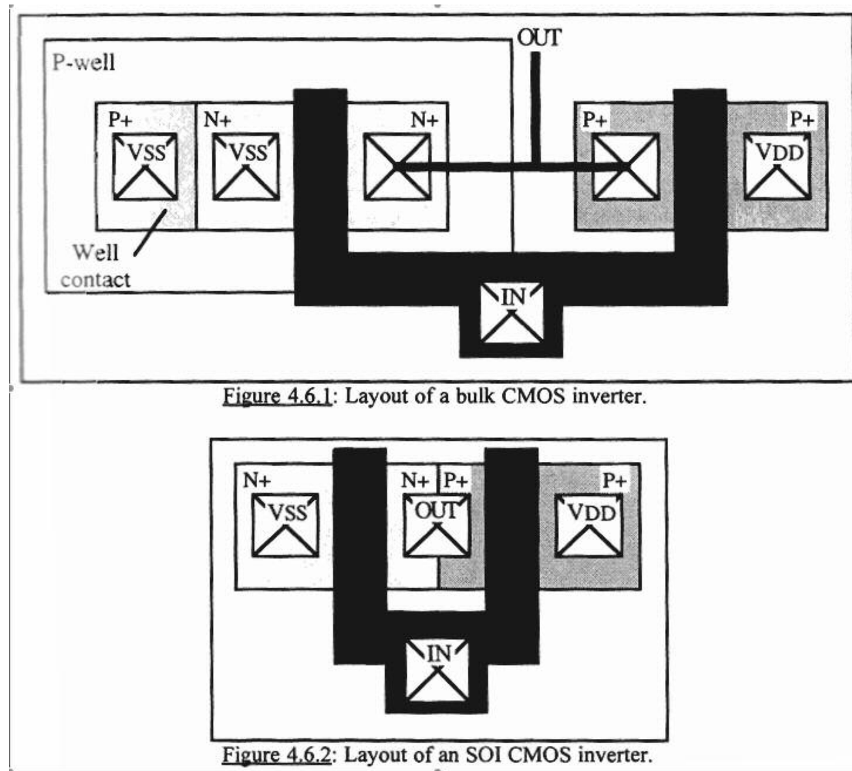


Figure 2.3 Comparison of areas in bulk and SOI processes [2]

2.4 Performance issues in PD-SOI and FD-SOI

2.4.1 PD-SOI CMOS process

Floating body in partially depleted device results in bipolar effect and hysteretic threshold variation introducing kink in dc I-V characteristics, lowering threshold voltage at high drain bias, degrading breakdown voltage and causing instability during dynamic operations [2], that represents serious design issues for circuit designers. Since PD SOI devices have their body floating, circuit simulation consumes more time for DC convergence and memory. Floating body effect can be reduced by selectively dropping body contacts without increasing area much.

On the other hand, partially-depleted devices alleviate the constraint on the source/drain series resistance and threshold voltage, offering higher performance and easing the manufacturing problem by allowing the doping profiles to be tailored for any desired threshold [4]. The process and device design in case of partially depleted SOI are much more compatible with the bulk CMOS but introducing body contacts makes it non-compatible. PD SOI provides tighter control of short channel effect than fully depleted SOI devices

2.4.2 FD-SOI CMOS process

Fully depleted devices possess larger source/drain series resistance the partially depleted devices, which limits the performance in terms of speed [2]. The process and design are less compatible with the bulk CMOS. In these devices, threshold voltage is decoupled from film thickness and is process sensitive making it difficult to manufacture and scale the value. Fully depleted device significantly reduces the floating-body effect making design easier for circuit designers.

2.5 Peregrine Semiconductor process

Peregrine Semiconductors of United States has implemented Ultra Thin Si (UTSi) technology for developing 0.5µm Silicon-on-Sapphire fully depleted process. UTSi greatly improved crystallization characteristics of the Si film on sapphire substrate [7]. Some of the features of SOS process are its complete isolation of devices, very low junction capacitances and extremely high radiation resistance. Being a fully depleted

process, floating body effects are eliminated giving less sensitive threshold voltage towards frequency as compared to partially depleted devices where body voltage varies with voltage variations on source, gate and drain terminals which is more significant a problem at high frequencies due to rapid switching of devices making it difficult to track threshold voltage, less severe subthreshold kink effect and low parasitic bipolar gain as well as low radiation back channel leakage.

2.6 High-voltage design

Full dielectric isolation of SOI devices results in monolithic integration of both high-voltage and low-voltage CMOS devices on a single chip [1].

CHAPTER 3

STANDARD CELL LIBRARY DESIGN ISSUES

3.1 Introduction

The quality of a system-on-a-chip design heavily relies on viability of ASIC standard-cell library. At the early design stage, cells are targeted to meet certain function and performance requirements. Typically, the cells can be designed with the intent to either optimizing for area or in optimizing speed. The former uses minimum sized transistors to achieve the smallest area while the latter uses larger transistors to provide good drive qualities.

3.2 Standard Cell Library Design Flow

In industry, the design approach adopted for developing a standard cell library is based on the optimization level required between the level of automation and layout density. Though a significant reduction in the IC's time-to-market is achieved, layout density is sacrificed as a result of the higher degree of automation chosen. Manual layout of standard cells on the other hand provides substantially low densities for the resulting

huge designs, since each of the standard cell might appear in millions in number in almost all large designs. Thus this method of laying out cells is still widely employed

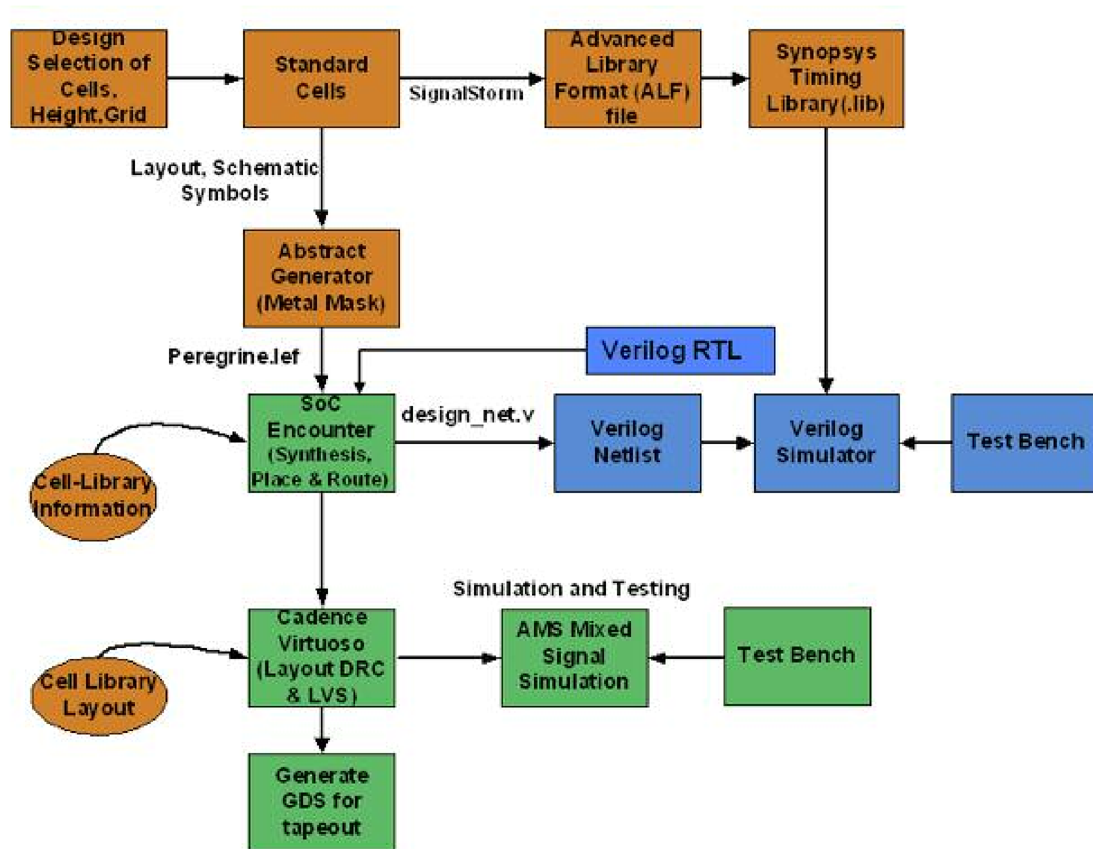


Figure 3.1 General Flow for creating a standard cell

Manual layout is employed for this work without considering for any of the above. The usual design flow for standard cell library development is depicted in the figure 3.1 (blocks highlighted in orange) and it proceeds as follows:

1. Widths and lengths for the NMOS and PMOS devices are set using analytical approach to meet the design requirements in terms of drive currents, area or noise margins.

2. Transistor level schematics for the cells are generated and performance is verified using spice/spectre circuit simulation tool.
3. Physical layouts for the cells are created using layout tools making them as dense as possible while complying with certain design rules provided by foundry/facility for their fabrication process. Besides DRC, cell layouts are also compared with the transistor level schematics (LVS check) to confirm that they have correct connectivity and proper device sizes.
4. The spice simulations that were run earlier for cell schematics should be repeated using the new netlist derived from extraction of the cell layout to evaluate the effects of parasitics.
5. The cells are simulated to ensure proper functionality and timing. To obtain realistic manufacturing process characteristic, circuit simulation is performed with temperature, voltage and process parameter over the range of values that are expected to occur. Since many repetitive executions of the circuit simulator are required for each cell, the characterization is done using an automatic cell characterization tool, i.e. signal storm.
6. After characterization is performed, the cell's functional description and timing data are transformed to the format required by specific design tools for integrating the standard cells into digital logic during ASIC design synthesis, simulation and place and route. Synthesis and place and route tools incorporate delay values from timing library during timing optimization to meet design constraints.
7. Along with timing library, place and route tool also requires a physical description library that includes definitions of blockages of routing layers and pin

information. Cadence abstract generator is used for getting Layout Exchange Format (LEF) file and abstract views for all the cells.

3.3 Deliverables of a standard digital cell library

A standard digital cell library that is intended to be used for an ASIC design, however designed, irrespective of vendor, should include the below listed:

1. Layout, schematic, abstract, extracted and symbolic views of all cells in the library.
2. Timing libraries across the best, worst and typical cases i.e. process, temperature, and voltage, realized in standard formats that are compatible with synthesis and place and route tools.
3. Physical description of the cells in terms of routing layers and pins to be used with automatic place and route tools. This is also called routing model.
4. Behavioral code for all the cells.
5. Verilog/VHDL model for all the cells.
6. Documentation that summarizes the functionality and timing of each cell. The functionality is frequently described with a truth table, and timing data is presented in a simple format in the datasheet. Documentation contains setup and hold times, minimum pulse widths, removal and recovery times, fan-in and fan-out, operating range of temperature and voltage.

3.4 Design Aspects

Critical design aspects at every step of a cell library design are reviewed in this section. Focus should always lie on setting the right geometries for devices to be used, selection of cells to be implemented using several layout techniques to get denser and error free layouts and providing accurate and self-sufficient technology library for later use with ASIC design.

3.4.1 Selecting geometries for NMOS and PMOS devices

Operating conditions for the intended use of the cell library and its performance requirements dictate geometries for NMOS and PMOS devices to be used in the library. This project was designed to operate at 5V and up to temperatures of 125°C. The Peregrine processes are designed to be a 4V process. At high supply voltages both leakage currents and avalanche currents can be high leading to circuit malfunction. As a result considerations must be under taken to avoid, avalanche breakdown, gate oxide break down and excessive leakage current as a result of the bipolar kink effect. Avalanche breakdown is a current multiplication process that occurs in the presence of strong electric fields caused by even moderate voltages over very short distances like in semiconductor devices. The voltage at which avalanche breakdown occurs in a given device poses an upper limit on the operating voltages because; the associated electric fields can start the process and cause excessive current flow and resulting in destruction or rapid aging of the device. Several NMOS devices with gate lengths starting 1µm and PMOS devices with gate lengths starting from 0.5µm have been tested on silicon at room temperature and 125°C (some of the plots are shown in figures 5.4 to 5.7) with drain

voltage of 5V. The data obtained shows that the electric field to which the carriers are subjected to, by applying 5V across drain and source does not start the avalanche breakdown process. Thus avalanche is not a problem even for minimum length devices for 5V of power supply both at room and high temperatures.

Due to reduced gate oxide thickness, a high voltage applied across gate and substrate results in high electric fields across the oxide. When the oxide is subjected to high electric fields, electrons will be able to tunnel through oxide layer and contribute to gate current. With increase in electric field across oxide, for values greater than certain threshold, oxide starts breaking down completely giving rise to very large gate currents therby causing the device to fail. Gate tunneling is not as problematic as is evident by the test data for the NMOS and PMOS devices of figures 3.2 and 3.3 devices showing no signs of gate tunneling when powered up to 8V.

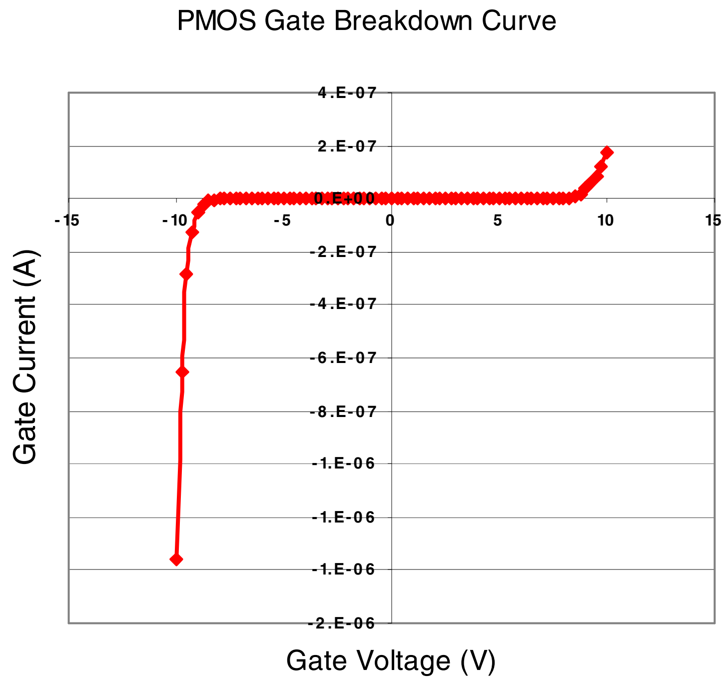


Figure 3.2 Gate breakdown voltage of Regular PMOS at 275˚C.

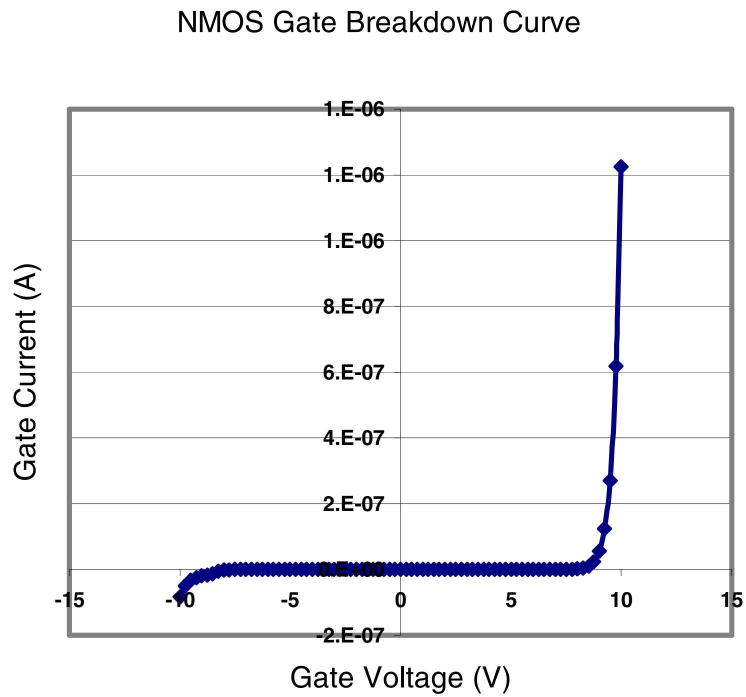


Figure 3.3 Gate breakdown voltage of Regular NMOS at 275˚C.

One other problem to be overcome for high voltage operation design is to obtain as low a leakage current as possible with reasonable Ion/Ioff ratios. Leakage current or transistor off-state current (Ioff) is the drain current when the gate voltage is zero. Ioff depends on the threshold voltage, channel physical dimensions; channel/surface doping profile, drain/source junction depth, gate oxide thickness, and Vdd. Drain to source leakage current is given by

$$I_{ds} = \mu_0 C_{ox} \frac{W}{L}(m-1)(v_T)^2 \times e^{(V_g - V_{th})/mv_T} \times (1 - e^{-v_{DS}/v_T}) \quad (3.1)$$

where

$$m = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{\frac{\varepsilon_{si}}{W_{dm}}}{\frac{\varepsilon_{ox}}{t_{ox}}} = 1 + \frac{3t_{ox}}{W_{dm}} \quad (3.2)$$

and V_{th} is the threshold voltage, and v_T = KT/q is the thermal voltage, C_{ox} is the gate oxide capacitance, μ_0 is the zero bias mobility; and m is the sub threshold slope coefficient. W_{dm} is the maximum depletion layer width, and t_{ox} is the gate oxide thickness. C_{dm} is the capacitance of the depletion layer.

Of several process-level and circuit-level techniques available for reducing leakage currents, controlling lengths of the devices is used for this work. Since NMOS devices were found to avalanche and leak more than PMOS at shorter channel lengths, design starts by choosing channel length for NMOS device that would give reasonable Ion/Ioff ratio. Hardware testing is performed on several NMOS devices with different lengths at

room temperature and 125°C to obtain Ion/Ioff ratios. Plots for on-state current and off-state current are shown in figure 3.4. A channel length of 1.6μm is chosen for NMOS device that is tested to demonstrate Ion/Ioff ratio of more than 80 at 125°C as is evident from plots shown in figure 3.4 for NMOS device with gate length of 1.6μm. Channel length of 0.5μm which is the minimum gate length for this process is chosen for PMOS device.

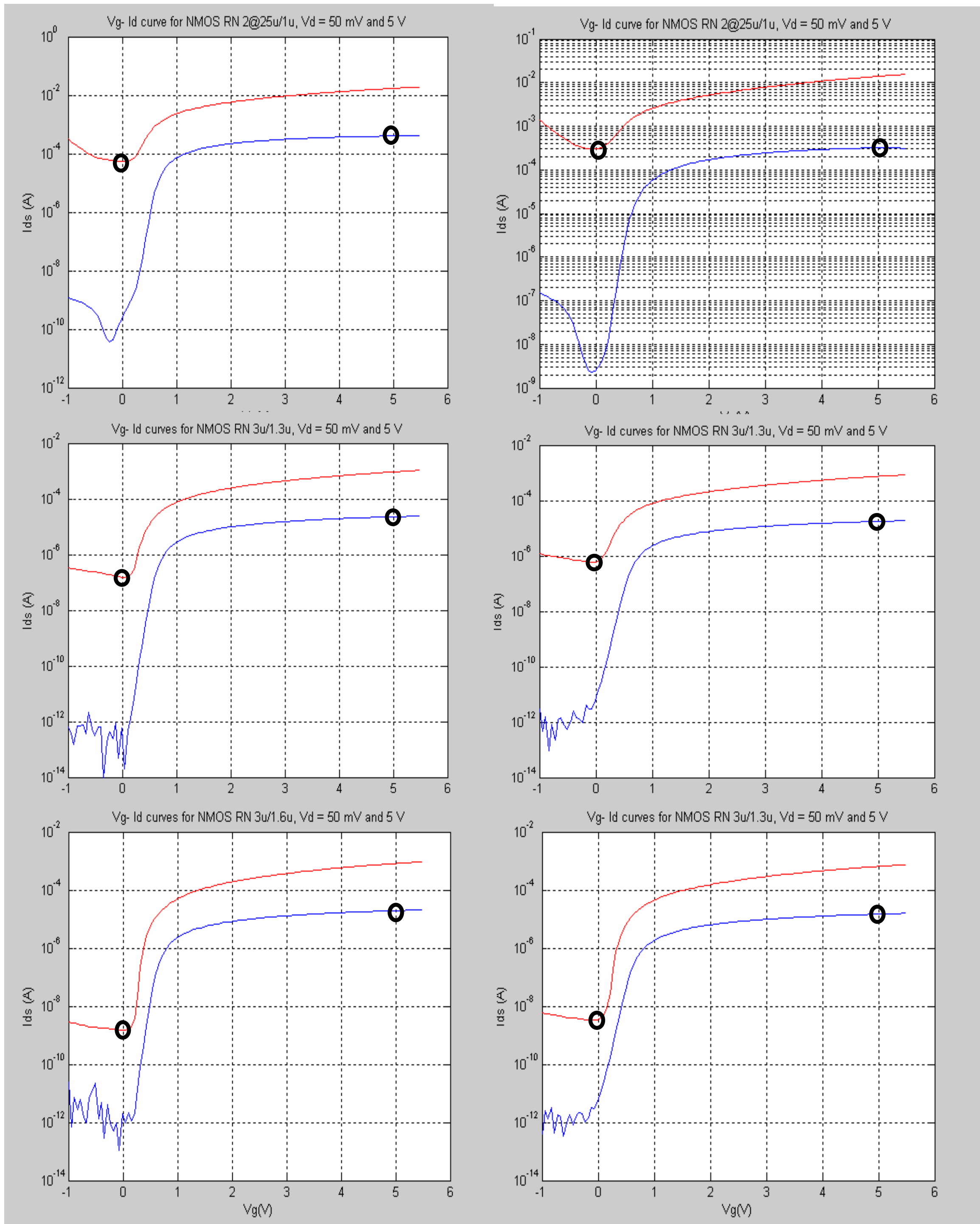


Figure 3.4 Plots for Ion and Ioff at RT (left) and 125°C for NMOS device with length of (a) 1µm, (b) 1.3µm and (c) 1.6µm

With lengths of both devices fixed, widths are sized up to meet the driving current requirements. For optimal noise margins, devices are beta matched and dimensions for devices are finalized with (4.6µm/0.5µm) for a 1X PMOS device and (7.4µm/1.6µm) for a 1X NMOS device. Schematic view for an inverter is generated using the above mentioned dimensions for devices and is simulated for VTC curve, inverter source and sink currents. Plots for VTC curve, derivative of VTC curve, Isink and Isource are shown in figure 3.5 below. It can be observed from the plots that the drive current requirement of 1mA for a 1X drive gate is met with the chosen dimensions.

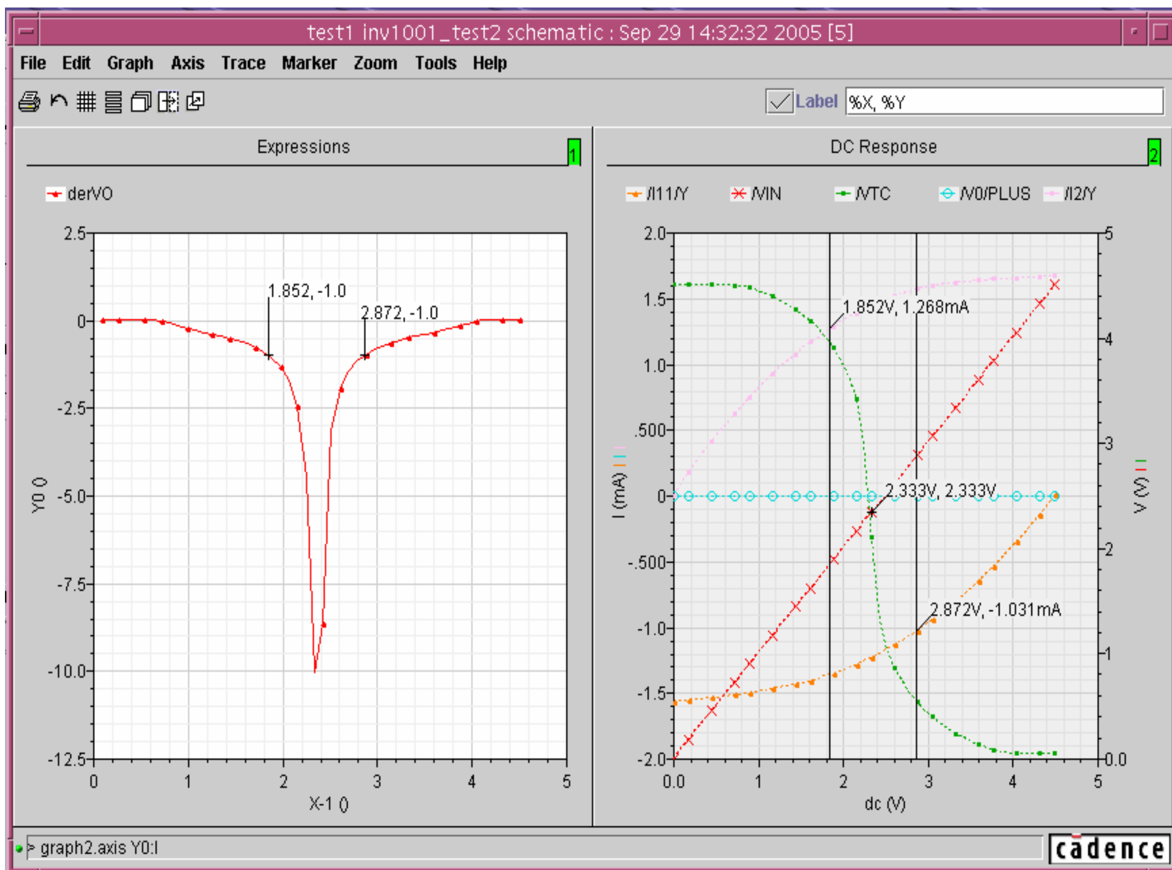


Figure 3.5 VTC curve, its derivative, Isink and Isource of an inverter (at TJ=27°C, Typical process, VDD= 4.5 V)

3.4.2 Layout methodology

This section illustrates how the cells were created using manual layout techniques in cadence virtuoso layout editor. Layout uses standard cell technique where signals are routed in polysilicon perpendicular to the power. This approach results in a dense layout for CMOS gates. Once lengths and widths of transistors are finalized as explained in the earlier section,

1. Cell height is chosen to be the lowest possible integer multiple of metal1 routing grid that could accommodate most complex cell in the library such as a flip-flop. This way it is ensured that any other cell in the entire library would fit in that fixed cell height.
2. All cell pins are placed on grid points, thus avoiding slow off-grid routing.
3. Pins are staggered wherever possible allowing for easier pin access by the router.
4. Physical verification is performed to make sure cells are DRC and LVS violation free.
5. Though there are no errors existing in the layouts, there might some showing up when two cells are placed side by side. So, there should be some spacing (at least half the amount of spacing required to avoid DRC violation for every layer used in cell layout such as metal1, poly, nlocos, plocos and pplus) left for every layer from cell boundary, which would ensure no violations present in the final design using this library.

3.4.3 Cell library layout format

3.4.3.1 Power rail width

Power rail width to be used is set by the maximum allowable current per unit rail width or in other words, maximum allowable IR drop across the rail in the design. Using the switching power equation $P = CV^2f$ and solving for current, switching current is estimated to be 24mA for a 3mm x 3mm die assuming 50 to 60 gates would be placed across the die (when placed with cells abutted and alternate rows flipped). Using sheet resistance value for metal1, found to be 8kΩ/µm from the Peregrine foundry manual, maximum allowable current is set to 4mA/µm thereby setting power rail width to be 5.8µm (integer multiple of 2.2 nearest to 6µm).

3.4.3.2 Cell height, cell width and grid spacing

Layout format followed in developing the standard cell library is shown in figure 3.5 with layout rules and values summarized in table 3.1. The power rails are 5.8um wide, routed horizontally in metal1. The I/O of the cell is routed vertically in metal2 over the cell, connecting to terminal pins defined by labeled metal2-metal1 pins. All I/O pins are placed on a gx by gy grid to get increased efficiency with place and route tool. All cells will be n*gx wide where n is a lowest possible integer that accommodates the cell. Since there is over-the-cell routing, I/O terminals can be placed anywhere on the predefined grid points. Also since routing tools use fixed-grid three-level routing, the terminals must have a center-to-center spacing along both axes. All metal1 must be wholly contained between the power rails; only polysilicon and locos are allowed to extend to within ss of

the cell boundary. Metal3 when used runs horizontally while metal2 runs vertically. The grid spacing gx and gy are set respectively by the minimum spacing requirement between two m1-m2 vias and m2-m3 vias. The routing grid is chosen to be 2.2um for metal1 and metal2 and 2.4um for metal3.

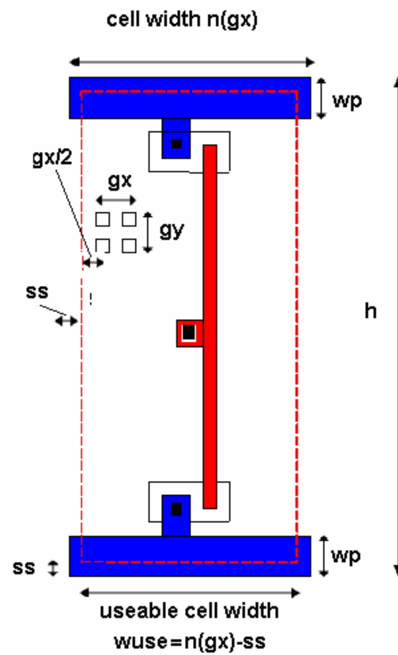


Figure 3.6 Layout format for logic cell library

Table 3.1 Geometry definitions and values

Parameter	**Values**	**Comments**
g_x	2.2um	Horizontal grid spacing (isolated metal width)
g_y	2.2um	Vertical grid spacing
s_s	0.5um for metal1 0.4um for poly 0.5um for nlocos and plocos 0.5um for pplus	Safety zone required to avoid abutting DRC errors
w_p	5.8um	Power rail width
h	74.8um	m equals 34
w_{use}	$n*g_y$ - $2s_s$	n must be an integer

3.5 Schematics, symbols, extracted views and abstract views

For each cell layout (figure 3.9) in the library, there exists a schematic view (figure 3.8) drawn using cadence schematic composer for the purpose of simulation of logic for the design. Schematic views are also used for physical verification (LVS). Extracted views are created for every layout using diva extraction tool. These are more realistic views as they can include every parasitic capacitor derived due to devices, interconnect wires and power rails and thus give more realistic simulation results when characterized. Netlists generated from extracted views will be used for LVS verification. Abstract views (figure 3.10) are generated for all the layouts using Cadence abstract generator. First Encounter uses these abstract views for automatic placing and routing along with Library Exchange Format (LEF) file (generated using Cadence abstract generator along with abstract views) while virtuoso layout uses them during design exchange when DEF file is imported.

3.6 Snapshots of cells

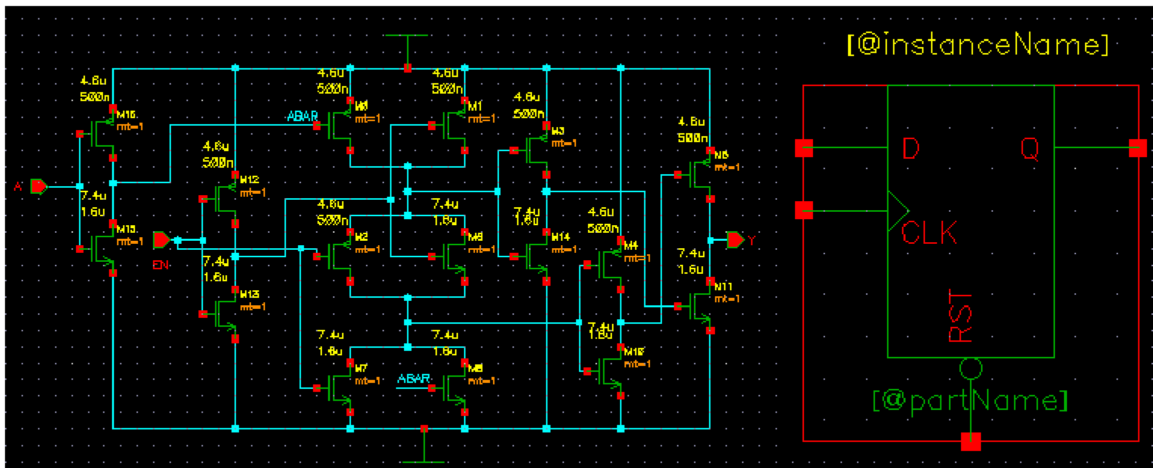


Figure 3.7 Schematic and Symbol view of a positive edge triggered Flip-Flop

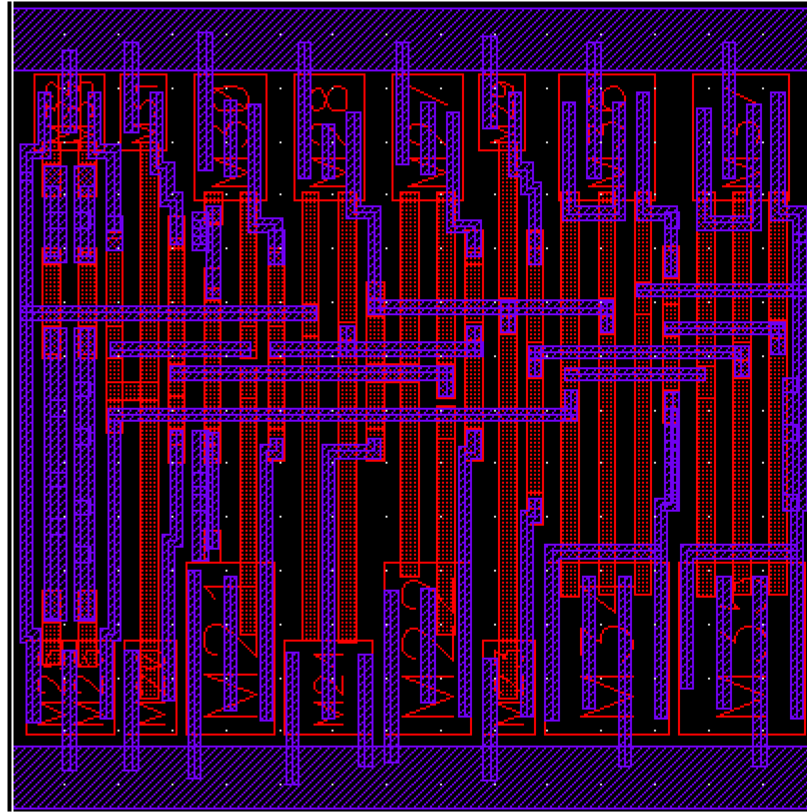


Figure 3.8 Layout View of a positive Edge Triggered Flip-Flop

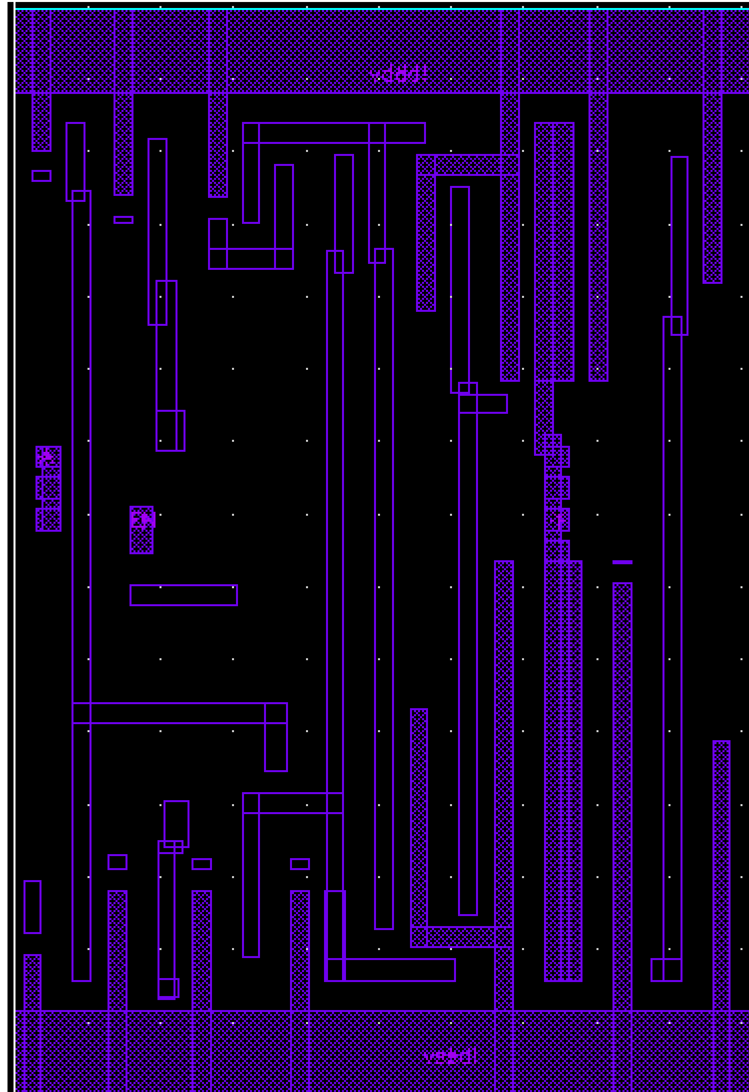


Figure 3.9 Abstract View of a Positive Edge Triggered Flip-Flop

CHAPTER 4

TIMING LIBRARIES: MODELING AND CHARACTERIZATION

4.1 Introduction

Standard cell characterization is the process of generating a simple model for each of the cell in the standard cell library with parameters like cell delays, logic/function, timing constraints and leakage power defined. Functional/delay simulation and power extraction at the chip level for the whole design for GDSII netlist with no pre-characterized cells down the hierarchy takes huge amount of time. Also extraction of functionality and automatic detection of timing constraints are complicated at that level. Hence pre-characterization of standard cells with respect to various driving and loading conditions at cell/gate level and storing the obtained data in standard format are necessary. Characterization flow diagram depicting is shown in figure 4.1 and the flow begins with extraction of netlist and specification of operating conditions. This step is followed by measurement of timing delays using simulation tools, generation of characterized data in specific format timing files and verification of the timing files to ensure the correctness of the characterization data. Synthesis, simulation and place and route tools use these libraries for acquiring timing delays and logic or functional description during design realization, verification and optimization.

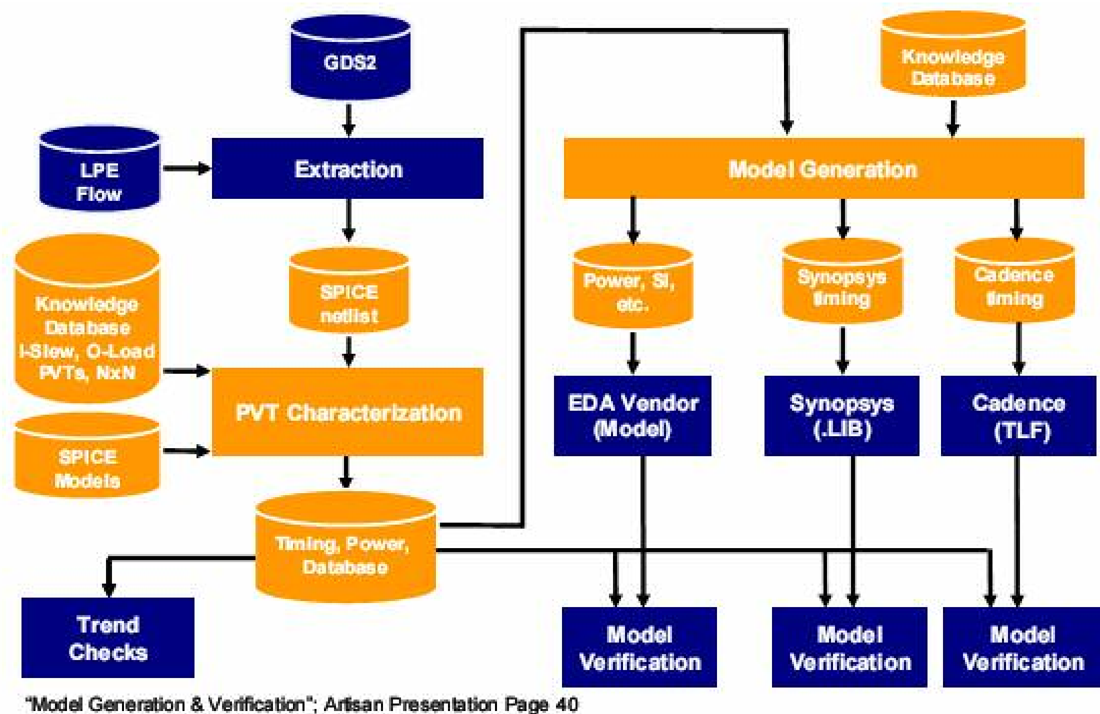


Figure 4.1 Characterization flow[21]

4.2 Technology libraries

4.2.1 Components of Technology Library

Characterization of a cell library generates a technology/timing library which is a text file containing information regarding timing and functional characteristics of an ASIC cell library. Several components of a technology library used by an ASIC design at various phases of design procedure are listed below:

1. Global parameters – These include PVT corner specifications (V = 5V ± 10%; T = 27°C, 125°C), unit definitions, threshold values for input and output transitions and maximum output capacitance and slew limits.
2. Functionality for mapping during synthesis and functional simulations.

3. Area, power, timing constraints and delay values for optimization and delay simulation.
4. Pin locations, geometry of cells, routing blockages and grids for place and route.

4.2.2 Technology library structure

Technology library structure for Synopsys Liberty Format (.lib) which is the most common format used is shown in figure 4.2. It includes cell descriptions and environmental descriptions as detailed below.

1. Cell descriptions define each individual cell in the ASIC cell library,.including cell, bus, pin, area, function, and timing. It includes
   - Structural information – Describes each cell's connectivity to the outside world, including cell, bus and pin descriptions.
   - Functional information – Describes the logical function of every output pin of every cell so that the synthesis tools can map the logic of a design to the cells of the library. Cells without functional description are untouched during synthesis and optimization
   - Timing information – Describes different delay parameters for pin-to-pin timing relationships and delay calculation for each cell in the library. This information ensures accurate timing analysis and timing optimization of a design.
2. Environment descriptions define default cell attributes, values of the components of the delay scaling equations, effects of variations in manufacturing process, operating temperatures and supply voltages on the technology data and

interconnect wire resistance and capacitance for interconnect estimation. All this is the information that is not unique to individual cells and applies to the entire set of cells.

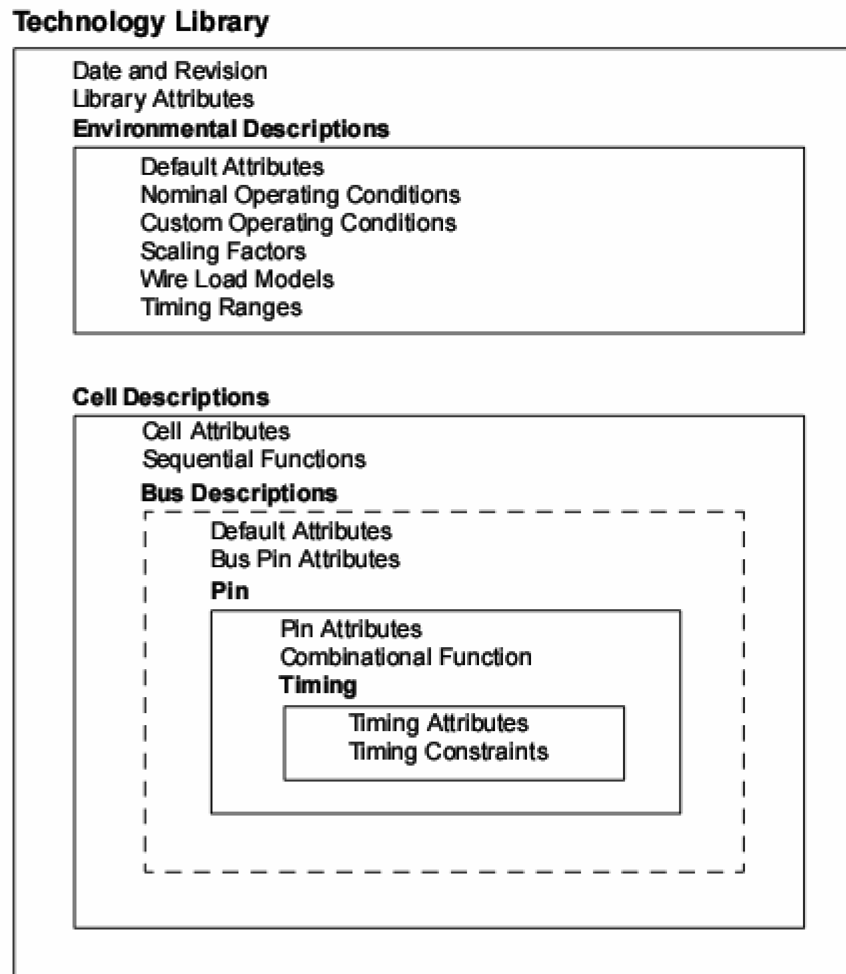


Figure 4.2 Technology library format[13]

4.3 Delay models

Circuit performance heavily relies on the accuracy of timing library since timing analysis like dynamic simulation, static timing verification and speed-or-power optimization performed at chip level use the data from the timing libraries. Delays of a circuit depend

on device characteristics, circuit topology, transistor sizes, parasitic and interconnect capacitors, node capacitors and input waveform shapes. Listed here are various delay models simplified up to different extents for achieving increased computational speeds while sacrificing the accuracy.

- CMOS generic delay model
- CMOS nonlinear (table-lookup) delay model
- Scalable polynomial delay model
- CMOS piecewise linear delay model

The delay module chosen for generating timing data for a library is applicable for all the cells in the library. Each component of each delay model equation is affected differently by variations in the manufacturing process, operating temperature and supply voltage. Nonlinear delay model is chosen for this project. It uses lookup tables and data interpolation techniques for computing delays giving more accurate delay predictions. As a result, the model is flexible enough to provide close timing correlation with a wide variety of submicron delay modeling schemes [12].

4.3.1 CMOS generic delay model

CMOS generic delay model which is based on the linear RC (resistor-capacitor) delay modeling technique is known to be optimal in terms of memory usage and computational speed in the contest of logic and physical synthesis but at the cost of accuracy. Modeling digital CMOS circuits by linear RC networks has demonstrated to be successful in digital timing analysis for following reasons:

1. It consumes lesser time performing numerical integrations during timing simulation.
2. Interconnect delays modeled as distributed resistances and capacitances can easily be taken into account in the linear RC network.
3. It can model timing also for MOS structures like pre-charged logic, pass-transistor buses, static and dynamic storage cells.
4. Timing simulators and analyzers based on linear RC model have computation speeds close to that of switch-level logic simulators.

However CMOS generic RC delay model is an over-simplified linear model and cannot guarantee reliable accuracy of nonlinear MOSFETs. This model assumes input waveform to be a step with infinite slope ignoring the propagation time of the input signal exhibited due to its finite-slope.

4.3.2 Piecewise-linear timing delay model

Nonlinear timing data generated can be greatly simplified in terms of computation using simple piecewise linear model. Outputs of the digital cells, during transition either from GND to VDD or from VDD to GND, exhibit exponential tail regions (rest can be approximated to be linear) due to their inherent resistance and capacitance. Linear model approximates the slope to be linear neglecting exponential behavior at tail, which provides highly inaccurate results as this might cause inaccuracies in the later stages driven by this stage as well. For providing more accurate while still achieving computational simplicity, an n segment piecewise linear curve fitting technique is employed where n is the number of segments into which the slope or transition is divided.

n is usually 2 or 3 set based on accuracy needed. This helps in approximating huge data by few simple delay formulas thereby decreasing the complexity during timing analysis. One other method of simplifying nonlinear delay values using piecewise linear model is to break the data into different sets for each range of load capacitance and then linearize in the region.

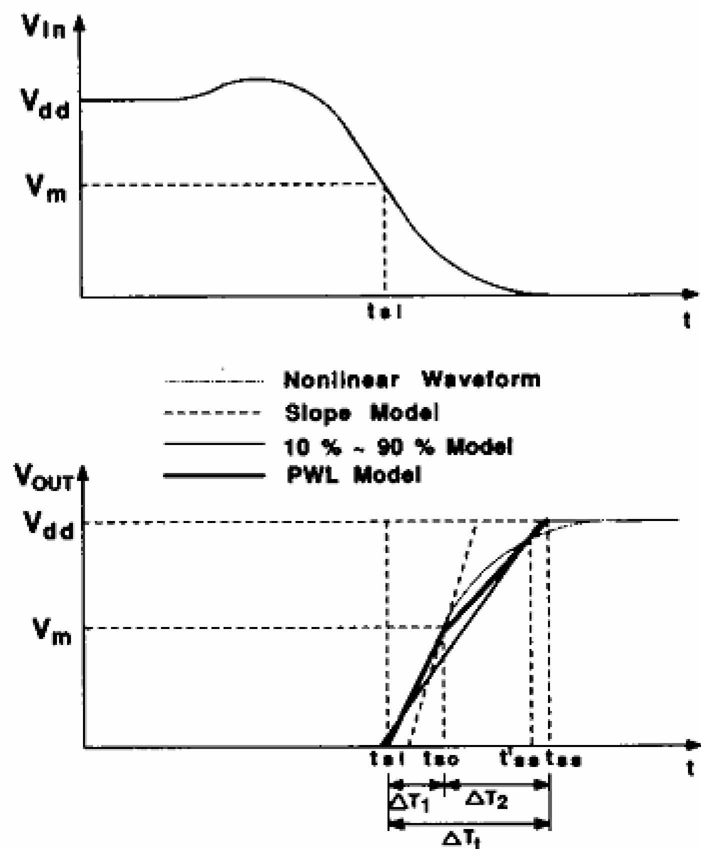


Figure 4.3 Approximation of nonlinear transition using different delay models[20]

4.3.3 Scalable polynomial delay model

Though nonlinear delay models are highly accurate, accuracy doesn't vary much for majority of the cells in the technology library that behave well in timing vs. output load and input transition. Also it is difficult to derive a single nonlinear equation that fits all

the values derived for a timing arc. Thus scalable polynomial method has evolved that tries to reduce the order of analytical function using table lookup values and form a scaled down equation. Taylor series expansion is the highly used technique while generating scalable polynomial. It has got an advantage of including temperature and voltage as parameters of the polynomial thereby eliminating the need for having multiple libraries for different operating conditions. Some tools like library compiler support the conversion of nonlinear delay model into scalable polynomial delay model. By scaling down of appropriate parameters from the analytical function,

1. Memory usage is significantly improved.
2. Computational speed is increased.
3. Accuracy can be still be retained by leaving cells with complex tables (for which curve fitting is not possible or complex) in table lookup format and working with the rest.
4. Entire range and specified variable domain is specified ensuring continuity and completeness.

4.3.4 CMOS nonlinear delay model

For reflecting various nonlinear effects in MOS circuits, reliable circuit simulations or measurements are performed to generate timing data for standard cells (being the most typical subcircuit structures) with various driving and loading conditions. And the huge data obtained is stored in the table lookup format to generate nonlinear delay model. One big advantage of storing data in table formats without manipulating with it can be seen in cases where there exists no closed form equation for modeling certain behavior. In this

case the solution would be to use nonlinear table lookup model and used interpolation techniques for calculating delays. Major drawbacks of using table lookup model are its memory consumption and adverse impact on synthesis speed. Two dimensional delay tables have to be limited to lower sizes, typically 5x5. Large tables sized about 64x128 are difficult to handle for the above said reasons. Thus accuracy at that level has to given up. Also because nonlinear dependencies of delays upon various factors like voltage and temperature need for adoption of 3D tables has arose making it non-feasible to have larger tables. Scaling technique that has been used so far for taking different operating conditions into account is fount to be inaccurate and thus multiple technology libraries at different operating conditions are loaded while synthesis and simulation.

4.3.4.1 Delay components

Total delay between the input pin of a gate and the input pin of the next gate has two major components: cell delay (D_{cell}) and connect delay (D_c). This can be expressed as

$$D_{total} = D_{cell} + D_C$$

1. **Cell delay:** Delay contributed by the gate itself is called the cell delay. It is typically measured from 50% of the input pin voltage to the 50% of the output pin voltage. D_{cell} is calculated as the sum of transition delay ($D_{transition}$) and propagation delay ($D_{propagation}$).
    a. **Propagation delay:** Time from 50% of the input voltage until the output pin just begins to switch (typically 20%). rise_propagation and fall_propogation are the timing groups defining propagation delay tables.

b. **Transition delay:** Time required for an output pin to change state, typically measured from 20% to 80% of the final value. Transition delay can also be constrained as a design rule. $D_{transition}$ is a function of output capacitance and input pin transition. rise_transition and fall_transition are the delay groups used in the transition delay tables of a technology library.

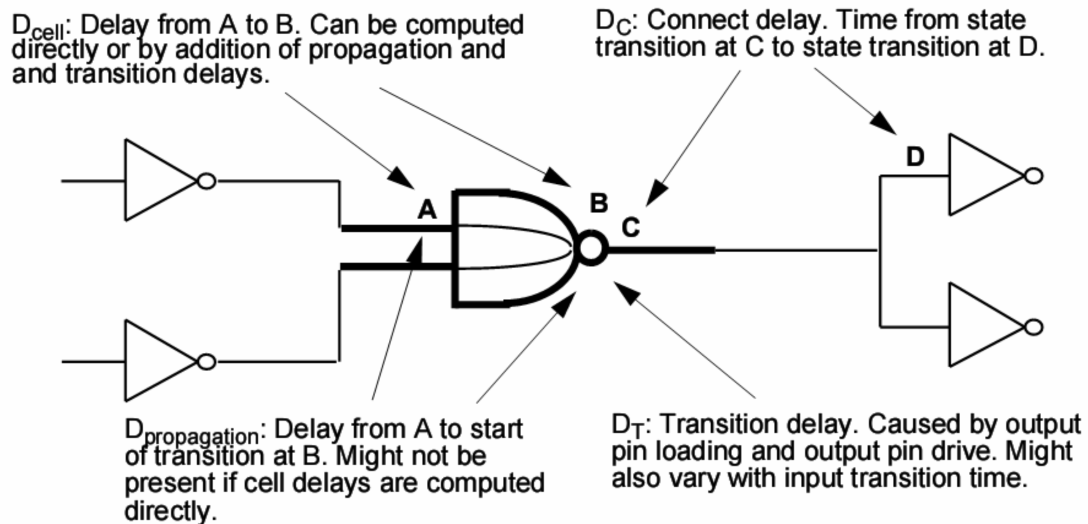


Figure 4.4 Delay components for CMOS nonlinear delay model[12]

Cell delay is usually a function of both output loading and input transition time (input slew rate). If cell delay tables are defined in the library file, propagation delays must not be defined. Two groups in the timing group of the library defining cell delay tables are cell_rise and cell_fall accompanied by rise_transition and fall_transition that are used for looking up delays for the next stage from the delay table of the cell followed by the current one.

2. **Connect delay:** It is the time taken by an input pin to charge after the pin driving it has made a transition. It is also called wire delay since it is the time taken by a

waveform to travel along the wire connecting driving output pin to the input pin. There are three cases representing different models for estimation of interconnect delay are shown in figure 4.5.

a. **Best_case_tree:** It models the load pin to be physically adjacent to the driver implying that only wire capacitance has to be considered ignoring the wire resistance. Hence this models leads to a zero interconnect delay but increases transition delay due to additional wire capacitance.

b. **Worst_case_tree:** It models the load pin to be at the extreme end of the wire. This model includes full wire capacitance and full wire resistance. Connect delay is calculated to be $D_{Connect_{worst}} = R_{wire}(C_{wire} + \sum_{pins} C_{pin})$.

c. **Balanced_tree:** It models all the load pins on separate, equal branches of the interconnect wire implying that each load pin incurs an equal portion of the wire capacitance and wire resistance giving the delay of

$$D_{Connect_{balanced}} = \frac{R_{wire}}{N}\left(\frac{C_{wire}}{N} + C_{pin}\right).$$

R_{wire} is estimated by scaling the resistance factor specified in the wire_load group up to the length of the wire. C_{wire} is estimated using fanout_length, number of fanout pins and capacitance factor specified in the wire_load group.

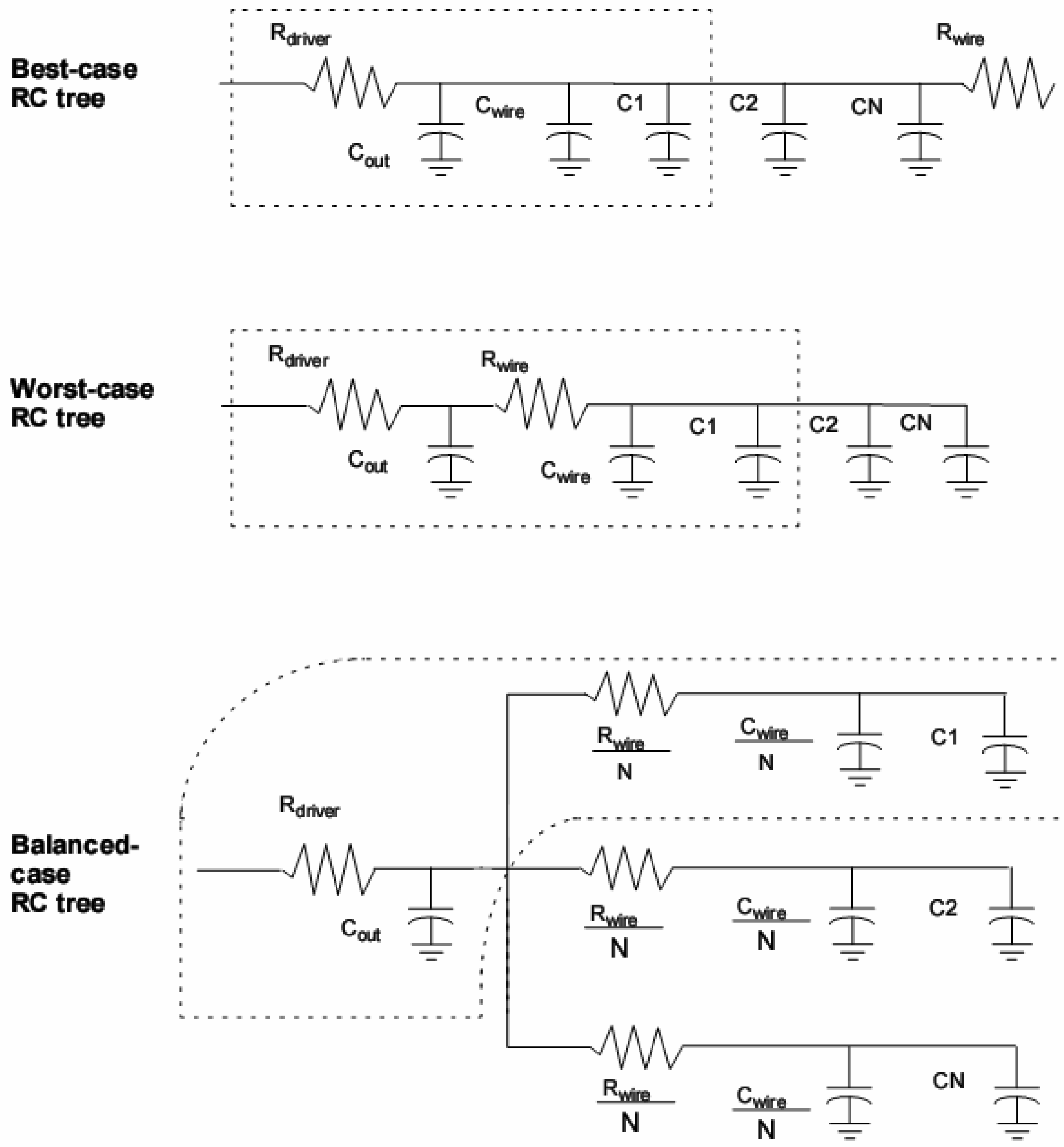


Figure 4.5 Modeling of connect delay [12]

4.3.4.2 Delay calculation using data interpolation

For calculating falling delay of cell U1 in the delay calculation schematic in figure 4.6, slew/transition time at node N0 and output load capacitance at node N1 are required since the delay tables for cell U1 are indexed by its input slew and output load. Rise transition

at the node N0 is to be considered since the timing sense for cell U1 is negative unate. Rise transition at node N0 is obtained from the previous stage U0's delay table for its corresponding input slew and output load (which is loading at node N0). Load at node N1 is calculated to be the sum of the input pin capacitance of the cells connected to that node and the capacitance contributed by the wire itself (calculated using wire_load model). Once the input transition and output load for cell U1 are obtained, corresponding value from the delay table is taken as cell delay for that stage.

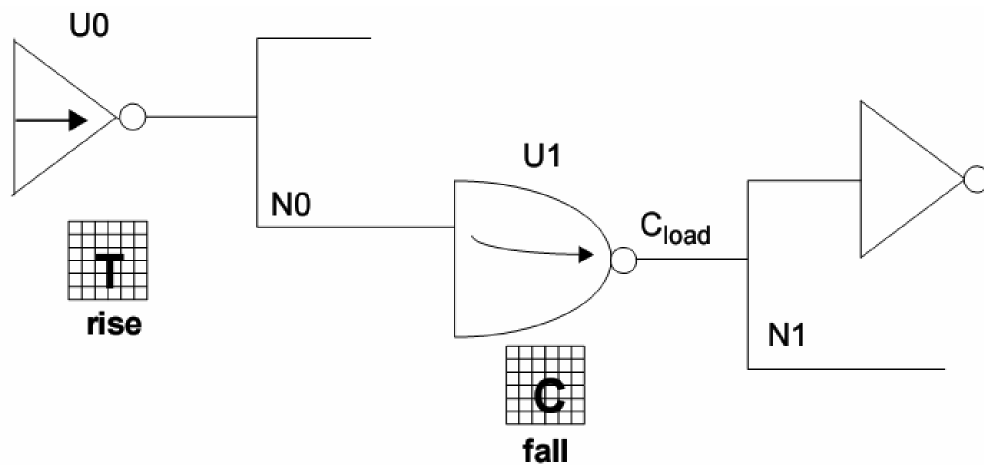


Figure 4.6 Nonlinear delay calculation schematic [12]

If either the calculated transition time at N0 or the load capacitance at N1 is not indexed in the delay tables of the cell U1, then data interpolation technique has to be used. Four neighboring table values as shown in figure 4.7 are determined first by examination. With the use of curve-fitting techniques, coefficients for the equation of the surface embraced by the four points are obtained. Equation for the surface can be represented as $Z = A + B.X + C.Y + D.X.Y$ where, Z is the delay of the cell to be calculated, X is the input transition time, Y is the output load capacitance and A, B, C and D are calculated coefficients.

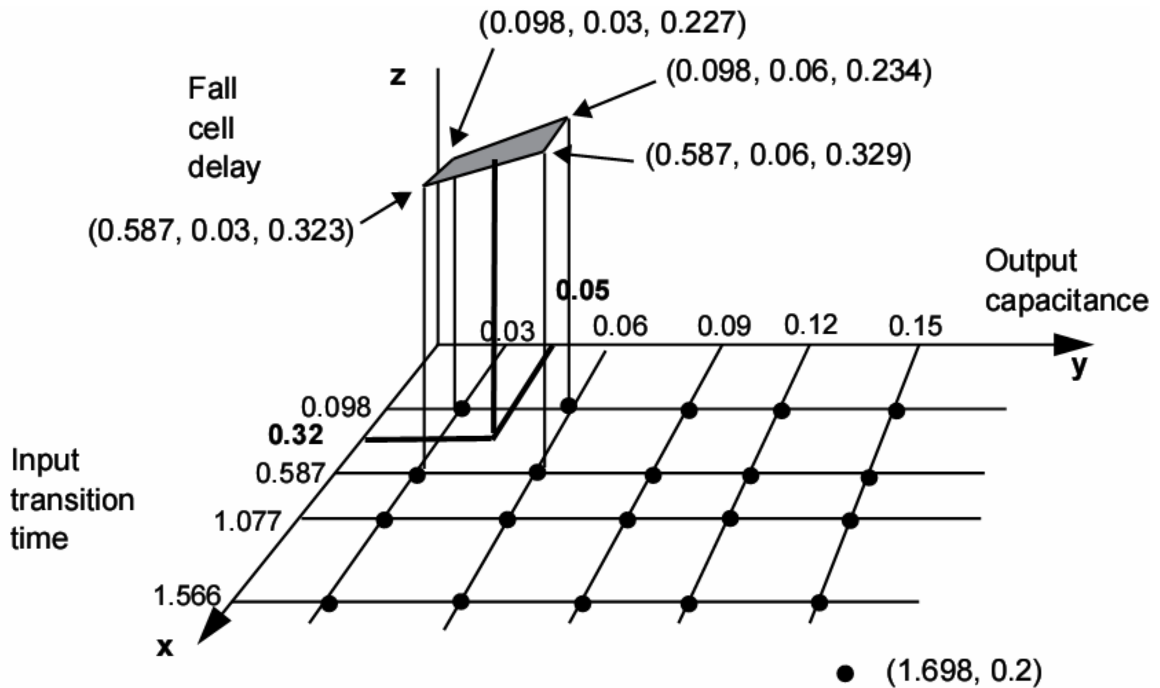


Figure 4.7 Data interpolation using table lookup delay model[12]

4.4 Characterization using SignalStorm

The SignalStorm library characterizer is an automatic library characterization tool that generates characterization data for logic, delay, and power models, non-linear driver models, and gate capacitance information based on model files for the devices, transistor connectivity for the standard cells and simulation conditions such as voltage, temperature, process corner parameters, waveform measurement levels, loading capacitance and input slew rates. It outputs all of the extracted characteristics of the cell library in an industry-standard advanced library format (ALF) file which can be converted into library compiler, Verilog and VHDL libraries and documentation in HTML format.

4.4.1 Characterization techniques

Since SignalStorm is just an automatic tool for characterization based on the parameters user gives, it lacks any intelligence that has to do with design details of specific topology implemented by user. There are several parameters and commands that can be played and tweaked with for obtaining best out of that tool. Setting right values for parameters comes with design experience and understanding of the circuit behavior and highly depends on the design requirements. (rise/fall) of a library can be obtained by performing analytical calculations Some of the important parameters to be set are

1. Input slew times – based on how slow the outputs of the majority of the standard cells are falling or rising over a range of typical output loads that might occur in the design, input slew times in the index statement are to be fixed. This ensures that the delay value to be calculated in the design falls within four neighboring points around. Also the increments in the values of consecutive slew rates to be specified are based on the tradeoff of memory consumption/computational speed and accuracy requirement. Value of maximum output slew defined for the library (explained in the next point) is used for setting upper limit under slew definition. And as low a slew time as a simple gate's (inverter) transition time or f_t of the process can be used for setting lower limit in the index statement. Typically, incremental values used for slews should be such that it generates a delay table with a dimension of 5 or 6 across slew time.

   Fastest transition time or by simulating in analog environment [might be for an inverter with highest drive strength cell of all available drives with least amount of load]. This should be the fastest slew time in setup file. Slowest slew time

should be maximum allowable output slew for the given library. Selecting these values as explained so will give better results than selecting a smaller window because, for the input slew values outside the window may result in interpolation of delay values with only two adjacent values as compared to four while any timing analysis.

2. Maximum allowable output slew – based on this value the maximum output load that each cell can drive is generated in the output file. Synthesis and place and route tools use the value for maximum output load that can be driven by a cell during timing optimization. The value to be chosen for this variable in simulation setup file depends on the frequency requirement of the design, how fast the cells in the library behave which in turn depends on transistor sizing. Typically, a design with 1X drive capability can be made to drive up to 3X load with not much increase in transition times and output delays observer. Based on a general idea on how fast the outputs of cells in the library are to be rising and falling and by desired behavior of a most complex cell, two times or three times the transition time obtained with 1X load can be set to be the maximum output slew. This might have to be reiterated sometimes based on the design under consideration.
3. Nominal statement –A single timing arc for output transition of a cell with respect to a related pin's input transition can occur for more than a single combination of logic states of non-related input pins. Each of those input combinations gives rise to a different value for delay all of which correspond to the same timing arc. From the range of the different values obtained for delay, nominal statement can be used to to chose the value for delay that has to be provided in the output timing

file. Considering minimum value of delay to be the nominal value might cause setup timing violation whereas considering maximum value of delay to be the nominal value might cause hold timing violation. Knowledge of setup and hold timing values helps in setting nominal statement. If hold timing seems to be larger than setup time, it might be difficult to meet hold time constraint. So nominal value chosen should be towards lower side.

The Parameters required for characterizing a flip-flop are selected as follows:

Input slew times and output loads that are to be selected in a similar way as for combinatorial circuits

Binary search:

Start - The value assigned to this parameter should be a simulation point of Data transition lead with respect to active clock edge for which setup timing constraint is guaranteed to meet. You can be liberal in choosing this value except that it might take bit more of a time for convergence. You should perform simulations before you know that what you are providing is a pass point. It is not worthy to spend much time on this since if you can pick some value and start running simulation, SignalStorm should issue an error message saying that the timing is not converging.

End - The value assigned to this parameter should be a simulation point of data transition lag with respect to active clock edge for which setup timing is guaranteed to fail. The explanation under "start" parameter holds well for this "end" parameter.

Resolution - The maximum value of error in setup/hold time that is tolerable for you library. Resolution should be a value less than the delay of fastest gate in your cell library.

4.4.2 Setup and hold time characterization

SignalStorm library characterizer uses binary search technique for characterizing input timing constraints (setup time, hold time, release time, removal time) for sequential logic.

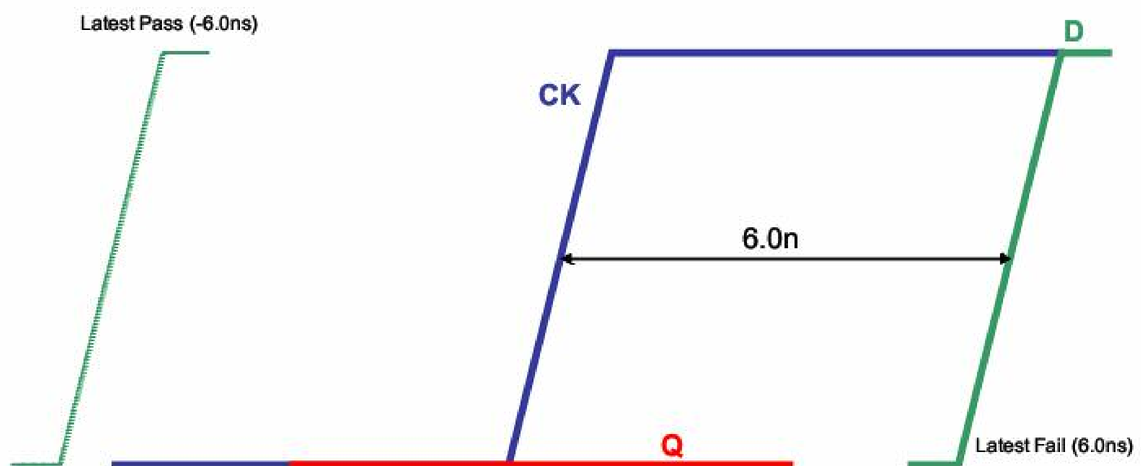


Figure 4.8 Binary search step used in SignalStorm[14]

Under simulation statement, for 'bisec' parameter in setup file, two values for time are provided of which first one should be a guaranteed pass point and second one should be a guaranteed fail point. A guaranteed pass point has to be an amount of time lead of data over clock such that the estimated setup time constraint is met. Similarly, a guaranteed fail point has to be an amount of time lag of data with respect to clock that would violate the setup timing requirement. Based on whether the current simulation point passes or fails, either latest pass point or latest fail point is updated. Any simulation point thereon

would be an average of the latest pass point and the latest fail point. Simulations are repeated until the resolution specified in the 'bisec' parameter (third value) is met. Simulation point at any time is calculated to be D – CK = (latest pass point + latest fail point)/2, where D – CK is the amount of time lead of data over clock. Hold, removal and recovery times are characterized in a similar fashion with appropriate signs for the first two parameters considered.

4.5 Library formats

There are several types of standard formats existing in the industry for describing library's characterized data. Different tools from different vendors read the same information from the technology libraries in their corresponding formats.

1. Synopsys liberty library (LIB) – is used by Synopsys products for synthesis, timing and power information. This format supports most models, virtually a standard and can be compiled into .db format (Synopsys database format file).
2. Timing Library Format (TLF) – is used by cadence products for synthesis, timing and power information. It has got same feature as that of LIB file and can be compiled.
3. Advanced Library format (ALF) – is more descriptive than .lib format file. SignalStorm generates this file as an output from its database.
4. Ambit Library Format (ALF) – is used by ambit library synthesizer by cadence for synthesis of behavioral verilog.

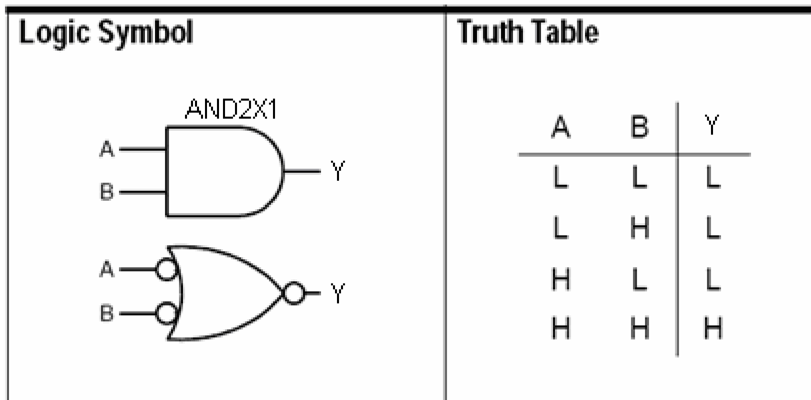
For integration with cadence synthesizer and simulator, SignalStorm generated timing data in ALF file format is converted into Synopsys liberty file format using 'alf2lib'

command in the SignalStorm shell. The same library information needs to be further converted into corresponding formats for integrating with synthesizer (ambit), simulator (verilog) and design compiler (Synopsys). LIB file can be further converted into Ambit Library Format file using 'libcompile' that comes with the cadence ambit synthesizer package. HTML documents are created for timing and leakage power reference using 'alf2html' command at SignalStorm command prompt. Datasheets have digital logic's truth table, Boolean expression, cell schematic, verilog and vhdl syntax, delay tables and node capacitances.

4.6 Data sheet examples

AND2Xx

Description:
AND2X1 is a family of two input gates that perform the logical AND function.



A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

HDL Syntax
Verilog .... AND2Xx *insLname* (Y, A, B);
VHDL................ *insLname:* AND2Xx port map (Y, A, B);

Area	
AND2X1	AND2X8
580.80 μm^2	774.40 μm^2

Pin Loading:

Pin Name	Capacitance (pF)	
	AND2X1	AND2X8
A	0.021	0.021
B	0.021	0.021

Propagation delays (ns)

Conditions: TJ = 25°C, VDDD = 5 V, VSSD = 0 V, Typical process

			Intrinsic Delay (ns)	Transition Delay (ns/pF)
AND2X1	From: A To: Y	tpLH	0.589	0.071
		tpHL	0.594	0.995
	From: B To: Y	tpLH	0.621	0.070
		tpHL	0.741	0.093
AND2X8			Intrinsic Delay (ns)	Transition Delay (ns/pF)
	From: A To: Y	tpLH	1.186	0.120
		tpHL	1.105	0.109
	From: B To: Y	tpLH	1.269	0.103
		tpHL	1.215	0.110

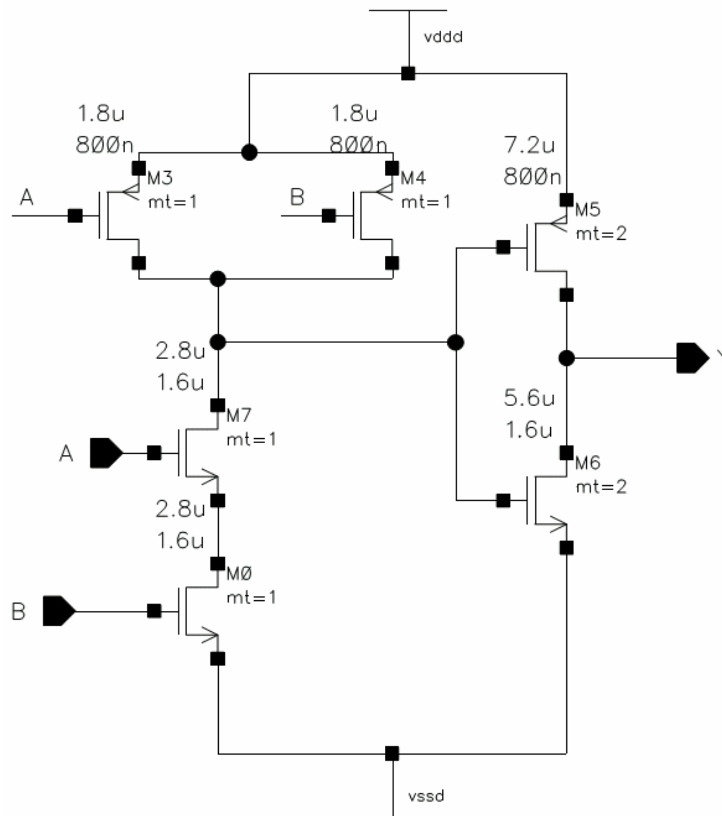
Conditions: TJ = -55°C, VDDD = 5.5 V, VSSD = 0 V Fast process

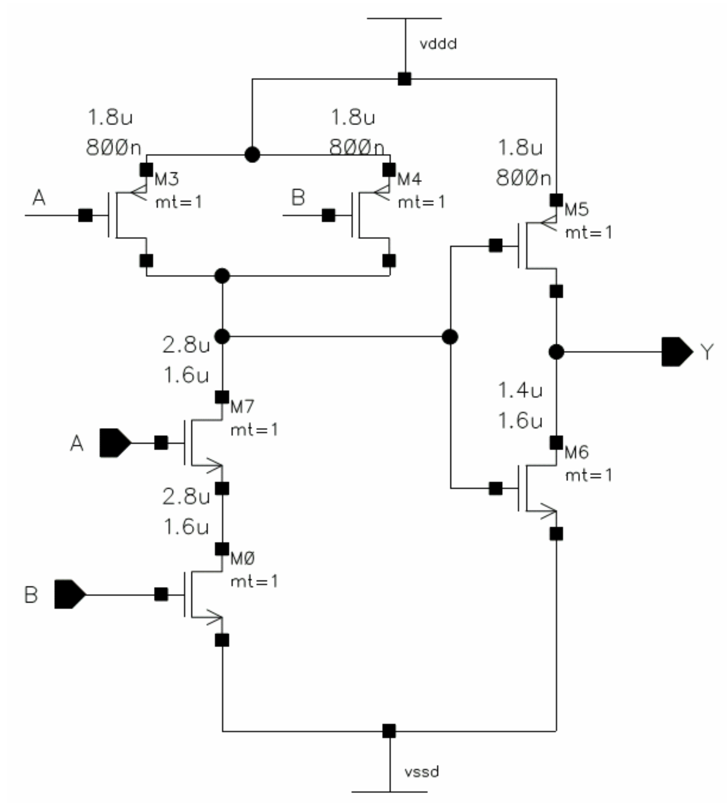
			Intrinsic Delay (ns)	Transition Delay (ns/pF)
AND2X1	From: A To: Y	tpLH	0.360	0.042
		tpHL	0.385	0.051
	From: B To: Y	tpLH	0.356	0.042
		tpHL	0.461	0.054
AND2X8			Intrinsic Delay (ns)	Transition Delay (ns/pF)
	From: A To: Y	tpLH	0.729	0.060
		tpHL	0.735	0.062
	From: B To: Y	tpLH	0.708	0.062
		tpHL	0.788	0.066

Conditions: TJ = 125°C, VDDD = 4.5 V, VSSD = 0 V Slow process

			Intrinsic Delay (ns)	Transition Delay (ns/pF)
AND2X1	From: A To: Y	tpLH	0.968	0.123
		tpHL	0.989	0.171
	From: B To: Y	tpLH	1.087	0.124
		tpHL	1.194	0.176
			Intrinsic Delay (ns)	Transition Delay (ns/pF)
AND2X8	From: A To: Y	tpLH	2.044	0.183
		tpHL	1.861	0.182
	From: B To: Y	tpLH	2.203	0.175
		tpHL	2.035	0.187

Delays vary with input slew rate. See pages 8/9 for input conditions and interconnect estimates.




vddd
1.8u
800n
M3
mt=1
A
1.8u
800n
M4
mt=1
B
1.8u
800n
M5
mt=1
2.8u
1.6u
M7
mt=1
A
2.8u
1.6u
M0
mt=1
B
Y
1.4u
1.6u
M6
mt=1
vssd

CHAPTER 5

CELL LIBRARY VALIDATION

5.1 Introduction

A standard cell based design for implementing digital ASICs has become the routine approach by designers in industry as it provides very high gate density and good electrical performance but more importantly rapid time to market. Standard cells are implemented as functional blocks with known electrical characteristics including; propagation delay, capacitance and power representation in third party tools. An RTL description, constructed based on design requirements using HDL such as Verilog or VHDL, is transformed into a gate-level netlist using a pre-characterized collection of these standard cells. Also placing and routing tool uses the delay, area and power information for achieving optimized solution during chip design. Thus, early validation of characterization data for the standard cells on physical silicon that provides simulation and synthesis accuracy is necessary to ensure the final design implemented in silicon functions correctly over all extremes of the process, voltage and temperature.

5.2 Validation Process

In validating cell library timing models, they should be proven to match actual silicon performance. In the process of validation, NMOS and PMOS devices on silicon are tested

for Id-Vd characteristics, I_{on} and I_{off} characteristics and performance is compared with the model file based simulation data. A test chip was designed to verify timing delays that include parameters based on cell output loading and cell input transition for inverter, 3-input NAND and 3-input NOR gates. The test chip is tested at operating environments that matches with simulation corners to encompass datasheet-specified operating conditions. Since designing a test chip for validating each and every cell from the library is not feasible in terms of cost and time consumption, a test chip for an inverter, a multi-input NAND gate and a NOR gate are designed. Also since an inverter is a basic cell with a single NMOS and PMOS configuration, a NAND gate has stacked NMOS devices in the pull-down circuitry with parallel PMOS devices in the pull-up circuitry and a NOR gate has stacked PMOS devices in the pull-up circuitry with parallel NMOS devices in the pull-down circuitry, most of the configuration cases that might occur in combinatorial circuits are taken care of in the designed test chip. Hence, in the verification of the timing models for inverter, NAND and NOR gates for accuracy, SignalStorm's delay tables are verified to be accurate. Therefore, the generation methodology which is SignalStorm in this case is made a standard method for obtaining timing and thus is employed for characterizing rest of the combinatorial cells in the library with obtained data assumed accurate.

5.2.1 Test Chip Design

For timing delay analysis, the test chip consists of delay chains with several delay modules/blocks in each chain. Inverter, NAND and NOR cell types are instanced in these delay chains as shown in figure 5.1. Delay chains allow for extraction of both intrinsic

and load-dependent cell delays. The delay chains are designed to generate pulses with their widths proportional to delays of chains and large enough to ensure accurate measurement. There is a pulse generated for every transition of input as shown in the figure 5.1. Inverter being a single-input cell is simply chained to generate a pulse whereas multi-input cells like NAND and NOR are chained using only one input with rest of the inputs tied either high or low to result in an output transition. For NAND and NOR chains, an inverter is placed after every NAND or NOR gate so also in addition inverter delay parameters appear in the delay equations and gives a tighter control of the five parameters to be extracted. For determining load dependent delays, load capacitor configurations equivalent to 3X and 6X loads are placed between alternate pair of cells (loading the NAND, NOR etc.) of the delay chain with the choice of switching them in and out of the chain using T-gate switches. Load capacitors are accommodated in the ground rail and are connected at the output pin through T-gates for the existing intrinsic chain itself in order to achieve greater reduction in area as compared to implementing three separate chains dedicated for each of intrinsic, 3X and 6X loads.

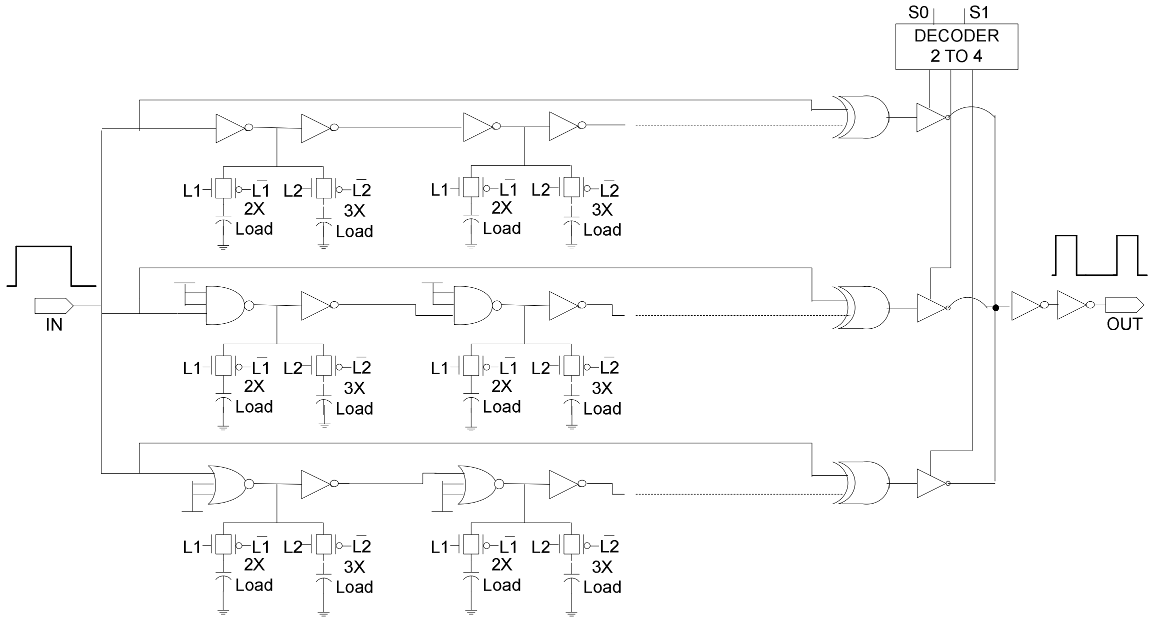


Figure 5.1 Test chip design for inverter, NAND and NOR gate delay testing

A single input pad is used to supply input to all the three chains. Separate power pads are used to power up each of the chains. Two input pads are used for switching T-gates while selecting loads at the output pins of cells. A single output pad is used to observe output data for all the three chains that are connected to a single node through tri-state enabled buffers. Three enable signals for these tri-state buffers are generated using a 2x4 decoder circuitry. Layout for padded out delay chains is shown in figure 5.2. GSG probes are used for supplying input pulse to the chip as well as to take output pulses off the chip to obtain better decoupling. Each device under test (DUT) is followed by an inverter. The optional load cells in between the DUT and the inverter is called a delay module. There are 32 delay modules in the inverter, 42 in NAND and 42 in NOR chains respectively giving easily measured pulse widths. Delay chains consumed an area of 1.5mm x 0.9mm.

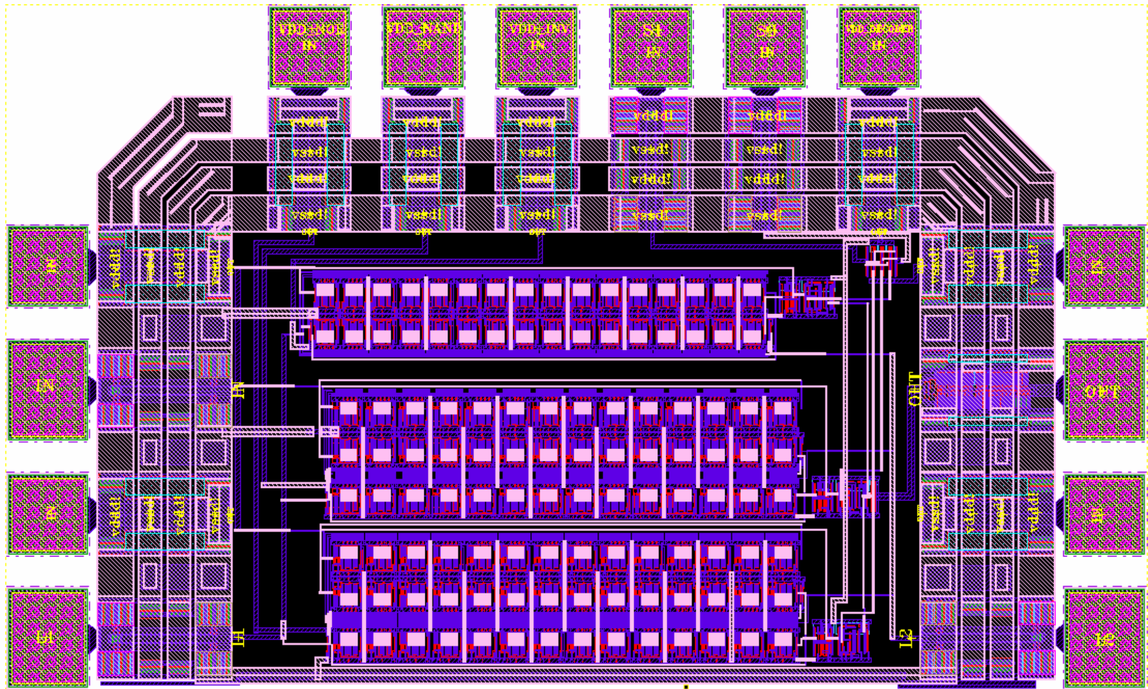


Figure 5.2 Layout view of padded out delay chains

5.2.2 Test Chip Characterization

The Test chip was manufactured at Peregrine Semiconductor fabrication facility on a 3mm x 3mm die. The test chip is then measured at 27°C and 125°C with a supply voltage of 5V, and pulse widths measured to extract intrinsic as well as load dependent configurations for both high-to-low and low-to-high transition timing. Test data for up to 10 dies is taken and tabulated in an excel sheet for further analysis. Since the delay of the chain is given by width of the pulse, it is only a function of the pulse generator circuit and does not depend on input, output and control circuits. An Agilent arbitrary waveform generator, a Tektronix programmable power supply and an Agilent infiniium Oscilloscope (1.5 GHz, 8 Ga/s) are used for measuring test data on a 8" Cascade Alessi

(Rel-6130) semiautomatic probe station. A DC wedge is used to supply power to the chains and inputs to the decoder.

Figure 5.3 Snap of the die on probe station with probes landed

5.2.3 Data measurements

The main purpose of comparing the measured test chip results with by SignalStorm results is to verify that the timing generated for the cell library truly portrays silicon performance. Since SignalStorm results are only as accurate as the database given to it, spice models for NMOS and PMOS transistors obtained from Peregrine foundry are tested for DC characteristics, Ion and Ioff ratios and compared to measured devices. Delay chain data for each delay module is compared with delay values obtained for

corresponding delay module from SignalStorm's slew based model and also with simulation data for each delay module obtained from Analog Enviroment simulation performed for the whole test chip.

5.2.3.1 Device Characteristics

Id-Vd characteristics for a 10/1.6 NMOS device (rn) measured at 27°C and 125°C for 4 units are compared to simulation data for a 7.4/1.6 device with their drain currents normalized per µm of width. Id-Vd characteristics for a 1.2/0.5 PMOS device are also measured and compared with simulation data for a 4.6/0.5 µm device with their drain currents normalized. Both PMOS and NMOS devices are also tested for on-state and off-state currents. Simulation data is plotted for typical, best and worst case processes to encompass all possible ranges of variation in Id-Vd characterisics. Plots for both the devices are shown below and the percentage variations of currents from room temperature to 125°C as well as the percentage variations of the measured data, simulated fast and slow model's data as compared to simulated typical model's data are presented. Plots presented in figures 5.4, 5.5, 5.6 and 5.7 and the table 5.1 with percentage variation of measured data and simulated data at best and worst case corners show that the measured data falls with the skew plots obtained from models with minor exceptions. Table 5.2 gives the percentage variation of the currents at 125°C as compared to the values at 27°C.

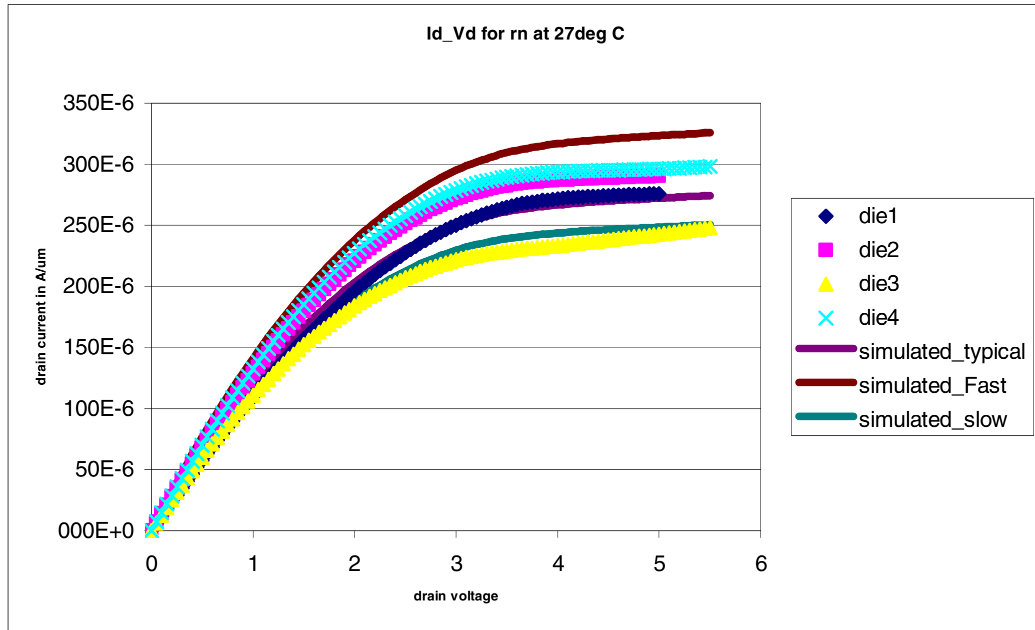


Figure 5.4 Id-Vd curves tested and simulated for 1.6µm length NMOS transistors at 27 C normalized per µm of width

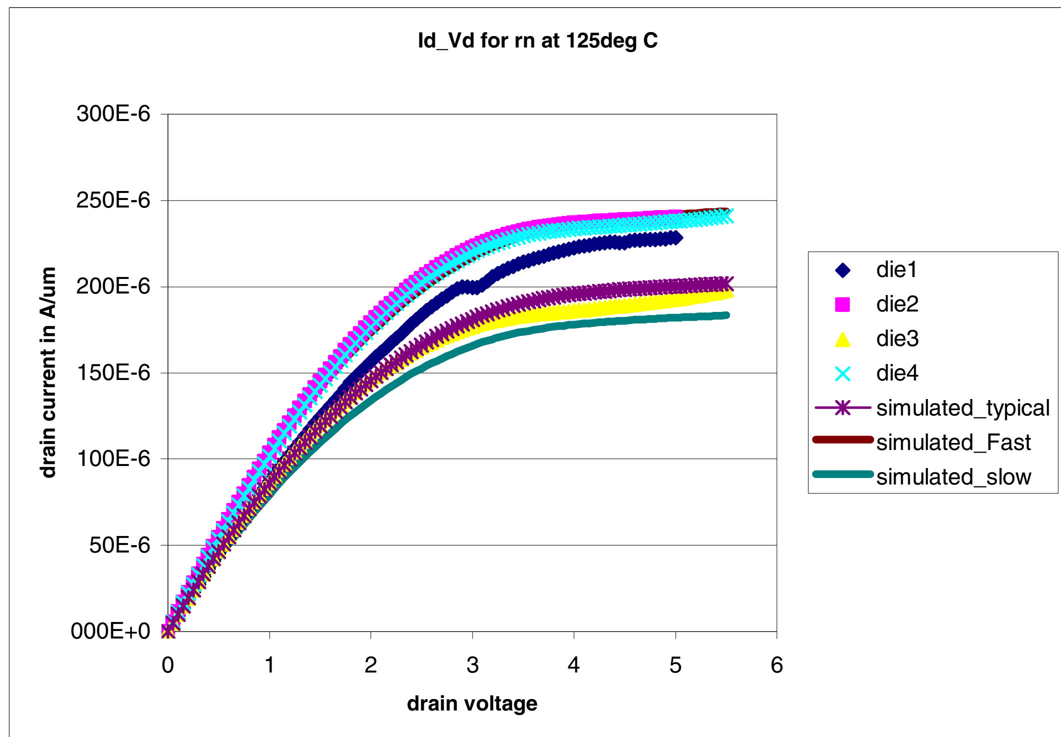


Figure 5.5 Id-Vd curves tested and simulated for 1.6µm length NMOS transistors at 125°C normalized per µm of width

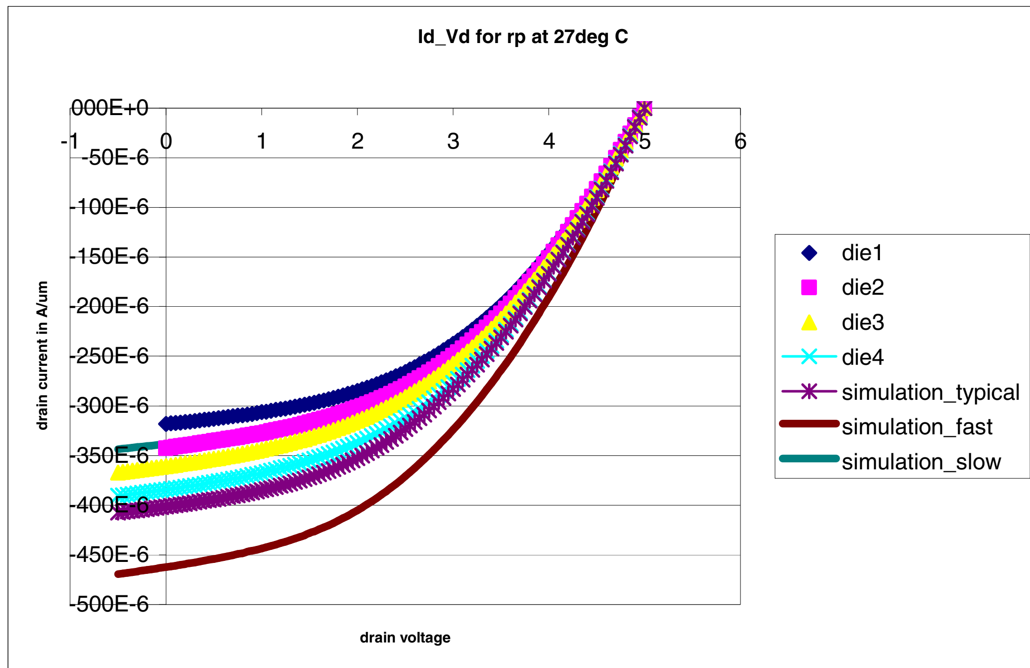


Figure 5.6 Id-Vd curves tested and simulated for 0.5μm length PMOS transistors at 27°C normalized per μm of width

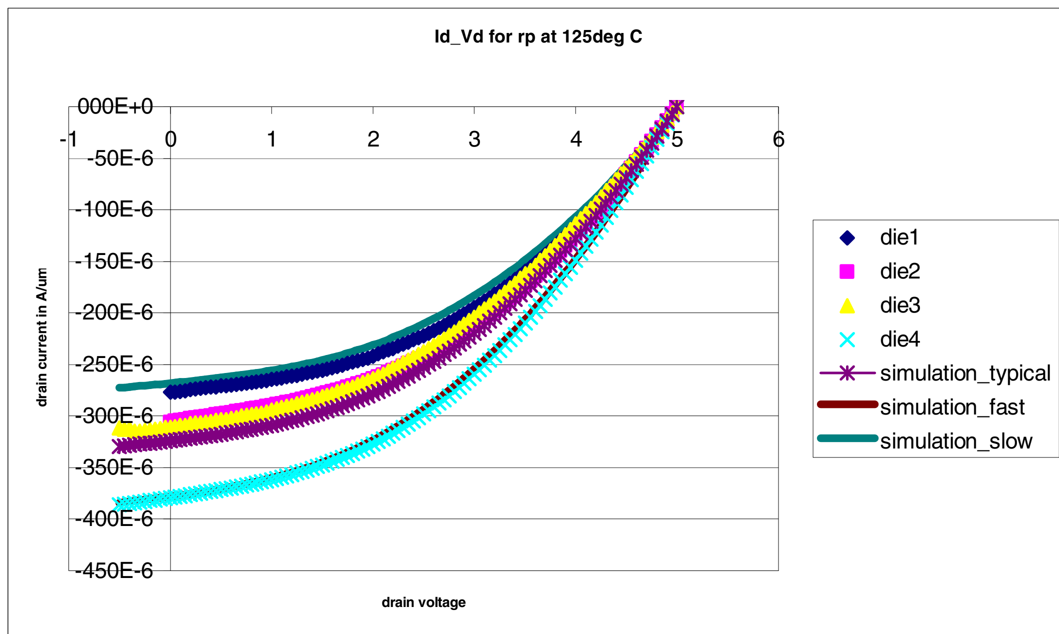


Figure 5.7 curves tested and simulated for 0.5μm length PMOS transistors at 125°C normalized to width

Table 5.1 Percentage variation of measured data and simulated data with fast and slow models as compared to simulatd data with typical model

corner	Current (relative to typical value)			
	RN at 27°C	RN at 125°C	RP at 27°C	RP at 125°C
Fast model	+18%	21%	15%	17%
Slow model	-11%	-9%	-16%	-17%
Measured data (Average)	1.6%	12%	-13%	2%

Table 5.2 Percentage variation of drain currents of measured data at 125°C as compared to values at 27°C

	RN device	RP device
Drain current variation at 125°C with respect to 27°C	-19%	-16%

5.2.3.2 Delay Chain Analysis

In Elmore's delay model, a chain of transistors are represented as an RC ladder which is arrived at by approximating nonlinear current-voltage characteristics of a transistor fairly well as a switch in series with a resistor (effective resistance is chosen to match the average amount of current delivered by the transistor). Though Elmore delay model works remarkably well for many practical applications, because it is based on linear delay model it has some limitations. The largest source of error in this model is the input slope effect. Transistor is said to be off for gate voltages less than transistor threshold voltage with transistor drawing minimum current and fully on for gate voltages equal to supply

voltage with transistor drawing maximum current. As the rise time of the input increases, active transistor is not all the way on for intermediate values of gate voltage during input transition with transistor currents lower than their maximum values thereby giving increased delays.

Since SignalStorm library characterizer generates delays in two dimensional lookup table format based on input slew rates and output loads, slew rate also has to be accounted for while analyzing data for better accuracy. This is made possible by comparing timing data at a single delay module level shown in figure 5.8 rather than by trying to derive coefficients for an equation as a function of output load and input slew using curve-fitting techniques. Thus for verifying simulation data accuracy, timing data obtained per delay module is not further decomposed into intrinsic and transition delays but compared with SignalStorm data evaluated for each delay module using delay tables generated by SignalStorm.

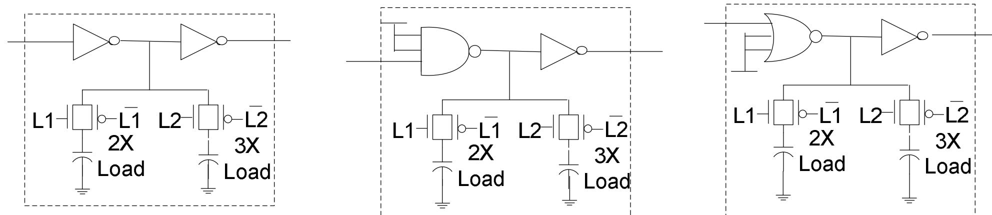


Figure 5.8 Delay modules for inverter, NAND and NOR

5.2.3.2.1 Test data

Delay measurements taken for inverter, NAND and NOR delay chains for 1X, 3X and 6X loads at 27°C and 125°C are normalized per delay module by dividing with the number of modules present in each chain and the data is plotted. Plots for fall delays (output of DUT is falling while input is rising) and rise delays (output of DUT is rising while input

is falling) are generated in separate plots. Simulation is performed for the entire test chip taking into account the extracted parasitics in Cadence Analog Environment at all process corners (fast, slow and typical) to encompass process variation range that might have occurred during test chip measurement on probe station. Obtained simulated data is plotted on the same plots as that of the measured data for easy comparison. Since the delay chains are long with the same module repeated over, it can be approximated that the input transition time for each delay module is same as the corresponding output transition time. Thus several iterations are performed in SignalStorm while generating delay tables to ensure that the input slew value that is converging with the output slew value is indexed in the generated tables. Also realistic output load values obtained during the first iteration are incorporated in the tables. The data so obtained from the generated SignalStorm tables is appended to the existing plots. Plots for inverter, NAND and NOR delay modules for both rising and falling inputs and at both 27°C and 125°C are shown below.

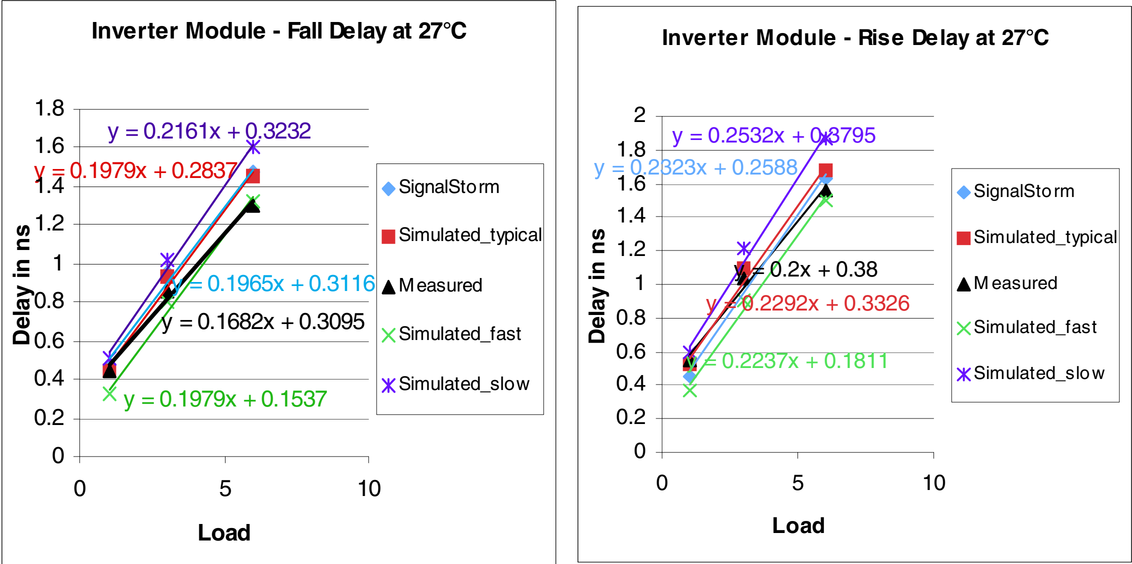


Figure 5.9 Fall and rise delay plots for inverter delay module at 27°C

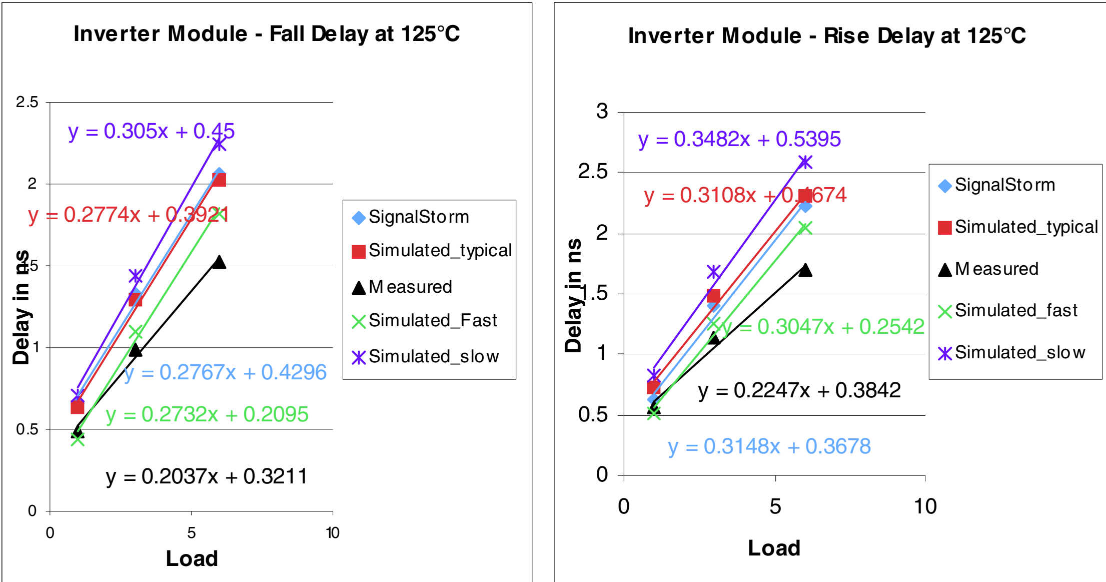


Figure 5.10 Fall and rise delay plots for inverter delay module at 125°C

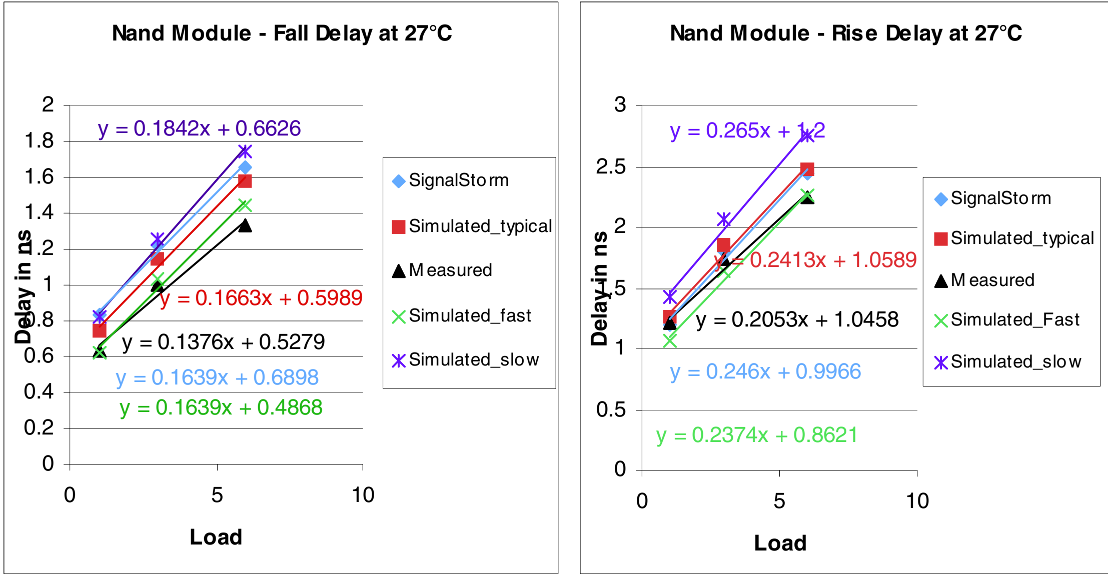


Figure 5.11 Fall and rise delay plots for NAND delay module at 27°C

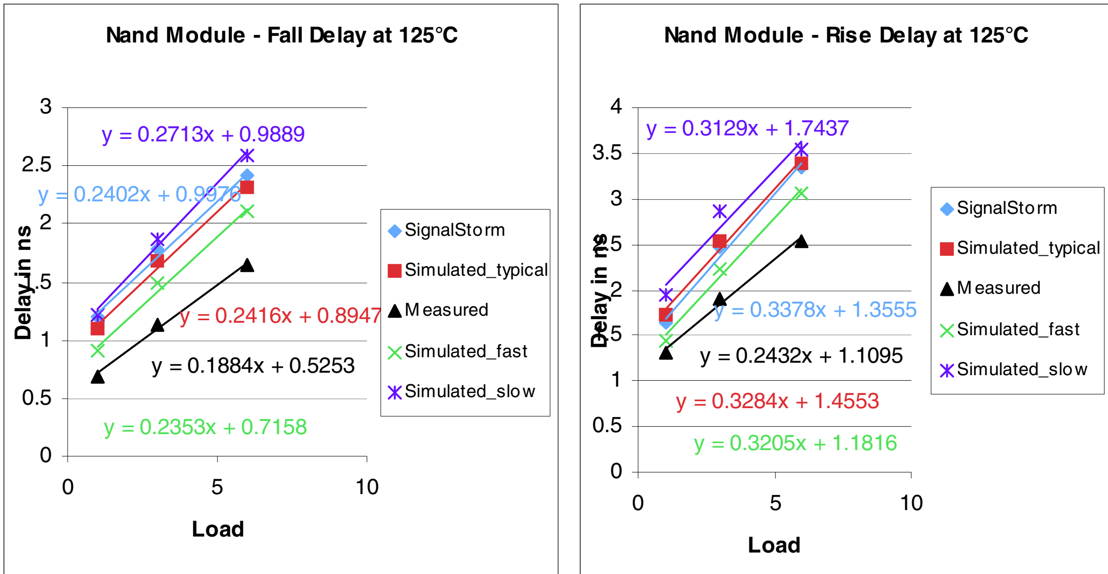


Figure 5.12 Fall and rise delay plots for NAND delay module at 125°C

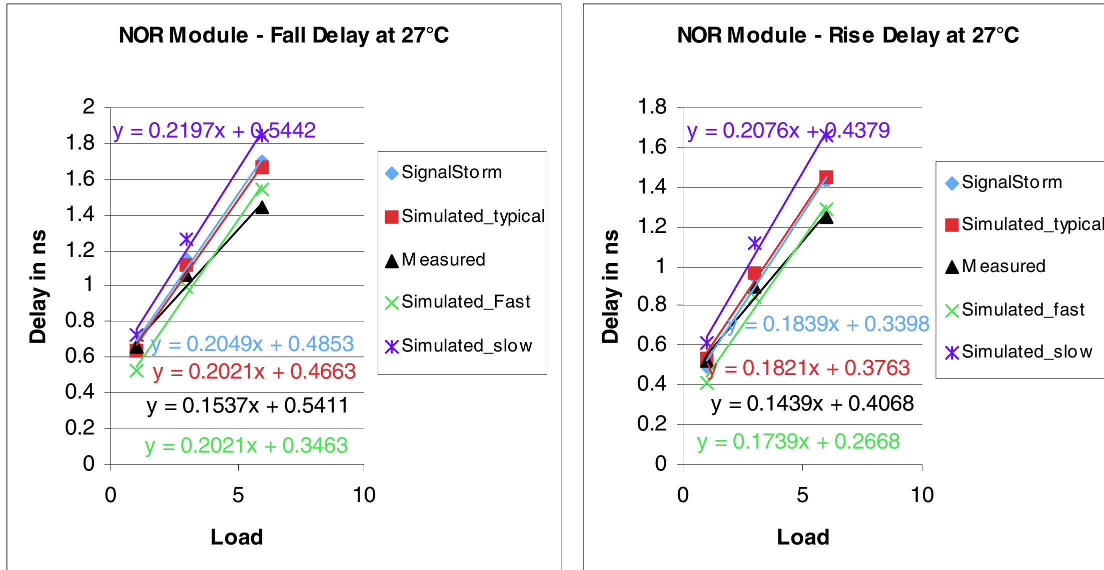


Figure 5.13 Fall and rise delay plots for NOR delay module at 27°C

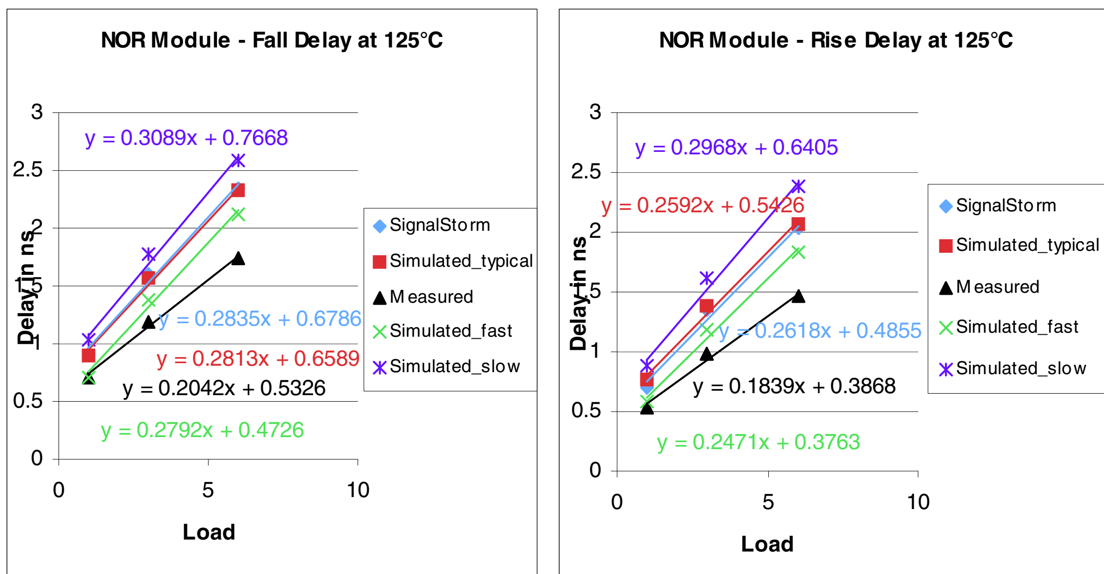


Figure 5.14 Fall and rise delay plots for NOR delay module at 125°C

5.2.3.2.2 Interpretation of results

Variation in fall delays and rise delays at 125°C as compared to room temperature at different loads is presented in the tables 5.3 and 5.4 respectively.

Table 5.3 Variation in fall delays of delay modules at 125°C with respect to 27°C

	INV module	NAND module	NOR module
1X	-8%	-9%	-7%
3X	-13%	-11%	-11%
6X	-14%	-19%	-17%

Table 5.4 Variation in rise delays of delay modules at 125°C with respect to 27°C

	INV module	NAND module	NOR module
1X	-2%	-8%	-4%
3X	-10%	-9%	-10%
6X	-9%	-12%	-15%

From table 5.2, it can be seen that variation in drain current of NMOS device at high temperature as compared to RT is -19% and for RP device, it is -16%. Fall delays in table 5.3 are varying consistently at high temperature for different loads with maximum variation of -19% for NAND gate at 6X load. Also for rise delays, variations in values are consistently increasing with loads. Below in table 5.5, variations of the delays with respect to the simulated value with typical process are shown. From the plots shown in figures 5.9, 5.11 and 5.13, it can be seen that all the measured data at room temperature falls within the skew range and is well in agreement. At high temperature devices perform faster than the simulated values. SignalStorm data and simulated data agree well in all cases confirming no errors exist in the SignalStorm characterization process.

Table 5.5 Variation in measured slopes and intercepts of cells as compared to simulation values with typical model

		Inverter		NAND		NOR	
		Slope	Intercept	Slope	Intercept	Slope	Intercept
At 27°C	fall	-15%	9%	-17%	-12%	-24%	16%
	rise	-13%	14%	-15%	-1%	-21%	8%
At 125°C	fall	-27%	-18%	-22%	-40%	-27%	-19%
	rise	-28%	-18%	-26%	-24%	-29%	-29%

5.3 Power/current characteristics

A couple of new test dies are first tested up to 3.3V of power supply for variation in leakage as well as switching currents with voltage and frequency and the variation is observed to be linear with voltage as well as with frequency. The dies are then tested up to 5V for the leakage and switching current characteristics and non-linear variation in currents is observed from 4.0V to 5.0V.

CHAPTER 6

CONCLUSION

6.1 Conclusion

A 5V digital cell library intended for ASIC design flow operable up to 125°C has been developed. The standard cell library developed consists of 25 cells that are sufficient to realize a VHDL code for ALU. The library has drive strength of 1mA for a 1X gate. High leakage currents and gate tunneling currents at high temperatures and high voltages cause circuits to malfunction. Leakage currents have been brought down to tolerable limits by increasing length of NMOS device and gate tunneling has been proven to be absent until up to 8.5V thereby demonstrating the robustness of the library designed. Library has been characterized for timing and power, and abstracted for use with place and route design flow. A hardware validation procedure has been developed as explained in chapter V and results are verified on silicon demonstrating the accuracy of the library.

6.2 Future work

The cell library can be expanded by including some more standard cells to the existing one covering wide range of digital logic that is typically part of a standard cell library and also by adding cells with the different drive strengths. Validation procedure and test chip design need to be made even more robust to overcome any drawbacks that exist in the

current one specifically to identify reasons for the faster than expected behavior of the silicon devices. Test bench for sequential logic has to be developed and hardware verification of sequential cells needs to be performed. Typically k-factors are specified in the environment description section of a typical timing library to incorporate variation in delay values with process, temperature and voltage. Simulation, synthesis and place and route tools use these k-factors to arrive at the delay values that pertain to operating conditions under consideration. Hence, k-factors for delay variations across fast, slow and typical libraries over the entire operating range of PVT can be developed instead of having multiple libraries. SignalStorm nanometer delay calculator or some other software tool can be employed for accurate interpolation of measured data during validation process.

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VITA

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Candidate for the Degree of

Master of Science

Thesis: DEVELOPMENT OF A 5V DIGITAL CELL LIBRARY FOR USE WITH THE PEREGRINE SEMICONDUCTOR SILICON-ON-SAPPHIRE (SOS) PROCESS

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Title of Study: DEVELOPMENT OF A 5V DIGITAL CELL LIBRARY FOR USE WITH THE PEREGRINE SEMICONDUCTOR SILICON-ON-SAPPHIRE (SOS) PROCESS

Pages in Study: 76 Candidate for the Degree of Master of Science

Major Field: Electrical Engineering

Scope and Method of Study:

The scope of the thesis work presented here is to develop a standard digital cell library operable at 5V of power supply and up to the temperatures of 125°C using Peregrine 0.5µm^2 3.3V CMOS process. Peregrine 0.5µm process was selected as a result of its availability via commercial foundry at moderate cost radiation and high temperature tolerant properties. Testing data was obtained showing no measurable gate tunneling at gate voltages below 8.5V and no source to drain avalanche below 5.5V ensuring safe operation below the 5V design corners of 5.5V. Device geometries are selected to meet drive current requirement of 1mA and acceptable Ion/Ioff ratios at high temperature. Layouts for cells, schematic, symbolic and abstract views were generated. Timing, power and area characterization data is realized in several formats compatible with Cadence and Synopsys synthesizer, place & route and simulation tools.

Findings and Conclusions:

A test chip for delay chains with single input and multi-input combinatorial gates were designed and fabricated as a part of the validation on silicon. Measured data at room temperature is well in agreement with SignalStorm's data. At 125°C, delay chains performed faster in silicon by up to 25% as compared with simulated data obtained using typical model. Device characteristics for rn and rp device are obtained and percentage variations in their Id-Vd characteristics with models are calculated. Variation in test data for the test chip as compared to the simulated data is observed to be consistent with the device current variation plotted across process corners. Adherence of the targeted design specifications (from simulation) with the actual measured values verifies the cell library's functionality, timing and power parameters.

ADVISER'S APPROVAL: Dr. Chris Hutchens