A 2.45GHz RF-FRONT END FOR A MICRO NEURAL INTERFACE SYSTEM

By

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A 2.45GHz RF-FRONT END FOR A MICRO NEURAL

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TABLE OF CONTENTS

Chapter Page

CHAPTER I 1
1.1 Introduction 1
1.2 Research Objective 7
1.3 Dissertation Organization 8

CHAPTER II 10
2.1 Matching Network 10
2.1.1 Shunt Matching 12
2.1.2 Series Matching 13
2.2 Literature Review of the RF –DC converter 15
2.3 RF-DC Converter 17
2.4 Working of the RF-DC converter circuit 23
2.5 Schottky diode behavior 26
2.6 Input impedance of the RF-DC converter 30

CHAPTER III 38
3.1 Miller Compensation 39
3.2 Indirect Compensation 43
3.2.1 Indirect compensation with current injected at different nodes 45
3.2.2 Indirect compensation with current injected at same node 48

CHAPTER IV 51
4.1 Introduction to sub-threshold design 51
4.2 Square law versus sub-threshold behavior 52
4.2.1 Square law behavior 52
4.2.2 Sub-threshold behavior 53
4.3 Voltage reference 58
4.3.1 DC operation 59
4.3.2 AC operation 62
4.3.3 Noise in voltage reference 64
4.4 Global bias generator 66
4.5 Linear drop out regulator 70
4.5.1 Compensation of the LDO 73
4.6 Power on reset 79
4.7 Demodulator 80

CHAPTER V 84
5.1 High temperature sub-blocks for Vee-squared controlled DC-DC converter 84
5.1.1 Reduced capacitance compared to bulk device 85

5.1.2 Latch-up prevention 86
5.1.3 Higher IONIOFF ratio 86
5.2 Fully depleted versus partially depleted device 88
5.3 Stacked transistors 90
5.4 Control loop architectures 91
5.4.1 Voltage mode Control 92
5.4.2 Current mode Control 93
5.4.3 Vee –squared control 94
5.5 Voltage Reference 97
5.6 Comparator 100
5.7 Hysteretic comparator 102
5.8 Error Amplifier 103
CHAPTER VI 107
6.1 Test procedure for pad frame-1 108
6.2 Test procedure for the pad frame-2 110
6.3 Concluding Remarks 120
6.4 Future Work 122
REFERENCES 126

LIST OF TABLES

Table Page

Table 1.1 Specification of the power harvesting front end 8
Table 2.1 Summary of antenna and rectifier impedance combinations 11
Table 2.2 Survey of RF-DC architectures 17
Table 2.3 Simulation of diode current parameters with Vin =1V, IL = 54uA 30
Table 3.1 Pole Zero locations of a two stage miller OTA 40
Table 3.2 Pole zero locations in indirect compensation scheme................................. 42
Table 3.3 Conventions and assumptions used in indirect compensation 44
Table 3.4 Pole zero locations for current injected at different nodes. 47
Table 3.5 Pole zero locations for current injected at same nodes 49
Table 4.1 Reference current generated for the various blocks in the front end 69
Table 4.2 Pass transistor parameters for minimum and maximum load currents 74
Table 4.3 Pole zero locations for the uncompensated loop of the LDO 75
Table 4.4 Performance summary of the LDO.. 78
Table 5.1 Specification of the DC-DC converter system... 92
Table 5.2 Comparison of voltage references 100
Table 6.1 Description of the pad frame -1 108
Table 6.2 Description of the pad frame- 2 111
Table 6.3 Power consumed by individual blocks 115
Table 6.4 Comparison of the power harvesting works 118
Table 6.5 Demodulator input settings 120

LIST OF FIGURES

Figure Page

Figure 1.1 Simplified model of the inductive link ... 3
Figure 1.2 Block diagram of the front end system... 8
Figure 2.1 Network representing the maximum power transfer theorem ... 10
Figure 2.2 Network representing a shunt LC match ... 12
Figure 2.3 Network representing a series LC match... 13
Figure 2.4 Illustration of Q boost in series match... 14
Figure 2.5 Block diagram of the power harvesting front end ... 17
Figure 2.6 (a) Plot of ID vs. Vin and (b) f_T vs. Vin for N Schottky diode ... 20
Figure 2.7 (a) Plot of ID vs. Vin and (b) f_T vs. Vin for MOS diode ... 21
Figure 2.8 Current through the switch ... 21
Figure 2.9 Schematic of the one stage RF-DC converter and its waveform [28] ... 23
Figure 2.10 Waveform at the output of the rectifier with diode drop and R_L... 25
Figure 2.11 Layout of a N type Schottky diode... 27
Figure 2.12 Band diagram of the metal and semiconductor [31] ... 27
Figure 2.13 Waveforms of the current through the schottky diode ... 31
Figure 2.14 Input impedance transformation of a RF-DC network [23] ... 32
Figure 2.15 Plot of DC voltage vs. load current ... 36
Figure 3.1 Small signal model of a generic two stage miller OTA[33, 34]... 39
Figure 3.2 Bode plot of a miller compensated OTA... 40
Figure 3.3 Feeding back a current using a common gate device [33] ... 42
Figure 3.4 Bode plot of the indirect compensated OTA ... 43
Figure 3.5 Four possible structures for indirect compensation. ... 44
Figure 3.6 Small signal model of OTA with current injection at different nodes ... 46
Figure 3.7 Small signal model of OTA with current injection at same node ... 48
Figure 4.1 Schematic of the voltage reference... 58
Figure 4.2 Monte-Carlo distribution of V_{REF} = 400mV at 27°C ... 62
Figure 4.3 Monte-Carlo distribution of V_{REF} from 25°C to 125°C... 62
Figure 4.4 Plot of voltage reference loop gain and phase versus frequency... 64
Figure 4.5 Noise plot at the output of the reference node voltage... 66
Figure 4.6 Global bias generator for the signal conditioning blocks... 67
Figure 4.7 Distribution of $V_{ds} – V_{dsat}$ for the reference current leg at 27°C ... 69
Figure 4.8 Distribution of $V_{ds} – V_{dsat}$ for the reference current leg at 125°C ... 69
Figure 4.9 Schematic of the linear drop out regulator ... 70

Figure 4.10 Block level diagram of loop gain of the LDO 73
Figure 4.11 Movement of poles under light load to full load condition 75
Figure 4.12 Loop gain and phase plots for minimum and full load conditions 76
Figure 4.13 Load regulation of the LDO for a step change in input voltage 77
Figure 4.14 Load regulation of the LDO for a step change in load current 78
Figure 4.15 Settling time of the LDO from no load to full load 78
Figure 4.16 Schematic of the power on reset circuit 79
Figure 4.17 Simulation and power on reset circuit 80
Figure 4.18 Schematic of the demodulator 80
Figure 4.19 Output waveform of the demodulator 82
Figure 5.1 Cross section of a NMOS device in Bulk versus SOI [52] 85
Figure 5.2 Cross section of (a) Bulk device and (b) SOI device 86
Figure 5.3 Cross section of (a) partially depleted and (b) fully depleted device[53] 88
Figure 5.4 Equivalent schematic of the floating body transistor 89
Figure 5.5 ID vs. VDS of a NMOS device showing the kink effect [51] 90
Figure 5.6 Schematic of the stacked transistor 90
Figure 5.7 Schematic of the voltage mode control of the buck converter[50] 92
Figure 5.8 Schematic of the current mode control [50] 93
Figure 5.9 Schematic of the vee-squared control loop [50] 94
Figure 5.10 Schematic of the cascaded pair of error amplifier and comparator [50] 95
Figure 5.11 Equivalent circuit of the switch and LC filter in the on state [50] 96
Figure 5.12 Bode plot of the loop response of the vee-squared controller 96
Figure 5.13 I-V plot of the SN resistor 97
Figure 5.14 I-V plot of the PP resistor. 98
Figure 5.15 ID-VD plot for the NG diode in the peregrine process 98
Figure 5.16 (a) schematic (b) layout and (c) measured results of voltage reference 99
Figure 5.17 (a) Schematic of the comparator (b) layout of the comparator 100
Figure 5.18 (a), (b) and (c) Measured results of the comparator 102
Figure 5.19 Block diagram of the hysteretic comparator 103
Figure 5.20 Hysteresis plot versus temperature 103
Figure 5.21 Schematic of the error amplifier 104
Figure 5.22 Layout of the error amplifier in the VREF pad frame 105
Figure 5.23 Measured parameters of the error amplifier 105
Figure 6.1 Chip micrograph of the Padframe-1 108
Figure 6.2 Unregulated voltage versus load current at constant input power 109
Figure 6.3 Unregulated voltage versus input power at constant load current 110
Figure 6.4 Chip micrograph of the Padframe-2 111
Figure 6.5 Reference voltage versus input power 112
Figure 6.6 Regulated voltage versus input power 113
Figure 6.7 Regulated voltage of LD0-1 versus V_{DD} 114
Figure 6.8 Regulated voltage of LD0-2 versus V_{DD} 115
Figure 6.9 Double side band AM wave 119
Figure 6.10 Demodulator outputs 120
Figure 6.11 Schematic of the limiter 124

LIST OF SYMBOLS AND ABREVIATIONS

Chapter I

BMI	Brain machine interface
VLSI	Very large scale integration systems
SOC	System on chip
RF	Radio frequency
DC	Direct current
R_P	Resistance of the primary winding
C_P	Capacitance of the primary winding
L_P	Inductance of the primary winding
I_P	Current in the primary winding
R_S	Resistance of the secondary winding
C_S	Capacitance of the secondary winding
L_S	Inductance of the secondary winding
I_S	Current in the secondary winding
M	Mutual inductance between the primary and secondary
K	Coupling coefficient
ω_o	Resonant frequency of the primary and secondary
V_{in}	Input voltage of the primary
V_{out}	Output voltage at the secondary
Q_P	Quality factor of the primary coil
Q_S	Quality factor of the secondary coil
Δf	Bandwidth of the system
η	Efficiency of the inductive model
RFID	Radio frequency identification
TDMA	Time division multiple access
CDMA	Code division multiple access
MNI	Micro neural interface
MNS	Micro neural stimulator
P_r	Power density at the receive antenna
P_t	Power density at the transmit antenna
G_t	Gain at the transmit end of the antenna
G_r	Gain at the receive end of the antenna
λ	Wavelength of the medium
r	Transmission distance
FDTD	finite-difference time-domain
SAR	specific absorption rate

ADC	Analog to digital converter
PLL	Phase lock loop
FIFO	First in First out
LDO	Low drop out regulator
POR	Power on reset

Chapter II

RF-DC	Radio frequency to Direct current
MOS	Metal oxide semiconductor
V_S	Voltage source
Z_S	Impedance of the source
R_S	Real part of the resistance of the antenna
X_S	Imaginary part of the resistance of the antenna
Z_{in}	Impedance of the RF-DC converter
R_{in}	Real part of the resistance of the RF-DC converter
X_{in}	Imaginary part of the RF-DC converter
L_{match}	Matching network inductance
C_{match}	Capacitance of the matching network
P_{in}	Input power
V_S	Peak voltage at the input of the antenna
PMOS	P- type metal oxide semiconductor
V_o	Output voltage of the RF-DC converter
N	Number of stages
V_P	Peak voltage at the input of the RF-DC converter
V_D	Voltage drop across the switch
C_{in}	Input capacitance of the RF-DC converter
J_{DIODE}	Current density of a schottky diode
J_{NMOS}	Current density of a NMOS transistor
I_S	Saturation current of Schottky diode
V_T	Thermal voltage
n	Ideality factor of a diode
μ_n	Mobility of a NMOS transistor
V_G	Gate voltage of the NMOS transistor
V_{TN}	Threshold voltage of the NMOS transistor
f_{TDIODE}	Unity current gain of the schottky diode
I_D	Diode current
U_T	Thermal voltage
CJ	Junction capacitance of the Schotty diode
A	Cross section area of the schottky diode
I_{SO}	Saturation current density
C_{JO}	Junction capacitance per unit area
f_{TNMOS}	Unity current gain of the MOS transistor diode
C_{GG}	Equivalent gate capacitance of the MOS transistor
L	Length of the MOS transistor
Cox	Oxide capacitance of the MOS transistor
A	Amplitude of the current pulse
b_n	Fourier coefficient
D_1, D_2	Schottky diodes in the RF-DC converter
C_S	Series capacitor in the RF-DC converter

C_L	Load capacitor in the RF-DC converter
MIM	Metal-insulator-metal capacitor
V_R	Magnitude of the ripple voltage
$\emptyset_m$	Work function of the metal
$\emptyset_s$	Work function of the doped semiconductor
X	Electron affinity
E_F	Fermi energy level
E_C	Energy level of the conduction band
E_V	Energy level of the valence band
□B_n	Potential barrier from metal to semiconductor
V_{bi}	Built in potential of the Schottky diode
J	Forward bias current density of the Schottky diode
Va	Applied forward bias
C	Capacitance per unity area of an ideal p-n junction diode
e	charge of the electron
ε_S	Permittivity of free space
N_d	concentration of the donor atoms
V_R	Reverse bias voltage
J_{ST}	reverse saturation current density
K	Boltzmann's constant
T	Temperature in Kelvin
A	Richardson constant
I_{DF}	Fundamental component of diode current
I_{inF}	Fundamental component of input current
I_{Dmin}	Minimum value of the diode current
I_{Dmax}	Maximum value of the diode current
Q_{NW}	Quality factor of the matching network
C_{D1} ,C_{D2}	Junction capacitance of the schottky diode
R_{FD}	Fundamental resistance of the schottky diode

Chapter III

OTA	Operational trans conductance amplifier
MDAC	Multiplying digital to analog converter
ADC	Analog to digital converter
g_m	Trans conductance of a MOS device
R	Small signal resistance of the MOS device
C_C	Compensation capacitance
C	Capacitance
GBP	Gain bandwidth product
g	Output conductance of the MOS transistor
K_r	Ratio of the mobility of the NMOS to PMOS device
LHP	Left half complex plane
RHP	Right half complex plane

Chapter IV

P	Power
C	Total gate capacitance
V	Supply voltage
f	Operating frequency

I	Total current consumed
SNR	Signal to noise ratio
V_{DD}	Supply voltage
KP	Trans conductance parameter
ΔV	Over drive voltage of the MOS device
V_{THN}	Threshold voltage
BJT	Bipolar junction transistor
V_G	Gate voltage of a transistor
V_D	Drain voltage of a transistor
V_S	Source voltage of a transistor
I_F	Forward current
I_R	Reverse current
V_P	Pinch off voltage
V_{TO}	Zero bias threshold voltage
B	MOS transistor gain factor
Ψ	Surface potential of the MOS transistor
IC	Inversion coefficient
I_D	Drain current of the MOSFET
A_{VTH}	Pelgrom coefficient
V_{GS}	Gate to source voltage of a MOS transistor
R_{ds}	Small signal output resistance of a MOS device
PTAT	Proportional to absolute temperature
CTAT	Complementary to absolute temperature
V_{REF}	Voltage reference
T_{LG}	Loop gain
V_B	Bias voltage

Chapter V

SOS	Silicon on sapphire
I_{ON}	On current of the transistor
I_{OFF}	Off current of the transistor
SOI	Silicon on insulator
SiO2	Silicon di oxide
C_{BOX}	Oxide capacitance
DIBL	Drain induced barrier lowering
RN	Regular VT device
NL	Low VT device
TF	Transfer function of the loop gain

Chapter VI

m	Modulation index
η	Efficiency
AM	Amplitude modulation
DSB-AM	Double side band amplitude modulation

CHAPTER I

This chapter consists of three main sections: introduction, research objective and dissertation organization. Section 1.1 provides an introduction to implantable medical electronics and the various options that exist to power active medical implants. Section 1.2 states the objective of the research and section 1.3 discusses the dissertation organization.

1.1 Introduction

Implantable medical devices over the past six decades have evolved in solving a host of medical issues e.g. pacemakers and internal cardiac defibrillators in regulating heartbeat, cochlear implants in aiding hearing among the severely deaf patients, subcutaneous drug delivery etc. Medical implants can be classified into two main categories: a) Passive implants and b) Active implants. Passive implants are devices that do not require electric power to perform their function. Some common examples of passive implants include structures liked rods , screws etc. made out of bio compatible material like titanium , silicone that are used to support a damaged bone/tissue. Active implants on the other hand require electric power to be operational. One of the promising areas of research using the active implants is the brain machine interface system. By monitoring the raw neurological signals and post processing it in the electronics domain a host of motor

commands of the human body like arm reaching , grasping and mobility can be reproduced [1]. This electric power required for the implants can be delivered using batteries, transcutaneous energy transmission and energy harvesting from the environment. While traditionally batteries have been used to power these implants, they have the disadvantage of having to be replaced frequently. This poses a risk of frequent surgery for the patient user. In addition, wires are currently being used for communication between the BMI and the host system. These wires provide a tethering force to the neural interface and can cause tissue damage, restrict movement and in general limit results. A more attractive solution for medical implants is the use of wireless power and communication. Recent advances in wafer packaging technologies and advanced VLSI processes together offer the possibility of a system on chip (SOC) solution for active implants using energy harvesting. Active implants powered using wireless power are able to last for decades without replacement and also minimize tissue heating.

The three main approaches for wireless power implementation are: 1) electrostatic coupling, 2) inductive coupling, 3) RF or electromagnetic waves [2, 3]. In an inductively coupled system, a power amplifier coupled to an external controller drives the primary coil in the RF transmitter. An implanted coil on the secondary side receives this power and rectifies it to supply adequate DC voltage to the implant. Power transfer in an inductive link depends on the following [4]:

1. Ratio of secondary to primary voltage
2. Power efficiency
3. Bandwidth

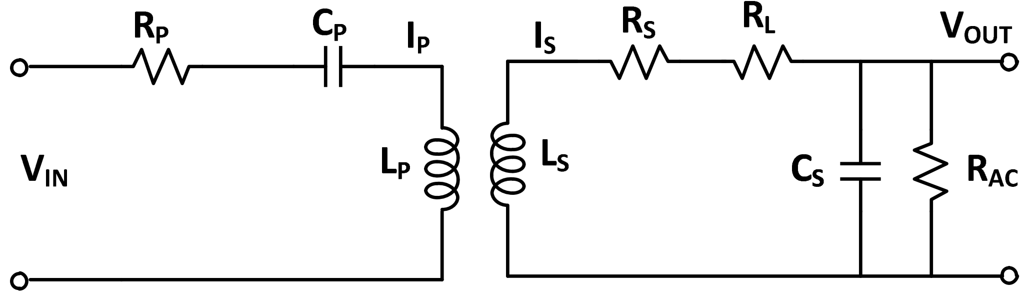


Figure 1.1 Simplified model of the inductive link

Figure 1.1 shows the simplified two port schematic of the inductive link model. R_P, C_P and L_P represent the resistance, capacitance and inductance of the primary and R_S, C_S and L_S represent the resistance, capacitance and inductance of the secondary side. The mutual inductance between the primary and the secondary can be expressed as $M=K\sqrt{L_P L_S}$, where K is defined as the coupling coefficient. Both the primary and secondary are tuned at the same resonant frequency which can be expressed as:

$$\omega_o=\frac{1}{\sqrt{L_P C_P}}=\frac{1}{\sqrt{L_S C_S}} \tag{1.1}$$

The transfer function from V_{in} to V_{out} can be expressed as [4]:

$$\left(\frac{V_{out}}{V_{in}}\right)=-\frac{\omega^2}{\omega_0^2}\frac{k\sqrt{\frac{L_s}{L_P}}}{\left[k^2+\frac{1}{Q_P Q_S}-\left(1-\frac{\omega^2}{\omega_0^2}\right)+j\left(1-\frac{\omega^2}{\omega_0^2}\right)\left(\frac{1}{Q_P}+\frac{1}{Q_S}\right)\right]} \tag{1.2}$$

Where $Q_P=\frac{\omega L_P}{R_P}$ and $Q_S=\frac{\omega L_S}{R_S+R_L}$. Taking a derivative of equation (1.2) , we find that the maxim value of $\left(\frac{V_{out}}{V_{in}}\right)$ occurs when $k=\frac{1}{\sqrt{Q_P Q_S}}$ and is given as:

$$\left(\frac{V_{out}}{V_{in}}\right)_{max}=\frac{1}{2K_C}\sqrt{\frac{L_s}{L_P}}=\frac{1}{2}\sqrt{Q_P Q_S}\sqrt{\frac{L_s}{L_P}} \tag{1.3}$$

Equation (1.2) reveals that the response of the inductive link is analogous to a narrow band pass filter. The bandwidth of this transfer function at critical coupling frequencies can be expressed as [4]:

$$\Delta f = \frac{\omega_0}{2\pi Q}\sqrt{2} \tag{1.4}$$

The coupling coefficient 'K' depends on the mutual inductance 'M' and the Q's of the components used in the coil. The coils used in the inductive links are often implemented as off chip components which give them a very high Q and because they are separated by a layer of skin which is a few centimeters thick , the value of the overall coupling coefficient is small. Since coupling depends on proper coil orientation, precise placement of these structures within the human body will be difficult. Also the high Q value results in a low bandwidth for communication purposes. One may think of increasing the value of L_S and L_P to raise the value of M. This can be achieved by using a multi turn coil and maintaining the number of turns in the secondary higher than the primary to get a high V_{out}. Multiple turn external coils could be a possibility were it not for coupling inefficiency due to the large ratio between the area of the external primary coil (10's of cm^2) and the sensor coil (100's of μm^2). Increasing the number of turns causes the series resistance of both the primary and secondary windings to go up and these results in poor efficiency. Efficiency of the above two port model can be expressed as:

$$\eta = \frac{(\omega M)^2/(R_S+R_L)}{R_P+(\omega M)^2/(R_S+R_L)}\frac{R_L}{R_S+R_L} \tag{1.5}$$

The communication data rate in inductive coupling is decided by the choice of the carrier frequency. A lower carrier frequency results in reduced power loss but the size of the

antenna and the passive LC components required to implement increases dramatically. Even for the highest frequency of commercial mutual inductance systems (13.56 MHz for those with RFID passive tags), 5 MHz bandwidth represents a system bandwidth requirement of 37%.This is simply too wide for a neural interface design and one might consider TDMA or CDMA for such high bandwidth at the expense of on chip processing cost in both area and power [5, 6]. Moving to a higher carrier frequency results in an opportunity for a higher data rate for communication together with the benefit of smaller sized passives, but comes at a cost of increased transmission power loss in the tissue. These losses may result in unsafe heating of the tissue. Nevertheless inductive coupling has been applied for medical application such as retinal prostheses, muscular stimulation and cochlear implants [7, 8]. Detailed studies using this approach indicate that the antenna coils are several centimeters in dimension [9, 10]. Successful results in power and data transmission have also been obtained by using a much smaller dimension [11, 12]. From the discussion and studies mentioned above we can conclude that inductive links are suitable for short range communication from one or few devices. The restricted volume, communication bandwidth, and depth of implant for the micro neural interface sensor (MNI) and micro neural interface stimulator (MNS) pair, render mutual coupling impractical.

Electromagnetic waves at RF frequency offers the opportunity to power and communicate with large number of implanted devices providing a number of control signals in a highly robust and stable interface. Electromagnetic radiation from the antenna can be classified based on their intensity into two main categories [13]: a) Near field and b) far field. The term near field usually refers to distances within one wavelength from

the antenna. Electromagnetic waves from the antenna consist of time varying ‘E’ and ‘H’ fields that propagate in free space or the medium exposed. In the near field region these waves act as field lines (inductive and capacitive) that begin and terminate on the antenna. The far field region is usually referred to regions of two wavelengths and above from then antenna to infinity. In tissue at 1 to 2.5 GHz these one wavelength translate to 8.5 to 3.5 cm in tissue. Beyond this region, the amount of reactive power is less and the only available power is the RF, normal perpendicular to the direction of propagation. The power density of the RF power in this region is inversely proportional to the square of the distance $\frac{1}{r^2}$ from propagation and can be expressed as [13]:

$$P_r = P_t G_t G_r \left(\frac{\lambda}{4\pi r}\right)^2 \quad (1.6)$$

Where P_r , P_t are the power densities at the transmit and receive end of the antennas with gains G_t and G_r. The distance r must be greater than the wavelength λ of the medium. Thus the far field RF radiation offers an opportunity to supply energy to a load at distances greater than the wavelength of the source.

Authors Sun Mingui et al. in [14], Ibrahim et al. in [15] and Kennedy in [16] have carried out 2D and 3D simulations on the brain machine interface system to report the power absorption and temperature changes of the brain tissue. The authors report an average value of the safe limit of incident power to be 3mW before a rise of 1ºC in tissue temperature. The 3D simulations were made using finite-difference time-domain (FDTD) method [17], a full-wave electromagnetic simulation technique. A preliminary simulation was done by Dr.Ibrahim’s group using a half-wavelength (6.2 cm at 2.45 GHz) monopole

antenna mounted approximately 7 mm above the head to excite the BMI chip(s). Based on these simulation results and the results reported in [15] , maximum power levels of up to 3mW for a single chip and 1.25mW for a eight chip configuration can be tolerated before a 1ºC increase in tissue temperature. The maximum average specific absorption rate (SAR) allowed by the FCC commissions is 1.6 W/kg in 1 gram of tissue [18, 19]. Authors Xu and Meng have reported a detailed study on the effects of specific absorption rate(SAR) of an ingestible wireless device taking into account the variations of conductivity and permittivity of the human body tissue[20]. The authors have reported acceptable SAR levels of 0.89W/Kg for an input power level of 25mW at 430MHz. Xu and Meng results demonstrate that the deeper an implantable device is inserted into the human head and as distances between transmit and receive antennas grow; less signal is received by the implant. Furthermore, the SAR distributions illustrate greatest electromagnetic power absorption in close proximity to the transmit antenna. The 3D FDTD studies demonstrate that RF power and VLSI technology together give us the opportunity to develop circuitry that can harvest useful power from a far field source and be operational to perform a variety of functions for the brain machine interface.

1.2 Research Objective

Figure 1.2 shows the block diagram of the entire RFID sensor system. The entire system is capable of harvesting power, amplifying, and recording, digitizing and transmitting data in real time. The RFID system consists of band pass amplifier, 8 bit ADC, reference chains, PLL, FIFO memory, controller and the power harvesting front end. The entire system is designed to dissipate less than 100µW of power with the electronics consuming less than 40µW. The objective of this research work is to demonstrate a working solution

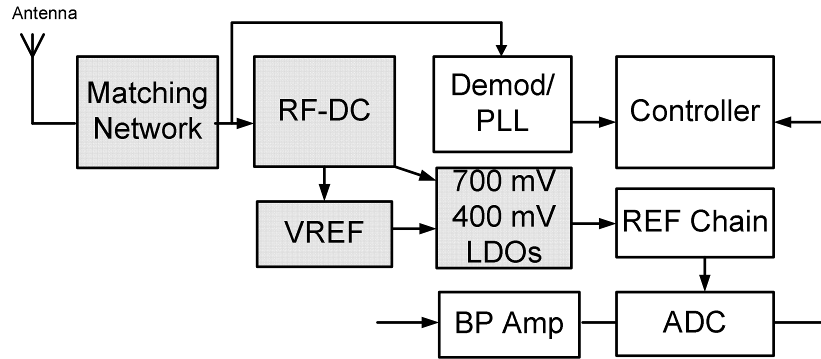


Figure 1.2 Block diagram of the front end system

in silicon for a power harvesting front end comprising the antenna matching network, RF-DC converter, voltage reference, linear drop out regulator and the demodulator. The power harvesting front end blocks are shown in grey color in Figure 1.2. The design of the antenna is beyond the scope of this work and will not be discussed. The impedance of the antenna was assumed to be 50 ohms with the expected variation to be in the range of 40-74 ohms.

The system design parameters and the expected output characteristics of the front end are shown in Table 1.1.

Table 1.1 Specification of the power harvesting front end

Specification	Value
Input power	Min: -3dBm Max : 0 dBm
Output voltage	Min: 680mV Max: 720mV
Output power	50 µW
Efficiency	10 – 15 %

1.3 Dissertation Organization

The dissertation has 6 chapters including the present chapter. Chapter II discusses the matching network together with the RF-DC converter. The properties of the schottky

diode based rectifier and the analysis of the input impedance of the RF-DC converter is also presented.

Chapter III discusses the OTA as a key block in the front end. Various ways of compensating the op-amp and their analyses shall be discussed. Emphasis is laid on the indirect compensation method.

Chapter IV discusses the Voltage reference, LDO, global bias generator and the demodulator as the blocks comprising the RF- Front end system.

Chapter V introduces the VEE squared control DC- DC converter and the various high temperature blocks in building the DC-DC controller system.(This work is not a part of the micro-neural interface system described in chapters I-IV).

Chapter VI provides the measurement and test results for the RF-Front end along with concluding remarks and future work.

CHAPTER II

This chapter is divided into six sub-sections. Section 2.1 describes the need for a matching network and the different matching network options available. Section 2.2 provides a survey of the various architectures found in literature for implementing the RF-DC converter followed by section 2.3, which describes the choices available for implementing the switch in the RF-DC converter. A comparison between the schottky diode and MOS diode is provided. Section 2.4 describes the procedure to develop an expression for DC voltage at the output of the RF-DC converter. The behavior of the schottky diode under forward and reverse bias and the difference between the schottky diode and a regular p-n junction diode is explained in section 2.5. Section 2.6 details the procedure to calculate the real and imaginary parts of the input impedance of the RF-DC converter along with the matching network and preliminary simulations.

2.1 Matching Network

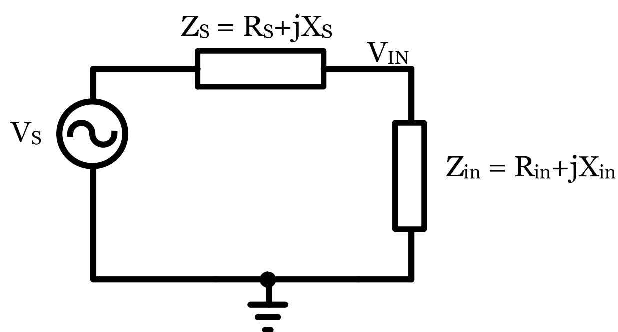


Figure 2.1 Network representing the maximum power transfer theorem

A matching network is designed to maximize the power transfer between the antenna and the RF-DC converter. Figure 2.1 represents a two port network that illustrates the maximum power transfer theorem [21]. V_S represents the peak value of the signal amplitude at the antenna, Z_S is the antenna impedance with R_S, X_S being the real and imaginary parts respectively and Z_{in} represents the input impedance of the rectifier, with R_{in}, X_{in} being the real and imaginary parts of the input impedance. The available DC power at the input of the rectifier based on Figure 2.1 can be expressed as follows[21]:

$$\frac{|V_{in}|^2}{R_{in}} = \frac{R_{in}|V_S|^2}{(R_{in}+R_S)^2+(X_{in}+X_S)^2} \tag{2.1}$$

By differentiating equation (2.1) and equating it to zero, the conditions for maximum power transfer between the antenna and the rectifier can be summarized as follows:

1. R_{in} should be equal to R_s.

2. X_{in} and X_s should cancel each other at the desired operating frequency ω_0.

Based on the above criteria, the maximum obtained voltage amplitude at the input of the rectifier is equal to $V_{in}/2$ and the maximum efficiency obtained is 50%. Table 2.1 summarizes the voltage levels at the input of the rectifier for different values of the real part of the input impedance.

Table 2.1 Summary of antenna and rectifier impedance combinations

Case (i)	$R_{in} \ll R_S$	$V_{in} \ll \frac{V_S}{2}$
Case(ii)	$R_{in}=R_S$	$V_{in}=\frac{V_S}{2}$
Case (iii)	$R_{in} \gg R_S$	$V_{in}=V_S$

The input impedance of the RF-DC converter (including both real and imaginary parts) is usually higher than the antenna impedance by a factor of five [22, 23]. If the RF-DC converter is connected directly to the antenna, this would result in a higher voltage at the input of the rectifier as highlighted by case (iii), but the power transfer efficiency will be quite low. In order to achieve both a high voltage and maximum power transfer, a matching network that transforms the low value of the antenna impedance to a higher value is required. The three methods to implement the matching networks are [22] :

1. Transformer matching

2. Series LC matching

3. Shunt LC matching

Transformer based matching network can be used when the antenna is differential in nature (e.g. like a quarter wave dipole) and the rectifier architecture is full wave producing both positive and negative rectified voltages. In order to get a high voltage at the input of the rectifier, the ratio between the primary and secondary needs to be high. This requirement translates into the inductor sizes being too large for on chip operation and hence makes this choice infeasible.

2.1.1 Shunt Matching

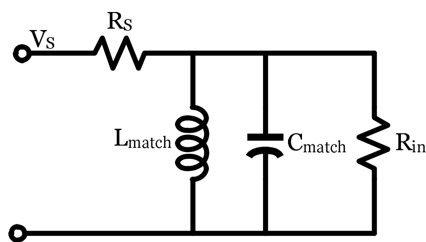


Figure 2.2 Network representing a shunt LC match

Figure 2.2 represents a two-port network with shunt LC matching network. The shunt inductor tunes the equivalent shunt capacitance including the parasitics at the desired operating frequency as per the equation (2.2)

$$\omega_0 = \frac{1}{\sqrt{L_{match} C_{match}}} \tag{2.2}$$

Since no series element is present, a boost in voltage and impedance transformation does not occur [23]. The antenna and the rectifier have to be designed in concert to match the real parts of the impedance .The maximum available or peak voltage at the input of the rectifier is $V_S/2$ for any given input power. The peak voltage at the input of the antenna for a power level P_{in} and antenna impedance R_S is given as [23]:

$$V_S = \sqrt{2 P_{in} R_S} \tag{2.3}$$

From equation (2.3), V_S is directly proportional to P_{in} and R_S. Shunt matching is good candidate when the combination of available input power and antenna impedance translates to a voltage large enough to turn on the rectifying devices in the RF-DC converter. This however is not the case for an implantable device in the human body, where the incident power levels may be lower than -3dBm. A series matching network solves this problem by providing a boost in voltage at the input of the rectifier.

2.1.2 Series Matching

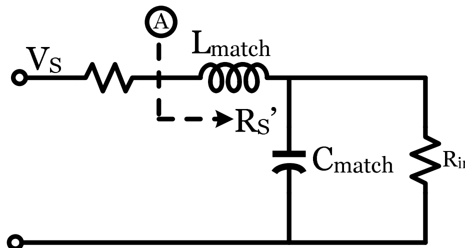


Figure 2.3 Network representing a series LC match

Figure 2.3 represents a network with series LC match. The real part of the rectifier impedance R_{in} is assumed to be greater than the antenna impedance R_S. The LC network converts R_{in} to a much lower resistance R_S' at node A. From the view point of the source V_S, a higher current flows into node A and this is impressed on R_{in} to get a voltage boost of Q. Figure 2.4 illustrates this phenomenon.

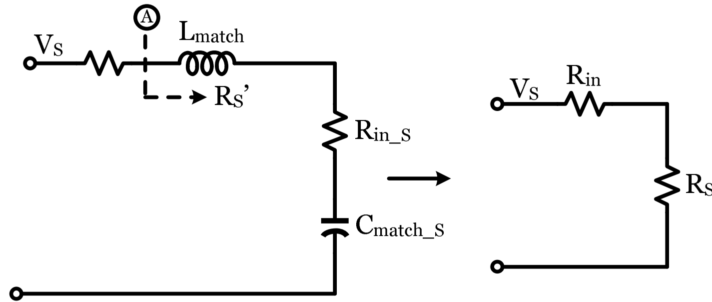


Figure 2.4 Illustration of Q boost in series match

The parallel combination of R_{in} and C_{match} can be transformed into a series equivalent circuit as follows [21]:

$$R_{in_S}=\frac{R_{in}}{1+Q^2}$$
$$C_{match_S}=C_{match}\left(\frac{1+Q^2}{Q^2}\right) \tag{2.4}$$

This newly formed RC network is now in series with L_{match} and the total impedance looking at node A can be expressed as:

$$R_S^{'}=R_{in_S}+j\left(\omega_0 L_{match}-\frac{1}{\omega_0 C_{match_S}}\right) \tag{2.5}$$

R_S' is purely real when $\omega_0 L_{match} = \frac{1}{\omega_0 C_{match_S}}$ and is equal to R_{in_S}. Substituting this condition in equation (2.4) for maximum power transfer, R_S' should be equal to R_{in_S}, or in other words

$$Q = \sqrt{\frac{R_{in}}{R_S} - 1} \tag{2.6}$$

Equation (2.6) suggests that once the antenna resistance and the input resistance of the RF-DC converter are determined, the network transformation ratio is automatically fixed. Using the definition of Q, the expressions for L_{match} and C_{match} are given as:

$$L_{match} = \frac{QR_S}{\omega_o} \tag{2.7}$$

$$C_{match} = \frac{Q}{\omega_o R_{in}} \tag{2.8}$$

2.2 Literature Review of the RF –DC converter

The RF-DC converter is the critical circuit in the power harvesting front end that produces the rectified DC voltage. A literature review of the existing RF-DC architectures for implementing this circuit block reveals that the behavior of the RF-DC converter is similar to the behavior of the charge pump and/or the voltage multiplier circuits. One of the very famous and widely used architectures for the voltage multiplier circuits is the Dickson charge pump [24]. The Dickson architecture uses a signal from a low impedance source and two out of phase non-overlapping clocks to generate an output voltage that is a multiple of the input voltage. This architecture is infeasible in the RFIDS (RFID sensor system) because of the absence of a readily available clocking signal and

power supply. Nevertheless, the results provided by the Dickson charge pump prove useful in the study of the RF-DC converter. The RF-DC architectures found in literature can be broadly classified as:

1. Full wave rectifiers
2. Half wave rectifiers

In the half wave rectifier architecture, the switch does not conduct during the negative half cycle allowing the load to be discharged over one entire period. The full wave rectifier architecture conducts during both the positive and negative cycles of the input and hence the magnitude of the ripple is lower for the same value of the load capacitor as compared to the half wave architecture. Authors Curty et al. have used the full wave architecture to implement the RF-DC converter in [25]. The switch was implemented as a diode connected MOS device in a 0.5µm peregrine SOI process. Authors Mandal and Sarpeshkar have used the full waver rectifier design by using self-driven MOS transistors as switches to implement the RF-DC converter [26]. Three stages were cascaded to obtain the required DC voltage. The work done by authors Shameli et al. in [27] and Barnett et al. in [23] use the half wave rectifier design with MOS diode and series matching , Schottky diode and shunt matching respectively. Though the full wave architecture offers the advantage of lower ripple and the feasibility to generate bipolar rectified supplies, it increases the amount of losses per stage and the required area for implementation. The desired ripple ratio can be met by using a capacitor of moderate size and post regulation of the raw developed voltage. In this work, we choose to implement the RF-DC converter as a half wave rectifier. Table 2.2 provides a summary of the various architectures surveyed for implementing the RF-DC converter.

Table 2.2 Survey of RF-DC architectures

Author	Frequency (MHz)	Process	Matching type	Switch type	No. of stages	Output voltage(V)	Load current range(μA)	Efficiency (%)
Curty[25]	915	0.5μm SOI	Series	MOS diode	3	0-5	1	0-10
Sarpeshkar[26]	950	0.18μm Bulk	Shunt	MOS	2	0-5	4	16-23
Barnett[23]	900	0.18μm Bulk	Shunt	Schottky diode	16	0-3	1-8	4-8
Shameli[27]	920	0.18μm Bulk	Series	MOS diode	4	0-1	2	5-10

2.3 RF-DC Converter

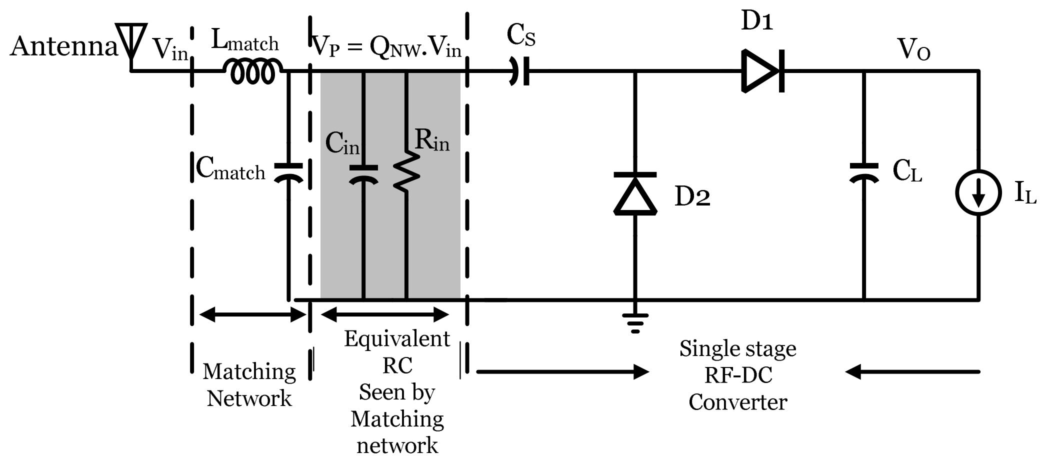


Figure 2.5 Block diagram of the power harvesting front end

Figure 2.5 shows the schematic of the RF-DC converter with the LC matching network and the equivalent circuit seen by the matching network. For proper RFIDS operation, the RF-DC converter needs to generate 30 to 40uW of power at DC voltages of 650 to 700mV for the analog section, 370 to 400mV for the digital circuits to power the signal conditioning and logic circuitry, and 900mV to power the voltage reference. The RF to DC circuit topology is primarily dictated by three factors: 1) power requirements, 2) available power and 3) rectifying switch types, i.e. Schottky diode or CMOS switch. Voltage levels must be sufficient to turn on the rectifying switch. The Q of the matching network and the minimum value of the unregulated voltage required to power up the

circuits are governed by circuit architecture, topology and the choice of VLSI process. For this work we chose the IBM 180nm RF CMOS process. The choice of a minimum of 0.9V for the voltage reference architecture arises because of the parasitic bipolar transistor and two PMOS transistors in series, forming the reference core. While, the use of Schottky diodes or diode connected MOS diodes for the reference core would reduce the supply voltage, they fail to achieve the desired accuracy. From a circuit design perspective, efficient energy harvesting depends on: available input power, impedance of the antenna, and input impedance of the RF-DC converter. Using fewer stages in the RF-DC converter to get the rectified DC- voltage and minimize the RF-DC losses requires the use of higher voltage at the input of the rectifier, which can be obtained using a matching network. The output voltage of the RF-DC converter can be approximated as [28]:

$$V_O \approx 2N(V_P - V_D) \tag{2.9}$$

where V_O is the output voltage of the RF-DC converter, N is the number of stages, V_P is the peak voltage at the input of the rectifier and V_D is the drop across the switch. Based on equation (2.9), in order to get a high DC voltage with a minimum number of stages, V_P has to be maximized and V_D minimized. From equations (2.7), (2.8) and (2.9) we see that in order to design a matching network and implement the RF-DC converter, we need an accurate estimate of the real (R_{in}) and imaginary parts (C_{in}) of the rectifier and V_D. $R_{in,}$ C_{in} and V_D are governed by the choice of the switch that is used in the RF-DC converter. The possible candidates for implementing the switch in the half wave rectifier based RF-DC converter are: (1) N Schottky diode (2) P Schottky diode and (3) MOS diode. Three factors influence the choice of Schottky diodes over a MOS diode: the MOS threshold

voltage, the available switching voltage and switch current density per sheet capacitance, the figure of merit being A/fF. The current density for a Schottky diode and MOS transistor can be expressed as follows:

$$J_{DIODE} \approx \frac{I_S}{A} e^{\left(\frac{V_D}{n.V_T}\right)} \tag{2.10}$$

$$J_{NMOS} \approx \frac{2n\mu_n {V_T}^2}{L^2} \left(e^{\left(\frac{V_G - V_{TN}}{n.V_T}\right)} \right) \tag{2.11}$$

The f_T for the schottky diode can be expressed as:

$$f_{TDIODE} = \frac{1}{2\pi} \left(\frac{ID}{nV_T C_J} \right)$$

$$= \frac{1}{2\pi} \left(\frac{I_S e^{\left(\frac{V_D}{n.V_T}\right)}}{nV_T C_J} \right)$$

$$= \frac{1}{2\pi} \left(\frac{I_{S0} A e^{\left(\frac{V_D}{n.V_T}\right)}}{nV_T C_{J0} A} \right)$$

$$= \frac{1}{2\pi} \left(\frac{I_{S0} e^{\left(\frac{V_D}{n.V_T}\right)}}{nV_T C_{J0}} \right) \tag{2.12}$$

The f_T for the MOS diode can be expressed as:

$$f_{TNMOS} \approx \frac{1}{2\pi}\left(\frac{ID}{nU_T C_{gg}}\right)$$

$$= \frac{1}{2\pi}\left(\frac{I_S e^{\left(\frac{V_G - V_{TN}}{n.V_T}\right)}}{nU_T C_{gg}}\right)$$

$$= \frac{1}{2\pi}\left(\frac{2\mu_n U_T e^{\left(\frac{V_G - V_{TN}}{n.V_T}\right)}}{L^2 C_{OX}}\right) \tag{2.13}$$

Equation (2.12) and (2.13) reveal that a higher f_T for a diode and MOSFET is obtained when the diode has as higher current density for the same overdrive voltage. Figure 2.6(a) and (b) show the plot of the current and f_T respectively versus the input voltage of a schottky diode for areas ranging from 1μm^2 up to 25 μm^2. Figure 2.7(a) and (b) show the plot of I_D and f_T of an NMOS transistor for lengths ranging from 220nm to 2000nm. From these plots, the log –linear range for the schottky and MOS diodes can be approximated from 0.3V to 0.5V.

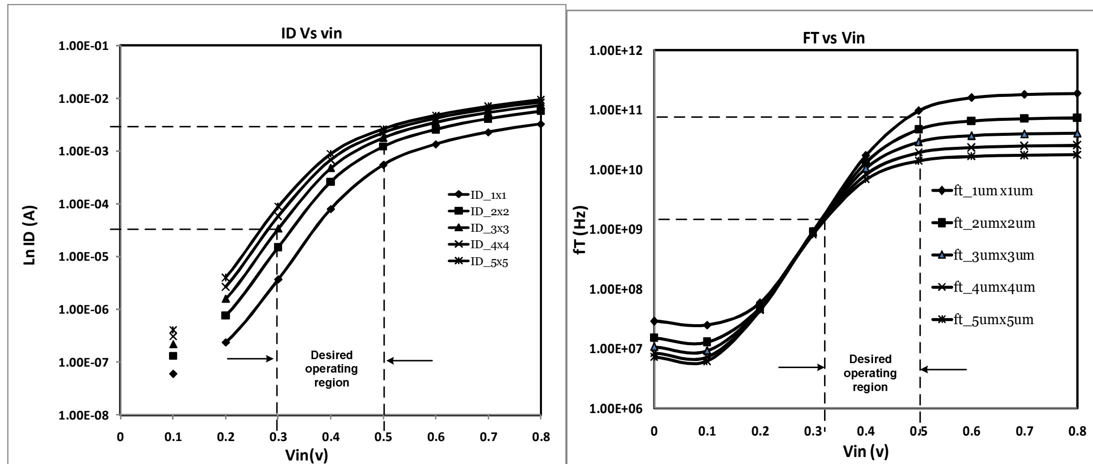


Figure 2.6 (a) Plot of ID vs. Vin and (b) f_T vs. Vin for N Schottky diode

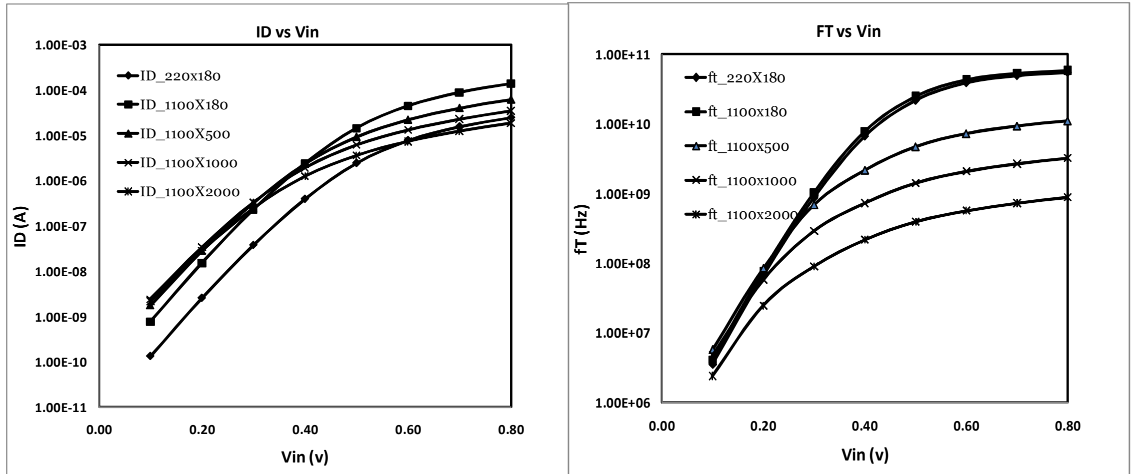


Figure 2.7 (a) Plot of ID vs. Vin and (b) f_T vs. Vin for MOS diode

The switches chosen for the RF-DC converter must have a minimum f_T greater than 2.4GHz, as this is the chosen carrier frequency. From Figure 2.6(b) and Figure 2.7 (b) we can see that all schottky diodes and MOS devices with a minimum length of 220nm meet this criterion around an input voltage of 320mV.The input to the RF-DC converter is a large signal sine wave and the current through the switch is a highly nonlinear pulse. This pulse can be approximated as a raised cosine wave shown in Figure 2.8. The maximum amplitude of the diode current is greater than the DC load current of the RF-DC converter by a factor of 8-10 [23].

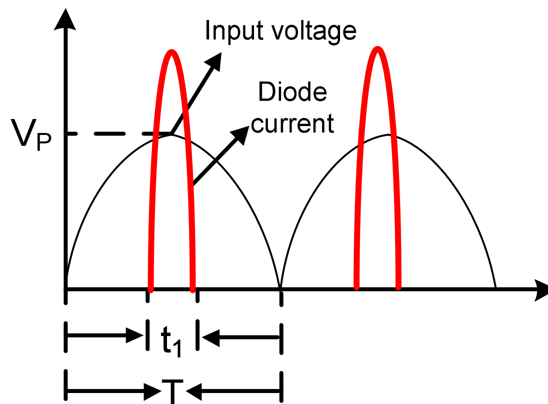


Figure 2.8 Current through the switch

The current through the diode can be written as:

$$I_D = I_S e^{\frac{(V_P \cos \omega t - V_D)}{nV_T}} \tag{2.14}$$

The Taylor series expansion of the current pulse up to five terms is given as:

$$I_D = \frac{I_S e^{\left(\frac{V_P}{nV_T} - \frac{V_D}{nV_T}\right)}}{24{V_T}^2 n^2}\left(24{V_T}^2 n^2 + V_T V_P n t^2 \omega^2 (t^2\omega^2 - 12) + 3{V_P}^2 t^4 \omega^4\right) \tag{2.15}$$

As shown in Figure 2.8, the diode conducts only for duration of "t_1" during the entire period "T" of the input. The conduction angle of the diode can be expressed as [29]:

$$\theta_C = \sqrt{\frac{2V_r}{V_P}} \tag{2.16}$$

Where V_r is the ripple magnitude and V_P is the peak voltage at the input of the rectifier. Substituting a ripple value of 5mV and V_P equal to 0.9V in equation (2.16) we find that the conduction angle is less than 20 degrees and is a valid assumption. The relationship between t_1 and T can be expressed as:

$$t_1 = KT \tag{2.17}$$

Where K is less than one and can be expressed as:

$$K = \frac{\pi}{\theta_C} \tag{2.18}$$

The Fourier series coefficient of the diode current can be expressed as:

$$a_n = \frac{t_1}{K} \int_{\frac{-t_1}{2K}}^{\frac{t_1}{2K}} \frac{I_S e^{\left(\frac{V_P}{nV_T} - \frac{V_D}{nV_T}\right)}\left(24{V_T}^2 n^2 + V_T V_P n t^2 \omega^2 (t^2\omega^2 - 12) + 3{V_P}^2 t^4 \omega^4\right)}{24{V_T}^2 n^2} \cos(N\omega t)\,dt \tag{2.19}$$

which evaluates to

$$a_n=e^{\left(\frac{V_P}{nV_T}-\frac{V_D}{nV_T}\right)}\frac{\left(2I_S V_P{}^2\pi^2\left(N^2(\pi^2)-12\right)\left(-1^N\right)\right)}{3N^4V_T{}^2n^2\omega^2} \tag{2.20}$$

Summation of this Fourier series beyond four terms produces an error of less than one percent in the final result. This suggests that faithful reproduction of this raised cosine pulse wave needs at least four harmonics and the switches must be able to support this. From Figure 2.6(a) and (b) we see that the schottky diodes meet these criteria while still being in the log linear range and achieving the required f_T. Even if the DC load current increases by a factor of 8, the schottky diodes have the required f_T to be operational. A wider MOS device can achieve the required current range but fails to achieve the required f_T. We therefore choose the schottky diode as the device for implementing the switch D_1 and D_2 in the RF-DC converter. Figure 2.6(a) and (b) also reveal that a diode with lower current density and adequate f_T is a preferred device for its lower V_D. MOS devices achieve the required current range and f_T but are less efficient. This helps to minimize the $I_D.V_D$ loss in the RF-DC converter and maximize the desired rectified voltage as per equation (2.9). Based on this discussion a 5μm X 5μm schottky diode was selected to implement the switch in the RF-DC converter. We shall now study the operation of the rectifier in detail.

2.4 Working of the RF-DC converter circuit

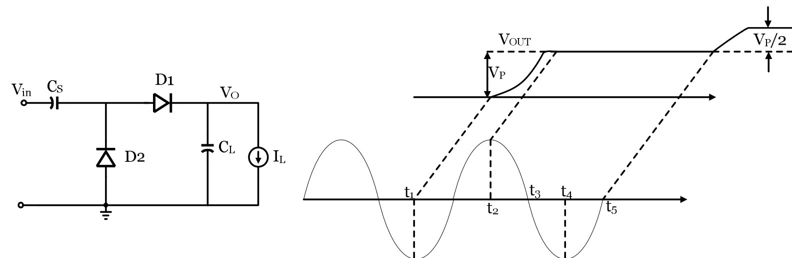


Figure 2.9 Schematic of the one stage RF-DC converter and its waveform [28]

Figure 2.9 shows the schematic of a single stage RF-DC converter and the associated waveform at the V_{OUT} node. Diodes D_1 and D_2 are implemented as Schottky diodes in an N-well, capacitors C_S and C_L are implemented as a dual MIM capacitors in an N-well. I_{DC} is the total load current drawn by the signal conditioning circuitry, V_{in} is the input to the rectifier obtained from the matching network and V_{OUT} is the unregulated DC voltage. We assume that the two diodes D_1 and D_2 are ideal (i.e. zero voltage drop) and I_{DC} is equal to zero. We start with the assumption that V_{in} goes below zero to begin with and the initial condition on V_{OUT} is zero. For $0<t<t_1$, D_2 is reverse biased and D_1 turns on disconnecting node X from V_{OUT} and thus V_{OUT} = 0V in this period. Beyond t_1, V_{in} continues to rise up to V_P at $t = t_2$. During this time, i.e. $t_1<t<t_2$ diode D_1 shuts off and D_2 is turned on. Node X follows V_{in}, until D_2 is turned on and beyond that point; the circuit is a simple capacitive divider between C_S and C_L. For $t_1<t<t_2$,

$$\Delta V_{OUT}=\frac{C_S}{C_S+C_L}\Delta V_{IN}$$

$$\Delta V_{OUT}= \frac{C_S}{2.C_S}\left(V_P-(-V_P)\right) \tag{2.21}$$

$$\Delta V_{OUT}= V_P$$

At $t= t_2$, $V_{OUT} = V_X = V_P$ and the voltage across C_1 is zero. Beyond t_2, V_{in} continues to fall and D_2 shuts off thus disconnecting V_{OUT} and V_X. To maintain the voltage across C_1 equal to zero, V_X follows V_{in} up to t_3. At t_3, $V_X = 0$. Beyond t_3, D1 turns on and D_2 is off while V_X is held at zero up to t_4. As V_{in} continues to rise beyond t_4, V_x follows V_{in} as both D_1 and D_2 are off. V_x changes by the same amount as V_{in} but with reference to zero. At t_5, D_2 is on and the capacitive divider network between C_S and C_L is formed again and

a change of V_P at the input is reflected as change of $\frac{V_P}{2}$ at the output. This is added to the previously stored value of V_P and the new value of the output is $\frac{3V_P}{2}$. The change in output is equal to half the change in input for every subsequent cycle and the final value of the output can be written as [28]:

$$V_{OUT} = V_P\left(1+\frac{1}{2}+\frac{1}{4}+\ldots\right)$$

$$= \frac{V_P}{1-\frac{1}{2}}$$

$$= 2V_P \tag{2.22}$$

Equation (2.22) can be modified to include the diode drop V_D and the presence of the current source I_{DC} which is modeled as a resistor R_L as follows,

$$V_{OUT} = 2(V_P - V_D) \tag{2.23}$$

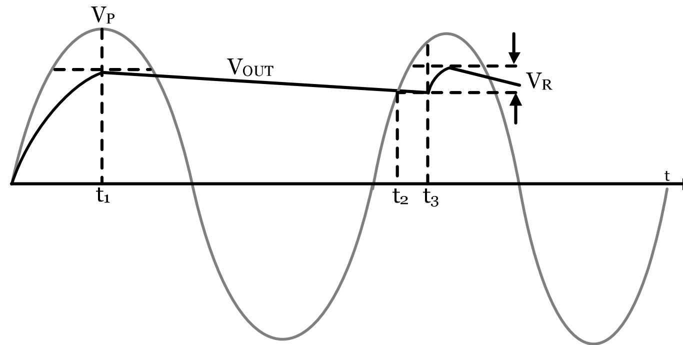


Figure 2.10 Waveform at the output of the rectifier with diode drop and R_L

Figure 2.10 shows the waveform at the output of the rectifier in the presence of load resistor R_L. The drop in voltage is a result of load capacitor being discharged through the load resistor in every half cycle. This behavior is characteristic of a first order RC circuit behavior and the output voltage in time can be expressed as follows

$$V_{OUT} \approx (V_P\text{-}V_D)e^{\frac{-t}{R_L.C_L}}$$

$$\approx (V_P\text{-}V_D)\left(1\text{-}\frac{t}{R_L.C_L}\right)$$

$$\approx (V_P\text{-}V_D)\text{-}\frac{(V_P\text{-}V_D)}{R_L}.\frac{t}{C_L} \qquad (2.24)$$

The first term in equation (2.24) represents the initial condition on the load capacitor C_L and the second term represents the amount of ripple on C_L. The ripple amplitude can be expressed as

$$V_R \approx \frac{(V_P\text{-}V_D)}{R_L C_L F_{IN}}$$

$$\approx \frac{I_L}{C_L F_{IN}} \qquad (2.25)$$

Substituting I_L=60µA and f_{IN}=2.45GHz and a target ripple voltage of 5mV, we find C_L to be greater than 2pF. The Final value of C_L was chosen to be 24pF in the final RF-DC design to keep the ripple amplitude even smaller and prevent the dropout of the voltage due to short signal loss.

2.5 Schottky diode behavior

This section describes the behavior of the schottky diode and the physics that governs their behavior. A schottky diode is rectifying junction formed between a metal and a doped semiconductor material. Depending on the type of the semiconductor material used, they can be classified as either P type schottky barrier diodes or N type schottky barrier diodes.

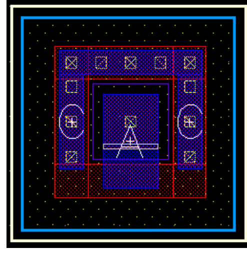


Figure 2.11 Layout of a N type Schottky diode

Figure 2.11 shows the cross section of an N type schottky diode with "A" representing the anode and "C" representing the cathode. The contact from the metal to the substrate is made through the active layer without the implant (i.e. the select layer)[30].

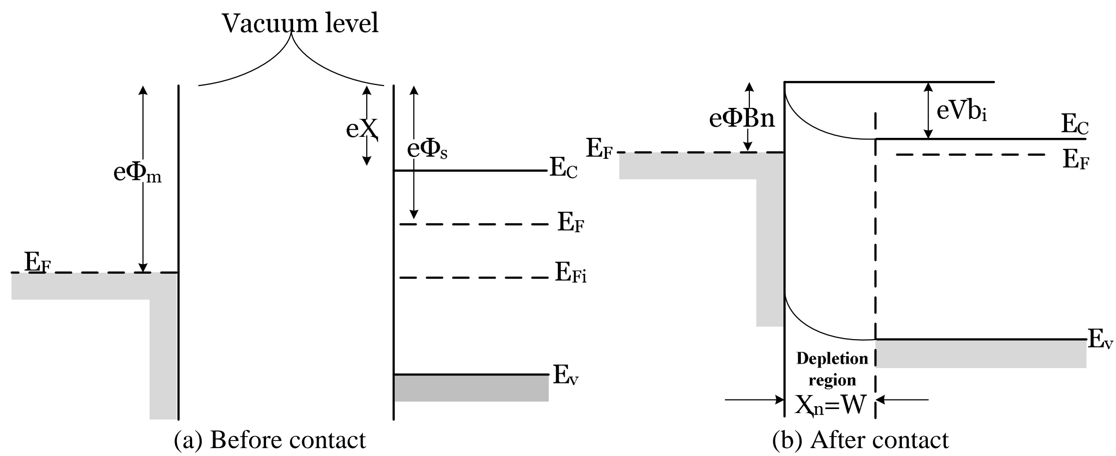


Figure 2.12 Band diagram of the metal and semiconductor [31]

Figure 2.12 shows the energy band diagram of the metal and semiconductor. In the above figure $\emptyset_m$ is the work function of the metal, $\emptyset_s$ is the work function of the doped semiconductor and X is the electron affinity. E_F, E_C and E_V represent the Fermi level, conduction band level and valence band level in the semiconductor. Figure 2.12(a) shows the band diagram before the metal and semiconductor are brought in contact. The fermi level of the doped semiconductor is slightly higher than the metal. When the metal and semiconductor are brought in contact and thermal equilibrium is reached, the fermi levels of both the semiconductor and the metal are equal. Thermal equilibrium is reached by the

flow of electrons form the metal into the semiconductor. The potential barrier seen by these electrons moving from the metal to the semiconductor can be expressed as [31]:

$$\phi_{Bn}=(\phi_n-\chi) \tag{2.26}$$

Similarly, the electrons in the semiconductor conduction band try to move to the metal and the barrier seen by them can be expressed as[31]:

$$V_{bi}=(\phi_{Bn}-\phi_n) \tag{2.27}$$

A schottky diode is considered forward biased when the metal is biased positive with respect to the semiconductor. In this case, the built in potential V_{bi} reduces and the schottky barrierϕ_{Bn} remains constant. The reduction in barrier height causes a majority of the electrons from the semiconductor to move into the metal. This phenomenon is seen as a forward bias current ‘J’ from the metal to the semiconductor in the external circuit and has an exponential relationship with the forward applied voltage V_a. The schottky diode is said to be reverse biased when the semiconductor is biased positive with respect to the metal. The diode exhibits a reverse biased capacitance like an ideal p-n junction whose magnitude can be expressed as [31]:

$$C'=\left[\frac{e\varepsilon_s N_d}{2(V_{bi}+V_R)}\right]^{\frac{1}{2}} \tag{2.28}$$

Where C’ is the capacitance per unit area, e is the charge of the electron ε_s is the permittivity of free space , N_d is the concentration of the donor atoms, V_{bi} is the built in potential of the schottky metal junction and V_R is the applied reverse voltage. The current equation for a schottky diode can be expressed as[31]:

$$J=J_{ST}\left[\exp\left(\frac{eV_a}{KT}\right)-1\right] \tag{2.29}$$

This equation resembles the equation of the p-n junction diode where J is the current flowing through the diode, J_{ST} is the reverse saturation current density, K is the Boltzmann's constant, T is the temperature in Kelvin, e is the charge of the electron and V_a is the applied forward voltage. The reverse saturation current density J_{ST} can be expressed as[31]:

$$J_{ST}=A^{*}T^{2}\exp\left(\frac{-e\emptyset_{Bn}}{KT}\right) \tag{2.30}$$

Where A^{*} is called the Richardson constant. This value depends upon the type of metal used to interface with the semiconductor. The reverse saturation current density for a normal p-n junction can be expressed as [31]:

$$J_{S}=\frac{eD_{n}n_{pO}}{L_{n}}+\frac{eD_{p}p_{nO}}{L_{p}} \tag{2.31}$$

Eq (2.30) and (2.31) were developed based on two fundamental differences in the current flow mechanisms in the diode. Equation (2.30) was developed based on the thermionic emission of majority carriers in the schottky diode while (2.31) was developed based on the diffusion of minority charge carriers in the p-n junction diode. Typical numbers for the Richardson constant, T, $\emptyset_{Bn}$, D_n, n_{po}, D_p ,p_{no}, L_n and L_p reveal that the reverse saturation current density Jst for a schottky diode is larger than Js by a factor of 10^6 [31]. This causes the schottky diodes to a have a lower V_a for a given current as per equation (2.29).

In a conventional p-n junction under forward bias, the electrons from the n type material

try to move to the p side and the holes from the p- type material move to the n side. As these minority carries cross the p-n junction, a capacitance is formed between the p-side electrons and n-side holes. This capacitance is the diffusion capacitance or the stored charge capacitance in the diode. This charge must be removed before the forward biased diode can be turned off. Since majority carriers cause the current flow in a schottky diode, there is no stored charge to be removed to turn off the schottky diode and hence no diffusion capacitance associated with it. This makes the schottky diode switch faster as compared to the regular diode.

2.6 Input impedance of the RF-DC converter

The input voltage or carrier signal across the diode is sinusoidal in nature and the current through the diode is highly nonlinear resulting in highly nonlinear impedance. The nonlinear diode current is comprised of the fundamental and other higher order harmonics. The series LC matching network that precedes the RF-DC converter tunes out these harmonics from the antenna, leaving only the fundamental component. This fundamental component of the diode current is used in calculating the fundamental impedance of the RF-DC converter at the desired operating frequency. Calculating the fundamental impedance of the RF-DC converter requires an initial guess of the voltage available at 2.45GHz in order to estimate the real and imaginary parts of the input impedance [23]. Since the minimum unregulated voltage that is desired is around 1V, preliminary simulations were carried out on a single stage RF-DC converter that was driven by an ideal generator with 1V peak amplitude at 2.45GHz and 54uA load current.

Table 2.3 Simulation of diode current parameters with Vin =1V, IL = 54uA

Diode Area	ID_F (μA)	Iin_F (mA)	ID_{max} (μA)	ID_{min} (μA)	ID_F/I_L	ID_{max}/I_L	$R_{in}(K\Omega)$	$C_{in}(fF)$	Q_{NW}
$1\mu m$ X $1\mu m$	112.4	2.206	547.7	-54.77	2.08	10.14	4.31	142.4	9.21

2μm X 2μm	196.2	2.467	682.5	-213.4	3.63	12.63	3.9171	159.6	8.85
3μm X 3μm	377.3	2.883	672.7	-463.8	6.97	12.45	□.722	186.6	8.56
4μm X 4μm	645	3.45	736.2	-821.6	11.9	13.63	3.34	223.7	8.11
5μm X 5μm	990.6	4.173	1062	-1277	18.33	19.66	2.82	270.4	7.41

Table 2.3 shows the various RF-DC parameters obtained where ID_F is the fundamental component of the diode current and Iin_F is the fundamental component of the input current. ID_{max}, I_{Dmin} are the maximum and minimum diode current values, I_L is the load current, R_{in} is the real part of the RF-DC converter and C_{in} is the imaginary part of the RF-DC converter and Q is the parameter described by equation (2.6).

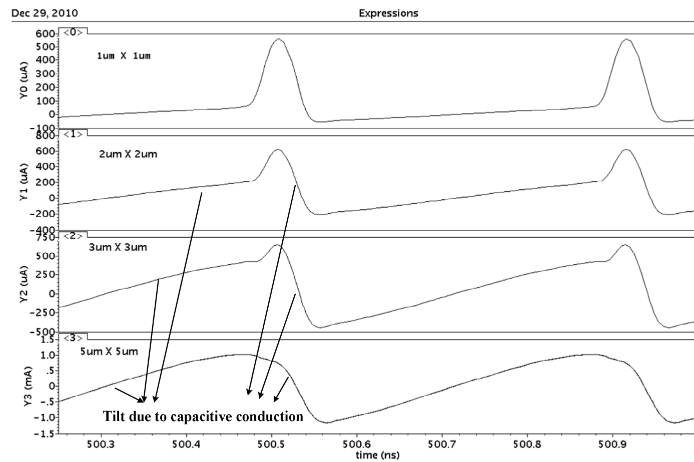


Figure 2.13 Waveforms of the current through the schottky diode

Leakage current and junction capacitance are directly proportional to area of the diode. From Figure 2.13 we observe that a 1µm X 1µm schottky diode has, low leakage and reduced junction capacitance. As a result it behaves like an ideal switch. As schottky diode area is progressively increased, the deviation from the ideal behavior happens for two reasons: conduction through the junction capacitance C_J is significant compared to the diode current and the diode f_T is reduced. We will follow the model for the RF-DC converter outlined in [23] for calculation of the real and imaginary part of the input impedance. The fundamental component of the diode current can be found by taking the Fourier series expansion of the diode current and can be expressed as follows[23, 32]:

$$I_1 = \frac{2}{T}\int I_D(t)\cos(\omega t)dt \cong \frac{2}{T}\int I_D(t)dt = 2I_{LOAD} \quad (2.32)$$

The above equation assumes that the conduction angle of the diode is small and the conduction is taken over a small period, such that $\cos(\omega t) \approx 1$. If the diode were ideal and the parasitics were minimum, an increase in load current would cause the pulse to have a higher peak value and become more narrower to maintain the average value over a one period equal to I_L.

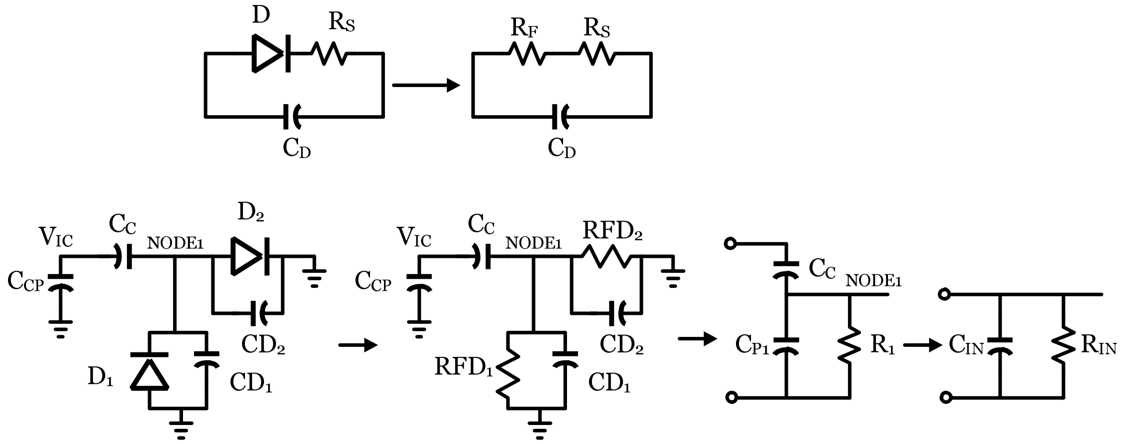


Figure 2.14 Input impedance transformation of a RF-DC network [23]

Figure 2.14 shows the transformation of the fundamental impedance of the Schottky diode into the real and imaginary parts at the input of the RF-DC converter. The output DC voltage is considered as an AC ground for evaluating the real and imaginary parts of the input impedance of the rectifier. V_{IC} represents the voltage at the rectifier input terminals. The voltage at NODE1 can be expressed by the voltage divider between CC and CD1+ CD2 as follows[23]

$$V_{NODE1} = V_{IC}\left(\frac{C_C}{C_C + C_{D1} + C_{D2}}\right) \quad (2.33)$$

The fundamental diode resistance can be expressed as

$$r_{fd}=r_{fd1}=r_{fd2}=\frac{V_{NODE1}}{I_1} \tag{2.34}$$

Where I_1 is the fundamental component of the current as evaluated in Table 2.3

$$r_{fd}=r_{fd1}=r_{fd2}=\frac{V_{IC}}{I_1}\left(\frac{C_C}{C_C+C_{D1}+C_{D2}}\right) \tag{2.35}$$

The shunt resistance R_1 at NODE1 can be expressed as a parallel combination of r_{fd1} and r_{fd2} and the total capacitance C_{P1} as a sum of C_{D1} and C_{D2} [23]

$$R_1= r_{fd1} \| r_{ff2}=\frac{r_{fd1} . r_{fd2}}{r_{fd1}+r_{fd1}}=\frac{r_{fd}}{2}$$

$$C_{P1}= C_{D1}+C_{D2} \tag{2.36}$$

The transformation from R1 to Rin is described below

$$I_{IN}= (V_{IC}-V_{NODE1})j\omega C_C$$

$$I_1= V_{NODE1}j\omega C_{P1}$$

$$I=\frac{V_{NODE1}}{R_1}$$

$$I_{IN}= I_1+I$$

$$(V_{IC}-V_{NODE1})= V_{NODE1}j\omega C_{P1}+\frac{V_{NODE1}}{R_1}$$

$$V_{IC}j\omega C_C=V_{NODE1}(j\omega C_{P1}+j\omega C_C)+\frac{V_{NODE1}}{R_1}$$

$$=V_{NODE1}\left(\frac{1}{R_1}+j\omega(C_{P1}+C_C)\right)$$

$$=V_{NODE1}\left(\frac{1+j\omega R_1(C_{P1}+C_C)}{R_1}\right)$$

$$V_{NODE1}=V_{IC}\frac{j\omega C_C R_1}{1+j\omega(C_{P1}+C_C)R_1}$$

Substituting V_{NODE1} in I_{IN} we have

$$I_{IN}=\left(V_{IC}-V_{IC}\frac{j\omega C_C R_1}{1+j\omega(C_{P1}+C_C)R_1}\right)j\omega C_C$$

$$=V_{IC}\left(\frac{1+j\omega C_{P1}R_1}{1+j\omega(C_{P1}+C_C)R_1}\right)j\omega C_C$$

$$\frac{I_{IN}}{V_{IC}}=\left(\frac{1+j\omega C_{P1}R_1}{1+j\omega(C_{P1}+C_C)R_1}\right)j\omega C_C$$

$$=\frac{(1+j\omega C_{P1}R_1)(1-j\omega(C_{P1}+C_C)R_1)}{1+\omega^2(C_{P1}+C_C)^2R_1^{\,2}}j\omega C_C$$

$$=\frac{1-j\omega(C_{P1}+C_C)R_1+j\omega C_{P1}R_1+\omega^2C_{P1}R_1^{\,2}(C_{P1}+C_C)}{1+\omega^2((C_{P1}+C_C)^2)R_1^{\,2}}j\omega C_C$$

$$=\frac{1-j\omega C_C R_1+\omega^2(C_{P1}+C_C)C_{P1}R_1^{\,2}}{1+\omega^2(C_{P1}+C_C)^2R_1^{\,2}}\ j\omega C_C$$

$$=\frac{\omega^2C_C^{\,2}R_1+j\omega C_C\left(1+\omega^2C_{P1}(C_{P1}+C_C)R_1^{\,2}\right)}{1+\omega^2(C_{P1}+C_C)^2R_1^{\,2}}$$

If $\omega^2(C_{P1}+C_C)^2R_1^{\,2}\gg 1$ then

$$\frac{I_{IN}}{V_{IC}}=\frac{C_C^{\,2}}{(C_{P1}+C_C)^2R_1}+\frac{jC_C\left(1+\omega^2C_{P1}(C_{P1}+C_C)R_1^{\,2}\right)}{\omega(C_{P1}+C_C)^2R_1^{\,2}}$$

If $\omega^2C_{P1}(C_{P1}+C_C)R_1^{\,2}\gg 1$

$$\frac{I_{IN}}{V_{IC}} = \frac{{C_C}^2}{(C_{P1}+C_C)^2 R_1} + j\omega \frac{C_{P1} C_C}{(C_{P1}+C_C)}$$

The above equation suggests that the real part of the input impedance is given as

$$R_{IN} = \frac{(C_{P1}+C_C)^2 R_1}{{C_C}^2}$$

$$R_{IN} = \left(1+\frac{C_{P1}}{C_C}\right)^2 R_1$$

$$R_{IN} = \left(1+\frac{C_{P1}}{C_C}\right)^2 \frac{1}{2} \frac{V_{IC}}{I_1} \left(\frac{C_C}{C_C+C_{D1}+C_{D2}}\right)$$

Since $C_C \gg C_{P1}$ we have

$$R_{IN} \cong \frac{V_{IC}}{2I_1}$$

And the imaginary part of the impedance is given as

$$C_{IN} = C_{CP} + \frac{C_{P1} C_C}{(C_{P1}+C_C)}$$

The 1µm X 1µm diode follows the cosine current pulse model, but as the diode area is increased; the ratio of the fundamental to load current reaches a maximum value of 18.33. A 5µm X 5µm diode was selected to implement the RF-DC switch. Perfect matching of Rin for the 5µm X 5µm Schottky diode from equations (2.7) and (2.8) requires an L_{match} and C_{match} of 23.91 nH and 173.2 fF respectively. The total extracted Cin is greater than the value required to match and the process does not support inductor values with such high Q. A series inductor of 9.489nH having a Q in the range of 4 was selected. This

value of inductor is feasible for on chip matching. The series LC match, requires no additional capacitance and the obtained network Q value (Q_{NW}) is 4.5. This Q is sufficient to provide a 0.9V signal at the input of the rectifier from a 50 ohm -3dBm source. Figure 2.15 shows the operational range of a single stage RF-DC converter driven from a 50 ohm port, while supporting a 54uA DC load current. The simulation shows that up to -3.5 dBm power can be harvested and an unregulated voltage of 1V can be developed to power the reference circuits.

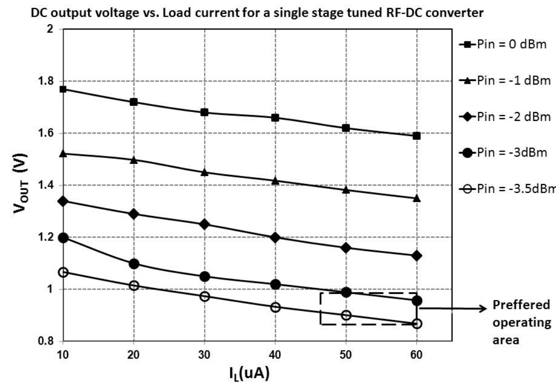


Figure 2.15 Plot of DC voltage vs. load current

Summary

In this chapter we looked into the necessity for a matching network in between the antenna and the RF-DC converter and the different types of matching networks available. The series matching was selected as it provided a voltage boost of Q and the required impedance transformation. Various works were reviewed for implementing the RF-DC converter and the half wave rectifier based design was chosen. The tradeoffs between the MOS diode and Schottky diode were studied and the schottky diode was chosen as it provided the required f_T and lower V_D. The RF-DC converter was implemented as a single stage design preceded by an LC match network to get a high voltage at the input of the rectifier. An expression for the output voltage was developed and the behavior of the

schottky diode was explored. Differences between the schottky diode and the p-n junction were studied and used in calculating the real and imaginary parts of the input impedance of the RF-DC converter. The matching network and the RF-DC converter were designed to be operational in a 50 ohm environment capable to harvesting up to -3dBm of input power while providing a minimum unregulated voltage of 0.9V and supporting 54uA load current.

CHAPTER III

This chapter describes techniques for compensating an operational trans conductance amplifier (OTA). The OTA / Op-amp form the critical circuit in most signal conditioning blocks like the voltage reference, linear dropout regulator, band pass amplifier, MDAC and ADC etc. The OTAs used in the design of these circuits are expected to work in a low V_{DD} range of 0.7V -1V. Most of the OTAs/ OPAMPs are used in a closed loop configuration to guarantee stability during operation. The OTAs can be compensated internally or externally depending on the choice of the application. In this chapter, internal compensation methods would be reviewed for the following configurations:

1. Review of the two stage miller compensation.
2. Indirect compensation for a folded cascode structure with the compensation current and small signal current fed to different nodes.
3. Indirect compensation for a folded cascode structure with the compensation current and the small signal current fed to the same node.

Indirect compensation refers to the scheme of compensation where the feedback current from the second stage of the OTA is fed to the output of the first stage by connecting the compensation capacitor to a low impedance node in the OTA rather than the high impedance output of the first stage [33].

3.1 Miller Compensation

The small signal model for a general two stage OTA is shown in Figure 3.1 below [34, 35]

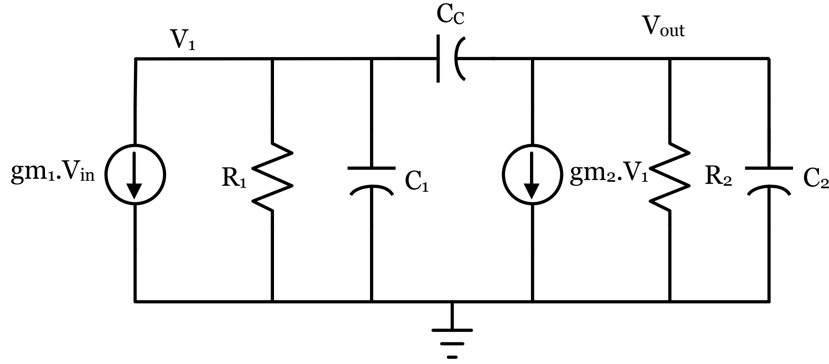


Figure 3.1 Small signal model of a generic two stage miller OTA[33, 34]

In Figure 3.1, gm_1, R_1, C_1 are the transconductance, resistance and capacitance of the first stage, C_C is the compensation capacitor and gm2, R_2, C_2 are the equivalent trans conductance, resistance and capacitance of the second stage respectively. The capacitor C_2 includes the load capacitor that is connected to the second stage. The small signal nodal equations for node V_1 and V_{OUT} are given as follows:

For node V_1:

$$gm_1 V_{in} + \frac{V_1}{R_1} + (V_1 s\, C_1) + (V_1 - V_{OUT})sC_C = 0 \tag{3.1}$$

For node V_{OUT}:

$$gm_2 V_1 + \frac{V_{OUT}}{R_2} + (V_2 sC_2) + (V_{OUT} - V_1)sC_C = 0 \tag{3.2}$$

The transfer function $\frac{V_{OUT}(s)}{V_{in}(S)}$ can be expressed as [33]:

$$\frac{V_{out}(s)}{V_{in}(s)} = gm_1 R_1 gm_2 R_2 \frac{\left(1\text{-}j\frac{f}{f_Z}\right)}{\left(1\text{-}j\frac{f}{f_1}\right)\left(1\text{-}j\frac{f}{f_2}\right)} \tag{3.3}$$

The location of the poles and zeros of the transfer function are summarized in Table 3.1

Table 3.1 Pole Zero locations of a two stage miller OTA

Parameter	Value
DC gain	$gm_1 R_1 gm_2 R_2$
RHP Zero	$\left(\frac{gm_2}{C_C}\right)$
Dominant Pole	$\left(\frac{1}{gm_2 R_2 R_1 C_C}\right)$
Non- dominant pole	$\frac{gm_2 C_C}{(C_C C_1 + C_C C_2 + C_1 C_2)}$
GBP	$\left(\frac{gm_1}{C_C}\right)$

The transfer function has a dominant pole, a non-dominant pole and a right half plane zero (RHP) zero. The bode plot of the transfer function is shown in Figure 3.2 [33]

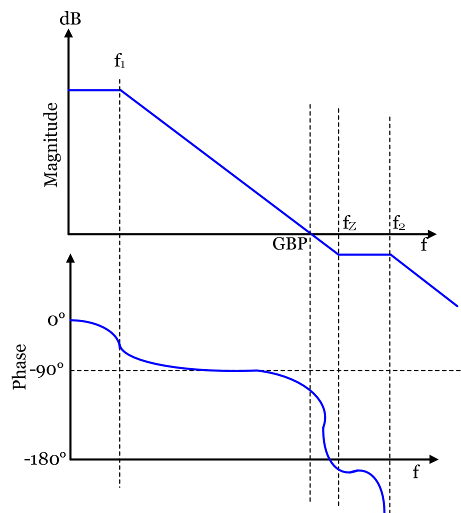


Figure 3.2 Bode plot of a miller compensated OTA

Miller compensation achieves pole splitting by moving the dominant pole to a lower frequency and the non-dominant pole to a higher frequency. In addition, it also creates a RHP zero between the GBP and the non-dominant pole. The RHP zero flattens the magnitude response of the OTA but degrades the phase response. This is because the RHP zero has the same effect as that of a LHP pole, i.e. it increases the overall delay in the closed loop system. The presence of this RHP zero degrades the phase margin significantly thus affecting the stability of the closed loop OTA. The current through the compensation capacitor in equations 3.1 and 3.2 is given as (V_1- V_{OUT}) sC_C. The feed forward part of the current is V_1sC_C and the feedback current is -V_{OUT} sC_C. By blocking the feed forward part of the current through the compensation capacitor, the RHP zero can be eliminated. Two common methods to cancel the RHP zero that are found in the literature are [36-38]:

1. Including a series resistor (R_Z) with the compensation capacitor.
2. Using current buffers and/or common gate stage to feed the compensation current back to the output of the first stage.

In the first method, the series resistor can be implemented as a physical resistor or as a MOS device operating in the triode region. If a physical resistor is used, precise cancelling of the zero will not take place as there will be variations in the resistor depending on the process skew giving rise to pole-zero doublets. If a MOS device operating in the triode region is used as resistor, a separate bias voltage for the gate has to be created. This leads to an increase in the power consumption of the overall structure and is a deterrent for low power design applications.

The second method uses a voltage buffer/ common gate structure to prevent feed forward current and feed the compensation current back to the output of the first stage. The schematic of the indirect compensation scheme using the common gate architecture is shown in Figure 3.3.

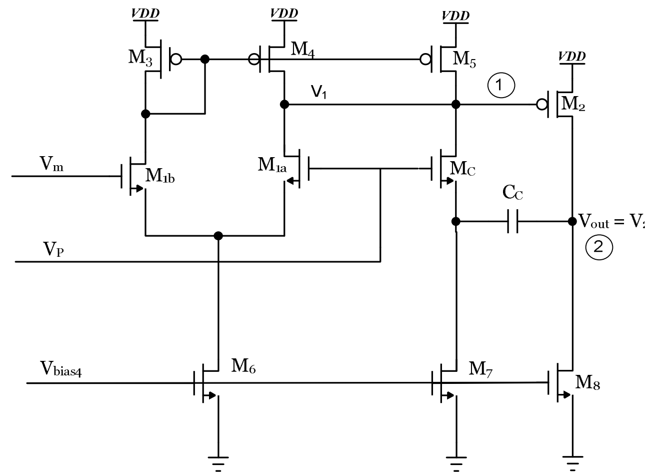


Figure 3.3 Feeding back a current using a common gate device [33]

A detailed analysis of the compensation scheme using the current buffer / common gate device is outlined in [34, 37] and the summary of the pole zero locations is outlined in Table 3.2

Table 3.2 Pole zero locations in indirect compensation scheme

Parameter	Value
DC gain	$gm_1 R_1 gm_2 R_2$
LHP Zero	$\left(\frac{gm_c}{C_C}\right)$
Dominant Pole	$\left(\frac{1}{gm_2 R_2 R_1 C_C}\right)$
Non- dominant pole	$\frac{gm_2 C_C}{C_1 (C_C + C_2)}$
GBP	$\left(\frac{gm_1}{C_C}\right)$

Comparing the parameters of Table 3.1 and Table 3.2, it can be seen that the value of the DC gain, dominant pole and the unity gain frequency (GBP) remain unchanged. A comparison of the non-dominant pole for the miller OTA versus the indirect compensated OTA reveals that the non-dominant pole is located further away from the GBP by a factor of $\left(\frac{C_C}{C_1}\right)$. This value in modern VLSI processes happens to be around 5. The indirect compensation scheme also introduces a LHP zero between the GBP and the non-dominant pole. The positive phase shift of the signal through C_C adds directly to the output of the first stage enhancing the speed and the phase margin of the OTA.

The choice of using a current buffer versus a common gate device depends on the choice of the architecture of the OTA. While current buffers need an additional leg of current to bias them, common gate structures can be self-embedded in the main OTA. Thus the choice of a self-embedded common gate device with indirect compensation helps realize OTAs with a higher GBP and sufficient phase margin in a low power environment. The bode plot of an indirect compensated OTA is shown in Figure 3.4

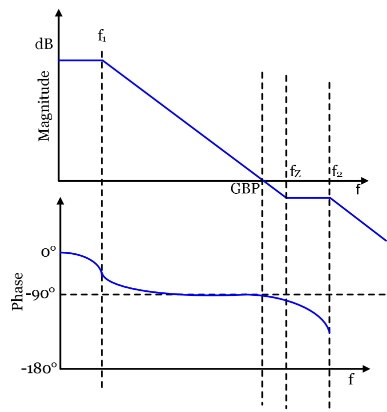


Figure 3.4 Bode plot of the indirect compensated OTA

3.2 Indirect Compensation

The four possible candidates for the indirect compensation are shown in Figure 3.5

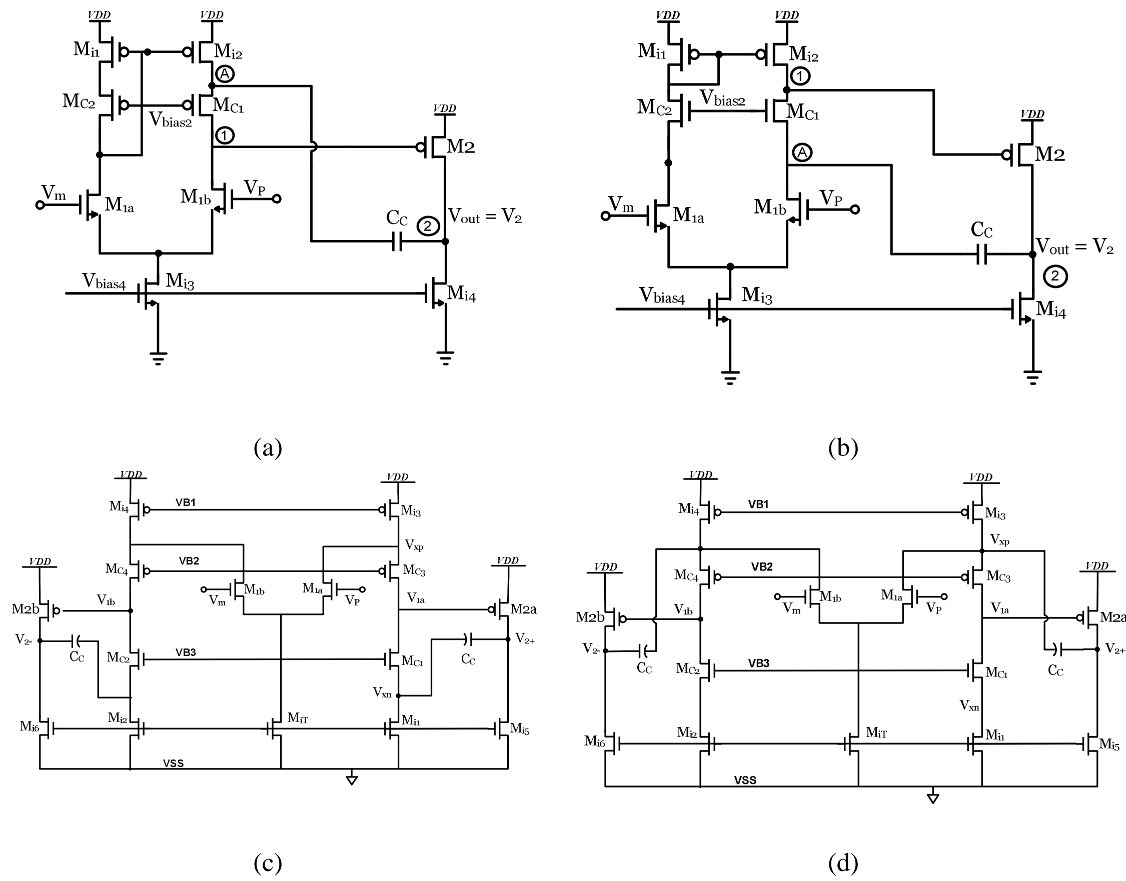


Figure 3.5 Four possible structures for indirect compensation.

Figure 3.5 (a) represents a single ended version of the indirect compensated OTA where the PMOS current mirror is cascoded and Figure 3.5(b) represents a single ended OTA where the input pair devices are cascoded. The detailed analysis of the single ended architecture shown in (a), Figure 3.5(b) is given in [34, 37]. In this work the transfer function of the folded cascode differential OTA with indirect compensation as shown in Figure 3.5(c) and Figure 3.5(d) is analyzed. The following symbolic conventions and assumptions have been made while analyzing the OTA.

Table 3.3 Conventions and assumptions used in indirect compensation

Symbol	Description	Equivalent substitution
gm_1	Trans conductance of the input stage	gm_1
g_i	Output conductance of the	$\frac{gm}{\mu}$

	rail side devices	
g_{cc}	Conductance of the cascode devices	$\frac{gm}{\mu}$
gmc_n,gmc_p	Trans conductance of the cascode devices	gm
C_{xn}	Capacitance of the rail side N Device at node V_{xn}	
C_{xp}	Capacitance of the rail side P Device at node V_{xp}	$C_{xp}= K_r.C_{xn}$
C_{g2}	Output capacitance of the first stage at node V_1	
C_C	Compensation capacitor	
g_{m2}	Trans conductance of the second stage	
g_2	Conductance of the second stage	$\frac{gm_2}{\mu_2}$
C_2	Output capacitance of the second stage	

3.2.1 Indirect compensation with current injected at different nodes

The small signal model of the differential OTA of Figure 3.5(c) with the main differential pair small signal current and compensation current injected at two different nodes V_{XP} and V_{XN} respectively is shown in Figure 3.6

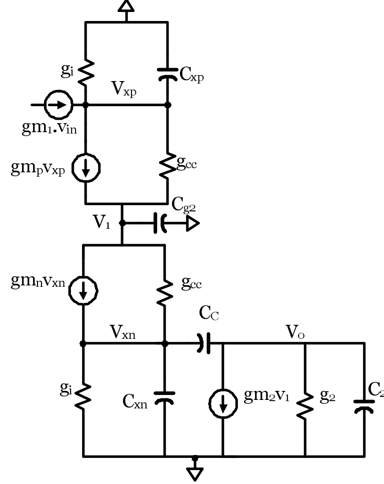


Figure 3.6 Small signal model of OTA with current injection at different nodes

The nodal equations for the above model can be written as:

Vo:

$$V_0 g_2 + V_0 sC_2 + gm_2 V_1 + (V_0 - V_{xn})sC_C = 0 \tag{3.4}$$

Vxn:

$$V_{xn}sC_{xn} + V_{xn}g_i + (V_{xn} - V_0)sC_C + (V_{xn} - V_1)g_{cc} + gm_n V_{xn} = 0 \tag{3.5}$$

V1:

$$(V_1 - V_{xn})g_{cc} - gm_n V_{xn} + V_1 sC_{g2} + (V_1 - V_{xp})g_{cc} - gm_p V_{xp} = 0 \tag{3.6}$$

Vxp:

$$V_{xp}s\,C_{xp} + V_{xp}g_i - gm_1 V_{in} + (V_{xp} - V_1)g_{cc} + gm_p V_{xp} = 0 \tag{3.7}$$

Solving for the transfer function $\frac{V_{OUT}(s)}{V_{in}(S)}$, the location of the prominent poles and zeros are summarized in Table 3.4

Table 3.4 Pole zero locations for current injected at different nodes.

Parameter	Value
LHP Zero	$\left(\frac{gm}{C_C+C_{xn}}\right)$
ω dominant	$\left(\frac{2gm}{C_C\mu^2\mu_2}\right)$
ω non- dominant	$\left(\frac{gm_2C_C}{C_{g2}(C_C+C_2)}\right)$
ω non- dominant	$\frac{gm}{(C_C\Vert C_2)}$
ω non- dominant	$\left(\frac{gm}{C_{xn}K_r}\right)$

Solving the nodal equations (3.4) - (3.7), we obtain a transfer function which has a first degree numerator and a fourth degree denominator. Solving the numerator yields the location of the zero as shown in Table 3.4. The denominator which contains the location of the poles has four possible roots. We make the assumption that the dominant pole and the first non-dominant pole occur at lower frequencies. The location of the dominant pole and the first non-dominant pole using this assumption is given in Table 3.4. The fourth degree expression is reduced to a second degree expression in trying to solve the third and fourth pole locations. This expression is given as:

$$\frac{C_C C_2 s^2}{g_m \omega_{TA}(C_C+C_2)}+\frac{C_C C_2 s}{g_m(C_C+C_2)}+1=0 \tag{3.8}$$

Solving equation (3.8) would yield the exact locations of the remaining non –dominant poles. These poles are placed well beyond the unity gain current gain frequency of the device and do not affect the frequency response of the OTA in use.

3.2.2 Indirect compensation with current injected at same node

The small signal model of the differential OTA of Figure 3.5(d) with the main differential pair small signal current and compensation current injected at the same node V_{XN} is shown in Figure 3.7.

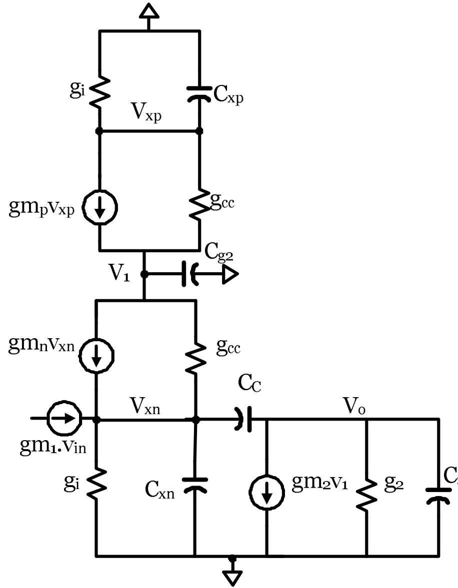


Figure 3.7 Small signal model of OTA with current injection at same node

Since the main small signal current flows into the node V_{XN}, we can ignore node V_{XP} in the nodal analysis. The nodal equations for the above model can be written as:

V_O:

$$V_0 g_2 + V_0 sC_2 + gm_2 V_1 + (V_0 - V_{xn}) sC_C = 0 \tag{3.9}$$

V_{xn}:

$$V_{xn} sC_{xn} + V_{xn} g_i + (V_{xn} - V_0) sC_C + (V_{xn} - V_1) g_{cc} + gm_n V_{xn} - gm_1 V_{in} = 0 \tag{3.10}$$

V_1:

$$(V_1 - V_{xn}) g_{cc} - gm_n V_{xn} + V_1 sC_{g2} = 0 \tag{3.11}$$

Solving the nodal equations (3.9) - (3.11) , we obtain a transfer function which has a second degree numerator and a third degree denominator. The location of the prominent poles and zeros are summarized in Table 3.5

Table 3.5 Pole zero locations for current injected at same nodes

Parameter	Value
LHP Zeros	$\sqrt{\frac{gm.gm_2}{C_C Cg_2}}$
ω dominant	$\left(\frac{2gm}{C_C \mu_2 \mu}\right)$
ω non- dominant	$\frac{gm_2}{Cg_2\left(1+\frac{C_2}{C_C}\right)}, \frac{gm_2\mu}{C_2}$
ω non- dominant	$\frac{gm}{C_2}\left(1+\frac{C_2}{C_C}\right), \frac{gm}{Cg_2\mu}$

Summary:

The indirect compensation of two stage topologies presented in this chapter has been used in the design of the linear drop out regulator. From the above analyzes presented in subsections 3.2.1, and 3.2.2 we see that by using indirect compensation scheme, we can realize stable OTAs with a higher GBP for a chosen compensation capacitor value compared to miller compensation method. Injecting the main small signal current and the feedback compensation current at different nodes yields one LHP zero between the GBP and the non-dominant pole of the OTA. The zero location can be adjusted by proper sizing of the self-embedded common gate device and the compensation capacitor to ensure adequate phase margin for the OTA. The second method of injecting the small signal current and the feedback compensation current yields a cluster of two LHP zeros in

the frequency response of the OTA. Both the methods nevertheless ensure a higher value of non-dominant pole for a chosen C_C in comparison to miller compensated OTA. A minor variant of the indirect compensation scheme uses series connection of transistors to realize a self-embedded common gate device and low impedance node to feed the compensation current. A detailed analysis of this method can be found in [34] .

CHAPTER IV

This chapter is divided into seven sub sections. Section 4.1 presents an introduction to sub threshold design and section 4.2 details the differences between square law behavior and sub threshold behavior. The description of the blocks succeeding the RF-DC converter is outlined in sections 4.3 - 4.7. Section 4.3 describes the design procedure for the temperature independent voltage reference. It covers the DC, AC and noise analysis. Section 4.4 describes the design procedure for the global bias generator that is used to set the reference current for the PLL, ADC, MDAC and thresholder circuits. The description of the low drop out regulator used in generating regulated supplies for the digital and analog blocks is covered in section 4.5 followed by the power on reset circuit and demodulator in section 4.6 and 4.7 respectively.

4.1 Introduction to sub-threshold design

Circuits operating in a neural /biological environment have a strict limitation on the maximum amount of power that can be dissipated while still being fully functional. The circuit blocks succeeding the RF-DC converter consist of both analog and digital circuits like the voltage reference, linear drop out regulators for providing a regulated supply to the digital and analog blocks, state machine, PLL, band pass amplifier and

ADC. The power consumed by digital circuit is given as $P = CV^2f$ were C is the total gate capacitance, V is the supply voltage and f is the operating frequency. The power consumed by analog circuits is given as P = VI, where V is the supply voltage and I is the total current consumed. While the power consumed by the digital circuits can be reduced quadratically by scaling down the supply voltage by a factor of two, the same cannot be done in analog circuits without sacrificing performance. Power consumption of an analog circuit is related to achieving a desired signal to noise ratio (SNR) or dynamic range. The minimum power consumed by the circuit is a ratio of the supply voltage to available signal swing. In a low voltage environment, the signal swing can be maximized by having minimum number of devices between V_{DD} and ground, but to push the noise floor (KT/C) of a circuit further, a high transconductance (g_m) is desired. Analog circuits must therefore be designed to obtain a high value of g_m per unit current i.e. (g_m/I) while still maintaining the required SNR and adequate speed (f_T). When circuits are operated in weak inversion, the relationship between the current and applied input voltage is exponential and results in higher transconductance efficiency and is therefore the preferred mode of operation for low power design.

4.2 Square law versus sub-threshold behavior

4.2.1 Square law behavior

When a MOSFET is operated in the square law region, the unity current gain frequency(f_T) is given as [39]:

$$f_T = \frac{1}{2\pi}\left(\frac{g_m}{C_{gs}}\right) \propto \frac{KP \cdot \Delta V}{L^2 \cdot Cox} \tag{4.1}$$

Where g_m is the transconductance and C_{gs} is the total gate to source capacitance of the MOSFET respectively. Equation (4.1) can be re-written as [39]:

$$f_T = \frac{3KP_n(V_{GS}-V_{THN})}{4\pi L^2 C_{OX}'} = \frac{3\mu_n}{4\pi}\frac{V_{DSAT}}{L^2} \tag{4.2}$$

Equation (4.2) suggests that to obtain high speed, a smaller channel length (L) and a high overdrive voltage (V_{DSAT}) are desired. The transconductance of a MOSFET operating in square law is given as:

$$g_m = \beta_n(V_{GS}-V_{TH}) = \sqrt{2I\beta_n} = \frac{2I}{(V_{GS}-V_{TH})} \tag{4.3}$$

The transconductance efficiency of a MOSFET can be expressed as:

$$\frac{g_m}{I} = \frac{2}{(V_{GS}-V_{TH})} \tag{4.4}$$

Devices in the signal path of the circuit require an overdrive voltage i.e. V_{GS} - V_{TH} of at least 0.2V to obtain a self-gain and transconductance efficiency of 10. This means that if PMOS and NMOS transistors were cascoded to get high gain and output impedance, the permissible signal swing is only 200mV in a 1V V_{DD} environment. Thus operating the transistors in square law region is of very little use in low power designs.

4.2.2 Sub-threshold behavior

The equation for current flowing through a MOSFET in square law region is given as:

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS}-V_{TH})^2 \tag{4.5}$$

Equation (4.5) assumes that when V_{GS} is less than V_{TH}, the drain current of the MOSFET is zero. This however is not true as still a considerable amount of current flows from

source to drain. This region of operation where $V_{GS} << V_{TH}$ is called the sub threshold region. In a square law device, the applied gate voltage causes carriers under the channel to drift from the source to drain across the depletion region, but in sub threshold region , the carriers diffuse from source to drain along the channel causing a current flow in the device [39]. This behavior is analogous to a BJT (with the exception that that they are majority not minority carriers) where carriers are emitted from the emitter and diffuse across the base to the collector. The expression for drain current of a MOSFET operating in sub threshold region is given as [40]:

$$I_D = I_F - I_R = I_{DO} \exp\left[\frac{V_G}{nU_T}\right]\left\{\exp\left[\frac{-V_S}{U_T}\right] - \exp\left[\frac{-V_D}{U_T}\right]\right\} \quad (4.6)$$

where I_{DO} is the leakage current at $V_G = 0$ and is expressed as:

$$I_{DO} \equiv I_S \exp\left[\frac{-V_{TO}}{nU_T}\right] \quad (4.7)$$

I_F and I_R are called the forward current and reverse current respectively and can be expressed as [40]:

$$I_F = I_S \exp\left[\frac{V_P - V_S}{nU_T}\right] \quad (4.8)$$

$$I_R = I_S \exp\left[\frac{V_P - V_D}{nU_T}\right] \quad (4.9)$$

V_S, V_D and V_G are defined as the source, drain and gate voltages of the MOSFET and V_P is defined as the pinch off voltage and is expressed as:

$$V_P = \frac{V_G - V_{TO}}{n} \quad (4.10)$$

In the equations (4.8) and (4.9), I_S is called specific current and represents the asymptotic intersection point of strong and weak inversion regions on the normalized trans conductance versus drain current plot [40] . The specific current can be expressed as:

$$I_S=2n\beta U_T^2 \tag{4.11}$$

$$\beta= \mu_n C_{OX}\frac{W}{L} \tag{4.12}$$

The specific current is used as an important design parameter in sizing the MOS transistors at a particular current density. The term 'n' in equation (4.11) is defined as the sub threshold slope. In sub threshold operation the surface potential is assumed to be constant along the channel [41]. Therefore any change in the gate to substrate voltage of the MOS transistor is to be shared between the gate oxide and the total surface capacitance. The ratio of the change in surface potential to the gate voltage can be expressed as:

$$\frac{\partial\psi}{\partial V_G}=\frac{1}{n}=\frac{C_{OX}}{C_{OX}+C_S} \tag{4.13}$$

For BULK CMOS processes, n ranges from 1.25 to 2. The sub threshold region has three distinct regions of operation and they are:

1. Weak inversion
2. Moderate inversion
3. Strong inversion

Distinction between these three regions is done on the basis of inversion coefficient. The inversion coefficient can be expressed as [42]:

$$IC = MAX\left(\frac{I_F}{I_S}, \frac{I_R}{I_S}\right) \tag{4.14}$$

And the regions of operation can be distinguished as:

Weak inversion: $IC \ll 1$

Moderate inversion: $IC \cong 1$

Strong inversion: $IC \gg 1$

The drain current expression in (4.6) can be rewritten as [40]:

$$I_D = I_F - I_R = I_s \exp\left[\frac{V_P - V_S}{U_T}\right]\left\{1 - \exp\left[-\frac{V_D - V_S}{U_T}\right]\right\} \tag{4.15}$$

When V_D - V_S is greater than 4 or $5U_T$ (100 to 125 mV) the error introduced by the term $1-\exp\left[-\frac{V_D-V_S}{U_T}\right]$ is less than 2% of the drain current. This suggests that we can keep transistors in saturation with 100-125mV of V_{DS} and still maintain an exponential behavior of drain current with respect to V_{GS} and high self-gain. Thus the transistor acts as good voltage controlled current source when operated in weak or moderate inversion resulting in a low gds. The transconductance of the MOSFET operating in sub threshold is found by taking a partial derivative of equation (4.15) with respect to V_{GS} and can be expressed as follows:

$$g_m = \frac{W}{L}\frac{I_S}{nU_T}\exp\left(\frac{V_{GS}-V_T}{nU_T}\right)\left[1-\exp\left(-\frac{V_{DS}}{U_T}\right)\right] = \frac{I_D}{nU_T}$$

$$\frac{g_m}{I_D} = \frac{1}{nU_T} \tag{4.16}$$

Comparing equations (4.16) and (4.4) we find that transconductance efficiency is about 4 times greater in weak inversion than strong inversion. The advantages and disadvantages of operating in weak inversion can be summarized as follows:

Advantages:

1. Exponential relationship between I_D and V_{GS} leads to improved gm efficiency.
2. Voltage required to keep the transistor in saturation is only 4~5 U_T. This gives us a permissible signal swing of 0.8V with PMOS and NMOS transistors between V_{DD} and V_{SS} in a 1V V_{DD} environment.
3. Intrinsic or self-gain (μ) of the device is 4X or higher compared to square law.

Disadvantages:

1. The current mismatch in sub threshold is expressed as [42]: $\frac{\Delta I_D}{I_D} = \frac{\Delta V_{T0}}{nU_T}$ and in square law it is given as: $\frac{\Delta I_D}{I_D} = \frac{2\Delta V_{T0}}{\Delta V}$. The current mismatch is at least four times higher in sub threshold compared to square law. The current mismatch is largely dependent on the threshold voltage change and this is mitigated by allocating sufficient gate area based on $\Delta V_{T0} = \frac{AV_{TH}}{\sqrt{WL}}$ [43].
2. The f_T of a transistor operating in weak inversion is lower compared to the f_T of the device operating in square law and can be expressed as:

$$f_T \cong \frac{\mu_n U_T}{2\pi L^2} \tag{4.17}$$

In a neural / biological environment, the signal bandwidth is from 80Hz – 8 KHz dictating the use of unity gain op-amps approaching 100KHz. For the chosen 180nm bulk

CMOS process, the f_T of an 180nm device is about 6GHz. This offers sufficient bandwidth to operate in weak inversion. Based on the advantages and disadvantages described above, we choose the weak inversion mode of operation to design the front end circuits.

4.3 Voltage reference

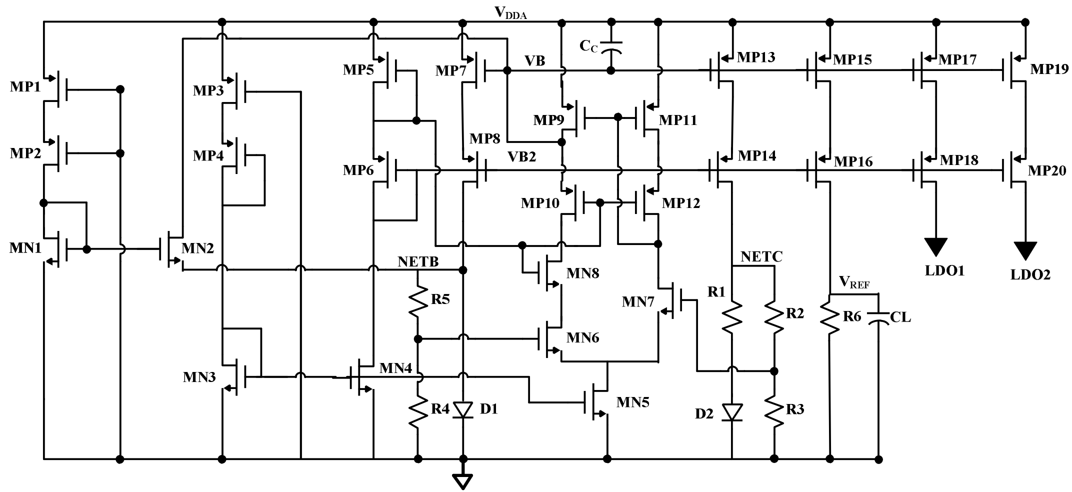


Figure 4.1 Schematic of the voltage reference

Figure 4.1 shows the transistor level schematic used to generate the temperature independent voltage reference and the reference current for the linear drop out regulators. The circuit consists of PMOS transistors MP1-MP20, NMOS transistors MN1-MN8, resistors R1-R6, capacitor C_C, and forward biased PN junction diodes D1 and D2. All PMOS and NMOS transistors are nominal V_{TH} transistors with the bulk of the PMOS transistors connected to V_{DD} and NMOS transistors connected to V_{SS}. MP1 –MP2, MN1-MN2 make up the start-up circuit. Transistors MP3-MP8 and MN3-MN4 provide the required bias voltages VB and VB2. The main reference core consists of diodes D1-D2, resistors R1-R5 and transistors MP7, MP8, MP13 and MP14. An op-amp consisting of transistors MP9-MP12, MN5-MN8 is used for equalizing the node voltages NETB and NETC. MP15, MP16 and resistor R6 form the leg that generates the temperature

independent reference and transistors MP17-MP18 and MP19-MP20 form the reference current legs for the two linear drop out regulators. As V_{DD} is being ramped up, a start-up current is established in transistors MP1-MP2, MN1 as follows:

$$I_{START_UP}=\frac{V_{DD}-VGS_{MN1}}{rds_{MP1}+rds_{MP2}} \tag{4.18}$$

MP1 and MP2 are sized as long channel devices with length equal to 50µm to keep their output resistances high and keep the startup current to a low value of 53nA. The startup current flows through the diode connected transistor MN1 to establish the gate voltage to MN2 to about 550mV. This turns on transistor MN2 which pulls the output of the op-amp i.e. VB low and the inverting terminal of the op-amp high. The feedback loop is turned on and current begins to flow in transistors MP7 and MP13 causing NETB and NETC to rise to 650mV. Since the source of transistor MN2 is connected to NETB, the value of the V_{GS} of MN2 is 100mV once the circuit has reached steady state. With the V_{TH} of MN2 being 450mV, transistor MN2 is turned off and disconnected smoothly once the reference core is stabilized.

4.3.1 DC operation

The reference core consists of diodes D1, D2, resistors R1-R6. The main idea is to add currents of opposite temperature coefficients together to generate a temperature independent current and mirror that current on to a resistor to obtain a temperature independent reference voltage. A current whose value rises linearly with increase in temperature is referred to as a PTAT (proportional to absolute temperature) current and a current whose value reduces with an increase in temperature is referred to as a CTAT

current (complementary to absolute temperature). When two PN junctions are biased at different current densities, the voltage difference between them can be expressed as [44]:

$$\Delta V = nV_T \ln(K) \tag{4.19}$$

Where n is the ideality factor of the diodes, V_T is the thermal voltage and K is the ratio of the areas of the diode. V_T can be further written as KT/q where K is the Boltzmann's constant, T is the temperature in Kelvin and q is the charge of the electron. The value of VT at a room temperature of 300K is 25.68mV. From equation (4.19) we can observe that ΔV is proportional to absolute temperature (PTAT). A diode area ratio of 8 has been chosen to keep this PTAT voltage to 50mV at room temperature. A PTAT current I_{PTAT} is generated by converting this voltage to current using resistor R1 and can be expressed as [44]:

$$I_{PTAT} = \frac{\Delta V}{R1} = \frac{nV_T \ln(K)}{R1} \tag{4.20}$$

R1 was chosen equal to 50KΩ to keep I_{PTAT} equal to 1μA. The voltage drop across a diode biased at constant current exhibits a CTAT behavior [44]. This voltage is used to generate a CTAT current using resistors R_2' and R_4'. R_2' and R_4' were implemented as a series combination of R2-R3 and R4-R5 at NETC and NETB respectively. This series combination was necessary to generate bias nodes that would facilitate a lower input common mode range for the OTA in the reference core. The CTAT current is given as

$$I_{CTAT} = \frac{V_{D1}}{R_2'} = \frac{V_{D1}}{(R_2 + R_3)} \tag{4.21}$$

Choosing R_2', R_4' to be equal to L R1 and the resistor required to generate the voltage reference be NR1, the expression for a temperature independent reference voltage is

obtained by adding equations (4.20) and (4.21) together and multiplying it by NR1 as follows [44]:

$$V_{REF}=\frac{n.V_T.\ln(K).N.R_1}{R_1}+\frac{N.V_{D1}}{L} \tag{4.22}$$

where "L" and "N" are integer ratios of the PTAT resistor R1.Taking a derivative of equation (4.22) for temperature independent behavior and equating it to zero, the value of L can be expressed as [44]:

$$L=\frac{\frac{\partial V_{D1}}{\partial T}}{n\cdot \ln(K)\cdot\frac{\partial V_T}{\partial T}}=9.41 \tag{4.23}$$

This makes the value of R_2' and R_4' equal to 470.5KΩ. R2 was implemented as 200KΩ and R3 was implemented as 266KΩ. This deviation from a total value of 470.5KΩ was necessary to achieve the desired curvature for the temperature independent current. To obtain a target reference voltage of 400mV, the value of N was found out to be [44]:

$$N=\frac{V_{REF}}{n\,V_T\cdot \ln K+\frac{V_{D1}}{L}}=3.28 \tag{4.24}$$

All resistors in the voltage reference circuit have been implemented as RP (precision poly silicon) resistors with a sheet resistance of 165Ω/□. An OTA comprising transistors MP9-MP12 and MN5-MN8 has been used to equalize the node voltages NETB and NETC. The input pair devices in the OTA have been cascoded to increase the output impedance and to obtain a high gain of 4800, to keep the difference between NETB and NETC under a 1mV. Figure 4.2 and Figure 4.3 show the Monte-Carlo DC results of V_{REF} at 27C and across temperature respectively.

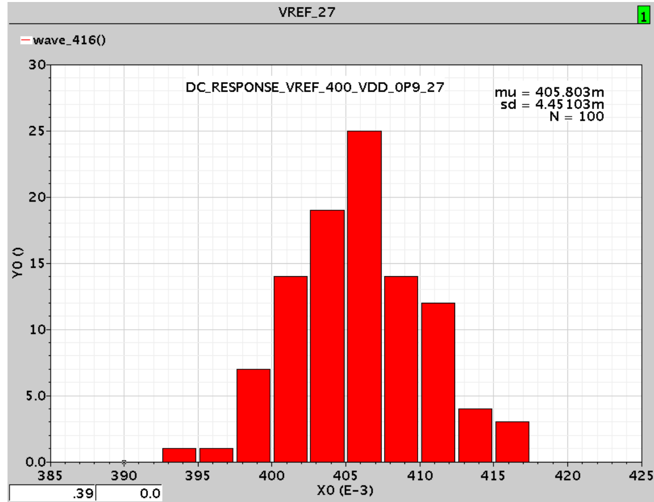


Figure 4.2 Monte-Carlo distribution of V_{REF} = 400mV at 27°C

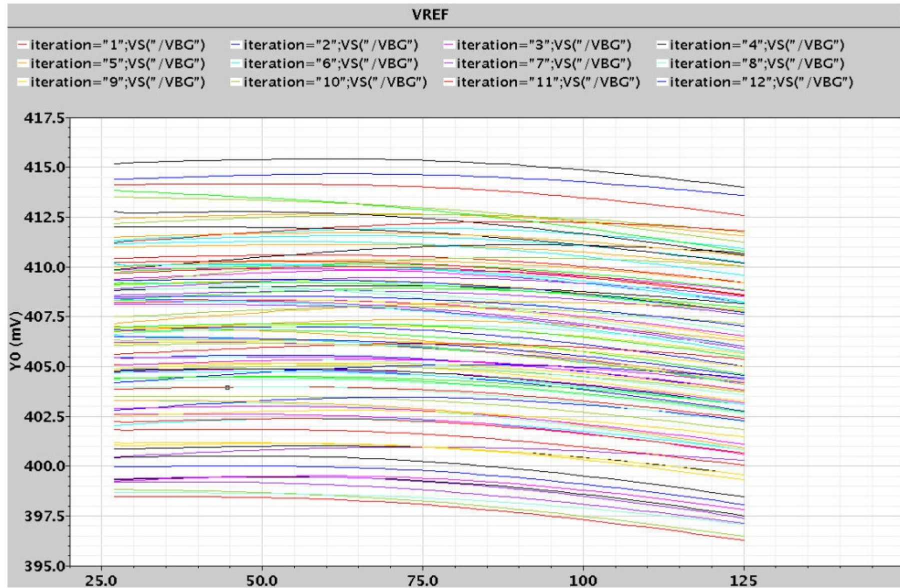


Figure 4.3 Monte-Carlo distribution of V_{REF} from 25°C to 125°C

4.3.2 AC operation

The OTA described above has both positive and negative feedback loops around it. The positive and negative loop gain for the OTA can be expressed as follows:

$$T_{LG+}=g_{m7}\left(gm_7\ ro_7^2 \left\|\left((R_5+R_4)\right\|\frac{1}{gm_1}\right)\right)\frac{A_0}{\left(1+\frac{s}{\omega_{P1}}\right)} \tag{4.25}$$

$$T_{LG-}=g_{m13}\left(gm_{13}\ ro_{13}^2 \left\|\left(R_2+R_3\left\|\left(R_1+\frac{1}{gm_2}\right)\right)\right)\right)\frac{A_0}{\left(1+\frac{s}{\omega_{P1}}\right)} \tag{4.26}$$

where A_O is the DC gain of the OTA and ω_{P1} is the dominant pole of the OTA. Ensuring TLG_- is greater than TLG_+ guarantees loop stability. Proper sizing of capacitor C_C at VB sets the dominant pole ω_{p1} of the OTA and ensures adequate phase margin. The main sources of error in this cell are the OTA offset voltage, resistor mismatch, and mirroring error of M15. Adequate sizing based on [43] ensures 3σ variation of the voltage reference is under 5mV.Capacitor C_C is implemented using a zero V_{TH} NMOS device with its drain and source tied together and $\frac{W}{L}=\frac{300\mu m}{5\mu m}$. This gives us an C_C equal to 20pF and ensures stability of the reference core. The figure below shows the magnitude and phase response of the loop around the OTA. The loop response was obtained by breaking the loop at the output of the OTA i.e. node VB and taking a ratio of the output signal to the test signal injected. Figure 4.4 shows the magnitude and phase plots of the loop response obtained from simulation. The loop has a magnitude of 76dB and a phase margin of 80°.

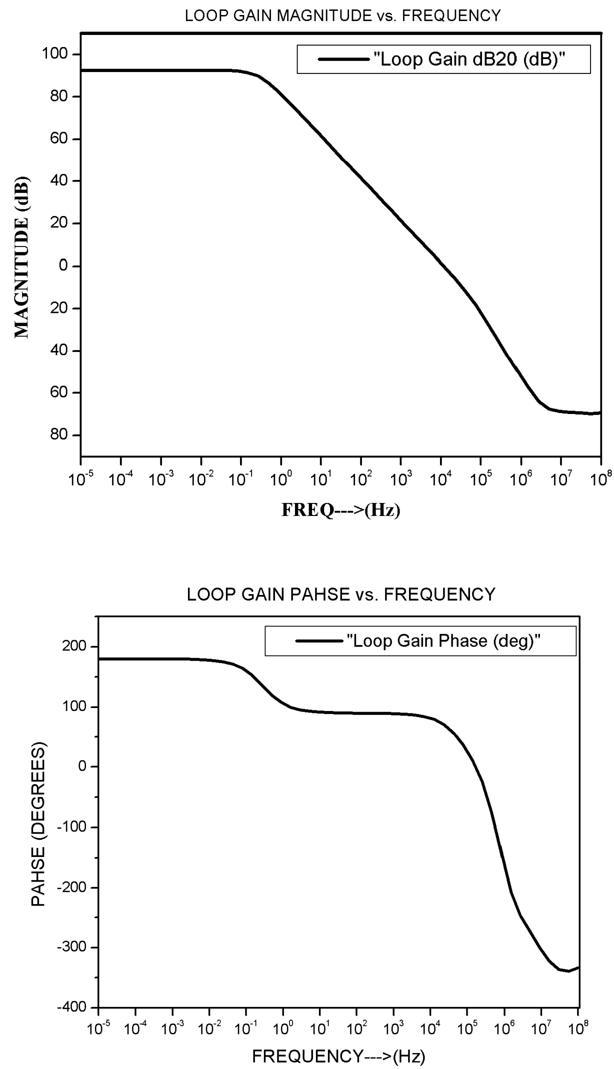


Figure 4.4 Plot of voltage reference loop gain and phase versus frequency

4.3.3 Noise in voltage reference

The reference shown in Figure 4.1 has many devices contributing to the noise at the output node V_{REF}. These can be broadly classified into three main categories:

1. Noise from the core reference consisting of R1-R5, D1 and D2 and the OTA (E_{CORE}).
2. PMOS device MP15
3. Resistor R6.

All sources of noise have to propagate to node VB to get to the output node V_{REF}. The total noise at the reference node can be expressed as follows[45]:

$$V_{noise} = (gm_{15}R_6)\sqrt{E_{g15}^2 + E_{CORE}^2 + \left(\frac{E_{R6}}{gm_{15}R_6}\right)^2} \tag{4.27}$$

Where E_{g15} is noise of the PMOS transistor MP15 and E_{R6} is the thermal noise of resistor R6 and can be expressed as [45]:

$$E_{R6} = \sqrt{4kTR_6} \tag{4.28}$$

$$E_{g15} = \sqrt{\left(\frac{2qI}{gm_{15}^2}\right) + \left[\frac{KF}{f}\frac{1}{gm_{15}^2}\frac{(I)^{AF}}{C_{O?}(L_{15})^2}\right]} \tag{4.29}$$

The cascode device MP16 contributes negligible noise and can be ignored for getting a reasonable noise estimate at the reference output. The derivation of the noise from the reference core E_{CORE} is expressed below. E_{CORE} can further be divided into three categories and they are: E_{NETC}, E_{NETB} and E_{OTA}

$$E_{NETC} = \sqrt{\left(\frac{4KT}{R_3} + \frac{4KT}{R_2}\right)R_2^2 + \left(\frac{4KT}{R_1} + 2qI\right)R_1^2} \tag{4.30}$$

E_{NTEC} propagates to VB as per the following equation:

$$E_{NETCVB} = \frac{1}{gm_{13}} \frac{E_{NETC}}{(R_2+R_3) \parallel \left(R_1 + \frac{1}{gm_2}\right)} \tag{4.31}$$

$$E_{NETB} = \sqrt{\left(\frac{4KT}{R_4} + \frac{4KT}{R_5}\right)R_5^2 + (2qI)(R_4+R_5)^2} \tag{4.32}$$

E_{NETB} propagates to VB as per the following equation:

$$E_{NETBVB1}=\frac{1}{gm_{13}}\frac{E_{NETB}}{(R_5+R_4)\|\left(\frac{1}{gm_1}\right)} \tag{4.33}$$

E_{CORE} can be expressed as a root mean square of $E_{NETCVB1}$, $E_{NETBVB1}$ and E_{OTA} as follows:

$$E_{CORE}=\sqrt{E_{NETBVB1}{}^2+E_{NETCVB1}{}^2+E_{OTA}{}^2} \tag{4.34}$$

A high value capacitor, CL cannot be used as the reference voltage is connected to the non-inverting input of the LDO without impacting its stability. Capacitor CL is selected equal to 2pF to not affect the stability. Figure 4.5 shows the noise plot at the V_{REF} node.

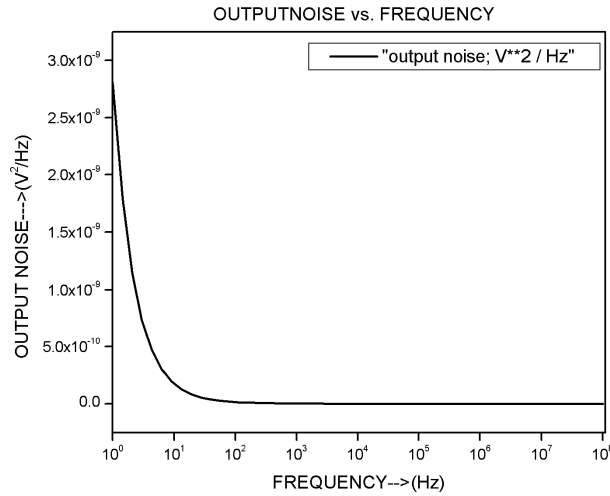


Figure 4.5 Noise plot at the output of the reference node voltage

The plot shows that in the signal frequency of interest i.e. from 500Hz to 8 KHz, the major source of noise is the thermal noise. With a 2pF load at the reference node, the noise voltage level is only about 5pV^2/Hz.

4.4 Global bias generator

A global bias generator that establishes a reference current for the signal conditioning blocks like the PLL, ADC, band pass amplifier etc is shown in Figure 4.6

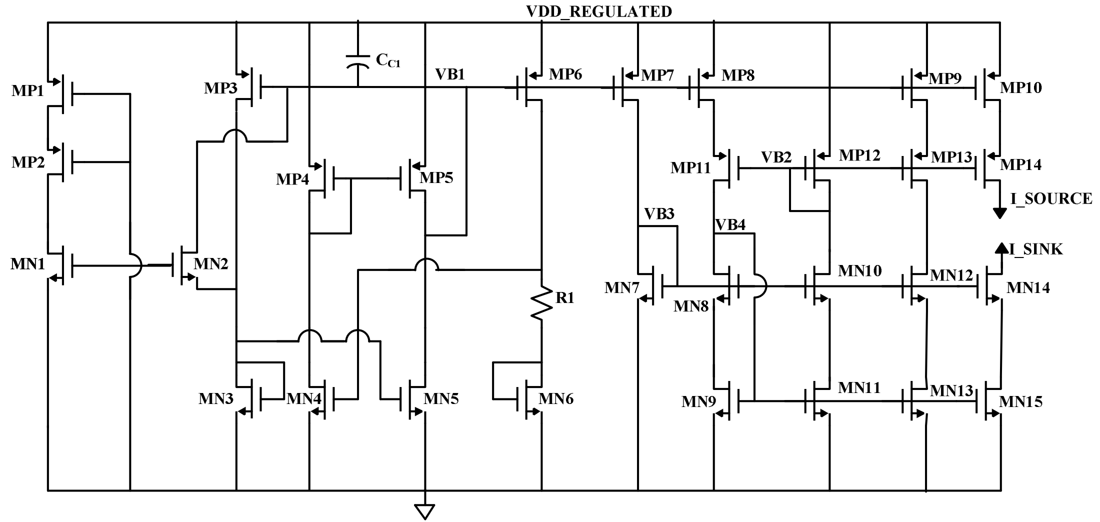


Figure 4.6 Global bias generator for the signal conditioning blocks

The above circuit is a "constant gm" circuit that has been modified for low voltage sub threshold operation. Transistors MP1, MP2, MN1 and MN2 form the start up circuit. The beta multiplier core consists of transistors MN3, MN6 and R1. The minimum V_{DD} for this reference core is given by VGS_{MN6} + I_{REF}R1 + V_{DSMP6}. This value turns out to be about 700mV. Currents of transistor MP3 and MP6 match when their drain-source voltages are equal. Since it is difficult to cascode the PMOS transistors MP3 and MP6, in a 0.7V supply, a tail-less op-amp consisting of MP4-MP5 , MN4-MN5 is used to equalize the drain voltages of MP3 and MP6. Transistors MP3 and MP6 are not diode connected and instead regulated by the OTA. This creates a high impedance node at the output of the OTA and makes the compensation simple by creating a dominant pole at the output with the introduction of the C_{C1}. The VGS of MN3 and MN6 when biased in the sub threshold region can be expressed as:

$$V_{GS3}=nV_T \ln\left(\frac{I_{REF}L_3}{I_{Do}W_3}\right)+V_{TH} \tag{4.35}$$

$$V_{GS6}=nV_T \ln\left(\frac{I_{REF}L_6}{KI_{Do}W_6}\right)+V_{TH} \tag{4.36}$$

Knowing

$$I_{REF}=\frac{V_{GS3}-V_{GS6}}{R_1} \tag{4.37}$$

We get

$$I_{REF}=\frac{nV_T}{R_1}\ln K \tag{4.38}$$

Or

$$R_1=\frac{nV_T}{I_{REF}}.\ln K \tag{4.39}$$

Using the values K = 2, n = 1.5, V_T = 26mV and I_{REF} = 100nA, we get R_1 = 267.9KΩ. Transistor MP7 has been chosen as the main source of the reference current mirror to generate VB2, VB3 and VB4. This was done primarily to add the C_{gs} of MP7 along with Cgs_3 and Cgs_6 and reduce the size of the compensation capacitor required to stabilize the loop. Transistors MP9, MP13, MN12 and MN13 form the final leg of the reference current from which current sources or sinks for the other blocks such as band pass amplifier, PLL, ADC etc. are generated. Figure 4.7 and Figure 4.8 show the Monte-Carlo distribution of the bias margin i.e. V_{DS} minus V_{DSAT} for MP9, MP13, MN12 and MN13. A minimum bias margin of 50mV is maintained across these transistors and the simulation suggests that it is possible to stack four regular V_{TH} PMOS and NMOS transistors in a 700mV supply (4x (5 UT +50mV). Table 4.1shows the reference currents generated for the various blocks in the front end circuit.

Table 4.1 Reference current generated for the various blocks in the front end

Block	Value
PLL	75nA
ADC	25nA
Thresholder	50nA
MDAC	50nA

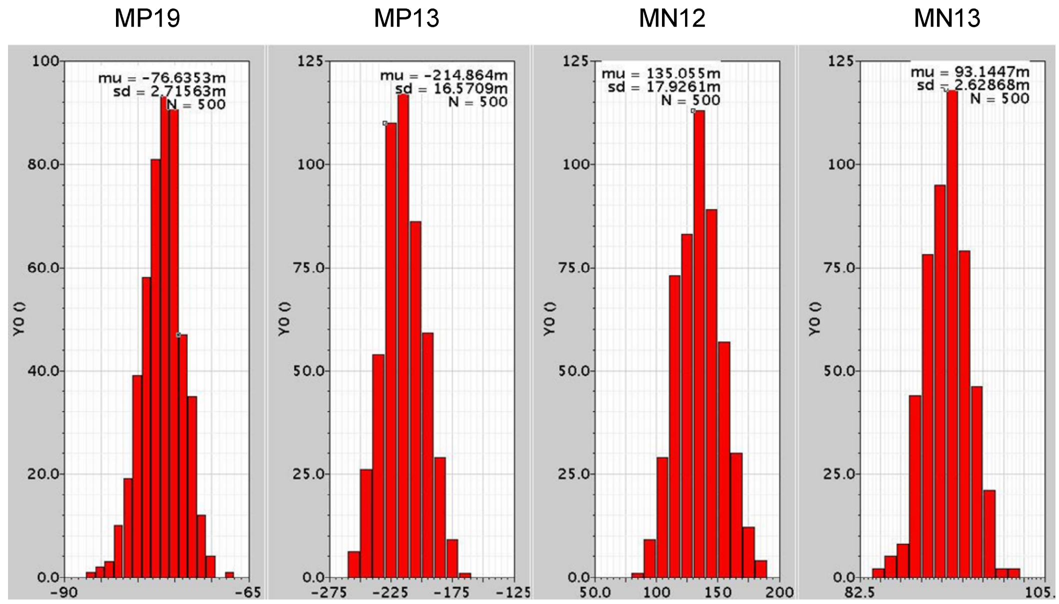


Figure 4.7 Distribution of $V_{ds} - V_{dsat}$ for the reference current leg at 27°C

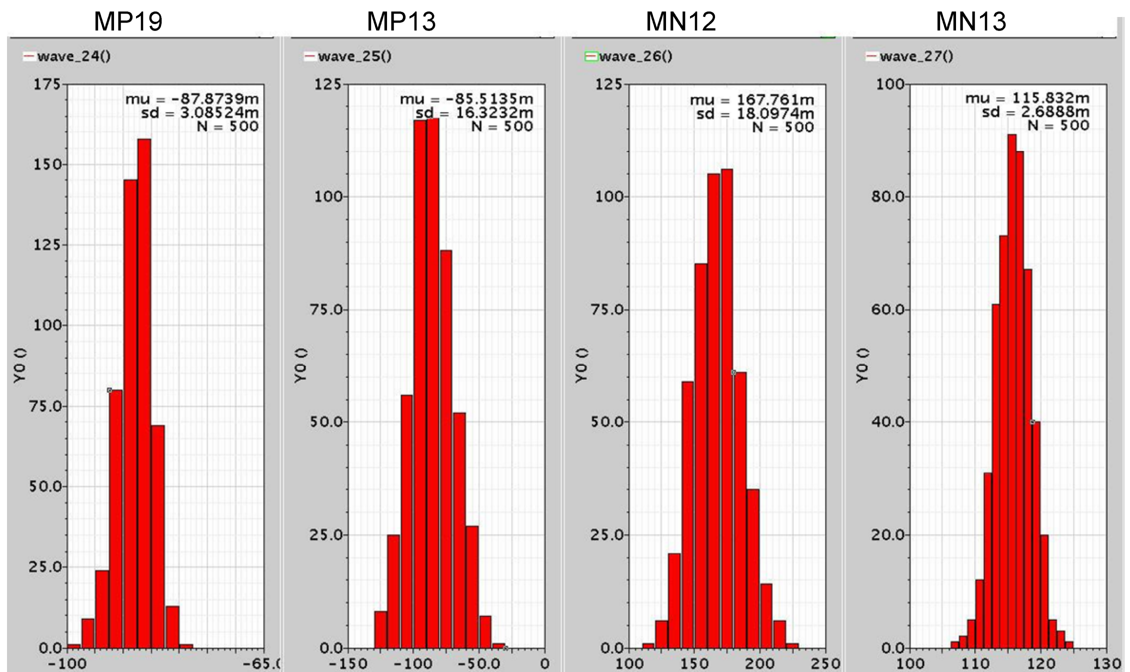


Figure 4.8 Distribution of $V_{ds} - V_{dsat}$ for the reference current leg at 125°C

4.5 Linear drop out regulator

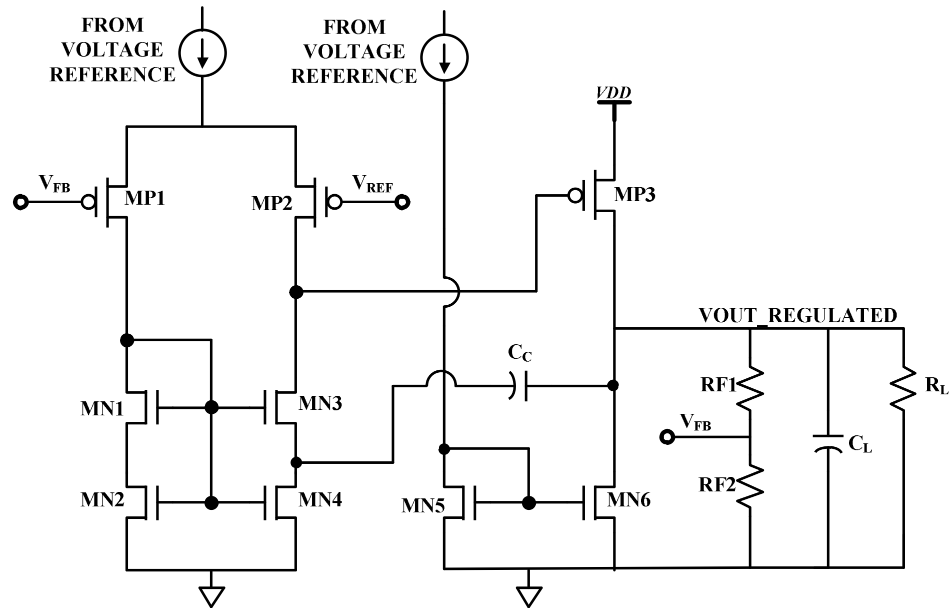


Figure 4.9 Schematic of the linear drop out regulator

A voltage regulator is a device that produces a constant output voltage for a limited range of load currents. Such a circuit is necessary in the RF- Front end for the following reasons:

(1) Isolate the signal conditioning blocks from the main RF-DC converter.

(2) Provide a regulated and scaled down version of the raw V_{DD} generated by the RF-DC converter.

(3) Provide a stable V_{DD} for all the signal conditioning blocks even if there is a change in the input power or load current.

Figure 4.9 shows the schematic of the linear drop out regulator used in generating the regulated power supply for both the digital and analog blocks. The circuit consists of a single stage error amplifier comprising of transistors MP1-MP2, MN1-MN4. The input pair is implemented using PMOS transistors in order to facilitate lower common mode voltage operation. Transistors MN1- MN4 form the NMOS mirror load of the error

amplifier. The mirror load devices were implemented as a series combination of devices with their lengths split in half. This arrangement aids the compensation of the LDO using a left half plane zero (LHP zero) just outside the gain bandwidth product [46]. A current mirror comprising of transistors MN5 and MN6 is connected to the gate of the pass transistor MP3. This was done in order to have minimal current through the pass transistor under no load condition of the LDO. A target value of 700mV is chosen as the analog V_{DD} for the signal conditioning blocks and 400mV for the digital circuits. Performance of this LDO is characterized by the following specifications [47]:

(1) DC PERFORMANCE

The bias currents for the error amplifier (excluding the band gap reference), currents through transistors MN5-MN6 and the current through the feedback ladder RF1-RF2 constitute the DC performance of this circuit. The bias currents of the error –amplifier and the mirror leg have been chosen equal to 2.45µA (temperature independent current from the band-gap reference). The feedback ladder consists of two series resistors RF1 and RF2 of value 38KΩ and 51kΩ respectively. The quiescent current consumed by the LDO under nominal conditions is 15.5µA and the power consumed for an unregulated V_{DD} of 0.9V is 14µW.

(2) AC PERFORMANCE

AC performance will largely be characterized by the loop gain and phase margin around the unity gain frequency. This procedure will be repeated under full load and no load conditions for the LDO to check for stability.

(3) TRANSIENT RESPONSE

The transient response of the LDO comprises of two main phenomena:

(a) Line regulation: It is the ability of the circuit to maintain its output voltage constant for any small change in the input voltage. It is characterized by applying a step input voltage and measuring the change in output voltage. Mathematically , it can be expressed as [48]:

$$\text{line regulation}= \frac{\Delta V_o}{\Delta V_{in}} \tag{4.40}$$

$$\frac{\Delta V_o}{\Delta V_{in}} = \frac{1}{A_{EA}\beta} \tag{4.41}$$

In other words, the line regulation can be minimized by having a high loop gain.

(b) Load regulation: It is the ability of the circuit to maintain its output voltage constant for any change in the output load current. It is characterized by applying a step change in load current and measuring the amount of change in output voltage. Mathematically it can be expressed as:

$$\text{load regulation}= \frac{\Delta V_o}{\Delta I_O} \tag{4.42}$$

The total time taken by the circuit to go from an initial steady state voltage to a final steady state voltage upon the application of a load transient current is called the full load settling time of the circuit. The load regulation of the LDO can be expressed as [48]:

$$\frac{\Delta V_o}{\Delta V_{in}} = \frac{1}{G_{EA}\alpha}\left(\frac{R_{f1}}{R_{f2}}+1\right)\frac{1}{(R_{DS}+R_L)} \tag{4.43}$$

The above equation suggests that the load regulation can be minimized by maximizing the transconductance of the error amplifier and the current gain.

4.5.1 Compensation of the LDO

Figure 4.10 shows the major blocks of the LDO when the feedback loop is broken to analyze the loop gain of the LDO.

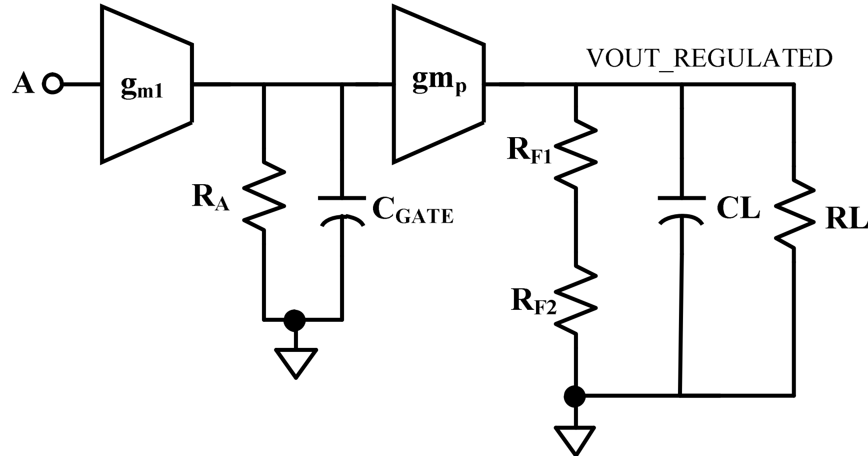


Figure 4.10 Block level diagram of loop gain of the LDO

In the figure shown above, gm1 is the transconductance of the error amplifier, R1 is the effective output impedance of the error amplifier; C_{GATE} is the total capacitance at the output of the error amplifier (gate of the pass transistor). RF1 and RF2 are the feedback resistors required to establish a DC voltage of 400mV at the input of the error amplifier. CL is the load capacitor of 50pF and resistor RL is used for simulating the load current. The effective load resistance at the output of the LDO can be expressed as follows:

$$R_{Leff} = (rds_3 \parallel rds_6) \parallel (RF1 + RF2) \parallel RL \tag{4.44}$$

The minimum unregulated voltage is 0.9V from the RF-DC converter and the minimum value of the regulated supply is 0.7V, the pass transistor MP3 is required to maintain a minimum drop-out voltage of 200mV. Under the maximum load current of 60µA, the drain current of the PMOS pass transistor can be expressed as:

$$I_D = \frac{1}{2}\mu_p C_{OX}\left(\frac{W}{L}\right)(V_{DSAT})^2 \quad (4.45)$$

Using a channel length of 300nm in order to obtain the maximum f_T, we find that for a drop out voltage of 200mV, the width of the pass transistor is required to greater 32µm. The table below shows the properties of the pass transistor stage for minimum and maximum load currents obtained from simulation.

Table 4.2 Pass transistor parameters for minimum and maximum load currents

I_{LOAD}	g_{mpass}	R_{leff}	$g_{mpass}\,R_{leff}$
60uA	668.2µS	7.9 kΩ	5.28
10uA	183.9µS	10 KΩ	1.8563

Referring to Figure 4.10 the transfer function of the loop can be expressed as:

$$\text{Loop gain} = T_1 T_2 T_3 \quad (4.46)$$

Where the transfer function of the error amplifier which is given as:

$$T_1 = \frac{-gm_1 R_A}{(1+sR_A C_{GATE})} \quad (4.47)$$

knowing $R_A = r_{ds2} \| r_{ds3}$ and $C_{GATE} = \left(C_{db2} + C_{db3} + Cgs_{mp3} + Cgd_{mp3}\left(1+gmp_3 R_{leff}\right)\right)$

The transfer function of the pass transistor stage and the feedback ladder stage can be expressed as:

$$T_2 = \frac{-gmp_3 R_{leff}}{\left(1+s.CL(R_{leff})\right)} \quad (4.48)$$

And

$$T_3 = RF2/(RF2+RF1) \quad (4.49)$$

The above equations suggest that there are two poles that are prominent in the frequency response of the LDO. The location of these poles and zero are given as:

$$P_1 = 1/(2\pi C L R_{leff}) \tag{4.50}$$

And

$$P_2 = 1/(2\pi\, R_A C_{GATE}) \tag{4.51}$$

Table 4.3 and Figure 4.11 below show the pole –zero locations and the bode plot for full load and light load conditions.

Table 4.3 Pole zero locations for the uncompensated loop of the LDO

I_L	R_A	C_{GATE}	P_1	P_2
60 µA	8.9MΩ	125.3fF	141.43KHz	402.86KHz
10µA	19.377MΩ	169.41fF	48.50kHz	93.6KHz

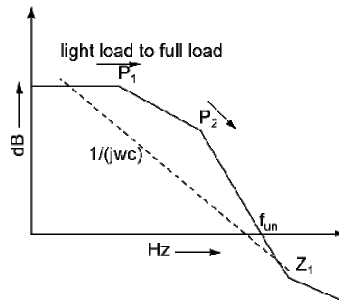


Figure 4.11 Movement of poles under light load to full load condition

The two poles are very low in frequency for both light load and full load conditions and a capacitor of 50pF cannot be used to stabilize the LDO as the phase margin approaches 0°. When the load capacitor is increased to 1uF or 10uF, then the pole associated with the output node becomes the dominant pole. For an SOC solution in a neural environment, such capacitor sizes cannot be realized on chip and are highly undesirable off chip. To compensate the LDO, we choose the indirect compensation scheme with split length implementation of the current mirror load in the error amplifier [49]. The indirect compensation scheme results in pole splitting of the dominant and non-dominant poles by

indirectly feeding back the signal from the second stage (i.e. the output node) to the output of the first stage [49]. In addition to pole splitting, it also introduces a left half plane zero between the GBP of the OTA and the non-dominant pole. The LHP zero helps improve the phase margin of the LDO. The unity gain frequency and the LHP zero location are given as follows [49]:

$$f_{un} = \frac{1}{(2\pi)} \frac{gm_1}{C_C} \tag{4.52}$$

And

$$f_{LHP\ ZERO} = \frac{1}{(2\pi)} \frac{4\sqrt{2}gm_1}{3 \cdot C_C} \tag{4.53}$$

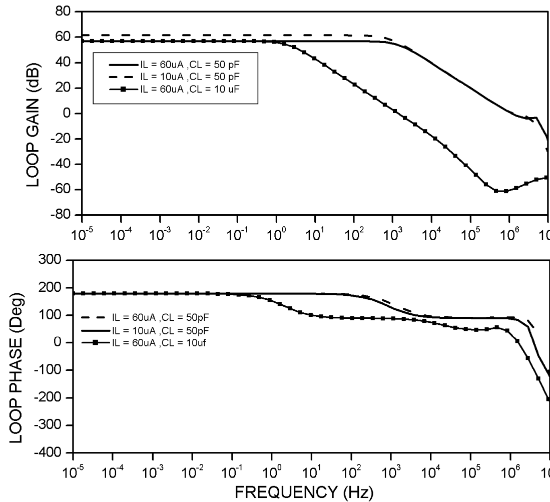


Figure 4.12 Loop gain and phase plots for minimum and full load conditions

Figure 4.12 shows the magnitude and phase response of the loop of the LDO. This loop response has been obtained by breaking the loop between V_{FB} and A as shown in Figure 4.10. The loop GBP is around 1MHz with a compensation cap of 3.2pF for both light load and full load conditions. The phase margin in both the methods is between 85° and 90° respectively. The LDO has been designed with a DC loop gain of 60dB, a unity gain

frequency of 1.02MHz at 54uA and 1MHz at 10uA while consuming 15uA current. The second LDO for the digital blocks has an identical architecture as the LDO for the analog blocks. Since the regulated voltage required for the digital blocks is 400mV, this LDO has been connected in the unity gain configuration without additional feedback ladder. This LDO consumes 3.6μA of current. Figure 4.13 shows the behavior of the output node for a step change in the input voltage. The input voltage was varied from 0.9V to 1.1V in 1μS .The simulated line regulation is 0.03 V/V.

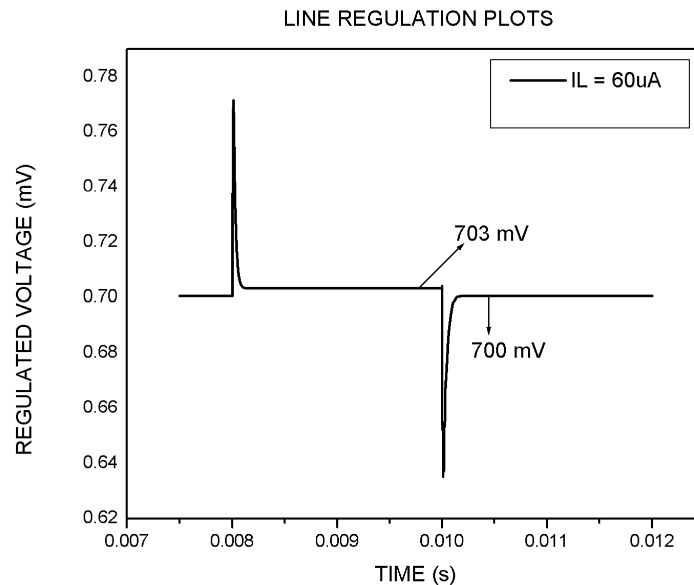


Figure 4.13 Load regulation of the LDO for a step change in input voltage

Figure 4.14 shows the response of the output node of the LDO for a step change in load current from 10μA to 60μA in 1μS and Figure 4.15 shows the settling time of the LDO.

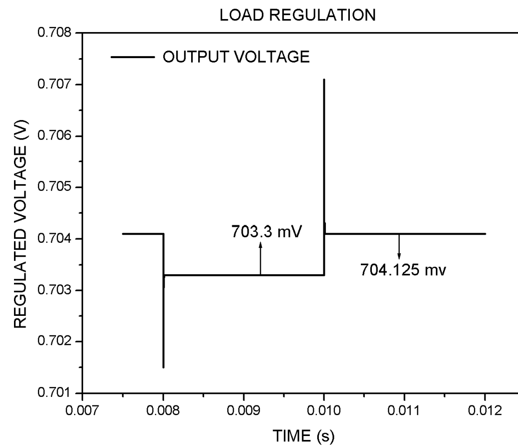


Figure 4.14 Load regulation of the LDO for a step change in load current

The simulated load regulation is 0.001 V/V. The settling time of the LDO from a light load of 10µA to a full load of 60 µA is equal to 3.2 µS.

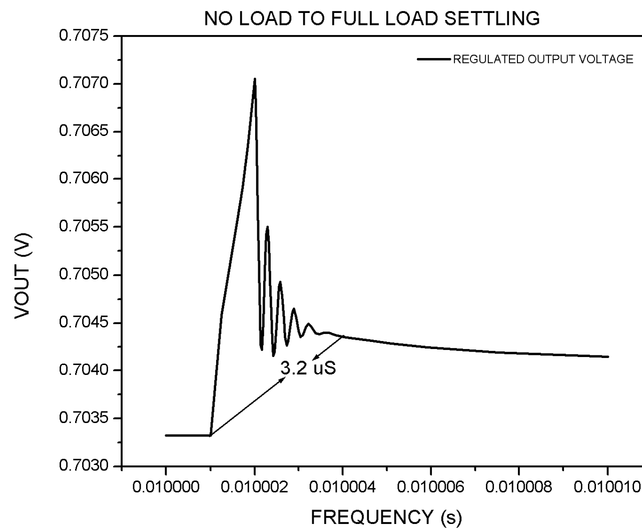


Figure 4.15 Settling time of the LDO from no load to full load

The simulated performance of the LDO is summarized in Table 4.4.

Table 4.4 Performance summary of the LDO

Parameter	Specification
DC LOOP GAIN	60 dB
GBW	1.02 MHZ (IL = 60 µA) 1MHZ (IL = 10uA)
PSRR	-32 dB @DC -20 dB @ 1KHz
Settling time	3.2 µS (no load to full load settling)

Quiescent current	15 µA

4.6 Power on reset

A power on reset is a signal to the other blocks i.e. the memory, PLL, ADC etc. that the regulated power supply has reached its desired steady state value. This signal is also used to reset the flip flops to a desired starting logic level. The POR places the other circuits is reset mode until a stable reference voltage has been obtained. The POR is based on the rise time of the regulated power supply. The regulated supply is compared with a delayed level of the reference voltage and this signal is further delayed to set the power on reset signal. Figure 4.16 and Figure 4.17show the schematic of the power –on –reset circuit and the simulation result.

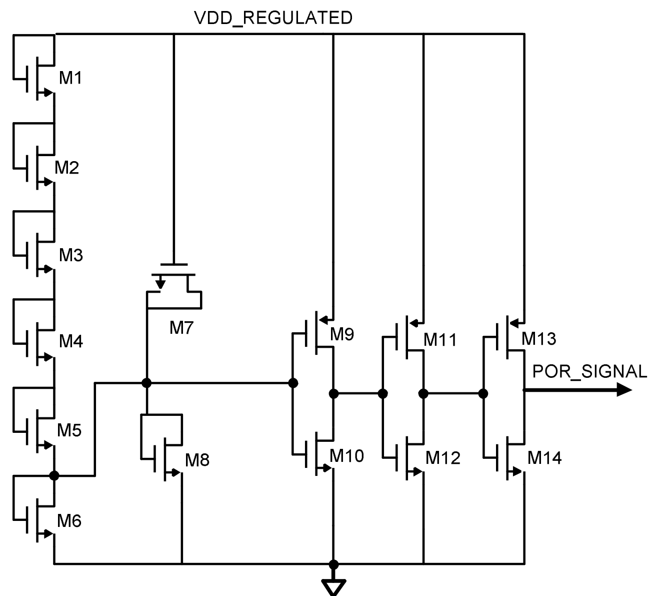


Figure 4.16 Schematic of the power on reset circuit

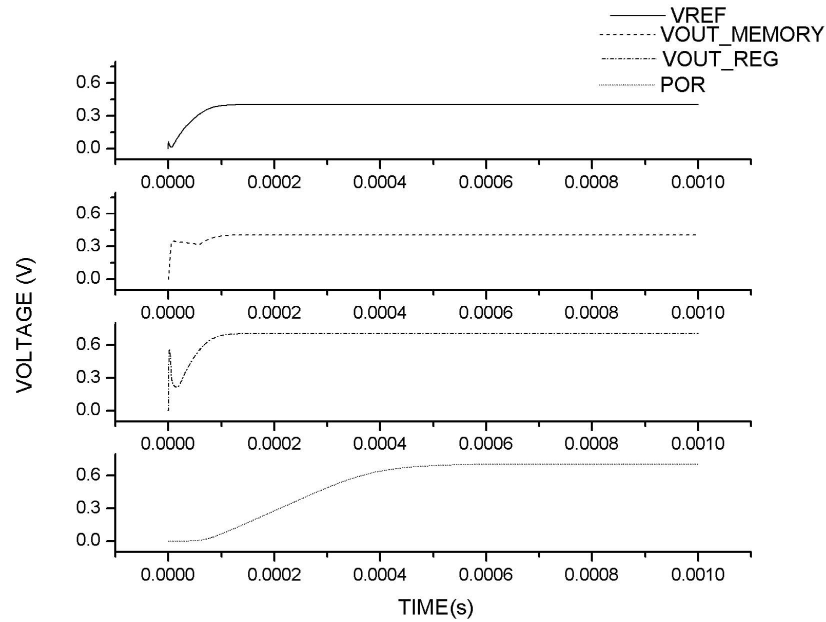


Figure 4.17 Simulation and power on reset circuit

4.7 Demodulator

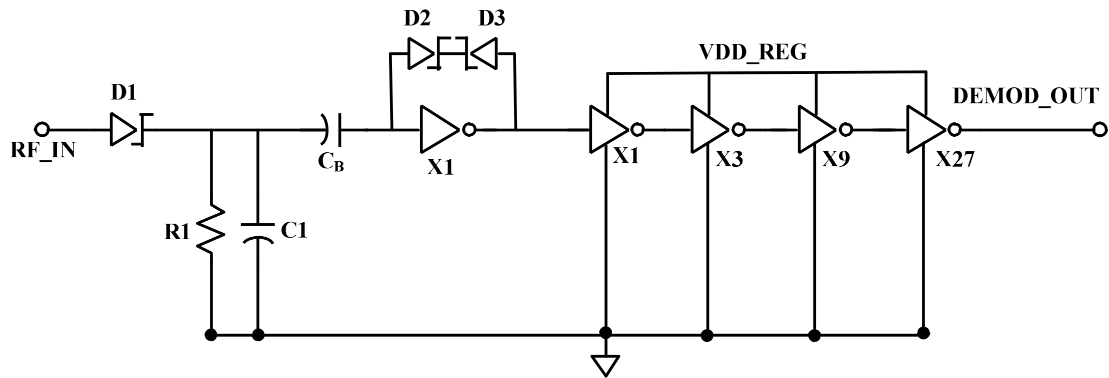


Figure 4.18 Schematic of the demodulator

Figure 4.18 shows the schematic of the demodulator. The demodulator is a circuit that is used to establish the reference clock signal for the PLL. The input signal to this demodulator / RF-DC converter is usually an amplitude modulated signal that has both signal and the carrier information in it. The signal information is at 3.2MHz and the carrier is at 2.45GHz which need to be separated. The demodulator consists of a peak

detector circuit comprising the diode D1, R1 and C1. The peak detector is followed by a simple amplifier which is followed by a series of buffers to get a final clear demodulated signal. Capacitor C_B is used to AC couple the peak detected wave to the amplifier. The simple amplifier comprises of an inverter whose input and output are connected using back to back Schottky diodes as shown in Figure 4.18. The inverter is biased at or near $V_{DD}/2$ when operated in this configuration. During the positive cycle of the modulated signal the capacitor is charged by the current of diode D1 to V_P-V_D where V_P is the carrier peak voltage and the V_D is the voltage drop across the diode. In the negative cycle the diode D1 is reversed bias and the capacitor C1 starts discharging through the resistance R1. The RC time constant must be chosen such that it is slow enough for the ripple at the output to be low and fast enough to follow any change of the modulating signal. The diode D1 was implemented as a schottky diode R1, C1 have been chosen equal to 8.5KΩ and 1.2fF respectively. This gives us a RC time constant of 10.2ns or an upper cut off frequency of 15.62MHz. The carrier frequency in our case is 2.4GHz and the modulating frequency is 3.2MHz. The demodulator and the RF-DC converter have common inputs and are connected to the output of the matching network. The matching network and the RF-DC converter have been designed in such a manner that the minimum peak voltage of the carrier wave is 900mV. For a target modulation index of 10% to 20%, the minimum modulation depth that can be obtained is 180mV. With the depth of modulation being 180 mV and the inverter biased at $V_{DD}/2$, the peak detector should not decay more than 90mV between two positive peaks of the carrier. The minimum value of the carrier frequency that can be used is calculated as follows:

$$V_P-V_D-0.09=(V_P-V_D)e^{\frac{-t}{\tau}} \tag{4.54}$$

$$\frac{t}{\tau} = \ln\left(\frac{V_P - V_D}{V_P - V_D - 0.09}\right)$$

or

$$t = \tau \ln\left(\frac{V_P - V_D}{V_P - V_D - 0.09}\right)$$

substituting V_P = 0.9V, VD = 0.5V and τ = 10.2nS, the minimum carrier frequency necessary for modulation is found to be 340MHz. The figure below shows the waveforms of the demodulated output for a amplitude modulated input.

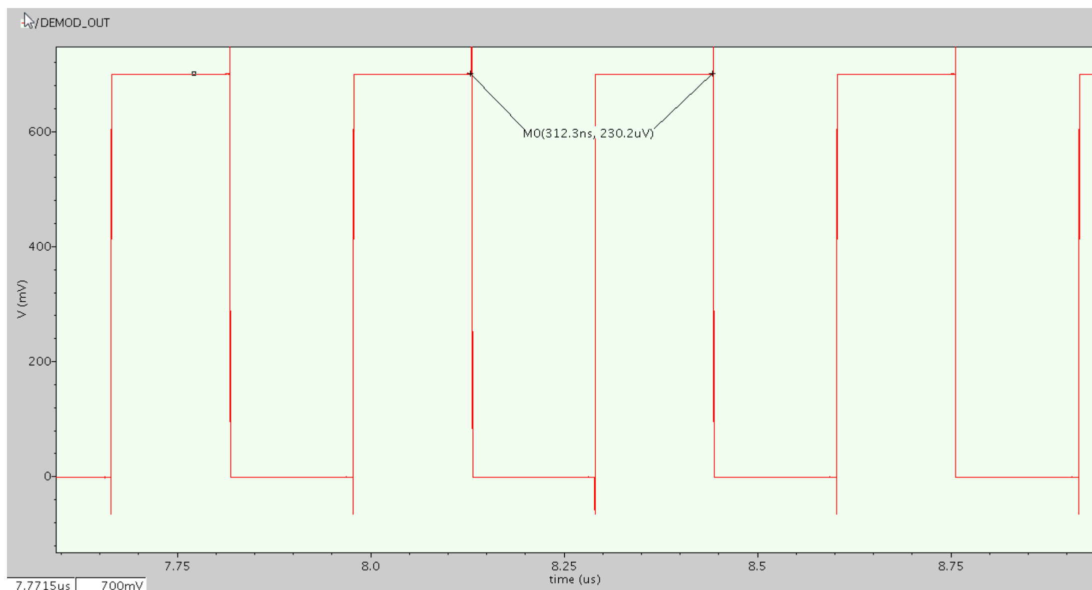


Figure 4.19 Output waveform of the demodulator

Summary

In this chapter we looked into the behavior of the MOS transistor in the sub threshold regime to begin with. Operating MOS transistors in sub threshold regime is preferred for circuits operating in the neural environment where power dissipation must be minimized. The transistors have the required f_T to be operational while providing the required

dynamic range and SNR. The exponential relationship between the drain current and the gate to source voltage of the MOS device leads to an increased transconductance efficiency. The ability of a MOS device to be in saturation with just 100 – 125 mV gives us enough head room for signal swing in a 1V V_{DD} environment with high open loop gain. The design of the temperature independent voltage reference that produces a 0.4V reference voltage for the LDOs has been looked into. Analysis of the DC, AC, transient response and noise sources has been looked into. A global bias generator that provides reference current to the PLL, ADC, thresholder and MDAC has been designed in the sub-threshold regime. Two LDOs that provide regulated voltages of 0.7V and 0.4V for the analog and digital blocks respectively has been looked into. The LDOs were compensated using the indirect compensation scheme which achieves a wide bandwidth for a smaller value of compensation capacitance. The indirect compensated LDO achieves a GBP of 1MHz and an excellent phase margin of 80º. In addition to the above mentioned blocks, the design of the power on reset and the demodulator has been explored in this chapter.

CHAPTER V

This chapter describes the basic blocks involved in the design and development of a high temperature Vee- squared DC-DC controller. Section 5.1 and its sub sections provide an introduction of the SOI/SOS process outlining its advantages and disadvantages. Section 5.2 describes the two differences between the fully depleted and partially depleted devices. Section 5.3 describes the use of stacked transistors to mitigate the kink effect phenomenon in the SOS/SOI design process. Section 5.4 provides an overview of the various control loop architectures for the DC – DC system followed by the description of voltage reference, comparator, hysteretic comparator and error amplifier in sections 5.5, 5.6, 5.7 and 5.8 respectively.

5.1 High temperature sub-blocks for Vee-squared controlled DC-DC converter

This chapter presents the design of the various sub-blocks used in designing a Vee squared controller for a DC-DC converter system [50]. The following sub-blocks were designed in the 0.5µm Peregrine SOS process to support high temperature operation up to 275°C:

1. Temperature independent voltage reference that provides 0.4V and 0.8V reference voltage values.

2. Error amplifier used in the Vee-squared controller.

3. Comparator

4. Hysteretic comparator that is used in the hysteretic mode operation.

The peregrine SOS process has been selected as the preferred choice of the VLSI technology for very high temperature applications for the following reasons [51]:

1. Reduced junction and side wall capacitance of the source and drain regions of the transistors enabling high speed operations for both digital and analog designs.

2. Absence of a thermally induced latch-up problem.

3. A higher I_{ON}/I_{OFF} ratio for the transistor.

The sub sections below describe each reason in detail.

5.1.1 Reduced capacitance compared to bulk device

Figure 5.1 show the cross section of a bulk device and an SOI device. In a bulk device,

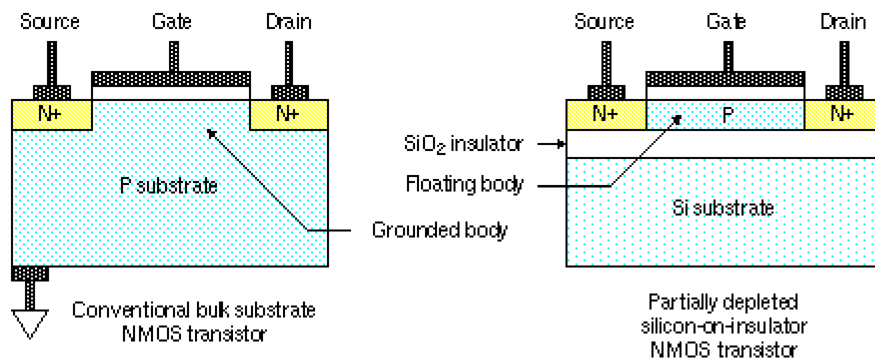


Figure 5.1 Cross section of a NMOS device in Bulk versus SOI [52]

the total capacitance from the source and drain regions of the MOSFET comprises of the reverse biased junction capacitors. This is primarily controlled by the area of the defined source and drain regions and the doping concentration of the substrate. In case of the SOI device as shown in Figure 5.1, the total capacitance from the source and drain sides is in

series with the oxide capacitance (C_{BOX}). Because of the higher thickness and lower permittivity of the (SiO2) oxide layer, the overall capacitance to the substrate is dominated by the oxide capacitance. In addition, because of the presence of the oxide layer, full dielectric isolation of N and P devices is possible. A result is reduced side wall capacitance and no well to substrate leakage paths. Thus, the overall capacitance to the substrate is smaller compared to a bulk device and results in a higher value of f_T for the same feature size compared to the bulk processes of the same length.

5.1.2 Latch-up prevention

Figure 5.2 (a) and (b) show the cross section of the bulk device with the parasitic bipolar transistors and that of an SOI device respectively.

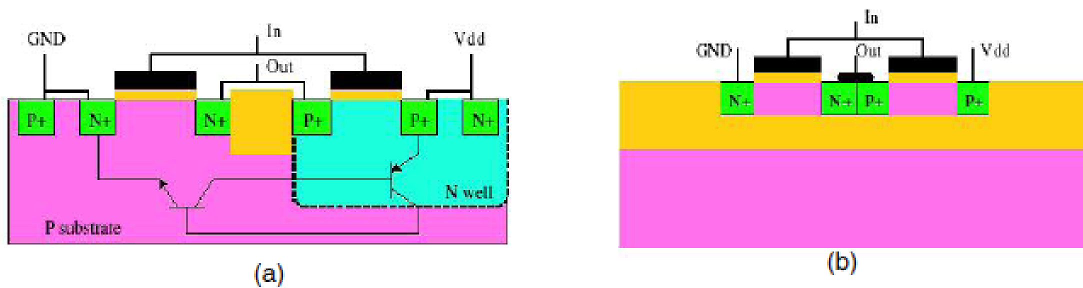


Figure 5.2 Cross section of (a) Bulk device and (b) SOI device

The presence of the NPN and PNP transistors in a positive feedback configuration resembles that of a thyristor. An unwanted disturbance like transient switching or self-heating of the device can cause carriers to be injected into the base of these bipolar transistors which can trigger the positive feedback loop. This can cause the circuit to latch up .In case of an SOI device because of the presence of the buried oxide, these parasitic bipolar transistors are nonexistent and the device is not prone to latch up.

5.1.3 Higher $^{I_{ON}}/_{I_{OFF}}$ ratio

For an SOI/SOS device, the sources of leakage are: (1) sub-threshold leakage (2) Gate induced drain leakage (3) Punch through (4) Gate oxide tunneling current. In addition a bulk device has one or more well to substrate paths. The predominant source of leakage among the above listed mechanisms is the sub-threshold leakage. The sub threshold leakage current can be approximated as:

$$I_D = I_S e^{\left\{\frac{V_{GS}-V_{th}}{\eta V_T}\right\}} \tag{5.1}$$

Where V_T = 25.8mV, I_S is the current when V_{GS} is equal to V_{TH} and

$$\eta = 1 + \frac{C_{eq}}{C_{OX}} \tag{5.2}$$

Sub threshold slope is defined as the inverse ratio of the logarithm of the drain current with respect to V_{GS} and can be defined as:

$$S = \frac{\partial V_{GS}}{\partial(\log_{10} I_D)} = 2.3\left(1 + \frac{C_{eq}}{C_{OX}}\right)\frac{KT}{q} \tag{5.3}$$

The lowest possible value of the sub threshold slope that can be obtained is 60mV for η=1. Measured devices in 0.5 µm peregrine SOS process have reported a sub threshold slope of 62 mV/dec for the NMOS and 65mv/dec for the PMOS [51]. As the temperature is increased, the threshold voltage reduces and this increases the I_{off}. Devices with a lower value of S have better leakage performance and acceptable I_{ON}/I_{OFF} ratio and are the preferred choice for high temperature operation for equal thresholds. From equation (5.1) it is evident that, as the threshold voltage reduces, the leakage current is going to increase. One reduction mechanism for threshold voltage is the DIBL effect which is predominant in short channel devices. As the channel length is reduced, the depletion region from the drain end extends into the channel and the amount of voltage required to

invert the channel is reduced thus reducing the threshold voltage. An SOS/SOI device is usually made of thin film Silicon. The total capacitance that controls the active region is much smaller because of the presence of the oxide and this in conjunction with thin film Silicon results in better control for the gate over the active region. Thus the reduction of threshold voltage because of DIBL is less in an SOS/SOI device, compared to bulk.

5.2 Fully depleted versus partially depleted device

Figure 5.3 (a) and (b) show the cross section of a fully depleted and partially depleted SOS/SOI device respectively.

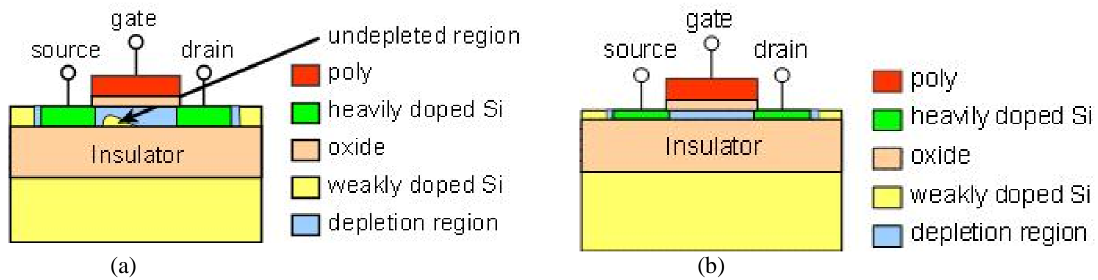


Figure 5.3 Cross section of (a) partially depleted and (b) fully depleted device[53]

While manufacturing an SOI/SOS device, the source, drain and the body regions of the MOSFET are isolated from the substrate. While the source and drain ends of the MOSFET are connected to well defined nodes in the circuit, the body is usually left unconnected. The floating body MOSFETs can be classified into two major types:

(a) Fully depleted device and (b) partially depleted device.

Fully depleted device: The cross section of a fully depleted device is shown in Figure 5.3 (b). In a fully depleted device the thickness of the depletion region is greater than the Si film used to make the device. A positive charge on the gate can cause the depletion of carriers underneath it and hence the name fully depleted device.

Partially depleted device: The cross section of a partially depleted device is shown in Figure 5.3(a). In a partially depleted device, the thickness of the depletion layer is much greater than the thickness of the Si film used to make the device. When a positive voltage is applied to the gate, all the carriers underneath it will not be depleted and an undepleted region exists under the gate as shown in Figure 5.3(a). This undepleted region has a possibility of being charged due to switching transients of the device and causes the kink effect. The equivalent circuit schematic of a partially depleted floating body device is shown in Figure 5.4. The floating body causes a parasitic NPN device to appear in

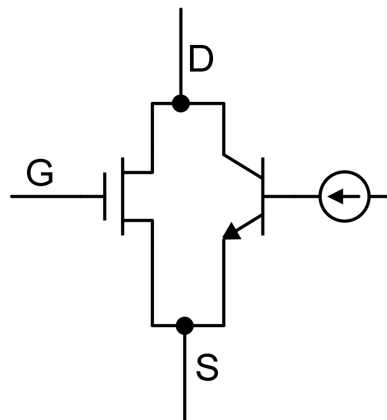


Figure 5.4 Equivalent schematic of the floating body transistor

parallel to the main transistor. An increase in the drain voltage causes the electrons near the drain to form electron –hole pairs because of impact ionization. The electrons from these new electron-hole pairs are attracted to the drain and the holes get accumulated on the undepleted region i.e. the base. For small drain –source voltages this parasitic bipolar transistor usually remains off, but as the drain to source voltage is further increased the base voltage of the bipolar transistor also raises turning the BJT device on and leading to an increase in current consumption and reduced ION/IOFF ratios or even total loss of control of the CMOS transistor. This phenomenon is reportedly observed around a V_{DS} value of 1.4-1.6V as shown in Figure 5.5.

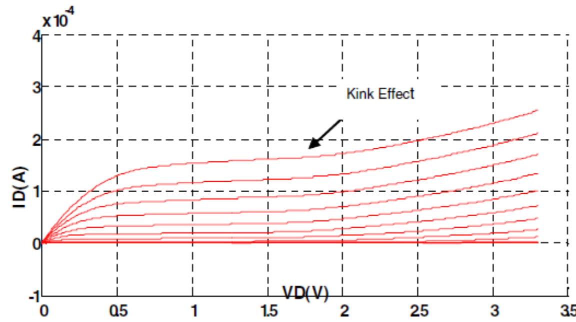


Figure 5.5 ID vs. VDS of a NMOS device showing the kink effect [51]

The kink effect can be beneficial for the digital designs as it helps lower the switch resistance for a given value of V_{DS} or harmful reducing the I_{ON}/I_{OFF} ratios. High NMOS leakage kink can destroy the functionality if NOR gates at extreme temperatures. Note NMOS kink in the measured curves if Figure 5.5 at V_{DS} equal 1.5V and $I_D \approx 0$, This kinking is unacceptable for analog designs which relies on output resistance of the device for high self-gains and high circuit gains.

5.3 Stacked transistors

Figure 5.6 shows the schematic of a composite transistor made by stacking a high threshold (RN) device in series with a low threshold (NL) device.

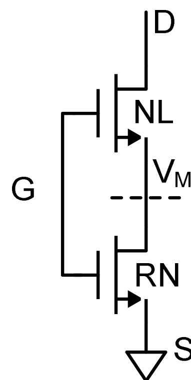


Figure 5.6 Schematic of the stacked transistor

The main motivation for using a series combination of transistors with different threshold voltages is to mitigate the kink effect. The effective output resistance of this stacked cascode can be expressed as [54]:

$$R_{cas} = gm_1 ro_1 ro_2 + ro_1 + ro_2 \tag{5.4}$$

Where gm_1,ro_1 are the trans-conductance and output resistance of the RN device and ro_2 is the output resistance of the NL device. For a given value of the V_{DS} the RN and NL devices can be sized such that the RN device remains in saturation and serves as the main transistor in the signal path with the required self-gain and f_T. The NL device is sized such that the V_{DS} value of the RN device is always lower than 1.4 V and greater than VDS_{Sat} to prevent the lower RN from experiencing the kink effect. The stacked transistor configuration also helps reduce the off state leakage in digital design. For a zero input voltage at the gate of the stacked device and a high value of V_{DS}, the intermediate node V_M as shown in Figure 5.6 stays positive. The negative value of V_{GS} causes the NL device to self –reverse bias itself and this reduces the sub-threshold leakage current. The upper NL devices are viewed as being sacrificial. Also of sum assistance a large value of V_{DS} is now split between the two transistors and the effective V_{DS} across each transistor is much lower. This also mitigates the threshold voltage lowering caused by the DIBL effect. This stacked transistor configuration will be used in the design of the sub-blocks for the Vee-squared controller.

5.4 Control loop architectures

A high temperature DC-DC buck converter has been designed for the following specifications in [50]:

Table 5.1 Specification of the DC-DC converter system

Specification	Value
Operating Temperature	0-275°C
Input voltage range	15- 20V
Output voltage range	1.5 to 1.8V
Output Watts	2 W
Regulation	2%
Efficiency	80-90 %
Stability(Phase margin)	75°

A control loop is essential in the DC-DC converter to establish the proper feedback between the scaled version of the output and the input in order to achieve the necessary accuracy at the output and the desired phase margin. The three main architectures that are used to implement the control loop architectures for the DC-DC converter are:

(1) Voltage mode control

(2) Current Mode control

(3) Vee- squared mode control

5.4.1 Voltage mode Control

The schematic of a voltage mode control of a buck converter is shown in Figure 5.7

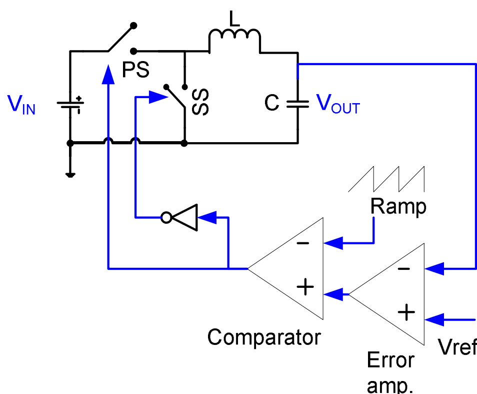


Figure 5.7 Schematic of the voltage mode control of the buck converter[50]

In the voltage mode control, the error amplifier compares the output or the scaled version of the output with a predetermined reference voltage to produce an error voltage. This

error voltage is used as the reference for the comparator which compares this with an artificially produced ramp. The ramp is usually produced by a V-I converter, and this current is integrated to produce a voltage ramp by the capacitor. The output of the comparator is a pulse width modulated waveform which is used to control the high side and low side switch in the buck converter. While the architecture for the voltage mode control is very simple and consists only of the error amplifier and the comparator as the main blocks in the feedback path additional compensation is still required to maintain stability to achieve the necessary phase margin.

5.4.2 Current mode Control

The schematic of the current mode control for a buck converter is shown in Figure 5.8

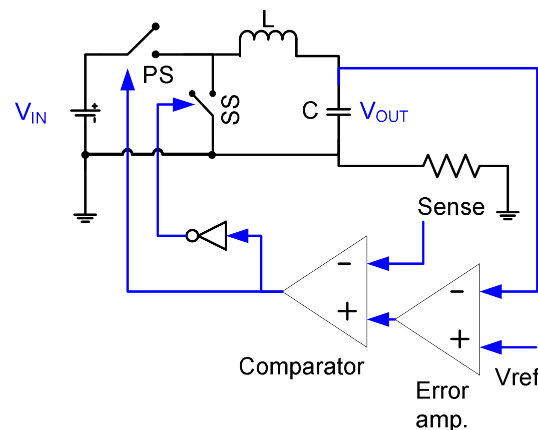


Figure 5.8 Schematic of the current mode control [50]

The error amplifier in the current mode control performs the same function as described in the voltage mode control. The reference ramp signal for the comparator in the current mode control scheme is derived from the inductor current. The current information from the inductor is converted to a voltage by using either a sense resistor or an isolation transformer [50]. The loop still needs to be compensated to achieve the necessary phase

margin. The three main compensation schemes used to achieve stability of the control loop are:

1. Type I compensation

2. Type II compensation

3. Type III compensation

A detailed description of the type I , II and III compensation schemes for the DC-DC converter is given in [50, 55].Though the type II and III compensation schemes yield robust stability , implementing them requires extra components and increase the bill of materials of the system. In addition, since the transient behavior has to propagate through the error amplifier, the bandwidth of the error amplifier has to be high. High bandwidth for the error amplifier comes at an expense of increased power consumption and is undesirable.

5.4.3 Vee –squared control

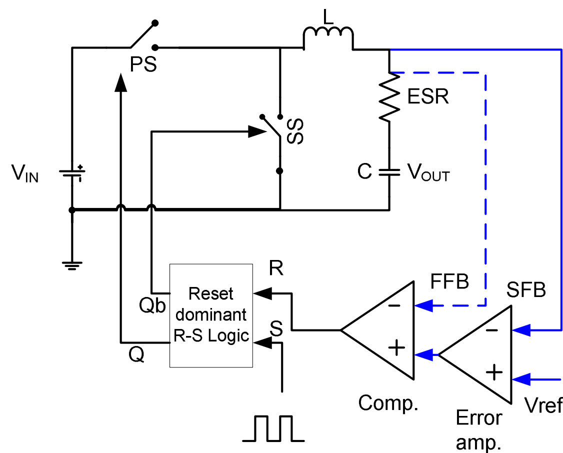


Figure 5.9 Schematic of the vee-squared control loop [50]

The schematic of a vee-squared control loop is shown in Figure 5.9. The vee- squared control mechanism consists of two loops. A slow feedback loop(SFB) where the DC information of the output or a scaled version of the output is fed to the error amplifier for establishing the error voltage. Any transient change that occurs at the load is sensed by

the ESR of the capacitor and fed directly to the comparator. The output of the comparator is given to R-S flip-flop which over rides the system clock to quickly respond to load changes. Since the error amplifier is out of the transient path, the response is only limited by the comparator delay, delay of the digital logic and the switch delay. This eases the requirement on the band width of the error amplifier and as a result it is much slower consuming less power. Compensation is still necessary to make the system stable to achieve the desired phase margin. The loop transfer function of the vee-squared controller is obtained by breaking the loop at the output node and applying a small test signal and measuring the ratio of the output to the test signal applied. The transfer function of the cascaded pair of comparator and the error amplifier can be expressed as

$$TF_1 = A_c.A_e \tag{5.5}$$

A simplified schematic of the cascaded pair of the error amplifier and comparator is shown in Figure 5.10

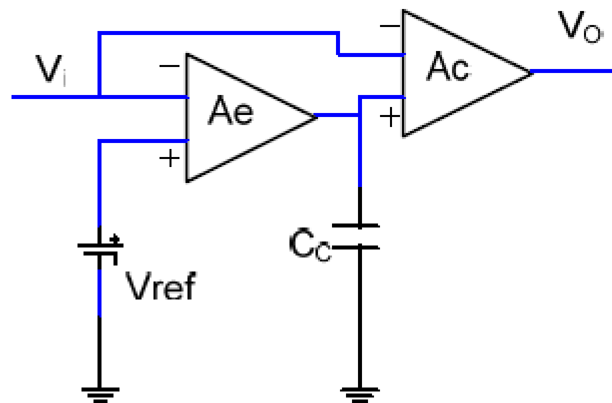


Figure 5.10 Schematic of the cascaded pair of error amplifier and comparator [50]

We can write [50]

$$TF_1 = A_c\left(-v_i - \frac{v_i.A_e}{1+\zeta s}\right) \tag{5.6}$$

Where $A_e = gm.r_o$ and $\zeta = r_o.C_c$

Rearranging the above equation we have [50]

$$TF_1=-A_c.A_e\left[\frac{\frac{s}{\omega_z}+1}{1+\frac{s}{\omega_p}}\right] \tag{5.7}$$

The pole and zero location for TF_1 are given as $\omega_p=\frac{1}{r_o.C_c}$ and $\omega_z=\frac{gm}{C_c}$ respectively. The small signal model of the switch along with the output filter is shown in Figure 5.11

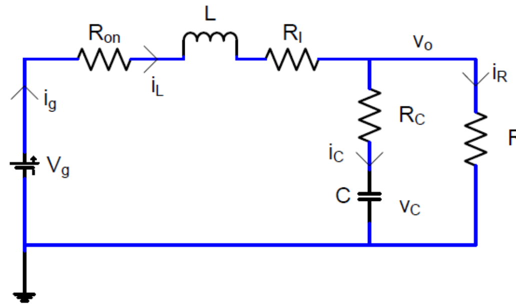


Figure 5.11 Equivalent circuit of the switch and LC filter in the on state [50]

The transfer function of the above network can be expressed as [50]:

$$TF_2=\frac{R(1+sCR_C)}{s^2LC(R+R_C)+s\big(C\big(R(R_l+R_C+R_{on})+R_C(R_l+R_{on})\big)+L\big)+(R_l+R_C+R_{on})} \tag{5.8}$$

The overall loop response is the product of the transfer functions TF_1 and TF_2 and the bode plot of the composite loop response is shown below.

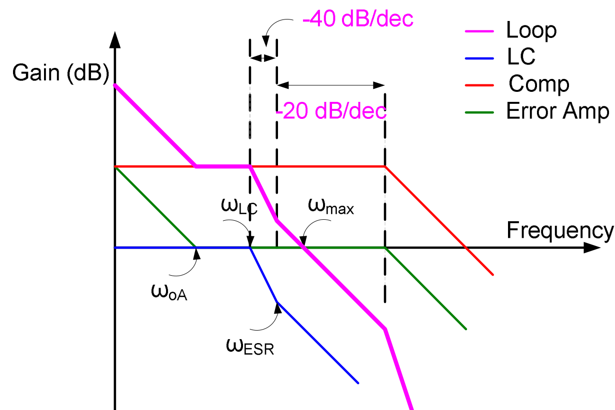


Figure 5.12 Bode plot of the loop response of the vee-squared controller

By inserting a compensation capacitor at the output of the error amplifier, a LHP zero is realized in the overall transfer function. The location of this LHP zero is chosen to be about 1/10th the frequency of the LC filter. By choosing a proper capacitor and its associated ESR value, a 20 dB/dec roll off can be obtained around the unity gain frequency with sufficient phase margin.

5.5 Voltage Reference

A temperature independent voltage reference sets the DC accuracy of the DC-DC converter in steady state. Two reference voltages of 0.4V and 0.8V were established for the vee-squared controller. 0.4V was chosen as the reference value for the following reasons:

(1) Preliminary studies were conducted on the NG diode and resistors to find the useful region of operation. The figure below shows the I-V plots of the SN resistors in the peregrine 0.5 µm process.

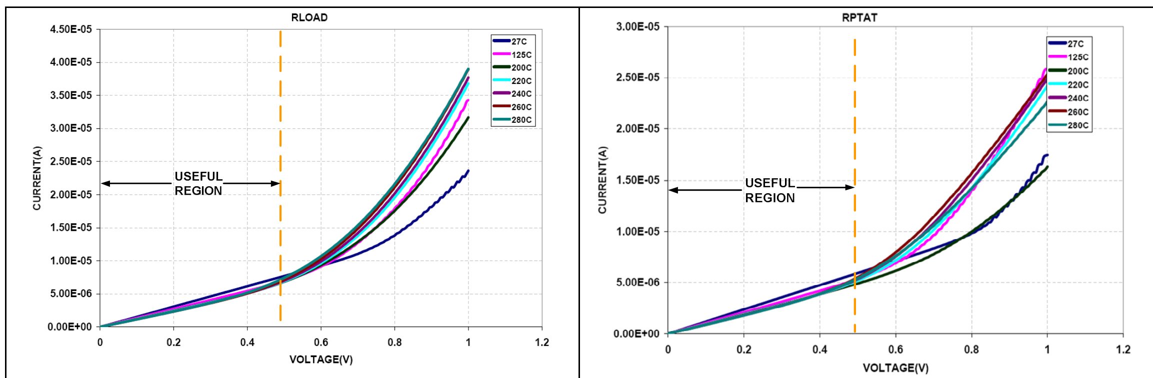


Figure 5.13 I-V plot of the SN resistor

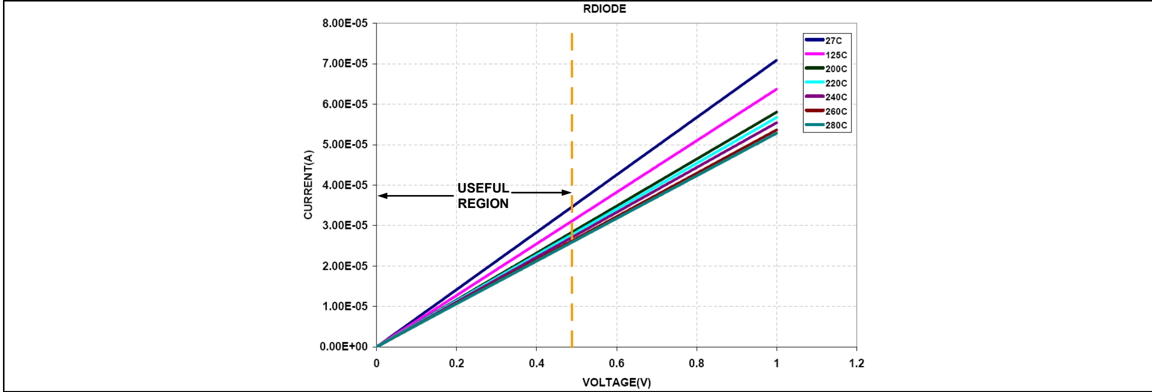


Figure 5.14 I-V plot of the PP resistor.

Figure 5.13 and Figure 5.14 indicate that linear ohmic region for the resistors are around 0.45V. Beyond this region of operation, the resistors exhibit a voltage coefficient and are hence undesirable. The temperature coefficient of the SN resistors was found to be 540ppm/ °C. The SN resistor was chosen for its lower temperature coefficient.

(2) Figure 5.15 shows the ID-VD plot for the NG diode in the peregrine process.

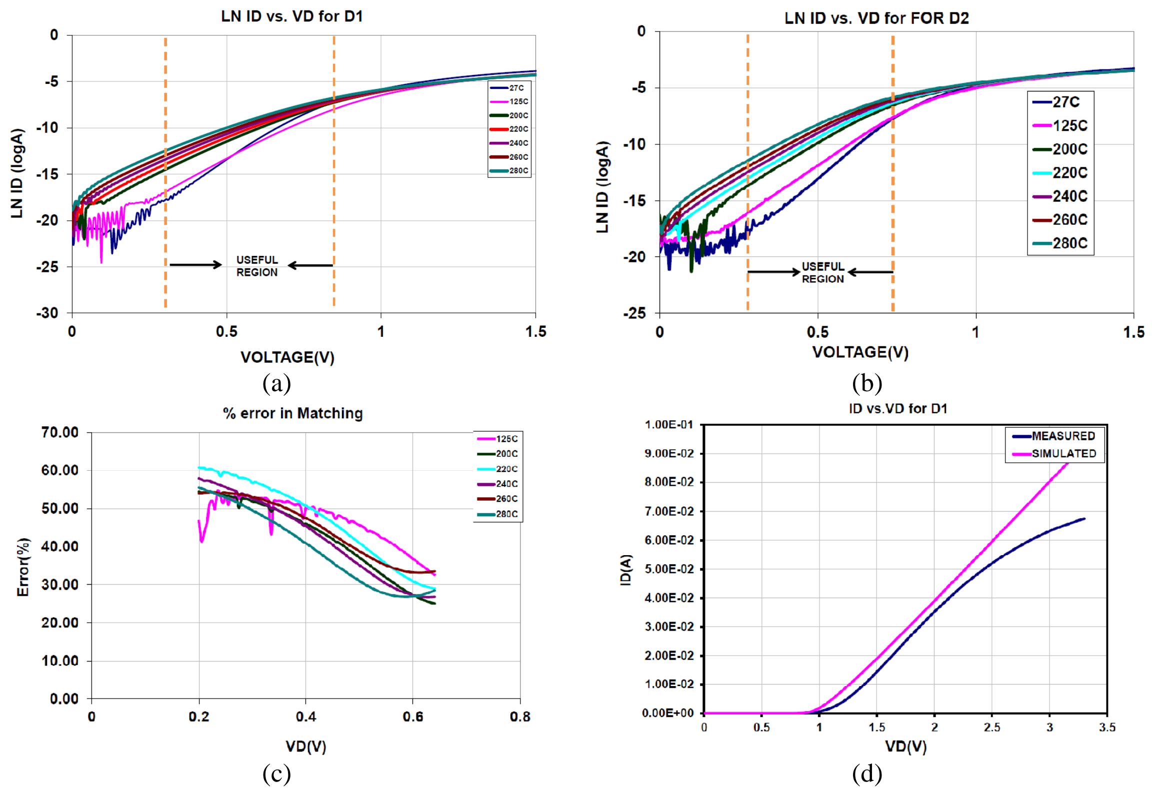
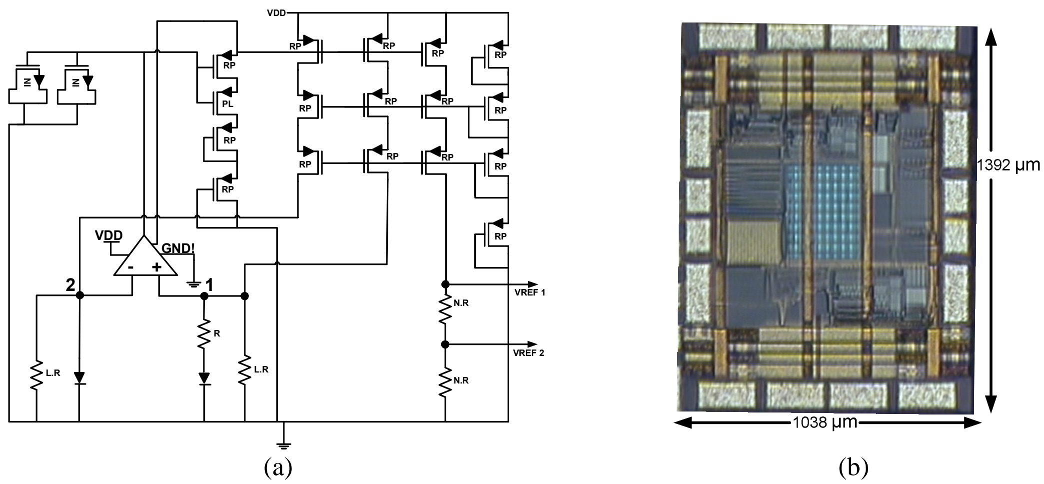
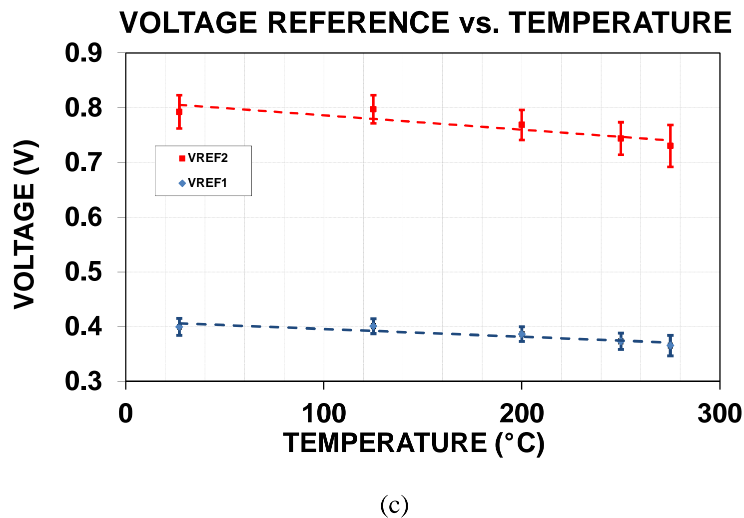


Figure 5.15 ID-VD plot for the NG diode in the peregrine process

The plot above also shows that the log linear range for the diode from 25°C to 275°C is around 0.45V.Based on this measured information, the voltage drop across the resistors and diodes was not allowed to exceed 0.4V. Figure 5.16 shows the schematic, layout and the measured results for the voltage reference. The chosen architecture and the design procedure is the same as described in the voltage reference section in chapter IV. The measured temperature coefficient of the reference voltage was found to be 143 μV/°C across the temperature range 25°C to 275°C.





(c)

Figure 5.16 (a) schematic (b) layout and (c) measured results of voltage reference

The measured results reported here are the first of its kind at such elevated temperatures.

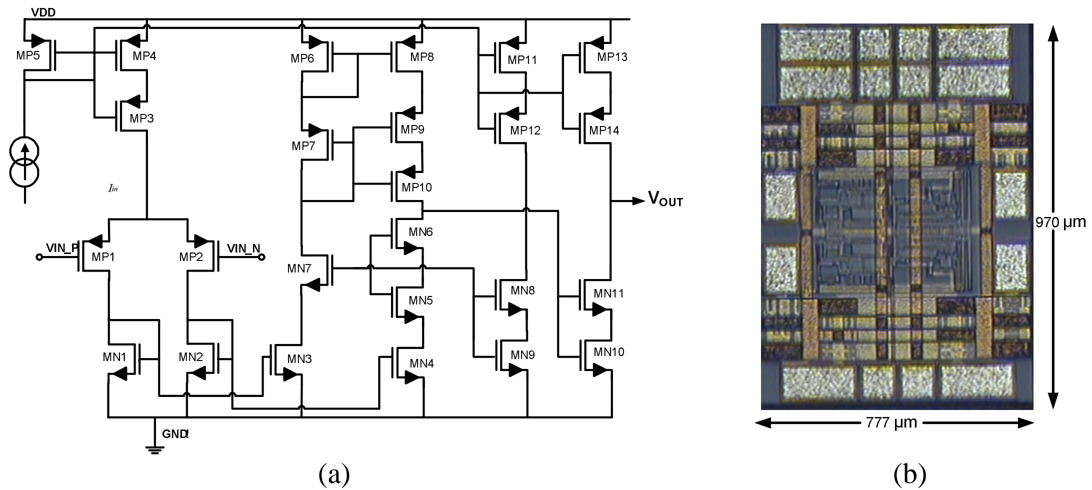
These results demonstrate better temperature coefficient for the voltage reference in comparison with the existing solutions in the market.

Table 5.2 Comparison of voltage references

Vendor	Temp-Co	Range
Cissoid [56]	350 µV/°C	-30°C - 225°C
This work	143 µV/°C	27°C - 275°C

5.6 Comparator

Comparators and hysteretic comparators are used in the controller to perform under voltage lock out and duty clamp functions etc. The schematic and layout of the core comparator is shown in Figure 5.17 (a) and (b) respectively. The circuit was designed using PMOS transistors for the input pair to support lower common mode levels. A set-reset NAND latch was implemented to provide the hysteresis function in the hysteric comparator.



(a) (b)

Figure 5.17 (a) Schematic of the comparator (b) layout of the comparator

Transistors MP1 and MP2 were sized to keep the 3σ input referred offset to less than 5mV based on the following equation:

$$V_{os} \ll \frac{3.10}{\sqrt{WL}} \tag{5.9}$$

Choosing a target V_{OS} of 1.25 mV, the total gate area obtained was 576 μm^2. A gate length of 3µm was chosen and the width was chosen to be 192 µm. This was implemented as 32 fingers of 6µm each. The comparator shown is a two stage circuit where the first stage is folded current cascode architecture and the second stage is a cascode stage. Since the output pair MP13-MP14 swings from 0 to 3.3V, the V_{DS} across these transistors is greater than 1.4V. The stacked configuration was used to prevent kink effect in these for these devices and MN10-MN11. To maintain the current mirroring accuracy, MP3-Mp4 and MP11-MP12 were also implemented as stacked pairs. The second stage consists of a simple cascode stage where the P side rail devices MP6-MP8 were diode connected. This was necessary to achieve the differential to single ended conversion without kink errors. . Note MP10 and MN6 are sacrificial devices ensuring stage 2 gain and are allowed to kink. While the P side devices were diode connected to achieve the necessary gate bias, the N side cascode devices were biased from a separate leg of current. This was necessary as it was not feasible to have 4 diode connected transistors in a 3.3V supply. Again, transistors MP10 and MN6 implemented pair stacking to mitigate the kink effect. The comparator achieves a DC gain greater than 80dB and a GBP of 2.3MHz while driving a 50pF load capacitance temperature. These values of GBP and DC gain are sufficient in implementing the Vee -squared control. Figure 5.18 shows the measured results of the open loop gain, rise/fall times, rise/fall delay and offset voltage of the comparator. The rise/fall time and rise/fall delay were measured with a 50pF load capacitance and 50mV overdrive voltage.

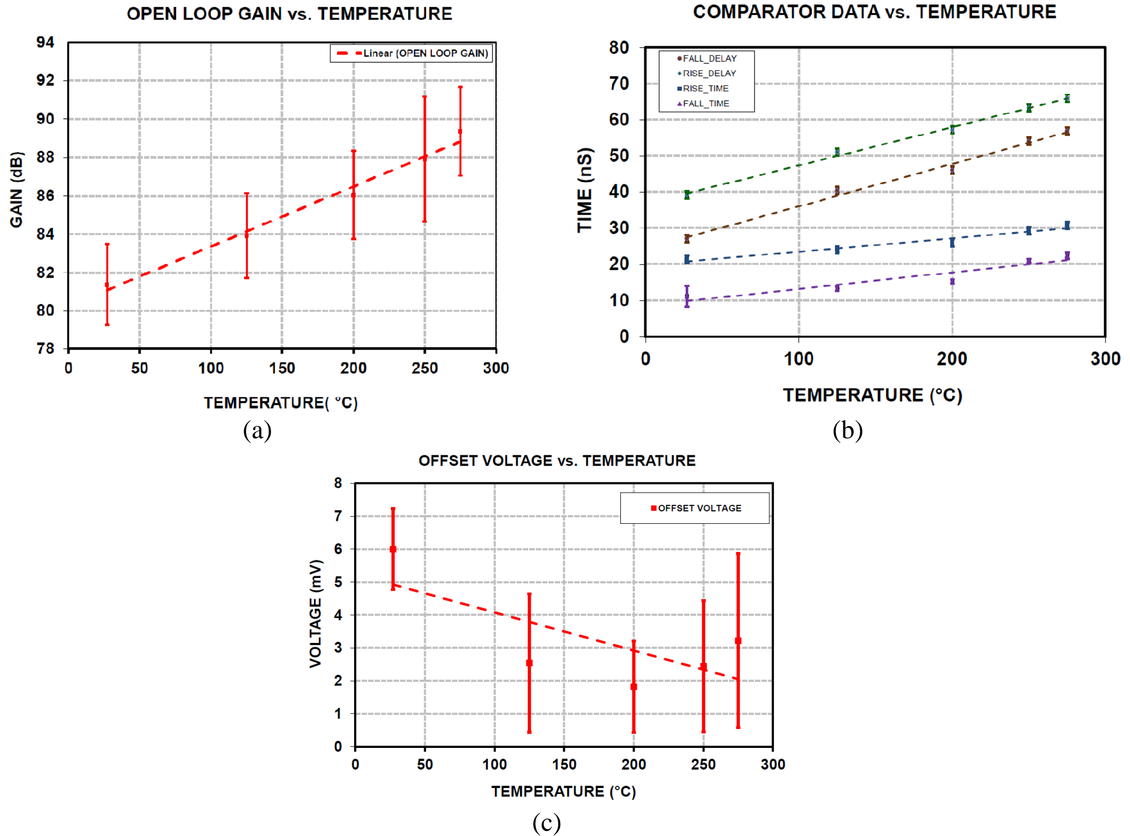


Figure 5.18 (a), (b) and (c) Measured results of the comparator

5.7 Hysteretic comparator

The hysteretic comparator is used to implement the under voltage lock out scheme in the Vee –squared controller. It can also be used as a control mechanism under light load conditions. The popular ways of implementing the hysteresis function are:

(1) Employing positive feedback around the comparator

(2) Use of two separate comparators and an RS latch.

While method (1) may be popular among the discrete circuits, realizing the positive feedback using resistors and the required high and the resulting reduction in switching performance makes it an impractical option. Additionally the resistors consume large area. The second method was selected for implement the hysteresis function as hystertic

comparator delay is limited by the delay of either analog comparator. The block diagram shown in Figure 5.19 and the measured results are shown in Figure 5.20.

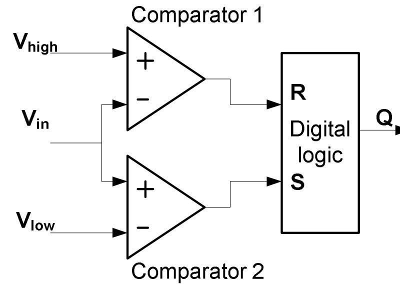


Figure 5.19 Block diagram of the hysteretic comparator

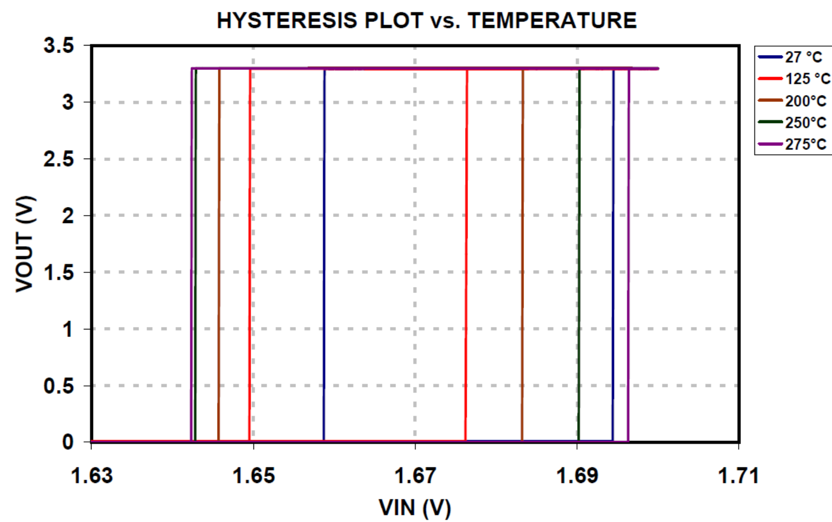


Figure 5.20 Hysteresis plot versus temperature

5.8 Error Amplifier

The error amplifier is a critical building block of the DC-DC controller. It compares the scaled output voltage with a reference voltage to produce an output which will be used by the comparator for stabilizing the control loop. The schematic of the proposed error amplifier is shown in Figure 5.21.

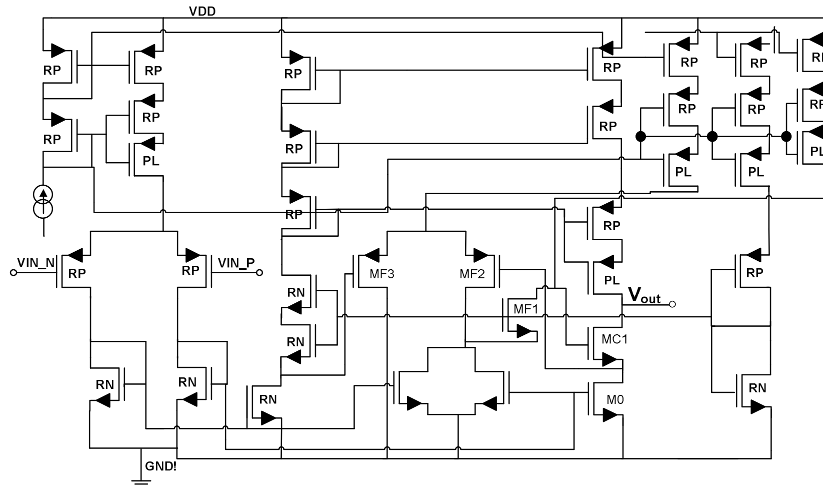


Figure 5.21 Schematic of the error amplifier

Since the generated reference voltage is around 400mV, PMOS transistors have been chosen to implement the input differential pair. Based on the stability requirements of the control loop, the error amp has been designed for a GBP of 300Hz, an open loop gain greater than 60dB, and a slew rate of 300mV/µS. The size of the compensation capacitor planned for use in the control loop is 15nF. From the requirements of the GBP at a selected device an overdrive voltage of 200mV, the size of the input pair devices was found to be W/L = 4 @ 6µ/12µ. Again a folded current architecture along with additional cascoding and device stacking were employed similar to that described in the comparator. Operating on lower common mode voltages around 200mV (in the absence of MF1-MF5) can force transistor M0 in the triode region. This can severely affect the output impedance and gain of the OTA. A feedback boost amp consisting of transistors MF1-MF5 compensates for the anticipated loss of gain when the output swing forces MC1 into the triode or linear region. The dimensions of the gain boosting amplifier (MF1-MF5) are chosen similar to the input pair and current folding devices of the error amplifier ensuring matched behavior. The layout and the measured results of the error amplifier are shown in Figure 5.22 and Figure 5.23 respectively.

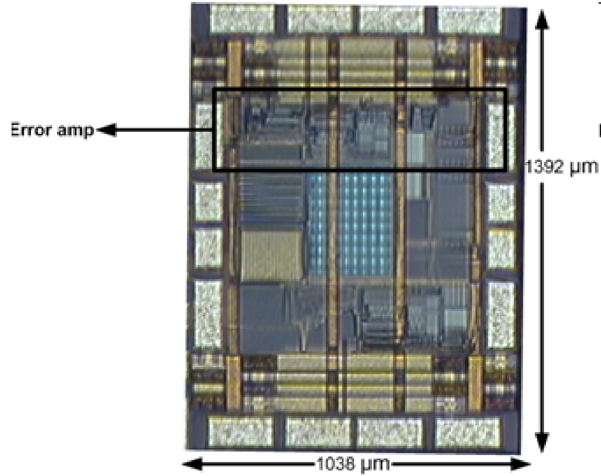


Figure 5.22 Layout of the error amplifier in the VREF pad frame

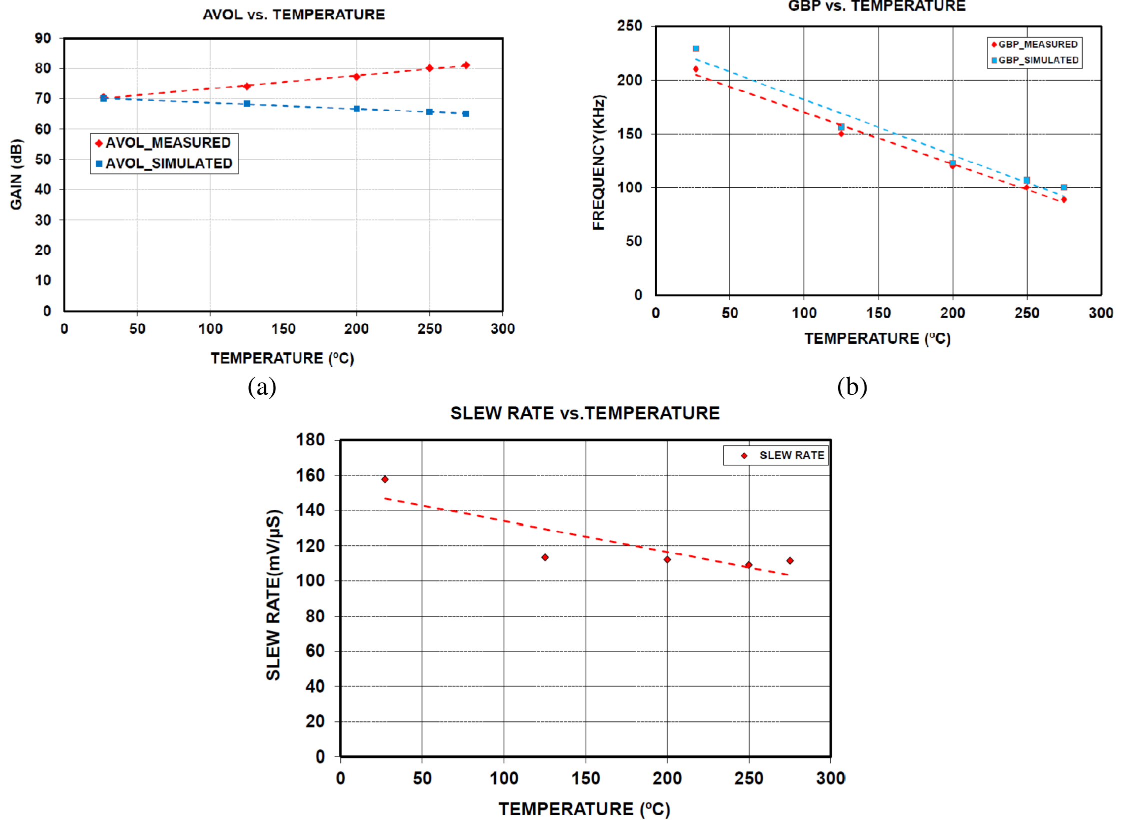


Figure 5.23 Measured parameters of the error amplifier

The measured open loop gain tends to be slightly higher than the simulated values. This is because the design is based on a constant overdrive voltage method. Also, the stacked devices used in the error amplifier kink less with an increase in temperature. This

increases the overall gain of the error amplifier. The peregrine models do not reflect the kink behavior at such high temperatures. The GBP of the error amplifier matches well the simulated values. This is because the mobility of the devices reduces with an increase in temperature.

Summary

In this chapter the peregrine SOS/SOI process was introduced outlining its advantages and disadvantages over the bulk process. The differences between the fully depleted and partially depleted devices have been introduced and the root cause of the kink effect in partially depleted devices has been traced. The stack transistor structure has been used as single composite device in analog circuits to mitigate the kink effect and achieve the desired performance. The design and development of various blocks for a DC-DC buck converter capable of operating up to 275°C is presented. The control circuitry design is based on the Vee-square control mechanism. A temperature independent voltage reference providing a high impedance output of 0.4V and 0.8V has been designed using the NG diodes and SN resistors. The measured temp-co was found to be 143 µV/°C. A comparator and hysteretic comparator have also been designed to be operational at 275°C. The comparators have a common mode range from 0.3V to 2.2 V with a propagation delay of less than 100 nS for a 50 mV overdrive voltage. The measured rise/fall time for a 50pF load capacitance is less than 20 nS. An error amplifier used in the main feedback loop has also been designed and tested. The error amplifier has a GBP of 300Hz with a 15 nF capacitor and an open loop gain greater than 55 dB.

CHAPTER VI

This chapter describes the test and measurement results of the power harvesting front end. Two pad frames have been designed and fabricated in the IBM 180nm RF-process. The pad frames consist of the following circuits:

(1) Padframe-1: A RF-DC converter with the matching network and a programmable bias current source.

(2) Padframe-2: A full circuit comprising a matching network, RF-DC converter, LDOs and demodulator.

Section 6.1 describes the test procedure for Padframe-1 which includes variation of V_{DD} with respect to load current and input power. Section 6.2 describes the test procedure for padframe-2 and measures the voltage reference and regulated voltages of the two LDOs versus input power followed by the testing of the demodulator. Section 6.3 concludes the chapter along with future work mentioned in section 6.4.

6.1 Test procedure for pad frame-1

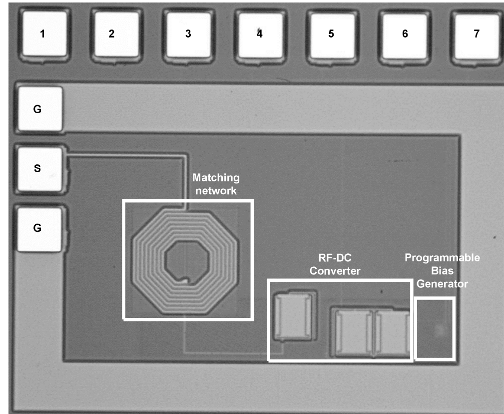


Figure 6.1 Chip micrograph of the Padframe-1

Figure 6.1 shows the chip micrograph of Padframe-1 and Table 6.1 contains the pad information.

Table 6.1 Description of the pad frame -1

Pad name/ No.	Type	Label	Description
GSG	Input	GSG	Input to circuit connecting the network analyzer
1	NC	-	No connection
2	NC	-	No connection
3	Output	VDD	DC Voltage of the RF-DC converter
4	NC	-	No Connection
5	Input	V_S	Connection to the bias resistor
6	Input	V_R	Connection to the bias resistor
7	Ground	G_{nd}	0V ground connection

The following tests were performed on pad-frame 1:

TEST 1: To study the relationship of the rectified DC voltage versus load current of the matched RF-DC converter.

Test equipment used: HP 8720D network analyzer and HP 4155A function generator.

Test Procedure: The input power was supplied to the circuit by the connecting the GSG input pad to the 8720D network analyzer and was held constant at -3 dBm(500μW). The entire current consumed by the RFID sensor system was mimicked by a programmable current source. The current in the programmable current source was varied from 0μA to 54 μA in steps of 10μA and the DC voltage was recorded using the HP 4155A. A total of 10 dies were measured and the Figure 6.2 below shows the plot of the results obtained.

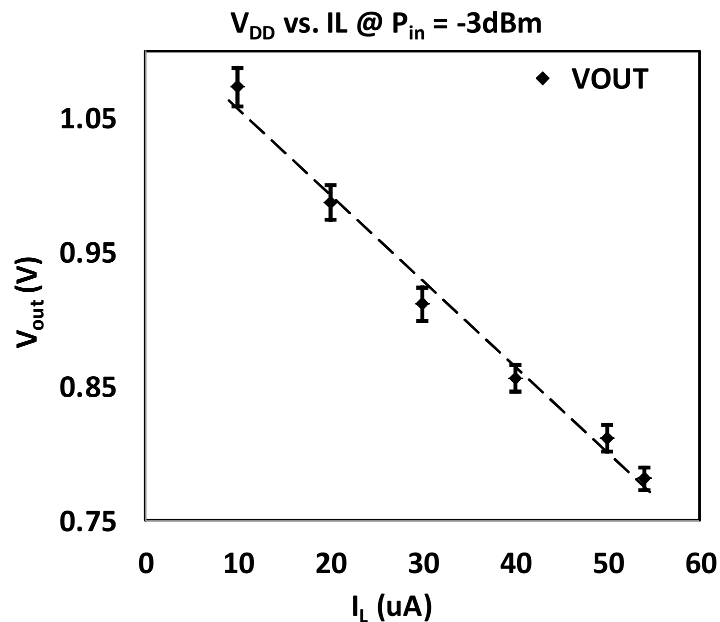


Figure 6.2 Unregulated voltage versus load current at constant input power

For a peak load current of 54μA, the unregulated voltage developed is 780mV. This value of V_{DD} is just sufficient to power the voltage reference and the LDOs. The average 1σ value obtained from the measurement at any load current is 0.008447 V.

TEST 2: To study the relationship of the rectified DC voltage versus input power at a constant load current.

Test equipment used: HP 8720D network analyzer and HP 4155A function generator.

Test Procedure: The input power was supplied to the circuit by the connecting the GSG input pad to the 8720D network analyzer and was swept from -4 dBm (400 μW) to 0 dBm(1mW) in steps of 1 dBm. The load current was held at constant values of 54 μA(full load) and 27 μA(50 % load) using the HP 4155A.

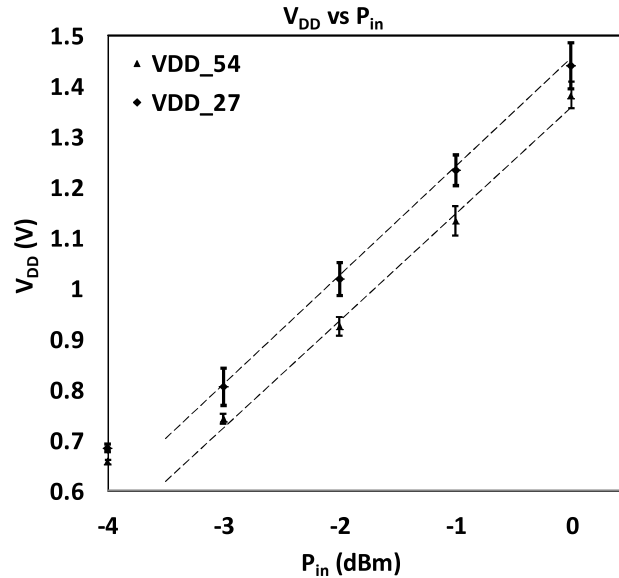


Figure 6.3 Unregulated voltage versus input power at constant load current

Figure 6.3 shows the plot of the unregulated voltage versus input power at constant load currents of 54μA and 27μA. The difference between the two V_{DD}s in at any given power level is about 125mV and is consistent with Figure 6.2. The RF-DC converter has a measured start-up time of 1μS and the ripple on the unregulated V_{DD} is 4mV at an input power of -3 dBm (500μW) and a load current of 54μA.

6.2 Test procedure for the pad frame-2

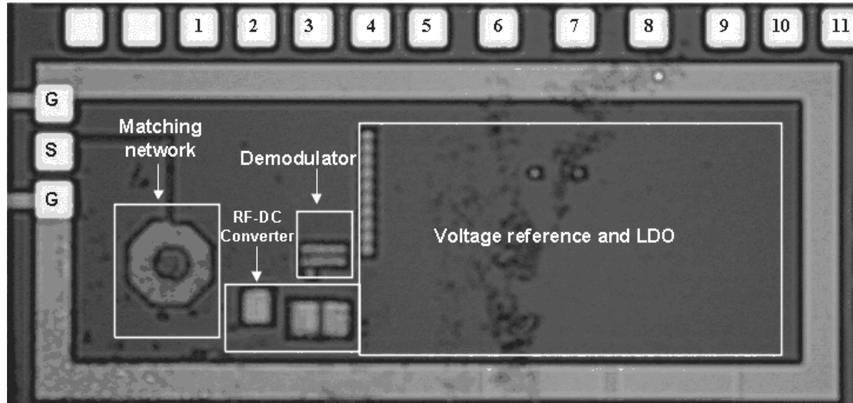


Figure 6.4 Chip micrograph of the Padframe-2

Figure 6.4 shows the chip micrograph of Padframe-2 and Table 6.2 contains the pad information.

Table 6.2 Description of the pad frame- 2

Pad name/ No.	Type	Label	Description
GSG	Input	GSG	Input to circuit connecting the network analyzer
1	Input/output	V_{DDA}	Output of the RF-DC converter
2	Output	V_{OUT_REG}	Regulated output of LDO1
3	Output	V_{DD_FSM}	Regulated output of LDO1
4	Input	V_{DD_1P2}	1.2V supply for the pad driver
5	Input	V_{DD_0P7}	0.7V supply for the pad driver
6	Output	D_{EMOD_OUT}	Demodulator output
7	Output	P_{OR}	Power on reset signal
8	Output	V_{REF_535}	535 mV reference voltage
9	Output	V_{REF_400}	400mV reference voltage
10	Output	V_{REF_135}	135mV reference voltage
11	Input	D_{EMOD_IN}	Demodulator input

TEST 1: To study the relationship of the voltage reference versus input power.

Test equipment used: HP 8720D network analyzer and HP 4155A function generator.

Test Procedure: The input power was supplied to the circuit by the connecting the GSG input pad to the 8720D network analyzer and was swept from -4 dBm (400 µW) to 0 dBm(1mW) in steps of 1 dBm. The load current was held at constant values of 54 µA(

full load) and 27 μA(50 % load) using the HP 4155A. The reference voltage was measured from pad 9 using the 4155A.

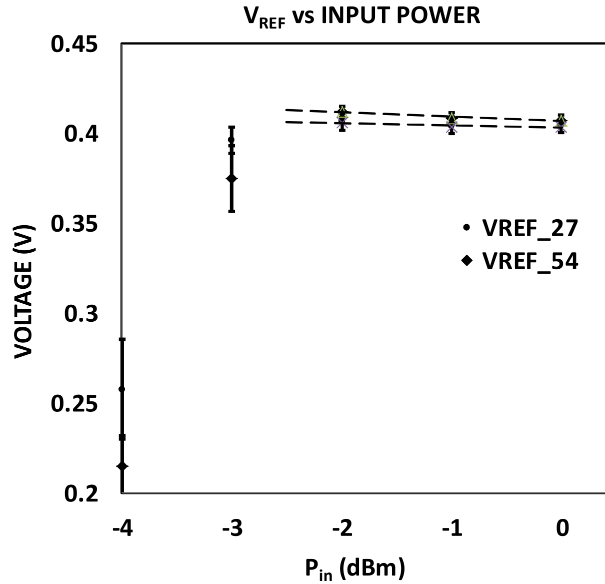


Figure 6.5 Reference voltage versus input power

At -4dBm of input power, there is insufficient V_{DD} developed to power the voltage reference or LDOs etc. In the power range from -3dBm to -1dBm regulation is maintained and the voltage reference accuracy is 5.7bits and 6.34 bits at -3dBm and 0dBm respectively. This happens for the following reasons: in Figure 4.1 the node"VB_2" is biased from a current source whose current is overly dependent on V_{DD}. As V_{DD} rises, bias current also increases and causes a change in the early voltage of transistors MP_7, MP_{13}, MP_{15}, MP_{17} and MP_{19}.This results in a power supply rejection ratio (PSSR) error in the value of V_{REF}. The measured results have a 1 σ value of 0.00276 V.

TEST 2: To study the relationship of the regulated voltage of the LDOs versus input power.

Test equipment used: HP 8720D network analyzer, HP 4155AA function generator, voltmeter and resistors to set the load current.

Test Procedure: The input power was supplied to the circuit by the connecting the GSG input pad to the 8720D network analyzer and was swept from -4 dBm (400 µW) to 0 dBm(1mW) in steps of 1 dBm. HP 4155A was used to complete the ground connection to the circuit and the regulated voltage of the two LDOs was measured using the voltmeter at pads 2 and 3.

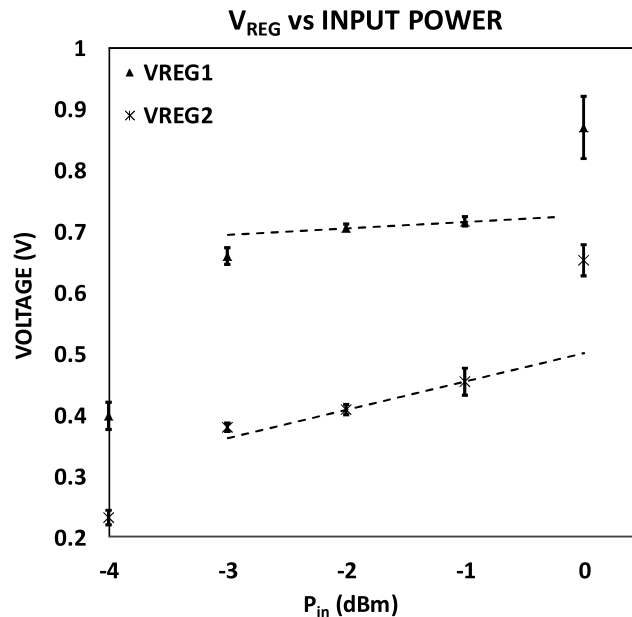


Figure 6.6 Regulated voltage versus input power

Figure 6.6 suggests that the rate of increase of V_{DD}, V_{REG1} and V_{REG2} beyond -1dBm is around 150mV/dBm. At this rate, the projected maximum V_{DD} of 1.8V would be reached at +3dBm input power. Any increase in input power beyond this point would damage the nominal devices used in this process. In order to prevent this from happening, an over voltage protection circuit i.e. shunt regulator must be added to limit the maximum V_{DD} to

safe limits. This feature need not come at a significant increase in LDO or RF to DC power.

TEST 3: To study the relationship of the regulated voltage of the LDOs versus V_{DD}.

Test equipment used: HP 4155A function generator, voltmeter and resistors to set the load current.

Test Procedure: The RF-DC converter was disconnected from the rest of the circuit and the two LDOs were powered directly from pad -1.V_{DD} was varied from 0 V to 1.5 V in steps of 0.1V and the measurements for V_{REG1} and V_{REG2} have been made at pad-2 and pad-3.

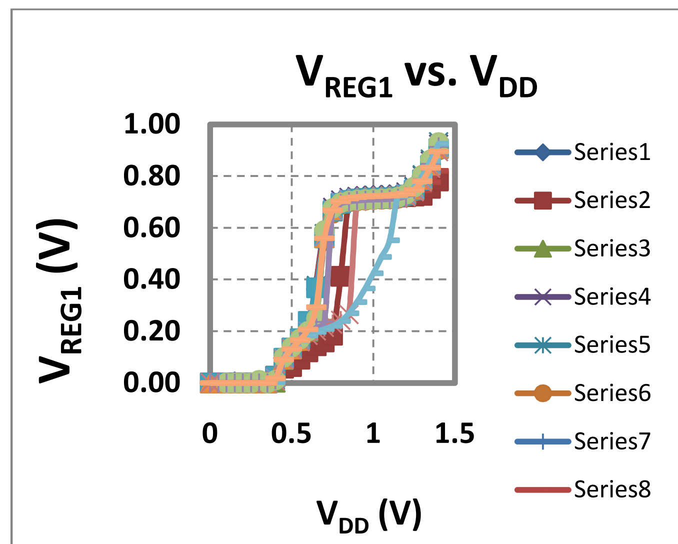


Figure 6.7 Regulated voltage of LD0-1 versus V_{DD}

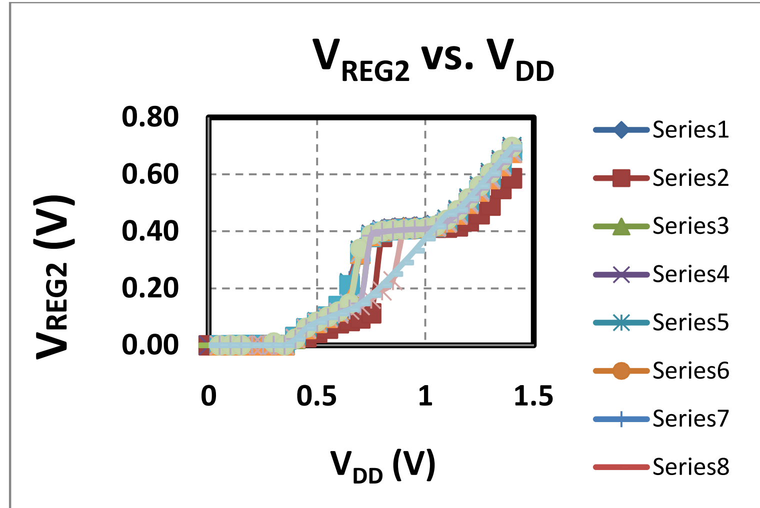


Figure 6.8 Regulated voltage of LD0-2 versus V_{DD}

Figure 6.7 and Figure 6.8 indicate that below 0.75V, there is not sufficient V_{DD} developed to establish a reference voltage of 0.4 V and hence the two LDOs are out of the regulation range. The required voltages of 0.7V for LDO1 and 0.4V for LD02 are established around a V_{DD} of 0.75V. Regulation is maintained in the VDD range from 0.75V to 1.2 V. Results from Figure 6.7 and Figure 6.8 is consistent with the results of Figure 6.2 and Figure 6.3. A V_{DD} value of 0.75 V is developed while supporting a 54μA load current at -3dBm input power level.

Table 6.3 Power consumed by individual blocks

Block name	Symbol	Supply Voltage (V)	Quiescent current(μA)	Power Consumed(μW)
RF-DC converter	P_{RFDC}	Input power		-3 dBm(500 μW)
Voltage reference	P_{VREF}	0.9	8	7.2
LDO1	P_{LDO1}	0.9	7.5	6.75
Feedback ladder	P_{FB}	0.7	8	5.6
LDO2	P_{LDO2}	0.9	3.6	3.24
Demodulator	P_{DEMOD}	0.7	1	0.7

Table 6.3 shows the power consumed by the individual circuit blocks of the power harvesting front end. The total current consumed by the individual blocks is 28.1μA while the power consumption is 23.49μW. The system has been designed for a total load current of 54μA, indicating that 26μA is available for the signal conditioning circuitry blocks. Out of the 26μA available for the signal conditioning circuitry, the memory consumes 5μA current from a 0.4V regulated supply and the ADC , band pass amplifier together have 21μA available from the 0.7V regulated supply. Harvesting efficiency can be defined as the ratio of the total harvested power to the total available input power. At -3dBm (500μW) of input power, the unregulated DC voltage developed is around 0.78V and the circuit can handle 54μA load current making the total harvested power 42.1μW.

$$\eta_{\text{harvested}} = \frac{P_{\text{HARVESTED}}}{P_{\text{IN}}} = \frac{42.1}{500} = 8.42\% \tag{6.1}$$

The total power consumed by all the blocks can be expressed as:

$$P_{TOTAL} = P_{RFDC} + P_{VREF} + P_{LDO1} + P_{LDO2} + P_{FB} + P_{DEMOD} + P_{SIGNAL} \tag{6.2}$$

Equation (6.2) can be re-arranged as:

$$P_{TOTAL} = P_{LOSS} + P_{OVERHEAD} + P_{SIGNAL}' \tag{6.3}$$

where

$$P_{LOSS} = P_{RFDC} \tag{6.4}$$

and

$$P_{OVERHEAD} = P_{LDO1} + P_{LDO2} + P_{FB} \tag{6.5}$$

Where P_{LOSS} represents the $I_D V_D$ loss in the RF-DC converter and $P_{OVERHEAD}$ is the combined loss in the two LDOs and the feedback ladder. P_{SIGNAL}' can be expressed as:

$$P_{SIGNAL}' = P_{VREF} + P_{ANALOG} + P_{MEMORY} \tag{6.6}$$

Where P_{VREF} is the power consumed by the voltage reference, P_{ANALOG} is the power

consumed by the analog circuits and P_{MEMORY} is the power consumed by the memory. Since the LDOs and the signal conditioning circuit consume power from the same node i.e. the unregulated V_{DD} obtained from the RF-DC converter, we define the useful power conversion efficiency i.e. "LDO efficiency" as the ratio of P_{SIGNAL}' to $P_{HARVEST}$ and can be written as:

$$\eta_{LDO} = \frac{I_{LDO}}{I_{LDO}+I_{SIGNAL}} \qquad (6.7)$$

Substituting the values of P_{SIGNAL}' and $P_{HARVEST}$ in equation (6.7) , we find that the LDO conversion efficiency to be:

$$\eta_{LDO} = \frac{18.3}{18.3+26} = 40.92\% \qquad (6.8)$$

P_{TOTAL} must be kept the under target 100µW limit in order to avoid tissue heating. To maximize the useful power available for the signal conditioning circuitry, i.e. P_{SIGNAL}', losses in the RF-DC converter P_{RFDC} and $P_{OVERHEAD}$ must be minimized. For an "N" stage RF-DC converter, the total losses can be expressed as NI_DV_D. The losses can be minimized by having a single stage RF-DC converter and a low V_D for the schottky diode. Having a low V_D also maximizes the final out put voltage as mentioned in chapter II. The CMRF180nm IBM process only supported n type schottky diodes when this work was initiated but have since added more efficient p type schottky The P-type schottky diode that has a lower V_D of 0.12V in comparison with a n-type schottky diode but more important a lower VD for the same f_T. The second generation design of this work will feature the design of the RF-DC converter with the P-type schottky diodes.

$P_{OVERHEAD}$ represents the power consumed by the two LDOs and the feedback ladder. The present value of $P_{OVERHEAD}$ is 15.6µW. By reducing the quiescent current consumption in

the LDO1, by a factor of 2 and replacing the feedback ladder with either MOS connected diodes or un-doped poly resistors, this value can be reduced to 8µW.

Table 6.4 Comparison of the power harvesting works

Author	Frequency (MHz)	Process	Matching type	Switch type	No. of stages	Output voltage(V)	Load current range(µA)	Efficiency (%)
Curty	915	0.5µm SOI	Series	MOS diode	3	0-5	1	0-10
Sarpeshkar	950	0.18µm Bulk	Shunt	MOS	2	0-5	4	16-23
Barnett	900	0.18µm Bulk	Shunt	Schottky diode	16	0-3	1-8	4-8
Shameli	920	0.18um Bulk	Series	MOS diode	4	0-1	2	5-10
This work	2450	0.18 bulk	Series	Schottky diode	1	0.65-1.3	10-54	7.5-10

Table 6.4 represents the comparison of this work with other works found in the literature. The work done by authors Curty, Barnett and Shameli is intended for commercial RFID applications only. The load current in these works comprises only of digital circuitry like the memory and is less than 10 µA. T**his work is the first of its kind in implementing a power harvesting front end with a series matching network and single stage RF-DC converter. More significant in this work is a complete power system for a smart RFID and including harvesting, regulation, and dual analog/digital regulators. The load current range supported is from 10µA to 54µA. The overall efficiency obtained in this work is comparable with the other works as shown in Table 6.4 with the exception of Sarpeshkar which is switch transistor with using complex body biasing.**

TEST 4: To study the working of the demodulator circuitry.

Test equipment used: Tektronix 1180B digital sampling scope, Rhode and Schwartz AM function generator, Agilent 33250A function generator, HP 4155A and Agilent infinium scope.

Test Procedure: A double sideband amplitude modulation signal that contains both the carrier and data was created to the test the demodulator. The data signal was created using the Agilent 33250A function generator and modulated using the Rhode and Schwartz function generator to create the DSB-AM wave. The DSB-AM wave was connected to the input of the demodulator using the GSG input. HP4155A was used to power to the demodulator at pad-2 and the pad drivers at pads 4 and 5 respectively. The output of the demodulator was measured from pad-6 using the Agilent infinium oscilloscope. A picture of the DSB - AM wave is shown in Figure 6.9.

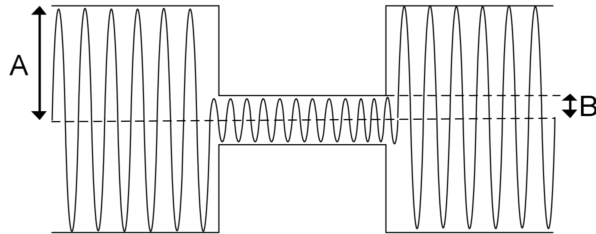


Figure 6.9 Double side band AM wave

The Gen-2 RFID standard defines the modulation index as follows[57]

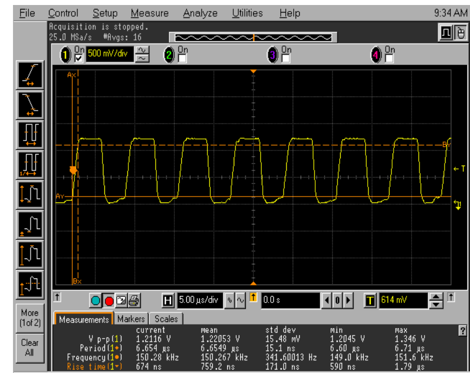
$$m= \left(\frac{A-B}{A}\right) = \left(1-\frac{B}{A}\right) \tag{6.9}$$

Typical values of "m" for the Gen -2 RFID standard range from 80% to 100%. To test the demodulator, we choose a conservative value of $\frac{B}{A}$ = 0.3, setting m = 70% in the Gen-2 Standard. Figure 6.10(a) - Figure 6.10(d) represent the output of the demodulator for various combinations of the signal and carrier frequencies as mentioned in Table 6.5.

Table 6.5 Demodulator input settings

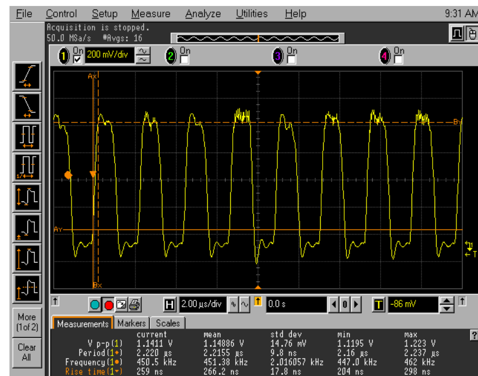
Figure number	Signal frequency(KHz)	Carrier Frequency(MHz)	Modulation index (%)
Figure 6.10 (a)	100	600	70
Figure 6.10 (b)	100	900	70
Figure 6.10 (c)	450	600	70
Figure 6.10 (d)	450	900	70

(a)



(b)

(c)



(d)

Figure 6.10 Demodulator outputs

The signal frequencies chosen for the test were 100 KHz and 450 KHz due to limitation of the test equipment Rhode and Schwartz to modulate signals only up-to 500 KHz. The carrier frequency was chosen to be 600MHz and 900 MHz based on the discussion in chapter IV where 600MHz is a conservative number and 900 is Gen-2 Standard.

6.3 Concluding Remarks

A power harvesting front end complete with LDOs, voltage reference, and demodulator suitable for operating at 2.45GHz for neural/biosensor applications capable of harvesting greater than 40μW at – 3dBm of RF signal levels was presented. Regulated supplies of 700mV and 400mV supporting 54uA of total load current heavily weighted for analog signal conditioning, a Gen2 compatible demodulator and 400mV voltage reference have been demonstrated. Measured results are within the process skew parameters of ± 10% with exception of the voltage reference PSRR. Maximum measured regulated output voltage range for the LDOs is from -3dBm to -1dBm and with efficiencies greater 8.5%. Harvesting efficiency compares favorably to previous works in Table 6.4. The harvester system presented here is a full functioning regulated power system were an order of magnitude of greater power suitable for powering for signal acquisition and data transmission.

The following papers have been submitted and published during the course of this work:

Journal paper:

(1) S.Venkatarman , C.Hutchens , R.Renakker II, Tamer Ibrahim and Rehan Ahmed, *" A 2.45GHz Power Harvesting Front End for Neural applications"* draft in preparation to be submitted to the IEEE Transactions in circuits and systems –I

Conference Publications:

(1) C.Hutchens, R.Renakker II , S.Venkatarman , Rehan Ahmed, R.Liao and S.Ibrahim : *"Implantable Radio Frequency Identification Sensors: Wireless Power and Communication,"* 33rd Annual International Conference of the IEEE Engineering in Medical and Biological Society , Boston ,MA , 2011.(Accepted)

(2) S.Venkatarman and C.Hutchens , *" RF-Front end for wireless powered neural applications"*, 51st Midwest Symposium on Circuits and Systems,Knoxville,TN,2008.(Accepted)

6.4 Future Work

In this work we have demonstrated a power harvesting front end capable of harvesting up to -3dBm (500µW) of power and delivering a 0.7V and 0.4V regulated supply voltages while supporting a 54µA load current. In order harvest even lower power levels up to -6 dBm (250 µW) inside the human body the following changes are proposed for the second generation front - end design:

(1) Matching network: One of the main reasons for choosing 2.45 GHz frequency of operation is the feasibility of small size passive elements and antenna for the matching network. As mentioned in chapter II, equation 2.6, the Q of the matching network is given as $Q_{NW}=\sqrt{\frac{R_{in}}{R_S}-1}$. This equation assumes that Q_{ind} of the series inductor has a value greater than Q_{NW}. In the 180nm IBM process, Q values of the inductor required to match the RF-DC converter are in the range from 3-5. A high Q inductor is desirable as it helps boost the voltage at the input of the RF-DC converter without any power loss. The series inductor can be absorbed in the antenna design which will be made on a biocompatible flexible PCB. Inductors made on the PCB have much higher Qs compared to on chip inductors and the overall frequency of operation can be brought down from 2.45GHz to 900MHz. Another solution is to use DM metal option for the inductors in the IBM process. Inductors manufactured with DM metal option have slightly higher Qs compared to the LM metal option in the standard design kit. This option however comes at an

increased cost of wafer production.

(2) RF-DC converter: The output of the RF-DC converter as mentioned in chapter II is given as $V_{OUT} = 2N (V_P - V_D)$. The output voltage can be maximized by the following ways: (1) increasing the number of stages (2) maximizing V_P and (3) minimizing V_D. V_P can be maximized by increasing the Q of the matching network and V_D can be minimized further by choosing a different switch in the RF-DC converter. During the implementation of the first generation design of the power harvesting front end, the choice of switches was limited to N-Schottky diodes and MOS devices. The IBM 180nm process has been supplemented with an additional P-type schottky diode whose V_D is around 120mV. Proper sizing of the P-type Schottky diodes ensures adequate f_T and lower V_D thus maximizing the output of the RF-DC converter with a fewer number of stags. By increasing the number of stages in the design to 4 and changing the switch to a P-type schottky device, power levels up-to -6 dBm can be harvested. Increasing the number of stages can however pose a risk of developing excessive voltage as the input power levels increase. A proposed solution is to add a shunt regulator that dumps the extra power to ground and prevents the output of the RF-DC converter from exceeding the rated 1.8V or alternately reflect power into the tissue for better dispersal.

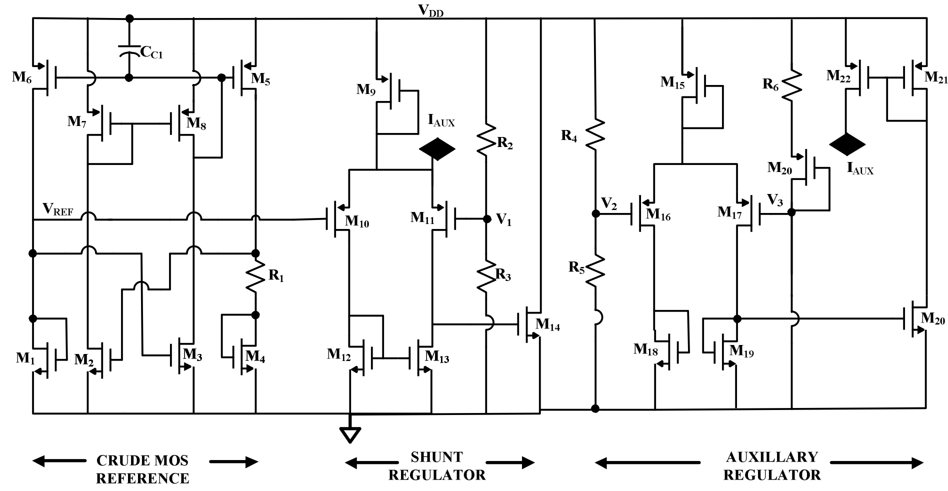


Figure 6.11 Schematic of the limiter

Figure 6.11 shows the schematic of the proposed limiter circuit. It consists of the crude MOS reference of 0.4V, a shunt regulator and an auxiliary regulator circuit. The crude MOS reference is designed in such a manner that V_{REF} has a rise time nearly equal to that of the unregulated V_{DD}. This value happens to be around 1µS. R_2 and R_3 have been sized such that $V_1 = 0.4V$ when V_{DD} has reached 1V as follows:

$$V_1 = \left(\frac{R_3}{R_2+R_3}\right) 1 = 0.4V \tag{6.10}$$

This gives V_{GS14} sufficient strength to turn on and pull the V_{DD} node lower, dumping the extra power to ground. An auxiliary regulator is added to assist the main regulator in preventing the V_{DD} node from rising beyond 1.5V. R_4 and R_5 have been sized such that

$$V_2 = \left(\frac{R_5}{R_4+R_5}\right) 1.2 = 0.6\ V \tag{6.11}$$

and

$$V_3 = V_{DD} - I_{REF} R_6 \tag{6.12}$$

As V_{DD} rises even further, the current in transistors M_{19} and M_{17} increases and is mirrored to the main shunt regulator. This causes the V_{GS} of M_{14} to further increase and pull the V_{DD} node further preventing it from reaching the target 1.8V.

(3) LDO and voltage reference: The quiescent current consumption of the LDOs is to be reduced from 2.45µA to 1.2µA in the both the designs. The feedback ladder for the LDO is to be replaced with un doped poly resistors or MOS devices. In the second generation design, the total power consumed by the front end blocks is redesigned as follows to 15µW.

$$P_{FRONTEND} = P_{VREF} + P_{LDO1} + P_{LDO2} + P_{FB} + P_{DEMOD} \quad (6.13)$$

$$P_{FRONTEND} = (0.9*8)+(3.6*0.9)+(3.6*0.9)+(1*0.7)+(1*0.7)=15\mu W \quad (6.1$$

To increase the PSRR of the voltage reference, it is proposed to replace the biasing of the node V_{B2} in figure 3.1 by a constant current circuit, and make it supply independent.

REFERENCES

[1] M. A. Lebedev and M. A. L. Nicolelis, "Brain-machine interfaces: past, present and future," *Trends in Neurosciences,* vol. 29, pp. 536-546, 2006.

[2] L. Shuenn-Yuh and L. Shyh-Chyang, "An implantable wireless bidirectional communication microstimulator for neuromuscular stimulation," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 52, pp. 2526-2538, 2005.

[3] S. Venkataraman, C. Hutchens, and R. L. Rennaker, "RF-front end for wireless powered neural applications," in *51st Midwest Symposium on Circuits and Systems*, 2008, pp. 682-685.

[4] K. Iniewski, *VLSI circuits for biomedical applications*: Artech House, 2008.

[5] www.olmicrowaves.com/menucontents/designsupport/rfid/AN90121_9.pdf

[6] A. Jalali and P. Mermelstein, "On the bandwidth efficiency of CDMA systems," in *Communications, 1994. ICC '94, SUPERCOMM/ICC '94, Conference Record, 'Serving Humanity Through Communications.' IEEE International Conference on*, 1994, pp. 515-519 vol.1.

[7] A. Y. Chow, V. Y. Chow, K. H. Packo, J. S. Pollack, G. A. Peyman, and R. Schuchard, "The artificial silicon retina microchip for the treatment of vision loss from retinitis pigmentosa," *Arch Ophthalmol,* vol. 122, pp. 460-9, 2004.

[8] M. F. Dorman, P. C. Loizou, and D. Rainey, "Simulating the effect of cochlear-implant electrode insertion depth on speech understanding," *J Acoust Soc Am,* vol. 102, pp. 2993-6, 1997.

[9] F. Flack, E. James, and D. Schlapp, "Mutual inductance of air-cored coils: Effect on design of radio-frequency coupled implants," *Medical and Biological Engineering and Computing,* vol. 9, pp. 79-85, 1971.

[10] D. C. Galbraith, M. Soma, and R. L. White, "A Wide-Band Efficient Inductive Transdennal Power and Data Link with Coupling Insensitive Gain," *IEEE Transactions on Biomedical Engineering,* vol. BME-34, pp. 265-275, 1987.

[11] W. J. Heetderks, "RF powering of millimeter- and submillimeter-sized neural prosthetic implants," *IEEE Transactions on Biomedical Engineering,* vol. 35, pp. 323-327, 1988.

[12] C. R. Neagu, H. V. Jansen, A. Smith, J. G. E. Gardeniers, and M. C. Elwenspoek, "Characterization of a planar microcoil for implantable microsystems," *Sensors and Actuators A: Physical,* vol. 62, pp. 599-611, 1997.

[13] R. Sarpeshkar, *Ultra low power Bioelectronics*: Cambridge university presss, 2010.

[14] S. Mingui, M. Mickle, L. Wei, L. Qiang, and R. J. Sclabassi, "Data communication between brain implants and computer," *Neural Systems and Rehabilitation Engineering, IEEE Transactions on,* vol. 11, pp. 189-192, 2003.

[15] T. Ibrahim, D. Abraham, and R. Rennaker, "Electromagnetic Power Absorption and Temperature Changes due to Brain Machine Interface Operation," *Annals of Biomedical Engineering,* vol. 35, pp. 825-834, 2007.

[16] P. R. Kennedy and R. A. Bakay, "Restoration of neural output from a paralyzed patient by a direct brain connection," *Neuroreport,* vol. 9, pp. 1707-11, Jun 1 1998.

[17] A. C. Hoogerwerf and K. D. Wise, "A three-dimensional microelectrode array for chronic neural recording," *IEEE Transactions on Biomedical Engineering,* vol. 41, pp. 1136-1146, 1994.

[18] J. F. Hetke, J. L. Lund, K. Najafi, K. D. Wise, and D. J. Anderson, "Silicon ribbon cables for chronically implantable microelectrode arrays," *IEEE Transactions on Biomedical Engineering,* vol. 41, pp. 314-321, 1994.

[19] R. J. Vetter, J. C. Williams, J. F. Hetke, E. A. Nunamaker, and D. R. Kipke, "Chronic neural recording using silicon-substrate microelectrode arrays implanted in cerebral cortex," *IEEE Transactions on Biomedical Engineering,* vol. 51, pp. 896-904, 2004.

[20] X. Lisheng, M. Q. H. Meng, and C. Yawen, "Effects of Dielectric Parameters of Human Body on Radiation Characteristics of Ingestible Wireless Device at Operating Frequency of 430 MHz," *Biomedical Engineering, IEEE Transactions on,* vol. 56, pp. 2083-2094, 2009.

[21] T.H.Lee, "*The Design of CMOS Radio-Frequency Integrated Circuits*," Second ed: Cambridge Univ. Press, 2005, pp. 94-95.

[22] R. Barnett, S. Lazar, and L. Jin, "Design of multistage rectifiers with low-cost impedance matching for passive RFID tags," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2006, p. pp.4

[23] R. E. Barnett, L. Jin, and S. Lazar, "A RF to DC Voltage Conversion Model for Multi-Stage Rectifiers in UHF RFID Transponders," *IEEE Journal of Solid-State Circuits,* vol. 44, pp. 354-370, 2009.

[24] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid-State Circuits,* vol. 11, pp. 374-378, 1976.

[25] J. P. Curty, N. Joehl, F. Krummenacher, C. Dehollain, and M. J. Declercq, "A model for μ-power rectifier analysis and design," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 52, pp. 2771-2779, 2005.

[26] S. Mandal and R. Sarpeshkar, "Low-Power CMOS Rectifier Design for RFID Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 54, pp. 1177-1188, 2007.

[27] A. Shameli, A. Safarian, A. Rofougaran, M. Rofougaran, and F. De Flaviis, "Power Harvester Design for Passive UHF RFID Tag Using a Voltage Boosting Technique," *IEEE Transactions on Microwave Theory and Techniques,* vol. 55, pp. 1089-1097, 2007.

[28] B. Razavi, "*Fundamentals of Microelectronics*," 1st ed: Wiley, 2008, p. 108.

[29] Richard C.Jaeger and T. N.Blalock, *Microelectronic Circuit Design* 4th ed., 2004.

[30] R. J. Baker, "CMOS Circuit Deisgn,Layout and Simulation," 3rd ed: Wiley, 2010, pp. 760-761.

[31] Donald.A.Neamen, "Semiconductor Physics and Devices: Basic Principles," 1 ed: Irwin, 1992 p. 325.

[32] T.H.Lee, "*The Design of CMOS Radio-Frequency Integrated Circuits*," Second ed: Cambridge Univ. Press, 2005, pp. 614-615.

[33] R. J. Baker, "CMOS Circuit Design,Layout and Simulation," 3 ed: Wiley 2010, p. 784.

[34] V. saxena, "Indirect Feedback Compensation Techniques for Multi-Stage Operational Amplifiers," M.S, Department of Electrical and Computer Engineering, Boise State University, Boise, 2007.

[35] R. J. Baker, "CMOS Circuit Design,Layout and Simulation," 3 ed: Wiley 2010, pp. 678-679.

[36] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *Solid-State Circuits, IEEE Journal of,* vol. 18, pp. 629-633, 1983.

[37] P. J. Hurst, S. H. Lewis, J. P. Keane, F. Aram, and K. C. Dyer, "Miller compensation using current buffers in fully differential CMOS two-stage operational amplifiers," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 51, pp. 275-285, 2004.

[38] P. R. Gray, Hurst, P.J., Lewis, S.H., Meyer, R.G., , *"Analysis and Design of AnalogIntegrated Circuits,"* 4th Ed., ed.: John Wiley & Sons, , 2001.

[39] R. J. Baker, "CMOS Circuit Design,Layout and Simulation," ed: Wiley 2005, pp. 290-291.

[40] C. Enz and E. Vittoz, "CMOS low-power analog circuit design," *Designing Low Power Digital Systems, Emerging Technologies,* vol. 1, pp. 79-133, 1996.

[41] E. VITTOZ and J. FELLRATH, "CMOS analog integrated circuits based on weak inversion operation," *IEEE Journal of Solid-State Circuits,* 1977.

[42] E. A.Vittoz, "Weak inversio in analog and digital circuits," presented at the CCCD Workshop Lund, 2003.

[43] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits,* vol. 24, pp. 1433-1439, 1989.

[44] R. J. Baker, "CMOS Circuit Design,Layout and Simulation," ed: Wiley 2005, pp. 768-769.

[45] K. Sanborn, M. Dongsheng, and V. Ivanov, "A Sub-1-V Low-Noise Bandgap Voltage Reference," *IEEE Journal of Solid-State Circuits,* vol. 42, pp. 2466-2481, 2007.

[46] R.J.Baker, "CMOS Circuit Design,Layout and Simulation," 3 ed: Wiley 2010, pp. 783-787.

[47] A. Islas Ohlmaier, "Design of programmable, low power, low dropout voltage regulators for portable applications," M.S thesis, Electrical and Computer Engineering, Texas A&m, 2005.

[48] E. S. Sinencio, "Low Drop-Out Voltage Regulators," in *Lecture 12 ELEN 607*, ed, 2007.

[49] V. Saxena and R. J. Baker, "Compensation of CMOS op-amps using split-length transistors," in *Circuits and Systems, 2008. MWSCAS 2008. 51st Midwest Symposium on*, 2008, pp. 109-112.

[50] V. MAdhuravasal, "Extreme Temperature Switch Mode Power Supply Based on Vee-Squared Control Using Silicon Carbide,Silicon on Sapphire,Hybrid Technology," Ph.D dissertation, Department of Electrical and Computer Engineering, Oklahoma State University, Stillwater, 2009.

[51] N. Kayathi, "Extended Models of silicon on sapphire transistor for analog and digital design at elevaed temperature," M.S dissertation, Department of Electrical and Computer Engineering, Oklahoma State University, Stillwater, 2005.

[52] http://www.soiconsortium.org/pdf/SOI_Implementation_WhitePaper_Infotech_v2.pdf.

[53] http://www.es.isy.liu.se/projects/SOI/background.html#SOI.

[54] B. razavi, "Design of CMOS Analog Integrated circuit Design," 2006.

[55] http://www.intersil.com/data/tb/tb417.pdf.

[56] *http://www.cissoid.com/images/stories/pdf/Datasheets/cht-bg3m.pdf*.

[57] *"EPC Radio-Frequency Protocols Class -1 Generation-2 UHF RFID Protocol for Communications at 860 MHz-960MHz"*.

VITA

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Doctor of Philosophy

Dissertation: A 2.45 GHz RF-FRONT END FOR A MICRO NEURAL INTERFACE SYSTEM

Major Field: Electrical Engineering

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Education:

Completed the requirements for the Doctor of Philosophy in Electrical Engineering at Oklahoma State University, Stillwater, Oklahoma in July, 2011.

Master of Science – Electrical and Computer Engineering, Oklahoma State University, Stillwater, OK, December 2003.

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Experience:

Research assistant in the Mixed Signal VLSI Group, Oklahoma State University since January 2005.
Worked on the design of circuits for high temperature applications using SOI process. Jan' 2005 – June 2008
Duties included design, layout and testing of analog circuits in the peregrine SOS process.
Worked on micro neural interface system using the IBM process.
June 2008 – July 2011.
Responsible for the design, layout and testing of RF-Front end circuits.

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Institution: Oklahoma State University Location: Stillwater, Oklahoma

Title of Study: A 2.45 GHz RF – FRONT END FOR A MICRO NEURAL INTERFACE SYSTEM

Pages in Study: 131 Candidate for the Degree of Doctor of Philosophy

Major Field: Electrical Engineering

Scope and Method of Study:
Active implants inside the human body should be capable of performing their intended function for decades without replacement with minimal tissue heating. It is therefore highly desirable for them to operate reliably and efficiently in a battery-less environment at very low power levels. Traditionally inductive coupling has been the preferred choice of power transfer to the active implants. Inductive coupling suffers from bandwidth and alignment issues that limit their usefulness for distributed sensor systems. The ability to use both near field and far-field RF to power and communicate with sensors distributed in the body would provide a major advance in implantable device technology. Recent advances in wafer packaging technologies and advanced VLSI processes together offer the possibility of a highly reliable system on chip (SOC) solution using RF energy as a source to power the active implants. This research work deals with the design and testing of a RF- Front end capable of harvesting up to 42µW at -3dBm power levels while providing 700mV and 400mV regulated DC voltages under 50µA and 4µA continuous load conditions respectively for signal conditioning electronics and control. In addition the RFIDS contains both an AM demodulator and a 400mV voltage reference. The RF front end chip occupies an area of 2.32 mm^2 and has been fabricated in 180nm IBM CMRF7SF process.

Findings and Conclusions:

A power harvesting front end complete with LDOs, voltage reference, and demodulator suitable for operating at 2.45GHz for neural/biosensor applications capable of harvesting greater than 40µW at – 3dBm of RF signal levels was presented. Regulated supplies of 700mV and 400mV supporting 54µA of total load current heavily weighted for analog signal conditioning, a Gen-2 compatible demodulator and 400mV voltage reference have been demonstrated. Measured results are within the process skew parameters of ± 10% with the exception of the voltage reference PSRR. Maximum measured regulated output voltage range for the LDOs is from -3dBm to -1dBm and with efficiencies greater than 8.4%. The harvester system presented here is a fully functioning regulated power system suitable for powering signal acquisition and data transmission hardware.

ADVISER'S APPROVAL: Dr. Chris Hutchens