A 700mV LOW POWER LOW NOISE IMPLANTABLE NEURAL RECORDING SYSTEM DESIGN

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Abstract: This dissertation presents the work for design and implementation of a low power, low noise neural recording system consisting of Bandpass Amplifier and Pipelined Analog to Digital Converter (ADC) for recording neural signal activities. A low power, low noise two stage neural amplifier for use in an intelligent Radio-Frequency Identification (RFID) based on Operational Transconductance Amplifier (OTA) is utilized to amplify the neural signals. The optimization of the number of amplifier stages is discussed to achieve the minimum power and area consumption. The amplifier power supply is 0.7V. The midband gain of amplifier is 58.4dB with a 3dB bandwidth from 0.71 to 8.26 kHz. Measured input-referred noise and total power consumption are 20.7μVrms and 1.90 μW respectively. The measured result shows that the optimizing the number of stages can achieve lower power consumption and demonstrates the neural amplifier's suitability for instu neutral activity recording. The advantage of power consumption of Pipelined ADC over Successive Approximation Register (SAR) ADC and Delta-Sigma ADC is discussed. An 8 bit fully differential (FD) Pipeline ADC for use in a smart RFID is presented in this dissertation. The Multiplying Digital to Analog Converter (MDAC) utilizes a novel cancellation technique robust to device leakage to reduce the input drift voltage. Simulation results of static and dynamic performance show this low power Pipeline ADC is suitable for multi-channel neural recording applications. The performance of all proposed building blocks is verified through test chips fabricated in IBM 180nm CMOS process. Both bench-top and real animal test results demonstrate the system’s capability of recording neural signals for neural spike detection.

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GLOSSARY

Abbreviations:

RF	-	Radio Frequency
INI3	-	Integrated Neural Interface 3
FSK	-	Frequency-shift keying
ADC	-	Analog to Digital Converter
PMOS	-	P- type Metal Oxide Semiconductor
OTA	-	Operational Transconductance Amplifier
NEF	-	Noise Efficiency Factor
MOS	-	Metal Oxide Semiconductor
NMOS	-	N- type Metal Oxide Semiconductor
BP	-	Bandpass Amplifier
ASIC	-	Application Specific Integrated Circuit
ICMS	-	Intracortical Microstimulation
SoC	-	System-on-chip
SAR	-	Successive Approximation Register
RFID	-	Radio Frequency Identification
IC	-	Integrated Circuit
EPC	-	Electronic Product Code
WISP	-	Wireless Identification and Sensing Platform
RAM	-	Random-access Memory
CMOS	-	Complementary Metal Oxide Semiconductor
PWM	-	Pulse-width Modulation
PSK	-	Phase-shift Keying

PLL	-	Phase Lock Loop
LDO	-	Low-dropout regulator
RF-DC	-	Radio Frequency to Direct Current
EEG	-	Electroencephalography
EMG	-	Electromyography
ECG	-	Electrocardiography
ID	-	Identification
FOM	-	Figure of Merit
MDAC	-	Multiplying Digital-to-Analog Converter
GBP	-	Gain Bandwidth Product
CMFB	-	Common Mode Feedback
DAC	-	Digital to Analog converter
OSR	-	Oversampling Times
CM	-	Common Mode
FD	-	Fully Differential
CDS	-	Correlated Double Sampling
FFT	-	Fast Fourier Transform
DNL	-	Differential Nonlinearity
INL	-	Integral Nonlinearity
OCP	-	Open-circuit Potential
PCB	-	Printed Circuit Board
V_T	-	Threshold Voltage
VLSI	-	Very large scale integration
DR	-	Dynamic Range
ENOB	-	Effective number of bits
MIM	-	Metal-Insulator-Metal

CHAPTER I

INTRODUCTION

This chapter consists of four main sections: motivation, literature review, system design and dissertation organization. Section 1.1 provides an introduction to implantable medical electronics. Section 1.2 reviews the various existing neural recording systems. Section 1.3 states the complete system design and section 1.4 discusses the dissertation organization.

1.1 Motivation

Due to the rapid advancement of microelectronics and integrated circuits, compelling applications in both the scientific and medical monitoring of biosignals have created a demand for wireless, unobtrusive sensors to collect this data [1-3]. Commercial medical implants like artificial pacemakers, cochlear implants and vagus nerve stimulators are providing the common functions like measuring of physiological information or stimulating nerves as medical implant devices [4, 5]. Example biosignals include; temperature, blood pressure, Electrocardiogram, heart rate, blood glucose level, neural signals and neural activity. In scientific applications, measurements of biosignals assist researchers to observe and study complex biological systems and their interactions, the effect of various diseases, and associated research treatments. In clinical settings, these signals are used by the physician or patient to either detect disease at onset or assist in the administration of treatment [6-8].

Measurement of biosignals presents several challenges. 1) Most importantly, the sensor must be unobtrusive or transparent as practical to the user. This involves minimizing the size and weight of the sensor and batteries. 2) The mobile nature of applications requires the entire system to operate on a limited power budget. The sensors should consume minimal power to maximize the sensor lifespan [9-13]. A number of solutions have been proposed to power smart sensors for data collection and communication including; a small batteries, an inductive power link, energy harvesting (light, RF etc.) as well as in combination [14-20]. Unfortunately, battery-powered sensors suffer from short lifespan due to the size and weight constraints of the battery [21, 22]. Inductively-coupled devices suffer from short wireless range (on the order of cm) [23-25]. 3) A means of wireless data collection is necessary for scientific research, where data should be available in real-time, and for medical biosensors where data is otherwise inaccessible. Wired connections suffer from infection and seriously restrain freedom of movement. As a result wireless telemetries are essential to the design of system of mobile biological subjects [26, 27]. 4) Compatibility of the system with bandwidth or noise floor of neural amplifier programmable is also essential because of a wide range of monitoring objects.

In this dissertation, we focus on neural recording system design. Neural activities can be observed simultaneously in more details down to a single cell [10] and Neuromotor prostheses is used to assist those paralyzed individuals to restore the lost motor functions [11]. Many experiments in human subjects showed that control signals derived from clusters of neurons' spike activities can be applied to the control and use of a computer mouse, a keyboard and robotic arms [11-31].

These neural signals range from 50-500 uV. Their successful use requires that the input-referred noise to be less than 5-10μV [31], as a result there are major design challenges in developing very small low-power circuits while simultaneous achieving acceptable input-referred noise levels. Given allowed neural power constraints of less than 100uW [10-14], signal fidelity is limited by either capacitor matching or input referred noise. Capacitor mismatching error can be alleviated

by capacitor trimming and/or calibration techniques. Lower input referred noise is in direct conflict with low power performance. For chronic clinical applications where these devices may remain implanted for the life of the patient, another challenge is powering and communicating with these devices without the presence of wires or batteries.

1.2 Literature Review

Many neural recording systems have been developed in the past years [14-31]. Harrison [14, 15] proposed a neural amplifier using a pseudoresistor as a high-resistance element and on-chip capacitors to amplify low frequency signals down to millihertz range. Most neural amplifiers [16-31] use Harrison's structure or a modification there of, differential to single ended or differential to differential modes. There is also a tradeoff between distortion and power in neural amplifier design. Sarpeshkar [16] presented an amplifier based on modified folded-cascode OTA structure replacing the degenerated MOS transistor current with a degenerated resistor. Ming [17] developed a programmable gain and bandwidth amplifier. Sitong [18] designed an alternative programmable bandwidth amplifier using current biased pseudo-resistor. A microphotograph of a low power low voltage neural recording chip is shown in Figure 1.1.

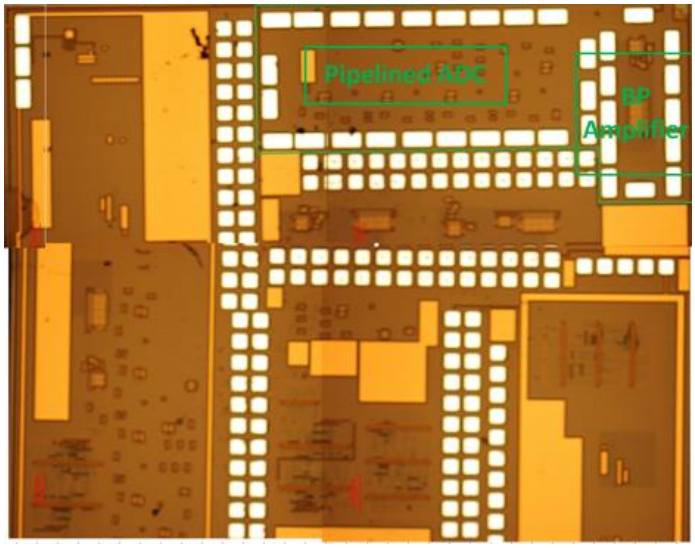


Fig.1.1 Microphotograph of a low power low voltage neural recording Chip

Harrison's group [14] integrated all the functionalities including neural signal amplification, data reduction, neural signal digitization, and wireless communication into a single chip. The system contains 100 neural recording channels and includes a wireless data transmission feature by a fully-integrated FSK (Frequency-shift keying) transmitter. The power and commands are transferred from an external unit to the implanted system via an inductive power link. The system utilizes a simple thresholding scheme with analog spike detection circuitry to reduce the amount of data needed to be transmitted and allow one raw analog channel to be selected for full digitization by a 10 bit resolution ADC (Analog to Digital Converter). The total power consumption of the system is 13.5mW. In Figure 1.2, a novel bioamplifier was designed and tested that uses a pseudoresistor element to amplify low-frequency signals down to the millihertz range while rejecting large dc offsets [15]. Transistors Ma-Md are acting as pseudo resistors. When Vgs is negative, each device functions as a diode connected PMOS transistor; when Vgs is positive, the parasitic source-well-drain p-n-p bipolar junction transistor is utilized to achieve extremely high resistor r_{inc}. For $\Delta V<0.2V$, r_{inc} is measured higher than $10^{11}\Omega$. The low frequency of amplifier is given by $1/ (2\pi r_{inc}C_2)$. The amplifier uses a standard wide-output swing operational transconductance amplifier (OTA) with capacitive feedback to realize a gain of approximately 40 dB. The resulting amplifier passes signals from 0.025 Hz to 7.2 kHz with an input-referred noise of 2.2 uV_{rms} and a power dissipation of 80 uW while consuming 0.16 mm^2 of chip area.

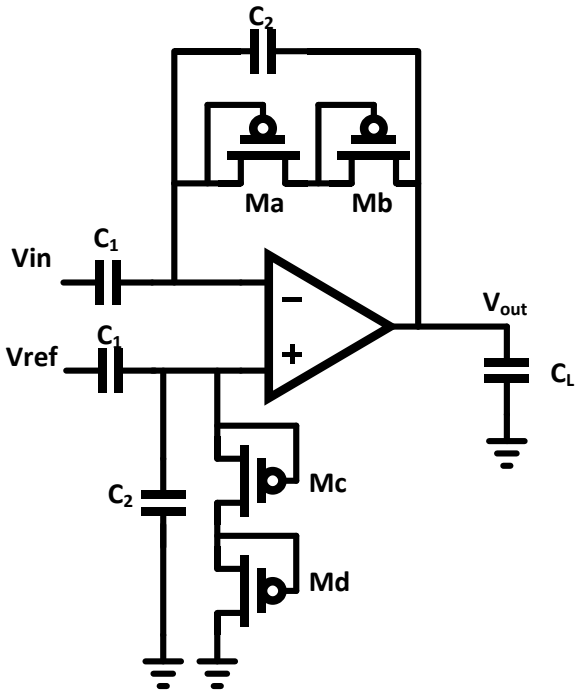


Figure1.2 Schematic of Harrison's neural amplifier [15]

The tradeoff between power and noise is quantified with a NEF (noise efficiency factor). Where the NEF is given as:

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi U_T * 4kT * BW}} \tag{1.1}$$

Where $V_{ni,rms}$ is the input referred rms noise voltage, I_{tot} is the total amplifier supply current, and BW is the amplifier bandwidth. In weak inversion, the expression for NEF reduces to

$$NEF = \sqrt{\frac{4}{n^2}} \cong 2.9 \tag{1.2}$$

Assuming n=1.4, where n is the subthreshold slope factor. This is the theoretical NEF limit for amplifier with that circuit topology constructed, the current mirror ratios of unity are assumed. In

practice, the NEF will be limited by the ratios of other currents to differential pair current and 1/f noise.

Sarpeshkar [16] shows that the minimum NEF for any existing amplifier topology using a differential pair as the input stage is equal to 2.02 for a typical value of n=1.4 by setting differential pair current dominates current of amplifier. Moreover, an NEF 2.67 is measured by using the modified folded-cascode OTA structure, which is in very close agreement with the theory. The Sarpeshkar's amplifier shown in Figure 1.3 yielded a midband gain of 40.8 dB and a 3-dB bandwidth from 45 Hz to 5.32 kHz; the amplifier's input-referred noise was measured to be 3.06 uV_{rms} while consuming 7.56 uW of power from a 2.8-V supply.

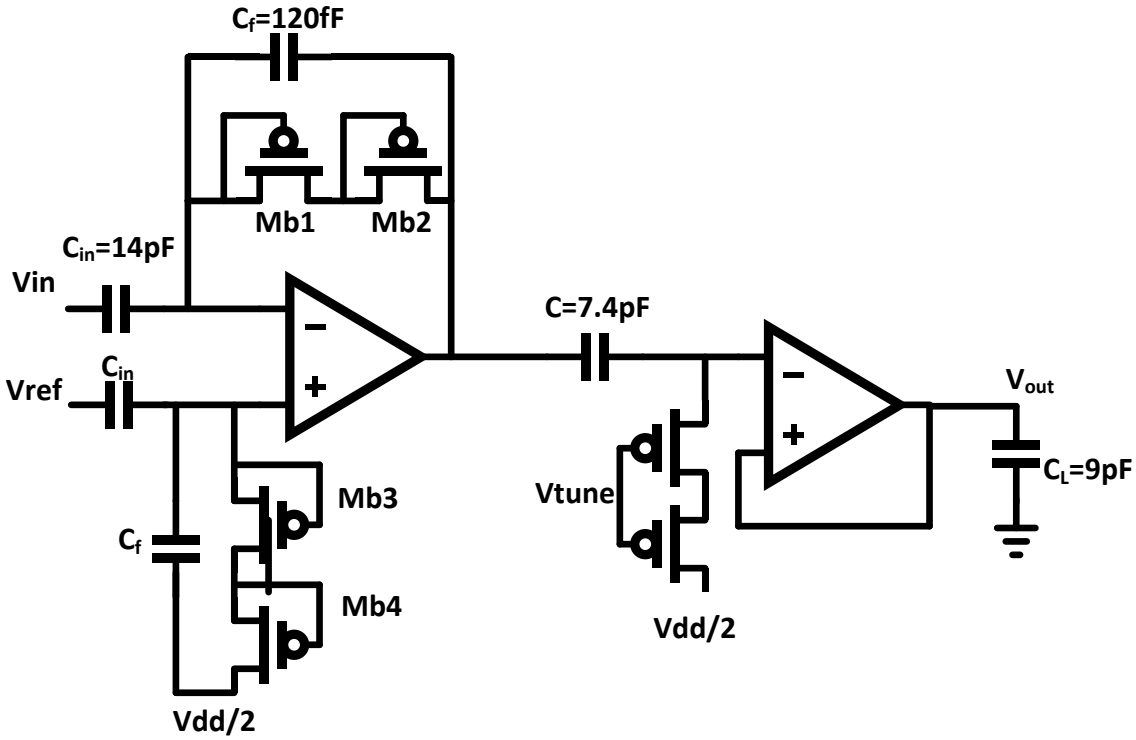


Figure1.3 Schematic of Sarpeshkar's BP amplifier [16]

A modified version of a standard folded-cascode OTA topology with source-degenerated current mirrors achieves a very efficient power–noise tradeoff because it uses a new low-power low-noise OTA topology that makes efficient use of the supply current. The schematic of a modified

version of a folded cascaded topology low-noise OTA is shown in Figure 1.4. The current source is implemented by M5, M6 and source degeneration resistors R1 and R2. With an appropriate choice of degeneration resistors, the noise contributions of new current source are mainly from the resistors and can be made much smaller than the contributions from MOS transistors. The tradeoff of using resistors as current sources is the greater current (possible excessive) consumed by the differential pair, the area consumed by the resistors over the MOS transistors current sinks, reduced gain and power inefficiency.

Subthreshold noise current is $\overline{i_n^2} = 2nkTg_m$ [32], n is slope factor, k is Boltzmann's constant, T is temperature, gm is transconductance.

M1 and M2 operate in weak inversion and M11 and M12 operate in strong inversion. The input referred noise spectral density of the OTA is

$$\begin{aligned} v_{n,1}^2 &= \frac{1}{g_{m1}^2}(2*2nkTg_{m1} + \frac{8kT}{R_1} + \frac{16}{3}kTg_{m11}) \\ &= \frac{1}{g_{m1}}4nkT(1 + \frac{2U_T}{I_1R_1} + \frac{4}{3}k\alpha\frac{I_{11}}{I_1}) \end{aligned} \tag{1.3}$$

Where k=0.7 and $\alpha = \frac{2}{(1+\sqrt{1+4*IC_{11}})} \approx 1$, IC is the inversion coefficient of the transistor which is defined as the ratio of its channel current to the moderate inversion characteristic current. Equation (1.3) suggests that I_1R_1 should be large compared to $2U_T$ and current ratio I_1/I_{11} should also be large. In the implementation, the second and third terms in (1.3) are 0.18 and 0.054. Then equation (1.3) reduces to

$$v_{n,1}^2 = \frac{4.94*nkT}{g_{m1}} \tag{1.4}$$

Assuming the classical folded cascade amplifier is using P diff pair while P diff pair and P rail side devices have 1:1 current ratio. For folded cascode amplifiers the current noise spectral density is

$$i_{n,2}^2 = 2*2nkTg_{m1} + 2*2nkTg_{mn} + 2*2nkTg_{mp} \tag{1.5}$$

Where gm_1 is the transconductance of differential pair, gm_n is the transconductance of N rail side transistor and gm_p is the transconductance of P rail side transistor. Input referred noise spectral density is

$$v_{n,2}^2 = \frac{i_n^2}{g_{m1}^2} = \frac{2*2nkT}{g_{m1}} + \frac{2*2nkTg_{mn}}{g_{m1}^2} + \frac{2*2nkTg_{mp}}{g_{m1}^2}$$
$$= \frac{4nkT}{g_{m1}}(1+2+1) = \frac{16nkT}{g_{m1}} \tag{1.6}$$

From (1.4) and (1.6) the input referred noise spectral density of Sarpeshkar's OTA is around 1/4 time as classical folded cascade amplifier which is more energy efficient topology.

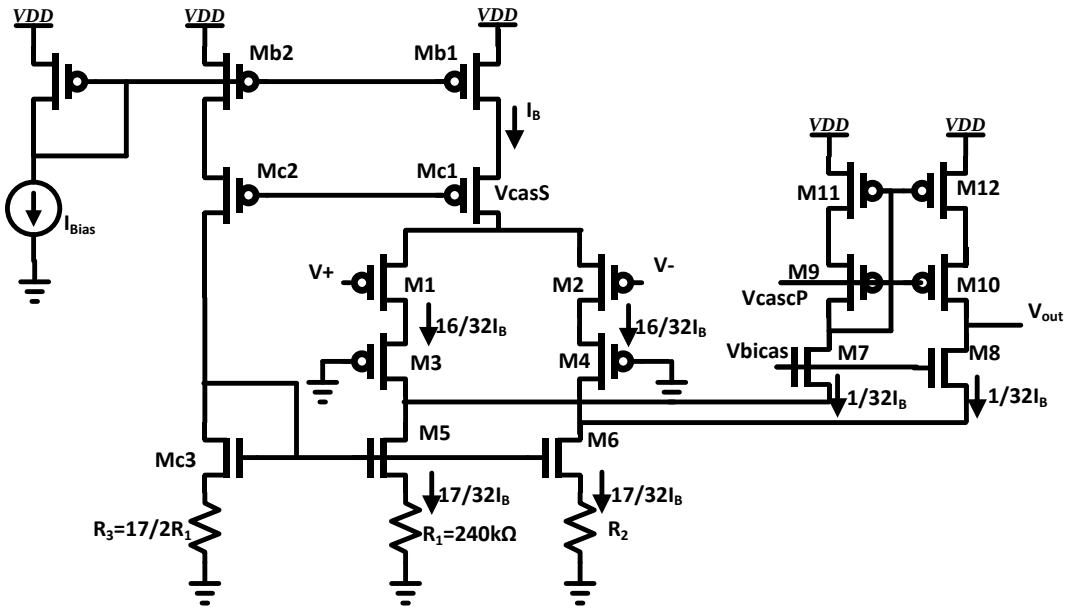


Figure1.4 Schematic of Sarpeshkar's low-noise OTA [16]

The schematic of Ming Yin's BP amplifier is shown is Figure 1.5. The amplifier current consumption is 8 μA with a ±1.7 V supply, with two measured AC gains of 39.3 dB and 45.6 dB [17]. The measured input referred noise is 3.6 μV over 20 Hz ~ 10 kHz. The low cutoff frequency is from 0.015 Hz to 700 Hz by varying the gate bias voltage of pseudo resistor. The high cutoff frequency is 4-bit programmable and can be adjusted from 120 Hz to 12 kHz at negligible load and 40 Hz to 4 kHz with a 2 pF active probe loading. The tunable high cutoff frequency is realized by two sets of PMOS and NMOS tail current transistors with gate enable bits B1-B4.

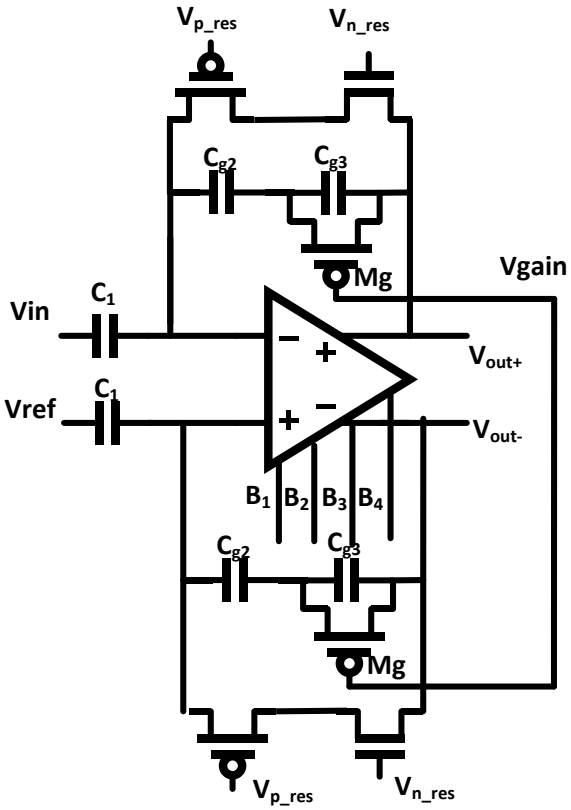


Figure1.5 Schematic of Ming Yin's BP amplifier [17]

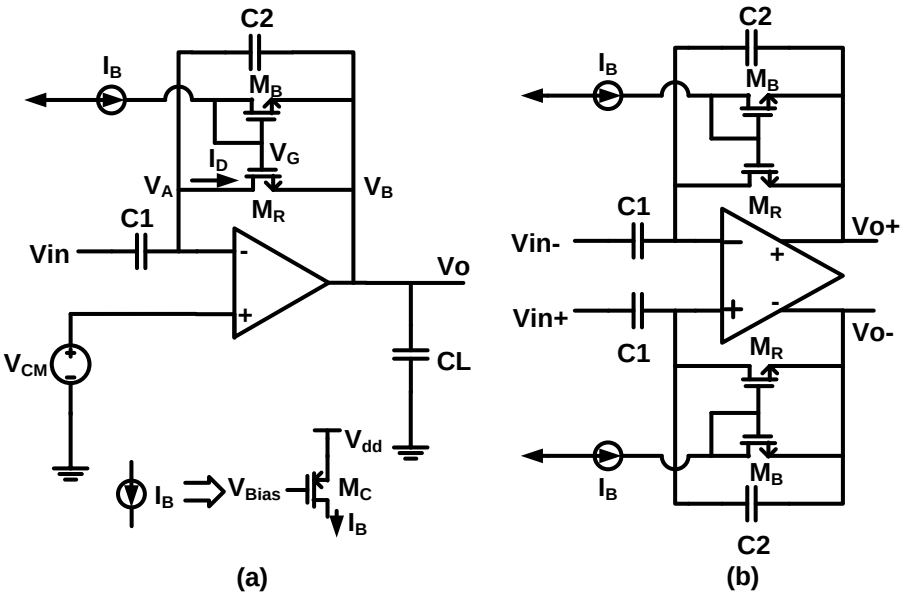


Figure1.6 Schematic of Sitong's BP amplifier [18]

The schematic of Sitong's BP amplifier is shown in Figure 1.6 [18]. The bandwidth of this filter is from 500 Hz to 5 KHz. The power consumption is 0.6 μW for a gain of 19.5 dB. The input referred noise is 67.7 μVrms with a power supply of 5 V. A current biased programmable pseudo-resistor for implantable extracellular neural signal recording applications is introduced to reduce this feedback resistor variation. The pseudo-resistor, biased in the subthreshold operation, is able to realize a very large resistance while keeping the silicon area small. The lower cutoff frequency is tunable from tens of Hz to hundreds of Hz by offering a wide range of resistances implemented by log nature of the bias current. The effective resistance is given as:

$$R_{eq} = \frac{S_B U_T}{S_R I_B} \tag{1.7}$$

where S_B and S_R are the aspect ratios (W/L) of M_B and M_R. I_B is the bias current of M_B. Equation (1.7) shows that the effective resistance accuracy is limited by the matching between MR and MB and the accuracy of I_B.

Another system with 64 channels was reported by Sodagar in [19]. The penny-size microsystem implemented on the platform is shown in Figure 1.7. To record from 64 channels, the system utilizes four 16-channel neural preconditioning ASICs in parallel. The preconditioning ASICs are interfaced with a neural processing unit which consists of two 32-channel neural processing chips. The system also contains a bi-directional telemetry chip for transmitting neural data to the external world, and for receiving power, commands, and a clock to operate the implant. The recording front-end was characterized as having a mid-band gain of 59.5dB, an input referred noise of 8μV, a tunable low frequency range from 0.1Hz to 100Hz and high cutoff frequency 9.1 kHz. The scan rate of the channel is 62.5kS/sec using 2MHz clock with the power dissipation of 225μW/Ch.

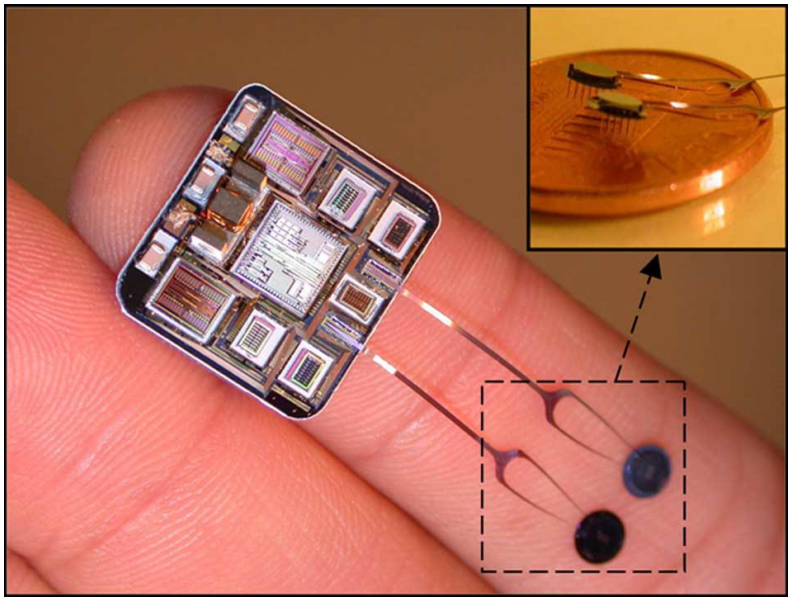


Fig.1.7 The penny-size microsystem implemented on the platform in [19]

Rabaey [20] presents an area-efficient neural signal acquisition system in Figure 1.8 that uses digital blocks to reduce system area while operating on a power supply 0.5V. Replacing ac coupling capacitors and analog filters with a dual servo loop, the system is enables simultaneous digitization of the action and local field potentials. A noise efficient DAC and a compact sampling ADC are used to cancel input offset and prevent noise folding. The system consumes

5uW with input-referred noise of 4.9uV for a 10 kHz bandwidth. In order to reduce the dynamic range requirement of the instrumentation amplifier and ADC, the feedback of digital low-pass filter and DAC regenerate the sum of low-frequency components. The ADC is 8bit resolution and DAC performs 7 bit coarse offset cancellation.

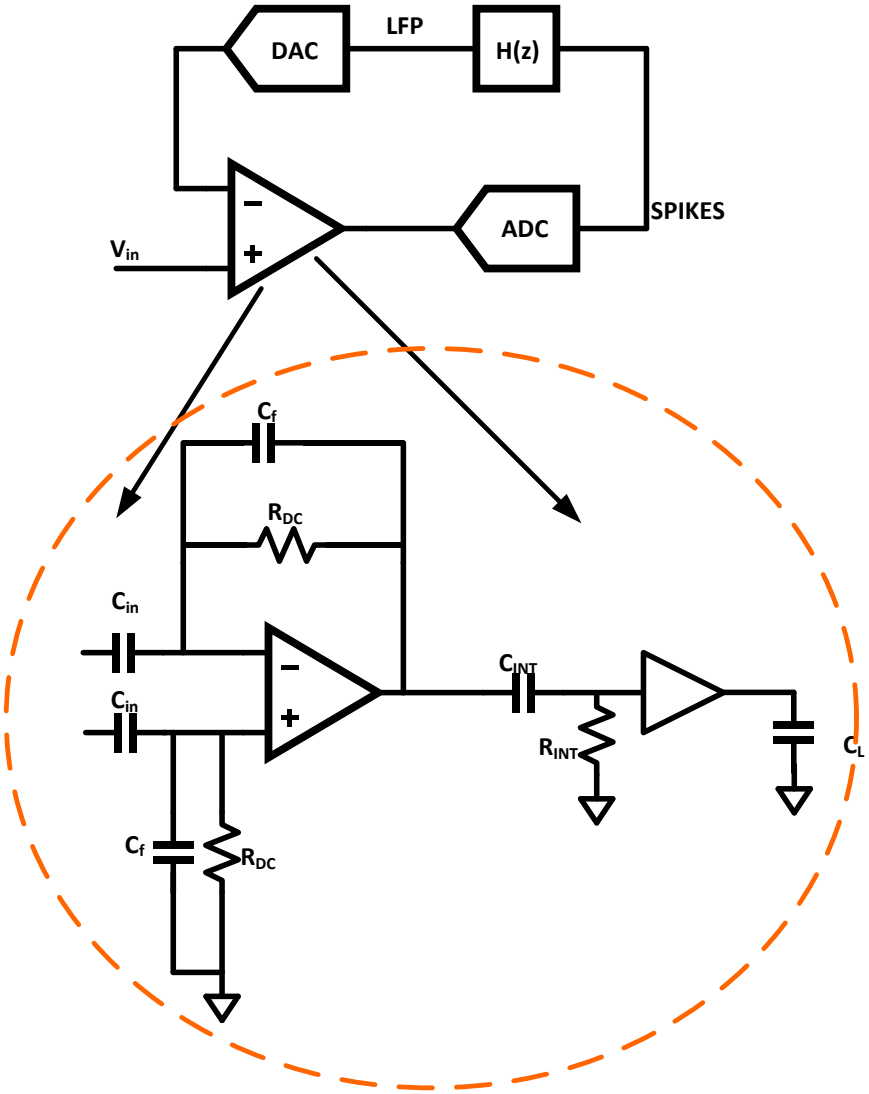


Figure 1.8 Mixed-signal feedback architecture in [20]

Mohseni [21] designed an activity-dependent intracortical microstimulation (ICMS) system-on-chip (SoC) that converts the extracellular neural spikes to an electrical stimuli delivered to

another region of the brain in real time in *vivo*. The proposed ICMS architecture is shown in Figure 1.9. The ICMS architecture incorporates two identical 4-channel modules and each consisting of; An analog recording front-end with a total input noise voltage of 3.12 uV and an NEF of 2.68 (Folded Cascode), consuming 5.9uW, an 10-bit successive approximation register analog-to-digital converters (SAR ADC) at 35.7 kS/Ch consuming 12.4uW with a digital spike discrimination processor, and a programmable constant-current microstimulating back-end that delivers up to 94.5 uA with 6-bit biphically stimulus to cortical tissue when triggered by neural activity.

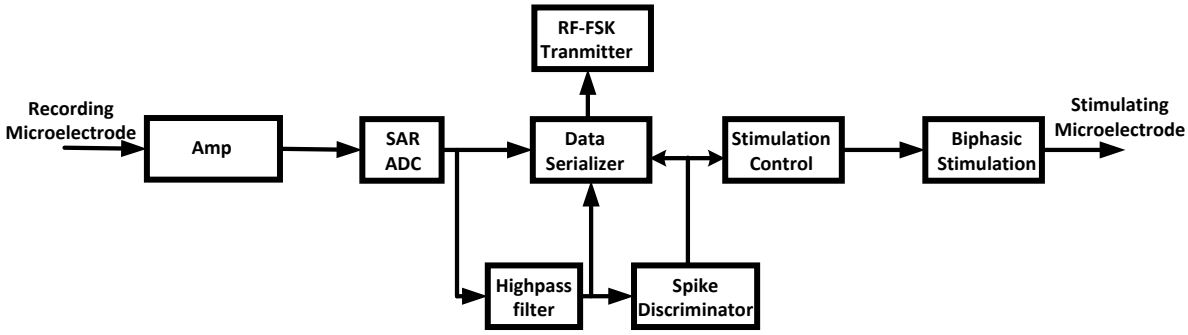


Figure 1.9 Proposed architecture of proof-of-concept system for activity-dependent ICMS in [21]

A number of full tag RFID (Radio Frequency Identification) implementations have been presented in the literature [9, 22-24]. Otis presented a fully-passive 900 MHz RFID tag IC (Integrated Circuit) with addressability, full EPC (Electronic Product Code) Class 1 Generation 2 (Gen2) protocol compatibility, a 1.25 μV_{rms} integrated noise chopper-stabilized micropower sensor interface amplifier from 0.05Hz to 100Hz, and an 8b ADC in [9]. The block of system is shown in Figure 1.10. An off-the-shelf RFID reader is enabling previously impossible recording scenarios like temperature and motor patterns of small insects with communication range 3 m.

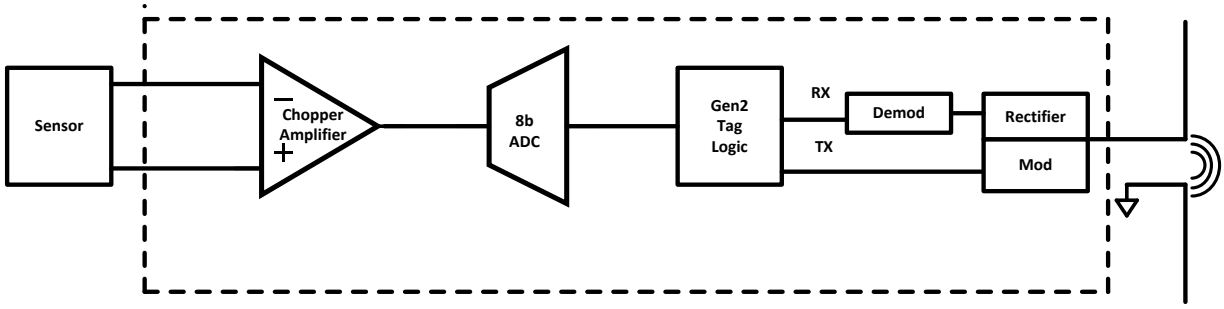


Figure 1.10 Block diagram of system in [9]

Table 1.1 Survey of existing work in neural interface SoC

Work	**Application**	**Supply Voltage (V)**	**Midband Gain (dB)**	**Band Width (kHz)**	**Input Referred Noise (µVrms)**	**NEF**	**Total Power (µW)**
Harrison [14]	Neural recording	3.3	60	5	4.8	4.8	80
Azin [21]	Neural recording& Stimulation	1.5	51.9-65.6	12	3.12	3.9	26.9
Zhiming [25]	Neural recording	0.8	49	6.2	14	6.5	20
Walker [26]	Neural recording& Stimulation	1.2	40	10	2.2	4.5	43
M.Chae [27]	Neural recording	±1.65	40	20	4.9	5.0	46.9
F.Shahrokhi [28]	Neural recording & Stimulation	3	73	5	6.08	5.55	15.52

Table 1.1 reviews the performance of existing research work in neural interface SoC. Extracellular action potentials signal amplitude range from 50-500µV with most of neural activity between 0.1 Hz and 5 kHz [31]. Most neural amplifiers and ADC consume about 100µW of power while attaining low input referred noise 5-10 µV with a bandwidth of 5-10 kHz and the

background neural noise of recording site is 5-10 μV [14-21]. The extracellular action potential is sensed by the electrode and amplified by the neural amplifier. The actual input voltage of the amplifier is determined by the impedance ratio of the electrode and amplifier's input impedance. The input impedance of neural amplifier should be high enough to keep the gain error low. The impedance of electrode used for neural recording could be as high as 1MΩ at 1K Hz [27], as a result the input impedance of neural amplifier needs to be at least a few MΩ at 1K Hz. Fully differential architectures are utilized to provide high common-mode rejection ratio (CMRR) and reduce the even harmonic distortion.

Table 1.2 Performances of Neural Amplifiers

Author	**Supply Voltage (V)**	**Midband Gain (dB)**	**Bandwidth (Hz)**	**Input Referred Noise (μV_{rms})**	**Noise Effective Factor**	**Total Power (μW)**
[15]Harrison	±2.5	40	0.025-7.5k	2.1	4.8	80
[16]Sarpeshkar	2.8	40.85	45-5.32k	3.06	3.21	7.56
[17]Yin	1.7	39.3-45.6	0.015-4k	3.6	4.9	27.2
[18]Sitong	±2.5	19.5	500-5k	67.7	9.5	0.6

Table 1.2 reviews the performance of existing neural amplifiers. Most amplifiers consumes less than 100 μW power to achieve low input referred noise ($<5\mu V_{rms}$) in the bandwidth 5-10k Hz [15-18].

1.3 Research Objective

The many challenges associated with the design of a low power low noise implantable neural recording system include: 1) Efficient RF, thermal, or light power harvesting scheme are used to support signal conditioning bandpass amplifiers, ADC, system control and communications circuits [10-14]; 2) The implanted devices must not consume too much power due to the harmful effects to the surrounding tissue. Neural recording systems must consume less than 100uW [15-21]; 3) To achieve a large dynamic range, the total input referred noise from the recording circuit

less than 5-10μV [14-21]; 4) The input impedance of neural amplifier needs to be at least a few MΩ to minimize gain error [27].

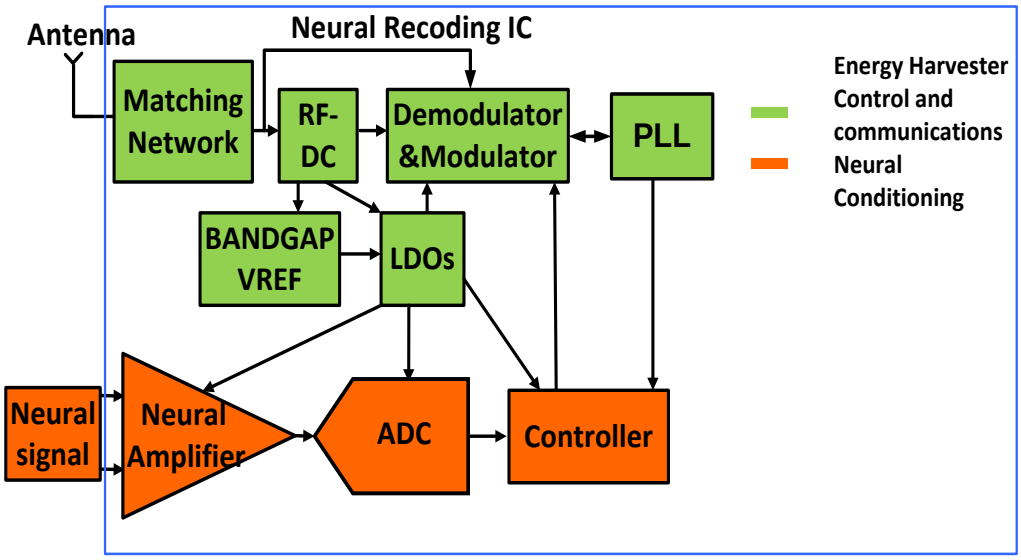


Figure 1.11 Block diagram of the neural recording system

A typical neural recording system architecture is shown in Fig. 1.11. The neural recording system consists of a neural amplifier, an 8-bit ADC, a controller, a power harvesting front end, a voltage reference and a PLL. The whole system is capable of harvesting power and amplifying, recording, digitizing and transmitting data in real time. The objective of this dissertation is to design and develop a signal conditioning circuit including a neural amplifier and an ADC. The neural amplifier will be designed to provide a 900 mid-band gain, a 500 to 8 kHz bandwidth, and a 10-μV_{rms} input referred noise. An 8-bit, 16ksps Pipelined ADC will then be designed to digitize the amplified sensor data. The neural amplifier and ADC both will use a 700mV power supply.

1.4 Thesis organization

Chapter I introduced the background, motivation and objective of this work. Chapter II reviews the FOM (Figure of Merit) of different OTA/Opamps for subthreshold application and two stage neural amplifier bandwidth, power and noise performance/efficiency. Chapter III reviews the power consumption advantage of Pipelined ADC over Sigma-Delta and Successive Approximation ADC. The design methodology and building blocks of 8 bit Pipelined ADC

including MDAC (Multiplying Digital to Analog Converter), comparators and non overlapping clocks are also discussed. Chapter IV presents test results for the neural amplifier and pipelined ADC. Chapter V summarizes the results of this work.

CHAPTER II

REVIEW OF OTA/OPAMP TOPOLOGOIES, THEIR DESIGN IN SUBTHRESHOLD AND APPLICATION TO BP AMPLIFIER DESIGN

There are ten sections in this chapter: sections 2.1-7 review seven more prominent OTA and Opamp topologies and developing a FOM (Figure of Merit) for each in subthreshold. Section 2.8 reviews and addresses neural amplifier design and section 2.9 present the performance summary of neural amplifier. Section 2.10 summarizes the chapter. The OTA/Opamp is the most significant block in bandpass amplifier design, providing low noise, low distortion, high gain, and sufficient output swing for input neural signal. The OTA or Opamps with best FOM is to be selected for the bandpass amplifier.

The GBP-Dynamic range/watt FOM [15, 16] for OTA/Opamps is defined as follows;

$$FOM = \frac{GBP_{OL} * DR}{Power}$$

Where GBP_{OL} is open loop Gain Bandwidth Product and DR is Dynamic Range of OTA/Opamp. It is necessary to make several assumptions to facilitate ease of analysis before proceeding with the topology comparison.

- Only thermal noise is considered for simplicity where in subthreshold the thermal noise model is given by [32]:

$\overline{i_n^2} = 2nkTg_m$, $g_m = \frac{I}{nU_T}$ and $n = \frac{C_j + C_{ox}}{C_j}$ $\overline{i_n^2}$ is noise current spectral density, n is slope factor, k is Boltzmann's constant, T is temperature, gm is transconductance, U_T is thermal voltage, C_j is depletion layer capacitance and C_{ox} is gate-oxide capacitance.

- The OTA/Opamps used in the bandpass amplifiers are required to achieve the same performance specification; equal gain bandwidth and noise requirement. Additionally it is assumed all OTA/Opamps will support similar or equal load capacitance requirements.
- All devices are assumed to be operating in subthreshold saturation, V_{ds} greater than $5U_T$ or approximately 125mV.
- For two stage OTA/Opamps, there are three different cases for the relationship between the load and compensation capacitance: $C_L \approx Cc$, $C_L >> Cc$ and $C_L << Cc$.
    1. For $C_L \approx Cc$, to shift the non-dominant pole requires the second stage leg of current I_2 be greater than the stage 1 differential pair current I_0;
    2. For $C_L >> Cc$, the current of second stage leg of current I_2 is required to be much greater than the stage 1 differential pair current I_0;
    3. For $C_L << Cc$, the current I_0 of first stage of two stage OTA/Opamps will dominate the total power consumption.
- The V_{ds} of each transistor is greater than or equal $5U_T$, to ensure all OTA/Opamps transistors are saturated, VDD is selected greater than $30U_T \approx 750mV$. With greater VDD comes greater signal swing and greater SNR or DR efficiency.

The initial evaluation uses open loop analysis. However, in fully differential applications the closed loop GBP_{CL} equals half the open loop GBP_{OL}. To achieve critical settling phase margin (PM) in closed loop is selected to be 76 degrees [40]. For two stage OTA/Opamps comparisons where the feedback factor β is less than 0.1 (See neural amplifier design specification in section 2.8) PM can be written as;

$$PM = 360 - 180 - \tan^{-1}\frac{GBP_{CL}}{\beta GBP_{CL}} - \tan^{-1}\frac{GBP_{CL}}{1.2*GBP_{CL}} + \tan^{-1}\frac{GBP_{CL}}{xGBP_{OL}}$$
$$= 180 - 88 - 40 + \tan^{-1}\frac{GBP_{CL}}{x\,GBP_{OL}} = 76 \qquad (2.1)$$

$$1/2x = \tan(76 + 88 + 40 - 180) = \tan(24) = 0.44$$
$$x = 1.1 \qquad (2.2)$$

From (2.1) the non-dominant pole is set 1.2*GBP_{CL} for 20% process variation with GBP_{CL} and left plane zero is found as 1.1*GBP_{OL} equals 2.2*GBP_{CL}.

After assumptions are introduced, we will start the FOM comparison of OTA/Opamps topologies.

2.1 Telescopic OTA where $C_C = C_L$

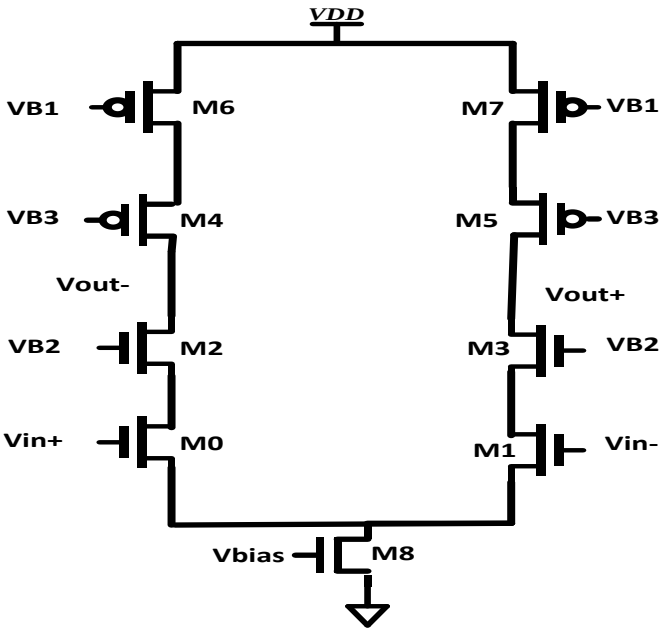


Figure 2.1 Schematic of Telescopic OTA [40]

Input referred noise spectral density is given: $\overline{v_n^2} = \frac{4nkT}{g_{m1}}\left(1 + \frac{g_{m6}}{g_{m1}}\right) \approx \frac{8nkT}{g_{m1}}$ (2.3)

Output referred noise is:

$$\overline{v_{no}} = \frac{1}{\beta}\sqrt{\frac{8nkT}{g_{m1}}}\sqrt{\frac{\pi}{2}\beta * GBP_{CL}} = \sqrt{\frac{1}{\beta^2}\frac{8nkT}{g_{m1}}\frac{\pi}{2}\beta\frac{g_{m1}}{2*2\pi C_L}} = \sqrt{\frac{nkT}{\beta C_L}} \quad (2.4)$$

$$GBP_{OL} = \frac{g_{m1}}{C_L} = \frac{I_1}{nU_T C_L} = 2 * GBP_{CL} \quad (2.5)$$

Fully differential dynamic range is:

$$DR \quad \propto \quad \frac{\left(\frac{V_o}{\sqrt{2}}\right)^2}{\overline{v_{no}^2}} = \frac{\left(2*\frac{(V_{DD}-5*5U_T)}{\sqrt{2}}\right)^2}{\frac{nkT}{\beta C_L}} = \frac{\left(2*\frac{(30U_T-5*5U_T)}{\sqrt{2}}\right)^2}{\frac{nkT}{\beta C_L}} = \frac{2*25U_T^2}{\frac{nkT}{\beta C_L}} \quad (2.6)$$

$$\text{Power=VDD*2I}_1 = 60U_T I_1 \quad (2.7)$$

$$FOM = \frac{GBP_{OL} * DR}{Power} = \frac{\frac{I_1}{nU_T C_L} * \frac{2*25U_T^2}{\frac{nkT}{\beta C_L}}}{60U_T I_1} = 0.83 * \frac{\beta}{n^2 kT} \quad (2.8)$$

2.2 Folded Cascode OTA where $C_C = C_L$

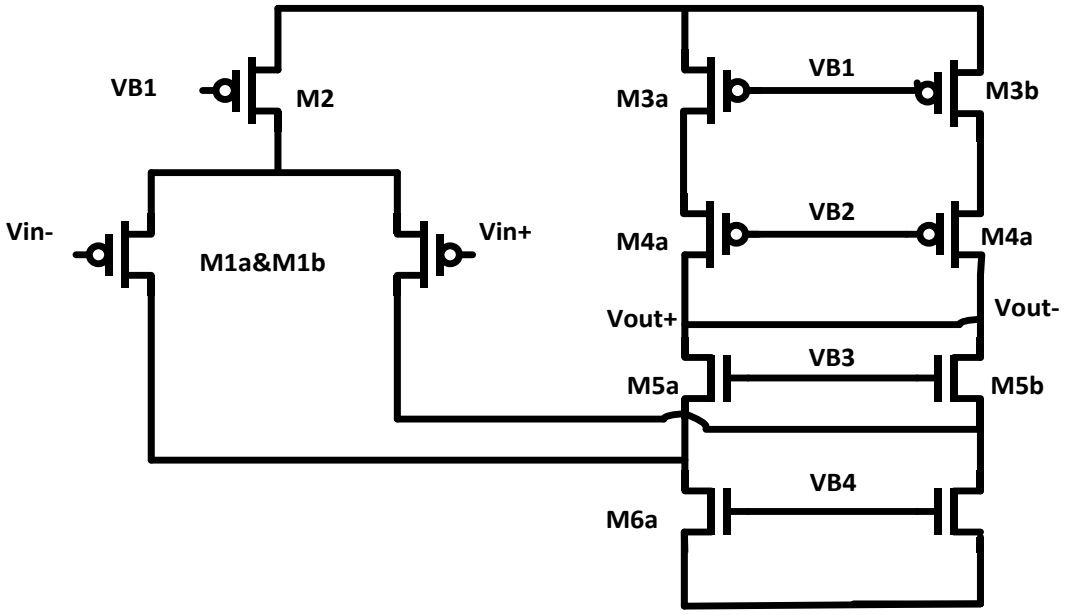


Figure 2.2 Schematic of folded cascode OTA [40]

Input referred noise spectral density is given:

$$\overline{v_n^2} = \frac{4nkT}{g_{m1}}\left(1+\frac{g_{m3}+g_{m6}}{g_{m1}}\right) \approx \frac{16nkT}{g_{m1}} \qquad \text{Assume } gm_1=gm_3 \approx 1/2gm_6 \tag{2.9}$$

$$GBP_{OL} = \frac{g_{m1}}{C_L} = \frac{I_1}{nU_T C_L} = 2*GBP_{CL} \tag{2.10}$$

Output referred noise is:

$$\overline{v_{no}} = \frac{1}{\beta}\sqrt{\frac{16nkT}{g_{m1}}}\sqrt{\frac{\pi}{2}\beta * GBP_{CL}} = \sqrt{\frac{1}{\beta^2}\frac{16nkT}{g_{m1}}\frac{\pi}{2}\beta\frac{g_{m1}}{2*2\pi C_L}} = \sqrt{\frac{2nkT}{\beta C_L}} \tag{2.11}$$

$$DR \propto \frac{\left(\frac{V_o}{\sqrt{2}}\right)^2}{\overline{v_{no}^2}} = \frac{\left(2*\frac{(V_{DD}-4*5U_T)}{\sqrt{2}}\right)^2}{\frac{2nkT}{\beta C_L}} = \frac{\left(2*\frac{(30U_T-4*5U_T)}{\sqrt{2}}\right)^2}{\frac{2nkT}{\beta C_L}} = \frac{2*100U_T^2}{\frac{2nkT}{\beta C_L}} \tag{2.12}$$

$$\text{Power} = VDD*2I_1*2 = 120U_T I_1 \tag{2.13}$$

$$FOM = \frac{GBP_{OL} * DR}{Power} = \frac{\frac{I_1}{nU_T C_L} * \frac{2*100U_T^2}{\frac{2nkT}{\beta C_L}}}{120U_T I_1} = 0.83 * \frac{\beta}{n^2 kT} \tag{2.14}$$

2.3 Two stage opamp with Miller compensation

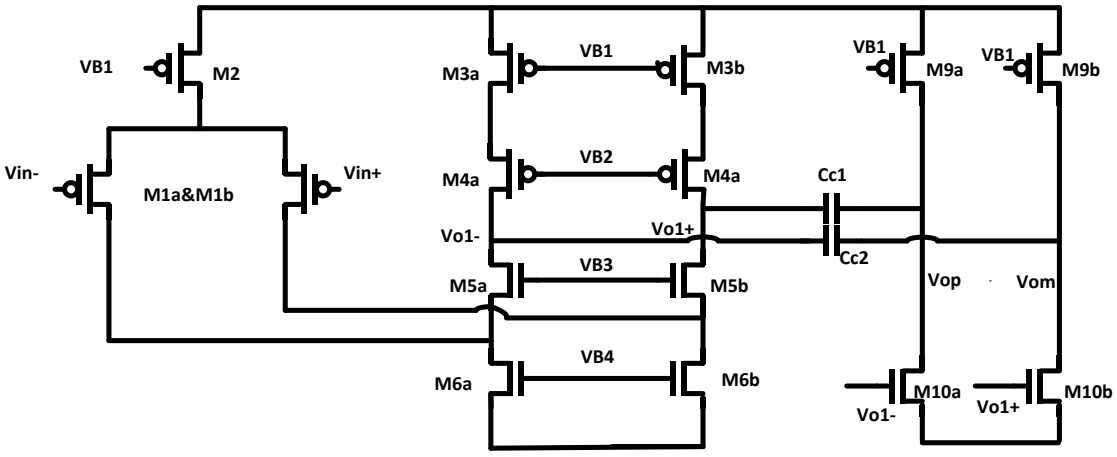


Figure 2.3 Schematic of two stage opamp with Miller compensation [33]

Input referred noise spectral density is given:

$$\overline{v_n^2} = \frac{4nkT}{g_{m1}}\left(1 + \frac{g_{m3} + g_{m6}}{g_{m1}}\right) \approx \frac{16nkT}{g_{m1}} \qquad \text{Assume } gm_1 = gm_3 \approx 1/2 gm_6 \tag{2.15}$$

$$GBP_{OL} = \frac{g_{m1}}{C_c} = \frac{I_1}{nU_T C_c} = 2 * GBP_{CL} \tag{2.16}$$

Output referred noise is:

$$\overline{v_{no}} = \frac{1}{\beta}\sqrt{\frac{16nkT}{g_{m1}}\frac{\pi}{2}\beta * GBP_{CL}} = \sqrt{\frac{1}{\beta^2}\frac{16nkT}{g_{m1}}\frac{\pi}{2}\beta\frac{g_{m1}}{2*2\pi C_c}} = \sqrt{\frac{2nkT}{\beta C_c}} \tag{2.17}$$

Because right plane zero equals non-dominant pole [40],

$$\omega_{non} \approx \frac{g_{m9}}{C_L} \approx \omega_z \approx \frac{g_{m9}}{C_C} \tag{2.18}$$

The non-dominant pole and right plane zero are set to 3.6*GBP_{OL},

$$\begin{aligned} \mathrm{PM} &= 360 - 180 - \tan^{-1}\frac{\mathrm{GBP_{CL}}}{\beta GBP_{CL}} - \tan^{-1}\frac{\mathrm{GBP_{CL}}}{xGBP_{OL}} - \tan^{-1}\frac{\mathrm{GBP_{CL}}}{\mathrm{x}GBP_{OL}} \\ &= 180 - 88 - 2\tan^{-1}\frac{\mathrm{GBP_{CL}}}{x\,GBP_{OL}} = 76 \end{aligned} \tag{2.19}$$

$$\begin{aligned} &1/2\mathrm{x} = \tan[\frac{(180-88-76)}{2}] = \tan(8) = 0.14 \\ &x = 3.6 \end{aligned} \tag{2.20}$$

$$\omega_{non} \approx \frac{g_{m9}}{C_L} = 3.6\frac{g_{m1}}{C_c} \tag{2.21}$$

$$g_{m9} = 3.6 g_{m1} \tag{2.22}$$

$$DR \propto \frac{\left(\frac{V_o}{\sqrt{2}}\right)^2}{\overline{v_{no}^2}} = \frac{\left(2*\frac{(V_{DD}-2*5U_T)}{\sqrt{2}}\right)^2}{\frac{2nkT}{\beta C_c}} = \frac{\left(2*\frac{(30U_T-2*5U_T)}{\sqrt{2}}\right)^2}{\frac{2nkT}{\beta C_c}} = \frac{2*400U_T^2}{\frac{2nkT}{\beta C_c}} \tag{2.23}$$

$$\mathrm{Power=VDD*(2I_1*2+2*3.6I_1)= 336U_TI_1} \tag{2.24}$$

$$FOM = \frac{GBP_{OL} * DR}{Power} = \frac{\frac{I_1}{nU_TC_c} * \frac{2*400U_T^2}{\frac{2nkT}{\beta C_c}}}{336U_TI_1} = 1.19 * \frac{\beta}{n^2kT} \tag{2.25}$$

2.4 Two stage opamp with indirect compensation

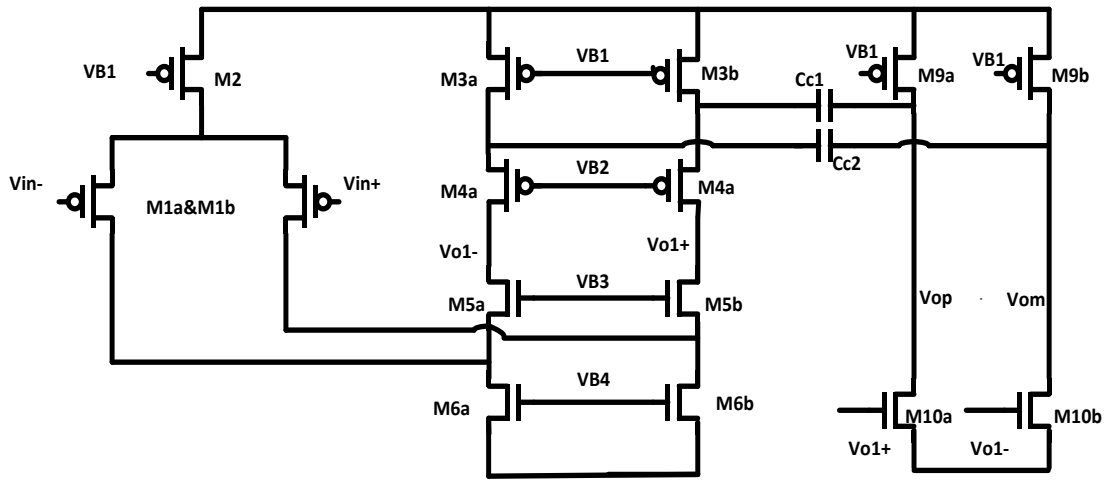


Figure 2.4 Schematic of two stage opamp with indirect compensation [40]

Input referred noise spectral density is given:

$$\overline{v_n^2} = \frac{4nkT}{g_{m1}}\left(1+\frac{g_{m3}+g_{m6}}{g_{m1}}\right) \approx \frac{16.8nkT}{g_{m1}} \quad \text{Assume } gm_3=1.1gm_1 \text{ and } gm_6=2.1gm_1 \tag{2.26}$$

$$GBP_{OL} = \frac{g_{m1}}{C_c} = \frac{I_1}{nU_T C_c} = 2 * GBP_{CL} \tag{2.27}$$

Output referred noise is:

$$\overline{v_{no}} = \frac{1}{\beta}\sqrt{\frac{16.8nkT}{g_{m1}}\frac{\pi}{2}\beta * GBP_{CL}} = \sqrt{\frac{1}{\beta^2}\frac{16.8nkT}{g_{m1}}\frac{\pi}{2}\beta\frac{g_{m1}}{2*2\pi C_c}} = \sqrt{\frac{2.1nkT}{\beta C_c}} \tag{2.28}$$

The non-dominant pole [40] equals $0.6*GBP_{OL}$,

$$\omega_{non} \approx \frac{g_{m9}C_c}{C_1(C_L+C_c)} = 0.6\frac{g_{m1}}{C_c} \tag{2.29}$$

Where C_1 is the capacitance of the node Vo1, assume C_1 equals $0.1C_c$,

$$g_{m9} = 0.12 g_{m1} \tag{2.30}$$

$$DR \propto \frac{\left(\frac{V_o}{\sqrt{2}}\right)^2}{\overline{v_{no}^2}} = \frac{\left(2*\frac{(V_{DD}-2*5U_T)}{\sqrt{2}}\right)^2}{\frac{2.1nkT}{\beta C_c}} = \frac{\left(2*\frac{(30U_T-2*5U_T)}{\sqrt{2}}\right)^2}{\frac{2.1nkT}{\beta C_c}} = \frac{2*400U_T^2}{\frac{2.1nkT}{\beta C_c}} \quad (2.31)$$

$$\text{Power}=\text{VDD}*(2*I_1+2*1.1I_1+2*0.12I_1) = 133.2U_TI_1 \quad (2.32)$$

$$FOM = \frac{GBP_{OL}*DR}{Power} = \frac{\frac{I_1}{nU_TC_c}*\frac{2*400U_T^2}{\frac{2.1nkT}{\beta C_c}}}{133.2U_TI_1} = 2.86*\frac{\beta}{n^2kT} \quad (2.33)$$

2.5 Two stage opamp with split length transistors compensation

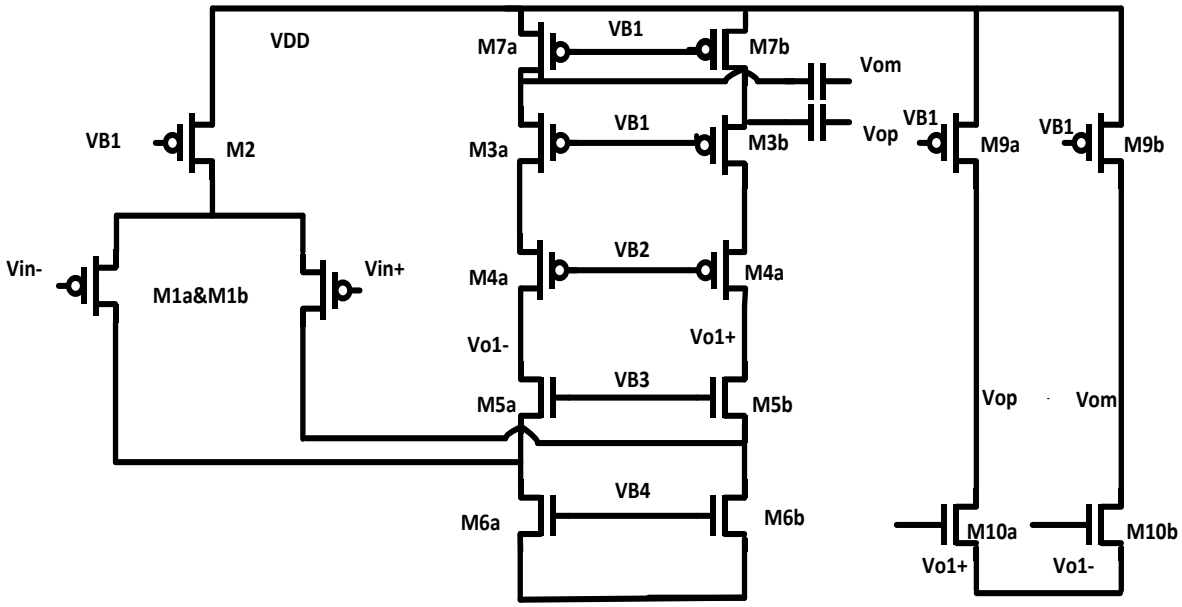


Figure 2.5 Schematic of two stage opamp with split length transistors compensation [40]

Input referred noise spectral density is given:

$$\overline{v_n^2} = \frac{4nkT}{g_{m1}}\left(1+\frac{g_{m3}+g_{m6}}{g_{m1}}\right) \approx \frac{12.4nkT}{g_{m1}} \quad \text{Assume } gm_3=0.55gm_1 \text{ and } gm_6=1.55gm_1 \quad (2.34)$$

$$GBP_{OL} = \frac{g_{m1}}{C_c} = \frac{I_1}{nU_TC_c} = 2*GBP_{CL} \quad (2.35)$$

Output referred noise is:

$$\overline{v_{no}} = \frac{1}{\beta}\sqrt{\frac{12.4nkT}{g_{m1}}\frac{\pi}{2}\beta * GBP_{CL}} = \sqrt{\frac{1}{\beta^2}\frac{12.4nkT}{g_{m1}}\frac{\pi}{2}\beta\frac{g_{m1}}{2*2\pi C_c}} = \sqrt{\frac{1.55nkT}{\beta C_c}} \tag{2.36}$$

The non-dominant pole [40] equals 0.6*GBP_{OL},

$$\omega_{non} \approx \frac{g_{m9}C_c}{2C_1C_L} = 0.6 * \frac{g_{m1}}{C_c} \tag{2.37}$$

Where C_1 is the capacitance of the node Vo1, assume C_1 equals $0.1C_c$

$$g_{m9} = 0.12 g_{m1} \tag{2.38}$$

$$DR = \frac{\left(\frac{V_o}{\sqrt{2}}\right)^2}{\overline{v_{no}^2}} = \frac{\left(2 * \frac{(V_{DD} - 2*5U_T)}{\sqrt{2}}\right)^2}{\frac{1.55nkT}{\beta C_c}} = \frac{\left(2 * \frac{(30U_T - 2*5U_T)}{\sqrt{2}}\right)^2}{\frac{1.55nkT}{\beta C_c}} = \frac{2*400U_T^2}{\frac{1.55nkT}{\beta C_c}} \tag{2.39}$$

$$\text{Power}=VDD*(2*I_1+2*0.55*I_1+2*0.12I_1)=100.2U_TI_1 \tag{2.40}$$

$$FOM = \frac{GBP_{OL} * DR}{Power} = \frac{\frac{I_1}{nU_TC_c} * \frac{2*400U_T^2}{\frac{1.55nkT}{\beta C_c}}}{100.2U_TI_1} = 5.15 * \frac{\beta}{n^2kT} \tag{2.41}$$

2.6 Two stage opamp with Miller p-z compensation

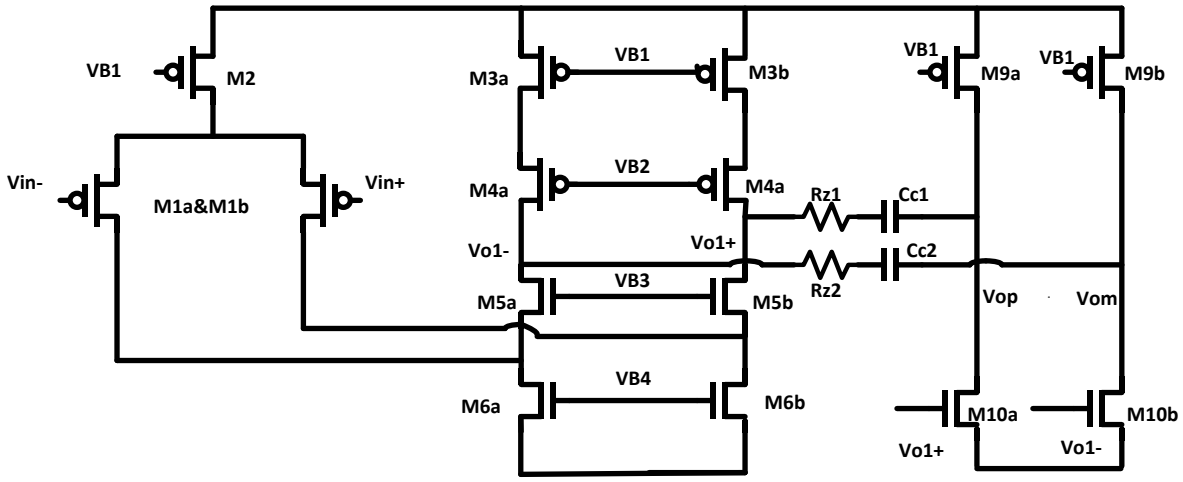


Figure 2.6 Schematic of two stage opamp with Miller p-z compensation [40]

Input referred noise spectral density is given:

$$\overline{v_n^2} = \frac{4nkT}{g_{m1}}\left(1+\frac{g_{m3}+g_{m6}}{g_{m1}}\right) \approx \frac{12nkT}{g_{m1}} \quad \text{Assume } gm_3=1/2gm_1 \text{ and } gm_3=1/3gm_6 \tag{2.42}$$

$$GBP_{OL} = \frac{g_{m1}}{C_c} = \frac{I_1}{nU_T C_c} = 2*GBP_{CL} \tag{2.43}$$

Output referred noise is:

$$\overline{v_{no}} = \frac{1}{\beta}\sqrt{\frac{12nkT}{g_{m1}}\frac{\pi}{2}\beta * GBP_{CL}} = \sqrt{\frac{1}{\beta^2}\frac{12nkT}{g_{m1}}\frac{\pi}{2}\beta\frac{g_{m1}}{2*2\pi C_c}} = \sqrt{\frac{1.5nkT}{\beta C_c}} \tag{2.44}$$

The non-dominant pole equals $0.6*GBP_{OL}$,

$$\omega_{non} \approx \frac{g_{m9}}{C_L} = 0.6\frac{g_{m1}}{C_c} \tag{2.45}$$

$$g_{m9} = 0.6g_{m1} \tag{2.46}$$

$$DR = \frac{\left(\frac{V_o}{\sqrt{2}}\right)^2}{\overline{v_{no}^2}} = \frac{\left(2*\frac{(V_{DD}-2*5U_T)}{\sqrt{2}}\right)^2}{\frac{1.5nkT}{\beta C_c}} = \frac{\left(2*\frac{(30U_T-2*5U_T)}{\sqrt{2}}\right)^2}{\frac{1.5nkT}{\beta C_c}} = \frac{2*400U_T^2}{\frac{1.5nkT}{\beta C_c}} \quad (2.47)$$

$$\text{Power}=\text{VDD}*(I_1*2+2*0.5I_1+2*0.6I_1)=126U_TI_1 \quad (2.48)$$

$$FOM = \frac{GBP_{OL}*DR}{Power} = \frac{\frac{I_1}{nU_TC_c}*\frac{2*400U_T^2}{\frac{1.5nkT}{\beta C_c}}}{126U_TI_1} = 4.23*\frac{\beta}{n^2kT} \quad (2.49)$$

Section 2.7 Sarpeshkar's modified OTA

Sarpeshkar's modified OTA is shown in Figure 1.4.

Input referred noise spectral density is given [16]:

$$\begin{aligned}\overline{v_n^2} &= \frac{1}{g_{m0}^2}\left(4nkTg_{m0}+4nkTg_{m11}+\frac{8kT}{R_1}\right)\\ &= \frac{4nkT}{g_{m0}}\left(1+\frac{g_{m11}}{g_{m0}}+\frac{2U_T}{I_0R_1}\right)\approx\frac{4nkT}{g_{m0}}\end{aligned} \quad (2.50)$$

$$GBP_{OL} = \frac{g_{m0}}{C_L} = \frac{I_0}{nU_TC_L} \quad (2.51)$$

Output referred noise is:

$$\overline{v_{no}} = \frac{1}{\beta}\sqrt{\frac{4nkT}{g_{m0}}}\sqrt{\frac{\pi}{2}\beta*GBP_{CL}} = \sqrt{\frac{1}{\beta^2}\frac{4nkT}{g_{m0}}\frac{\pi}{2}\beta\frac{g_{m0}}{2*2\pi C_L}} = \sqrt{\frac{nkT}{\beta 2C_L}} \quad (2.52)$$

The current of transistor M11 is negligible compared with I_0 and I_0R_1 should be higher than $20U_T$ to ensure the resistor noise contribution negligible.

Total current is:

$$2*(I_0+I_{11})\approx 2I_0 \quad (2.53)$$

Since the input neural signal range is 50-500uV, the minimum gain of first stage amplifier is 20; the maximum output signal amplitude is 10mV as a result U_T is included for output swing and the common mode variation is also U_T, the power supply VDD is given,

$$VDD=5*5U_T+ U_T + U_T +(I_0+ I_{11}) R_1\approx27U_T+I_0R_1\approx47U_T \quad (2.54)$$

$$Power=VDD*2I_0=94U_TI_0 \quad (2.55)$$

$$DR \propto \frac{\left(\frac{V_o}{\sqrt{2}}\right)^2}{\overline{v_{no}^2}} = \frac{\frac{V_O^2}{2}}{\frac{nkT}{\beta 2C_L}} = \frac{U_T^2}{\frac{nkT}{\beta C_L}} \quad (2.56)$$

FOM of Sarpeshkar's modified OTA is

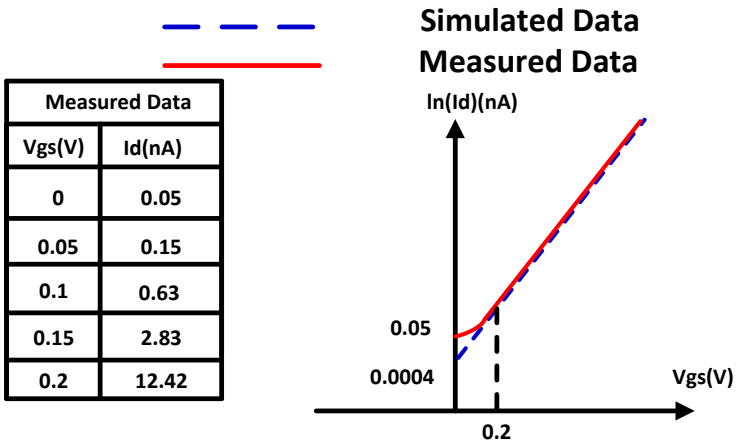
$$FOM_{Sarp} = \frac{GBP_{OL} * DR}{Power} = \frac{\frac{I_0}{nU_TC_L} * \frac{U_T^2}{\frac{nkT}{\beta C_L}}}{94U_TI_0} = 0.01 * \frac{\beta}{n^2kT} \quad (2.57)$$

Table 2.1 Comparison of Performance of OTA/Opamps

OTA architecture	Output Referred Noise	Output swing	Dynamic Range	Power	FOM
Telescopic OTA	$\sqrt{\frac{nkT}{\beta C_L}}$	$2*5U_T$	$\frac{2*25U_T^2}{\frac{nkT}{\beta C_L}}$	$60U_TI_1$	$0.83*\frac{\beta}{n^2kT}$
Folded cascade OTA	$\sqrt{\frac{2nkT}{\beta C_L}}$	$2*10U_T$	$\frac{2*100U_T^2}{\frac{2nkT}{\beta C_L}}$	$120U_TI_1$	$0.83*\frac{\beta}{n^2kT}$
Two stage opamp with Miller compensation	$\sqrt{\frac{2nkT}{\beta C_c}}$	$2*20U_T$	$\frac{2*400U_T^2}{\frac{2nkT}{\beta C_c}}$	$336U_TI_1$	$1.19*\frac{\beta}{n^2kT}$
Two stage opamp with indirect compensation	$\sqrt{\frac{2.1nkT}{\beta C_c}}$	$2*20U_T$	$\frac{2*400U_T^2}{\frac{2.1nkT}{\beta C_c}}$	$133.2U_TI_1$	$2.86*\frac{\beta}{n^2kT}$
Two stage opamp with split length compensation	$\sqrt{\frac{1.55nkT}{\beta C_c}}$	$2*20U_T$	$\frac{2*400U_T^2}{\frac{1.55nkT}{\beta C_c}}$	$100.2U_TI_1$	$5.15*\frac{\beta}{n^2kT}$
Two stage opamp with Miller p-z compensation	$\sqrt{\frac{1.5nkT}{\beta C_c}}$	$2*20U_T$	$\frac{2*400U_T^2}{\frac{1.5nkT}{\beta C_c}}$	$126U_TI_1$	$4.23*\frac{\beta}{n^2kT}$
Sarpeshkar's modified OTA	$\sqrt{\frac{nkT}{2\beta C_L}}$	U_T	$\frac{U_T^2}{\frac{nkT}{\beta C_L}}$	$94U_TI_1$	$0.01*\frac{\beta}{n^2kT}$

Table 2.1 summarizes the FOM comparisons of OTA/Opamps. From the Table 2.1, two stage Opamp with split length compensation has the best FOM and Sarpeshkar's modified OTA has the lowest FOM due to its limited output swing. From equation (2.52), Sarpeshkar's modified OTA can achieve the lowest output referred noise, however, the drawbacks of Sarpeshkar's modified OTA are: 1) for the input power@-6dBm, power harvester can achieve raw VDD 1.1V with output load current 70μA [28], after Low Dropout Regulator (LDO) we can only get power supply less than 0.9V. Power supply VDD of Sarpeshkar's modified OTA needs to be higher than $45U_T \approx 1.1V$, which frequently requires to increase the number of stages rectifier resulting in

reducing harvester efficiency; 2) the ratio of I_{11}/I_0 should be less than 1/10 to ensure the noise contribution of M11 is negligible, for I_0 equals 100nA, I_{11} needs to be less than 10nA, this is not practical from measurement data. Figure 2.7 shows the simulated and measured subthreshold current of NMOS transistor with width/length 9.92um/2.2um, we can see the measured leakage current is higher than simulated current when Vgs is less than 200mV, which proves the bias current less than 10nA is not practical. For the 1st stage neural amplifier's requirement of low noise, low power and no strict constraint of output swing, Telescopic OTA is the best choice.



Measured Data	
Vgs(V)	Id(nA)
0	0.05
0.05	0.15
0.1	0.63
0.15	2.83
0.2	12.42

Figure2.7 Simulated and measured subthreshold current

Table 2.2 summarizes three different two stage opamp topologies with first stage telescopic, folded cascoded and Sarpeshkar's modified OTA, two stage opamp with Miller compensation is not discussed in Table 2.2 due to its right plane zero degrading PM and high power consumption. With Sarpeshkar's modified OTA input stage, two stage opamp topologies may achieve the lower noise but higher power consumption than telescopic and folded cascode stage; however, due to non-availability of realization of closed loop PM of 76 degree, these telescopic and Sarpeshkar's modified OTA stage topologies are very difficult to be implemented in closed loop applications. Additionally, Sarpeshkar's modified OTA needs higher VDD for operation, which is not feasible for our low voltage design.

Table 2.2 Comparisons of two stage opamps with telescopic, folded cascode and Sarpeshkar's modified OTA input stage

	Noise	Closed loop PM@76 Feasibility	Power
2 stage opamp with indirect compensation with telescopic stage	$\sqrt{\frac{nkT}{\beta C_c}}$	No	$67.2U_TI_1$
2 stage opamp with indirect compensation with folded cascode stage	$\sqrt{\frac{2.1nkT}{\beta C_c}}$	Yes	$133.2U_TI_1$
2 stage opamp with indirect compensation with Sarpeshkar's modified OTA	$\sqrt{\frac{nkT}{2\beta C_c}}$	No	$282U_TI_1$
2 stage opamp with split length compensation with telescopic stage	$\sqrt{\frac{nkT}{\beta C_c}}$	No	$918U_TI_1$
2 stage opamp with split length compensation with folded cascode stage	$\sqrt{\frac{1.55nkT}{\beta C_c}}$	Yes	$100.2U_TI_1$
2 stage opamp with split length compensation with Sarpeshkar's modified OTA	$\sqrt{\frac{nkT}{2\beta C_c}}$	No	$282U_TI_1$
2 stage opamp with Miller p-z compensation with telescopic stage	$\sqrt{\frac{nkT}{\beta C_c}}$	No	$96U_TI_1$
2 stage opamp with Miller p-z compensation with folded cascode stage	$\sqrt{\frac{1.5nkT}{\beta C_c}}$	Yes	$126U_TI_1$
2 stage opamp with Miller p-z compensation with Sarpeshkar's modified OTA	$\sqrt{\frac{nkT}{2\beta C_c}}$	No	$150.4U_TI_1$

2.8 Neural amplifier design

The neural amplifier system block diagram is shown in Figure 2.8. The neural amplifier includes two stages: a bandpass stage and a gain stage. The bandpass amplifier which utilizes a fully differential structure is based on Harrison's capacitive and resistive feedback method [15]. The lower 3dB frequency is determined by the feedback capacitor and current biased Pseudo resistor [18, 37]. A fully differential approach is selected to improve common mode rejection and reduce distortion. Because the input neural signal (50-500μV) is much less than a few thermal voltages (26mV) there is no slew rate limitation for either amplifier design. The midband gain of neural amplifier is 58.6dB with a 3dB bandwidth from 500 to 8 kHz. The input referred noise is $10\mu V_{rms}$ with power supply of 0.7V.

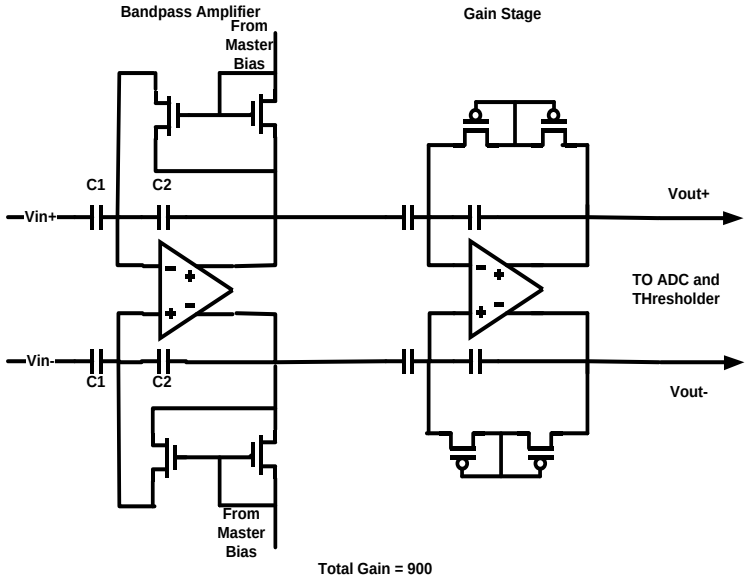


Figure 2.8 Neural Amplifier system block diagram, first stage with current programmable band pass function and stage two gain function.

2.8.1 Stages for Power consumption, Area and Gain

Amplifier gain, K is set by the ratio of the input capacitance and feedback capacitance (C_1/C_2) with the lower 3dB frequency given by:

$$f_{low} = \frac{1}{2\pi \cdot R_2 \cdot C_2} \tag{2.59}$$

Because R_2 is inversely proportional to the current through the Pseudo resistor mirror, then the lower 3dB frequency is made tunable by trimming the scaled down current from the master bias circuit. The higher 3dB frequency is set by OTA loading and given by:

$$f_{high} = \frac{g_m}{2\pi \cdot \left[K(C_2 + C_L) + C_L + C_{gs} + C_L C_{gs}/C_2\right]} \tag{2.60}$$

where gm is the transconductance of the differential amplifier, gain per stage K equal C_1/C_2, R_2 is the resistance of the pseudo resistor, C_{gs} is the gate capacitance of input pair and C_L is the amplifier load capacitance, i e. stage 2 OTA or ADC.

In this application, low power and low area consumption are both important. This makes optimizing the number of amplifier stages very important. Assuming the OTA of each stage is a folded cascode structure with equal gains K, and gain bandwidth products:

$$BW = \frac{g_m}{2\pi C_{leff}} = \frac{g_m}{2\pi K(K+2)C_2} = \frac{GBP}{(K+1)} \tag{2.61}$$

$$C_{leff} = K(C_L + C_2) + C_L = K(K+2)C_2, C_L = C_1 = KC_2 \tag{2.62}$$

The bandwidth shrinkage of n stages is [38]:

$$\left|A(1+ j\omega\tau)\right| = \frac{1}{\left|(1+ j\omega\tau)\right|^n} = \frac{1}{\sqrt{2}} \tag{2.63}$$

Solving for ω and n>2

$$\omega_{amplifier} = \frac{1}{\tau}\sqrt{2^{\frac{1}{n}} - 1} noting\, 2^{\frac{1}{n}} \approx 1 + \frac{1}{n}\ln(2) \tag{2.64}$$

$$\omega_{amplifier} = \frac{1}{\tau}\sqrt{\frac{1}{n}Ln(2)} = \frac{0.833}{\tau}\frac{1}{\sqrt{n}} = \omega_{3dB}\frac{0.833}{\sqrt{n}} \tag{2.65}$$

Substitute ω into total power consumption [37] :

$$P \propto \frac{2\pi n * \sqrt[n]{G_T}(\sqrt[n]{G_T} + 2)}{(\sqrt[n]{G_T} + 1)} * \frac{0.833}{\sqrt{n}} \tag{2.66}$$

where n is the number of amplifier stages, C_{leff} is the effective load capacitance, GBP is the open loop gain bandwidth product, G_T is total required gain of neural amplifier, $\omega_{amplifier}$ is the bandwidth of neural amplifier, ω_{3dB} is the bandwidth of each stage amplifier. Taking G_T equal 900, and identical ω_{3dB} and gain K for all stages, n=2, 3, 4, the total power consumption can be found. Continuing this approach, we can derive the optimal number of stages for the power area product:

$$P\,\&\,Area \propto \frac{2\pi n^2 * \sqrt[n]{G_T}(\sqrt[n]{G_T} + 2)}{(\sqrt[n]{G_T} + 1)} * \frac{0.833}{\sqrt{n}} \tag{2.67}$$

Normalizing and plotting of (2.67), Figure 2.9 shows the optimal number of stages is 3 to 4. Considering that each stage should have a gain greater than 10 to ensure noise contributions for following stages is negligible, and the G_T requirement is 900, a 2 stage amplifier with a gain of 30 per stage was selected. The 1st stage OTA sets amplifier bandwidth and noise and the second stage OTA maintains gain and noise performance while ensuring high output swing. From post layout of two stage neural amplifier, the area of 1st stage is only 10% larger than that of 2nd stage, which is ensuring our previous assumption.

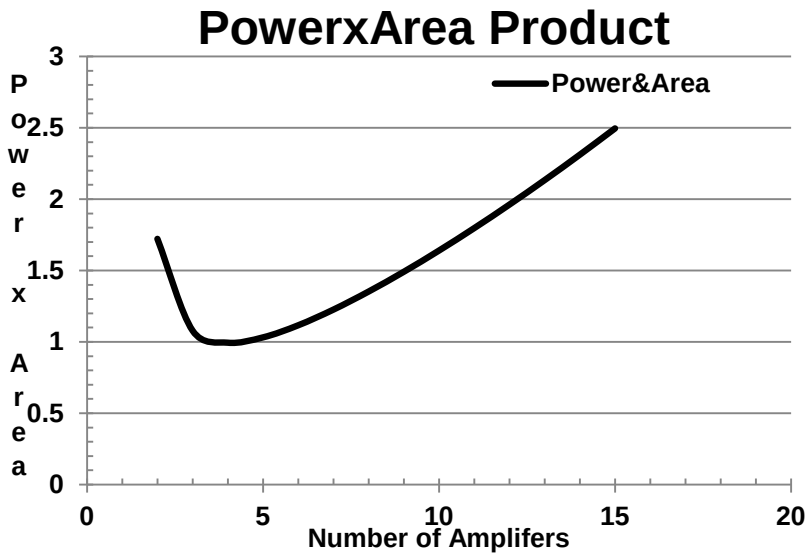


Figure 2.9 Plot of normalized power area product for different number of stages.

2.8.2 Noise Analysis and Sizing

The schematic of the 1st stage OTA including the common mode feedback (CMFB) circuit is shown in Figure 2.10. The main contributors to input referred OTA noise are the input pairs and NMOS current sources. PMOS differential pairs are selected due to their lower 1/f noise properties [40]. The geometries of the transistors for the first and second OTA are shown in Table 2.3.

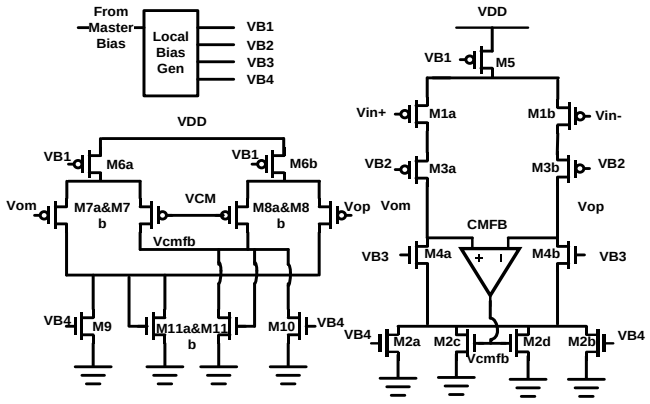


Figure 2.10 Schematic diagram of stage one OTA with its common mode feedback circuit [40].

As a result of source degeneration, cascode transistors make no significant noise contributions to OTA. The rail side NMOS transistors and differential pair should be made as large to as practical to minimize flicker noise. The spectral density of input thermal noise voltage is written as [40]:

$$\overline{v_{ni,thermal}^2} = \frac{4nkT}{g_{m1}}\left(1+\frac{g_{m2}}{g_{m1}}\right) \approx \frac{8nkT}{g_{m1}} \tag{2.68}$$

where gm_1 is the transconductance of input pair, gm_2 is the transconductance of NMOS current sources, n is slope factor in subthreshold operation, k is Boltzmann's constant and T is the absolute temperature, the input thermal noise voltage is shown:

$$\overline{v_{ni,thermal}} \approx \sqrt{\frac{8nkT}{g_{m1}} * \frac{\pi}{2} \frac{g_{m1}}{2*2\pi K(C_L+C_2)}} = \sqrt{\frac{nkT}{K(C_L+C_2)}} \tag{2.69}$$

The input flicker noise of the OTA is:

$$\overline{v_{ni,flicker}} = \sqrt{2Ln(B)\left(\frac{K_{flicker,p}}{W_1 L_1 C_{oxp}} + \frac{K_{flicker,n}}{W_{2a,2b} L_{2a,2b} C_{oxn}} + \frac{K_{flicker,n}}{W_{2c,2d} L_{2c,2d} C_{oxn}}\right)} \tag{2.70}$$

where W, L, C_{ox} take on their usually meaning for M1 and M2; $K_{flicker,n}$ and $K_{flicker,p}$ are process-dependent constants and B is the 3dB bandwidth.

The total input-referred noise is:

$$\begin{aligned}\overline{v_{ni,total}} &\approx \sqrt{\frac{nkT}{K(C_L+C_2)} + 2Ln(B)\left(\frac{K_{flicker,p}}{W_1 L_1 C_{oxp}} + \frac{K_{flicker,n}}{W_{2a,2b} L_{2a,2b} C_{oxn}} + \frac{K_{flicker,n}}{W_{2c,2d} L_{2c,2d} C_{oxn}}\right)} \\ &\approx \sqrt{2Ln(B)\left(\frac{K_{flicker,n}}{W_{2a,2b} L_{2a,2b} C_{oxn}} + \frac{K_{flicker,n}}{W_{2c,2d} L_{2c,2d} C_{oxn}}\right)}\end{aligned} \tag{2.71}$$

The noise contributions of transistors in the first OTA are summarized in Table 2.3. From the noise simulation, the flicker noise of NMOS current source dominates the total input-referred noise.

Table 2.3 Noise contribution of transistors in first OTA

Transistors	Contributions (Flicker/Thermal noise)
M2c&M2d	40.02%/8.36%
M2a&M2b	19.26%/9.3%
M1a&M1b	1.08%/13.74%

The schematic of the 2nd stage opamp including the CMFB circuit as well as their geometries are shown in Figure 2.11 and Table 2.4 respectively. Due to high output swing requirements of the second stage is a 2 stage folded cascode structure employing split length compensation for its highest FOM, as its main contribution is signal swing and not signal fidelity. BP2 requires Cc equals 2.5pF the maintain 10 bit accuracy and I_{diff} equals 276.9nA for sufficient bandwidth.

The voltage divider of Vop and Vom, the resistance of RC network in the CMFB circuit needs to be large enough to ensure the gain of OTA is not degraded and does not introduce distortion in the OTA. When Vop > Vom, M15b and M15d are off, M15a and M15c are diode connected, according to linear pseudo-Ohm's law [38]:

$$I_{DS} = G^*(V_D^* - V_S^*) \tag{2.72}$$

$$G^* = \frac{1}{R^*} = \frac{I_S}{V_0}\exp(\frac{V_G - V_{T0}}{nU_T}) \tag{2.73}$$

where R* and G* are the pseudo resistance and pseudo conductance between Vop, Vom and V_{osum}, and are the pseudo voltages, I_S is the specific current, V_{T0} is the threshold voltage of transistors M15, V_G is the gate voltage and V_0 is the arbitrary scaling voltage. For I_S equal 100nA,

U_T at room temperature and n equal 2, R* is estimated using I_{OFF} in the configuration providing common mode summing for the CMFB circuit, while requiring sufficient area to control mismatch error.

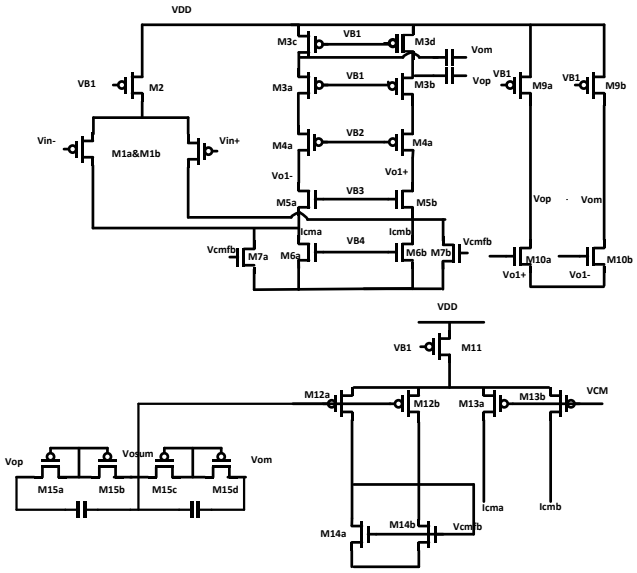


Figure 2.11 Schematic diagram of stage two opamp with its common mode feedback circuit.

Table 2.4 Geometries of transistors in first and second OTA/opamp

1st OTA		2nd OTA	
Devices	W/L(μm)	Devices	W/L(μm)
M1a&M1b	40/1.6	M1a&M1b	13.3/2
M2a&M2b	24/4.4	M2	60/4
M2c&M2d	26.4/2.4	M3a&M3b	24/4
M3a&M3b	40/1.6	M4a&M4b	8/0.6
M4a&M4b	96/2.2	M5a&M5b	6.4/2.5
M5	238.08/1.6	M6a&M6b	18/12
M6a&M6b	39.68/1.6	M7a&M7b	6.4/3
M7a&M7b M8a&M8b	9.92/1.6	M8a&M8b	8/3
M9&M10	8/4.4	M9a&M9b	264/4
M11a&M11b	8.8/2.4	M10a&M10b	2/3
		M11	96/4
		M12a&M12b	10/1
		M13a&M13b	6.4/3
		M14a&M14b	3.6/2
		M15a&M15b M15c&M15d	2/8

2.9 Performance Summary of Neural Amplifier

Table 2.5 Simulated Performance of Neural Amplifier

	Midband Gain	**f_low _3dB**	**f_high_ 3dB**	**Input referred noise**	**Total Harmonic Distortion**	**Power Consumption**	**Power Supply**
Stage 1	30.2dB	625Hz	12kHz	9.4uV	0.1%	0.76uW	0.7V
Stage 2	30.2dB	250Hz	11.6kHz	47.7uV	0.28%	0.67uW	0.7V
Two Stages	58.6dB	560Hz	8kHz	10uV	0.3%	1.81uW	0.7V

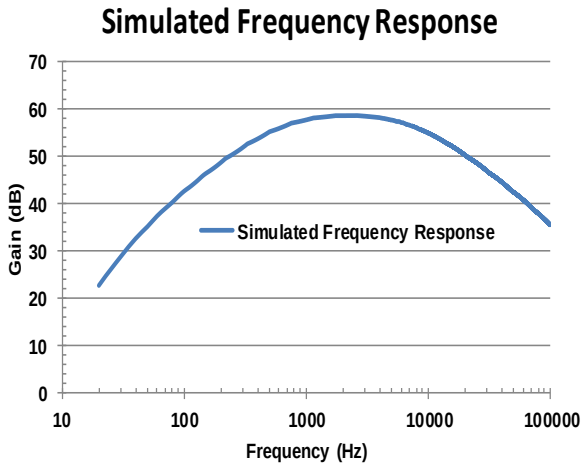


Figure 2.12 Simulated frequency response of two stage neural amplifier

Figure 2.12 shows the simulated neural amplifier frequency response. The midband gain is 58.6dB and the cutoff frequency is from 500Hz to 8 kHz. Input-referred noise is 10μVrms and Total Harmonic Distortion for both stages referred to the input stage is 0.3%. The performances of neural amplifier are summarized in Table 2.5.

2.10 Conclusion

In this chapter we reviewed seven different OTA/Opamps topologies and developed the FOM comparisons in the subthreshold application. From above comparisons, 2 stage OTA with split length compensation has the highest FOM. For the 1st stage neural amplifier design, single stage Telescopic OTA is selected for its low power and low noise advantage; for the second stage neural amplifier, 2 stage opamp with split length compensation is selected for its highest FOM. The optimized stage for power, area and gain is discussed to ensure the lowest power and area products. Because 1st stage neural amplifier sets the noise floor, the noise analysis of 1st stage OTA is investigated. The simulation result of neural amplifier is summarized in the end.

CHAPTER III

REVIEW OF ADC POWER CONSUMPTION AND PIPELINED ADC DESIGN

There are five sections in this chapter: ADC power consumption comparison, 8 bit Pipelined ADC design, MDAC (Multiplying Digital to Analog Converter) errors analysis, full Pipelined ADC simulation results and conclusion. Section 3.1 presents the three ADC power consumptions comparisons for neural recording applications; section 3.2 introduces Pipelined ADC design with the system structure and details of building blocks; in section 3.3 MDAC errors resulting in the degradation of performance of ADC will be discussed; complete Pipelined ADC simulation results will be presented in the section 3.4; section 3.5 summarizes the chapter.

As a result of the limited power requirements for neural signal recording, minimization power consumption in ADC is very important. There are three prominent ADC architectures: Pipelined ADC, Successive Approximation (SAR) ADC and Sigma Delta ADC. A SAR ADC is limited due to the the number of unit capacitor growing exponentially [41-47]; Sigma Delta ADC increases the effective input capacitance by the oversampling constrain utilizing extra bandwidth in its application [48-54]. For simplicity of understanding and comparison, we compare the increased power consumption of second stage neural amplifier required to drive the effective load capacitance of the different ADCs.

3.1 ADC power consumption comparison

3.1.1 Pipelined ADC power consumption

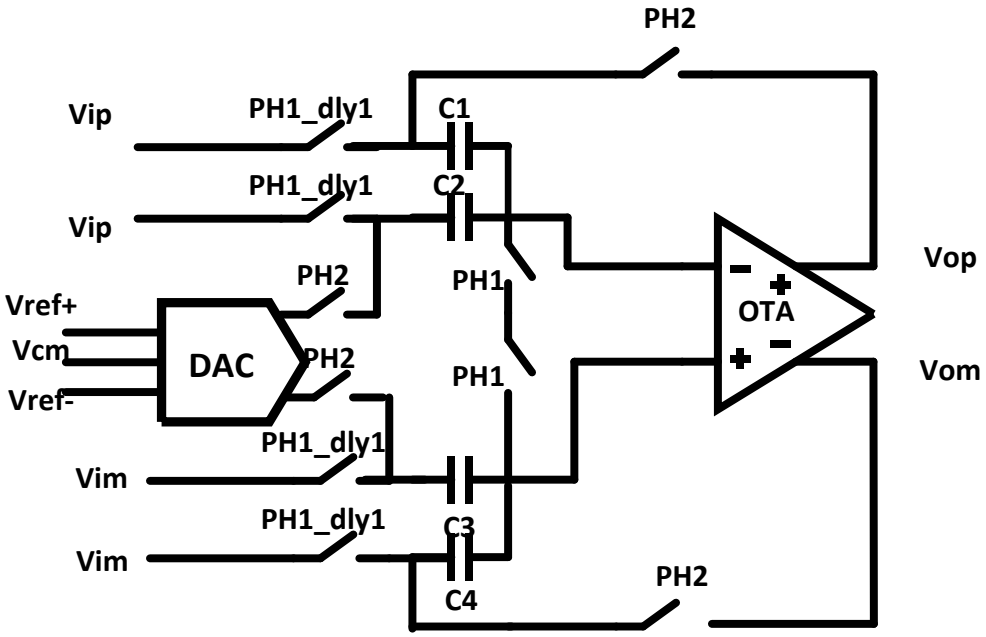


Figure 3.1 Schematic of 1.5 bit MDAC [55]

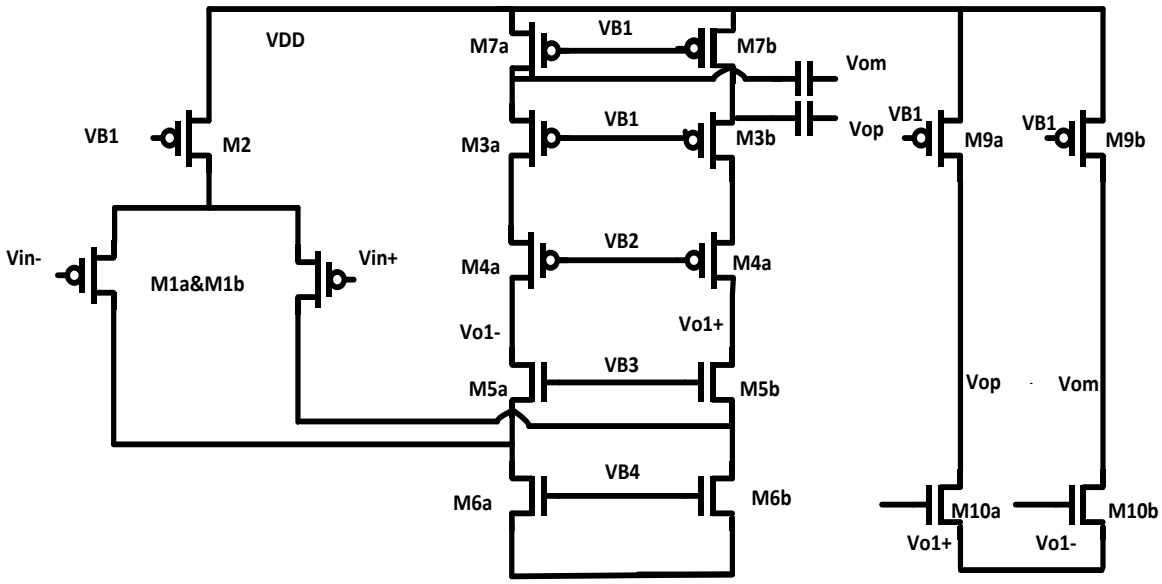


Figure 3.2 Schematic of two stage opamp with split length transistors compensation [40]

First the power comparison of Pipelined ADC is discussed. The schematic of a 1.5 bit MDAC is shown in Figure 3.1. The opamp used in 1.5 bit MDAC is shown in Figure 3.2. It will be assumed every stage in Pipelined ADC uses 1.5 bit MDAC and each MDAC uses a two stage split length transistors compensation opamp. For ease of presentation the power analysis below is based on single sided operation.

During PH1, the noise voltage sampled on the capacitors is:

$$v_{n1}^2 = \frac{KT}{C_1 + C_2} \tag{3.1}$$

The total noise charge is q^2_{n1} equals $v^2_{n1}(C_1+C_2)^2$. During PH2, the noise charge is transferred to the feedback capacitor and the output thermal noise from sampling switches is [55]:

$$v_{out,n1}^2 = \frac{q_{n1}^2}{C_1^2} = \frac{KT(C_1 + C_2)}{C_1^2} = \frac{2KT}{C_1} \tag{3.2}$$

During PH2, thermal noise is given by section 2.5

$$v_{out,n2}^2 = \frac{3.1nKT}{C_c} \tag{3.3}$$

The total noise of output is:

$$v_{out,tot} = \sqrt{v_{out,tot}^2} = \sqrt{v_{out,n1}^2 + v_{out,n2}^2} = \sqrt{\left(\frac{2KT}{C_1} + \frac{3.1nKT}{C_c}\right)} \tag{3.4}$$

To preserve 10 bit resolution with capacitor mismatch consideration, C_1 and C_c are selected as 180f and 237f respectively. After the sampling capacitor size of the 1st stage MDAC is known, the power consumption of the second stage amplifier (BP2) may be calculated. From the neural amplifier specification (See Section 2.8), BP2 requires Cc equal 2.5pF to maintain 10 bit

accuracy with I_{diff} equal 277nA to insure sufficient bandwidth. The non-dominant pole of BP2 is found to be $0.6*GBP_{OL}$ as outlined in section 2.5 and C_L from equation (3.4) equals 360fF ($2xC_1$), and the current of second stage of BP2 equals $0.01I_{diff.}$

The total current of opamp in BP2 is,

$$2I_{diff}*(1+0.55+0.01) =3.12*I_{diff}=864nA \quad (3.5)$$

The diff pair current of opamp in 1st stage MDAC needs to be 5.4nA to maintain 10 bit settling accuracy (see settling error in section 3.3.2). The total current of opamp is,

$$2I_{diff}*(1+0.55+0.18) =3.46*5.4nA=18.7nA \quad (3.6)$$

As a result total opamp current for the 7 stages Pipelined ADC without scaling down is,

$$18.7nA*7=131nA \quad (3.7)$$

While with scaling total pipelined ADC currents approaches 38nA. With each MDAC having a pair of comparators current of consuming 1nA, the combined current of BP2 and the Pipelined ADC combined is approximated as

$$864nA+131nA+1nA*8=1003nA \quad (3.8)$$

With scaling total current approaches 910nA or only a 10% improvement.

3.1.2 Sigma-Delta ADC power consumption

The switched-capacitor implementation of an integrator is shown in Figure 3.3.

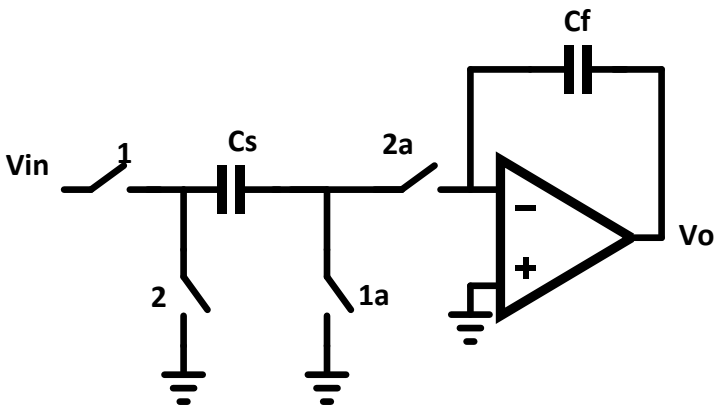


Figure 3.3 Switched-capacitor implementation of an integrator [61]

It will be assumed that Sigma-Delta ADC use similar split length transistors compensation opamp architecture in Pipelined ADC and half of fully differential version is analyzed. The SNR of Sigma-Delta modulator loop is based on oversampling ratio (OSR) modulator order O and a B-bit quantizer [61],

$$SNR_{\Delta-\Sigma} = (20O+10)\log OSR + 10\log(2O+1) + 6.02B + 1.76 - 9.94O \quad (3.9)$$

The two stage modulator architecture utilizing OSR equals 32 with 1-bit quantize ensuring greater than 12 architectural bits thus allowing the thermal noise floor to rise to 10 bits.

The first integrator dominates the overall system noise floor, assume the first loop coefficient is fulfilled by C_F (C_F=C_s). The integrator noise floor is dominated by the size of its sampling capacitor C_s [61].

$$V_{n,sample} = \sqrt{\frac{2kT}{C_s}} \quad (3.10)$$

With the use of oversampling in the modulator design, the sampling capacitor can be scaled down and sampling noise can be modified as

$$V_{n,sample} = \sqrt{\frac{2kT}{OSR * C_s}} \tag{3.11}$$

Thermal noise of the opamp is given in section 2.5 as;

$$V_{n,integ} = \sqrt{\frac{1.55nkT}{OSR * \beta * C_{c1}}} \tag{3.12}$$

The thermal noise of BP2 is also reduced by oversampling technique so the compensation capacitor in BP2 can also be scaled down,

$$V_{n,BP2} = \sqrt{\frac{1.55nkT}{OSR * \beta * C_{c2}}} \tag{3.13}$$

The total output noise is

$$v^2_{out,tot} = v^2_{n,sample} + v^2_{n,integ} + v^2_{n,BP2} \tag{3.14}$$

To preserve 10 bit resolution considering capacitor mismatch the noise from sampling may now be considered negligible, C_s is selected as 180fF. Assuming an ideal Sigma-Delta the noise contribution of Cc_1 is neglected and Cc_2 selected to minimize power consumption of BP2. C_s and Cc_2 are selected as 180fF and 137fF respectively. BP2 must have a bandwidth that is 32X higher (25X for 3rd order) with an 180fF load (single sided) where I_{diff} equals 485.4nA providing sufficient settling bandwidth. The total current of BP2 is calculated as in Pipelined ADC section 3.1.1;

$$2I_{diff}(1+0.55+0.16)=3.42*485nA=1660nA \tag{3.15}$$

for either a 2nd and 3rd order Sigma Delta. Since the increased power consumption of BP2 required to driving the Sigma-Delta ADC is significantly higher than the 1uA required to drive the pipelined ADC, there is no need to consider the power consumption of Sigma-delta ADC.

3.1.3 SAR ADC power consumption

The schematic of SAR ADC is shown in Figure 3.4.

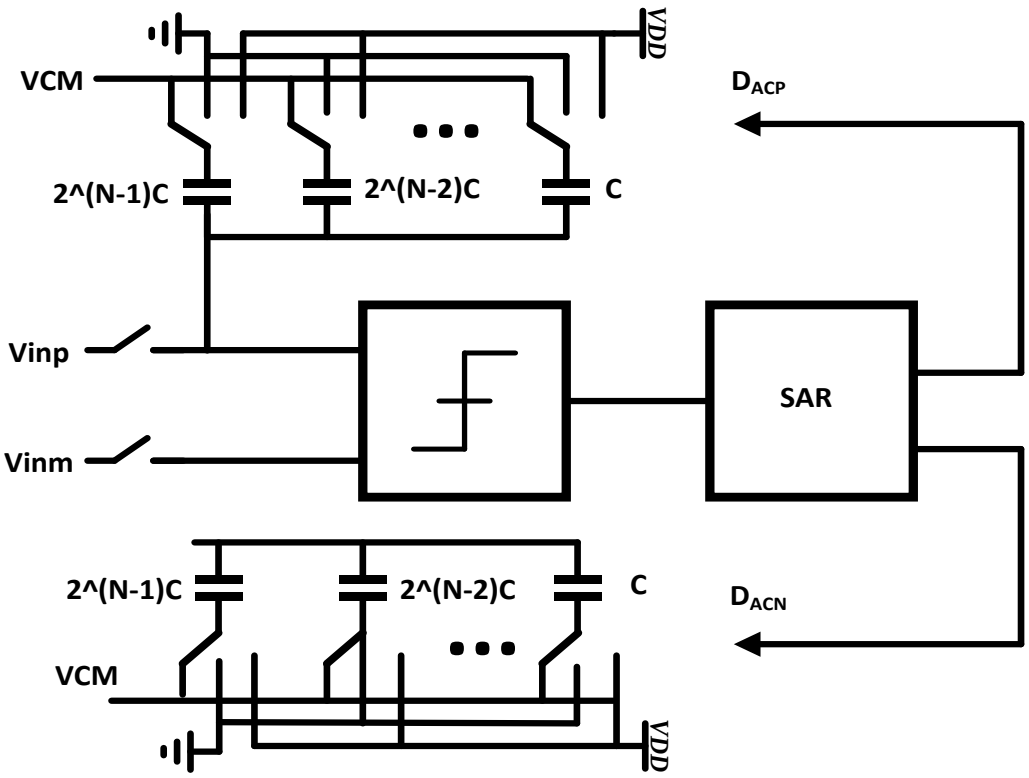


Figure 3.4 Schematic of SAR ADC [41]

The single side analysis is presented for ease in comparison. The core comparator noise is given by [41]:

$$v_{n,comp} = \sqrt{\frac{4nKT}{g_m} * \frac{g_m}{2 * 2\pi Cp} \frac{\pi}{2}} = \sqrt{\frac{nkT}{2Cp}} < \frac{V_{FS}}{2^{n+1}} \tag{3.16}$$

Where C_p is unit capacitor. C_p is selected as 54fF to preserve a 10 bit accuracy and the total capacitance of capacitor arrays $C_{p,total}$ equals 13.9pF.

The power consumption of BP2 driving SAR ADC is calculated as presented in Pipelined ADC section 3.1.1, total BP2 current is calculated as,

$$2I_{diff}(1+0.55+0.67)=4.44*I_{diff}=1229nA \quad (3.17)$$

Since the increased power consumption of BP2 as result of driving SAR ADC significantly greater than the pipelined ADC, there is no need to consider the power consumption of SAR ADC.

The comparison in power consumption for BP2 driving the three ADCs types is summarized in Table 3.1. The power consumption of BP2 driving Pipelined ADC with the addition of Pipelined ADC is the lowest. Therefore, Pipelined ADC is considered the best choice for the low power low voltage neural application.

Table 3.1 Power Consumption Comparison of three ADCs

	Pipelined ADC	Sigma-Delta ADC	SAR ADC
Power Consumption	1003nA	1660nA	1229nA

3.2 Pipelined ADC design

Pipelined ADCs are widely used in nyquist rate sampling applications with high throughput rate and MDAC is the most critical block [55-57]. It includes several cascaded stages and in each stage, there is a sample and hold network, a sub-ADC, a sub DAC (Digital to Analog converter), a subtractor and an inter-stage gain amplifier. The operation fundamental is as follow: The sampled input is first quantized by the sub ADC and generates digital code for this stage. Then the digital code is converted to analog signal by the sub DAC, which will be subtracted from the input signal. The resulting residue is amplified and passed to the next stage. The overall resolution of the Pipelined ADC is the sum of the number of bits of each stage. The throughput rate of the Pipelined ADC is the same as each stage.

There are several advantages of Pipelined ADC [58, 59]: 1) the complexity of circuitry increases linearly with the converter's resolution, unlike the flash ADC increasing exponentially with

resolution. 2) The throughput rate doesn't change with the number of stages because of pipelining. 3) Digital correction reduces the pipelined ADC's sensitivity in the sub ADC, which makes the design of comparators in sub ADC easier.

The system block diagram of Pipelined ADC is shown in Figure. 3.5 [62, 63]. The 8 bit Pipelined ADC with sampling frequency at 16 kHz is comprised of a 2.5 bit front end followed by five 1.5 bit stage MDACs. Each stage is driven by the two non-overlapping clock1 and clock2 and digital output is processed by digital correction logic to the final outputs. In the following, the main building blocks design of Pipelined ADC will be described.

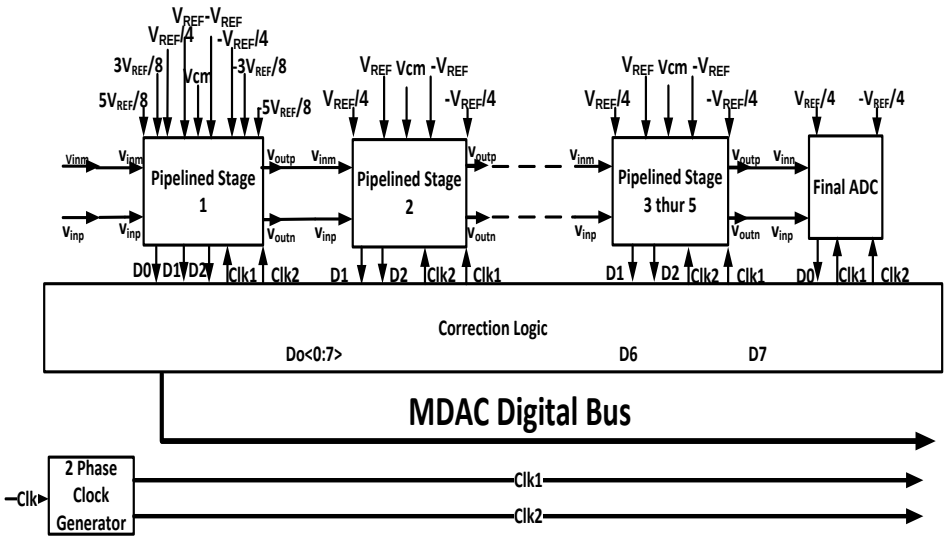


Figure 3.5 Block Diagram of Pipelined ADC.

3.2.1 1.5 bit MDAC with low input drift voltage

For ease of presentation, 1.5 bit MDAC is discussed in the following. The 1.5 bit MDAC architecture is shown in Figure 3.6. The Fully Differential (FD) configuration and Correlated Double Sampling (CDS) techniques [68] are applied to reduce the nonlinear distortion but with a tolerable increase in power.

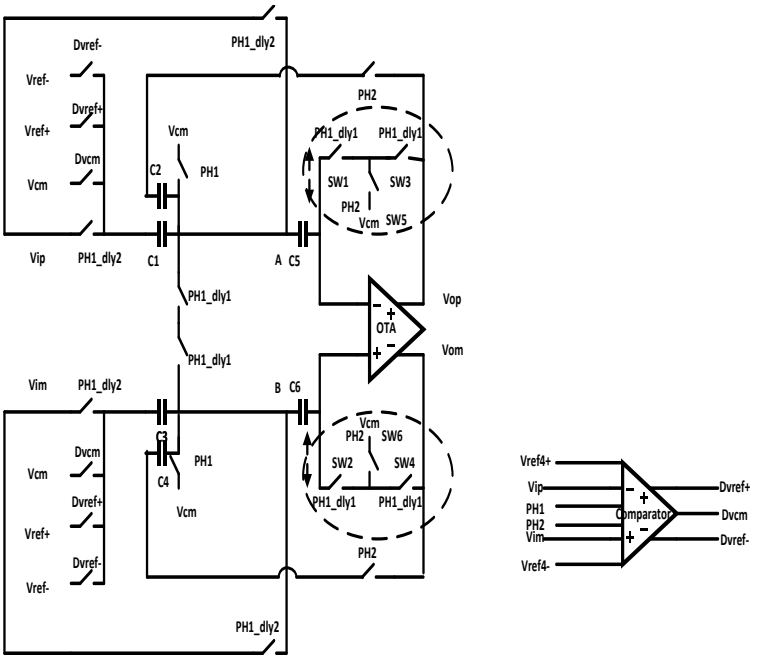


Figure 3.6 Proposed 1.5 bit MDAC architecture

As a result of leakage current from turned off switches resulting in an induced differential drifted voltage at the inputs of opamp, a simple cancellation technique, robust to device leakage, is introduced to correct this error. During PH1, both inputs and outputs of opamp are connected to common mode (CM) voltage. During PH2, with SW 1, 2, 3 and 4 turned off but the leakage current through these switches causes the voltage at the inputs of opamp to drift with a differential error due to coupling from the output. To solve this problem, CDS capacitors are isolated from switch leakage through the switches by SW 5 and 6. The Monte Carlo simulation results of settling error and differential error voltage of MDAC are summarized in Table 3.2. The Monte Carlo simulation results show a settling error less than 1/2 LSB demonstrating MDAC has sufficient bandwidth, acceptable capacitor mismatch error, and drift error. The differential error indicates that cancellation technique functions correctly robust to leakage. Based on capacitor mismatch consideration, the sizes of capacitors C1-4 are chosen as 180fF in the first three stages and 120fF in the final three stages.

Table 3.2 Settling error and Differential error of MDAC

Parameters (100 runs)	3σ data
Settling error	419uV
Differential error	86uV

3.2.2 Self-timing static comparator

The self-timing static comparator used in MDAC is shown in Figure 3.7. P differential pair inputs shorted to the CM voltage on the right has 7 and 9 different fingers. During the settling phase, the offset voltage caused by the finger mismatch will trigger the self-timing comparator. The finger difference sets the latch timing delay, tracks the MDAC quantizer and defines an upper bound on conversion timing. To ensure the output have sufficient time to settle, the pulse width of Clk2_dly should be less than 10% of PH2 cycle.

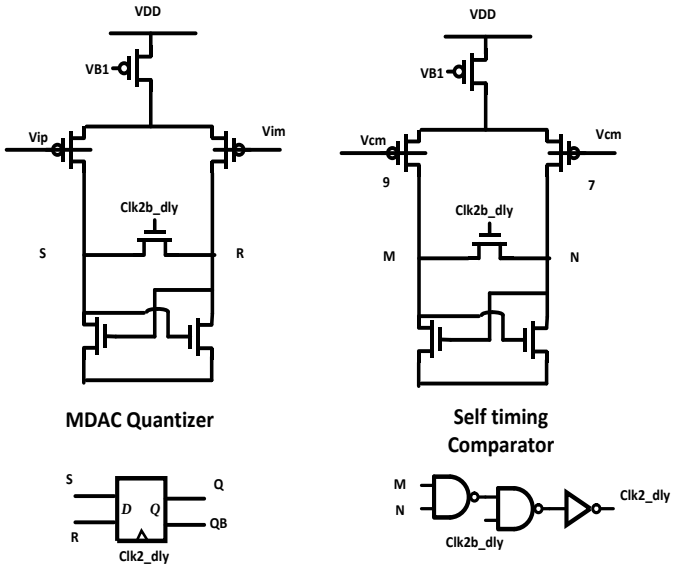


Figure. 3.7 Schematic of self-timing static latched comparator

3.2.3 Bootstrapped Switch

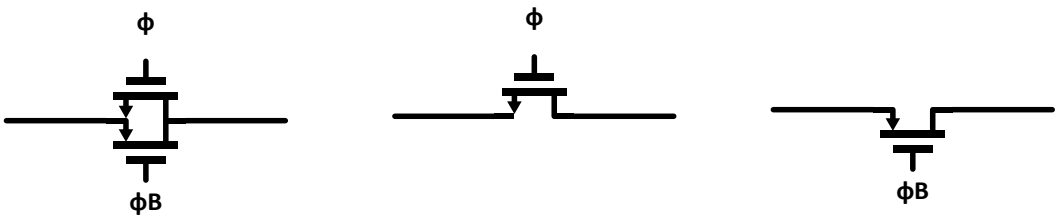


Figure 3.8 MOS switches

The MOS switches widely used in switched capacitor circuit are shown in Figure 3.8 [55-57]. For their application, NMOS/PMOS switches are used in the node where fixed voltages are applied (NMOS switched for lower voltage and PMOS switches for higher voltage), and CMOS switches are used in the signal path where the voltage changing between low to high or high to low. There are two main concerns about designing MOS switches: on-resistance and charge injection. The on-resistance of NMOS switch is:

$$R_{on} \approx \frac{1}{\mu_n C_{ox}(\frac{W}{L})(V_{GS} - V_{th})} = \frac{1}{\mu_n C_{ox}(\frac{W}{L})(V_{DD} - V_{in} - V_{th})} \tag{3.18}$$

Where μ_n is the mobility of electrons, C_{ox} is the gate oxide capacitance, V_{th} is the threshold voltage, and W and L are the width and length of MOS transistor. The charge injection voltage is:

$$V_{ch} \approx \frac{\mu_n C_{ox} WL(V_{GS} - V_{th})}{C_{eq}} = \frac{\mu_n C_{ox} WL(V_{DD} - V_{in} - V_{th})}{C_{eq}} \tag{3.19}$$

where C_{eq} is the total capacitance of source/drain of the MOS switch. From the above two equations, we can observe that the on-resistance and charge injection is dependent highly on input

signal amplitude. In the practical design, the sizes of MOS switches need to be optimized to minimize the on-resistance and charge injection. Furthermore, the on-resistance of the MOS switch which is dependent on the V_{GS} causes a nonlinearity when it used in the sampling switches in the Pipelined ADC, which will degrade the dynamic performance of ADC. This is especially problematic for low voltage designs, V_{GS} can be less than the threshold voltage and the MOS switch may not turn on.

To solve the above issue, bootstrapped switches are used as sampling switches in Pipelined ADC [63, 69]. The operation is shown in Figure 3.9.

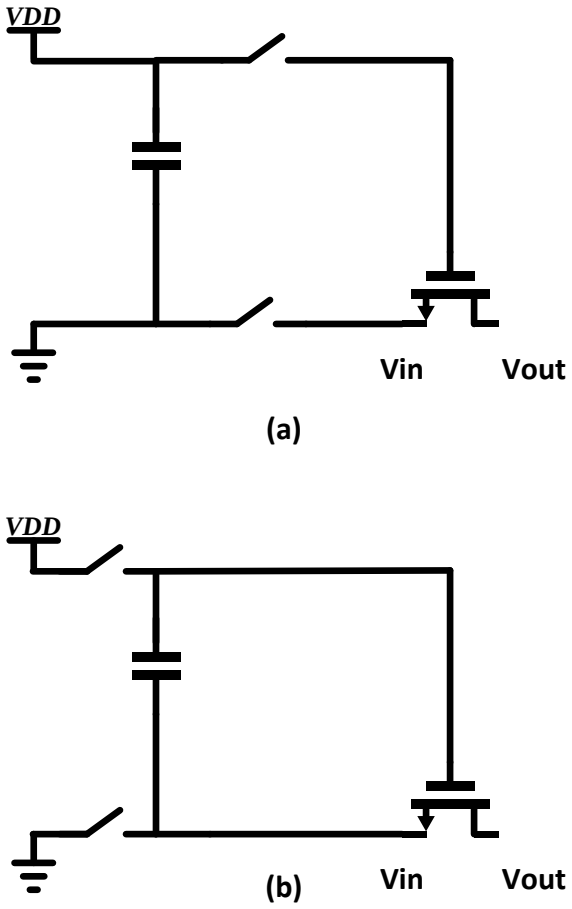


Figure 3.9 Operation of bootstrapped switch [62]

In phase a, a constant voltage VDD is placed across the sampling capacitor to charge it during the sampling phase; in the phase b, the charged capacitor is connected between the gate and source of MOS switch, the gate voltage will be (Vin+VDD), making the gate-source voltage V_{GS} as constant voltage VDD. Thus the on-resistance of switch is constant because the V_{GS} equal VDD as the input signal is changing with time. The bootstrapped switch used in Pipelined ADC is illustrated in Figure 3.10 [69].

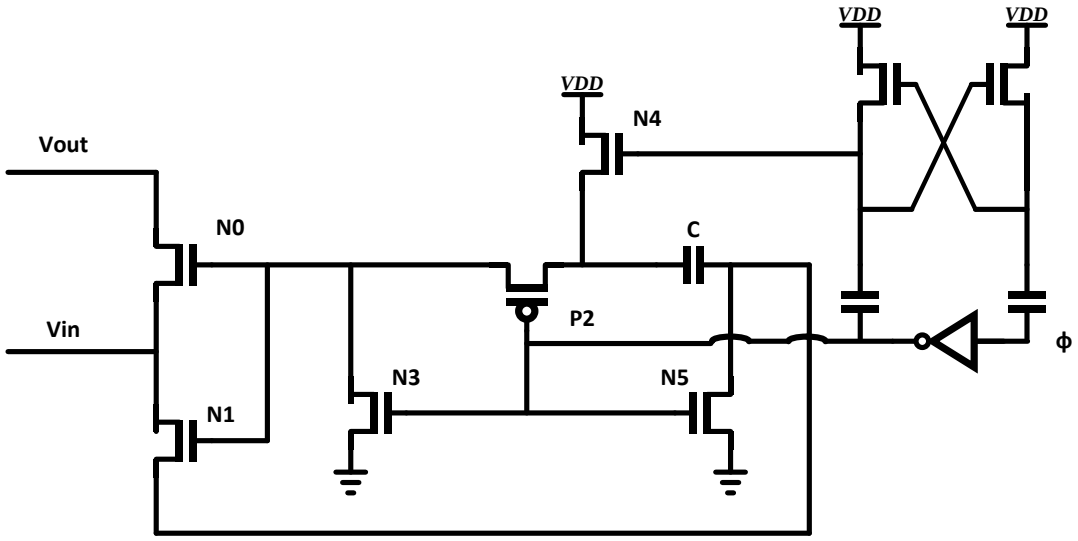


Figure 3.10 Schematic of bootstrapped switch [69]

3.3 MDAC errors

The errors such as finite open loop gain, inadequate bandwidth, capacitor mismatch and noise introduced from the MDACs can have a harmful effect on the performance of Pipelined ADC [62, 63]. These MDAC errors will be discussed in the below sections.

3.3.1 Finite OTA gain error

Opamp is one of the most important building blocks in switched capacitor implementation of Pipelined ADC [55-61]. The non-idealities caused by opamp will affect the performance of ADC.

First the effect of finite open loop gain of opamp will be discussed. The operation of 1.5 bit MDAC in amplifying phase is illustrated in Figure 3.11. Capacitor C_p is the input parasitic capacitance of opamp and the finite DC gain of opamp is A.

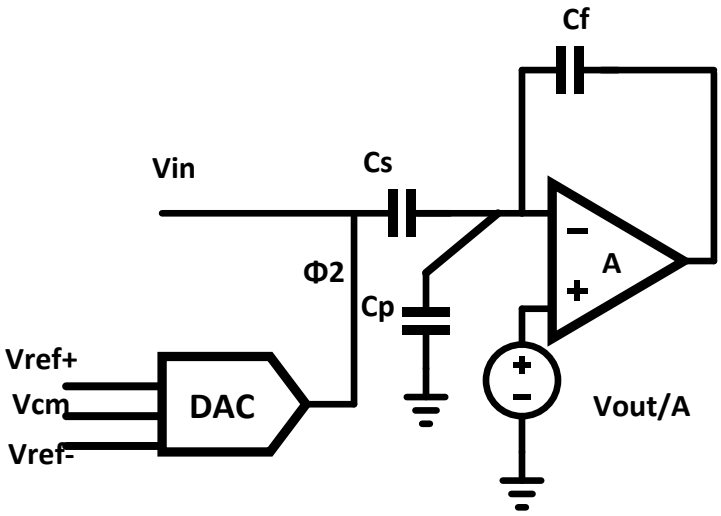


Figure 3.11 1.5 bit MDAC in amplifying phase

In the sampling phase, the sampling capacitor Cs and feedback capacitor C_f are connected to the input, sampling the input signal to the capacitors. The total charge stored on capacitor C_s and C_f in the sampling phase is:

$$q_s = (0 - V_{in}) \cdot (C_s + C_f) \tag{3.20}$$

In the amplifying phase, feedback capacitor C_f is connected to the output of opamp and sampling capacitor C_s is connected to $\pm V_{ref}$ or ground depending on the output of sub ADC. The total charge stored in amplifying phase is:

$$q_a = (V_- - s \cdot V_{iref}) \cdot C_s + (V_- - V_{out}) \cdot C_f + V_- \cdot C_p \tag{3.21}$$

Where V_ is the negative input of the opamp and s is the selection signal from the sub ADC ranging from ±1 to 0.

The total charge is kept the same in the two phases,

$$q_s=q_a \tag{3.22}$$

From above equations, the output of MDAC is:

$$V_{out}=V_{in}\cdot\left(\frac{C_s+C_f}{C_f}\right)+V_{-}\cdot\left(\frac{C_s+C_f+C_p}{C_f}\right)-s\cdot V_{ref}\cdot\left(\frac{C_s}{C_f}\right) \tag{3.23}$$

The feedback factor β in this MDAC structure is given:

$$\beta=\frac{C_s}{C_s+C_f+C_p} \tag{3.24}$$

The negative input voltage V_ can be found as

$$V_{-}=-\frac{V_{out}}{A} \tag{3.25}$$

Substituting (3.24) and (3.25) into (3.23), we can find

$$V_{out}=\left(\frac{1}{1+\frac{1}{A\beta}}\right)\cdot\left(\frac{C_s+C_f}{C_f}\right)V_{in}-\left(\frac{1}{1+\frac{1}{A\beta}}\right)\cdot s\cdot V_{ref}\cdot\left(\frac{C_s}{C_f}\right) \tag{3.26}$$

Applying Taylor expansion to (3.26),

$$V_{out}\approx\left(1-\frac{1}{A\beta}\right)\cdot\left(\frac{C_s+C_f}{C_f}\right)V_{in}-\left(1-\frac{1}{A\beta}\right)\cdot s\cdot V_{ref}\cdot\left(\frac{C_s}{C_f}\right) \tag{3.27}$$

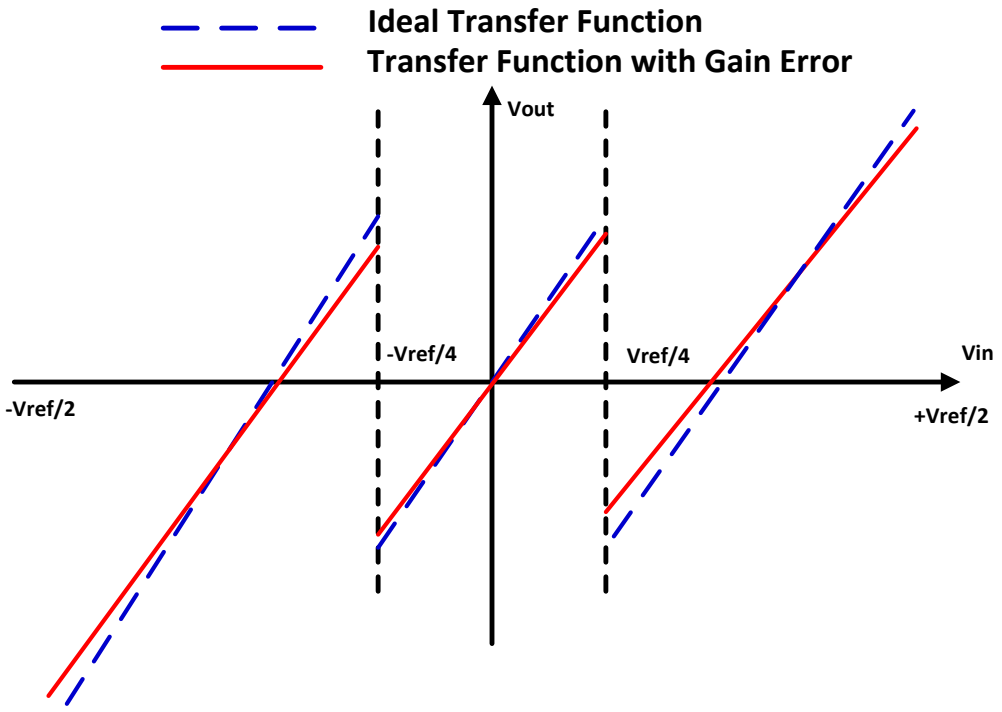


Figure 3.12 Finite gain effect on 1.5 bit MDAC transfer function

The effect of finite gain of opamp in 1.5 bit MDAC is shown in Figure 3.12. The blue line represents an ideal transfer function and red line shows a transfer function with finite gain error. It is shown that the finite gain cause the inter stage gain of MDAC to change. From equation (3.27), 1/Aβ should be less than ½ LSB to meet the accuracy requirement.

3.3.2 Finite OTA bandwidth

Another important non-ideality caused by opamp in MDAC is the finite OTA bandwidth [55, 56]. Assuming opamp has a linear single–pole frequency response and infinite DC gain, the output voltage of MDAC can be found as:

$$V_{out} = (1 - e^{-\frac{t_s}{\tau}}) \cdot \left((\frac{C_s + C_f}{C_f}) V_{in} - s \cdot V_{ref} \cdot \frac{C_s}{C_f} \right) \tag{3.28}$$

Where t_s is the settling time and τ is the time constant of MDAC. The time constant τ is given by

$$\tau = \frac{1}{\omega_{3dB}} = \frac{1}{\omega_u \cdot \beta} = \frac{1}{2\pi \cdot f_u \cdot \beta} \tag{3.29}$$

Where ω_{3dB} is the 3dB bandwidth of MDAC, β is the feedback factor, ω_u is the unity gain bandwidth and f_u is unity gain frequency of opamp. For example, for an 8 bit Pipelined ADC with 1.5 bit/stage, if the clock frequency is 16 kHz and the clock period is 62.5us, then the maximum settling time of MDAC is 31.25us. The settling error of the first stage should be less than 0.4% to realize 8 bit accuracy. The required unity gain frequency of opamp is:

$$f_{un} = \frac{(N+1)\ln 2}{2\pi\beta t_s} = \frac{(8+1)\ln 2}{2\pi\beta t_s} = \frac{9*2}{2\pi t_s}\ln 2 = 63.6kHz \tag{3.30}$$

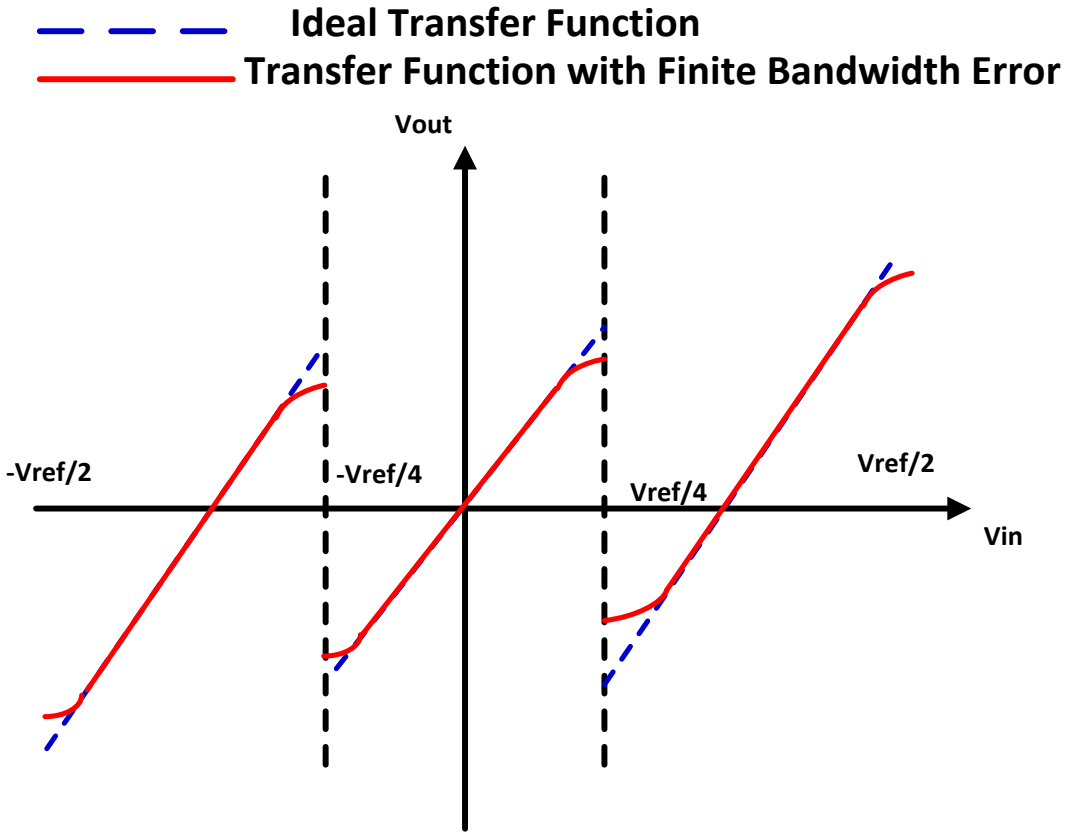


Figure 3.13 Finite opamp bandwidth effect on 1.5 bit MDAC transfer function

The effect of finite opamp bandwidth in 1.5 bit MDAC transfer function is shown in Figure 3.13. The blue line represents an ideal transfer function and red line shows a transfer function with finite a significant gain bandwidth error. The settling error cause harmonic distortion. Therefore, the bandwidth of opamp should be high enough to minimize the settling error of MDAC.

3.3.3 Capacitor mismatch

Capacitor mismatch is another error term in MDAC which is harming the performance of Pipelined ADC [57-59]. Assume ΔC_s is the mismatch error of sampling capacitor C_s and ΔC_f is the mismatch error of feedback capacitor C_f. The output voltage of MDAC with capacitor mismatch is:

$$V_{out} = \left(\frac{C_s + \Delta C_s + C_f + \Delta C_f}{C_f + \Delta C_f} \right) V_{in} - s \cdot V_{ref} \cdot \left(\frac{C_s + \Delta C_s}{C_f + \Delta C_f} \right) \tag{3.31}$$

Suppose $C_s=C_f=C$ and $\Delta C_s/C= \varepsilon_1$, $\Delta C_f/C=\varepsilon_2$, then we have

$$\begin{aligned} V_{out} &= \left(\frac{C_s + \Delta C_s + C_f + \Delta C_f}{C_f + \Delta C_f} \right) V_{in} - s \cdot V_{ref} \cdot \left(\frac{C_s + \Delta C_s}{C_f + \Delta C_f} \right) \\ &\approx (2 \pm \sqrt{\varepsilon_1^2 + \varepsilon_2^2}) V_{in} - s \cdot V_{ref} (1 \pm \sqrt{\varepsilon_1^2 + \varepsilon_2^2}) \end{aligned} \tag{3.32}$$

The capacitor mismatch effect on 1.5 bit MDAC transfer function is shown in Figure 3.14. The blue line represents the ideal transfer function and the red line shows the transfer function with capacitor mismatch. For 180nm process, the size of 180fF is chosen to realize 8 bit accuracy in the first three stages and 120fF in the final three stages.

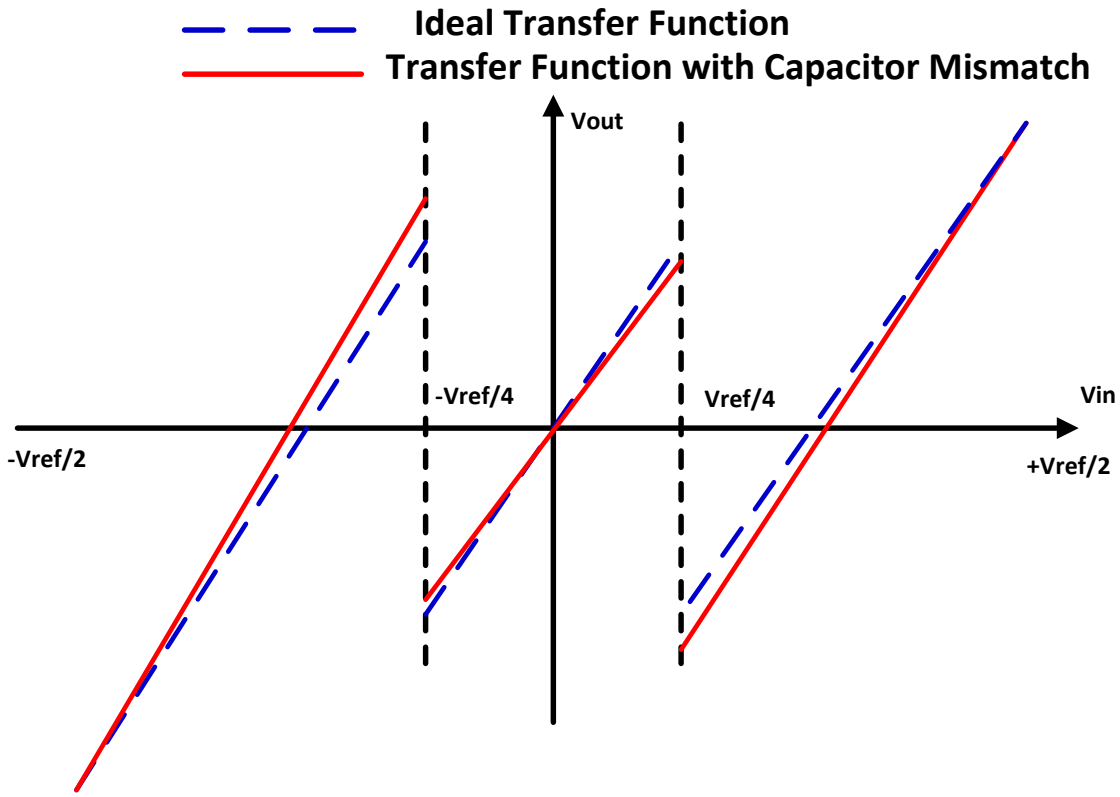


Figure 3.14 Capacitor mismatch effect on 1.5 bit MDAC transfer function

3.3.4 Noise in MDAC

Noise is another very important factor in Pipelined ADC [62-66]. The total input referred noise in Pipelined ADC is [40]:

$$v_{n\_in}^2 = v_{n\_1}^2 + \frac{1}{2^{2m}} v_{n\_2}^2 + \frac{1}{2^{4m}} v_{n\_3}^2 + \Lambda + \frac{1}{2^{2km}} v_{n\_k}^2 + \Lambda \qquad (3.33)$$

Where $v^2_{n\_1}$ is the first stage noise, $v^2_{n\_k}$ is the noise in the *k*th stage and m is the inter stage gain of each stage. Since the noise from the following stages is reduced by the inter stage gain, the noise in the first stage is the most significant noise source and needs to be carefully calculated and designed.

The structure of 2.5 bit MDAC is shown in Figure 3.15.

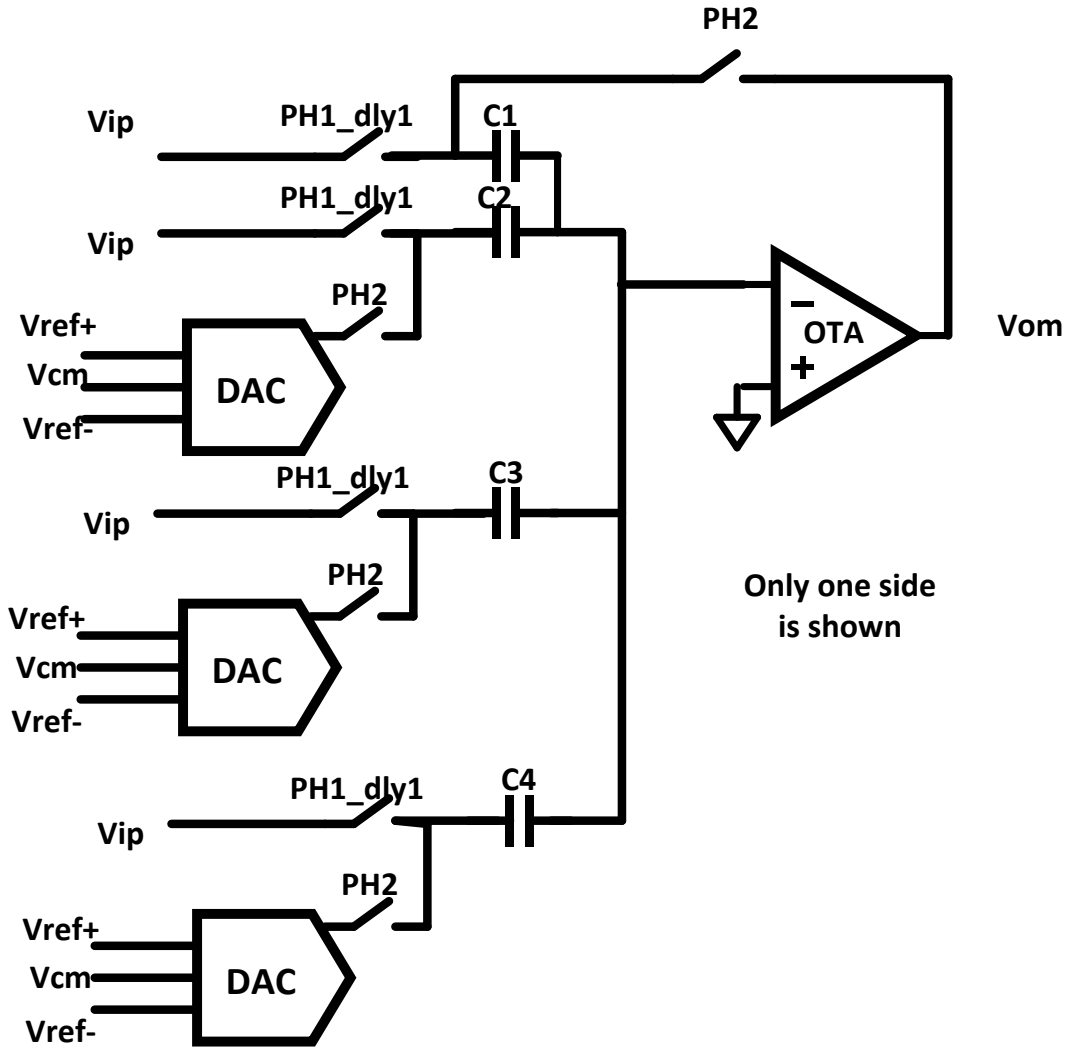


Figure 3.15 2.5 bit MDAC [66]

As discussed in section 3.1.1, the total noise of output is:

$$v_{out,tot} = \sqrt{v_{out,tot}^2} = \sqrt{v_{out,n1}^2 + v_{out,n2}^2} = \sqrt{\left(\frac{4KT}{C_1} + \frac{3.1nKT}{C_c}\right)} \tag{3.34}$$

C_1 is found as 180f and C_c equals 400f resulting in $v_{out,tot}$ equals 387uV less than LSB/4.

3.4 Pipelined ADC simulation results

Fully differential sinusoid signals of 218 Hz and 2.1 KHz Sinusoid with Vp equal 200mV were applied to the ADC input spectre model and sampled at 16 kHz. The simulated ADC outputs FFT (Fast Fourier Transform) spectrums are shown in Figures 3.16 and 3.17. The resulting SNDR is 49.64dB, 48.22dB with an ENOBs (Effective number of bits) of 7.95, and 7.71 bits respectively.

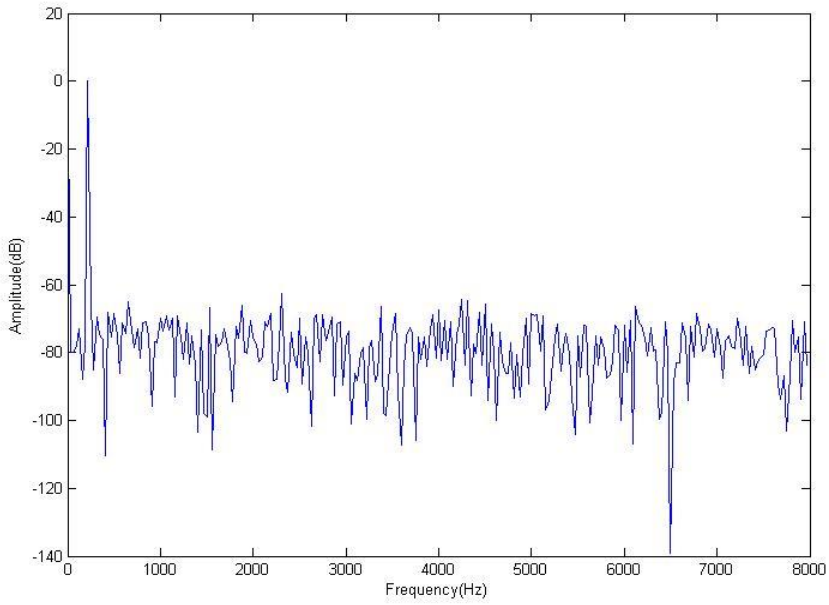


Figure 3.16 Simulated ADC Output FFT Spectrum Input@218Hz

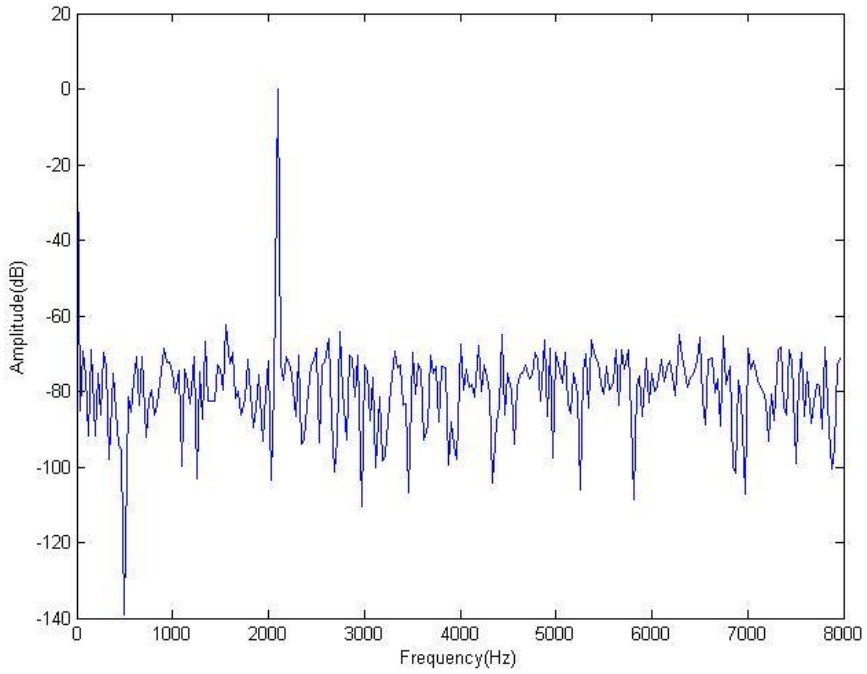


Figure 3.17 Simulated ADC Output FFT Spectrum Input@2.1kHz

Figure 3.18 and Figure 3.19 show the simulated DNL (Differential Nonlinearity) and INL (Integral Nonlinearity) error plots for the ADC. From the plot, the DNL and INL error are both within ±0.5LSB. The total simulated power consumption of ADC is 3.92uW. The performance of ADC is summarized in the Table 3.3 as below.

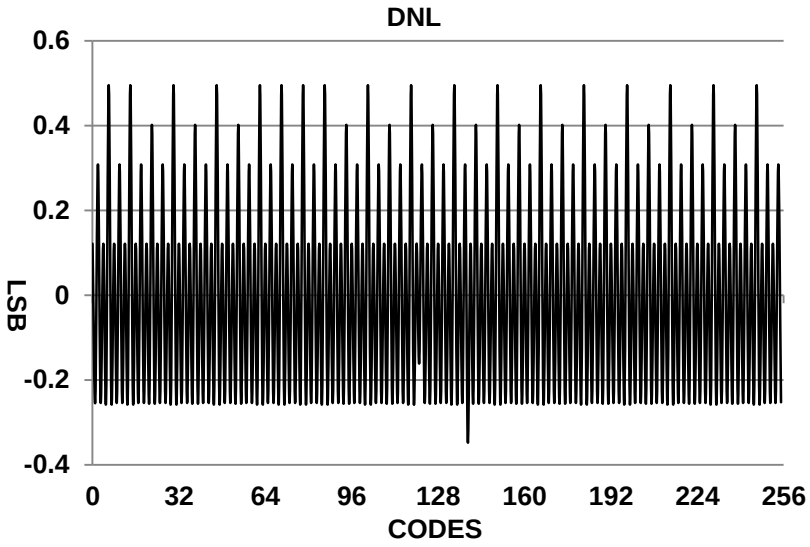


Figure 3.18 Simulated DNL

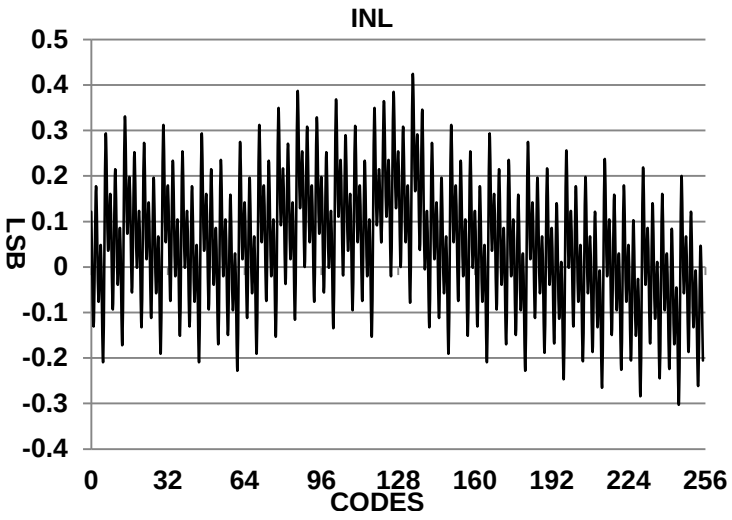


Figure 3.19 Simulated INL

Table 3.3 ADC Performance

Parameters	**Simulation Results**
Supply Voltage (V)	0.7
Input Range (V)	0.8Vpp
ENOB (bit)	8
Sampling Frequency (KHz)	16
Power Consumption (uW)	3.92
DNL&INL (LSB)	±0.5
FOM=Power/(2^{ENOB}*fs)	0.96pJ/step

3.5 Conclusion

The power consumptions of second stage neural amplifier driven by Pipelined ADC, SAR ADC and Sigma-Delta ADC for neural recording applications have been discussed in this chapter. A Pipelined ADC results in the lowest total power consumption ensuring higher power efficiency for the neural recording system. The main building blocks of Pipelined ADC were introduced and all significant MDAC errors were reviewed to set the parameters to meet the requirement of accuracy. The whole system static and dynamic simulation results of Pipelined ADC were shown in the end.

CHAPTER IV

MEASUREMENT RESULTS

This chapter summarizes the measurements results for the low power, low noise implantable neural recording system consisting of; 1) Low power, low noise fully differential neural amplifier including BP1, BP2 and BP1&2 measurement results with saline solution and real animal neural recording data; 2) 8 bit low-power fully differential Pipelined ADC with the most significant blocks 2.5 bit and 1.5 bit MDAC testing Results.

4.1 Neural amplifier test results

4.1.1 BP1 test results

The bandpass amplifier which utilizes a fully differential structure is based on capacitive and resistive feedback architecture [15]. The lower 3dB frequency is determined by the feedback capacitor and current biased pseudo resistor [18]. The die picture for neural amplifiers is shown in Figure 4.1 and test set up for bandpass amplifiers is shown in Figure 4.2. The PMOS follower with unity gain is used to drive the large external capacitance load and 150uA current source is injected into follower to bias it.

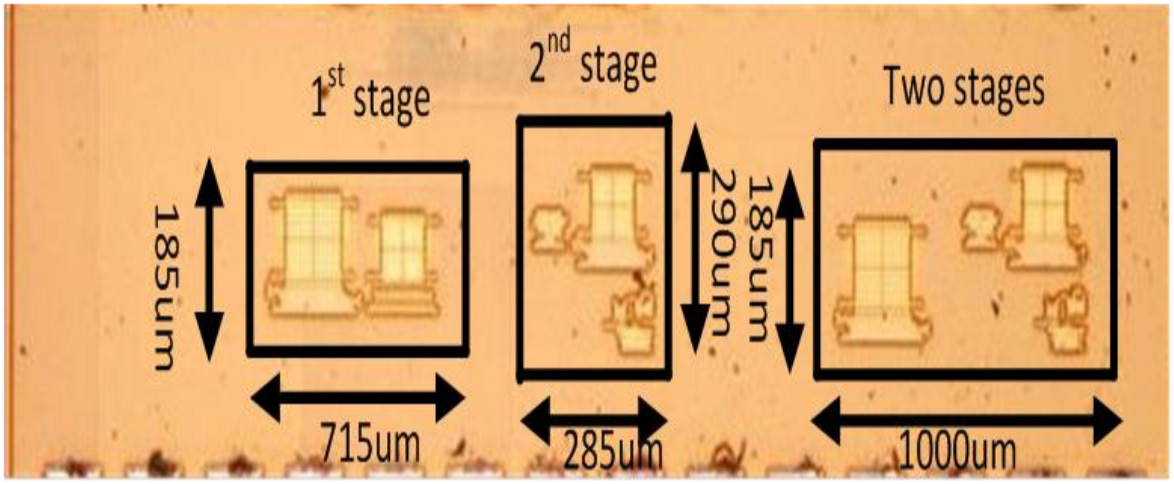


Figure 4.1 Die picture of bandpass amplifiers

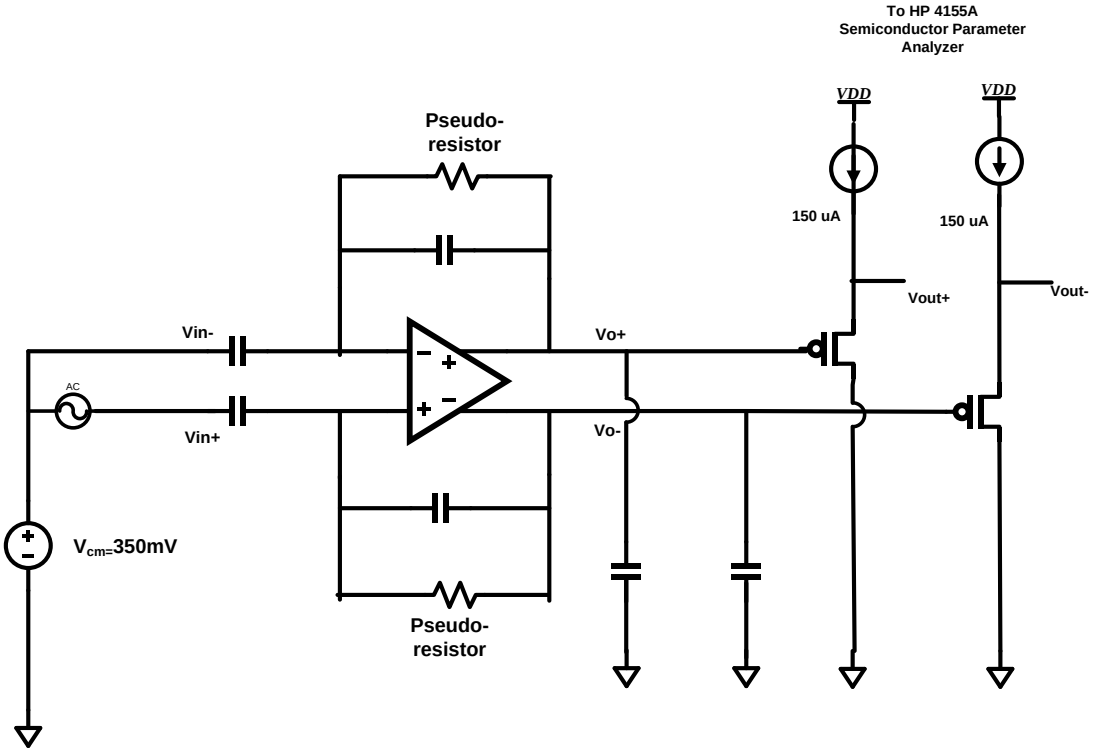


Figure 4.2 Test set up for bandpass amplifiers

The BP1 frequency response is presented in Figure. 4.3 demonstrating a midband gain of 30.0dB and a bandpass of 0.56 KHz to 11.8 KHz. The excellent agreement between measured and

simulated results is observed. The BP1 operates on a 0.7V supply and total power consumption is less than 0.77 µW.

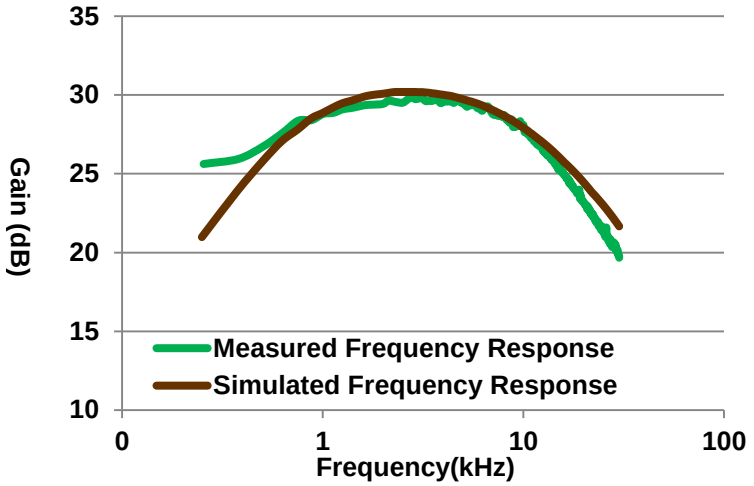


Figure 4.3 Simulated and measured frequency response of BP1.

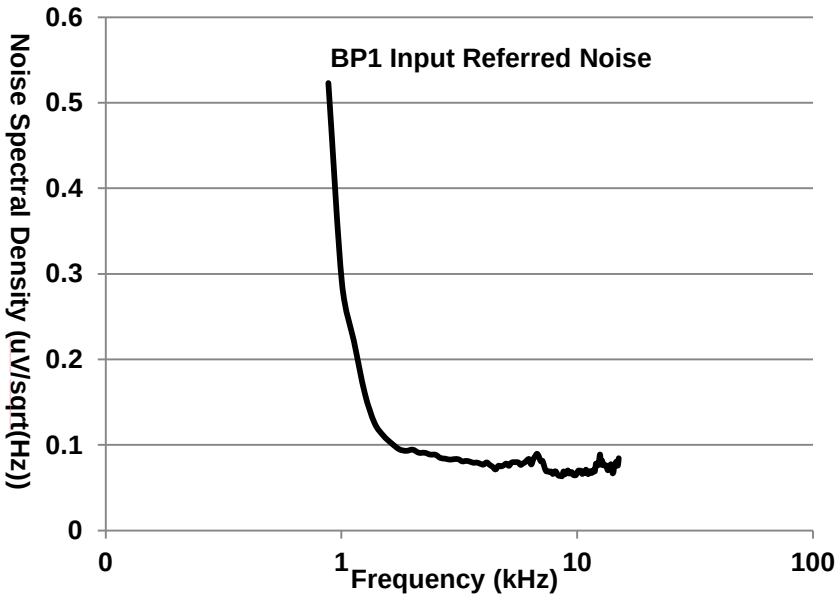


Figure 4.4 Measured input referred noise of BP1.

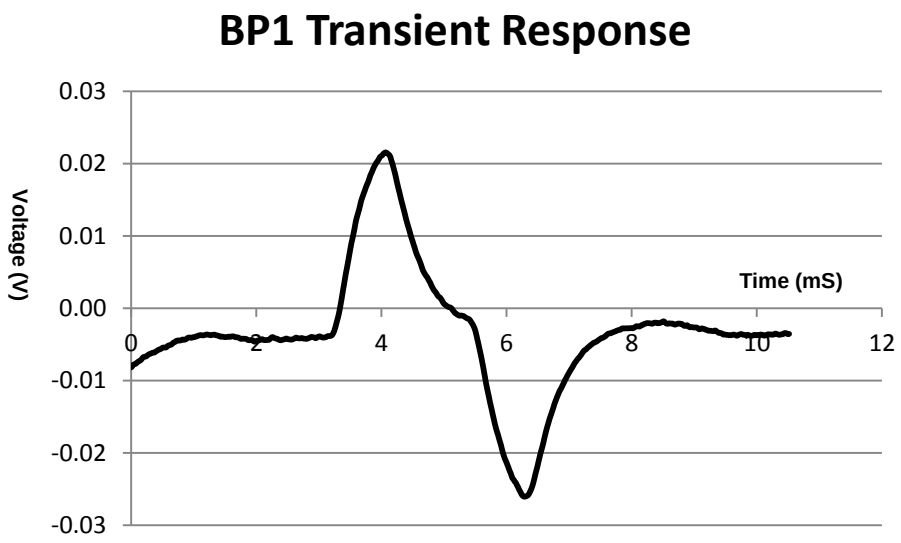


Figure 4.5 BP1 transient response

The input-referred noise spectrum of the BP1 is shown in Figure 4.4. Integrating the area under the curve from 100Hz to 100 kHz yields a total noise of 13.7μV. The transient response of BP1 is shown in Figure 4.5. Large signal behavior was confirmed by applying a 2mV, 1.5ms pulse. The differentiated output, shown in Figure 4.5 where V_p equal 20.4 mV and the rise and fall times are approximately 750us validates the expected bandpass response. Given;

$$dV_{out} = RC \times \frac{dV_{in}}{dt} \times K \tag{4.1}$$

$$RC = \frac{20.4mV}{2mV \times 0.8/750\mu s} \times \frac{1}{30} \tag{4.2}$$

From (4.1) and (4.2) 1/RC equals 3.13*10^3, consistent with the low 3dB frequency.

4.1.2 BP2 test results

The BP2 provides gain for neural amplifier and has lower 3dB frequency than BP1. The simulated and measured frequency response of BP2 is shown in Figure 4.6. The measured

midband gain is 30.2dB and bandwidth is from 202 Hz to 10.9 KHz. The measured input referred noise of BP2 is shown in Figure 4.7. The total input referred noise integrating from 100Hz to 100 kHz is 62.9uV. The power consumption of BP2 is 0.77uW with 0.7V power supply.

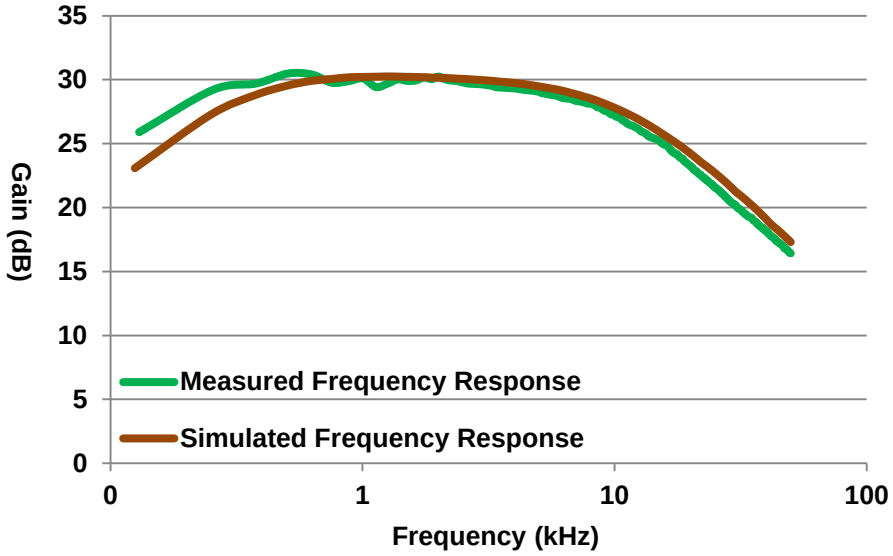


Figure 4.6 Simulated and measured frequency response of BP2.

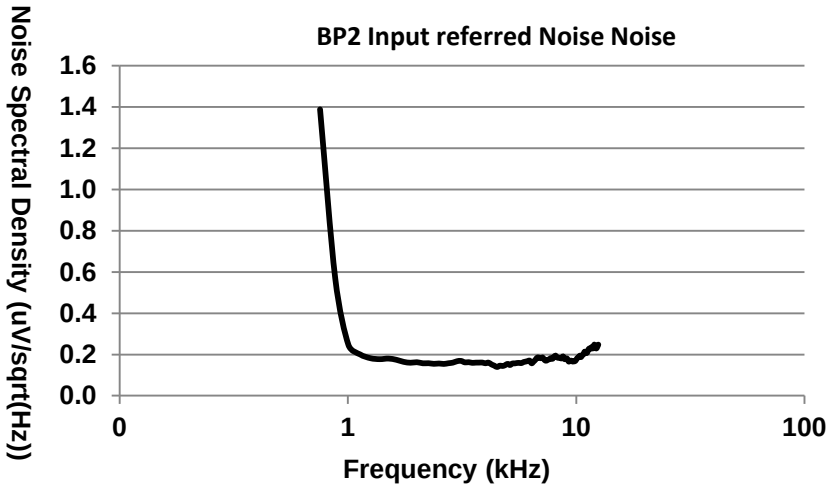


Figure 4.7 Measured input referred noise of BP2.

4.1.3 BP1&2 test results

Figure 4.8 is the combined BP1&2 frequency response. The midband gain is 58.4dB with a bandwidth of 710Hz to 8.26 kHz. The BP1&2 operates with 1.2V to 0.7V supplies and is consuming less than 1.90 μW at 700mV.

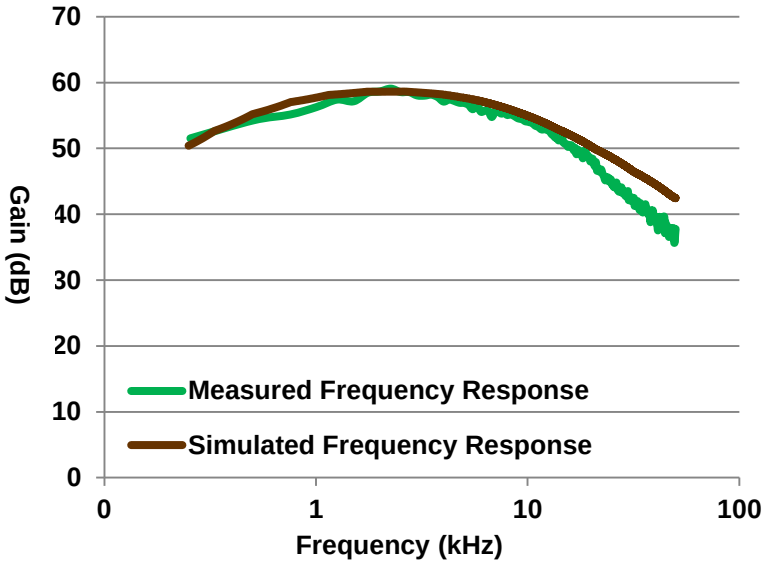


Figure 4.8 Simulated and measured frequency response of BP1&2

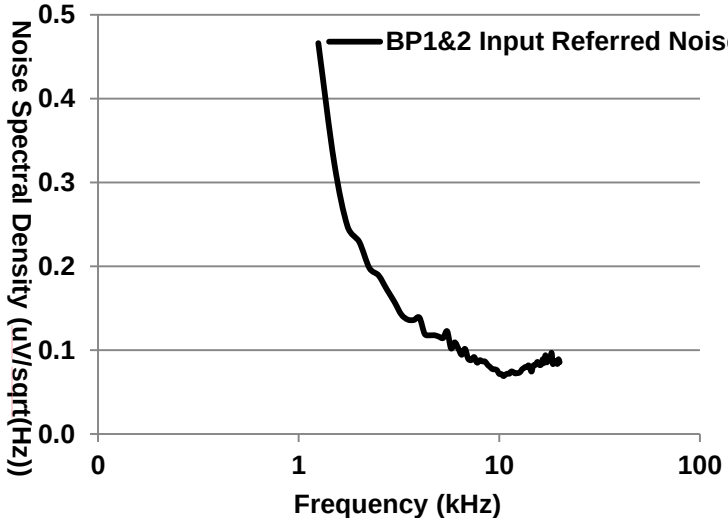


Figure 4.9 Measured input referred noise of BP1&2

The input-referred noise spectrum of the BP1&2 in cascade is shown in Figure 4.9 has a total input referred noise of 20.7uVwhen integrating from 100Hz to 100 kHz.

Again large signal behavior of BP1&2 in cascade is validated with an input 0.5mV pulse 1.5mS in duration is shown in Figure 4.10. The resulting 114mV differentiated output with rise/fall equal 750us validated expected behavior. Given;

$$RC = \frac{114mV}{0.5mV \times 0.8/750\mu s} \times \frac{1}{900} \tag{4.3}$$

From (4.3) 1/RC equals 4.2*10^3, confirming the lower 3dB frequency.

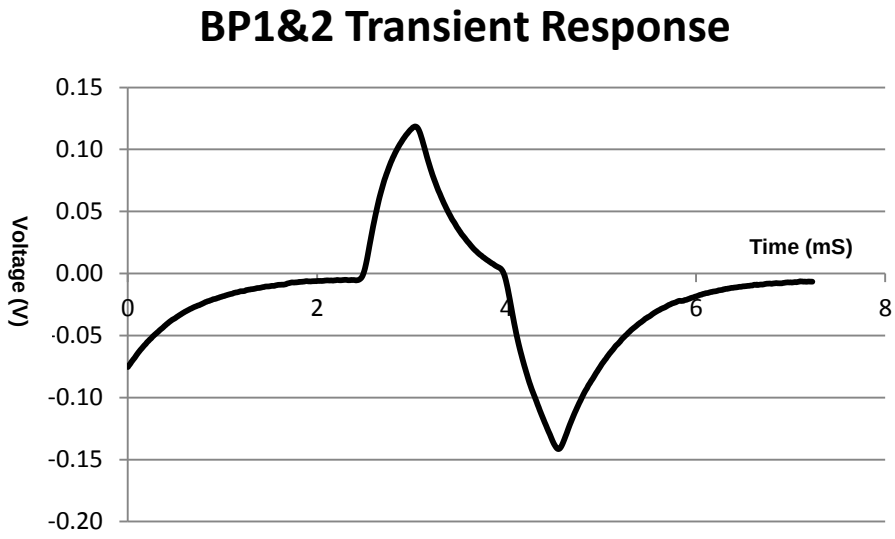


Figure 4.10 BP1&2 transient response

The performance of the neural amplifier is summarized in Table 4.1. The two stage low-noise neural amplifier has a gain of 58.4dB and bandwidth from 0.71 kHz to 8.26 kHz. The total power consumption is 1.90uW with input referred noise of 20.7uV. The measured results demonstrate the neural amplifier's suitability for instu neutral activity recording.

Table 4.1 Performance summary of BP amplifiers

	Midband Gain	**f_low _3dB**	**f_high_ 3dB**	**Input referred noise**	**Output SNDR**	**Power Consumption**	**Power Supply**
Stage 1	30dB	565Hz	11.8kHz	13.7uV	46.5dB	0.77uW	0.7V
Stage 2	30.2dB	202Hz	10.9kHz	62.6uV	45.2dB	0.77uW	0.7V
Two Stages Simulated	58.6dB	560Hz	8kHz	10uV	48.1dB	1.81uW	0.7V
Two Stages Measured	58.4dB	710Hz	8.26kHz	20.7uV	44.7dB	1.90uW	0.7V

The BP amplifier was also tested in a sterilized saline solution used to emulate real animal's brain tissue with 25um tungsten micro-wires insulated with Teflon. The impedance of electrode is 50kΩ at 1 kHz. Figure 4.11 and 4.12 show the experimental setup for the saline solution test. The input signal may be contaminated with 60Hz interference with much larger amplitude than the pre-recorded signal, as a result, an oven is used as Faraday cage to minimize the 60Hz interference for the amplifier. An artificial EEG signal was generated using an Agilent 33250A arbitrary waveform generator. This signal was fed into the saline solution through electrode A. Electrode B collected the signal and the BP amplifier amplified and filtered the input signal.

The output signal of neural amplifier is shown in Figure 4.13 when the inputs sensing 240uV sinusoid signal with frequency of 1 kHz in the saline solution. The Vp-p amplitude is about 227mV confirming the gain of neural amplifier. Table 4.2 summarizes the output signal amplitudes with different input signals amplitudes. The output spectrum is shown in Figure 4.14; the input referred noise is 18uV by integrating this output spectrum from 100 to 100k Hz. The output spike signal of neural amplifier is shown in Figure 4.15 when the inputs sensing 200uV pulse signal in the saline solution. The recorded data from rats is shown in Figure 4.16.

Figure 4.11 Experimental setup for saline test of BP amplifier

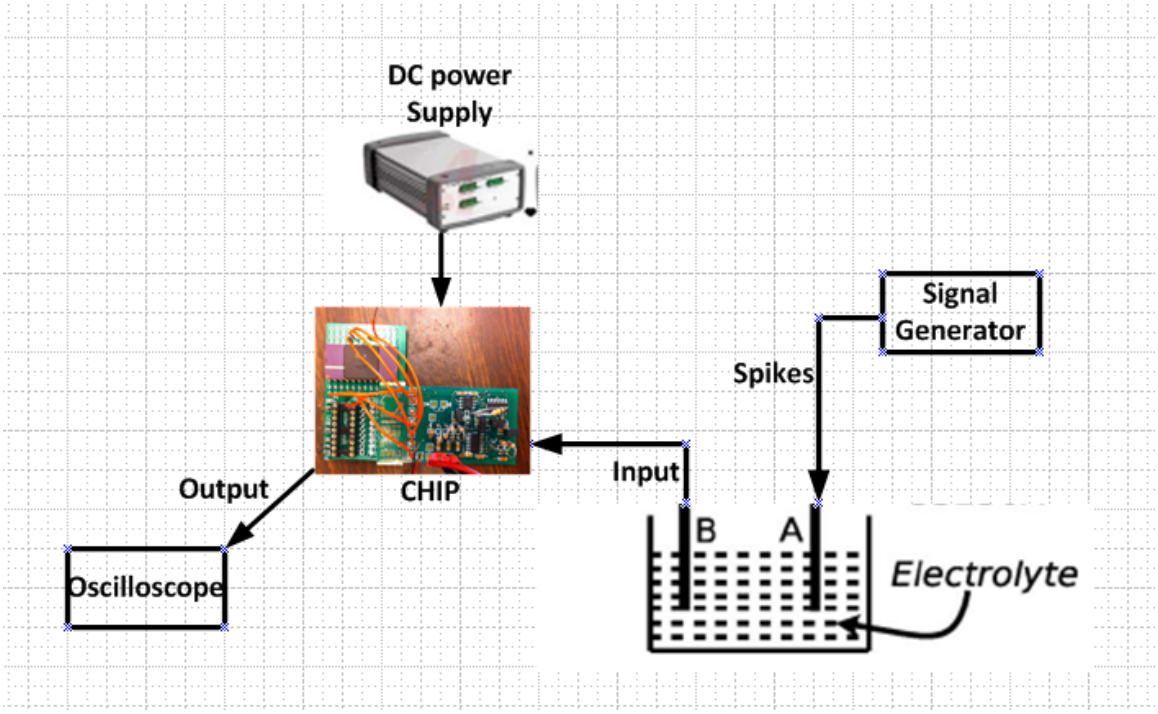


Figure 4.12 Saline solution test setup for BP amplifier

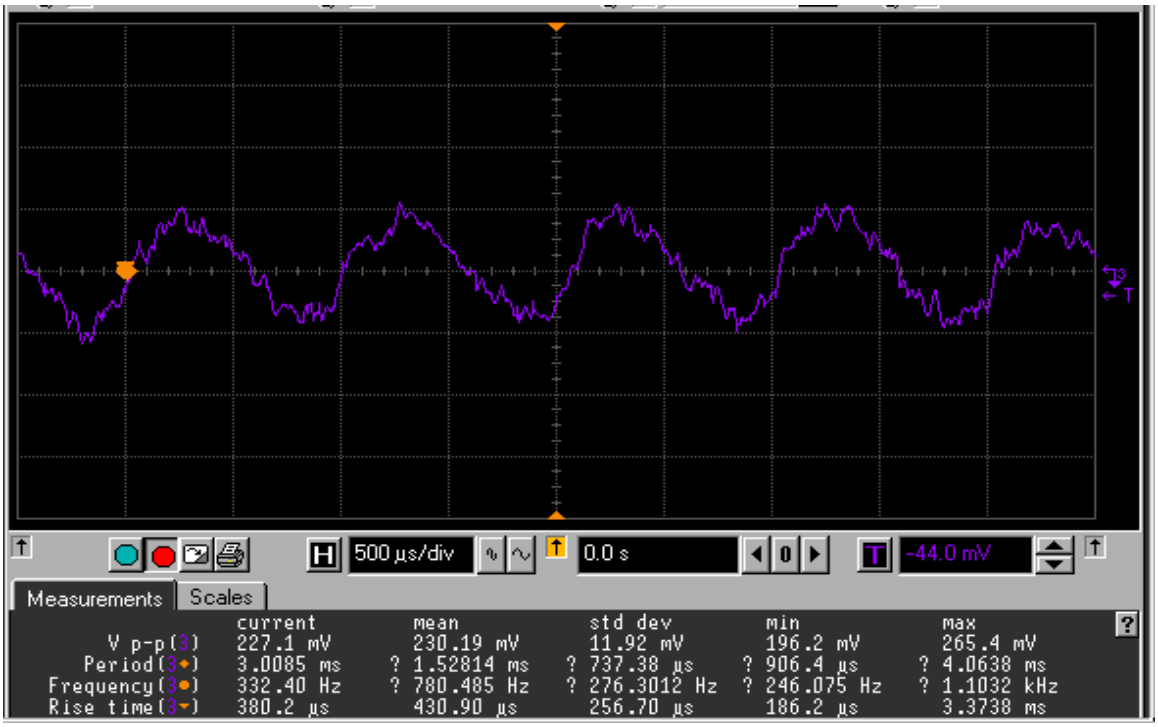


Figure 4.13 Output sinusoid signal when sensed input equals 240uV@1kHz in saline solution

Table 4.2 Output signal amplitudes of BP amplifiers

Sense signal	Output amplitude
263uV	298mV
200uV	227mV
175uV	196mV

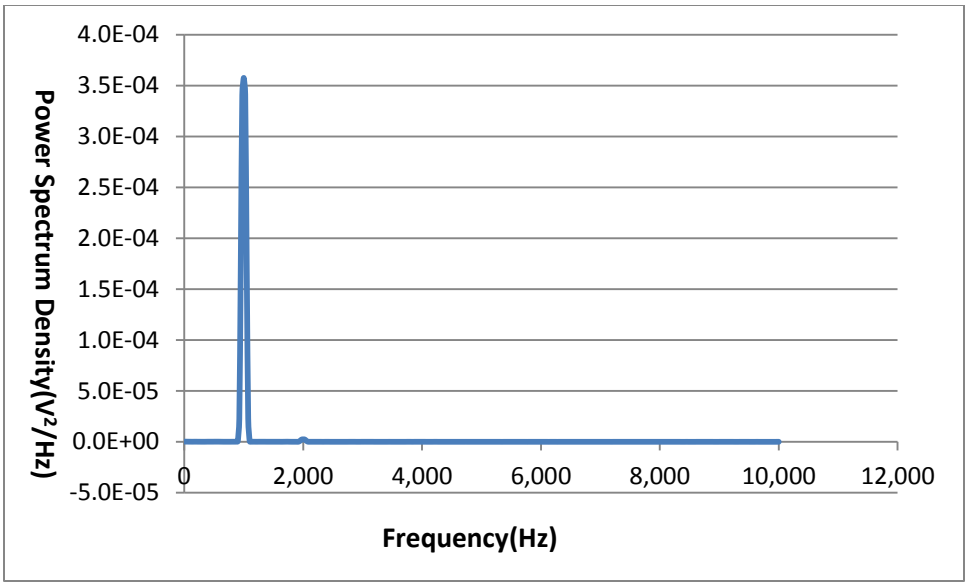


Figure 4.14 Output signal spectrum when sinusoid signal input is sensed

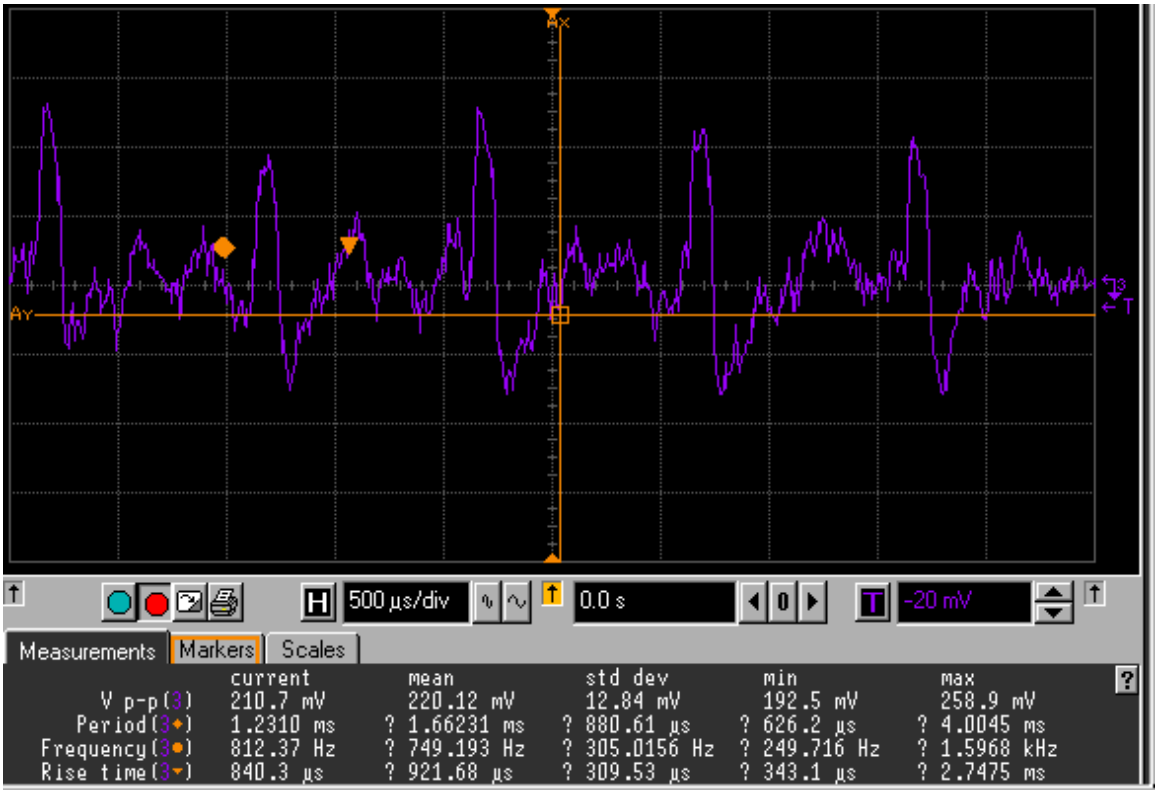


Figure 4.15 Output pulse signal when sensed pulsed input equals 200uV@1kHz in saline solution

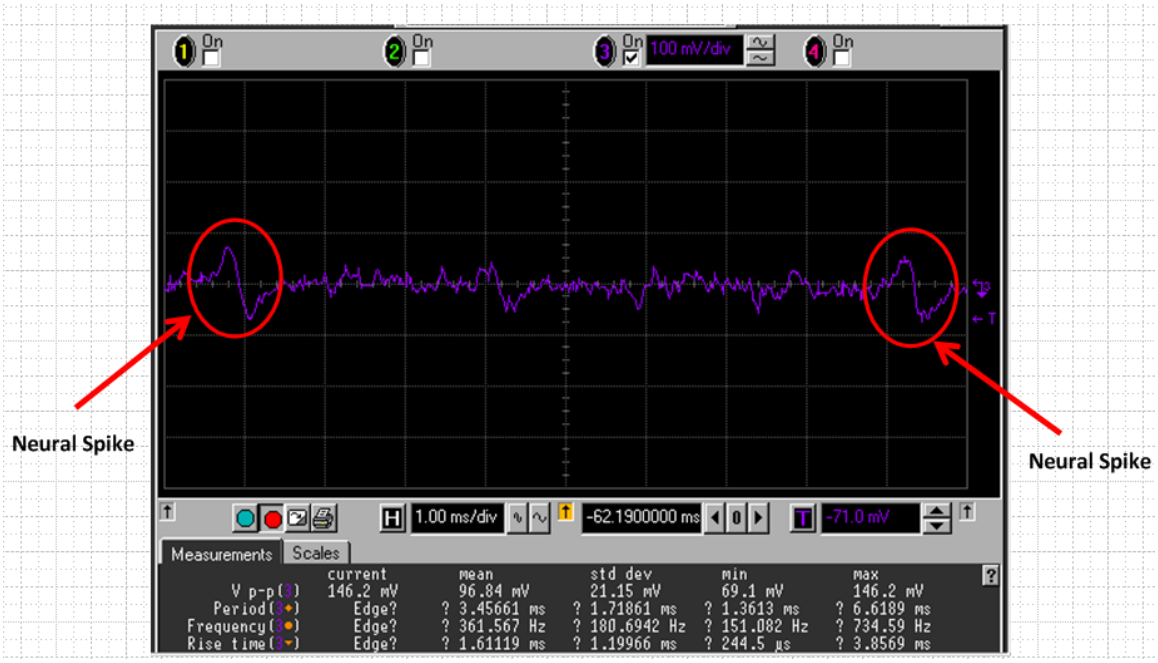


Figure 4.16 Recorded data from rats

4.2 Pipelined ADC test results

The die picture for Pipelined ADC testing is shown in Figure 4.17. The 8 bit Pipelined ADC with sampling frequency at 16 kHz is comprised of a 2.5 bit front end followed by five 1.5 bit stage MDACs. Both MDACs were padded out for validation testing for power consumption, gain, noise, and conversion accuracy.

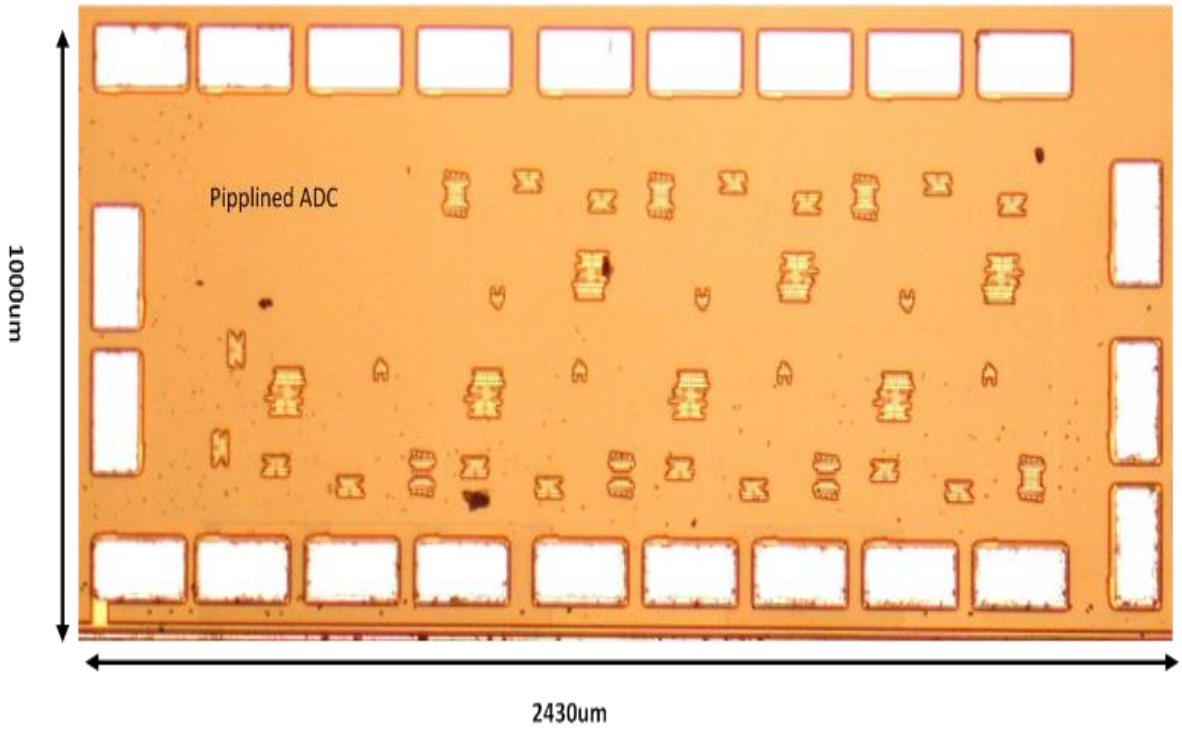


Figure 4.17 Die for 8 bit Pipelined ADC

4.2.1 MDAC 2.5 bit test results

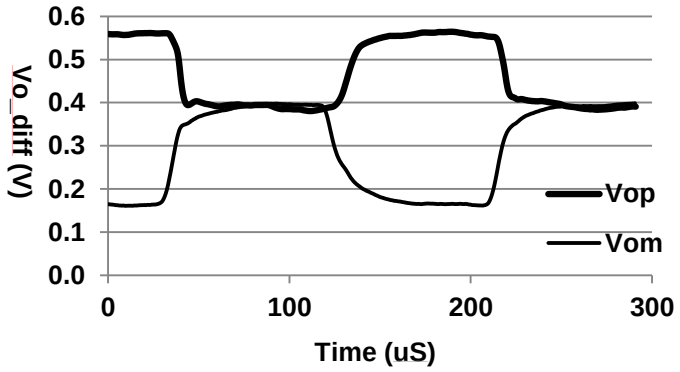


Figure 4.18 2.5 bit MDAC transient response

The measured transient response of the 2.5 bit MDAC to an input with positive full V_{ref} equals 400mV is shown in Figure 4.18. The measured settling time constant (τ) is 4.9 μs resulting in 9.2 bit settling accuracy.

$$N = \frac{t_s}{\tau \ln(2)} = \frac{31.25\mu s}{4.9\mu s \times \ln 2} = 9.2 \tag{4.4}$$

For stage one 8.5 bits of settling accuracy must be maintained providing a settling margin of 0.7 bits. Since the MDAC 2.5 bit can achieve to 9.2 bit in the settling period, which is higher than the settling accuracy 8.5 bit, the MDAC 2.5 bit has no slewing rate problem.

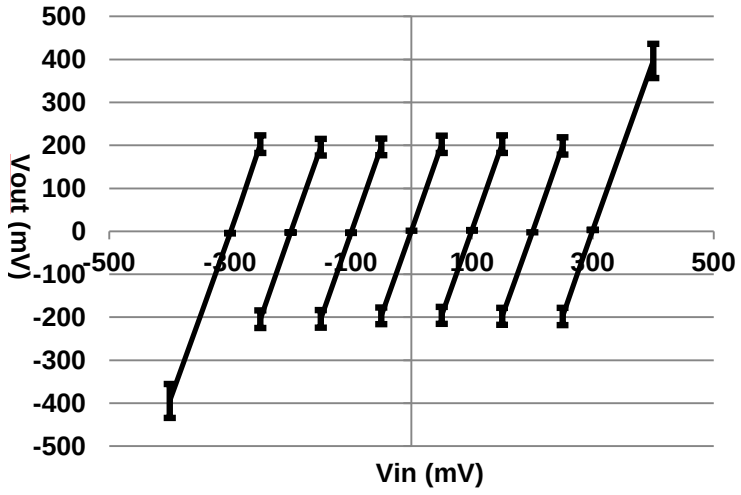


Figure 4.19 2.5 bit MDAC transfer function

The measured 2.5 bit MDAC transfer function is shown in Figure 4.19 with measured coefficients in Table 4.3.

Table 4.3 2.5 bit MDAC transfer function

Input	Transfer Function
Vin>5/8Vref	Vout=3.96*Vin -1186 mV
5/8Vref >Vin>3/8Vref	Vout=3.96*Vin -793 mV
3/8Vref >Vin>1/8Vref	Vout=3.98*Vin -395 mV
1/8Vref >Vin>-1/8Vref	Vout=3.99*Vin +2.4 mV
-1/8Vref >Vin>-3/8Vref	Vout=4.00*Vin +396 mV
-3/8Vref >Vin>-5/8Vref	Vout=4.00*Vin +796 mV
-5/8Vref >Vin	Vout=3.97*Vin +1192 mV

The MDAC noise was measured by shorting the two inputs to V_{cm}, giving the non-overlapping clock, measure the output noise spectrum. The measured output noise includes kT/C and OTA noise. The input-referred noise spectrum of the 2.5 bit MDAC bit is shown in Figure 4.20. Integrating the area under the curve from 100Hz to 100 kHz yields a total input referred noise of 435μV.

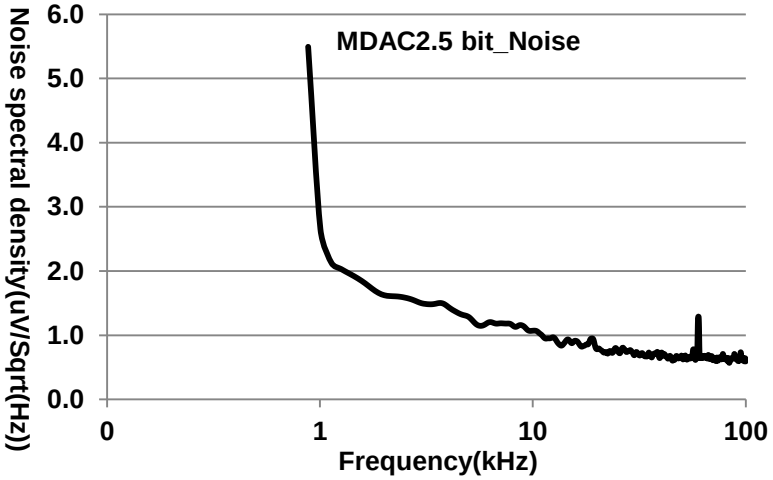


Figure 4.20 Measured noise of 2.5 bit MDAC

The 2.5 bit MDAC error sources are shown in Table 4.4. Capacitor matching to 8.4 bits is given by the PDK model.

Table 4.4 2.5 bit MDAC errors

MDAC Errors	**Measurement (Number of Bits)**
Gain error	9.1
Settling error	9.2
Slewing rate limited	No Slewing problem
MDAC noise	9.1
Capacitor Mismatch	8.4

4.2.2 1.5 bit MDAC test results

The transient response of the 1.5 bit MDAC to a step input with positive V_{ref} equal 400mV is shown in Figure 4.21. The measured settling time constant is 6us resulting in 7.5 bits of settling accuracy.

$$N = \frac{t_s}{\tau \ln(2)} = \frac{31.25\mu s}{6\mu s \times \ln 2} = 7.5 \tag{4.5}$$

Post stage one 6 bits of settling accuracy is required providing a 1.5 bit a settling margin. Since the MDAC 1.5 bit can achieve to 7.5 bit in the settling period, which is higher than the settling accuracy 6 bit, the MDAC 1.5 bit has no slewing rate problem.

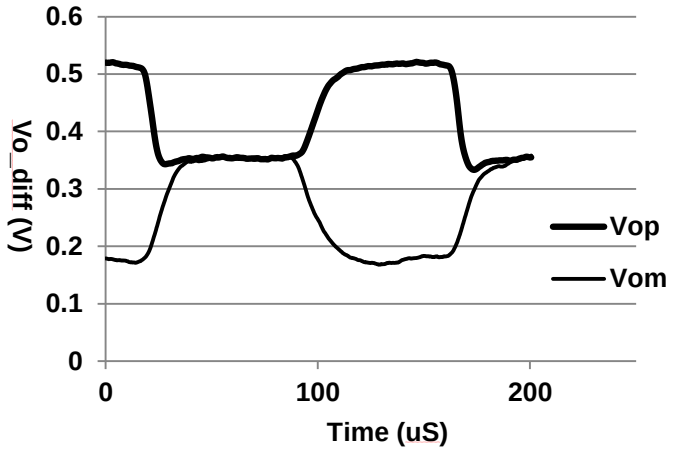


Figure 4.21 1.5 bit MDAC transient response

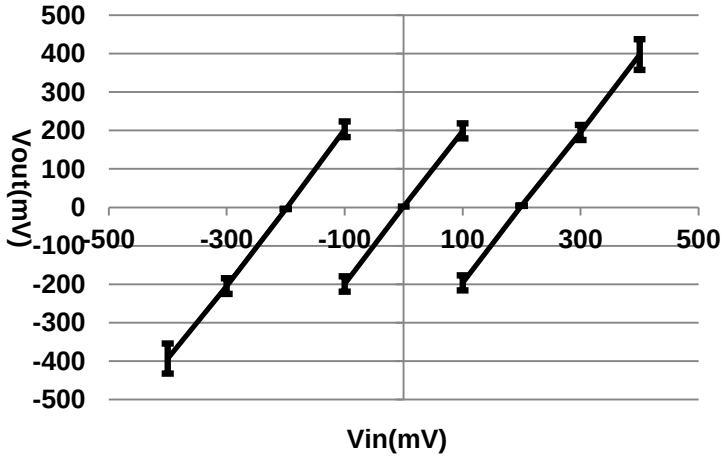


Figure 4.22 1.5 bit MDAC transfer function

The measured 1.5 bit MDAC transfer function is shown in Figure 4.22 with measured results in Table 4.5.

Table 4.5 1.5 bit MDAC transfer function

Input	Transfer Function
Vin>1/4Vref	Vout=1.97*Vin-393mV
1/4Vref >Vin>-1/4Vref	Vout=1.99*Vin+0.5mV
-1/4Vref >Vin	Vout=1.99*Vin +398mV

The input-referred noise spectrum of the 1.5 bit MDAC is measured in an identical manner as the 2.5 bit MDAC and shown in Figure 4.23 resulting in an input referred noise of 163μV.

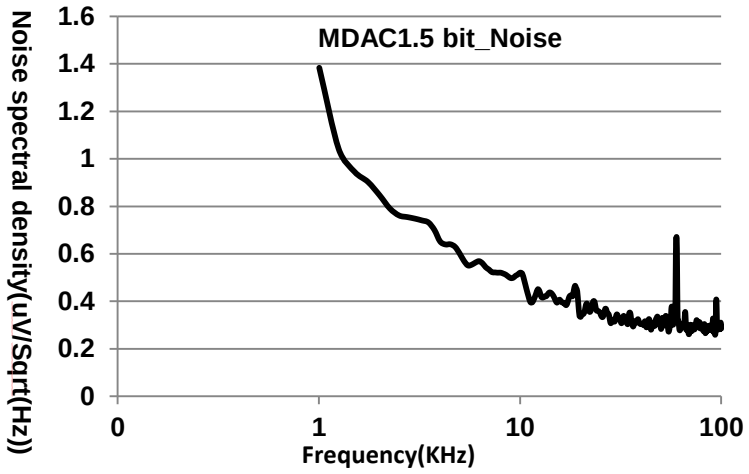


Figure 4.23 Measured noise of 1.5 bit MDAC

The 1.5 bit MDAC error sources are shown in Table 4.6 and capacitor matching to 7.4 bits is given by the PDK model.

Table 4.6 1.5 bit MDAC errors

MDAC Errors	**Measurement (Number of Bits)**
Gain error	8.4
Settling error	7.5
Slewing rate limited	No Slewing problem
MDAC noise	10.5
Capacitor Mismatch	7.4

Table 4.7 Performance comparisons with existing neural interface

Work	**Year**	**Supply Voltage (V)**	**Midband Gain (dB)**	**Bandwidth (kHz)**	**Input Referred Noise (μVrms)**	**NEF (Noise Effective Factor)**	**Total Power (μW)**
Harrison [14]	2009	3.3	60	5	4.8	4.8	80
M.Chae [21]	2008	±1.65	40	20	4.9	5.0	46.9
Walker [25]	2011	1.2	40	10	2.2	6.5	43
Azin [26]	2011	1.5	51.9-65.6	12	3.12	4.5	26.9
Zhiming [27]	2010	0.8	49	6.2	14	7.1	20
F.Shahrokhi [28]	2010	3	73	5	6.08	5.0	15.52
This work	2013	0.7	58.4	8	20.7	4.8	5.47

Table 4.7 shows the comparisons of the performance of our work with other groups. From the table, it is shown that our design utilizing optimal stage design of neural amplifier for minimizing power and area, choosing power efficient OTA/Opamps topologies, selecting Pipelined ADC to

digitize the amplified neural signal has the lowest power consumption of 5.47μW with 2.8X improvement over the current state-of-the-art [28].

4.3 Conclusion

This chapter summarized the measurements results of two stage neural amplifier and Pipelined ADC with the most significant blocks 2.5 and 1.5 bit MDAC. The saline solution and real animal measurement are realized to record the neural data to verify the function of neural amplifier. Measurement results of MDACs proved the function of ADC performance.

CHAPTER V

CONCLUSIONS

This chapter consists of two main sections: summary and future work. Section 5.1 summarizes the architecture and design of low power, low noise neural recording system. Section 5.2 introduces the extension of this work.

5.1 Summary

This research discusses the challenges, design and implementation of a low power and low noise neural recording system. The work mainly involves two essential building blocks: neural amplifier and Pipelined ADC. The methodological design and chip implementation are presented. The real animal experiment is realized to study the suitability of biomedical applications.

The neural amplifier requires low power and low noise operation for chronic recording of real animals' neural signals. The transistors working in subthreshold region consumes much lower current and provides better transconductance efficiency. The performances of OTAs in subthreshold application and FOM comparisons are summarized. The optimized number of amplifier stages demonstrates the minimum power and area consumption; noise analysis of 1st OTA ensures the low input referred noise of neural amplifier.

A low power low voltage 8 bit Pipelined ADC design is presented. The advantage of power consumption of Pipelined ADC over SAR ADC and Delta-Sigma ADC is discussed. 2.5 bit and 1.5 bit MDAC are selected to achieve enough resolution for neural recording with low power

consumption. The MDAC utilizes a novel drift differential voltage cancellation technique robust to device leakage to reduce the input drift voltage.

The performance of all proposed building blocks is verified through test chips fabricated in IBM 180nm CMOS process. Both bench-top and real animal test results demonstrate the system's capability of recording neural signals for neural spike detection. The prototype circuit shows the feasibility of including itself to a future implantable neural recording interface for use in a RFID system.

5.2 Future work

For the extension of this PhD work, it would be interesting to complete the whole RFID neural recording interface. To accomplish this, there are more challenges besides the recording-channel development. The future work could include but not limit to 1) a 4x or 8x bandpass amplifiers shorting together to achieve lower noise floor; 2) calibration circuit helps improving the performance of Pipelined ADC; 3) the immunity of front-end circuit to stimulation induced artifacts.

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